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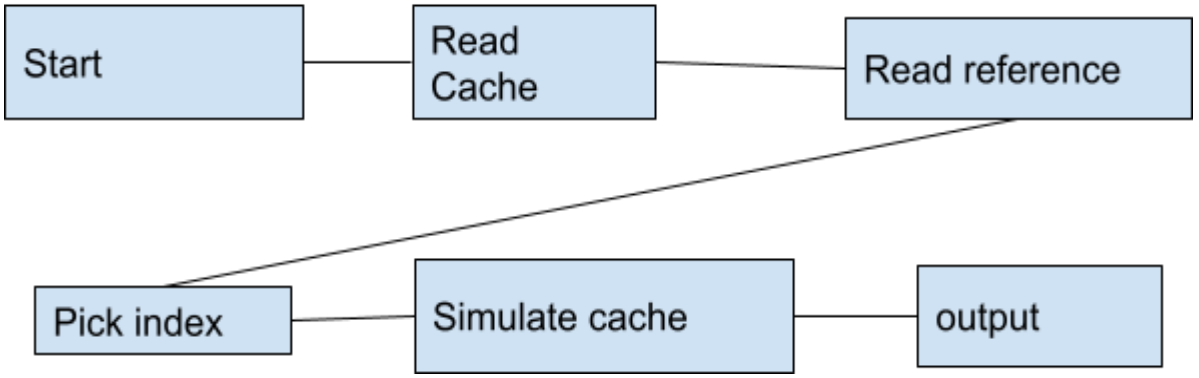
The cache behavior simulation

Flow chart



Lru

INPUT

- After getting the input we can get the offset and index length by
    - B_offset = log2(block_size);
    - index_length = log2(cache_sets);
- We will also create the cache organization using cache set and associativity

Pick index

- In an address it will be |tag|index|offset so the tag will be after the offset for index length
- I use the vector “emplace_back” the new element is added to the end.
    - reverse so print from MSB to LSB

Simulate cache

- For each tag I have an int last to keep track of the last use
- Loop through every address
- First get the tag
- check whether set is not full or tag already existed
    - If not add the cache in
    - If tag already exist the output[i] is a hit
- If cache is miss
    - Replace the (last) with associativity - 1
- update the last by adding 1 to them

OPT index

- Choose an index, from len, len = addr_bits - B_offset

Quality Measures

- vector<int> Z(len); // z == 0
- vector<int> O(len); // O == 1
- vector<double> Q(len); // Quality Measures min(Zi, Oi)/max(Zi, Oi)

Correlations

```
vector<vector<int>> E(len, vector<int>(len)); // E = identical value
vector<vector<int>> D(len, vector<int>(len)); // D = different value
vector<vector<double>> C(len, vector<double>(len));
```

Picking

Pick the best Quality measure then for the next one Select Q[j] * Correlations