Check for updates

IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

Voltage-mode robust controller design for DC–DC boost converter at the presence of wide load and input voltage variations based on finite-state-machine model

ISSN 1755-4535
Received on 7th March 2017
Revised 23rd November 2017
Accepted on 25th December 2017
E-First on 21st February 2018
doi: 10.1049/iet-pel.2017.0136
www.ietdl.org

Seyedeh-Nafiseh Mirebrahimi[1], *Farshad Merrikh-Bayat*[1], *Asghar Taheri*[1] ✉
[1]*Department of Electrical and Computer Engineering, University of Zanjan, Zanjan, Iran*
✉ *E-mail: taheri@znu.ac.ir*

Abstract: In this study, first, a new definition is proposed for the state of the boost converter. In this approach, the state is defined based on the relative value of two successive samples of the output voltage with respect to the reference voltage. Then a finite-state-machine (FSM) model, which takes into account the possible variations of the input voltage and load resistance, is proposed. This model is discrete-time and represents the evolution of states implicitly based on the events like load and input voltage variation. One advantage of this model is that it is valid both in continuous conduction mode and discontinuous conduction mode. At the next step, a voltage-mode controller, which can regulate the output voltage at the presence of load and input voltage variations, is proposed. Stability of the resulting closed-loop system is studied using the FSM model and the discrete-time Lyapunov method. Simulations and experimental results are presented.

1 Introduction

So far various methods have been proposed by researchers for modelling and control of DC–DC converters. In the field of modelling, the averaging method [1] is widely used in practise. Two other well-known methodologies are piecewise affine [2–4] and mixed logical dynamical (MLD) [5, 6] modelling which unlike the averaging method are of hybrid nature. A wide variety of methods are also used to control these converters. For example, adaptive control [7], model predictive control (MPC) [8], adaptive fuzzy logic [9], linear optimal feedback and non-linear feed-forward control [10] and sliding mode control (SMC) [11–13] can be found in the literature.

The methods available for controlling DC–DC converters do not have the same popularity. Among others, SMC is one of the methods widely used in practice. One big advantage of this control strategy is that it takes into account the uncertainties of a model for controller design. However, it has the disadvantage of needing all states of the converter, e.g. the inductor current and capacitor voltage in dealing with a boost converter, for calculating the control. Of course, instead of using a current sensor one may use an observer to estimate the inductor current [14]. This approach considerably increases the complexity of design and it may even happen that one cannot calculate the stabilising switching law due to this complexity.

Hybrid modelling and control methods have also attracted many attentions [15–18]. Especially, MLD provides us with an effective tool for modelling a wide variety of DC–DC converters. Unfortunately, in practise, it is often difficult to employ it because of the high computational effort needed for computing the control. More precisely, it is common practice to control the system modelled by MLD by MPC [5], which numerically solves an optimisation problem at each time sample. However, in dealing with a DC–DC converter we have a very limited time to update the control which is often much shorter than the time needed to solve such an optimisation problem by trivial processors. The other advantage of MLD is that it generates a model which is valid for both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) operations [19]; however, the robustness is not considered in the formulation of the problem.

The main reason for the difficulty of designing a controller of any type for a DC–DC boost converter is that even its average model is non-linear both in CCM and DCM operations. Saturation of duty cycle adds another non-linearity to equations. Uncertainty and/or time-variation of load resistance and/or input voltage makes the control problem much more complicated and linear controllers like proportional–integral–derivative (PID) usually lead to very poor results in such cases. For example, Fig. 1 shows the results of a simulation where the proportional–integral (PI) controller $C(s) = 0.01 + 2/s$ is used to pulse width modulation (PWM) control of a standard boost converter with $L = 220\,\mu$H, $C = 500\,\mu$F and $R = 100\,\Omega$ (the input voltage and the frequency of PWM are equal to 12 V and 50 kHz, respectively). As it is observed in this figure, for $0 < t < 0.15$ s the output voltage tracks the reference but in the time interval $0.15 < t < 0.35$ s, the system suddenly becomes unstable and although the amplitude of reference voltage for $0.35 < t < 0.5$ s is the same as $0 < t < 0.15$ s the system cannot track it. This failure is not limited to PIDs and any controller with integrator may lead to a similar result under certain circumstances (recall that application of an integrator is mandatory for tracking the step command without steady-state error).

To explain the reason, consider the dome-like static $d - V$ curve of a practical boost converter as shown in Fig. 2 where d and V_o stand for the duty cycle and the corresponding output voltage at steady state, respectively. In this figure, the maximum achievable voltage at steady state and the corresponding duty cycle are shown by V^* and d^*, respectively. Now consider the problem of regulating the output voltage using, e.g. a classical PI in the standard feedback connection. First, consider the case where the reference voltage, V_{ref}, is constant and larger than V^* as shown in Fig. 2*a*, and assume that the duty cycle is initially smaller than d^* (initial values of duty cycle and output voltage are denoted as d_{init} and V_{init}, respectively). In this case, assuming that the gain of integrator is positive, the controller begins increasing the duty cycle. According to Fig. 2*a* this increasing of duty cycle initially leads to increasing the output voltage as it is desired. However, as soon as the duty cycle reaches d^* the integrator still tries to decrease the tracking error by increasing the duty cycle which in contrary increases the tracking error. In this situation, the output voltage becomes unstable and finally reaches the value corresponds to $d = 1$, which is close to zero. It is important to note that in the problems with uncertain load, the maximum achievable voltage, V^*, is not fixed and strictly depends on the load resistance such that larger resistance results in a larger V^*. Hence, with an integrator in the loop, the closed-loop

© The Institution of Engineering and Technology 2018

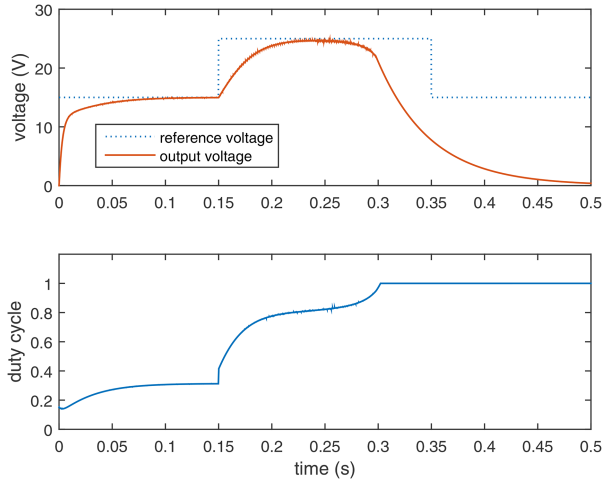

Fig. 1 *Failure of a PI controller for output voltage regulation of a boost converter*

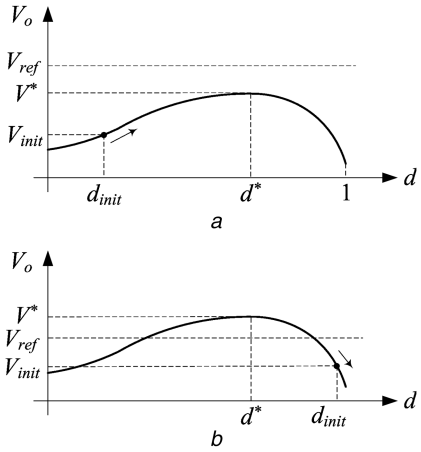

Fig. 2 *Static $d-V$ curve of a practical boost converter*
(a) Operating point is in the left hand side of d^*, ***(b)*** Operating point is in the right hand side of d^*. The arrow near operating point shows the direction of movement when the gain of the integrator of controller is positive

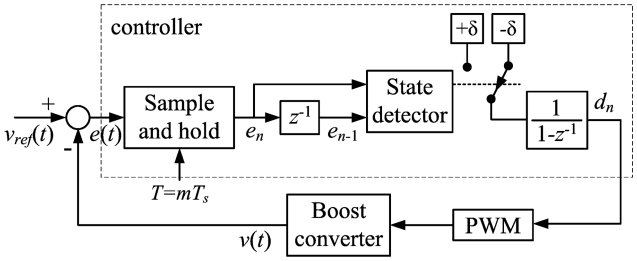

Fig. 3 *Block diagram of the proposed control method*

system can become unstable by changing the load or reference or input voltage. Even when the reference voltage is reachable, a sudden change in the parameters of the converter can cause the case $d^* < d_{\text{init}}$ which can destabilise the system when the gain of integrator is positive (see Fig. 2*b*).

According to the above discussion, in order to stabilise the closed-loop system, the gain of integrator must automatically change sign during the ordinary work of controller such that a positive gain is applied when $d < d^*$ and vice versa, where d^* is uncertain and time-varying. The controller proposed for this purpose in this paper is actually a discrete-time integrator whose gain's sign is automatically adjusted in this manner. This controller works based on the output voltage feedback and is robust to load and input voltage variations. It is especially useful when the input voltage and/or load resistance vary slowly in time (e.g. considering a regenerative braking or a solar cell as the input voltage source and electroplating or battery charging as load). Analysis and design of this controller are based on the finite-state-machine (FSM) model proposed in this paper. Although not discussed in this paper, the proposed FSM model and the controller can also be applied to other DC–DC converters. Very recently, some applications of FSM for modelling and control of DC–DC converters have been reported in the literature [20, 21]. This paper and the authors of [20, 21] provide two intrinsically different definitions for the *states* of converter, which are crucial to constructing an FSM model. It concludes that the models, methods, and results of this paper are completely different with [20, 21].

2 Main results

Fig. 3 shows the block diagram of the proposed control method. In this figure, the *sample and hold* box takes a sample of error signal denoted as e_n. Then the current and past sample of error signal enters the box named *state detector*. The function of this box is detecting the *state* of converter, which will be defined in Section 2.1. In brief, the state of converter determines whether the duty cycle must be increased or decreased at the next time sample in order to decrease the absolute value of tracking error. Hence, the state detector puts either $+\delta$ or $-\delta$ at the input of discrete-time integrator to increase or decrease the duty cycle to this amount at the next time sample, where $\delta > 0$ is a small constant number.

In the following discussions the frequency of PWM is assumed to be constant and the frequency of A/D converter, which is not shown in Fig. 3, is considered equal to $f_s = 1/T_s$. The sampling period of all discrete-time systems is considered equal to $T = mT_s$, where m is a positive integer typically in the range of tens or hundreds (in fact, the A/D takes samples of error signal with a frequency f_s and the *sample and hold* box downsamples the resulted data with a factor m). In the remaining of this paper, whenever we talk about the *sampling period*, the sampling period of the controller, T, is meant unless it is mentioned explicitly. The seminal assumption of this paper is that the value of T is considered sufficiently large such that the transient response of converter to a small step change equal to $\pm\delta$ in duty cycle settles down in at most T seconds under any circumstances. Note that the duty cycle of PWM is updated every T second. In the following, we will study the controller of Fig. 3 with more details.

2.1 FSM model of the boost converter

The proposed controller updates the duty cycle every T second according to the *state* of converter which is defined based on the relative value of two successive samples of the output voltage (or tracking error) with respect to the reference voltage. For a mathematical definition of states let v_{n-1}, v_n, and v_{n+1} stand for the samples of the output voltage of converter at time instances $(n-1)T$, nT, and $(n+1)T$, respectively, i.e. $v_k = v(kT)$, where $v(t)$ is the output voltage. Similarly, denote the samples of tracking error at time instances $(n-1)T$, nT, and $(n+1)T$ as e_{n-1}, e_n, and e_{n+1}, respectively, i.e.

$$e_k = v_{\text{ref}}(kT) - v(kT), \tag{1}$$

where $v_{\text{ref}}(t)$ is the reference voltage. In order to address the state of converter in terms of successive samples of tracking error first notice that as it is shown in Fig. 4, e_{n-1}, e_n, and 0 can be arranged only in six different ways with respect to each other; each one is considered as a *state* of converter. For example, Figs. 4*a* and *b* show the states $S_1: 0 < e_n < e_{n-1}$ and $S_2: e_n < 0 < e_{n-1}$, respectively (for the sake of simplicity, the equality condition is not considered in the definition of states). In Fig. 4, the samples of output voltage are shown by small black circles connected to each other by a black solid line. These lines are plotted only to clearly show the slope of changes in the samples of the output voltage and does not indicate the real value of output voltage between two samples. Note also that as it is shown in Fig. 4 the value of v_{ref} can be changed between the two successive samples of the output voltage and the states are defined only based on the *relative* values of

© The Institution of Engineering and Technology 2018

17554543, 2018, 5, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/iet-pel.2017.0136 by Readcube (Labtiva Inc.), Wiley Online Library on [14/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

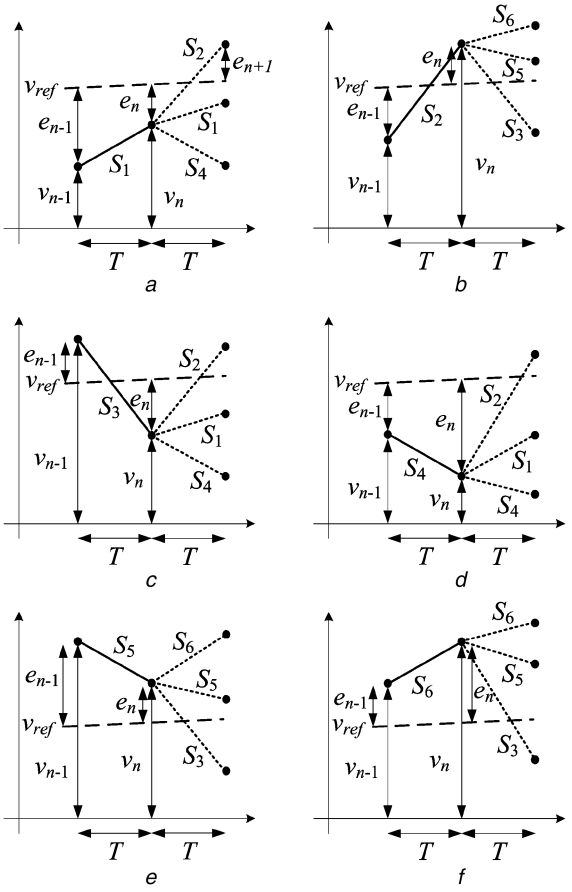

Fig. 4 *Current and the next possible states. For example, in (f) the current state is S_6 and the next possible states are S_3, S_5, and S_6*
(a) current state is S_1, ***(b)*** current state is S_2, ***(c)*** *current state is S_3,* ***(d)*** *current state is S_4,* ***(e)*** *current state is S_5,* ***(f)*** current state is S_6

samples and the reference voltage. Hence, according to Fig. 4 the ith state denoted as S_i ($i = 1, \ldots, 6$) is defined as the following:

$$S_1\colon\ 0 < e_n < e_{n-1}, \tag{2}$$

$$S_2\colon\ e_n < 0 < e_{n-1}, \tag{3}$$

$$S_3\colon\ e_{n-1} < 0 < e_n, \tag{4}$$

$$S_4\colon\ 0 < e_{n-1} < e_n, \tag{5}$$

$$S_5\colon\ e_{n-1} < e_n < 0, \tag{6}$$

$$S_6\colon\ e_n < e_{n-1} < 0. \tag{7}$$

Now, assuming that the current state of converter is any of the six states mentioned above, it can move only to three certain states at the next step as shown in Fig. 4. For example, as it can be observed in Fig. 4*a*, assuming that the current state of converter is S_1, the next state is S_2 if $e_{n+1} < 0 < e_n$, is S_1 if $0 < e_{n+1} < e_n$, and is S_4 if $0 < e_n < e_{n+1}$. In fact, in order to determine the next possible states of converter in Fig. 4*a* we note that the new sample of the output voltage can be either larger than both the previous sample and reference, or larger than only the previous sample, or smaller than the previous sample, but clearly, no other situation can be imagined. The same discussion goes on the other states plotted in Fig. 4.

The condition under which the converter moves from a certain state at the current step to a certain state at the next step is called the *trigger condition*. In this paper, the trigger conditions are expressed based on the states of converter. To be more precise, consider again Fig. 4*a*. According to this figure when the current state of converter is S_1, the next state is S_2 if $e_{n+1} < 0 < e_n$, is S_1 if $0 < e_{n+1} < e_n$, and is S_4 if $0 < e_n < e_{n+1}$. In this example, the inequality conditions $e_{n+1} < 0 < e_n$, $0 < e_{n+1} < e_n$, and $0 < e_n < e_{n+1}$ which can be used to determine the next state of converter serve as the trigger conditions. Clearly, in practice when the current state is S_1 only one of the three trigger conditions mentioned above can be satisfied and consequently the converter can move only to one of the states S_1, S_2, or S_4 in the next step.

To sum up, e_n, e_{n+1}, and 0 can be arranged in six different ways as follows to form the trigger conditions denoted as c_i ($i = 1, \ldots, 6$):

$$c_1\colon\ 0 < e_{n+1} < e_n, \tag{8}$$

$$c_2\colon\ e_{n+1} < 0 < e_n, \tag{9}$$

$$c_3\colon\ e_n < 0 < e_{n+1}, \tag{10}$$

$$c_4\colon\ 0 < e_n < e_{n+1}, \tag{11}$$

$$c_5\colon\ e_n < e_{n+1} < 0, \tag{12}$$

$$c_6\colon\ e_{n+1} < e_n < 0. \tag{13}$$

The relation between the current state, next state, and the corresponding trigger conditions can be depicted using an FSM model as shown in Fig. 5*a*. One important property of this FSM model is that it is valid for any controller and at the presence of load and input voltage variations.

2.2 Proposed controller

In order to design the details of the controller in Fig. 3 let us denote the duty cycle of PWM at time instances $(n-1)T$ and nT as d_{n-1} and d_n, respectively, where $d_n = d_{n-1} + \Delta d_n$ and Δd_n is the (small) change in duty cycle at the time instance nT. Moreover, assume that the value assigned to T is sufficiently large such that the converter response to a step change equal to Δd_n in duty cycle settles down in at most T seconds for all values of parameters which are in the range. To proceed, consider Fig. 4*a* and assume that the load resistance and input voltage are constant. In this figure, the tracking error at the time instance $(n-1)T$ is equal to e_{n-1}. At this moment the controller adds Δd_{n-1} to the duty cycle, which leads to the smaller error e_n at the next time sample. Considering the fact that v_n is still smaller than v_{ref}, the best control strategy at the time instance nT is to change the value of duty cycle in the same direction as the previous sample, i.e. to set $\Delta d_n = \Delta d_{n-1}$, hoping that this decision again leads to increasing the output voltage at the next sample.

Now consider Fig. 4*b*. In this figure, applying a change equal to Δd_{n-1} to duty cycle at the time instance $(n-1)T$ has changed the output voltage from v_{n-1}, which is smaller than the reference voltage, to v_n, which is larger than it. In this figure setting $\Delta d_n = \Delta d_{n-1}$ is a wrong decision since it will lead to increasing the absolute value of tracking error at the next time sample (state S_6 in Fig. 4*b*) which is not desired. Hence, the best control strategy when the current state of the converter is S_2 is to set $\Delta d_n = -\Delta d_{n-1}$ to make the next state of converter equal to S_3 (assuming that all parameters of the converter are fixed). The best control strategy when the current state of converter is one of the remaining four states in Fig. 4 can be deduced similarly. In general, Δd_n can have either the same or the opposite sign as Δd_{n-1}. In order to determine the correct sign we assume that the output voltage will continue changing in the same direction as the previous sample if Δd_n has the same sign as Δd_{n-1}, and vice versa. Hence, using this intuitive rule, the best control strategy at the time instance nT is to set $\Delta d_n = \Delta d_{n-1}$ if changing the output voltage in the current direction decreases the absolute value of tracking error, and $\Delta d_n = -\Delta d_{n-1}$ otherwise. Table 1 summarises the proposed control strategy.

Fig. 6*a* shows a method for implementing the proposed controller based on the IF–THEN rules of Table 1. In this figure, the sampling period of all transfer functions in z is equal to

© The Institution of Engineering and Technology 2018

17554543, 2018, 5, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/iet-pel.2017.0136 by Readcube (Labtiva Inc.), Wiley Online Library on [14/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

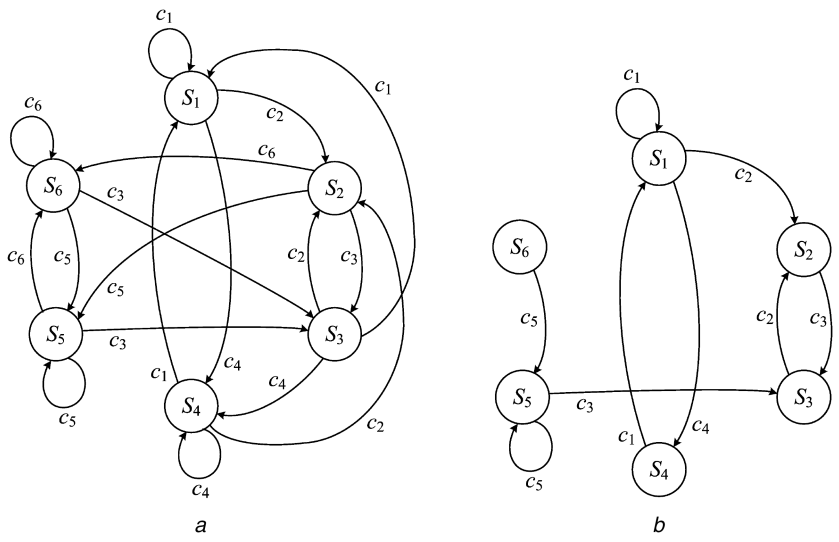

Fig. 5 *Changes in the state of converter*
(a) FSM model of the boost converter which takes into account the possibility of load, input voltage, and reference voltage variations, ***(b)*** FSM model of the boost converter right after fixing all of its parameters

Table 1 IF–THEN rules governing the proposed controller

IF the current state is	THEN $\Delta d_n =$
S_1	Δd_{n-1}
S_2	$-\Delta d_{n-1}$
S_3	$-\Delta d_{n-1}$
S_4	$-\Delta d_{n-1}$
S_5	Δd_{n-1}
S_6	$-\Delta d_{n-1}$

$T = mT_s$. The boxes with '>' and '<' operators compared the two inputs and return the Logical 1 (or 0) at the output if the result of the comparison is logically true (or false). In Fig. 6*a*, first a sample-and-hold, shown by S/H box, takes the samples of tracking error, $e(t)$, with the sampling period T and generates e_n. Then this sample passes through the unit delay box to generate e_{n-1}. Now the state of converter can be determined by comparing e_n and e_{n-1} (see (2)–(7)). It can be easily verified that the output of the AND gate denoted as G_1 (or G_2) in Fig. 6*a* is equal to Logical 1 if and only if the state of converter is S_1 (or S_5). Hence, the output of OR gate is equal to Logical 1 if and only if the state of converter is either S_1 or S_5, and it is equal to the Logical 0 otherwise. The output of the box named *Conditional switch* is equal to its upper input if the middle input is greater than 0.5, which happens only when the output of OR gate is 1, or equivalently, the state of converter is either S_1 or S_5. Hence, at the output of *Conditional switch* we have $\Delta d_n = \Delta d_{n-1}$ if the state of converter is S_1 or S_5, and $\Delta d_n = -\Delta d_{n-1}$ otherwise. Considering the fact that the initial condition of the unit delay box connected to the *Conditional switch* is equal to δ ($\delta > 0$), the input of integrator in Fig. 6*a* is changed with steps $\pm\delta$ (i.e. $|\Delta d_n| = |\Delta d_{n-1}| = \delta$). Assigning smaller (positive) values to δ leads to smaller fluctuations of the output voltage at steady state at the cost of a larger rise time.

In Fig. 6*a*, the amplitude of the changes applied to duty cycle is constant regardless of the tracking error (i.e. $\Delta d_n = \delta$ for all n). The problem with this approach is that as soon as the output voltage reaches the reference and the converter oscillates between S_2 and S_3, the output voltage may contain undesired large ripples. This problem can be solved by considering Δd_n proportional to the amplitude of tracking error. In this manner, the controller applies smaller changes to duty cycle when the output voltage is close to reference and vice versa. The modified controller as shown in Fig. 6*b* is designed for this purpose and elaborated in the following.

In Fig. 6*b*, sat(.) is the saturation function defined as follows:

$$\text{sat}(x) \triangleq \begin{cases} \varepsilon_1, & |x| < \varepsilon_1 \\ x, & \varepsilon_1 \le |x| \le \varepsilon_2, \\ \varepsilon_2, & \varepsilon_2 < |x| \end{cases} \tag{14}$$

where ε_1 and ε_2 are positive real constants such that $0 < \varepsilon_1 < \varepsilon_2$. This function avoids applying very large or very small changes to duty cycle since the first one leads to large oscillations of the output voltage at steady-state and the second one leads to very slow convergence of output voltage specially when the tracking error is small. The multiplier M_1 in Fig. 6*b* has two inputs: the right input determines the sign of changes applied to duty cycle and the left (positive) input determines its amplitude. When the state of converter is either S_1 or S_5 the output of OR gate is Logical 1 which concludes that

$$\Delta d_n = \text{sgn}(\Delta d_{n-1}) \times \text{sat}(|e_n|) \times \delta\,. \tag{15}$$

According to (15) at the current sample, the duty cycle is changed in the same direction as the previous sample and the amplitude of this change is equal to δ ($\delta > 0$) scaled by the factor $\text{sat}(|e_n|)$. Hence, when the amplitude of tracking error is mediocre, we have $\text{sat}(|e_n|) = |e_n|$ and (15) yields

$$\Delta d_n = \text{sgn}(\Delta d_{n-1}) \times |e_n| \times \delta, \tag{16}$$

which means that the amplitude of changes in duty cycle is proportional to the tracking error. Similarly, when the tracking error is sufficiently large (or small) amplitude of changes in duty cycle is limited to $\Delta d_n = \text{sgn}(\Delta d_{n-1}) \times \varepsilon_2 \times \delta$ (or $\Delta d_n = \text{sgn}(\Delta d_{n-1}) \times \varepsilon_1 \times \delta$).

On the other hand, when the state of converter is neither S_1 nor S_5 the output of OR gate is Logical 0 which concludes that

$$\Delta d_n = -\alpha \times \text{sgn}(\Delta d_{n-1}) \times \text{sat}(|e_n|) \times \delta\,. \tag{17}$$

In this case, assuming $\alpha > 0$ the sign of Δd_n is the negative of the sign of Δd_{n-1}, which is desired according to Table 1. Using α makes it possible to adjust the rate of changing Δd_n in the same and opposite direction of Δd_{n-1} independently.

2.3 Stability analysis and tracking properties of the closed-loop system

As long as the load resistance and/or input voltage and/or reference voltage are varying with time, the state of converter is evolved as shown in Fig. 5*a*. However, as soon as all of these parameters are fixed, the output voltage first exhibits a transient response wherein

© The Institution of Engineering and Technology 2018

17554543, 2018, 5, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/iet-pel.2017.0136 by Readcube (Labtiva Inc.), Wiley Online Library on [14/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

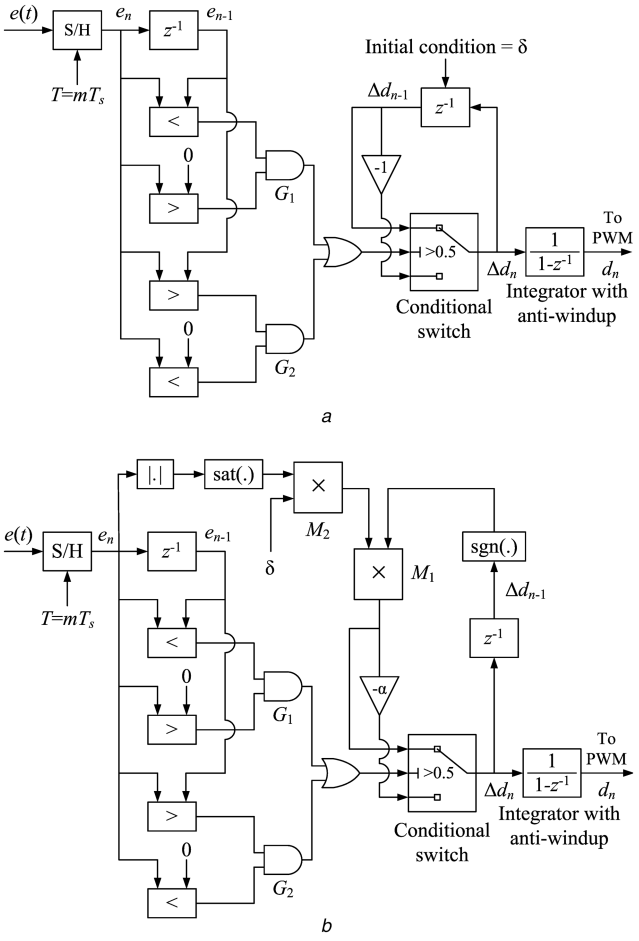

Fig. 6 *Proposed designs for controller in Fig. 3*
(a) Duty cycle is changed with fixed steps, ***(b)*** Duty cycle is changed proportionally to the tracking error

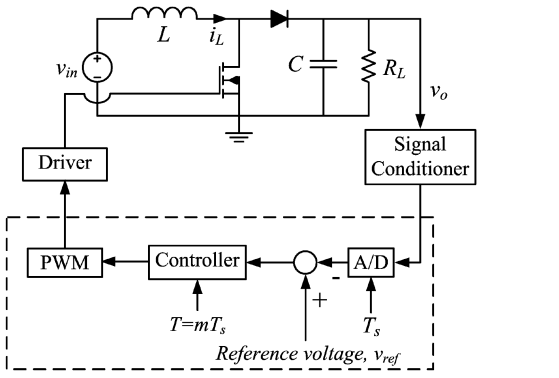

Fig. 7 *DC–DC boost converter and the proposed controller*

the converter moves repeatedly from one state to another. After this transition, the system exhibits a stable oscillation either between S_2 and S_3, which corresponds to tracking the reference voltage when it is reachable, or S_1 and S_4, which occurs when the reference voltage is too high and not reachable. For example, suppose that the state of converter when all parameters are fixed is S_6. According to Table 1, in this case, the controller changes the duty cycle in the opposite direction of the previous sample which causes the output voltage of converter changes in the opposite direction as well, and consequently, the state moves from S_6 to S_5 (it means that in Fig. 5*a* the trigger condition c_6 is not satisfied in this case). It leads to the following sequence of state evolutions:

$$S_6 \to S_5 \to \cdots \to S_5 \to S_3 \to S_2 \to S_3 \cdots \tag{18}$$

Hence, in this case, the output voltage eventually tracks the reference voltage by generating stable oscillations between S_2 and S_3. When the state of converter is anything other than S_6, the FSM model of Fig. 5*a* can be simplified in a similar manner which leads to the simplified FSM model of Fig. 5*b*. This FSM model shows the evolution of states during transient response right after fixing all parameters of the converter. In this figure, it can be verified that assuming any initial state, finally, the converter oscillates between either S_2 and S_3 or S_1 and S_4.

In the following, we mathematically prove the stability of the closed-loop system. For the sake of simplicity and without a considerable loss of generality, the proof is presented assuming the ideal model of the boost converter, i.e. by neglecting the parasitic elements. Moreover, the frequency of PWM is considered infinitely large. To prove the stability first we derive the discrete-time model of the closed-loop system and then by using the Lyapunov stability theorem we show that once all parameters of the converter are fixed, it has only one equilibrium point which is globally stable. The closed-loop system of Fig. 3 totally has four states; two of them (inductor current and capacitor voltage) belong to the converter and are continuous in nature, and two others (the output of z^{-1} and $1/(1-z^{-1})$ boxes in Fig. 6*a*) belong to the controller and are discrete-time. Considering the fact that the sampling period of discrete-time states is large enough such that the continuous-time states are settled down after one sampling period, the closed-loop system can be modelled using discrete-time equations as described below.

The state-space equation of the ideal boost converter (as shown in Fig. 7) is as follows (for the sake of simplicity in notation, i_L and v_o are dented as i and v, respectively)

$$\begin{bmatrix} L\dot{i}(t) \\ C\dot{v}(t) \end{bmatrix} = \begin{bmatrix} 0 & -1+d(t) \\ 1-d(t) & -\dfrac{1}{R_{\mathrm{L}}} \end{bmatrix} \begin{bmatrix} i(t) \\ v(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} v_{\mathrm{in}}(t). \tag{19}$$

At the nth sampling period, the controller sets the duty cycle equal to d_n. The voltage of capacitor and the current of inductor vary in response to this change in duty cycle. Assuming that the sampling period is large enough and $v_{\mathrm{in}}(t)$ and $v_{\mathrm{ref}}(t)$ are constant ($v_{\mathrm{in}}(t) = v_{\mathrm{in}}$ and $v_{\mathrm{ref}}(t) = v_{\mathrm{ref}}$), the capacitor voltage and inductor current at the end of this sampling period (denoted as v_{n+1} and i_{n+1}, respectively) can be calculated from (19) as follows:

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & -1+d_n \\ 1-d_n & -\dfrac{1}{R_{\mathrm{L}}} \end{bmatrix} \begin{bmatrix} i_{n+1} \\ v_{n+1} \end{bmatrix} + \begin{bmatrix} v_{\mathrm{in}} \\ 0 \end{bmatrix}. \tag{20}$$

Note that we put the derivatives in (19) equal to zero to arrive at (20) because it was assumed that the voltage and current are settled down after one sampling period. Solving (20) with respect to i_{n+1} and v_{n+1} yields

$$i_{n+1} = \frac{v_{\mathrm{in}}}{R_{\mathrm{L}}(1-d_n)^2} \triangleq f_i(d_n), \tag{21}$$

$$v_{n+1} = \frac{v_{\mathrm{in}}}{1-d_n} \triangleq f_v(d_n). \tag{22}$$

The third state of the closed-loop system is d_n at the output of integrator in Fig. 6*a* which is updated as

$$d_{n+1} = d_n + s(v_n, v_{n+1})\Delta d_n, \tag{23}$$

where

© The Institution of Engineering and Technology 2018

17554543, 2018, 5, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/iet-pel.2017.0136 by Readcube (Labtiva Inc.), Wiley Online Library on [14/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

$$s(v_n, v_{n+1}) =$$

$$\begin{cases} -1, & S_2\colon\ v_n < v_{\text{ref}} < v_{n+1} \text{or} S_3\colon\ v_{n+1} < v_{\text{ref}} < v_n \text{or} \\ & S_4\colon\ v_{n+1} < v_n < v_{\text{ref}} \text{or} S_6\colon\ v_{\text{ref}} < v_n < v_{n+1} \\ +1, & S_1\colon\ v_n < v_{n+1} < v_{\text{ref}} \text{or} S_5\colon\ v_{\text{ref}} < v_{n+1} < v_n \end{cases} \tag{24}$$

(For the sake of simplicity, we used the variable v_{n+1} in the right hand side of (23), which is not standard in state-space representation since the subscript of all variables in the right hand side of equations should be n. This problem can be solved by representing v_{n+1} in terms of d_n using (22). Note also that $|\Delta d_n| = \delta$ in (23).) Finally, the fourth state is e_n which is updated as follows:

$$e_{n+1} = v_{\text{ref}} - v_{n+1} = v_{\text{ref}} - \frac{v_{\text{in}}}{1 - d_n}. \tag{25}$$

Equations (21)–(25) constitute the (non-linear) discrete-time state-space equations of the closed-loop system when the load resistance and input voltage are fixed. This system has one equilibrium point at $x^* = (i^*, v^*, d^*, e^*)$. In order to determine this point, we assume that at steady state the duty cycle oscillates between $d^* + \delta/2$ and $d^* - \delta/2$; i.e. the equilibrium value of duty cycle is defined as the average of the repeated values it takes at steady state (the same method is used to define the equilibrium value of other variables). Trivial calculations conclude that in response to these *symmetric* oscillations of duty cycle around d^*, the other states also exhibit symmetric variations around i^*, v^*, and e^* as given below:

$$v^* = \frac{(1 - d^*)v_{\text{in}}}{(1 - d^*)^2 - \delta^2/4}, \quad i^* = \frac{v_{\text{in}}[(1 - d^*)^2 + \delta^2/4]}{R_{\text{L}}[(1 - d^*)^2 - \delta^2/4]^2}, \quad e^* = v_{\text{ref}} - v^*. \tag{26}$$

Notice that in (26) for $\delta \to 0$ we have $v^* = v_{\text{in}}/(1 - d^*)$. Hence, assuming that the value of δ is sufficiently small, we have $v^* = v_{\text{ref}}$ and the value of d^* can be calculated from $v_{\text{in}}/(1 - d^*) = v_{\text{ref}}$. It concludes that by proving the global stability of x^*, we have actually proved that the output voltage of converter converges to $v^* = v_{\text{ref}}$ regardless of the initial condition of the system.

To prove the stability of x^* defining the Lyapunov function

$$V(x_n) = \frac{R_{\text{L}}^2}{v_{\text{in}}^2}(i_n - i^*)^2 + \frac{1}{v_{\text{in}}^2}(v_n - v^*)^2 + (d_n - d^*)^2 + (e_n - e^*)^2, \tag{27}$$

where $x_n = [i_n v_n d_n e_n]$. After trivial calculations, we have

$$\Delta V(x_n) = V(x_{n+1}) - V(x_n), \tag{28}$$

$$= \left[\frac{1}{(1 - d_n)^2} - \frac{(1 - d^*)^2 + \delta^2/4}{[(1 - d^*)^2 - \delta^2/4]^2}\right]^2, \tag{29}$$

$$-\left[\frac{1}{(1 - d_{n-1})^2} - \frac{(1 - d^*)^2 + \delta^2/4}{[(1 - d^*)^2 - \delta^2/4]^2}\right]^2, \tag{30}$$

$$+\left[\frac{1}{1 - d_n} - \frac{1 - d^*}{(1 - d^*)^2 - \delta^2/4}\right]^2, \tag{31}$$

$$-\left[\frac{1}{1 - d_{n-1}} - \frac{1 - d^*}{(1 - d^*)^2 - \delta^2/4}\right]^2, \tag{32}$$

$$+[d_n + s(v_n, v_{n+1})\Delta d_n - d^*]^2 - [d_n - d^*]^2, \tag{33}$$

$$+\left[v^* - \frac{v_{\text{in}}}{1 - d_n}\right]^2 - \left[v^* - \frac{v_{\text{in}}}{1 - d_{n-1}}\right]^2. \tag{34}$$

To prove the stability of x^* we must show that $\Delta V(x_n)$ is negative semi-definite. For the sake of brevity, we only prove the negative semi-definiteness of the summation of (29) and (30). Negative semi-definiteness of other paired terms can be proved similarly. For this purpose, note that d_n, d_{n-1}, and d^* in (29) and (30) can be arranged in six different ways with respect to each other as given below:

$$\begin{aligned} &D_1\colon\ d_{n-1} < d_n < d^*, \\ &D_2\colon\ d^* - \delta/2 = d_{n-1} < d^* < d_n = d^* + \delta/2, \\ &D_3\colon\ d^* - \delta/2 = d_n < d^* < d_{n-1} = d^* + \delta/2, \\ &D_4\colon\ d_n < d_{n-1} < d^*, \\ &D_5\colon\ d^* < d_{n-1} < d_n, \\ &D_6\colon\ d^* < d_{n-1} < d_n. \end{aligned}$$

By a simple algebraic reasoning, it can be shown that the summation of (29) and (30) is negative for cases D_1 and D_5, and zero for cases D_2 and D_3. The cases D_4 and D_6 cannot occur in practise when the proposed controller is applied. To prove this, one can assume the last state of converter equal to any of the states (2)–(7) and show that neither D_4 nor D_6 can happen at the next sample. For example, assuming that the last state of converter is equal to $S_1\colon v_{n-1} < v_n < v^*$ (or equivalently, $D_1\colon d_{n-1} < d_n < d^*$) the controller sets $\Delta d_{n-1} = +\delta$, or equivalently, $d_n = d_{n-1} + \delta$ which leads to either D_1 or D_2 (but not D_4 or D_6) at the next sample. This completes the proof. Note also that since $V(x_n)$ is radially unbounded, x^* is *globally* stable.

A very similar proof can be represented when the converter works in DCM. The main difference, in this case, is that (21) and (22) must be substituted with (35) and (36), which are concluded from [18]:

$$v_{n+1} = \frac{v_{\text{in}}}{2}\left[1 + \sqrt{1 + \frac{2R_{\text{L}}d_n^2 T}{L}}\right] \triangleq f_v(d_n), \tag{35}$$

$$i_{n+1} = \frac{v_{\text{in}}}{2L}\left[Td_n^2 + \frac{L}{R_{\text{L}}}\left(1 + \sqrt{1 + \frac{2R_{\text{L}}d_n^2 T}{L}}\right)\right] \triangleq f_i(d_n). \tag{36}$$

In order to determine the equilibrium point, we assume that at steady state the duty cycle repeatedly changes between $d = d^* + \delta/2$ and $d = d^* - \delta/2$, where d^* can be calculated from the equation $f_v(d^*) = v_{\text{ref}}$ provided that δ is sufficiently small. Define

$$v^* = \frac{f_v(d^* + \delta/2) + f_v(d^* - \delta/2)}{2}, \quad i^* = \frac{f_i(d^* + \delta/2) + f_i(d^* - \delta/2)}{2}, \quad e^* = v_{\text{ref}} - v^*, \tag{37}$$

and

$$V(x_n) = (i_n - i^*)^2 + (v_n - v^*)^2 + (d_n - d^*)^2 + (e_n - e^*)^2. \tag{38}$$

Then

$$\Delta V(x_n) = V(x_{n+1}) - V(x_n), \tag{39}$$

$$= [f_i(d_n) - i^*]^2 - [f_i(d_{n-1}) - i^*]^2, \tag{40}$$

$$+[f_v(d_n) - v^*]^2 - [f_v(d_{n-1}) - v^*]^2, \tag{41}$$

$$+[d_n + s(v_n, v_{n+1})\Delta d_n - d^*]^2 - [d_n - d^*]^2, \tag{42}$$

© The Institution of Engineering and Technology 2018

17554543, 2018, 5, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/iet-pel.2017.0136 by Readcube (Labtiva Inc.), Wiley Online Library on [14/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

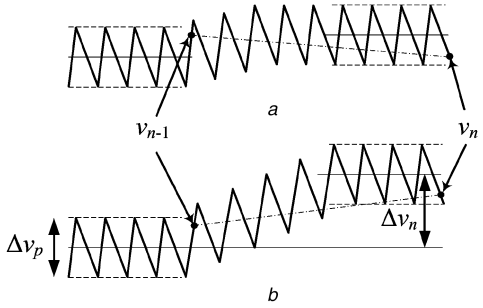

Fig. 8 *Effect of ripples in output voltage on determining the state of converter*

$$+[v^* - f_v(d_n)]^2 - [v^* - f_v(d_{n-1})]^2. \quad (43)$$

Again, we must show that $\Delta V(x_n) \leq 0$ to prove the global stability of x^*. For this purpose, it is sufficient to show that each of the terms (40)–(43) are negative semi-definite. This task can be done exactly the same as before (note that both in CCM and DCM, v_{n+1} and i_{n+1} are monotonically increasing functions of d_n). For example, by substituting $f_v(d_n)$ from (35) and v^* from (37) to (41), and considering the condition D_2: $d^* - \delta/2 = d_{n-1} < d^* < d_n = d^* + \delta/2$ it is observed that (41) is equal to zero. A similar reasoning shows that (41) is equal to zero for D_3, and negative for D_1 and D_5 (the cases D_4 and D_6 cannot occur in practice for the same reason as mentioned before). Hence, (41) is negative semi-definite. Negative semi-definiteness of other terms can be deduced similarly.

2.4 Effect of switching

In the previous discussions, the effect of switching was neglected for the sake of simplicity. The ripples in output voltage caused by switching can mislead the controller about the state of converter and result in malfunction of the closed-loop system. To be more precise, consider Fig. 8*a* which shows the ripples in a typical output voltage. In this figure, a change in duty cycle has increased the average value of output voltage but the samples were taken from it (shown by small black circles and denoted as v_{n-1} and v_n) mislead the controller about the state of converter since it wrongly feels that the output voltage has been decreased. In order to avoid this situation, the change made in duty cycle must be sufficiently large such that for any permitted values of parameters, the minimum (maximum) value of the measured output voltage after changing the duty cycle (taking into account the effect of ripples) be larger than the maximum (minimum) value of the measured voltage before applying that change. This condition is equivalent to have

$$\Delta v_n > \Delta v_p. \quad (44)$$

In Fig. 8*b*, where Δv_n is equal to the change in the average value of output voltage at steady state in response to the change in duty cycle, and Δv_p is the peak-to-peak value of ripple voltage. In (44) assuming that the converter works in CCM, Δv_p can be approximated as follows [1]:

$$\Delta v_p = \frac{d_{n-1} T_s}{R_L C} v_o, \quad (45)$$

where v_o is the average value of output voltage as shown in Fig. 8. On the other hand, considering the fact that by neglecting the effect of parasitic elements, at steady state we have $v_o/v_{in} \simeq 1/(1 - d_{n-1})$, Δv_n in (44) is calculated as follows:

$$\Delta v_n = \frac{v_{in}}{(1 - d_{n-1})^2} \Delta d_n. \quad (46)$$

Substitution of (45) and (46) into (44) yields

$$\Delta d_n > \frac{(1 - d_{n-1})^2 d_{n-1} T_s}{R_L C} \times \frac{v_o}{v_{in}}. \quad (47)$$

Now substitution of $v_o/v_{in} \simeq 1/(1 - d_{n-1})$ in (47) yields

$$\Delta d_n > \frac{(1 - d_{n-1}) d_{n-1} T_s}{R_L C}. \quad (48)$$

In (48), the maximum value of $(1 - d_{n-1})d_{n-1}$ is equal to 0.25 which is obtained by setting $d_{n-1} = 0.5$. Hence, in order to avoid any error in detecting the state of converter because of the effect of switching, for all permitted values of load resistance, we must have $\Delta d_n > 0.25 T_s/R_L C$, or equivalently

$$\varepsilon_1 > \frac{0.25 T_s}{R_{L,\min} C}, \quad (49)$$

where $R_{L,\min}$ is the minimum possible value of the load resistance.

3 Simulation results

In the following simulations, it is assumed that the load resistance and input voltage are uncertain and time-variant such that $80\,\Omega \leq R_L \leq 160\,\Omega$ and $3\,V \leq v_{in} \leq 5\,V$. The values of C and T_s are considered equal to 4700 and 100 μs, respectively, (the choice of C affects the ripples in output voltage according to $\Delta v_p/v_o \leq T_s/R_L C$). The proposed values for C and T_s guarantee pretty small ripples in output voltage for all permitted values of load resistance. Moreover, according to (49) application of a large capacitor makes it possible to use a smaller ε_1, which leads to a smoother response specially at steady state. The values of L, α, ε_1, ε_2, δ are considered as 550 µH, 1, 0.1, 10, 0.01, respectively. Using these values, the minimum and maximum changes in duty cycle will be equal to 0.001 and 0.1, respectively. Various values of T are used in the following simulations to show the effect of this parameter on results. One method to find a reasonable initial estimation for T is to calculate the eigenvalues of the system matrix of boost converter for various values of R_L and d in the range. The reciprocal of the eigenvalue with smaller amplitude is approximately equal to the time-constant of response (the value of T can be considered equal to three times of this value). It is observed that in this problem $T = 100$ ms is sufficiently large to keep the closed-loop system stable under all circumstances.

Fig. 9*a* shows the ability to track the step command in the presence of input voltage variations assuming that the load resistance is fixed. In this simulation, the input voltage drops from 5 to 3 V for $6 < t < 8$ s. Since the reference voltage is reachable for all values of the input voltage, the output voltage tracks it without steady-state error. It is also observed that the application of $T = 25$ ms instead of $T = 50$ ms makes the converter response faster at the cost of making the closed-loop system less stable.

In the simulation of Fig. 9*b*, for $0 < t < 3$ s the output voltage, tracks the reference. However, for $3 \leq t < 6$ s the reference voltage is equal to 35 V which is too high and not reachable. In this time interval, the output voltage fluctuates around 27 V. At $t = 6$ s, the load resistance is suddenly increased from 80 to 160 Ω. According

© The Institution of Engineering and Technology 2018

17554543, 2018, 5, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/iet-pel.2017.0136 by Readcube (Labtiva Inc.), Wiley Online Library on [14/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

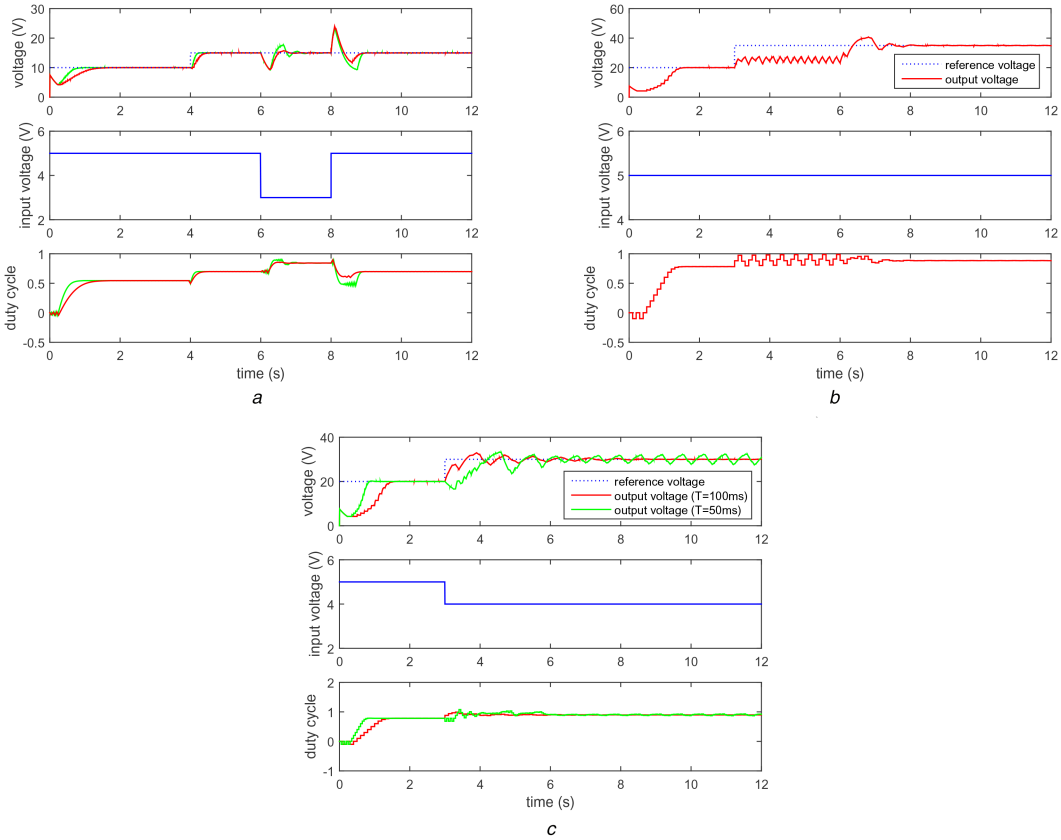

Fig. 9 *Simulation results*

(a) Tracking the step command assuming $R_L = 80\,\Omega$ ($T = 25$ ms (green) and $T = 50$ ms (red)), ***(b)*** Load resistance is changed from 80 to 160 W at $t = 6$ s ($T = 100$ ms), ***(c)*** Simultaneous change of reference voltage, input voltage, and load resistance (from 80 to 160 W) at $t = 3$ s

to this change, the 35 V reference voltage which was not reachable for $R_L = 80\,\Omega$ becomes reachable.

In the simulation of Fig. 9*c*, at $t = 3$ s the load resistance, input voltage, and reference voltage are simultaneously changed from 80 to 160 Ω, 5 to 4 V, and 20 to 30 V, respectively. The results are presented for both $T = 50$ and 100 ms. For $T = 100$ ms, the controller can effectively deal with this simultaneous change in parameters such that after a few seconds the output voltage tracks the reference voltage.

4 Experimental results

Fig. 7 shows the DC–DC boost converter and the proposed method for realising the controller. The elements of boost converter are considered as $L = 550\,\mu$H, $C = 4700\,\mu$F, IRF740 power MOSFET, and a 1N4001 diode. The 6N137 optocoupler is used to drive the power MOSFET and the current transducer CKSR 6-NP is exploited to measure the currents. The components inside the dashed box are implemented using the DSP TMS320f2812. A signal conditioner is used to scale the output voltage of converter from 0–24 to 0–3.3 V since the A/D of DSP accepts voltages in the latter range. The A/D of DSP takes samples from the output voltage of converter with a period $T_s = 100\,\mu$s. The sampling period of digital controller is considered equal to T which is related to the sampling period of A/D as $T = mT_s$ (see the discussion below). It signifies that the controller down-samples the output of A/D with factor m and updates all of its signals, including the tracking error at the input and the duty cycle at the output with a period T. The controller is implemented as shown in Fig. 6*b* and its parameters are considered as $\varepsilon_1 = 1$, $\varepsilon_2 = 8$, $\alpha = 4$, and $\delta = 0.008$. Notice that the functionality of the closed-loop system is not so sensitive to the special values assigned to these parameters and consequently their suitable values can be obtained by a simple trial and error considering the discussions of Section 2.

Fig. 10*a* shows the effects of stepwise changes in load resistance on the output voltage, load current, and inductor current when $v_{in} = 6$ V, $v_{ref} = 12$ V, $T = 200$ ms (or equivalently, $m = 2000$), and the frequency of PWM is equal to 1 kHz. In this figure, the load resistance is initially equal to 245 Ω which first drops to 100 Ω and then to 50 Ω, and finally again rises from 50 to 245 Ω. As it can be observed in this figure, the controller can effectively regulate the output voltage at the presence of these changes in load resistance. In Fig. 10*b*, everything is the same as Fig. 10*a* except the frequency of PWM which is equal to 8 kHz. We see that the transient response of converter becomes faster and the steady-state ripples in output voltage become smaller as the frequency of PWM increases from 1 to 8 kHz. Note that the converter works in DCM when the frequency of PWM is equal to 1 kHz and it works in both DCM and CCM when the frequency of PWM is equal to 8 kHz. These experiments show the ability of the proposed controller to work in both modes of operation.

Figs. 10*c*, *d* and 11*a* show the ability of the closed-loop system for tracking various reference voltages assuming that the load resistance and the input voltage are fixed at $R_L = 245\,\Omega$ and $v_{in} = 6$ V, respectively, and $T = 200$ ms. In all of these experiments, the reference voltage takes on values equal to 12, 18, 15, and 8 V, respectively. The only difference between these three experiments is that in Fig. 10*c* the frequency of PWM is equal to 8 kHz while in Figs. 10*d* and 11*a* it is equal to 66 and 1 kHz, respectively. These experiments clearly show that the proposed controller is not so sensitive to the frequency of PWM and a wide variety of values can be used for this purpose. Note that in Fig. 11*a* the converter always works in DCM while in Fig. 10*d* it works in CCM. These experiments again confirm the ability of the proposed controller to work in both CCM and DCM.

Fig. 11*b* shows the effect of stepwise changes in input voltage on the output voltage and load current when the load resistance, reference voltage and frequency of PWM are fixed at 100 Ω, 10 V and 8 kHz, respectively. In this experiment, the input voltage takes on values (approximately) equal to 5, 8, 1.5, and 9 V, respectively. It is observed that when the input voltage is equal to either 5 V or 8 V or 9 V the controller can effectively regulate the output voltage at the desired value. However, when the input voltage is equal to 1.5 V the reference voltage is not reachable and the controller

© The Institution of Engineering and Technology 2018

17554543, 2018, 5, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/iet-pel.2017.0136 by Readcube (Labtiva Inc.), Wiley Online Library on [14/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

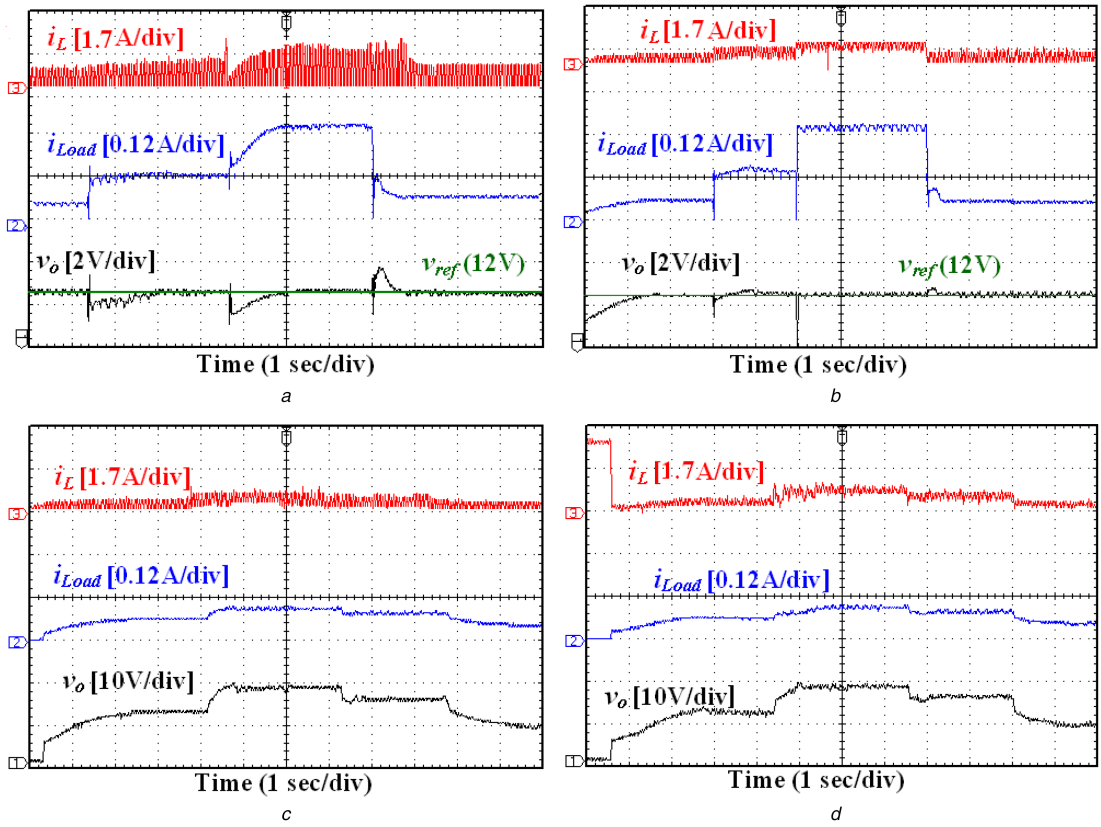

Fig. 10 *Experimental results*

(a) Effect of step changes in load resistance on the currents and output voltage of converter ($v_{in} = 6$ V, $v_{ref} = 12$ V, $T = 200$ ms, frequency of PWM = 1 kHz, and R_L takes on values equal to 245, 100, 50, and 245 Ω, respectively), ***(b)*** Experiment is the same as Fig. 10*a* with the frequency of PWM equal to 8 kHz, ***(c)*** Tracking a time-varying reference voltage which takes on values equal to 12, 18, 15, and 8 V, respectively ($R_L = 245$ Ω, $v_{in} = 6$ V, $T = 200$ ms, and frequency of PWM = 8 kHz), ***(d)*** Experiment is the same as Fig. 10*c* with the frequency of PWM equal to 66 kHz

results in a voltage approximately equal to 2.5 V at the output of the converter. This experiment reveals one big advantage of the proposed controller over classical PIDs. Recall from the discussions at the beginning of this paper that when the reference voltage is not reachable, the integral term of PID makes the closed-loop system unstable. However, in this experiment, we see that setting the reference voltage equal to a value which is not reachable, does not make the system unstable and the output voltage can again automatically track the reference voltage as soon as it becomes reachable. It is important to note that because of the uncertainties of the load resistance and input voltage we do not know in advance whether a given reference voltage is reachable or not.

Fig. 11*c* shows the effects of large stepwise changes in load resistance on the output voltage and inductor current assuming $v_{in} = 6$ V, $v_{ref} = 10$ V, $T = 300$ ms, and frequency of PWM equal to 8 kHz. In this experiment, the load resistance is initially equal to 47 Ω which first rises to 700 Ω and then again changes between 47 and 700 Ω. As it can be observed in this figure, the proposed controller can effectively regulate the output voltage at the presence of such a wide variations of load resistance. The experiment of Fig. 11*d* is the same as Fig. 11*c* with the only difference that the value of T is considered equal to 150 ms (note that in Fig. 11*d* the load resistance is initially equal 47 Ω). Comparing Figs. 11*d* and *c* reveals the fact that exploiting smaller values of T slightly decreases the steady-state ripples in load current and the output voltage at the cost of a slightly slower transient response.

5 Conclusion

A new definition for the state of boost converter based on the relative value of two successive samples of the output voltage with respect to the reference voltage is presented. Using this definition, it is shown that the boost converter has only six discrete-time states whose evolution can be modelled by a FSM. One advantage of this model is that it is valid at the presence of load and input voltage variations provided that the sampling period of the model is considered sufficiently large such that the system response to a small change in duty cycle settles down in one period for any value of load resistance in the range. A discrete-time controller is designed for the boost converter and stability of the resulted discrete-time closed-loop system is studied by means of the Lyapunov method. This stability analysis is rather simple since the number of states is limited and the negative semi-definiteness of the Lyapunov function needs to be proved only for the six possible states of the system.

One advantage of the proposed method is that it provides us with a simple discrete-time model for a closed-loop system containing both continuous-time and discrete-time systems (i.e. the converter and controller). Clearly, having access to such a model simplifies the controller design problem and stability analysis of the closed-loop system at the presence of uncertainties and non-linearities. As another advantage, the proposed controller is voltage-mode, i.e. no current sensor is required. The main disadvantage of the proposed controller is that the transient response of the resulted closed-loop system is slower compared to SMC.

© The Institution of Engineering and Technology 2018

17554543, 2018, 5, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/iet-pel.2017.0136 by Readcube (Labtiva Inc.), Wiley Online Library on [14/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

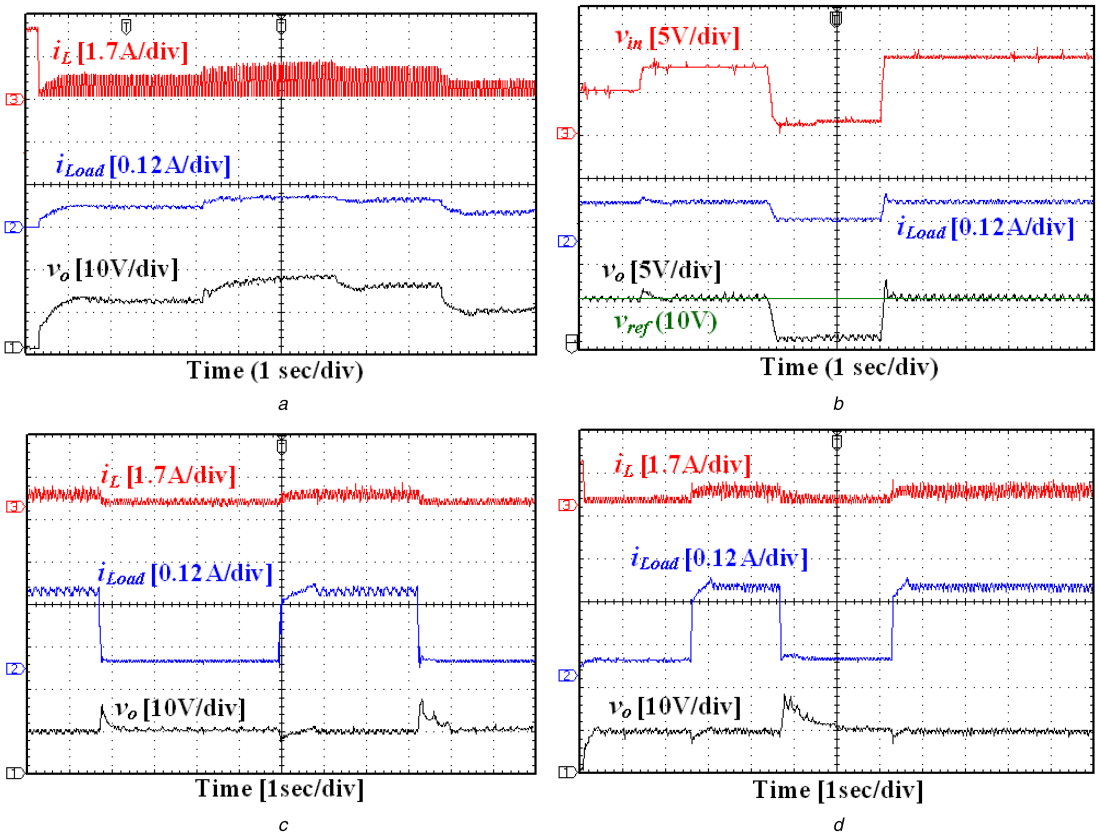

Fig. 11 *Experimental results*

(a) Experiment is the same as Fig. 10*d* with the frequency of PWM equal to 1 kHz, ***(b)*** Effect of variations of input voltage on the output voltage and load current ($R_L = 100\Omega$, $v_{ref} = 10$ V, and frequency of PWM = 8 kHz), ***(c)*** Effect of repeated stepwise changes of load resistance between 47 and 700 Ω on output voltage and currents ($v_{in} = 6$ V, $v_{ref} = 10$ V, $T = 300$ ms, and frequency of PWM = 8 kHz), ***(d)*** Experiment is the same as Fig. 11*c* with $T = 150$ ms

6 References

[1] Mohan, N., Undeland, T.M., Robbins, W.P.: '*Power electronics: converters, applications, and design*' (Wiley, Hoboken, New Jersey, USA, 2002, 3rd edn.)

[2] Molla-Ahmadian, H., Tahami, F., Karimpour, A., *et al.*: 'Hybrid control of DC-DC series resonant converters: the direct piecewise affine approach', *IEEE Trans. Power Electron.*, 2014, **30**, (3), pp. 1714–1723

[3] Vlad, C., Rodriguez-Ayerbe, P., Godoy, P., *et al.*: 'Advanced control laws of DC-DC converters based on piecewise affine modelling: application to a stepdown converter', *IET Power Electron.*, 2013, **7**, pp. 1482–1498

[4] Ferrari-Trecate, G., Alessandro Cuzzola, F., Mignone, D., *et al.*: 'Analysis of discrete-time piecewise affine and hybrid systems', *Automatica*, 2002, **38**, (12), pp. 2139–2146

[5] Bemporad, A., Morari, M.: 'Control of systems integrating logic, dynamics, and constraints', *Automatica*, 1999, **35**, (3), pp. 407–427

[6] Zhang, J., Xie, Z., Yang, G.: 'Mixed logical dynamical modeling and constrained optimal PWM control of DC/DC converters', *Electr. Mach. Control*, 2012, **16**, (4), pp. 106–112

[7] Pahlevaninezhad, M., Drobnik, J., Jain, P.K., *et al.*: 'A load adaptive control approach for a zero-voltage-switching DC/DC converter used for electric vehicles', *IEEE Trans. Ind. Electron.*, 2011, **59**, (2), pp. 920–933

[8] Karamanakos, P., Geyer, T., Manias, S.: 'Direct voltage control of DC-DC boost converters using enumeration-based model predictive control', *IEEE Trans. Power Electron.*, 2013, **29**, (2), pp. 968–978

[9] Elmas, C., Deperlioglu, O., Sayan, H.H.: 'Adaptive fuzzy logic controller for dc-dc converters', *Expert Syst. Appl.*, 2009, **29**, (2), pp. 1540–1548

[10] Garofalo, F., Marino, P., Scala, S., *et al.*: 'Control of DC/DC converters with linear optimal feedback and nonlinear feedforward', *IEEE Trans. Power Electron.*, 2005, **9**, (6), pp. 607–615

[11] Utkin, V.: 'Sliding mode control of DC/DC converters', *J. Franklin Inst.*, 2013, **350**, (8), pp. 2146–2165

[12] Oucheriah, S., Guo, L.: 'PWM-based adaptive sliding-mode control for boost DC-DC converters', *IEEE Trans. Ind. Electron.*, 2013, **60**, (8), pp. 3291–3294

[13] Tan, S.-C., Lai, Y.-M., Tse, C.K.: 'General design issues of sliding-mode controllers in dc-dc converters', *IEEE Trans. Ind. Electron.*, 2008, **55**, (3), pp. 1160–1174

[14] Zhang, C., Wang, J., Li, S., *et al.*: 'Robust control for PWM-based DC-DC buck power converters with uncertainty via sampled-data output feedback', *IEEE Trans. Power Electron.*, 2014, **30**, (1), pp. 504–515

[15] Senesky, M., Eirea, G., John Koo, T.: '*Hybrid modelling and control of power electronics*' (Springer Berlin Heidelberg, Berlin, Germany, 2003), vol. **2623,** (the series Lecture Notes in Computer Science), pp. 450–465

[16] Branicky, M.S., Borkar, V.S., Mitter, S.K.: 'A unified framework for hybrid control: model and optimal control theory', *IEEE Trans. Autom. Control*, 1998, **43**, (1), pp. 31–45

[17] Papafotiou, G., Geyer, T., Morari, M.: 'Hybrid modelling and optimal control of switch-mode dc-dc converters'. Proc. IEEE Workshop on Computers in Power Electronics, 15–18 August 2004, pp. 148–155

[18] Sreekumar, C., Agarwal, V.: 'A hybrid control algorithm for voltage regulation in DC-DC boost converter', *IEEE Trans. Ind. Electron.*, 2008, **55**, (6), pp. 2530–2538

[19] Hejri, M., Mokhtari, H.: 'Hybrid predictive control of a DC-DC boost converter in both continuous and discontinuous current modes of operation', *Optim. Control Appl. Methods*, 2011, **32**, (3), pp. 270–284

[20] Fernandez, D., Madrenas, J., Alarcon, E.: 'An asynchronous finite state machine controller for integrated buck-boost power converters in wideband signal-tracking applications'. Proc. IEEE Int. Symp. on Circuits and Systems, Seattle, WA, 18–21 May 2008, pp. 2210–2213

[21] Fernandez, D., Madrenas, J., Alarcon, E.: 'An asynchronous finite-state-machine-based buck-boost converter for on-chip adaptive power supply', *Analog Integr. Circuits Signal Process.*, 2013, **74**, (1), pp. 227–238

© The Institution of Engineering and Technology 2018

17554543, 2018, 5, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/iet-pel.2017.0136 by Readcube (Labtiva Inc.), Wiley Online Library on [14/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License