

New bidirectional multilevel inverter topology with staircase cascading for symmetric and asymmetric structures

Hosein Samsami¹, Asghar Taheri¹ , Rahim Samanbakhsh¹

¹Electrical Engineering Department, University of Zanjan, Zanjan, Iran

E-mail: taheri@znu.ac.ir

Abstract: Inverters, as one of the key components of electrical systems, have experienced a great evolution in the last decade, and their performance improvement is a challenge even today, leading to many researches on topologies and control schemes. This study introduces a new multilevel converter topology which is able to supply bidirectional current loads. The proposed structure has fewer power electronic devices such as power switches, driver circuits, power diodes, and DC voltage sources and, can be designed in both symmetric and asymmetric structures. In order to increase the number of output levels and the proposed basic unit development, modular expansion or cascading methods can be used. This study demonstrates that the aforementioned methods have the best results in asymmetric and symmetric structures of the proposed topology, respectively. The comparison between the proposed converter and some previous topologies shows that it has better conditions with respect to the used semiconductor count, switching and conduction losses, and total blocking voltage. The operation and performance of the proposed multi-level converter have been ascertained through simulations and verified experimentally for a single-phase symmetric thirty-one-level inverter which shows the proposed converter's ability in smooth sinusoidal output voltage generation with minimum total harmonic distortion.

1 Introduction

DC-to-AC power converters, which are commonly referred to as inverters, are one of the key components of electrical systems and have had many applications such as: reactive power compensators, adjustable-speed drives, uninterruptible power supplies, high-voltage DC power transmissions, and electric vehicles [1–3]. On the other hand, grid tie-renewable energy systems with power inverters supplying grid active power or compensating reactive power are ever-increasing. Therefore inverters have experienced a great evolution in the last decade, and their performance improvement is a challenge even today, leading to many researches on topologies and control schemes [4–6]. Conventional inverters produce square-wave output with two positive and negative voltage levels [7, 8]. The switching voltages across power switches, and dv/dt stresses of the mentioned topologies are considerable.

To overcome the mentioned problem, multi-level inverters (MLIs) with more than three-level output waveform have been introduced. Moreover, as the output voltage level increases, the instantaneous voltage variation of such inverters decreases, allowing the use of smaller and less expensive switches. Also, the number of voltage levels on the DC side increases, and the synthesised output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion. In addition, they can operate with a lower switching frequency.

Classical MLIs are classified into three topologies: neutral point clamped converters [9, 10], flying capacitors converters [11, 12], and cascaded H-bridge converters [13, 14]. When they are designed for an increased number of output voltage steps, they require a large number of power semiconductor switches, thereby increasing cost, volume, and control complexity. Therefore new topologies are being proposed and reported to reduce the overall count of active and passive devices for multi-level power conversion [4, 15–18]. New MLIs are classified into two categories: with and without transformer.

In the first type, the transformer's primary voltage steps have been produced by the bridge and can be changed by the transformer's secondary and tertiary voltage cascading and their ratio variations. On the one hand, the transformer establishes

isolation between the inverter and the grid. In addition, the transformer is a bulky component and the source of additional cost and power losses [19, 20]. Additional information about this topology can be found in [21–23].

The second type of the new MLIs, which are commonly referred to as 'hybrid inverters' has two main parts. First, a level-generation part which synthesises the multiple levels with only one polarity, and requires high-frequency switches to generate the required levels. Second, a polarity-generation part which is a bridge to convert this single polarity waveform to a bipolar one at the line frequency, and requires low-frequency switches [24–28].

This paper consists of five sections: the inverter power circuit with its working principle is presented in Section 2. In order to prove the performance of the proposed circuit, various comparisons with other recently suggested topologies have been conducted in Section 3. The experimental results are verified and comprehensively discussed in Section 4. Finally, conclusion is drawn in Section 5.

2 Proposed topology and operation principle

The basic unit of the multilevel converter, presented in [29], is illustrated in Fig. 1a. It consists of several DC voltage sources and bidirectional switches. If n capacitors are used, $n+1$ different values can be obtained for V_o , by $n+1$ bidirectional switches ($2n+2$ IGBTs (insulated-gate bipolar transistors) and $2n+2$ diodes). Fig. 1b illustrates the proposed structure in [30] which has improved the proposed topology in [29]. It generates the $n+1$ -level output voltage by n -bidirectional switches ($2n$ IGBTs and $2n$ diodes).

One switch consists of an IGBT and its anti-parallel diode can work as bidirectional switch and its IGBT and diode can conduct the current in forward and reverse directions, respectively. However, this structure cannot be used as switches of the presented topology in Fig. 1b (S_1, \dots, S_{n-1}). Due to, when S_k is turned ON, its below diodes (D_2, \dots, D_{k-1}) are turned ON. Therefore, the switches should be designed as bidirectional switches consisting of two IGBTs and their anti-parallel diodes connected in a common-emitter form. The presented topology in [30] has used all of the switches in this form.

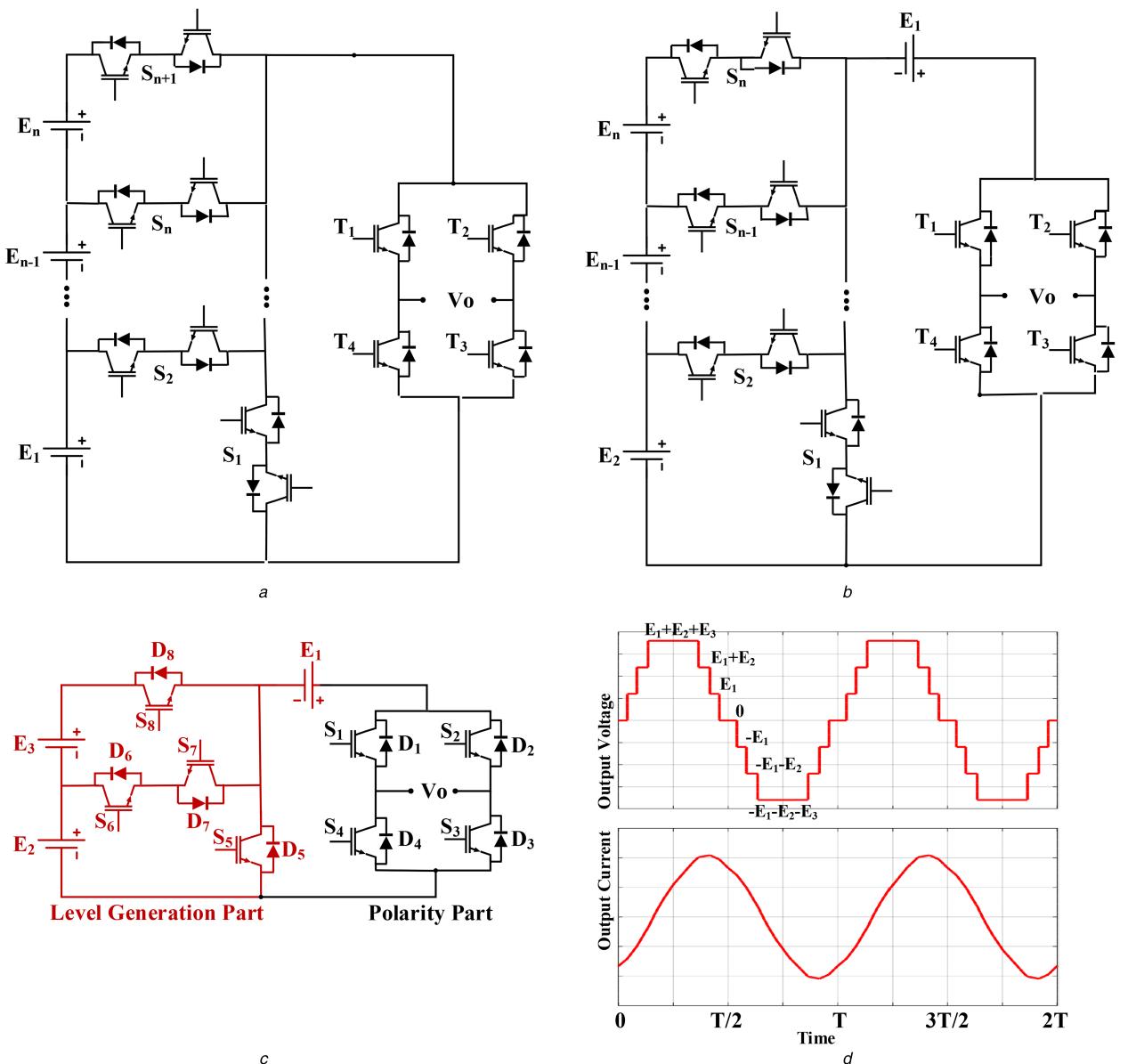


Fig. 1 Converter topologies

(a) Presented topology in [29], (b) Presented topology in [30], (c) Proposed topology, (d) Output voltage and current of the proposed inverter

Table 1 Switching states of the proposed basic unit

\$V_o\$	\$S_1\$	\$S_2\$	\$S_3\$	\$S_4\$	\$S_5\$	\$S_6/S_7\$	\$S_8\$
\$E_1 + E_2 + E_3\$	ON	OFF	ON	OFF	OFF	OFF	ON
\$E_1 + E_2\$	ON	OFF	ON	OFF	OFF	ON	OFF
\$E_1\$	ON	OFF	ON	OFF	ON	OFF	OFF
0	ON	ON	OFF	OFF	OFF	OFF	OFF

However, the aforementioned rule is not correct about the last switch (\$S_n\$). Because, there is not any switch after that which causes undesirable forward biasing of \$D_n\$ diode. Also, if the first switch (\$S_1\$) is designed in reverse direction in compare to others (its diode and IGBT conduct the current in forward and backward directions, respectively), the other switches cannot affect the \$D_1\$ diode. Based on this idea, this paper modifies the presented topology in Fig. 1b [30] and converts the aforementioned switches (\$S_1\$ and \$S_n\$) from bidirectional switches with two IGBTs and two diodes to bidirectional switches with one IGBT and one diode. These modifications decrease two IGBTs and two diodes of each module of the proposed converter in compare to presented topology in [30] and 2 m IGBTs and 2 m diodes in a cascaded converter with \$m\$ units.

Fig. 1c shows a seven-level basic inverter of the proposed topology. It is able to supply inductive load with bidirectional current and generate a staircase seven-level output voltage which can be seen in Fig. 1d. Due to the bidirectional switches (such as \$S_6\$ and \$S_7\$) the number of output voltage levels can be increased from seven to nine, if the voltage sources are selected asymmetrically.

Its switching modes are indicated in Table 1. According to the table, when the \$S_6/S_7\$ and \$S_8\$ switches are turned OFF, the \$S_5\$ (\$D_5\$) switch turns ON and conducts the current. Therefore, the DC-link voltage equals to \$E_1\$. In the second mode, the \$S_6\$ or \$S_7\$ switch is turned ON and the current flows from \$E_2\$ voltage source. As a result, the DC-link voltage becomes equal to the sum of \$E_1\$ and \$E_2\$. In the third mode, the \$S_8\$ switch conducts the current and the DC-link voltage is equal to \$(E_1 + E_2 + E_3)\$.

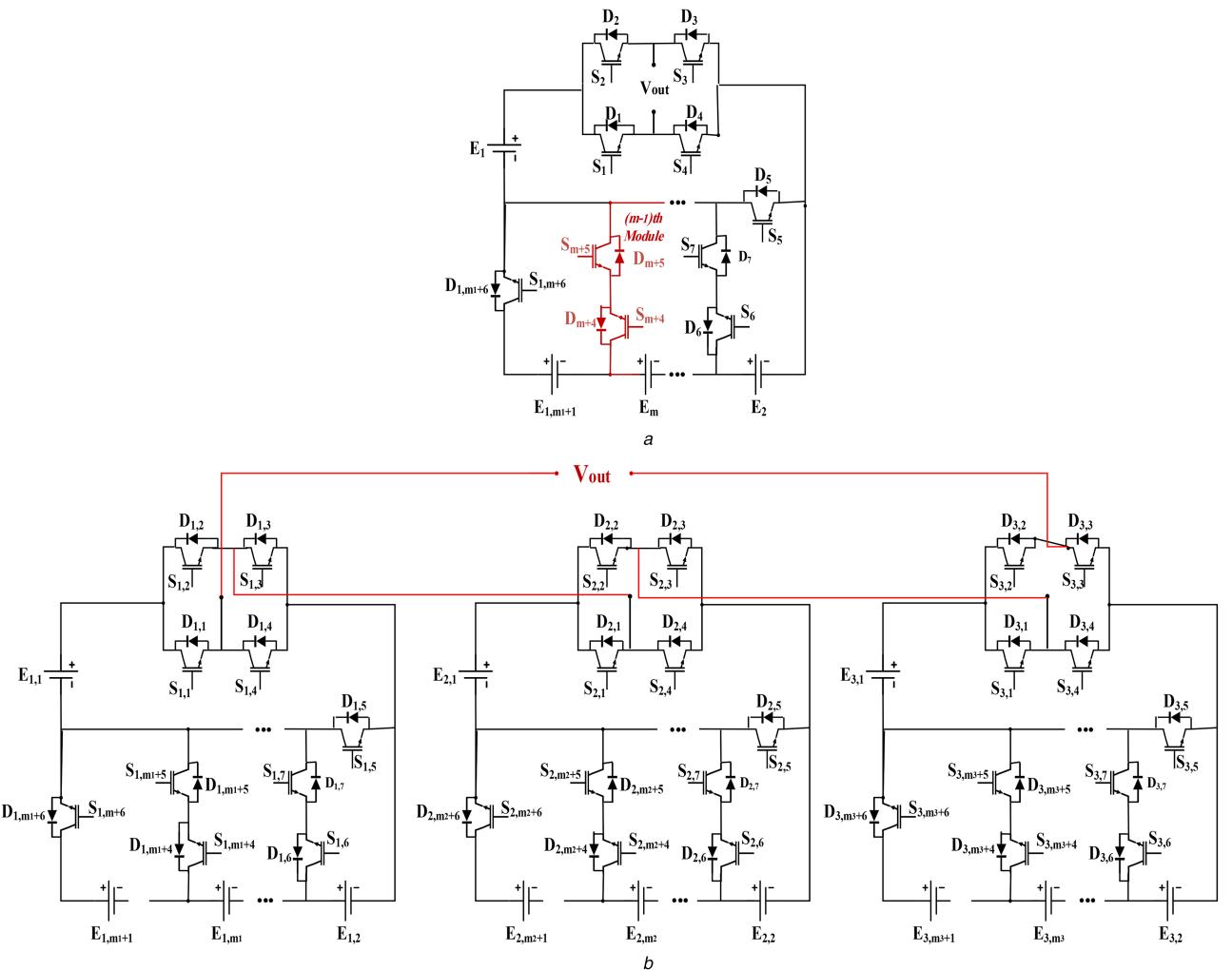


Fig. 2 Expansion of the proposed topology

(a) Modular, (b) Cascading

Table 2 Comparison of the level-increasing methods

Topology		Number of output level	Switch count
modular expansion	symmetric	$2m + 1$	$2 + 2m$
modular expansion	asymmetric	$1 + 2\sum C(m - 1, i) \quad 0 \leq i \leq m - 1$	$2 + 2m$
normal cascaded	symmetric	$1 + 2\sum m_i \quad 1 \leq i \leq k$	$2 + 2\sum m_i \quad 1 \leq i \leq k$
normal cascaded	asymmetric	$1 + 2\sum \sum C(m_i - 1, j) \quad 0 \leq j \leq m_i - 10 \leq i \leq k$	$2 + 2\sum m_i \quad 1 \leq i \leq k$
staircase cascaded	symmetric	$2 \prod (m_i + 1) \quad 11 \leq i \leq k$	$2 + 2\sum m_i \quad 1 \leq i \leq k$
staircase cascaded	asymmetric	$2 \prod (\sum C(m_i - 1, j) + 1) \quad 10 \leq j \leq m_i - 1, 0 \leq i \leq k$	$2 + 2\sum m_i \quad 1 \leq i \leq k$

The number of voltage levels on the DC side increases, and the synthesised output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion. In order to increase the number of output levels, two methods are used. First, according to Fig. 2a, switches and the DC voltage source count increase, which is named the ‘modular expansion method’. In this case, the inverter with symmetric n modules (the DC voltage source with the related bidirectional switch) can generate $2n + 3$ levels of output voltage. The second method is the basic unit series connecting to generate a new cascaded MLI. An inverter with k basic units is shown in Fig. 2b. The units can have similar switching patterns with phase shifting or the pattern proposed in [31]. In this method, each unit generates all of its levels in each level of the previous unit. These methods are named ‘normal cascaded’ and ‘staircase cascaded’, respectively. Both of them can be used in symmetric and

asymmetric structures. Fig. 2b uses both of the mentioned methods to expand the MLI base of the proposed topology. In other words, it consists of cascaded units which are expanded with the modular method.

Table 2 compares the aforementioned level-increasing methods. In this table, m is the number of DC voltage sources of the modular inverter. Also, m_i and k are the number of units and DC voltage sources of the cascaded inverter, respectively. In order to clarify the comparison of their quantity parameters, Table 3 lists their parameters in two study cases. It is illustrated that in symmetric and asymmetric topologies, the staircase cascaded and modular expansion structures have the fewest switches and most output level in comparison to others, respectively.

Table 4 indicates the switching states of the general inverter which is shown in Fig. 2b. The DC voltage sources of its units are based on (1) and (2) for symmetric and asymmetric structures, respectively, where E is the base value of the DC voltage sources which is the value of the first DC source of the first unit ($E_{1,1}$ in Fig. 2b), and m_k is the number of DC voltage sources of the k th unit

$$E_{k,i} = \frac{E}{\prod_{i=2}^k (m_i + 1)} \quad (1)$$

$$E_{k,i} = \begin{cases} \frac{E}{\prod_{i=2}^k (2^{m_k-1} + 1)} & i = 1 \\ \frac{2^{i-2} E}{\prod_{i=2}^k (2^{m_k-1} + 1)} & i > 1 \end{cases} \quad (2)$$

Table 3 Comparison of the level increasing methods

Topology	DC source count = 6			DC source count = 8	
		Number of output levels	Switch count	Number of output levels	Switch count
modular expansion	symmetric	13	14	17	18
	asymmetric	65	14	257	18
normal cascaded	symmetric	13	16	17	20
	asymmetric	17	16	33	20
staircase cascaded	symmetric	31	16	49	20
	asymmetric	49	16	127	20

Table 4 Switching states of Fig. 2b

Output voltage (V_{out})	ON state switches			
	First unit	Second unit	... kth unit unit	
$\left(m_1 + \frac{m_2}{m_2+1} + \frac{m_k}{\prod_{i=2}^k (m_i+1)}\right)E$	$S_{1,1}, S_{1,3}, S_{2,1}, S_{2,3}, \dots, S_{k,1}, S_{k,3}$			
	$S_{1,m1+6}$	$S_{2,m1+6}$	$S_{k,m1+6}$	
:	:	:	...	:
$\left(m_1 + \frac{m_2}{m_2+1}\right)E$	$S_{1,1}, S_{1,3}, S_{2,1}, S_{2,3}, \dots, S_{k,1}, S_{k,2}$			
	$S_{1,m1+6}$	$S_{2,m1+6}$		
:	:	:	...	:
$(m_1)E$	$S_{1,1}, S_{1,3}, S_{2,1}, S_{2,2}, \dots, S_{k,1}, S_{k,2}$			
	$S_{1,m1+6}$			
:	:	:	...	:
0	$S_{1,1}, S_{1,2}, S_{2,1}, S_{2,2}, \dots, S_{k,1}, S_{k,2}$			
:	:	:	...	:
$-(m_1)E$	$S_{1,2}, S_{1,4}, S_{2,3}, S_{2,4}, \dots, S_{k,3}, S_{k,4}$			
	$S_{1,m1+6}$			
:	:	:	...	:
$-\left(m_1 + \frac{m_2}{m_2+1}\right)E$	$S_{1,2}, S_{1,4}, S_{2,2}, S_{2,4}, \dots, S_{k,3}, S_{k,4}$			
	$S_{1,m1+6}$	$S_{2,m1+6}$		
:	:	:	...	:
$-\left(m_1 + \frac{m_2}{m_2+1} + \frac{m_k}{\prod_{i=2}^k (m_i+1)}\right)E$	$S_{1,2}, S_{1,4}, S_{2,2}, S_{2,4}, \dots, S_{k,2}, S_{k,4}$			
	$S_{1,m1+6}$	$S_{2,m1+6}$	$S_{k,m1+6}$	

The aforementioned level increasing methods have variables such as the number of units, the number of modules in each unit, and the ratio of voltage sources between the units. They can be optimised to reach minimum costs, losses, number of switches, and output harmonic contents. To further describe the optimisation, the Fourier series of the output voltage of the MLI consisting of two units has been determined. The units have N and M levels in their DC-link voltages, respectively. The voltage level can be defined as follows:

$$V_{IJ} = \sum_{i=1}^I E_{1i} + \sum_{j=1}^J E_{2j}, \quad I \leq N, J \leq M \quad (3)$$

where E_{1k} is the k th DC voltage of the first unit and E_{2j} is the j th DC voltage of the second unit. Now, if the output signal has a half-wave symmetric scheme, the harmonic content can be defined as follows:

$$V_o = \sum_{n=1,3,5,7,\dots} a_n \cos(n\omega t) + b_n \sin(n\omega t) \quad (4)$$

$$a_n = \frac{2}{n\pi} \left[\sum_{K=1}^N \sum_{i=K}^N \sum_{j=0}^M (\sin(nT'_{ij}) - \sin(nT_{ij})) E_{1k} \right. \\ \left. + \sum_{h=1}^M \sum_{r=0}^N \sum_{s=h}^M (\sin(nT'_{rs}) - \sin(nT_{rs})) E_{2h} \right] \quad (5)$$

$$b_n = \frac{2}{n\pi} \left[\sum_{K=1}^N \sum_{i=K}^N \sum_{j=0}^M (\cos(nT_{ij}) - \cos(nT'_{ij})) E_{1k} \right. \\ \left. + \sum_{h=1}^M \sum_{r=0}^N \sum_{s=h}^N (\cos(nT_{rs}) - \cos(nT'_{rs})) E_{2h} \right] \quad (6)$$

3 Power distribution ratio of the sources

Multi-level converters often use several isolated voltage sources. The distribution of the power generation among the sources is important and should be considered and controlled. This section analyses it and shows the power distribution ratio of the sources at different modulation indices. The output active power of m th voltage source (P_m) of the MLI is according to the following equation:

$$P_m = \sum_{k=m}^N P_{mk} \quad (7)$$

where P_{mk} is the output active power of m th voltage source in the k th level of the output voltage. It can be derived as follows:

$$P_{mk} = \int_{t_k}^{t_{k+1}} i_{mk}(t) E_{mk}(t) dt = \int_{t_k}^{t_{k+1}} i_k(t) E_m(t) dt \quad (8)$$

where E_{mk} and i_{mk} are the voltage and current of the m th voltage source in the k th level of the output voltage, respectively. Also, i_k is the load current in the k th level of the output voltage. If the output voltage of the MLI is assumed as shown in Fig. 3a, the i_k can be derived as in (9), where R and L are the resistance and inductance of the load, respectively. Also, I_0 is the initial current of the load

$$i_k(t) = I_0 e^{-(R/L)t} - \frac{E_k}{R} e^{-(R/L)(t-t_k)} + (1 - e^{-(R/L)(t-t_k)}) \sum_{i=1}^k \frac{E_i}{R} \quad (9)$$

With attention to (9), (8) can be rewritten as follows:

$$P_{mk} = \left[\frac{L I_0 E_m}{R} (e^{-(R/L)t_k} - e^{-(R/L)t_{k+1}}) + (t_{k+1} - t_k) \sum_{i=1}^k \frac{E_i E_m}{R} \right. \\ \left. + \left(E_k + \sum_{i=1}^k E_i \right) (1 - e^{-(R/L)(t_{k+1} - t_k)}) \frac{L E_m}{R^2} \right] \quad (10)$$

Now, the combination of (7) and (10) results the output active power of the m th voltage source as (see (11))

In a symmetric topology ($E_i = E$) without any initial load current ($I_0 = 0$), (11) can be rewritten as

$$P_m = \left[\left(\frac{T}{4} - t_m \right) + \sum_{k=m}^N \left[(k+1)(1 - e^{-(R/L)(t_{k+1} - t_k)}) \frac{L}{R} \right] \right] \frac{E^2}{R} \quad (12)$$

where T is the period of output voltage in radian (2π) and N is the number of the DC voltage sources. Therefore, the active power factor of the m th voltage sources can be defined as follows:

$$F_{Pm} = \left(\frac{\pi}{2} - t_m \right) + \sum_{k=1}^N \left[(k+1)(1 - e^{-(R/L)(t_{k+1} - t_k)}) \frac{L}{R} \right] \quad (13)$$

Also, the active power distribution ratio factor of the voltage sources can be defined as follows:

$$F_{DPm} = \frac{F_{Pm}}{\sum_{i=1}^N F_{Pi}} \quad (14)$$

In MLIs which use pulse-wide modulation with a sinusoidal reference signal and several carrier signals to generate switching patterns, the t_i times [in Fig. 3a and (8)–(13) formulas] and subsequently the active power distribution ratio factor of the voltage sources are depend on the reference signal amplitude [modulation index, which is defined as (15)], the initial phase of the reference signal, and pattern of the carrier signals

$$m_a = \frac{A_r}{NA_c} \quad (15)$$

where A_r and A_c are the amplitude of the reference and carrier signals, respectively. Fig. 3b shows the variation of power distribution ratio factors of the voltage sources against the modulation index in a seven-level inverter based on introduced topology. It can be illustrated that the ratio of first source is decreased with the modulation index increasing. Conversely, the last source has direct relationship with the modulation index and the intermediate sources have different behaviour and are first increased and then decreased.

With other switching methods like SHE and optimisation methods, the minimisation of the power distribution can be defined as one of the optimisation objects and controlled better. In other words, t_i times are derived in order to optimisation of the objects like minimisation of power distribution ratio factor differences, selective harmonics elimination and fundamental voltage and current control.

4 Comparison with other topologies

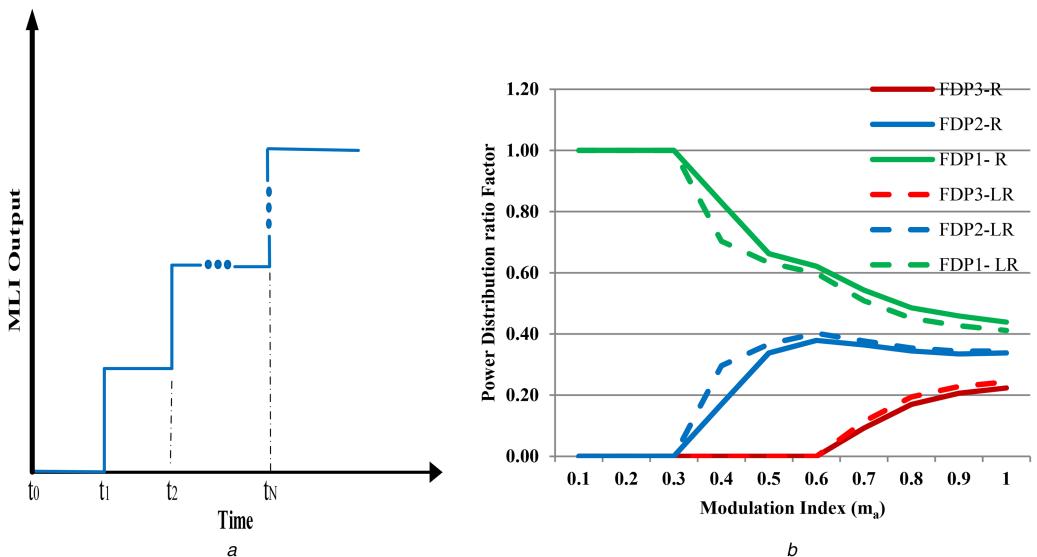


Fig. 3 Power distribution analysis

(a) General output voltage of the MLI, (b) Power distribution of the voltage sources of the introduced topology with resistive (R) and inductive (RL) loads

4.1 Comparison of the conduction losses

The resistance of the semiconductor component causes losses when the switches conduct the current. This type of losses is named ‘conduction losses’ which can be derived as

$$P_{\text{cond}} = V_{\text{on}}(t) \cdot I(t) \quad (16)$$

where $V_{\text{on}}(t)$ and $I(t)$ are the instantaneous voltage and current of the turned ON switches, respectively. Equation (17) can be rewritten for transistors and diodes as follows:

$$P_{\text{cond},T} = (V_{\text{on},T}(t) \cdot R_T I^\beta(t)) \cdot I(t) \quad (17)$$

$$P_{\text{cond},D} = (V_{\text{on},D}(t) \cdot R_D I(t)) \cdot I(t) \quad (18)$$

where $V_{\text{on},T}$ and $V_{\text{on},D}$ are the voltages of the transistor and diode during the ON state, respectively, while R_T and R_D are the equivalent resistances of the transistor and diode, respectively, and β is a constant that depends on the specification of the transistor. The average conduction losses of the introduced inverter with N_D number of diodes and N_S number of switches (IGBTs) can be determined with the following equation:

$$P_{\text{cond}} = \sum_{i=1}^{N_S} \frac{1}{T} \int_0^{T_i} (V_{\text{on},Ti}(t) \cdot R_{Ti} I^{\beta_i}(t)) \cdot I_i(t) dt + \sum_{j=1}^{N_D} \frac{1}{T} \int_0^{T_j} (V_{\text{on},Dj}(t) \cdot R_{Dj} I(t)) \cdot I_j(t) dt \quad (19)$$

where R_{Ti} and I_i are the equivalent resistance and current of the i th switches, respectively. Also, R_{Dj} and I_j are the equivalent resistance and current of the j th diodes, respectively. Variation of the conduction losses against the output signal level number (N_{level}) in the introduced topology have been compared with other structures, as shown in Fig. 4a. It demonstrates that the proposed structure has the fewest losses.

$$P_m = \left[\frac{LI_0}{R} (e^{-(R/L)t_m} - e^{-(R/L)t_{n+1}}) + \sum_{i=m+1}^N \frac{(E_{i-1} - E_i)}{R} t_i + \left(\frac{T}{4} - t_m \right) \frac{E_m}{R} \times \sum_{k=m}^N \left[\left(E_k + \sum_{i=1}^k E_i \right) \left(1 - e^{-(R/L)(t_{k+1} - t_k)} \right) \frac{L}{R^2} \right] \right] E_m \quad (11)$$

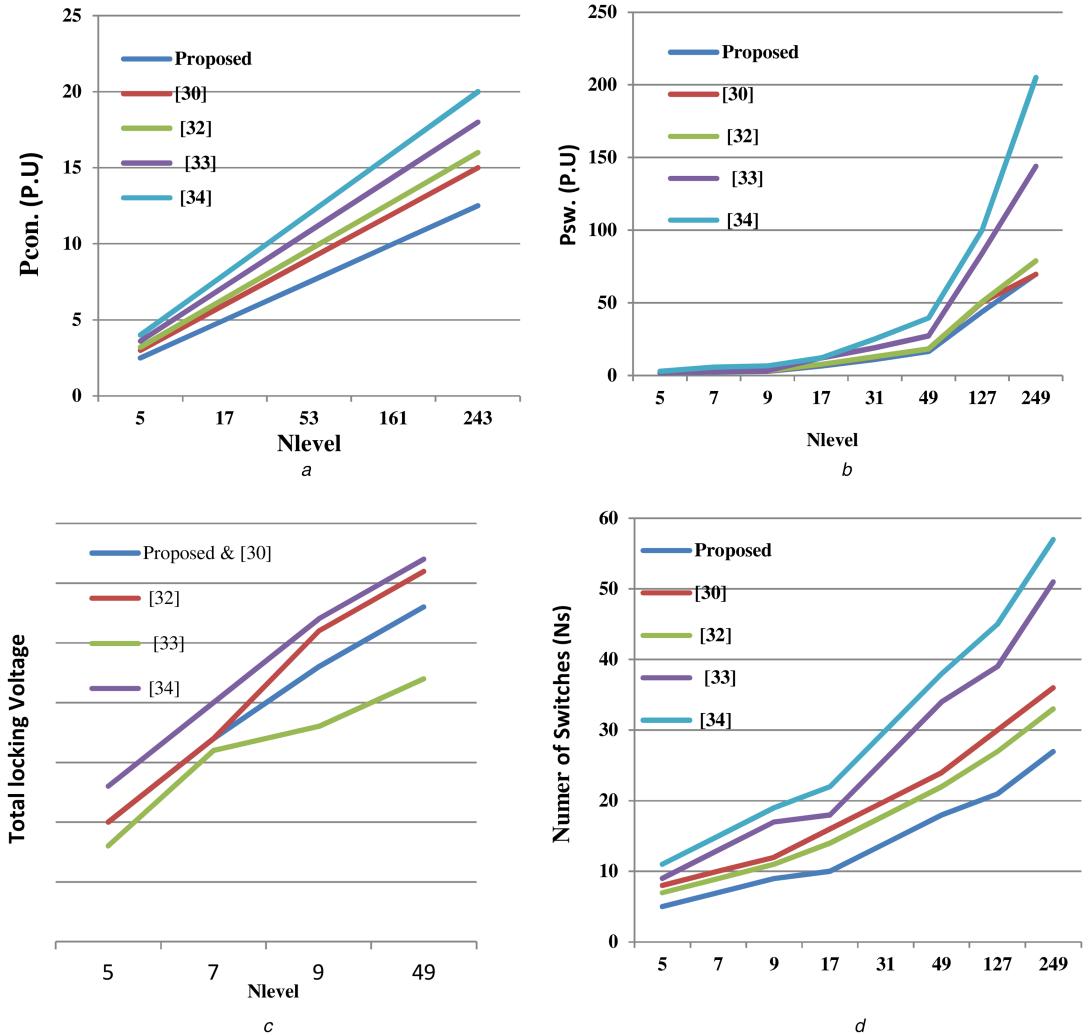


Fig. 4 Comparison of the proposed topology with others

(a) Conduction losses of the switches, (b) Switching losses, (c) Total blocking voltage, (d) Number of the switches (N_S)

4.2. Comparison of the switching losses

The turning ON process of a switch decreases its voltage from its OFF state value (V_S) to zero, and increases the current from zero to load current (I) in a short time (T_S); in the turning OFF process, the reverse of this happens and this variation causes another type of losses named ‘switching losses’. Equation (20) is used for the average of switching losses [32], where t_{off} is the starting time of the turning ON process. Fig. 4b compares the proposed inverter’s switching losses with those of previous structures which have been introduced in [24, 30, 33, 34]. It can be seen that our topology has the fewest switching losses:

$$\begin{aligned} P_{\text{sw}} &= 2 \int_0^{T_S} V(t) I(t) dt \\ &= 2 \int_0^{T_S} \left[\left(\frac{V_S \cdot t}{t_{\text{off}}} \right) \left(-\frac{I(t - t_{\text{off}})}{t_{\text{off}}} \right) \right] dt \\ &= \frac{V_S \cdot I \cdot T_S}{3} \end{aligned} \quad (20)$$

4.3 Comparison of the blocking voltages on switches

The selection of the MLI switches depends on their blocking voltages and ON state currents which affect the inverter cost. The current depends on load and the topology cannot affect it. On the other hand, the blocking voltage completely depends on structure and topology of the inverter. The aim of studies is designing topologies with a minimum total blocking voltage (V_B) which can be obtained as

$$V_B = V_{BL} + V_{BB} \quad (21)$$

where V_{BL} is the blocking voltage of the switches of the level-generation part, and V_{BB} is the blocking voltage of the bridge switches

$$V_{BLj} = \sum_{i=1}^n V_{BLij} = \begin{cases} 2\left((n-1) + \dots + \frac{(n-2)}{2}\right) + \frac{n}{2} + n = \frac{3n^2}{4} & \text{for even } n \\ 2\left((n-1) + \dots + \frac{(n-1)}{2}\right) + n = \frac{3n^2+1}{4} & \text{for odd } n \end{cases} \quad (22)$$

where V_{BLj} and V_{BLij} are the blocking voltages of the j th unit level generation part and its i th switch, respectively. Now, if G is defined as follows:

$$G = \begin{cases} 2\left((n-1) + \dots + \frac{(n-2)}{2}\right) + \frac{n}{2} + n = \frac{3n^2}{4} & \text{for even } n \\ 2\left((n-1) + \dots + \frac{(n-1)}{2}\right) + n = \frac{3n^2+1}{4} & \text{for odd } n \end{cases} \quad (23)$$

V_{BL} can be determined as follows:



Fig. 5 Experimental setup of the proposed topology

$$V_{BL} = \sum_{j=1}^m V_{BLj} = \sum_{j=1}^m G_j V_{DCj} \quad (24)$$

where m is the number of units, and V_{DCj} is the DC source value of the j th unit. If the value of the DC source of the k th unit is $E/(n+1)^{k-1}$ and all of the units have the same number of sources (n), V_{BL} can be determined as follows:

$$V_{BL} = \begin{cases} \frac{3n^2}{4} E \sum_{j=1}^m \frac{1}{(n+1)^{j-1}} & \text{for even } n \\ \frac{3n^2+1}{4} E \sum_{j=1}^m \frac{1}{(n+1)^{j-1}} & \text{for odd } n \end{cases} \quad (25)$$

Now, the blocking voltage of the bridge switches should be determined as

$$V_{BB} = \sum_{j=1}^m V_{BBj} = \sum_{j=1}^m 4nV_{DCj} = \sum_{j=1}^m \frac{4nE}{(n+1)^{j-1}} \quad (26)$$

Combining of (21), (25) and, (26), the following equation is derived:

$$V_B = \begin{cases} \left(\frac{3n^2+16n}{4}\right) \left(\sum_{j=1}^m \frac{1}{(n+1)^{j-1}}\right) E & \text{for even } n \\ \left(\frac{3n^2+16n+1}{4}\right) \left(\sum_{j=1}^m \frac{1}{(n+1)^{j-1}}\right) E & \text{for odd } n \end{cases} \quad (27)$$

Fig. 4c shows the total blocking voltage of previous structures and compares them with the proposed inverter. This comparison demonstrates that it has a better specification than [33] and [24], although, [34] has the lowest one.

4.4. Comparison of the required number of switches

The switches including IGBTs and anti-parallel diodes are the main part of the MLIs which affects the cost, size of the circuit, and the control complexity. A comparison between the proposed topology and other structures in [24, 30, 33, 34] based on the number of switches (N_S) against the number of output levels (N_{level}) is shown in Fig. 4d. It can be concluded that the recommended topology requires fewer switches. It should be noted that all of them are symmetric and bidirectional, with a staircase cascaded structure.

5 Simulation and experimental results

The verification and validation of the above-mentioned topology are done with simulation and experimentation on a thirty-one-level converter based on the proposed structure. The simulation has been carried out in MATLAB/SIMULINK. For practical tests, the switching control is carried out by EZDSP2812 which provides the switching pulses. The power electronic switches are IGBTs from the BUP306D and BUP314D type for the level-generation and the

bridge part, respectively. The staircase cascaded method is used to control the converter and its switching. The converter is designed to generate of 225 V peak output voltage, consisting of three 60 V steps in the first unit and three 15 V steps in the second unit. Simulation and experimentation have both been conducted with the frequency of 50 Hz and a series $R-L$ load (10Ω of resistance and 0.05 H of inductance). The experimented converter (Fig. 5) uses 8 gate driver circuits, 16 switches (IGBTs and diodes) and 6 DC voltage sources.

The output voltages of the first and second units of the simulated converter are shown in Figs. 6a and b, respectively. The final output voltage is cascaded of them, which is shown in Fig. 6c. The corresponding results demonstrate that the converter based on the proposed topology can generate the staircase output voltage with the expected levels. Fig. 6d shows the load current of the simulation which is almost a sinusoidal waveform with a phase-angle difference with respect to the output voltage because of the inductive load.

Fig. 7 shows the experimental results of the thirty-one-level inverter based on the proposed topology. Figs. 7a-d show the output voltage of the first unit, output voltage of the second unit, output voltage and current, respectively. It is shown that the simulations and the experimental results have a good agreement with each other. However, the voltage drop on the switches in the experimental results may cause a little difference. It should be noted that the simulations are done with ideal switches.

The fast Fourier transform (FFT) analysis of the voltage and current of the experimental setup are shown in Figs. 8a and b, respectively. It is demonstrated that the THD values of the output voltage and current are 3.27 and 0.37%, respectively.

6 Conclusion

In this paper, a basic unit has been proposed for the multi-level converters. Then, several modifications have been applied to enable the converter to supply the inductive load with a bidirectional current. Moreover, its expansion and output level-increasing methods have been discussed. The results demonstrate that the modular expansion and staircase cascading are the best methods for asymmetric and symmetric structures, respectively. In the proposed topology, the number of switches, switching losses, conduction losses and total blocking voltage are reduced for a specific number of voltage levels in comparison with the topologies presented in [32] which leads to the reduced installation space and cost of the inverter.

Finally, the abilities of the proposed topology were verified with simulation and experimentation on a thirty-one-level converter. The corresponding results show that the simulations and the experimental results have a good agreement with each other, which verifies the fact that the proposed topology is able to generate the output voltage with the expected levels and magnitude.

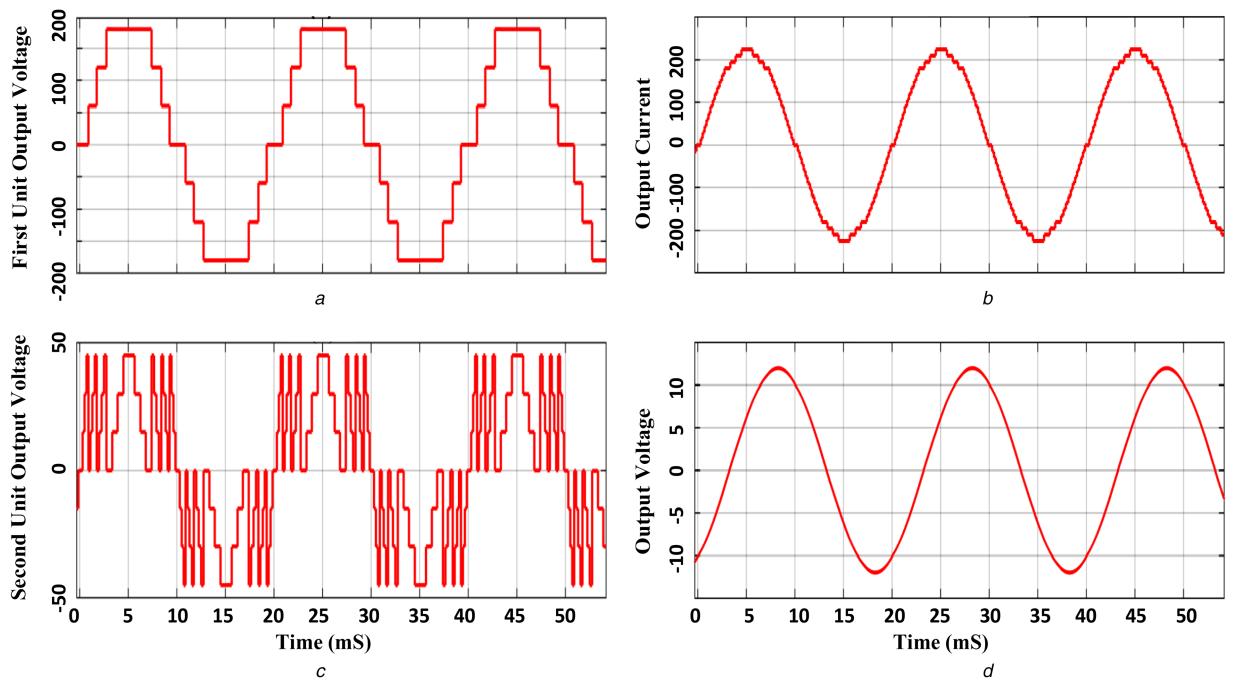


Fig. 6 Simulation results of the proposed converter with $R-L$ load

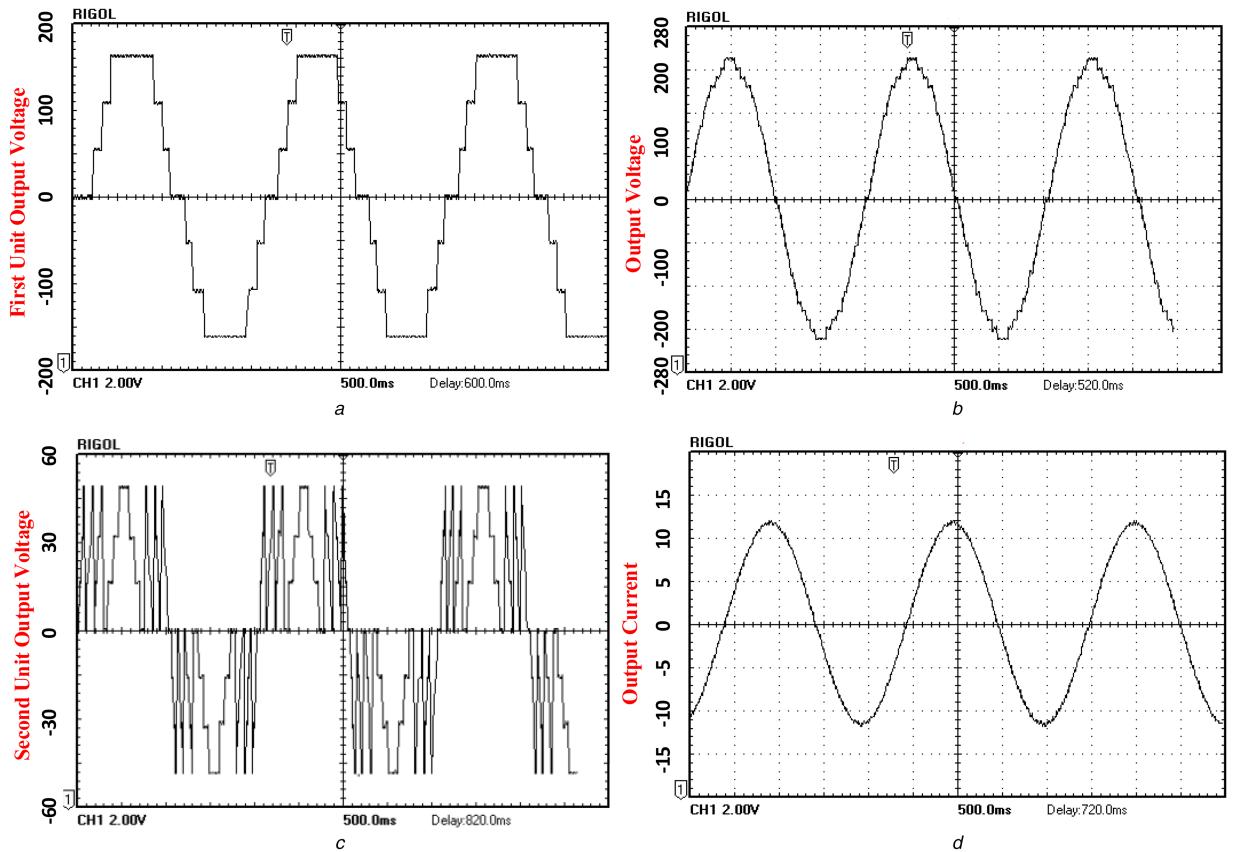


Fig. 7 Experimental results of the proposed converter with $R-L$ load

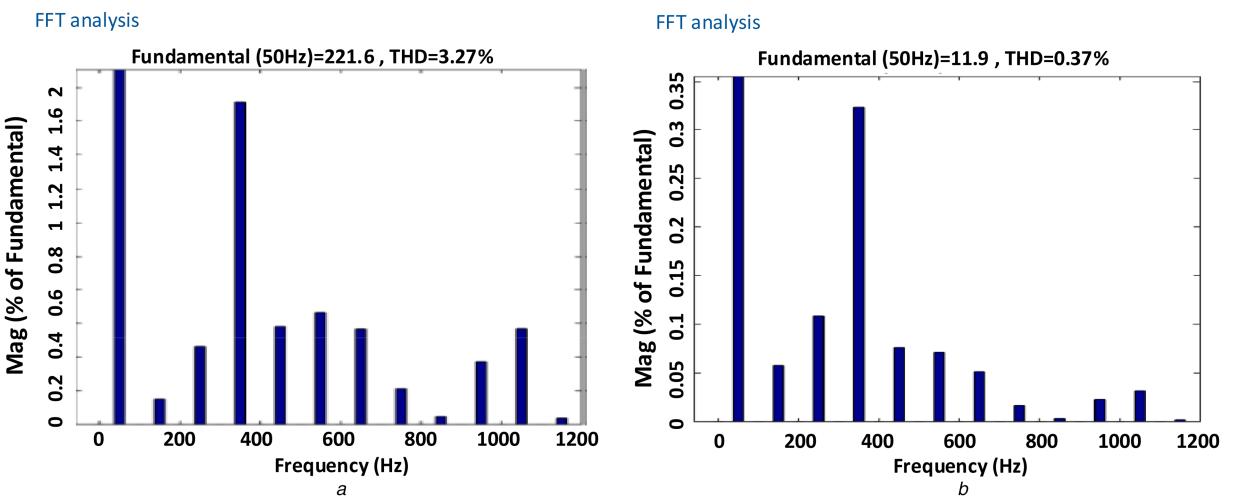


Fig. 8 FFT analysis of the proposed converter with R-L load

(a) FFT analysis of output voltage, (b) FFT analysis of output current

7 References

- [1] Espinoza, J.R., Rashid, M.H.: 'Inverters', 'Power electronics handbook' (Elsevier, New York, NY, USA, 2001), pp. 225–269
- [2] Abbott, D.: 'Keeping the energy debate clean: how do we supply the world's energy needs?', *Proc. IEEE*, 2010, **98**, (1), pp. 42–66
- [3] Xinghuo, Y., Cecati, C., Dillon, T., et al.: 'The new frontier of smart grids', *IEEE Ind. Electron. Mag.*, 2011, **5**, (3), pp. 49–63
- [4] Liao, Y.H., Lai, C.M.: 'Newly-constructed simplified single-phase multi string multi-level inverter topology for distributed energy resources', *IEEE Trans. Power Electron.*, 2011, **26**, (9), pp. 2386–2391
- [5] Gupta, K.K., Jain, S.: 'Topology for multilevel inverters to attain maximum number of levels from given DC sources', *IET Power Electron.*, 2012, **5**, (4), pp. 435–446
- [6] Rahim, N.A., Fathi, M., Elias, M., et al.: 'Transistor-clamped H-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing', *IEEE Trans. Ind. Electron.*, 2013, **60**, (8), pp. 2943–2956
- [7] Lai, J.S., Peng, F.Z.: 'Multilevel converters – a new breed of power converters', *IEEE Trans. Ind. Appl.*, 1996, **32**, (3), pp. 509–517
- [8] Tolbert, L.M., Chiasson, J.N., Du, Z., et al.: 'Elimination of harmonics in a multilevel converter with noequal DC sources', *IEEE Trans. Ind. Appl.*, 2005, **41**, (1), pp. 75–81
- [9] Nabae, A., Takahashi, I., Akagi, H.: 'A new neutral-point clamped PWM inverter', *IEEE Trans. Ind. Appl.*, 1981, **17**, (5), pp. 518–523
- [10] Nabae, A., Takahashi, I., Akagi, H.: 'A neutral-point-clamped PWM inverter'. Proc. Conf. Rec. IEEE IAS Annual Meeting, Cincinnati, OH, USA, 1980, vol. 3, pp. 761–766
- [11] Meynard, T.A., Foch, H.: 'Multi-level choppers for high voltage applications', *Eur. Power Electron. Drives J.*, 1992, **2**, (1), pp. 41–45
- [12] Lavieille, J.P., Carrere, P., Meynard, T.: 'Electronic circuit for converting electrical energy and a power supply installation making use thereof'. U.S. Patent 5 668 711, 1997
- [13] Hammond, P.: 'A new approach to enhance power quality for medium voltage ac drives', *IEEE Trans. Ind. Appl.*, 1997, **33**, pp. 202–208
- [14] Baker, R.H.: 'Switching circuit'. U.S. Patent 4210826, 1980
- [15] Chaturvedi, P.K., Jain, S., Agarwal, P.: 'A simple carrier based neutral point potential regulator for 3-level diode clamped inverter', *Int. J. Power Electron.*, 2011, **3**, (1), pp. 1–25
- [16] Liu, Y., Luo, F.L.: 'Multilevel inverter with the ability of self-voltage balancing', *IEE Proc. Electr. Power Appl.*, 2006, **153**, (1), pp. 105–115
- [17] De, S., Banerjee, D., Siva Kumar, K., et al.: 'Multilevel inverters for low-power application', *IET Power Electron.*, 2011, **4**, (4), pp. 384–392
- [18] Hua, C.-C., Wu, C.-W., Chuang, C.-W.: 'A novel dc voltage charge balance control for cascaded inverters', *IET Power Electron.*, 2009, **2**, (2), pp. 147–155
- [19] Barater, D., Lorenzani, E., Concari, C., et al.: 'Recent advances in single phase transformer-less photovoltaic inverters', *IET Renew. Power Gener.*, 2016, **10**, (2), pp. 260–273
- [20] Pan, C.T., Tu, W.C., Chen, C.H.: 'A novel GZV-based multilevel single phase inverter'. Proc. Taiwan Power Electron Conf., 2010, pp. 1391–1396
- [21] Daher, S., Schmid, J., Antunes, F.L.M.: 'Design and implementation of an asymmetrical multilevel inverter for renewable energy systems'. Proc. COBEP, Recife, Brazil, 2005, pp. 199–204
- [22] Daher, S.: 'Analysis, design and implementation of a high efficiency multilevel converter for renewable energy systems'. PhD. dissertation, Dept. Elec. Eng., Kassel Univ., Kassel, Germany, 2006
- [23] Daher, S., Schmid, J., Antunes, F.L.M.: 'High performance inverter for renewable energy systems', *Rev. Eletrônic. Potência*, 2007, **2**, pp. 253–260
- [24] Najafi, E., Yatim, A.H.M.: 'Design and implementation of a new multilevel inverter topology', *IEEE Trans. Ind. Electron.*, 2012, **59**, (11), pp. 4148–4154
- [25] Alishah, R.S., Nazarpour, D., Hosseini, S.H., et al.: 'New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels', *IET Power Electron.*, 2014, **7**, (1), pp. 96–104
- [26] Liao, Y.-H., Lai, C.M.: 'Newly-constructed simplified single-phase multistring multilevel inverter topology for distributed energy resources', *IEEE Trans. Power Electron.*, 2011, **26**, (9), pp. 2386–2392
- [27] Calais, M., Agelidis, V.G., Dymondc, M.S.: 'A cascaded inverter for transformer-less single-phase grid-connected photovoltaic systems', *Renew. Energy*, 2001, **22**, (1), pp. 255–262
- [28] Stu, G.J.: 'Multilevel DC-link inverter', *IEEE Trans. Ind. Appl.*, 2005, **41**, (3), pp. 848–854
- [29] Babaei, E.: 'A cascade multilevel converter topology with reduced number of switches', *IEEE Trans. Power Electron.*, 2008, **23**, (6), pp. 2657–2664
- [30] Ebrahimi, J., Babaei, E., Gherehpetian, G.B.: 'A new multilevel converter topology with reduced number of power electronic components', *IEEE Trans. Ind. Electron.*, 2012, **59**, (2), pp. 655–667
- [31] Samanbakhsh, R., Taheri, A.: 'Reduction of power electronic components in multilevel converters using new switched capacitor-diode structure', *IEEE Trans. Ind. Electron.*, 2016, **63**, (11), pp. 7204–7214
- [32] Villanueva, E., Correa, P., Rodriguez, J., et al.: 'Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photo voltaic systems', *IEEE Trans. Ind. Electron.*, 2009, **56**, (11), pp. 4399–4406
- [33] Alishah, R.S., Nazarpour, D., Hosseini, S.H., et al.: 'Reduction of power electronic elements in multilevel converters using new cascade structure', *IEEE Trans. Ind. Electron.*, 2015, **62**, (1), pp. 256–267
- [34] Babaei, E., Kangarlu, M.F., Hosseinzadeh, M.A.: 'Asymmetrical multilevel converter topology with reduced number of components', *IET Power Electron.*, 2013, **6**, pp. 1188–1196