Nonlinear Digital PID Controller for DC-DC Converters

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***Abstract*- This paper introduces an approach for the design and implementation of a non-linear digital PID controller. The proposed PID controller includes nonlinear proportional, integral and differential gains that are selected based on the input error signal value to achieve significantly improved dynamic responses. This implementation uses an off-the-shelf digital PWM controller well suited for practical high-frequency SMPS applications. Simulation and experimental results are presented for a point-of-load 12V-to-1V, 40A, 500kHz dual phase synchronous buck converter to verify the improved dynamic performance of the non-linear digital controller.**

I. INTRODUCTION

To comply with today's tight requirement for transient performance of the switched-mode power supplies (SMPS), utilization of nonlinear controllers are inevitable. Nonlinear controllers [1-14] can overcome the transient performance limitations caused by the finite sampling rate, and most importantly, the inherent saturation limits corresponding to the on or off state of the control switch (i.e., the duty cycle is between 0 and 1). In addition to robustness and stability issues, a difficulty that until now has prevented the prevalent use of nonlinear controllers is the controller implementation complexities. Simplicity, flexibility and reliability of digital controllers made them an attractive platform for implementing nonlinear control techniques. Various nonlinear digital techniques have been reported [8-14] to achieve improved transient performance of SMPS. For example a combined linear PID and a nonlinear controller with pre-computed on/off times stored in a look-up-table for a limited set of possible step load transients is described in [11]. The approach presented in [12] also combines a linear PID with a near-time-optimal controller in transients. Based on detecting the valley (or peak) in the output voltage waveform, the on/off control is executed with the times t_{on2}, t_{off} stored in a look-up table. A proximate time-optimal digital controller, which combines a linear PID and a nonlinear switching surface (sliding mode) controller is introduced in [13]. The PID controller operates near a reference point while the nonlinear switching surface is activated in transient. A digital capacitor current estimator is also implemented that enables switching surface operation and eliminates the need for current sensing. All of these digital approaches achieve near-time optimal transient performance. However, stability analysis and robustness study are required for these controllers. Furthermore, using these controllers for a multi-phase application is not a simple task. A simple nonlinear digital PID controller with programmable analog to digital converter (A/D) quantizer is shown in [14]. The controller achieves improved dynamic responses without compromising stability margins, but the effective gain of the A/D is the only programmable section of the controller.

In this paper we introduce a simple, yet effective nonlinear controller, inspired by nonlinear PID technique developed earlier for industrial process control applications [15, 16]. Features of the proposed digital nonlinear PID controller include:

- Improved transient performance, superior compared to standard linear PID control;
- No change in the digital implementation for single or multi-phase applications;
- Standard constant switching frequency, no limit-cycling oscillations.

Section II presents the dual phase buck converter design. The controller design is provided in Section III. Simulation results for dual-phase synchronous buck converter are shown in section IV. Section V gives a stability analysis for the closed loop SMPS with nonlinear controller. Section VI provides experimental results for the digitally controlled two-phase synchronous buck, point-of-load converter.

II. DUAL PHASE BUCK CONVERTER DESIGN

Figure 1 shows the simplified structure of the digitally controlled two-phase synchronous buck converter. To obtain the small-signal model of the power stage, the two-phase synchronous buck converter is modeled with an equivalent one phase synchronous buck converter with the inductor $L_p = L_{p1}/2$ ($L_{p1} = L_{p2}$), phase capacitor $C_p = 2\text{x}C_{p1}$ ($C_{p1} = C_{p2}$), inductor series resistance $R_{Lp} = R_{Lp1} \| R_{Lp2}$, and the phase capacitor series resistance $R_{esrp} = R_{esrp1} \| R_{esrp2}$. The control to

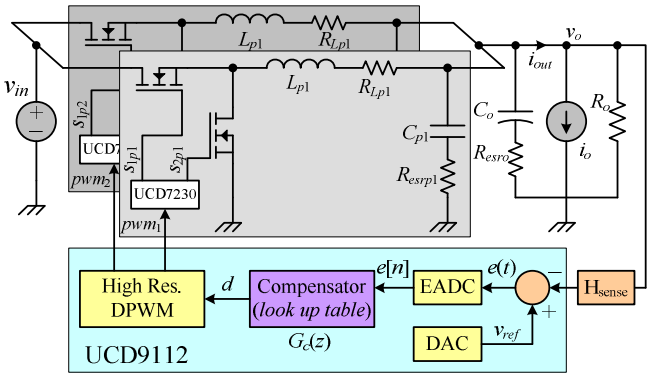

Figure 1. Dual phase synchronous buck converter with digital controller

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output small signal transfer function is obtained using the discrete modeling for DC-DC converters described in [17-19]. The controller is implemented on a programmable digital controller UCD9112 [20] from Texas Instruments. The output voltage is sensed though a sensing block, H_{sense} and is compared with the reference voltage, v_{ref}, generated by the programmable digital to analog converter (DAC). The continuous error signal $e(t)$ is sensed by the window type analog to digital converter, EADC, which generates the discrete error signal $e[n]$. The EADC includes 17 error bins, which are error values between +/–8. The compensator is look-up table based, including three columns corresponding to three different values of present error signal $e[n]$, and previous error signals, $e[n\text{-}1]$, and $e[n\text{-}2]$. The sampling frequency of the EADC and the compensator is the switching frequency f_s. The high resolution DPWM (175 ps resolution) generates two interleaved outputs, pwm_1 and pwm_2 (with 180° phase shift) for the two synchronous buck converters. The gate driver, UCD7230 [21], is used to generate the gate signals for the MOSFET switches.

III. Nonlinear PID Controller

A general nonlinear PID controller has the form of

$$d(\cdot) = K_P(\cdot) + \int K_I(\cdot)dt + K_D\left(\frac{d}{dt}\cdot\right), \quad (1)$$

where $K_P(\cdot)$, $K_I(\cdot)$, and $K_D(\cdot)$ are the proportional, integral and the derivative gains of the controller, respectively. In general, the gains can be functions of input error signal $e(t)$ and are constants in the case of linear controller. The corresponding compensator transfer function for a linear PID is

$$G_c(s) = \frac{d(s)}{e(s)} = K_P + \frac{K_I}{s} + K_D\frac{s}{1+s/\omega_p}, \quad (2)$$

A high frequency pole ω_p, relative to the switching frequency f_s, is added to the differential term to reduce the switching noise. In this design the pole, ω_p, is placed at $f_p = \omega_p/2\pi = f_s/\pi$ [22]. The discrete form of the compensator in (2) is derived using bilinear transformation:

$$s = 2f_s\frac{z-1}{z+1}. \quad (3)$$

Consequently, the discrete time-domain equation for the output of the compensator $G_c(z)$ is obtained as:

$$d[n] = d[n\text{–}1] + b_0e[n] + b_1e[n\text{–}1] + b_2e[n\text{–}2], \quad (3)$$

where, the coefficients b_0, b_1 and b_2 are:

$$b_0 = K_P + K_I/2f_s + K_Df_s,\ b_1 = -K_P + K_I/2f_s - 2K_Df_s,\ \text{and } b_2 = K_Df_s. \quad (4)$$

The digital compensator is implemented in the UCD9112 hardware as a look-up table with three columns of product terms $b_0e[n]$, $b_1e[n\text{–}1]$, and $b_2e[n\text{–}2]$. Therefore, by defining the nonlinear gains, $K_P(e)$, $K_I(e)$, and $K_D(e)$, the nonlinear coefficients $b_0(e)$, $b_1(e)$, and $b_2(e)$ can be found and programmed in the digital controller.

III.A. Proportional gain $K_P(\cdot)$

In (1), the proportional term, makes the controller to respond to instantaneous input error signal, while the integral and derivative terms help to eliminate the steady state error and improve damping of the system respectively. In a traditional linear PID controller, increasing the integral gain $K_I(\cdot)$ in (1), increases the total gain of the compensator and thus the bandwidth of the closed loop system. The disadvantage of the integral term is its phase lag, which reduces the phase margin. Furthermore increasing the integral gain increases its windup problem. Therefore, a nonlinear proportional gain of

$$K_P(e(t)) = \begin{cases} K_{Pl}|e|^{\alpha-1}, & |e| > b \\ K_{pt}, & b > |e| > a \\ K_{Pl}, & |e| < a \end{cases}, \quad (5)$$

Where, $e = v_{ref} - v_o \cdot H_{sense}$, is selected to increase the total gain of the controller using the proportional term, and to decrease the role of the integral gain $K_I(\cdot)$. In (5) K_{Pl} is the proportional gain obtained from the linear PID controller design. The value of α is between 0 and 1. For $\alpha = 0$, the proportional term represents hysteretic control and for $\alpha = 1$, it represents a linear proportional control. For the error signals larger than the threshold value of b, the proportional gain increases by the factor of $|e|^{\alpha-1}$ (e is a normalized value between +/– 1). Around steady state operation, where the input error signal is less than the threshold value of a, the proportional gain is held at it's original linear value to maintain the stability criteria in steady state and reduce the sensitivity of the system to the high frequency noise. A smooth transition, K_{pt}, connects the proportional gain between the two threshold points of a, and b. However, at the large values of $|e|$ the gain rolls-off to eliminate the windup problem because of the inherent saturation in the PWM modulator.

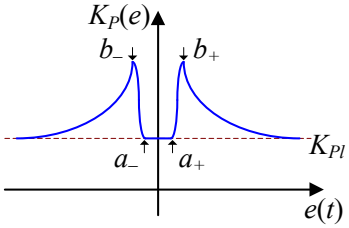

Figure 2. Nonlinear proportional gain

Figure 3 shows the proportional effort of the compensator versus input error signal. The proportional effort is defined as:

$$U_p(e) = K_P(e)\cdot e \quad (6)$$

It is shown that the linear proportional effort, U_{Pl}, (green solid line) is linear (K_P is constant). The nonlinear proportional effort U_{PNlin} (red solid line) is initially equivalent to U_{Pl} around zero error and increases in value for error values between a and 1. It is shown that the proportional effort $U_{PNlin} = U_{Pl}$ at $e = 1$.

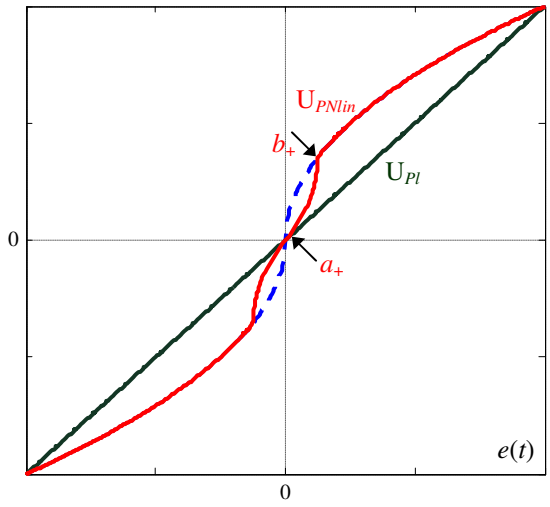

Figure 3. Proportional effort U_P

III.B. Integral gain $K_I(\cdot)$

The integral gain is applied only in the region of steady state operation. This reduces the saturation and phase lag problem and help maintains zero steady state error without requiring a large proportional gain at small error values. Therefore, the integral gain is defined as:

$$K_I(e(t)) = \begin{cases} K_{I\min}, & |e| > b \\ K_{It}, & b > |e| > a \\ K_{Il}, & |e| < a \end{cases}, \qquad (7)$$

Close to steady state point ($|e| < a$), the integral gain is similar to the designed value using a linear PID approach. For error values away from the steady state ($|e| > b$), the integral gain is set to a very low value. During large transient the proportional gain might not be large enough to force the error value close to zero. Therefore, it is important to have a small, non-zero integral gain away from the steady state point. A smooth transition, K_{It}, connects the integral gain between the two threshold points of a, and b. Figure 4 shows the nonlinear integral gain versus input error signal.

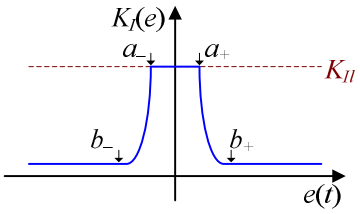

Figure 4. Nonlinear integral gain

III.C. Differential gain $K_D(\cdot)$

The differential term improves the transient performance by increasing the phase margin. However, in the region of steady state where the error signal is close to zero, the differential term is dominated by the noise in the system. The differential gain is set very similar to the proportional gain, (except that in steady state it can be set to a value less than the linear design value of K_{Dl}).

$$K_D(e(t)) = \begin{cases} K_{D\max}, & |e| > b \\ K_{Dt}, & b > |e| > a \\ K_{D\min}, & |e| < a \end{cases}. \qquad (8)$$

In equation (8) K_{Dl} is the differential gain obtained from the linear PID controller design. For the error signals smaller than the threshold value of a, the differential gain is set to a minimum value of K_{Dmin} to minimize noise amplification. For the error values larger than the threshold value of b, the differential gain is set to K_{Dmax} to maintain reasonable damping and phase margin. Figure 5 shows the nonlinear differential gain K_D.

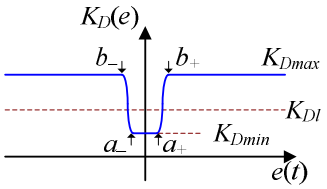

Figure 5. Nonlinear differential gain

It is important to note that the threshold values of a and b are not necessarily the same for the nonlinear proportional, integral and differential terms.

IV. Simulation Results for Dual-Phase Synchronous Buck Converter

A dual phase synchronous buck converter is designed with: $L_p = L_{p1}/2 = L_{p2}/2 = 0.24\ \mu$H, $R_{Lp}=R_{Lp1}/2=R_{Lp2}/2 = 2.4$ mΩ, $C_p=2C_{p1}=2C_{p2}= 376\ \mu$F, $C_o = 2000\ \mu$F, $R_{esro} = 1$ mΩ, $R_{esrp}=R_{esrp1}/2=R_{esrp2}/2 = 0.6$ mΩ, $V_{in} = 12$ V, $V_{ref} = 1$ V, $f_s = 500$ KHz. The error ADC has the quantization value of $q_{AD} = 5$ mV. The DPWM resolution is 175 ps. The linear PID controller is designed according [26] to provide minimum closed-loop output impedance magnitude while GM > 10 dB. The resulting linear PID controller provides a loop-gain with bandwidth of $f_c = 45$ kHz and phase margin of $\phi_m = 65^o$. Figure 6 shows the magnitude and phase Bode plot of the control to output transfer function and the loop gain using linear PID controller. The switching power supply and the DPWM are directly modeled in discrete domain according to [17].

The threshold error values for the nonlinear PID controller is selected as $a_P = a_I = a_D = 2q_{AD} = 10$ mV, and $b_P = b_I = b_D = 3q_{AD} = 15$ mV. The differential gains are selected such that: $K_{Dmin} = 1\text{x}K_{Dl}$, and $K_{Dmax} = 2\text{x}K_{Dl}$. The value α is set to be $\alpha = 0.5$. The integral gain is set as $K_{Imin} = 0.1\text{x}K_{Il}$.

Figure 7 shows simulation results for the 8 to 30 A load transient in a synchronous buck converter equivalent with the dual phase synchronous buck converter. The i_{Ltot} is the sum of the two phase inductor currents. The results are illustrated for the two cases of linear and nonlinear digital PID controller.

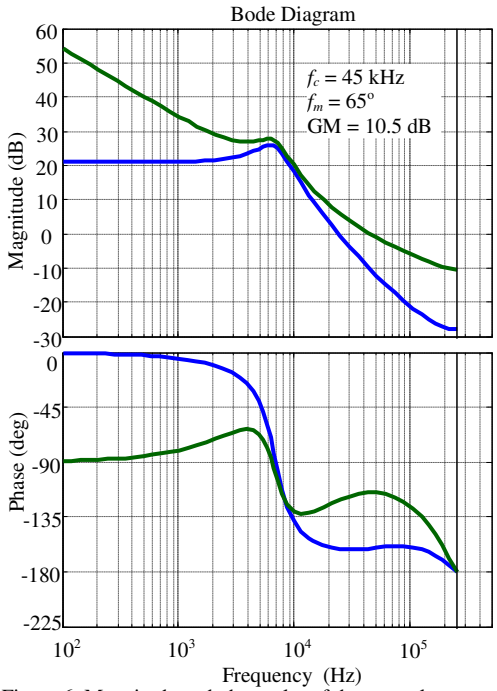

Figure 6. Magnitude and phase plot of the control to output transfer function G_{vdz} (blue) and the loop-gain (green)

It is shown that the nonlinear PID controller improves the load transient performance significantly. It is shown that during transient the increase in proportional gain $K_P(\cdot)$ decreases the undershoot, while decreasing the integral gain decreases the settling time. Furthermore, reducing the integral gain also decreases the chance of limit-cycling oscillation [23].

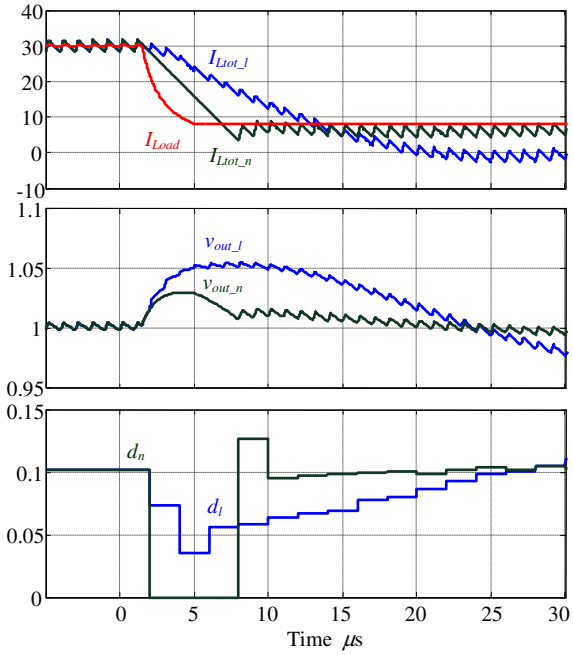

Figure 7. Comparison of linear and nonlinear digital PID controller for load transient of 8 to 30 A

V. Stability

The stability of the closed loop system including nonlinear PID controller is studied in this section. The closed loop system is assumed to be linear around any single error value of $e = V_{ref} - v_{out}.H_{sense}$. For any single error e the nonlinear proportional, differential and integral gains are known, and as a result the corresponding linear compensator $G_c(s)$ and $G_c(z)$ and the loop-gain can be obtained.

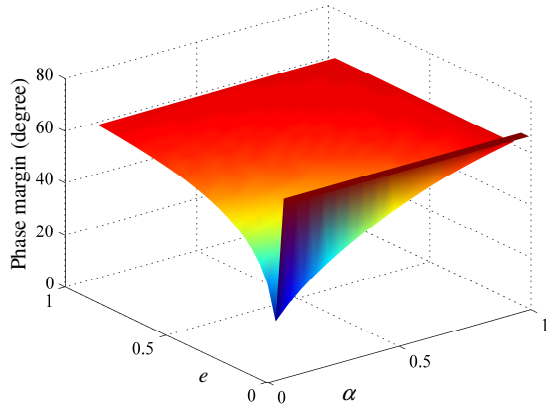

Figure 8. Phase margin versus error e and α

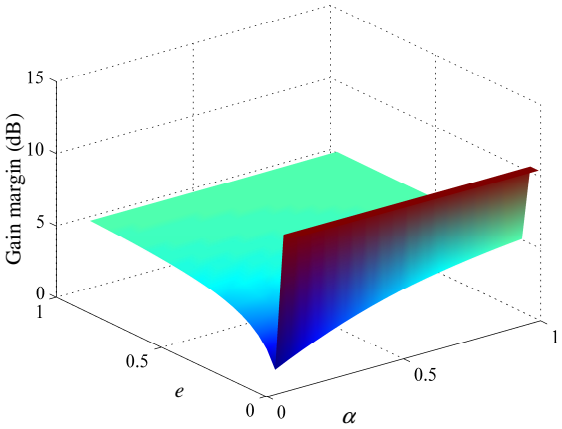

Figure 9. Gain margin versus error e and α

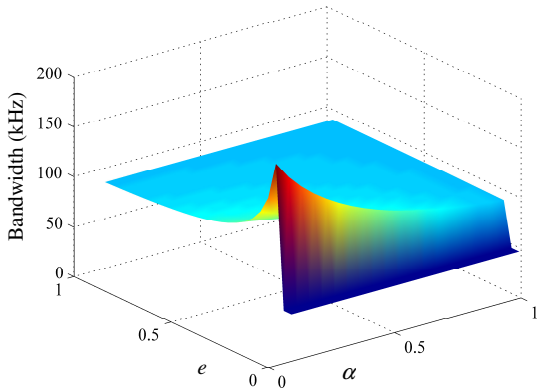

Figure 10. Bandwidth versus error e and α

Figure 8, 9, and 10 show the phase margin, gain margin and the resulting bandwidth of the loop-gain obtained from the dual phase synchronous buck converter and the nonlinear gains described in Section IV. It is shown that for small error

values the gain/phase margin and the bandwidth is similar to what is shown in Fig. 6. It is also observed that for the entire range of error value e and the nonlinear part of $K_P(.)$, α, the system is stable ($\phi_m > 45^o$, and GM > 4dB). It is interesting to note that for large error values of e, the equivalent bandwidth of the closed loop system increases to 90 kHz. This increase in the equivalent bandwidth is the main reason for the better load transient performance.

VI. Experimental results

An experimental dual phase synchronous buck converter was designed with the parameters given in Section II. The pre-computed values of $b_0e[n]$, $b_1e[n–1]$, and $b_2e[n–2]$ are stored in a lookup table in UCD9112 for different quantized error values. Figure 11 and 12 show the 10-to-30A load transient response with linear and nonlinear PID controller, respectively. The response with the linear PID controller has the undershoot of $\Delta V_{out} > 44$ mV and a settling time of $t_{settle} > 50$ μs, while the response with the nonlinear PID controller has the values of $\Delta V_{out} < 26$ mV and a settling time of $t_{settle} < 22$ μs. It is shown that the nonlinear PID improves the transient performance significantly.

The difference between simulation and experimental results are because of different load step rate applied to the output.

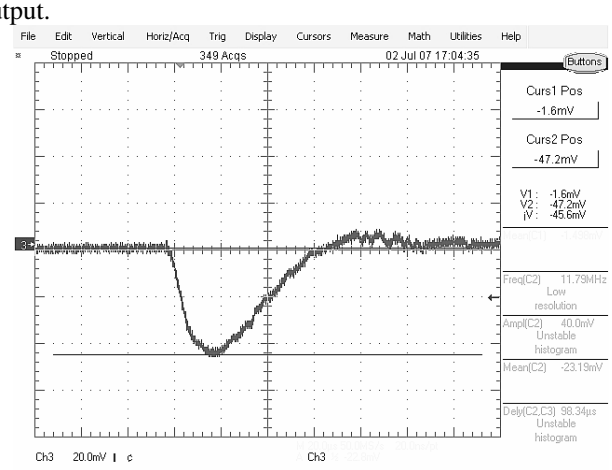

Figure 11. Load transient response with linear PID

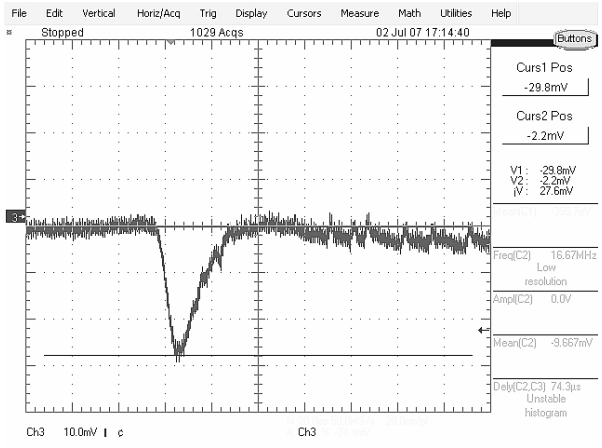

Figure 12. Load transient response with nonlinear PID

VII. Conclusion

This paper presents a simple method for design and implementation of a non-linear PID controller. It is shown that the proportional, integral and differential gains of a PID controller can be selected based on the input error signal value to achieve significantly improved dynamic response. The implementation includes a look-up table based digital compensator which is well suited for practical high-frequency SMPS controllers [24, 25]. Simulation and experimental results are presented for a 40A, 12V-to-1V point-of-load, dual phase, synchronous buck converter to show the improved load transient responses under non-linear control.

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