David Gao

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Education

University of Waterloo — Waterloo, ON
Bachelor of Applied Science in Electrical Engineering — *Sep. 2023 – Present*

Technical Skills

Tools: Quartus/Vivado, VCSMX, DVE, Verdi **Languages**: System/Verilog, C/C++, Bash, Tcl, Python, Perl

Experience

SoC Engineering Intern — Jan. 2026 - Present
Arm — *Toronto, ON*

- Improve scripts parsing **AMBA AXI** and **CHI** performance testing traces by switching to hashmaps from arrays, resulting in a 64x reduction in memory and 28x speedup
- Maintained SystemVerilog testbenches for **multi-die** performance verification of **Ethernet** and **PCIe** datapaths

Digital Design Engineering Intern — May – Aug. 2025
Altera — *Toronto, ON*

- Designed and **testbenched** a frequency checker module in **SystemVerilog** using **VCSMX**, implemented **CDC-safe** handshaking for a bus synchronizer, achieving clean **STA** closure by applying comprehensive **SDC** constraints, ensuring proper clock programming for **dynamic reconfiguration of 50G+ transceiver IP**
- Collaborated with the transceiver firmware team to resolve critical **SERDES** issues to deliver product on time
- Implemented a **MAC** and optimized counters, **FIFOs**, adders, and **priority muxes** using **pipelining**, carry-select logic, 3:2 compressors, and recursion to improve LUT usage and fMAX during an optimization bootcamp
- Migrated cron job-based test automation to a scalable weekly testing framework using Perl

Graphics Hardware Engineering Intern — Sep. – Dec. 2024
Intel — *Toronto, ON*

- Designed a **4-layer** dual mode HDMI-DisplayPort switcher PCB controlled by a ATmega32u4, with impedance matched traces to ensure **signal integrity** and reducing **crosstalk**, enabling automated remote testing.
- Diagnosed and resolved hardware and software bugs by conducting hands-on lab debugging and experiments, utilizing tools such as **multimeters, WinDbg, and oscilloscopes** to track, triage, and identify root causes.
- Debugged GDDR6 memory **signal integrity** issues through sweeping through different memory corners and running shmoo **eye diagrams** to minimize **BER** in data center **GPUs** with Python test cases.
- Executed powercycle and **PCIe** test plans to confirm platform functionality across a 20+ host motherboards.

Research and Projects

FPGA Research Assistant | *University of Waterloo*

- Working with **Dr. Mina Arashloo** to build a protocol-agnostic transport-layer FPGA accelerator on Alveo U250
- Designed rate-variable FIFO for use in DCQCN algorithm to enable **RoCEV2** on accelerator platform

Optical Research Assistant | *University of Waterloo*

- Assisted hardware bringup of multi-digitizer card system to enable higher bandwidth of imaging information to enable molecular differentiation as a part of research with **Photomedicine Labs and Dr. Parsin Haji Reza**

SRAM Precharge and Equalization | *SPICE*

- Designed SRAM precharge and equalization circuitry on **SkyWater 130nm** process node, and ran **Monte Carlo** simulations to ensure non-destructive reads and writes

Analog IC Design Engineer | *UWASIC*

- Designed **8-bit segmented DAC** for analog Matrix-Vector Multiplier, and ran Monte Carlo simulations to ensure design robustness, characterizing INL, DNL and PVT variations

SoC Engineer | *UW Reality Labs*

- Architecting an SoC integrating an ORB vision accelerator with IMU tagging to enable real-time SLAM on CPU

Macropad | *KiCAD, C, ATmega2U4, QMK*

- Used **KiCAD** and **C** to design and program double layered circuit board for a fully programmable reduced-sized keyboard enabling on-the-spot programming of keys.