Faculty of Engineering, Mathematics and Science

School of Computer Science and Statistics

BA (Mod.) Computer Science **Hilary Term 2016**
Year 3

CS3021 Computer Architecture II

13 January 2016 **Exam Hall** **9:30 – 11:30**

Dr Jeremy Jones

Instructions to Candidates:

Answer **THREE** questions.
All questions carry equal marks
All questions are marked out of 20

Q1. Briefly describe the IA32 and x64 procedure calling conventions. Draw diagrams of the typical procedure stack frames. Make sure that you describe the register set, the volatile registers, how parameters and local variables are allocated and accessed and, in the case of the x64 calling convention, the use of *shadow space.*

[8 Marks]

What are the main advantages of the x64 procedure calling convention compared with that of the IA32?

[2 marks]

Convert the follow code segment into IA32 and x64 assembly language Assume int is 32 bits for IA32 and 64 bits for x64.

```
int fx(int n)
{
    int i = 0;
    while (n) {
        n >>= 1;
        ++ i;
    }
    return i - 1;
}
fx(1048576);
```

[5 + 5 marks]

Q2. Explain the operation of the RISC I register windows and explain how its design strives to achieve a single cycle procedure call and return. Use diagrams to illustrate your answer.

[6 marks]

Why is a register window overflow and underflow mechanism needed? Explain in detail the conditions under which register window underflow and overflow occur and the steps taken to resolve them.

[6 marks]

Consider the following ackermann function.

```
int ackermann(int x, int y)
{
    if (x == 0) {
        return y+1;
    } else if (y == 0) {
        return ackermann(x-1, 1);
    } else {
        return ackermann(x-1, ackermann(x, y-1));
    }
}
```

Add code to the function to determine the number of register window overflows and underflows that would occur if it is executed by a RISC I microprocessor with N register windows.

[8 marks]

Q3. What is a cache? How does a cache reduce the effective memory access time?

[1 marks]

With the aid of diagrams, explain how a cache organisation can be characterised by the three constants LKN. Show in detail how a data item is accessed in a LKN cache.

[6 marks]

Compute the number of hits and misses if the following list of addresses (in hexadecimal) is applied to (a) a 128 byte direct mapped cache with 16 bytes per line and (b) a 128 byte 2-way set associative a cache with 16 bytes per line.

0x0000, 0x0040, 0x0008, 0x0040, 0x00c0, 0x0044, 0x0004, 0x0024,
0x0000, 0x00a0, 0x0000, 0x0040, 0x0000, 0x0020, 0x0080, 0x00a0

Assume (1) the low 4 address bits are used as an offset into the cache line and the next log2(N) address bits select the set (2) all cache lines are initially invalid and (3) a LRU replacement policy.

[8 marks]

IA32 CPUs often maintain the tags in a set in pseudo least recently used order. Explain how this is achieved using K-1 bits per set. If K = 4 and the tags are accessed in following order 1, 2, 0, 1 and 3, which tag is considered to be the pseudo least recently used (assume that the K-1 bits are initially 0)?

[5 marks]

Q4. What is the cache coherency problem? Briefly explain the states and operation of the Write-Once and MESI cache coherency protocols.

(8 marks)

Consider a three CPU multiprocessor system where each CPU has its own cache. Each cache is direct mapped with 2 sets. Even addresses (a0, a2) map to set 0 and odd addresses (a1, a3) map to set 1. The caches are initially empty. Explain in detail the bus traffic and cache line state transitions that occur when the following sequence of "memory" accesses are made by the specified CPU if (1) a Write-Once and (2) a MESI protocol is used.

CPU 0: read a2
CPU 0: write a2
CPU 0: write a2
CPU 1: read a2
CPU 1: read a0
CPU 0: write a2
CPU 0: write a2

[10 marks]

What major advantage does the MESI protocol have over the Write-Once protocol?

[2 marks]