UNIVERSITY OF DUBLIN

TRINITY COLLEGE

Faculty of Engineering and Systems Sciences
Department of Computer Science

Integrated Computer Science
Year 3 Annual Examinations

Hilary Term 2015

CS3021 – Computer Architecture II

Tuesday 6th January **Luce Upper** **9.30-11.30**

Dr Jeremy Jones

Instructions to Candidates:

Answer **THREE** questions.

Q1. Briefly explain how the RISC-1 microprocessor attempts to achieve a single cycle procedure call and a single cycle return from procedure. Compare the RISC-1 approach with that of the IA32 CPU. Use diagrams to illustrate your answer.

[8 marks]

Convert the follow code segment into RISC-1 and IA32 assembly language.

```
int gcd(a, b)
{
   while (a != b {
      if (a > b) {
         a = a – b;
      } else {
         b = b – a;
      }
   }
   return a;
}

gcd(14, 21);
```

[6 + 6 marks]

Q2. What is a pipelined processor? What are the benefits of pipelining? Explain the organization and operation of the DLX five stage execution pipeline.

[4 marks]

What are data hazards? Describe two techniques (which prevent stalls) that can be used to overcome data hazards in the DLX pipeline. Show, using diagrams, how the data hazards in the following code sequence are overcome by the DLX CPU.

1. r1 ← r2 + r3
2. r4 ← r1 + r1
3. r10 ← r1 + r4
4. r11 ← r4 + r1

[10 marks]

What is a load hazard? Describe a technique that can be used to avoid load hazards. Show how the load hazards in the following code sequence can be overcome when executed by the DLX CPU (assume a, b, c, d, e and f are memory locations).

1. a ← b + c
2. d ← a – e + f

[6 marks]

Q3. What is a cache? How does a cache reduce the effective memory access time?

[1 marks]

With the aid of diagrams, explain how a cache organisation can be characterised by the three constants LKN. Show in detail how a data item is accessed in an LKN cache.

[6 marks]

Compute the number of hits and misses if the following list of addresses (in hexadecimal) is applied to (a) a 128 byte direct mapped cache with 16 bytes per line and (b) a 128 byte 4-way set associative a cache with 16 bytes per line.

0x0000, 0x0004, 0x0080, 0x0008, 0x0084, 0x0090, 0x008C, 0x0094, 0x0000, 0x0060, 0x0000, 0x0040, 0x0000, 0x0020, 0x0080, 0x0060

Assume (i) that the lower 4 bits are used as the offset into the cache line and the next $\log_2(N)$ bits select the set; (ii) all cache lines are initially empty/invalid and (iii) a LRU replacement policy.

[8 marks]

IA32 CPUs often maintain the tags in a set in pseudo least recently used order. Explain how this is achieved using K-1 bits per set. If K = 4 and the tags are accessed in following order 1, 2, 0, 1 and 3, which tag is considered to be the pseudo least recently used (assume that the K-1 bits are initially 0).

[5 marks]

Q4. What is the cache coherency problem? Briefly explain the states and operation of the Write Once cache coherency protocol.

[6 marks]

Consider a three CPU multiprocessor system where each CPU has its own cache. Each cache is direct mapped with 2 sets - even addresses map to set 0 and odd addresses map to set 1. The caches are initially empty. Explain in detail what happens when each of the following "memory" accesses are made by the CPUs (e.g. bus traffic and state transitions).

t	CPU 0	CPU 1	CPU 2
0	read a0		
1	read a0		
2		read a0	
3		write a0	
4			read a0
5			write a0
6	write a0		
7	read a0		
8		read a0	
9	write a0		
10		write a0	

[10 marks]

Assuming the multiprocessor described above, imagine that each CPU can execute a tight loop which continuously increments a shared variable *v*. Comment on the rate at which *v* is incremented if 1, 2, or 3 CPUs are concurrently executing the loop. Assume a round robin bus arbiter.

[4 marks]