Coláiste na Tríonóide, Baile Átha Cliath
Trinity College Dublin
Ollscoil Átha Cliath | The University of Dublin

Faculty of Engineering, Mathematics and Science

School of Computer Science & Statistics

Integrated Computer Science **Trinity Term 2017**
Year 2 Annual Examinations
Integrated Engineering
Year 3 Annual Examinations

CS2022 – Computer Architecture I

Tuesday 09th May 2017 **RDS Main Hall** **09.30 – 11.30**

Dr. Michael Manzke

Instructions to Candidates:

Attempt **three** questions. All questions carry equal marks. Each question is scored out of a total of 20 marks.

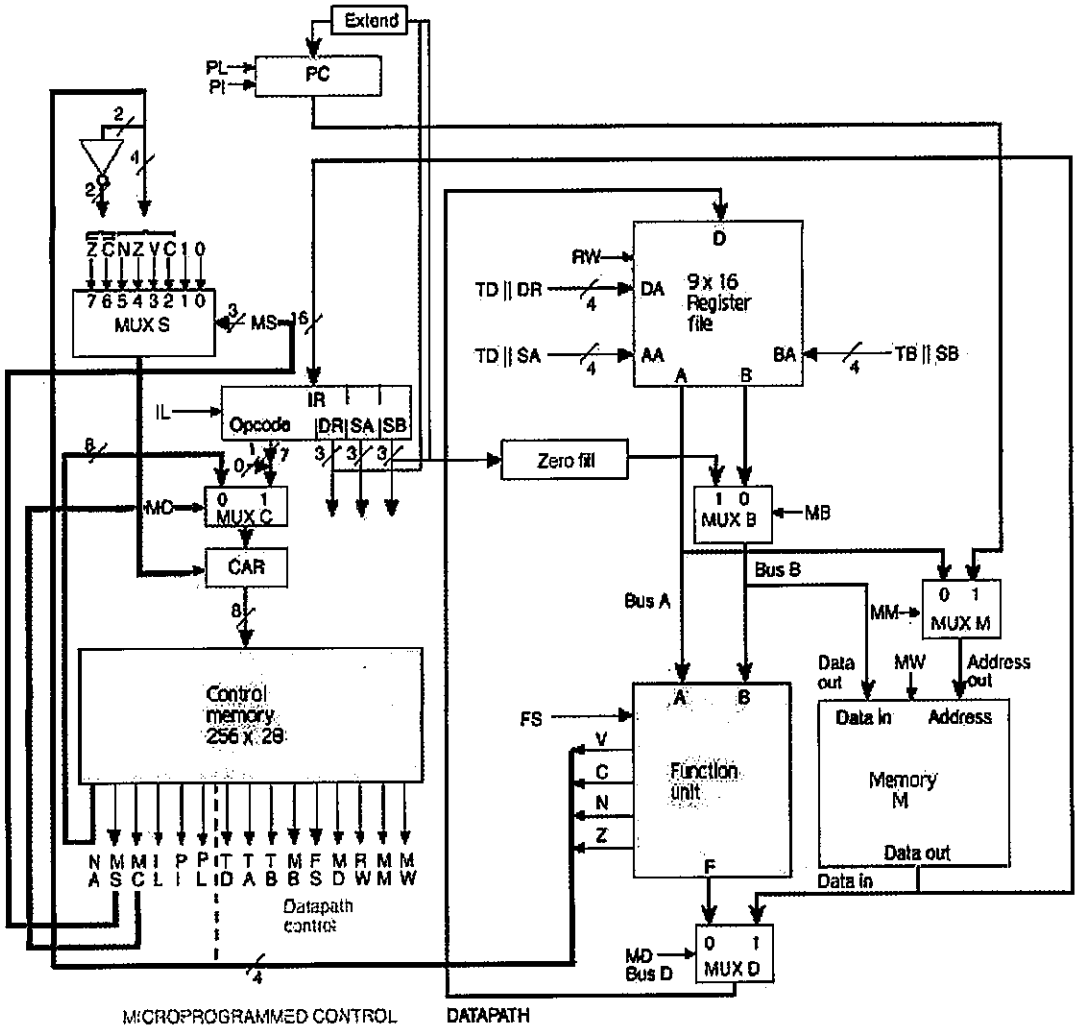
You may not start this examination until you are instructed to do so by the invigilator.

Materials Permitted for this examination:

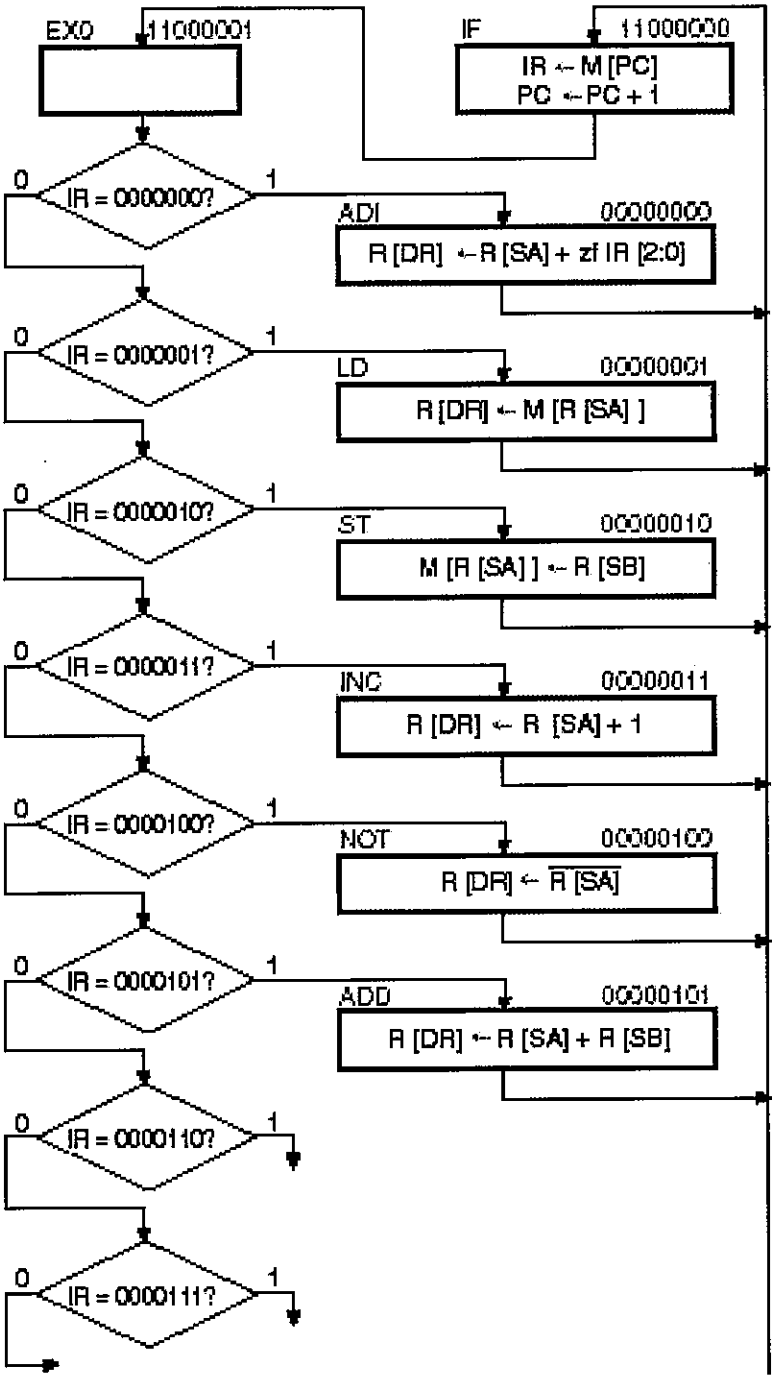
Non-programmable calculators are permitted for this examination – please indicate the make and model of your calculator on each answer book used.

1. (a) Explain in detail the operations that take place when the following multiple cycle microprogrammed instruction set processor executes machine instructions. Your explanation must include operations in the processor's control e.g. how does one instruction in the IR register execute several control words in the Control Memory.

[13 marks]



(b) Provide micro code for the following instructions.



[7 marks]

2. (a) Provide a detailed schematic for a *Function Unit* that implements the following *micro-operations*:

[15 marks]

Table 1: FS code definition

FS	Micro-operation
00000	$F = A$
00001	$F = A + 1$
00010	$F = A + B$
00011	$F = A + B + 1$
00100	$F = A + \bar{B}$
00101	$F = A + \bar{B} + 1$
00110	$F = A - 1$
00111	$F = A$
01000	$F = A \wedge B$
01010	$F = A \vee B$
01100	$F = A \oplus B$
01110	$F = \bar{A}$
10000	$F = B$
10100	$F = srB$
11000	$F = slB$

(b) What do the following Boolean Expressions implement? Please provide a detailed discussion. How would you implement C8?

Ci+1 = gi + piCi

C1 = x0y0 + C0(x0 +y0)

= g0 + C0p0

C2 = x1y1 + C1(x1 +y1)

= x1y1 + [x0y0 + C0(x0 +y0)](x1 +y1)

= g1 + p1g0 + p0p1C0

C3 = g2 + p2g1 + p1p2g0 + p0p1p2C0

C4 = g3 + p3g2 + p2p3g1 + p1p2p3g0 + p0p1p2p3C0

[5 marks]

3. (a) Provide a schematic for a Binary Multiplier data path that can execute the following computation. Why is it possible to perform this operation with a 5 bit adder?

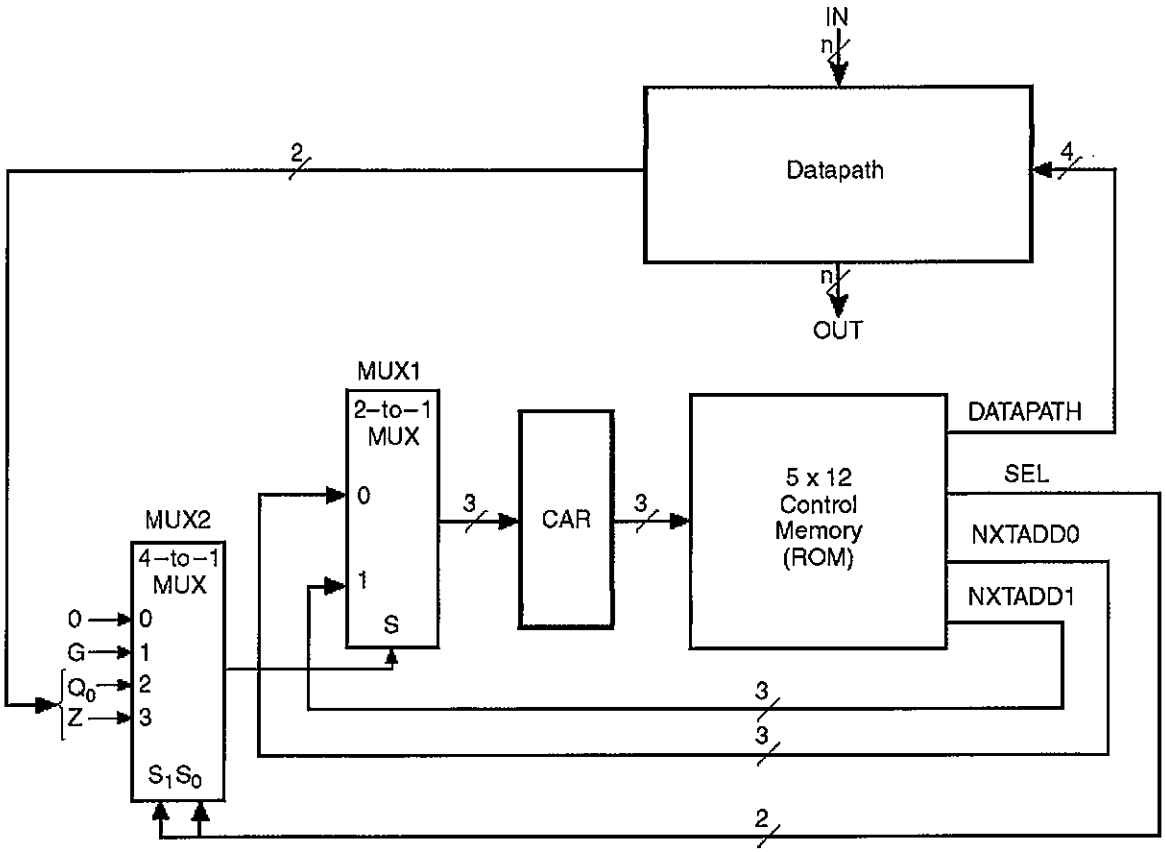
23	10111	Multiplicand
19	10011	Multiplier
	00000	Initial partial product
	10111	Add multiplicand, since multiplier bit is 1
	10111	Partial product after add and before shift
	010111	Partial product after shift
	10111	Add multiplicand, since multiplier bit is 1
	1000101	Partial product after add and before shift[a]
	1000101	Partial product after shift
	01000101	Partial product after shift
	001000101	Partial product after shift
	10111	Add multiplicand, since multiplier bit is 1
	110110101	Partial product after add and before shift
437	0110110101	Product after final shift

[10 marks]

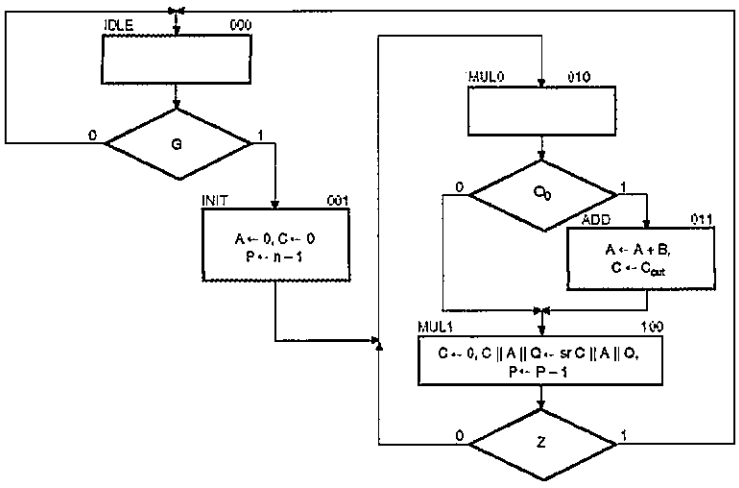
(b) Provide a control schematic for the above Binary Multiplier data path with a Sequence Register and Decoder control unit.

[10 marks]

4. (a) Provide micro-code for the following Microprogrammed Control Unit. This unit controls a Binary Multiplier.

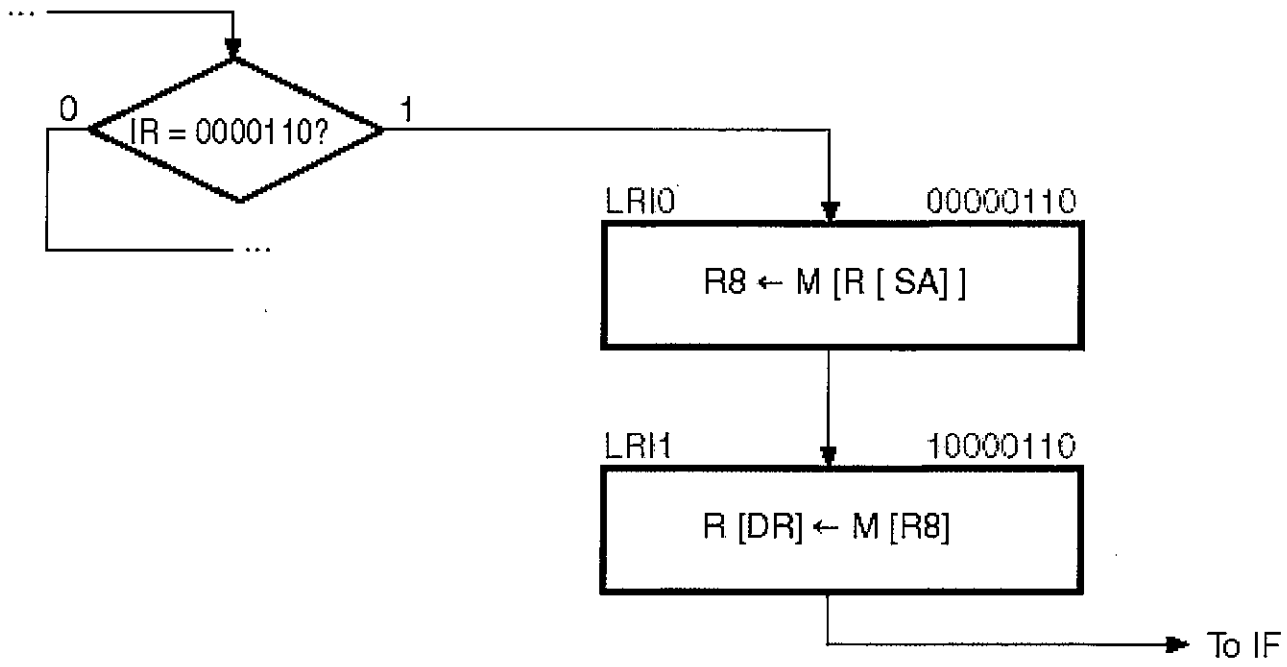


Control Signal	Register Transfers	States in Which Signal is Active	Micro-instruction Bit Position	Symbolic Notation
Initialize	$A \leftarrow 0, P \leftarrow n-1$	INIT	0	IT
Load	$A \leftarrow A+B, C \leftarrow C_{out}$	ADD	1	LD
Clear_C	$C \leftarrow 0$	INIT, MUL1	2	CC
Shift_dec	$C\|A\|Q \leftarrow \text{sr } C\|A\|Q, P \leftarrow P-1$	MUL1	3	SD



[15 marks]

(b) The following ASM defines an instruction for our microprogrammed multiple cycle instruction set processor. What instruction does the ASM describe?



[5 marks]