Coláiste na Tríonóide, Baile Átha Cliath
Trinity College Dublin
Ollscoil Átha Cliath | The University of Dublin

Faculty of Engineering, Mathematics and Science

School of Computer Science & Statistics

Integrated Computer Science Programme **Trinity Term 2018**
Year 2 Annual Examinations
Integrated Engineering Programme
Year 3 Annual Examinations

CS2022 – Computer Architecture I

Friday 4th May 2018 **Exam Hall** **09.30 – 11.30**

Dr. Michael Manzke

Instructions to Candidates:

Attempt **three** questions. All questions carry equal marks. Each question is scored out of a total of 20 marks.

You may not start this examination until you are instructed to do so by the invigilator.

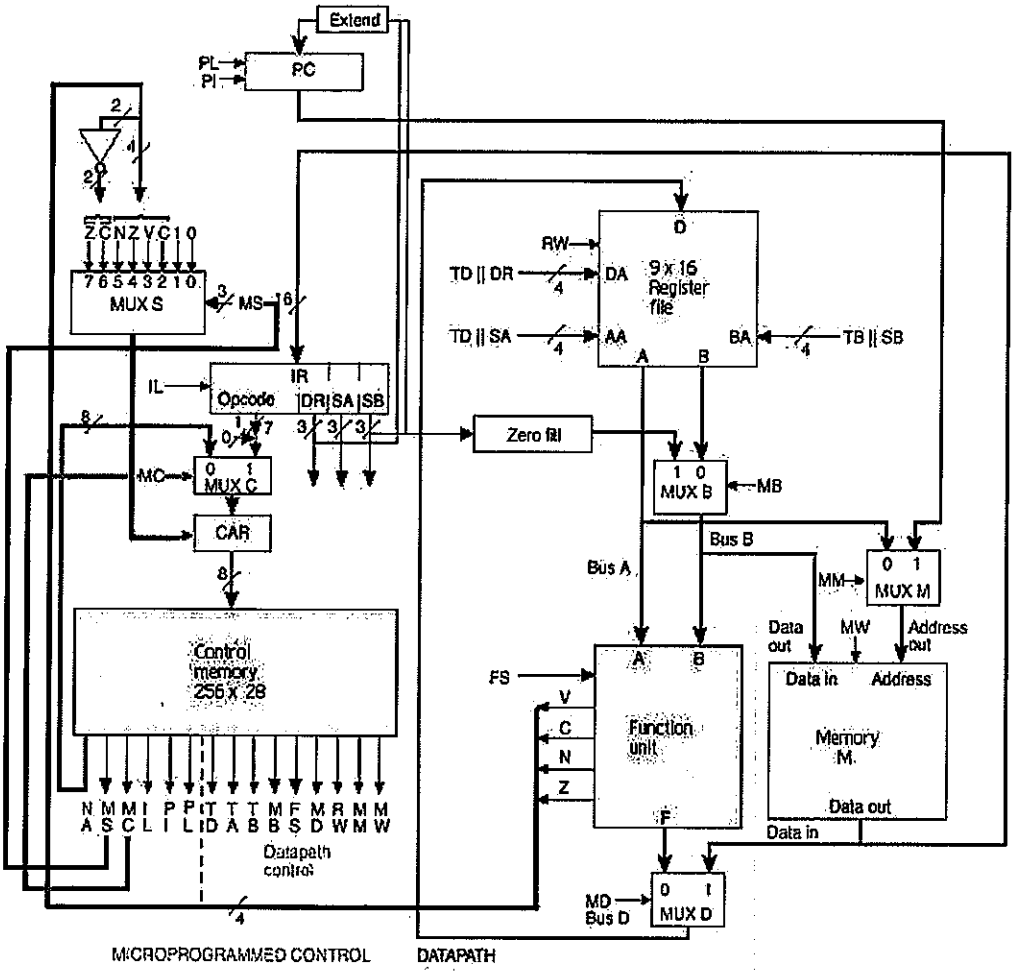
Exam Paper is not to be removed from the venue

Materials Permitted for this examination:

Non-programmable calculators are permitted for this examination – please indicate the make and model of your calculator on each answer book used.

1. (a) Explain in detail the operations that take place when the following multiple cycle microprogrammed instruction set processor executes machine instructions. Your explanation must include operations in the processor's control e.g. how does one instruction in the IR register execute several control words in the Control Memory.

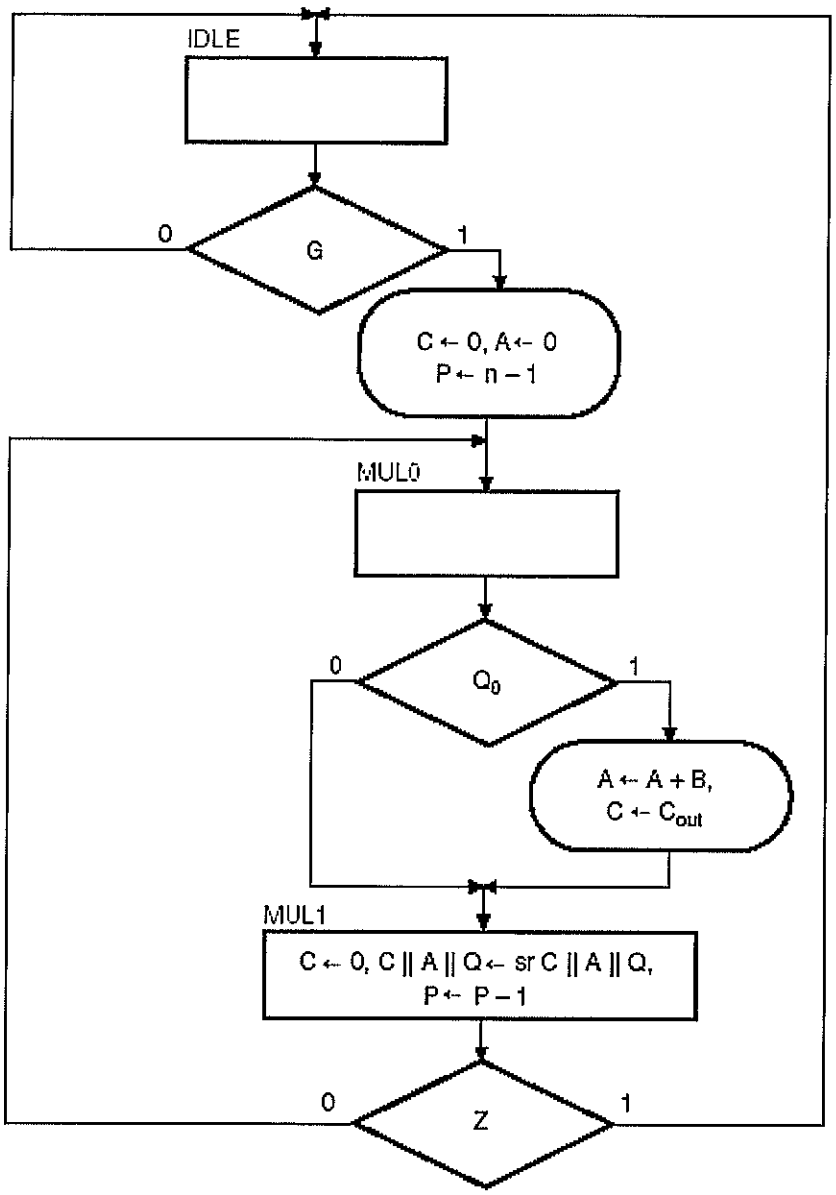
[15 marks]



(b) How would you implement the PC and CAR?

[5 marks]

2. The following Algorithmic *State Machine* (ASM) chart shows the operations of a *Binary Multiplier*.



a) Provide an example (multiply two binary numbers) that explains the operations of the *Binary Multiplier*.

[8 marks]

(Question 2 continues on next page)

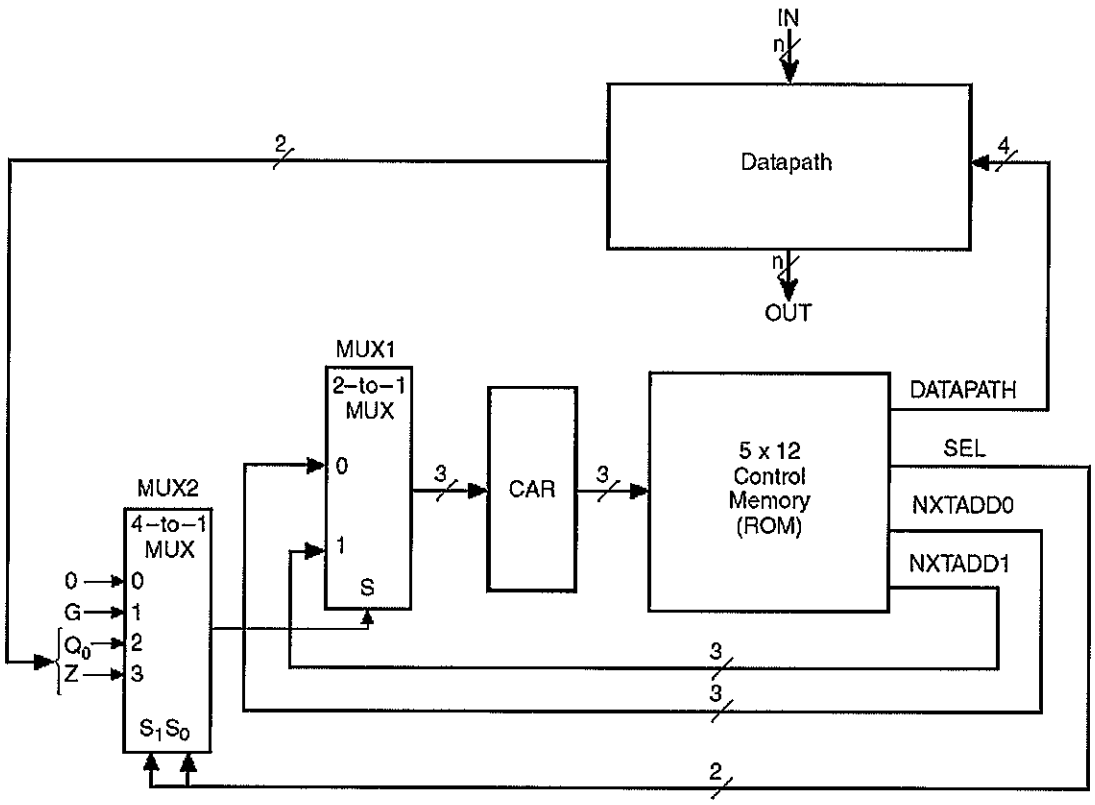
(Question 2 continued from previous page)

b) Write VHDL code that implements the *Binary Multiplier* by providing the following VHDL processes:

- A process that moves the ASM to the next state
- A process that determens the next state
- A process that executes the required register transfer operations for the current state

[12 marks]

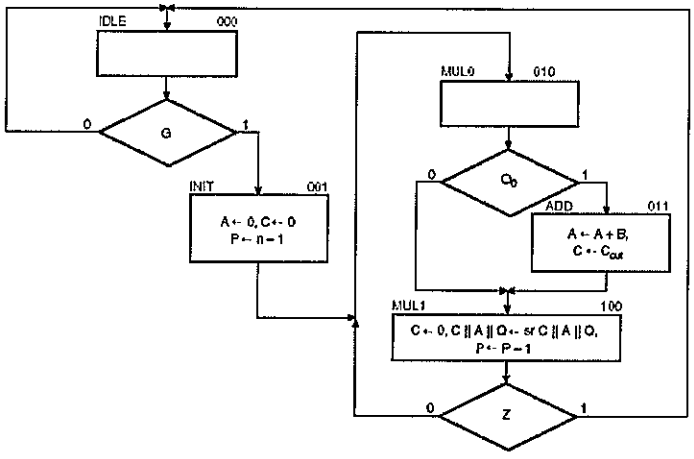
3. (a) Provide micro-code for the following Microprogrammed Control Unit. This unit controls a Binary Multiplier.



(Question 3 continues on next page)

(Question 3 continued from previous page)

Control Signal	Register Transfers	States in Which Signal is Active	Micro-instruction Bit Position	Symbolic Notation
Initialize	$A \leftarrow 0, P \leftarrow n-1$	INIT	0	IT
Load	$A \leftarrow A+B, C \leftarrow C_{out}$	ADD	1	LD
Clear_C	$C \leftarrow 0$	INIT, MUL1	2	CC
Shift_dec	$C \| A \| Q \leftarrow \text{sr } C \| A \| Q, P \leftarrow P-1$	MUL1	3	SD

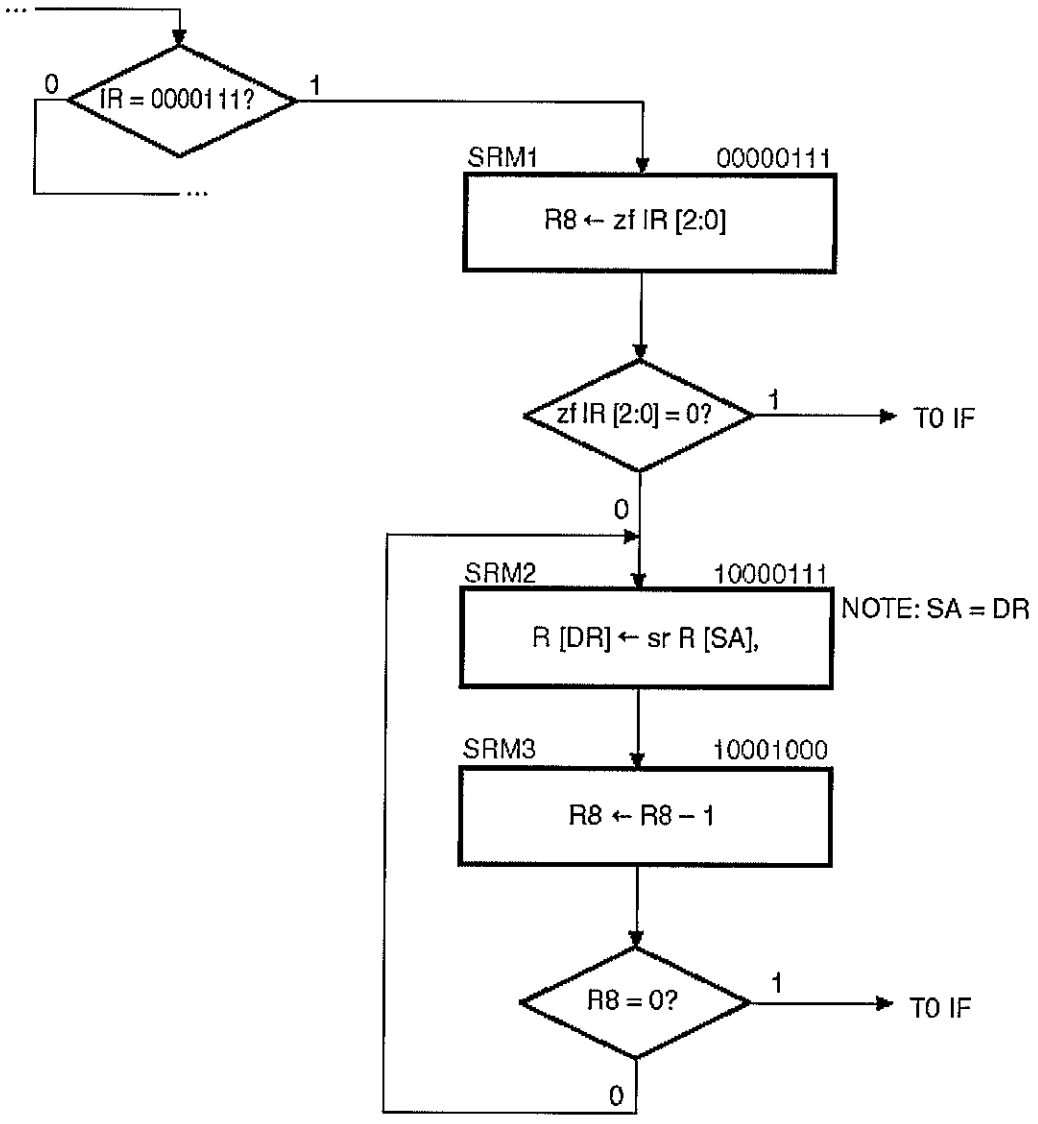


[15 Marks]

(Question 3 continues on next page)

(Question 3 continued from previous page)

(b) The following ASM defines an instruction for our microprogrammed multiple cycle instruction set processor. What instruction does the ASM describe?



[5 marks]

4. (a) Provide a detailed schematic for a *Function Unit* that implements the following *micro-operations*:

[15 marks]

Table 1: FS code definition

FS	Micro-operation
00000	$F = A$
00001	$F = A + 1$
00010	$F = A + B$
00011	$F = A + B + 1$
00100	$F = A + \bar{B}$
00101	$F = A + \bar{B} + 1$
00110	$F = A - 1$
00111	$F = A$
01000	$F = A \wedge B$
01010	$F = A \vee B$
01100	$F = A \oplus B$
01110	$F = \bar{A}$
10000	$F = B$
10100	$F = srB$
11000	$F = slB$

(b) What do the following Boolean Expressions implement? Please provide a detailed discussion. How would you implement C_8?

$C_{i+1} = g_i + p_iC_i$

$C_1 = x_0y_0 + C_0(x_0 + y_0)$

$= g_0 + C_0p_0$

$C_2 = x_1y_1 + C_1(x_1 + y_1)$

$= x_1y_1 + [x_0y_0 + C_0(x_0 + y_0)](x_1 + y_1)$

$= g_1 + p_1g_0 + p_0p_1C_0$

$C_3 = g_2 + p_2g_1 + p_1p_2g_0 + p_0p_1p_2C_0$

$C_4 = g_3 + p_3g_2 + p_2p_3g_1 + p_1p_2p_3g_0 + p_0p_1p_2p_3C_0$

[5 marks]