Coláiste na Tríonóide, Baile Átha Cliath
Trinity College Dublin
Ollscoil Átha Cliath | The University of Dublin

Faculty of Engineering, Mathematics and Science

School of Computer Science and Statistics

Integrated Computer Science
Year 3 Annual Examinations

Hilary Term 2018

CS3021Computer Architecture II

8 January 2018 | Goldsmith Hall | 09:30 – 11:30

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Instructions to Candidates:

Answer **THREE** questions.
All questions carry equal marks
All questions are marked out of 20

Q1. Briefly describe the IA32 and x64 procedure calling conventions. Make sure that you describe the register set, draw a diagram of a typical procedure stack frame, list the volatile registers and in the case of the x64 calling convention explain the use of *shadow space*.

[6 Marks]

What is the main advantage of the x64 procedure calling convention compared with the IA32 procedure calling convention?

[2 marks]

Convert the following code segment into (i) IA32 and (ii) x64 assembly language (assume INT is a 32 bit integer for IA32 code and a 64 bit integer for x64 code):

```
INT g = 4;

INT max(INT a, INT b, INT c) {
   INT v = a;
   if (b > v)
      v = b;
   if (c > v)
      v = c
   return v;
}

INT p(INT i, INT j, INT, k, INT l) {
   return max(max(g, i, j), k, l);
}
```

[12 marks]

Q2. How are virtual addresses converted to physical addresses by a two level page table? Assume a page table structure as per an IA32 based CPU. Draw diagrams to illustrate your answer.

[4 marks]

What is the advantage of using a two level page table compared with a single level page table? Comment on the amount of physical memory needed for the page tables of (i) a "small" process and (ii) a "maximum sized" process using a single level and a two level page table structure. Draw diagrams to illustrate your answer.

[4 marks]

Draw a diagram showing the structure an IA32 2 level kernel page table which maps the first 16MB of the kernel's virtual address space starting at address 0x00000000 onto 8MB of memory located at physical address 0x10000000 and 8MB of memory located at physical address 0x20000000.

[12 marks]

Q3. With the aid of a diagram, explain how a cache organisation can be characterised by the three constants LKN. Explain, in detail, how a data item is accessed in an LKN cache. Why does a cache normally reduce the effective memory access time?

[6 marks]

Compute the number of hits and misses if the following list of hexadecimal addresses is applied to (1) a 64 byte direct mapped cache with 16 bytes per line and (2) a 64 byte fully associative cache with 16 bytes per line.

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0x0000 → 0x0010 → 0x0020 → 0x0030 →
0x0034 → 0x0020 → 0x0010 → 0x000c →
0x0050 → 0x0040 → 0x002c → 0x0008 →
0x0030 → 0x0020 → 0x0010 → 0x0000

Assume that (i) the low 4 bits of the address is used as the offset into the cache line and the next log2(N) bits select the set (ii) the cache is initially empty and (iii) a LRU replacement policy is used.

[10 marks]

Would you expect an associative cache of size N and line size L to always have a higher hit rate than direct mapped cache of size N and line size L. Explain the reasoning behind your answer.

[4 marks]

Q4. What is the cache coherency problem? Briefly explain the states and operation of the Write Once cache coherency protocol.

[8 marks]

Consider a three CPU multiprocessor system where each CPU has its own cache. Each cache is direct mapped with 2 sets; (i) even addresses map to set 0 and odd addresses map to set 1 and (ii) the caches are initially empty. Explain in detail what happens when each of the following memory accesses are made by the CPUs assuming a Write Once cache coherency protocol (e.g. bus traffic and state transitions).

t	CPU 0	CPU 1	CPU 2
0	read a0		
1	read a0		
2		read a0	
3		write a0	
4			read a0
5			write a0
6	write a0		
7	read a0		
8		read a0	
9	write a0		
10		write a0	
11		write a0	

[12 marks]