ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 242E

DIGITAL CIRCUITS LABORATORY EXPERIMENT REPORT

EXPERIMENT NO	:	1
EXPERIMENT DATE	:	17.03.2023
LAB SESSION	:	FRIDAY - 16.00
GROUP NO	:	G18

GROUP MEMBERS:

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SPRING 2023

Contents

1 INTRODUCTION [10 points]

Briefly describe what you have done during the experiment.

2 MATERIALS AND METHODS [40 points]

Answer all questions and provide everything that are indicated in the "Report" section of the related experiment in "Experiments Booklet". Edit following sub-heading as you wish.

2.1 Preliminary

Figure 1: An Example Figure Caption[**?**]

2.2 Experiment

- **Part 1:** Design and implement the logic circuits for the given expressions below by using the necessary gates.
  $F_1(a, b) = a + ab$
  $F_2(a, b) = (a + b).(a + \overline{b})$

  NOTE: In order to design and implement boolean functions, we benefit from Logisim tool which enables us to simulate our circuits with different input combinations and detect possible errors.

Design of F_1:

To design and implement F_1, we need to use a 2-input AND gate, a 2-input OR gate.

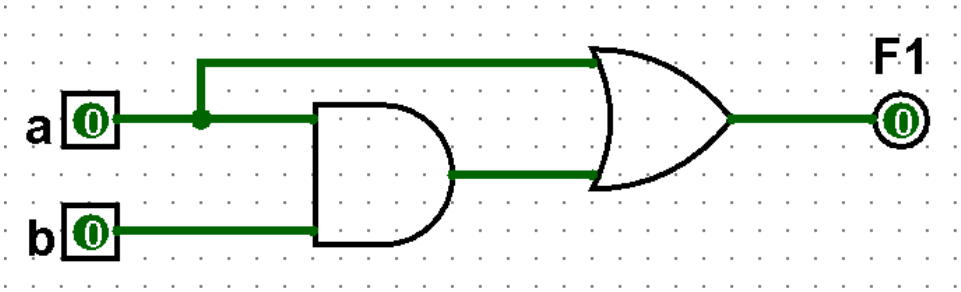

Figure 2: Design of F_1 in Logisim

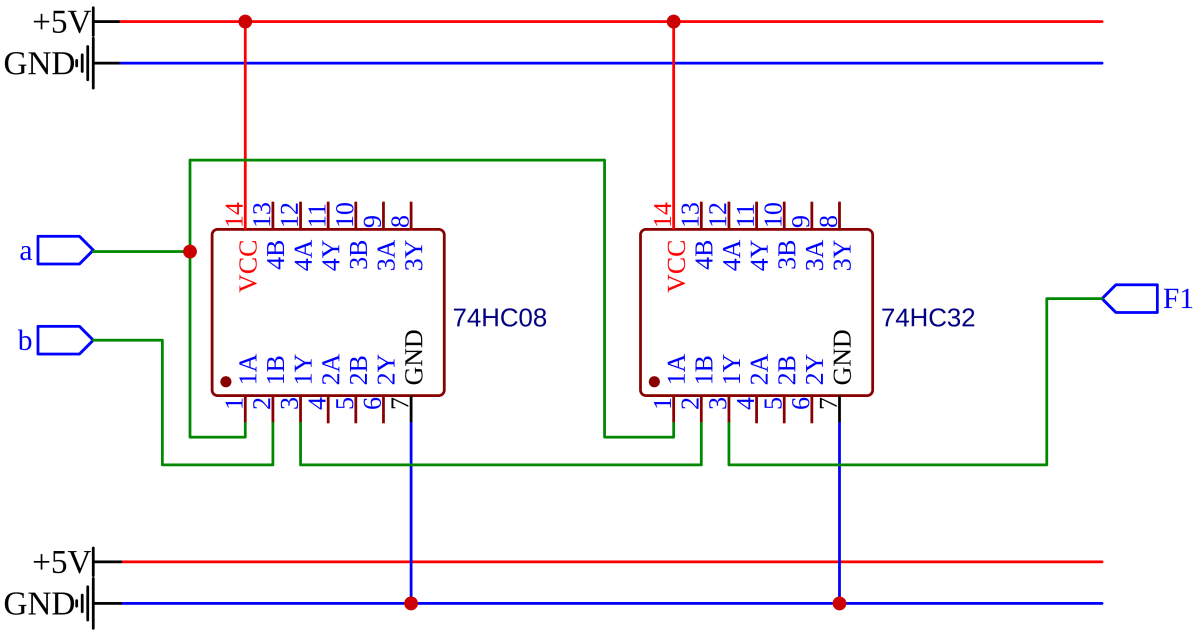

Figure 3: Design of F_1 in EasyEDA

Design of F_2:

To design and implement F_2, we need to use two 2-input OR gates, a 2-input AND gate, a NOT gate.

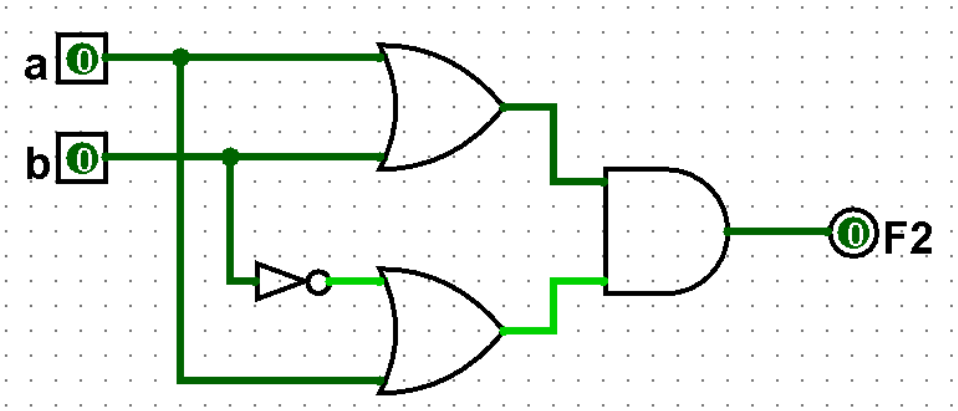

Figure 4: Design of F_2 in Logisim

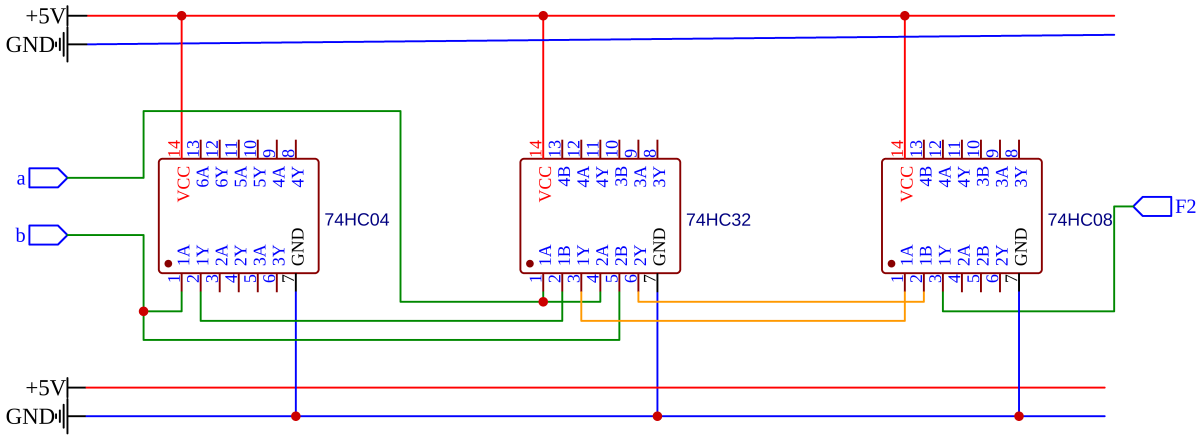

Figure 5: Design of F_2 in EasyEDA

To validate our designs of F_1 and F_2, we need to create truth tables of them. Both F_1 and F_2 functions have the same truth tables.

a	b	F_1
0	0	0
0	1	0
1	0	1
1	1	1

Figure 6: Truth table of the function F_1 and F_2

Our implementations of F_1 and F_2 are compatible with their truth table.

- **Part 2:** A theorem is given as: $a + (a \cdot b) = a$. First, determine the dual of the given theorem and then, implement the functions for both sides of the dual theorem by using logic gates. Validate the truth of the theorem by comparing the changes in the outputs.

  First of all, the dual of a theorem is an expression created by replacing OR with AND, AND with OR, 1 with 0 and 0 with 1. Also, the order of operations should be preserved, so we need to put extra parentheses. In this formula, $(a \cdot b)$ is done first:

$$a + (a \cdot b) = a \qquad \text{(Original)}$$
$$a \cdot (a + b) = a \qquad \text{(Dual)}$$

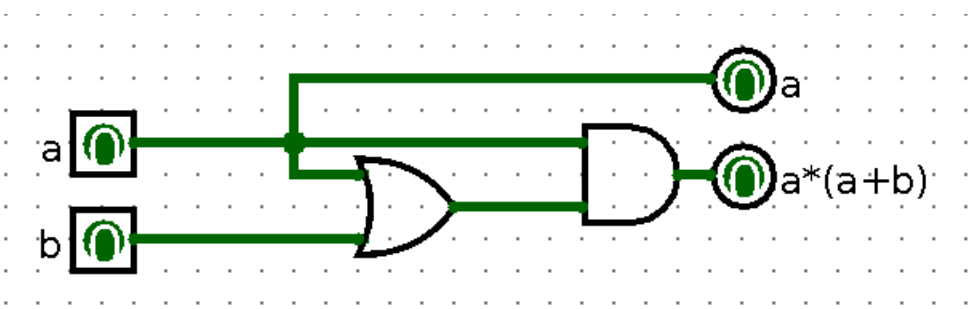

Figure 7: Design in Logisim

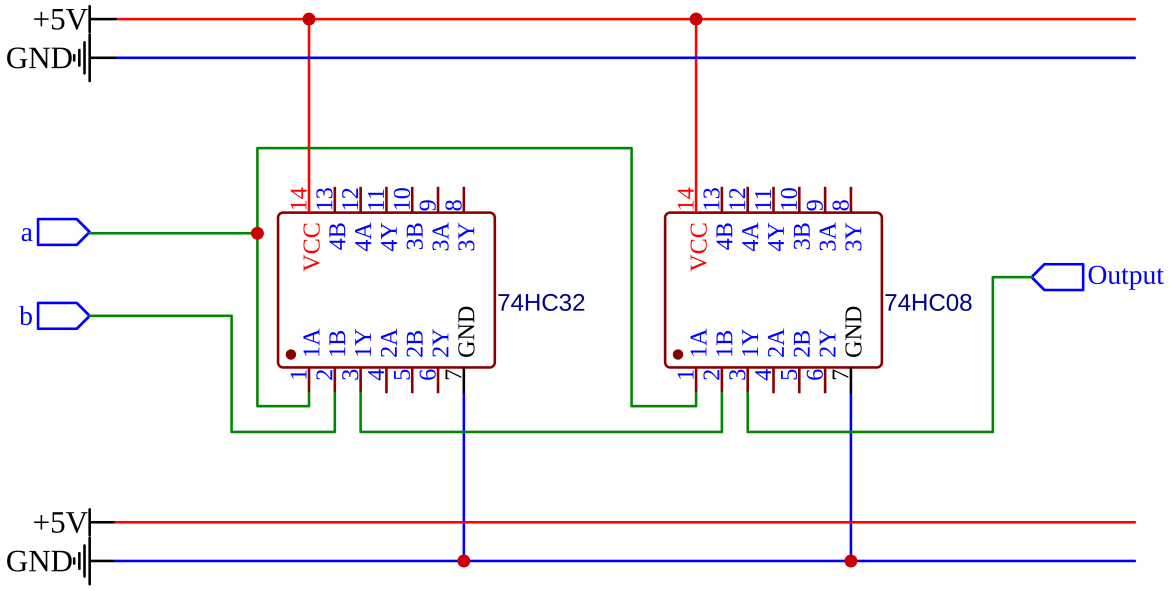

Figure 8: Design in EasyEDA

To check validity of the dual theorem, the following truth table is constructed:

a	b	$a \cdot b$	$a + b$	$a + a \cdot b$	$a \cdot (a + b)$
0	0	0	0	0	0
0	1	0	1	0	0
1	0	0	1	1	1
1	1	1	1	1	1

As it is clear from the table, the last two columns, which are the original expression's and its dual's left-hand side truth values, are identical to the first column, the right-hand side of the both equations. The equivalency of functions a and $a \cdot (a + b)$ confirms the dual theorem.

- **Part 3:** $F_3(a, b, c) = ab + \overline{a}c$ is given. First, determine the complement of the given function (F_3). Then, implement the circuit which realizes the complementary function ($\overline{F_3}$). Validate your implementation by using the truth table.

Step 1: In the first step, we find the complement of the given function F_3 by applying **De Morgan's** rule.

Step 1.1: $\overline{F_3(a, b, c)} = \overline{ab + \overline{a}c}$

Step 1.2: $\overline{F_3(a,b,c)} = (\overline{a} + \overline{b}).(a + \overline{c})$

Step 2: In the second step, we implement the circuit which realizes the function $\overline{F_3}$.

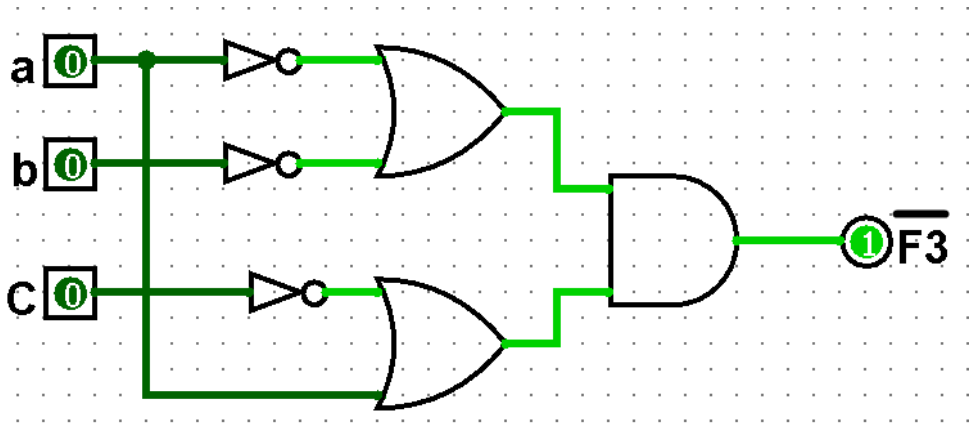

Figure 9: Design of $\overline{F_3}$ in Logisim

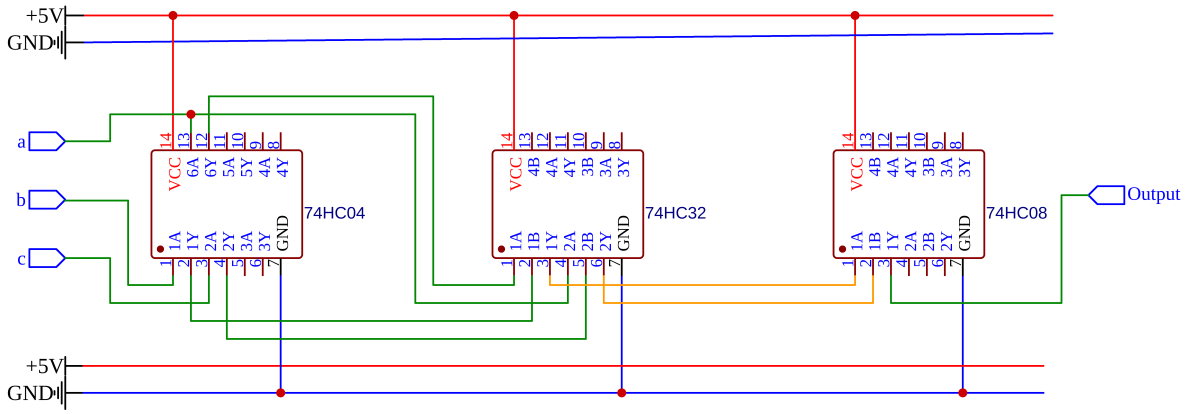

Figure 10: Design of $\overline{F_3}$ in EasyEDA

Step 3: In the third step, we validate our implementation of the function $\overline{F_3}$ using truth table.

a	b	c	$\overline{F_3}$
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Figure 11: Truth table of $\overline{F_3}$

According to the truth table, our implementation is correct.

- **Part 4:** A basic logical function F_4 is defined as follows. $F_4(a, b, c, d) = \cup_1(1, 2, 5, 6, 9, 10, 13, 14)$. First, simplify given logical function and implement the simplified expression using logic gates. Validate your circuit by observing the outputs for each possible input.

  Simplification is done using Karnaugh map. The result suggests only two prime implicants as show below:

ABCD	F_4
0000	0
0001	1
0010	1
0011	0
0100	0
0101	1
0110	1
0111	0
1000	0
1001	1
1010	1
1011	0
1100	0
1101	1
1110	1
1111	0

$\longrightarrow$

AB \ CD	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$\longrightarrow$ $C\overline{D} + \overline{C}D$

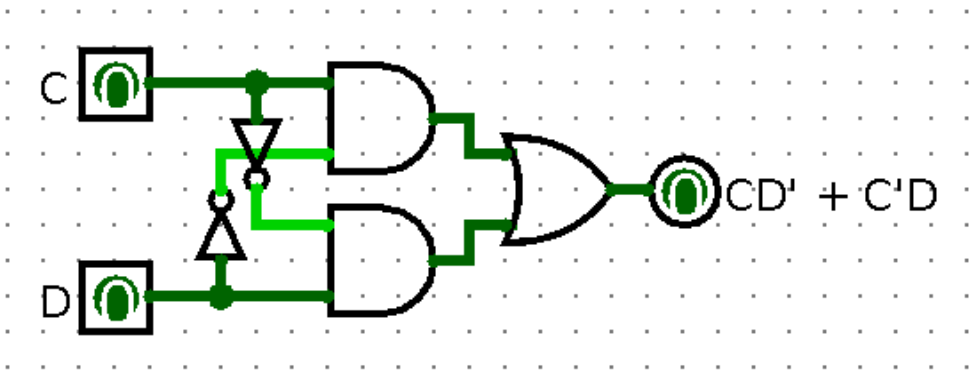

Figure 12: Design of F_4 in Logisim

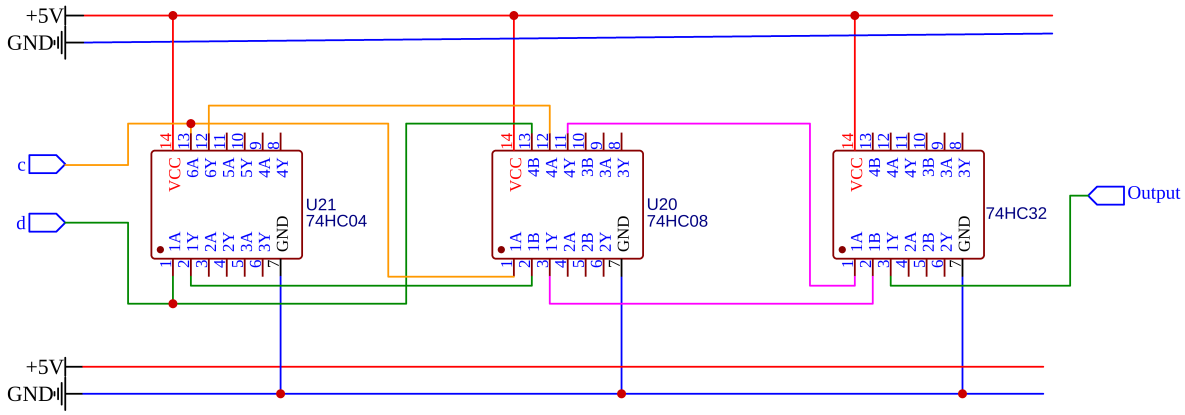

Figure 13: Design of F_4 in EasyEDA

- **Part 5:**
- **Part 6:**

3 RESULTS [15 points]

Give the your results what did you get during the experiment. You can also add table, image, etc.

4 DISCUSSION [25 points]

Please explain, analyze, and interpret what have you done during the experiment.

5 CONCLUSION [10 points]

Comment on any difficulties you have faced, what you have learned etc.