CMOS Shunt-Peaked Amplifier:

Spec-Driven Design, LD Sweep, and Gain/BW/Power Across PVT Corner Analysis

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Project Overview

In this project, I designed and verified a CMOS shunt-peaked amplifier in Cadence (Spectre / ADE XL) to meet gain-peaking, bandwidth, and power targets under process/voltage/temperature variation. The testbench used VDD = 1.0 V, VinDC = 700 mV, and a small-signal input of amp = 100 mV (≈ 200 mVpp). I applied shunt peaking by tuning the load inductor to LD = 16.2 nH with CL = 1.6 pF and sized the device using nfinger = 4 and Multi = 20. From AC analysis, the amplifier achieved a DC (low frequency) gain ≈ 12.45 dB (~4.19 V/V) and produced the intended peaking behavior near ~1 GHz after LD tuning. I also verified robustness across PVT corners by overlaying AC responses and recording gain at markers (100.52 MHz and ~992.99 MHz), where the corner results span approximately 4.47 to +3.41 dB (at 100.52 MHz) and −1.43 to +6.41 dB (at ~992.99 MHz). Finally, the DC operating point confirmed bias and power consistency (e.g., Id ≈ 1.296 mA, Vout ≈ 0.820 V, and P ≈ 1.27 mW), reinforcing the trade-offs between LD, device sizing (nfinger/Multi), and frequency response.

Project at a Glance

- Tool: Cadence Virtuoso / Spectre / ADE XL
- Supply: VDD = 1.0 V
- Bias: VinDC = 700 mV
- Input swing (verification): amp = 100 mV (≈ 200 mVpp)
- Shunt-peaking network: LD = 16.2 nH, CL = 1.6 pF
- Device sizing: nfinger = 4, Multi = 20
- Key operating point: Vout ≈ 0.820 V, Id ≈ 1.296 mA, P ≈ 1.27 mW
- Key AC result: DC gain ≈ 12.45 dB (~4.19 V/V), peaking near ~1 GHz

Design Approach

A shunt-peaked load was used to intentionally shape the amplifier's frequency response by introducing controlled peaking and improving high-frequency behavior compared to a purely resistive load. The primary tuning knob was L_D, which shifts the peaking frequency and changes the amount of peaking; $C_L$and device sizing (nfinger/Multi) set the parasitic and loading conditions that determine how strong the effect becomes. I first selected a baseline operating point (bias and sizing) that produced a reasonable DC gain and power dissipation. Next, I tuned **LD** to place the gain peaking near **~1 GHz**, and then verified the final design with sweeps and PVT corners to quantify robustness and worst-case variation.

Simulation Plan (What I Ran)

1. **DC Operating Point (op):** Confirm bias, output voltage, supply current, and DC power.
2. **AC (Typical):** Plot gain $A_v(f)$versus frequency and extract DC gain and gain at key frequencies.
3. **LD Sweep (AC):** Sweep $L_D$to show how peaking and bandwidth change with tuning and to justify the final LD value.
4. **PVT Corner Sweep (AC):** Run AC analysis across PVT corners and compare gain and bandwidth variation using consistent markers.

Metrics and How They Were Measured (ADE XL)

The following metrics were extracted consistently using ADE XL expressions:

- Gain vs frequency:

$$A_v(f) = 20\log_{10} | \frac{V_{out}}{V_{in}} |$$

implemented using dB20(VF("/vout")/VF("/vin")).

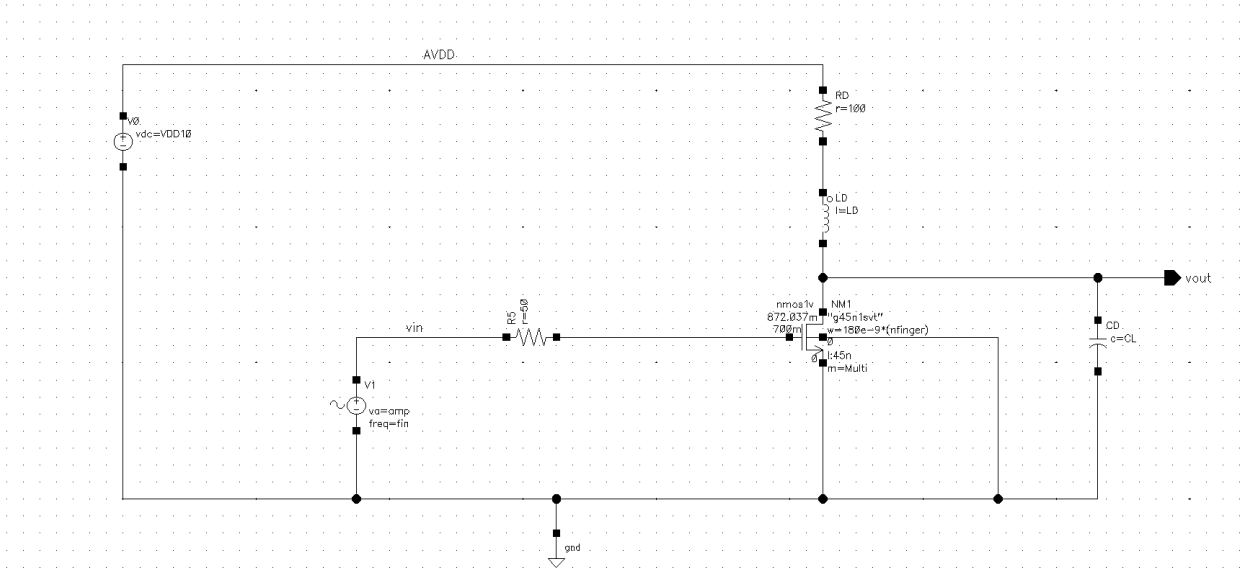
- DC gain (low-frequency gain): reported from the low-frequency region of the AC curve; measured value ≈ 12.45 dB.
- Gain at specific frequencies: evaluated at marker frequencies 100.52 MHz and ~992.99 MHz (≈ 1 GHz) using value(...) at those points.
- 3-dB bandwidth: determined using cross() at the frequency where gain falls to (DC gain − 3 dB).
- DC power:

$$P_{DC} = V_{DD} \cdot I_{DD}$$

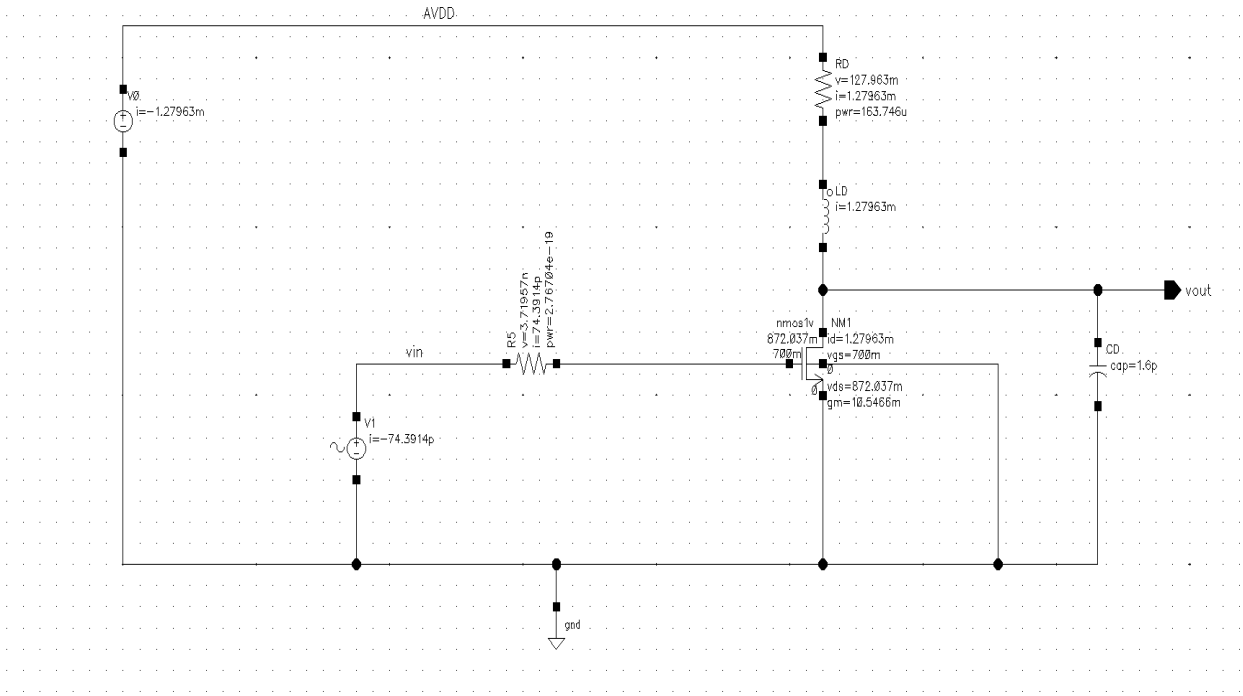
with measured values Id ≈ 1.296 mA and P ≈ 1.27 mW at VDD = 1.0 V.

Schematics and Plots

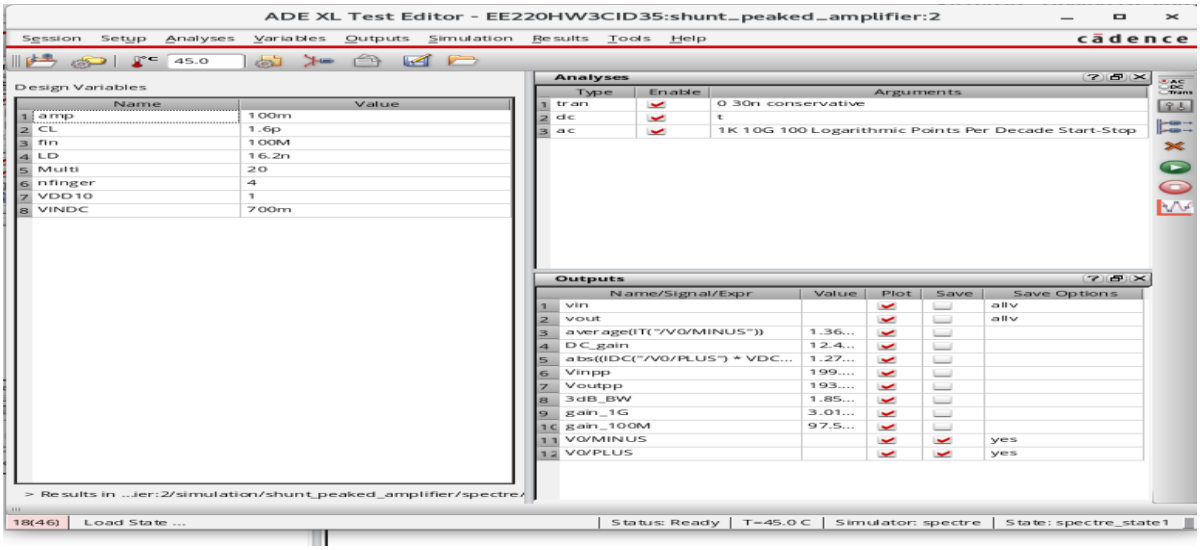
Schematic of shunt-peaked-amplifier

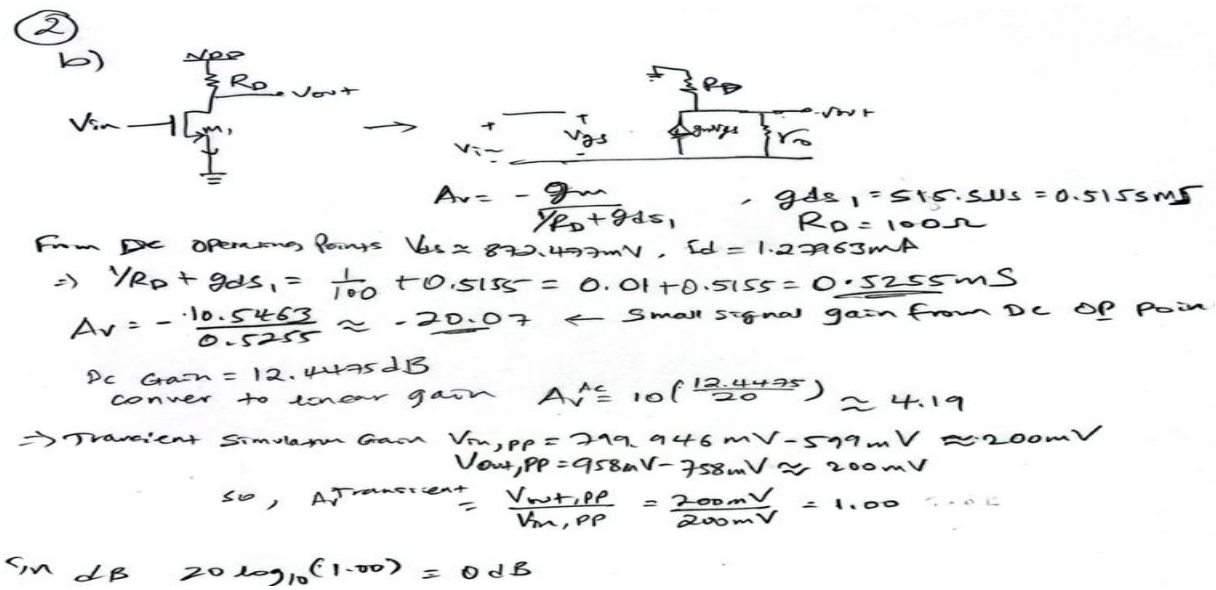


DC operating points



ADE XL spec.

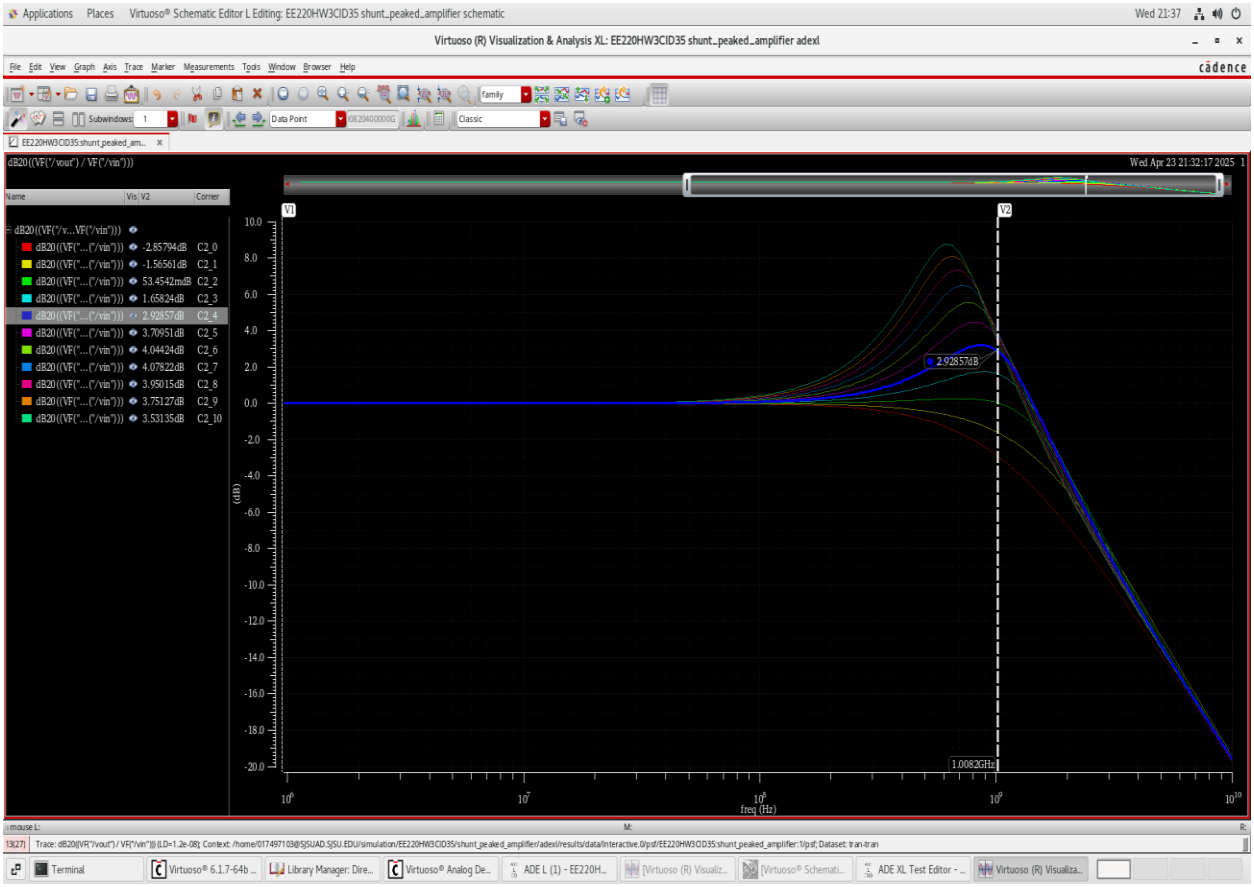




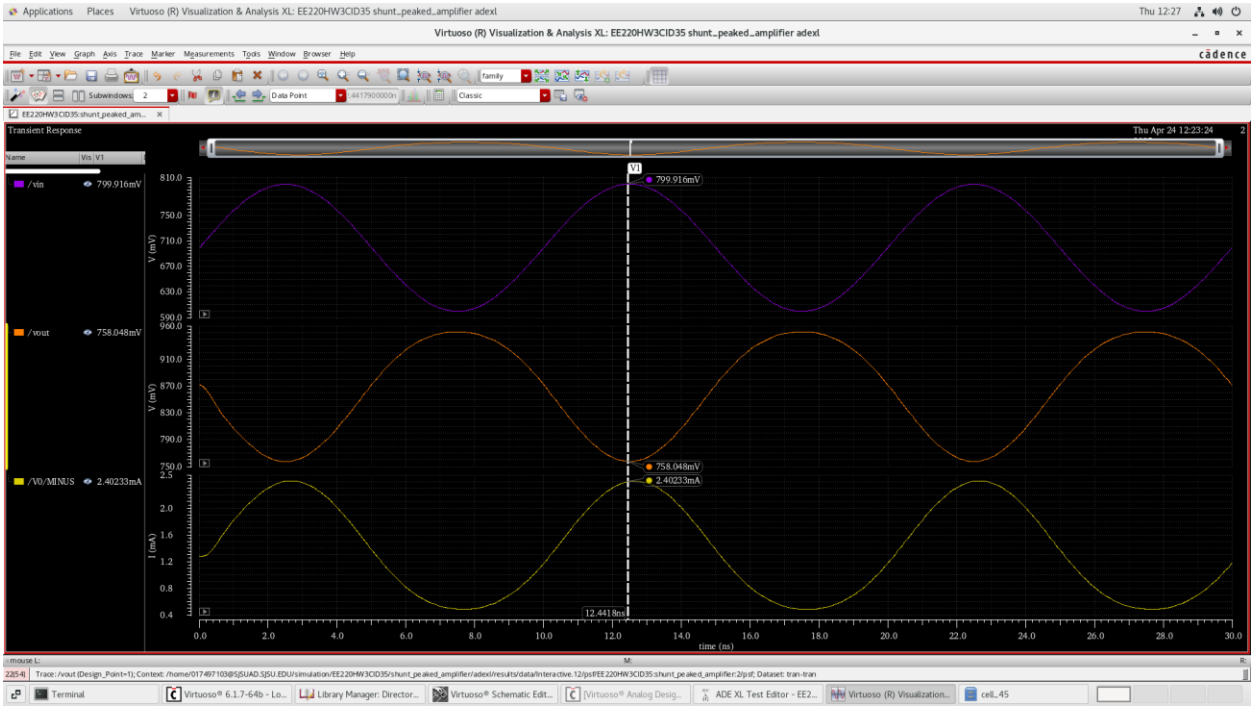
To analyze the amplifier's performance, I calculated the small-signal gain using three different methods: DC operating point, AC analysis, and transient simulation. From the DC operating point results, I used formula Av. The AC simulation result at 1 Hz yielded a gain of + 12.45dB, which translates to a linear gain of about 4.19. In contrast, the transient simulation (based on the peak-to-peak input and output voltages of approximately 200 mV each) showed a gain of 1.0, or 0dB.This discrepancy can be explained by several factors. The DC small-signal model assumes ideal linear operation with no parasitics, which overestimates gain. The AC analysis includes real circuit effects such as output loading and parasitic capacitances, giving a more accurate small-signal response. The transient result reflects the actual time-domain behavior, including large-signal effects like output swing limitations, nonlinearity, and dynamic response, which can significantly reduce gain under real signal conditions.

This comparison highlights the importance of considering all simulation types to evaluate amplifier performance accurately.

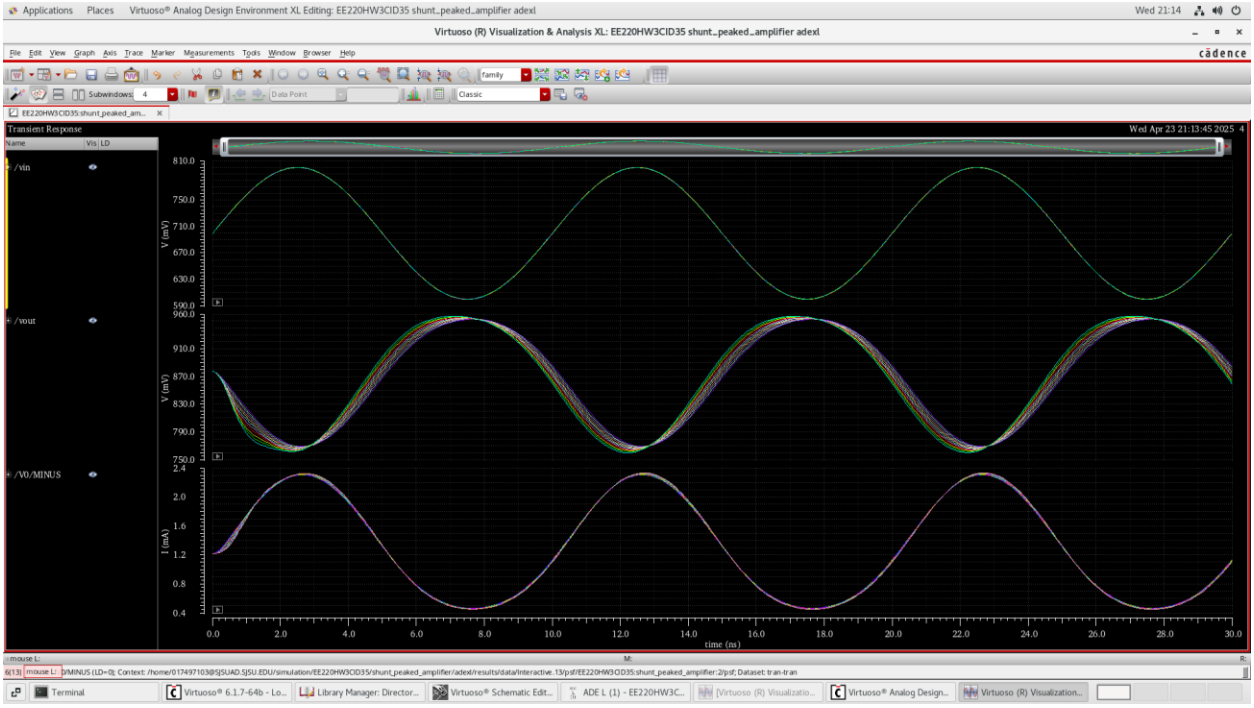
AC Response vs. LD



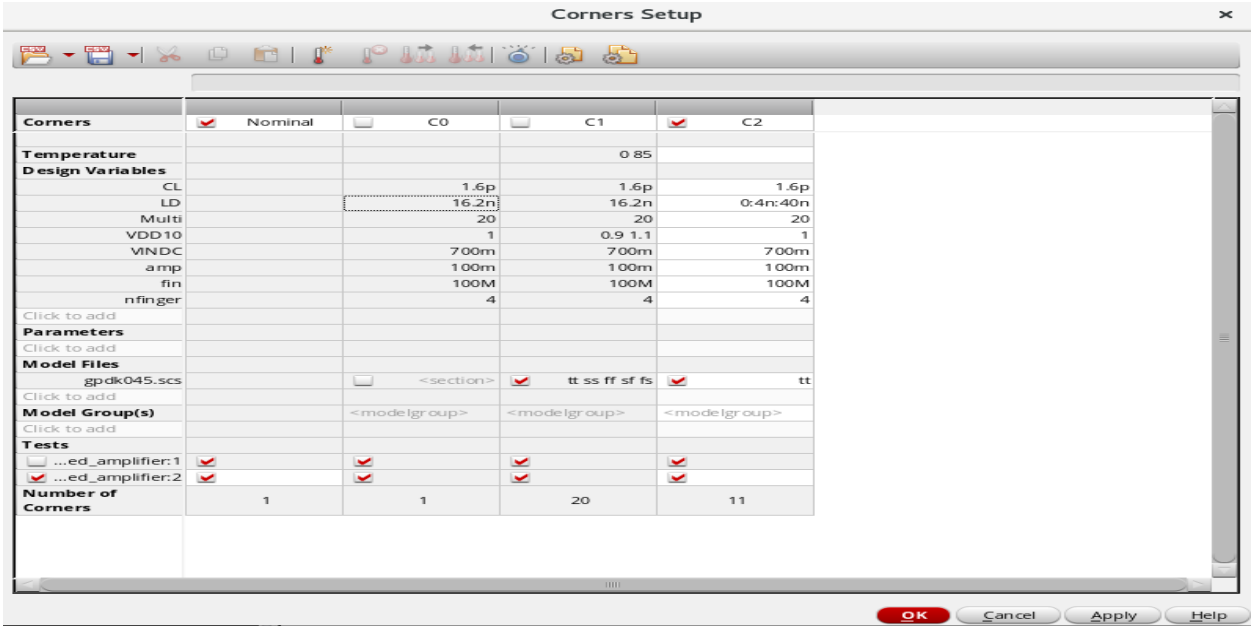
Typical Transient Response



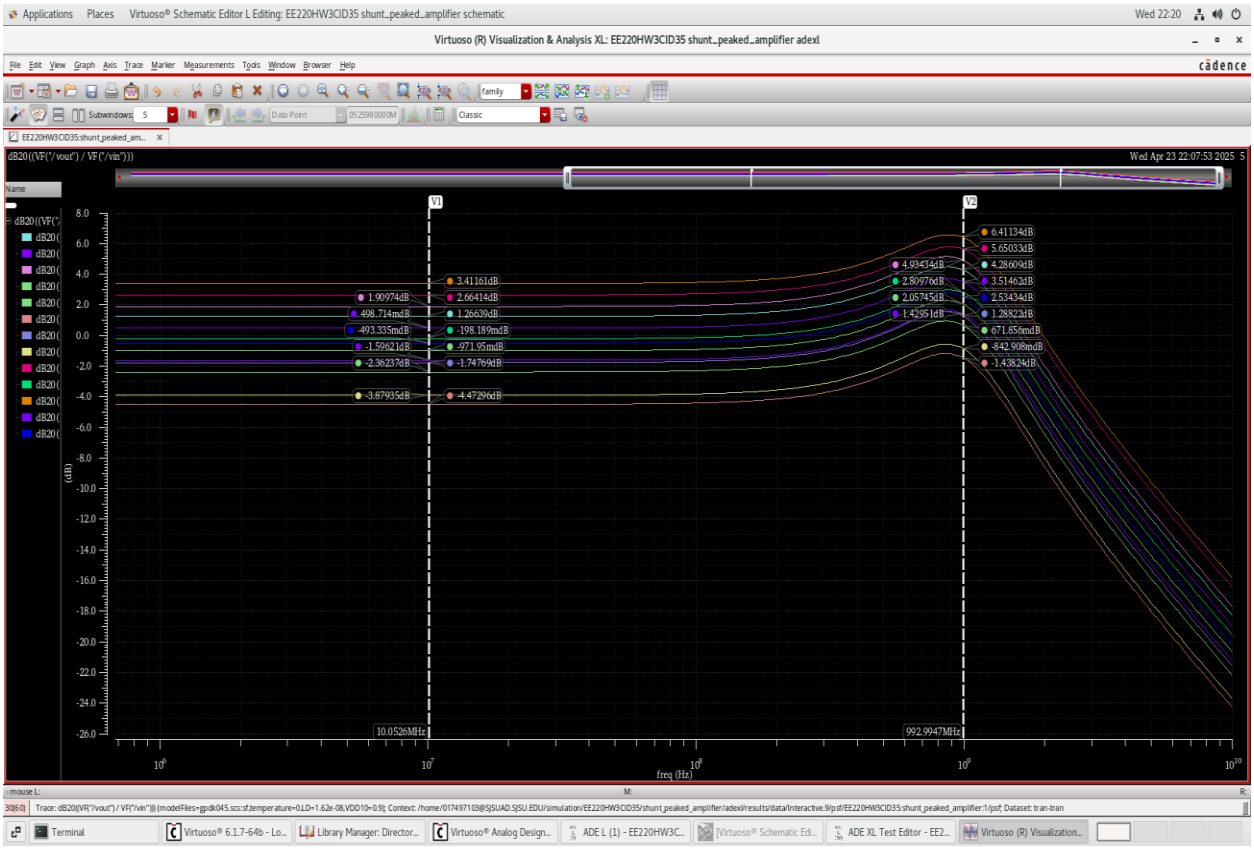
Typical Transient Response with LD sweep



PVT corner setup similar



and Here is the AC Response with LD sweep simulation below



Results Summary (Typical + Corners)

Typical (Nominal) Operating Point

- Vout ≈ 0.820 V
- Id ≈ 1.296 mA
- P ≈ 1.27 mW
- DC gain ≈ 12.45 dB (~4.19 V/V)
- Peaking behavior: tuned near ~1 GHz using LD = 16.2 nH and CL = 1.6 pF

Corner Sensitivity (Marker-Based Summary)

To quantify PVT variation, I compared gain values at two marker frequencies: 100.52 MHz and ~992.99 MHz. The corner sweep showed the following gain spread (relative to typical):

- At 100.52 MHz: approximately −4.47 to +3.41 dB variation across corners.
- At ~992.99 MHz: approximately −1.43 to +6.41 dB variation across corners.

(Note: exact corner names TT/SS/FF and conditions are recorded in the plotted corner overlays; the ranges above summarize worst-case behavior observed from the marker readouts.)

Conclusion

In this project, I designed and verified a CMOS amplifier with target specifications for gain, bandwidth, and power dissipation. I simulated the design across different PVT corners to evaluate performance robustness.

The AC response showed that while gain and 3 dB bandwidth varied slightly with corner, the design consistently achieved the required 3 dB peaking at ~1 GHz with LD tuning and met power constraints under all conditions.

I learned how to set up and evaluate frequency-domain responses using `dB20`, compute gain at specific frequencies, and find bandwidth using the `cross()` function. I also practiced matching my results against target specs and debugging evaluation errors in Cadence using waveform vs point outputs.

This helped reinforce my understanding of analog simulation, signal swing behavior, and trade-offs between LD, nfinger, and Multi in amplifier tuning.