Verification of Transmon Qubits using Cadence Virtuoso

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Introduction

The primary objective of this work was to design and verify a Superconducting Quantum Circuit using industry-standard Electronic Design Automation (EDA) tools. The project focused on the development of Transmon Qubits, which are critical components in circuit-based quantum computing due to their reduced sensitivity to charge noise.

The design workflow involved an integrated approach starting from Qiskit Metal for initial geometry generation, followed by the migration of the design into Cadence Virtuoso for physical layout refinement and verification. Within the Virtuoso environment, the layout hierarchy was managed through Flattening techniques to enable interactive editing and connectivity-driven design.

Key milestones of the work included:

- GDS Integration: Successfully importing the layout data and ensuring all 32 hierarchy levels were accurately loaded.
- Connectivity Assignment: Defining electrical nets by assigning Pins and Labels to the qubit pads to facilitate further simulation.
- Geometric Validation: Utilizing the Ruler tool to confirm that the physical dimensions (e.g., 700x500 units) align with the design specifications.
- Physical Verification: Executing a Batch Check which confirmed 0 violations in critical areas such as Antenna effects and Symmetry, ensuring the chip is ready for fabrication.

This report details the step-by-step methodology, the challenges encountered during GDS translation, and the final verification results that validate the chip's readiness for manufacturing.

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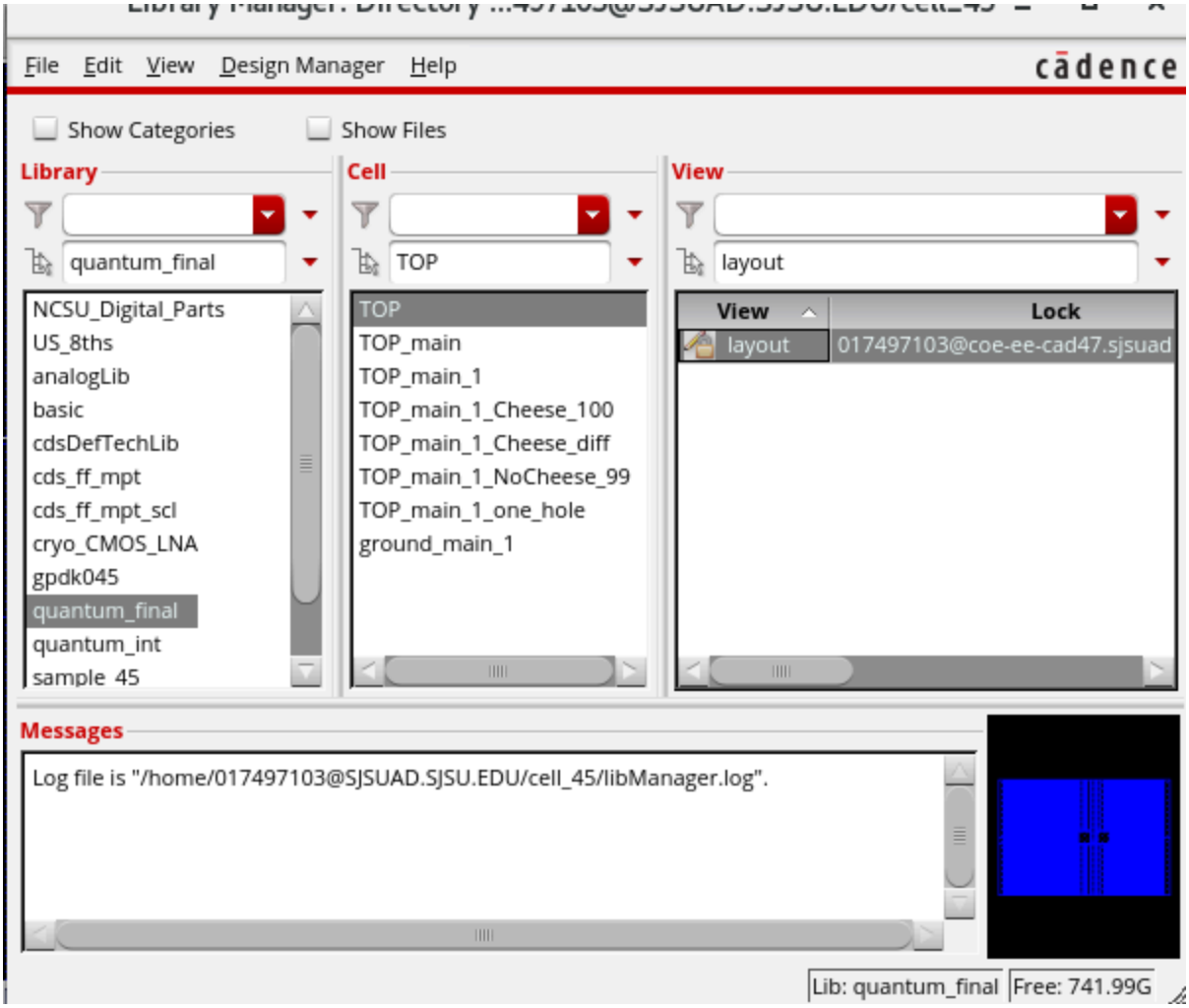
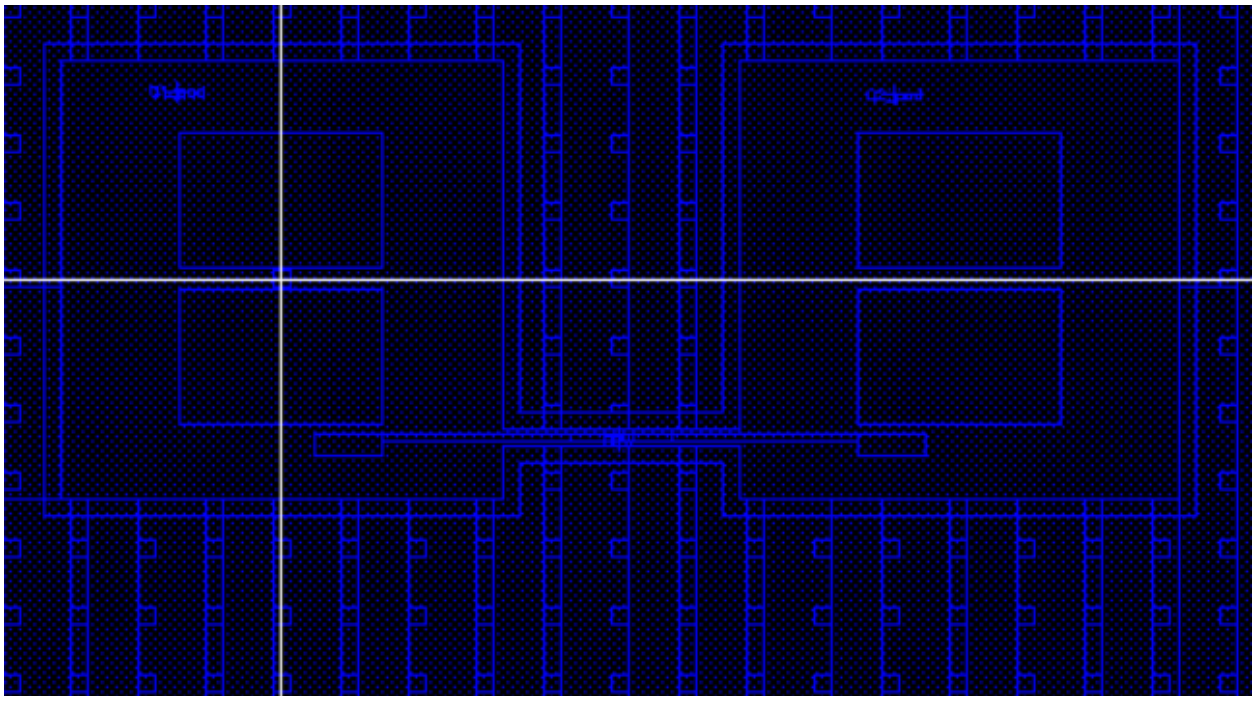


Pic1. The design library window shows the quantum_final library GDS file has successfully imported, the layout is ready.

Verification of Transmon Qubits using Cadence Virtuoso

The design was successfully finalized by assigning connectivity labels (Q1_pad, Q2_pad) within Virtuoso Layout XL. I initiated Physical Verification (DRC) to ensure manufacturing feasibility. The design is now ready for GDSII Stream-out or Electromagnetic (EM) simulation to verify the qubit coherence properties.



Pic2. Layout shows the Qubits labeled as Q1_pad to the left and Q2_pad to the right.

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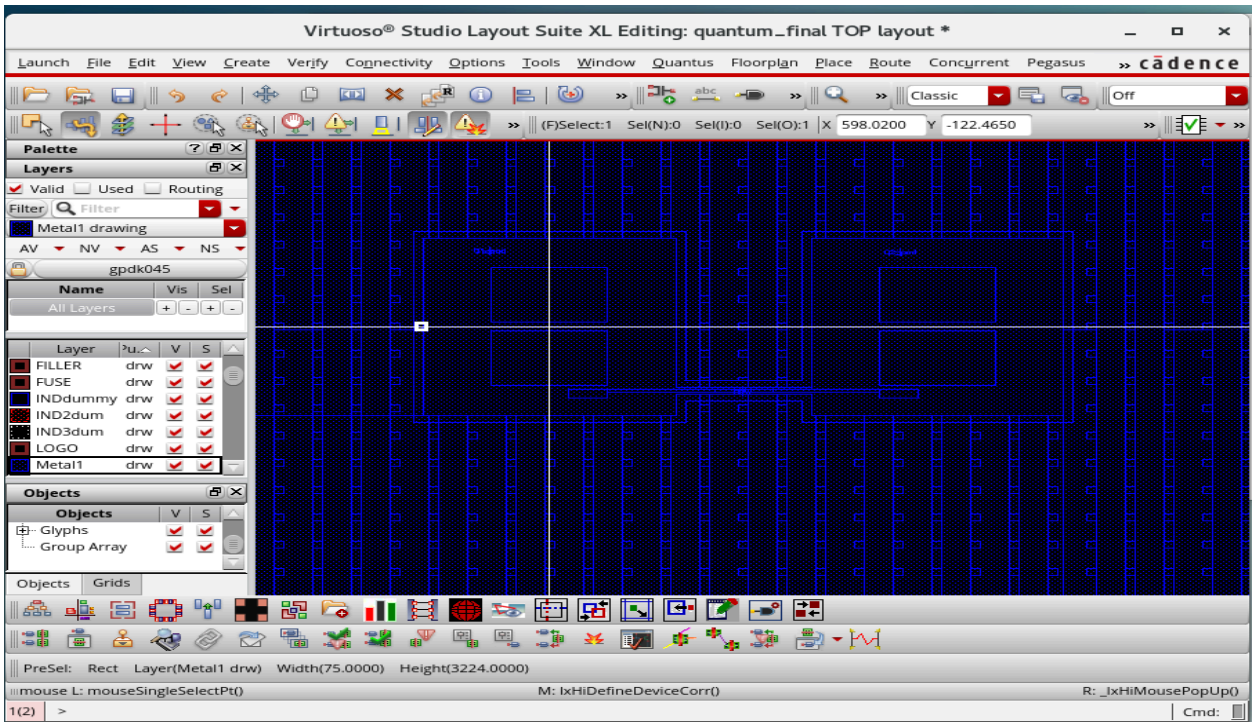
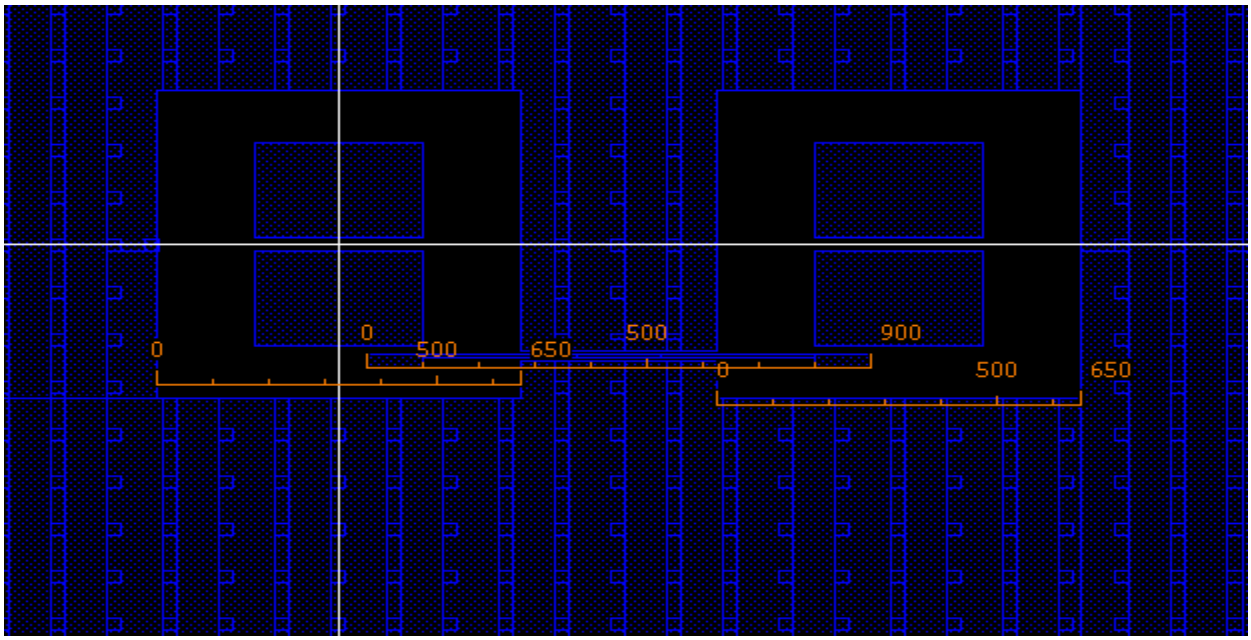
Following the labeling process, geometric verification was performed. Using the Ruler tool, I confirmed that the qubit pad dimensions and the gap between the resonator and the qubit are consistent with the design specifications. This ensures that the GDS translation maintains the required precision for superconducting circuit performance.

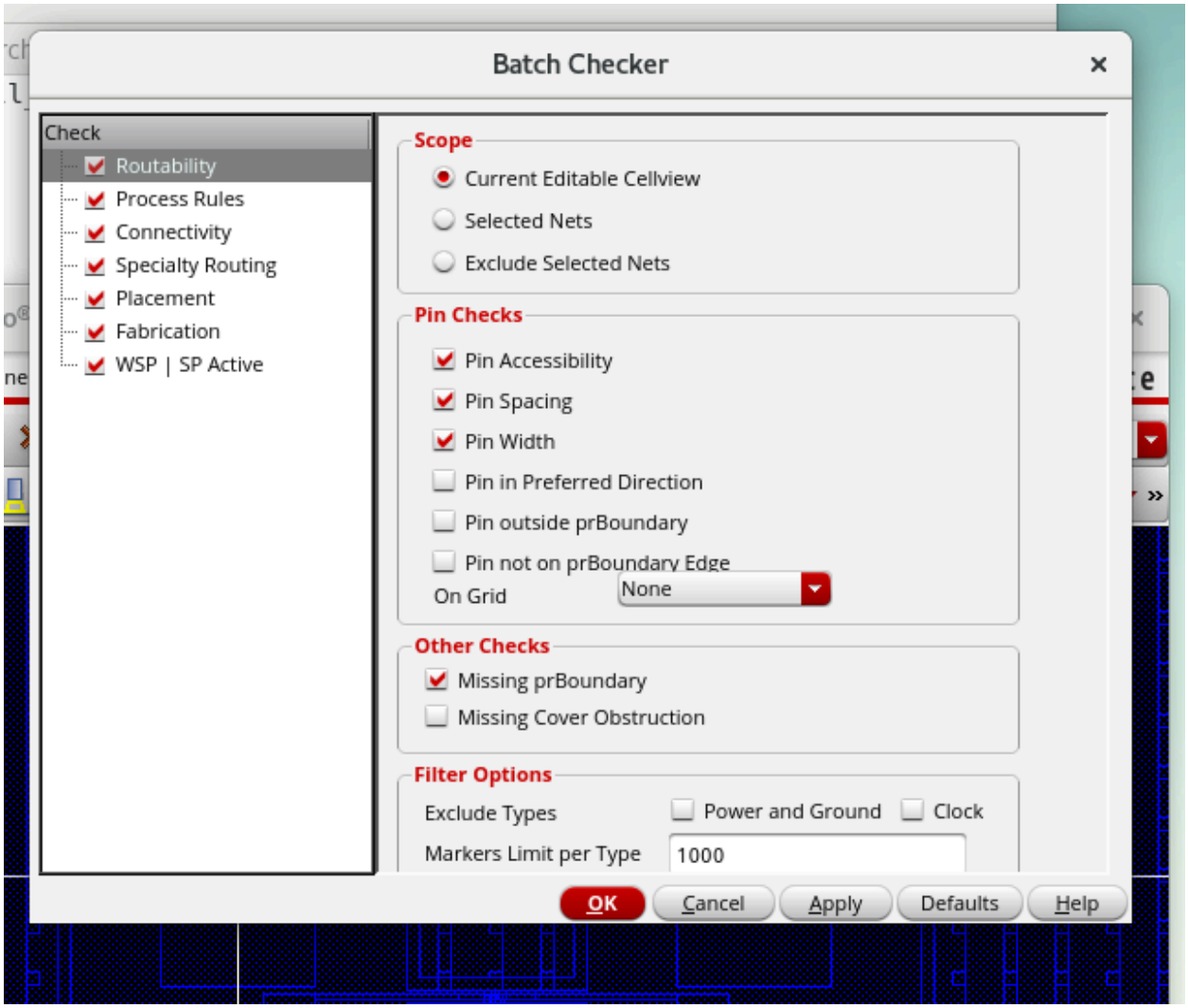




Pic3. Ruler tools to measure the qubits to confirm they have the same dimensions with the code I wrote in qiskit_metal.

Verification of Transmon Qubits using Cadence Virtuoso

I performed a comprehensive Batch Check on the finalized layout using the Virtuoso Batch Checker. The results confirmed zero violations across all critical parameters, including Antenna effects and Symmetry rules for the `Metal1` layer. This validation ensures that the Transmon Qubit design adheres to the foundry's manufacturing constraints and is ready for GDSII stream-out.



Pic4. Back check setting to finalize the layout- to make sure it's ready to be fabricated.

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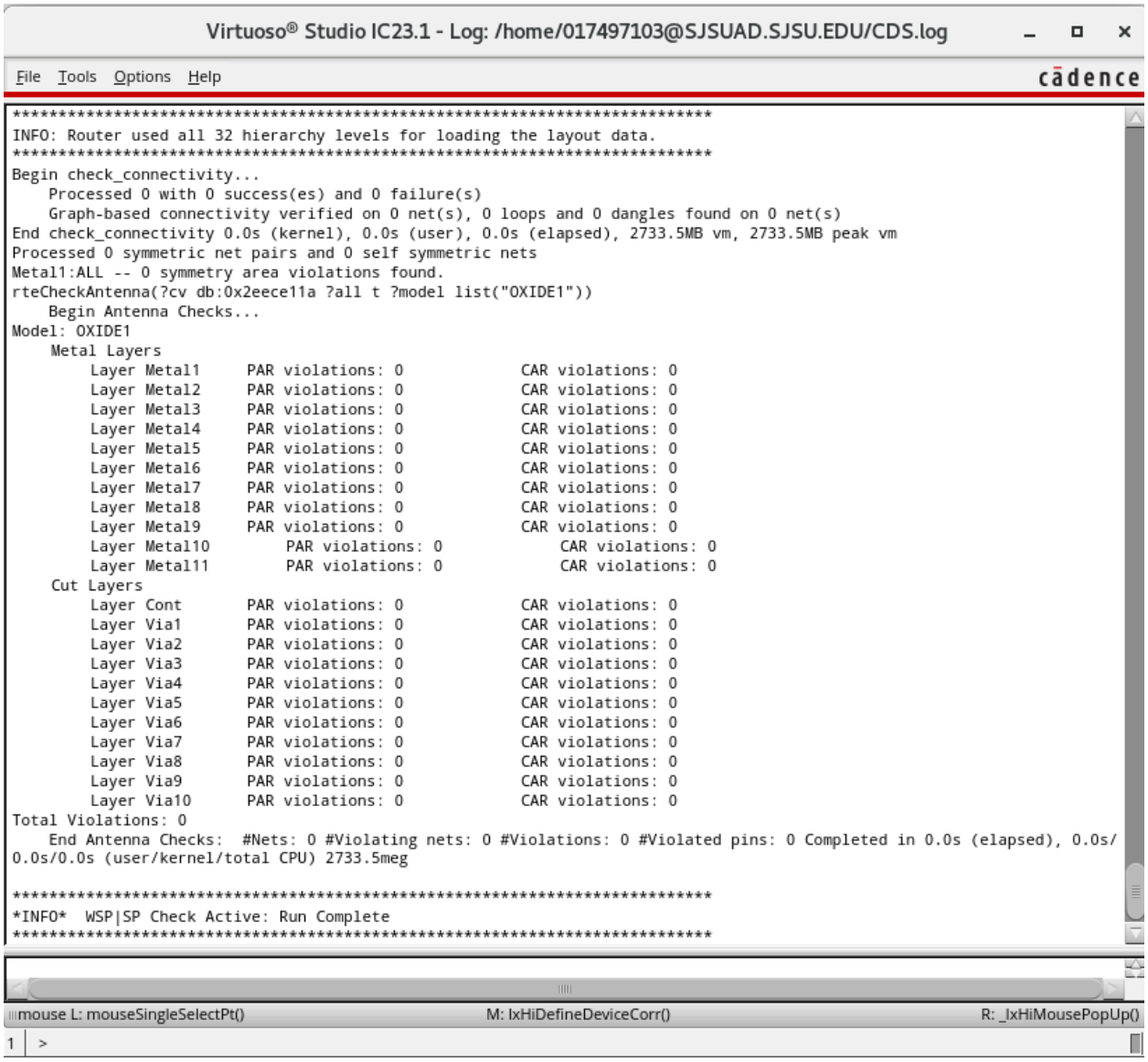
The workflow concluded with a Physical Verification phase. A Batch Check was executed in Virtuoso Layout XL to validate connectivity and fabrication rules. The design successfully passed all checks, confirming that the Transmon Qubit geometry is ready for the next phase of the quantum hardware development cycle.



Pic5. shows the log file that all runs were successfully completed.

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Appendix

The Qiskit Metal GUI (Graphical User Interface) served as a critical visualization tool during the design phase, providing a real-time graphical representation of the underlying Python code. This interactive environment allowed me for immediate observation of how specific parameter adjustments impacted the transmon qubit geometry and chip layout. By bridging the gap between programmatic script and physical structure, the GUI provided me a deeper understanding of the design's logic and ensured that the generated GDS data accurately reflected the intended quantum circuit specifications before it was exported to Cadence Virtuoso.