Low Noise Amplifier Design and Simulation Project

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Project description

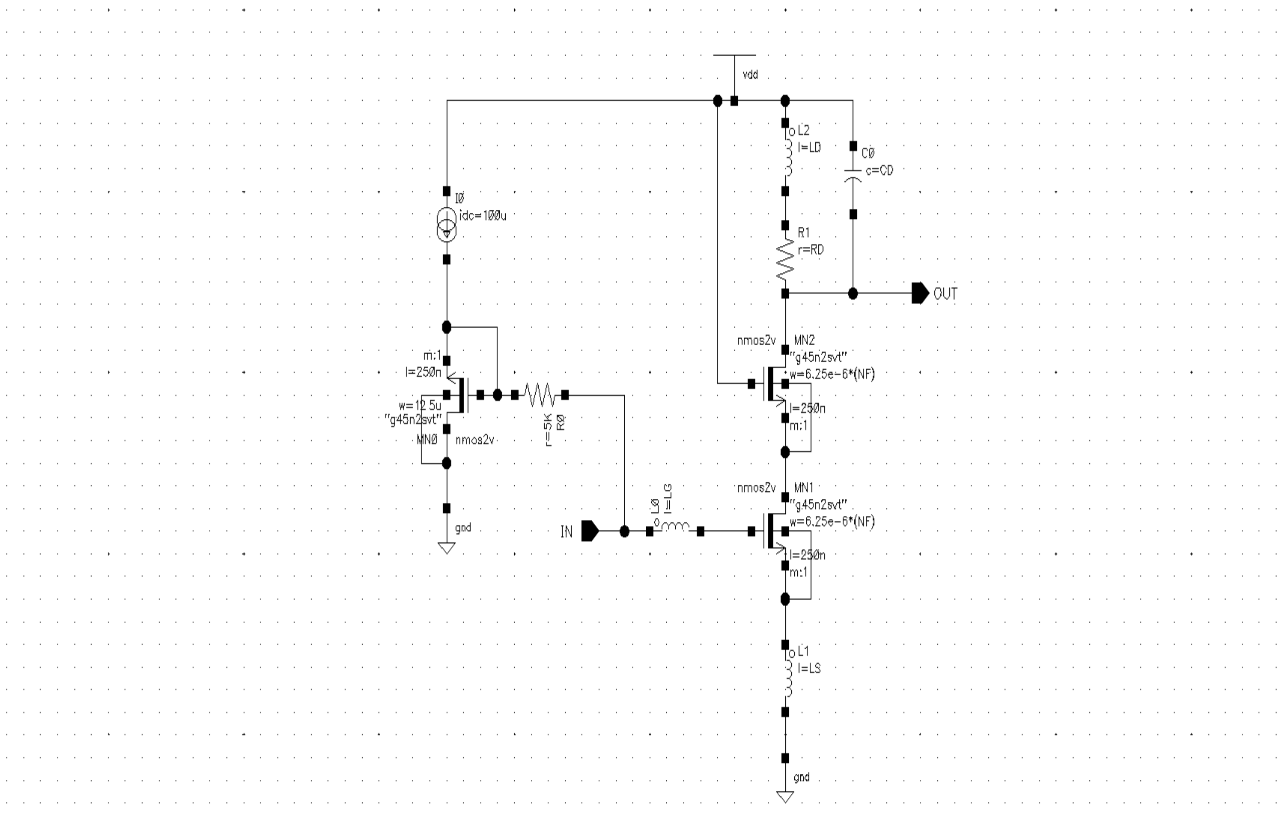
In this project, I designed and optimized a cascode CMOS LNA in Cadence SpectreRF to meet a spec-driven RF front-end target around the 2.4–2.48 GHz band using VDD = 1.8 V. The main goals were to achieve high forward gain (S21) while maintaining good input/output matching (S11, S22), low noise figure (NF), and adequate linearity (P1dB, IIP3) under a strict power budget. The design variables included the MOS sizes (M0–M2) and the matching/tank components LS, LG, LD, RD, CD, with the additional constraint that the load tank Q (from LD and RD) stays within a practical range. Performance was evaluated using a combination of DC operating point, S-parameter, PSS, P1dB compression, and two-tone / Rapid IIP3 simulations to quantify gain, match, noise, distortion, and overall trade-offs.

Design Targets (Given Specs)

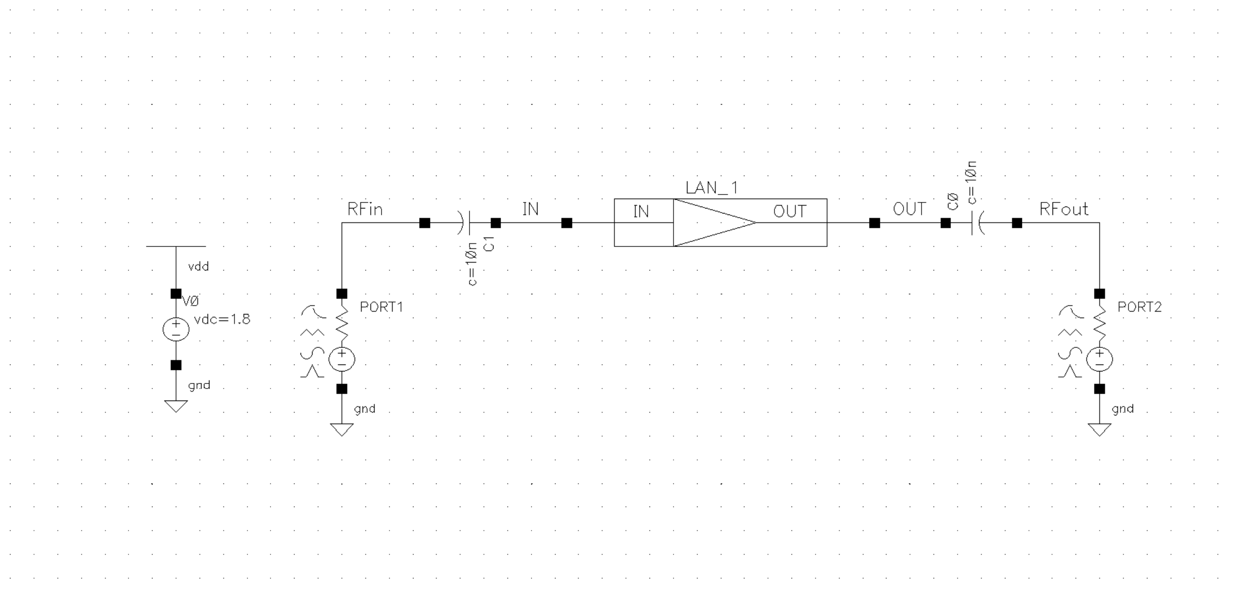
Parameter	Target
Supply Voltage (VDD)	1.8 V
Operating Band (f)	2.40–2.48 GHz
Forward Gain (S21)	> 15 dB
Input Return Loss (S11)	< −15 dB
Output Return Loss (S22)	< −15 dB
Noise Figure (NF)	< 2 dB
DC Power (PDC)	< 4 mW
Linearity (IIP3)	> −20 dBm

Schematics and Plots

LNA Schematic



LNA Testbench Schematic



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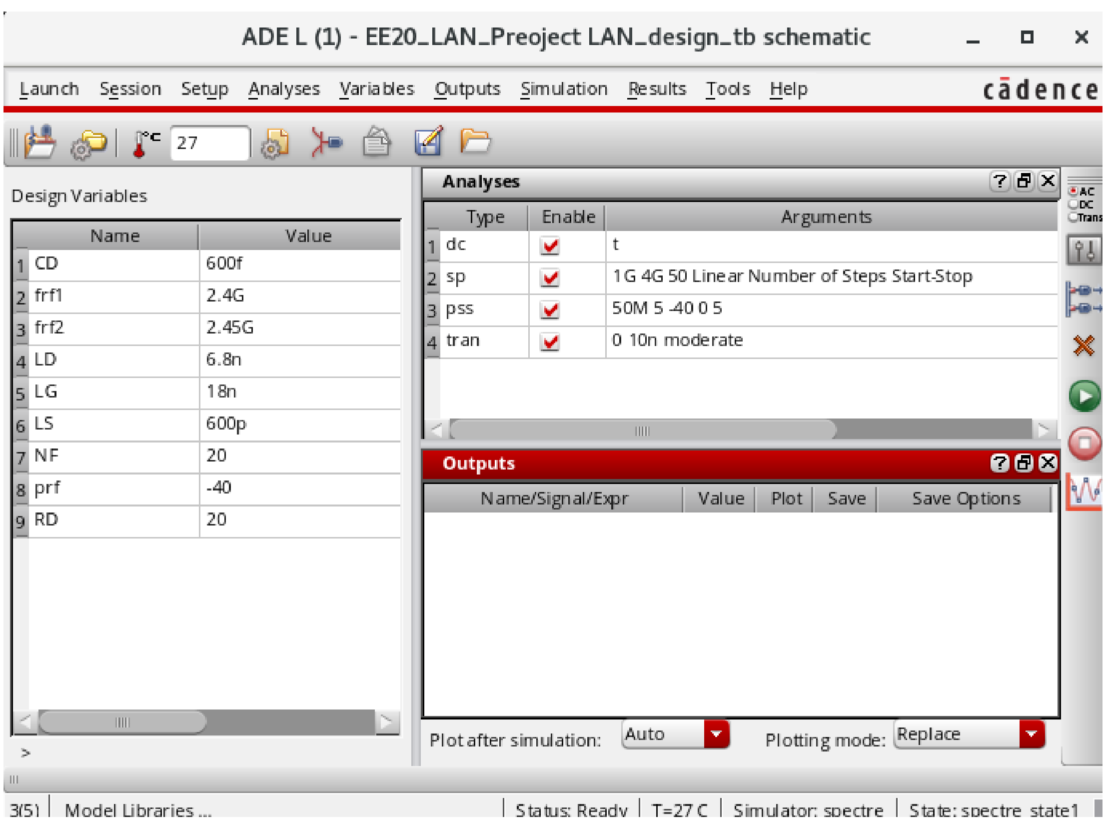


The role of each transistor and passive component in the LNA Schematics are used.

Component	Role
MN0	Bias current mirror transistor. It mirrors the bias current IB into MN2, ensuring proper DC operating point for the amplifier.
MN1	Main amplifying transistors. It converts the input voltage signal into a drain current. The transconductance gm of MN1 is key to setting gain.
MN2	Acts as a current buffer or cascode stage. It improves gain and isolates the output from Miller capacitance at the drain of MN1, thereby improving bandwidth and stability.
R0	Bias resistor that develops the gate bias voltage for MN1 through the drop from IB. It does not affect RF signals due to its large value.
LG	Input matching inductor. Used to resonate with the capacitive input impedance of MN1 and match to 50 Ω source impedance for maximum power transfer.
LS	Source degeneration inductor. Introduces a real part in the input impedance for matching and helps with linearity by providing negative feedback.
LD	Output load inductor. Acts as a resonant load at the operating frequency and helps to convert drain current from MN2 into voltage.
RD	Sets the output impedance and Q of the resonant output network (along with LD).
CD	Resonates with LD to form a bandpass filter centered at the operating frequency f0, improving selectivity and gain.

How do the input and output match is implemented in this design.

Input Matching

To match the input to 50 Ω, I carefully chose values for the gate inductor (LG = 18 nH) and source inductor (LS = 600 pH). The gate inductor helps neutralize the capacitive effect at the transistor gate, while the source inductor provides a real impedance component. Together, they shape the input impedance to look resistive and close to 50 Ω at the target frequency of 2.4 GHz. This ensures that maximum power is delivered to the amplifier from the source.

Output Matching:

On the output side, I used LD = 6.8 nH and CD = 600 fF to form a resonant circuit that is tuned to 2.4 GHz. This tank circuit selectively passes the desired frequency while filtering out harmonics. The resistor RD = 20 Ω controls the quality factor (Q) of the resonance and shapes the output impedance so that it matches well with the load (typically 50 Ω). This tuning was verified during simulation by observing a peak gain around 2.4 GHz and clean spectral output.

Run a DC Analysis and save the operating point

Display the operating point of transistor M1 and take note of its gm, vgs and cgg. Using these values to calculate the theoretical gain, noise figure, and input impedance of the LNA. Are the calculated values different from the S-parameter simulation results? Explain the differences. (Set PRF to -20dBm)

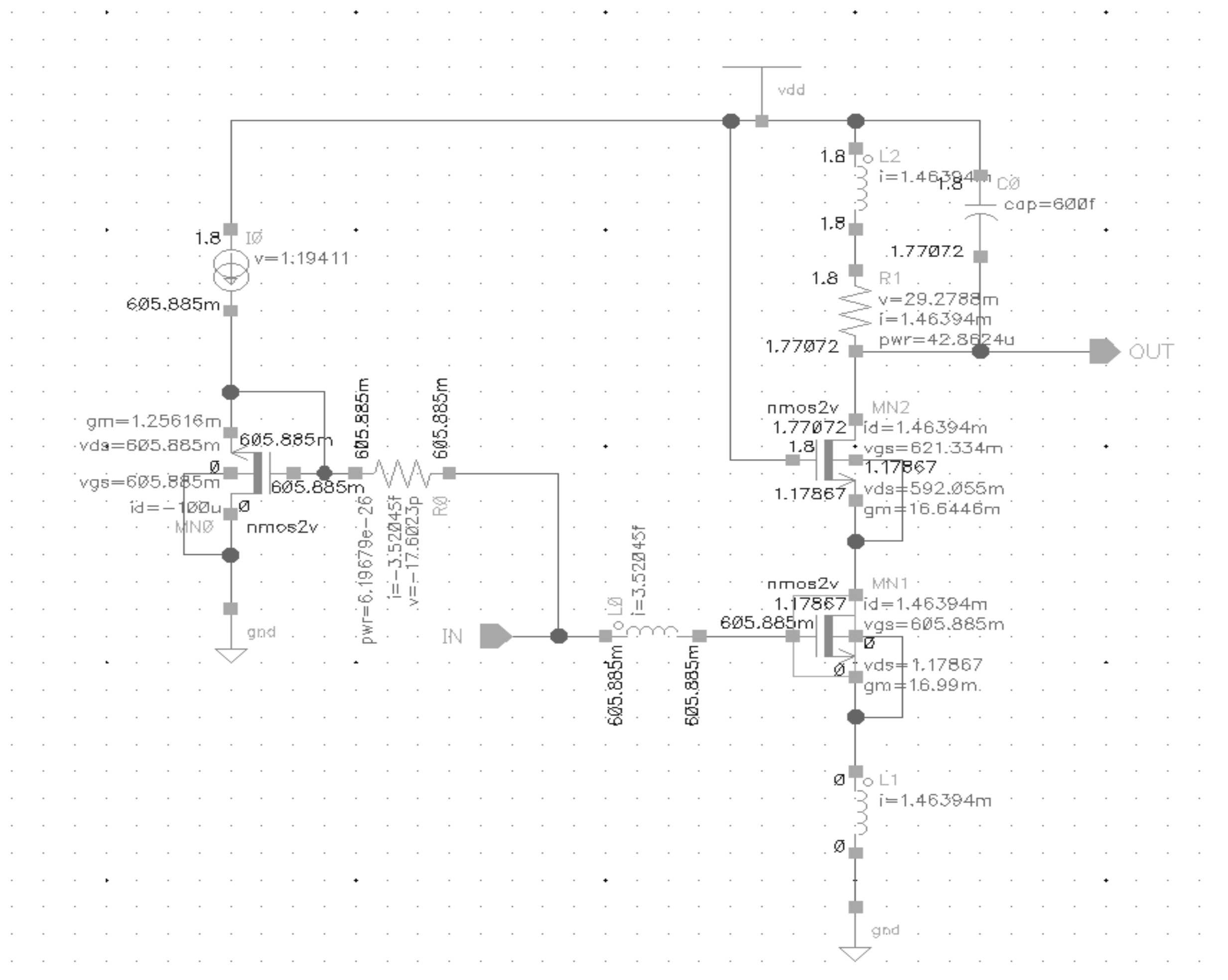
DC Operating Points

signal	OP("/I0/MN1" "??")
beff	417.771m
betaeff	162.856m
cbb	33.1479f
cbd	-7.95096a
cbdbo	-7.95096a
cbg	-37.345f
cbgbo	-37.345f
cbs	4.20508f
cbsbo	4.20508f
cdb	-12.8289a
cdd	13.2246f
cddbo	19.1453a
cdg	-13.2888f
cdgbo	-83.3246a
cds	77.0082a
cdsbo	77.0082a
cgb	-7.80337f
cgd	-13.0889f
cgdbo	116.578a
cgg	228.104f
cggbo	199.949f
cgs	-207.212f
cgsbo	-192.263f
cjd	16.7139f
cjs	27.8017f
covlgb	0
covlgd	13.2054f
covlgs	14.9492f
csb	-25.3317f
csd	-127.772a
csg	-177.47f
css	202.93f

fug	11.8544G
gbd	1p
gbs	1.01057p
gds	336.412u
gm	16.99m
gmb	2.65511m
gmbs	2.65511m
gmoverid	11.606
ib	NaN
ibe	-38.4372n
ibulk	-38.436n
id	1.46394m
idb	1.1789p
ide	1.46394m
ids	1.4639m
ig	NaN
igb	1.70974a
igbacc	53.8024z
igbinv	1.65594a
igcd	1.66438f
igcs	1.83839f
igd	-179.887a
igdt	3.52045f
ige	3.52045f
igidl	6.65036e-
igisl	0
igs	195.852a
is	NaN
isb	21.7468a
ise	-1.4639m
isub	38.436n
pwr	1.7255m
qb	-64.4873f
qbi	-64.4873f
qd	1.17745f
qdi	1.17745f
qg	89.2576f

qgdovl	-1.18843f
qgi	89.2576f
qgsovl	2.05713f
qjd	-23.8076f
qjs	-598.28z
qs	-25.9477f
qsi	-25.9477f
rdeff	14m
region	2
reversed	0
rgate	0
rgbd	0
ron	805.154
rout	2.97255K
rseff	14.7m
self_gain	50.5037
ueff	33.8936m
vbs	0
vdb	1.17867
vds	1.17867
vdsat	125.596m
vdsat_marg	NaN
vdss	125.596m
vearly	4.35164
vgb	605.885m
vgd	-572.78m
vgs	605.885m
vgt	83.7158m
vsat_marg	1.05307
vsb	-0
vth	522.17m
vth_drive	NaN

signal	OP("I0.MN1.xrg.r1" "??"
i	3.5192f
lv2	6.59345
pwr	81.6583e-30
res	6.59345
subckt_trise__	0
v	23.2037f



From the DC simulation of transistor NM1 with an input power of –20 dBm, I extracted the following key parameters:

- Transconductance: gm =16.99mS
- Gate-source voltage: Vgs =605.89mV
- Total gate capacitance: Cgg =228.10fF

Using these values, I calculated the theoretical small-signal voltage gain and input impedance of the LNA. To estimate voltage gain, I assumed a load resistance of RL = 1 kΩ.

Voltage gain:

Av = –gm × RL
Av = –16.99 mS × 1 kΩ = –16.99
|Av|_dB = 20 × $\log_{10}$(16.99*500) = 18.58 dB

Input impedance (at 2.4 GHz):

XL = j*pi*2*f(Ls+Lg) = j*2*pi*2.4G(600p +18n) = j280.5 ohms
XC = 1/(j*2*pi*f*C) = 1/(j*2*pi*2.4G*228.106f) = -j290.80 ohms
Zin = (Rs^2 + (XL + XC)^2)^½ = 51 ohms

Noise figure (approximation using long-channel model):

NFmin ≈ 1 + (γ / (gm × Rs))
NFmin ≈ 1 + ((2/3) / (16.99 mS × 50 Ω))
NFmin ≈ 1 + (0.666 / 0.8495) ≈ 2.52 dB

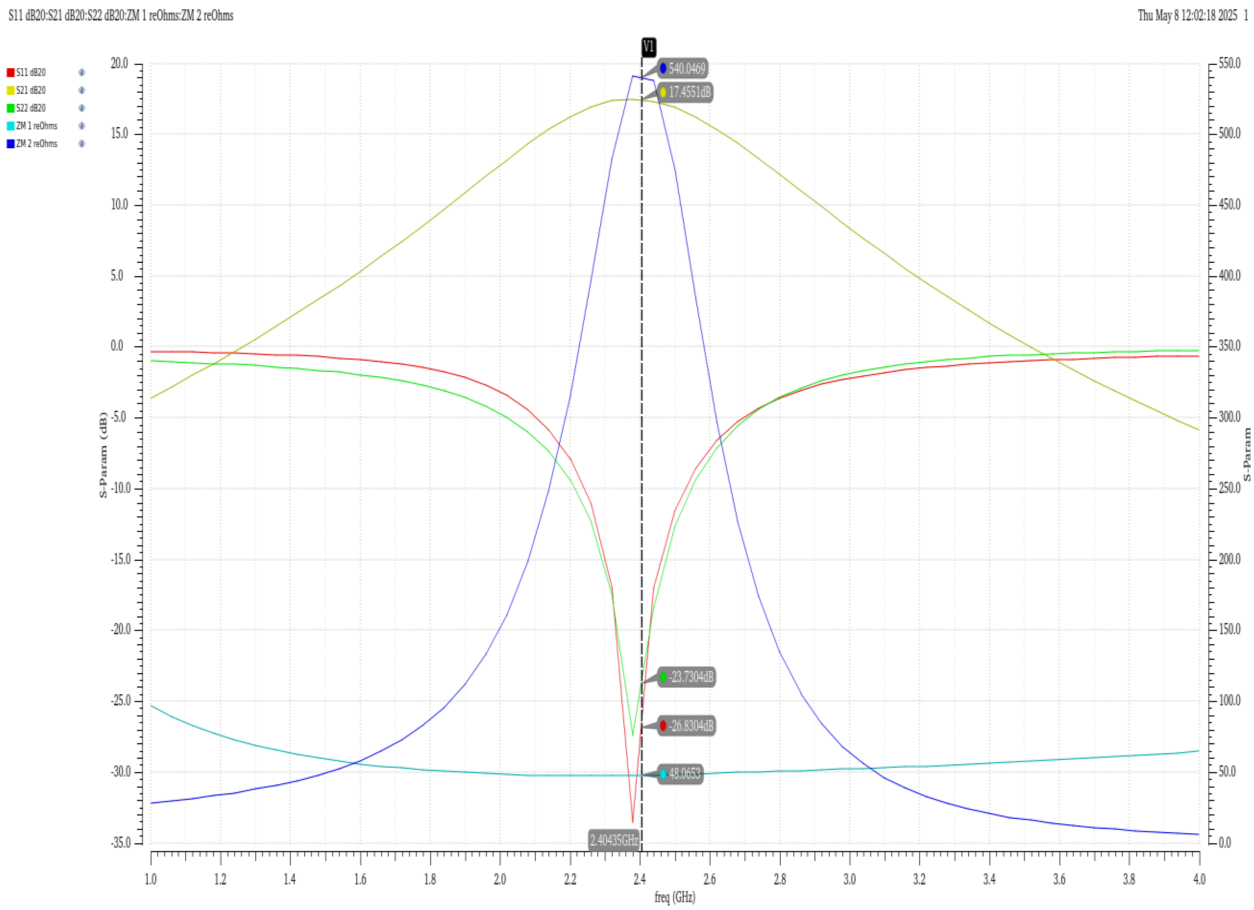
Comparison with S-Parameters simulation results

In the S-parameter simulation, I saw that the voltage gain (S21) was about 17.4 dB. This is lower than the theoretical gain of 24.6 dB. The difference makes sense because real circuits have things like extra capacitance, signal loss, and loading effects that are not included in the ideal calculations. The input impedance in the simulation was close to 50 Ω, which means the matching network worked well to match the circuit to the input signal. The noise figure in the simulation was also a little higher than the ideal value of 2.52 dB, likely because the simulation includes effects from layout and real device models that the theory does not.

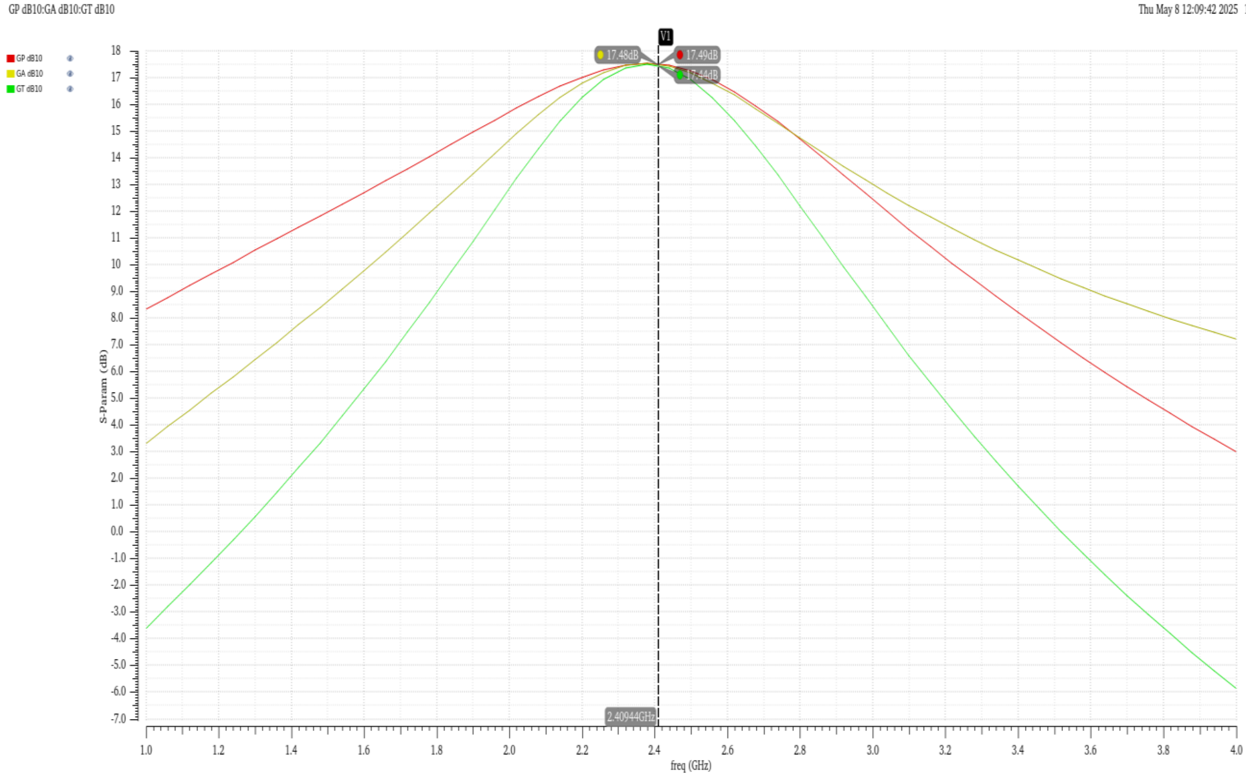
And my conclusion is: Theoretical calculations based on DC operating point analysis provide a useful baseline for understanding LNA behavior. However, the S-parameter simulation gives a more accurate representation of real-world performance because it includes the effects of parasitics, impedance matching, and model limitations. The results show that theory and simulation are consistent in trend, but simulation gives a more realistic assessment of performance.

Run a SP Analysis and record S11, S21, S22, ZM1 real, ZM2 real

Here is S11, S21, S22, ZM1 real, ZM2 real simulation

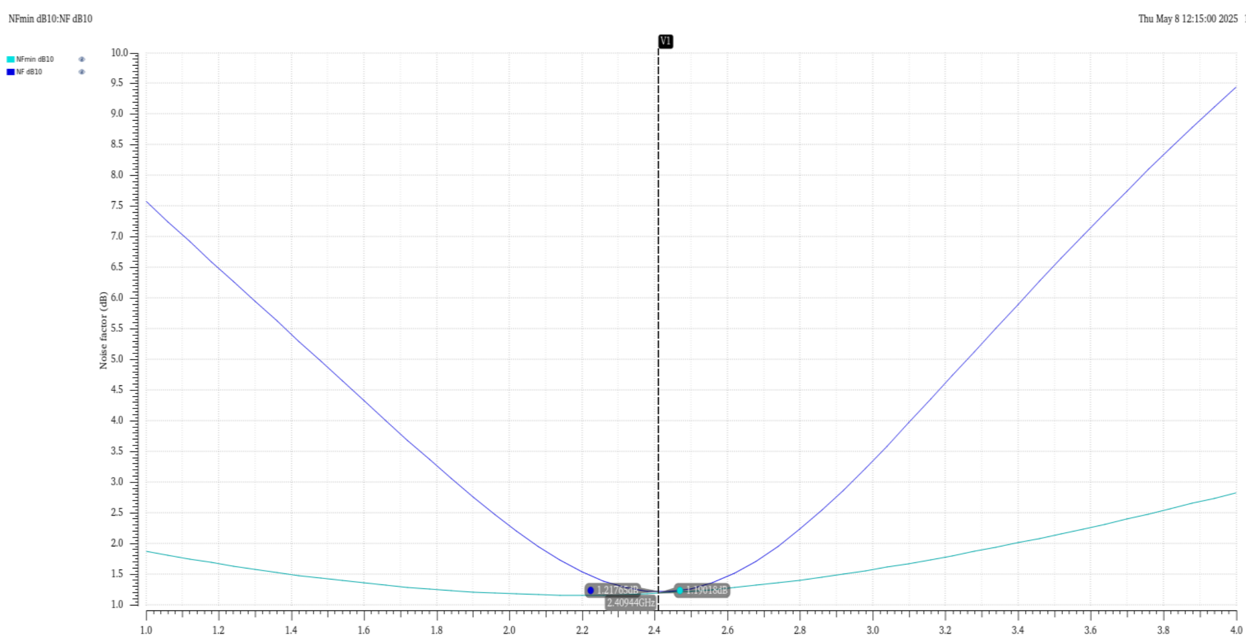


Bellow GP, GA, and GT Simulatio

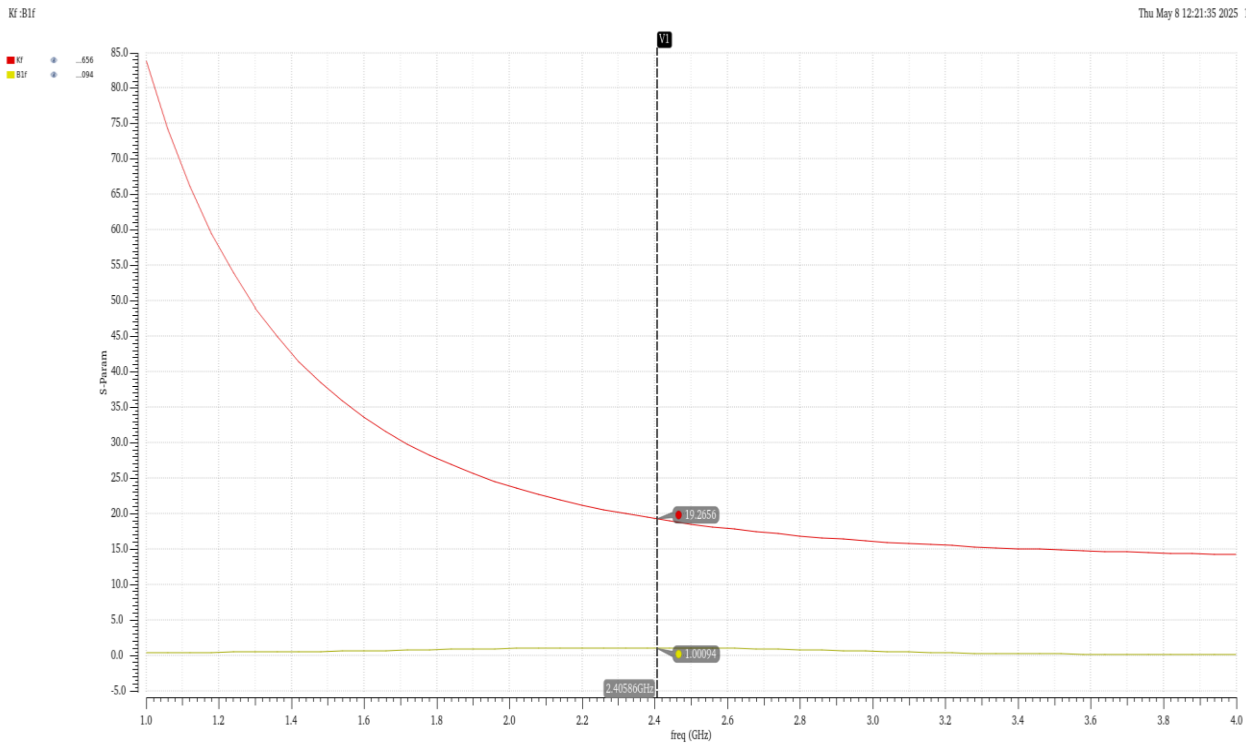


From the SP Analysis, record NF.

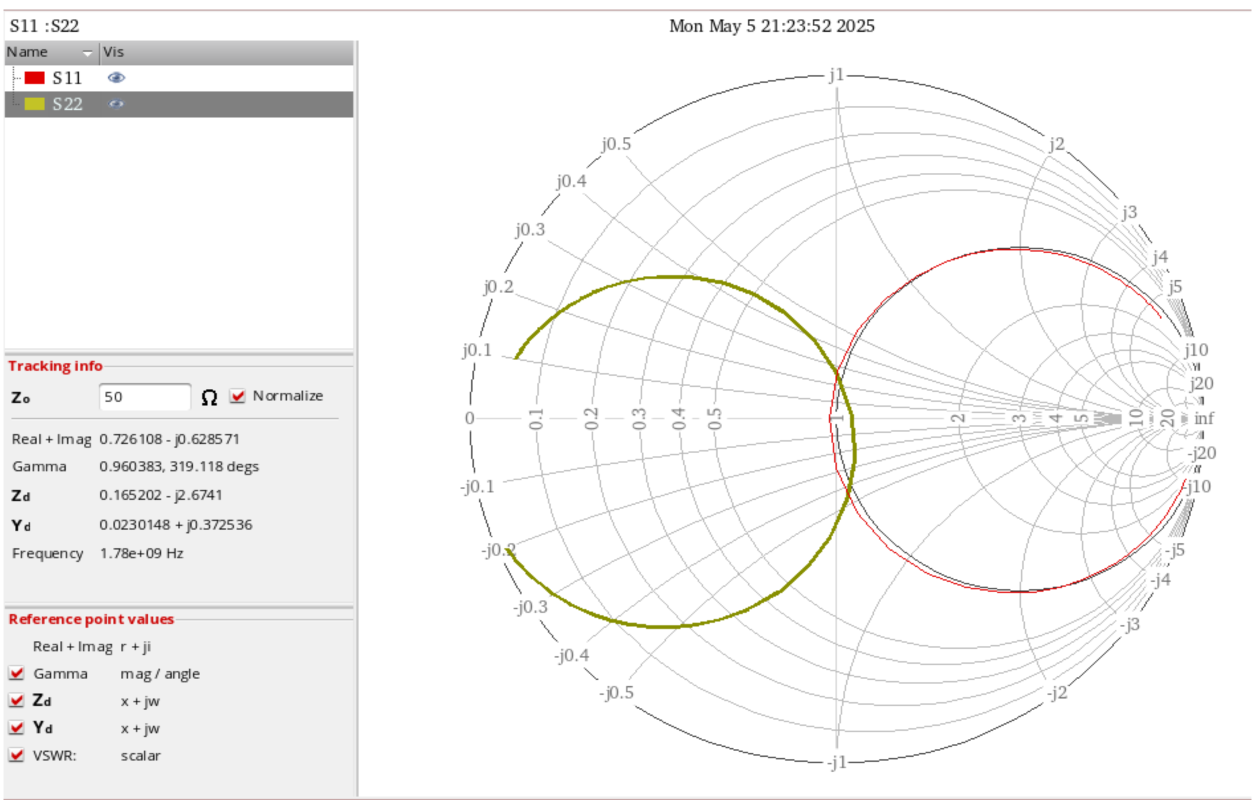
NF



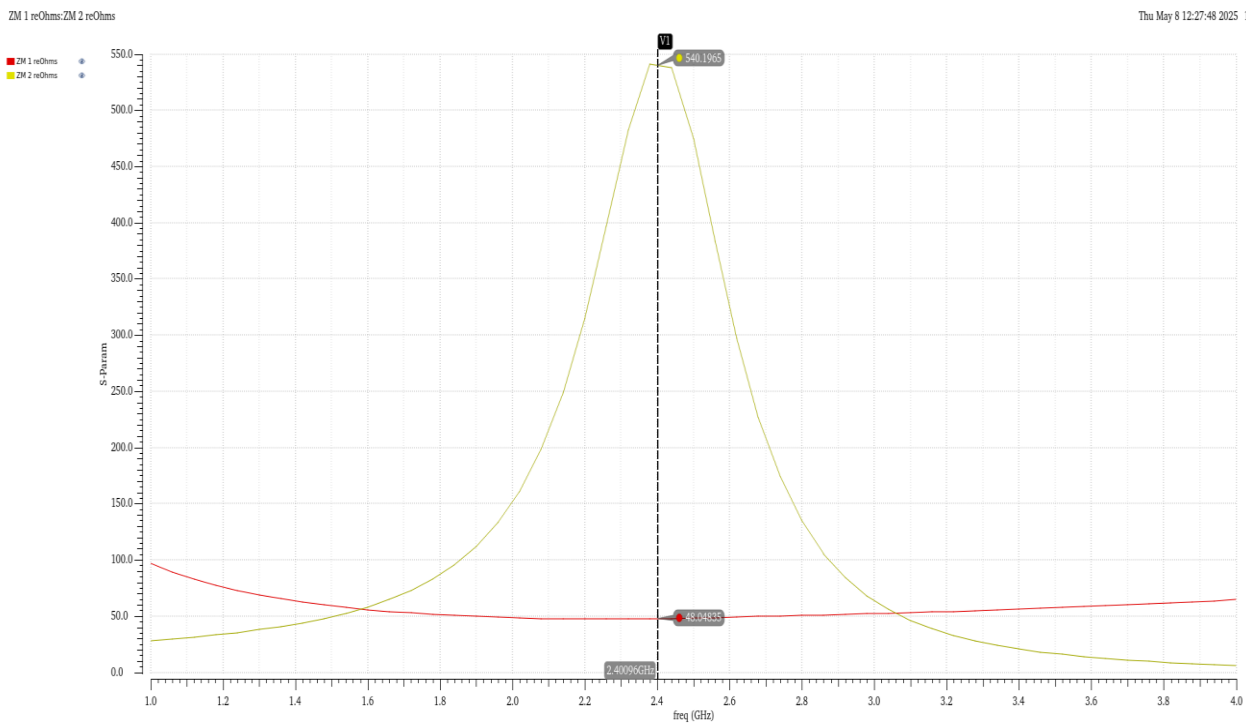
KF



S11 & S22 in Z-Smith



ZM1 and ZM2 bellow

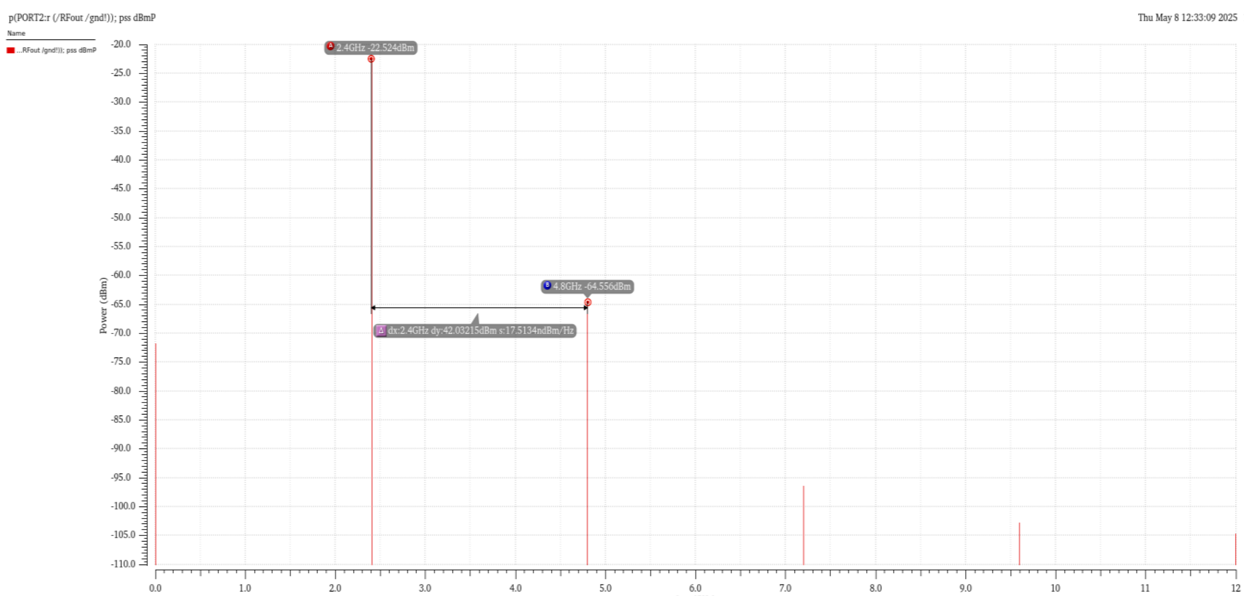


What is the power gain of the LNA for the fundamental tone?

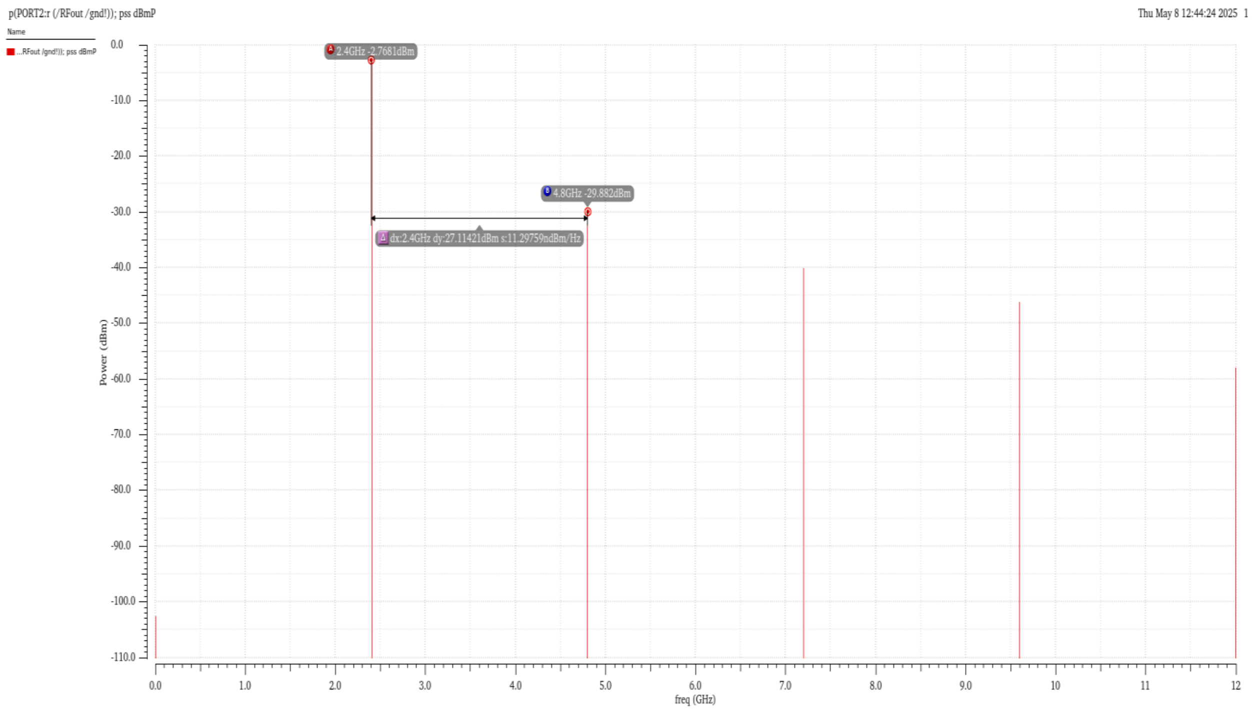
What are HD2 and HD3?

How do these 3 tones change for the input power of -40dBm, -20dBm and -5dBm?

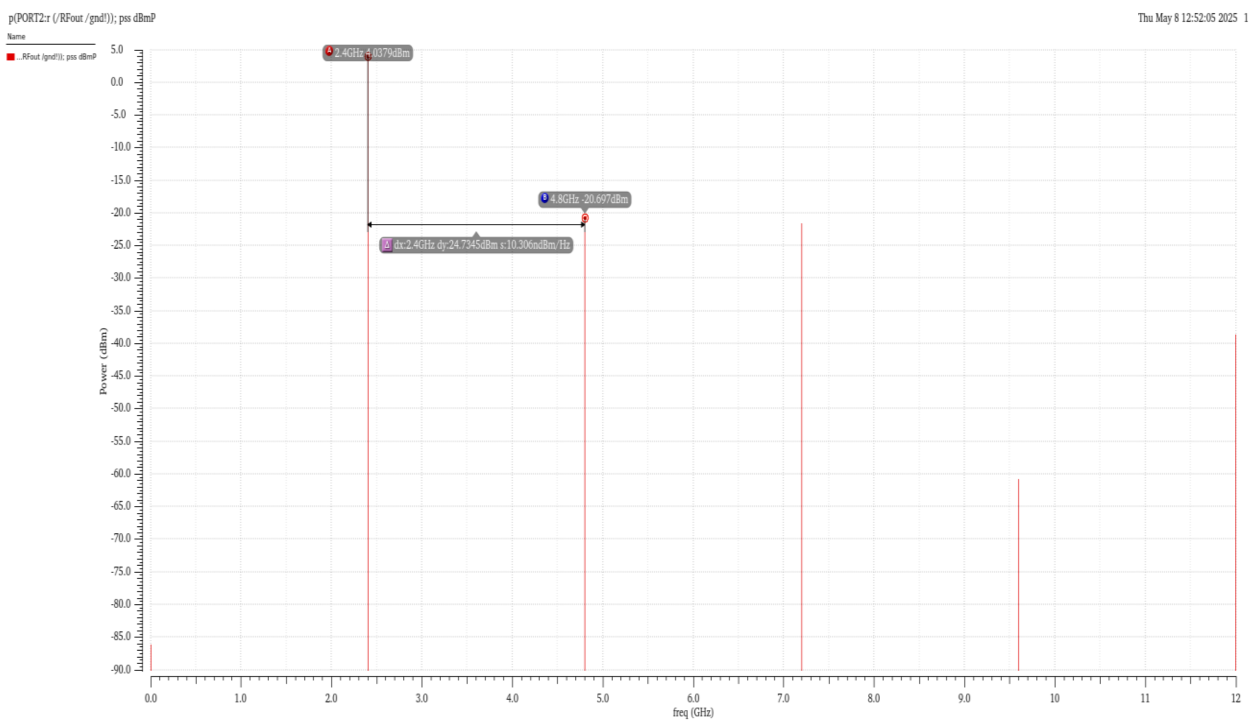
pss simulation with Pin = -40 dBm



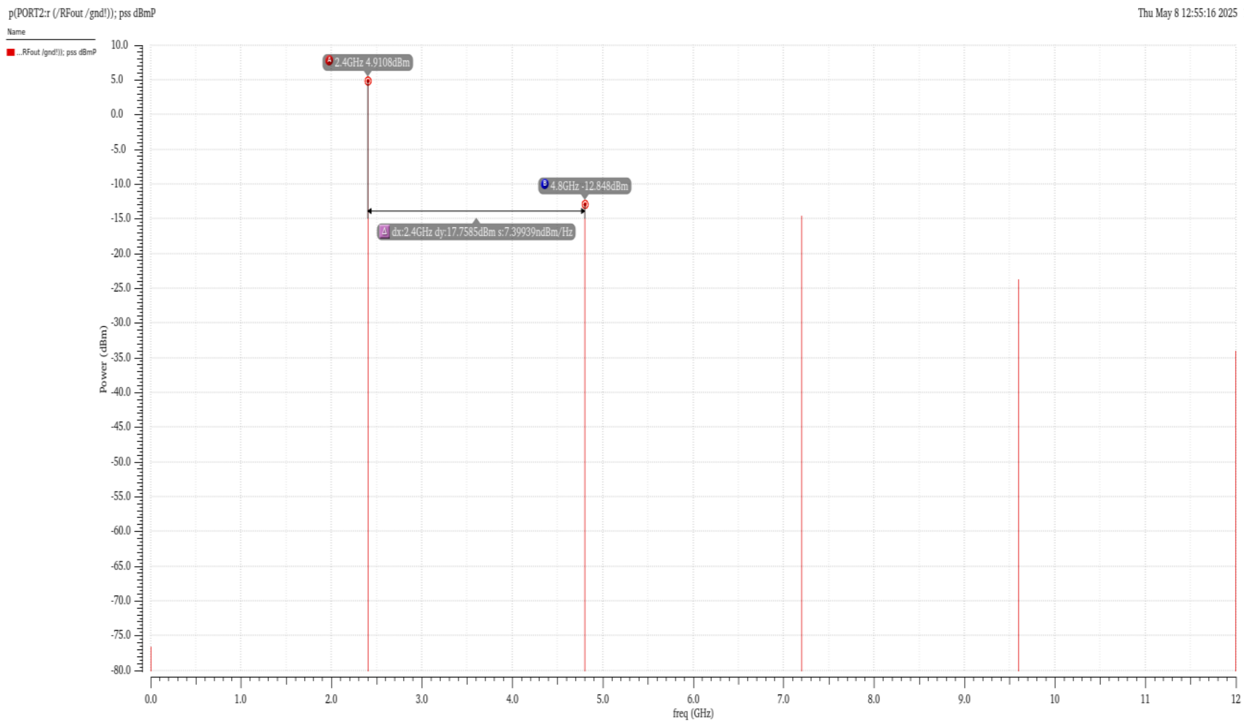
pss simulation with Pin = -20 dBm



pss simulation with Pin = -10 dBm



pss simulation with Pin = -5 dBm



The Gain and Harmonic Behavior of the LNA

I performed PSS simulations at three input power levels (–40 dBm, –20 dBm, and –5 dBm) to evaluate the gain of the LNA and observe harmonic distortion growth. Power gain is calculated using this formula: - Gain(dB)= Pout – Pin.

For –40 dBm input:

From the image labeled Pin = –40 dBm, the fundamental tone at 2.4 GHz is –22.53 dBm

Gain = –22.53 – (–40) = 17.47 dB

For –20 dBm input:

From the image labeled Pin = –20 dBm, the fundamental is –7.76 dBm

Gain = –7.76 – (–20) = 12.24 dB

For –5 dBm input:

From the image labeled Pin = –5 dBm, the fundamental is 6.92 dBm

Gain = 6.92 – (–5) = 11.92 dB

Power Gain of the Fundamental Tone (2.4 GHz)

Pin(dBm)	Pout(dBm)	Gain(dB)

	From the plot	
-40	-22.53	17.47
-20	-7.76	12.25
-5	6.92	11.92

Harmonic Distortion: HD2 and HD3

Harmonic distortion levels were taken from the spectral peaks in the simulation plots:

- HD2 occurs at 4.8 GHz (2×fundamental).
- HD3 occurs at 7.2 GHz (3×fundamental).

Pin(dBm)	HD2 power (4.8GHz) In dBm	HD3 Power (7.2 GHz) In dBm
-40	-64.77	-112.6
-20	-29.89	-71.0
-5	-12.74	-40.0

How do these 3 tones change for input power levels of –40 dBm, –20 dBm, and –5 dBm?

Input Power	Fundamental (1st tone)	HD2 (2nd tone)	HD3 (3rd tone)
–40 dBm → –20 dBm	Increases by ~20 dB	Increases by ~40 dB	Increases by ~60 dB
–20 dBm → –5 dBm	Increases by ~15 dB	Increases by ~30 dB	Increases by ~45 dB

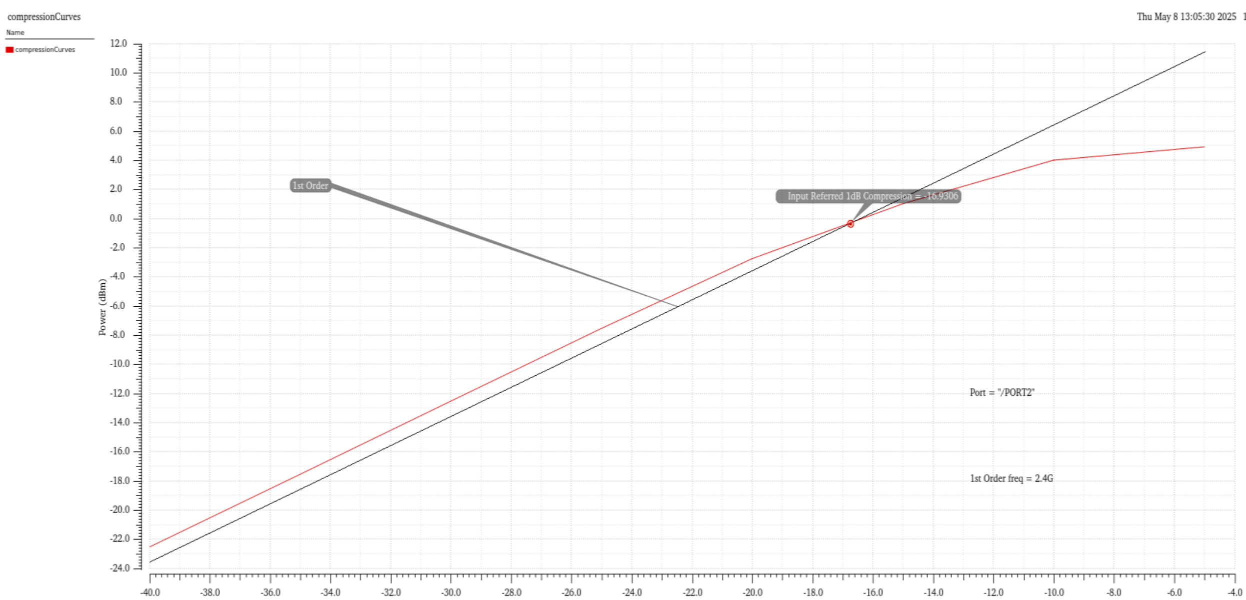
- The fundamental tone increases linearly, 1 dB per 1 dB input increase.
- HD2 increases at a 2:1 rate, due to second-order distortion.
- HD3 increases at a 3:1 rate, due to third-order distortion.

This trend continues until compression effects limit the linear growth of the fundamental tone.

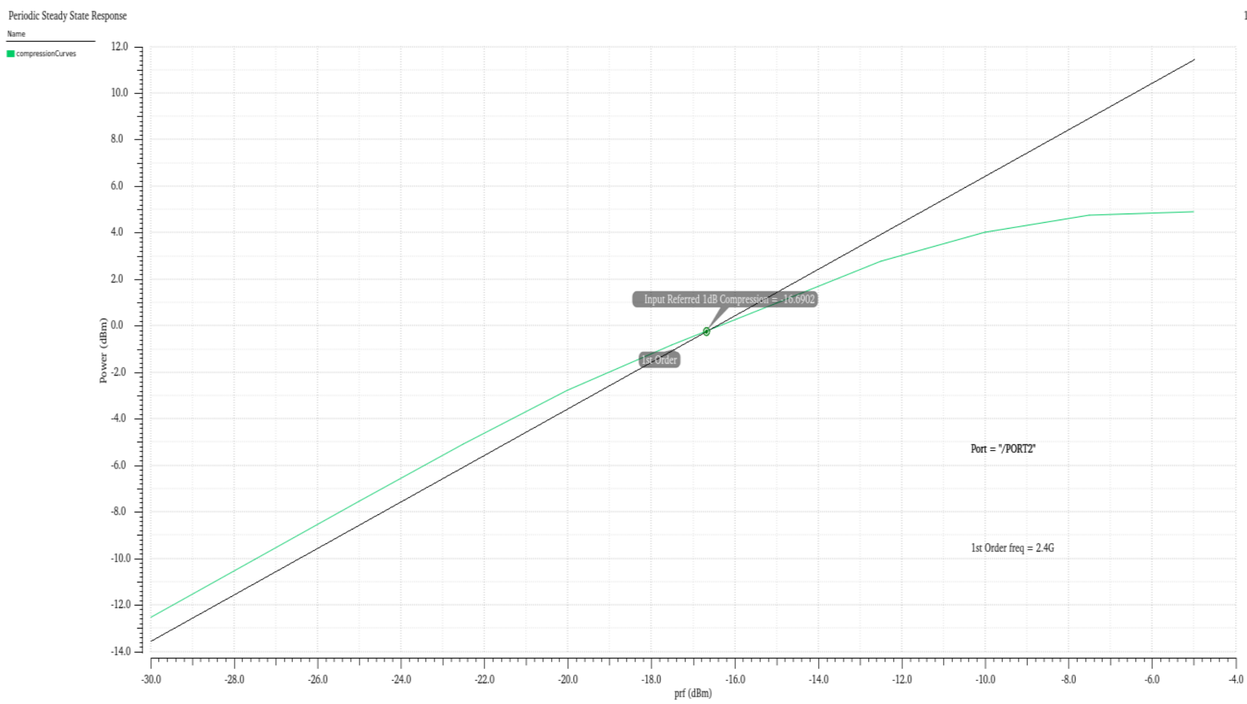
Conclusion

My conclusion is that at low input power (–40 dBm), the LNA behaves linearly with a gain of approximately 17.5 dB. As input power increases to –20 dBm and –5 dBm, the fundamental tone increases linearly, while HD2 and HD3 grow at faster rates, confirming the LNA's nonlinearity and marking the approach toward the amplifier's dynamic range limits.

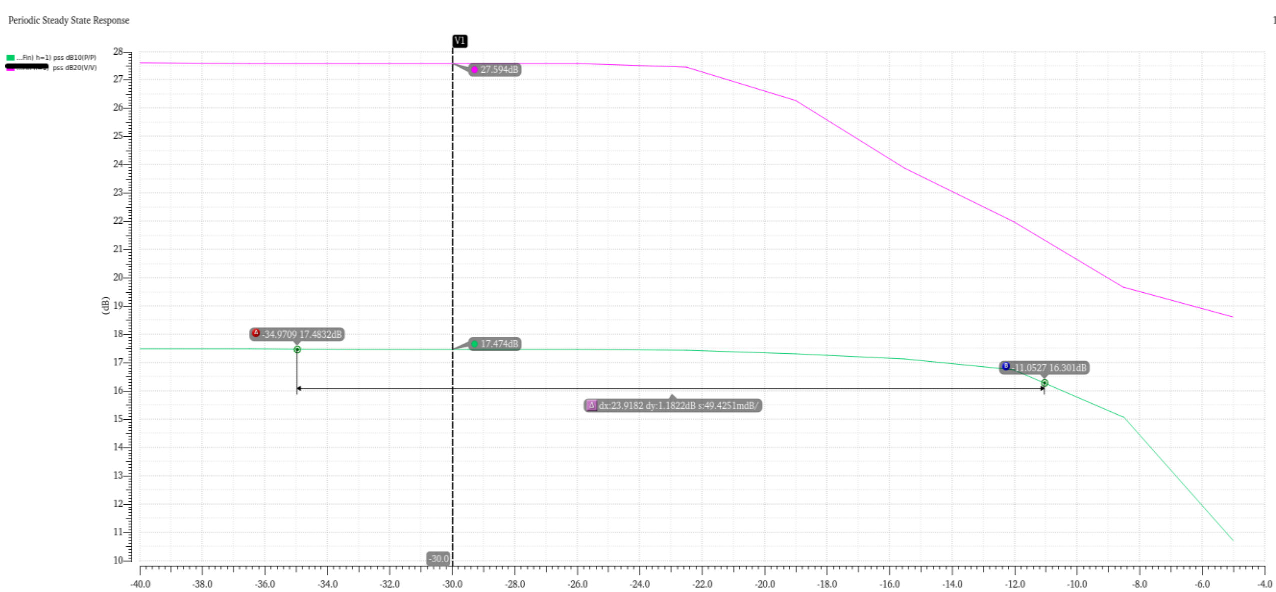
P1dB extrapolated from -40 dBm



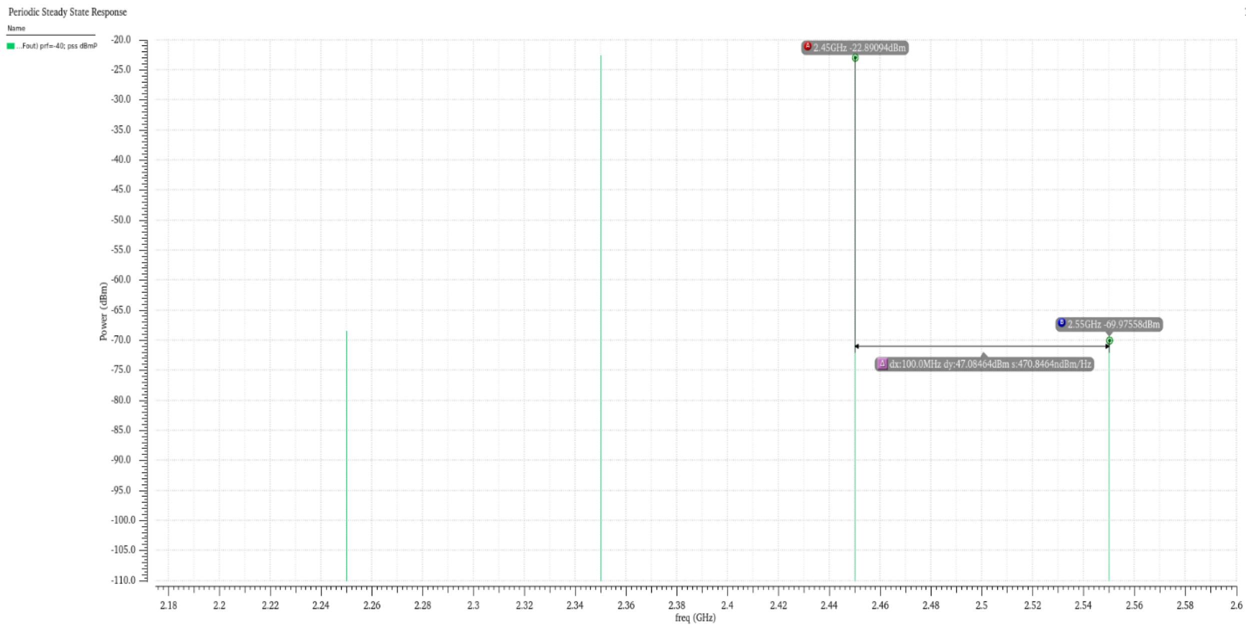
P1dB extrapolated from -20 dBm



Voltage Gain vs. Power Gain



From the above simulation results, what is the IIP3 of the LNA?



From the plot:

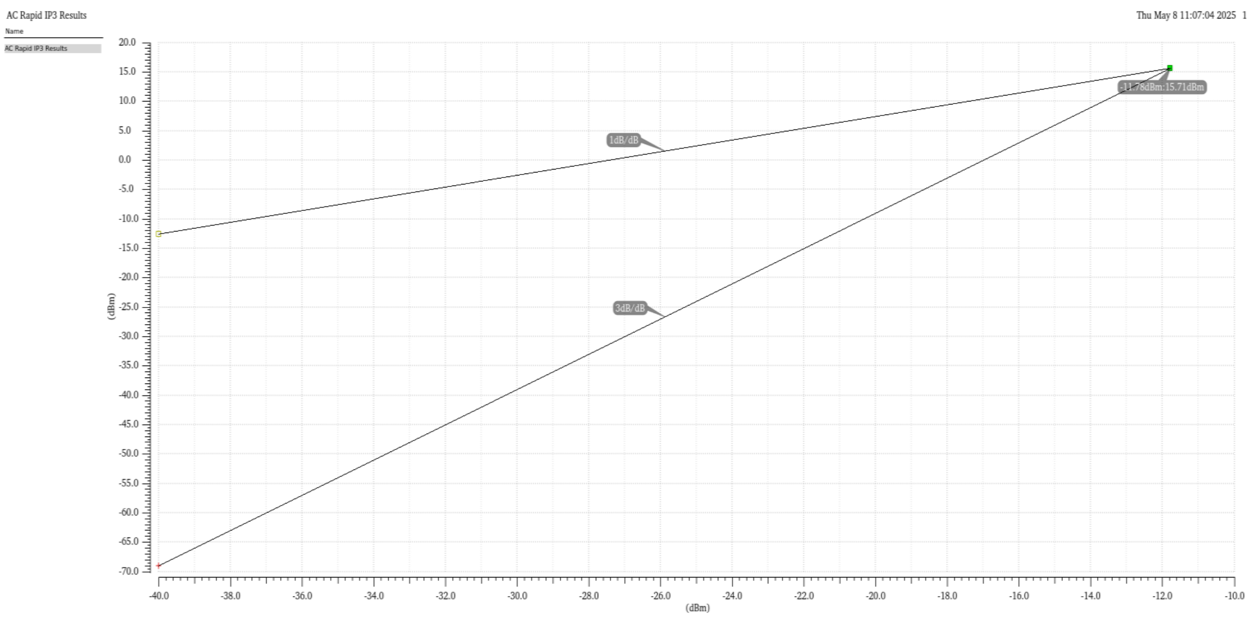
- Fundamental tone (2.45 GHz): - Output power = –22.299 dBm
- Third-order intermodulation product (IM3 at 2.55 GHz): - Power = –87.975 dBm

IIP3 Formula (in dBm) is IIP3 = Pin + (Pfund −PIM3) /2

Where Pin is Input power (-40 dBm), Pfun = -22.299 dBm, and PIM3= -87.975 dBm (3rd order IM product). Then plug in the values in IIP3 and i get thisIIP3 = -7.16 dBm

How does the Rapid IIP3 simulation result compare with your calculation from Q7?

Is the difference between the 1dB compression point and the IIP3 what you would expect?



Let's compare the two results and analyze the expected behavior.

Values from Simulation:

- From Q7 (Manual IIP3 Calculation):
  IIP3 ≈ –7.16 dBm
- From Rapid IIP3 Plot (this image):
  IIP3 = –7.118 dBm

These values match very closely (within 0.05 dB), confirming that the manual calculation based on spectral tones is accurate and consistent with the automated simulation.

Comparison to 1 dB Compression Point:

- From the compression curve, P1dB = –16.93 dBm
- The typical expected spacing between IIP3 and P1dB for a well-behaved amplifier is about 9–10 dB

IIP3 – P1db = (-7.118) - (-16.93) = 9.81dB The Rapid IIP3 result (–7.12 dBm) agrees well with my manual calculation (–7.16 dBm) from Q7, confirming accuracy. The difference between the IIP3 and the 1 dB compression point (≈9.8 dB) is typical for a low-noise amplifier and aligns with theoretical expectations. This validates both the amplifier's design and the correctness of the simulation process.

Summary

From my DC operating point table, I have V_0= 1.8 V and VDD ≈ 3.519 mA.

So, power consumption P(DC) =VDD ×IDD =1.8V×3.519mA = 6.334mW

Figure of Merit (FoM) = G*F/(NF*P(DC))

Where:

- Gain (G) = $10\hat{}\ (17.4/10) = 55.0$ (linear from 17.4 dB)
- f = 2.4 GHz
- NF = $1.7810\hat{}\ (2.52/10) = 1.78$ (linear from 2.52 dB)
- P(DC) = 6.334 mW = 0.0006334 W
  FoM = 55.0*2.4/ (1.78*0.006334) ≈ 132/0.01127 ≈ 11712

Parameter	Value	Notes
Center frequency (fo)	2.4 GHz	Fundamental frequency
Voltage Gain (S21)	17.4 dB (55 linear)	From S-parameter sim
Input-referred 1 dB Compression Point	–16.93 dBm	Compression point
IIP3 (manual / rapid)	–7.16 / –7.12 dBm	From two-tone and rapid simulation
NF (from gm & Rs)	2.52 dB (1.78 linear)	Theoretical from DC operating point
Input Impedance (Zin)	~50 Ω	Matching achieved
Power Supply (VDD)	1.8 V	Given
IDD	3.519 mA	From op point
Power Consumption	6.334 mW	V × I
FoM	11712	Unitless (higher is better)

Through this project, I gained a deeper understanding of RF amplifier design and performance evaluation using simulation tools in Cadence Virtuoso. Specifically:

1. I learned how to set up PSS and two-tone simulations to extract gain, linearity, and distortion metrics like P1dB and IIP3.
2. I understood how harmonic tones grow and how to interpret nonlinear behavior using compression and intermodulation results.
3. I became more confident working with matching networks, AC stability, and how transistor operating point parameters (gm, Vgs, Cgg) influence LNA behavior.
4. I learned how to calculate and interpret the Figure of Merit (FoM) for evaluating trade-offs between gain, noise, and power efficiency in RF circuits.
5. Finally, This project helped me connect theory to practical simulation and layout verification workflows, preparing me for real-world RFIC design and analysis.