EE 371 Project 3

Designing an Underwater Digital Scanning System….

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Introduction:

Luigi Bellabarca, long a famous and beloved gondolier working the canals of Venezia, has recently learned of Earthlife and wants to join the program to help to restore the original beauty and pristine nature of the waters in and around his city. To this end, he has decided that he needs to study and understand the present conditions beneath the waters on which he has lived and worked for many years. To aide in this study, he has hired your company, *Scanning Far and Wide International* to design and build a control system for a digital scanning / imaging system that will installed on a number of gondolas and used to collect detailed data on the canal's environment and current state. The prototype system will demonstrate two scanners that can continuously collect a variety of image data.

Because the data storage aboard the gondolas will be limited and his goal is to scan or sample continuously, the imaging system must periodically transfer the collected data to any one of a number of stations along the canals. To meet such a requirement, the basic configuration must comprise a minimum of two scanners and each must have a data buffer associated with it.

Prerequisites:

Familiarity with the Quartus II development environment and the *Signal Tap* (nope still ain't *Spinal Tap*) logic analyzer will definitely help. A continued willingness to learn and to explore. No birra or Barbera del Monferrato until the project is completed and you can turn on a several LEDs indicating the status of your scanner system. Hey, these are all still good.

Musings:

Are cross purposes really angry or just a little upset? If C and C++ support casting integers and floats, why don't they also support casting aspersions? Can fishermen cast aspersions? Why do the same kinds of animals make different sounds in different countries? Do they really learn to speak the local language? If a Chinese rooster comes to the U.S., does it crow in English or Chinese? Which dialect? Does it have an accent? If you told a French dog to lay down, would it understand? Why is Donald Duck a duck not a drake? Is it possible to defenestrate an elephant? What would happen if an elephant swallowed a mangle wurtzel then sneezed? If water going down a toilet goes anticlockwise south of the equator, do bottles and jars open clockwise? Is it true that when Luigi goes home at night, his boat really becomes a gone dola.

Observations:

With the latest in high tech ultra child-proof containers, only the truly intelligent children will be able to open the medicine bottles and ingest what they shouldn't. Kind of makes an interesting statement, doesn't it.

Background:

Have some knowledge of the C language and ability to develop simple C programs. Have a working understanding of basic methods of system I/O such as switches and LEDs.

For this project, you should understand and know how to:

1. Start from a textual description of the behaviour of a system,
2. Extract the behavioural requirements from the textual description,
3. Express the requirements in a state diagram,
4. Utilize the Verilog HDL to formulate a physical model of the state diagram as a finite state machine (FSM) taking into consideration real-world constraints,
5. Test the model to ensure concurrence with the specified requirements,
6. Synthesize the model onto an FPGA
7. Test the physical implementation to ensure concurrence with the specified requirements.
8. Be comfortable working with and utilizing the Signal Tap logic analyzer.

Objectives:

The major objectives of this project follow those of the previous and include:

- Continue to use knowledge and understanding of FSMs and HDL modeling to execute the design and test of a basic real-world system.
- Continue to work with simple I/O and selection and routing logic to model the source and destination of signals into and out of a digital system.
- Extend and apply the basic concepts of a time base and intra system timing and timing constraints.
- Continue to work with and follow the formal development cycle.
- Continue to work with basic C variables and their addresses.

High Level Requirements

Overview

The objective is to design and build a control system for a portion of a digital scanning system to be mounted on gondolas traveling back and forth along the canals. A network of such scanners will be used for executing a detailed mapping of the state of environment in and along the bottoms of the canals as part of the ongoing research into identifying possible environmental damage, potential root causes, and possible solutions to repair and restore the original water quality. The prototype system, to be contained aboard a single gondola, will demonstrate a two scanner system that can continuously collect a variety of data and, on command, transfer the collected data to a station along the canal.

Detailed Requirements

The required system operation is as follows.

- A scanner will collect data until its buffer is 80% full.
- When the data buffer is 80% full, the system will contact a station to request permission to transfer and generate a signal that can be used by other onboard scanners to wake up and go to the standby state.
- When the data buffer is 90% full, the system will generate a signal that can be used by other scanners to move from standby to collecting mode.
- When the buffer is 100% full and a transfer command transfer command has been received, the system will transmit the stored data to a collection station. The transfer takes approximately half as long as collecting.
- When the buffer is 100% full, if transfer command has not been received, the scanner enters the idle state. If the transfer command is received before the second scanner has filled its buffer to the 50% point, the transfer process proceeds otherwise, the scanner clears the buffer, and powers down. Clearing the buffer takes half as long as collecting.
- For test purposes, the state of the system should be displayed for easy user viewing.

High Level Design Requirements

Operation

Internally, the system comprises a memory system and an imager control system. The memory system may be modeled using a basic counter.

Commands, typically sent from a station, can be entered via a set of switches.

The required system operation is as follows.

- When a system is not scanning, transferring, or flushing, it should enter the *LowPower* state.
- When a scanner is issued a *StartScanning* command, it enters the *Active* state, begins scanning, and issues a *Scanning* status indicator.
- When the data buffer for the active scanner is 80% full, the system issues a *ReadyToTransfer* signal to a local station to request permission to transfer and a *GoToStandby* command to the second scanner.
- When the data buffer is 90% full, the system generates *StartScanning* signal for other scanner. The second scanner comes out of the *Standby* state, enters the *Active* state, and begins scanning.
- When the buffer is 100% full and if the active scanner has received a *Transfer* command, the system shall transmit the data to the local station then enter a *LowPower* state.
- When the buffer is 100% full and permission has not been granted to transfer, the scanner enters the *Idle State*. If the transfer command is received before the second scanner has filled its buffer to the 50% point, the transfer process proceeds as normal otherwise, it enters a *Flush* state and clears the buffer. When the flush or transfer operation completes, the scanner enters the *LowPower* state.
- All output signals are active low.
- All input signals are active high.
- All times are specified in local units.

Learning the C Language – The Next Steps:

We will conclude this project by introducing and working with variables and data types in the C language.

1. Write a program that prompts for a temperature value, the scale, Celsius, Fahrenheit, or Kelvin and the scale to which that temperature is to be converted. Display the result in the requested scale. Think about an informative way to print the answer.

2. When designing high-speed circuits, it is often very important to know the delay from the point where the signal enters the path until it leaves.

   The delay of a signal propagating along a printed circuit board trace is 180 picoseconds (10^{-12} seconds) per inch. The delay through a logic device is approximately 5 nanoseconds (10^{-9} seconds). Assume that the logic devices are placed on the circuit board with a printed circuit board trace of 0.1 inches connecting the output of one device to the input of the next.

   Write a program that prompts the user for the number of logic devices in a signal path and displays the total delay along the path. Think about an informative way to print the answer.

Deliverables:

A lab demo showing…

1. The design and working implementation of the digital scanner control system that meets the specified requirements.
2. The design and working implementation of the two C programs.

A short lab report including…

1. The report should follow the guidelines on the class webpage. Be certain to include an abstract, introduction, general description of your hardware and software design, discussion of any problems that you had with the development of the project, a summary, and a conclusion.
2. The annotated Verilog source code for all applications on the DE1-SoC board and the C code for the two C exercises.