INTERNSHIP PROJECT REPORT

Keypad-Controlled Password Lock System

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Project Synopsis

This project, developed during my internship, involves the design and implementation of a digital password lock system using Verilog HDL on the Xilinx Vivado platform. The system uses a 4x4 matrix keypad for user input and verifies a preset password to control a digital lock. The design was modularized and verified through simulation.

Brief Overview

The Password Lock System operates by scanning user inputs from the keypad, matching them against a stored password, and activating a lock/unlock signal accordingly. The system includes three major modules:

- Keypad Scanner: Detects key presses and outputs the corresponding key value.

- Password Matcher: Verifies the input sequence with the stored password.

- Top Module: Integrates the subsystems and interfaces with simulation/testbench.

The system was tested successfully with clear waveform outputs, ensuring accurate detection and validation of the password sequence.

Technologies and Tools

- HDL: Verilog (pure, synthesizable)

- Simulation and Synthesis Tool: Xilinx Vivado

- Waveform Viewer: Vivado XSim

- Platform: Windows 10

- Other: GitHub for version control and repository creation

Development Process

1. Planning and Design:

- Defined the password logic and input mechanism.
- Broke down functionality into scanner and matcher modules.

2. Module Implementation:

- Developed the keypad_scanner.v to handle keypad interfacing.
- Built password_matcher.v to verify input sequences.

3. Simulation and Debugging:

- Created tb_top.v for functional verification.
- Debugged timing and logic errors using waveform output.

4. Validation:

- Simulated scenarios of correct and incorrect inputs.
- Verified "unlocked" signal assertion for valid password.

5. Optimization:

- Refactored logic in password_matcher.v to ensure reliability.
- Cleaned up RTL for GitHub-readiness and waveform clarity.

*Click the hyperlink to access the source code of project (GitHub repository).

Summary and Future Directions

This project demonstrates a secure and modular Verilog-based design for password-protected systems. All modules were synthesized and simulated successfully, showcasing both functional correctness and a clean digital workflow.

Future Enhancements may include:

- EEPROM integration for dynamic password storage.
- Buzzer/LED interface for user feedback.
- Retry limit logic with timed lockout for security.