Serial Protocols

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Serial Protocols

Protocols

Protocols means set of rules enable data to be transferred between devices to send and receive messages.

In the document explaining only 5 serial protocols

Types of Communication serial protocol

1. UART
2. SPI
3. I2C
4. CAN

Transmission Modes

Simplex Mode

Half Duplex Mode

Full Duplex Mode

Simplex Mode:

In Simplex Mode, the communication in unidirectional. Only 1 device will transmit and another device just receive the signal

Ex: Radio.

Half Duplex Mode:

In Half Duplex Mode, both way communication can happen but only 1 way at a time.

Ex: Walkie Talkie.

Full Duplex Mode:

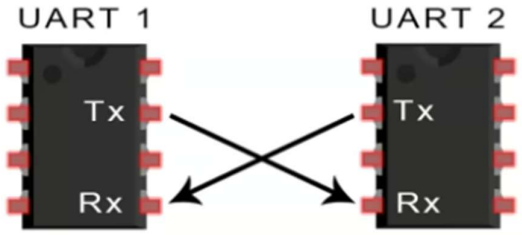
In Full Duplex Mode, both way communication can happen at the time simultaneously.

Ex: Telephone.

Serial Protocols

1. UART – Universal Asynchronous Receiver and Transmitter

UART is protocol that communicate between the two micro-controllers. The best part is that it uses only 2 wire to communicate such as TX and RX.



UARTs transmit data asynchronously, which means there is no clock signal to synchronize the output of bits from the transmitting UART to sampling of bits by the receiving UART. Instead of clock it contains the start bit, data bit, parity bit and stop bit. The UART uses a particular frequency to communicate is known as baud rate.

Baud rate – Number of signals transmitted per second is known as baud rate.

Bit Rate – Number of bits transmitted per second is known as bit rate.

Baud rate Calculation

The baud rate of 10% margin will be acceptable both transmitting and receiving side.

Standard baud rate used for the UART communication is **4800, 9600, 19200 and 115200**.

Example: Baud rate 9600. Fclk is Micro controller Uart peripheral frequency 72 Mhz. Find out Uart Div register value.?

Baud rate = Fclk/(16 * UARTDIV)

9600 = 72000000/(16 * UARTDIV)

UARTDIV = 468.75

Hex = 1D4

Convert into hex to feed into the register.

0.75 * 16 = 12

Hex = C

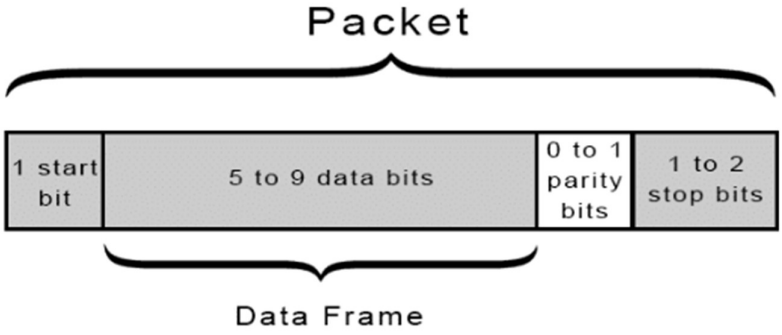
UARTDIV = 0x1D4C

How UART Works

UART will communicate between the 2 micro-controllers. The data is transferred from data bus to the transmitting TX using parallel form. Then it will add the start bit, parity bit and stop bit. The data is sent

serially. After receiving the data from the RX line, the data convert back to parallel and removes the start, parity and stop bit.

Data Bits



Start bit

The UART data transmission line held high voltage level when it's not transmitting the data. To start the data transfer, pull the voltage from high to low for 1 bit. when receiving end detects the high to low voltage transition, it begins to start reading the data.

Data Frame

The data frame contains the actual data being transferred. It contains 8 bits. In most of the cases LSB sent first.

Parity Bit

Parity is error detection method (even, odd or none). Parity will describe the evenness or oddness of the number. The parity the way of receiving the data changed during the transmission. Bits can be changed due to electromagnetic radiation, mismatched baud rates, or long distances. If the parity bit is 0 it means it's even number parity. If the parity bit is 1 it means odd number parity. When parity bit is matches it means transmission is successful without any errors.

Stop Bit

After the successful data transmission, the voltage is pulled low to high. It contains 1 bit.

Advantage

Only 2 wire requires for communication

No clock signal required for the communication

Disadvantage

Not supports to multi master and multi slave.

Baud rate must match within the range such as 10%.

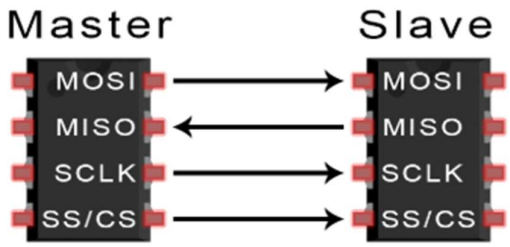
RS232 VS RS485

Feature	RS232	RS485
Speed	Slow (115 kbps)	Fast (1 Mbps)
Distance	Short	Long
Multi – Drop	No	Yes
Signal Style	Single Ended	Differential
Noise Immunity	Lower	Higher
Application	Short distance	Industrial

2. SPI – Serial Peripheral Interface

It is developed by the Motorola.

SPI it is used for the short-range communication. The SPI is an interface between the micro-controller and slaves like (sensors, display and memory device). It allows to high-speed data transmission. The maximum speed up to 10Mbps. It is full duplex communication. This protocol depends on the clock. The connection diagram as shown below.



The Pins Details:

MOSI – Master Out Slave In, Share the data from the master to the slave

MISO – Mater In, Slave Out Share the data from the slave to the master.

SS – Slave Select, each slave contains the dedicated SS pin. If the master will communicate with particular slave. Multiple slaves can share the MOSI, MISO and SCLK but it must be having a separated SS.

SCLK – Serial Clock, this clock signal is used by the master and the slave devices for the coordinating the data transfer.

Key Features

Synchronous communication

Master slave Architecture

Full Duplex

Four wire configurations

Clock polarity and Clock phase

Multiple slaves

How it works

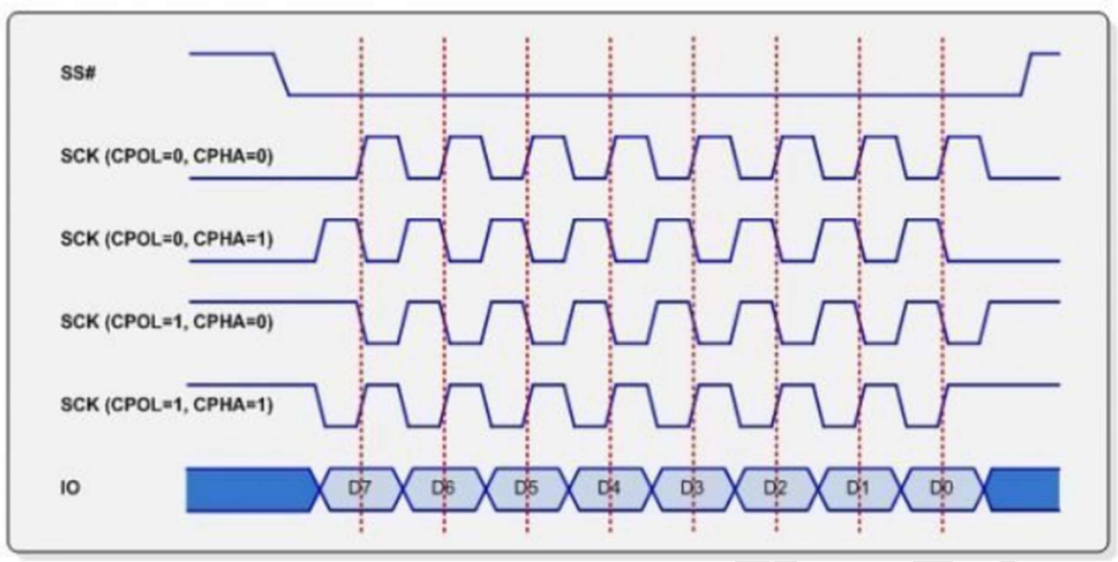
The SPI communication always initiated by master since the master configure and generates the clock. The data is transmitted master and the slave synchronized with the clock. The master sends the data bit by bit, in serial through the MOSI. The data is sent from the master is MSB first. The data is also sent from the slave to master in this case LSB first.

Clock Polarity (CPOL) and Clock Phase (CPHA)

These are used define the relation between the data signals and the clock signals. The data signals are MOSI and MISO. The SLCK is clock signal. There are for 4 available methods for the CPOL and CPHA as follows.

SPI Modes with CPOL and CPHA

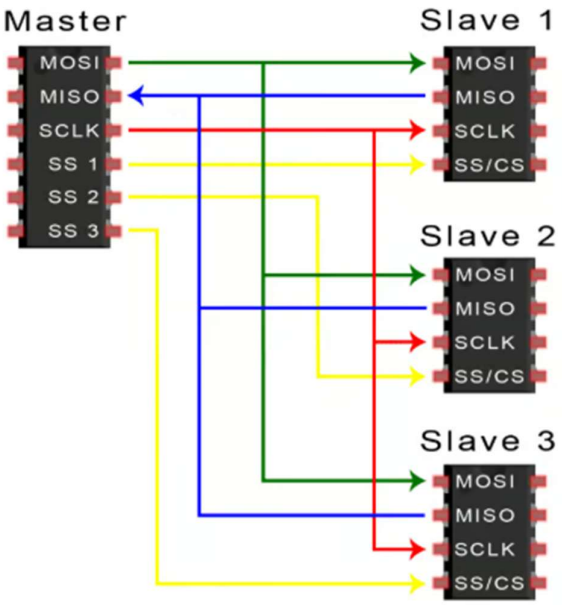
SPI MODE	CPOL	CPHA	Clock Polarity in idle state	Clock Phase used to sample and shift data
0	0	0	Logic Low	Data sampled on rising edge and shifted out on the falling edge
1	0	1	Logic Low	Data sampled on falling edge and shifted out on the rising edge
2	1	0	Logic High	Data sampled on falling edge and shifted out on the rising edge
3	1	1	Logic High	Data sampled on rising edge and shifted out on the falling edge



Multi-Sub node Configuration

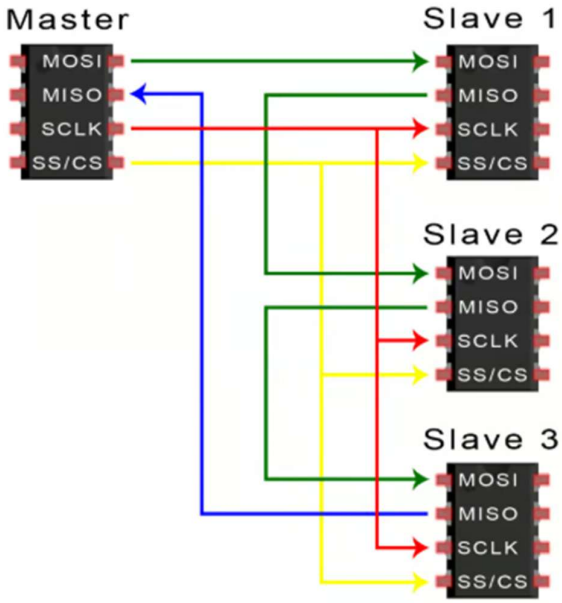
Regular SPI Mode:

If a master has multiple slaves with using multiple slaves select pin from the microcontroller



If an only 1 pin available for the slave select then the devices are connected in the daisy chain matter.

Daisy-Chain Method:



Advantage

Higher data transfer

Full duplex

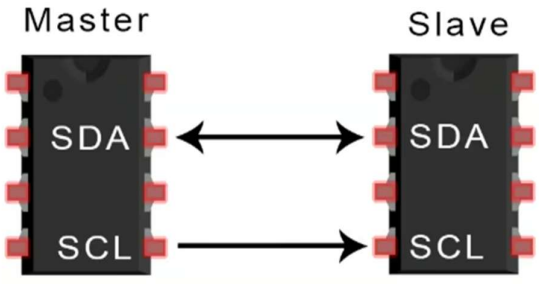
Disadvantage

Used 4 wire for communication

No acknowledgement for successful receive

3. I2C – Inter Integrated Circuit

It is 2 wire serial communication protocol. It is combination of the SPI and UART. Because it can communicate with multiple slaves with 2 wires. It is used for the short-range distance communication. It is developed by the Philips. It uses the master slave architecture where as master device micro-controller communicate between peripherals (EEPROM, DAC, ADC etc). The connection diagram as shown below. The speed of the I2C is 100 kbps standard mode to 3.4 mbps high speed mode.



Pin details:

SDA: Serial Data

SCL: Serial Clock

Key Features:

Two wire communication

Synchronous communication

Half duplex

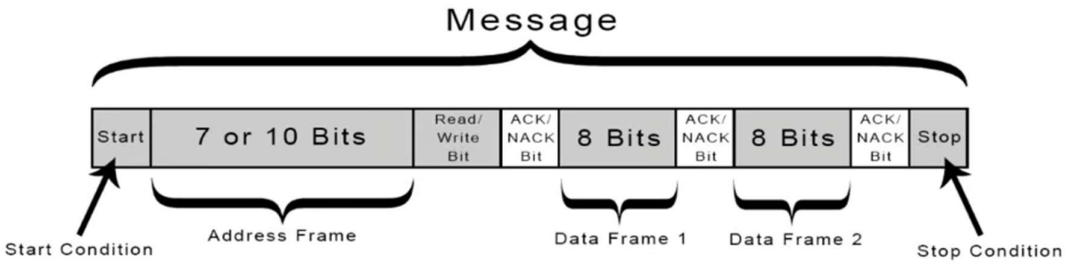
Multi master/Multi slave

Addressing

I2C Works

The communication is happened with use address of the slave boards. The message contains start bit, address bit, read/write bit, data bit, ack bit and stop bit.

Data Bits



Start bit

The SDA line is held high voltage level switches to low voltage level before SCLK line switches from High to Low.

Address bit

A 7-to-10-bit unique address for each slave that identifies the slave when the master wants to communicate with the slave board. Each slave board compare the address sent from the master to its own address. If it matches it sends back low voltage acknowledge bit back to the master. If the address doesn't match the slave doesn't change and SDA line remains high. Max 127 number of slave boards can connect the to master board.

Read/Write bit

A single bit decides the master is sending the data to slave or receiving data from the slave. The address frame includes a single bit at the end that informs the slave whether the master wants to right the data or read the data. If master wants to send the data it will low the voltage level. If master wants to read data from slave the bit is held high voltage level.

Ack/Nack Bit

Each frame in the message is followed by the acknowledge / no-acknowledged bit. if address and data send successfully acknowledge bit is set and send it to the master board.

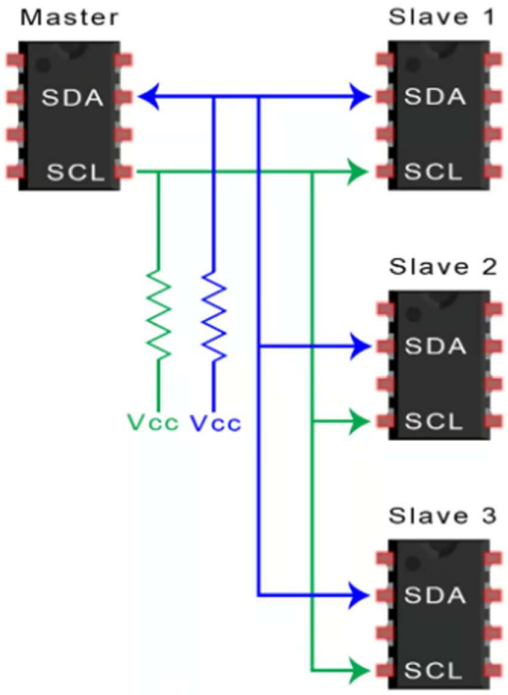
Data Bit

After master detects acknowledge bit from the slave, the master board is ready send the first Data frame. The data frame is always 8 bit long, and the MSB bit always send first. Each data frame immediately followed by the ACK/NACK bit to verify the data is successfully received or not. After all the data bit sent, the master can send the stop condition for the slave board.

Stop Bit

The voltage is made to low to high to stop the communication.

Multiple Slaves



Pull Up resister selection

Speed Mode	Max Rise Time	Typical R (3.3V–5V)	Notes
Standard (100 kHz)	1000 ns	4.7kΩ – 10kΩ	Default for most
Fast (400 kHz)	300 ns	2.2kΩ – 4.7kΩ	Short lines
Fast+ (1 MHz)	120 ns	1kΩ – 2.2kΩ	Short, low C

Serial Protocols

CLOCK GENERATION

The SCLK is always generated by the I2C master. The SCLK line is dedicated to carrying the clock signal providing a synchronization point of all the devices on the I2C bus.

BUS ARBITRATION

One of the key features of the I2C is Arbitration, which allows multiple devices to communicate on the same bus. In I2C protocol arbitration is required to resolve the conflict of the two-device attempt to transmit the data at the same time. The arbitration mechanism ensures that only one device has a control the bus at a time and the data is transmitted without any errors.

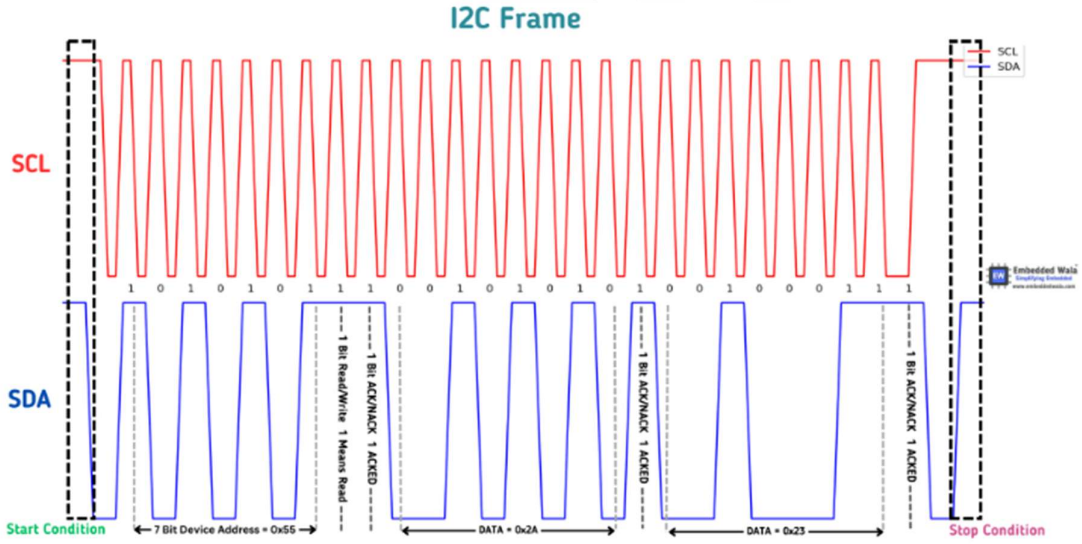
The arbitration process in the I2C protocol is wired-AND logic system. In this system if the two devices try to communicate at a same time. During this arbitration process both the masters will persist the lines until one of them successfully pulls down first.

Ex: Master '0' – **0x2A** – 0x0010 1010

Master '1' – **0x2F** – 0x0010 1111

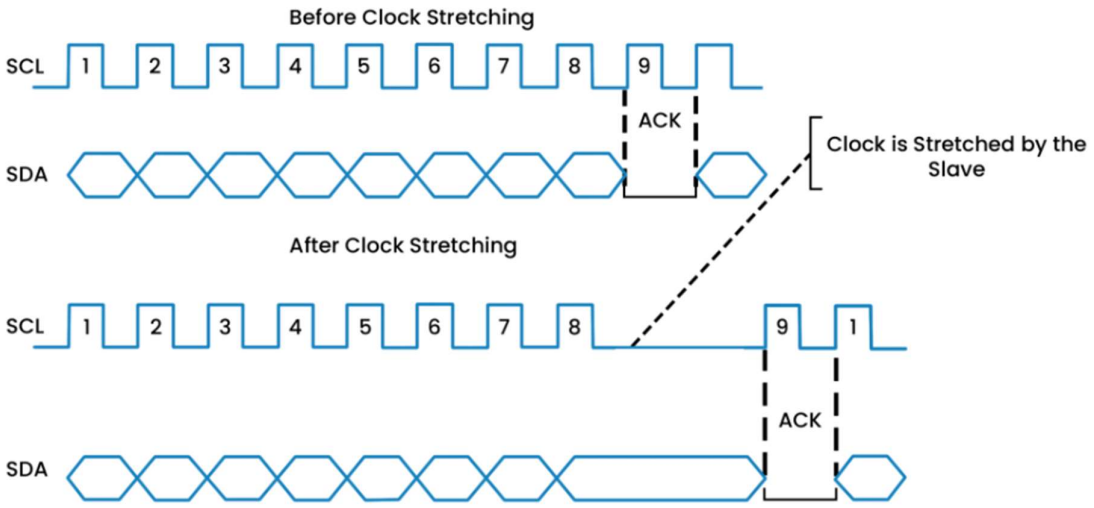
From above example the master '0' win the arbitration and sends the data first. In next cycle the second data will get transmit.

I2C FRAME



CLOCK STRETCHING

I2C devices can slow down communication by stretching SCLK. An I2C slave device can use clock stretching to push the master device to wait.



Advantage

Only two wire communication.

Supports multi masters multi slaves.

ACK/NACK gives the confirmation for the transmission of the data.

Widely used Protocol.

Disadvantage

Speed is slower.

The data is just 8 bits.

4. CAN – Control Area Network

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