Homework 2

This homework is due on Friday, February 4, 2022 at 11:59PM. Self-grades and HW Resubmissions are due the following Friday, February 11, 2022 at 11:59PM.

1. **Reading Lecture Notes**

   Staying up to date with lectures is an important part of the learning process in this course. Here are links to the notes that you need to read for this week: Note 2 and Note 3.

   (a) **How do we deal with piecewise constant inputs as introduced in the notes?**

   (b) **What conclusions do we get after approximating any function $u(t)$ as being piecewise constant over fixed interval widths Δ?**

2. Uniqueness Counterexample

This problem explores an example of a differential equation that does not have a unique solution. The purpose is to show that uniqueness cannot always be assumed.

Along the way, this problem will also show you a heuristic way to guess the solutions to differential equations that is often called "separation-of-variables." The advantage of the separation-of-variables technique is that it can often be helpful in systematically coming up with guesses for nonlinear differential equations. However, as with any technique for guessing, it is not a proof and the guess definitely needs to be checked and uniqueness verified before proceeding.

The idea of separation-of-variables is to pretend that $\frac{d}{dt}x(t) = \frac{dx}{dt}$ is a ratio of quantities rather than what it is — a shorthand for taking the derivative of the function $x(\cdot)$ with respect to its single argument, and then writing the result in terms of the free variable "t" for that argument. This little bit of make-believe (sometimes called "an abuse of notation") allows one the freedom to do calculations.

To demonstrate, let's do this for a case where we know the correct solution: $\frac{d}{dt}x(t) = \lambda x(t)$. This is how a separation-of-variables approach would try to get a guess:

$$\frac{d}{dt}x(t) = \lambda x(t) \tag{1}$$

$$\frac{dx}{dt} = \lambda x \tag{2}$$

$$\frac{dx}{x} = \lambda \, dt \qquad \text{separating variables to sides} \tag{3}$$

$$\int \frac{dx}{x} = \int \lambda \, dt \qquad \text{integrating both sides} \tag{4}$$

$$\ln(x) + C_1 = \lambda t + C_2 \tag{5}$$

$$x(t) = Ke^{\lambda t} \qquad \text{exponentiating both sides and folding constants} \tag{6}$$

With the above guess obtained, $x(t) = Ke^{\lambda t}$ can be plugged in and seen to solve the original differential equation. Then of course, a uniqueness proof is required, but you did that in the previous homework.

To see why this technique can cause trouble, we will consider the following nonlinear differential equation involving a third root[1].

$$\frac{d}{dt}x(t) = \alpha x^{\frac{1}{3}} \tag{7}$$

with the initial condition

$$x(0) = 0. \tag{8}$$

Let's apply separation-of-variables and see what happens:

$$\frac{d}{dt}x(t) = \alpha x^{\frac{1}{3}} \tag{9}$$

$$\frac{dx}{dt} = \alpha x^{\frac{1}{3}} \tag{10}$$

$$x^{-\frac{1}{3}} \, dx = \alpha \, dt \tag{11}$$

$$\int x^{-\frac{1}{3}} \, dx = \int \alpha \, dt \tag{12}$$

$$\frac{3}{2}x^{\frac{2}{3}} + C_1 = \alpha t + C_2 \tag{13}$$

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[1]This type of differential equation can arise from a physical setting of a inverted pyramidal container that had $x(t)$ liters of water in it, where the rate of water being poured in is proportional to the height of the water $x^{\frac{1}{3}}$. This fractional power arises since volume is a cubic quantity while the water is being poured in at a rate governed by a one-dimensional quantity of length. Similar equations can arise in microfluidic dynamics.

$$x = \left(\frac{2}{3}\alpha t + C_3\right)^{\frac{3}{2}} \tag{14}$$

(a) Given our separation-of-variables based calculation, let us guess a solution of the form

$$x(t) = \left(\frac{2}{3}\alpha t + c\right)^{\frac{3}{2}} \tag{15}$$

Show that this is a solution to the differential equation (7)**, and find the c that satisfies the initial condition.** (*HINT: You'll need to use the power rule and chain rule.*)

(b) Let us guess a second solution:
$$x(t) = 0 \tag{16}$$

Show that this new guess also satisfies (7)**, and the initial condition ($x(0) = 0$).** [2]

(c) A known (not by you yet, but by the mathematical community) sufficient condition for the uniqueness of solutions to differential equations of the form $\frac{d}{dt}x(t) = f(x(t))$ is that the function $f(x)$ be continuously differentiable (i.e. $\frac{d}{dx}f(x)$ is a continuous function of x) with a bounded derivative $\frac{d}{dx}f(x)$ at the initial condition $x(0)$ and everywhere that the solution $x(t)$ purports to go. (You will understand the importance of this condition and where it comes from better when we are in Module 2 of 16B. We are not going to prove it.)

Does this differential equation problem satisfy this condition that would let us trust guessing and checking?

(d) The separation-of-variables technique may involve steps that may not agree with the initial condition. **Explain why** (11) **might be a bit problematic.** (*HINT: When is it not permissible to divide both sides of an equation by the same thing?*)

(e) **Write an example of a differential equation that satisfies this uniqueness condition, and explain why.**

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[2]Indeed, any solution of the form

$$x(t) = \begin{cases} 0, & \text{if } t < t_0 \\ \left(\frac{2}{3}\alpha\left(t - t_0\right)\right)^{\frac{3}{2}}, & \text{if } t \geq t_0 \end{cases} \tag{17}$$

also satisfies (7) and the initial condition $x(0) = 0$, for any $t_0 > 0$, which concludes that (7) has infinitely many solutions. We leave the verification of this solution for those who are interested.

3. IC Power Supply

Digital integrated circuits (ICs) often have very non-uniform current requirements which can cause voltage noise on the supply lines. If one IC is adding a lot of noise to the supply line, it can affect the performance of other ICs that use the same power supply, which can hinder performance of the entire device. For this reason, it is important to take measures to mitigate, or "smooth out", the power supply noise that each IC creates. A common way of doing this is to add a "supply capacitor" between each IC and the power supply. (If you look at a circuit board, and the supply capacitor is the small capacitor next to each IC.)

Here's a simple model for a power supply and digital circuit:
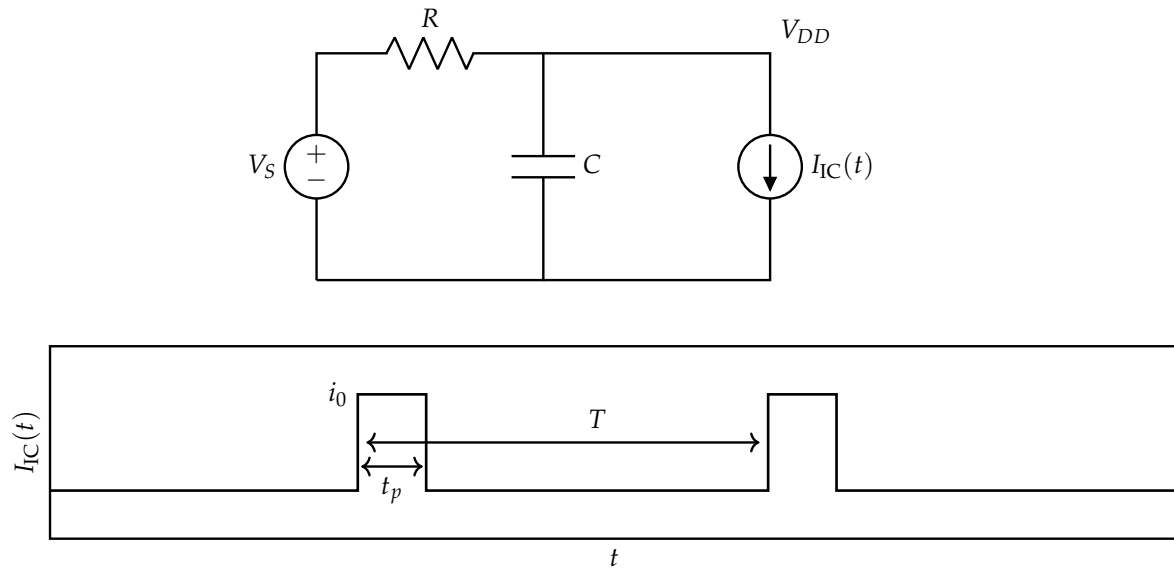
The current source is modeling the "spiky," non-uniform nature of digital circuit current consumption. 'The resistor represents the sum of the source resistance of the supply and any wiring resistance between the supply and the load.

The capacitor is added to minimize the noise on V_{DD}. Assume that $V_S = 3\,\text{V}$, $R = 1\,\Omega$, $i_0 = 1\,\text{A}$, $T = 11\,\text{ns}$, and $t_p = 1\,\text{ns}$.

(a) **Sketch the voltage V_{DD} vs. time for two T periods assuming that $C = 0$.**

(b) **Give expressions for and sketch the voltage V_{DD} vs. time for two T periods for each of three different capacitor values for C: $1\,\text{pF}$, $1\,\text{nF}$, $1\,\mu\text{F}$. ($1\,\text{pF} = 1 \times 10^{-12}\,\text{F}$, $1\,\text{nF} = 1 \times 10^{-9}\,\text{F}$, $1\,\mu\text{F} = 1 \times 10^{-6}\,\text{F}$).** For this part, to find the initial condition for V_{DD}, feel free to assume that for a very long time, $I_{IC} = 0$.

(c) Launch the attached Jupyter notebook to interact with a simulated version of this IC power supply. Try to simulate the scenarios outlined in the previous parts. For one of these scenarios, keep the RC time constant fixed, but vary the relative value of R vs. C (e.g. compare $R = 1, C = $ 2e-9 to the case where $R = 2, C = $ 1e-9). **Is it better to have a lower R or lower C value for a fixed RC time constant when attempting to minimize supply noise? Give an intuitive explanation for why this might be the case.**

Be sure to play with the y limits on the graph as well as how long the simulation runs to best understand what is going on here.

4. Simple Scalar Differential Equations Driven by an Input

In this question, we will show the existence and uniqueness of solutions to differential equations with inputs. In particular, we consider the scalar differential equation

$$\frac{\mathrm{d}}{\mathrm{d}t}x(t) = \lambda x(t) + bu(t) \tag{18}$$

$$x(0) = x_0 \tag{19}$$

where $u \colon \mathbb{R} \to \mathbb{R}$ is a known function of time. Feel free to assume u is "nice" in the sense that it is integrable, continuous, and differentiable with bounded derivative – basically, let u be nice enough that all the usual calculus theorems work.

(a) We will first demonstrate the existence of a solution to eqs. (18) and (19).

Define $x_d \colon \mathbb{R} \to \mathbb{R}$ by

$$x_d(t) := e^{\lambda t}x_0 + \int_0^t e^{\lambda(t-\tau)}bu(\tau)\,\mathrm{d}\tau. \tag{20}$$

Show that x_d satisfies eqs. (18) and (19).

(*HINT: When showing that x_d satisfies eq. (18), use the product rule, and use the fundamental theorem of calculus to take the derivative of the integral.*)

(b) Now, we will show that x_d is the unique solution to eqs. (18) and (19).

Suppose that $y \colon \mathbb{R} \to \mathbb{R}$ also satisfies eqs. (18) and (19). **Show that $y(t) = x_d(t)$ for all t.**

(*HINT: This time, show that $z(t) := y(t) - x_d(t) = 0$ for all t. Do this by showing that $z(0) = 0$ and $\frac{\mathrm{d}}{\mathrm{d}t}z(t) = \lambda z(t)$, then use the uniqueness theorem for homogeneous first-order linear differential equations from the last homework. Note that the specific form of $x_d(t)$ in eq. (20) is irrelevant for the solution and should not be used.*)

(c) In this part, we will calculate some values of x_d for common values of u.

   i. If $u(t) := u$ is a constant function, **what is $x_d(t)$?**

   ii. If $u(t) := e^{\alpha t}$ for some real number $\alpha \neq \lambda$, **what is $x_d(t)$?**

   iii. If $u(t) := e^{\lambda t}$, **what is $x_d(t)$?**

NOTE: Assume for simplicity that $\lambda \neq 0$.

5. Op-Amp Stability

In this question we will revisit the basic op-amp model that was introduced in EECS 16A and we will add a capacitance C_{out} to make the model more realistic (refer to figure 1). Now that we have the tools to do so, we will study the behavior of the op-amp in positive and negative feedback (refer to figure 2). Furthermore, we will begin looking at the integrator circuit (refer to figure 3) to see how a capacitor in the negative feedback can behave. In the next homework, you will see why it ends up being close to an integrator.
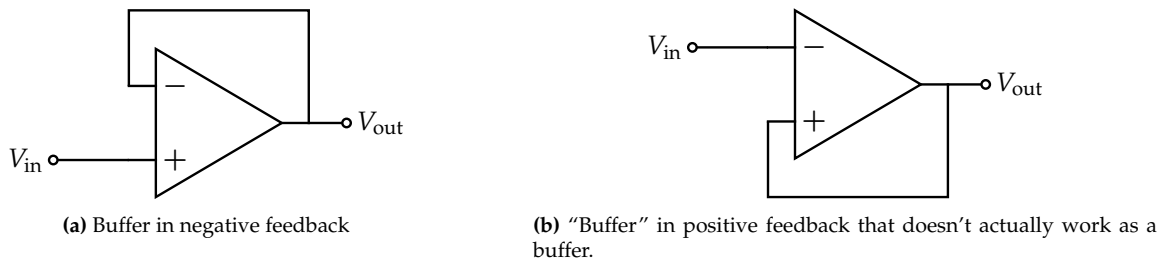

Figure 1: Op-amp model: $\Delta V = V_+ - V_-$

(a) Buffer in negative feedback

(b) "Buffer" in positive feedback that doesn't actually work as a buffer.
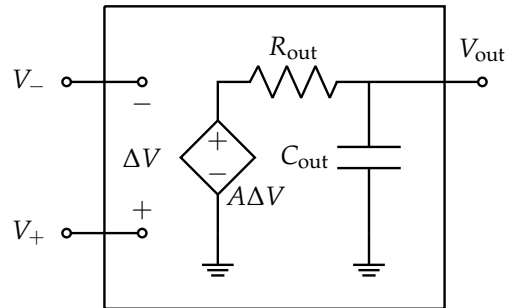
Figure 2: Op-amp in buffer configuration

(a) Using the op-amp model in figure 1 and the buffer in negative-feedback configuration in figure 2a, **draw a combined circuit**. Remember that $\Delta V = V_+ - V_-$, the voltage difference between the positive and negative labeled input terminals of the op-amp. (*HINT: Look at figure 4 to see how this was done for the integrator. That might help.*) *NOTE*: Note: here, we have used the equivalent model for the op-amp gain. In more advanced analog circuits courses, it is traditional to use a controlled current source with a resistor in parallel instead.

(b) Let's look at the op-amp in negative feedback. From our discussions in EECS 16A, we know that the buffer in figure 2a should work with $V_{out} \approx V_{in}$ by the golden rules. **Write a differential-equation for V_{out} by replacing the op-amp with the given model and show what the solution will be as a function of time for a static V_{in}. What does it converge to as $t \to \infty$?** Note: We assume the gain $A > 1$ for all parts of the question. For this part, you can assume the initial condition $V_{out}(0) = 0$.

(c) Next, let's look at the op-amp in positive feedback. We know that the configuration given in figure 2b is unstable and V_{out} will just rail. **Again, using the op-amp model in figure 1, show that V_{out} does not converge and hence the output will rail. For positive DC input $V_{in} > 0$, will V_{out} rail to the positive or negative side? Explain.** For this part, you can assume the initial condition $V_{out}(0) = 0$.

(d) For an ideal op-amp, we can assume that it has an infinite gain, i.e., $A \to \infty$. **Under these assumptions, show that the op-amp in negative feedback behaves as an ideal buffer, i.e., $V_{out} = V_{in}$.**

(e) Let's extend our analysis to the integrator circuit shown below (figure 3). Simplifying all the equations, we get a system of differential equations in two variables V_C and V_{out}, where V_C and V_{out} are the voltage drops across the capacitors C and C_{out}. **Fill in the missing term in the following matrix differential equation.**

$$\frac{d}{dt}\begin{bmatrix} V_{out}(t) \\ V_C(t) \end{bmatrix} = \begin{bmatrix} -\left(\frac{A+1}{R_{out}C_{out}} + \frac{1}{RC_{out}}\right) & -\left(\frac{1}{RC_{out}} + \frac{A}{R_{out}C_{out}}\right) \\ -\frac{1}{RC} & ? \end{bmatrix}\begin{bmatrix} V_{out}(t) \\ V_C(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{RC_{out}} \\ \frac{1}{RC} \end{bmatrix} V_{in}(t) \quad (21)$$

(*HINT: We picked an easier term to hide. You don't have to write out all the equations and do a lot of algebra to figure out what the missing term is.*)
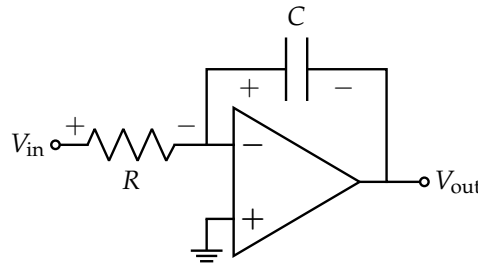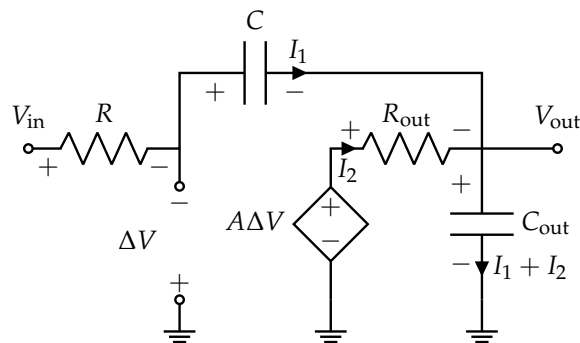

Figure 3: Integrator circuit

Figure 4: Integrator circuit with op-amp model.

6. **Successive Approximation Register Analog-to-Digital Converter (SAR ADC)**

An analog-to-digital converter (ADC) is a circuit for converting an analog voltage into an approximate digital representation of that voltage. One commonly used circuit architecture for analog-to-digital converters is the Successive Approximation Register ADC (SAR ADC), which you will see in Lab 3. An N-bit SAR ADC converts an input analog voltage to an N-bit binary string between 0 and $2^N - 1$. This binary string represents an integer, which in term approximates the value of our analog input voltage.

The SAR ADC does this by following one of the key themes in 16B: reducing a problem into subproblems that we already know how to solve. In this case, the two ingredients are the DAC (digital to analog converter) that we saw in HW 1, and a binary search tree that you saw in 61A. As you remember from 61A, the key operation required for a binary search is dividing a group into two halves, solving the problem at the current step with a less-than/greater-than comparison, and descending into one of the halves. We continue this until we can no longer subdivide the problem. The comparison operation is therefore key to a binary search tree. Fortunately, we have a circuit element from 16A that lets us do that: a comparator.

Explicitly, the SAR ADC implements the binary search algorithm by feeding trial digital codes into a **DAC**, like the one we analyzed in Homework 1. The circuit then takes the resuling analog voltage from the DAC and compares it with the analog input voltage using a **comparator**. It then uses feedback (**SAR logic**) to adjust the DAC output voltage to get as close as possible to the input analog voltage, step by step. The algorithm starts by determining the most significant bit (MSB), which is the bit with the largest binary weight (i.e. furthest to the left in a traditional binary number), and then moving on to determine the next bit.

If this is not clear to you, think about how you would play 20 questions to guess an integer between 0 and $2^{20} - 1$, which is approximately 1 million. This is a game where you have to guess what number your friend is thinking of, and they can only tell you if your guess is too high or too low. You have 20 guesses to get your number as close as possible to your friend's. Would you start by guessing 0, then 1, then 2, etc.? Or would you start in the middle, let's say 500,000, see if you're too high or low, then move into the next half, e.g. 250,000 or 750,000 depending on your result? The latter approach of divide-and-conquer is a faster way of solving the problem! The SAR ADC is basically a circuit implementation of this game. The input voltage is the "number" your friend has in mind, the DAC code is your guess, the comparator is your friend's response (too high vs. too low), and the SAR logic used to adjust the next code is you deciding what to guess next. For a 20-bit SAR DAC, you have 20 guesses; for an N-bit SAR DAC, you have N guesses.

Figure 5 illustrates a high-level circuit diagram of a SAR ADC. The analog input voltage is one of the inputs to the comparator. The other comparator input, V_{DAC}, is the DAC voltage output, i.e. the analog representation of your code/guess. The comparator compares these two values and outputs a logical high (1) if $V_{IN} \geq V_{DAC}$ or a logical low (0) if $V_{IN} < V_{DAC}$. This comparator decision then feeds into the SAR logic, implemented in a microcontroller in this case. This logic is basically the brain that implements the binary search pattern, deciding which bits in the code need to be changed. The updated code then propagates back to the DAC, which updates V_{DAC}, and the cycle continues N times. Once this is done, the final N-bit output code comes out of the register storage units for use by other circuits. If you're wondering what V_{REF} does for the DAC, recall from Homework 1 that it tells the DAC what the maximum possible input voltage is.
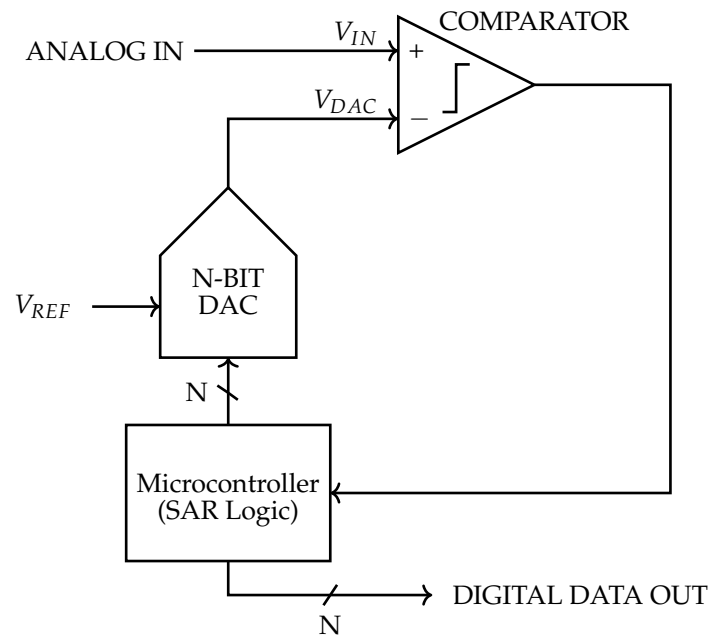
Figure 5: SAR ADC circuit diagram

Here is an illustration of the algorithm, which the SAR logic takes care of.
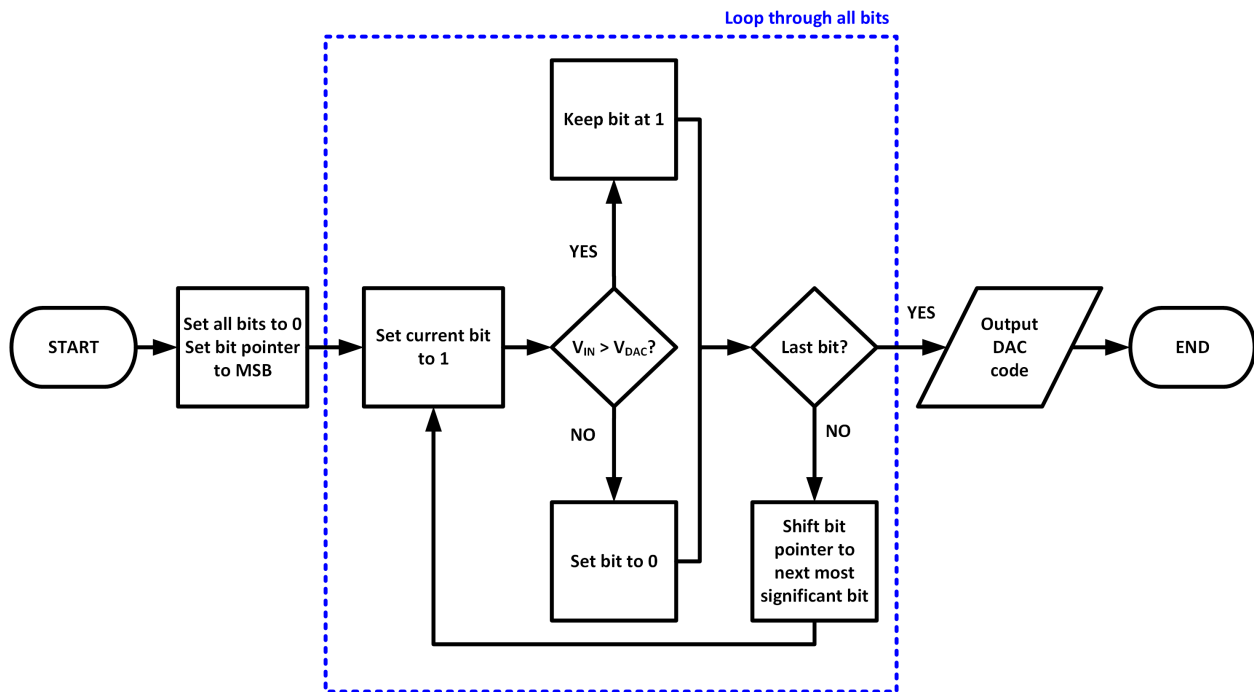

Figure 6: Flow chart of SAR ADC algorithm.

Let's look at a 3-bit SAR ADC as an example. The voltage transfer curve of the 3-bit SAR ADC is shown in Figure 7. For $V_{\text{IN}} = 0.3V_{\text{REF}}$, the operation of SAR ADC is shown in Figure 8.
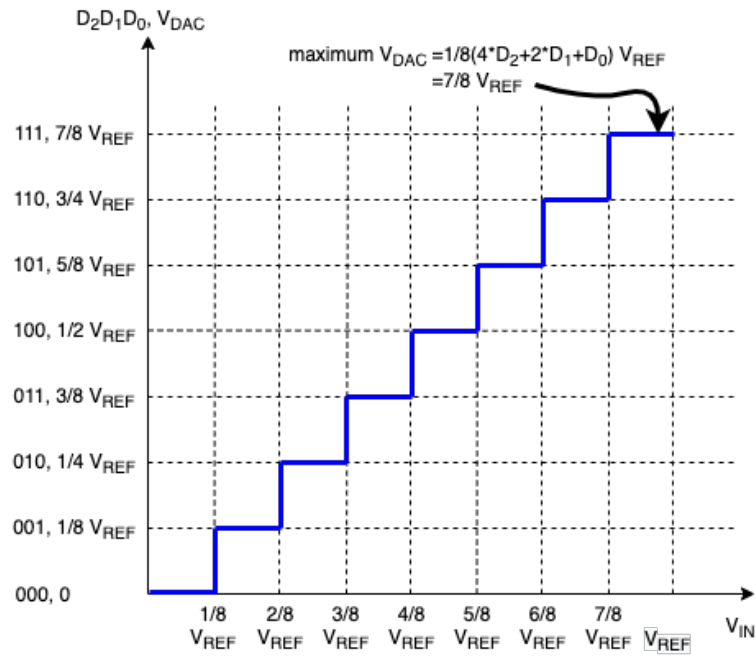
Figure 7: Voltage transfer curve of 3-bit SAR ADC: $D_2D_1D_0$ is the output digital code of the ADC. Notice that the maximum voltage of the V_{DAC} is $\frac{2^N-1}{2^N} V_{REF}$ where N is the number of bits ($N = 3$ in this case)
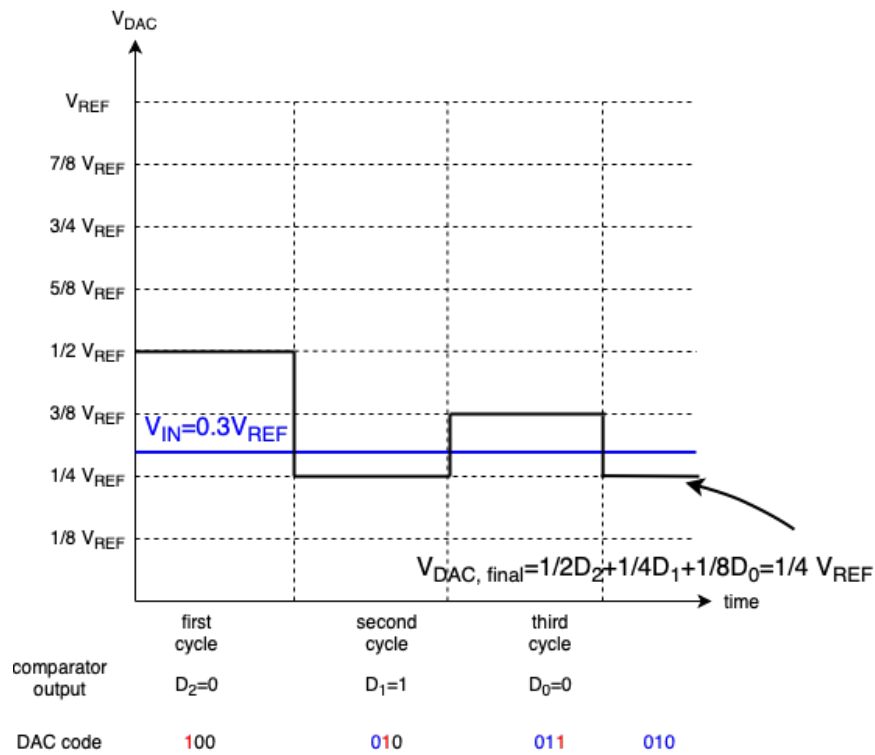

Figure 8: Timing diagram of SAR output code. Red digit in DAC code is the bit being decided in the cycle; blue digits are the bits determined by the previous conversion cycles.

From the timing diagram in Figure 8, it can be seen that the final digital output code is 010 which

represents the closest DAC output voltage $\left(\frac{1}{4}V_{\text{REF}}\right)$ to the input analog voltage $V_{\text{IN}} = 0.3V_{\text{REF}}$ with a 3 bit binary representation.

We will now analyze the operation of a 4-bit SAR ADC with the input voltage range between $0\,\text{V}$ and $5\,\text{V}$ and output code range between 0000 (0) and 1111 (15). In other words, V_{REF} is $5\,\text{V}$ and $0\,\text{V} < V_{\text{in}} < 5\,\text{V}$ in Figure 5.

(a) **If the ADC output code is 0000, what is the corresponding DAC voltage? What about code 1111? Code 1001?** (*HINT: Try to draw the transfer curve for 4-bit SAR ADC, similar to that for the 3-bit SAR ADC in Figure 7.*)

(b) **If the input analog voltage is $V_{\text{IN}} = 3\,\text{V}$, what is the ratio between the input voltage V_{IN} and the maximum input voltage $V_{\text{REF}} = 5\,\text{V}$? What should be the output code of the SAR ADC?**

(c) Again, if the input analog voltage is $V_{\text{IN}} = 3\,\text{V}$, draw the operation of a 4-bit SAR ADC resolving its output code (see Figure 8 as reference). Specifically:

    i. **Plot the output voltage of the DAC in the timing diagram in Figure 9.**

    ii. **Fill out the output of the comparator in each conversion cycle.**

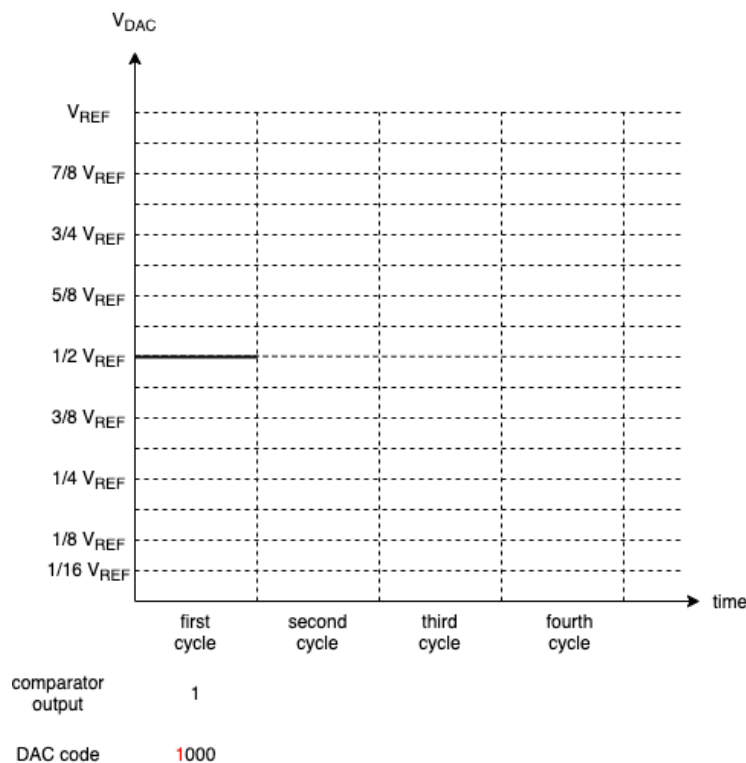   iii. **Fill out the ADC output code ($D_3 D_2 D_1 D_0$) in each conversion cycle.**

Figure 9: SAR ADC V_{DAC} timing diagram

7. **(OPTIONAL) Make Your Own Problem.**

   Write your own problem about content covered in the course thus far, and provide a thorough solution to it.

   NOTE: This can be a totally new problem, a modification on an existing problem, or a Jupyter part for a problem that previously didn't have one. Please cite all sources for anything (including course material) that you used as inspiration.

   NOTE: High-quality problems may be used as inspiration for the problems we choose to put on future homeworks or exams.

8. **Homework Process and Study Group**

   Citing sources and collaborators are an important part of life, including being a student!

   We also want to understand what resources you find helpful and how much time homework is taking, so we can change things in the future if possible.

   (a) **What sources (if any) did you use as you worked through the homework?**

   (b) **If you worked with someone on this homework, who did you work with?**
   List names and student ID's. (In case of homework party, you can also just describe the group.)

   (c) **Roughly how many total hours did you work on this homework? Write it down here where you'll need to remember it for the self-grade form.**

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