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**RIP-Felix**
Senior Member

Power Control Topology - Part 3

(SYSCON Switches and Power On Sequencing)

Introduction:

You may have heard of the term booting a computer. But what actually is taking place is more complex than you may realize. The term "BOOT" actually refers to a "bootloader" program that loads the operating system (OS). But before the Bootloader can start, the console must first be able to enter standby. Then it needs to clear Power On Sequence Testing (POST).

When you plug in your PS3, or flip power rocker at the back, the Power Supply Unit delivers power to System Control (SYSCON) and a crystal for its clock. There are also some thermal monitors and analog voltage regulators needed for the most basic standby functions. What's happening is the SYSCON is powered and waiting. The LED goes solid red. The Bluetooth subsystem is powered so that you can start the console with your controller. The PS3 is just waiting for you to press the power button. If your PSU is dead or the fuses to those Analog Voltage regulators are blown, then you won't even get into Standby!

When you turn the console on it goes through a process called Power On Sequence Testing (POST), which includes 2 processes.

- 1. Power On Sequencing (POS):** The SYSCON "switches" on voltages to the console subsystems one at a time. They need to be powered on in a certain



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synchronize the chipset. For example, the CPU/GPU/SB are held in reset until the clocks and power supplies have been "switched" on (enabled) by SYSCON and their output has stabilized (Power Good). Then reset is released and the chipset will startup synchronized. Then they will be ready for initialization and configuring.

Once the console has cleared POST the bootloader can begin loading the operating system.

Of course that's the simplified explanation! It doesn't do us much good when you are having an issue and need to track down the culprit. Thanks to the [SYSCON errorlogs](#), we now have error codes that give us information about the problem. More specifically, there is a 4-digit code that points to a particular area. We have [already discussed that in great detail](#).

I recently collated 250+ consoles worth of data and presented an analysis. What I learned is that many of the 4-digit codes overlap. They don't always tell you what you want to hear - That your NEC/TOKINs are bad, or there is specific fuse that needs replaced. Instead it narrows down the list to a number of possibilities. You still need to troubleshoot the board (continuity, resistance, ESR of electrolytic caps, voltages, etc). And you need to observe the console history. Has it been opened? What work has been done? What are past errors in the errorlog telling you? This context leads us to a better diagnosis.

What's less understood and probably more useful in the 2-digit Step Number just before the 4-digit error. For example 20 2120. All the 2120 tells us is that the error is related to the HDMI transmitter. So does that mean the HDMI chip is dead? Well, that depends on context. How does it look? Are there shorts, missing voltages, blown fuses, flux residues, what other errors are in the log? That can help rule out lots of potential issues.

Step# 20 tells us when error 2120 occurred! It tells us if the error occurred in Standby, POST, BOOT, System ON, or System Off states. It's the key to understanding the meaning of the 4-digit error code, because knowing [what the console was doing when the error occurred provides vital context](#). If that step is when the SYSCON switches on a voltage regulator, then it could be a fuse that



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/213013. At Step# 20 SYSCON switches on IC6301, which powers up DC/DC converters for the AV Backend. This I/O subsystem is known to cause 2120 errors, but the Step# tells us where to look first. Since it occurred when the SYSCON first enables those voltages, we should really suspect the fuses and voltage regulators. So focus your attention on probing that area. Sure enough, users have reported this error combination can be caused by blown F6302, short C6320, etc. That theose voltages were not present when they attempted to power the console on.

On the other hand, If the same error occurs at a different Step#, it can mean something completely different. For example, @db260179 reported a 00 2120. 2120 is the same 4-digit HDMI error, but the Step# 00 refers to standby. For context, he got the error as soon as he plugged in the console, not when turning it on. He repaired by replacing TH2501, which protects +5V_ANA voltage for the HDMI port. He noted with it blown, IC2501 regulator on pin 6 (HDMI Initialize) is not getting anything. I don't believe he ever mentioned if the replacing the fuse fixed that console or not. It's possible that a bad HDMI cable, or it got knocked, cause a short blowing that fuse. There could have been more damage. The point is, this was the same 2120 error with a completely different issue. The Step# was the only thing that might have clued us in. That is if we weren't preoccupied looking at the HDMI chip and RSX power (tokin or BGA). We were too focused on guessing that we missed a simple fuse. This emphasizes the need to troubleshoot the board THOROUGHLY! Check fuses!!!

"Get on with it!"

So now we know the Step# is important, we just need to know what each Step Number means. What is the console doing?

We have been having this discussion for awhile now...

M4j0r said: ↑

I've also added the voltage descriptions here:
https://www.psdevwiki.com/ps3/index.php?title=File:RSX_SKEMA.jpg&diff=prev&oldid=62463.



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M4j0r said: ↑

@RIP-Felix

You might be interested in this: <https://pastebin.com/B62i3UsY>. I created that some time ago, it's for the Cytology platform, neither 100% correct nor complete.

You can't match all the CELL init steps to the HIG since the IBM HIG only proposes a possible implementation and Sony doesn't stick to that...

He's referring to this IBM Hardware Installation Guide for the 65nm CELL CPU. I read it pretty thoroughly and inferred the general "cytology" from their "example." It seems like it needs to follow most of that general order. It is highly technical and took several days to even begin to wrap my head around it, but very helpful to understand the Attention, Hard reset, Machine Checkstops, and Livelock signals.

While SONY may not have stuck to the HIG, there is a great deal of information in there about the required sequencing. Anyway, between the HIG and the SYSCON codes I put together the following. Like yours, it's definitely not 100% accurate or anything. Just me attempting to organize the step numbers in context of SYSCON switches and what the console is doing.

Here are just a few of the more useful excerpts:

Spoiler: General POR Phase Overview

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However, the GRID_TEST signal can be used to verify that the core PLL (clock source) is functioning correctly. This signal shows the lock status of the core PLL, and should be active (locked) by the time the HARD_RESET signal can be changed to inactive. If GRID_TEST does not become active, then verify the following conditions:

- The V_{DDA} quality (voltage level and filtering).
- The reference clock frequency (PLL_REFCLK) and signal level.
- The order in which power and the reference clock are applied.

2.3.2 POR Phase 2 Entry Check

When the HARD_RESET signal goes inactive, the Cell BE processor will begin POR phase 2. During this phase, there are two times at which intervention from the system controller is required. The first is the configuration-ring load, which should happen almost immediately after HARD_RESET is inactive. The system controller should detect that the ATTENTION signal is active almost immediately after HARD_RESET is inactive.

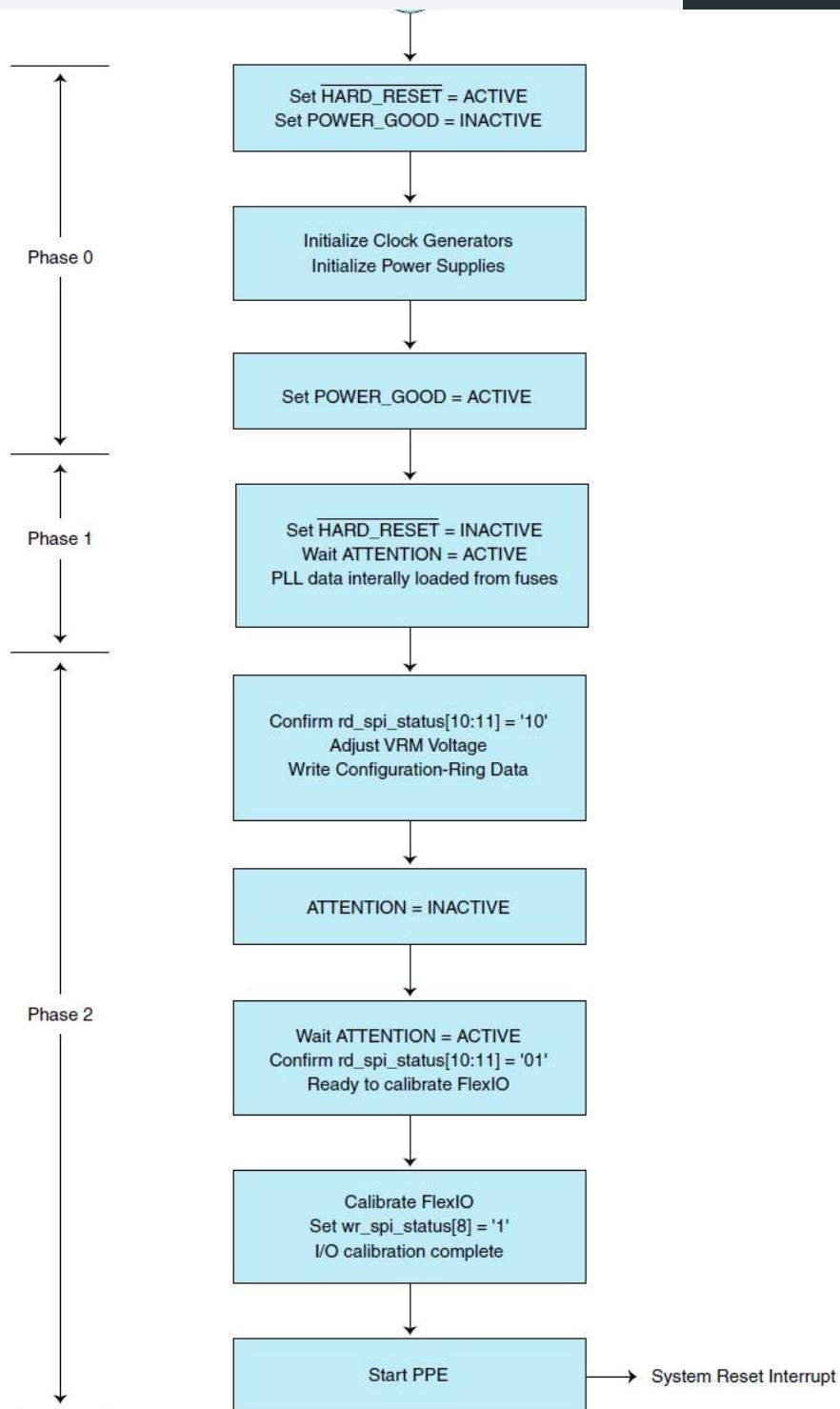
If this does not happen, verify the following conditions:

- The PLL is locked (see *POR Phase 1 Check*).
- The signal level of the HARD_RESET signal is correct according to the recommendations in the *Cell Broadband Engine Datasheet*.
- The signal level of the ATTENTION signal is correct according to the *Cell Broadband Engine Datasheet*.
- The following signal levels that might affect the POR:
 - CHECKSTOP_IN must be inactive.
 - PLL_CTL[0:1] must be tied inactive.
 - SPI_CTL[0:1] must match the system controller settings and follow the recommendations in the *Cell Broadband Engine Datasheet*.
 - SYS_CONFIG[0:3] must be tied inactive.
 - Pin AY17 must be tied to ground.
 - EXT_CLK_EN must be tied inactive.

Spoiler: POR Flow-Chart



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Spoiler: POR Sequence



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		and the HARD_RESET pin active. Apply voltage to the clock generator and activate the reference clocks.
Phase 0		Wait the minimum time (see <i>Cell Broadband Engine Datasheet</i>) after the power supply is in regulation and the reference clocks are stable. Drive the POWER_GOOD pin active.
	Detect the start of POR.	
Phase 1	Scan the initial state of the memory-mapped I/O (MMIO) and SPRs to their POR values listed in the <i>Cell Broadband Engine Registers</i> document.	
	Read the pins SYS_CONFIG[0:3] for the configuration sequence information. These pins are typically tied to '0000'. Write the nominal PLL data from the fuses into the internal PLL configuration latches. Wait for HARD_RESET to become inactive.	
		Wait the minimum time (see <i>Cell Broadband Engine Datasheet</i>) after POWER_GOOD goes active.
	Continue initialization when HARD_RESET goes inactive.	Wait for the ATTENTION signal to become active.
	Activate ATTENTION to request configuration data.	
		Read the serial peripheral interface (SPI) Status Register to determine the reason for the ATTENTION signal. rd_spi_status[10:11] should be '10'.
		Read the VID value from the SPI. Adjust the V _{DD} and V _{CS} voltages as required. Wait for the power supply to stabilize.
		Write the configuration-ring data through the wr_config_ring SPI register.
		Wait for the ATTENTION signal.
Phase 2	Continue the internal initialization, which includes initializing the FlexIO and XIO PLLs.	
	Activate ATTENTION to indicate that calibration is required.	
		Read the SPI Status Register to determine the reason for the ATTENTION signal. rd_spi_status[10:11] should be '01'.
	Participate in the FlexIO calibration.	Participate in the FlexIO calibration.
		Calibrate the FlexIO interface.

2.3.4 Configuration-Ring Load Check

When the Cell BE processor drives the ATTENTION signal active, the reason for the attention is stored in the rd_spi_status register that is accessible from the SPI interface. At this point in POR phase 2, the Cell BE processor should be requesting the configuration-ring data. Check the following conditions by reading the rd_spi_status register:

- If the rd_spi_status register reads as all zeros or all ones, then the data is not being correctly read. Confirm that the simple read sequence (*Section 3.3.2* on page 106) for reading this register matches what the Cell BE processor expects.
- rd_spi_status[0] reflects the state of the ATTENTION signal. If it does not match the ATTENTION signal, confirm that the system controller sequence matches what the Cell BE processor expects.
- rd_spi_status[1:4,7] are attention conditions caused by software. Because no software is involved at this point, these bits should all be '0'.
- rd_spi_status[6] is the thermal condition. This function is not enabled at this point in the POR sequence, so this bit should be a '0'.
- rd_spi_status[10:11] shows the attention request from the Cell BE POR state machine. This bit field should equal '10'.
- rd_spi_status[25] is the inverse of the HARD_RESET signal. This bit should always be '0' when the HARD_RESET signal is inactive.
- rd_spi_status[30:31] are constants. This bit field should equal '01'. If it is not, then verify the SPI sequence.

If the attention was caused by the request for configuration-ring data, read the VID and adjust the VRM for V_{DD} and V_{CS}. See *Section 2.1.5.1 VRM Adjustment with VID Value* on page 38.

After the VRM is adjusted and the core V_{DD} power supply has stabilized, read rd_spi_status again and confirm that bits [10:11] are still equal to '10'. The status should not have changed, because the Cell BE POR state machine should still be waiting for the configuration ring to be loaded.

To confirm that reads of SPI registers are working correctly, the rd_chip_id register can be read. The values in this register are hardwired on the Cell BE processor for each specific version of the chip.

Before the configuration-ring data is loaded, the SPI rd_partial_good register must be read, because this data is needed to load the configuration ring with the correct SPE partial good information. See *Section 3.4.7 Read Partial Good Register (rd_partial_good)* on page 122. See *Section 4.2 Bit Descriptions* on page 128 for loading the configuration ring.

To summarize, check the following conditions:

- That the rd_spi_status register matches the expected value.
- That V_{DD} and V_{CS} are adjusted to the correct voltage indicated by the VID according to the *Cell Broadband Engine Datasheet*.
- That the configuration ring is loaded with the partial good information from the rd_partial_good register.
- That the following configuration-ring information is correct:

Spoiler: FlexIO Calibration



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After the POR sequence has completed, the rd_spi_status register will be updated. Although this is performed internally by the Cell BE processor, the following operations performed by Cell BE POR state machine affect the rd_spi_status register:

- rd_spi_status[8,9,28,29] contain the POR status of the FlexIO and XIO interfaces. These bits should all be '1' at this point in the sequence. If not, check the following conditions:
 - The FlexIO and XIO interfaces run off separate PLLs from the core PLL. These PLLs are configured by the configuration ring. Confirm that the configuration-ring data for the FlexIO and XIO all match the values recommended by Rambus for the specific version of the Cell BE processor.
 - The FlexIO and XIO PLLs are correctly set up and are connected to the correct power supply voltage levels.

The Cell BE POR state machine waits for the system controller to notify the Cell BE processor that the FlexIO calibration has completed. After the calibration is completed, the system controller writes a '1' to the wr_spi_status[8] bit, and the Cell BE POR state machine finishes the POR sequence.

Spoiler: POR Completion

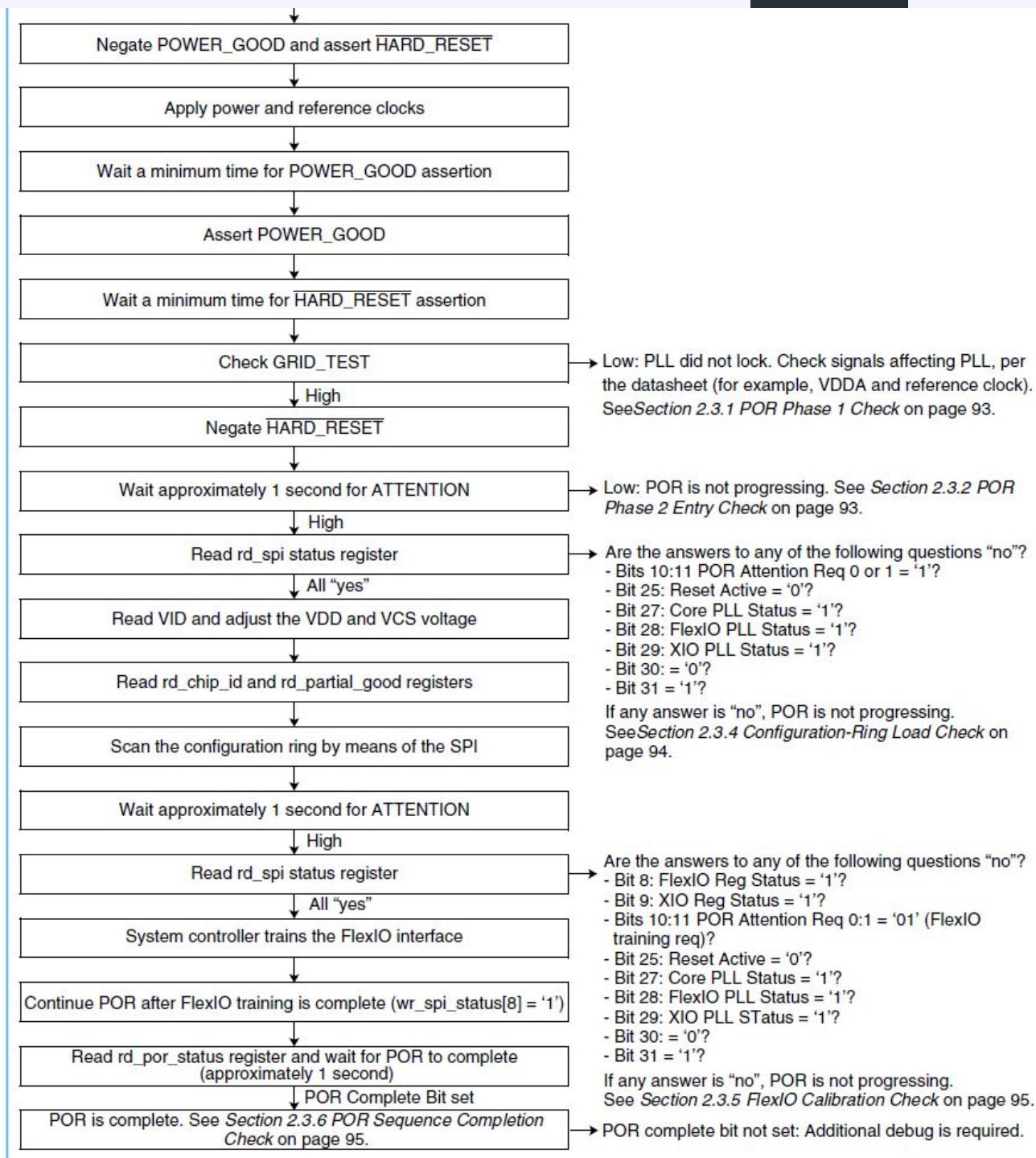
2.3.6 POR Sequence Completion Check

To determine whether the Cell BE POR state machine has correctly completed the POR sequence, read the rd_por_status register and check the following conditions:

- rd_por_status[0] indicates whether an error occurred during the POR sequence. This bit should be '0'.
- rd_por_status[1] indicates whether any of the POR instructions did not complete as expected. This only applies to Cell BE internal instructions and not to external requests, such as a configuration-ring data request or a FlexIO calibration request. These external requests do not have any time duration checking.
- rd_por_status[9] shows whether the FlexIO calibration is complete. This bit should be '1'.
- rd_por_status[11] shows whether the Cell BE POR state machine has acknowledged the configuration-ring data. If this bit is '0', the loading of the configuration ring was not successful. See *Section 2.3.4 Configuration-Ring Load Check* on page 94 for information about diagnosing the configuration ring load operation.
- rd_por_status[17] should be '1'.
- rd_por_status[20] should be '0'. If it is '1', check the SYS_CONFIG signal setting.
- rd_por_status[22] is the POR complete bit. This should be '1'.
- rd_por_status[23] should be '1'. If not, go back to *Section 2.3.2 POR Phase 2 Entry Check* on page 93.

Spoiler: POR Debug Flow-Chart





Spoiler: Firmware Sequence



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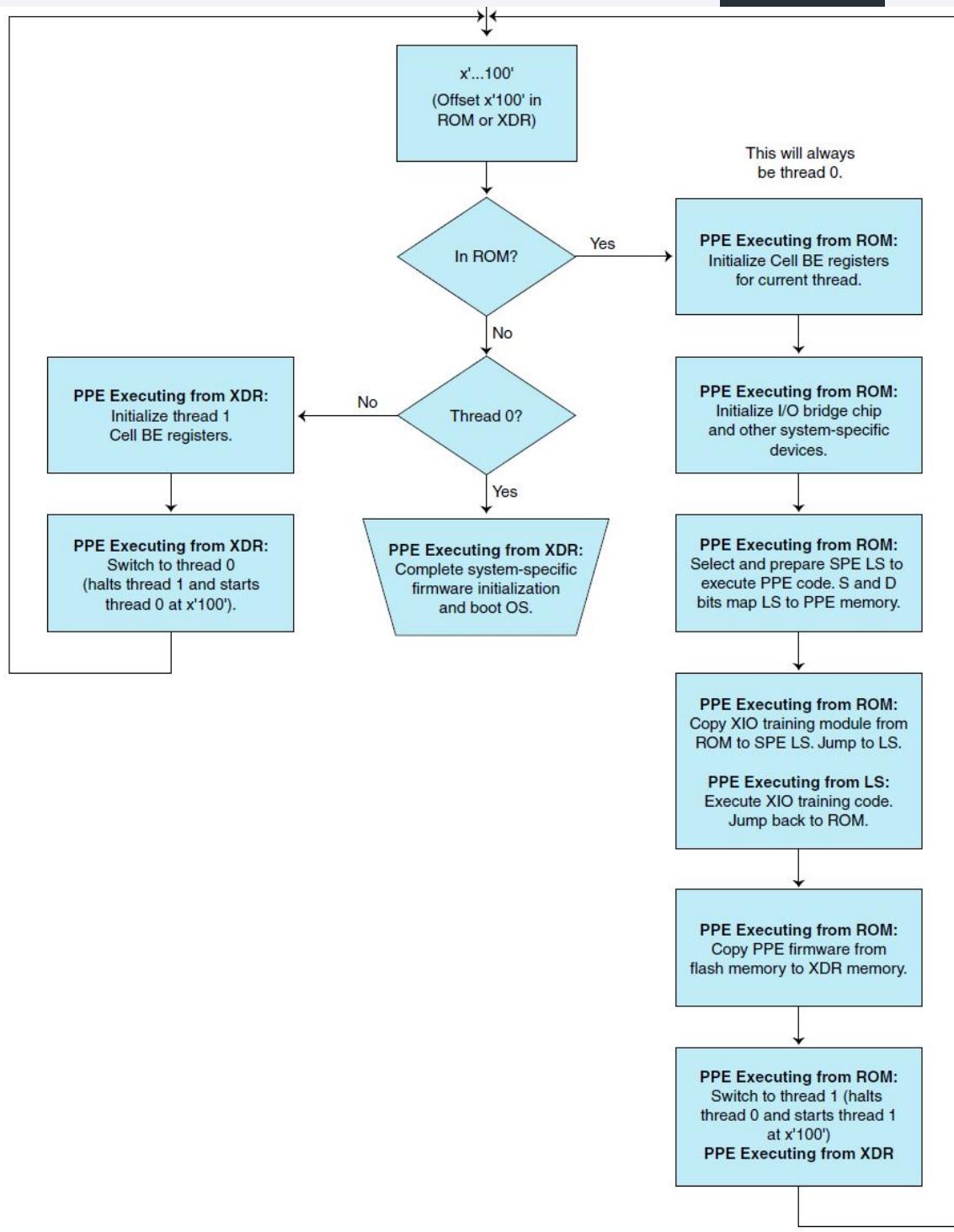
to indicate that I/O calibration has completed and is no longer active. The POR sequence is then completed, and the POR state machine instructs the PPE to begin running code. This indicates the beginning of the firmware sequence. A flowchart and pseudocode for the sequence are given in *Section 2.2.1* on page 57.

Because the HID1 SPR defaults to all zeros during POR, the PPE takes a system reset interrupt and starts thread 0 from the address specified in the *PPE SReset Vector* field of the configuration ring. As a result of the system reset interrupt, the hypervisor and 64-bit-mode bits, MSR[HV] and MSR[SF], are both set to '1', so that the PPE comes up in hypervisor mode.

From this point forward, the system controller does not participate in Cell BE initialization. If the ATTENTION signal switches to active after the POR sequence is complete, it indicates that an error condition has occurred and that the Cell BE processor needs the system controller's help. In this case, the system controller must read the rd_spi_status register to determine what caused the ATTENTION signal and take appropriate action.



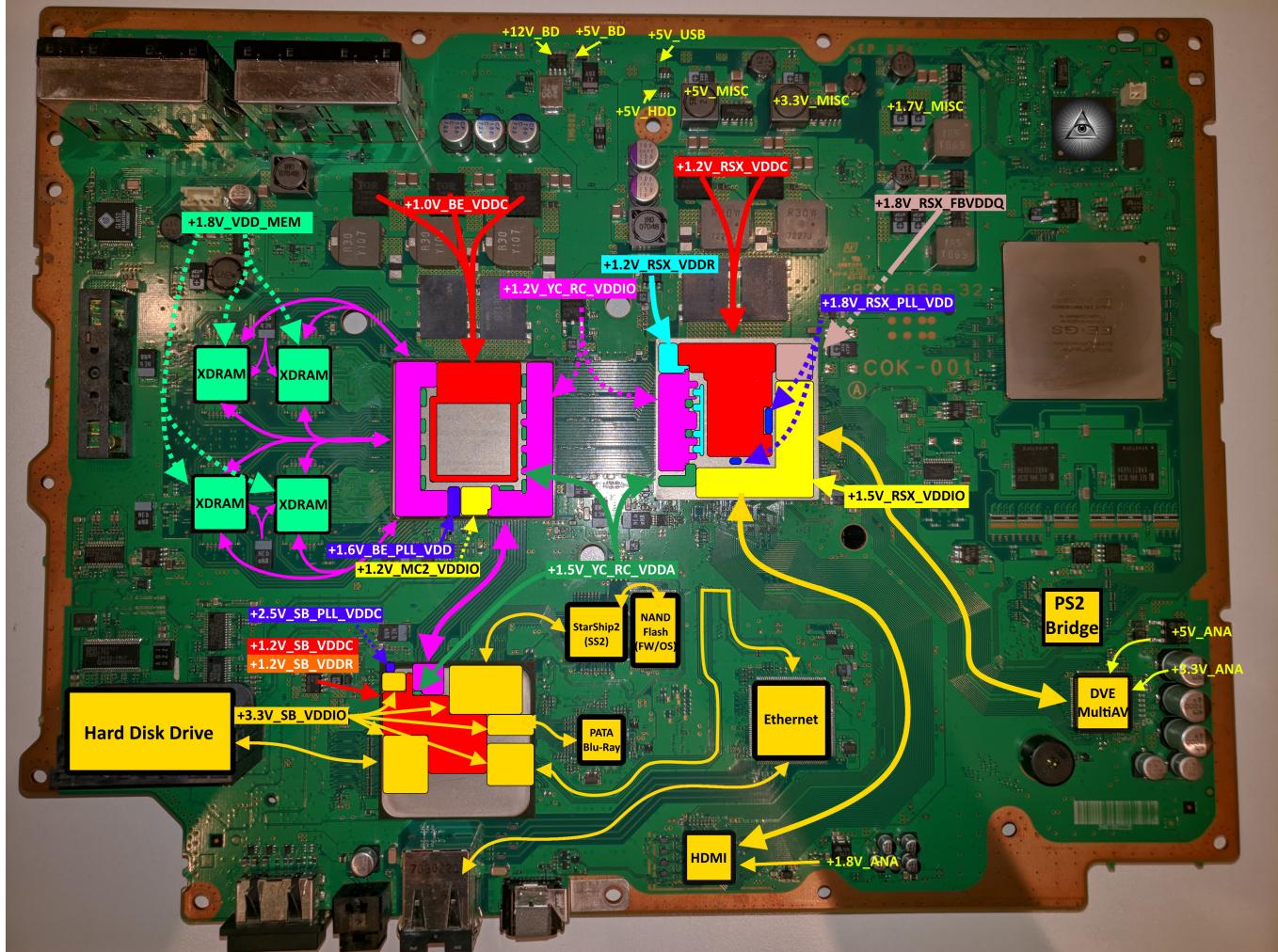
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I understand if that's TMI! It's a complicated process. And that was just IBM's example. As @M4j0r pointed out, SONY deviates from it. That only complicates matters for us. If this interests you at all, I did make an effort to translate the above information in terms of the PS3. To follow is the rotten fruit I yielded...

Initialization Sequence – AKA Power On Sequence Testing (POST).

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**Spoiler: Power On Reset (POR)****Spoiler: Firmware Sequence**

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I'm still trying to figure how the step numbers fit in.

A more simplified overview:

When you use the bringup command in Mullion SYSCONs there are SSM states that seem to indicate when the SYSCON performs certain actions. I made a simplified overview using them...

Spoiler: SSM States

- 000 -> 101
 - Power sequence setup called
 - 12 steps (00 - 11 & 20).
- 101 -> 201
 - AV Backend Setup
- 201 -> 102
 - 2 steps (21 & 22)
 - SW_8_B & SW_8_C enable AV Backend DC/DC converters.
 - HDMI Transmitter initialization. Confirmed using HDMI VFB command in SYSCON.
 - +1.5V_RSX_VDDIO is POR for DVE
- 102 -> 202
 - Doesn't have any steps? I don't have an explanation for this.

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- Must be some kind of RSX initialization/checks.
- 103 -> 203
 - CPU Livelock setup
- 203 -> 104
 - 3 steps (31, 32, & 40)
 - load Configuration Ring Data.
 - 31 3032 = BE Initialization error. Reported when a user knocked R5167 off. +1.2V_YC_RC_VDDIO reference voltage for the CPU's Redwood FlexIO Controller reference clock (BE_RC_REFCLK_P).
 - Calibrate the FlexIO
 - 40 3034 = CPU/GPU (FlexIO) Power Failure (YC_RC_VDDIO) Usually caused by a BGA defect. These are the SPI voltage lines that connect the CPU/GPU.
 - 40 4xxx = Data error (FlexIO). Usually caused by a BGA defect. These are the SPI DATA lines that connect the CPU/GPU.
 - Psbd_SbTransMode_Full:0x20e2
 - 4 steps (50-52 & 60)
 - 50 3035 = Occurred on a console exhibiting 3034/4002 then after a failed reflow attempt 232102. After a pressure test the console GLOD with the 503035. There is an 80 1002 in there too.
 - 60 3040 = NAND/NOR Flash Memory, where the OS firmware is stored. The OS can't load if the chip containing it isn't powered. This would be one of the last checks before the power on state is reached, because a power failure here would prevent the boot loader from initializing.
 - 104 -> 204
 - Doesn't have any steps? I don't have an explanation for this
 - 204 -> 105
 - 3 Steps (61, 62, & FF)
 - 105 -> 400
 - Power On State



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Digging in deeper:

And here I attempted to really dive into exactly what's happening at each Step Number...

Spoiler: Step# A0

SYSCON Reset

- A0 = 2030, 2031, 2033, 2124, 2131.
- When the power Rocker is flipped on, IC6004 receives +5V_EVER directly from the PSU. It produces /SYSCON_RST automatically.
- An error immediately after SYSCON reset probably indicates an issue with the following...
 - SYSCON Reset serves as enable for IC6009, which forms +3.3V_THERMAL for RSX/CPU/SB Thermal Monitors.
 - IC6005/6 are also powered by +5V_EVER and produce +3.3V_EVER and 1.8V_EVER respectively.

Spoiler: Step# 00 - 11

SYSCON Switches on Clocks and Power Supplies (DC/DC converters)

- SYSCON runs "Bringup", "OnStartingBePowOn()", and "PowerSeq_Setup" which enables clocks and DC/DC converters. SYSCON SW Lines control most of the DC/DC converters. SYSCON waits a certain period of time for the voltages to stabilize and Power Good. After that, SYSCON will error at any point if there is a power fail signal on any of the main voltages it's directly monitoring.
- Errors can occur during successive step numbers if the new load and noise generated causes a previously good voltage to fall out of regulation (AC coupling, common mode noise, insufficient decoupling/bypassing etc). So error codes may overlap with later step numbers.
- Note: I don't know which step number corresponds to which Switch exactly, but that could be figured out by sabotaging each DC/DC



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Spoiler: Reported Errors by step#

- A0 = 2030, 2031, 2033, 2124, 2131. Immediately After SYSCON Reset.
- 00 = 2120, +5V_ANA for HDMI (TH2501 bad)
- 00 = 3001, +12V_MAIN from PSU to IC6023. /POW_FAIL Low if bad
- 02 = 2110, +3.3V_MK_VDD (IC6020) for Clock Synthesizer (F6001 or PS6001 Bad)
- 05 = 1004, Unstable power
- 06 = 1002, Unstable Power
- 07 = 1002, Unstable Power
- 08 = 1001, 1002, 1004, Unstable Power
- 09 = 1001, 2024, 2113, 2131, 3003 (BE_POW_FAIL), 3004 (RSX_POW_FAIL)
- 10 = 1001, 1002, 2131 Unstable Power
- 11 = 2131, Dead Thermal Monitor

- Here's what I suspect...

Spoiler: Hypothetical, educated guessing

- 00 = PWR Switch (Rocker on back)
 - Note: +12V_MAIN powers analog voltages. So 00 step numbers are possible with DVE/HDMI errors.
- 01 = SW_0 (5V, 3.3V, 1.7V MISC)
- 02 = SW_1 Start system clocks (powers Clock Synthesizer & Clock Generators).
- 03 = SW_2 (Memory Core voltage)
- 04 = SW_3 (Start SB Digital Logic Core)
- 05 = SW_4 (Ethernet, USB, SB Peripherals, and SB PLL)
- 06 = SW_5 (Power RSX VRM, default VID)

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- A = +1.6V_BE_VDDA & +1.5V_YC_RC_VDDA.
MIC & IOIF Analog Voltages. These Controllers interface Analog signals with the digital Core over the FlexIO interface.
- 10 = PS2 Bridge Chip? (Switches its own subsystem)
- 11 = Maybe just finishing up initialization of the thermal monitors? IDK. One user had 2131 from a dead thermal monitor that gave an error with this step #. He replaced it to fix.

Spoiler: Step# 20 - 22

Initialize CPU/RSX Core and Adjust VRM to VID. AV Backend

Step# 20

- Errors reported with Step# 20 = 1802, 2031, 2120, & 3010
- Bringup calls “BeforeBeOn()”
- SYSCON Initializes the RSX core, VRM adjust voltage according to VID, and the AV backend initializes. If the RSX is dead or missing it returns 20 1802.
 - 20 = SW_8 (RSX)
 - B = +1.5V_YC_RC_VDDIO, +9V_ANA, +5V_ANA, +3.3V_ANA & +1.8V_ANA. Analog Voltages for MultiAV Digital Video Encoder (IC2406), Audio DAC (IC2405), & HDMI Transcoder (IC2502).
 - +1.5V_RSX_VDDIO acts as Power On Reset for the DVE (MultiAV).
 - C = RSX PLL Voltage and thermal monitor initialization.
 - SYSCON enables and sets up the HDMI Transmitter. It communicates over I2C.

Step# 21

- Errors reported with Step# 21 = 3010 & 3013 (CPU voltage related)



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for Soft Start and PWRGD formation (for the voltage to stabilize). I'm not sure how long that procedure takes, but once PWRGD is formed the normal rise time adds about 10µs (RC time constant). 3010 appears to be the error when PWRGD is formed too quickly.

- @DeadEnd got a 20 3010 injecting 3.3v on BE_POWGD. SYSCON didn't like that the timing delay was 0µs. It shouldn't have come back so quickly.
- @Kleon1876 had a 21 3013 when he damaged a CPU trace while delidding. It caused a BE_SPI DI/DO ERROR - CELL not communicating to syscon via SPI. Many others have had 3013 errors associated with 20 2120. Usually associated with Reflows or Mods involving the CPU (eraser mod). Check MC2 VDDIO Bypassing (C1444-1453).

Spoiler: Step# 23

SYSCON checks if CPU/GPU/SB are ready

- Errors reported with Step# 23 = 1002, 1200, 2102, & 3020.
- Not really sure what's going on here.

Spoiler: Step# 30 - 32

EDIT:

Found a connection to the Southbridge and step# 30. In the A01 service manual (pg 20/45) there is a list of sub-systems that are powered by +3.3v_SB_VDDIO. And in that list "SB_MAIN(P30)" is listed. In a series of Sabotage tests, @Computer Booter Lifted EN Pin 3 (IC6305), which disables the main power to the Southbridge. The errors it produced were A0302203 & A0403034 (SB:RRAC:B0:B0:FLEXIO_ID). The step number 30 was produced when SB_Main power was cut!

I didn't make that connection until I was going over the error 60 3040 (NAND Power error). When 3.3v to NAND is cut you get error 60. And in that same list

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telling us what step number each of those sub-systems is powered up in and if we get an error with those numbers, what went wrong.

- P30 = SB_Main
- P31 = SB_Peripheral Parts
- P32 = SB_Rear USB, ATA0, and PCI
- P33 = SB_Front USB
- P34 = SB_ATA1
- P35 = SB_Ethernet
- P40 = SC_Main
- P50 = MK_XCG
- P60 = POWER

Could test this hypothesis, by removing R3846. This will disable the SS2 XEXPOR (power on reset). If we get an error with step number 60, then I'm onto something. This strategy can be used with other voltages on the list, to test the same hypothesis.

Clearly have something to do with the PLL and require the Clock generators to be fully functional.

- Errors reported with Step# 30 = 3030
- Errors reported with Step# 31 = 3031 & 3032
- Errors reported with Step# 32 = Non Reported

- Bringup calls “Before BeOn2()”
- DECR Boot Log shows...

Code:

```
BE_LIVELOCK_MODE:0xff
BE_LIVELOCK_ACTION:0x2
BE_LIVELOCK QUIESCE:0xff
[SSM] state: 0203 -> 0104
```

- Load Configuration Ring Data?
- Differential Signal Power sequencing for BE_RC_REFCLK is needed for timing the FlexIO interface before proceeding to Bit Training. User



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3032 by accidentally knocking R5167 off, which disrupted the True side of Differential reference clock pair output (IC5004 Pin 24, BE_RC_REFCLK_P). I guess that the Complementary side of Differential reference clock pair output (IC5004 Pin 23, BE_RC_REFCLK_N), who's external resistor network can be disrupted by knocking off R5170, would generate error 31 3033. But that should be tested to confirm.

Spoiler: Step# 40

Claibrate the FlexIO (BitTraining)

- Errors reported with Step# 40 = 1301, 2101, 2120, 3034, 4001, 4002, 4102, 4322, 4401, 4402, 4411, 4412, 4421, 4422, & 4432.
- BitTraining Calibrates the FlexIO interface, which is how the SB/CPU/RSX communicate.

Spoiler: Step# 50 - 60

Initialize the IO Interface

- Errors reported with Step# 50 - 52 = 3035 (MK XCG interface or connection?)
- Errors reported with Step# 60 = 3040 (SS2/Flash Power)
- CPU/SB/RSX to begin coordinating and initializing over the I/O interface.
- Not really sure what's happening here exactly, but I guess POR checks each SB peripheral was initialized properly and is not in an error state. If CPU/SB/RSX are not in an error state, then power on self test completed successfully.
- End of POST.



Spoiler: Step# 61 - 62

Load Firmware and OS



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loads.

Spoiler: Step# FF/80

Power On Sequence Finished (System On)

- Errors reported with Step# 80 = 1001, 1002, 1004, 1103, 1200, 1301, 1401, 14FF, 1601, 1701, 1802, 2022, 2024, 2120, 2124, 2203, 5FFF.
- XMB loads and the game console is ready for use.
- Any power related issue that causes the voltage to fall out of regulation, such as excessive ripple/noise can trigger a YLOD.
- Any unresolved CPU errors can cause BE Attention signal to go high. The SYSCON immediately shuts off the console, then reads the SPI Status Register to determine the cause. Then it records the error A0801701 in its errorlog. Errors that can cause the Attention include...
 - Unresolved Checkstop errors (14FF)
 - Livelock Detection (1601)
 - PLL Unlock Condition (1301)
 - BGA/Bump Defect that occurs while the Console was On (Step# 80). Subsequent attempts to power on the console would result in 3034/4xxx errors.

Spoiler: Step# 90

Shutdown Sequence (System Off)

- Errors reported with Step# 90 = 1001, 2024, 2031, 2120, 2124, 2203
- Hypothesis: System settings are saved, and the console powers down. If an error prevents the settings from being saved, the SYSCON will throw an error during this state. Often there are HDMI errors during this step. If BGA defects affect the VDDIO line between the RSX and HDMI Transmitter, it will not be able to save user selected video configuration to the EEPROM on the SYSCON. It stalls during the waiting operation beyond the expected delay, SYSCON assumes there's a problem and

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The following is just here because I don't have a great place to put them. But I still wanted to get it out there for completeness.

Spoiler: Clocks

Clock Synthesizer (IC5001)

- Powered by +3.3V_MK_VDD.
- A 14.31818MHz input crystal (X5001) provides a reference clock from which 4 PLLs generate System clocks.
 - MK_USB_CLK = USB Clock
 - SB_SYSCLK = South Bridge System Clock
 - SB_PCI_CLK = South Bridge PCI Clock
 - SB_PCI0_CLK = South Bridge PCI0 Clock
 - SB_SS2_CLK = South Bridge / Starship2 Clock
 - BC_PCI_CLK = PS2 Bridge Chip PCI Clock
 - RSX_PLL_REFCLK = Processor Clock
 - YRCG0 = Yellowstone / Redwood Clock Generator 0
 - MK_XCG0 = XDR Clock Generator 0
 - <-- BE_PLL_VDDA
 - --> BE_PLL_REFCLK (IC5003)
 - MK_XCG2 = XDR Clock Generator 2
 - <-- +1.2V_YC_RC_VDDIO
 - --> SB_RC_REFCLK (IC5004)
 - --> RSX_RC_REFCLK (IC5004)
 - --> BE_RC_REFCLK (IC5004)
 - YRCG1 = Yellowstone / Redwood Clock Generator 1
 - MK_XCG3= XDR Clock Generator 3
 - --> BE_Y0_RQ (IC5002)
 - --> BE_Y1_RQ (IC5002)

XDR 2-Differential Pair Clock Generator (IC5002)

- Powered by +2.5V_LREG_XCG_500_MEM.
- XCG_EN à EN Pin 11. Where is this sent from?

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BE_Y1_RQ) and read from device 0. Question: What does this accomplish?

- /BYPASS Pin 14 is tied High for PLL Mode

XDR 2-Differential Pair Clock Generator (IC5003)

- Powered by +2.5V_LREG_XCG_500_MEM.
- XCG_EN à EN Pin 11. Pulled High by R5048 when +2.5V_LREG_XCG_500_MEM is present.
- Default SMBus Address select 1 (ID0 Pin 12) is tied low & Address select 2 (ID0 Pin 13) is tied Low. This designates a read operation on device 0 (BE_PLL_VDDA). It also sets the operating mode to Hi-Z, disabling the output.
- /BYPASS Pin 14 is tied High for PLL Mode

XDR 4-Differential Pair Clock Generator (IC5004)

- Powered by +2.5V_LREG_XCG_500_MEM.
- XCG_EN à EN Pin 11. Where is this sent from?
- SMBus Address bit 0 (ID0 Pin 12) is tied low & SMBus Address bit 1 (ID0 Pin 13) is tied High. This forms the device ID and designated operation. In this case a read operation on device 3 (RSX_RC_REFCLK and YC_RC_VDDIO). Question: What does this accomplish?
- /BYPASS Pin 14 is tied High for PLL Mode

Last edited: Feb 6, 2023

Jan 29, 2022 Report

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RIP-Felix
Senior Member

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