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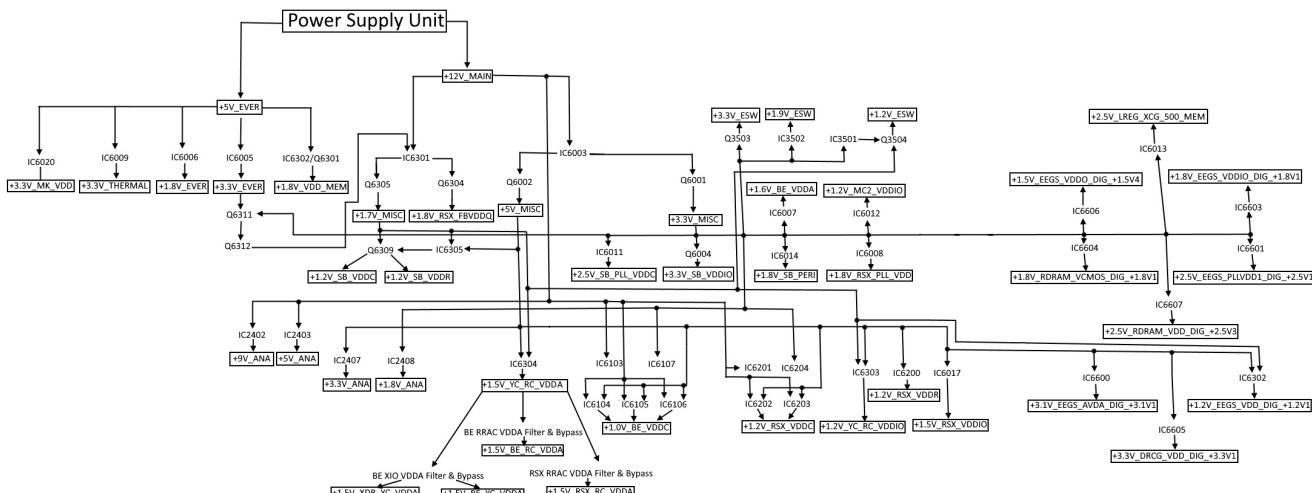
Power Control Topology - Part 2

(Power Good & Voltage Regulation)

Wikipedia said:

*The Power Good signal (**power-good**) is a signal provided by a computer power supply to indicate to the motherboard that all of the voltages are within specification and that the system may proceed to boot and operate*

The PlayStation 3 Power Supply Unit (PSU) outputs 2 voltages from which all other system voltages are derived - 12V_MAIN and 5V_EVER. I made the following flowchart of a COK-001 to illustrate.



Here is the text version...

Spoiler: Voltage Tree

PSU +5V_EVER

- > /SYSCON_RST (IC6004)
- > +3.3V_THERMAL (IC6009)
 - > IC1101
 - > IC2101
 - > IC3101
- > +3.3V_EVER (IC6005)

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--> +1.8V_VDD_MEM (IC6302/Q6301) (JL9647)

PSU +12V_MAIN

--> /POW_FAIL (IC6023) (Error A0003001)

--> +12V_BD (Q6010) (JL6064)

--> +5V_ANA (IC2403)

--> +5V_MISC (IC6003/Q6002)

--> +5V_HDD (Q6006/Q6007) (JL6067)

--> +5V_USB (Q6006/Q6008) (JL6057)

--> +5V_BD (Q6010) (JL9658)

--> +3.3V_MK_VDD (IC6020) (JL6053)

--> +3.3V_Bridge (IC6022) (JL6070)

--> +3.3V_DRCG_VDD_DIG_+3.3V1 (IC6605) (JL6360)

--> +3.1V_EEGS_AVDA_DIG_+3.1V1 (IC6600) (JL6359)

--> +1.2V_RSX_VDDR (IC6200) (JL9651)

--> +1.5V_RSX_VDDIO (IC6017) (JL9656)

--> +1.5V_YC_RC_VDDA (IC6304) (JL9655)

--> +1.2V_EEGS_VDD_DIG_+1.2V1 (IC6302) (JL6361)

--> +1.2V_YC_RC_VDDIO (IC6303) (JL9652)

--> +1.2V_SB_VDDC (IC6305) (JL9648)

--> +1.2V_ESW (IC3501) (JL9649)

--> +1.2V_RSX_VDDC, RSX VRM (2 Phase)

--> IC6202 (JL6205/6)

--> IC6203 (JL6207/8)

--> +1.0V_BE_VDDC, CELL BE VRM (3 phase)

--> IC6104 (JL6109/10)

--> IC6105 (JL6111/12)

--> IC6106 (JL6113/14)

--> +3.3V_MISC (IC6003/Q6601)

--> +3.3V_SB_VDDIO (Q6004) (JL6058)

--> +3.3V_ESW (Q5303) (JL3551)

--> +2.5V_EEGS_PLLVDD1_DIG_+2.5V1 (IC6601) (JL6357)

--> +2.5V_RDRAM_VDD_DIG_+2.5V3 (IC6607) (JL6358)

--> +2.5V_SB_PLL_VDDC (IC6011) (JL6060)

--> +2.5V_LREG_XCG_500_MEM (IC6013) (JL6054)

--> +1.8V_RSX_PLL_VDD (IC6008) (JL6048)

--> +1.8V_SB_PERI (IC6014) (JL6061)



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--> +1.5V_AVCG_VDDIO (IC6019) (JL6056)
--> +1.5V_Bridge (IC6021) (JL6069)
--> +1.5V_EEGS_VDDO_DIG_+1.5V4 (IC6606) (JL6354)
--> Q6311 (**What's happening here?**)
--> +1.2V_MC2_VDDIO (IC6012) (JL6063)
--> +1.2V_RSX_VDDC (IC6204) --> DRVON --> ENABLE (IC6202/3)
--> +1.0V_BE_VDDC (IC6107) --> DRVON --> ENABLE (IC6104/5/6)
--> +1.7V_MISC (IC6301/Q6305) (JL9656)
--> +1.5V_YC_RC_VDDA (Q6308) (JL9655)
--> +1.2V_SB_VDDC (Q6309) (JL9648)
--> +1.2V_SB_VDDR (Q6309) (JL9648)
--> +1.2V_YC_RC_VDDIO (Q6310) (JL9652)
--> +1.2V_RSX_VDDR (Q6200) (JL9651)
--> +1.2V_EEGS_VDD_DIG_+1.2V1 (Q6600) (JL6361)
--> +1.2V_ESW (Q3504) (JL9649)
--> +1.8V_RSX_FBVDDQ (IC6301/Q6304) (JL9657)
--> +1.2V_RSX_VDDC
 --> IC6201 (2 Phase Buck Controller)
 --> IC6202 (JL6205/6)
 --> IC6203 (JL6207/8)
--> +1.0V_BE_VDDC
 --> IC6103 (3 Phase Buck Controller)
 --> IC6104 (JL6109/10)
 --> IC6105 (JL6111/12)
 --> IC6106 (JL6113/14)

12V_MAIN is the one from which most other system voltages are derived (5V, 3.3v, 1.8v, 1.7, 1.2, 1.0 etc). The CPU/GPU/SB, are all powered from this 12V_MAIN. But each one of them has a chain of chips before the correct voltage can get to them. The purpose of these chips is to provide stable voltage and control of when that voltage is delivered.

For example, the CPU's 1.0V_BE_VDDC is produced by its Voltage Regulation Module (VRM). It includes IC6103, a buck controller which drives IC6104, IC6105, IC6106 buck converters. That controller is enabled by the syscon chip at

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Module.

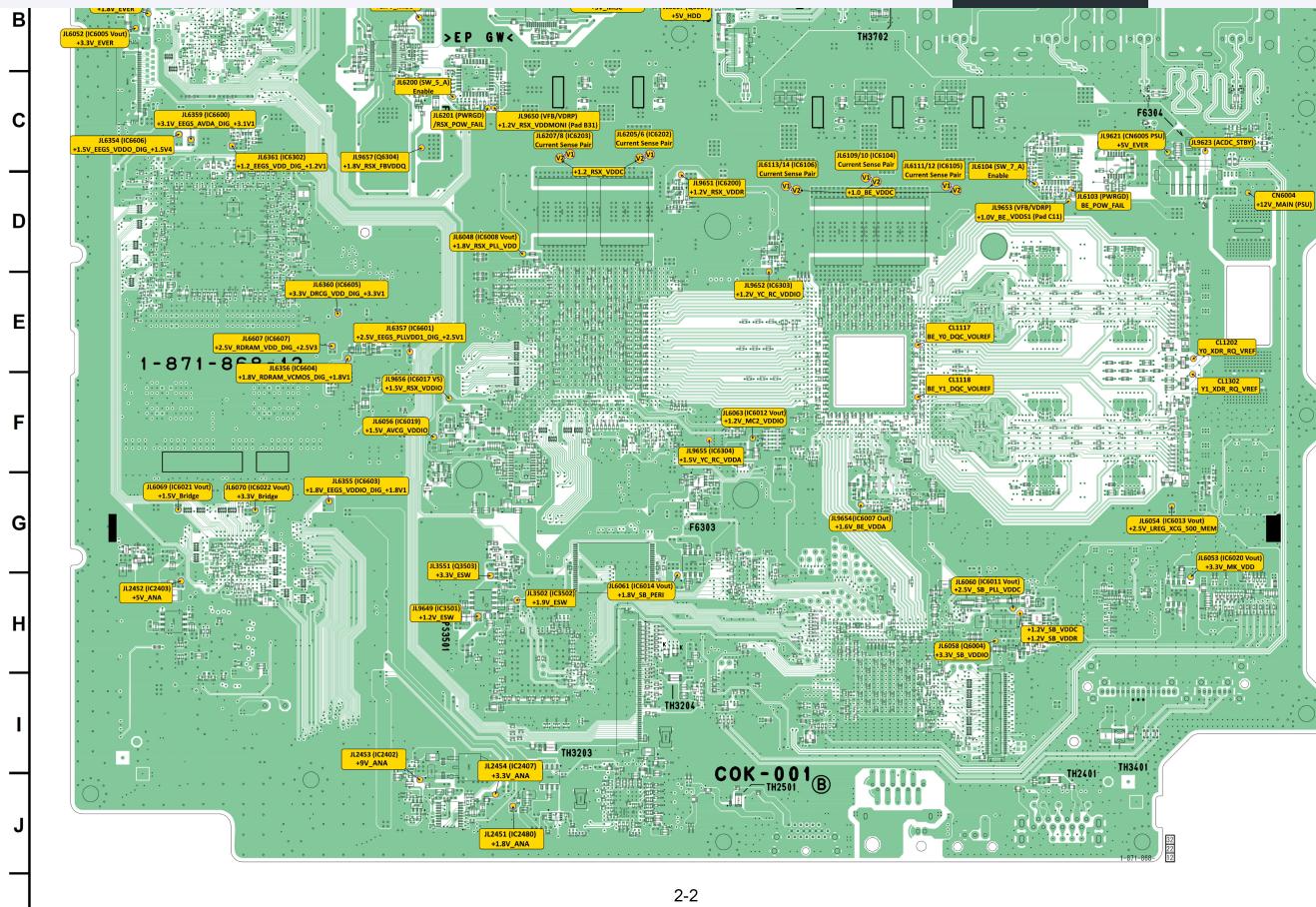
The RSX has it's own VRM, the SB too. Most subsystems have have an IC controller that enables their voltage at the appropriate time in the Power On Sequence. The Voltage flowchart I made above is the general manner in which these subsystems receive their voltages. Not every IC in the PS3 is listed, just the major ones involved in producing the system voltages marked by a square box. Also that image was based off the COK-001 Service Manual. It does not apply to all models, but can be used as a general guide for them. Obviously, the PS2 Hardware section will not be included in non-backward compatible models.

How does this relate to power good? Well, each system voltage in a box in that image has a controller IC that is monitoring it's output voltage. If that voltage is within regulation, it will report power good to the SYSCON "system control." If any one of them falls out of regulation and reports no power good, the syscon will refuse to boot.

The voltage flowchart above combined with the MB Side B "Jumper Lead" Test Pad locations below should make diagnosing and troubleshooting easier.

A blue rectangular button with a white gear icon and the word "privacy" written vertically next to it.

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I made this one from scratch, with high enough resolution to read the Labels and to still upload to the forum. I was really pushing the limit here. This will make it easier for you to search the service manual when you find a voltage that's missing. When I say this took a long time to make, it's an understatement.

Speaking of time consuming projects. Here's more fruit from that effort.

Spoiler: Abbreviations

ATA = Hard Drive Interface

BC = PS2 Bridge Chip

BEI = Redwood Broadband Engine Interface Controller (AKA RC)

CE = Control Enable

CELL BE = CPU (“Cell Broadband Engine”)

CG = Clock Generator

CLK = Clock

CONT = Control



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EN = Enable

ESW = Ethernet Switch or Switchable

FB = Feedback

FlexIO = Redwood Rambus FlexIO CPU/GPU Interface

GS = Graphics Synthesizer (PS2 GPU)

MC2 = ? (VDDIO à BE_SPI, CHKSTP, JTAG, TBEN, & P_L_BYPASS)

MIC = Yellowstone Memory Interface Controller (AKA YC)

PCI = PS2 Hardware Interface

PLL = Phase-Locked Loop

PPE = Power Processor Element (main dual threaded CPU)

PWRGD = Power Good

RC = Redwood Broadband Engine Interface Controller (AKA BEI)

RRAC = Redwood Rambus FlexIO CPU/GPU Interface Voltage (VDDR)

RST = Reset

RSX = GPU ("Reality Synthesizer")

SB = South Bridge

SPE = Synergistic Processing Element (8x, 1 disabled for redundancy)

STBY = Standby

SW = Switch

VDD = Positive Field Emitting Transistor (FET) Voltage

VDDA = Positive FET Voltage Supply for Analog Subsystems

X = Rambus XDRAM Memory Subsystem

XDR = Yellowstone XDRAMTM System Memory (Y0_XDR0, Y0_XDR1,

Y1_XDR0, & Y1_XDR1)

XGC = XDRAM Clock Generator

XIO = Yellowstone Rambus CPU/XDR Memory Interface ("Extreme Data Rate IO")

YC = Yellowstone Memory Interface Controller (AKA MIC)

YRAC = Yellowstone Rambus CPU/XDR Memory Interface Voltage

Spoiler: System Voltage Definitions

+1.0V_BE_VDDC = Cell Be Processor Core (PPE/SPEs)

+1.5V_BE_THERMAL_VDDA = CPU Thermal Power?

+1.6V_BE_VDDA = CPU ADC Voltage for PLL & Thermal

+1.5V_BE_YC_VDDA = CPU/XDR Yellowstone XIO Controller ADC Interface



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- +1.2V_RSX_VDDR = RSX Redwood Rambus FlexIO Core
- +1.2V_RSX_VDDC = RSX Processor Core
- +1.5V_RSX_RC_VDDA = RSX Redwood Rambus FlexIO Controller ADC Interface
- +1.5V_RSX_VDDIO = VDDP_VO (Voltage for Picture, Video Out to DVE/HDMI)
- +1.8V_RSX_PLL_VDD = RSX Phase-Locked Loop
- +1.8V_RSX_FBVDDQ = RSX DRAM

- +1.2V_YC_RC_VDDIO = XDR/CPU/SB Yellowstone XIO & Redwood Rambus FlexIO Core
- +1.2V_MC2_VDDIO = BE_SPI, CHKSTP, JTAG, TBEN, & P_L_BYPASS
- +1.5V_XDR_YC_VDDA = Yellowstone Memory Interface Controller
- +1.5V_YC_RC_VDDA = CPU/SB Yellowstone XIO & Rambus FlexIO Controller ADC Interface
- +1.8V_VDD_MEM = XDRAM Voltage

- +1.2V_ESW = Ethernet Controller (IC3503) VDD_Core (IC3501/Q3504)
- +1.9V_ESW = Ethernet Controller (IC3503) VDDAH (IC3502)
- +3.3V_ESW = Ethernet Controller (IC3503) VDDO (Q3501)

- +1.2V_SB_VDDC = Southbridge Processor Core
- +1.2V_SB_VDDR = SB Redwood Rambus FlexIO Core
- +1.8V_SB_PERI
 - = VCC18 Starship2 Flash Controller
 - = VDDP Starship2 Flash Controller
 - = SB_ATA1 (P34)
 - = Power (P60)
- +2.5V_SB_PLL_VDDC =Southbridge Phase-Locked Loop
- +3.3V_SB_VDDIO
 - = VDD33 Starship2 Flash Controller
 - = Nand Flash 0 & 1
 - = SB_Main EBUS (P30)
 - = SB_Peripheral Parts (P31)
 - = SB_Rear USB, ATA0, & PCI (P32)
 - = SB_Front USB (P33)
 - = SB_ATA1 (P34)

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Spoiler: SYSCON Switches (Enable & Control)

/SYSCON_RST --> EN Pin 3 (IC6009) --> +3.3V_THERMAL

--> Vdd Pin 1 (IC1101)

--> Vdd Pin 1 (IC2101)

--> VDD Pin 8 (IC3101)

/BE_POW_FAIL <-- PWRGD Pin 7 (IC6103) (JL6103)

/RSX_POW_FAIL <-- PWRGD Pin 7 (IC6201) (JL6201)

/POW_FAIL (12V) --> OUT Pin 4 (IC6023)

SW_ATA --> Enables Gate Pin 2 (Q6006) --> Enables Gate (Q6007) -->
+5V_HDD

SW_PCI

--> CONT Pin 5 (IC6021) --> +1.5V_Bridge (IC7301)

--> CONT Pin 5 (IC6022) --> +3.3V_Bridge (IC7301)

SW_0

--> CTL1 Pin 9 (IC6003) --> +5V_MISC

--> CTL2 Pin 10 (IC6003) --> +3.3V_MISC

--> STBY2 Pin 10 (IC6301) --> +1.7V_MISC

SW_1_A --> CONT Pin 5 (IC6020) --> +3.3V_MK_VDD (IC5001)

- For Clock Synthesizer

SW_1_B --> CONT Pin 5 (IC6013) --> +2.5V_LREG_XCG_500_MEM

- Analog Voltage for the core PLL of IC5004, which is an ICS9214 Clock Generator used to support the Rambus XDR memory subsystem and Redwood logic interface.

SW_2

--> IN_PSV Pin 1 (IC6302) --> +1.8V_VDD_MEM (JL9647)



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--> +1.2V_SB_VDDR (JL9648)

SW_4_A

--> Base Q3501
--> Enable Pin 3 (IC3501) --> +1.2V_ESW
--> CONT Pin 5 (IC3502) --> +1.9V_ESW
--> Base (Q3502) --> Base (Q3503) --> +3.3V_ESW
--> P3_ENABLE PD Pin 93 (IC3503) --> Ethernet Controller

SW_4_B

--> Enables Gate Pin 5 (Q6006) --> Enables Gate (Q6008) --> +5V_USB
--> CONT Pin 5 (IC6014) --> +1.8V_SB_PERI
--> EN Pin 3 (IC6011) --> +2.5V_SB_PLL_VDDC

SW_5_A

--> Enable Pin 29 (IC6201)
--> PWM Pin 3 (IC6202) --> +1.2V_RSX_VDDC (JL6205/6)
--> PWM Pin 3 (IC6203) --> +1.2V_RSX_VDDC (JL6207/8)

SW_6

--> CE Pin 3 (IC6012) --> +1.2V_MC2_VDDIO
--> EN Pin 3 (IC6303) --> +1.2V_YC_RC_VDDIO (JL9652)

SW_7_A

--> Enable Pin 29 (IC6103)
--> PWM Pin 3 (IC6004) --> +1.0V_BE_VDDC
--> PWM Pin 3 (IC6005) --> +1.0V_BE_VDDC
--> PWM Pin 3 (IC6006) --> +1.0V_BE_VDDC

SW_8_A

--> EN Pin 3 (IC6007) --> +1.6V_BE_VDDA (JL9654)
--> EN Pin 3 (IC6304) --> +1.5V_YC_RC_VDDA (JL9655)

SW_8_B

--> EN Pin 3 (IC6019) --> +1.5V_AVCG_VDDIO (IC2102)
--> EN Pin 3 (IC6017) --> +1.5V_RSX_VDDIO



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--> STBY1 Pin 9 (IC6301) --> +1.8V_RSX_FBVDDQ

To PS2 Bridge

SW_1.2 --> EN Pin 3 (IC6602) --> +1.2V_EEGS_VDD_DIG_+1.2V1 (JL6361)

SW_1.5 --> CE Pin 5 (IC6606) --> +1.5V_EEGS_VDDO_DIG_+1.5V4 (JL6354)

SW_1.8 --> EN Pin 3 (IC6604) --> +1.8V_RDRAM_VCMOS_DIG_+1.8V1
(JL6356)

SW_1.81 --> CONT Pin 5 (IC6603) --> +1.8V_EEGS_VDDIO_DIG_+1.8V1
(JL6355)

SW_2.5 --> EN Pin 3 (IC6601) --> +2.5V_EEGS_PLLVDD1_DIG_+2.5V1 (JL6357)

SW_2.65 --> CONT Pin 5 (IC6607) --> +2.5V_RDRAM_VDD_DIG_+2.5V3
(JL6358)

SW_3.1 --> CE Pin 3 (IC6600) --> +3.1V_EEGS_AVDA_DIG_+3.1V1 (JL6359)

SW_3.3 -->CONT Pin 3 (IC6605) --> +3.3V_DRCG_VDD_DIG_+3.3V1 (JL6360)

AUDIO Pin 16 (IC2102)

- --> RSX_AVCLK3
- --> A1 Pin 2 (IC2105)
 - --> DRCG_GEN18M --> Xin Pin 4 (IC7001) --> IC7002 (RDRAM)
 - --> IC7003 (RDRAM)
 - --> IC7004 (EE+GS)

Do not take the above as gospel. If you notice anything needing updated let me know and I'll edit back as necessary.



Getting back to Power good:

Notice the GPU Buck Controller (IC6201). It's locate at B5. This controller is what controls power to the RSX. I have labeled the jumper locations for Enable, which is the signal SYSCON sends to power on the RSX. I also labeled Power Good (PWRGD), which is the signal the controller sends back to the SYSCON about the power regulation. If it's bad, /RSX_POW_FAIL goes low and the syscon throws an error. Which error? 3004 or 1002. Which one is a mystery still. I hypothesize it depends upon the Step number of the Power On Sequence. Basically, when power good went low. The hypothesis is that earlier step numbers = 3004. Later step

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The last pad I labeled on the RSX VRM Controller is the voltage feedback/drop jumper. This is what the controller is monitoring to decide if power is good or not. We should be able to probe this point to see voltage drop across RSX_VDDC. If it drops too much it triggers under voltage lock out and the controller will send no power good (PWRGD low). The syscon will error. The CPU has the same and other controllers around the board have a similar function.

Since, preventing voltage drops on the CPU/GPU is important for system stability, the NEC/TOKIN's are a concern. If they can't sustain the voltage for long enough underload, the voltage drop will fall out of regulation. One way to prevent this is to replace failing/aged tokins with new tantalum capacitors. Everyone is already familiar with that. But there is another way. By adjusting the power good voltage dropout threshold, so that there is a wider range the voltage can fall before triggering an error.

Adjusting Power Good Threshold

Vid pins VID0-5 on the buck controller form a 6-digit code corresponding to the Vout No load setpoint. Power Good Vmin and Vmax thresholds are relative to that set point. With the stock COK-00X voltage divider values (15K and 20k), Vmin = -163mV. Vmax is always +100mV. The Vout voltage cannot deviate more than that. If it does power good goes low and the SYSCON will error.

$$V_{LOWER} = \frac{V_{OUTNoLoad}}{2} \times \frac{R_1 + R_2}{R_2}$$

$$V_{UPPER} = V_{OUTNoLoad} + 100 \text{ mV}$$

In some official SONY refurbished consoles, new resistor values (27K and 10K) change Vmin = -400mV. So the Low Voltage threshold is now more than twice as low, allowing much more voltage ripple before it triggers an error. My hypothesis is SONY did this to reduce the frequency of 1001 and 1002's errors. That would explain why they did it to both buck controllers (CPU and GPU). A sort of admission of guilt that they either set it too aggressively or were compensating for bad NEC/TOKINs without replacing them.



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Currently, 1002's are assumed to be bad NEC/TOKIN's. Replacing aged bulk filter capacitors certainly works, but just because changing them fixes the error doesn't mean that's the only way to skin a cat.

I have intentionally held off recommending this mod to people, because I'm only freshly aware of it's potential. Before I conclude this is okay to do, I would like to know what the VID at idle is, so we can compare actual voltage measurements with the low voltage threshold. On a console with 1001/1002 errors, Vout should drop more than that before it experiences a YLOD. That means I need oscilloscope measurements of Vout on both the CPU/GPU and PWRGD. Then, by replicating Sony's mod, I would like to see if the error goes away AND the system is stable (requires stress testing)! If so, then we have discovered an easier method of resolving these errors.

Replacing those resistors is fine micro-soldering work that pretty much requires a microscope. And I need oscilloscope measurements of the voltage drop and PWRGD (Cell BE for 1001 and RSX for 1002). So it's not too easy or cheap.

That's more than enough to digest for now.

To be concluded...

Last edited: Feb 6, 2023

Dec 18, 2021 Report

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vyktormvmpay25
Senior Member

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@feng_ye your software side is fine, otherwise you won't be able to see "Connecting to Debug Device (SB UART)."

This is either one missing resistance from rsx side to AV ic /Hdmi ic, either that special glod. If you want to try exchange AV ic or Hdmi ic is your choice, or focus and compare that area. not sure what to say from here, but I am sure no software errors on that unit.

