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A New Simplified Space–Vector PWM Method for Three-Level Inverters

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***Abstract*—In this paper, a new simplified space–vector pulse width modulation (SVPWM) method for three-level inverter is proposed. This method is based on the simplification of the space–vector diagram of a three-level inverter into that of a two-level inverter. If simplified by the proposed method, all the remaining procedures necessary for the three-level SVPWM are done like conventional two-level inverter and the execution time is greatly reduced. The dc-link neutral-point potential control algorithms are implemented more easily. And the proposed method can be applied to the multi-level inverters above three-level. The validity of the new SVPWM method is verified by experiment with a 1000 KVA three-level insulated gate bipolar transistor (IGBT) inverter.**

***Index Terms*—Multilevel inverter, space-vector PWM, three-level inverter.**

I. Introduction

RECENTLY, with the dramatic improvements in high voltage technologies, high voltage insulated gate bipolar transistor (HVIGBT) and gate commutated thyristor (GCT) are expanding the area of their application. For the high performance ac drive systems at increased power level, high quality inverter output with low harmonic loss and torque pulsation is necessary. In case of the conventional two-level inverter configuration, the harmonic contents reduction of an inverter output current is achieved mainly by raising the switching frequency.

However in the field of high voltage, high power applications, the switching frequency of the power device has to be restricted below 1 KHz, even with the HVIGBT and GCT, due to the increased switching loss. So the harmonic reduction by raised switching frequency of a two-level inverter becomes more difficult in high power applications. In addition, as the dc link voltage of a two-level inverter is limited by voltage ratings of switching devices, the problematic series connection of switching devices is required to raise the dc link voltage. By series connection, the maximum allowable switching frequency has to be more lowered, thus the harmonic reduction becomes more difficult.

From the aspect of harmonic reduction and high dc-link voltage level, three-level approach seems to be the most promising alternative. The harmonic contents of a three-level inverter are less than that of a two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the dc-link voltage. So the three-level inverter topology is generally used in realizing the high performance, high voltage ac drive systems [1].

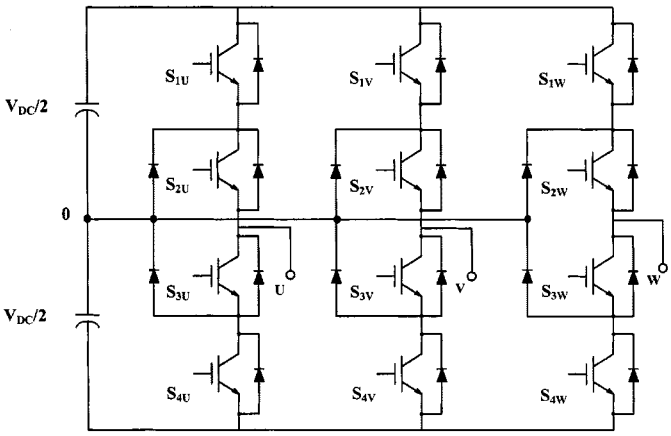

Fig. 1. Circuit diagram of a three-level inverter.

However, the inherent neutral-point potential variation of a three-level inverter has to be effectively suppressed to fully utilize the above-mentioned advantages of a three-level inverter. So many PWM strategies have been proposed to solve the neutral-point potential unbalance problem [2], [3], [5]. But many of them are focused mainly on the neutral-point potential control method, while still using the complicated dwelling time calculation and the switching sequence selection method.

In this paper, a simple SVPWM method for three-level inverter is proposed. By using the new PWM strategy, dwelling time calculation and switching sequence selection are easily done like conventional two-level inverter. And the neutral-point voltage control algorithm can be easily implemented. In this paper, the proposed three-level SVPWM method is explained in detail and verified using 2500 V, 1000 KVA three-level IGBT inverter system.

II. Simplified Space–Vector PWM Method

A. Basic Principles of the Proposed SVPWM Method

Fig. 1 is a circuit diagram of a three-level inverter and the switching states of each phase of the inverter are listed in Table I. There are three kinds of switching states P, O, and N in each phase, so there exist 27 switching states in three phase three-level inverter.

By using the space–vector diagram of a three-level inverter, the basic principle of the proposed SVPWM method can be

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TABLE I
SWITCHING STATES AND TERMINAL VOLTAGES OF A THREE-LEVEL INVERTER (X = U, V, W)

Switching Symbols	Switching States				Terminal Voltage
	S_{1X}	S_{2X}	S_{3X}	S_{4X}	
P	ON	ON	OFF	OFF	$V_{DC}/2$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-V_{DC}/2$

easily explained. The space–vector diagram of a three-level inverter, shown in Fig. 2, can be thought that it is composed of six small hexagons that are the space–vector diagrams of conventional two-level inverters. Each of these six hexagons, constituting the space–vector diagram of a three-level inverter, centers on the six apexes of the inner small hexagon as is shown in Fig. 3. So, if these six small hexagons are shifted toward the center of the inner hexagon by $V_{dc}/3$, the space–vector diagram of a three-level inverter is simplified to that of a two-level inverter. To simplify into the space–vector diagram of a two-level inverter as explained above, the following two steps have to be taken. First, from the location of a given reference voltage, one hexagon has to be selected among the six hexagons. Secondly the original reference voltage vector has to be subtracted by the amount of the center voltage vector of the selected hexagon. By these two steps, the three-level space–vector plane is transformed to the two-level space–vector plane.

Then the determination of switching sequence and the calculation of the voltage vector duration time are done as conventional two-level SVPWM method. As the proposed SVPWM method is same in principle as conventional two-level SVPWM, various techniques used in two-level SVPWM can be applied to this proposed method too.

B. Correction of Reference Voltage Vector

In this section, the first procedure for the simplified three-level space–vector PWM method is described in detail. By the location of a given reference voltage vector, one hexagon is selected among the six small hexagons that comprise the three-level space–vector diagram. The reference voltage vector should stay at the inner of the selected hexagon. This procedure divides the three-level space–vector diagram into six regions that are covered by each small hexagon as shown in Fig. 3. The value of s in Fig. 3 represents the selected hexagon. There exist the regions that are overlapped by adjacent small hexagons in the three-level space–vector diagram. So if the reference voltage vector stays at those regions, s can have any values that are possible. Fig. 3(a) and (b) illustrate two possible ways of selecting the value of s. If those methods shown in Fig. 3(a) and (b) are used, the value of s at the shaded region of Fig. 2 can have the value of 1 or 2.

Once the value of s is determined, the origin of a reference voltage vector is changed to the center voltage vector of the selected hexagon. This is done by subtracting the center vector of the selected hexagon from the original reference vector, as shown in Fig. 4. This is summarized in Table II.

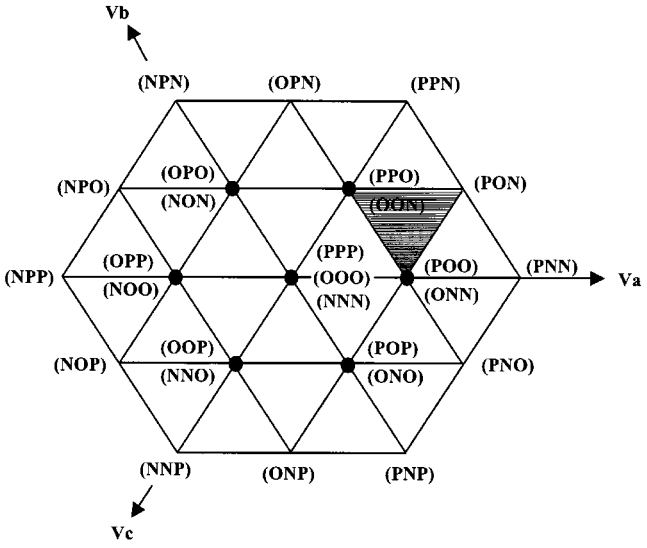

Fig. 2. Space–vector diagram of a three-level inverter.

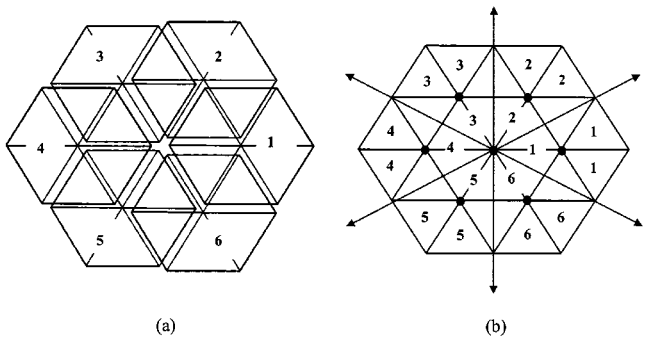

Fig. 3. Simplification of a three-level space–vector diagram.

In Fig. 4, V^* is the original reference voltage vector and $\hat{U}^*$ is the corrected reference voltage vector seen from the location of the (POO), (ONN) vector.

Following is the sample program of this procedure explained in this section.

```
If(V*_a_ref V*_b_ref V_c_ref ≥ 0) {
    If(V_a_ref ≥ 0.)          {s = 1;  a = 2;  b = −1;}
    else if(V_b_ref ≥ 0.)     {s = 3;  a = −1;  b = 2;}
    else                      {s = 5;  a = −1;  b = −1;}
}
else {
    If(V_a_ref < 0.)          {s = 4;  a = −2;  b = 1;}
    else if(V_b_ref < 0.)     {s = 6;  a = 1;  b = −2;}
    else                      {s = 2;  a = 1;  b = 1;}
}
V_a_ref− = a*V_dc/6;.
V_b_ref− = b*V_dc/6;.
V_c_ref = −V_a_ref − V_b_ref;
```

Sample Program for the Simplifying of the Three-Level Space–Vector Diagram

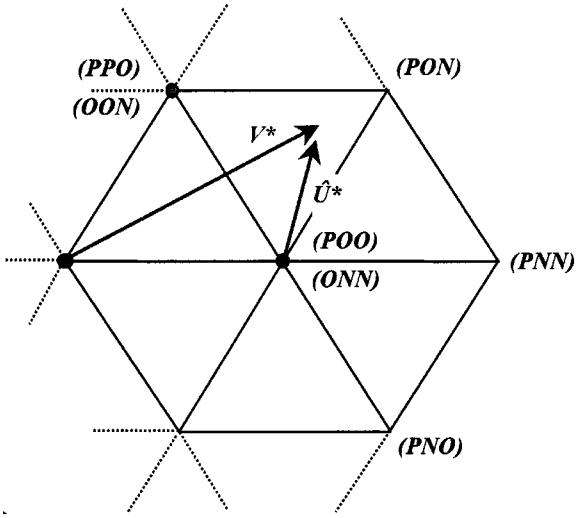

Fig. 4. Changing the base vector of an original reference voltage vector.

C. Calculation of the Dwelling Times

If the reference voltage vector is redefined as explained in the previous section, the dwelling times are calculated at the same manner as conventional two-level SVPWM method. The calculation of dwelling times can be done more efficiently by the method presented in [4] as shown in the following example. In calculating the dwelling times, the only difference between the two-level SVPWM and the three-level SVPWM is the factor 2 appearing at the first two lines of the following example.

$T_a = 2.^*V^*_{as\_ref}T_{samp}/V_{DC};$
$T_b = 2.^*V^*_{bs\_ref}T_{samp}/V_{DC};$
$T_c = -(T_a + T_b);$
`if`$(T_a > T_b) \quad \{a = T_a; \quad b = T_b;\}$
`else`$\{a = T_b; \quad b = T_a;\}$
`if`$(T_c > a) \quad a = T_c;$
`if`$(T_c < b) \quad b = T_c;$
$T_0 = T_{samp} - (a - b);$
$a = T_0^*(1 - f) - b;$
$T_a += a; \quad T_b += a; \quad T_c += a;$
`if`$(Flag\_on\_off)$
$\{T_a = T_{samp} - T_a;$
$T_b = T_{samp} - T_b;$
$T_c = T_{samp} - T_c;\}$

Sample Program for the Dwelling Time Calculation

If the dwelling times are calculated, the switching sequence has to be determined. However the switching sequence is determined automatically by the value of s. That is, on the basis of the center voltage vector of the selected hexagon, the switching sequence is determined as conventional two-level inverter. For example, in case of Fig. 4, the switching sequence will be (POO)-(PON)-(OON)-(ONN). If the (ONN) vector is selected as a base and the notations used in two-level space–vector diagram are adopted, the switching sequence can be expressed as (111)-(110)-(010)-(000). This switching sequence is exactly the same as that of conventional two-level SVPWM. Therefore in determining the switching sequence, the only thing to do is selecting the switches that have to be enabled to change their states among the four switches in each phase. This is realized by simple logic gates using the value of s.

TABLE II
REFERENCE VOLTAGE VECTOR CORRECTION OF THE PROPOSED SVPWM METHOD

S	Vas_ref =	Vbs_ref =
1	Vas_ref – Vdc/3.	Vbs_ref + Vdc/6.
2	Vas_ref – Vdc/6.	Vbs_ref – Vdc/6.
3	Vas_ref + Vdc/6.	Vbs_ref – Vdc/3.
4	Vas_ref + Vdc/3.	Vbs_ref – Vdc/6.
5	Vas_ref + Vdc/6.	Vbs_ref + Vdc/6.
6	Vas_ref – Vdc/6.	Vbs_ref + Vdc/3.

(*) Vcs_ref= -Vas_ref – Vbs_ref

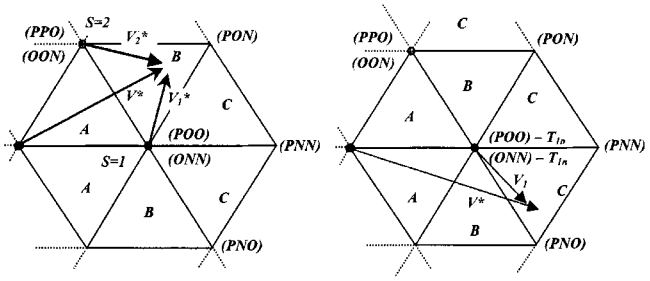

Fig. 5. Neutral-point potential control of a three-level inverter.

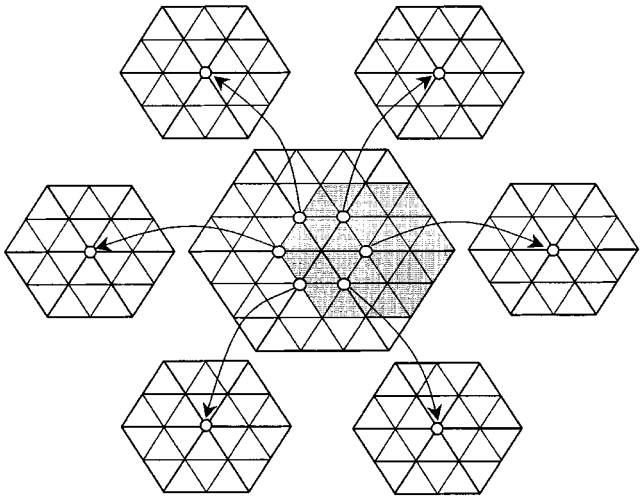

Fig. 6. Application of the proposed SVPWM method to the four-level inverter.

D. Neutral-Point Potential Control

It is well known that there are two methods controlling the neutral-point potential of a three-level inverters. The first is changing the switching sequence and the second is rearranging the time distribution of the redundant voltage vectors. These two methods can be easily implemented with the proposed SVPWM method. The switching sequence is easy to change using the index s.

1) Method 1: Changing the Switching Sequence

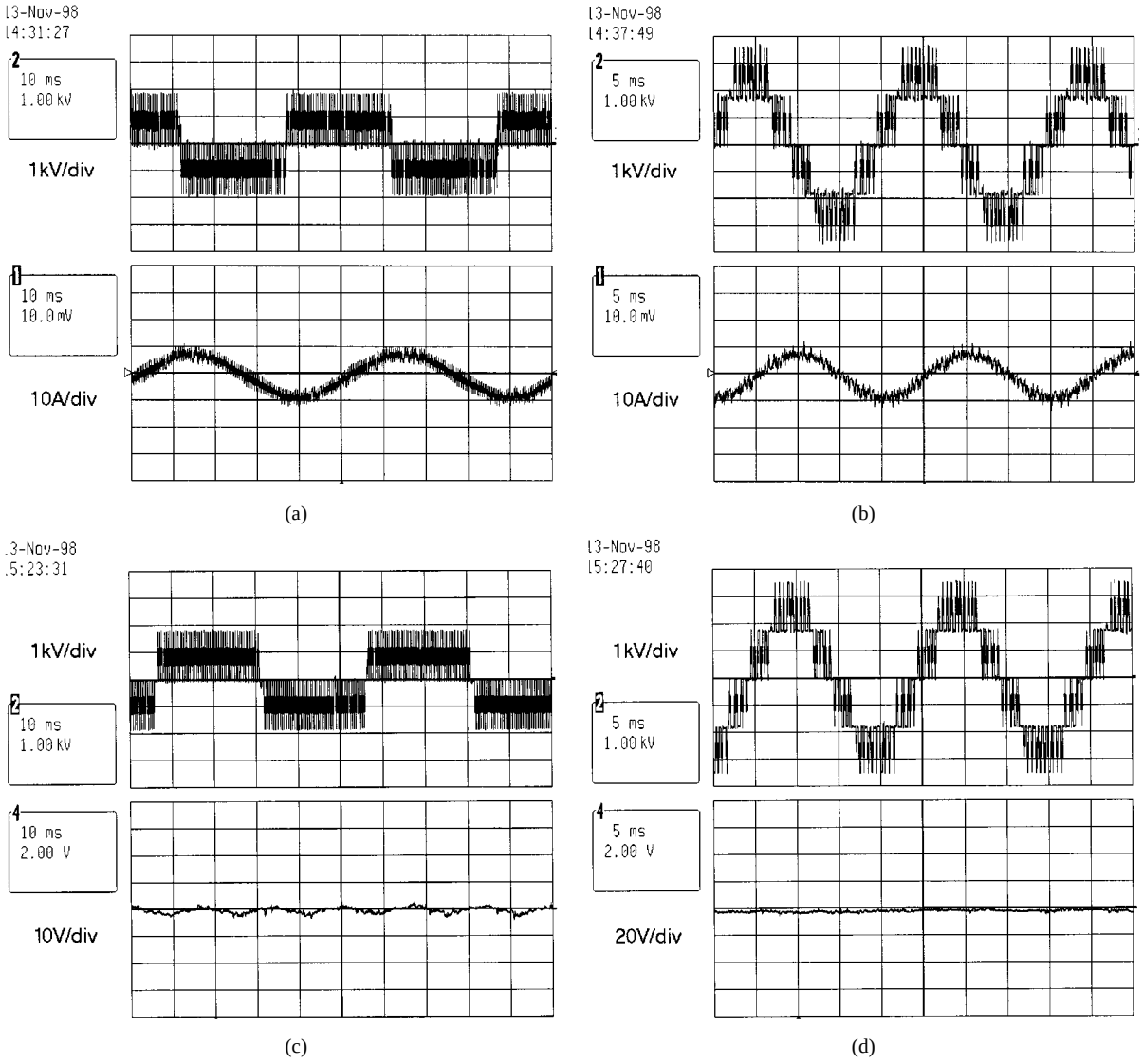

Fig. 7. Test results of the proposed SVPWM method with 100 kW induction motor. (a) Line-to-line voltage and phase current at $f_0 = 20$ [Hz]. (b) Line-to-line voltage and phase current at $f_0 = 50$ [Hz]. (c) Line-to-line voltage and dc-link voltage error $(V_{c1} - V_{c2})$ at $f_0 = 20$ [Hz]. (d) Line-to-line voltage and dc-link voltage error $(V_{c1} - V_{c2})$ at $f_0 = 20$ [Hz].

If the reference voltage vector stays at the region, that is overlapped by adjacent small hexagon, the neutral-point potential can be controlled by changing the switching sequence. When the reference is given as in Fig. 5(a), the index s can have the value 1 or 2 as explained in the preceding section. In this case, the switching sequence can be given in the order of (POO)-(PON)-(OON)-(ONN) or (PPO)-(POO)-(PON)-(OON). The former sequence is the case that the index s has the value of 1, and the latter is the case that the index s has the value of 2. In Fig. 5(a), V^* is the original reference voltage vector and V_1^* is the corrected reference voltage vector when the index s has the value of 1. V_2^* is the corrected reference voltage vector when the index s has the value of 2. If the former switching sequence is selected and the load current flows out from dc-link capacitors, the load current will discharge the lower capacitor, while charging the upper capacitor of the dc-link. But on the contrary, if the latter switching sequence is selected, the upper capacitor is discharged and the lower capacitor is charged. So if the value of index s is changed depending on the voltage error and the direction of the power, the neutral-point potential is controlled. This is realized by simple procedure, subtracting or adding 1 from the value of s.

2) Method 2: Rearranging the Time Distribution of the Redundant Voltage Vectors

If the reference voltage vector stays at the region C in Fig. 5(b), the switching sequence is given as follows:

$$\begin{array}{ccccccc} (\mathrm{POO}) & - & (\mathrm{PNO}) & - & (\mathrm{PNN}) & - & (\mathrm{ONN}) \\ T_{1\mathrm{P}} & - & T_2 & - & T_3 & - & T_{1\mathrm{N}}. \end{array}$$

$T_{1\mathrm{P}}$, T_2, T_3, and $T_{1\mathrm{N}}$ are dwelling times of the corresponding voltage vectors.

In this case, the neutral-point voltage is controlled by adjusting the value of Tip and Tin in response to the voltage error and to the load conditions [5]. As the voltage vector (POO) and (OON) are same in magnitude and in phase, changing the dwelling times of the two vectors has

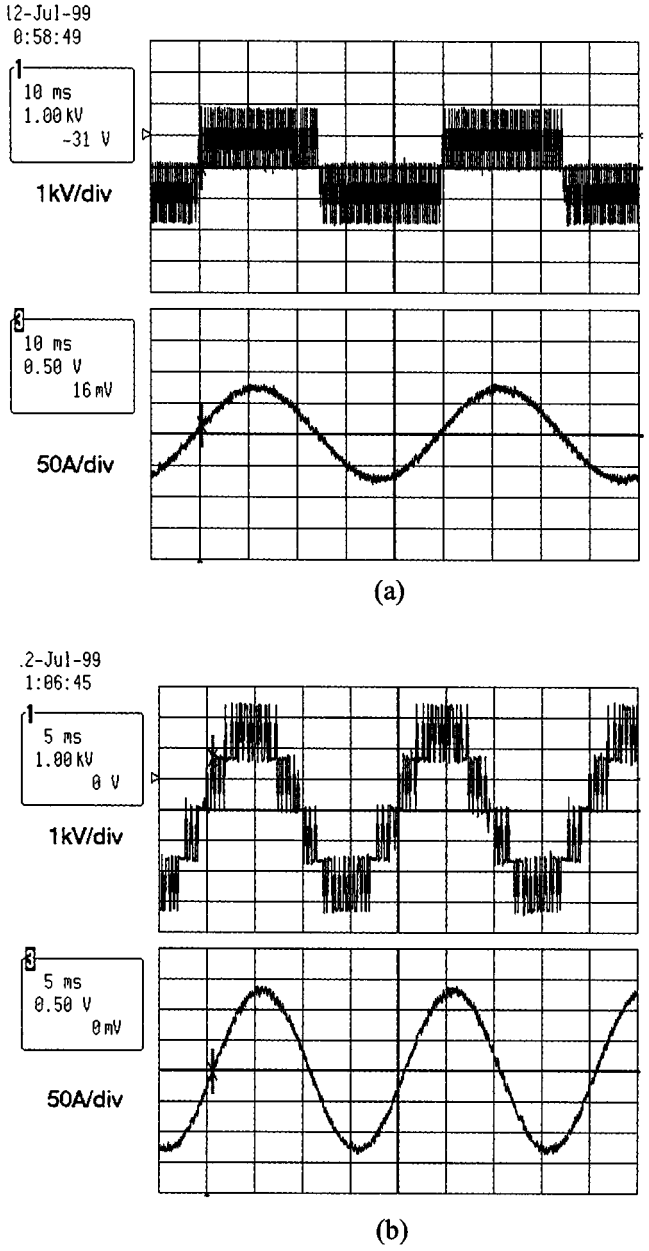

Fig. 8. Test results of the proposed SVPWM method with RL load. (a) line-to-line voltage and phase current at $f_0 = 20$ [Hz]; (b) line-to-line voltage and phase current at $f_0 = 50$ [Hz].

no effect on the output voltage vector only if the following equations are satisfied

$$T_{1n} + T_{1p} = T_1, \quad T_{1n} = T_1^* \frac{(1+f)}{2}$$
$$T_{1p} = T_1^* \frac{(1-f)}{2}, \quad [-1 \le f \le -1].$$

The underlined part of the sample program in Section II-C shows this process.

E. Application to the Multilevel SVPWM

The proposed SVPWM method is also applicable to the multi-level SVPWM above three-level. For example, the four or five-level space–vector diagram can be simplified to the three-level space–vector diagram on the same principles explained in this paper. Fig. 6 shows the case of four-level SVPWM. From Fig. 6, we can know that the space–vector diagram of a four-level inverter is composed of six three-level space–vector diagrams whose center vectors are shown as circles. If it is simplified to the three-level space–vector diagram, the remaining procedures for the SVPWM can be done like that of the proposed three-level SVPWM method.

III. Test Results

The proposed SVPWM method was programmed with the TMS320C31 DSP board and the 3300 V, 1200 A, EUPEC IGBT's are used to develop the three-level inverter. The inverter was designed for driving the 630 kW, 2500 V induction motor, but the 3300 V, 100 kW induction motor and RL load was used for the test.

The test results of the developed system are shown in Figs. 7 and 8. The waveforms shown in Fig. 7 are the test results of driving the 3300 V, 100 KW induction motor at 3600 V dc-link voltage. Fig. 8 shows test results when the RL is used as a load of inverter at 3250 V dc-link voltage. From the test results, we can know that the proposed SVPWM is good at pulse-width modulation of a three-level inverter and the voltage balance of the dc-link is controlled fairly well in the whole speed range of the motor, even though the proposed method is simple in its structure.

IV. Conclusion

In the field of high power, high performance applications, the three-level inverter seems to be the most promising alternative. In this paper, a new simplified space–vector PWM method for the three-level inverter is proposed and described in detail. The proposed SVPWM method has the following features.

1) The switching sequence is determined without a look-up table, so the memory of the controller can be saved.
2) The dwelling times of voltage vectors are calculated at the same manner as two-level SVPWM. Thus the proposed method reduces the execution time of the three-level SVPWM.
3) It is easy to implement the neutral-point potential control algorithm.
4) It can be applied to the multi-level SVPWM method above four-level.

The validity of the presented SVPWM method is verified by experimental results. The developed three-level IGBT inverter system was applied to the #2 steel making factory of Pohang Steel Corporation (POSCO).

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