TEXAS INSTRUMENTS

ADS125H02 ±20-V Input, 2-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADC With PGA and Voltage Reference

1 Features

- ±20-V input, 24-bit delta-sigma ADC
- Programmable data rate: 2.5 SPS to 40 kSPS
- High-voltage, high-impedance PGA:
  - Differential input range: up to ±20 V
  - Programmable gain: 0.125 to 128
  - Common-mode input voltage: up to ±15.5 V
  - Input impedance: 1 GΩ (minimum)
- High-performance ADC:
  - Input noise: 45 nV_{RMS} (20 SPS)
  - CMRR: 105 dB
  - Normal-mode rejection at 50 Hz, 60 Hz: 95 dB
  - Offset drift: 5 nV/°C
  - Gain drift: 1 ppm/°C
  - INL: 2 ppm
- Integrated features and diagnostics:
  - 2.5-V reference: 3 ppm/°C drift
  - Clock oscillator: 2.5% error (maximum)
  - Excitation current sources
  - GPIO to drive external mux
  - Signal and reference voltage monitors
  - Cyclic redundancy check (CRC)
- Power supplies:
  - AVDD: 4.75 V to 5.25 V
  - DVDD: 2.7 V to 5.25 V
  - HVDD: ±5 V to ±18 V
- Operating temperature: –40°C to +125°C
- 5-mm × 5-mm VQFN package

2 Applications

- PLC analog input modules:
  - Voltage (such as ±10 V or 0 V to 5 V)
  - Current (such as 4 mA to 20 mA with shunt)
  - Temperature (such as RTDs, thermocouples)
- Test and measurement:
  - High common-mode voltage inputs
  - Battery testing
  - High-side current measurement

3 Description

The ADS125H02 is a ±20-V input, 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADC features a low-noise programmable gain amplifier (PGA), an internal reference, clock oscillator, and signal or reference out-of-range monitors.

The integration of a wide input range, ±18-V PGA and an ADC into a single package reduces board area up to 50% compared to discrete solutions.

Programmable gain of 0.125 to 128 (corresponding to an equivalent input range from ±20 V to ±20 mV) eliminates the need for an external attenuator or external gain stages. 1-GΩ minimum input impedance reduces error caused by sensor loading. Additionally, the low noise and low drift performance allow direct connections to bridge, resistance temperature detector (RTD), and thermocouple sensors.

The digital filter attenuates 50-Hz and 60-Hz line cycle noise for data rates ≤ 50 SPS or 60 SPS to reduce measurement error. The filter also provides no-latency conversion data for high data throughput during channel sequencing.

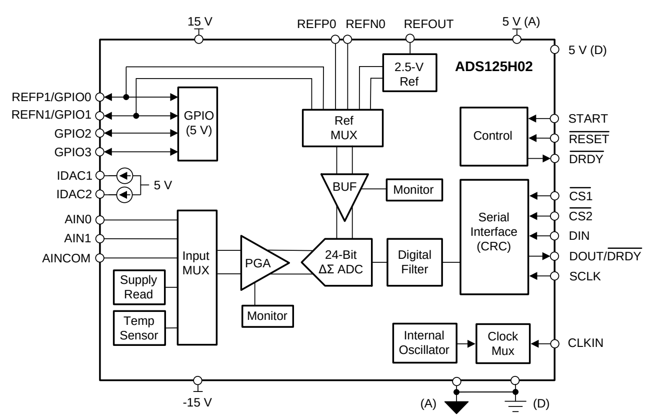
The ADS125H02 is housed in a 5-mm × 5-mm VQFN package and is fully specified over the –40°C to +125°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS125H02	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

TLV2186 Precision, Rail-to-Rail Input and Output, 24-V, Zero-Drift Operational Amplifier

1 Features

- High precision:
  - Offset drift: 0.1 µV/°C
  - Low offset voltage: 10 µV
- Low quiescent current: 90 µA
- Excellent dynamic performance:
  - Gain bandwidth: 750 kHz
  - Slew rate: 0.35 V/µs
- Robust design:
  - RFI/EMI filtered inputs
- Rail-to-rail input/output
- Supply range: 4.5 V to 24 V

2 Applications

- Precision high-side current sensing
- Bridge amplifier
- Strain gauge
- Temperature measurement
- Resistance temperature detector
- Weigh scale
- Thermal meter
- Power supply

3 Description

The TLV2186 is a low-power, 24-V, rail-to-rail input and output zero-drift operational amplifier (op amp). The TLV2186 features only 10 µV of offset voltage (typical) and 0.1 µV/°C of offset voltage drift over temperature (typical). This device is a great choice for precision instrumentation, signal measurement, and active filtering applications.

Low quiescent current consumption (90 µA) makes the TLV2186 an excellent option for power-sensitive applications, such as battery-powered instrumentation and portable systems.

Moreover, the high common-mode architecture along with low offset voltage allows for high-side current shunt monitoring at the positive rail. This device also provides robust ESD protection during shipment, handling, and assembly.

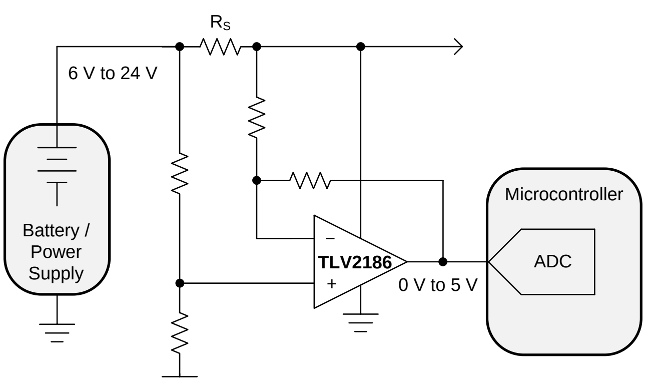
The device is specified for operation from –40°C to +125°C.

Device Information[(1)]

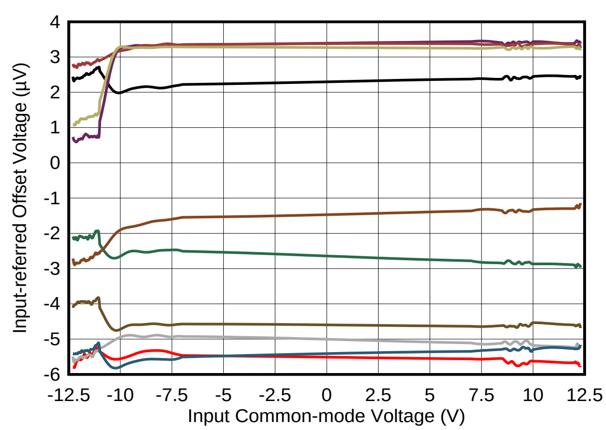
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV2186	SOIC (8)	4.90 mm × 3.90 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

High-Side Current Shunt Monitor Application



V_{OS} vs Input Common Mode Voltage



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

TLV320ADC5140 Quad-Channel, 768-kHz, Burr-Brown Audio ADC

Texas Instruments Burr-Brown Audio

ADVANCE INFORMATION

1 Features

- Multichannel high-performance ADC:
  - 4-channel analog microphones or line-in,
  - 8-channel digital PDM microphones, or
  - Combination of analog and digital microphones
- ADC line and microphone differential input performance:
  - Dynamic range (DR):
    - 120-dB, dynamic range enhancer (DRE) enabled
    - 108-dB, DRE disabled
  - THD+N: –95 dB
- ADC channel summing mode, DR performance:
  - 111-dB, DRE disabled, 2-channel summing
  - 114-dB, DRE disabled, 4-channel summing
- ADC input voltage:
  - Differential, 2-V_{RMS} full-scale inputs
  - Single-ended, 1-V_{RMS} full-scale inputs
- ADC sample rate (f_S) = 8 kHz to 768 kHz
- Programmable channel settings:
  - Channel gain: 0 dB to 42 dB, 1-dB steps
  - Digital volume control: –100 dB to 27 dB
  - Gain calibration with 0.1-dB resolution
  - Phase calibration with 163-ns resolution
- Programmable microphone bias or supply voltage generation
- Low-latency signal processing filter selection
- Programmable HPF and biquad digital filters
- Automatic gain controller (AGC)
- I^2C or SPI controls
- Integrated high-performance audio PLL
- Automatic clock divider setting configurations
- Audio serial data interface:
  - Format: TDM, I^2S, or left-justified (LJ)
  - Word length: 16 bits, 20 bits, 24 bits, or 32 bits
  - Master or slave interface
- Single-supply operation: 3.3 V or 1.8 V
- I/O-supply operation: 3.3 V or 1.8 V
- Power consumption for 1.8-V AVDD supply:
  - 8.7 mW/channel at 16-kHz sample rate
  - 9.5 mW/channel at 48-kHz sample rate

2 Applications

- Microphone array systems
- Voice-activated digital assistants
- Teleconferencing systems
- Security and surveillance systems

3 Description

The TLV320ADC5140 is a high-performance, Burr-Brown audio analog-to-digital converter (ADC) that supports simultaneous sampling of up to four analog channels or eight digital channels for the pulse density modulation (PDM) microphone input. The device supports line and microphone inputs, and allows for both single-ended and differential input configurations. The device integrates programable channel gain, digital volume control, a programmable microphone bias voltage, a phase-locked loop (PLL), a programmable high-pass filter (HPF), biquad filters, low-latency filter modes, and allows for sample rates up to 768 kHz. The device supports time-division multiplexing (TDM), I^2S, or left-justified (LJ) audio formats, and can be controlled with either the I^2C or SPI interface. These integrated high-performance features, along with the ability to be powered from a single-supply of 3.3 V or 1.8 V, make the device an excellent choice for space-constrained audio systems in far-field microphone recording applications.

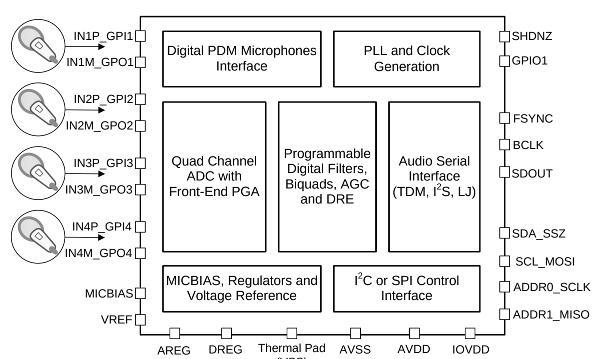
The TLV320ADC5140 is specified from –40°C to +125°C, and is offered in a 24-pin WQFN package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV320ADC5140	WQFN (24)	4.00 mm × 4.00 mm with 0.5-mm pitch

(1) For all available packages, see the package option addendum at the end of the data sheet.

Simplified Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for pre-production products; subject to change without notice.

采用超薄 **SOT** 封装的 **LM284x** 和 **LM284x-Q1 100**、**300** 或 **600mA**、**42V** 输入 降压直流/直流稳压器

1 特性

- LM2840-Q1、LM2841-Q1 和 LM2842-Q1 符合汽车 应用要求
- 具有符合 AEC-Q100 测试指导的以下结果：
  - 器件温度 1 级：-40°C 至 125°C 的环境工作温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
- 输入电压范围：4.5V 至 42V
- 100mA、300mA 和 600mA 的输出电流选项
- 0.765V 反馈引脚电压
- 550kHz (X) 或 1.25MHz (Y) 开关频率
- 低关断 I_Q：16µA（典型值）
- 短路保护
- 内部补偿
- 软启动电路
- 小型总体解决方案尺寸（SOT-6L 封装）
- 使用 LM2840 并借助 WEBENCH® 电源设计器创建定制设计方案
-

2 应用

- 电池供电类设备
- 工业分布式电源 应用
- 便携式媒体播放器
- 便携式手持仪器

3 说明

LM284x 和 LM284x-Q1 器件是 PWM 直流/直流降压稳压器。该器件具有 4.5V 至 42V 的输入范围，适合各种 应用（例如，从非稳压源进行电源调节）。它们具有低 R_{DSON}（典型值 0.9Ω）内部开关，可实现最大效率（典型值 85%）。此外，它们还具有 550kHz（X 选项）和 1.25MHz（Y 选项）的固定工作频率，可在保证低输出电压纹波的同时支持小型外部组件。可通过结合使用关断 ($\overline{SHDN}$) 引脚和外部 RC 电路来执行软启动，从而方便用户根据特定应用调整软启动时间。

经过优化后，LM2840 和 LM2840-Q1 的负载电流高达 100mA，LM2841 和 LM2841-Q1 的负载电流高达 300mA，而 LM2842 和 LM2842-Q1 的负载电流高达 600mA。它们都具有 0.765V 的标称反馈电压。

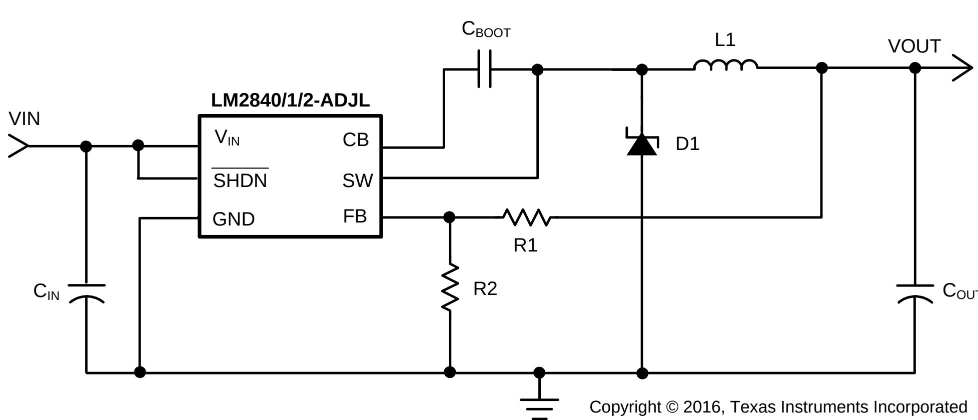
此器件还提供其他 功能， 例如热关断、V_{IN} 欠压锁定和栅极驱动欠压锁定。LM284x 和 LM284x-Q1 均采用低厚度 SOT-6L 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM2840、LM2840-Q1、LM2841、LM2841-Q1、LM2842、LM2842-Q1	SOT (6)	1.60mm x 2.90mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

典型应用电路



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (October 2015) to Revision F	Page
• Changed I_{POWER} from 1 mA to 10 mA in the *Absolute Maximum Ratings* table	4

Changes from Revision D (July 2015) to Revision E	Page
• 删除了 TPD1S514-3 的"预览"状态。	1
• Changed Max value of I_{VBUS_SLEEP} PARAMETER for TPD1S514-3 (Preview) from 308 µA to 335 µA.	5
• Updated TEST CONDITIONS for T_{OFF_DELAY} PARAMETER.	8

Changes from Revision C (July 2015) to Revision D	Page
• 已添加 TPD1S514 和 TPD1S514-3（预览）	1

Changes from Revision B (September 2014) to Revision C	Page
• 删除了已预览的 TPD1S514-3 和可编程 特性。	1

Changes from Revision A (July 2014) to Revision B	Page
• 已更改 更改了封装尺寸以修正舍入误差。	1

Changes from Original (April 2014) to Revision A	Page
• 删除了 TPD1S514-2 的"预览"状态。	1
• Updated Device Comparison table.	3
• Updated Electrical Characteristics OVP Circuit table.	7

Copyright © 2014–2019, Texas Instruments Incorporated

LM284x/LM284x-Q1 100/300/600mA、42V入力降圧型 DC/DCレギュレータ、薄型SOTパッケージ

1 特長

- LM2840-Q1、LM2841-Q1、LM2842-Q1は車載アプリケーションに認定済み
- 以下のAEC-Q100試験ガイダンス:
  - デバイス温度グレード 1:–40°C～125°C 周囲動作温度
  - デバイスHBM ESD分類レベル2
- 入力電圧範囲: 4.5V～42V
- 100mA、300mA、600mAの出力電流オプション
- 0.765Vのフィードバック・ピン電圧
- 550kHz (X)または1.25MHz (Y)のスイッチング周波数
- 低いシャットダウンI_Q: 16µA (標準値)
- 短絡保護
- 内部補償
- ソフトスタート回路
- ソリューション全体のサイズの小型化(SOT-6Lパッケージ)
- WEBENCH® Power Designerにより、LM2840を使用するカスタム設計を作成
-

2 アプリケーション

- バッテリ駆動の機器
- 産業用分散電源アプリケーション
- 携帯用メディア·プレーヤー
- 携帯用ハンドヘルド計測器

3 概要

LM284xおよびLM284x-Q1デバイスは、PWM DC/DCバック(降圧型)レギュレータです。4.5V～42Vの範囲の入力電圧で動作するため、レギュレートされていないソースからのパワー·コンディショニングなど、広範なアプリケーションに適しています。R_{DSON}の低い(標準値0.9Ω)内部スイッチにより、最高の効率を実現しています(標準値85%)。動作周波数は550kHz (Xオプション)および1.25MHz (Yオプション)に固定され、小型の外部部品を使用可能にしながら、低い出力電圧リップルを実現しています。シャットダウン(SHDN)ピンと外部のRC回路を使用してソフトスタートを実装できるため、ユーザーは特定のアプリケーションに応じてソフトスタート時間を変更できます。

LM2840およびLM2840-Q1は最大100mA、LM2841およびLM2841-Q1は最大300mA、LM2842およびLM2842-Q1は最大600mAの負荷電流に最適化されています。いずれのデバイスも、公称フィードバック電圧は0.765Vです。

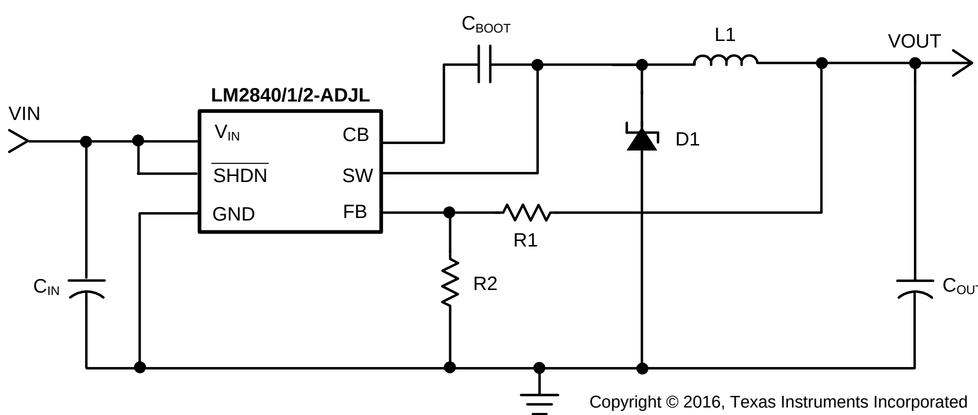
追加機能として、サーマル·シャットダウン、V_{IN}低電圧誤動作防止、ゲート·ドライブ低電圧誤動作防止が搭載されています。LM284xおよびLM284x-Q1は、低プロファイルのSOT-6Lパッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM2840、LM2840-Q1、LM2841、LM2841-Q1、LM2842、LM2842-Q1	SOT (6)	1.60mm×2.90mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーション回路



Copyright © 2016, Texas Instruments Incorporated

英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision I (September 2016) から Revision J に変更	**Page**
• Added this new text for Pin 4	3
• Added this new line of text in Shutdown Operation section	12

Revision H (April 2013) から Revision I に変更	**Page**
• 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加	1
• Added *Thermal Information* table	4

Revision G (April 2013) から Revision H に変更	**Page**
• ナショナル・セミコンダクターのデータシートのレイアウトをTIフォーマットへ 変更	1

Copyright © 2009–2017, Texas Instruments Incorporated

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2019) to Revision C — **Page**

- Deleted ADS125H01 from document 1
- Changed *Device Comparison Table* 3
- Added *Effective resolution* parameter to *Electrical Characteristics* table 7
- Added *Offset Voltage Long-Term Drift* curves to *Typical Characteristics* 15
- Added *Gain Long-Term Drift* curves to *Typical Characteristics* 16
- Added *Internal Reference Voltage Long-Term Drift* curve to *Typical Characteristics* 17
- Added *Oscillator Frequency Long-Term Drift* curve to *Typical Characteristics* 19
- Changed *Noise Performance* section 20
- Added effective resolution and noise-free resolution data in *Noise Performance* 23
- Changed sinc1, sinc3, sinc4, and sinc5 values and footnote in *Conversion Latency Time* table 40
- Changed start-conversion delay value from 0 µs to 50 µs in the *Start-Conversion Delay* section 40
- Changed sinc mode values in *Calibration Time* table 44
- Changed address 00h default value from xxh to 6xh in *Register Map Summary* table 53
- Changed reset value from xxh to 6xh in *Device Identification (ID) Register* 54

Changes from Revision A (January 2019) to Revision B — **Page**

- Changed status of ADS125H02 from Advance Information to Production Data 1

Copyright © 2018–2019, Texas Instruments Incorporated

Table of Contents

4 Revision History

DATE	REVISION	NOTES
July 2019	*	Initial release

Copyright © 2019, Texas Instruments Incorporated

TMS320F2838x Microcontrollers With Connectivity Manager

1 Features

- Dual-core C28x architecture
  - Two TMS320C28x 32-bit CPUs
    - 200 MHz
    - IEEE 754 double-precision (64-bit) Floating-Point Unit (FPU)
    - Trigonometric Math Unit (TMU)
    - CRC engine and instructions (VCRC)
    - Fast Integer Division (FINTDIV)
  - 512KB (256KW) of flash on each CPU (ECC-protected)
  - 44KB (22KW) of local RAM on each CPU
  - 128KB (64KW) of global RAM shared between the two CPUs (parity-protected)
- Two Control Law Accelerators (CLAs)
  - 200 MHz
  - IEEE 754 single-precision floating-point
  - Executes code independently of C28x CPU
- System peripherals
  - Two External Memory Interfaces (EMIFs) with ASRAM and SDRAM support
  - Two 6-channel Direct Memory Access (DMA) controllers
  - Up to 169 General-Purpose Input/Output (GPIO) pins with input filtering
  - Expanded Peripheral Interrupt controller (ePIE)
  - Low-power mode (LPM) support
  - Dual-zone security for third-party development
  - Unique Identification (UID) number
  - Embedded Real-time Analysis and Diagnostic (ERAD)
  - Background CRC (BGCRC)
- Connectivity Manager (CM)
  - Arm® Cortex®-M4 processor
  - 125 MHz
  - 512KB of flash (ECC-protected)
  - 96KB of RAM (ECC-protected or parity-protected)
  - Advanced Encryption Standard (AES) accelerator
  - Generic CRC (GCRC)
  - 32-channel Micro Direct Memory Access (µDMA) controller
  - Universal Asynchronous Receiver/Transmitter (CM-UART)
  - Inter-integrated Circuit (CM-I2C)
  - Synchronous Serial Interface (SSI)
  - 10/100 Ethernet 1588 MII/RMII
  - MCAN (CAN-FD)
- C28x communications peripherals
  - Fast Serial Interface (FSI) with two transmitters and eight receivers
  - Four high-speed (up to 50-MHz) SPI ports (pin-bootable)
  - Four Serial Communications Interfaces (SCI/UART) (pin-bootable)
  - Two I2C interfaces (pin-bootable)
  - Power-Management Bus (PMBus) interface
  - Two Multichannel Buffered Serial Ports (McBSPs)
- CM-C28x shared communications peripherals
  - EtherCAT® Slave Controller (ESC)
  - USB 2.0 (MAC + PHY)
  - Two Controller Area Network (CAN) modules (pin-bootable)
- Analog subsystem
  - Four Analog-to-Digital Converters (ADCs)
    - 16-bit mode
      - 1.1 MSPS each
      - 12 differential or 24 single-ended inputs
    - 12-bit mode
      - 3.5 MSPS each
      - 24 single-ended inputs
    - Single sample-and-hold (S/H) on each ADC
    - Hardware post-processing of conversions
  - Eight windowed comparators with 12-bit Digital-to-Analog Converter (DAC) references
  - Three 12-bit buffered DAC outputs
- Control peripherals
  - 32 Pulse Width Modulator (PWM) channels
    - High resolution on both A and B channels of 8 PWM modules (16 channels)
    - Dead-band support (on both standard and high resolution)
  - Seven Enhanced Capture (eCAP) modules
    - High-resolution Capture (HRCAP) available on two of the seven eCAP modules
  - Three Enhanced Quadrature Encoder Pulse (eQEP) modules
  - Eight Sigma-Delta Filter Module (SDFM) input channels, 2 independent filters per channel

ADVANCE INFORMATION

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for pre-production products; subject to change without notice.

- Configurable Logic Block (CLB)
  - Augments existing peripheral capability
  - Supports position manager solutions
- Clock and system control
  - Two internal zero-pin 10-MHz oscillators
  - On-chip crystal oscillator
  - Windowed watchdog timer module
  - Missing clock detection circuitry
  - Dual-clock Comparator (DCC)
- 1.2-V core, 3.3-V I/O design
- Package options:
  - Lead-free, green packaging
  - 337-ball New Fine Pitch Ball Grid Array (nFBGA) [ZWT suffix]
- Temperature options:
  - S: –40ºC to 125ºC junction
  - Q: –40ºC to 125ºC ambient (AEC Q100 qualification for automotive applications)

2 Applications

- Advanced Driver Assistance Systems (ADAS)
- Building automation
- Electric Vehicle/Hybrid Electric Vehicle (EV/HEV) powertrain
- Factory automation
- Grid infrastructure
- Industrial transport
- Medical, healthcare, and fitness
- Motor drives
- Power delivery
- Telecom infrastructure
- Test and measurement

3 Description

C2000™ 32-bit microcontrollers are optimized for processing, sensing, and actuation to improve closed-loop performance in real-time control applications such as industrial motor drives; solar inverters and digital power; electrical vehicles and transportation; motor control; and sensing and signal processing.

The TMS320F2838x is a powerful 32-bit floating-point microcontroller unit (MCU) designed for advanced closed-loop control applications. The F2838x supports a dual-core C28x architecture along with a new Connectivity Manager that offloads critical communication tasks, significantly boosting system performance. The integrated analog and control peripherals with advanced connectivity peripherals like EtherCAT and Ethernet also let designers consolidate real-time control and real-time communications architectures, reducing requirements for multicontroller systems.

The dual real-time control subsystems are based on TI's 32-bit C28x floating-point CPUs, which provide 200 MHz of signal processing performance in each core. The C28x CPUs are further boosted by the TMU accelerator, which enables fast execution of algorithms with trigonometric operations common in transforms and torque loop calculations.

The F2838x microcontroller family features two CLA real-time control coprocessors. The CLA is an independent 32-bit floating-point processor that runs at the same speed as the main CPU. The CLA responds to peripheral triggers and executes code concurrently with the main C28x CPU. This parallel processing capability can effectively double the computational performance of a real-time control system. By using the CLA to service time-critical functions, the main C28x CPU is free to perform other tasks, such as communications and diagnostics. The dual C28x+CLA architecture enables intelligent partitioning between various system tasks. For example, one C28x+CLA core can be used to track speed and position, while the other C28x+CLA core can be used to control torque and current loops.

The Connectivity Manager subsystem is based on the Cortex-M4 CPU and has access to advanced communication IPs like EtherCAT, Ethernet, MCAN (CAN-FD), and AES.

The TMS320F2838x supports up to 1.5MB (512KB per CPU) of flash memory with error correction code (ECC) and up to 312KB (216KB total for C28x CPU1 and CPU2, and 96KB on the Cortex-M4) of SRAM. Two 128-bit secure zones are also available on the device for code protection.

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

Migrating From MSP430F541x and MSP430F543x MCUs to MSP430F541xA and MSP430F543xA MCUs

Miguel Morales — *MSP430 Applications*

ABSTRACT

This application report helps you migrate an application based on an MSP430F541x or MSP430F543x microcontroller (MCU) to an MSP430F541xA or MSP430F543xA MCU. This application report describes the main differences between the two device families and provides migration solutions for both software and hardware.

Contents

List of Figures

List of Tables

Trademarks

MSP430 is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

Copyright © 2009–2019, Texas Instruments Incorporated

Application Report

Migrating From MSP430F541x and MSP430F543x MCUs to MSP430F541xA and MSP430F543xA MCUs

Miguel Morales *MSP430 Applications*

ABSTRACT

This application report helps you migrate an application based on an MSP430F541x or MSP430F543x microcontroller (MCU) to an MSP430F541xA or MSP430F543xA MCU. This application report describes the main differences between the two device families and provides migration solutions for both software and hardware.

Contents

List of Figures

List of Tables

Trademarks

MSP430 is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

Copyright © 2009–2019, Texas Instruments Incorporated

Design Guide: TIDEP-01017
Cascade Imaging Radar Capture Reference Design Using Jacinto™ ADAS Processor

TEXAS INSTRUMENTS

Description

This reference design provides a processing foundation for a cascaded imaging radar system. Cascade radar devices can support front, long-range (LRR) beam-forming applications as well as corner- and side-cascade radar and sensor fusion systems.

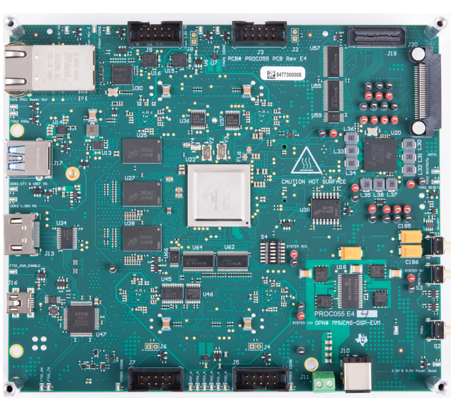
This reference design provides qualified developers the design materials to create a functioning software evaluation platform for developing and testing ADAS applications. The design shortens the development time of a base platform supporting multiple automotive radar front end and antenna subsystems.

Resources

TIDEP-01017	Design Folder
TDA2SX	Product Folder
VisionSDK	Tool Folder
TIDEP-01012	Design Folder

TI E2E™ Community

ASK Our E2E™ Experts

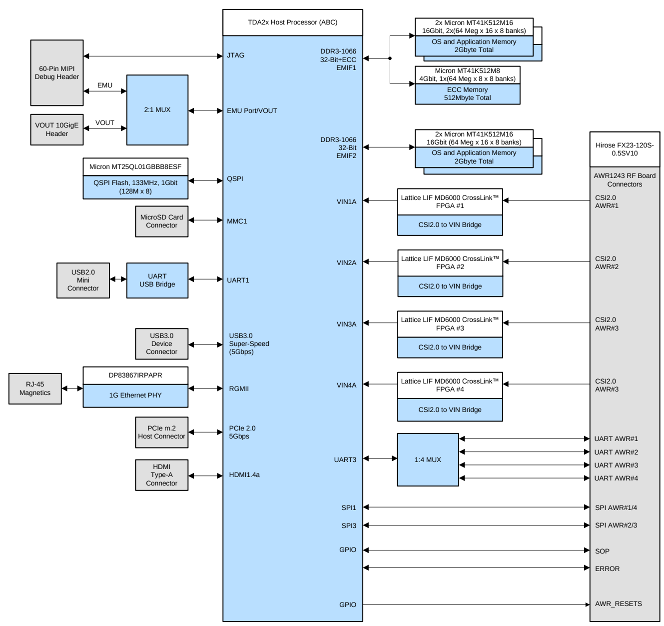


Features

- Compatible with SVTronics AWRx CIR radar antenna reference design
- 4 × Lattice CrossLink™ FPGA-based interfaces (1 each, per AWRx)
- High-performance TDA2x device with 4 radar processing SIMD accelerators (1 EVE per AWRx)
- Ethernet and PCIe connectivity for control and data respectively

Applications

- Long-range radar
- Imaging radar
- Drive assist ECU
- Radar ECU
- Medium and short range radar
- ADAS domain controller



An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

Copyright © 2019, Texas Instruments Incorporated

1 System Description

Autonomous control of a vehicle provides quality-of-life and safety benefits in addition to making the relatively mundane act of driving safer and less difficult. The quality-of-life features include the ability of a vehicle to park itself, or to determine whether a lane change is possible, and provide features like automatic cruise control—where a vehicle maintains a constant distance with respect to the car ahead of it, essentially, tracking the velocity of the car in front of it. Autonomous braking and collision avoidance are safety features that prevent accidents caused by driver inattention. These features work by observing the area in front of a car and alerting the ADAS subsystems if obstacles are observed that are likely to hit the car. Implementing these technologies requires a variety of sensors to detect obstacles in the environment and track their velocities and positions over time.

1.1 Key System Specifications

This reference design has two sets of specifications because the radar is used as a multi-mode radar. MIMO is the first specification. TX beamforming (TXBF) is the second specification,

Table 1. Key System Specifications

RECOMMENDED OPERATING CONDITIONS	MIN	TYP	MAX
Input voltage (V_{IN})	6 V	12 V	24 V

1.2 Why Cascade Radar?

Frequency-modulated continuous-wave (FMCW) radars allow the accurate measurement of range and relative velocity of obstacles and other vehicles; therefore, radars are useful for autonomous vehicular applications (such as parking assist and lane change assist) and car safety applications (autonomous breaking and collision avoidance). An important advantage of radars over camera and light-detection-and-ranging (LIDAR)-based systems is that radars are relatively immune to environmental conditions (such as the effects of rain, dust, and smoke). FMCW radars can work in complete darkness and also bright daylight (radars are not affected by glare) because they transmit and receive electromagnetic waves. When compared with ultrasound, radars typically have a much longer range and much faster time of transit for their signals.

Despite the many advantages of radar technology, in many cases, automotive manufacturers today still use camera sensors as the primary sensor technology used to make final safety decisions in the system.

The radar sensor is being used as the secondary sensor; meaning, the vehicle system receives the Radar warning, but decides to take an action only upon the camera sensor verification. The main reason is limitation in radar angular resolution. The radar sensors deployed today in most vehicles lack the ability to distinguish between static objects with the same range and same relative velocity.

Today, a typical front radar sensor has about a 5-degree angular resolution that corresponds to the ability of the sensor to distinguish between objects that are 8.5 m apart at 100 m. Objects that are closer than 8.5 m appear as one object. For example, a vehicle stopped in the right lane, might look like a shoulder road street lamp for example, and therefore would be ignored by the safety system.

This is about to change with the introduction of the Imaging Radar solution from Texas Instruments (TI).

The TI Imaging Radar is a four-chip cascade solution, that acts like a single-chip sensor but achieves 20Log10(N_{TX}) SNR gain in TX beamforming mode and 360/(N*pi) angular resolution (N is the number of virtual antennas in a MIMO configuration).

The TI Imaging Radar solution, we can distinguish between static objects 0.6 degrees apart with all antennae placed in single dimension linearly, and reach a 350-m object detecting range(angular resolution is dependent on the antenna configuration and the number of TX/RX antennae).

This performance enables TI Imaging Radar to become the primary sensor in the vehicle and enhance safety across weather and visibility conditions by providing a high-resolution image for both static and moving objects.

Copyright © 2019, Texas Instruments Incorporated

Tech Note
Voltage Reference Solutions in Motor Drives

Introduction

Motor drives have a critical need for a precision signal chain to measure motor speed, position, torque, and power rails for high performance system robustness and efficiency. This applies to all motor systems such as servo drives, AC Inverter and speed-controlled BLDC drives as they all share common subsystems such as *Voltage/Current Sensing*,*SIN/COS AFE*, and *Analog I/OExternal Voltage References* are able to help maximize the resolution and accuracy of the analog signal chain, which optimize the drive performance and efficiency.

Motor Drive Basics

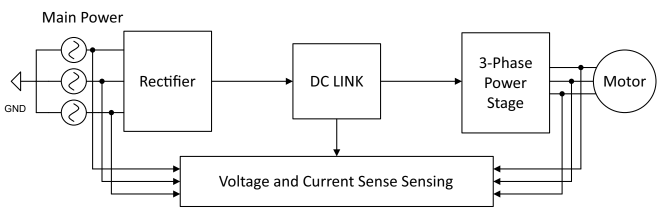


Figure 1. Motor Power Stage Example

All motor drives require a motor power stage to provide power and control the motor but they can be inefficient due to its high power consumption. There is a need for lower power consumption that is partially driven by government regulations such as EN 50598 which call for higher power efficiency of variance speed drives which include its power stage. The power stage typically convert a fixed frequency AC input into a variable frequency 3-phase AC output as shown in Figure 1 but due to motor reliability and high power requirements, this stage requires constant sensing.

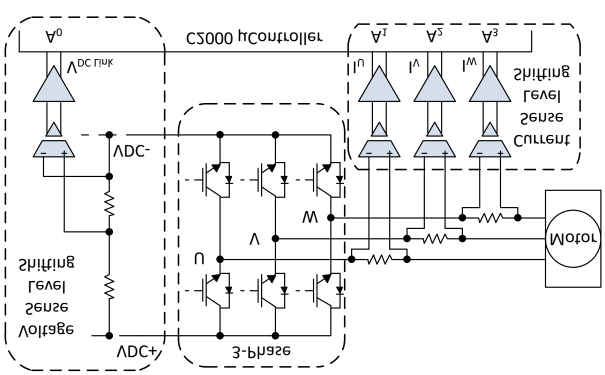


Figure 2. Voltage and Current Sense Example Use Case

There are two common ways of measuring voltage and current in motor power stage and they both involve an isolated amplifier as shown in Figure 2. For voltage measurements, there is a resistor divider that is connected to an isolated amplifier and for current measurements there is typically an inline resistor in each of the 3 phases isolated amplifier. The isolated amplifier is used because it enables the rejection of large common-mode voltages and transients and it is also a requirement of safety standard *IEC 61800-5-1* . The use of a isolated amplifier is typically required to be level shifted and scaled to the input of the ADC.

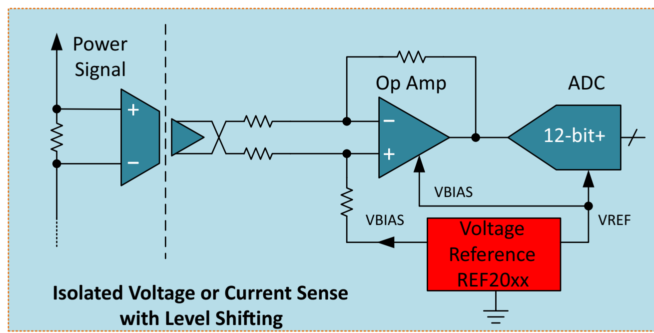


Figure 3. Level Shifting with Voltage Reference

TIDA-00366 is a design that focuses on high-bandwidth phase current and voltage measurements in 3-phase motor power drives. In this design the required voltage sense accuracy is 1% and current sense accuracy is 0.5% across temperature. This design uses the REF2033, a 8 ppm/°C low temperature drift series voltage reference, is used to provide a high precision voltage that is used for level shifting from the isolated amplifier for the internal C2000 ADC. This is because the low 8 ppm/°C in the wide industrial temperature range will only contribute a temperature offset of 0.1%. For example, a higher temperature coefficient of 50ppm/C would have a variation of 0.8% across temperature, which is outside the specification.

Motor Feedback

One of the most important features of a high-performance motor control drive is how the system handles the control loop feedback of the speed or position sensors. Motor control feedback is a feature common in synchronous servo motors and in high end AC/VFD motors. The two traditional ways of measuring motor speed are done with either a resolver or an encoder. For example, in a resolver the sine (SIN) and cosine (COS) signals are induced through

Copyright © 2019, Texas Instruments Incorporated

the resolver excitation windings and are used to calculate the angular speed of the motor. the other hand, an encoder will add sensors on the motor to read either SIN/COS signals or quadrature signals to calculate the angular speed.

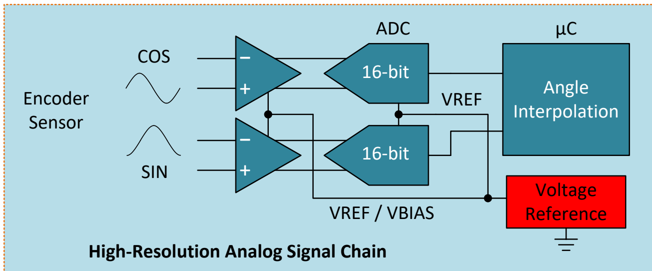


Figure 4. Encoder Sensing Circuits

The benefit of encoders over resolvers is that they can achieve higher accuracy but at the cost of an increase in system complexity. It is common to see motors with only digital or analog encoders such as in Figure 4 but a combination of both can yield a much more accurate system. For example, in TIDA-00176, the encoder sensor signal chain is a combination of comparators and a ADS8354 ADC that sample the SIN/COS signals to produce a high resolution interpolated position. In this design the REF2033 is used to provide the same voltage reference for both the SIN and COS channels because the gain drift of the reference cancels out due to the operation of SIN/COS. The critical component of a voltage reference is going to be its effect on the SIN/COS offset and offset drift, for more information see TIDA-00176 section 1.4.1. Additionally, the TIDA-00316 shows how to interface with hall sensors such as the ones used in encoders. In this design the REF2033 and REF2025 are used to create a high accuracy reference for level shifting for hall sensors to guarantee an accuracy of 0.5% across temperature. More details on resolvers and encoders can be found *in this white paper*.

There is a need for a high precision on the voltage reference due to the gain and quantization error that can cause the ADC to increase the phase error. The gain error is affected by parameters such as initial accuracy, temperature drift, and long term drift such as in the Equation 1. In table 7 of TIDA-00176, a gain error of 0.1% will translate to a phase error of 0.15° and this is the combination of the gain error of the voltage reference and ADC such as in equation. It is common to have initial calibration and routine calibration to keep the phase error low as even the temperature drift, as shown in Table 1, can significantly affect the gain error..

$$\text{Gain Error}_{\text{VREF}}\big|_{\text{Total}} = \sqrt{(\text{Accuracy})^2 + (\text{TempCo})^2 + (\text{TempHyst})^2 + (\text{Long Term Drift})^2 + (1/f\ \text{Noise})^2} \quad (1)$$

$$\text{Gain Error}_{\text{VREF+ADC}}\big|_{\text{Total}} = \sqrt{\left(\text{Gain Error}_{\text{VREF@AIN}}\big|_{\text{Total}}\right)^2 + \left(\text{Error}_{\text{ADC}}\big|_{\text{Total}}\right)^2} \quad (2)$$

Table 1. External Voltage Device Recommendations for Resolvers and Encoders

Temp Co (ppm/°C)	Gain Error (-40°C to 85°C)	Gain Error (-40°C to125°C)
1	0.0125%	0.0165%
5	0.0625%	0.0825%
10	0.125%	0.165%
50	0.625%	0.825%

Analog I/O

Another area in motor drives that require high accuracy is the analog I/O module which is commonly used to communicate between the motor control board with the motor control drive. Common analog I/Os are ±10V analog signals or 4-20mA current signals. Typically the communication has to be very robust and accurate across temperature. Since most systems are very customizable, the analog I/O is often discrete. External voltage references can be used in a variety of ways such as level shifting, VREF for an ADC/DAC, and provide a precision power source.

The most common way to increase the accuracy of a motor drive is to use a precision voltage references in the ADC of the 4-20mA receiver or DAC of the 4-20mA transmitter. This is common when using the C2000 integrated ADCs to sample the input signal. In this case, it is common to use a REF3030 to provide the input VREF for the C2000 processor as it is often a 12-Bit multichannel SAR ADC. The resolution for the ADC signal chain in analog I/O commonly go up to 16-Bit through external ADCs and at this ADC resolution there is always a need for a precision voltage reference. Common ADCs that are used in Analog I/O are the ADS8688 and the external voltage reference pairings for this ADC are the REF3440 and REF3140. Both the REF3440 and REF3140 provide very low noise inputs to the ADC which can allow for a greater effective resolution. But the REF3440 is a higher performance voltage reference compared to the REF3140 and the higher performance is often chosen to make the calibration process easier and to maximize the accuracy of the ADC. An comparison table for series voltage references is shown in Table 2.

Table 2. External Voltage Device Recommendations for Motor Drives

DEVICE	INITIAL ACCURACY	TEMPERATURE DRIFT
REF3030	0.2%	75 ppm/°C
REF3140	0.2%	15 ppm/°C
REF2033	0.05%	8 ppm/°C
REF3440	0.05%	6 ppm/°C

Copyright © 2019, Texas Instruments Incorporated

TI Confidential — NDA Restrictions

AM65x/DRA80xM Processors

Texas Instruments Family of Products

Technical Reference Manual

Literature Number: SPRUIE8D
April 2018–Revised June 2019

Texas Instruments

Contents

Copyright © 2018–2019, Texas Instruments Incorporated

List of Figures

List of Tables

Copyright © 2018–2019, Texas Instruments Incorporated

Preface

SPRUIE8D–April 2018–Revised June 2019

Read This First

About This Manual

This Technical Reference Manual (TRM) details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the device.

Related Documentation From Texas Instruments

For a complete listing of related documentation and development-support tools for the device, visit the Texas Instruments website at www.ti.com.

Copyright © 2018–2019, Texas Instruments Incorporated

Chapter 3

SPRUIE8D–April 2018–Revised June 2019

System Interconnect

The following sections describe the device system interconnect.

Topic **Page**

Copyright © 2018–2019, Texas Instruments Incorporated

Frequently Asked Questions and Known Issues

This appendix presents solutions to frequently asked questions regarding the MSP-FET430 hardware.

Topic **Page**

Copyright © 2009–2018, Texas Instruments Incorporated