NWEN242 Homework Assignment 4

Due date: Thursday 08 October at 23:59

Total marks: 23

Q1 [3 marks] In this exercise we look at memory locality properties. The following code is written in C, where elements within the same row are stored contiguously. Assume each word is a 32-bit integer.

```
for (I=0; I<8; I++)
     for (J=0; J<8000; J++)
          A[I][J]=B[I][0]+A[J][I];
```

a) [1 mark] How many 32-bit integers can be stored in a 16-byte cache block?

b) [1 mark] References to which variables exhibit temporal locality?

c) [1 mark] References to which variables exhibit spatial locality?

Q2 [2 marks] Caches are important to providing a high-performance memory hierarchy to processors. Below is a list of 32-bit memory address references, given as word addresses.

3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253

a) [2 marks] For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. (Use the table below to fill in your answers. Use decimal notation for the Tag and Index fields.)

Word Address	Binary Address	Tag	Index	Hit/Miss
3		(use decimal notation)	(use decimal notation)	
180				
43				
2				
191				
88				
190				
14				
181				
44				
186				
253				

b) [2 marks] For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with two-word blocks and a total size of 8 blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. (Use decimal notation for the Tag and Index fields.)

c) [5 marks] You are asked to optimize a cache design for the given references. There are three direct-mapped cache designs possible, all with a total of 8 words of data: C1 has 1-word blocks, C2 has 2-word blocks, and C3 has 4-word blocks. In terms of miss rate, which cache design is the best? If the miss stall time is 25 cycles, and C1 has an access time of 2 cycles, C2 takes 3 cycles, and C3 takes 5 cycles, which is the best cache design? (Hint: fill in the table below and figure out the miss rate, and then use access time and miss stall time to find out how many cycles are needed for referencing the 12 word addresses. Use decimal notation for the Tag and Index fields.)

			Cache1		Cache2		Cache3	
Word Address	Binary Address	Tag	Index	Hit/Miss	Index	Hit/Miss	Index	Hit/Miss
3								
180								
43								
2								
191								
88								
190								
14								
181								
44								
186								
253								

d) [2 marks] Below are listed parameters for a given direct-mapped cache.

Cache Data Size: 32 KiB
Cache Block Size: 2 words

Calculate the total number of bytes required for the cache listed above, assuming a 32-bit address.

Q3 [3 marks] For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-5	4-0

a) [1 mark] What is the cache block size (in words)?

b) [1 mark] How many entries does the cache have?

c) [1 mark] What is the ratio between total bits required for such a cache implementation over the data storage bits?

Q4 [3 marks] In this exercise, we will look at how multilevel caches affect cache performance. Assume that main memory accesses take 70 ns. The following table shows data for L1 caches attached to each of two processors, P1 and P2.

	L1 Miss Rate	L1 Hit Time
P1	8.0%	0.66 ns
P2	6.0%	0.90 ns

a) [1 mark] What is the Average Memory Access Time (AMAT) for P1 and P2?

b) [1 mark] Assume that L2 cache is added to P1 with the following parameters.

	L2 Miss Rate	L2 Hit Time
P1	95%	5.62 ns

What is the Average Memory Access Time (AMAT) for P1?

c) [1 mark] For P1 (with L2 cache) to achieve an AMAT of 5.31 ns, what would be the required miss rate for the L2 cache?

Q5 [3 marks] This exercise examines the impact of different cache designs, specifically comparing associative caches to the direct-mapped caches. The sequence of references is shown in the table below. Work out the final cache contents for a three-way set associative cache with two-word blocks and a total size of 24 blocks by filling in the table below. (Use LRU replacement. For Block/Way fields, use `T(index) = tag` notation- this locates the block for the desired data.)

Word Address	Binary Address	Tag	Index	Hit/Miss	Block0 / Way0	Block1 / Way1	Block2 / Way2
3							
180							
2							
191							
14							
31							
190							
158							