NWEN242 homework assignment 2

Due date: **Thursday 20 August at 23:59**

Total marks: 26

Question 1: Suppose the program counter (PC) is set to 0x2000 0000.

Is it possible to use the jump (j) MIPS assembly instruction to set the PC to the address as 0x4000 0000? [**1 Mark**]

Is it possible to use the branch-on-equal (beq) MIPS assembly instruction to set the PC to this same address (i.e. 0x4000 0000)? [**1 Mark**]

Question 2: Translate the following C code to MIPS assembly code. Assume that the values of a, b, i, and j are in registers $s0, $s1, $t0, and $t1, respectively. Also, assume that register $s2 holds the base address of the array D. [**6 Marks**]

```
for(i=0; i<a; i++)
    for(j=0; j<b; j++)
        D[4*j] = i + j;
```

Question 3: Translate function f into MIPS assembly language. Assume the function declaration for func is "int func(int a, int b);". The code for function f is as follows: [**6 Marks**]

```
int f(int a, int b, int c, int d){
   return a+func(a,c);
}
```

Question 4: Consider the following code:

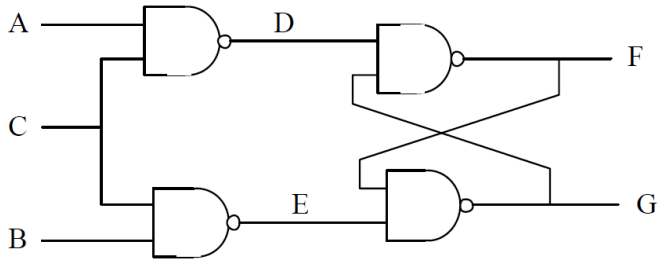
```
lbu $t0, 0($t1)
sb $t0, 0($t2)
```

Assume that the register $t1 contains the address 0x10000000 and the register $t2 contains the address 0x10000010. Note the MIPS architecture utilizes big-endian addressing. Assume that the word (in hexadecimal) stored originally at address 0x10000000 is: 0x11223344. After executing the two instructions above, what is the resulting word stored at address 0x10000000? [**2 Marks**]

Question 5: Construct the truth table for a four-input odd-parity function. An odd-parity function produces a parity bit that is set to one if there is an odd number of one bits in the inputs. The parity bit is set to zero otherwise. [**4 Marks**]

Question 6: Implement the four-input odd-parity function with AND, OR, and Inverse gates. Drawing the logic block diagram is optional. All you need is to give the Boolean expression in the Disjunctive Normal Form for your implementation. [**2 Marks**]

Question 7: Given the design of the sequential logic block below



Assuming that F is asserted and G is deasserted initially, draw the timing diagram for F [**2 Marks**] and G [**2 Marks**] with respect to the timing diagram of A, B, and C below.