

WP4 update - Analytical model demonstration

22nd March 2024



Naïve sequential BFS algorithm

```
1 void bfs(int *level, int *parent, std::vector<float> *G, int src, int
      num_nodes)
       for (int i = 0; i < num\_nodes; ++i)
 ^{2}
 ^{3}
           level[i] = -1;
           parent [i] = -1;
 4
 5
 6
       std::queue<int> queue;
 8
       level[src] = 0;
       queue.push(src);
 9
10
11
       while (!queue.empty())
12
           int u = queue.front();
13
           queue.pop();
14
           for (int v = 0; v < num\_nodes; ++v)
15
               if (G[u][v] > 0 \&\& level[v] = -1)
16
                    parent[v] = u;
17
18
                    level[v] = level[u] + 1;
19
                    queue.push(v);
```



Assumptions

- Graph only has a single connected component
- Write back cache
 - Memory write takes the same time as memory read



```
T_{BFS} = nT_{init}

T_{init} = 2T_{mem\_write}
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              if (G[u][v] > 0 && level[v] = -1)
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T_{BFS} = nT_{init} + nT_{while\_loop}
T_{init} = 2T_{mem\_write}
T_{while\_loop} = T_{q\_front} + T_{q\_pop} + n \left( T_{add} + T_{G\_mem\_read} + T_{mem\_read} \right)
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      num_nodes)
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```
T_{BFS} = nT_{init} + nT_{while\_loop} + nT_{visit\_node}
T_{init} = 2T_{mem\_write}
T_{while\_loop} = T_{q\_front} + T_{q\_pop} + n\left(T_{add} + T_{G\_mem\_read} + T_{mem\_read}\right)
T_{visit\_node} = 2T_{DRAM} + T_{L1} + T_{add} + T_{q\_push}
```

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```
T_{RFS} = nT_{init} + nT_{while\ loop} + nT_{visit\ node}
            T_{init} = 2T_{mem\_write}
     T_{while\_loop} = T_{a\_front} + T_{a\_pop} + n \left( T_{add} + T_{G\_mem\_read} + T_{mem\_read} \right)
     T_{visit\ node} = 2T_{DRAM} + T_{L1} + T_{add} + T_{a\ nush}
    T_{mem\ write} = T_{mem\ read} = (1 - MR_{L1})T_{L1} + MR_{L1}(1 - MR_{L2})T_{L2} +
                  MR_{L1}MR_{L2}(1-MR_{L3})T_{L3} + MR_{L1}MR_{L2}MR_{L3}T_{DRAM}
   MR_{L\{1,2,3\}} = \frac{1}{cacheLineSize_{L\{x\}}/sizeof(\texttt{int})}
   T_{G\ mem\ read} = (1 - G_{-}MR_{L1})T_{L1} + G_{-}MR_{L1}(1 - G_{-}MR_{L2})T_{L2} +
                  G_{-}MR_{L1}G_{-}MR_{L2}(1-G_{-}MR_{L3})T_{L3}+
                  G_{-}MR_{L1}G_{-}MR_{L2}G_{-}MR_{L3}T_{DRAM}
G\_MR_{L\{1,2,3\}} = \frac{1}{cacheLineSize_{L\{x\}}/sizeof(\mathtt{float})}
```

```
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- Cache line sizes are 64 bytes for L1, L2, and L3
- Memory latency (measured by using LMBench lat mem rd):

Memory level	latency (ns)
L1	1.26
L2	4.42
L3	20.9
DRAM	62.5

Table 1: Observed memory latency times



- Cache line sizes are 64 bytes for L1, L2, and L3
- Memory latency (measured by using LMBench lat mem rd):

Memory level	latency (ns)
L1	1.26
L2	4.42
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DRAM	62.5

Table 1: Observed memory latency times
$$MR_{L\{1,2,3\}} = G_{-}MR_{L\{1,2,3\}} = \frac{1}{64/4} = \frac{1}{16}$$

$$T_{mem_write} = T_{mem_read} = T_{G_mem_read}$$

$$= \frac{15}{16}1.26 + \frac{1}{16}\frac{15}{16}4.24 + \frac{1}{16}\frac{1}{16}\frac{15}{16}20.9 + \frac{1}{16}\frac{1}{16}\frac{1}{16}62.5$$

$$= 1.521484375$$

Operation latencies (measured by microbenchmarking):

Operation	latency (ns)
queue push	16.1
queue front	14.5
queue pop	11.2
integer add	0.326

Table 2: Observed operation latency times



• The final model:

$$T_{BFS} = nT_{init} + nT_{while_loop} + nT_{visit_node}$$

$$T_{init} = 2 \cdot 1.521484375$$

$$T_{while_loop} = 14.5 + 11.2 + n (0.326 + 1.521484375 + 1.521484375)$$

$$T_{visit_node} = 2 \cdot 62.5 + 1.26 + 0.326 + 16.1$$

$$T_{BFS} = n(2 \cdot 1.521484375 + 14.5 + 11.2 + n (0.326 + 1.521484375 + 1.521484375) + 2 \cdot 62.5 + 1.26 + 0.326 + 16.1) = 171.429n + 3.36897n^2$$

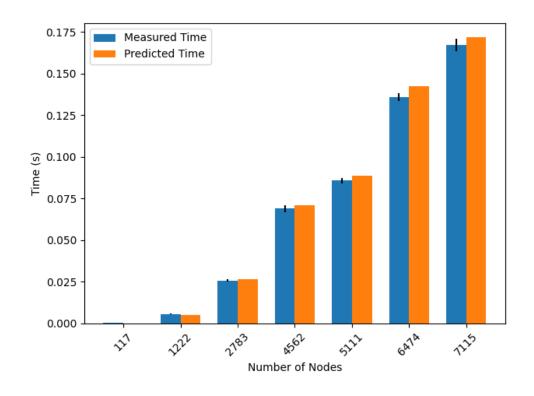


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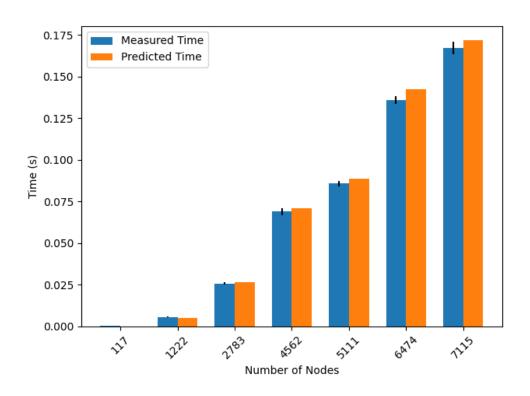
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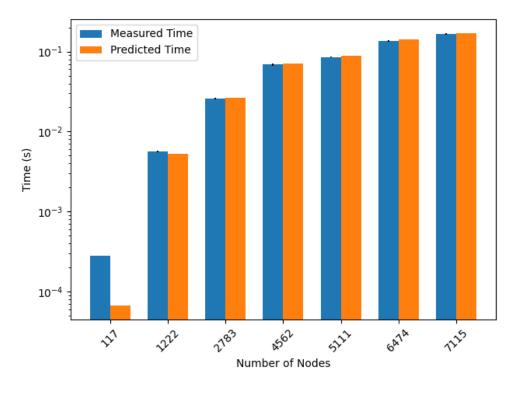
$$T_{BFS} = n(2 \cdot 1.521484375 + 14.5 + 11.2 + n (0.326 + 1.521484375 + 1.521484375) + 2 \cdot 62.5 + 1.26 + 0.326 + 16.1) = 171.429n + 3.36897n^{2}$$













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