H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters

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H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters

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***Abstract* — This paper presents an H-bridge class-D power amplifier for digital pulse modulation transmitters. For the proposed class-D amplifier, the drivers of the pull-up and pull-down devices were separated to minimize power loss associated with the shoot-through currents. The amplifier can be driven by binary digital signals generated by a delta-sigma modulator directly. The H-bridge class-D power amplifier system was tested with CDMA IS-95 signals at 800MHz. The drain efficiency of 31% was achieved with output power of 15 dBm and an ACPR of -43 dBc.**

***Index Terms* — class-D, delta-sigma, CDMA, power amplifiers.**

I. Introduction

With the rapid advance of CMOS technology, digital signal processing (DSP) techniques can be used at clock frequencies reaching into the microwave region. This permits the implementation of digital RF systems, implementing functions up to now in the domain of analog circuits.

In digital RF transmitters, signal processing such as base-band signal generation, filtering, and frequency conversion are completed in the digital domain. This digital approach increases the flexibility and programmability of the system, as well as avoiding the problems of aging, variable component values and interconnects difficulties associated with many analog circuits. Fig. 1 shows a possible architecture of digital pulse modulation transmitters [1]. Via DSP techniques, the modulated baseband signals are generated, up-converted, and sent to a band-pass delta-sigma modulator (BPDSM). The BPDSM quantizes the signals into a binary format to drive the following amplifier stage. The associated quantization noise can be spectrally shaped and removed out of band by the feedback loop in the BPDSM. The bandpass filter following the amplifier avoids power dissipation at undesired frequencies to achieve high efficiency. This architecture reduces the system complexity while increasing the flexibility.

Switching amplifiers are attractive candidates for the digital RF transmitters because of the potential to obtain high system efficiency while driven by digital signals. However, the suitable types of switching amplifiers are limited by the digital driving signals which are non-periodic and broadband. For instance, Class-E amplifiers can operate at RF frequencies efficiently by minimizing the output capacitance loss. However, the zero voltage switching condition for compensating the output capacitance loss cannot be maintained under non-periodic driving conditions, thus the conventional Class-E amplifier cannot achieve high efficiency when driven by the delta-sigma modulated signals.

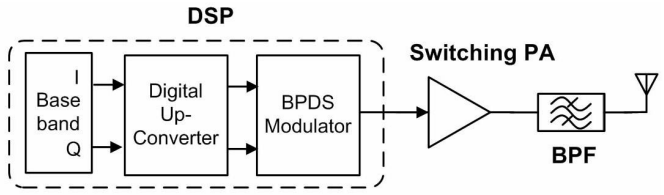

Fig. 1. Simplified block diagram of possible future digital RF transmitters with bandpass delta-sigma modulators.

Voltage-mode Class-D switching amplifiers have the potential to maintain high efficiency when the driving signals are not periodic. However, loss associated with the driving circuits (with limited bandwidth), the active devices (including shoot-through current loss) and filters (poor power recycling) can degrade the performance significantly. Previously, a bandpass delta-sigma Class-S amplifier was demonstrated at 10MHz, showing 33% drain efficiency with an IM3 of -40dBc [2]. A transformer-coupled amplifier was demonstrated at 170MHz with a drain efficiency of 8% [3]. A Class-D PA with a digital modulator based on quadrature pulse modulation was also demonstrated for EDGE signals [4].

This paper reports an H-bridge class-D amplifier implemented in CMOS which can be used in digital RF transmitters with linear and efficient amplification. The pull-up and pull-down devices of the Class-D amplifiers were driven separately to minimize the loss associated with the shoot-through currents. The H-bridge amplifier achieved a drain efficiency of 62% with 800MHz periodic signals. For CDMA IS-95 signals, the amplifier was driven by delta-sigma modulated signals with a clock rate of 3.2GHz. A drain efficiency of 31% was achieved with an output power of 15 dBm and an ACPR of -43dBc, demonstrating the feasibility of their application in digital RF transmitters.

II. Bandpass Delta-Sigma Modulation Signals

The driving signals of the H-bridge Class-D amplifier were generated by a simulated bandpass delta-sigma modulator

driven by CDMA signals with bandwidth 1.25MHz and 5.5dB peak to average power ratio. The bandpass delta-sigma modulator, as shown in Fig. 2, was composed of two resonators and two feedback loops, running at a clock rate of 3.2 GHz. The spectrum of the output binary signals is shown in Fig. 3. The desired signals are at 800 MHz. The quantization noise was spectrally shaped and removed out of band. A bandpass filter is required to recycle the out-of-band power including the harmonics and the quantization noise. For CDMA signals, the integrated power over the occupied signal bandwidth (1.25MHz) is defined as the inband power.

Inband power ratio, i. e. the ratio of the inband power to the total power, can be controlled by adjusting the feedback coefficient *B* of Fig. 2. Lower feedback coefficient *B* gives higher ratio of the desired inband power to total power. DSM driving signals with higher inband power ratio leads to higher amplifier output power as well as higher amplifier efficiency. However, signal quality is degraded with increasing inband power ratio. Fig. 4 displays the simulated adjacent channel power ratio (ACPR) and error vector magnitude (EVM) of the signals with increasing inband power ratio. The maximum power ratio is determined by the EVM and ACPR specifications of the system, which determine the tradeoff between PA efficiency and signal quality.

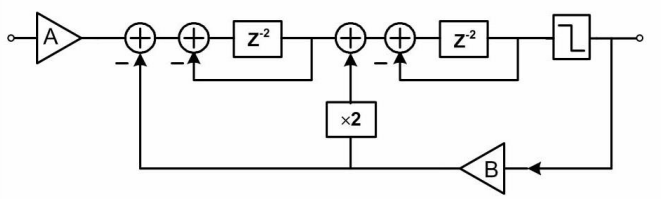

Fig. 2. Block diagram of a bandpass delta-sigma modulators. This modulator consists of two resonators and two feedback loops.

III. H-Bridge Class-D Amplifiers

A voltage-mode Class-D amplifier is one in which the output transistors are operated as switches. [5] The generated switch voltage waveform is sent to a series resonator which displays high impedance at all frequencies except for the resonant frequency, thus removing the out-of-band signals such as harmonics and quantization noise. Since the two devices are switched alternately, a voltage-mode class-D amplifier can be approximated as a voltage controlled voltage source, which operates efficiently when feeding a series resonator. This high efficiency feature can be maintained even if driven by non-periodic digital signals, as long as the reverse currents appearing in this condition can be provided by the active devices or parallel diodes during the ON state [6].

During the ON/OFF transition of the active devices, there is generally a short period of time when both PMOS and NMOS transistors are ON, resulting in a short-circuit between power supply and ground. A large current (known as shoot-through current) may be induced, which causes significant energy loss. To minimize this loss, the PMOS and NMOS were designed to have different driving circuits, as shown in Fig. 5. By modifying the pull-up and pull-down device size ratio of the drivers, the overlap of the turn ON time between the PMOS and the NMOS during the transition can be minimized.

Two voltage-mode Class-D amplifiers with shoot-through current suppression were designed and implemented with

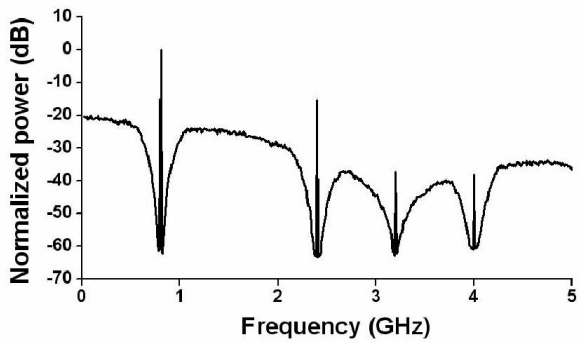

Fig. 3. Simulated spectrum of the delta-sigma modulated signals, showing that the quantization noise is shaped and removed out of band.

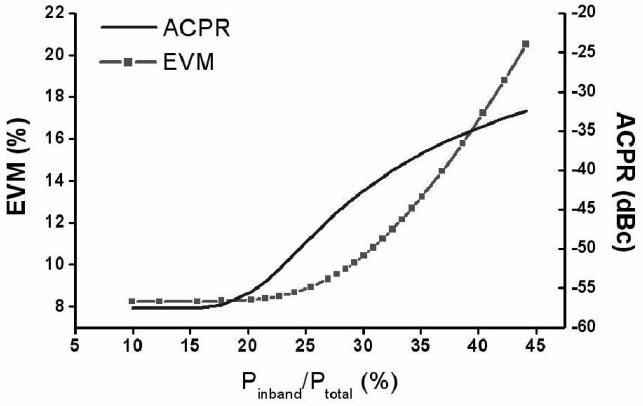

Fig. 4. Simulated ACPR and EVM for CDMA signals after passing through delta-sigma modulator as a function of inband power ratio.

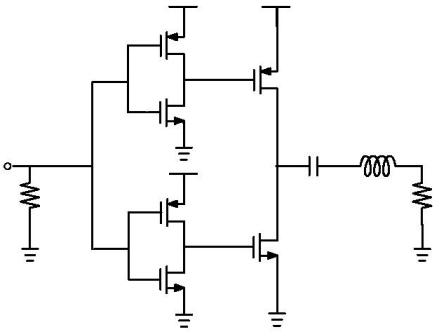

Fig. 5. Schematic of the voltage-mode Class-D power amplifier with shoot through current suppression by separating the driver for PMOS and NMOS at the output stage.

0.18um CMOS devices, as part of the Jazz BiCMOS technology. The transistor sizes of the NMOS and PMOS at the switching stage were 1.6mm and 4mm. The pull-up/pull-down device ratio of the drivers for NMOS and PMOS were 1:1 and 5:1, respectively. The reverse currents were obtained through the substrate diode of the MOS. The number of body contacts was maximized to reduce the parasitic resistance. The drain power supply voltage was 1.8V. Fig. 6 indicates the schematic of the H-bridge Class-D amplifier which consists of two Class-D amplifiers and a combiner. The driving signals Vin1 and Vin2 were complementary. A quarter-wave length of coaxial line combined the output signals and quarter-wave length transmission lines implemented the impedance transformation. In this work, the coaxial balun and the matching networks were realized off-chip. Both balun and matching networks can be implemented in an integrated fashion by CMOS technology in future work.

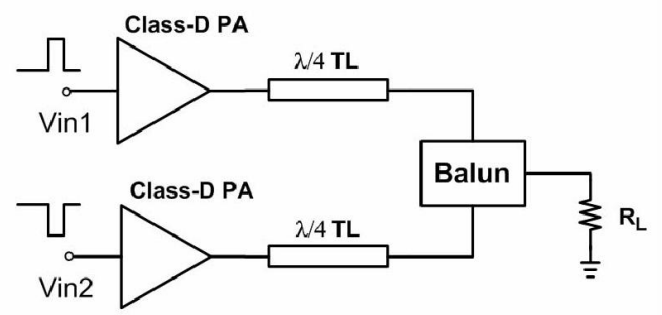

Fig. 6. Schematic of the H-bridge Class-D power amplifier.

IV. Amplifier Measurement Results

The drain efficiency and dc currents of the H-bridge Class-D amplifier were measured with periodic driving signals. Fig. 8 shows that the maximum current occurs at the desired frequency (800MHz) and drops dramatically for out of band frequencies. This feature verified the ability to reject out of band power of the DSM signals including harmonics and quantization noise. The peak drain efficiency and peak output power were 62% and 21 dBm, respectively. Here the drain efficiency considers the switching stage power consumption only, while the PAE considers the total DC power consumed by both driver and switching stage (since the input power to the driver is negligible).

A CDMA-like QPSK signal with a 1.25 MHz symbol rate and a 5.5 dB peak-to-average ratio was up-sampled and fed to a bandpass delta-sigma modulator. This modulated binary

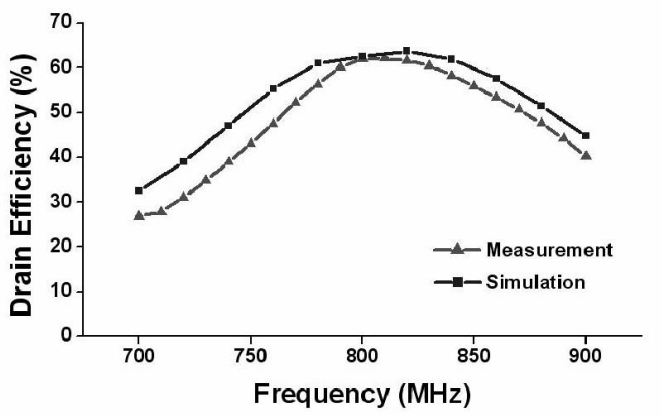

Fig. 7. Measured drain efficiency as a function of frequency

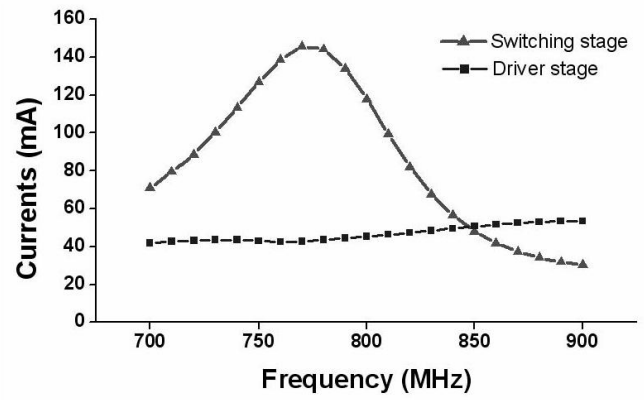

Fig. 8. Measured DC current as a function of frequency

pattern with a length of 12Mbits was implemented in Matlab and then sent to an Agilent 81134A pulse pattern generator which outputs two complementary binary signals with amplitude of 1.8V. These two complementary signals drove two Class-D PAs of the H-bridge amplifier, respectively. The input signal ACPR was measured after combining the differential signals with a quarter-wave coaxial combiner. The drain efficiency and the ACPR of the PA were measured with different inband power ratio. For the DSM signals with inband power ratio of 24%, the amplifier obtained a drain efficiency of 26% with an ACPR of -49 dBc, as shown in Fig. 9. For DSM signals with inband power ratio of 30%, a drain efficiency of 31% was achieved with an ACPR of -43 dBc. Both amplifier output spectrums meet the CDMA specifications which is -42 dBc at 885 kHz. Fig. 11 displays the measured ACPR of the input and output of the PA and the drain efficiency. Higher efficiency can be obtained by increasing the encoded inband power ratio, although the signal quality was degraded at the same time due to the characteristics of the DSM. This signal quality degradation limits the amplifier efficiency in digital RF transmitters.

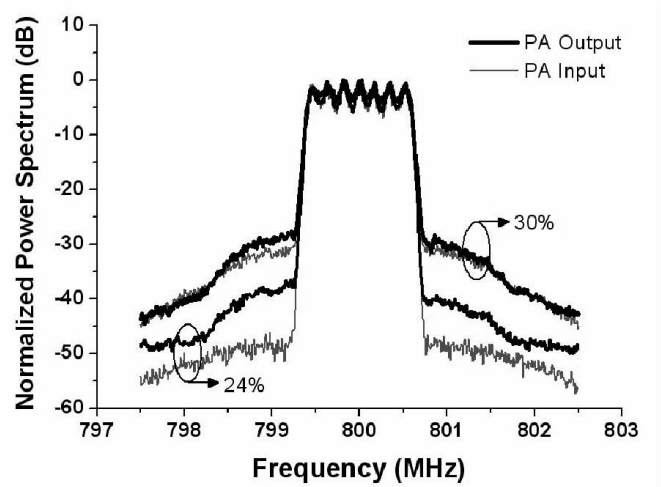

Fig. 9. Measured input and output spectrum for DSM signals with a inband power ratio of 30% and 24%, respectively.

Fig. 11 indicates the DC power consumption and the output power of the H-bridge Class-D PA as a function of the inband power contained in the input waveform. The output inband power increases with the input inband power linearly. The power consumption at the switch stage gradually increases with the measured input inband power while the power consumption at the driver stage keeps almost constant. The power consumption increases because the DC power consumed at the switch stage includes the output power and energy loss such as $\frac{1}{2}CV^2$ and ON-state resistance (R_{on}) loss. In the higher output power region, the switches have to conduct more current than at lower output power; therefore, R_{on} loss increases with output power.

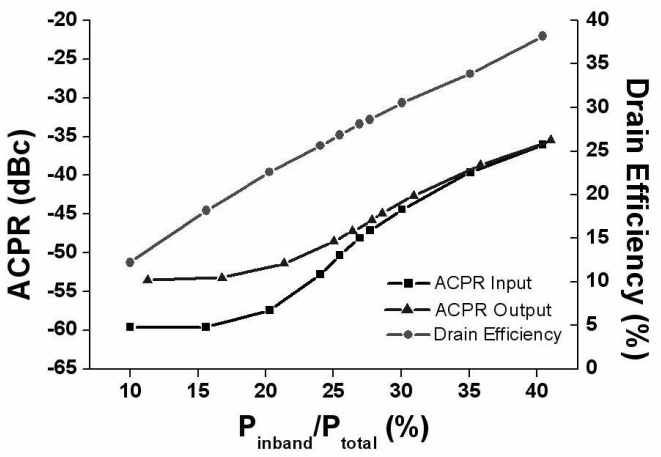

Fig. 10. Measured ACPR and drain efficiency of the CMOS H-bridge amplifier for DSM signals with different inband power ratio.

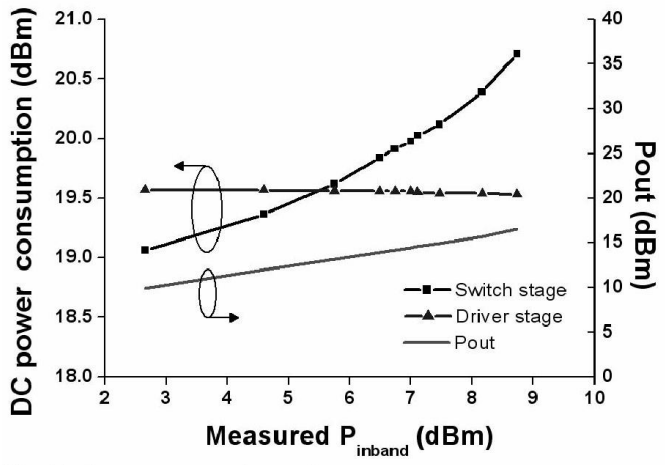

Fig. 11. Power consumption and output power

VII. Conclusion

An H-bridge Class-D amplifier was demonstrated at 800 MHz. The amplifier efficiency was increasing for the DSM signals with higher encoded inband power ratio. A drain efficiency of 31% was achieved with an ACPR of -43dBc for DSM signals with a inband power ratio of 30%. The results show the feasibility of using the H-bridge Class-D amplifier in digital RF transmitters.

The output power and efficiency of this amplifier approach can be expected to further improve with the application of stacked transistor technology, as well as reduced gate lengths.

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