Exercise 3 : Cache Coherency

Exercise 3.1: Memory Overhead

Cache Size of each Processor: 30 MB = 30.000.000 Byte

Cache Line Size: 64 Byte

Cache Lines per Cache: 30.000.000/64 = 468.750

As we want to use the MESI-protocol we have to assign, two additional bits to each cache line to present the four states „Modified“, „Exclusive“, „Shared“ or „Invalid“.

468.750 * 2 Bits = 937.500 Bits = 117.187,5 Byte = 117,1875 KB

So about 118 KB additional memory needed for each processor, which is about 0,3% more memory needed than without the MESI-protocol.

Exercise 3 : Cache Coherency

Exercise 3.2: Valid State Combinations

The valid state combinations are as follows:

	M	E	S	I
M	Invalid	Invalid	Invalid	Valid
E	Invalid	Invalid	Invalid	Valid
S	Invalid	Invalid	Valid	Valid
I	Valid	Valid	Valid	Valid

M: Modified, E: Exclusive, S: Shared, I: Invalid

Exercise 3 : Cache Coherency

Exercise 3.3: Sequence of Operations and States

Step	Op(Processor)	C0	C1	C2	C3	Comments
0		I	I	I	I	
1	Read(P0)	E	I	I	I	Invalid cache line in P0 has to be fetched and is now exclusive available in P0
2	Write(P0)	M	I	I	I	P0 writes at C0, now C0 differs from cache line in main memory, cache line in P0 was modified
3	Read(P1)	M	E	I	I	Invalid cache line in P1 has to be fetched and is now exclusive available in P1 (P0 was modified)
4	Write(P2)	M	E	M	I	P2 writes to an invalid cache line, this cache line is now „dirty“ and so it’s also modified
5	Read(P2)	M	E	M	I	P2 reads the „dirty“ cache line at C2, which is already marked as modified ➔ no changes
6	Read(P3)	M	S	M	S	Invalid cache line in P3 has to be fetched. As this cache line is also loaded to P1, it’s marked as **S**
7	Write(P0)	M	S	M	S	P0 overwrites the already modified cache line ➔
						no change of status bits needed
8	Write(P1)	M	M	M	E	P1 modifies C1 ➔ cache line C1 is now „dirty“ and so C3 is the exclusiv Cache which holds the cache line
9	Read(P0)	M	M	M	E	P0 reads the „dirty“ cache line at C0, which is already marked as modified ➔ no changes