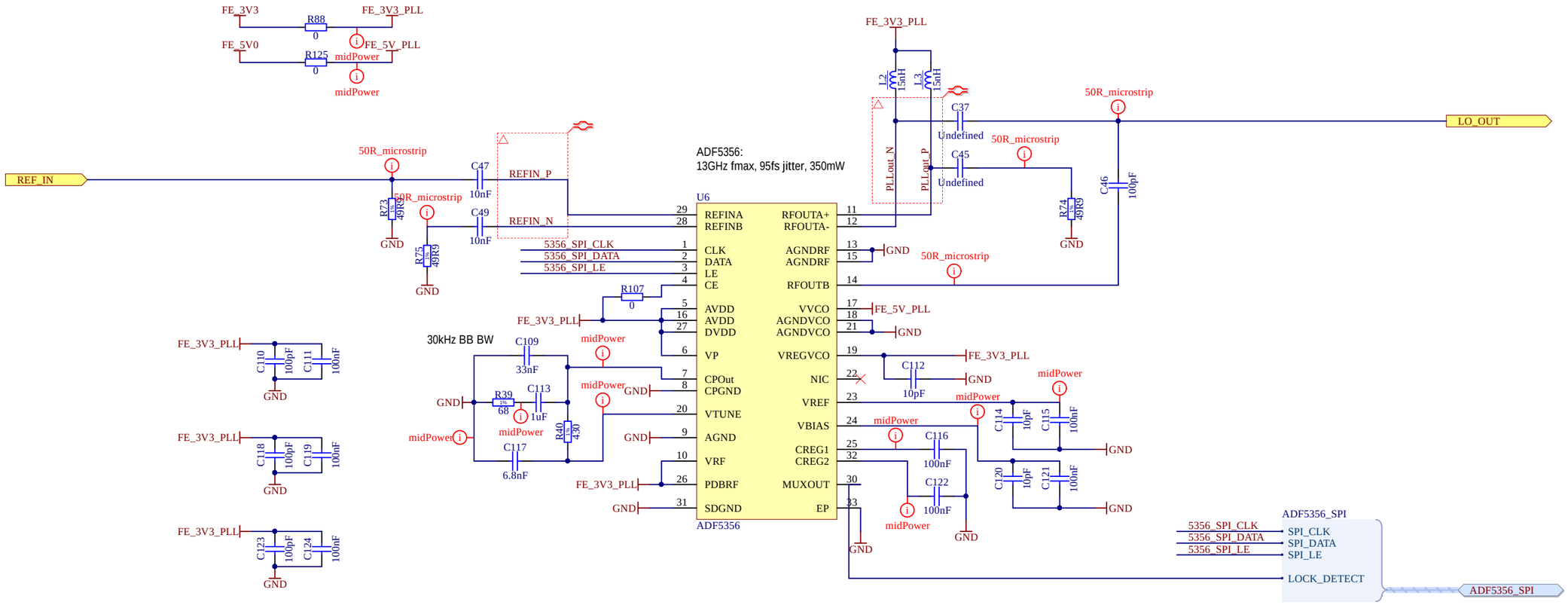

Overview

Features and Benefits | Product Details

- RF output frequency range: 53.125 MHz to 13,600 MHz
  - Noise floor integer channel: −227 dBc/Hz
  - Noise floor fractional channel: −225 dBc/Hz
- Integrated rms jitter (1 kHz to 20 MHz): 97 fs for 6 GHz output
- Fractional-N synthesizer and integer N synthesizer
- Pin compatible to the ADF5355
- High resolution, 52-bit modulus
- Phase frequency detector (PFD) operation to 125 MHz
- Reference input frequency operation to 600 MHz
- Maintains frequency lock over −40°C to +85°C
- Low phase noise, voltage controlled oscillator (VCO)
- Programmable divide by 1, 2, 4, 8, 16, 32, or 64 output
- Analog and digital power supplies: 3.3 V
- Charge pump and VCO power supplies: 5.0 V typical
- Logic compatibility: 1.8 V
- Programmable output power level
- RF output mute function
- Supported by the ADIsimPLL design tool

Project/Equipment -			
Document	Title Title2	Designer Designer	
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		Last Mod. -	07.02.2020
		File PLL.SchDoc	
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Separate ground plane for PA - no DC ground loop in case of powering from external connector.

Test without this filter. if harmonics are ok short it.

HFCN-1322+

J1 SMA — 50R_microstrip — FL1 (DC to 12000MHz) — 50R_microstrip — TGA3042 / TGA3042.SchDoc: RF_OUT, PA, RF_IN, Vdet

J6 Coax_1Male_1Shield — R7 Undefined — 50R_microstrip — PA_GND

50R_microstrip — FL2 (DC to 12000MHz) — R8 0

PreampTX / PreampTX.SchDoc: RF_OUT RF_IN

J2 Coax_1Male_1Shield — R2 Undefined — 50R_microstrip — PA_GND

50R_microstrip — FL3 (7900 to 11000 MHz) — R36 0

IC6 SIM-153+: RF, IF, LO, GND GND GND GND GND — LO_TX

J4 U.FL — R6 Undefined — 50R_microstrip — PA_GND

50R_microstrip — TX_IN — R44 0 — 50R_microstrip — BSC1

Can be exchanged for HFCN-9700+ or BFCN-5750+ for amateur bands. Can be short if not needed.

J3 SMA — FL6 (8250 to 8450MHz) — QPA2609 / QPA2609.SchDoc: RF_IN, LNA, RF_OUT

J9 U.FL — R55 Undefined — FL4 (5000 to 10100 MHz) — R65 0

IC7 SIM-153+: RF, IF, LO, GND GND GND GND GND — LO RX

J10 U.FL — R64 Undefined — R66 0 — FL5 (DC to 2400MHz)

PreampRX1 / Preamp.SchDoc: RF_IN, RF_OUT

PreampRX2 / Preamp.SchDoc: RF_IN, RF_OUT

J8 U.FL — R54 Undefined — C87 100pF — R67 0 — RX OUT — BSC4 BSC5 BSC21 BSC3 BSC7 BSC6

PreampLO_RX / Preamp.SchDoc: RF_IN, RF_OUT

IC8 YAT-3+: RFIN, RFOUT, GND GND GND GND GND EP

C88 100pF — LO RX — R104 Undefined — J13 U.FL

IC15 QCS-83+: SUM, PORT 1, PORT 2, GND GND, TERM — J11 U.FL — R68 Undefined — R69 0 — R71 49R9

IC16 YAT-3+: RFIN, RFOUT, GND GND GND GND GND EP

PreampLO_TX / PreampTX.SchDoc: RF_IN, RF_OUT — LO_TX — R106 Undefined — J14 U.FL

PLL / PLL.SchDoc: PLL, LO_OUT, REF_IN, ADF5356_SPI

J7 U.FL — R1 0

R72 0

OSC1 20MHZ: VCC, OUT, E/D, GND GND, NC NC NC NC NC — C13 100pF — C14 1nF — R9 0 — R5 Undefined — C43 100pF — C44 1nF

IC9 CDCLVC1102PW: CLKIN, Y0, Y1, 1G, VDD, GND — R4 Undefined — R3 Undefined — R25 Undefined

ADF5356_SPI: SPI_CLK, SPI_DATA, SPI_LE, SPI_CE, LOCK_DETECT — BSC8 BSC10 BSC11 BSC13 BSC20

VCO_Vtune — BSC14

REF_OUT — BSC2

J12

highPower — 3V3_FMC — FMC_3V3_IN — BSC18; FE_12V — FMC_12V_IN — BSC19

B9 SCH, B8 SCH, B31 SCH, B16 SCH, B5 SCH, B11 SCH, B15 SCH, B10 SCH, B30 SCH, B13 SCH, B29 SCH, B1 SCH, B3 SCH

GroundsCoupling / GroundsCoupling.SchDoc

FrontEnd_PS / FrontEnd_PS.SchDoc

POWER SUPPLY — TX_NSHDN, FE_NSHDN_DEEP

LNA_PD — BSC15

TX_NSHDN — BSC16

FE_NSHDN_DEEP — BSC17

CR_NSHDN — BSC12

Note: for debugging purposes shutdown pins are disconnected from FMC

INFO:

-due to filters used frontend shall operate with quite high IF 2GHz

LO FREQ can be adjusted from 4 to 8GHz (with component reassembly)

Project/Equipment	-		
Document	Title Title2	Designer Designer	
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		Last Mod. -	07.02.2020
		File FrontEnd.SchDoc	
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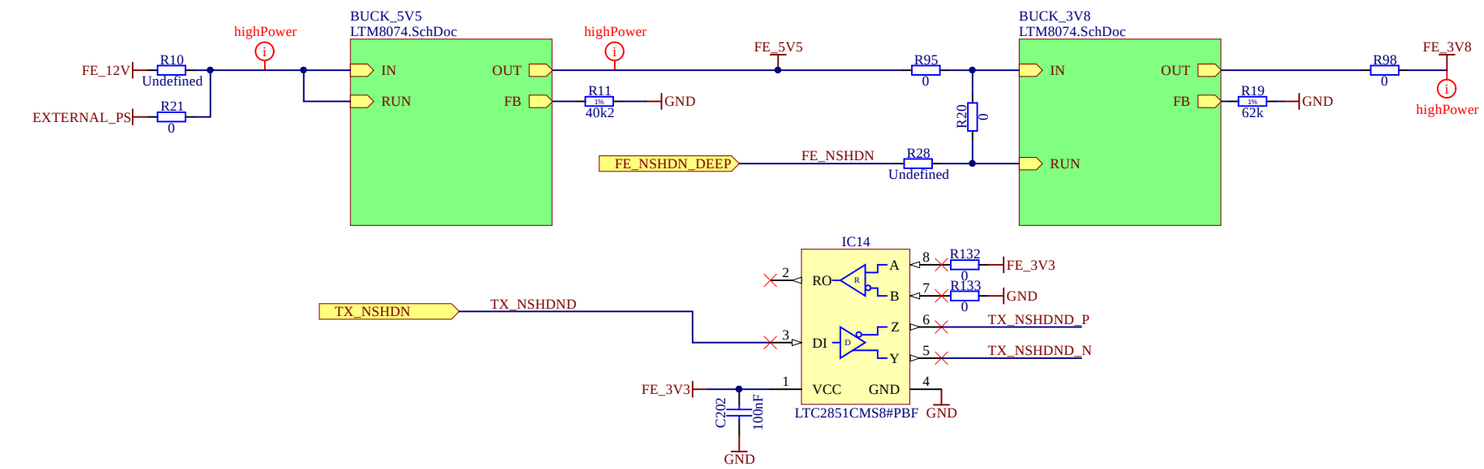

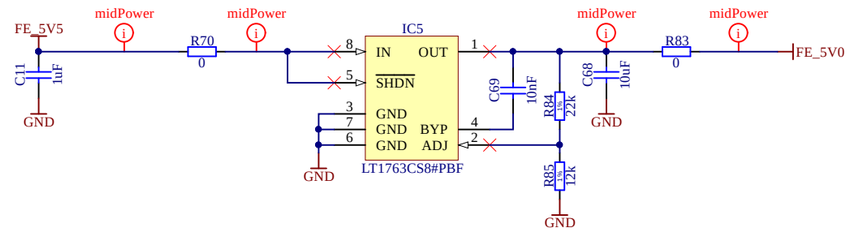

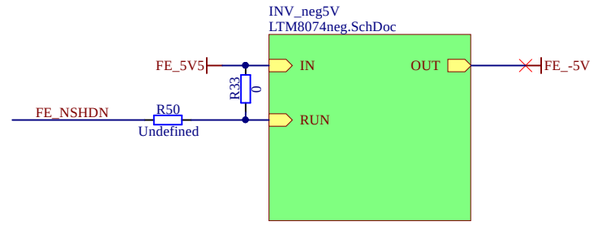

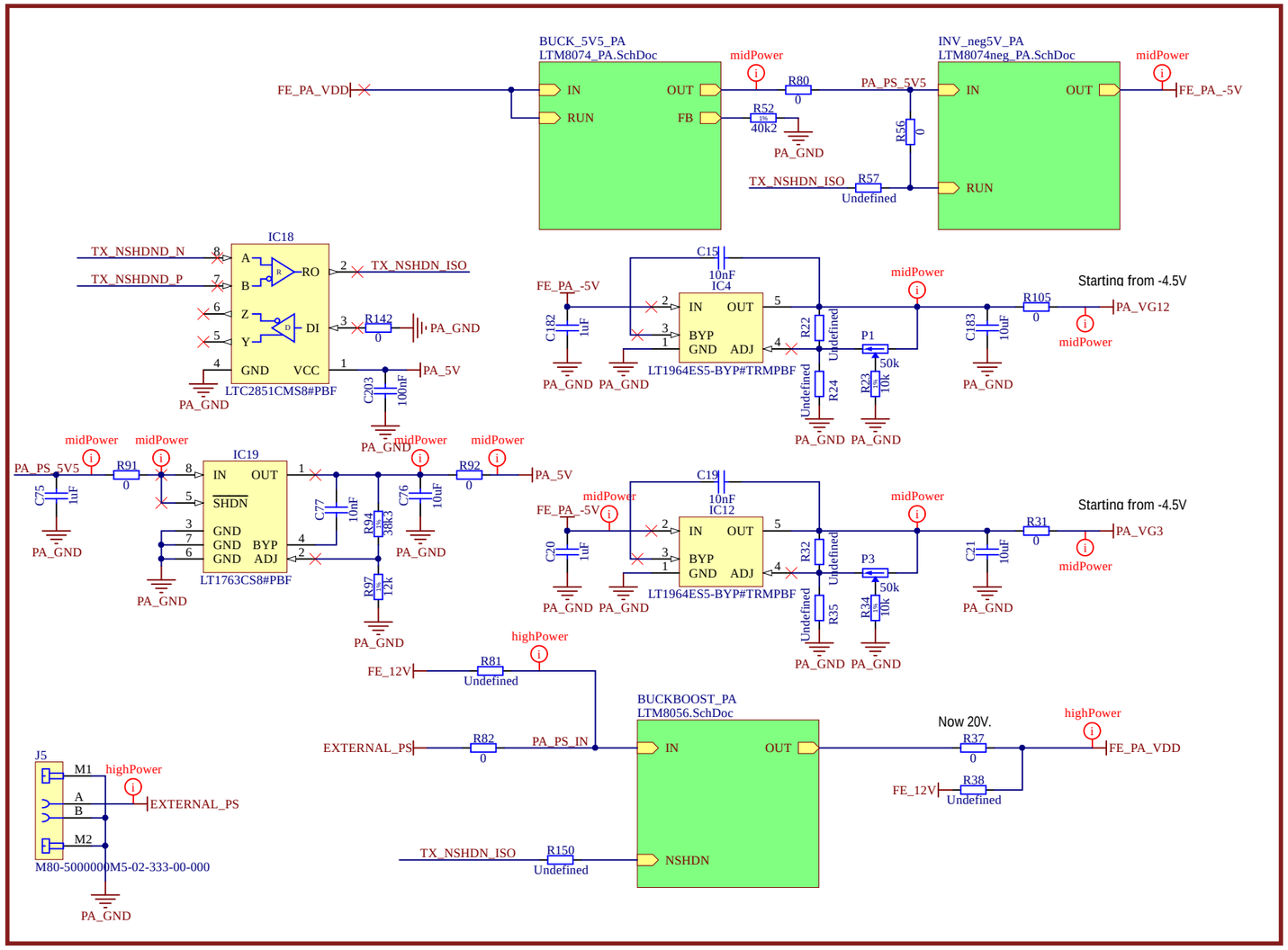

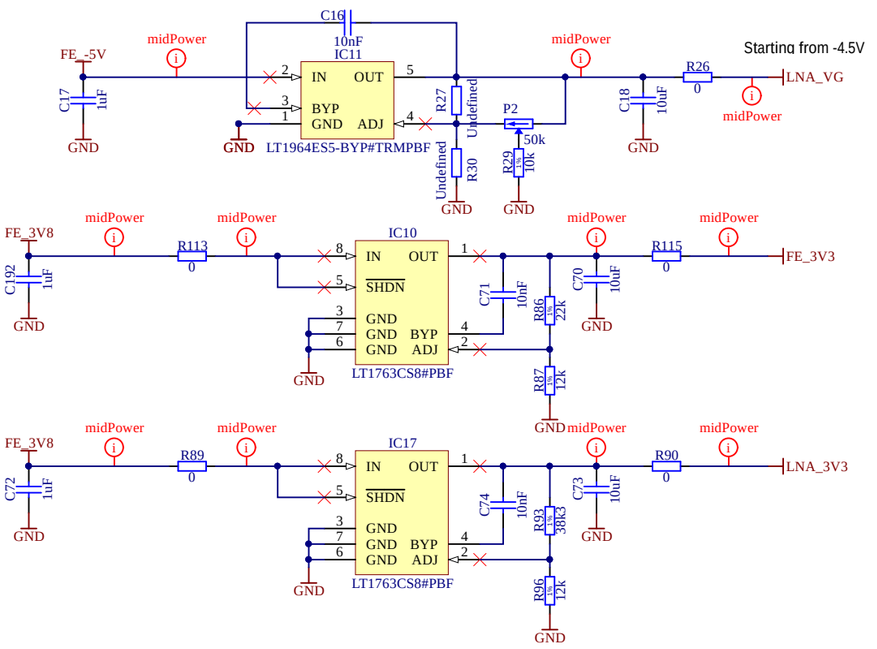

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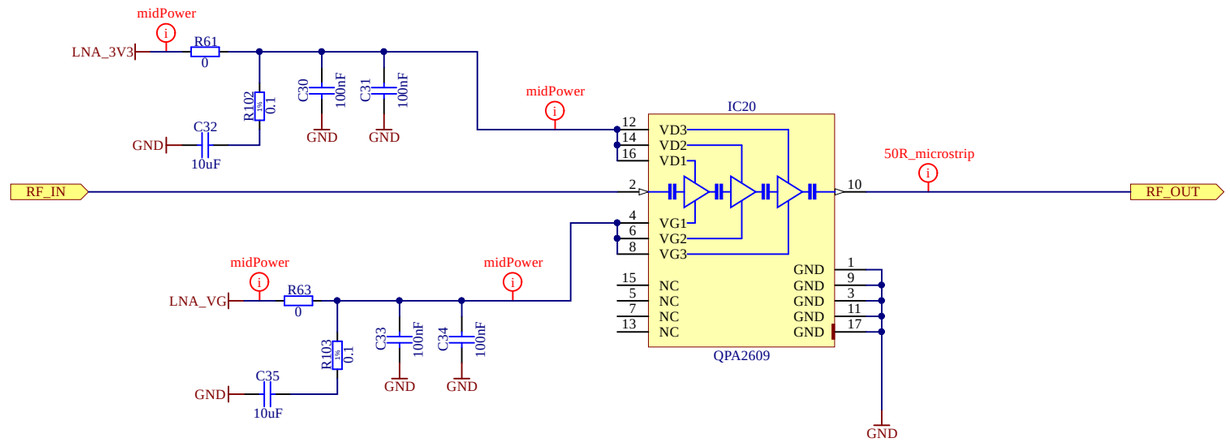
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-XXXXX-VX-X	Size A3 / Rev -



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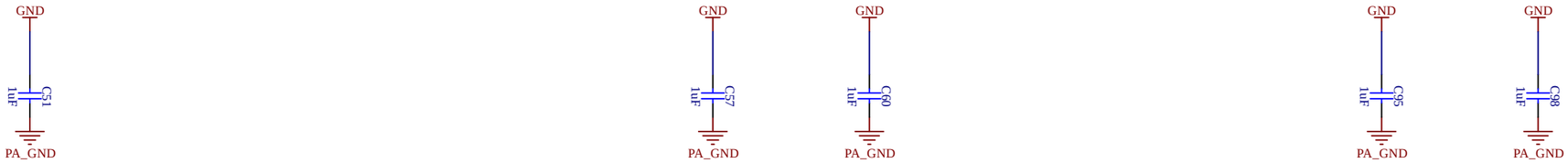
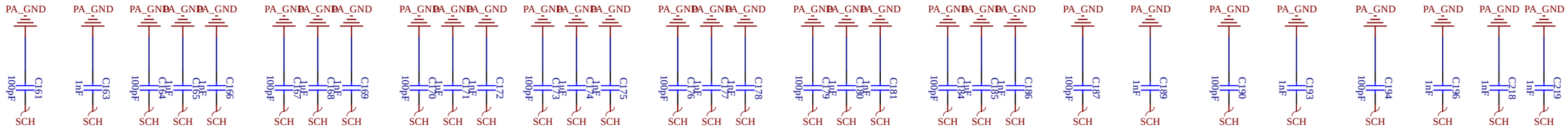
TE/MPE European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 Rev -

GND - PA GND coupling

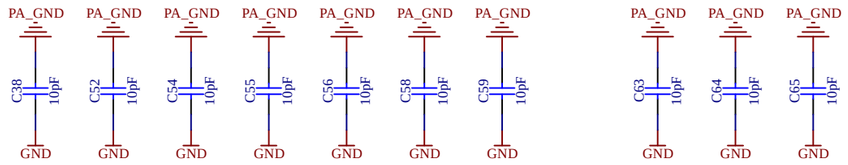


GND - shield coupling

PA GND - Shield Coupling



Ground couplinkg - RF signals



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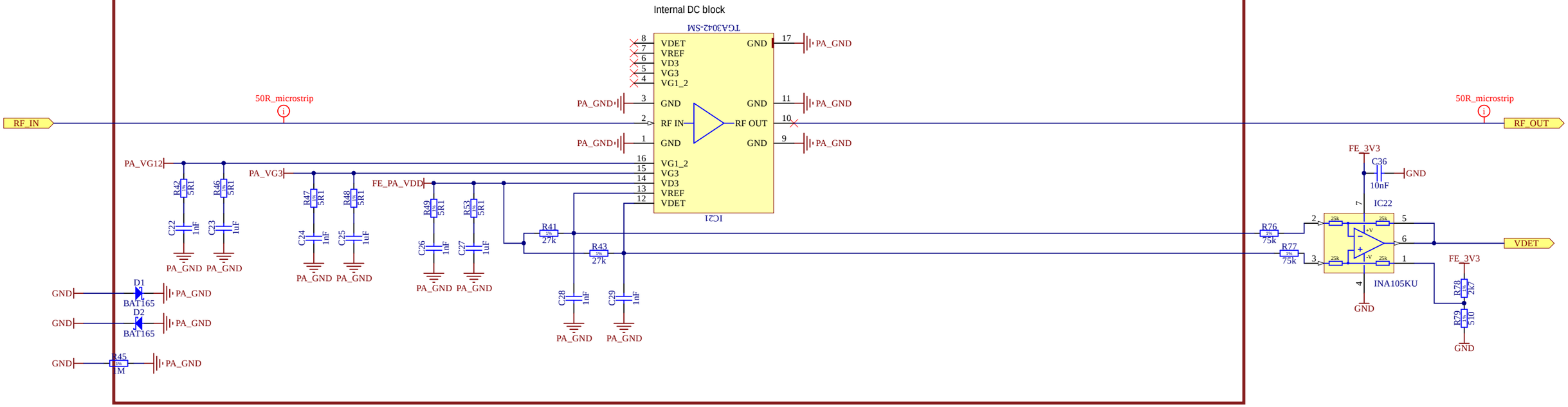
TE/MPE CERN	European Organization for Nuclear Research CH-1211 Genéve 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev -

Separate ground plane for PA - no DC ground loop in case of powering from external connector.

Internal DC block



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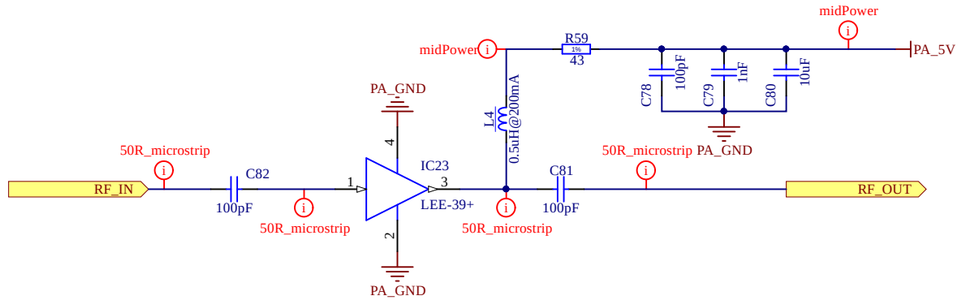
EDA-XXXXX-VX-X	Size A3 Rev -



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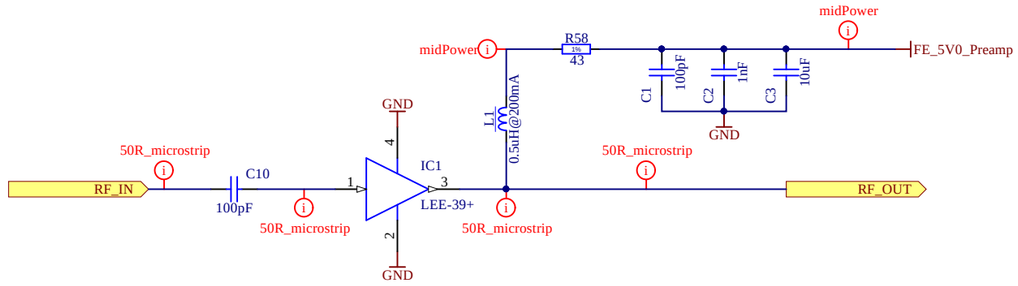

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European Organization for Nuclear Research
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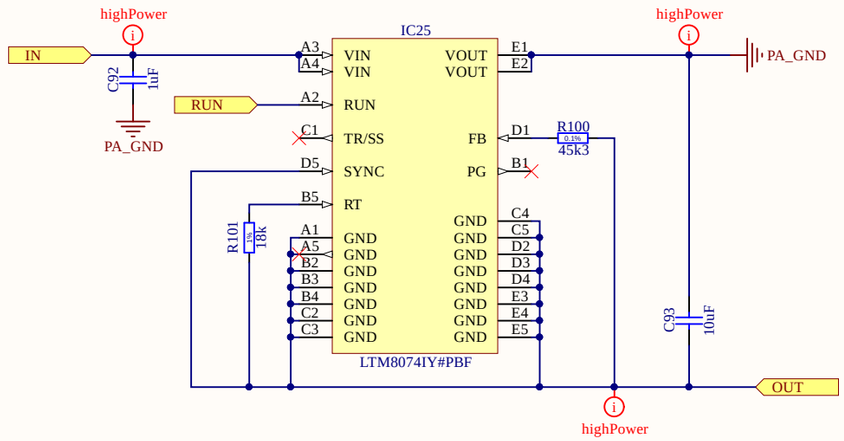

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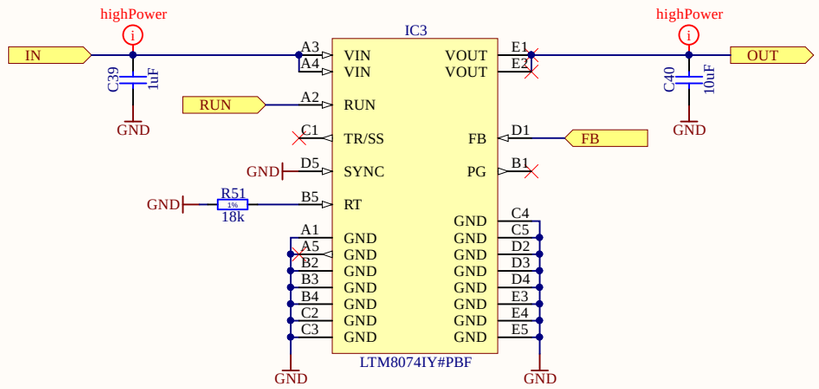

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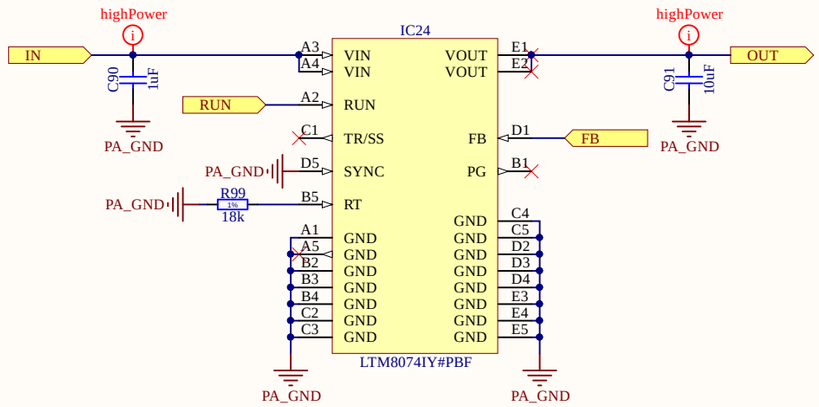

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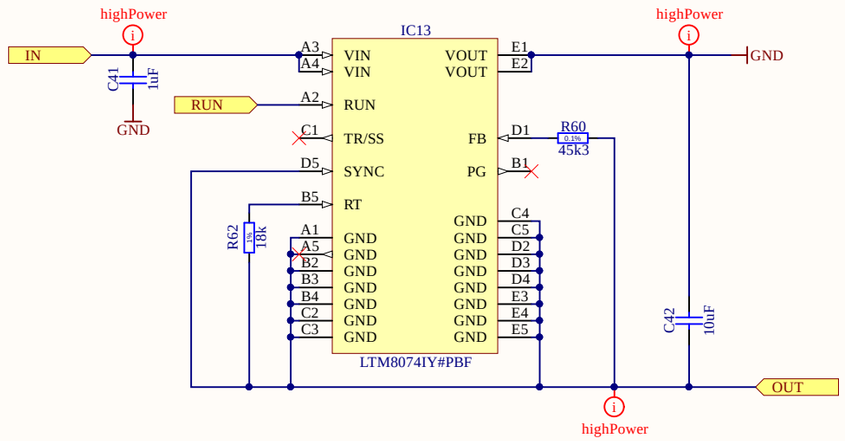

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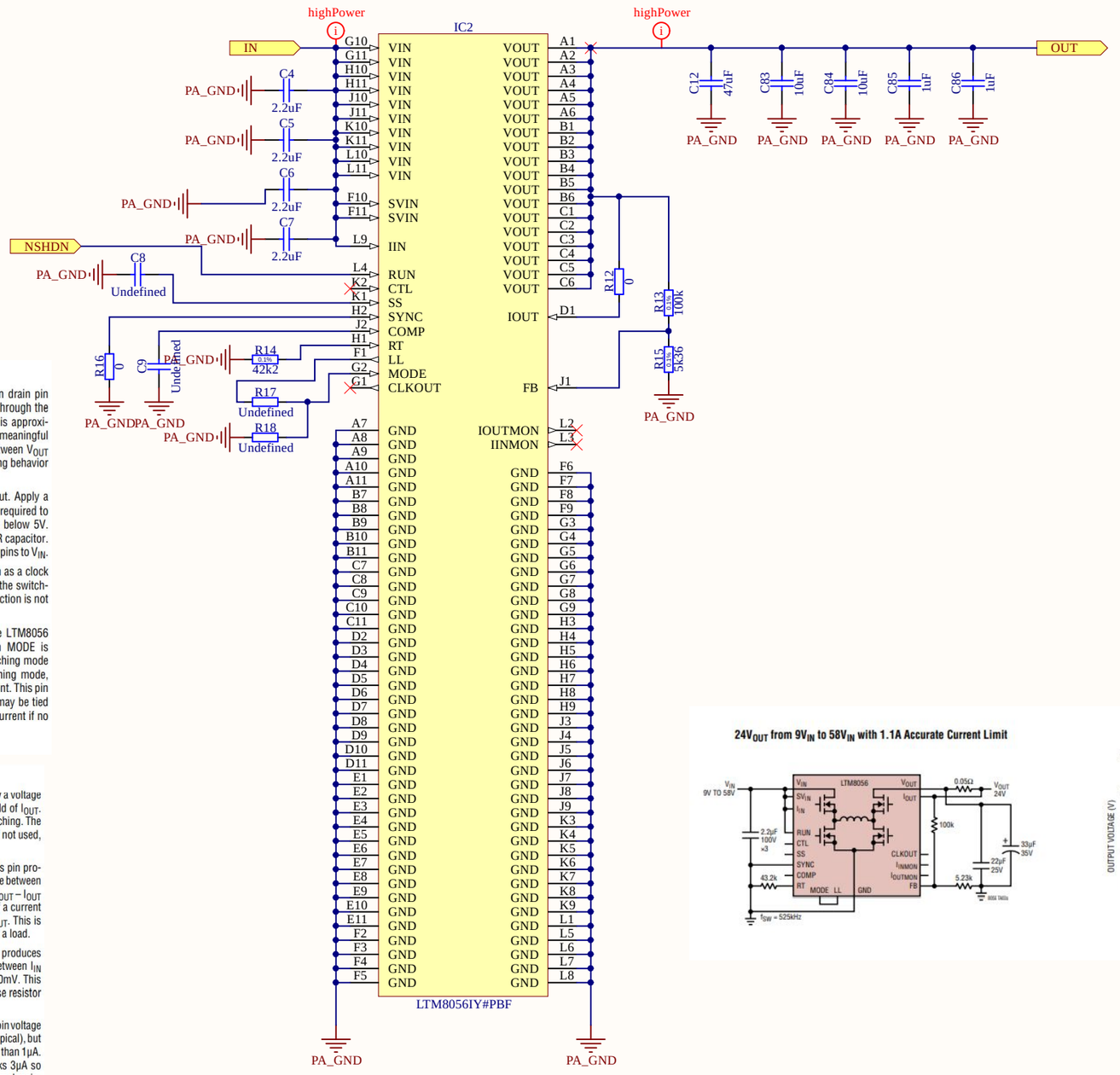


PIN FUNCTIONS

GND (Bank 1, Pin L1): Tie these GND pins to a local ground plane below the LTM8056 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8056 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the R_{FB1}/R_{FB2} feedback divider to this net.

V_{OUT} (Bank 2): Power Output Pins. Apply output filter capacitors between these pins and GND pins.

V_{IN} (Bank 3): Input Power. The V_{IN} pin supplies current to the LTM8056's internal power switches and to one terminal of the optional input current sense resistor. This pin must be locally bypassed with an external, low ESR capacitor; see Table 1 for recommended values.

I_{OUT} (Pin D1): Output Current Sense. Tie this pin to the output current sense resistor. The output average current sense threshold is 58mV, so the LTM8056 will regulate the output current to 58mV/R_{SENSE}, where R_{SENSE} is the value of the output current sense resistor in ohms. The load is powered through the sense resistor connected at this pin. Tie this pin to V_{OUT} if no output current sense resistor is used. Keep this pin within ±0.5V of V_{OUT} under all conditions.

LL (Pin F1): Light Load Indicator. This open drain pin indicates that the output current, as sensed through the resistor connected between V_{OUT} and I_{OUT}, is approximately equivalent to 6mV or less. Its state is meaningful only if a current sense resistor is applied between V_{OUT} and I_{OUT}. This is useful to change the switching behavior of the LTM8056 in light load conditions.

SV_{IN} (Pins F10, F11): Controller Power Input. Apply a separate voltage above 5V if the LTM8056 is required to operate when the main power input (V_{IN}) is below 5V. Bypass these pins with a high quality, low ESR capacitor. If a separate supply is not used, connect these pins to V_{IN}.

CLKOUT (Pin G1): Clock Output. Use this pin as a clock source when synchronizing other devices to the switching frequency of the LTM8056. When this function is not used, leave this pin open.

MODE (Pin G2): Switching Mode Input. The LTM8056 operates in forced continuous mode when MODE is open, and can operate in discontinuous switching mode when MODE is low. In discontinuous switching mode, the LTM8056 will block reverse inductor current. This pin is normally left open or tied to LL. This pin may be tied to GND for the purpose of blocking reverse current if no output sense resistor is used.

PIN FUNCTIONS

RT (Pin H1): Timing Resistor. The RT pin is used to program the switching frequency of the LTM8056 by connecting a resistor from this pin to ground. The range of oscillation is 100kHz to 800kHz. The Applications Information section of the data sheet includes a table to determine the resistance value based on the desired switching frequency. Minimize capacitance at this pin. A resistor to ground must be applied under all circumstances.

SYNC (Pin H2): External Synchronization Input. The SYNC pin has an internal pull-down resistor. See the Synchronization section in Applications Information for details. Tie this pin to GND when not used.

FB (Pin J1): Output Voltage Feedback. The LTM8056 regulates the FB pin to 1.2V. Connect the FB pin to a resistive divider between the output and GND to set the output voltage. See Table 1 for recommended FB divider resistor values.

COMP (Pin J2): Compensation Pin. The LTM8056 is equipped with internal compensation that works well with most applications. In some cases, the performance of the LTM8056 can be enhanced by modifying the control loop compensation by applying a capacitor or RC network to this pin.

SS (Pin K1): Soft-Start. Connect a capacitor from this pin to GND to increase the soft-start time. Soft-start reduces the input power source's surge current by gradually increasing the controller's current limit. Larger values of the soft-start capacitor result in longer soft-start times. If no soft-start is required, leave this pin open.

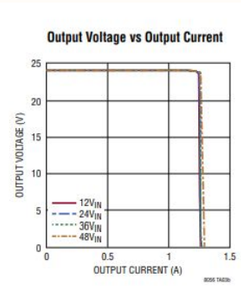
CTL (Pin K2): Current Sense Adjustment. Apply a voltage below 1.2V to reduce the current limit threshold of I_{OUT}. Drive CTL to less than about 50mV to stop switching. The CTL pin has an internal pull-up resistor to 2V. If not used, leave this pin open.

I_{OUTMON} (Pin L2): Output Current Monitor. This pin produces a voltage that is proportional to the voltage between V_{OUT} and I_{OUT}. I_{OUTMON} will equal 1.2V when $V_{OUT} - I_{OUT}$ = 58mV. This feature is generally useful only if a current sense resistor is applied between V_{OUT} and I_{OUT}. This is a high impedance output. Use a buffer to drive a load.

I_{INMON} (Pin L3): Input Current Monitor. This pin produces a voltage that is proportional to the voltage between I_{IN} and V_{IN}. I_{INMON} will equal 1V when I_{IN}-V_{IN} = 50mV. This feature is generally useful only if a current sense resistor is applied between V_{IN} and I_{IN}.

RUN (Pin L4): LTM8056 Enable. Raise the RUN pin voltage above 1.2V for normal operation. Above 1.2V (typical), but below 6V, the RUN pin input bias current is less than 1µA. Below 1.2V and above 0.3V, the RUN pin sinks 3µA so the user can define the hysteresis with the external resistor selection. This will also reset the soft-start function. If RUN is 0.3V or less, the LTM8056 is disabled and the SV_{IN} quiescent current is below 1µA.

I_{IN} (Pin L9): Input Current Sense. Tie this pin to the input current sense resistor. The input average current sense threshold is 50mV, so the LTM8056 will regulate the input current to 50mV/R_{SENSE}, where R_{SENSE} is the value of the input current sense resistor in ohms. Tie to V_{IN} when not used. Keep this pin within ±0.5V of V_{IN} under all conditions.



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