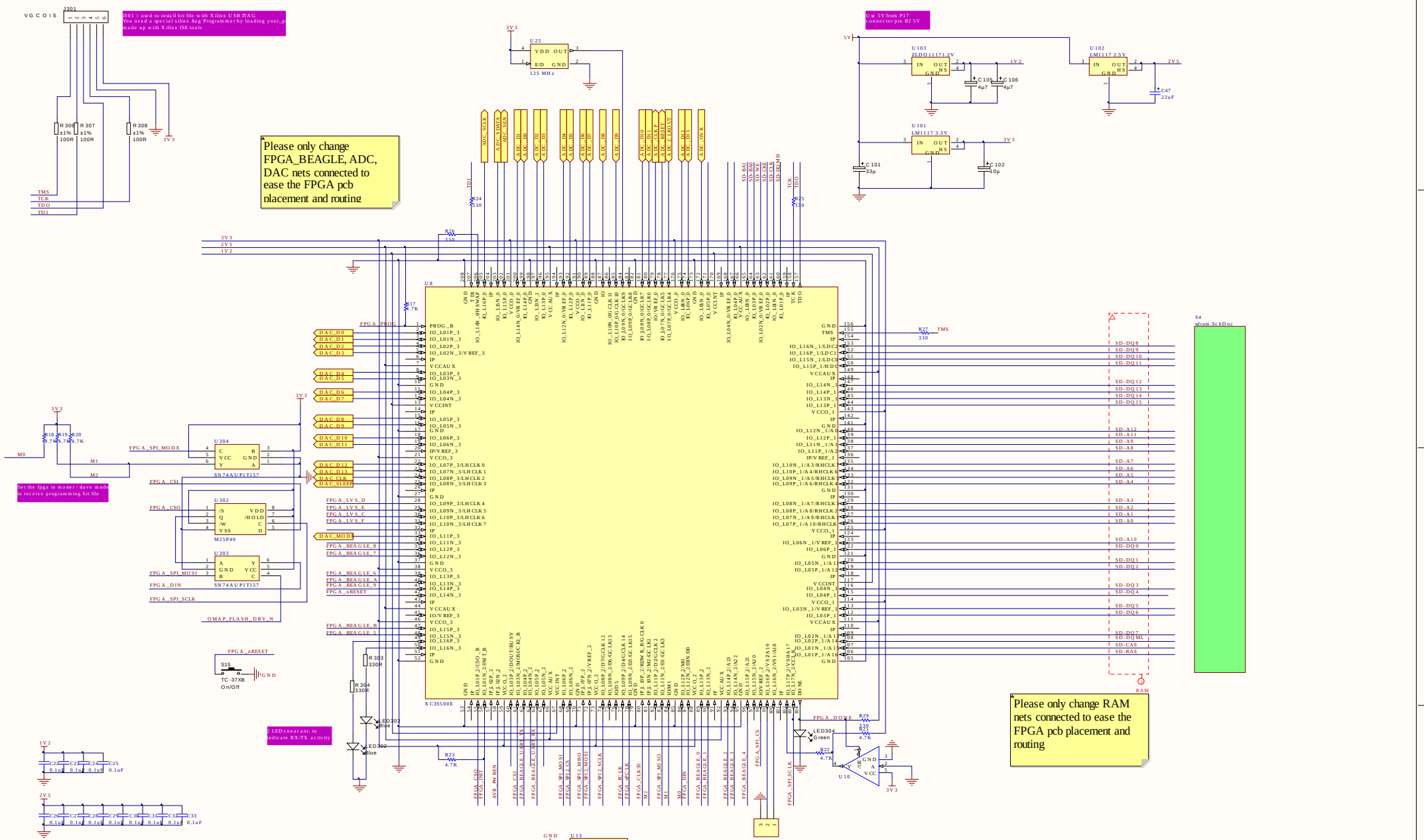
J301
VGCOIS
B01 = used to install bit file with Xilinx USB JTAG
You need a special Xilinx Jtag Programmer by loading your_p
made up with Xilinx ISE tools
R306 ±1% 100R
R307 ±1% 100R
R308 ±1% 100R
3V3
TMS
TCK
TDO
TDI
Please only change FPGA_BEAGLE, ADC, DAC nets connected to ease the FPGA pcb placement and routing
U25
VDD OUT
E/D GND
125 MHz
U8
XC3S500E
U103
ZLDO11171.2V
1V2
U102
LM1117 2.5V
2V5
U101
LM1117 3.3V
3V3
5V
U304
SN74AUP1T157
U302
M25P40
U303
SN74AUP1T157
FPGA_SPI_MODE
FPGA_CS1
FPGA_CS0
FPGA_SPI_MOSI
FPGA_DIN
FPGA_SPI_SCLK
OMAP_FLASH_DRV_N
FPGA_nRESET
S15
TC-37XB
On/Off
GND
LED303
Blue
LED302
Blue
LED304
Green
U10
R23 4.7K
R22 4.7K
R29 330
R31 4.7K
R27 330
TMS
R24 330
R25 330
R26 330
R17 4.7K
R18 4.7K
R19 4.7K
R20 4.7K
M0
M1
M2
Set the fpga in master/slave mode to receive programming bit file
2 LEDs near ant. to indicate RX/TX activity
U13
TXS0102
UART between FPGA and beagleboard-x15
JP5
Header
S4
sdram_SchDoc
RAM
Please only change RAM nets connected to ease the FPGA pcb placement and routing
Title
Size A2
Number
Revision
Date: 07/04/2018
Sheet of
File: C:\Users\ddc\schdoc
Drawn By: