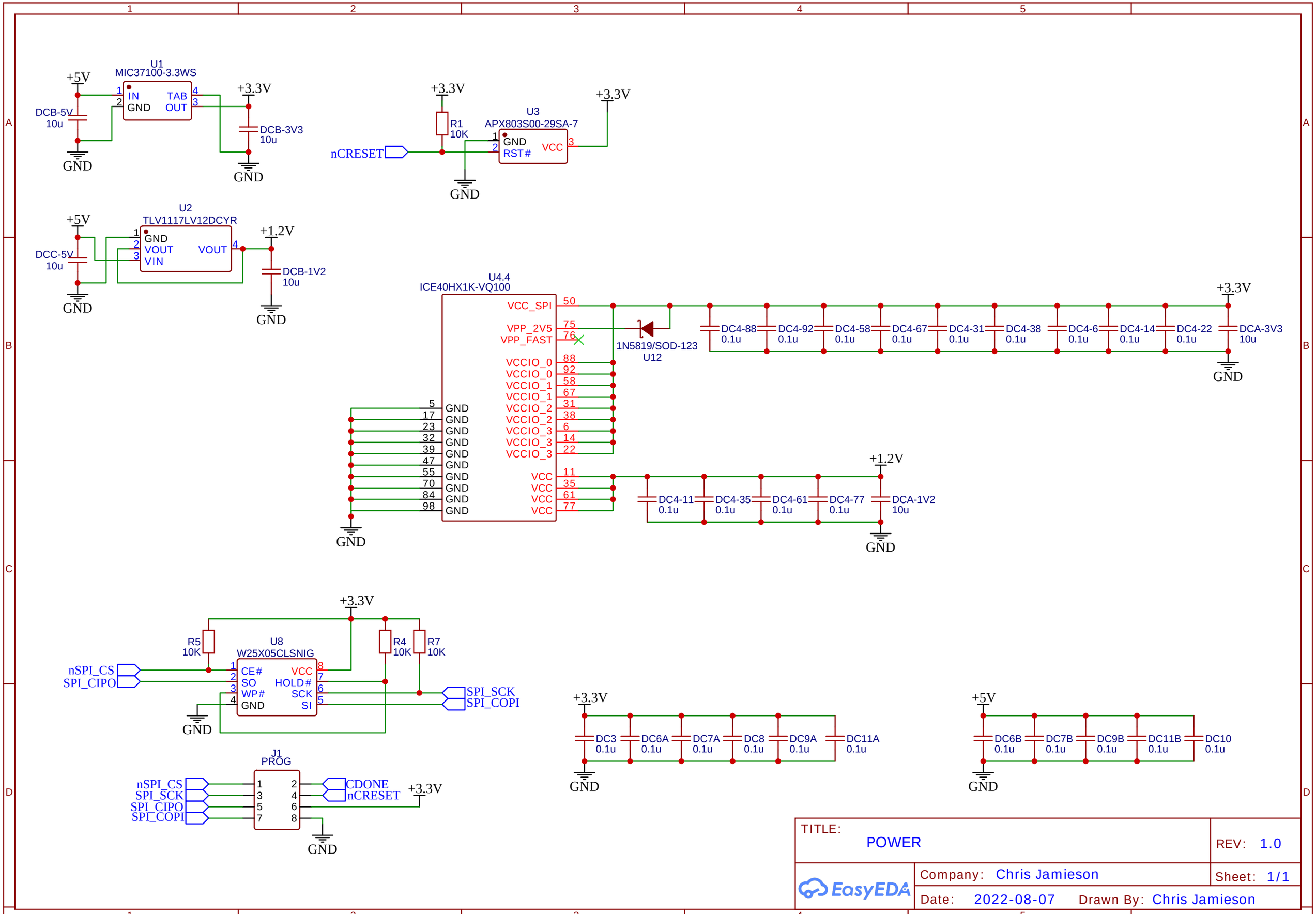


TITLE: POWER

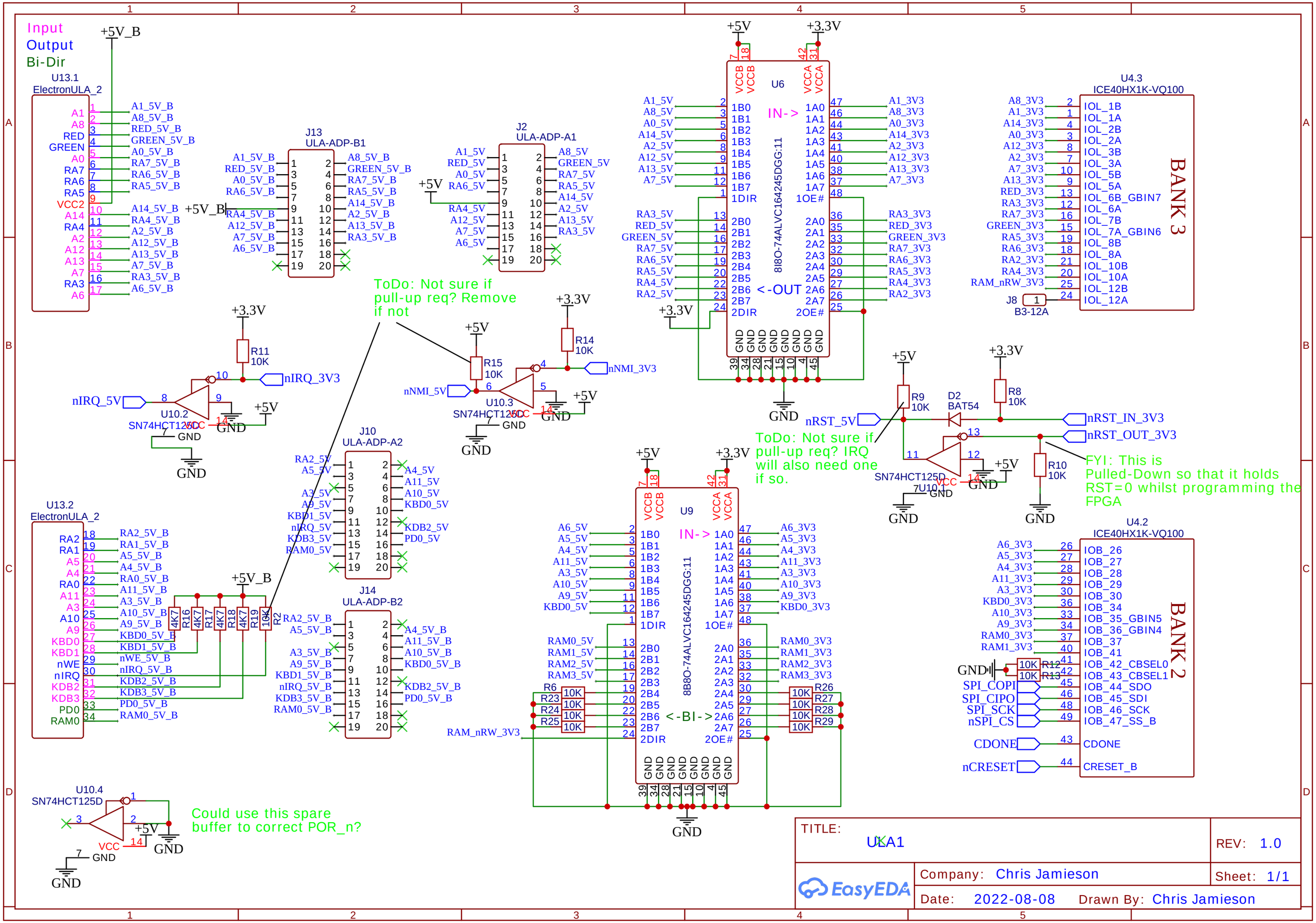
REV: 1.0

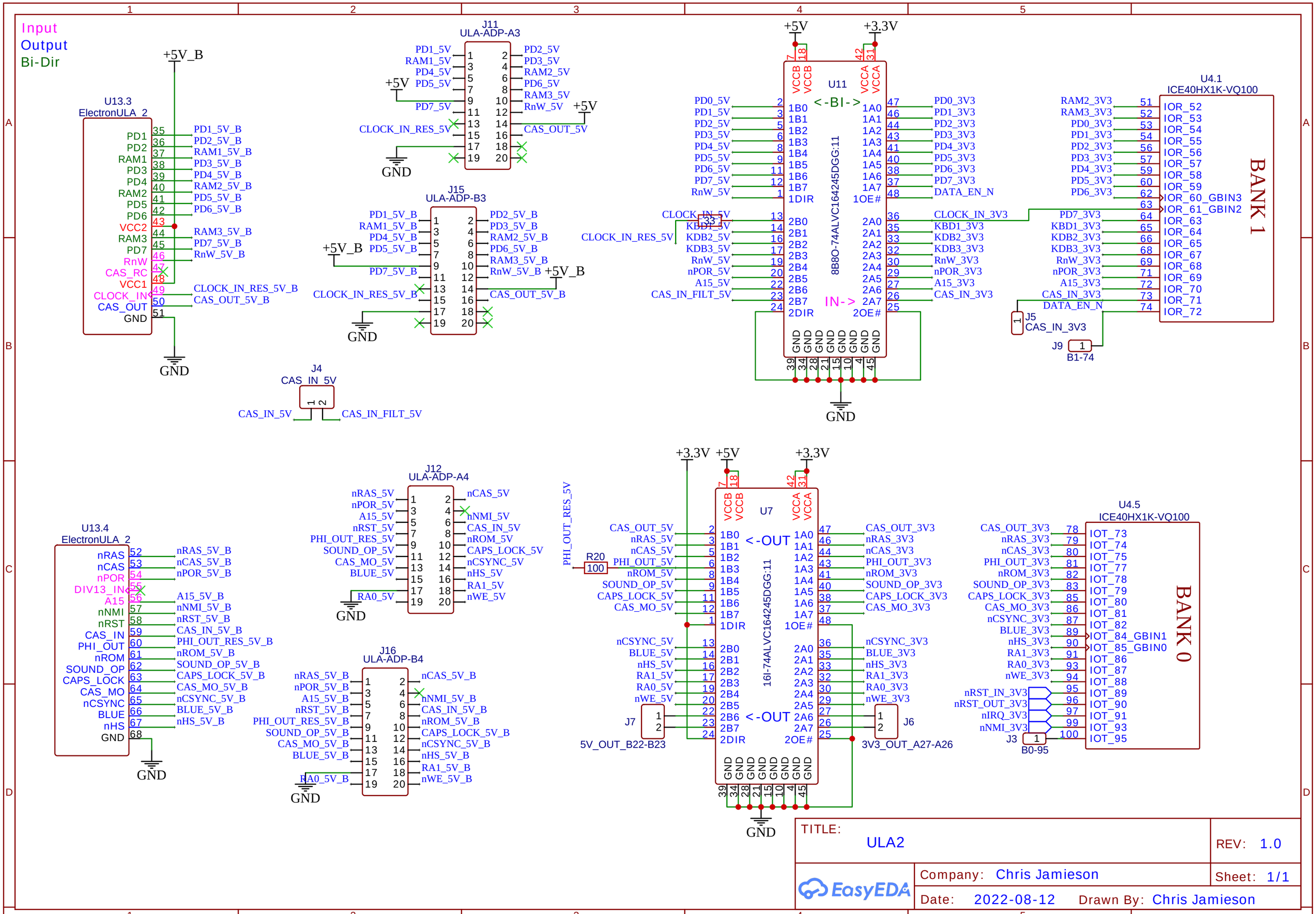
Company: Chris Jamieson

Sheet: 1/1

Date: 2022-08-07

Drawn By: Chris Jamieson


Input
Output
Bi-Dir
U13.1
ElectronULA_2
J13
ULA-ADP-B1
J2
ULA-ADP-A1
U6
8BO-74ALVC164245DGG:11
IN->
<-OUT
U4.3
ICE40HX1K-VQ100
BANK 3
J8
B3-12A
ToDo: Not sure if pull-up req? Remove if not
U10.2
SN74HCT125D
U10.3
SN74HCT125D
R11 10K
R15 10K
R14 10K
nIRQ_5V
nIRQ_3V3
nNMI_5V
nNMI_3V3
J10
ULA-ADP-A2
J14
ULA-ADP-B2
U13.2
ElectronULA_2
U9
8BO-74ALVC164245DGG:11
<-BI->
U4.2
ICE40HX1K-VQ100
BANK 2
R9 10K
D2 BAT54
R8 10K
R10 10K
nRST_5V
nRST_IN_3V3
nRST_OUT_3V3
U10.1
SN74HCT125D
ToDo: Not sure if pull-up req? IRQ will also need one if so.
FYI: This is Pulled-Down so that it holds RST=0 whilst programming the FPGA
U10.4
SN74HCT125D
Could use this spare buffer to correct POR_n?
TITLE:
ULA1
REV: 1.0
Company: Chris Jamieson
Sheet: 1/1
Date: 2022-08-08
Drawn By: Chris Jamieson
EasyEDA


Input
Output
Bi-Dir
U13.3
ElectronULA_2
+5V_B
PD1 35 PD1_5V_B
PD2 36 PD2_5V_B
RAM1 37 RAM1_5V_B
PD3 38 PD3_5V_B
PD4 39 PD4_5V_B
RAM2 40 RAM2_5V_B
PD5 41 PD5_5V_B
PD6 42 PD6_5V_B
VCC2 43
RAM3 44 RAM3_5V_B
PD7 45 PD7_5V_B
RnW 46 RnW_5V_B
CAS_RC 47
VCC1 48
CLOCK_IN 49 CLOCK_IN_RES_5V_B
CAS_OUT 50 CAS_OUT_5V_B
GND 51
GND
J11
ULA-ADP-A3
PD1_5V 1 2 PD2_5V
RAM1_5V 3 4 PD3_5V
PD4_5V 5 6 RAM2_5V
+5V PD5_5V 7 8 PD6_5V
PD7_5V 9 10 RAM3_5V
11 12 RnW_5V +5V
CLOCK_IN_RES_5V 13 14 CAS_OUT_5V
15 16
17 18
19 20
GND
J15
ULA-ADP-B3
PD1_5V_B 1 2 PD2_5V_B
RAM1_5V_B 3 4 PD3_5V_B
PD4_5V_B 5 6 RAM2_5V_B
+5V_B PD5_5V_B 7 8 PD6_5V_B
PD7_5V_B 9 10 RAM3_5V_B
11 12 RnW_5V_B +5V_B
CLOCK_IN_RES_5V_B 13 14 CAS_OUT_5V_B
15 16
17 18
19 20
GND
J4
CAS_IN_5V
1 2
CAS_IN_5V CAS_IN_FILT_5V
+5V +3.3V
U11
VCCB VCCB VCCA VCCA
<-BI->
PD0_5V 2 1B0 47 PD0_3V3
PD1_5V 3 1B1 46 PD1_3V3
PD2_5V 5 1B2 44 PD2_3V3
PD3_5V 6 1B3 43 PD3_3V3
PD4_5V 8 1B4 41 PD4_3V3
PD5_5V 9 1B5 40 PD5_3V3
PD6_5V 11 1B6 38 PD6_3V3
PD7_5V 12 1B7 37 PD7_3V3
RnW_5V 1 1DIR 48 DATA_EN_N
CLOCK_IN_5V 13 2B0 36 CLOCK_IN_3V3
CLOCK_IN_RES_5V 33 KBD1_5V 14 2B1 35 KBD1_3V3
KDB2_5V 16 2B2 33 KDB2_3V3
KDB3_5V 17 2B3 32 KDB3_3V3
RnW_5V 19 2B4 30 RnW_3V3
nPOR_5V 20 2B5 29 nPOR_3V3
A15_5V 22 2B6 27 A15_3V3
CAS_IN_FILT_5V 23 2B7 26 CAS_IN_3V3
24 2DIR 25
8B8O-74ALVC164245DGG:11
IN->
1A0 1A1 1A2 1A3 1A4 1A5 1A6 1A7 1OE#
2A0 2A1 2A2 2A3 2A4 2A5 2A6 2A7 2OE#
GND GND GND GND GND GND GND GND
39 34 28 21 15 10 4 45
GND
U4.1
ICE40HX1K-VQ100
RAM2_3V3 51 IOR_52
RAM3_3V3 52 IOR_53
PD0_3V3 53 IOR_54
PD1_3V3 54 IOR_55
PD2_3V3 56 IOR_56
PD3_3V3 57 IOR_57
PD4_3V3 59 IOR_58
PD5_3V3 60 IOR_59
PD6_3V3 62 IOR_60_GBIN3
63 IOR_61_GBIN2
PD7_3V3 64 IOR_63
KBD1_3V3 65 IOR_64
KDB2_3V3 66 IOR_65
KDB3_3V3 68 IOR_67
RnW_3V3 69 IOR_68
nPOR_3V3 71 IOR_69
A15_3V3 72 IOR_70
CAS_IN_3V3 73 IOR_71
DATA_EN_N 74 IOR_72
BANK 1
J5
CAS_IN_3V3
J9
B1-74
U13.4
ElectronULA_2
nRAS 52 nRAS_5V_B
nCAS 53 nCAS_5V_B
nPOR 54 nPOR_5V_B
DIV13_IN 55
A15 56 A15_5V_B
nNMI 57 nNMI_5V_B
nRST 58 nRST_5V_B
CAS_IN 59 CAS_IN_5V_B
PHI_OUT 60 PHI_OUT_RES_5V_B
nROM 61 nROM_5V_B
SOUND_OP 62 SOUND_OP_5V_B
CAPS_LOCK 63 CAPS_LOCK_5V_B
CAS_MO 64 CAS_MO_5V_B
nCSYNC 65 nCSYNC_5V_B
BLUE 66 BLUE_5V_B
nHS 67 nHS_5V_B
GND 68
GND
J12
ULA-ADP-A4
nRAS_5V 1 2 nCAS_5V
nPOR_5V 3 4 nNMI_5V
A15_5V 5 6 CAS_IN_5V
nRST_5V 7 8 nROM_5V
PHI_OUT_RES_5V 9 10 CAPS_LOCK_5V
SOUND_OP_5V 11 12 nCSYNC_5V
CAS_MO_5V 13 14 nHS_5V
BLUE_5V 15 16 RA1_5V
17 18 nWE_5V
RA0_5V 19 20
GND
J16
ULA-ADP-B4
nRAS_5V_B 1 2 nCAS_5V_B
nPOR_5V_B 3 4 nNMI_5V_B
A15_5V_B 5 6 CAS_IN_5V_B
nRST_5V_B 7 8 nROM_5V_B
PHI_OUT_RES_5V_B 9 10 CAPS_LOCK_5V_B
SOUND_OP_5V_B 11 12 nCSYNC_5V_B
CAS_MO_5V_B 13 14 nHS_5V_B
BLUE_5V_B 15 16 RA1_5V_B
17 18 nWE_5V_B
RA0_5V_B 19 20
GND
PHI_OUT_RES_5V
R20
100
+3.3V +5V +3.3V
U7
VCCB VCCB VCCA VCCA
<-OUT
CAS_OUT_5V 2 1B0 47 CAS_OUT_3V3
nRAS_5V 3 1B1 46 nRAS_3V3
nCAS_5V 5 1B2 44 nCAS_3V3
PHI_OUT_5V 6 1B3 43 PHI_OUT_3V3
nROM_5V 8 1B4 41 nROM_3V3
SOUND_OP_5V 9 1B5 40 SOUND_OP_3V3
CAPS_LOCK_5V 11 1B6 38 CAPS_LOCK_3V3
CAS_MO_5V 12 1B7 37 CAS_MO_3V3
1 1DIR 48
nCSYNC_5V 13 2B0 36 nCSYNC_3V3
BLUE_5V 14 2B1 35 BLUE_3V3
nHS_5V 16 2B2 33 nHS_3V3
RA1_5V 17 2B3 32 RA1_3V3
RA0_5V 19 2B4 30 RA0_3V3
nWE_5V 20 2B5 29 nWE_3V3
22 2B6 27
23 2B7 26
24 2DIR 25
<-OUT
16I-74ALVC164245DGG:11
1A0 1A1 1A2 1A3 1A4 1A5 1A6 1A7 1OE#
2A0 2A1 2A2 2A3 2A4 2A5 2A6 2A7 2OE#
GND GND GND GND GND GND GND GND
39 34 28 21 15 10 4 45
GND
J7
5V_OUT_B22-B23
J6
3V3_OUT_A27-A26
U4.5
ICE40HX1K-VQ100
CAS_OUT_3V3 78 IOT_73
nRAS_3V3 79 IOT_74
nCAS_3V3 80 IOT_75
PHI_OUT_3V3 81 IOT_77
nROM_3V3 82 IOT_78
SOUND_OP_3V3 83 IOT_79
CAPS_LOCK_3V3 85 IOT_80
CAS_MO_3V3 86 IOT_81
nCSYNC_3V3 87 IOT_82
BLUE_3V3 89 IOT_84_GBIN1
nHS_3V3 90 IOT_85_GBIN0
RA1_3V3 91 IOT_86
RA0_3V3 93 IOT_87
nWE_3V3 94 IOT_88
nRST_IN_3V3 95 IOT_89
nRST_OUT_3V3 96 IOT_90
nIRQ_3V3 97 IOT_91
nNMI_3V3 99 IOT_93
100 IOT_95
BANK 0
J3
B0-95
TITLE:
ULA2
REV: 1.0
Company: Chris Jamieson
Sheet: 1/1
Date: 2022-08-12
Drawn By: Chris Jamieson
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