80386

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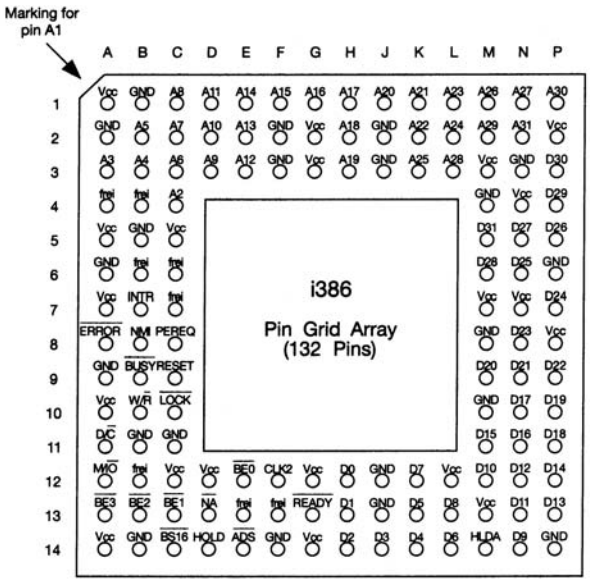
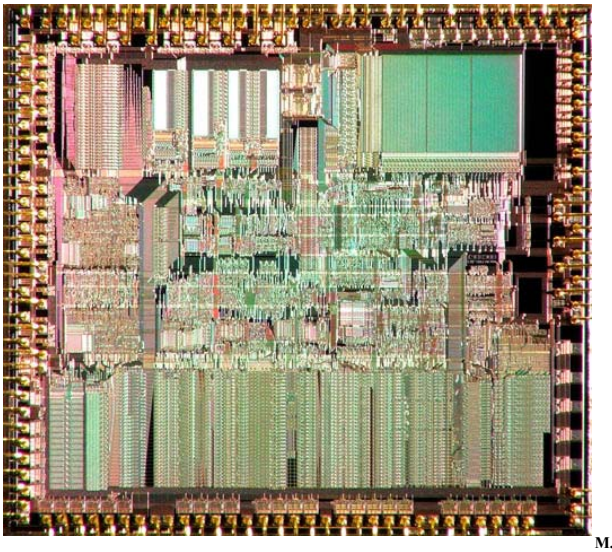
General information

- **First released in 1985**
- **Composed of about 275,000 transistors**
- **32-bit microprocessor**
- **32-bit registers**
- **16-byte prefetch queue**
- **Memory Management Unit (MMU) supporting segmentation and paging**
- **32-bit data and address busses**
- **Real, protected and virtual modes.**

Pinout



Layout

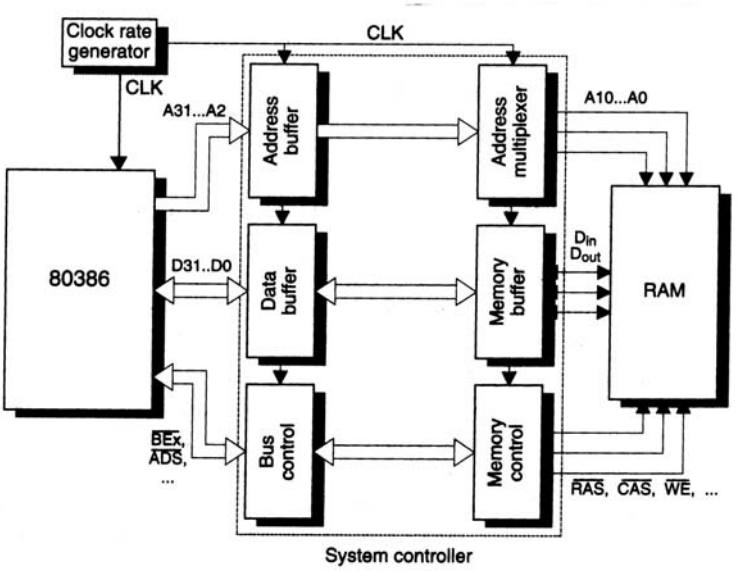


The bus controller

All the bus control signals are generated by the bus controller, which reads the status signals generated by the processor.

The bus controller also contains a number of buffers.

Processor/memory interface



Bus cycle

Every bus cycle requires at least 2 PCLK cycles, (corresponding to 4 CLK2 cycles) denoted by

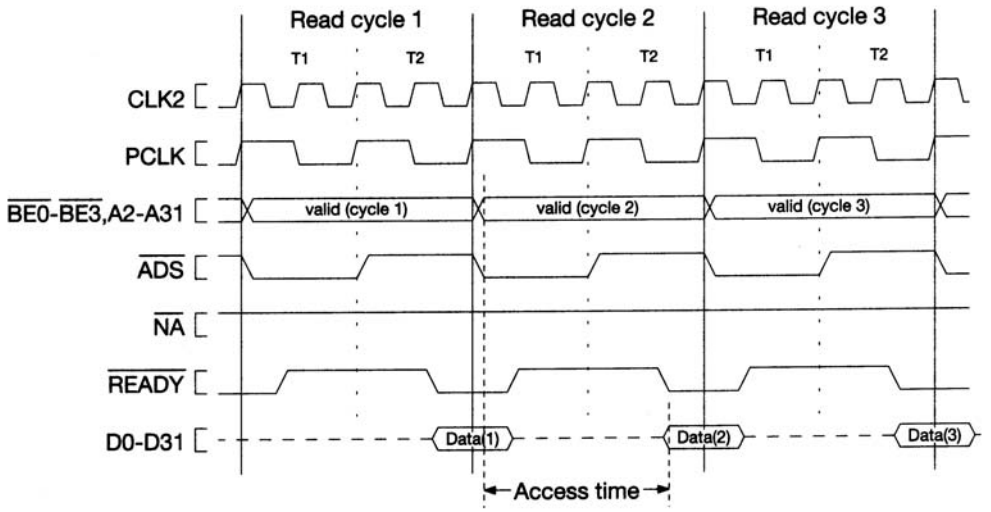
- **C1 (*status cycle*): the control and address signals are issued**
- **C2 (*command cycle*): the data transfer is executed.**

Bandwidth

A 40 Mhz 80386 can perform 20 million bus cycles per second.

Since the data bus is 32 bits-wide, the maximum bandwidth of 80386 is *80Mb/s*.

Read cycle



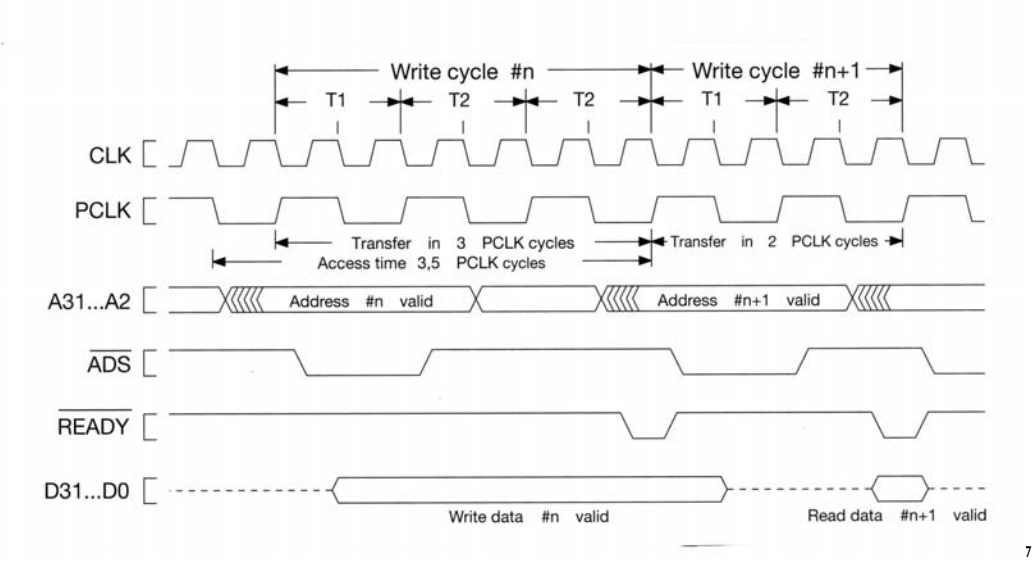
Wait states

If the memory or peripheral chip cannot conclude a read or write operation within the two PCLK periods,

- **the memory controller holds the READY signal high, and**
- **the 80386 implements another C2 cycle.**

The mechanism is iterated until the memory controller lowers the READ signal.

Wait states



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Address pipelining

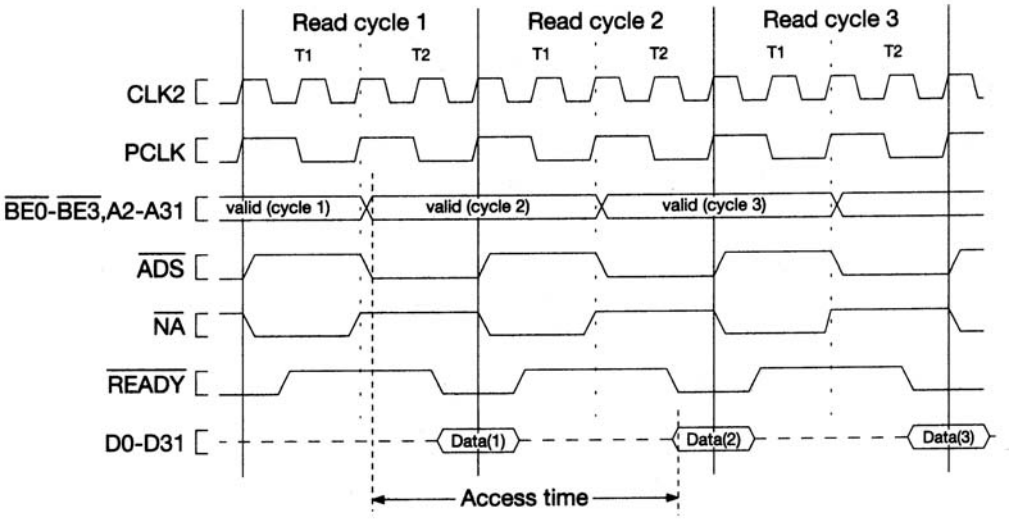
To give memory and ports more time, the 80386 can issue the address for an access during the C2 cycle of the previous bus cycle.

In this way, the address is transferred to the address decoding logic while the memory is performing the data transfer.

Therefore, each bus cycle lasts for 3 PCLK cycles, but the whole effect is that it is seen to last for 2 PCLK cycles.

Address pipelining is activated by the NA control signal.

Read cycle with address pipelining



Double word boundary

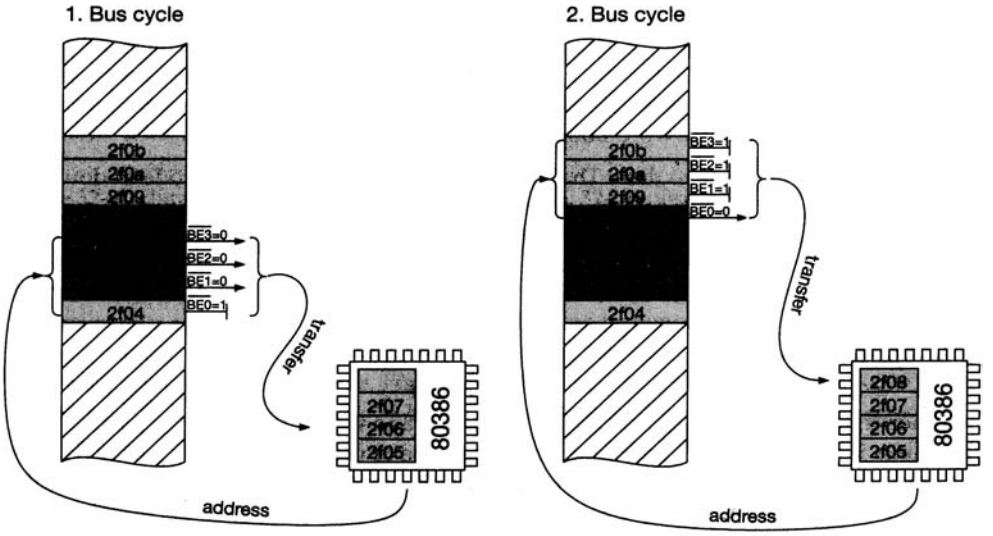
In a 80386 the RAM is normally organized as 32-bit memory, and can read/write a 32-bit word to/from the data bus in one bus cycle.

However, in some cases it is necessary to read/write data with a shorter length.

Signals BE0 to BE3 inform the outside on which bytes (out of the 4) are meaningful.

If a misaligned double word must be accessed, the processor automatically splits this operation over two bus cycles, generating the correct address and control signals.

Access to a misaligned double word



Support for 16- and 32-bit busses

The i386 is able to simultaneously support 16-bit and 32-bit data transfers.

For example, the processor can communicate over a 32-bit data bus with RAMS and over a 16-bit data bus with peripherals.

Using the BS16 pin, the single bus cycle can implement either a single 32-bit data transfer, or a couple of 16-bit data transfers. All the control signals are correctly driven.

I/O cycles

The 80386 supports both isolated I/O and memory mapped I/O.

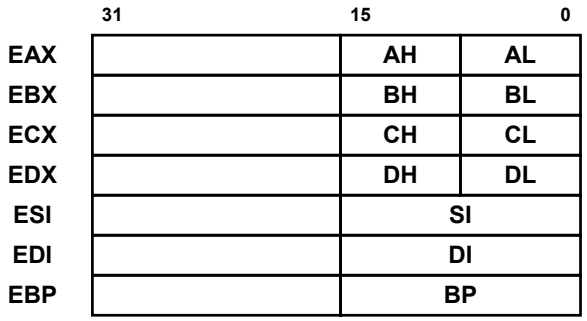
In the first case, the I/O space spans the addresses from 0 to 65,536.

I/O cycles are identical to memory cycles, apart from the value of the M/IO signal.

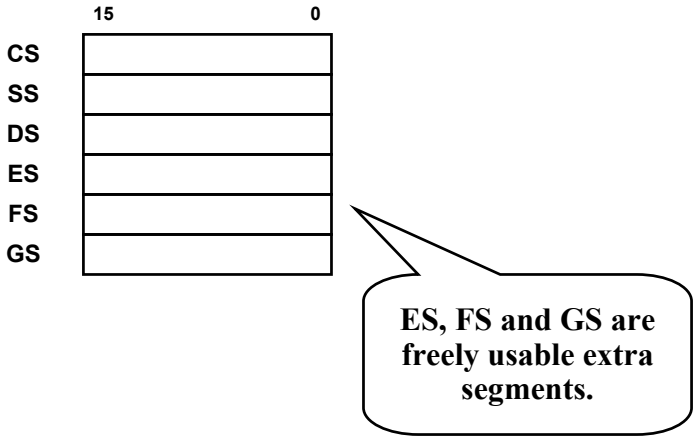
Registers

Most of the i386 registers are 32-bit large; for sake of compatibility with previous Intel processors, they can also be accessed as 16-bit registers.

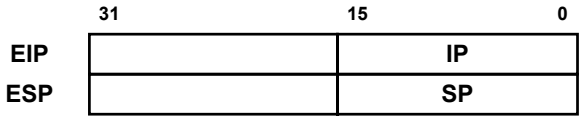
General-purpose registers



Segment registers



Instruction counter/stack pointer



Flag register