# Pentium Pro

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# Introduction

**The Pentium Pro (also known as P6) was introduced by Intel in 1995.**

**Intel integrated the CPU (5.5. million transistors) and the L2 cache (2 million transistors) into a single package (*cartridge*) composed of two dies.**

**The two parts are connected by a dedicated bus running at the full CPU speed (200 MHz).**

**Significant power consumption problems were raised by the new device.**

**Several important advances from the architectural point of view were also introduced.**

# Pipeline

**It is composed of 12 stages. Individual stages are simpler, thus allowing an increase in the clock frequency.**

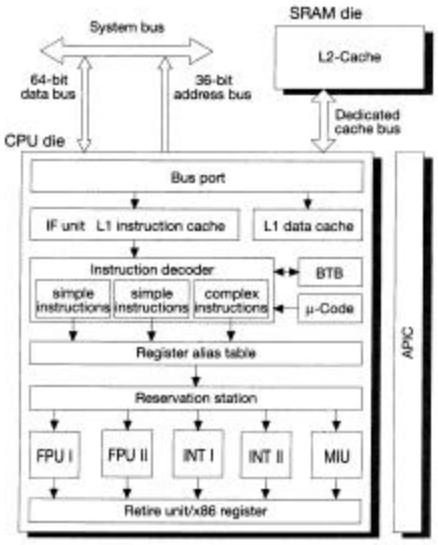
**Due to its length, it requires**

- **A very effective branch prediction mechanism**
- **An efficient instruction scheduling.**

**Intel claims that a sustained execution rate of 3 instructions/clock cycle can be attained.**



# Architecture



# L1 caches

**Both the data and instruction caches have some common characteristics**

- **8 Kb size**
- **2-way set-associative.**

**The data cache has two access ports, thus reducing conflicts. It fully supports the MESI protocol.**



# Decoding unit

**It fetches one cache line (32 bytes) per clock cycle from the L1 code cache.**

**It identifies instruction boundaries, and performs branch prediction.**

**It is composed of 3 units working in parallel: two for simple instructions and one for complex instructions.**

**Simple instructions are mapped to single m-ops. Complex instructions are mapped to several m-ops (up to 4).**

**The decoding stage can thus produce up to 6 m-ops per clock cycle, which are then written to the *instruction pool*.**

# Instruction pool

**It stores up to 20/30 m-ops.**

**It continuously checks which m-ops can be sent to the functional units.**

**m-ops can be sent to functional units in any order.**



# Branch prediction

**It is based on a BTB storing information about 512 branches.**

# Register alias table

**It converts references to x86 registers to references to the 40 internal registers of the Pentium Pro, thus performing *register renaming*.**



# Execution units

**They are**

- **Two units for FP instructions (FPUI, FPUII)**
- **Two units for integer instructions (INTI, INTII)**
- **One memory interface unit (MIU).**

**The 5 units can operate in parallel and independently.**

# Retire unit

**It continuously looks in the instruction pool for completed instructions.**

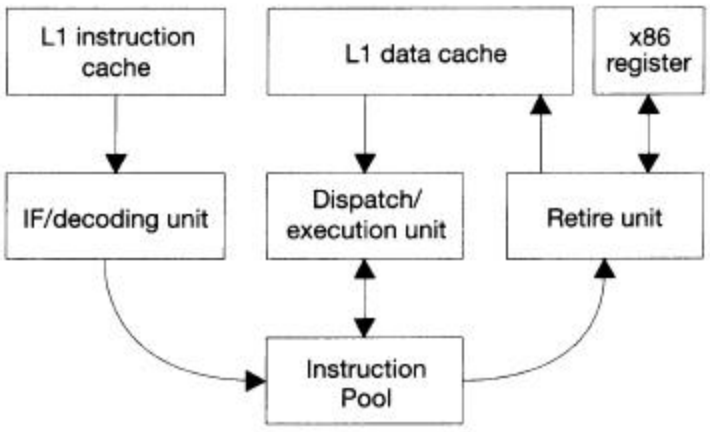
**Retirement happens according to a strict in-order strategy.**

**As soon as it becomes possible, it performs**

- **Data dependencies resolution**
- **Branch prediction verification**
- **Real register updating.**



# Flow of execution



# L2 cache

**It is connected to the CPU through a 64-bit bus working at the CPU speed.**

**It stores both data and code.**

**It is 4-way set-associative with a total size of 256 Kb or 512 Kb.**



# Conditional instructions

**To reduce the number of pipeline stalls, two conditional MOV instructions are supported:**

- **`CMOVcc` (conditional move)**
- **`FCMOVcc` (conditional FPU move).**

# Extended address bus

**The Pentium Pro address bus can be either 32- or 36-bit wide.**

**The size depends on the value of the PAE bit in the CR4 register.**



# Multiprocessing

**The Pentium Pro is particularly suited for multiprocessing.**

**Up to 4 Pentium Pros can be connected and work together without the need for additional logic.**

**A suitable bus arbitration mechanism is devised for this purpose.**

# Pentium II

**It was first introduced in 1997.**

**It supports MMX technology.**

**It includes 7.7 million transistors and is again shipped in a cartdridge including the L2 cache.**

**L1 caches have 16 Kb size, each.**



# Pentium III

**It was first introduced in 1999 and includes 9.5 million transistors.**

**It supports 72 new instructions known as *Internet Streaming Single Instruction Multiple Data Extension* (ISSE), which extend MMX technology to FP operations.**

**It supports an identification code of every single CPU.**

# Pentium IV

**It was first released in 2000 and incorporates 42 million transistors.**

**Its initial frequency is 1.5 GHz.**