Chipsets

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Introduction

The motherboard of the first PC systems (up to 286 systems) was composed of several (up to some tens) of components.

Thanks to the great advances in semiconductor technology, starting from the mid '80s it was possible to integrate all these components on a few chips.

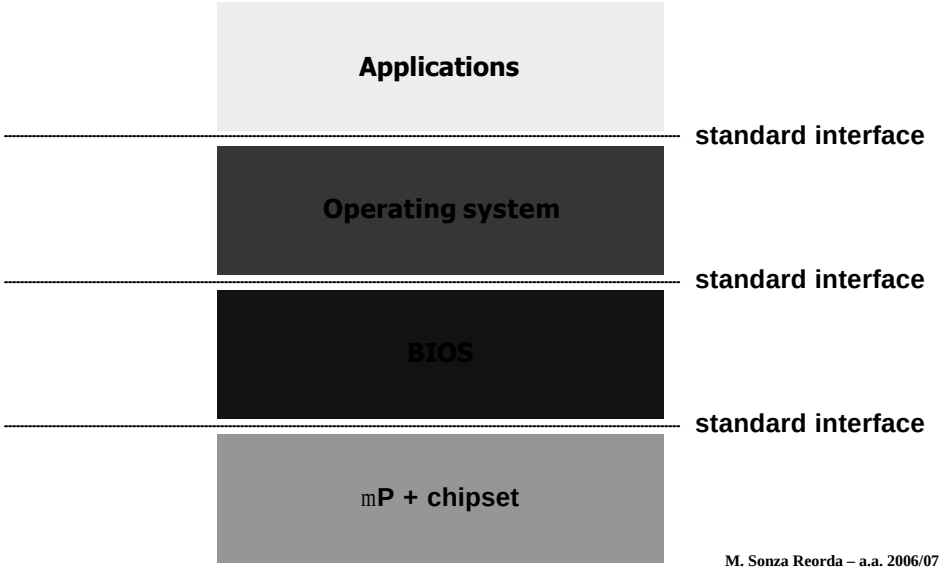
The set of chips developed to ease the design of a motherboard with a given processor is known as *chipset*.

Chipset SW compatibility

Chipsets are not compatible one with the other (in terms of supported functions, architecture, and signals), but the resulting motherboard must always be able to run the software developed for previous boards.

This is possible because for every chipset a proper low-level layer of the OS (e.g., the BIOS) is developed.

HW/SW layers



Chipset characteristics

Normally, a chipset is specifically designed for a given processor.

However, some non-Intel processors can integrate with Intel chipsets, since they exactly replace the Intel processor.

Chipset functions

They include

- **Cache support**
- **Memory support**
- **Timing and flow control**
- **Peripheral and I/O bus control**
- **Power management support.**

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Chipsets normally includes all the logic to manage external caches.
Chipset design defines the amount of *cachable memory*, which also depends on the size of the tag RAM.

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Chipsets differ in terms of amount and type of supported memory.

Chipse

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- Peripheral and I/O bus control
- Power management support.

It is up to the chipset to
- Generate the correct control signals for accessing the memory
- Possibly perform buffering of data from/to the processor
- Detect the amount and type of existing memory, and generate suitable signals to manage it (e.g., requesting wait states).

Chipse

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- Cache support
- Memory support
- Timing and flow control
- Peripheral and I/O bus control
- Power management support.

Chipsets normally include:
- A DMA controller
- Bridges, to connect with other busses (e.g., PCI/EISA)
- A couple of interrupt controllers
- Interface to USB
- Interface to AGP.

Chipse

Most recent chipsets support a group of features aimed at reducing the amount of power used by the PC during idle periods.
Power management works through a number of settings that dictate when to shut down various parts of the computer (e.g., the video, or the hard disk) when it becomes idle.

They include

- Cache support
- Memory support
- Timing and flow control
- Peripheral and I/O bus control
- Power management support.

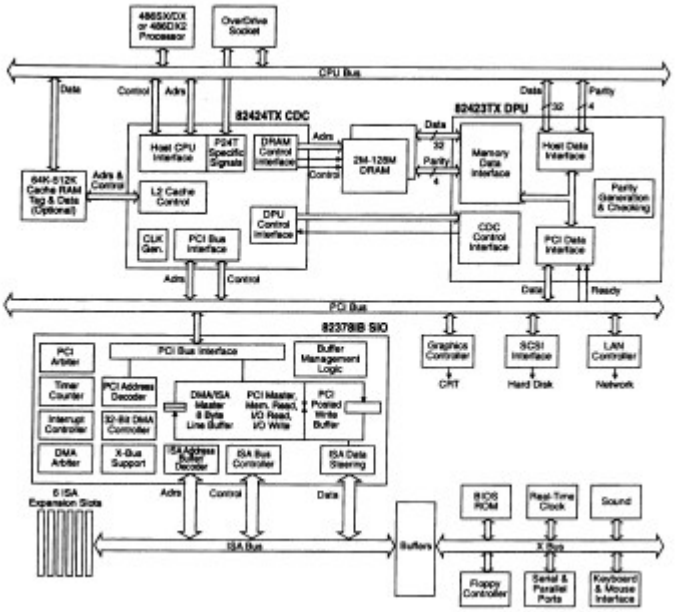
The Saturn chipset

It was developed by Intel for 486 CPUs.

It is composed of 3 chips:

- 82424TX: Cache/DRAM Controller (CDC)
- 82423TX: Data Path Unit (DPU)
- 82378IB: System I/O (SIO).

A PC based on the Saturn chipset



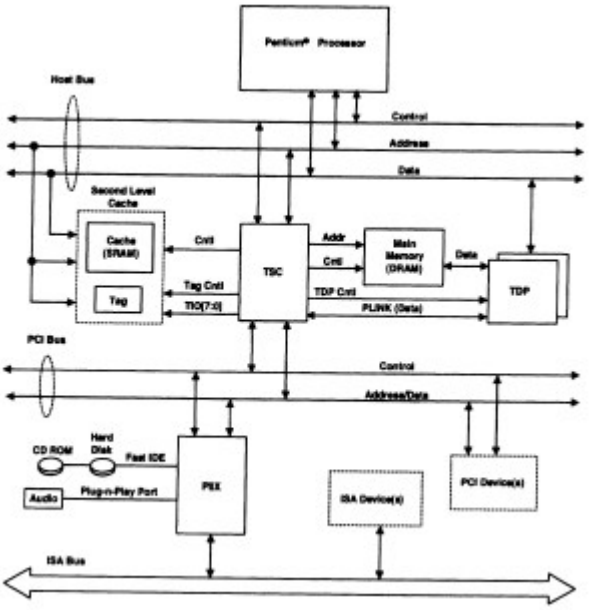
The Triton chipset

It was the second chipset released (1995) by Intel for the PCI Pentium systems, after the unsuccessful Mercury chipset.

The Triton chipset is composed of

- **S82437FX: Triton System Controller (TSC)**
- **S82438FX: Triton Data Paths (TDP)**
- **S82371FB: PCI ISA IDE Xcelerator (PIIX).**

A PC based on the Triton chipset



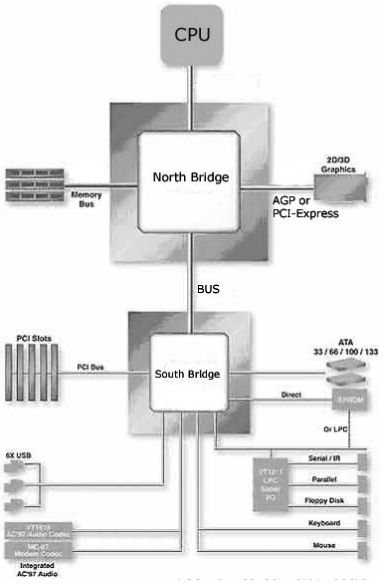
Triton chipset evolution

Data	430FX	430HX	430VX	430TX
System Controller	82437FX	82439HX	82437VX	82439TX
Data Path Unit	82438FX	in 82439HX	82438VX	in 82439TX
Maximum memory	128 Mb	512 Mb	128 Mb	256 Mb
Max. L2 cache	512 Kb	512 Kb	512 Kb	512 Kb
Cacheable area	64 Mb	512 Mb	64 Mb	64 Mb
USB support	no	yes	yes	yes
SDRAM support	no	no	yes	yes
Ultra DMA/33	no	no	no	yes
IDE Xcelerator	PIIX (82371FB)	PIIX3 (82371SB)	PIIX3 (82371SB)	PIIX4 (82371AB)
PCI specification	2.0	2.1	2.1	2.1

Current chipsets

The current Intel chipsets are based on two devices:

- **The North bridge**
- **The South bridge.**



North bridge

It is also called MCH (*Memory Controller Hub*).

It is connect directly to the CPU and has basically the following functions:

- **Memory controller**
- **AGP bus controller (if available)**
- **PCI Express x16 controller (if available)**
- **Interface for data transfer with south bridge.**

In these systems, the CPU does not directly accesses the RAM memory or the video card, and it is the north bridge that accesses these devices. Because of that, the north bridge chip has an ultimate role in the computer performance.

Since the memory controller is in the north bridge, it is this chip that limits the types and maximum amount of memory in the system.

South bridge

It is also called ICH (*I/O Controller Hub*).

It is connected to the north bridge and is basically in charge of controlling I/O devices and on-board devices, such as:

- **Hard disk drive ports (Parallel and Serial ATA ports)**
- **USB ports**
- **On-board audio**
- **On-board LAN**
- **PCI bus**
- **PCI Express lanes (if available)**
- **Real time clock (RTC)**
- **CMOS memory**
- **Legacy devices like interrupt controller and DMA controller.**

South bridge (II)

The south bridge is also connected to two other chips available on the motherboard:

- **the ROM chip storing part of the BIOS**
- **the Super I/O chip, which is in charge of controlling legacy devices like serial ports, parallel port and floppy disk drive.**

South bridge (III)

The south bridge is not so critic to performance as the north bridge.

It can have some influence on hard disk drive performance:

- **It is the south bridge that sets the number (and speed) of USB ports and the number and types (regular ATA or Serial ATA) of hard disk drive ports that the motherboard has, for example.**

Inter-bridge communication

When the bridge concept started to be used, the communication between the north bridge and the south bridge was done via PCI.

The bandwidth available for the PCI bus (132 MB/s) was shared between all PCI devices in the system and devices hooked to the south bridge (especially hard disk drives).

At that time, this was not a problem, since hard drives maximum transfer rates were of 8 MB/s and 16 MB/s.

Inter-bridge communication (II)

When high-end video cards (at that time, the video cards were PCI) and high-performance hard disk drives were launched, a bottleneck situation arouse.

As an example, modern ATA/133 hard disk drives have the same theoretical maximum transfer rate as the PCI bus.

In theory, an ATA/133 hard drive would thus use the entire bandwidth, slowing down the communication speed of all devices connected to the PCI bus.

AGP

For the high-end video cards, the solution was the creation of a new bus connected directly to the north bridge, called AGP (*Accelerated Graphics Port*).

Inter-bridge communication (III)

The general solution was to use a dedicated high-speed bus between north and south bridges and connecting the PCI bus devices to the south bridge.

Figure 6

Inter-bridge communication (IV)

The speed of this dedicated bus depends on the chipset model. For example, on the Intel 925X chipset this bus has a maximum transfer speed of 2 GB/s.

The chipset manufacturers call this bus with different names:

- **Intel: DMI (Direct Media Interface) or Intel Hub Architecture**
- **ULi/ALi: HyperTransport**
- **VIA: V-Link**
- **SiS: MuTIOL**
- **ATI: A-Link or PCI Express.**

AMD chipsets

AMD decided to integrate the functions of the North bridge directly in the processor.

Therefore, the chipset is only composed of the South bridge.