Memory

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Introduction

PC systems normally includes

- **DRAM, implementing the main memory**
- **SRAM, implementing the external cache.**

The management of both these memories requires a suitably implemented memory controller.

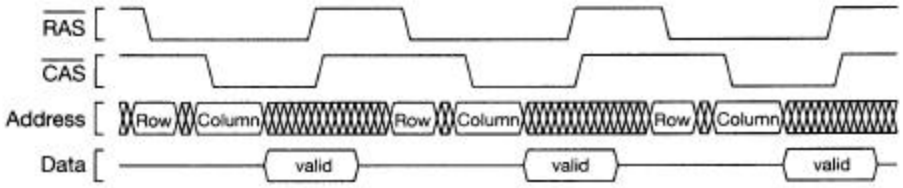
DRAM

Internally, a DRAM is normally organized as a matrix.

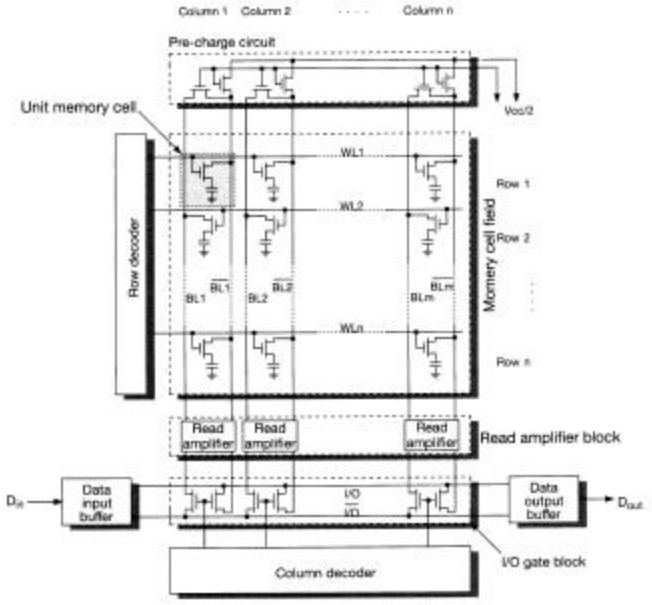
Accordingly, the address is often split in a row address and a column address.

The strobe signals controlling the transfer of the row/column address are denoted RAS and CAS, respectively.

Read access



Internal organization



Precharging

Before a cell access, the precharge circuit charges all bit line pairs up to the same value Vcc/2. This requires a certain time, named *RAS precharge time*.

Once this operation is completed, the proper word line is activated, and the sense amplifiers detect and amplify any difference in the bit lines.

Refresh

A refresh cycle is normally required every 1 to 16 ms, depending on the RAM type.

Three strategies are normally used for refreshing

- **RAS-only refresh**
- **CAS before RAS refresh**
- **Hidden refresh.**

RAS-only refresh

It is based on sending to the DRAM all the possible row addresses, each strobed with the proper RAS signal, without sending any column address.

In this way, the DRAM internally reads (and amplifies) the value of every row, without producing any data.

In the PC this is carried out by channel 0 of the 8237 DMA chip, which is periodically activated by counter 1 of the 8253/8254 timer chip and issues a dummy read cycle.

CAS-before-RAS refresh

For normal operations, first the RAS signal is activated (while the row address is given), and then the CAS signal is activated (while the column address is given).

Some DRAM chips have their own refresh logic (including a refresh counter).

To activate this logic, the CAS signal must be activated for a certain time period before RAS also drops. The refresh of a whole row is then performed, and the internal counter incremented.

Hidden refresh

The refresh cycle is activated after a read cycle by holding the CAS signal down for a longer time, and switching up and down the RAS signal, only,

The internal refresh circuitry performs the refresh by updating the refresh counter.

Since the time required for a refresh cycle is usually shorter than that for a read cycle, this refresh type saves time.

Page mode

Page mode can be exploited when two or more accesses are made, referring to locations having the same row address.

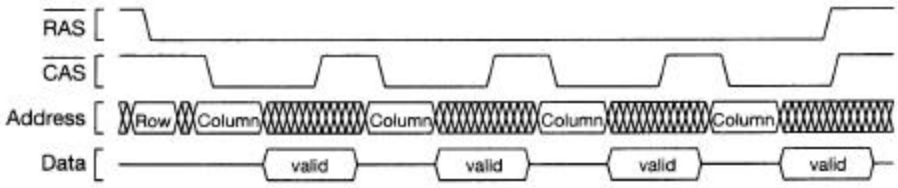
In this case, the row address (and the corresponding RAS signal) is given only once, and only the column address is provided (together with the CAS signal).

Read and write operations can be mixed while accessing to the same page in page mode.

A maximum number of consecutive operations in page mode is often defined.

Memories supporting page mode are normally called Fast Page Mode (*FPM*) DRAM.

Read access in page mode



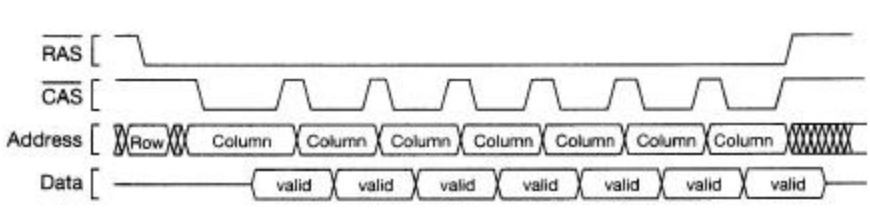
Advantages

Several advantages can be obtained using this mode:

- **the access time can be reduced up to 50%**
- **the cycle time can be reduced up to 70%.**

EDO mode

In hyper page (or Extended Data Out, EDO) mode, column address can be provided with higher frequency (usually 30% higher).



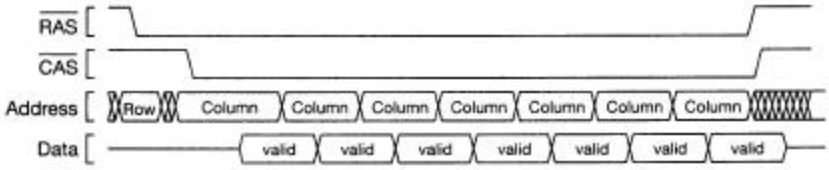
Static-column mode

It is a modified version of page mode, where the CAS signal does not need to be switched up and down while providing the column address.

The DRAM control logic detects the column address and accesses the new data.

This results in lower access and cycle time.

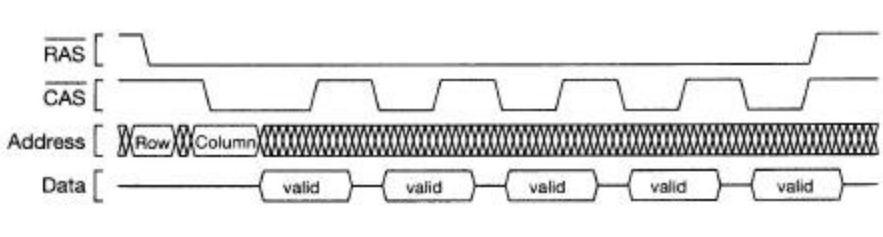
This mode is only used in some IBM PS72 models.



Serial mode

After the first access (when the row and column addresses are provided), the CAS signal is switched up and down rapidly, and each time one bit is shifted out.

This can be useful for accesses performed by CRTs.



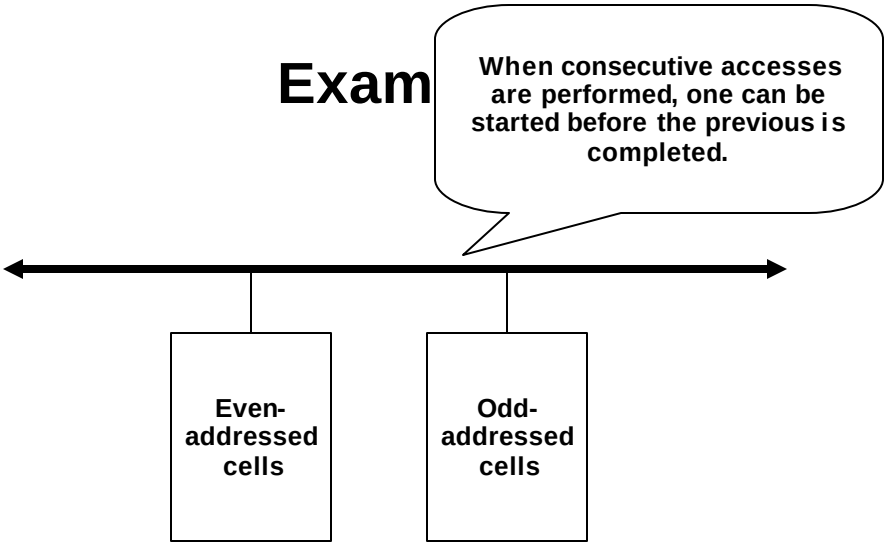
Interleaving

It can speed-up sequential accesses to memory.

It is based on dividing the memory words among several banks and accessing them alternatively.

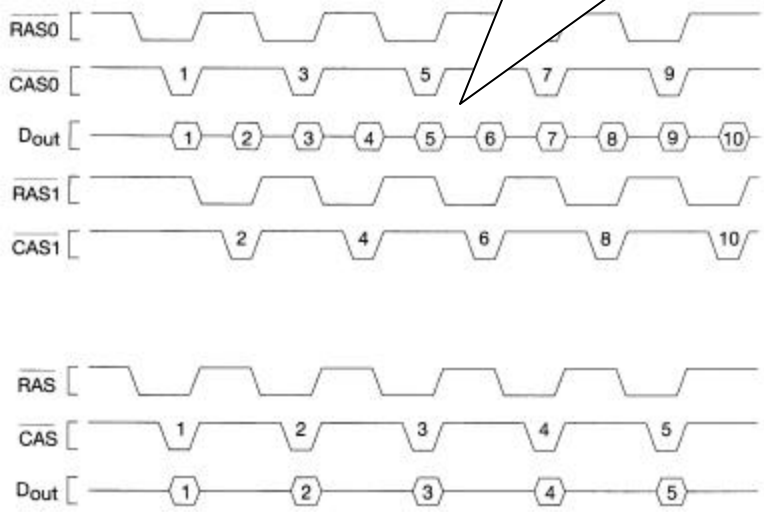
In this way the access time to different banks can be partly overlapped.

Exam

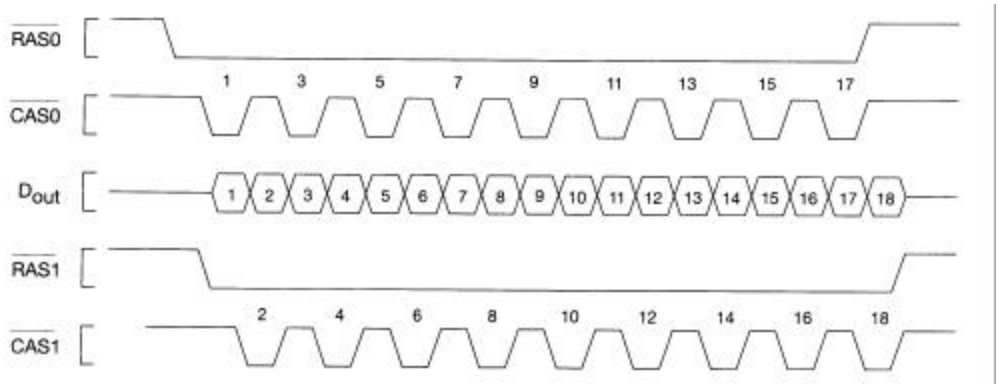


2-way inte

The access time is reduced.



2-way interleaving with page mode



Memory controller importance

It is up to the memory controller to understand

- **Whether a sequence of memory accesses refers to the same page, and thus enter page mode**
- **Whether the sequence alternates between odd and even addresses, and thus interleaving can be adopted.**

If neither of the two techniques can be adopted, it is up to the memory controller to ask for wait states.

SDRAM

FPM and EDO memories can hardly work within systems running at more than 75 MHz.

Over this threshold, *Synchronous DRAMs* (SDRAMs) are normally used; their access time can be in the range 50 ¸ 60 ns.

SDRAMs are connected to the system clock and work without waiting states.

Internally, they often exploit interleaving.

Apart from being synchronous, they work similarly to other memories, and support page mode in the same way.

DDR SDRAM

Double Data Rate SDRAM **double the bandwidth of the memory by transferring data twice per cycle, i.e., on both the rising and falling edges of the clock signal.**

Rambus DRAM

Rambus DRAM works more like an internal bus than a conventional memory subsystem.

It is based around what is called the *Direct Rambus Channel*, a high-speed 16-bit bus running at a clock rate of 400 MHz.

As with DDR SDRAM, transfers are accomplished on the rising and falling edges of the clock, yielding an effective theoretical bandwidth of approximately 1.6 Gbytes/second.

They have been first developed by a company named *Rambus*, and then adopted by Intel starting from the Camino chipset.

SRAMs

Their access time is approximately 8 to 20 ns.