· Content

1. Introduction

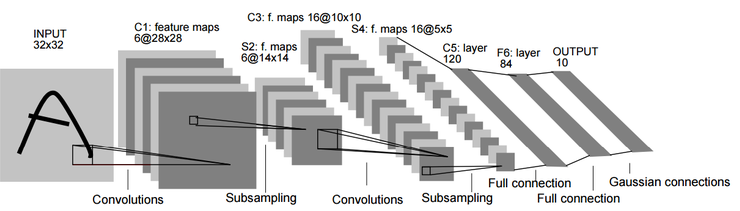
2. Block design / FSM

3. Address Map

1. Introduction

1) Convolutional Neural Network

The name “convolutional neural network” indicates that the network employs a mathematical operation called convolution. convolution is a specialized kind of linear operation. convolutional networks are simply neural networks that use convolution in place of general matrix multiplication in at least one of their layers.



2-1) CNN controller

We must consider Padding, Stride, Filter(Kernel) size. If padding, In Read state, Input data will be 0 when edge of image input. Our input image size is 224x224. when padding operates, input image size is 226x226 and we can check padding location by conditional logic. Stride and filter(kernel) size will affect in Convolution State.

1. Introduction

2-2) Condition

1) assumed ARM interface code and BRAM data are already exist.

2)　Input data and Weight data are changed 32bit floating point to

16bit fixed point.

3) Using three block memories.

4) Need to consider kernel size, stride, padding.

2. Block design / FSM

1) CNN controller (FSM)

Finite State Machine (IDLE)

· properties

1) start signal

2) enable signal

3) read done signal

4) conv done signal

5) done signal

· IDLE state properties

When Finite State Machine starts, First state is IDLE, means waiting

next state signal and doing nothing. If start signal goes high level, state will be next stage, READ.



2. Block design / FSM

1) CNN controller (FSM)

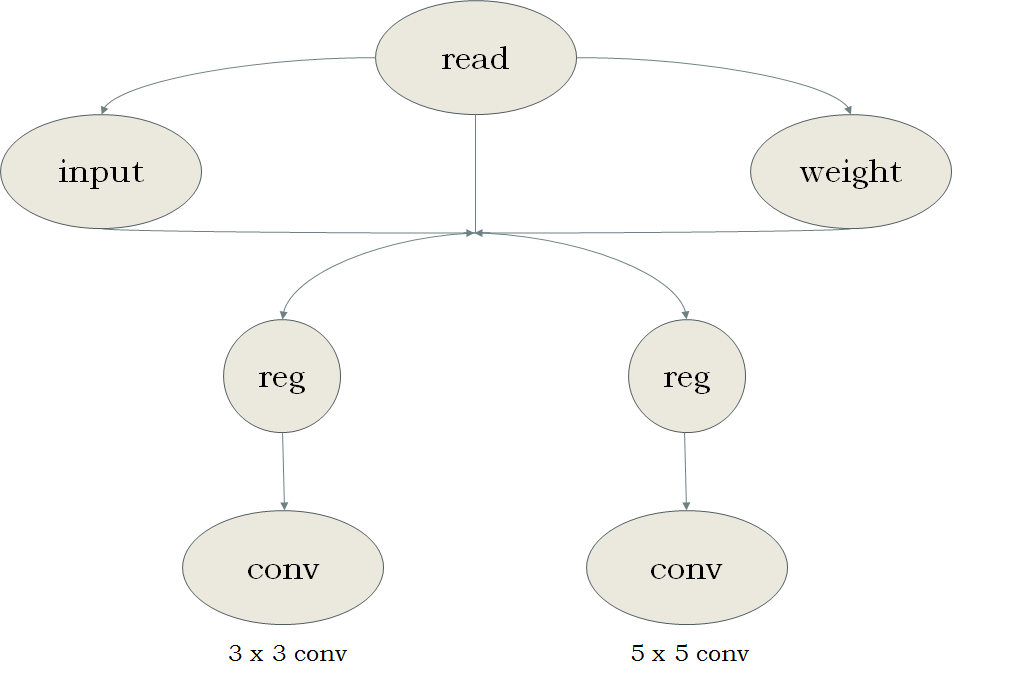
Finite State Machine (READ)

· READ state Properties

When start signal is high level , Read state begins. In Read

state, Finite state Machine send enable signal and address to

BRAM Input and Weight and register (choose 3x3 or 5x5 filter). it will read input data and weight data and register data. When all of data is read, it will send enable signal and then Read state will be done ,

read done signal goes high level.

2. Block design / FSM

1) CNN controller (FSM)

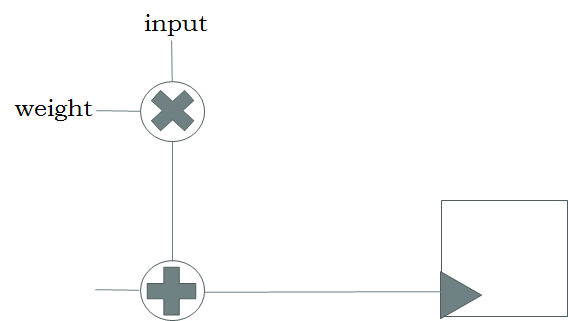
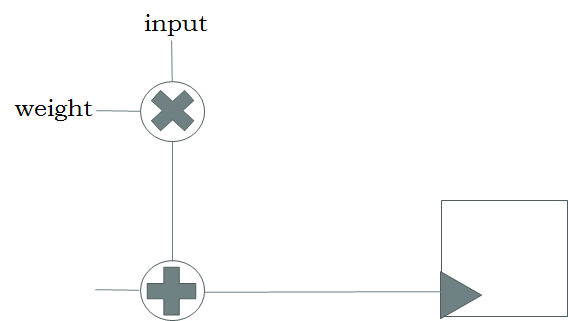
Finite State Machine (CONV)

· CONV state Properties

When read done signal is high level, convolution state begins. if convolution state begin, Input data multiplies to Weight data in

PE module. output data of PE module,send result register and saved.

When convolution state is done, conv signal goes high level.



2. Block design / FSM

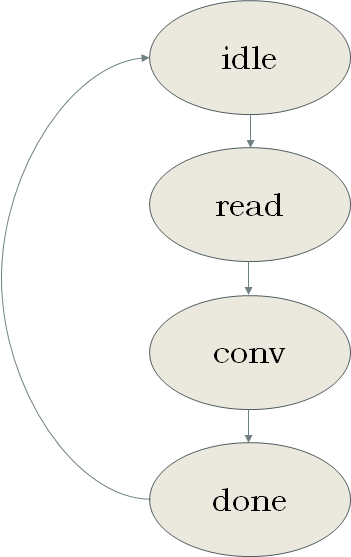
1) CNN controller (FSM)

Finite State Machine (DONE)

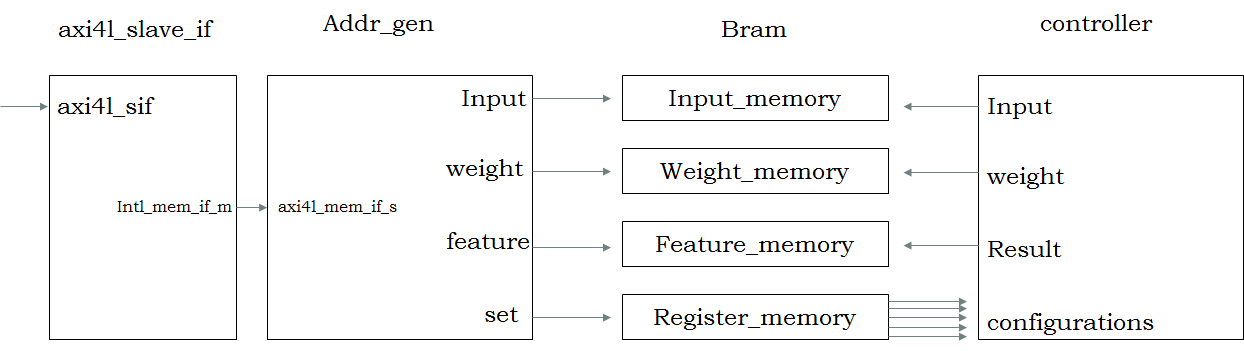
· DONE state Properties

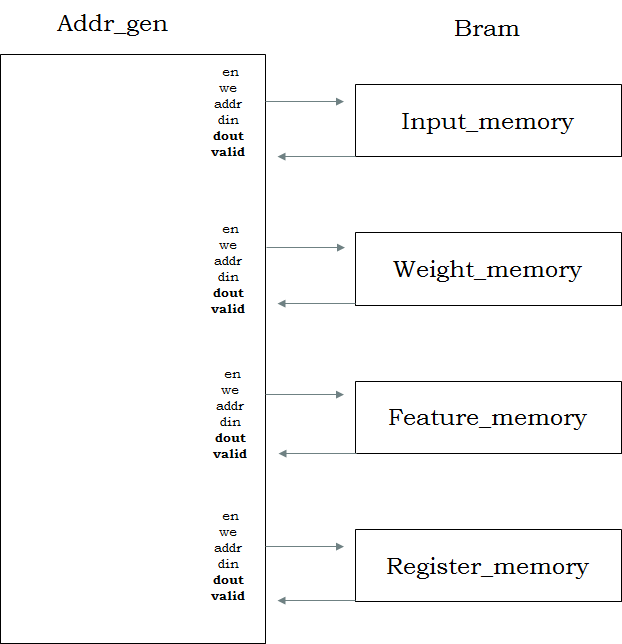
When conv signal is high level, done state begins. if done state begin, data of result register will be written and saved in BRAM\_Result memory, done signal goes high level and change the

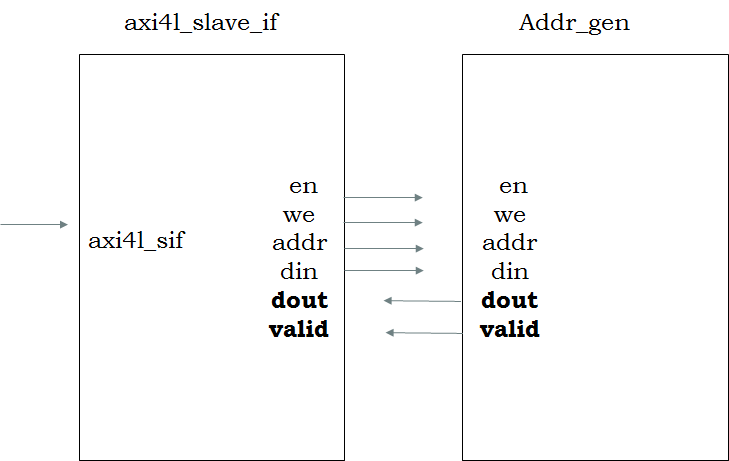
state to IDLE

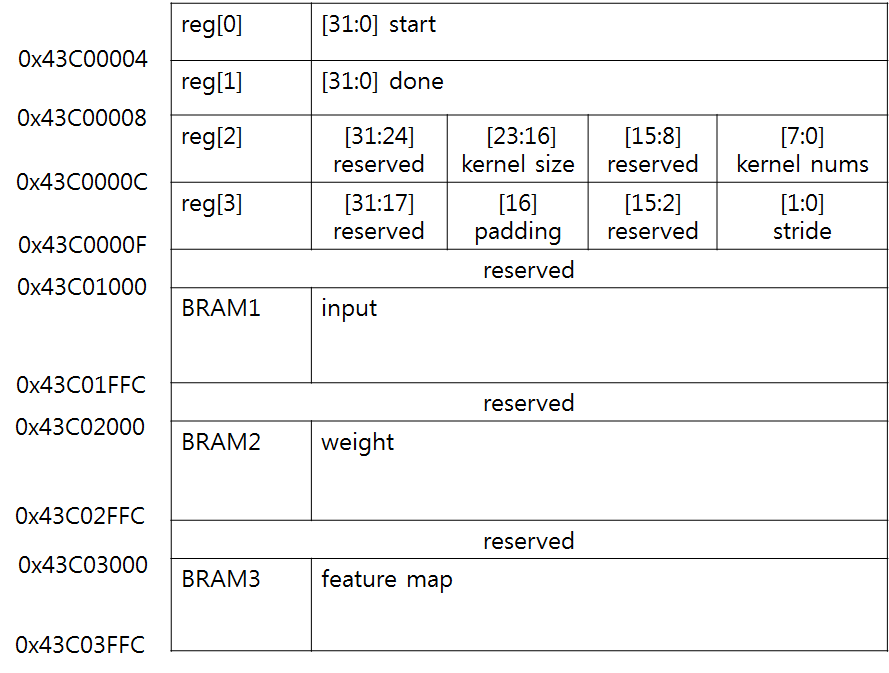


2. Block design





2. Block design

3. Memory map