

YAMAHA® LSI

YM3438

アプリケーションマニュアル

OPN2C 6ch, 4-OP. FM sound generator

1990年4月 現在

YAMAHA

Translated by @dcelctr ***

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■ General

OPN2C is a synthesizer sound source based on the FM method. It maintained compatibility between OPN (YM2203C) and FM sound source tone data. However, we expanded the simultaneous polyphony to 6 sounds. It is also possible to output 8-bit PC sound using 1 of the 6 sounds. It also has a built-in low-frequency oscillator for vibrato and vibration modulation, and a stereo DAC for audio output. On the other hand, we have removed the square wave source and I/O port from OPN and compacted it into a 24 pin package.

■ Specific

- FM Sound Source: 4 operators, 6 sounds simultaneously. Compatible with OPN tone data.
- PCM: 1 sound out of 6 sounds possible can be output by writing to an 8-bit register from the microcomputer.
- Low Frequency Oscillator: Vibrato, amplitude modulation, (LFO) modulation presence/absence and oscillation frequency can be set.
- Audio output: 2 channels, L and R Built-in 9-bit stereo DAC.
- Timer: 2 built-in programmable timers.
- Others: 5V single power supply. Low power consumption by CMOS. The package is a 24-pin plastic DIP

■ Main Functions

The functions of OPN2C are as follows. (Basically the same as OPN (YM2203C)).

Sound mode: 4 operator FM method 6 at the same time.

Algorithm: 8 types.

Parameters: Refer to the register map and various sound source functions.

LFO function: Sine wave LFO. Pitch (PM) and amplitude (AM) modulation. Variable oscillation frequency. PMS, AMS control and AM on/off for each operator are possible.

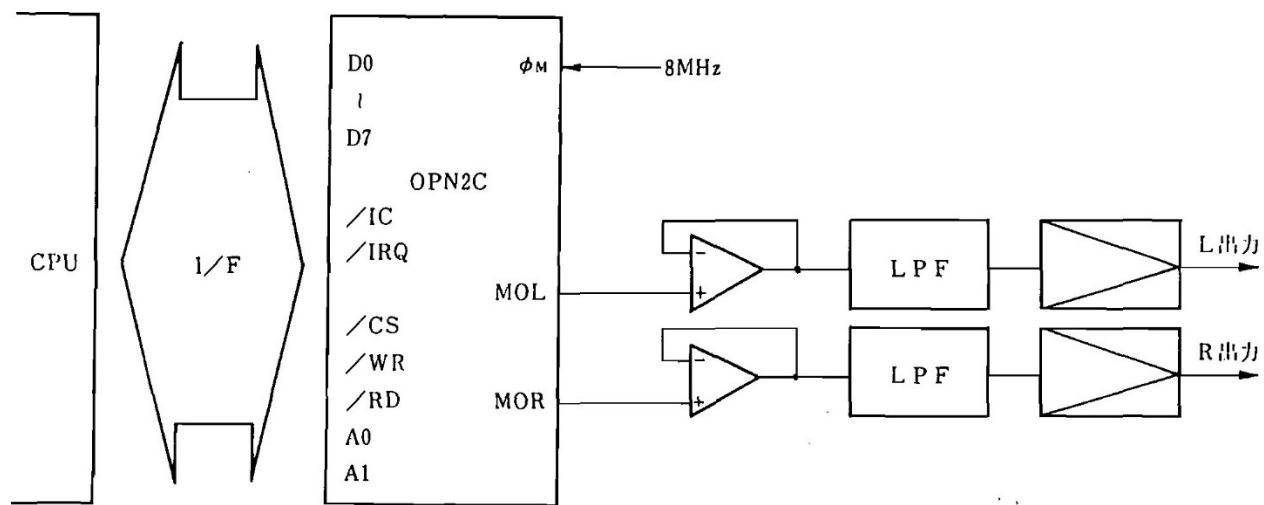
Composite sine wave synthesis: 1 out of 6 sounds is possible.

Timer function: Two types of timers, A and B.

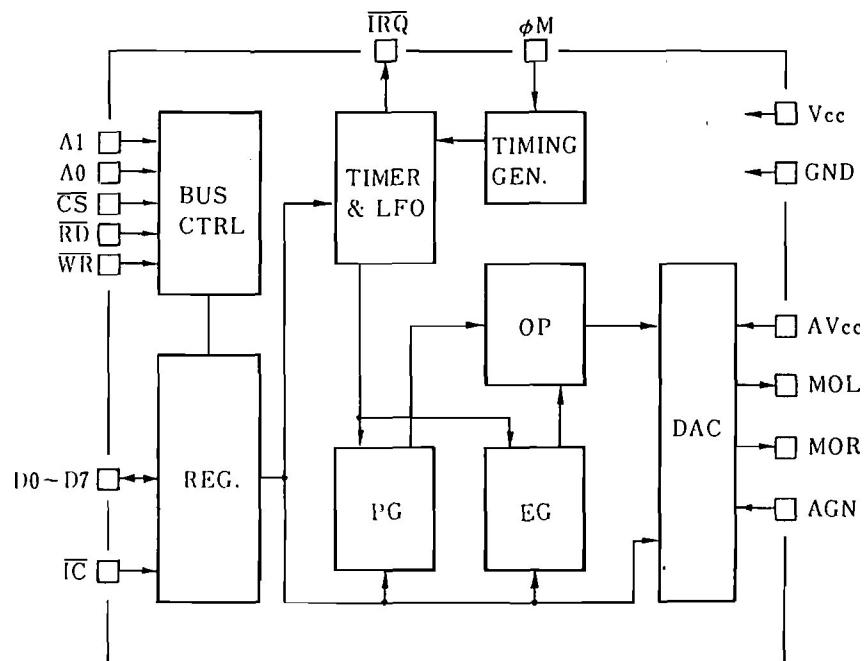
Output control: Built-in 9-bit D/A converter. L and R on/off.

PCM Function: Sampling rate 55.5 kHz. 8-bit output.

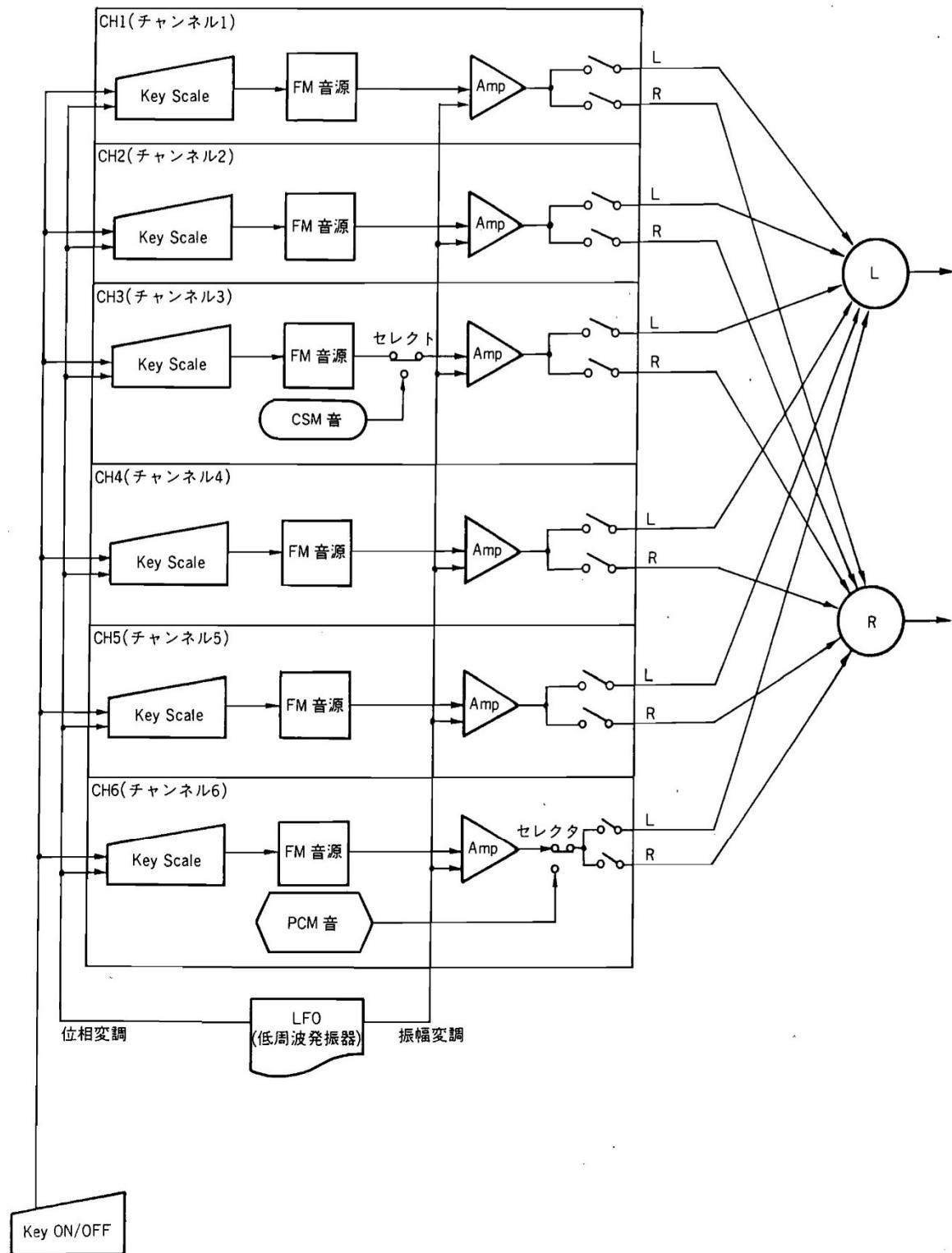
■ System Block Diagram



■ Block Diagram



■ System Concept Diagram



音源: Sound Source, チャンネル: channel, 位相変調: phase modulation,

低周波発振器: low frequency oscillator, 振幅変調: Amplitude modulation, セレクタ: selector

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■ Terminal Arrangement Diagram

GND	1	I		I	24	ϕM
D0	2	I/O		I	23	Vcc
D1	3	I/O		I	22	AVcc
D2	4	I/O		O	21	MOL
D3	5	I/O		O	20	MOR
D4	6	I/O		I	19	AGND
D5	7	I/O		I	18	A1
D6	8	I/O		I	17	A0
D7	9	I/O		I	16	\overline{RD}
* TEST	10	I/O		I	15	\overline{WR}
* \overline{IC}	11	I		I	14	$\overline{CS}*$
GND	12	I		O	13	\overline{IRQ}

This figure is TOP VIEW

The terminals marked with * are pulled up to V_{CC} by pull-up resistors.

■ Terminal Function

$\emptyset M$

Master clock input.

MOL · MOR

2 channel analog output. Voltage output.

D0 ~ D7

8-bit bi-directional data bus. Communicate data with the processor.

CS · RD · WR · A1 · A0

Controls the D0 ~ D7 data bus.

Table 1.1: Data Bus Control

CS	RD	WR	A1	A0	Address Range	Contents
0	1	0	0	0	\$21 ~ \$2C	Write the register address of a timer, etc.
					\$30 ~ \$B6	Write register addresses for channels 1 to 3.
0	1	0	0	1	\$21 ~ \$2C	Write register data such as timer.
					\$30 ~ \$B6	Write register data for channels 1 to 3.
0	1	0	1	0	\$30 ~ \$B6	Write register addresses for channels 4-6.
0	1	0	1	1	\$30 ~ \$B6	Write register data for channels 4 to 6.
0	0	1	0	0	\$XX	Read status.
0	0	1	0	1	\$XX	DO ~ D7 goes to high impedance.
0	0	1	1	0		
0	0	1	1	1		
1	X	X	X	X		

IRQ

An interrupt signal issued by two timers. After the time programmed into the timer has elapsed, it goes to a low level. This is an open-drain output.

IC

Initialize the internal registers.

TEST

This pin is for testing this LSI. Do not connect anywhere.

GND, AGND

Ground pin.

V_{CC}, AV_{CC}

+5V power supply pin.

- Data Bus Control

The CS, WR, RD, A0, and A1 signals are used to control the data bus for specifying register addresses and reading/writing data. The address ranges and data contents that can be controlled by the states of these signals are shown in Table 1.1 in Pin Functions.

The OPN2C registers consist of two series of register banks that share addresses \$30 ~ \$B6. Bank specification is performed by bus control signal A1. This method allows access to each register.

The assignment of register addresses by A1 is:

FM 共通部: FM common part

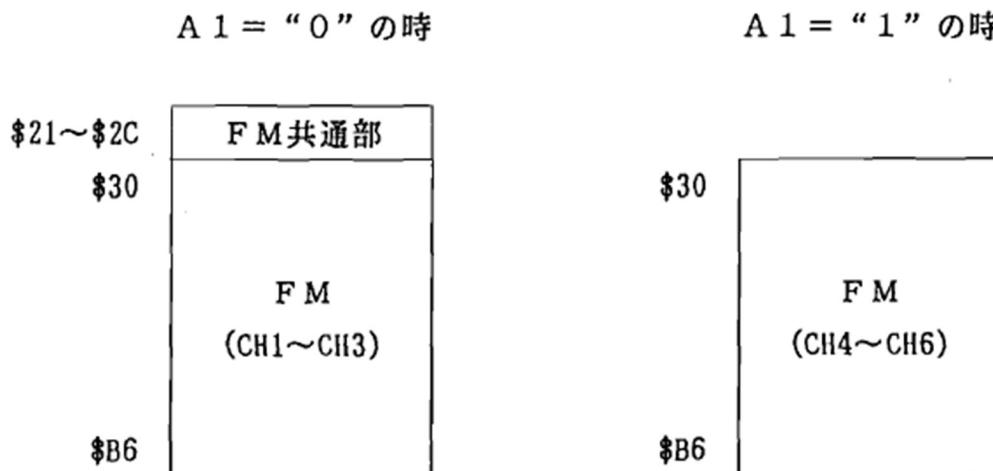


Figure 1.1: Register Address Assignment

Table 1.2: Register Control Modes for CS, WR, RD, A0, and A1.

	CS	RD	WR	A1	A0	Mode
1	0	1	0	*	0	Address write mode
2	0	1	0	*	1	Data write mode
3	0	0	1	0	0	Status read mode
4	0	0	1	0	1	Inactive read mode
	0	0	1	1	0	
	0	0	1	1	1	
5	1	X	X	X	X	Inactive mode

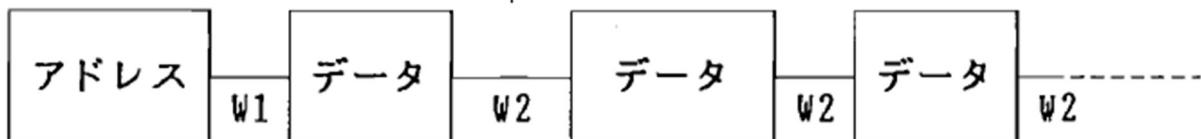
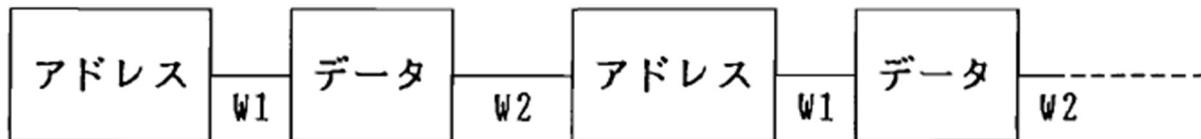
A1 = "*" specifies the bank.

1) Address write mode:

To write data from the CPU to a register or read data from a register, first specify the address of the register and then write or read the data. Addressing writes address data to data buses D0 to D7 when the bus control signal is <address write mode>. The specified address is retained until the next address is newly specified, so when accessing the same address continuously, writing the address data only needs to be done once at the beginning and is not required after that.

2) Data write mode:

After specifying the address, set the path control signal to <data write mode> and write the data on the data bus to the register.



アドレス: address, データ: data

W1: Wait time after address write

W2: Waiting time after data write

3) Status read mode:

When the bus control signal is set to <status read mode>, the status information generated in the status register is output to the data bus.

4) Inactive read mode:

Data buses D0 to D7 are high impedance, but the internal operation is the same as status read mode.

5) Inactive mode:

When CS is "1", data buses D0 to D7 become high impedance.

《Waiting time in/during write mode》

Table 1.3: After Address Write

Address	Wait Cycles
\$21 ~ \$B6	17

Table 1.4: After Writing Data

Address	Wait Cycles
\$21 ~ \$9E	83
\$A0 ~ \$B6	47

*The number of cycles is the number of master clock ØM cycles.

《Waiting time in/during read mode》

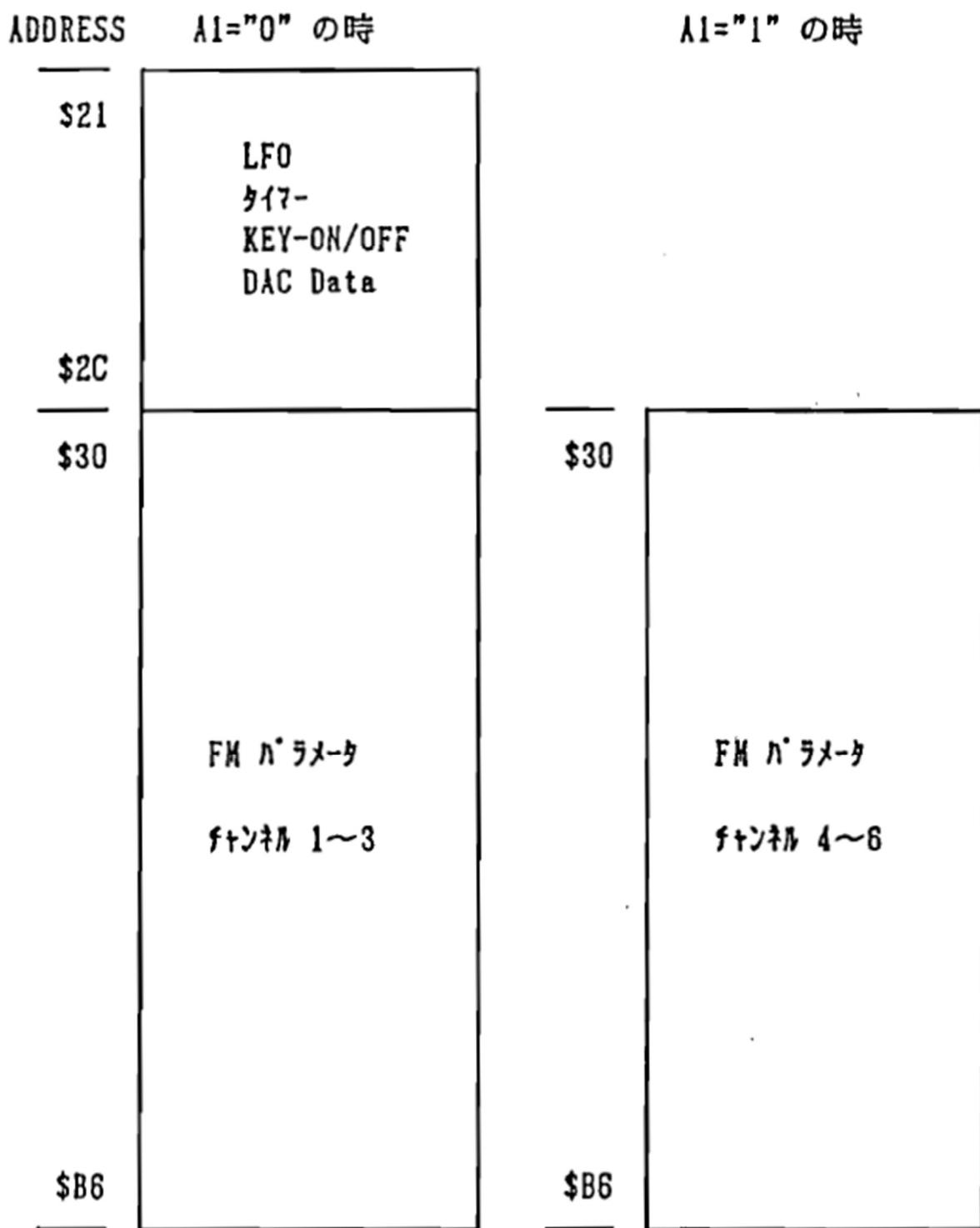
Table 1.5

Address	Wait Cycles
\$21 ~ \$B6	17

* Special time when reading after writing data and address

What must be noted with address and data writes is that it is necessary to set a specified waiting time before moving on to the next process after writing is complete. This is due to the data processing method inside the LSI. Therefore, be sure to set the wait time in order to correctly set the data in the register. Tables 1.3, 1.4, and 1.5 show the wait times for register writes.

■ Register map



FM パラメータ チャンネル 1~3 / 4~6: FM parameters Channel 1 ~ 3 / 4~6

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ADDRESS	COMMENT			
\$21	LSIのTest Data			
\$22	LFOのFreq Control			
\$24	Timer-Aの上位8ビット			
\$25	Timer-Aの下位2ビット			
\$26	Timer-Bのデータ			
\$27	Timer-A/BのControl及び 3CHのMode			
\$28	Key ON/OFF			
\$2A	DAC Data			
\$2B	DAC Select			
\$2C	LSIのTest Data			
\$30	Detune/Multiple (33, 37, 3Bのアドレスは無し)			
\$3E	Total Level (43, 47, 4Bのアドレスは無し)			
\$40	Key Scale/Attack Rate (53, 57, 5Bのアドレスは無し)			
\$4E	AMON/Decay Rate (63, 67, 6Bのアドレスは無し)			
\$50	Sustain Rate (73, 77, 7Bのアドレスは無し)			
\$5E	Sustain Level/Release Rate (83, 87, 8Bのアドレスは無し)			
\$60	SSG-Type Envelope Control (93, 97, 9Bのアドレスは無し)			
\$70	F-Number/BLOCK			
\$7E	3 CH - 3 Slot			
\$80	F-Number/BLOCK			
\$8E	Self-Feedback/Connection			
\$90	LR/AMS/PMS			
\$9E				
\$A0				
\$A1				
\$A2				
\$A4				
\$A5				
\$A6				
\$A8				
\$A9				
\$AA				
\$AC				
\$AD				
\$AE				
\$B0				
\$B1				
\$B2				
\$B4				
\$B5				
\$B6				

のアドレスは無し: no address for, 上位8ビット: Upper 8 bits, 下位2ビット: Lower 2 bits,
データ: data, 及び: as well as

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◆ Register contents and address map.

OPN2C registers are given internal addresses as shown in the address map. The contents of each register (address) are as follows.

(1)	\$21 ~ \$20	Test information. Always set to "0".
(2)	\$22	Sets the LFO ON/OFF control and the LFO oscillation frequency.
(3)	\$24 ~ \$26	Give a set time for timer A and timer B.
(4)	\$27	Controls the operation of timers A and B. In addition, it sets the mode of the 3rd channel of the FM sound source.
(5)	\$28	Controls ON/OFF of channels and slots.
(6)	\$2A	Write DATA directly to DAC.
(7)	\$23	Select whether to output her FM sound on channel 6 or output the DATA written o \$2A.
(8)	\$30 ~ \$3E	Detune and Multiple control. Used when setting the tone. Controls the relationship between the fundamental and overtones.
(9)	\$40 ~ \$4E	Give Total Level. This information becomes the volume (amplitude) of the modulated wave and the modulation index of the modulated wave
(10)	\$50 ~ \$5E	Key-Scale controls the rate of change of A/D/S/R according to the keyboard information. Attack Rate gives the rate of envelope change of attack.
(11)	\$60 ~ \$6E	Decay Rate is the rate at which the envelope changes during decay, and vibration modulation control ON/OFF.
(12)	\$70 ~ \$7E	Sustain Rate is the rate at which the envelope changes during sustain.
(13)	\$80 ~ \$8E	Sustain Level gives the level to transition from Decay to Sustain. Release Rate is the rate at which the envelope changes upon release.
(14)	\$90 ~ \$9E	Gives a preset envelope.
(15)	\$A0 ~ \$A6	Give a Key-Code (F-Number) for each channel.
(16)	\$A8 ~ \$AE	3-channel Key-Code (F-Number) in special mode.
(17)	\$B0 ~ \$B2	Gives the modulation type (Connection) of FM modulation and the modulation depth of feedback FM. (Self-feedback)
(18)	\$B4 ~ \$B6	Set depth to apply LFO to amplitude and oscillation frequency, L/R, ON/OFF.

■ Status Flag

ADDRESS	COMMENT			
\$XX	BUSY	/ / / / /	FLAG A B	Status

■ FM Sound Generator Functions

The OPN2C is a 4-operator FM sound source LSI that can produce 6 sounds/6 tones simultaneously. In addition to the high-quality FM sound produced by the 4-operator system, the built-in LFO function dramatically improves the possibilities of sound creation. Also, since there is software compatibility with OPN, the sound parameters created with OPN can be used. This chapter describes each block that configures the operator, focusing on the register functions of OPN2C.

1. Register Configuration

The parameters that control the operator are located in registers \$21 ~ \$B6. Sound creation and sound control of the FM sound generator is performed by writing appropriate data to each register.

1-1. Common Registers: \$21 ~ \$28

This block has functions common to all audio output channels. It consists of LFO, timer channel assignment function, etc.

(Note) In OPN, the input clock division number can be set to 1/2, 1/3, 1/6 by prescale function by \$ 2D, 2E, and 2F, but OPN2C does not have this function. The number of turns is fixed at 1/6.

Test: \$21

OPN2C test register. Not used by user applications.

LFO: \$22

(Refer to 5. LFO) Sets L FO's ON/OFF control and L FO's oscillation frequency.

Timer - A: \$24, \$25

The timer consists of two types of presetable timers and a timer controller that starts, stops, and flags each timer. At the same time that the timer flags assigned to D1 and D0 in the status (read mode) become "1", an IRQ is generated to perform a timer interrupt to the CPU.

Timer A is a timer counter with a resolution of $18\mu s$ ($fM = 8$ MHz) made of 10 bits of \$24 and \$25. The time interval that can be set can be calculated by formula ①.

	D7	D6	D5	D4	D3	D2	D1	D0
\$24	P9	P8	P7	P6	P5	P4	P3	P2
\$25	/	/	/	/	/	/	P1	P0

$$tA = 144 * (1024 - NA) / fM \dots \textcircled{1}$$

$$NA: P9 \times 2^9 + P8 \times 2^8 + P7 \times 2^7 + P6 \times 2^6 + \dots + P1 \times 2^1 + P0$$

fM: Master clock frequency [Hz]

(Example) When fM = 8 MHz,

$$tA (\text{MAX}) = 18432 \mu s$$

$$tA (\text{MIN}) 18 \mu s$$

Timer - B: \$26

Timer B is a timer counter with a resolution of $288 \mu s$ ($fM = 8$ MHz) made with 8 bits of \$26. The time interval that can be set can be calculated using the formula ②.

	D7	D6	D5	D4	D3	D2	D1	D0
\$26	P7	P6	P5	P4	P3	P2	P1	P0

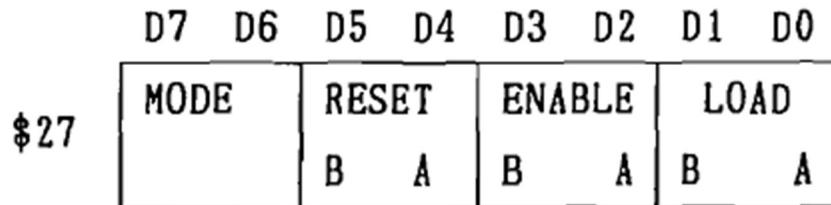
$$tB = 2304 * (256 - NB) / fM \dots \textcircled{2}$$

$$NB: P7 \times 2^7 + P6 \times 2^6 + \dots + P1 \times 2^1 + P0$$

fM: Master clock frequency [Hz]

□ Timer Control: \$27

Timers A and B are controlled by the \$27 timer controller.



- LOAD: Controls the start and stop of the timer.
Start with "1".
Stop at "0".
- ENABLE: Controls the status (read mode) timer flag.
When the value is "1", the timer flag "1" is set. Also, this timer flag generates an interrupt signal to the IRQ pin.
When it is "0", the flag will not change even if the timer counter overflows.
- RESET: Reset the timer flag. When "1", the status timer flag is reset and at the same time this bit itself is cleared to "0".
- MODE: Sets the mode of channel 3.
Channel 3 can be set by \$27 "D7, D6".

D7	D6	Mode	Function
0	0	Normal	Like other CHs, it is sounded normally.
1	0	CSM	The CSM voice synthesis mode is activated, and the F-Number can be set separately for each of the 4 slots. Key-on/off in CSM mode is done using timer A.
0	1	Sound Effect	Like the CSM, each slot can have a separate F-Number.

- Key on/off: \$28

Key assignment for each channel (チャンネル) is performed by channel designation and slot (スロット) on/off.

D7	D6	D5	D4	D3	D2	D1	D0		
\$28				SLOT	/	CH.			
D4				スロット 1 の ON/OFF					
D5				スロット 2 の ON/OFF					
D6				スロット 3 の ON/OFF					
D7				スロット 4 の ON/OFF					
				0	0	0	チャンネル 1		
				0	0	1	チャンネル 2		
				0	1	0	チャンネル 3		
				1	0	0	チャンネル 4		
				1	0	1	チャンネル 5		
				1	1	0	チャンネル 6		

- Test: \$2C

OPN2C test register. Not used by user applications.

1 - 2. D/A Registers: \$2A, \$2B

OPN2C can send the data written from the CPU directly to the D/A converter instead of the FM sound of channel 6. This register is for realizing this function.

- DAC Data: \$2A

Give the data you want to D/A convert. Create data in offset binary.

However, bit 0 is LSB and bit 7 is MSB.

- DAC Select: \$2B

This register selects whether to output the FM sound or the data written in register \$2A to channel 6. When bit 7 of this register is set to "0", FM sound is output, and when set to "1", DAC data is output.

1-3. Channel Register: \$30 ~ \$B6

This register contains sound parameters for 3 channels, F-Number, etc. \$30 ~ \$9E are the parameters set for each slot, and \$A0 ~ \$B6 are parameters set for each channel.

Channel selection is controlled by bus control signal: A1.

When A1 = "0", CH1~CH3 parameter control.

When A1 = "1", CH4~CH6 parameter control.

The relationship between register addresses and channels/slots is shown in Table 2.1.

Table 2.1: Relationship between Register Address and Channel Slot

SLOT パラメータ		CH 1 / CH 4				CH 2 / CH 5				CH 3 / CH 6											
		1	3	2	4	1	3	2	4	1	3	2	4								
DT/MULTI	3*	30	34	38	3C	31	35	39	3D	32	36	3A	3E								
TL	4*	40	44	48	4C	41	45	49	4D	42	46	4A	4E								
KS/AR	5*	50	54	58	5C	51	55	59	5D	52	56	5A	5E								
AM/DR	6*	60	64	68	6C	61	65	69	6D	62	66	6A	6E								
SR	7*	70	74	78	7C	71	75	79	7D	72	76	7A	7E								
SL/RR	8*	80	84	88	8C	81	85	89	8D	82	86	8A	8E								
SSG-EG	9*	90	94	98	9C	91	95	99	9D	92	96	9A	9E								
F-Num1		A 0				A 1				A 2											
Block/F-Num2		A 4				A 5				A 6											
3CH*F-Num1 *1										A9	A8	AA	A2								
3CH*(Block/F-Num2) *1										AD	AC	AE	A6								
FB/Algorithm		B 0				B 1				B 2											
L/R,AMS/PMS		B 4				B 5				B 6											

*1: \$A8 ~ \$AA, \$AC ~ \$AE are the frequency (Block, F-Number) setting registers when channel 3 is set to sound effect mode or CSM voice synthesis mode. It is not used in normal sound mode. For channel 3 mode settings, please refer to 1-1.

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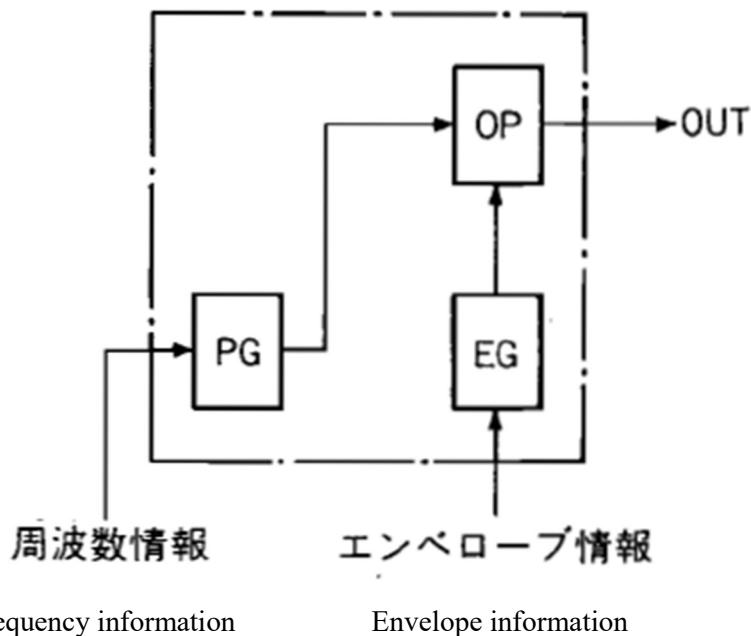
2. Operator

2-1. Operator

The FM tone generator can create various tones by combining multiple operators. However, a single operator is nothing more than a function that performs calculations according to data written to registers.

An operator is a sine wave oscillator that generates a sine wave according to given frequency information and output level (envelope) information.

An operator is represented by a block diagram as shown below.



Frequency information

Envelope information

OP: Signed Table.

PG: Phase Generator. Frequency (phase) information generation circuit. Generates the data read speed of the signature table.

EG: Envelope Generator. It controls the output level of the sine table and the temporal change of the output level.

In other words, if you give PG wavenumber information and EG envelope information, the operator will output a sine wave. However, this is not very interesting because it only gives a sine wave.

Therefore, by connecting multiple operators, it is now possible to create sounds that include overtone (harmonic) components.

Principles of FM . . . By modulating a sine wave with a sine wave, it is possible to create a waveform with a complex overtone structure.

Fig. 2.1 shows the block diagram of the two-operator FM, which is the basis of the FM method.

OPN2C connects four operators to create FM sounds. This connection method is called an algorithm, and 8 types of algorithms can be selected. → Refer 2-2 Algorithms

Algorithm: A connection form (combination method) of operators. There are 8 types in 4 operator FM. Since the algorithm determines the role of each operator, this is the first parameter to determine when creating a tone.

The β in Figure 2.1 represents the feedback rate of feedback modulation. Feedback self-modulates by feeding back its own output to the input. This effect is equivalent to having an infinite number of operators connected, and since the overtone structure is an integer-order harmonic, it is effective for sawtooth-like waveforms, such as string-type tones. You can think of the feedback function as one form of connection. → Refer to 2-2 Algorithms

Operators distinguish between the modulating sides as the modulator and the modulated (whether or not) output side as the carrier. However, the original function of the operator does not change, and it can be a modulator or a carrier depending on the algorithm.

This is just a name that represents the role of each operator, such as whether it works as a carrier or a modulator when selecting an algorithm.

In Figure 2.1, OP1 is the modulator and OP2 is the carrier.

To summarize what has been said so far, the following settings should be made to create sounds for FM sound sources.

- A . Choose an algorithm and determine the role of each operator.
- B . Set the PG (Phase Generator) parameters to determine the output frequency of each operator.
- C. Set the EG (envelope generator) parameters to determine the envelope and output level for each operator.
- D. Use feedback FM depending on the timbre.

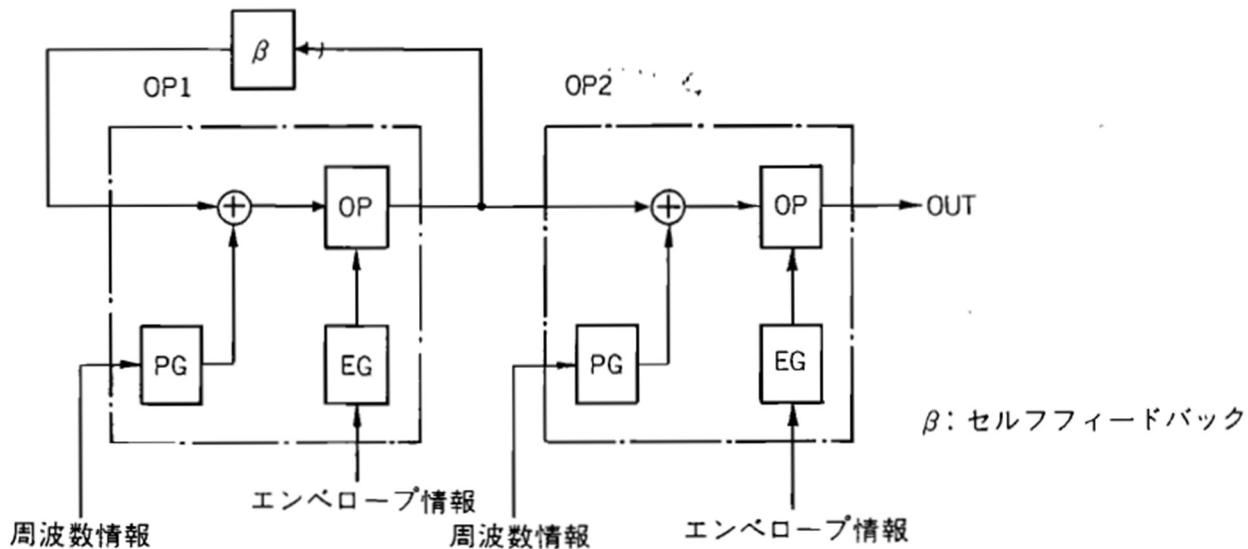


Figure 2.1

周波数情報: Frequency information, エンベロープ情報: Envelope information, β : self-feedback

2-2. Algorithm

A combination (connection configuration) of operators (slots) is called an algorithm. The 4-operator FM method such as OPN2C has 8 types of algorithms, and the operator selects the algorithm to function as a carrier or modulator.

However, the 4th slot is always set to carrier regardless of the algorithm.

Algorithm selection is the most important factor in creating the sound of an FM sound source. The basic procedure for creating sounds starts with selecting the algorithm most suitable for the desired tone color. After that, set the parameters for each slot to determine the tone.

Figure 2.2 shows the form of the algorithm. In addition, the characteristics of each algorithm are shown below.

- Characteristics of each algorithm:

- 1) Serial Quadruple Mode

Multiplex modulation is performed by connecting 4 slots in series. Multiple modulation schemes result in a very complex harmonic structure at the final carrier output as a result of continuous modulation repetitions.

S4 and S3 create the basic timbre, while S2 and S1 adjust the overtone components to add subtle flavor to the timbre.

- 2) Double Modulation Serial Triple Mode

Modulate S3 with the combined output of S2, S1. 1) Similarly, S4 and S3 create the basic tone, and S2 and S1 parameter settings create more detailed sounds.

- 3) Double Modulation Mode ①

S4 is modulated with a 2-line modulator. The basic timbre is created with S1 and S4, and additional sounds are added with S2 and S3 to give the timbre a natural feel.

- 4) Double Modulation Mode ②

Like 3), but the S3 does not have self-feedback, so it is suitable for woodwind sounds such as flutes. S2 and S1 create noise components.

Algorithms 1) to 4) have a single carrier, so they are a single timbre system and are suitable for solo instruments with complex overtone components.

- 5) 2 Serial / 2 Parallel Mode

This is a 2-operator 2-sequence algorithm. Although this mode is somewhat unsuitable for tones with many overtones, it can be used for a wide range of tones because it is relatively easy to create sounds and two types of tones can be created.

- 6) Common Modulation 3 Parallel Mode

A common modulator S1 modulates the three carriers S2, S3 and S4

- 7) Serial 2 Consecutive 2 Sign Mode

A composite output of one 2-operator FM and two sine waves is obtained.

8) 4 Parallel Sine Wave Synthesis Modes

The output is a composite of four sine waves. However, s1 can create a distorted sound by applying feedback.

In algorithms with multiple carriers, parameters related to the frequency information of each carrier are the decisive factor in sound creation.

For example, Algorithm "7" produces coupler effects like organ sounds by setting the multiple to different values for each carrier. Furthermore, depending on the detune setting value, shifting the pitch slightly will create an undulating sound, creating a so-called chorus (detune) effect.

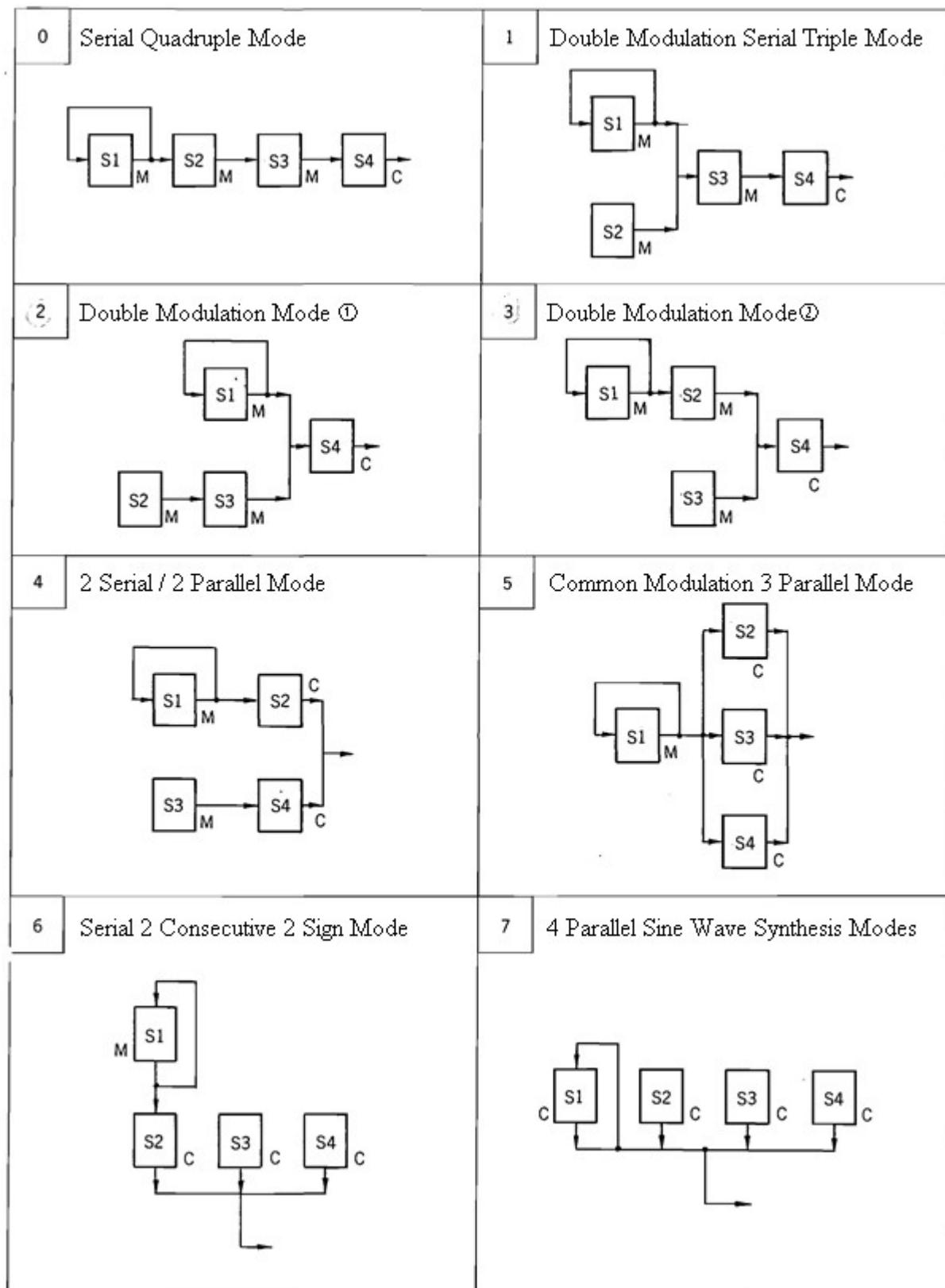


Figure 2.2: Algorithm M: Modulator C: Carrier

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2-3. Feedback

The first slot of each channel has a self-feedback function. Feedback is a function that performs self-modulation by allowing the operator to feed back his own output as a modulating signal to the input. A feedback factor of β represents the degree of modulation, and can be set in 8 steps from 0 to 7.

The feedback is equivalent to connecting multiple operators set to the same frequency in series. And this effect becomes an integral-order overtone structure in which the harmonic components are uniformly distributed. It is suitable for the generation of a harmonic spectrum seen in a sawtooth wave, and a string tone color or a noise component by deepening the modulation degree.



□ FB/Algorithm: \$B0 ~ \$B2

This register sets the self-feedback modulation depth and algorithm.

D7	D6	D5	D4	D3	D2	D1	D0
MSB				LSB		MSB	
\$B0 ~ \$B2							
/	/	Feedback		Algorithm			

Feedback modulation is shown in Table 2.2.

Table 2.2: Self-Feedback Modulation Depth (変調度)

Feedback	0	1	2	3	4	5	6	7
変調度	OFF	$\pi/16$	$\pi/8$	$\pi/4$	$\pi/2$	π	2π	4π

3. PG (Phase Generator)

The operator's output frequency (the speed at which the OP's sine table is read out at a given phase value) is determined by the frequency (phase) information generated by the PG. In other words, by increasing or decreasing the phase value, it is possible for the operator to generate sound at any output frequency.

Phase value, that is, frequency information, is performed by each parameter of F-Number / Block, Multiple, Detune.

3-1. F-Numbers and Blocks

A musical scale consists of a combination of pitches and octaves within one octave.

Therefore, if you create intervals within one octave with F-Number and set octave information with Blocks, you can easily create an 8-octave scale sequence.

The F-Number value within one octave can be calculated using the following formula, once the master clock and the required pitch frequency are determined.

$$\text{F-Number} = (144 \times \text{fnote} \times 2^{20} / \text{fM}) / 2^{(8-1)}$$

fnote: Sound frequency [Hz]

fM: Master clock frequency [Hz]

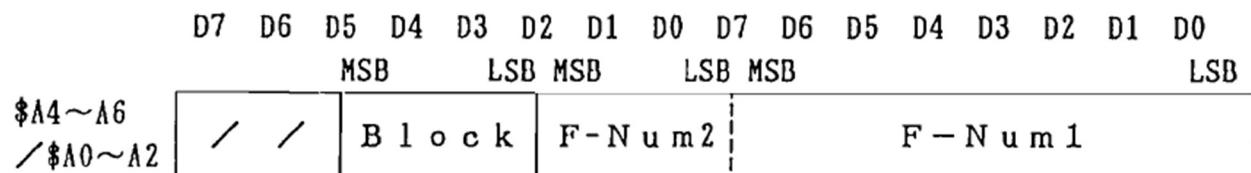
B: Block data

(Example) Find the F-Number of A4 (440Hz) when fM = 8MHz.

$$\begin{aligned}\text{F-Number (A4)} &= (144 \times 440 \times 2^{20} / 8 \times 10^6) / 2^{(4-1)} \\ &= 1038.1\end{aligned}$$

□ F-Number/Block: \$A0 ~ \$A2 / \$A4 ~ \$A6

This register sets F-Number and Block data. F-Number consists of lower 8bit / upper 3bit total 11bit, Block consists of 3bit. This data serves as common data for the four operators in the channel.



Be sure to follow the steps below to set the F-Number / Block data.

- ① Block/F-Num2 address and data write: \$A4 ~ \$A6
- ② F-Num1 address and data write: \$A0 ~ \$A2

3-2. F-Number table setting example

$fM = 8 \text{ Hz}$, octave: 4 (C4# ~ C5), A4 = 440 Hz

$fM = 8 \text{ M Hz}$ 、オクターブ: 4 (C4# ~ C5)、A4 = 440 Hz

Note	音 程 [Hz]	F- N u m b e r	F11~F9			F8~F5		F4~F1		Key Code		
			D2D1D0	D7D6D5D4	D3D2D1D0	N4	N3	分割				
C #	277.2	654.0	010	1000	1110	0	0	0				
D	293.7	692.9	010	1011	0100	0	0	0				
D #	311.1	734.0	010	1101	1110	0	0	0				
E	329.6	777.6	011	0000	1001	0	0	0				
F	349.2	823.9	011	0011	0111	0	0	0				
F #	370.0	872.9	011	0110	1000	0	0	0				
G	392.0	924.8	011	1001	1100	0	1	1				
G #	415.3	979.8	011	1101	0011	0	1	1				
A	440.0	1038.1	100	0000	1110	1	0	2				
A #	466.2	1099.9	100	0100	1100	1	0	2				
B	493.9	1165.3	100	1000	1101	1	1	3				
C	523.3	1234.6	100	1101	0010	1	1	3				

3-3. Creating Key Code by F-Number

One of the parameters of the envelope generator is the key-scale function. Key-Scale can have a scaling that changes the envelope plate (time) corresponding to the sounded pitch. (See 4. E.G.)

The division within one octave required for key scaling is performed using the F-Number value, and this division data is called Key Code.

From the upper 4 bits (F11 ~ F8) of F-Number data, divide 1 octave into 4.

* Wavenumber division within 1 octave (N4, N3)

$$N4 = F11$$

$$N3 = F11 \cdot (F10 + F9 + F8) + \overline{F11} \cdot F10 \cdot F9 \cdot F8$$

Furthermore, from 3-bit Block data, 32-step Key Code is created.

Detune, which will be explained on the next page, is also frequency-divided by this Key Code.

3-4. Multiple

Multiple is a parameter that sets the multiplier of the frequency information created by F-Number. The magnifications that can be set are shown in Table 2.3.

3-5. Detune

Detune is a parameter that gives the frequency information created by the F-Number a slight frequency shift for each slot. Also, Detune takes a value corresponding to each frequency information according to the Key Code obtained from F-Number.

□ Detune/Multiple

による倍率: Magnification by

*D6 is the sign bit.

D7	D6	D5	D4	D3	D2	D1	D0
MSB		LSB	MSB		MSB		LSB
\$30～\$3E	/	Detune		Multiple			

表2.3 Multipleによる倍率

Multiple(H)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
倍率	1/2	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

表2.4 Detune

Detune	0	1	2	3	4	5	6	7
FD	0	1	2	3	0	-1	-2	-3

*D6はサインビット。

(fM=7.9872MHz)

BLOCK	NOTE	FD=0	FD=1	FD=2	FD=3	BLOCK	NOTE	FD=0	FD=1	FD=2	FD=3
0	0	0.000	0.000	0.053	0.106	4	0	0.000	0.106	0.264	0.423
0	1	↑	↑	↑	↑	4	1	↑	0.159	0.317	0.423
0	2	↑	↑	↑	↑	4	2	↑	↑	↑	0.476
0	3	↑	↑	↑	↑	4	3	↑	↑	0.370	0.529
1	0	↑	0.053	0.106	↑	5	0	↑	0.212	0.423	0.582
1	1	↑	↑	↑	0.159	5	1	↑	↑	↑	0.635
1	2	↑	↑	↑	↑	5	2	↑	↑	0.476	0.688
1	3	↑	↑	↑	↑	5	3	↑	0.264	0.529	0.741
2	0	↑	↑	↑	0.212	6	0	↑	↑	0.582	0.846
2	1	↑	↑	0.159	↑	6	1	↑	0.317	0.635	0.899
2	2	↑	↑	↑	↑	6	2	↑	↑	0.688	1.005
2	3	↑	↑	↑	0.264	6	3	↑	0.370	0.741	1.058
3	0	↑	0.106	0.212	↑	7	0	↑	0.423	0.846	1.164
3	1	↑	↑	↑	0.317	7	1	↑	↑	↑	↑
3	2	↑	↑	↑	↑	7	2	↑	↑	↑	↑
3	3	0.000	↑	0.264	0.370	7	3	0.000	↑	↑	↑

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4. EG (Envelope Generator)

An EG is a circuit that generates temporal changes in volume and timbre from the rise to the end of a sound.

The EG consists of an envelope generator that generates the envelope and an output control circuit that determines the level of the envelope generator. Envelope information for starting the EG is set for each operator by the EG parameters assigned to the registers.

4-1. Envelope Generator

Generates an envelope that shapes the time course of the sound. The envelope is represented by four rates, Attack, Decay, Sustain and Release, and a Sustain level.

Figure 2.3 shows the envelope waveform.

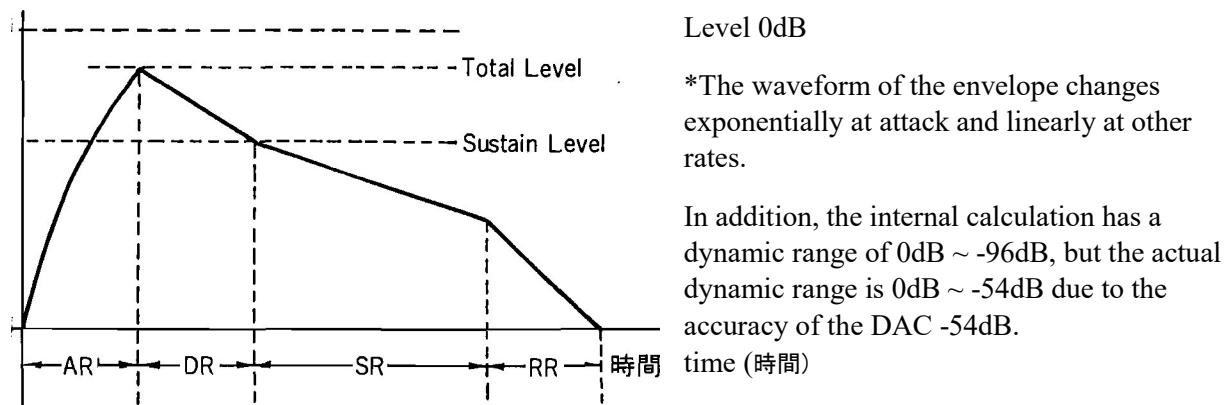


Figure 2-3: Waveform and parameters of the engine slope

□ AR (Attack Rate): \$50 ~ \$5E

Attack rate is the speed at which the maximum level is reached from the moment of key-on, and AR is a parameter that determines this rate. 5 bit; Set in 32 steps, the larger the AR, the faster the rise. Also, if set to "0", the attack rate will be infinite, and since the EG will not activate, no change in envelope will be obtained.

D7	D6	D5	D4	D3	D2	D1	D0
MSB				LSB			
\$50～\$5E				KS / Attack Rate			

※ K S は次頁参照。

※ See next page for KS.

□ DR (Decay Rate) : \$60 ~ \$6E

Decay rate is the speed at which the maximum level decays to the sustain level, and DR is the parameter that determines this rate. 5 bit; set in 32 steps, the larger the DR, the faster the attenuation. If set to "0", the decay rate will be infinite and the sound will be sustained at maximum level.

D7	D6	D5	D4	D3	D2	D1	D0
MSB				LSB			
\$60～\$6E				AMON / / Decay Rate			

※ AMON は 5. LFO 参照。

※ AMON see 5.LFO.

□ SL (Sustain Level): \$80 ~ \$8E

The sustain level is the level (attenuation amount) at which the decay rate switches to the sustain rate, and SL is the parameter that determines this level. 4 bit; Set in 16 steps, the greater the SL, the greater the attenuation. If set to "0", the amount of attenuation will be 0, and you will not get the feeling of attenuation due to decay. The weighting of each bit is shown in Table 2.5.

Table 2.5: SL Weighting of Each Bit (減衰量 Attenuation)

D7	D6	D5	D4	D3	D2	D1	D0	
				MSB	LSB			
\$80～\$8E				Sustain Level		Release Rate		

表 2.5 S L 各 b i t の重み付け

	D7	D6	D5	D4
減衰量(dB)	24	12	6	3

※ D7～D4 が全て “1” (15) の場合、
93 dB となります。

※ If D7 to D4 are all "1" (15), it will be 93 dB.

□ SR (Sustain Rate) \$70 ~ \$7E

Sustain rate is the speed at which sound decays from the sustain level, and SR is the parameter that determines this rate. 5 bit; set in 32 steps, the larger the SR, the faster the attenuation. If set to "0", the sustain level will be sustained (maintained).

D7	D6	D5	D4	D3	D2	D1	D0	
				MSB	LSB			
\$70～\$7E				Sustain Rate				

□ RR (Release Rate): \$80 ~ \$8E

Release rate is the speed of attenuation after key-off, and RR is the parameter that determines this rate. 4 bit; set in 16 steps, the larger the RR, the faster the attenuation.

The above A.D.S.R. parameter settings create an envelope for the operator. However, this alone will always give the same rate envelope to the operator, regardless of the operator's output frequency, which can be unnatural depending on the timbre.

Therefore, by using F-Number/Block data, each rate is changed according to the pitch. This function is called key scaling.

□ KS (Key-Scale): \$50 ~ \$5E

The key scale is a function that changes the time of the envelope according to the pitch. That is, the higher the note, the shorter each rate. 2 bit can be set in 4 stages, 0 for no effect, 3 for maximum difference (time). Table 6 shows the rate key scaling values by KS.

Each rate of the envelope generator is finally determined by the setting data of the A.D.S.R. parameters and the key scaling value. This value is expressed by the following formula.

$$\text{Rate} = 2R + R_{KS}; \text{ if } R = 0 \text{ then Rate} = 0$$

- R is the setting value of each parameter of A.D.S.R.

However, for RR (Release Rate), R is (set value $\times 2 + 1$).

- R_{KS} is the key scaling value.

※ The maximum Rate is 63, and the Rate = 63 when the calculation result is a value greater than 63.

Table 2. 1: Rate of Key - Scaling

KS	Note	0				1				2				3			
		0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
0		0								1							
1		0				1				2				3			
2		0	1	2	3	2	3	4	5	4	5	6	7	6	7	8	9
3		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

KS	Note	4				5				6				7			
		0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
0		2								3							
1		4				5				6				7			
2		8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
3		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

4-2. SSG-type Envelope Control

The envelope of the envelope generator can be controlled by a preset SSG-type envelope. The SSG-Type Envelope consists of the same waveform as the envelope found in the SSG sound source, and it is possible to add envelope changes that cannot be obtained only by setting the EG parameters. The shape of the envelope is shown in Figure 2.4.

When using this envelope, each parameter for E G corresponds as follows.

- ① Fix AR data setting to 1F (HEX).
 - ② The change in the envelope opening in the Keyon state is determined by the level settings of DR and SR rates and SL.
 - ③ RR works in the same way as in normal mode, setting the decay time after Key-off.
- SSG-EG: \$90 ~ \$9E

D7	D6	D5	D4	D3	D2	D1	D0
\$90～\$9E							SSG-EG

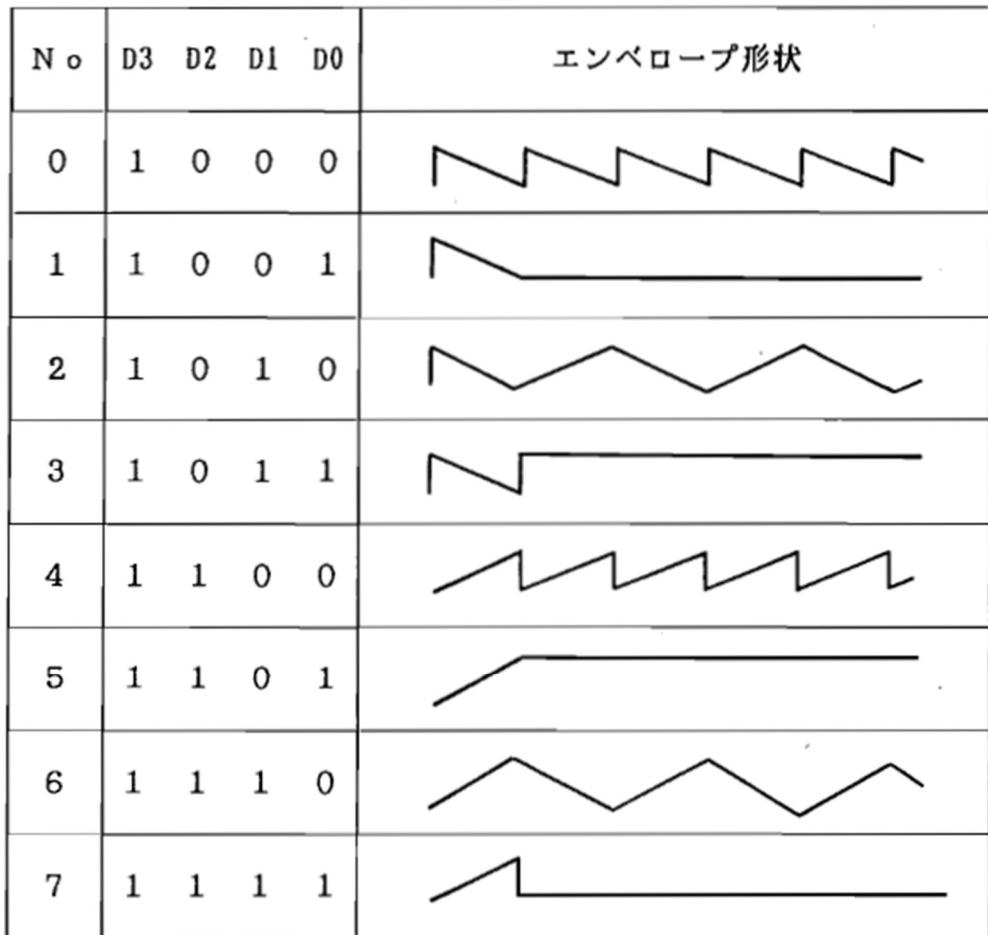


Figure 2.4: SSG-Type Envelope (エンベロープ形状: envelope shape)

4-3. Output Control Circuit

The envelope created by the envelope generator sets the level with the output control circuit. This determines the operator's output level, which has a dynamic range of 96 dB and a configurable resolution of 0.75 dB.

Note that the output level is expressed in terms of attenuation. In other words, it sets the amount of attenuation when the maximum value of the operator's output is 0 dB.

- TL (Total Level): \$40 ~ \$4E

The output level is set using the total level. The weighting of each bit indicates the amount of attenuation. Therefore, "00" is 0 dB (level max) and "7F" is attenuation 96 dB (level min).

However, in the case of OPN2C, the built-in D/A converter is 9 bit, so the actual analog audio output is equivalent to 54 dB. Therefore, when compared with OPN, analog audio output may overflow even if the parameters are set exactly the same.

Table 2.8: TL Weighting of Each Bit

D7	D6	D5	D4	D3	D2	D1	D0
\$40～\$4E	/						Total Level

表2.8 TL各bitの重み付け

	D6	D5	D4	D3	D2	D1	D0
減衰量(dB)	48	24	12	6	3	1.5	0.75

5. LFO: Low Frequency Oscillator

LFO is a function that modulates the operator with the output of the built-in low frequency oscillator to give periodic changes to the sound. OPN2C's LFO waveform is a sine wave, and the modulation is controlled by 5 parameters.

- LFOFREQ. : \$22

Sets the oscillation frequency that determines the LFO on/off control and LFO speed.

	D7	D6	D5	D4	D3	D2	D1	D0	
\$22	/	/	/	/	ON				LSB

D3 : "1" の時、LFO on。

D2 ~ D0 : 発振周波数の設定。

FREQ.CONT	0	1	2	3	4	5	6	7
freq (Hz)	3.98	5.56	6.02	6.37	6.88	9.63	48.1	72.2

D3: LFO on when "1".

D2 ~ D0: Oscillation frequency setting.

- PMS (Phase Modulation Sensitivity): \$B4 ~ \$B6

By adding (modulating) the LFO to the frequency (phase) information set by F-Number/Block, you can obtain periodic changes in pitch. PMS is a parameter that sets the depth of modulation and the degree of phase modulation for each channel.

- AMS (Amplitude Modulation Sensitivity): \$B4 ~ \$B6

By adding an LFO to Total Level, you can cyclically vary the operator's output level. AMS is a parameter that sets the modulation depth and amplitude modulation depth for each channel.

The effect on the sound when the LFO modulates the sound depends on the role of the operator. In other words, when the carrier is modulated, the volume changes, and the modulator changes the timbre.

	D7	D6	D5	D4	D3	D2	D1	D0	
\$B4~\$B6	L	R	AMS	/	PMS				LSB

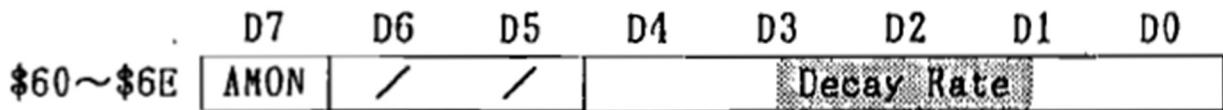
P M S	0	1	2	3	4	5	6	7
変調度 (cent)	0	±3.4	±6.7	±10	±14	±20	±40	±80

A M S	0	1	2	3
変調度 (dB)	0	1.4	5.9	11.8

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□ AMON: \$60 ~ \$6E

A switch to turn on/off amplitude modulation for each slot. On when "1".



Set the LFO with the above parameters.

If the built-in LFO does not provide sufficient results, use of the software LFO (sawtooth wave, square wave, triangle wave, S/H, etc.) is required. This is interrupt processing using the built-in timer, and it should be enough to give data according to the waveform of the LFO to each parameter of the operator.

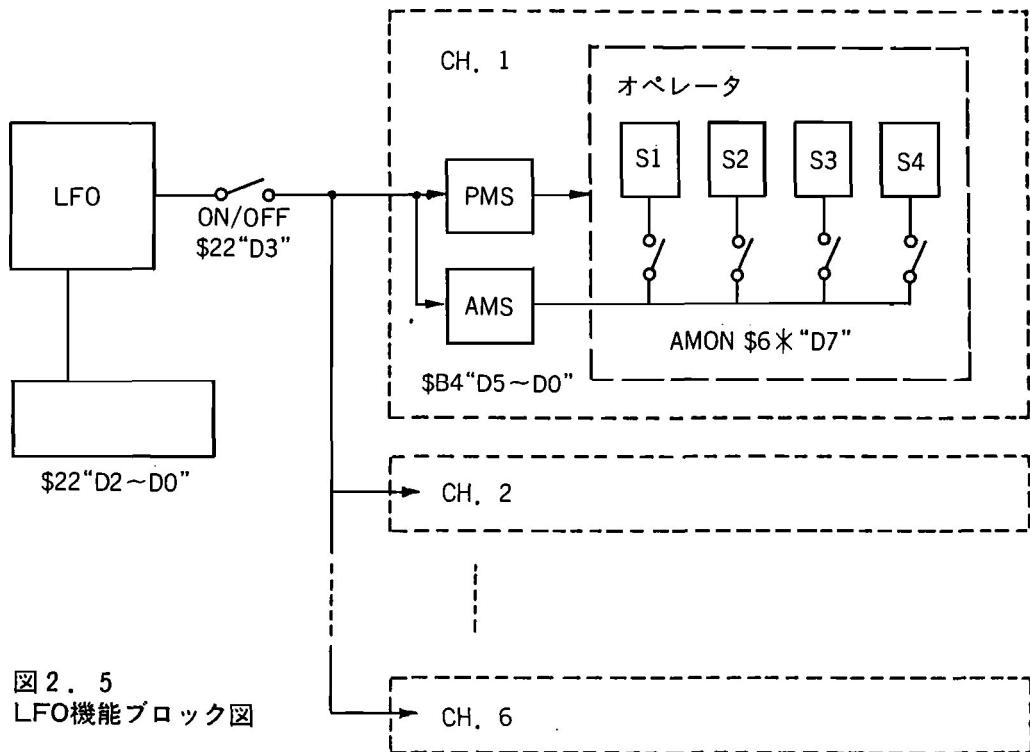


Figure 2.5: Block Diagram of the LFO Function.

[Reference] Cyclic changes in the sound produced by LFO produce the following effects on musical tones.

- Change in pitch (pitch): Vibrato
- Volume (level) change: Tremolo
- Changes in timbre (tone): Wuwu

6. Accumulator

The accumulator accumulates each slot output (9 bits) of each channel sent from the operator and sends it to the D/A converter.

Therefore, there is no need to be particularly careful when creating sounds.

7. D/A Converter and Output Selection

7-1. D/A Converter

The D/A converter converts the result calculated by the accumulator into an analog voltage.

The OPN2C can also D/A convert the data written to the address \$2A register. This is done by encoding the analog audio into 8-bit data and sequentially writing the data to the \$2A register.

The sampling rate at this time is 55.5 kHz.

→ Refer to 1-2. Register for D/A

7 - 2. Output Selection

The OPN2c has two channels of analog output, MOL and MOR, and can distribute 6 channels of FM sounds or 5 channels of FM sounds and 1 PCM sound to MOL and MOR, respectively, increase.

L/R: \$B4 ~ \$B6 "D7" "D6"

When "1", it turns ON and outputs to that CH.

◆ Electrical Characteristics

- Absolute Maximum Ratings ($V_{SS} = 0V$ standard)

Item	Symbol	Limits		Unit
		Min.	Max.	
Power Supply Voltage V_{CC}	V_{CC}	$V_S - 0.5$	$V_{SS} + 7.0$	V
Input Voltage	V_I	$V_S - 0.5$	$V_{SS} + 0.5$	V
Output Voltage	V_O	$V_S - 0.5$	$V_{SS} + 0.5$	V
Operating Temperature	T_{OP}	0	70	°C
Storage Temperature	T_{STG}	-50	125	°C
Input Terminal Current	I_{IP}	-20	20	mA

- Recommended Operating Conditions ($V_{SS} = 0V$ standard)

Item	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Power Supply Voltage V_{CC}	V_{CC}	4.75	5.00	2.25	V
Operating temperature	T_{OP}	0	25	70	°C
Low Level *1 Input Voltage	V_{IL}			0.8	V
High Level *1 Input Voltage	V_{IH}	2.0			V

Note *1: Excludes square input ($\emptyset M$).

- DC Characteristics (Under recommended operating conditions)

Item	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Leak Input Current	$\emptyset M$, WR, RD, A0, A1	I_L	$V_{IN} = 0 \sim 5V$	-10		10 μA
Three-State (off) Input Current	D0 ~ D7	I_{TSL}	$V_{IN} = 0 \sim 5V$	-10		10 μA
High Level Output Voltage	D0 ~ D7	V_{OH}	$I_{OH} = -80\mu A$	2.4		V
Low Level Output Voltage	D0 ~ D7	V_{OL}	$I_{OL} = 1.6mA$			0.4 V
Output Current (peak state)	IRQ	I_{OL}	$V_{OH} = 0 \sim 5V$	-10		10 μA
Supply Current		I_{CC}				25 mA
Resistance	TEST, IC, CS	R_{PU}		60		600 $k\Omega$

- DAC Characteristics (Under recommended operating conditions)

Item	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Maximum Output Amplitude	MOR, MPL	V_{OUT}			$AV_{CC} -0.08$	V
Decomposition Energy	MOR, MPL				9	BIT

- Clock Characteristics (Under recommended operating conditions)

Item	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
ØM Frequency	f _{MCLK}	Figure 1	7.7	8.0	8.3	MHz
ØM Duty Cycle H/L	Duty H/L	Figure 1	40	50	60	%
Low Cycle Input Voltage	V _{ILC}	Figure 1			0.8	V
High Cycle Input Voltage	V _{IHC}	Figure 1	2.0			V

$$\text{ØM duty rate } H = t_{HM} * f_{MCLK} \times 100$$

or ØM duty rate L * t_{LM} = f_{MCLK} × 100

- Terminal Capacity (Under recommended operating conditions)

Item	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Input Terminal Capacitance	C _I		5	8	pF
Forced Input Terminal Capacitance	C _{IC}			8	pF
Output Terminal Capacitance	C _O			10	pF
Input and Output Terminal Capacitance	C _{IO}			12	pF

Measurement conditions: T_{OP} = 25°C, V_{CC} = 5.0V

Input voltage: V_{IH} = 2.4V or more V_{IL} = 0.45V or less
 V_{IHC} = 3.0V or more V_{ILC} = 0.4V or less

Input signal frequency 1.0 MHz
 Connect measurement terminal to GND except V_{CC}

- Terminal Capacity (Under recommended operating conditions)

Item	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Setup Time	A0, A1	T _{AS}	Figures 2, 3	10		ns
Address Hold Time	A0, A1	T _{AH}	Figures 2, 3	10		ns
Chip Select Write Width	CS	T _{CSW}	Figures 2, 3	200		ns
Write Pulse Width	WR	T _{WW}	Figures 2, 3	200		ns
Data Write Setup Time	D0 ~ D7	T _{WDS}	Figures 2, 3	100		ns
Data Write Hold Time	D0 ~ D7	T _{WDH}	Figures 2, 3	20		ns
Chip Select Read Time	CS	T _{CSR}	Figure 2	350		ns
Read Pulse Width	RD	T _{RW}	Figure 2	350		ns
Data Read Setup Time	D0 ~ D7	T _{ACC}	Figure 2			250 ns
Data Read Hold Time	D0 ~ D7	T _{RDH}	Figure 2	10		ns
Write/Read Wait Time Read /Write Wait Time	WR, RD	T _{WRW} T _{RWW}	Figures 5, 6	750		ns
Write Access Prohibited Width	CS, WR, RD, A1, A0	T _{AIW}	Figure 5	17		cycles
Write Wait Width	WR	T _{WWW}	Figure 7 *1 *2 *3	17 83 47		cycles

Note) *1: Between address write and data write

*2: Between data write and address write and between data write and data write

However, when the register address to which data is written is \$21 ~ \$9E

*3: Between data write and address write and between data write and data write

However, when the register address to which data is written is \$A0 ~ \$B6

* Reset

Item	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Reset Pulse Width	IC	T _{IC}	Figure 4	192		cycles

- Timing Diagram (Timing is set on the basis of the values: $V_{IH} = 2.0V$, $V_L = 0.8V$)

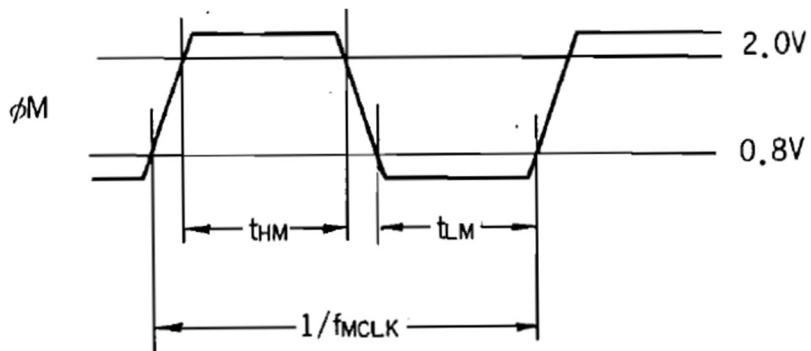


Figure 1. Clock Timing

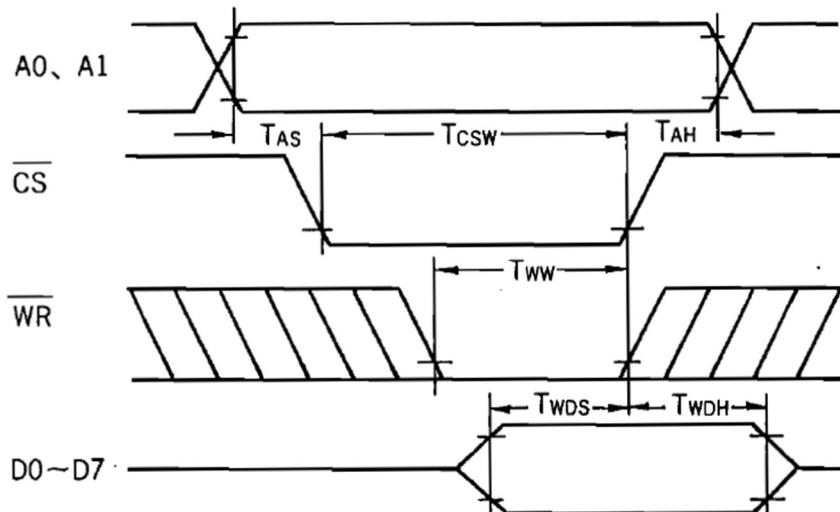


Figure 2. Write Timing

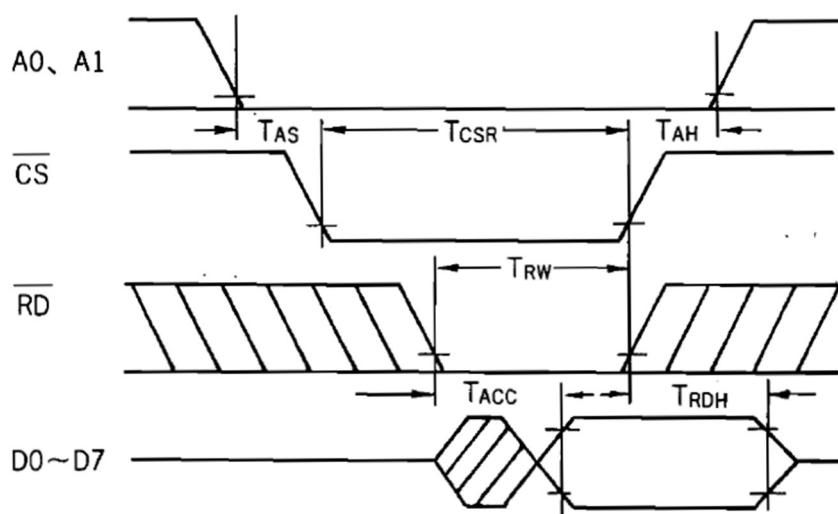


Figure 3. Read Timing

- Timing Diagram (continued)

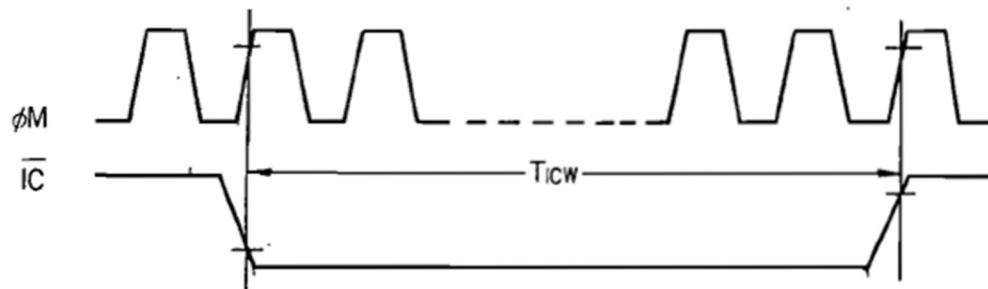


Figure 4. Reset Pulse Width

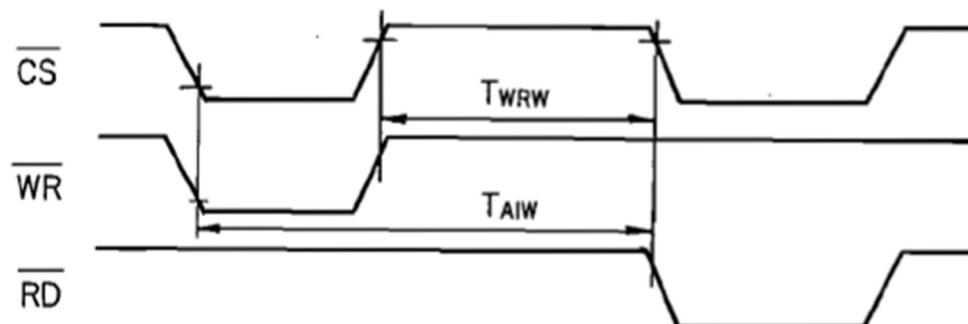


Figure 5. Write-Read Timing

- (Note) T_{AIW} is determined when either CS or WR goes LOW slowly and when either CS or RD changes slowly.
 T_{RWW} is determined when either CS or RD goes HIGH slowly and when either CS or WR changes quickly.
Also, T_{AIW} and T_{RWW} are unrelated to A0 and A1.

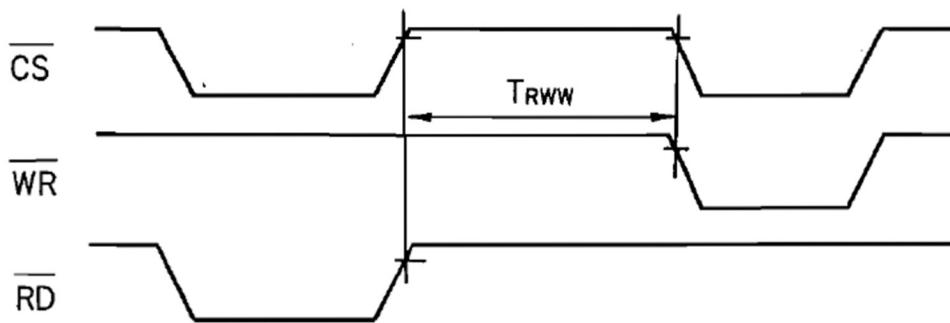


Figure 6. Write-Read Timing

- (Note) T_{RWW} is determined when either CS or RD goes HIGH slowly and when either CS or WR changes quickly.
Also, T_{RWW} is independent of A0 and A1.

- Timing Diagram (continued)

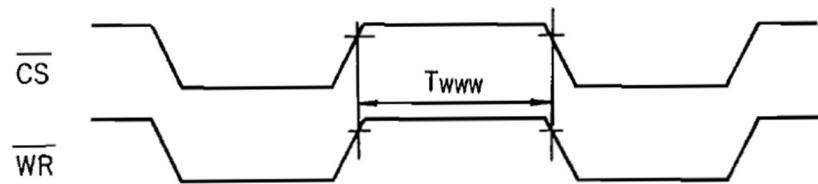
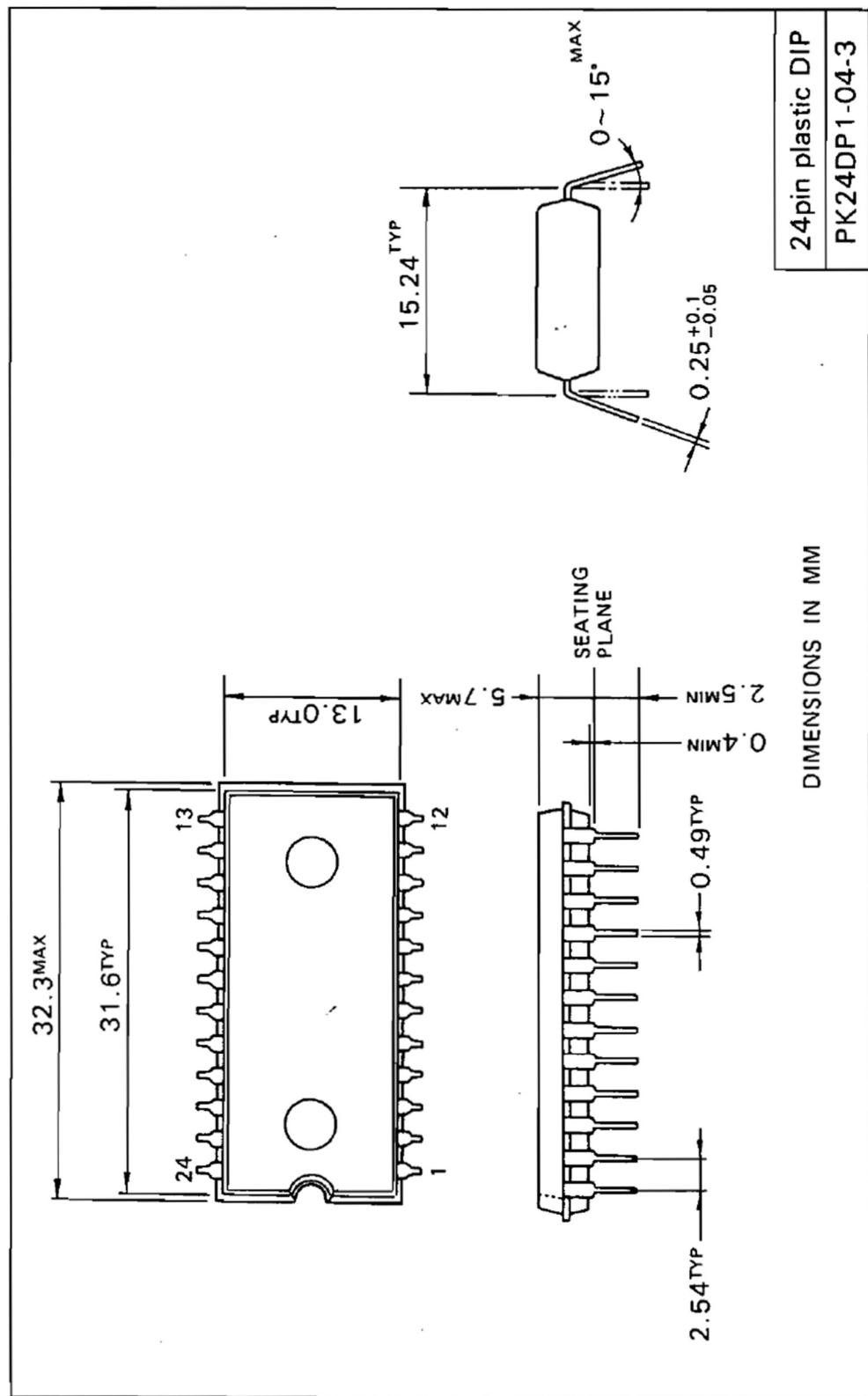


Figure 7. Write-Write Timing

(Note) T_{WWW} represents the time from when either CS or WR goes HIGH slowly to when either CS or WR changes slowly.
Also, T_{WWW} is independent of A0 and A1.

■ Outline Drawing



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■ Precautions when Converting OPN2 C Data

YM3438 (OPN2C) can produce 3CH or 6CH sounds by using YM2203 (OPN) and YM2608 (OPNA) software. However, in the case of OPN2C, due to its characteristics, it may not be possible to make it sound like OPN2.

However, even if OPN2 and OPN2C can be played with software created with OPN and OPNA, the same timbre as OPN and OPNA may not be obtained. This is because the dynamic range of the D/A converter is as narrow as 9 bits, so the output waveform overflows depending on the tone parameter settings.

To prevent this, it is necessary to adjust the Total Level in the tone parameters so that the output waveform is not distorted.

Also, be careful when creating sounds using OPN2 and OPN2C.

Thus, the compatibility of sound data between OPN2/OPN2C and OPN/OPNA is not 100%. Therefore, the guidelines for creating OPN2 and OPN2C data based on OPN, OPNA and YM2610 (OPNB) timbre data are shown below. This is the same when creating sounds using OPN2 and OPN2C.

- ① Check the data of connection (algorithm). If this data is between 0 and 3, the waveform will not be distorted even if TL = 0.
- ② When con. = 4, please set so that the sum of TL of two carriers is -6 [dB] or more.
- ③ When con. = 5 or 6, set so that the sum of TL of 3 carriers is -9.5 [dB] or more.
- ④ When con. = 7, set so that the sum of all TL is -12 [dB] or more.

■ FM Sound Generator Sound Samples

音色名：B E L L

	S 1	S 2	S 3	S 4
Total level	- 3 0	- 5	- 1 9	- 2
Multiple	1 5	3	7	2
Detune	3	- 1	- 1	0
Attack rate	3 1	3 0	3 1	3 1
Decay rate	4	8	4	5
Sus level	- 1	- 1 0	- 9	- 5
Sus rate	1 0	6	1 7	1 2
Release rate	3	3	1	3
Key scale	1	1	1	1
Am on/off	o n	o f f	o f f	o f f
EG control	o f f	o f f	o f f	o f f
L.F.O. 0				
Pitch C 3				
Ams 2 Pms 0				
Algorithm 4	Feed back 3			
				

音色名：PIANO

	S 1	S 2	S 3	S 4
Total level	- 3 7	- 3	- 3 3	- 3
Multiple	1	0	2	1
Detune	0	0	0	0
Attack rate	3 1	2 5	3 1	2 7
Decay rate	0	7	0	7
Sus level	- 4	- 3	- 4	- 3
Sus rate	8	6	8	6
Release rate	0	7	0	7
Key scale	3	2	3	2
Am on/off	o f f	o f f	o f f	o f f
EG control	o f f	o f f	o f f	o f f
L.F.O. off				
Pitch C# 5				
Ams 1 Pms 0				
Algorithm 4	Feed back 2			
				

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音色名：E O R G A N

	S 1	S 2	S 3	S 4
Total level	- 3 9	- 4 1	- 3 0	- 2 4
Multiple	5	2	8	1
Detune	3	3	3	3
Attack rate	3 1	3 1	3 1	3 1
Decay rate	1 8	1 5	4	1 5
Sus level	- 2	0	0	0
Sus rate	0	0	0	0
Release rate	1 5	1 5	1 5	1 5
Key scale	3	0	0	0
Am on/off	o f f	o f f	o f f	o f f
EG control	o f f	o f f	o f f	o f f
L.F.O. off				
Pitch G 3				
Ams 0 Pms 0				
Algorithm 5	Feed back 7			

音色名：B R A S S

	S 1	S 2	S 3	S 4
Total level	- 2 9	- 3 6	- 4 6	0
Multiple	1	2	1	1
Detune	0	0	0	0
Attack rate	1 2	2 4	1 2	1 9
Decay rate	5	2	5	3
Sus level	- 1 2	0	0	- 1
Sus rate	0	0	0	0
Release rate	8	8	8	8
Key scale	1	1	0	1
Am on/off	o f f	o f f	o f f	o f f
EG control	o f f	o f f	o f f	o f f
L.F.O. 1				
Pitch C 3				
Ams 0 Pms 2				
Algorithm 2	Feed back 7			

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音色名：S T R I N G

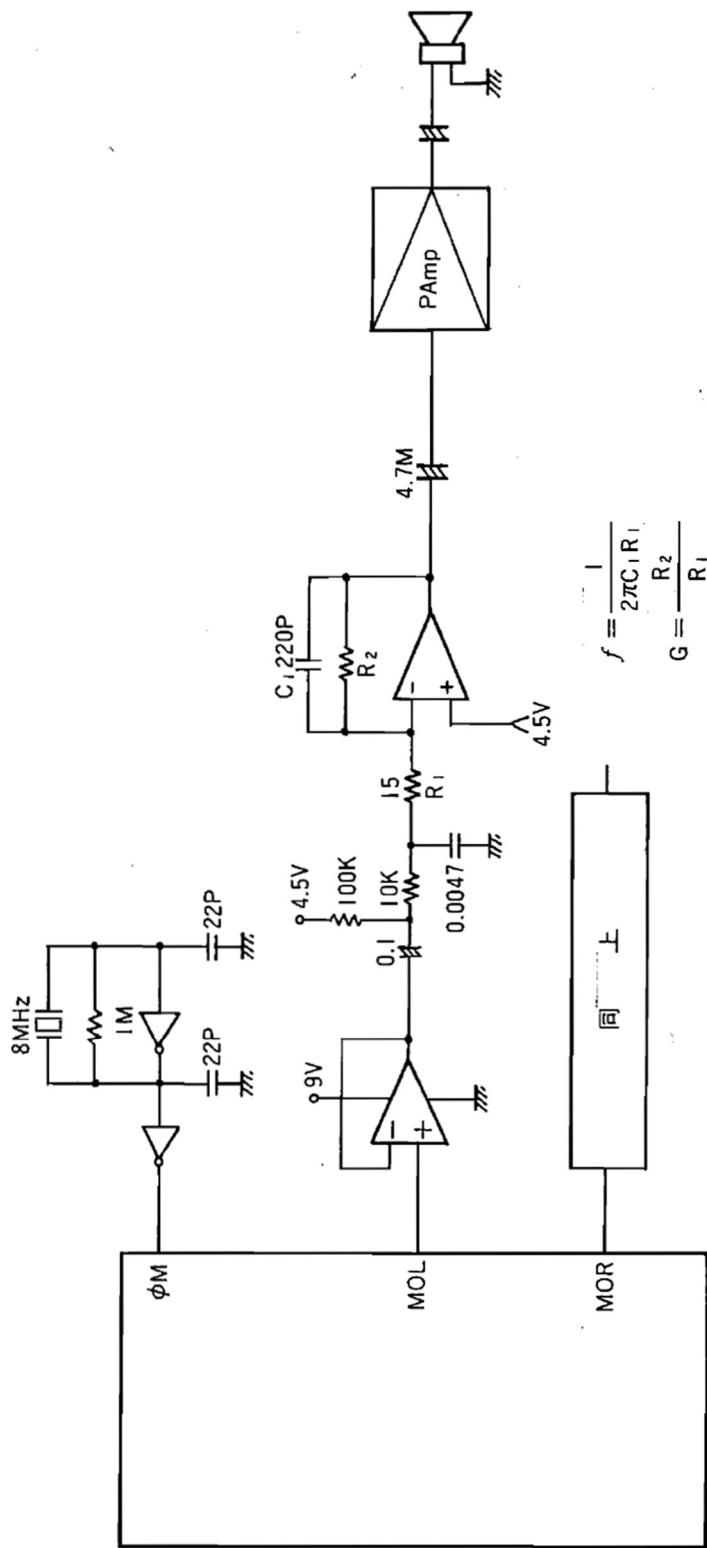
	S 1	S 2	S 3	S 4
Total level	- 2 6	- 3 3	- 3 7	0
Multiple	1	1	1	1
Detune	3	1	0	1
Attack rate	2 5	2 5	2 1	9
Decay rate	1 0	1 1	1 1	1 0
Sus level	- 1	- 4	- 2	0
Sus rate	0	0	0	0
Release rate	5	9	6	6
Key scale	1	1	1	1
Am on/off	o f f	o f f	o f f	o f f
EG control	o f f	o f f	o f f	o f f
L.F.O. 1				
Pitch E 3				
Ams 0 Pms 1				
Algorithm 2	Feed back 7			

音色名：V I B R P H N

	S 1	S 2	S 3	S 4
Total level	- 5 6	- 6	- 4 1	0
Multiple	1 2	8	7	1
Detune	- 1	- 3	0	0
Attack rate	3 1	3 0	3 1	2 8
Decay rate	1 6	1 2	4	6
Sus level	- 1 1	- 1 5	- 1	- 4
Sus rate	6	2	2	8
Release rate	7	1 0	0	1
Key scale	2	1	2	1
Am on/off	o f f	o f f	o n	o f f
EG control	o f f	o f f	o f f	o f f
L.F.O. 1				
Pitch C 5				
Ams 2 Pms 1				
Algorithm 4	Feed back 4			

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■ Reference Circuit Example



※ G is a constant setting so that the output does not clip at the time of simultaneous sounding of 6 sounds and maximum output.

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