Bandgap Reference with Minimal Temperature Dependence

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***Abstract*—This paper introduces the design of a Bandgap Reference Circuit with minimal Temperature Dependence accompanied by the simulation results of the circuit to demonstrate minimal temperature variation. Bandgap reference voltage is a commonly used circuit topology because of its ability to maintain a constant voltage regardless of the variations in power supply, temperature changes and loads. Further on, to produce a circuit with minimal temperature variation, a proportional to absolute temperature (PTAT) current was generated with a diode-connected NMOS load.**

Index Terms — Bandgap reference circuit, Proportional to Absolute Temperature (PTAT), Reference voltage

I. Introduction

BANDGAP voltages with a minimal temperature dependence are difficult to design due to the sensitivity to changes in temperature by other components in the circuit. Although the bandgap voltage is relatively temperature-independent, other components in the circuit, such as resistors can exhibit significant temperature dependence that can lead to errors in the reference voltage. [1] Mismatching between transistors and the temperature dependence coefficient of R_1 leads to variation in ID5 that deviates from an ideal current equation. [2] For this project, once the topology of the circuit was chosen, figuring out the device sizes, resistor values and BJT multiplier to achieve a minimal voltage variation over a given temperature range and generate 25 µA DC PTAT was the most challenging. A typical method that mitigates this is the Brokaw bandgap, which provides two internal voltage sources, one with a positive temperature coefficient and one with a negative temperature coefficient. It is possible to cancel the temperature dependence by summing the two together.

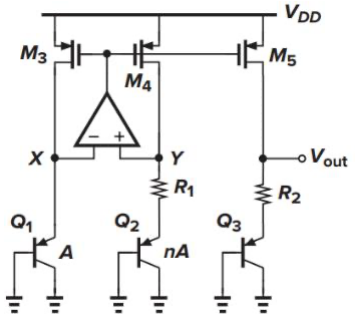

Fig. 1. Bandgap Reference with Generation of a Temperature- Independent Voltage.

II. Circuit description and analysis

A. Bandgap Reference Circuit with PTAT Current

Bandgap reference voltage circuits are one of the most commonly used circuit topologies given its versatility to produce a constant voltage regardless of variations in power supply, temperature and loads from a device. The bias current of the bipolar transistor at the output branch is disproportionate from absolute temperature whereas the current generated from the first two branches are proportional to the absolute temperature. Combining these two properties at the third branch, we can effectively generate a temperature independent voltage at the output node.

Knowing that $V^- = V^+$ we began to derive an equation to find the value of R_1, as shown below from (1) – (6).

Derivation for R_1:

$$V^- = V^+ \quad (1)$$

$$V_{BE1} = IR_1 + V_{BE2} \quad (2)$$

$$V_{BE1} - V_{BE2} = IR_1 \quad (3)$$

$$\Delta V_{BE} = IR_1 \quad (4)$$

$$V_T \ln(n) / I = R_1;\ \text{where } V_T = k_T / q = 0.026 \quad (5)$$

$$R1 = 0.026*\ln(2) / 25E\text{-}6 = 720\ \Omega \quad (6)$$

Now to solve for R_2 we use equation 12.51 from the Razavi textbook and the facts that $\partial V_{BE}/\partial T$ =-1.5 mV/K at 300 K and (k/q) = 0.087 mV/K; $V_{OUT} = V_{BE3} + mIR_2$ and take the partial derivative of V_{OUT} with respect to temperature (T). This leaves us with 0 = -1.5 mV + m*(R2/R1) * (k/q) *ln (n). By setting m = 1, R_1= 720 Ω, and n =2 and after a bit of algebraic manipulation we see that R_2 = 17909 Ω, as shown below from (7) – (14).

Derivation for R_2:

$$V_{OUT} = V_{BE3} + mIR_2 \quad (7)$$

$$V_{OUT} = V_{BE3} + m\left(\frac{V_T l(n)}{R_1}\right)R_2 \quad (8)$$

$$V_{OUT} = V_{BE3} + m\left(\frac{R_2}{R_1}\right)V_T \ln(n) \quad (9)$$

$$V_{OUT} = V_{BE3} + m\left(\frac{R_2}{R_1}\right)\left(\frac{kT}{q}\right)\ln(n) \quad (10)$$

$$\frac{\partial V_{OUT}}{\partial T}\left(V_{OUT} = V_{BE3} + m\left(\frac{R_2}{R_1}\right)\left(\frac{kT}{q}\right)\ln(n)\right) \quad (11)$$

$$0 = \frac{\partial V_{BE3}}{\partial T} + m\left(\frac{R_2}{R_1}\right)\left(\frac{kT}{q}\right)\ln(n)) \quad (12)$$

$$0 = \text{-}1.5E\text{-}3 + (1)\left(\frac{R_2}{720}\right)(0.087E\text{-}3)\ln(2) \quad (13)$$

$$R_2 = \frac{1.5E-3(720)}{(0.087E-3)(\ln(2))} = 17909\ \Omega \quad (14)$$

However, because of R_2 being too low, it caused our Temperature vs. V_{OUT} to be trending negatively so we increased the R_2 to 35kΩ. After having the voltage variation become minimal, we adjust the PMOS width at the fourth branch to 580nm to accommodate the requirement of having a PTAT current of 25 µA at room temperature (27 degrees Celsius). Our final circuit schematic is as shown below in Fig 2.

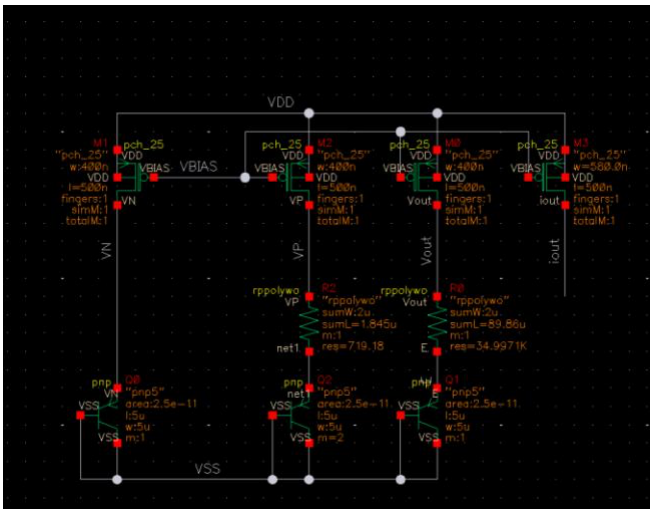

Fig. 2. Bandgap Reference Circuit Schematic

III. Results

After manipulating the R_2 resistor to achieve minimal output voltage variation across different temperature, we were able to get a small ΔV_{OUT} of just 2.7mV, with $V_{OUT, MAX}$ being 1.3777V and $V_{OUT, MIN}$ being 1.3750V.

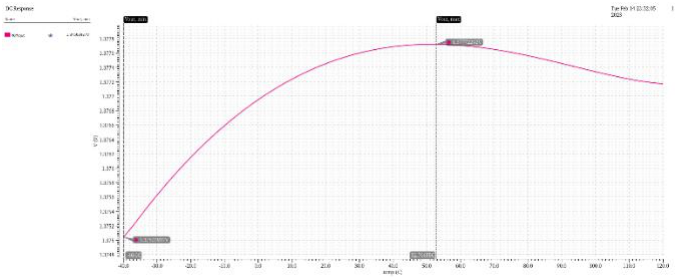

Fig. 3. V_{OUT} (V) vs. Temperature (Celsius)

Fig. 4. demonstrates the PTAT current generated at iout, with a current magnitude of 25 µA at room temperature (300K).

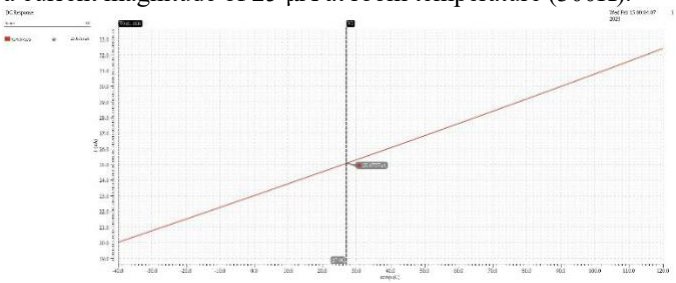

Fig. 4. iout (µA) vs Temperature (Celsius)

Table 1. Voltage Values Across Temperatures

$V_{OUT, MAX}$	1.3777 V
$V_{OUT, MIN}$	1.3750 V
V_{OUT}	1.3763 V
ΔV_{OUT}	0.0027 V
ΔV_{OUT} / V_{OUT}	0.0019 V/V

Table 2. Bandgap Reference Transisto r Sizes

Device Name	Width /Length	Multiplier	Current
M0 (PMOS)	400nm/500nm	1	18.11µA
M1 (PMOS)	400nm/500nm	1	18.74µA
M2 (PMOS)	400nm/500nm	1	18.74µA
M3 (PMOS)	580nm/500nm	1	25.08µA
Q0 (BJT)	5µm/5µm	1	ic = 9.178µA
Q1 (BJT)	5µm/5µm	1	ic = 6.018µA
Q2 (BJT)	5µm/5µm	2	ic = 12.04µA
NMOS Load	1µ/500n	1	25.08µA

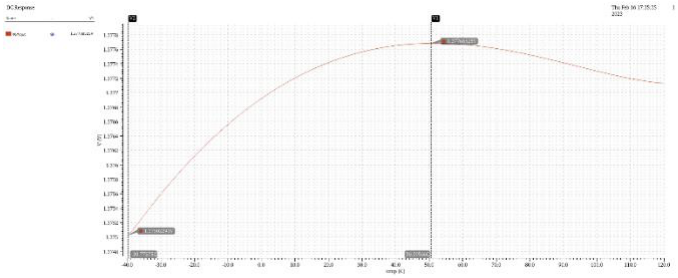

Fig. 5. V_{OUT} vs Temperature (Post Extraction)

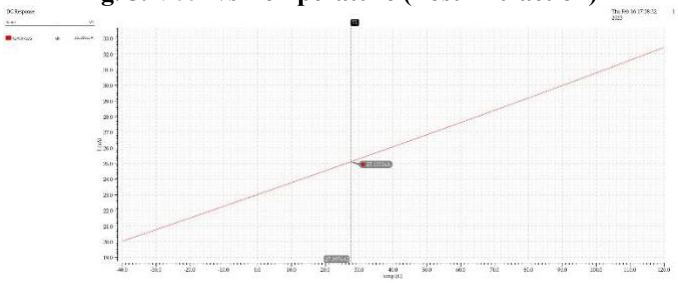

Fig. 6. iout vs Temperature (Post Extraction)

IV. Conclusions

For the design of bandgap reference circuit, on one hand we can figure out the circuit component values just by hand based on theory. However, on the other hand, we still need to figure out the way to accommodate the process parameters mismatch by tweaking resistor values in order to figure out the best solution to our bandgap circuit. We ended up having a variation of Vout of only 2.5 mV.

References

[1] R. Akshaya and S. Y. Siva, "Design of an improved bandgap reference in 180nm CMOS process technology," 2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), Bangalore, India, 2017, pp. 521-524, doi: 10.1109/RTEICT.2017.8256651.

[2] S. K. Wadhwa and N. Chaudhry, "High Accuracy, Multi-output Bandgap Reference Circuit in 16nm FinFet," 2017 30th International Conference on VLSI Design and 2017 16th International Conference on Embedded Systems (VLSID), Hyderabad, India, 2017, pp. 259-262, doi: 10.1109/VLSID.2017.52.

APPENDIX

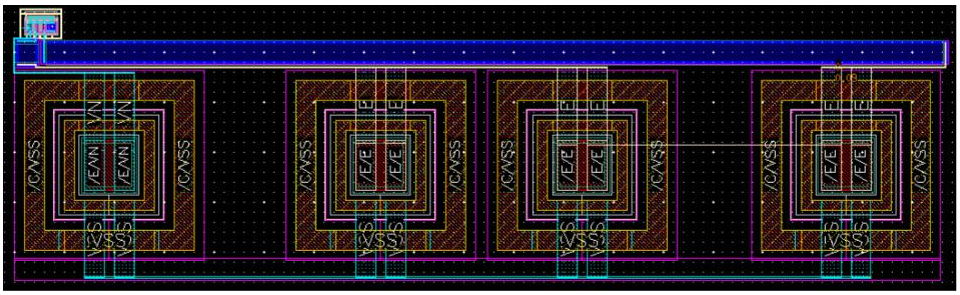

Fig. 7. Bandgap Reference Circuit Layout (Common Centroid)

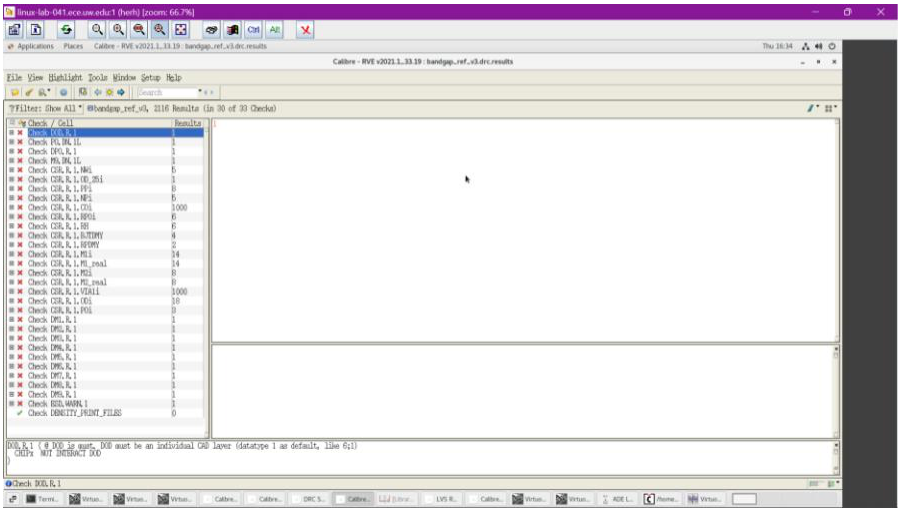

Fig. 8. DRC Result

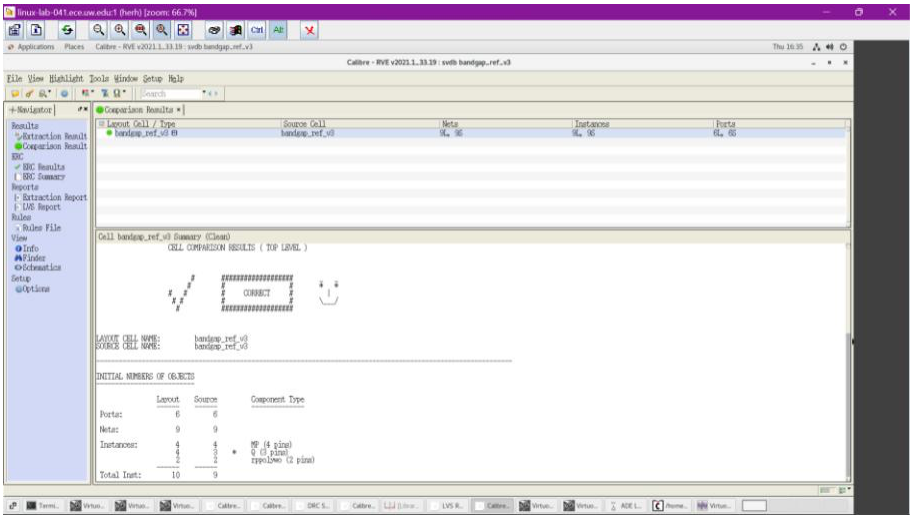

Fig. 9. LVS Check Result