DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
UNIVERSITY OF BRITISH COLUMBIA
CPEN 391 – Computer Systems Design Studio
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Tutorial 1.3: Adding SDRAM to your QSYS Project

In this tutorial, you will learn how incorporate SDRAM (Synchronous Dynamic Random Access Memory) into your QSYS project from Tutorial 1.2. You should have completed Tutorial 1.2 before starting this tutorial.

On your DE2 board, there are two types of memory. The FPGA chip itself has 483Kbits of memory on-chip. This is often called SRAM (Static RAM) and is very fast. Designers would typically use this memory for caches and to serve high-speed storage requirements. If your design is small enough, you can use some of this memory to store your program (program memory) and/or the working data (data memory) of your processor. This is what you did in Tutorial 1.2. If you remember, you specified your memory to use "on-chip RAM". This leads to a very fast processor, but for medium and large systems, you will run out of memory space very quickly. In this course, the programs you design will not fit into the on-chip memory.

The DE2 board itself has an SDRAM chip which is significantly larger (8 Mbytes). In this tutorial, you will learn how to construct a NIOS system in which the data memory and program memory are stored in this SDRAM chip. Compared to on-chip memory, this will be slower, but will allow you to write larger programs. On-chip memory will still be used for caches. If you take EECE 476, you will learn why a fast cache coupled with a slow SDRAM memory will lead to performance that is *almost as good* as a processor with only fast memory. For all designs in the rest of this course, you will use SDRAM memory.

For this tutorial, you should work through the attached tutorial from Altera. As you will learn, adding the SDRAM to your QSYS project is easy; the challenge is getting the clocking infrastructure correct. However, if you follow the instructions closely, you will not have any problems.

There is one potential error in the tutorial. In Figure 13, I had to change **sdram_clk** to **sdram_clk_clk**.