title: "Scale-Complete UFRF Guidance for Analog In-Memory Attention: S-Parameters, Projection Law, and REST-Gated Operation" author: - "UFRFv2 Collaboration" date: "2025-10-15" keywords: ["UFRF", "projection law", "S-parameters", "analog in-memory computing", "attention", "REST gating", "prime-length phasing", "noise shaping"] abstract: | We present a scale-complete engineering framework for analog in-memory attention engines that unifies scattering-parameter measurements with the Universal Field Resonance Framework (UFRF). We show how noise-looking artifacts are largely structured and technique-dependent, and we provide a concrete "Scale Ledger & Projection Budget" that spans device, cell, column, tile, SoC/clock, PDN/package/board, instrumentation, algorithm/training, and dataset/deployment domains. Central to the method are three levers: (i) operating at REST (E=B balance) which appears as an impedance match (|S11| minimum and flat group delay), (ii) enforcing E⊥B via quadrature (I/Q) and chopping, and (iii) breaking coherence with prime-length (13/26) timing to redistribute spurs. We give falsifiable predictions (√φ ≈ 1.272 efficiency/SNR window, spur reduction under 13/26 phasing, technique-dependent observables), and a measurement protocol for S(f, τ) with time-gated VNA capture. header-includes: - \usepackage{amsmath,amssymb,siunitx} - \usepackage{physics} - \newcommand{\mathrm{REST}}{\mathrm{REST}} - \newcommand{\varphig}{\varphi} - \newcommand{\mathbf{E}}{\mathbf{E}} - \newcommand{\mathbf{B}}{\mathbf{B}} - \newcommand{\mathbf{S}}{\mathbf{S}} - \newcommand{\angle}{\anglele} - \newcommand{\norm}[1]{\left\lVert #1 \right\rVert} - \setlength{\parskip}{0.45em}

1. Problem Statement and Approach

Goal. Reduce accuracy-limiting "noise" in an analog in-memory attention engine by treating it as *structured, scale-dependent projection* rather than purely stochastic disturbance. We unify the UFRF geometry (orthogonal $\mathbf{E}, \mathbf{B}$; 13-position cycle; REST at $E = B$; φ transfer window) with **scattering-parameter** practice so design, measurement, and training speak the same language.

Method in one line. *Operate at match* ($\mathrm{REST} \Leftrightarrow |S_{11}|$ minima with flat group delay), *enforce orthogonality* (I/Q + chopping), and *break coherence* (13/26 prime-length timing). Then account for **all relevant scales** explicitly in a **Projection Budget** so remaining residuals become small and structureless.

2. UFRF→S-Parameter Map (working dictionary)

- **REST $\equiv$ impedance match.** Define imbalance $\rho \triangleq \frac{|E-B|}{E+B}$. At $\mathrm{REST}, E = B$ so $\rho \to 0$ and the network view shows $|S_{11}| \downarrow$ with stationary phase (flat group delay). The UFRF transfer window gives an expected efficiency/SNR lift of $\varphi \approx 1.272$ near the match.
- **Cycle position $\leftrightarrow$ S-phase.** Use [p(\tau) \;=\; \frac{13}{2\pi}\,\angle S_{21}(f_0,\tau) \;\bmod\; 13,] to map instantaneous position on the 13-cycle; the quiet window appears near $p \approx 10$.
- **E⊥B $\leftrightarrow$ I/Q orthogonality.** Mixed-mode S-parameters (or de-embedded I/Q paths) quantify cross-coupling; minimizing I→Q, Q→I is the hardware enforcement of $\mathbf{E} \perp \mathbf{B}$.
- **Prime-length timing $\leftrightarrow$ spur shaping.** 13-slot micro-frames and 26-way interleaves spread coherent tones into weaker sidebands in $S(f)$ rather than concentrating them at harmonics/clock feedthrough.

3. Scale Ledger & Projection Budget

UFRF's projection law states that an observation is technique- and scale-relative. We therefore model the measured outcome O with an **additive projection over scales**: [\boxed{\;\ln O \;=\; \ln O^* \;+\; \sum_{k} d_{M,k}\,\alpha_k\,S_k \;+\; \varepsilon\;},] where k ranges over all relevant **scales/observers** (device, cell, column, tile, SoC/clock, PDN, package/board, instrumentation, algorithm, dataset/domain). Here $d_{M,k} = \ln(M_{\mathrm{obs}}/M_k)$ is the scale distance, $\alpha_k \in [0, 1]$ captures technique coupling, S_k summarizes systematic structure, and ε is small residual noise.

Table 1 — Minimal Scale Ledger (what to model and log)

Scale k	Typical “noise” signature	Surrogate S_k you should log	Control lever (UFRF)
Transistor/device	RTN, 1/f, g_m nonlinearity	RTN index, $1/f$ corner, HD2/HD3	Chopping; REST-biased biasing; I/Q
Gain-cell (2T1C/2T0C)	kT/C, charge injection, retention	Decay vs. refresh cadence; read disturb	REST-gated refresh; mid-swing precharge
Column/bitline	Capacitive division, coupling	Bitline RC, neighbor toggle stats	13/26 interleave; shielding
Tile/macro	Substrate/supply bounce, spurs	Spur table around carriers/harmonics	13-phase PWM; 26-way read permutation
SoC/clocking	Digital feedthrough, PLL jitter	Clock tree spectra; skew groups	Prime-phase skew groups; gated activity
PDN/VRM	Beat notes, PDN resonances	$Z_{\text{PDN}}(f)$ peaks, Q	Prime-phase VRM dithering; decap at modes
Package/board	Return-path L, board modes	Mixed-mode $S(f,\tau)$ at slot	Align reads to board-level $\lvert S_{11}\rvert$ minima
Instrumentation	Gate/IFBW bias; fixture errors	Gate placement, IFBW, de-embed meta	Time-gate to REST; consistent de-embed
Algorithm/training	Quantization, optimizer noise	Loss component spectra	Projection-aware loss; I/Q penalty
Dataset/domain	Domain shift, temp band	Token stats, temp profile	Projection head; lab→field calibration

Design rule: do **not** leave a populated row out of the sum; unmodeled scales come back as “noise”.

4. Measurement Protocol: $S(f,\tau)$ with time-gated VNA

P1 — Locate REST. Sweep the micro-frame (bias/timing) and compute $S(f,\tau)$. Mark the τ where $|S_{11}|$ is minimum and group delay is flattest. Expect a local peak in delivered power/SNR near this slot (the φ window).

P2 — Verify I/Q orthogonality. Enable dual 90° paths and acquire mixed-mode S; minimize I→Q/Q→I and confirm even-order cancellation. Chopping moves $1/f$ away from baseband offsets.

P3 — A/B timing schedules. Record spur tables under periodic vs. 13/26 timing. Expect 10–15 dB worst-spur reduction and energy re-distribution to $n/13$ and $m/26$ offsets.

P4 — Read–write coupling. Compare $\|\Delta\mathbf{S}\|$ during read when writes occur inside vs. outside REST slots. Inside-REST scheduling should reduce read-while-write disturbance.

5. Circuit & Timing Remedies (drop-in changes)

1. **REST-biased differential readout.** Precharge/read so electric and magnetic-energy proxies equalize at integration ($E=B$). Predict $\approx 2.1\,\mathrm{dB}$ SNR/efficiency lift (φ).
2. **Quadrature (I/Q) + chopper stabilization.** Two 90° paths recombined as $I+jQ$ suppress even-order distortion and push $1/f$ out of band.
3. **13-phase PWM + 26-way interleave.** Within a prime-length 13-slot micro-frame, scramble PWM edges and permute sub-tile reads (e.g., $n \mapsto n+5 \bmod 26$).
4. **REST-gated refresh; zero-bias idle.** Place writes adjacent to REST and keep unused cells at zero so decay is benign.

6. Learning & Calibration with S-Awareness

6.1 Projection-aware objective

Augment the training signal with the multi-scale projection model: [\ln O_k=\ln O_k^*+\sum_{r} d_{M,r}\,\alpha_{k,r} S_{k,r} + \varepsilon_{k}.] Learn small deltas of $\alpha_{k,r}$ while keeping $S_{k,r}$ logged from hardware (spur tables, $|S_{11}|$, phase stability, PDN modes, etc.).

6.2 I/Q consistency penalty

Enforce $\mathbf{E} \perp \mathbf{B}$ in software via an orthogonality penalty on the I and Q residuals: [\mathcal{L}_{\perp}=\lambda\,\frac{\langle r_I,\;r_Q\rangle}{\norm{r_I}\,\norm{r_Q}}.]

6.3 13/26 spectral regularizer

Bias the model against error energy at prime-length offsets: [\mathcal{L}*{13/26}=\mu\sum*\Omega\bigr)\right|^2 !\right).]} w_n\,\left(! \left|E\bigl(\omega=\tfrac{n}{13}\Omega\bigr)\right|^2+\left|E\bigl(\omega=\tfrac{n}{26

7. Predictions (falsifiable) and expected effect sizes

- **Efficiency/SNR window near REST.** $\eta_{\mathrm{REST}} = \underline{\varphi} = 1.272\ldots$ (about $+2.1$ dB).
- **Spur suppression with 13/26 schedules.** Worst spur reduced by ~ 10–15 dB vs. fully periodic scheduling, with residuals at $n/13, m/26$.

- **Even-order and $1/f$ reduction.** I/Q + chopper lowers HD2 and moves low-frequency noise out of baseband.
- **Technique dependence.** Different instruments/flows yield predictable offsets via α_k; as $S \to 0$ they converge.

8. Putting it together for an analog attention macro

For the volatile gain-cell attention block (K/V stored in capacitive cells; charge-to-pulse readout; sliding-window attention), we recommend: (i) mid-swing precharge and REST-balanced RC; (ii) I/Q chopper front-ends; (iii) 13-slot PWM edge scrambler and 26-step tile permutation; (iv) REST-gated refresh; and (v) training with the projection-aware loss and spectral/IQ penalties described above. Integrate measured $S(f, \tau)$ features into the initialization loop as fixed surrogates S_k.

9. Minimal A/B plan

1. **SPICE + behavioral**: sweep integrator bias to find REST; enable I/Q chopper; compare periodic vs. 13/26 spur tables.
2. **Bench S-params**: time-gated VNA to build $S(f, \tau)$; compute REST metrics and spur maps.
3. **HW-in-loop**: extend initialization with projection-aware loss and spectral/IQ penalties; evaluate accuracy/perplexity vs. baseline.

Appendix A — Notation and definitions

- $S(f, \tau)$: scattering parameters measured vs. frequency and micro-frame time.
- $|S_{11}|$: magnitude of input reflection (return).
- $\angle S_{21}$: phase of forward transmission.

- p: 13-position index computed from $\angle S_{21}$.
- REST: UFRF balance point $E = B$.
- $\underline{\varphi}$: square root of golden ratio (about 1.272).
- Mixed-mode S-parameters: differential/common-mode or I/Q decomposition.

Appendix B — Suggested data products to log

- Micro-frame trace of $|S_{11}|$, $\angle S_{21}$, group delay.
- Spur tables around carriers/harmonics for periodic vs. 13/26 schedules.
- PDN impedance peaks and Q; VRM phase policy.
- Package/board mixed-mode $S(f, \tau)$ at the operating slot.
- Instrumentation metadata: gate placement, IFBW, de-embedding.
- Training loss spectra and I/Q residual correlation.

Appendix C — REST identification heuristic (practical)

Compute a composite score [J(\tau)=w_1\,(|S_{11}|(\tau)) + w_2\,\mathrm{var}*f{\angle S*(f,\tau)},] where GD is group delay. REST is at $\tau^* = \arg\min_\tau J(\tau)$ (weights w_i positive).}(f,\tau)}+ w_3\,\mathrm{ripple}_f{\mathrm{GD

References (internal UFRF source set)

- UFRF core theory, axioms and first principles, Fourier connection, mathematical framework, integration summary, cross-domain validation, predictions/tests, and math appendix. These establish: $\mathbf{E} \perp \mathbf{B}$ geometry, the 13-position cycle with REST at $E = B$, the $\underline{\varphi}$ transfer window, and the projection law formalism used above.