Daniel Chen

Education

University of Toronto Expected May 2024
Bachelor of Applied Science in Computer Engineering
Relevant Coursework:

Experience

Advanced Micro Devices May 2022 – Aug 2023
ASIC Design Engineering Intern

- Implemented interface updates within the team's RTL using Verilog to support new 64-bit debug bus feature
- Investigated waveforms in Verdi and assisted the verification team in determining the functional coverage of the new debug bus feature
- Automated and revamped design checks result page to reduce manual effort and improve result visibility
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