



ECE 429 Final Exam (Take-Home)

Spring 2020

(April. 30th, Thursday, Midnight in US-Central)

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- This examination is a take-home exam.
- **Note1:** Please print out the questions and answer the questions in “Handwriting” except Question 8 (Spice Simulation). Then, scan your answer sheet and upload the scanned file to the Blackboard.
- **Note2:** For the Question 8, please submit your answer with modified source codes and simulation results including screen shots in a separate file.
- **Policy:** Final Exam report/source codes due date is at midnight on 4/30. Late submission will not be accepted. Copying assignments will call for disciplinary action. TA will run “Plagiarism Checker” and check all the source codes and time stamp of your submission.
- Good luck!

Question	Full Credit	Your Score
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
7	10	
8	30	
Total	100	



Question 1. (10 Points)

Let's say we have a $0.22 \mu\text{m}$ (micrometer) think Cu wire in a 65 nanometer process. Resistivity of the Cu is $2.2 \mu\Omega \cdot \text{cm}$ (micro-ohm·centimeter).

- a) Compute the sheet resistance of the wire

$$R_{\square} = \frac{P}{t} = \frac{2.2 \times 10^{-6}}{0.22 \times 10^{-4}} = \boxed{0.1 \Omega/\square}$$

$$\frac{1 \Omega}{\text{cm}} \rightarrow \frac{10^4 \Omega}{10^2 \text{ m}} = 10^4 \Omega/\text{m}$$

- b) Find the total resistance if the wire is $0.125 \mu\text{m}$ wide and 1mm long. (Ignore the barrier layer and dishing)

$$R_{\text{wire}} = R_{\square} \frac{l}{w} = (0.1 \Omega/\square) \frac{10^3 \text{ m}}{0.125 \times 10^{-6} \mu\text{m}} = \boxed{800 \Omega}$$

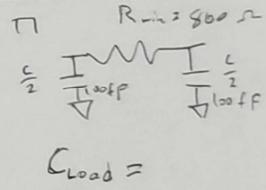
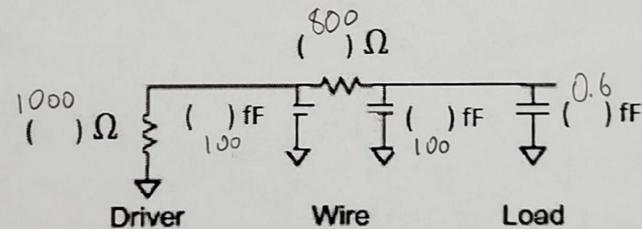
- c) Suppose that $10x$ unit-sized inverter drives a $2x$ inverter at the end of the 1mm long of the wire. Its wire capacitance is $0.2 \text{ fF}/\mu\text{m}$ and the unit-sized nMOS transistor has $R=10\text{k}\Omega$ and $C=0.1 \text{ fF}$. Complete the following equivalent circuit using a single-segment Π model.

$$C_{\text{wire}} = \frac{0.2 \times 10^{-15}}{10^{-3}} (10^5) = 200 \text{ fF}$$

$$R_d = \frac{10 \text{ k}\Omega}{10} = 1000 \Omega$$

Driver
10x2L

$$3(C_{\text{wire}}) \times 2 = 0.6 \text{ fF}$$



$$C_{\text{load}} =$$

- d) Estimate the propagation delay using a single-segment Π Elmore delay model. (neglect diffusion capacitance)

$$\begin{aligned} t_{pd} &\approx R_1 C_1 + (R_1 + R_2) C_2 = \frac{10^2}{1000} (100 \times 10^{-12}) + (1000 + 800) (100 \times 10^{-15} + 0.6 \times 10^{-15}) \\ &= 10^{-10} + (1800) (100.6 \times 10^{-15}) \\ &= 2.81 \times 10^{-10} \\ &\approx \boxed{281 \text{ ps}} \end{aligned}$$

Question 2. (10 Points)

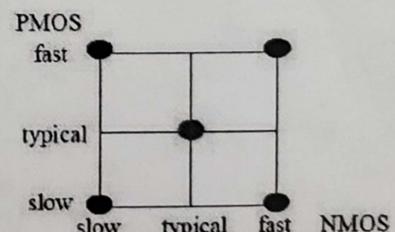
These questions are *multiple choice* questions that ask you to *select* only one *answer* choice from a list of three choices about temperature aware design in CMOSFET.

2.1) When temperature of a deeply scaled CMOS circuit is increased, then

- 1) the carrier mobility of the CMOS device will be
a) increased b) decreased c) not changed
- 2) the threshold voltage of the CMOS circuit will be
a) increased b) decreased c) not changed
- 3) the sub-threshold leakage current of the CMOS circuit will be
 a) increased b) decreased c) not changed
- 4) the depletion region of the CMOS device will be
 a) increased b) decreased c) not changed
- 5) the junction capacitance of the CMOS circuit will be
a) increased b) decreased c) not changed
- 6) the junction leakage current of the CMOS circuit will be
 a) increased b) decreased c) not changed
- 7) the active mode current (on-current) of the CMOS circuit will be
 a) increased b) decreased c) not changed
- 8) the standby mode current (off-current) of the CMOS circuit will be
a) increased b) decreased c) not changed

2.2) Following table shows critical design corners that designers should consider one of the process corners when they compensate PVT variations and close design timing and power for CMOS IC design. Choose (make a circle) one of the corners in the table in order to guarantee a chip design specification.

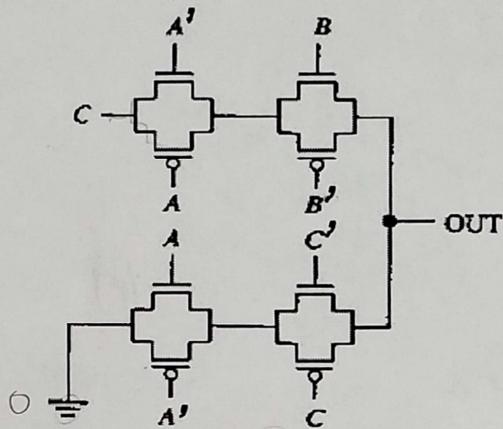
Purpose	nMOS	pMOS	V _{DD}	Temp
Cycle time	(Fast / Slow / Typical)			
Power	(Fast / Slow / Typical)			
Subthreshold leakage	(Fast / Slow / Typical)			
Pseudo-nMOS	(Fast / Slow / Typical)			



Question 3. (10 Points)

Provide a truth table that describes the functionality of each circuit in the Figure. (note: the output of the circuit may be high-Z) The symbol A' refers to the complement of A . $A' = \overline{A}$

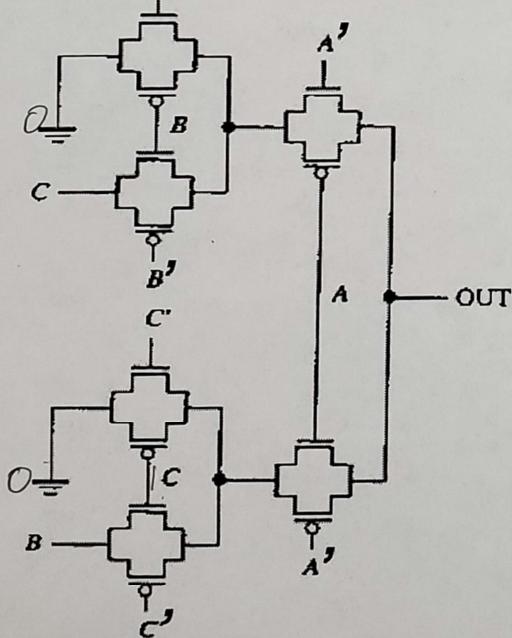
(a) $Out = \overline{ABC} + \overline{A} \overline{C} A$



A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

(b)

$$Out = (\overline{B} + BC)\overline{A} + (\overline{C} + BC)A = BC\overline{A} + BCA = BC(\overline{A} + A) = BC$$



A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

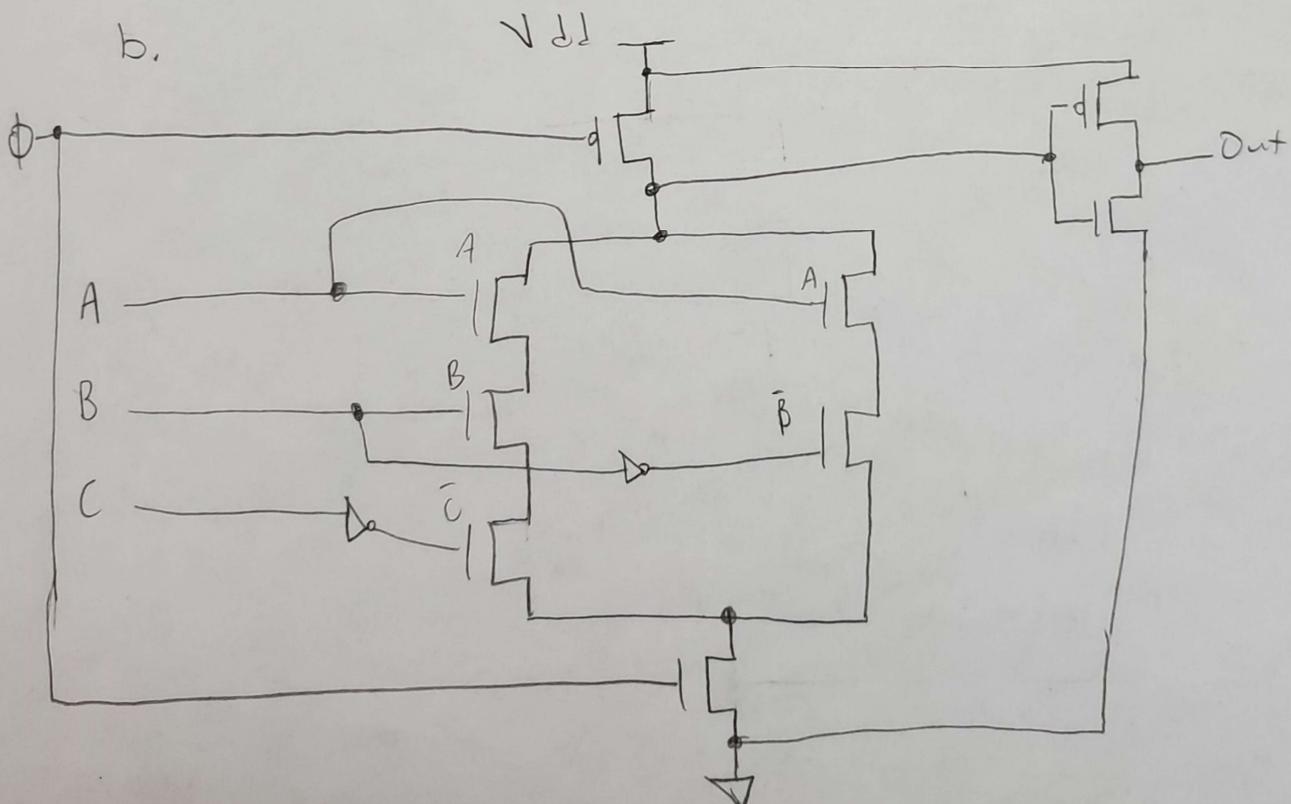
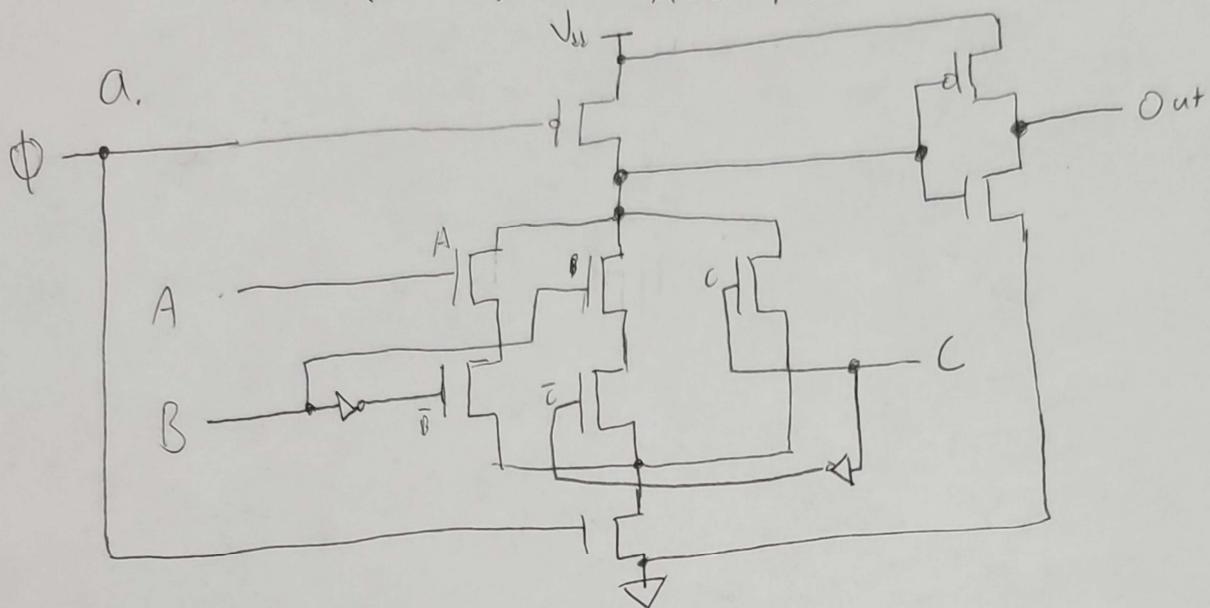


Question 4. (10 Points)

Design a domino circuit whose output is

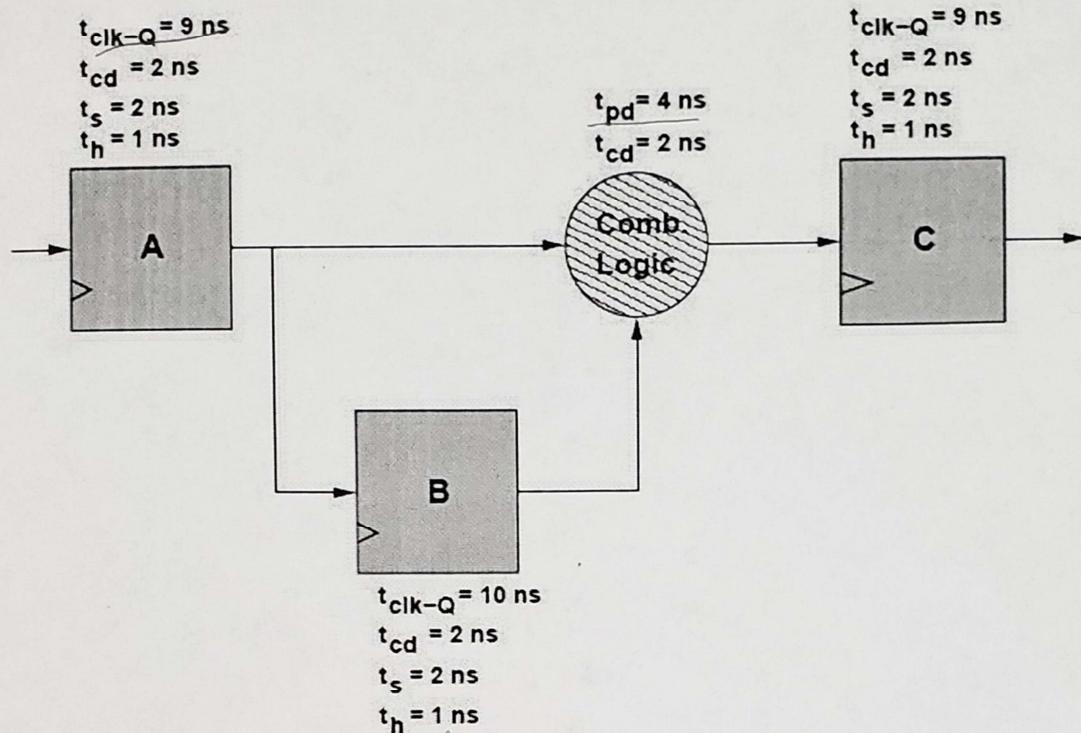
a. $Out = A\bar{B} + BC + \bar{C}$

b. $Out = (\bar{A} + \bar{B} + C) + A\bar{B} = A\bar{B}\bar{C} + A\bar{B}$





Question 5. (10 Points)



[*Note: cd: Contamination Delay, s: Setup, h: Hold time, pd: Propagation delay]

- a) Find maximum clock frequency of the above sequential circuit

$$f_{\max} = \frac{1}{t_{\min}} = \frac{1}{9 \text{ ns} + 4 \text{ ns} + 2} = 15 \text{ ns} \quad f_{\max} = \frac{1}{15 \times 10^{-9}} = 6.67 \times 10^7 \text{ Hz} = 66.7 \text{ MHz}$$

- b) Is the circuit guaranteed to work correctly without any timing violations? Explain how you can say that?

It is not guaranteed to work without timing violations due to the B-Flip-Flop



Question 6. (10 points)

PLA (Programmable Logic Array) performs any function in sum-of-products form and PLA design by ANDs and ORs is not very efficient in CMOS. Sketch a 3-input, 2-output PLA implementing following full-adder logic by using NOR-NOR PLAs. (Hint: Use DeMorgan's Law to convert to all NORs circuit.)

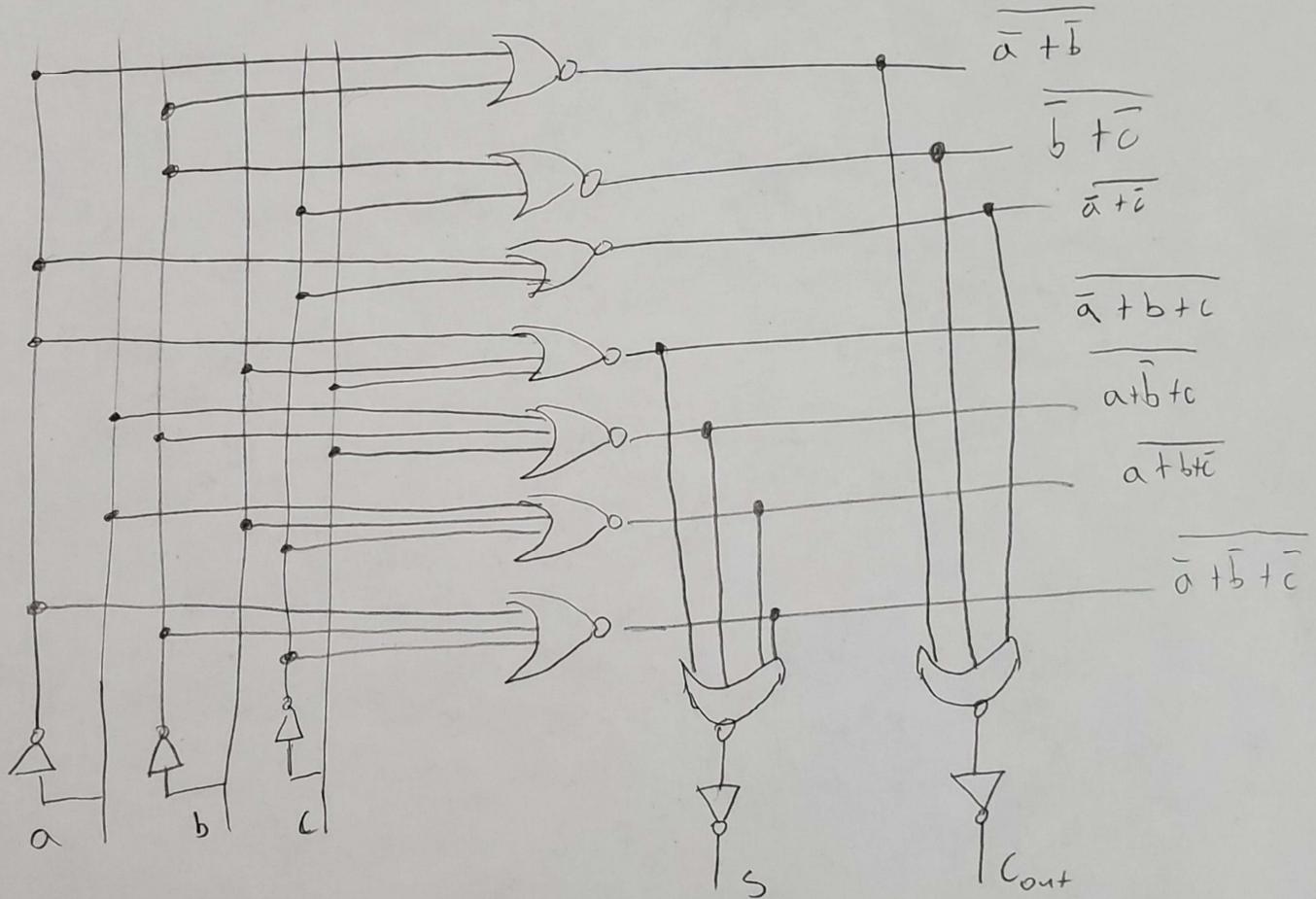
$$\boxed{A+B} = \overline{A}\overline{B}$$

$$s = ab\bar{c} + \bar{a}b\bar{c} + \bar{a}\bar{b}c + abc$$

$$c_{\text{out}} = ab + bc + ac$$

$$S = \overline{\overline{a+b+c}} + \overline{\overline{a+b+c}} + \overline{\overline{a+b+c}} + \overline{\overline{a+b+c}} + \overline{\overline{a+b+c}} + \overline{\overline{a+b+c}} + \overline{\overline{a+b+c}}$$

$$C_{\text{out}} = \overline{\overline{a+b}} + \overline{\overline{b+c}} + \overline{\overline{a+c}} = \overline{\overline{a+b}} + \overline{\overline{b+c}} + \overline{\overline{a+c}}$$





Question 7. (10 points)

Draw the logic diagram (synthesis output) using D F/F for the following HDL descriptions and evaluate the output values of b and c variables.

(a) **module blocking** (clk, a, c);
input clk;
input a;
output c;

wire clk;
wire a;
reg c;
reg b;

always @ (posedge clk)
begin
 b = a; // $b = a$
 c = b;
end

endmodule

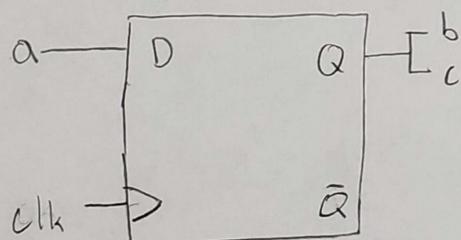
(b) **module nonblocking** (clk, a, c);
input clk;
input a;
output c;

wire clk;
wire a;
reg c;
reg b;

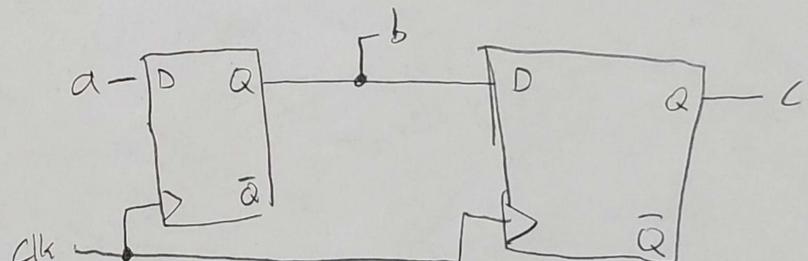
always @ (posedge clk)
begin
 b <= a;
 c <= b;
end

endmodule

a.



b.



Outputs:

$$b = a, c = b$$

$$\therefore c = a$$

for all a, b ,

$$\boxed{c = a}$$

first: $b = a$

Second: $c = b$

$c =$ previous states of b ,

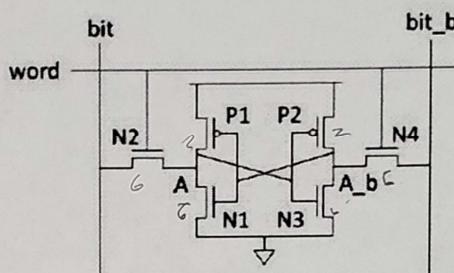
which is not equal to a .

Question 8. (30 points) – Spice Simulation Question

Please refer to the previous Spice lab session such as Lab 2,3,4 and 8 and Lec25 and Lec26. Complete the following SRAM circuit optimization procedure. Please submit your source codes of the spice net list and stimulus, simulation results, and screenshot of your simulation.

1. Design 6T SRAM cell as follow in virtuoso and simulate reading and writing operation.

(Vdd = 1.1v, Capacitance = 1f)



[Fig.1 6T SRAM]

- 1) Schematic and netlist of the 6T SRAM cell.
- 2) Plot of the Reading 0 and 1 operation (Please attach the cosmos scope result).
- 3) Plot of the Writing 0 and 1 operation (Please attach the cosmos scope result).
2. Re-simulate the reading and writing operation considering the delay.
- 1) Optimize each transistor size to minimize reading and writing delay.

TR	Size(1,2,4,6,8)
P1	2
P2	2
N1	6
N2	6
N3	6
N4	6

*Note : 1 =90nm, 2=180nm, 4=360nm, 6=540nm, 8=720nm

- 2) Plot of the Reading 0 and 1 operation (Please attach the cosmos scope result).
- 3) Plot of the Writing 0 and 1 operation (Please attach the cosmos scope result).
- 4) Delay measurement result in Hspice. (Please attach the screen shot of your delay measurement result(.mt0 file))

Operation	Original	Optimized
Reading 0		
Reading 1		
Writing 0		
Writing 1		

3. Explain 'read stability' and 'writability' by using Spice simulation.