Optimization of Quantum Boolean Circuits by Relative-Phase Toffoli Gates

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Abstract. To realize quantum Boolean circuits, Toffoli gates are often used as logic primitives. Then Toffoli gates are decomposed to physically realizable gates, i.e., CNOT, H and T gates when we consider fault-tolerant implementation. The realization cost of a T gate is huge compared to the other gates, and thus we often consider the number of T gates. We need seven T gates to decompose a Toffoli gate. However, if we allow to add some relative phases to some output quantum states, we can implement a Toffoli gate by only four T gates. Such an approximate Toffoli gate is called a relative-phase Toffoli gate (RTOF). This paper proposes an optimization method of quantum circuit by using RTOFs. When we optimize a circuit by replacing a Toffoli gate with a RTOF, some relative phase errors are added. Our method tries to correct such relative phases by using S gates.

Keywords: Relative Phase Toffoli Gate · T Gate · Optimization.

1 Introduction

To perform a quantum algorithm to solve a logical problem, we usually need to design a so-called *quantum Boolean circuit* to calculate some Boolean functions related to the target problem [1]. To realize such quantum Boolean circuits, a Toffoli gate is often used as a logic primitive. After designing a circuit by Toffoli gates, we decompose each Toffoli gate into physically realizable gates. When we consider fault-tolerant quantum computation, we consider T, H and CNOT gates as physically realizable gates, among which the cost of a T gate is considered to be very expensive. Thus, we often focus on the number of T gates which is called *T-count*.

A variant of Toffoli gate called a *Relative-Phase Toffoli gate (RTOF, hereafter)* [2] has been proposed recently. The T-count of an RTOF is only 4 whereas T-count of a Toffoli gate is 7. An RTOF can calculate the same logic function as a Toffoli gate, but the phases of some quantum basis states become different after performing an RTOF; we say that an RTOF adds *relative phase* errors. Because of the relative phase errors, we cannot simply replace a Toffoli gate with an RTOF in general, but RTOFs can be utilized when we decompose a generalized Toffoli gate because the relative phase errors can be canceled between two RTOFs in the decomposition. Therefore, we can replace Toffoli gates which do not change the state of the function of the circuit with RTOFs without adding *relative phase* errors.

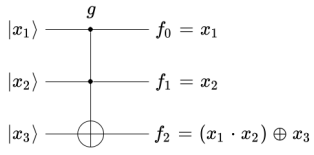

Fig. 1. Functional representations for the output of a Toffoli gate.

This paper seeks the way to replace Toffoli gates which change the state of the function of the circuit with RTOFs. More concretely, we propose a method to erase relative phase errors due to RTOFs. Then, by using our method, we may be able to decrease T-count of a circuit consisting of Toffoli gates as follows: first we replace each Toffoli gate with an RTOF gate, and then we erase the relative phase errors added by RTOFs by using our method. In the following, we present our idea how to erase relative phase errors efficiently; our method does not use T gates, but uses S gates whose implementation cost is much less than T gates.

2 Preliminary

2.1 Quantum Boolean Circuits

In this paper, we consider quantum Boolean circuits consisting of Toffoli gates, T gates, S gates and relative-phase Toffoli gates (RTOFs) [2]. Then, as we will explain later, it is enough to consider the functionality of such quantum circuits by using classical Boolean function with phase information independently.

First let us explain our notations how to represent functions in quantum Boolean circuits. We denote the primary inputs of a circuit by $x_1, x_2, \cdots, x_n$ when we have n primary inputs. Each qubit state in a circuit consisting Toffoli and RTOF gates can be represented by a Boolean function with respect to $x_1, x_2, \cdots, x_n$.

For example, Fig. 1 shows a circuit consisting of a Toffoli gate. The primary inputs are x_1, x_2 and x_3, and the functions to represent the qubit states after the gate are $f_1 = x_1, f_2 = x_2, f_3 = (x_1 \cdot x_2) \oplus x_3$ as shown in Fig. 1.

A quantum Boolean circuit calculates a Boolean function on a target qubit, and usually the other qubits should be restored to the input states if the circuit is used in a quantum algorithm. We can do so very easily by just attaching the reversed circuit of G without the gates which change the state of the target qubit on which G calculates the function. In addition, we do not have to consider the phase information of the gates of G because the relative phase errors are canceled between G and reversed circuit of G.

2.2 T Gates and S Gates

After designing a quantum Boolean circuits consisting of Toffoli gates, we need to decompose each Toffoli gate into physically realizable primitive gates. For fault-tolerant quantum computation, such primitive gates are often considered

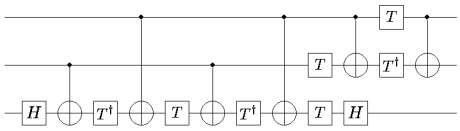

Fig. 2. A Toffoli gate by primitive gates.

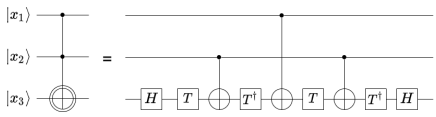

Fig. 3. An RTOF gate by primitive gates.

Table 1. Added phases by an RTOF.

input	added phase angle
000	0
001	0
010	0
011	0
100	0
101	$+\pi$
110	$+\pi/2$
111	$-\pi/2$

Table 2. An example of phase functions.

input	$F_{\pi/2}$	F_{π}	$F_{3\pi/2}$
000	0	0	0
001	0	0	0
010	0	0	0
011	0	0	0
100	0	0	0
101	0	1	0
110	1	0	0
111	0	0	1

to be CNOT, T and H gates. A T gate is a quantum-specific gate which acts on one qubit, and it adds $+\frac{\pi}{4}$ phase to the quantum state if the qubit is in $|1\rangle$. A $T^\dagger$ gate adds $-\frac{\pi}{4}$ phase.

In this paper, we also use S and $S^\dagger$ gates which add $+\frac{\pi}{2}$ and $-\frac{\pi}{2}$ phases, respectively similar to T gates. In other words, an S gate corresponds to two T gates. However, note that the realization cost of an S gate is much smaller than a T gate. Thus, in this paper, we utilize S or $S^\dagger$ gates when we need to add $+\frac{\pi}{2}$ and $-\frac{\pi}{2}$ phases.

2.3 Relative-Phase Toffoli Gates (RTOFs)

An RTOF (Relative-Phase Toffoli) gate [2] has two control bits and one target bit. It inverts the state of the target bit (i.e., $|1\rangle$ to $|0\rangle$ and $|0\rangle$ to $|1\rangle$) when the states of the both control bits are $|11\rangle$. A Toffoli gate consists of 7 T gates as shown in Fig. 2 whereas an RTOF consists of 4 T gates as shown in Fig. 3.

As Fig. 3, an RTOF has three inputs; the input quantum basis states are $|000\rangle$ to $|111\rangle$. Similar to Toffoli gates, an RTOF swaps $|110\rangle$ and $|111\rangle$. In addition to this logic operation, an RTOF adds some phases to some quantum states unlike Toffoli gates. The added phase are as shown in Table 1. For example, when the input state is $|110\rangle$, a phase $+\pi/2$ is added.

3 Optimization By Using RTOFs

To explain our method, first we need to introduce some terminologies to analyze the added phases by T ($T^\dagger$) and S ($S^\dagger$) gates in the following.

3.1 Phase Functions

Definition 1. *For an n-input quantum circuit consisting of RTOF and Toffoli gates, an* **added phase function** *is defined as a mapping from one specific pattern of n inputs, X, to the added phase to the input state corresponding to X by the circuit. In the following, we use the following notation $P(X)$ to denote an added phase function: $P(X) = \theta$ $(0 \leq \theta < 2\pi)$.*

For example, we can consider that Table 1 shows the truth table for the added phase function of the circuit as shown in Fig. 3.

We also need the following definition to explain our method.

Definition 2. *For an added phase function $P(X)$ of a quantum circuit, we define a* **phase function** *which is the following Boolean function with respect to the input variables X of the circuit:*

$$F_\theta(X) = 1 \text{ if } (P(X) = \theta),\ 0 \text{ otherwise.}$$

For example, for the added phase function as shown in Table 1, three phase functions, $F_{\frac{\pi}{2}}, F_\pi, F_{\frac{3\pi}{2}}$ can be shown in Table. 2. Note that a phase 2π is equivalent to a phase 0. Thus a phase $-\frac{\pi}{2}$ is equivalent to a phase $\frac{3\pi}{2}$.

We also use the following notation.

Definition 3. *$ON(F)$ is defined as the number of input patterns such that F becomes 1.*

3.2 Erasing Relative Phases

Now we are ready to explain our method to optimize a quantum Boolean circuit consisting of Toffoli gates. First we replace each Toffoli gate with an RTOF. Then T-count becomes 4/7 times because T-count of a Toffoli gate is 7 and T-count of an RTOF is 4. However, the circuit should have undesired added relative phases by RTOFs.

Thus our main problem considered in this paper is to erase such relative phases efficiently. For the problem, our first observation is as follows. An RTOF adds only relative phases of $\frac{\pi}{2}, \pi$ or $\frac{3\pi}{2}$. These phases corresponds to 2, 4, 6 times of applications of T gates. Because $T^2 = S$, we can cancel the above relative phases by S and $S^\dagger$ gates. Therefore our idea is to use S and $S^\dagger$ gates, and do not use T or $T^\dagger$ gates whose implementation cost would be much higher than those of S and $S^\dagger$ gates for the future fault-tolerant realization.

The outline of our method is as follows: we apply an $S^\dagger$ gate to all the input states, X, such that $P(X) = \frac{\pi}{2}$. Then we can make $ON(F_{\frac{\pi}{2}})$ to be 0. Our basic strategy to do so is to put the following sub-circuit at the beginning. The added circuit works as follows: (1) it first calculates $P(X)$ at one qubit, then (2) it applies $S^\dagger$ gate on the qubit, and (3) it calculates $P(X)$ again to reverse all the operations to calculate $P(X)$. For the states, X, such that $P(X) = \pi$ or $P(X) = \frac{3\pi}{2}$, we can modify the relative phases in similar ways where the number

of S or $S^\dagger$ gates may be different. For example, we need to apply $S^\dagger$ twice to erase phase π.

As explained, our basic strategy is to make sub-circuits to calculate functions which are used to erase the relative phases. If useful functions to erase relative phases already exist, we can utilize them instead of making new sub-circuits. Thus, we try to find a useful function f such that the ON-set of f is included in the ON-set of F_θ for some θ; we apply S or $S^\dagger$ gates appropriate times on a qubit where f is calculated in order to erase the relative phase of θ. By this operation, we can decrease $ON(F_\theta)$ with only adding S or $S^\dagger$ gates. So we try to find such useful functions and apply S or $S^\dagger$ gates as much as possible before we make the above-mentioned additional sub-circuits. The above procedure can be summarized in Algorithm 1.

Algorithm 1 Erasing Relative Phases.

Input: A quantum Boolean circuit consisting of RTOFs.
Output: A modified quantum Boolean circuit without relative phase errors.
Calculate each function after each gate, and the final relative phases for all the quantum states for the given circuit.
while a useful function f exists to decrease $ON(F_\theta)$ for each θ such that $ON(F_\theta) \neq 0$ **do**
Apply S or $S^\dagger$ gates appropriate times on a qubit where f is calculated.
end while
for $\theta = \frac{\pi}{2}, \pi, \frac{3\pi}{2}$ **do**
if $ON(F_\theta) \neq 0$ **then**
Add a sub-circuit to calculate a Boolean function $F_\theta(X)$ at the beginning.
Apply S or $S^\dagger$ gates appropriate times on a qubit where $F_\theta(X)$ is calculated.
Add a sub-circuit to calculate a Boolean function $F_\theta(X)$ again after the above S or $S^\dagger$ gates.
end if
end for

Let us show an example how our method can erase the relative phases. Suppose we are given a circuit consisting of Toffoli gates as shown in Fig. 4, and we want to optimize the circuit. The circuit has three inputs, and one ancilla qubit where we calculate a function. The function realized after each gate can be represented in Table 3. Because we have three variables, the truth table for each function has eight 0/1 entries, which can be represented by an 8-bit 0/1 string. Thus, in the table, each function is represented by an 8-bit 0/1 string. For example, the second row of column "g_1" (00111100) corresponds to $x_1 \oplus x_2$. The left-most bit of the bit string corresponds to the input pattern: $(x_1, x_2, x_3) = (0, 0, 0)$, and the right-most bit corresponds to the input pattern: $(x_1, x_2, x_3) = (1, 1, 1)$.

First we replace all the Toffoli gates in the circuit with RTOFs. Then T-count becomes 4/7 times, but some undesired relative phases are added. Note that when we design a quantum Boolean circuit we need to restore the input states (i.e., $|x_1\rangle$ to $|x_3\rangle$ in the above example). To do so, we have pairs of identical

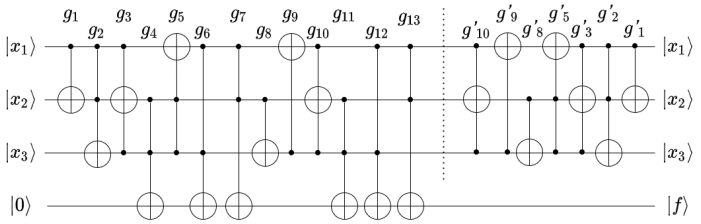

Fig. 4. Input: a circuit consisting of Toffoli gates.

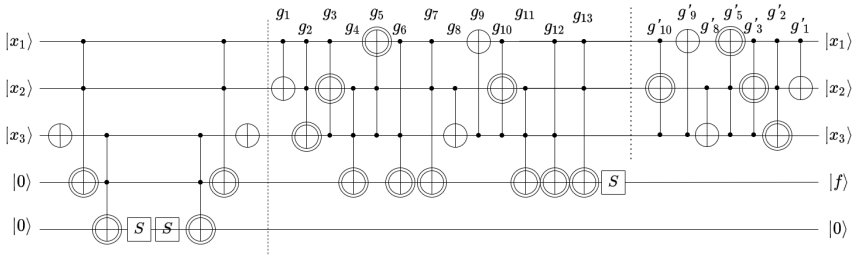

Fig. 5. Output: a circuit after erasing the relative phase errors.

Toffoli gates whose target bits are on the first three bits in this example. When we replace such a pair of two identical Toffoli gates with two RTOFs, we can cancel the added phases; we make the phases by the two RTOFs opposite. Therefore, we only consider the added phases by RTOFs whose target bits are the forth bit where we calculate the target function f in the following.

In Table 3, we show the added phase by each gate whose target bits are the forth bit in "Added Phase." "Total Phase" in a column "g_i" is the sum of "Added Phase" up to g_i. For example, "Total Phase" of the column "g_6" $(0000\frac{\pi}{2}00\frac{\pi}{2})$ means the total added phases by g_4 and g_6. The added phase function of the circuit can be represented by $P1 = 0\frac{3\pi}{2}\frac{3\pi}{2}0\frac{3\pi}{2}0\pi\frac{3\pi}{2}$. This representation is similar to the above representation for logic functions. For example, the second $\frac{3\pi}{2}$ means that the circuit adds phase $\frac{3\pi}{2}$ to state $|001\rangle$.

Then, we will erase the added relative phases by Algorithm 1. In the algorithm, we first try to find an existing function by which we can make $ON(F_\pi) = 0$ or $ON(F_{\frac{3\pi}{2}}) = 0$. The function on the forth bit after g_{13} is such a function. Thus, we put an S gate on the forth bit after g_{13} by which the added phase function of the circuit is changed to $P2 = 000000\pi0$; $ON(F_\pi)$ becomes 1.

There is no more function to erase more phases from $P2$, thus we go to the next step; we make a function $f = 00000010$ (which is $x_1 \cdot x_2 \cdot \overline{x_3}$) at the beginning of the circuit, and then we put two S gates after that in order to cancel the phase π. The transformed circuit is as shown in Fig. 5.

In this example, we can reduce T-count by $3 \times 6 = 18$ when we replace the Toffoli gates whose target bits are on the forth bit (where we calculate the target function f) with RTOFs at first. Then we need to add four RTOFs gates to erase

Table 3. The Function and Phase information after each gate in Fig. 4.

input		g_1	g_2	g_3	g_4	g_5	g_6
x_1	00001111	00001111	00001111	00001111	00001111	00010111	00010111
x_2	00110011	00111100	00111100	00111010	00111010	00111010	00111010
x_3	01010101	01010101	01011001	01011001	01011001	01011001	01011001
$\|0\rangle$	00000000	00000000	00000000	00000000	00011000	00011000	00001001
Added Phase					$000\frac{\pi}{2}\frac{\pi}{2}000$		$000\frac{3\pi}{2}000\frac{\pi}{2}$
Total Phase					$000\frac{\pi}{2}\frac{\pi}{2}000$		$0000\frac{\pi}{2}00\frac{\pi}{2}$
input	g_7	g_8	g_9	g_{10}	g_{11}	g_{12}	g_{13}
x_1	00010111	00010111	01110100	01110100	01110100	01110100	01110100
x_2	00111010	00111010	00111010	01011010	01011010	01011010	01011010
x_3	01011001	01100011	01100011	01100011	01100011	01100011	01100011
$\|0\rangle$	00011011	00011011	00011011	00011011	01011001	00111001	01101001
Added Phase	$000\frac{\pi}{2}00\frac{\pi}{2}\frac{2\pi}{2}$				$0\frac{3\pi}{2}0\pi\pi0\frac{\pi}{2}0$	$0\frac{3\pi}{2}\frac{\pi}{2}\pi0000$	$0\frac{\pi}{2}\pi\frac{3\pi}{2}0000$
Total Phase	$000\frac{\pi}{2}\frac{\pi}{2}0\frac{\pi}{2}\frac{3\pi}{2}$				$0\frac{3\pi}{2}0\frac{3\pi}{2}\frac{3\pi}{2}0\pi\frac{3\pi}{2}$	$0\pi\frac{\pi}{2}\frac{\pi}{2}\frac{3\pi}{2}0\pi\frac{3\pi}{2}$	$0\frac{3\pi}{2}\frac{3\pi}{2}0\frac{3\pi}{2}0\pi\frac{3\pi}{2}$

the relative phase errors; T-count is increased by $4 \times 4 = 16$. Therefore, in total, our method can decrease T-count by 2.

Note that in the above example we do not use Toffoli gates, but we use RTOFs to make an additional function. The reason is as follows. We can always pair two identical RTOFs in the added circuit in our algorithm. For example, in the left-hand sub-circuit before the dotted line in Fig. 5, we have two pairs of identical RTOFs. If there are two identical RTOFs, we can cancel the relative phases by swapping T and $T^\dagger$ in one RTOF so that the relative phases added by one RTOF becomes totally opposite to those by the other RTOF.

4 Conclusion

This paper proposed an optimization of quantum circuits consisting of Toffoli gates by utilizing RTOFs. Our key idea is to use $S/S^\dagger$ gates to erase undesired relative phases. Obviously our work is not completed; we need to apply our optimization methods to benchmark circuits to analyze how our method can optimize circuits.

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