Overview of IEEE-STD-1241 "Standard for Terminology and Test Methods for Analog-to-Digital Converters"

Steven J. Tilden, Thomas E. Linnenbrink, Philip J. Green
On Behalf of the IEEE TC-10 ADC Sub-Committee
Burr-Brown Corporation, 6730 Tucson Blvd., Tucson, AZ 85706
Q-DOT Inc., 1069 Elkton Drive, Colorado Springs, CO 80907-3579
Sandia National Laboratories, MS0980, Albuquerque, NM 87185-5800
Phone (520) 746-7587, Fax (520) 746-6033, email: tilden_steve@burr-brown.com

Abstract

IEEE-STD-1241 [1] has been drafted and is being revised this year to prepare for ballot and publishing. A year ago, the IEEE office asked us to also coordinate it's release with the IEC to make it a full International standard. We have been diligently working this requirement to ensure acceptance and use by engineers throughout the world. This paper introduces this soon-to-be-published standard for your review and comment in the hopes you will embrace it and help us make it useful to anyone who needs to characterize Analog-to-Digital-Converters (ADC's). ADC's may exhibit many unique characteristics due to the numerous features and wide range of application uses. It became apparent many years ago that there were inconsistencies between the way ADC's were specified and tested, which created the need for standardization. To help solve these issues, the IEEE formed a working group of dedicated experts to draft and edit a standard that could be used for many years and meet the needs of all users.

Introduction

This Standard is intended to provide a guide for the testing and evaluation of analog-to-digital converters (ADCs). This Standard is written for use by engineers who have a Bachelors of Science degree (or equivalent), but who have little experience. This Standard identifies ADC error sources and provides test methods with which to perform the required error measurements. The information in this Standard is useful both to manufacturers and users of ADCs in that it provides a basis for evaluating and comparing existing devices, as well as providing a template for writing specifications for the procurement of new ones. In some applications, the information provided by the tests described in this Standard can be used to correct ADC errors, e.g., gain and offset errors.

This Standard is divided into four chapters plus annexes as shown in Figure 1, the Standard's Table of Contents. Chapter 1 is a basic orientation. For further investigation, users can consult Chapter 2, which contains references to other IEEE standards on waveform measurement. The definitions of technical terms, abbreviations, and symbols used in the Standard are presented in Chapter 3. Chapter 4 presents a wide range of tests that measure the performance of an ADC. Annexes containing the bibliography and informative comments on the tests presented in Chapter 4 augment the Standard.

Figure 1: IEEE STD 1241 Table of Contents

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To verify an ADC's suitability for an application, the user must select a proper set of experiments with which to test the converter. To aid in the selection of test parameters, a table was created in the Standard titled "Critical ADC System Specifications". It is presented below as Figure 2.

The user of the Standard can look up an application here and see a summary of tests generally performed. Having these tests selected, they can then be grouped by test method, the measurements taken, and the results of these select experiments can then be calculated. Most of the test methods presented in this Standard can be altered to span wide ranges of amplitude, frequency, phase, temperature and power supply voltages to adequately characterize the ADC's performance throughout the range of intended use.

As an example for this paper, we will first select the initial application called "Spread Spectrum" which will allow us to test Signal-to-Noise-And-Distortion (SINAD), Spurious Free Dynamic Range (SFDR), and Inter-Modulation Distortion (IMD).

Figure 2. Critical ADC System Specifications

Typical Applications	Critical ADC Specifications	Performance Issues
Spread spectrum	SFDR, SINAD NPR, IMD Noise-to-Distortion Ratio	SINAD & IMD for quantization of small signals in a strong interference environment. SFDR for spatial filtering. NPR & IMD for inter-channel cross talk.

Image processing	DNL, Out-of-range recovery Full-scale step response	DNL for sharp-edge detection. Recovery from blooming.
Wide-band digital receivers, COMINT, ELINT, SIGINT	SFDR SINAD IMD	Linear dynamic range for detection of low-level signals in a strong interference environment.
Radar	IMD, SFDR, SINAD, Out-of-range recovery	SINAD for clutter cancellation and Doppler processing.
Infrared imaging	DNL, INL, SINAD	High-resolution at switching rate.
Tele-communication, Personal communications	SINAD, NPR, IMD, SFDR Word error rate	Wide input bandwidth channel bank. Inter-channel cross talk. Compression. Bit error rate.
Spectrum analysis	SFDR, SINAD	SFDR and SINAD for high dynamic range measurements.
Digital oscilloscope/ Waveform recorder	DNL, SFDR, SINAD, ENOB Bandwidth, Out-of-range Recovery, Word error rate	SINAD for better wide bandwidth amplitude resolution. SFDR to minimize distortion. Bit error rate.
Video	DNL, INL, SINAD, SFDR DP, DG	Linear with low distortion. Differential gain and phase errors.
Audio	IMD, SINAD, THD	Cross talk & gain matching. Power response.
Automatic control	Mono-tonicity, IMD Short-term setting	Transfer function. Inter-channel cross talk.
Geophysical	THD, SINAD Long-term stability	Low distortion. Sub Hertz response.

COMINT = communications intelligence
DG = differential gain
DNL = differential non-linearity
DP = differential phase
ELINT = electronic intelligence
IMD = inter-modulation distortion
INL = integral non-linearity
NPR = noise power ratio
SFDR = spurious free dynamic range
SIGINT = signal intelligence
SINAD = signal-to-noise and distortion ratio
THD = total harmonic distortion

Test Setups and Methods

With these tests in mind, we must determine the equipment and setup to be used. The Standard offers three general test setup diagrams, which provide a means to test the majority of the test parameters in the Standard. We will select the first setup, which is used primarily for sine wave testing. It is important at this time to clarify the definitions of a few parameters as they are currently defined in the Standard.

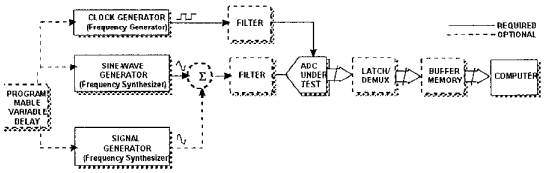

Figure 3: Setup for sine wave testing.

Signal-to-Noise And Distortion ratio (SINAD): For a pure sine wave input of specified amplitude and frequency, the ratio of the RMS amplitude of the ADC output signal to the RMS amplitude of the output noise. Noise is defined to include not only random errors but also nonlinear distortion and the effects of sampling time errors. SINAD in Standard 1241 is equivalent to SNR in Standard 1057[2]. In the context of ADCs, the term SNR is ambiguous, since it has been used to represent both SINAD and SNHR; therefore, it is currently replaced by SNHR in Standard 1241.

Effective number of Bits (ENOB): This is derived directly from the SINAD number with the formula:

$$ENOB = (SINAD - 1.74) / 6.02 \qquad \text{(eq. 1)}$$

Signal to Non-Harmonic Ratio (SNHR): For a pure sine wave input of specified amplitude and frequency, the ratio of the Root Mean Square (RMS) amplitude of the ADC output signal to the RMS amplitude of the output noise which is not harmonic distortion. (This is the definition for SNR as used by many manufacturers and users).

Spurious free dynamic range (SFDR): is the ratio of the amplitude of the ADC's output averaged spectral component at the input frequency, f_T, to the amplitude of the largest harmonic or spurious spectral component observed over the full Nyquist band, Max.{$|X(f_h)|$ or $|X(f_S)|$}:

$$SFDR(dB) = 20\log_{10}\left(|X_{avg}(f_r)| / \max_{f_{SP},f_H}\left\{|X_{avg}(f_H)| \text{or} |X_{avg}(f_{SP})|\right\}\right)$$

(eq. 4.4.5.8 of Std 1241)

where:

X_{avg} is the averaged power spectrum of the ADC output,

f_r is the input signal frequency,

f_H and f_{SP} are the frequencies of the set of harmonic and spurious spectral components.

Returning to our example, notice the optional filters at the input to the ADC under test. These were necessary, as

the sine wave generators did not provide the spectral purity we needed. The clock generator output may also be filtered or shaped to provide the edge slew rate and clarity we will need to obtain the performance we expect. This setup will allow us to test SINAD, SNHR and SFDR. A test bench like the one in Figure 3 was setup using a customer demonstration board provided from the manufacturer' of the ADC we chose to test. To ensure the minimum clock slew rate was met, a pulse generator was used in place of the optional filter shown at the output of the clock generator. A 7th order band pass filter was used to improve the harmonic spectral output of the signal generator applied to the input of the ADC under test. Care was taken to ensure the power supplies were applied within the specified range in the product data sheet. The generators were then set up to apply a CMOS-leveled clock signal of 50MHz and an input sine wave amplitude between the top and bottom reference of the ADC under test. The input signal generator frequency was set to approximately 10MHz according to the coherent sampling formula in the Standard.

$$f_s \cdot J = f_r \cdot M \qquad \text{(eq. 3.1.0.2 of Std 1241)}$$

where, f_s = the sampling frequency,
J = the integer number of cycles of the waveform in the data record,
f_r = the reciprocal of the period of the waveform
M = the number of samples in the data record.

When this relationship cannot be met, provision is made for the use of many other windows, although caution is expressed to accurately know the effects of the windows on the results. The number of bins counted on either side of the fundamental carrier, and the first decade of harmonics can greatly effect the results given for Signal to Non-Harmonic Ratio (SNHR), SINAD and THD. In this example, a 10MHz full-scale sine wave was sampled at 50MHz by a 12 bit Burr-Brown ADS807. The sample size of 2048 was chosen due to the limits of the capture memory size. A record of data was taken and a FFT was performed to generate a frequency spectrum. Notice in Figure 4 that the fundamental carrier sine wave was adjusted so the input was a large signal between 0.5dB and 1.0dB below full scale, to prevent saturation. 10MHz. In our example, as shown in Figure 3, we saw that the SINAD is approximately 68dB when referenced to full-scale and that the SFDR was estimated to be 82dBFS at the 3rd harmonic observed at approximately 30MHz (folded back to around 20MHz).

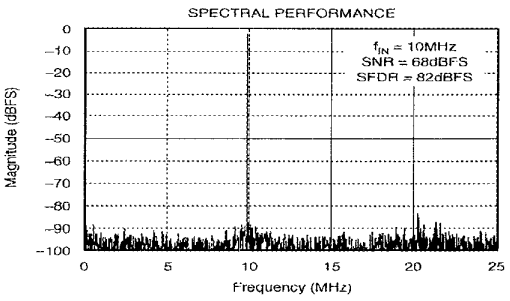

Figure 4: Burr-Brown ADS807 Spectral Performance at 50MS/s with an input of 10 MHz.

To test the IMD of the converter, the 2nd signal generator of Figure 3 is used to allow two tones of differing frequencies. As in the first test, filters are required on the signal generators to improve the harmonic performance, to well above the expected ADC's spectral performance.

In this case, setting all three generators to coherent frequencies is more difficult. We wish to provide inputs at 12MHz and 13Mz and still sample at 50MHz. Using equation 3.1.0.2 again, we adjust the clock frequency to be coherent to the 12MHz tone and then adjust the 13MHz tone to be coherent to the clock frequency thus avoiding the use of windows to stop spectral leakage . The amplitudes of the signal generators are adjusted to half the signal amplitude of the single generator used in the single tone test. This ensures the power envelope is not saturated by either tone when their phases cross at peak amplitude. A record of data is again taken and FFT performed. The 2nd, 3rd and 4th order inter-modulation products are computed. Each is then subtracted from the larger of the two input tone amplitudes and the results are then reported in dBc, referenced to the carrier signal amplitude. In this case, the Burr-Brown ADS807 exhibited a 3rd order IMD product of -71dBc below the two carrier signals as seen in figure 5.

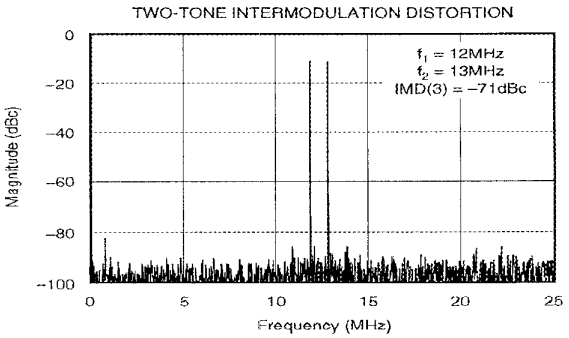

Figure 5. Burr-Brown ADS807 IMD Spectrum.

For our next example, we will look at an infrared imaging application where Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are important. Linearity tests can be performed several different ways.

For high speed ADC's like the one in our previous example, the sine wave histogram method is highly desirable. Here the setup from Figure 3 can again be used with a slight modification. We must adjust the amplitude of the sine wave such that we both under drive and overdrive the converter's entire input signal range to span the entire dynamic range and produce all output codes of the converter. This requires both amplitude and offset adjust controls be in place at the signal generator or summer. In Standard 1241 we recommend the use of the cumulative histogram method which provides relief on setting the exact amplitude, as it is very difficult to adjust to the precision necessitated by earlier methods. Also, in this case, we will adjust the coherent frequency for a much larger record size to ensure we 'walk' through all the output codes of the ADC equidistantly. This will provide adequate coverage and counts per code to give us a relatively accurate estimation of the ADC's linearity. In reality, our capture buffer is limited, so several records will need to be captured and then sorted into the corresponding histogram bins. This offers suitable randomness to give us a minimum number of counts per bin. For a 12 bit ADC, we need enough records to form a total sample size of approximately 4.2 million as estimated by the formula given in reference [3].

Once the data records have been captured, and the counts accurately sorted into the respective code bins, we can estimate the DNL and INL errors by using the formulas given in reference [1] and then plotted as shown in Figure 6 for DNL error and Figure 7 for INL error.

The authors of Standard 1241 thought it prudent to provide alternate methods for evaluating the linearity of ADC's, besides the popular sine-wave histogram method. An alternate ramp histogram method and a feedback method are suggested to allow selection of the best fit for different ADC architectures. These are all shown to provide the ability to estimate the ADC's offset, gain, integral and differential linearity errors. The different methods are shown to optimize the evaluation of different ADC architectures and can also be selected to optimize the time necessary to accurately evaluate the ADC's performance. This is particularly useful in today's environment where multiple channels in ADC's are becoming common.

With either the sine wave histogram, the ramp histogram or similar non-feedback methods, several channels and multiple ADC's can be tested in full parallel fashion. Feedback methods like the servo loop method, which senses the ADC's output codes after each

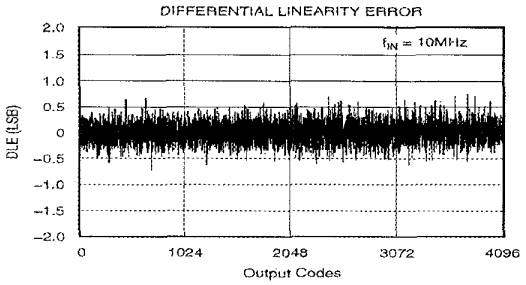

Figure 6. DNL error of the Burr-Brown ADS807 12 bit 50MHz ADC when sampling a 10MHz sine wave.

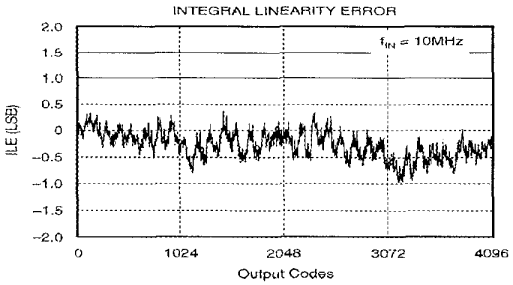

Figure 7. INL error of the Burr-Brown ADS807 12 bit 50MHz ADC when sampling a 10MHz sine wave.

conversion and varies the input stimulus, cannot be used in multiple channel testing without the duplication of complicated circuitry. They are, however, much more suited to higher resolution converters with lower sample rates that require a longer time constant to average out the noise present at the input of the ADC under test.

The Standard also provides another test setup, similar to the sine wave example, except the signal generators have been replaced with an Arbitrary Waveform Generator (AWG) composed of a Digital-to-Analog Converter (DAC) which can be used for locating code transitions and static transfer curve testing. This setup is shown in figure 8 and can also be used for slow step response tests which facilitate the need for using the equivalent time sampling test method to sample sharp edges.

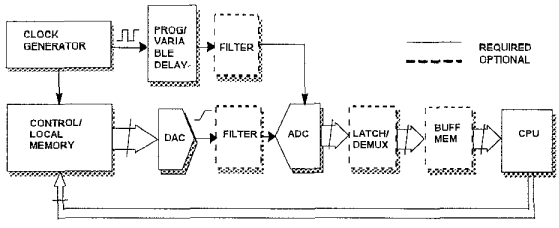

Figure 8. Test Setup for Arbitrary Signal Testing.

Finally, another setup is supplied for pulse and step signal testing where higher slew rates are required. This setup is shown in figure 9 and is used for step response testing. Here the user can adjust the slope of the input step for the slew rate desired to adequately characterize the ADC tracking ability. As time domain tests are less common for ADC testing, space does not allow us to cover them in this paper.

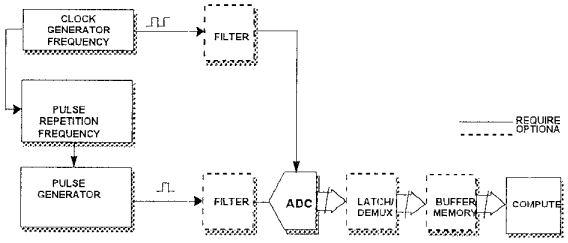

Figure 9. Test Setup for Pulse & Step Signal Testing.

ADC Test Methods not in IEEE-STD-1057

One of the test methods presented in the ADC Standard unique to ADC applications is the noise power ratio (NPR) test. This is covered in detail by another paper in this special session. This is of particular use in applications where the ability of the ADC to detect small signals in the presence of large interference signals is of importance.

Differential gain and differential phase are important parameters to understand for an ADC's use in video applications. A test method suitable for both the "National Television Standards Committee" (NTSC) and for the "Phase Alternation Line" (PAL) video standards is presented. With different input signal conditioning, the ADC input range can be mapped to a standard level of 140 IRE. Figures 9 and 10 show the setup and typical output results for these tests.

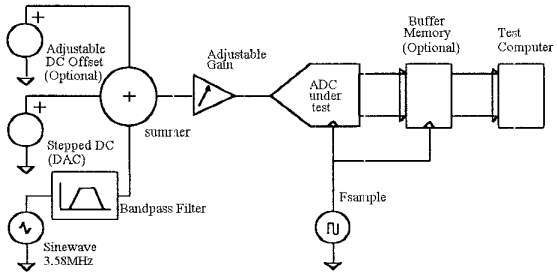

Figure 10. Setup for Differential Gain and Phase testing.

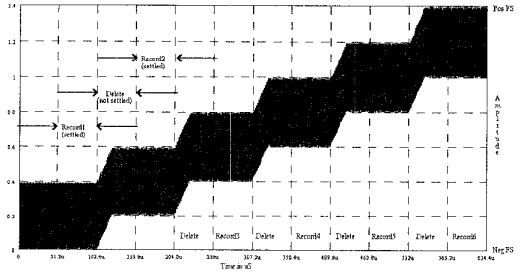

Figure 11. Example of Stepped Sinusoidal Waveform used in Differential Phase and Gain Test.

Comments and feedback

IEEE TC-10 plans to submit Standard 1241 to the IEC with the hope that it will evolve into an IEC standard. To that end, in 1998 TC-10 informally submitted preliminary drafts of 1241 to international groups who are also interested in ADC standards. As a result, TC-10 received reviews from IMEKO TC-4 (EUPAS) and DYNAD. These critical, provocative reviews are greatly appreciated by TC-10 and we welcome comment by other groups interested in reviewing the draft Standard. Please contact the authors for copies.

The papers following this one address various aspects of the draft Standard. They include robust sine wave fitting, the use of DFT in ADC testing, characterizing a state-of-the-art ADC, and measurement of noise-power ratio (NPR). Finally, some of the test methods described in Standard 1241 will be demonstrated in real time.

Summary

We have given the reader a brief overview of the current status of IEEE-STD-1241. We have shown our intent to expand its usefulness internationally and are open to your help in improving Standard 1241.

References

[1] IEEE-STD-1241 Draft - "Standard for Terminology and Test Methods for Analog-to-Digital Converters"

[2] IEEE-STD-1057-94 - "Standard for Digitizing Waveform Recorders"

[3] "Full Speed Testing of Analog-to-Digital Converters"- Joey Doenberg, IEEE transactions, 1978