Simple and Time-Effective Procedure for ADC INL Estimation

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Abstract—This paper deals with a novel testing technique aimed at estimating the accuracy of analog-to-digital converters (ADCs). The main advantage of the proposed approach is the higher testing speed, particularly the ability to achieve an accurate estimate of the low-frequency component (LCF) of the integral nonlinearity (INL) pattern of an ADC in a time that may be even one order of magnitude shorter than that of other standard techniques such as the sine wave histogram test (SHT). The estimation accuracy associated with the testing procedure is determined theoretically and validated by means of simulations and experimental results.

Index Terms—Analog-to-digital converters (ADCs), equivalent noise bandwidth (ENBW), integral nonlinearity (INL), sine wave histogram test (SHT).

I. INTRODUCTION

TESTING and characterizing analog-to-digital converters (ADCs) is still a challenging issue for mixed-signal device manufacturers, both in terms of time and cost. Indeed, 15% to 20% of the unit selling price of ADCs is due to testing procedures [1]. Generally, the goal of such procedures is to verify in a short time whether a given ADC meets its performance requirements. Testing time is related to the test setup as well as to the size of the data records to be collected and transferred to an automatic testing equipment (ATE), where parameter estimation is actually performed. As known, many techniques in the time, frequency, and amplitude domains have been proposed for ADC testing [2]. In particular, when the input stimulus can be modeled as a random variable with a known probability density function, ADC transition levels and integral nonlinearity (INL) errors can be estimated by means of histogram-based procedures of the ADC output codes. If the input test signal is a high-accuracy sinusoid, the testing procedure is referred to as a sine wave histogram test (SHT). The SHT is widely adopted by ADC manufacturers for reasons given in the following list.

1) The theoretical and computational complexity of the procedure is very low.

2) The sinusoidal stimuli can be generated easily.
3) The INL estimator is almost unbiased, and its variance is close to the Cramer–Rao lower bound [3], [4].

Unfortunately, an accurate estimation of high-resolution ADCs usually requires a large number of samples, i.e., it is expensive and time consuming. In this paper, a new testing procedure, which is referred to as fast sine wave histogram test (FSHT), is presented. The proposed solution is based on the observation that any INL pattern consists of both a low code frequency (LCF) contribution and a high code frequency (HCF) component [5]. Compared with other testing techniques based on either analytical models [5], [6] or frequency-domain analyses [7], [8], the FSHT enables a simple, fast, and very accurate estimation of the LCF of the INL pattern by suitably filtering the INL sequence obtained using a standard SHT over a reduced number of test samples. If the INL sequence exhibits a low-frequency spectral content, which is quite a mostly common case [5], [9], the FSHT also returns a good estimate of the whole INL sequence within given accuracy boundaries, provided that the bandwidth of the filter is chosen appropriately. In the succeeding sections, the theoretical steps underlying the FSHT are first described. Then, the testing results of a simulated and a real 16-bit ADC are reported and compared.

II. FAST SINE HISTOGRAM TEST

A. Theoretical Analysis

As known, the SHT is commonly employed to estimate the transition voltages T_k, $k = 1, \ldots, N-1$ of a B-bit ADC with $N = 2^B$ output codes. Basically, the SHT relies on the acquisition of a large record of low-distortion sinusoidal samples affected by a small amount of additive white Gaussian noise (AWGN). Such ADC output codes are used to build a cumulative histogram, whose kth column c_k represents the total number of acquired samples that exhibit an output code equal to or lower than k. As the probability density function associated with the input stimulus is known, the estimators $\hat{T}_k$ and $\hat{\mathrm{INL}}_k$ of the actual transition level T_k and of the corresponding INL value expressed in least significant bits (LSBs) are represented as random variables defined, respectively, as [2]

$$\hat{T}_k = d - A \cdot \cos\left(\pi \frac{c_k}{M}\right), \qquad k = 1, \ldots, N-1 \quad (1)$$

and

$$\hat{\mathrm{INL}}_k = \left(\hat{T}_k - T'_k\right)/\Delta, \qquad k = 1, \ldots, N-1 \quad (2)$$

where M is the size of the collected record, A is the amplitude of the test sinusoid, d is the offset of the input waveform, T'_k is the ideal kth transition voltage, and $\Delta = \text{FSR}/2^B$ is the ideal code-bin width of the ADC under test, which has a full-scale range equal to FSR. Thus, the whole estimated INL pattern can be modeled as

$$\hat{\text{INL}}_k = \text{INL}_k + \varepsilon_k, \qquad k = 1, \ldots, N-1 \qquad (3)$$

where INL_k is the sequence of unknown ADC INL values, and ε_k for $k = 1, \ldots, N-1$ is a random vector whose elements are the INL estimation errors. Of course, such errors affect INL estimators with both a systematic bias and a random uncertainty contribution. However, the estimator bias can be made negligible by overdriving the ADC with a sine wave whose peak-to-peak amplitude is suitably larger than FSR, whereas the variance of the random contribution is [10]

$$\begin{aligned}
\sigma_{\varepsilon_k}^2 &= \sigma_{\hat{\text{INL}}_k}^2 \\
&\cong \frac{1.78\sigma}{M \cdot \Delta^2} \sqrt{A^2 - (\hat{T}_k - d)^2} \\
&\leq 1.78 \cdot \frac{A\sigma}{M \cdot \Delta^2}, \qquad A \geq |\hat{T}_k - d| \qquad (4)
\end{aligned}$$

where σ is the standard deviation of the AWGN superimposed to the test sine wave, and $\hat{T}_k$ is the estimate of the kth transition voltage. If U_{INL} is the INL target expanded uncertainty expressed as a fraction of Δ and K_p is the coverage factor corresponding to a coverage level p [11], the data record size M required to estimate the transition voltages within U_{INL} using a standard SHT can be obtained by inverting (4), i.e.,

$$M \geq \frac{1.78 A \sigma K_p^2}{\Delta^2 \cdot U_{\text{INL}}^2}. \qquad (5)$$

Because $\Delta = \text{FSR}/2^B$, M tends to increase exponentially with the number of bits of the converter, thus causing a corresponding increment in testing time. In order to tackle this problem, the FSHT procedure enables a significant testing speedup by processing an INL pattern estimated from a single data record whose size is much smaller than the value given by (5). In fact, when the spectral content of an INL pattern is mostly due to the LCF component, the pattern itself can be estimated within a known U_{INL} simply by lowpass filtering the sequence resulting from (3). As the filter should not cause either amplitude distortion or delays within the band of interest, both its amplitude and phase responses should be constant and equal to one and to zero, respectively, in the code-frequency domain. Observe that the variance of the filtered INL estimators depends not only on the filter characteristics but also on the stochastic properties of ε_k, which are related to both the position of k in the output code domain and the amplitude of the AWGN superimposed to the test stimulus. In particular, when the noise amplitude is quite smaller than the code-bin width, the estimation errors ε_k tend to be uncorrelated and identically distributed. Conversely, if the noise amplitude is larger than Δ, the estimation errors
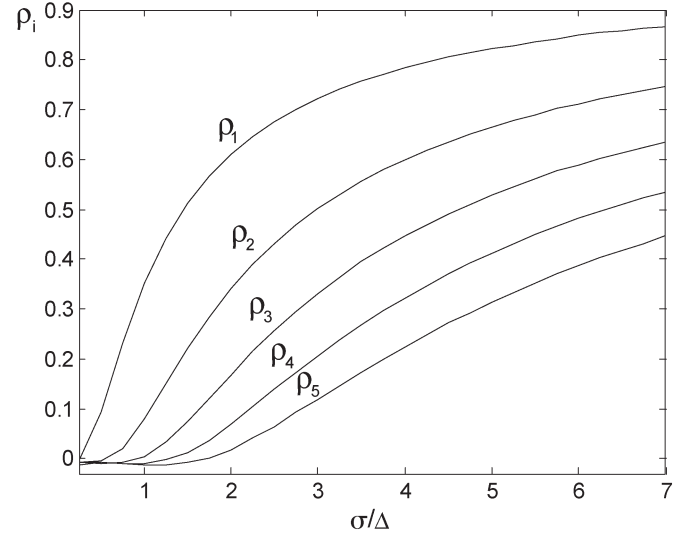

Fig. 1. Estimated correlation coefficients between couples of INL estimators that are $i = 1, \ldots, 5$ code bins far from each other as a function of the ratio between the standard deviation of the AWGN noise σ superimposed to the input sine wave and the quantization step Δ of an ideal ADC.

associated with neighboring transition voltages are increasingly correlated [12]. The correlation coefficients between the kth and the $(k+i)$th INL estimators, i.e.,

$$\rho_{k+i,k} = \frac{E\{\varepsilon_{k+i} \cdot \varepsilon_k\}}{\sigma_{\varepsilon_{k+i}} \sigma_{\varepsilon_k}}$$

$$i = 1-k, \ldots, N-1-k; \quad k = 1, \ldots, N-1 \qquad (6)$$

have been obtained by simulating multiple standard SHTs of variable-resolution ideal ADCs and eventually by applying suitable correlation estimators to the record of errors ε_k that result from subsequent tests [13]. Such a procedure has been repeated for various amounts of superimposed AWGN. According to simulation results, if the ADC input is overdriven appropriately [9], the correlation coefficients depend mostly on the distance i (in terms of code bins) between any pair of INL estimators, whereas they tend to be independent of both the actual position of the kth transition level (i.e., $\rho_{k+i,k} = \rho_i$) and the resolution of the converter. In Fig. 1, the estimated correlation coefficients for $i = 1, \ldots, 5$ are shown as a function of the ratio between the standard deviation of the superimposed AWGN and Δ. Notice that for any given ratio σ/Δ, a value of $0 < H \ll N$ exists such that ρ_i is negligible for $i > H$. In other words, estimators that are more distant than H bins from each other can be assumed to be uncorrelated. In particular, the number H of significant correlation coefficients is approximately equal to

$$H = \left\lfloor 2 \cdot \frac{\sigma}{\Delta} \right\rfloor \qquad (7)$$

where $\lfloor \cdot \rfloor$ rounds the operand to the nearest integer that is smaller than its argument. In the Appendix, it is shown that if

$\rho_i = 0$ for $i > H$, the variance of the kth filtered INL estimator for $L < M$ test samples is approximately given as

$$\sigma^2_{\hat{\text{INL}}_{\text{Fk}}} \cong \frac{1.78\sigma}{L \cdot \Delta^2} \sqrt{A^2 - (\hat{T}_k - d)^2} \cdot \text{ENBW} \cdot \left(1 + 2 \cdot \sum_{i=1}^{H} \rho_i\right) \quad (8)$$

where $k = 1, \ldots, N - 1$ ENBW ≤ 1 is the two-side normalized equivalent noise bandwidth of the chosen unit-gain filter. Equation (8) is particularly important because it implies that a suitable filtering reduces the variance of the kth INL estimator by a factor approximately proportional to ENBW. Such a variance reduction may lead to a remarkable improvement in INL estimation accuracy. Observe that, according to the results shown in Fig. 1, if the peak-to-peak amplitude of the superimposed AWGN noise is roughly smaller than $\Delta/2$, adjacent INL estimators can be assumed to be completely uncorrelated so that (8) can be simplified as

$$\sigma^2_{\hat{\text{INL}}_{\text{Fk}}} \cong \frac{1.78\sigma}{L \cdot \Delta^2} \sqrt{A^2 - (\hat{T}_k - d)^2} \cdot \text{ENBW} \quad (9)$$

$k = 1, \ldots, N - 1$, i.e., the accuracy of the LCF component of each filtered INL estimator is almost equal to the accuracy achievable using a standard SHT procedure over $M = L/\text{ENBW}$ data. On the other hand, if the standard deviation of the AWGN is larger than $\Delta/2$ (e.g., because of the high resolution of the ADC under test), the correlation coefficients in (8) cannot be neglected any longer, and the filtered INL estimator variance is reduced by a factor lower than ENBW.

B. Implementation Issues

The theoretical analysis previously detailed leads to the definition of a new fast industry-oriented method that is very time effective in large-volume ADC accuracy testing. Improving accuracy while reducing testing time is particularly beneficial for high-resolution devices, for which wideband estimation noise increasingly corrupts the actual INL pattern of the devices under test [6]. Of course, for the procedure to be maximally profitable, the type of filter must be chosen appropriately. To this purpose, we suggest using a technique based on the discrete Fourier transform (DFT) and inverse discrete Fourier transform (IDFT) for the following reasons.

1) It provides a good approximation of an ideal lowpass filter with a zero-phase response.
2) It is very simple to design because it requires choosing only the ENBW of the filter.
3) It can be easily standardized because the definitions of both DFT and IDFT are unambiguous.

Basically, the steps of the testing procedure can be summarized in the following list.

1) For a given target expanded estimator uncertainty U_{INL}, the number of necessary test samples M using the standard SHT is determined using (5).
2) The two-side normalized bandwidth B_{INL} of the INL pattern is estimated from an ADC model or from some previous tests performed by the manufacturer on a batch of devices of the same family [6].
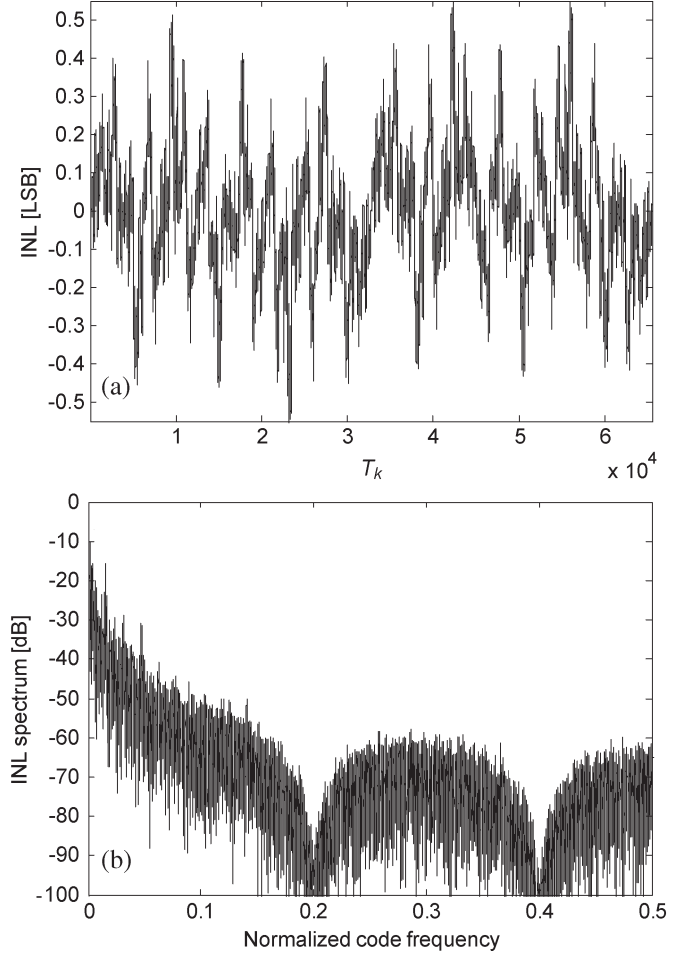

Fig. 2. (a) INL pattern and (b) spectrum of a simulated 16-bit bipolar ADC having an FSR = 20 V (i.e., between -10 and $+10$ V). The prevailing low-frequency behavior of the chosen pattern is clearly visible in (b).

3) The INL pattern is estimated using a single record of $L = [M \cdot B_{\text{INL}}]$ samples, where the operator $[\cdot]$ returns the nearest integer to its argument.
4) The DFT of the $N - 1$ values of the estimated INL pattern is calculated.
5) The transformed sequence is filtered simply by masking the $[(N - 1) \cdot (1 - B_{\text{INL}})]$ DFT samples that are located outside the band $[-B_{\text{INL}}/2, B_{\text{INL}}/2]$ with a zero pattern.
6) Finally, the filtered INL pattern is obtained from the IDFT of the masked sequence. Notice that in the case considered, the ENBW of the DFT-based filter is very close to B_{INL}.

III. SIMULATION AND EXPERIMENTAL RESULTS

A. Results Based on Simulations

In order to validate the theoretical analysis presented in Section II-A, the FSHT has been applied to a simulated 16-bit bipolar ADC with FSR = 20 V (i.e., ranging from -10 to $+10$ V), which is characterized by the INL pattern shown in Fig. 2(a) as a function of the transition level values T_k, $k = 1, \ldots, 2^{16} - 1$. The prevailing LCF content of this pattern is clearly recognizable in Fig. 2(b), where the spectrum of the sequence is shown as a function of the normalized code frequency

values [5]. The simulated input stimulus is 1-kHz high-accuracy sinusoid with a zero offset ($d = 0.0$ V) and an amplitude equal to 10.02 V. The chosen amount of overdrive (i.e., 0.02 V) is large enough to make the INL estimator bias negligible [10]. If a DFT-based filter with ENBW = 0.02 is applied, different values of U_{INL} can be achieved depending on the amount of the superimposed AWGN. Here, the results of two case studies are presented. In the first, the standard deviation of the additive noise superimposed to the input sine wave is set equal to $\sigma = \Delta/2$, and the FSHT has been designed to achieve $U_{\mathrm{INL}} = 0.15 \cdot \Delta$ with a coverage factor $K_p = 3$. In the second, the parameters of the test are $\sigma = 2 \cdot \Delta$, $U_{\mathrm{INL}} = 0.3 \cdot \Delta$, and $K_p = 3$. Observe that, according to (5), in both cases a standard SHT would demand about $M = 11.7 \cdot 10^6$ data to meet the specified target accuracies, whereas the FSHT procedure requires only $L \cong M \cdot \mathrm{ENBW} = 2.34 \cdot 10^5$ test samples. The simulated (gray patterns) and theoretical (black curves) INL estimator standard deviation values before and after applying the lowpass filter as well as the estimator biases are plotted in Fig. 3(a) and (b), respectively, as a function of the transition levels T_k, $k = 1, \dots, 2^{16} - 1$. Such standard deviation patterns have been obtained using 150 records of test samples. Observe that the estimator biases due to filtering are negligible (i.e., much smaller than the target U_{INL}), whereas the data record size is $1/\mathrm{ENBW} = 50$ times smaller than the original one. Therefore, the filtered pattern provides a good estimate of the actual INL sequence with considerable time saving. Notice also that a major difference exists between the two cases considered. In fact, when $\sigma = \Delta/2$, the INL estimators are almost uncorrelated and the theoretical standard deviation pattern resulting from the square root of (9) is about $\sqrt{\mathrm{ENBW}}$ lower than the corresponding values before filtering. Conversely, when $\sigma = 2 \cdot \Delta$, the simulated standard deviation pattern is slightly higher than the previous case due to the correlation between nearby INL estimators. In order to keep this additional contribution into account, the square root of (8) has been used to plot the theoretical standard deviation curve. In particular, by applying (7), $H = 4$ adjacent correlation coefficients have been used in (8). As shown in Fig. 3(b), an excellent accordance exists between the theoretical curves and the simulated results.

B. Experimental Results

The FSHT procedure has also been validated by some experiments performed using a real bipolar 16-bit ADC having the same full-scale range FSR = 20 V as in the simulated case (i.e., between -10 and $+10$ V). The device under test (DUT) is embedded on a data acquisition board NI 6011E with a sampling rate of 20 kSa/s. The INL pattern of the DUT has been estimated using both the standard SHT technique and the FSHT procedure. In both cases, the chosen ADC input stimulus is a 20-Hz sine wave produced by a Stanford Research DS-360 function generator, whose accuracy performance is maximum at very low frequencies. In order to make the estimation bias negligible, an overdrive equal to 2.5 mV (i.e., $A = 10.0025$ V) has been applied to the ADC input. Given that the measured σ/Δ ratio is about 0.8, by setting $U_{\mathrm{INL}} = 0.21 \cdot \Delta$ and $K_p = 3$, it results from (5) that the number of samples M required by
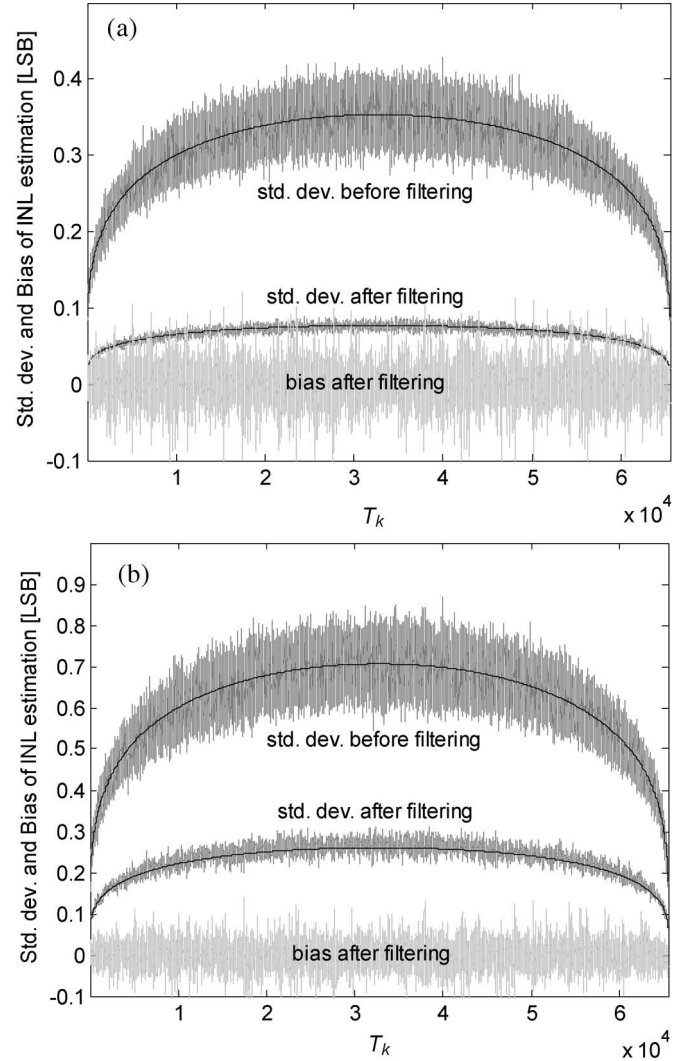

Fig. 3. INL estimator standard deviation and bias before and after filtering for (a) $\sigma = \Delta/2$, $U_{\mathrm{INL}} = 0.15 \cdot \Delta$, and $K_p = 3$ and (b) $\sigma = 2 \cdot \Delta$, $U_{\mathrm{INL}} = 0.3 \cdot \Delta$, and $K_p = 3$. The estimator bias before filtering is not shown because it is negligible. The black curves correspond to the theoretical standard deviation before and after filtering, whereas the gray patterns result from the simulations.

a standard SHT is about 10^7. On the other hand, by applying the FSHT procedure over $L = 10^6$ test samples, it follows from (7) and (8) that a similar estimation accuracy can be achieved for the given value of σ/Δ (i.e., $H = 1$) if a DFT-based filter with ENBW = 0.068 is applied. The INL patterns estimated using the standard SHT over 10^7 samples (black pattern) and 10^6 samples (gray pattern) are shown in Fig. 4(a), whereas the INL patterns obtained using both the standard SHT over 10^7 samples (black pattern) and the FSHT procedure with $L = 10^6$ and ENBW = 0.068 (gray pattern) are plotted in Fig. 4(b). As expected, in the former case, the estimation accuracy of the standard SHT over 10^6 samples is much worse than the chosen U_{INL}. Conversely, the estimation accuracy achieved with both SHT and FSHT is roughly the same, but the data record size required by the FSHT is 10 times smaller. The estimation accuracy improvement provided by the FSHT is even clearer in Fig. 4(c), where the LCF content of the INL pattern estimated over 10^6 test samples is shown. In fact, such a pattern is obtained using a DFT-based filter with ENBW = 0.0068,
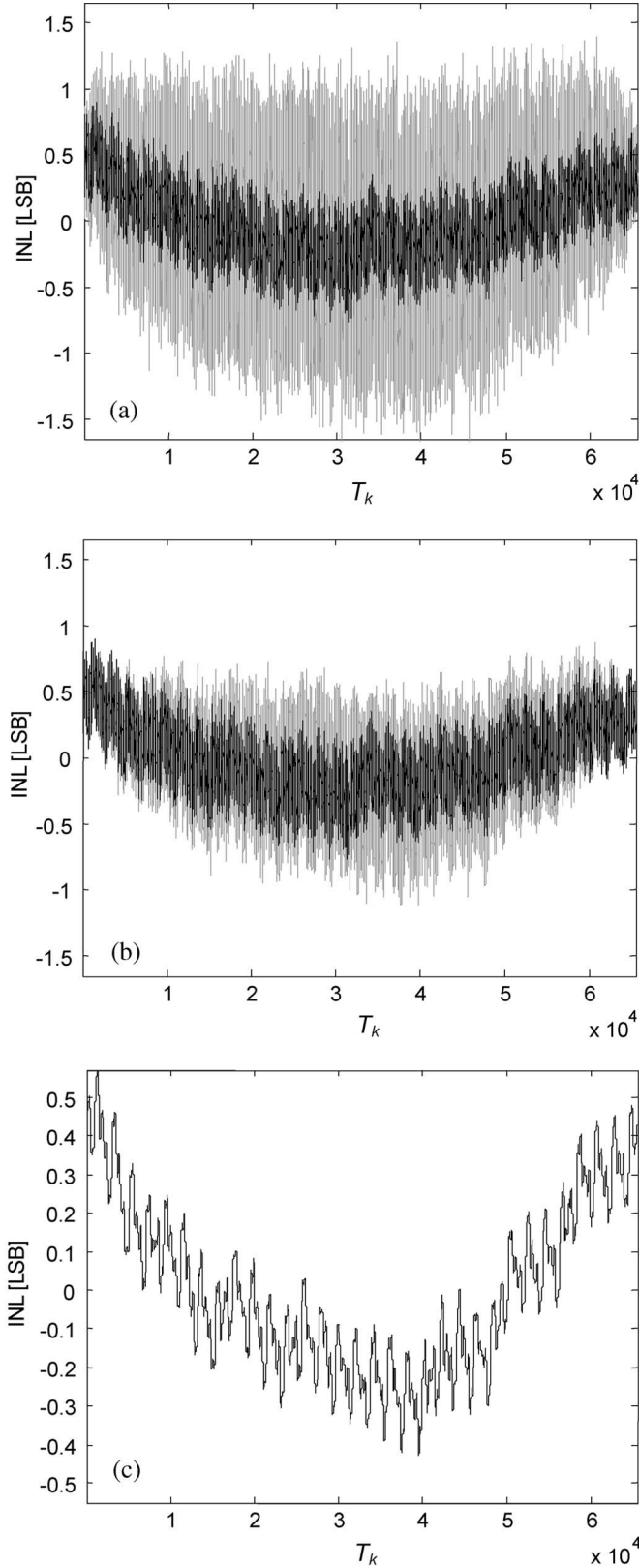
Fig. 4. Experimental INL patterns of a real bipolar 16-bit ADC resulting from both SHT and FSHT testing procedures. (a) Both patterns are estimated according to the standard SHT over about 10^7 (black pattern) and 10^6 test samples (gray patterns). (b) The INL patterns estimated using the standard SHT over 10^7 (black pattern) and the FSHT procedure over 10^6 samples with a filter having an ENBW $= 0.068$ (gray pattern) are compared. (c) The LCF component of the INL pattern estimated according to the FSHT procedure, and ENBW $= 0.0068$ is shown.

namely, an ENBW ten times smaller than in the previous case. Observe that, even though the HCF components of the sequence are filtered out, the main trend of the INL pattern is clearly visible. The expected estimation accuracy is $U_{\mathrm{INL}} = 0.02 \cdot \Delta$, which is comparable with the estimator bias uncertainty as well as with the accuracy that could be achieved using a standard SHT over $M = 10^8$ test samples.

IV. Conclusion

In this paper, a simple and robust technique to speed up the accuracy testing of high-resolution ADCs is described, justified theoretically, and validated by means of both simulations and experimental results. In particular, it is shown that by suitably low-pass filtering an INL pattern estimated through a standard SHT over a small number of test samples, a major reduction in testing time is achieved without serious consequences in terms of estimation accuracy. Some simulations and experimental evidence validate the theoretical analysis. According to the reported results, a testing procedure based on DFT filtering could be particularly profitable for semiconductor companies because it is straightforward to implement and very simple to standardize.

Appendix

This appendix explains the analytical steps leading to (8). According to (3), any estimated INL pattern can be modeled as a random sequence $\hat{\mathrm{INL}}_k \ k = 1, \ldots, N-1$, resulting from the superimposition of the actual unknown ADC INL pattern and the corresponding estimation errors ε_k. If the random sequence $\hat{\mathrm{INL}}_k$ is filtered by means of a linear and time-invariant system, the resulting filtered INL sequence $\hat{\mathrm{INL}}_{Fk}$ is given as

$$\hat{\mathrm{INL}}_{Fk} = \sum_{n=1}^{N-1} \hat{\mathrm{INL}}_n \cdot h_{k-n}, \qquad k = 1, \ldots, N-1 \quad (A1)$$

where h_n is the coefficients of the impulse response of the chosen filter. Therefore, if the mean value of the estimation errors is assumed to be negligible, as it occurs for a suitable amount of the ADC input overdrive [10], the mean value and the variance of the kth filtered INL estimator are, respectively, equal to

$$\begin{aligned} \mu_{\hat{\mathrm{INL}}_{Fk}} &= E\{\hat{\mathrm{INL}}_{Fk}\} \\ &= \sum_{n=1}^{N-1} E\{\hat{\mathrm{INL}}_n\} \cdot h_{k-n} \cong \sum_{n=1}^{N-1} \mathrm{INL}_n \cdot h_{k-n} \end{aligned} \quad (A2)$$

and

$$\begin{aligned} \sigma^2_{\hat{\mathrm{INL}}_{Fk}} &= E\left\{\hat{\mathrm{INL}}^2_{Fk}\right\} - E\{\hat{\mathrm{INL}}_{Fk}\}^2 \\ &\cong \sum_{n=1}^{N-1} \sigma^2_{\varepsilon_n} \cdot h^2_{k-n} \\ &\quad + 2 \cdot \sum_{n=1}^{N-2} \sum_{m=n+1}^{N-1} \rho_{m,n} \sigma_{\varepsilon_n} \sigma_{\varepsilon_m} h_{k-n} h_{k-m} \end{aligned} \quad (A3)$$

where $\sigma^2_{\varepsilon_n} = \sigma^2_{\hat{\mathrm{INL}}_n}$ is the variance of the nth INL estimation error, and $\rho_{m,n}$ is the correlation coefficients between pairs

of INL estimation errors. Ideally, in order to evaluate (A3), the standard deviation of every estimation error as well as the correlation coefficients $\rho_{m,n}$ should be estimated. However, in practical cases, (A3) can be considerably simplified because often, the following conditions hold:

1) The values of $\rho_{m,n}$ depend mostly on the relative distance $i = m - n$ between the INL estimators, rather than on their absolute positions m and n within the ADC output code domain, i.e., $\rho_{n+i,n} = \rho_i$ for any $i > 0$.
2) The INL estimators tend to be uncorrelated as the distance between m and n grows, i.e., a value $H > 0$ exists such that $\rho_{n+i,n} \cong 0$ for $i > H$, where H is small (Fig. 1).
3) For each given value of n, both the standard deviations of adjacent INL estimation errors and the coefficients of the impulse response of the lowpass filter can be assumed to be locally constant, i.e., $\sigma_{\varepsilon_n} \cong \sigma_{\varepsilon_{n+i}}$ and $h_{k-n-d} \cong h_{k-n}$ for $0 < i < H$, where $H \ll N$.

As a consequence, (A3) can be written as

$$\sigma^2_{\hat{\text{INL}}_{\text{Fk}}} \approx \sum_{n=1}^{N-1} \sigma^2_{\varepsilon_n} \cdot h^2_{k-n} + 2 \cdot \sum_{i=1}^{H} \rho_i \sum_{n=1}^{N-1} \sigma^2_{\varepsilon_n} h^2_{k-n}$$

$$= \left(1 + 2 \cdot \sum_{i=1}^{N-1} \rho_i\right) \cdot \sum_{n=1}^{N-1} \sigma^2_{\varepsilon_n} h^2_{k-n}. \qquad (A4)$$

Because the impulse response of a low-pass filter h_n tends to 0 when n becomes large, (A4) becomes approximately

$$\sigma^2_{\hat{\text{INL}}_{\text{Fk}}} \approx \left(1 + 2 \cdot \sum_{i=1}^{N-1} \rho_i\right) \cdot \sum_{n=-M}^{M} \sigma^2_{\varepsilon_n} h^2_{k-n} \qquad (A5)$$

where $M \ll N$ is a suitable value that depends on the bandwidth of the chosen filter. In fact, for $k - n < -M$ or $k - n > M$, the h_{k-n} coefficients are usually negligible. Since for any value of k except for those around 1 and $N - 1$, the variance $\sigma^2_{\varepsilon_n}$ is approximately equal to the upper bound resulting from (4); it follows that for L test samples, (A5) can be rearranged as

$$\sigma^2_{\hat{\text{INL}}_{\text{Fk}}} \cong \frac{1.78\sigma}{L \cdot \Delta^2} \sqrt{A^2 - (\hat{T}_k - d)^2} \cdot \left(1 + 2 \cdot \sum_{i=1}^{H} \rho_i\right) \cdot \sum_{n=-M}^{M} h^2_{k-n}$$

$$\cong \frac{1.78\sigma}{L \cdot \Delta^2} \sqrt{A^2 - (\hat{T}_k - d)^2} \cdot \left(1 + 2 \cdot \sum_{i=1}^{H} \rho_i\right) \cdot \sum_{n=-\infty}^{\infty} h^2_{k-n}. \qquad (A6)$$

Accordingly, by referring to the two-side ENBW of a filter as

$$\text{ENBW} = \frac{\frac{1}{2\pi} \int_{-\pi}^{\pi} |H(\omega)|^2 \, d\omega}{|H(0)|^2} = \frac{\sum\limits_{p=-\infty}^{\infty} h^2_p}{\left(\sum\limits_{p=-\infty}^{\infty} h_p\right)^2} \qquad (A7)$$

and if the filter has a dc unit gain (i.e., $|H(0)| = |\sum_{n=-\infty}^{\infty} h_n| = 1$), (8) is finally obtained.

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