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ADC Testing with IEEE Std 1241-2000

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Abstract *– While the new IEEE standard for ADC terminology and testing builds on IEEE Std 1057-1994 [2] (for digitizing waveform recorders), 1241 relies strongly on frequency domain techniques. Frequency domain techniques tend to be favored in manufacturing because two records of data can produce a robust characterization of the ADC. Processing a small data record (e.g., 2 - 8Ksample) with an FFT yields SINAD, SNHR, THD, SFDR, IMD (with multiple input tones), and other useful data. Generating a histogram of a large record (e.g., 2 – 4Msample) of overdriven data yields DNL and INL. Both theoretical and practical issues will be addressed in the context of actual ADC characterization data.*

Keywords *– ADC, Sinefit, FFT, histogram, IEEE Std 1241, IEEE Std 1057*

1. INTRODUCTION

IEEE Std 1241 (Standard for Terminology and Test Methods for Analog-to-Digital Converters [1] (ADCs) applies to application of ADCs in several ways. It provides a consistent set of terms, definitions, and test methods for use in specifying, characterizing, and evaluating ADCs. Standardized terms are especially important today since ADCs are manufactured and used across the globe. A user in Japan needs to be able to reliably compare performance data from ADC manufacturers in the US and Germany. Std 1241 provides a common basis for such a comparison.

In a manufacturing environment, time is of the essence. A significant part of the price of ADC in volume production is testing cost, typically 5-10%. Once a design is complete, several wafer lots are processed to characterize lot-to-lot differences. A statistically significant set of ADCs from each lot are packaged and tested over temperature and in several test fixtures. Data derived is used to specify parameter variation on data sheets and to establish acceptance limits for production. The data can also be used to determine which parameters need to be tested during production.

In production, the testing objective is to determine to some level of confidence that every ADC will meet its specified performance and to do so in the least possible time. In volume production, testing time dominates all other factors of test cost. Testing time is determined by the setup time, the amount of data acquired, the transfer time from capture memory to the processor memory and the time to process it. Different test methods may produce equivalent results in significantly different periods of time. These differences are a function of both hardware and software used. Different hardware/software combinations may favor one test method over another.

Std 1241 offers a robust set of test methods, especially in comparison to Std 1057 [2]. Principal Std 1057 test methods presume that the sampling clock is not accessible outside the waveform recorder. In Std 1241 the sampling clock is presumed to be generated externally. Also in Std 1241, output data is presumed to be available in real time, whereas Std 1057 presumes fast-in/slow-out operation. Therefore, while the test methods described in Std 1057 generally apply to ADC testing and are included in Std 1241, additional test methods are presented. Some of these new test methods exploit full clock control and/or real-time output data reduce testing time. As a result, Std 1241 offers more choice in test methods than does Std 1057. These test method choices provide a rich trade space from which to implement tests.

This paper discusses the selection of test methods for production acceptance testing of a monolithic ADC. Considerations in this selection process are related to the device architecture. Test data for this paper was acquired from both a physical ADC test and from and ADC simulator. Guidance is derived from this process to those devising production tests for ADCs.

The primary objective of production acceptance testing is to decide whether or not to ship each ADC. The secondary objective is to minimize the cost of this decision. The time required to acquire and process acceptance test data is the major variable in test cost. Long data records and/or multiple data records take more time to acquire than a shorter, single record. Std 1241 provides guidance in selecting the length and number of records required to achieve a given precision to a given confidence level. The number of parameters and number of test conditions (e.g., how many signal and clock frequencies to include) influence the setup time, acquisition time, data transfer time and the processing time. Deciding what data to acquire for an acceptance test is a complex process derived from an understanding of sensitivities in a particular ADC's architecture, qualification test results,

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performance parameters important to a specific application, and the precision and confidence required to make a decision to ship. This decision process is sensitive to ADC manufacturers and is not discussed further in this paper. Discussion commences when these decisions have been made.

2. ADC TEST

An 8-bit ADC (ADS931) [3] designed for operation up to 33Ms/s from 2.7V to 5.5V supplies, which is currently in production, is presented here. This particular ADC has an input bandwidth of 100MHz, adjustable full scale range through the use of an external reference, and is intended for battery powered applications such as camcorders, digital cameras, communications and portable test equipment. The manufacturer has decided to acquire and process two types of data records. An overdriven sine wave will be used to determine integral non-linearity (INL) and differential non-linearity (DNL). A large sine wave will be used to determine signal-to-noise-and-distortion (SINAD), SNHR (SNR), effective bits, Spurious Free Dynamic Range (SFDR) and total harmonic distortion (THD).

The test setup for both types of records is the Sine Wave Test Setup presented in Std 1241, Section 4.1.1.1. (Henceforth in this paper, specified references to portions of 1241 will be denoted by {}, e.g., {4.1.1.1} is section 4.1.1.1) The test setup {Fig. 1} is shown below.

For both tests, the sine wave generator is phase locked to the clock generator to establish a known relationship between the signal frequency and sampling frequency. The {4.1.4.5}, (equation 45) and {4.1.6.3.1}, (equation 64) criteria were used to select the frequency relationship between the input sine wave and the sampling clock. f_{opt} (the optimum input frequency) was adjusted slightly so the equation could be met that allowed J and M to remain relatively prime integers and f_s, to remain constant for all tests. Since generators with excellent frequency resolution (e.g., 15 digit) and stability were employed, an integer number of sine wave cycles was recorded in each data record (i.e., coherent sampling).

INL and DNL are derived from an over driven sine wave. The minimum amount of overdrive is a function of the combined noise level of the signal source and the ADC as well as specified accuracy of the code bin widths (see {4.1.6.3.3}). Care must also be taken to keep the overdrive below the point at which the ADC exhibits aberrant behavior. In this case the input signal was adjusted to approximately 102% of the full-scale range of the ADC. Also, the record length must be chosen such that exact integer number of cycles in a record is relatively prime (i.e., no common factors) to the number of samples in the record. This record length guarantees that the samples are uniformly distributed in phase from 0 to 2π. Note that if the record contains 2^N samples, any odd number of cycles is relatively prime. In addition, a sufficient number of samples must be acquired to attain a certain confidence level in the code transition levels (see {4.1.6.3.2}). In consideration of all of these factors, records were acquired at 30 Ms/s for two different signal frequencies: 500 kHz and 12.5 MHz.

The record length for the 500 kHz data is 262,144 samples, or 59 cycles at 500 kHz to obtain data to 0.1 LSB at 99% confidence. The histogram is presented in Fig. 2. DNL is the difference between a specified code bin width and the average code bin width, divided by the average code bin width. See equations 75 and 76 in Std 1241 for INL and DNL calculations, respectively. DNL for this data is plotted in Figure 3. INL, the maximum difference between the ideal and actual code transition levels is shown in Figure 4. The INL and DNL of an ADC with marginal performance are plotted. This can be seen clearly when one of the major carries has significant DNL error as a large step will occur.

The same ADC was tested with a 12.5 MHz input signal. A 262,144 sample (2^N x 1024) record was acquired to obtain 0.1 LSB accurate data at a 99% confidence level. The resulting histogram is presented as Fig. 5. INL and DNL are plotted in Figs. 6 and 7, respectively. Note that the ADC demonstrates performance at 12.5 MHz that is quite similar to its performance of 500 kHz.

Tests of both signal frequencies were performed in a similar manner. First, appropriate signal and power was connected to the ADC. Then the ADC was operated for a sufficient number of cycles to warm it to a normal operating temperature. Finally, data was acquired, transferred from capture memory to the computer and processed. The entire process for each of the signal frequencies was less than 300 ms.

Tests for SINAD, SNHR, THD, SFDR, and IMD were performed with a large sine wave signal. A large signal {3.1.39} is one whose peak-to-peak amplitude is as large as practical but is acquired by the ADC within, but not including, the maximum and minimum data codes. As a minimum, the signal must open at least 90% of the full-scale range of the ADC under test. In this case, the peak-to-peak signal was nominally 90% of full scale.

As in the histogram test, it is desirable to chose the number of cycles in the record to be relatively prime with respect to the number of samples in the record to spread samples uniformly in phase over 0 to 2π (see {4.1.4.5}). However, much shorter records are required to obtain adequate SINAD, ENOB, SFDR, and THD. Typically, records acquired to determine these parameters contain 1K samples to 8K samples. It is desirable to acquire precisely 2^M samples so that a Fast Fourier Transform (FFT) can be used to process the data.

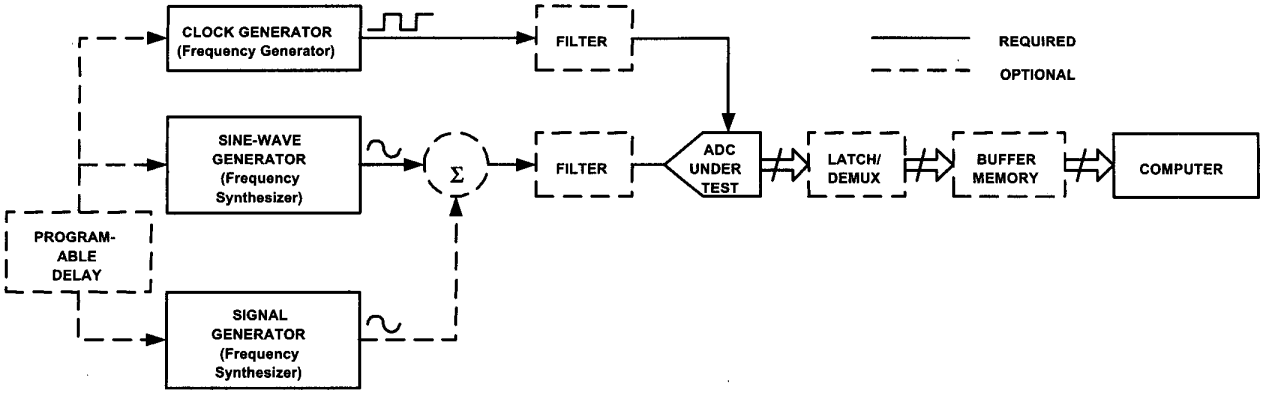

Fig.1. Setup for Sine Wave Testing

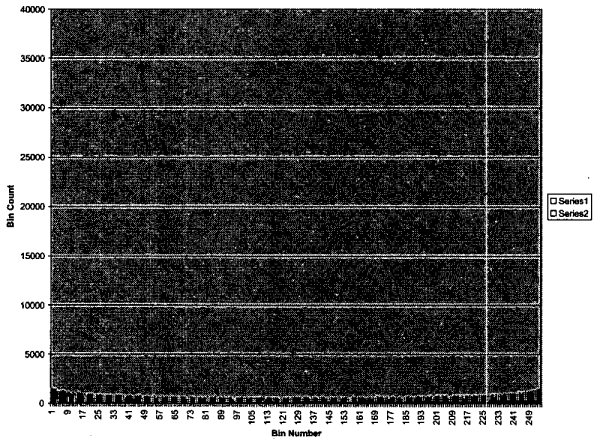

Fig. 2. Histogram of 8-bit ADC sampling 500 kHz sine wave at 33 Ms/s

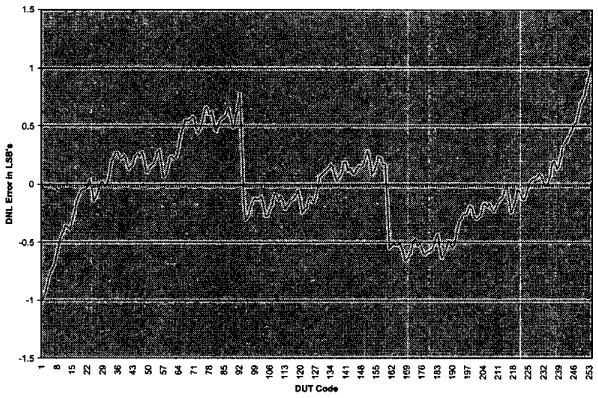

Fig. 4. INL error of 8-bit ADC sampling 12.5 MHz sine wave at 33 Ms/s

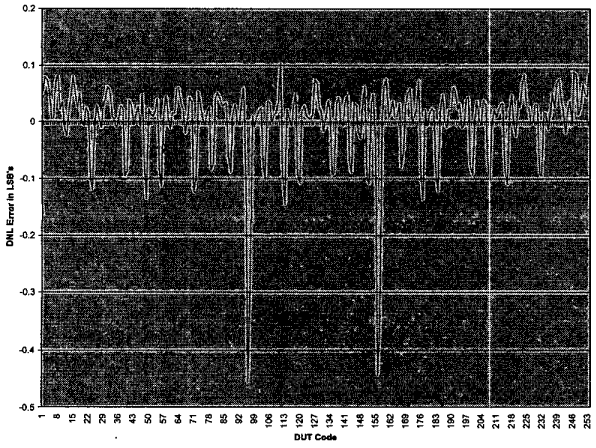

Fig. 3. DNL error of 8-bit ADC sampling 500 kHz sine wave at 33 Ms/s

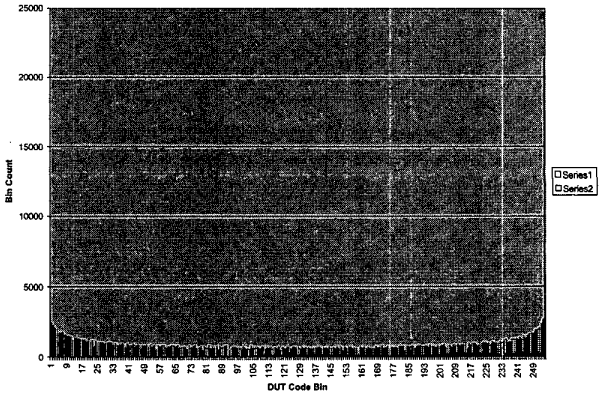

Fig. 5. Histogram of 8-bit ADC sampling 12.5 MHz sine wave at 33 Ms/s

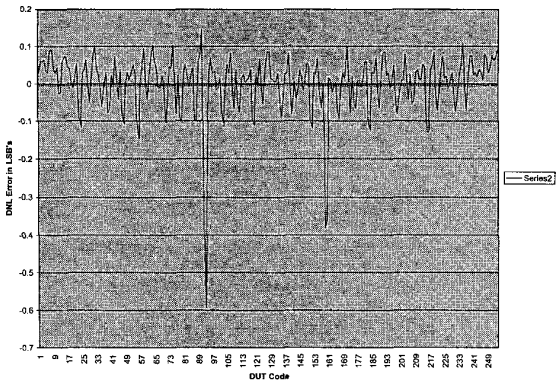

Fig. 6. DNL error of 8-bit ADC sampling 12.5 MHz sine wave at 33 Ms/s

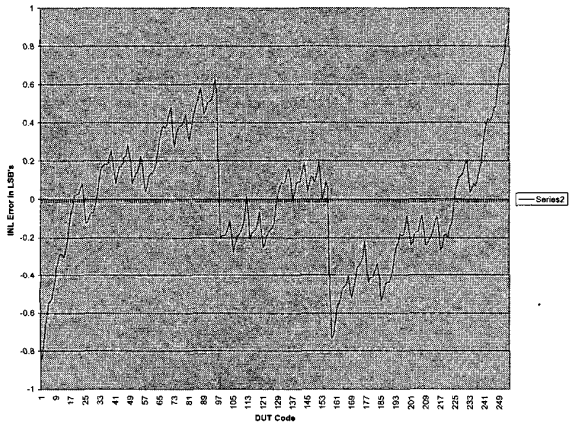

Fig. 7. INL error of 8-bit ADC sampling 500 kHz sine wave at 33 Ms/s

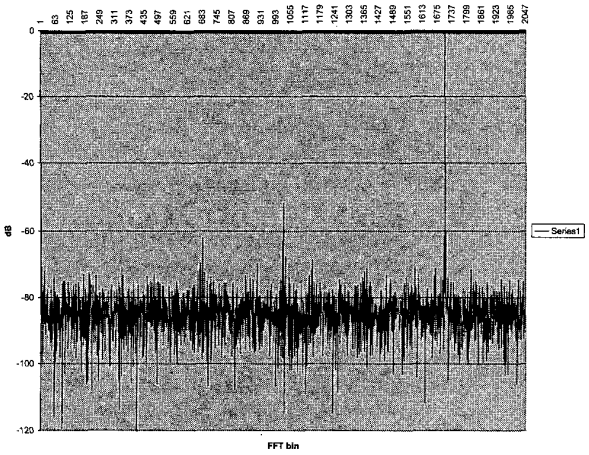

Fig.8. FFT power spectrum plot of 8-bit ADC sampling a 12.5 MHz sine wave at 33 Ms/s

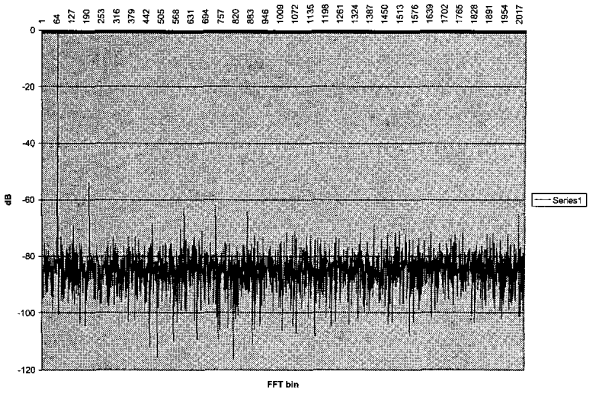

Fig. 9. FFT power spectrum plot of 8-bit ADC sampling a 500 kHz sine wave at 33 Ms/s

The actual test time data from the ADC used for the FFT tests were 93 ms, including setup time, an initial FFT to adjust the input signal amplitude, the acquisition time, data transfer time, and the time to process the FFT. Test time may also be approximated in the absence of real data. At 33 Ms/s, only 62 µs are required to acquire 2K samples and 248 µs to acquire 8K samples. As we will show, processing the data takes much longer. The FFT power spectrum plots are presented in Figs. 8 and 9 for 12.5 MHz and 500 kHz inputs.

3. ADC SIMULATED TEST

An ADC software simulator was used to generate data to assess the processing time for these data. The simulator was programmed to simulate an 8-bit ADC with additive noise but without jitter. Data were processed on two platforms: a personal computer with a 667 MHz Pentium III and RAMBUS memory and a laptop (IBM ThinkPad) with an 833 MHz Pentium III. The same data was processed on both platforms using three algorithms: an FFT, a three parameter sine wave fit (3p fit), and a four parameter sine wave fit (4p fit). The FFT is a hand-coded assembly language floating point FFT licensed from the Intel Performance Library. Both the 3p fit and 4p fit were calculated using matrix operations (see {4.1.4.1} and {4.1.4.3}, respectively. The sine wave fitting software produces SINAD, ENOB, THD, and SFDR. It also calculates jitter, although that data was not meaningful because the ADC simulator did not include jitter. The FFT produces only a power spectrum. Some relatively small additional amount of time is required to obtain the desired parameters.

Despite all of these caveats, the comparisons between the two platforms and among the three algorithms offer some insights. Data that calculated with the 667 MHz Pentium III with RAMBUS (667 MHz PIII) is tabulated in Table 1 and

plotted in Fig. 10. Note that the time to calculate all algorithms is nearly linearly proportional to the number of samples in the record. The 3p fit is generally 10-15% faster than the 4p fit. The FFT is faster for records of 1,024 or more samples. It is about 40% faster than 4p fit for 2,048 samples, 50% faster for 8,192 samples, and 55% faster for 65,536 samples. The computation times range from 31 ms (4p fit) to 19 ms (FFT) for 2K samples to 131 ms (4p fit) to 67 ms (FFT) for 8K samples. Although we do not have the computation portion of the roughly 300 ms histogram test discussed before, these times are generally consistent with the histogram tests. Also, they are more than two orders of magnitude longer than the data acquisition times.

Table 1. Calculation times for a PIII 667 MHz PC

Samples	FFT	Sine-Fit	3-pSine-Fit
512	0.0084	0.0081	0.0069
1024	0.0122	0.0153	0.0143
2048	0.0189	0.0308	0.0257
4096	0.0375	0.0600	0.0512
8192	0.0670	0.1309	0.1160
16382	0.1160	0.2750	0.2350
32768	0.2320	0.5400	0.4270
65536	0.4400	0.9950	0.9520

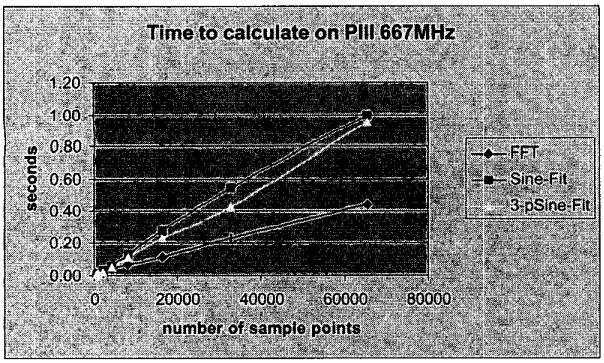

Fig. 10. Plot of time to calculate on a PIII 667 MHz PC

Table 2 indicates the range of values for ENOB, SINAD, and THD observed over a large number of simulations. It is interesting to note that the difference between maximum and minimum values for all of these parameters narrows substantially as the number of samples increases. Due to the amount of additive noise in these simulations, the ENOB and SINAD data does not reflect the typical numbers of modern ADCs. The ADC used in the actual tests has a typical SINAD of 45-46 dB, resulting in an ENOB value of approximately 7.2 – 7.35.

Table 2. Variance in ENOB, SINAD & THD calculations

Ebits	sdev(Ebits)	SINADmin	SINADmax	THDmin	THDmax
6.084	0.05	34.9	36.5	-60.1	-48.7
6.082	0.038	35.3	36.4	-62.7	-51.5
6.086	0.026	35.4	36.2	-67.2	-54.6
6.086	0.019	35.4	36.1	-72.4	-57.7
6.066	0.014	35.5	36.0	-70.1	-61.3
6.086	0.007	35.6	35.9	-73.4	-63.5
6.066	0.006	35.7	35.8	-74.2	-67.3
6.066	0.005	35.7	35.8	-76.1	-71.0

Data that was calculated with the 833 MHz Pentium III laptop (833 MHz PIII) is presented in Table 3 and Fig. 10. While the same general trends are observed, some interesting comparisons arise with respect to the 667 MHz PIII. The sine wave fit data is somewhat faster on the 883 MHz PIII. However, the calculation time is reduced by less than the ratio of processor speeds would suggest. The FFT calculation is substantially slower on the 88l MHz PIII. Although no measurements have been made, it seems possible that processor/memory data transfer rates are dominating the calculation time. In any case, it is clear that processor clock rate is not the sole determining factor for those FFT and sine wave fit calculations. Further, it appears that the selection of algorithms for minimum calculation time is strongly dependent on the hardware and software used.

Table 3. Calculation times for a PIII 883 MHz PC

Samples	FFT	Sine-Fit	3-param
512	0.0110	0.0074	0.0058
1024	0.0155	0.0135	0.0119
2048	0.0255	0.0254	0.0232
4096	0.0455	0.0505	0.0465
8192	0.0880	0.1065	0.0944
16382	0.1650	0.2020	0.1890
32768	0.2980	0.4130	0.3750
65536	0.7080	0.8550	0.8090

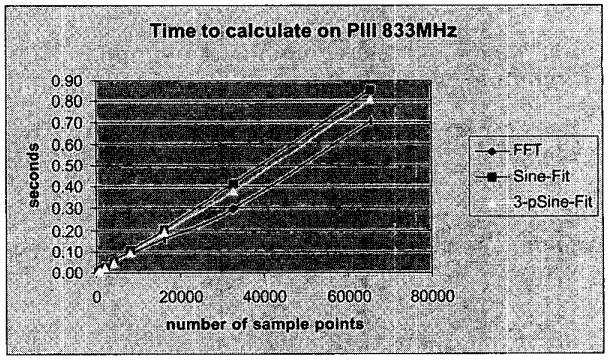

Fig.11. Plot of time to calculate on a PIII 883 MHz PC

4. IMPROVING ADC TEST TIME

Once you have optimized the ADC test time, other means must be employed to reduce test time, and that results in cost savings. The Automatic Test Equipment (ATE) has evolved into quite a machine. With high pin counts for digital resources and increasing signal source and digitizer channel counts, parallel testing has become a cost saving reality. Currently, ADCs are tested routinely in quad-site solutions and new handlers are now available offering octal and even higher numbers of device handling capability. What is ideal is to reduce the test time to just below the index time of the handler, thereby your throughput is that of the handler specification.

Several means are currently employed for ADC testing in parallel; straight captures such as the sine wave tests shown above where each ADC only needs enough digital pins with memory capture behind them. This is the optimum if the capture memory to computer data transfer time is very small. To overcome deficiencies in some testers, a real-time DSP method was employed to process the data as it is captured in real time, serially, which usually requires taking only decimated data at a sub harmonic of the sample frequency. A third method is to implement the histogram capture and sorting in hardware, so only the reduced data is read back to the host computer. Additionally, the DC ramp histogram has been used by many, which like the FFT test, allows multiple ADC and multiple channels of ADCs to be tested all in parallel.

5. SUMMARY

IEEE Std 1241 provides more testing methods to determine critical parameters than does its predecessor, IEEE Std 1057. These additional methods offer the user more choice in configuring and conducting ADC tests. The user can optimize his test setup, data acquisition, and data processing procedures. For production testing, Std 1241 offers the opportunity to reduce test time and ADC manufacturing cost.

ACKNOWLEDGEMENTS

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All of the authors are members of Technical Committee 10 (TC-10) of the Waveform Measurement and Analysis Committee under the IEEE Instrumentation and Measurement (I & M) Society. Mr. Linnenbrink chairs TC-10. Mr. Tilden chairs the TC-10 ADC Subcommittee. Dr. Miller is a member of the TC-10 ADC Subcommittee.

REFERENCES

[1] IEEE Std 1241-2000, "Standard for Terminology and Test Methods for Analog-to-Digital Converters."
[2] IEEE Std 1057-1994, "Standard for Digitizing Waveform Recorders."
[3] PDS-1349D, ADS931 Product Data Sheet (Burr-Brown products from Texas Instrument).