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IEEE Std 1241: The Benefits and Risks of ADC Histogram Testing

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Abstract *- The histogram technique for measuring the transition levels, inl, dnl, gain and offset of Analog to Digital Converters has been widely discussed. It is one of the methods recommended by the newly published IEEE Standard 1241. Histogram techniques are susceptible to errors caused by non-monotonic converters. A previously reported technique for correcting for these errors is shown to be fragile. Recommendations are made for properly testing non-monotonic converters. Discussion is included on the affect of alternation and hysteresis on histogram testing.*

Keywords *– ADC, Analog to Digital Converters, INL, DNL, Histogram, IEEE Std. 1241, Gain, Offset.*

A - I. INTRODUCTION

Analog to Digital Converters are often tested by applying to the converter under test, a waveform such as a sine wave [1] or a triangle wave [2] [3] with known characteristics. The incidence of each code is counted so as to generate a histogram. The code transition levels are evaluated from the histogram of the codes. As an illustration, consider a ±10 Volt 10 bit ADC. A triangle wave starting at –10.24V and finishing at -10.24V is applied with 100,000 levels. The waveform of the triangle wave is shown in Fig. 1. A typical histogram result is shown in Fig. 2.

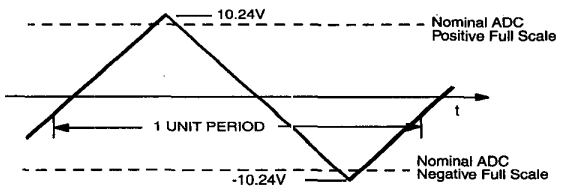

Fig. 1. Typical triangle waveform used for histogram testing

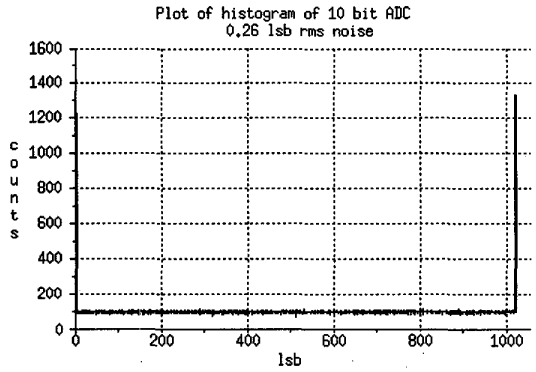

Fig. 2. Histogram generated by a 10 Bit ADC with 2.4% overdrive, and 100,000 measured points

By applying arithmetic to the histogram results it is possible to compute the gain, offset, inl and dnl for the converter under test. The arithmetic is described in the Appendix. The dnl and inl results are shown in Fig. 3 and Fig. 4

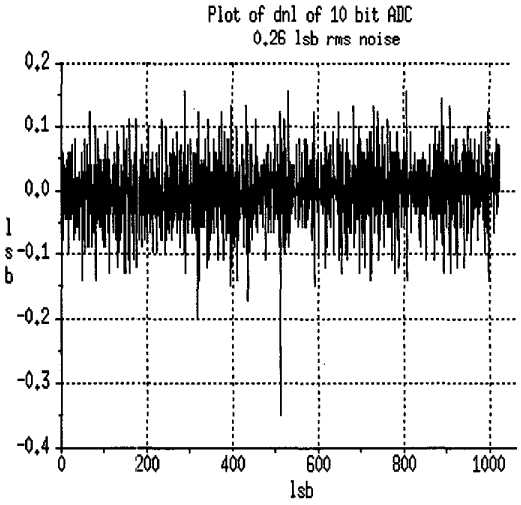

Fig. 3. Plot of dnl of 10 bit ADC with 100,000-point triangle wave applied.

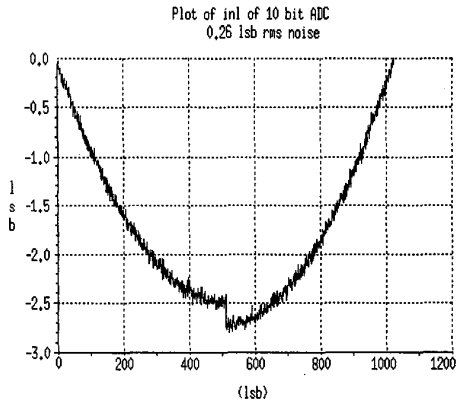

Fig. 4. Plot of typical endpoint calibrated inl of 10 bit ADC with 100,000-point triangle wave applied.

The histogram algorithm works properly with ADCs that have well behaved characteristics. An ideal 10 bit ADC has the transfer function shown below in Fig. 5

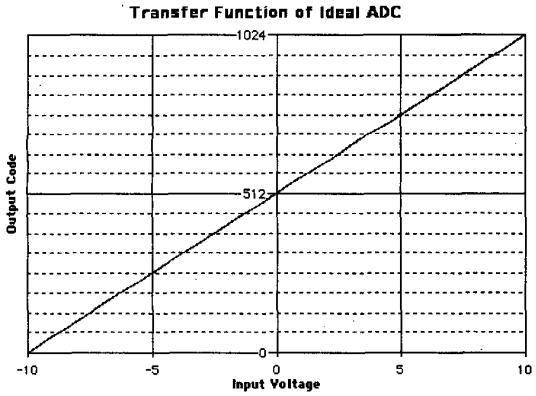

Fig. 5. Transfer function of ideal ADC with perfect monotinicity

A problem occurs if the transfer function is similar to the dramatically defective one shown in Fig. 6. Such a transfer function can occur if the converter digital interface has a logic defect. Similar transfer functions occur if bits are swapped in the output, or unusual sparkle codes occur.[5]

The histogram for the converter described in Fig. 6 will be identical to the histogram shown in Fig. 2. The inl and dnl computed from such a converter would appear similar to the ones shown in Fig. 2 and Fig. 3. The problem that converter manufacturers must resolve is how to rapidly identify converters which exhibit variations of non-monotonic behavior.

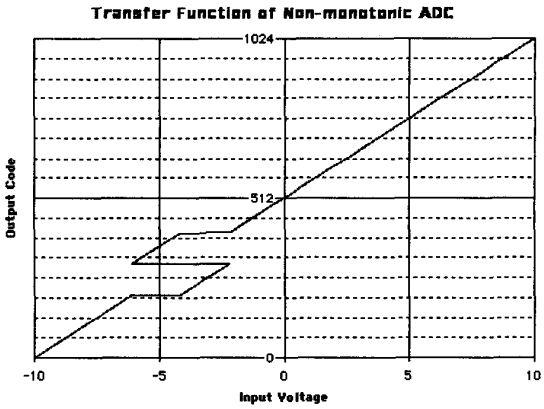

Fig. 6. Transfer function of 10 Bit ADC with non-monotinicity

A - II. SOLUTIONS TO THE MONOTINICITY PROBLEM

Mathew Mahoney [5], in his essay on converter testing proposed that a weight function be used. In the weight function, an array, the same size as the histogram array, collects the sum of the ramp indices in each code bin. An example of the weight array for a 10 bit ADC is generated by the pseudo code listed below:

```
histogram = 0
weight = 0
for i = 1 to 1e5 do
  v = -10.25 + (i-1) * 20.5 / 1e5
  set waveform source to v – Ramp
  J = ADC_output
  histogram[J+1] = histogram[J+1] + 1
  weight[J+1] = weight[J+1] + i
endfor
```

The code shown generates a ramp. The code can be modified to generate a triangle wave, and equivalent results can be obtained if the weight function is appropriately modified..

If the histogram array has no missing codes then the following math produces the inl function based on code centers:

```
W = weight / histogram -- W is W[1:1024]
```

```
for i = 1 to 1024 do
  unit_array = i
endfor
a = (W[1023] - W[2]) / 1021
inl = (W - W[2]) / a - unit_array
```

If the weight function is invoked the inl function then appropriately identifies the linearity problem as shown in Fig. 7.

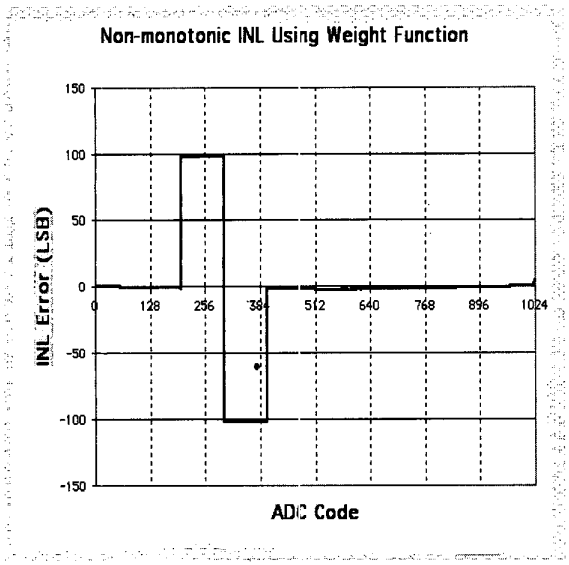

Fig. 7. Non-monotonic inl result with Mahoney algorithm

The algorithm becomes more difficult to justify if there are missing codes. The division of the weight by the tally becomes undefined when the histogram count is 0. There appears to be no simple way to make the computed inl match the true inl when there are missing codes, and there is a suspicion of non-monotonic behavior.

A - III. MISSING CODES AND NON-MONOTINICITY:

Missing codes and non-monotinicity is a characteristic which is often sensitive to the nature of the input. If an AC input is applied to the converter under test, certain frequencies can introduce "sparkle codes" in the output. These are spurious converter outputs that can differ significantly from the expected characteristics; Rapidly changing inputs can also cause missing codes. Converters which exhibits perfect monotinicity with quasi-static inputs can still generate occasional radically invalid output codes, or miss certain codes.

A - IV. RECOMMENDATIONS:

Converters that potentially have missing codes and non-monotonic transfer functions should be evaluated with the following strategy.

- Assume that the converters are monotonic, and perform the standard histogram test without the use of the weight function. This test will determine gain, offset, inl, and dnl.
- Apply a sine wave to the ADC input. Evaluate the SINAD. Verify that the SINAD results agree with the converter specifications. The compatibility of the SINAD results with the measured inl will confirm that non-monotinicity effects are not significant. This test is equivalent to the standard test for the effective number of bits, or ENOB. [6]

Special failure modes that may occur in certain ADC architectures are best evaluated by specific tests that are targeted at those failures.

A - V. HYSTERESIS AND ALTERNATION

Converters that exhibit hysteresis and alternation will generate results from histogram testing that must be properly interpreted.

Hysteresis is a familiar concept. If the input is increasing the code edge will appear at a higher voltage than would appear to occur with decreasing input voltages. A model of a 1-bit converter with hysteresis is shown in Fig. 7.

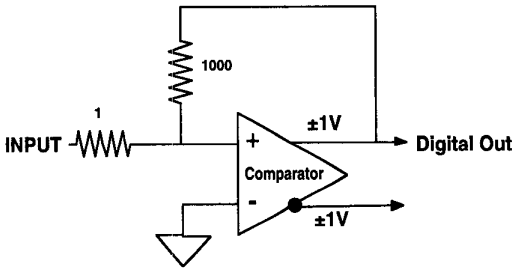

Fig.7. ADC equivalent circuit that demonstrates ADC hysteresis

The one bit converter exhibits different thresholds with a rising input and a falling input. A ramp attempting to evaluate the threshold of the model with a histogram

method would find a +1mV threshold for a positive going ramp, and a –1mV threshold for a negative going ramp. A triangle ramp would appear to generate a 0mV threshold when the two responses are averaged. The presence of noise makes the identification of hysteresis a stochastic process.

Some converters can exhibit a complementary function called alternation. The ADC alternation model for a 1-bit converter is shown in Fig. 8.

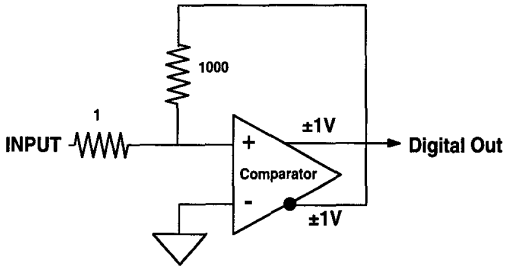

Fig. 8. ADC equivalent circuit that demonstrates ADC alternation

If a ramp or a triangle wave is applied to the converter model a band of alternating outputs appear at the digital output. If a histogram measurement is made the results will identify the code transition level as near 0mV. Another technique is needed to identify the aberrant behavior. A useful technique for detecting alternation is to perform an fft on the data collected when the input is in the alternation band. The presence of significant spectral energy at the sampling frequency divided by 2 is a good indicator of alternation.

Appendix – Mathematics of Histogram Testing

A - I. TRIANGLE HISTOGRAM ARITHMETIC

It is assumed that a triangle wave is applied to the converter being tested. The negative peak of the ramp is VM. The positive peak of the ramp is VP. Exactly M full periods of data are collected, where M is an integer (usually 1). The histogram of the codes is collected in array H[1:N] where N is the number of codes present at the converter output. H[1] is the number of codes observed with a value of 0. H[N] is the number of codes observed with a value of N-1. T[1] is the transition voltage at the lower edge of the "1" code. T[N-1] is the transition voltage at the lower edge of the "N-1" code. inl and dnl are expressed in units of lsb. G, the gain of the converter, is expressed in units of volts per lsb. The offset of the converter is T[1], the voltage corresponding to the 0 to 1 code transition. The algorithm which computes all the parameters is given below in a generic language.

```
H = 0.0
for i = 1 to sample_size do
  H[sample[i]+1] = 1.0 + H[sample[i]+1]
endfor
Hc[1] = H[1] - 0.5
for i = 2 to n do
  Hc[i] = Hc[i-1] + H[i]
endfor
S = Hc[n]
T[n-1] = VM + (VP-VM) / S * Hc[n-1]
T[1] = VM + (VP-VM) / S * Hc[1]
A = (T[n-1] - T[1]) / (S - Hc[1] - H[n])
C = T[1] - A * Hc[1]
G = (T[n-1] – T[1]) / (n-2)
T[2:n-2] = C + A * Hc[2:n-2]
for i = 1 to n do
  Ti[i] = T[1] + G * (i-1)
endfor
inl = (T[1:n] - Ti[1:n]) / G
dnl[1:n-2] = (T[2:n-1] - T[1:n-2] - G ) / G
```

The uncertainty of the measurements of inl, dnl, gain, and offset are approximately described by the plots shown in Fig. 8:

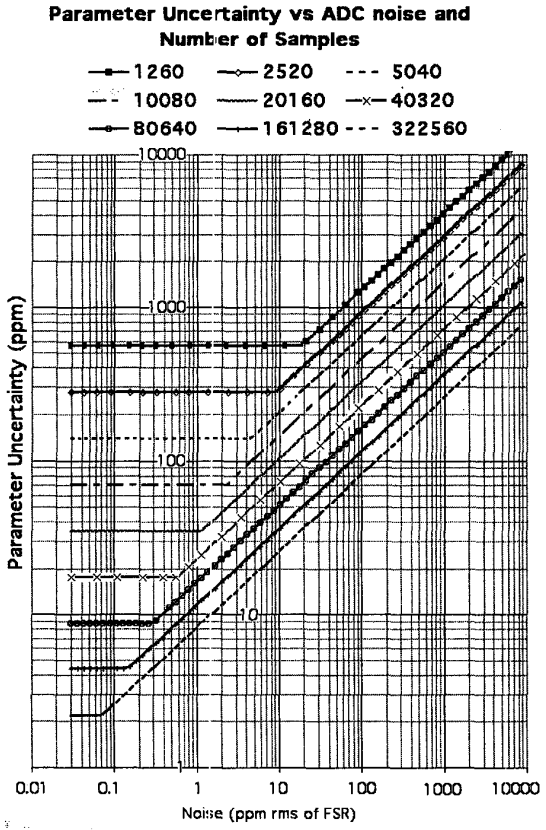

Fig. 8. inl, dnl, gain, and offset uncertainty as a function of ADC noise, and number of samples

The horizontal axes indicates the adc noise level in rms ppm of full scale. The vertical axes gives the uncertainty of the measurement of inl, dnl, gain, or offset in units of rms ppm of full scale. Each of the plot lines give the relationship for the given number of samples in the linear region of the converter. Converters with significant internal noise generate uncertainty in the parameters being measured according to the relationship shown below:

$$\sigma_{par} = 4.6\sqrt{\frac{ci_{ADC}}{N}} \qquad (1)$$

Note that the uncertainty is not a function of the ADC resolution.

A - II. LOW NOISE ANALYSIS

Both the number of samples, and the noise of the converter affect the uncertainty of the measured parameter. The parameter uncertainty for very low noise converters is determined by the number of samples taken (as indicated by the horizontal lines on the chart). The uncertainty varies as the reciprocal of the number of samples. The relationship is approximated by the equation:

$$\sigma_{par} = \frac{0.7}{N} \qquad \text{par = inl and gain: (2)}$$

The uncertainties of the measurement of the dnl and offset are slightly less and are given by Equation (2)

$$\sigma_{par} = \frac{0.4}{N} \qquad \text{par = dnl and offset: (3)}$$

The case where the change of the applied ramp between conversions is much greater than the converter noise needs some further discussion. An example of such a test algorithm is shown in Fig. 9.

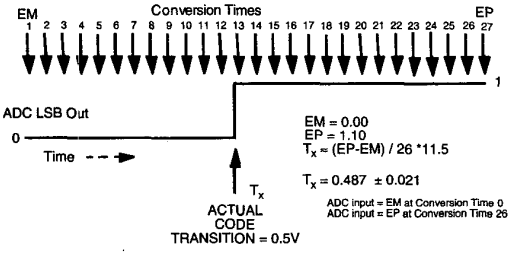

Fig. 9. Measurement of code transition voltage T_x

The actual code transition is located at 0.5V. Because the sample points occur at unknown voltages, the calculated location of the transition is uncertain. The value calculated by the algorithm shown is 0.487±0.021. The uncertainty, 0.021, is half of the resolution.

The uncertainty is a static uncertainty. For a given ramp with a fixed number of samples, the number of samples introduces a fixed round-off error. The round-off errors for each calculation are described by the classic relationship:

$$\sigma = \frac{1}{N\sqrt{12}} \cong \frac{0.29}{N} \qquad (4)$$

The round-off errors cascade through the calculations to give the relationship shown in Equations (2) and (3).

A - III. SINE HISTOGRAM ARITHMETIC

Similar expressions are used for evaluating sine wave histogram based parameters.

It is assumed that a sine wave is applied to the converter being tested. The negative peak of the waveform is VM. The positive peak of the waveform is VP. Exactly M full periods of data are collected, where M is an integer. The histogram of the codes is collected in array H[1:N] where N is the number of codes present at the converter output. H[1] is the number of codes observed with a value of 0. H[N] is the number of codes observed with a value of N-1. T[1] is the transition voltage at the lower edge of the "1" code. T[N-1] is the transition voltage at the lower edge of the "N-1" code. inl and dnl are expressed in units of lsb. G, the gain of the converter, is expressed in units of volts per lsb. The offset of the converter is T[1], the voltage corresponding to the 0 to 1 code transition. The algorithm which computes all the parameters is given below in a generic language.

```
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for i = 1 to sample_size do
  H[isamples[i]+1] = 1.0 + H[isamples[i]+1]
endfor
Hc[1] = H[1] - 0.5
for i = 2 to n do
  Hc[i] = Hc[i-1] + H[i]
endfor
S = Hc[n]
C = (VP + VM) / 2.0
A = (VP - VM) / 2.0
for i = 1 to n do
  T[i] = C - A * cos((PI * Hc[i]) / S)
endfor
G = (T[n-1] - T[1]) / (n-2)
for i = 1 to n do
  Ti[i] = T[1] + G * (i-1)
endfor
inl = (T[1:n] - Ti[1:n]) / G
dnl[1:n-2] = (T[2:n-1] - T[1:n-2] - G ) / G
```

The uncertainties of the measurements are somewhat higher when a sine histogram is used. See IEEE Standard 1241 for the details of the differences. The results are sensitive to the non-monitinicity illustrated by the transfer function shown in Fig. 6.

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