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Estimation for ADC's INL Using a Moving-average Filter

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***Abstract*—The sine wave code density test is the most prevalent technique to estimate integral nonlinearity (INL) of ADCs. The main disadvantage of this method is that the number of samples tends to increase exponentially with the resolution of ADCs. The moving-average filtered sine wave code density test under coherent sampling condition is proposed in this paper. The proposed method needs fewer samples within the almost same accuracy of INL, and it is especially suitable to the estimation for high-resolution ADCs' INL. The proposed method is analyzed theoretically and validated by means of simulation and experimental results.**

Keywords-ADC Test; Moving-average Filter; INL

I. INTRODUCTION

As a discrete device or an important module in system on chip (SoC), analog-to-digital converters (ADCs) are of widespread availability. However, it is very difficult to test its performance parameters in practical application. In order to obtain these parameters about ADCs, it is necessary that not only much time and expensive equipments for testing, but also complicated processing of the massive data getting from the test.

Integral nonlinearity (INL) is the important parameter denoting the linearity and missing codes. And it is particularly important to those ADCs used in image processing and video. Today manufacturers of ADCs frequently use the sine wave code density test to acquire the INL because of its simple principle and high accuracy [1][2]. Unfortunately, the main disadvantage of the test is that it requires hundreds, even thousands of samples per each code bin, which leads to a very large number of samples, and therefore it is very expensive and time-consuming, particularly for high–resolution ADCs (16 bits or more).

In order to shorten the test time and reduce the test cost, some methods to reduce the number of samples have been reported, such as in frequency domain, the literatures [3][4] adopt the methods based on DFT (Discrete Fourier Transform) to estimate ADC's INL in fewer samples. However, these methods have to analyze the complex spectrum of the ADC output and find the best Chebyshev polynomials approximation for the INL. Therefore, the theoretical analysis is very complicated. Besides, these methods can only estimate the smooth part of the ADC INL curve and should never be used to assess the maximum static INL usually reported in ADC data-sheets and in instrument specifications.

In this paper, the conventional sine wave code density test is improved and the moving-average filtered sine wave code density test is presented. The original INL is estimated roughly by the conventional sine wave code density test in fewer samples, and then the final INL will be obtained by the moving-average filter over the INL corresponding to several adjacent digital output codes of ADCs. The number of samples would be reduced significantly because of the usage of the moving-average filter. The proposed method owns the simple principle and needs no spectrum analysis, and the INL can be estimated directly in time domain. It can be very accurate when the ADC has a smooth nonlinear characteristic. In Section 2, the conventional sine wave code density test is introduced. The proposed method will be presented in Section 3. In the succeeding section, the simulation and experimental results are reported. Section 5 concludes this paper.

II. CONVENTIONAL SINE WAVE CODE DENSITY TEST

It is well known that the sine wave code density test is employed to estimate the DNL (Differential Nonlinearity) and INL of ADCs [5]. In the sine wave code density test, the input waveform can be represented by

$$V(t) = A\cos(\omega t + \phi) + C\,, \tag{1}$$

where A is the amplitude and A>0, $\omega = 2\pi f_i$ is the angular frequency, f_i is the frequency, ϕ is the initial phase and C is the offset.

The probability density function of $V(t)$ is [5]

$$f[V(t)] = \frac{1}{\pi\sqrt{A^2 - [V(t) - C]^2}}\,. \tag{2}$$

Integrating this density with respect to the voltage gives the probability that $V(t)$ falls in the region $(V_a, V_b]$ is

$$P\{V_a < V(t) \le V_b\} = \frac{1}{\pi}[\arcsin(\frac{V_b - C}{A}) - \arcsin(\frac{V_a - C}{A})]\,. \tag{3}$$

For an ideal N-bit ADC, let V_b-V_a=1LSB and LSB is the least significant bit of an ideal ADC, from (3) the probability of the n-th digital output code is

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$$P(n)=\frac{1}{\pi}\times\{\arcsin[FSR\times(n-2^{N-1})/(A\times 2^{N})] - \arcsin[FSR\times(n-1-2^{N-1})/(A\times 2^{N})]\} \quad (4)$$

where n represents the code bin number ranging from 1 to 2^N, FSR is the full-scale range, N is the resolution of the ADC.

DNL and INL (LSB) can be calculated as follows [5]:

$$DNL(n)=[H_{actual}(n)/H_{ideal}(n)]-1, \quad (5)$$

$$INL(n)=\sum_{i=1}^{n}DNL(i), \quad (6)$$

where $H_{\text{actual}}(n)$ is the actual measured number of samples in code bin n and $H_{\text{ideal}}(n)$ is the ideal number of samples in code bin n.

In the sine wave code density test, let $H[i]$ is the number of samples in code bin i, $H_c[k\text{-}1]$ is the total number of samples in the region between code bin 1 and code bin k-1, then

$$H_c[k-1]=\sum_{i=1}^{k-1}H[i]. \quad (7)$$

Let $T[k]$ is the k-th code transition level, and then $T[k]$ is [6]

$$T[k]=C-A\cos(\frac{\pi H_c[k-1]}{N_t}). \quad (8)$$

In sine wave code density test, in order to estimate the DNL and INL accurately, the number of samples, the sampling strategy and the choice of A and C are very important and discussed in detail as follows.

A. Number of Samples Needed

In order to describe the minimum number of samples needed for estimating DNL and INL, it is assumed that the estimated DNL has a Gaussian distribution with mean μ and standard deviation σ, and a 100(1-α) percent confidence interval of the form (μ-$\sigma Z_{\alpha/2}$, μ+$\sigma Z_{\alpha/2}$) is set up. This says that the measured DNL lies in the range (μ-$\sigma Z_{\alpha/2}$, μ+$\sigma Z_{\alpha/2}$) with 100(1-α) percent probability. α is chosen for the desired confidence level. $\sigma Z_{\alpha/2}$ is the precision to which the measured value differs from the true value α, $Z_{\alpha/2}$ is determined by (9) and can be found in the table of the standard normal distribution function.

$$\frac{1}{\sigma\sqrt{2\pi}}\int_{-Z_{\alpha/2}}^{Z_{\alpha/2}}e^{-\frac{x^2}{2\sigma^2}}dx=1-\alpha. \quad (9)$$

The minimum number of samples N_t needed for β bit precision (β<1) and 100(1-α) confidence is given by [5]

$$N_t\geq\frac{Z_{\alpha/2}\pi 2^{N-1}}{\beta^2}. \quad (10)$$

In (10), N_t tends to increase exponentially with the resolution of ADCs, N, and it means a corresponding increment in test time.

Table 1 shows the minimum number of samples N_t needed to estimate the DNL of an N-bit ADC (N equals 8, 12, 16, 20, 24) for 0.10 bit precision and 99 percent confidence. Table 1 indicates that the high–resolution ADCs (16 bits or more) require a large number of samples, and it means a very difficult test task.

B. The Sampling Strategy

Because the sine wave code density test is based on the statistical principle, for a given accuracy of estimation, the number of samples is enormous, which greatly increase the test time and cost. And at the circumstances of the limited samples, in order to ensure that every digital output code appears, the test signal frequency (f_i) and the sampling clock frequency (f_s) must satisfy the coherence condition, $\frac{f_i}{f_s}=\frac{J}{M}$, where J and M are mutually prime integers, M is the number of samples in each record, J is the number of the input signal periods in each record. There are exactly J cycles of the test signal in the M samples. Normally, several records are collected to build the histogram, so that N_t=RM, where R is the number of records.

C. The Choice of A and C

The variable A and C are normally chosen so as to contain all the code transition levels of the ADC. By overdriving the ADC with a sine wave whose peak-to-peak amplitude is suitably larger than FSR, the estimator bias of the DNL and INL can be made negligible [6].

III. The Proposed Moving-average Filtered Sine Wave Code Density Test

In practical test, the signal generator's noise, clock jitter and ADC's hysteresis can be equivalent to additive noise (hereinafter simply called noise) which is superimposed to the input sine wave. And it is assumed that the noise has a Gaussian distribution with zero mean and standard deviation σ_n.

TABLE I. N_t NEEDED FOR AN N-BIT ADC

N	N_t
8	2.7×10^5
12	4.2×10^6
16	6.9×10^7
20	1.1×10^9
24	1.8×10^{10}

In the absence of the noise, the sampling points whose voltages are less than the k-th code transition level $T[k]$ would be classified in the region between code bin 1 and code bin k-1. Now we consider the situation that the sampling points fall in the region between code bin 1 and code bin k-1 in the presence of the noise.

Let the sampled voltage without the noise is $T[k]$-x, x is the distance between the k-th code transition level $T[k]$ and the sampled voltage without the noise (x>0). If the noise presents, the particular sampling point will fall in the region between code bin 1 and code bin k-1 as long as the instantaneous noise is smaller than x. That is, the probability $p(x)$ that the sampling point will fall in the region between code bin 1 and code bin k-1 is

$$p(x) = \frac{1}{\sigma_n\sqrt{2\pi}}\int_{-\infty}^{x} e^{-\frac{v^2}{2\sigma_n}} dv \triangleq 1 - \frac{1}{2} erfc(\frac{x}{\sigma_n\sqrt{2}}). \quad (11)$$

For each individual sampling point i we define the random variable b_i which represents whether the sampling point falls in the region between code bin 1 and code bin k-1. If the sampling point falls in the region between code bin 1 and code bin k-1 then b_i =1; If the sampling point falls in code bin k or higher code bins then b_i =0. Therefore the mean value of the count contribution b_i is $p(x)$ and the variance is

$$\sigma_b^2(x) = p(x)(1 - p(x)). \quad (12)$$

Conversely, if the sampled voltage without the noise is $T[k]$+x, then the sampling point will fall in the region between code bin 1 and code bin k-1 if the instantaneous noise value is below $-x$. In the case, the mean value of the count contribution b_i is (1-$p(x)$) and the variance is the same as (12).

From (11) and (12) the variance is the function of the ratio x/σ_n, and is shown in Fig. 1.

As shown in Fig. 1, only the sampling points whose value deviates from the $T[k]$ by a few σ_n are able to contribute to the counter. Consequently, the conventional sine wave code density test introduced in Section 2 will be

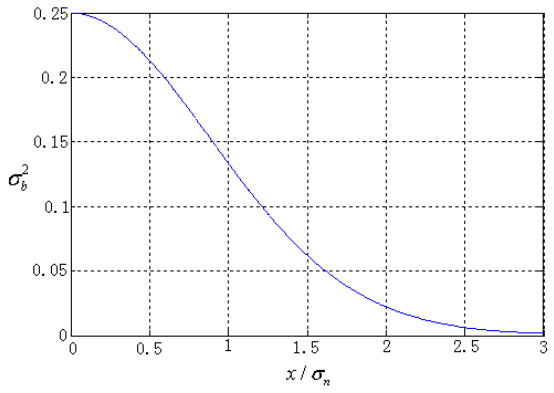

Figure 1. The variance of the count contribution b_i induced by the additive noise

applied to estimate the ADC INL in N_t samples, then the new sequence $INL_F(n)$ can be obtained by applying a moving-average filter over P adjacent INL estimators and expressed as

$$INL_F(n) = \frac{1}{P}\sum_{j=-(P-1)/2}^{(P-1)/2} INL(n+j). \quad (13)$$

where $n = (P-1)/2+1,...,2^N - 1 - (P-1)/2$, P is odd. It can easily be shown that, if the INL's estimation error sequence is modeled as a white noise, the relation between the variance $\sigma_{INL_F}^2$ of the sequence $INL_F(n)$ and the variance $\sigma_{INL_F}^2$ is approximately given by

$$\sigma_{INL_F}^2 \approx \sigma_{INL}^2 / P. \quad (14)$$

From (14), we can see that the precision of INL after applying the moving-average filter enhances P times. This means that the filtered method in N_t/P samples can achieve the same INL's accuracy as the conventional method in N_t samples.

The procedure of the moving-average filtered sine wave code density test can be outlined in two steps.

a) The conventional sine wave code density test is applied in N_t/P samples, and the original INL of ADC is estimated roughly.

b) A moving-average filter is applied over P adjacent INL estimators, and then the final INL can be obtained.

Thus the same INL's accuracy can be achieved by the proposed method and the number of samples is reduced by P times. As a result, time and cost can be saved. Of course, the selection of the filter length P depends on the ADC's nonlinearity characteristic and the target precision $\sigma Z_{\alpha/2}$. Additionally, P can be set a larger value with a higher N.

Because the moving-average filter is used, the proposed method can only estimate the smooth part of the ADC INL curve. Therefore, it is especially suitable for the ADC who has a smooth nonlinear characteristic.

In the moving-average filtered method, because of the reduced number of samples, it is very important that the input signal frequency and the sampling clock frequency should satisfy the coherence condition in order to ensure containing every digital output code.

IV. Simulation and Experimental Results

A. Simulation Results

In order to validate the theoretical analysis presented in Section 3, the proposed test strategy has been applied to a simulated 12-bit ADC whose FSR is 2V (i.e. ranging from -1 to +1V). In order to minimize the estimator bias, a sine wave at 1.512333 MHz frequency with a small overdrive of 0.02V and no offset (A=1.02V, C=0V) has been chosen for the test.

The sampling clock frequency is set to 40MHz so that the coherence condition can be satisfied. The standard deviation of the additive noise superimposed to the sine wave has been set equal to 0.5LSB. The conventional method has been initially used to achieve a target 0.10 bit precision with 99 percent confidence. According to (10) the minimum number of samples N_t is about 4.2 million. Alternatively, the proposed method requires only 2.5×10^5 samples when P equals to 17.

The INL patterns estimated by both methods are shown in Fig. 2(a) and Fig. 2(b) respectively. From Fig. 2 we can see that the INL_F in Fig. 2(b) tracks closely the changes of the INL in Fig. 2(a) and the main trend of the INL pattern is clearly visible in Fig. 2(b). Their maximum INLs are 0.43LSB and 0.33LSB respectively. The difference between them is only 0.10LSB, and it is within the acceptable range in measurement. Therefore, the results indicate that the moving-average filtered sine wave code density test with fewer samples is able to estimate the ADC INL accurately.

B. Experimental Results

The proposed method has also been validated experimentally by using a commercial 8-bit ADC whose FSR is 5V (i.e. ranging from 0 to 5V). The sine signal frequency is 49.999KHz, and its overdriving voltage and offset voltage are 50mV and 2.5V respectively (i.e. A=2.55V, C=2.5V). The frequency of sampling clock is 500KHz. Derived from (10), within 0.10 bit precision with 99 percent confidence, 2.7×10^5 samples are collected. Alternatively, the proposed method requires only 3×10^4 samples when P equals to 9. Fig. 3 shows the two INL patterns noted with blue solid line and red asteroid line respectively.

As expected, we can see that the INL_F tracks closely the changes of the INL and the main trend of the INL pattern is clearly visible in INL_F curve. Their maximum INLs are 0.27LSB and 0.18LSB respectively. The difference between them is only 0.09LSB, which is also within the acceptable range in measurement. Therefore, the proposed method is validated by the experimental results.

V. CONCLUSION

In this paper, a simple method to speed up the INL estimation of ADCs is presented, justified theoretically, and validated by means of both simulation and experimental results. In particular, the number of samples can be reduced significantly by the moving-average filtered sine wave code density test with the almost same accuracy of INL.

It is worth noting that the proposed method can only estimate the smooth part of the ADC INL curve, and should never be used to assess the maximum static INL usually reported in ADC data-sheets and in instrument specifications. But it can be very accurate when the ADC has a smooth nonlinear characteristic. This circumstance is especially likely to occur when resolution-enhancement techniques such as "dithering" technique are used, because these techniques usually "smear" the static characteristic of ADCs [7].

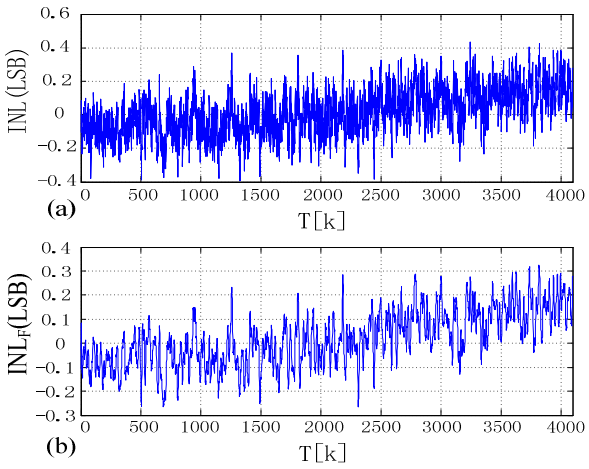

Figure 2. INL patterns of a simulated 12-bit ADC: (a) the INL curve estimated by the conventional method in 4.2×10^6 samples. (b) the INL curve estimated by the proposed method in 2.5×10^5 samples.

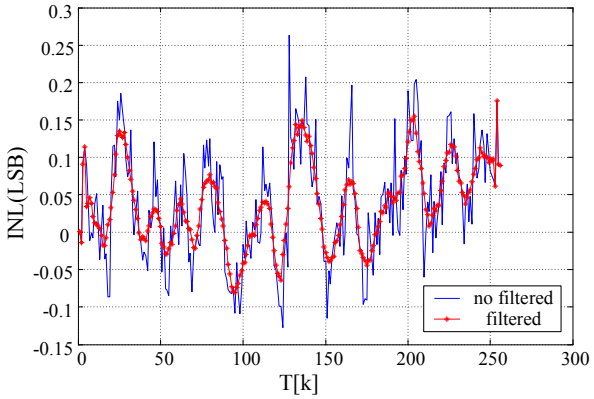

Figure 3. INL patterns of a commercial 8-bit ADC obtained by the conventional method (blue solid line) and the proposed method (red asteroid line).

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