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Accurate Digital Synthesis of Sinewaves

D. A. Lampasi[1], A. Moschitta[2], P. Carbone[2]

[1]Department of Electrical Engineering, University of Rome "La Sapienza"
Via Eudossiana, 18 – 00184 Rome, Italy
Phone: +39 06 44585543, Fax: +39 06 4883235, E–mail: alessandro.lampasi@uniroma1.it

[2]Department of Electronic and Information Engineering, University of Perugia
Via G. Duranti, 93 – 06125 Perugia (PG), Italy
Phone: +39 075 5853933, Fax: +39 075 5853654, E–mail: {antonio.moschitta, paolo.carbone}@diei.unipg.it

Abstract – *In this paper, the generation of spectrally pure sinusoidal signals is discussed. The proposed technique is implemented on a DSP and requires a digital–to–analog converter, an analog–to–digital converter and an analog filter. A modified $\Delta\Sigma$ topology is adopted to efficiently estimate and compensate the digital–to–analog converter non–linearities, while desensitizing the system to the non–idealities of the remaining circuital elements. It is shown that the proposed technique can improve the spurious–free dynamic range of the generated signal.*

Keywords – *Analog–to–digital conversion, digital–to–analog conversion, nonlinear distortion, sigma–delta modulation.*

I. INTRODUCTION

Sinewaves are a very important class of signals, not only because virtually every kind of signal can be obtained as a sum of sinewaves, but also because sinewave stimuli are widely used for communication systems, for analog and mixed–signal testing purposes, analog circuit fault diagnosis [1] and are the subject of various research and standardization activities [2] [3]. For example, the dynamic parameters of an analog–to–digital converter (ADC), but also its integral (INL) and differential (DNL) non–linearity are commonly estimated using sinewave–based tests [4]. Obviously, the performance of such procedures requires the generation of spectrally pure sinusoidal signals.

It is also worth noticing that test activities constitute a more and more relevant percentage of the overall production costs of integrated circuits also because the high integration level of modern devices is dramatically reducing the ratio between the externally accessible nodes and the components to be verified [5]. Built–in self–test (BIST) addresses some of these problems by inserting test facilities directly inside the device under test (DUT) [6] [7]. In this case low hardware complexity and low sensitivity to the parameter variations of circuital components become an important requirement. Due to the intrinsic limitations of conventional analog circuitry advanced digital architectures like phase locked loops, oversampling–based digital resonators [8] and binary sequences [9] are frequently used.

Direct digital synthesis (DDS) is currently the most commonly used method for generating analog signals. It consists in feeding a digital–to–analog converter (DAC) with a digitized and periodically repeated version of the desired signal, stored in a look–up table (LUT). DDS allows achieves highly stable and reproducible performances but, for multi–bit converters, the quality of the generated signals is affected by the DAC resolution and linearity.

Even though test and error compensation methods are generally more developed for ADCs [10], various techniques have been proposed to improve DDS accuracy. A fast and simple approach is based on the cancelation of unwanted spectral components present at the DAC output by pre–distorting the DAC input [11] [12]. This approach requires measurement equipment with higher accuracy and linearity than the DAC to be compensated [13]. Otherwise, the estimation procedure may erroneously ascribe to the DAC an unwanted component produced by the measuring equipment itself, and worsen the DAC performances when attempting to correct it by introducing an unneeded term.

In a previous work, the authors proposed a feedback mechanism based on a modified first–order $\Delta\Sigma$ architecture, in order to desensitize the spectral estimation with respect to the quantization error introduced by an ADC used for this purpose [14] [15]. In this paper some improvements to such methodology are introduced. In particular, the loop is modified to achieve stability also for high open–loop gains and the correction is limited to the components included in the analog filter's band. The residual disturbance given by the ADC is removed by opening the loop after the closed–loop optimization of the LUT. Finally, the proposed algorithm is verified by means of simulations and entirely implemented on a DSP–based board, including a 16–bit ADC and a 16–bit DAC.

II. COMPENSATION OF DAC NON–IDEALITIES

If a DAC is used to generate a sinewave signal modeled as

$$x[n] = V_1 \sin\left(\frac{2\pi k_1 n}{N}\right), \qquad n = 0, 1, \ldots, N-1, \quad (1)$$

where N is the number of generated samples, its output $y(t)$ may also contain harmonics and non–harmonic spurious tones. Various solutions have been proposed in the literature to mitigate this effect. The approach considered in this paper consists in compensating the unwanted components by feeding the DAC input with a modified sequence $\widehat{x}[\cdot]$, obtained superimposing to the fundamental sinewave other C sinewaves whose frequencies coincide to the terms to be corrected:

$$\widehat{x}[\cdot] = x[\cdot] + x_c[\cdot], \qquad x_c[n] = \sum_{i=1}^{C} A_i \sin\left(\frac{2\pi k_i n}{N} + \varphi_i\right). \tag{2}$$

where $\widehat{x}[\cdot]$ is then suitably quantized to fit the DAC resolution. The core of this method is the estimation of the amplitude A_i and phase φ_i of the various unwanted components. To this aim a spectrum analyzer can be used [13]. This approach guarantees good performances but has some disadvantages:

- the phase information is usually lost, thus requiring multi–step estimations [13];
- the analysis is long and presumably must be performed off–line;
- no BIST strategies can be implemented.

As shown in the following the proposed closed–loop compensation technique addresses these problems and may be used for BIST purposes.

III. CLOSED–LOOP COMPENSATION

A. Models and stability analysis of the loop

The methodology proposed in [14] relies on a $\Delta\Sigma$–like topology (Fig. 1) including a DAC, an ADC and an analog low–pass filter with transfer function $H(z)$. At first, in order to improve the DAC output spectrum, the ADC output $y_{adc}[\cdot]$ is stored and its spectrum is estimated using DFT techniques to identify the required cancelation terms for updating the LUT. The ADC output is then added to LUT content $\widehat{x}[\cdot]$ and quantized to feed the DAC. Once all significant unwanted components have been removed the LUT is no longer updated.

Since high resolution data converters are assumed in the following, in order to analyze the stability of the proposed feedback topology, the quantizer has been considered as a unitary gain. Moreover, notice that both the ADC and the DAC may introduce latencies between the input and output sequences, whose effect can be taken into account by using the discrete–time constant delays d_{ADC} and d_{DAC} reported in Fig. 1. In the same figure e_{adc}, e_{dac} e_H model the ADC error, the DAC error and the error introduced by the analog low–pass filter. In [14], the properties of $|H(\cdot)| \gg 1$ were exploited to desensitize y_{adc} to e_{adc}. The capability of the system to discriminate between ADC and DAC error contributions increases with the magnitude of $H(z)$ [14]. However, this cannot be arbitrarily raised, as the feedback loop may become unstable. Such a behavior was observed during experimental verifications, also because

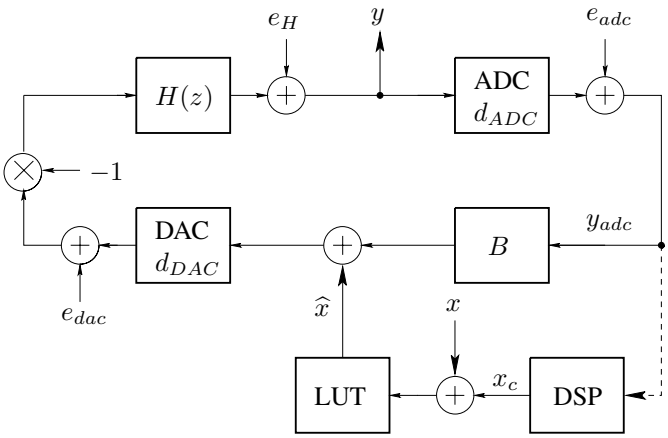

Fig. 1. Discrete–time model of the architecture used for closed–loop compensation.

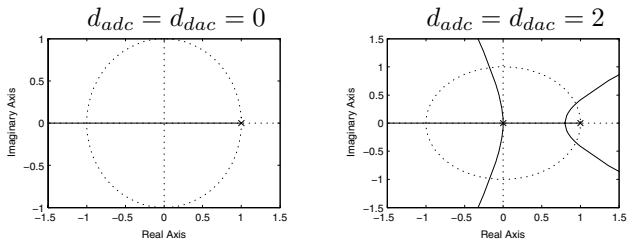

Fig. 2. Root locus assuming ideal integrator (3), data converters and different delays.

the delays d_{adc} and d_{dac} apparently reduce the phase margin and force the reduction of the loop gain.

To this aim, the stability of the considered system has been analyzed using the root locus technique as a function of a digital gain B inserted after the ADC to improve the system stability [17]. Fig. (2) shows the root locus for the system shown in Fig. 1, assuming an ideal integrator

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{3}$$

with various converter delays. In the first considered case, $d_{adc} = d_{dac} = 0$ and the pole is on the unitary circle for $B = 2$. In the second one, $d_{adc} = d_{dac} = 2$ and the dominant poles cross the circle for $B \simeq 0.34$. Therefore, the stability may become critical even for relatively small delays. However, to achieve the stability of the system independently of the variations of the analog and mixed hardware, the digital attenuation B shown in Fig. 1 is changed, after an estimation of $|H(0)|$, to satisfy the empirically determined condition

$$B \simeq \frac{1}{|H(j\omega)|} \simeq \frac{1}{|H(0)|} \ll 1, \quad \omega \quad \text{in the filter passband,} \tag{4}$$

which is also expected to prevent ADC and DAC overloading.

B. The Modified Procedure

The z-transform of the ADC output sequence can be written as follows[1]

$$Y_{adc}(z) = \frac{H(z)}{1+H(z)B}\widehat{X}(z) + \frac{H(z)}{1+H(z)B}E_{dac}(z) + \frac{1}{1+H(z)B}E_H(z) + \frac{1}{1+H(z)B}E_{adc}(z). \quad (5)$$

The analog signal generated at the output of the analog filter is:

$$Y(z) = \frac{H(z)}{1+H(z)B}\widehat{X}(z) + \frac{H(z)}{1+H(z)B}E_{dac}(z) + \frac{1}{1+H(z)B}E_H(z) + \frac{H(z)B}{1+H(z)B}E_{adc}(z). \quad (6)$$

Instead of estimating the unwanted components in (2) by processing the analog sequence $y[\cdot]$, the analysis is applied to the available digital sequence $y_{ADC}[\cdot]$. Nevertheless, when $|H(z)| \gg 1$ and (4) is verified, it can be observed that

$$|H(z)B| \to 1, \qquad \left|\frac{H(z)}{1+H(z)B}\right| \gg 1, \quad (7)$$

Therefore, due to the amplification by a factor $|H(z)|$, the contribution of e_{adc} on the measured signal y_{adc} is negligible with respect to e_{dac}, thus relaxing the ADC linearity requirements.

The removal of the errors from the $y_{adc}[\cdot]$ sequence does not imply the same effect on $y[\cdot]$. In fact, since

$$y[\cdot] \simeq y_{adc}[\cdot] - e_{adc}[\cdot] \quad (8)$$

the ADC error components may appear uncompensated in the analog output sequence. In order to avoid this phenomenon, the procedure proposed in [14] was modified as shown in the following. The algorithm operates on an iterative basis, updating the LUT after an appropriate evolution of the loop, by identifying and removing each time only the most powerful component:

$$k_i = \underset{\substack{k\in\mathcal{I}\\ k\neq k_0}}{\operatorname{argmax}} |Y_{adc}[k]|. \quad (9)$$

where $\mathcal{I}$ is the interval of digital frequency bins on which the procedure is applied, corresponding to the band characterized by high values of $|H(j\omega)|$, that is $|H(j\omega)| \gg 1$. This restriction ensures that, provided that the non–linearities of the data converters are weak and comparable, only the DAC contribution is identified and compensated. Furthermore, since only a

[1] Capital letters represent the z-transforms of the corresponding sequences.

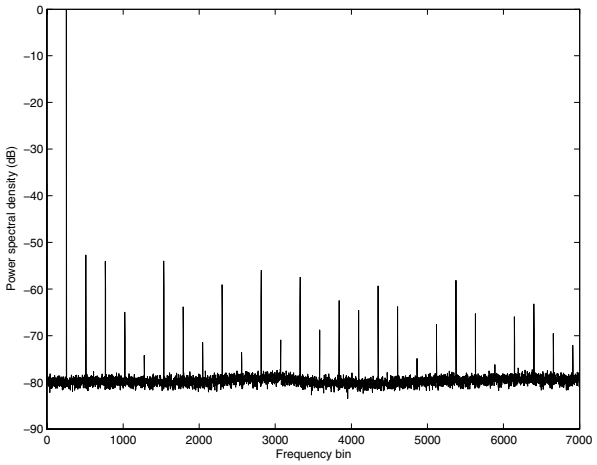

Fig. 3. Power spectrum of the signal $y[\cdot]$ generated by a simulated 8–bit DAC affected by a non–linearity randomly generated in ± 0.5 LSB.

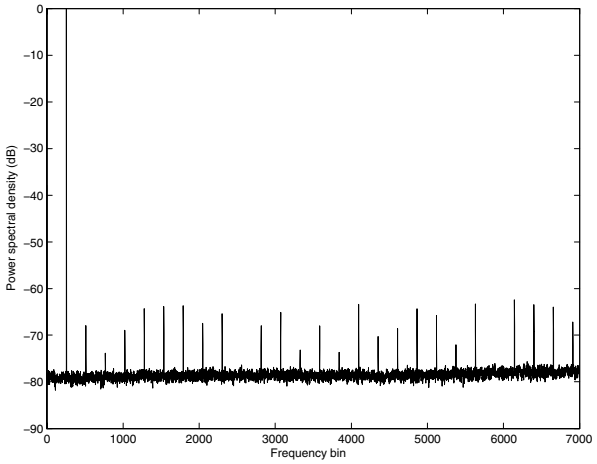

Fig. 4. Power spectrum of the signal $y[\cdot]$ generated by a simulated 8–bit DAC affected by a non–linearity randomly generated in ± 0.5 LSB after closed–loop compensation over the whole bandwidth $[0, N/2-1]$ $(N = 2^{14})$.

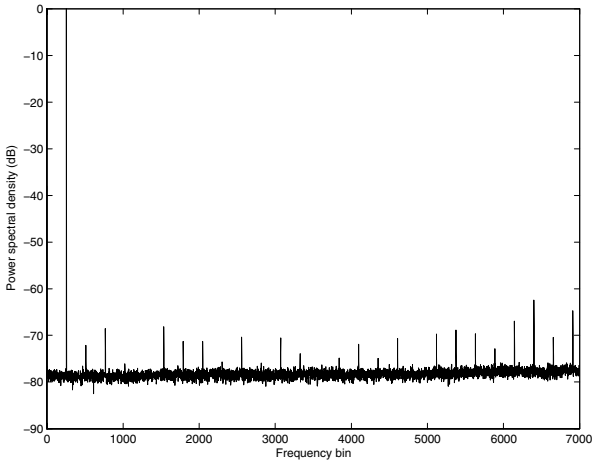

Fig. 5. Power spectrum of the signal $y[\cdot]$ generated by a simulated 8–bit DAC affected by a non–linearity randomly generated in ± 0.5 LSB, after a closed–loop compensation limited to the interval $[0, (3/8)N-1]$, $(N = 2^{14})$.

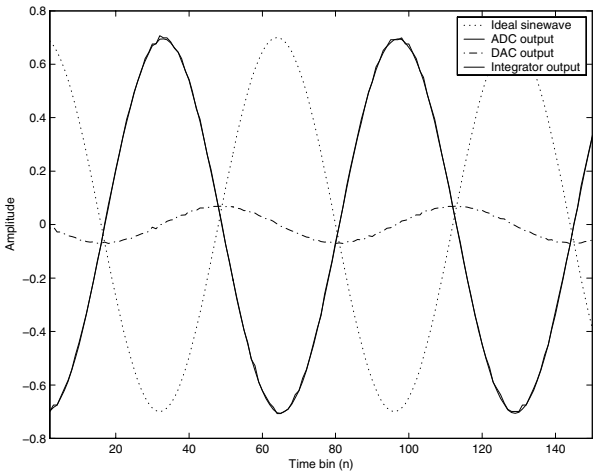

Fig. 6. Typical sequences generated during the closed–loop simulations.

few low–order harmonics are usually significant, the number of iterations is expected to be reasonably low.

Once k_i has been selected according to (9), its amplitude A_i and phase φ_i can be estimated from $Y_{adc}[k_i]$ and corrected using the frequency response relating $\widehat{x}[\cdot]$ and $y_{adc}[\cdot]$. Observe that the condition $|H(k_i)| \gg 1$ may be used to avoid the on–line estimation of the parameters in (2). In fact, in this case, the transfer function relating $\widehat{x}[\cdot]$ and $e_{dac}[\cdot]$ to $y[\cdot]$ reduces to $H(k_i)/2$.

In order to mitigate the effect of the error introduced by the ADC in the desired analog signal, at the end of the correction procedure, the loop is opened. Thus, only the compensated DAC unwanted components are expected to appear in the analog output, as the ADC is disconnected. This can be accomplished by setting $B = 0$ in the feedback loop and in the preceding equations. The compensation is still valid if the DAC input dynamic range does not change under both conditions. This may be forced by halving the open–loop LUT content, since $\frac{1}{1+H(z)B} \simeq 0.5$.

Fig. 3 and 4, obtained from simulations, show the signal spectrum at the output of the low–pass filter (3) before and after applying the correction procedure over the entire digital spectrum $(0, \frac{N}{2} - 1)$ where $N = 2^{14}$. An 8–bit DAC is assumed affected by a non–linearity randomly generated in ± 0.5 LSB and having full scale (FS) equal to 1. The simulated ADC has also 8–bit, $FS = 1$ and is affected by INL randomly generated in ± 0.5 LSB. Fig. 5 was obtained by applying the same algorithm in the reduced frequency range $(0, \frac{3}{8}N - 1)$. In this second case better results are achieved because the correction algorithm is applied only in the high gain frequency region.

Fig. 6 shows a time window of some sequences generated in the same simulations. The signal at the DAC output is remarkably smaller than its FS and therefore the DAC uses only a limited number of levels. Accordingly, it can be inferred that a good accuracy may still be obtained also using a low resolution DAC.

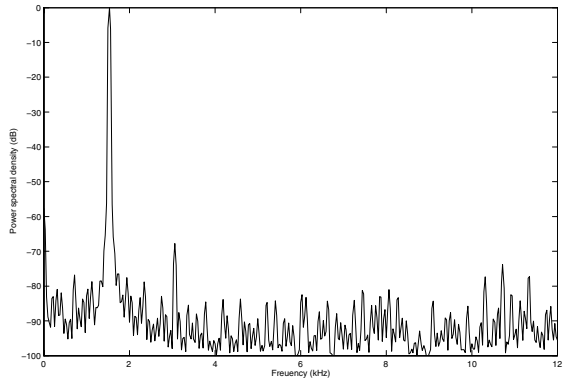

Fig. 7. Power spectrum of the uncorrected signal generated by a 16–bit DAC and conditioned by an active filter with low–frequency gain, $H(0) = 20$.

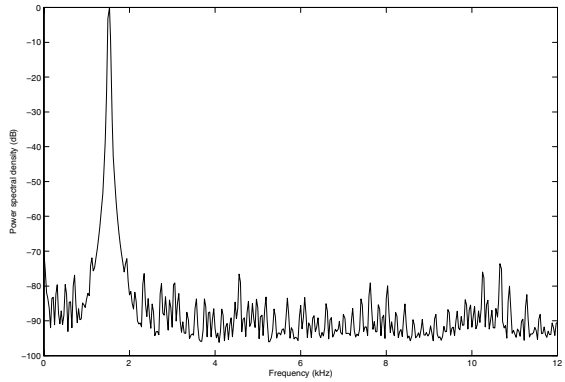

Fig. 8. Power spectrum of the signal generated by a 16–bit DAC and conditioned by an active filter with low–frequency gain, $H(0) = 20$, after a closed–loop compensation over a band corresponding to the first 4 harmonics.

IV. EXPERIMENTAL RESULTS

The proposed algorithm was tested on a DSP C6713 integrated on a development board DSK6713 in order to improve a 1.53 kHz sinewave generated by a 16–bit Burr Brown/Texas Instrument DAC8831, measured by a 16–bit Texas ADS8402. The simultaneous generation and acquisition is ensured by controlling the converters through two independent fast interfaces: a serial pheripheral interface (SPI) port for the DAC and a parallel port for the ADC. The high gain is obtained by an active filter with $|H(j\omega)| = 20$ over a 7 kHz band and assuming $B = 1/20$. Each component is estimated by averaging 50 DFT–based periodograms of $y_{adc}[\cdot]$ with $N = 1024$. The analysis is limited to the first 4 harmonics and the algorithm is iterated 30 times.

Fig. 7 and 8 compare the open–loop spectra measured at the filter's output by a network analyzer before and after applying the compensation algorithm. The proposed setup is able to correct the harmonic present in the low–frequency range. It can be

observed that the spurious–free dynamic range has increased by about 10 dB.

V. CONCLUSION

A technique has been presented which allows the improvement of the spurious free dynamic range of a DAC–based sinewave generator. The technique modifying a previously presented feedback topology, effectively removes the harmonics introduce by the DAC nonlinearities, after an estimation scarcely sensitive to the nonlinearity of the ADC used to this purpose. Theoretical, simulation and experimental results have been presented to validate the proposed approach.

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