Accurate Digital Synthesis of Sinewaves

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***Abstract*—This paper discusses the digital synthesis of spectrally pure sinusoidal signals. A modified Σ–Δ topology consisting of a digital-to-analog converter (DAC), an analog-to-digital converter (ADC), and an analog filter is adopted to efficiently estimate and compensate the DAC nonidealities while desensitizing the system to those of the remaining elements. The proposed correction procedure was implemented on a digital signal processing board equipped with general-purpose data converters. It is shown that the technique can improve the spurious-free dynamic range of the generated signals without requiring high-performance measurement equipment.**

***Index Terms*—Analog-to-digital conversion (ADC), digital-to-analog conversion (DAC), error compensation, nonlinear distortion, sigma–delta modulation.**

I. Introduction

SINEWAVES are a very important class of signals, not only because their sum can reproduce virtually every kind of signal but, also, because sinewave stimuli are widely used in communication systems for analog- and mixed-signal testing purposes and analog-circuit-fault diagnosis [1] and are the subject of various research and standardization activities [2], [3]. For example, the dynamic parameters of an analog-to-digital converter (ADC) and its integral (INL) and differential nonlinearity are commonly estimated using sinewave-based tests [4]. Obviously, the performance of such procedures is related to the spectral purity of the generated signals.

It is worth noting that test activities constitute an increasingly more relevant percentage of the overall costs necessary for the production and the optimal management of integrated circuits, because the high integration level of modern devices is also dramatically reducing the ratio between the externally accessible nodes and the components to be verified [5]. Built-in self-test (BIST) addresses some of these problems by inserting test facilities directly inside the device-under-test [6], [7]. In this case, low hardware complexity and low sensitivity to the parameter variations of circuital components become important requirements. Due to the intrinsic limitations of conventional analog circuitry, advanced digital architectures, like phase-locked loops, oversampling-based digital resonators [8], [9], and binary sequences [10], are frequently used.

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Direct digital synthesis (DDS) is currently the most common method for generating analog signals. It consists of feeding a digital-to-analog converter (DAC) with a digitized and periodically repeated version of the desired signal stored in a look-up table (LUT). DDS allows one to achieve highly stable and reproducible performances, but for multibit converters, the quality of the generated signals is affected by the DAC resolution and linearity.

Even though test and error compensation methods are generally more developed for ADCs [11], various techniques have been proposed to improve DDS accuracy. A fast and simple approach is based on the cancellation of unwanted spectral components present at the DAC output by predistorting the input sequence [12], [13]. This approach, of course, requires measurement equipment with higher accuracy and linearity than the DAC to be compensated [12]. Otherwise, the estimation procedure may erroneously ascribe to the DAC a component produced by the measuring equipment itself and, therefore, worsen the DAC performances when attempting to correct it by introducing an unneeded term.

In previous works, the authors proposed a feedback mechanism based on a modified first-order Σ–Δ architecture, in order to desensitize the spectral estimation with respect to the errors introduced by an ADC used for this purpose [14], [15]. In this paper, some improvements to such methodology are introduced and developed. In particular, the loop is modified to also achieve stability for high open-loop gains, and theoretical conditions for opening the loop are discussed in order to remove the residual disturbance after the closed-loop LUT optimization. Many numerical simulations were carried out to improve the algorithm settings and to investigate the influence of the ADC characteristics on the spectral estimation. Finally, the effectiveness of the procedure is verified by means of simulations and is entirely implemented on a digital signal processing-based board, including a 16-b ADC and a 16-b DAC.

II. Compensation of DAC Nonidealities

If a DAC is used to generate a sinewave signal modeled as

$$x[n] = A_0 \sin\left(\frac{2\pi k_0 n}{N}\right), \quad n = 0, 1, \ldots, N-1 \qquad (1)$$

where N is the number of generated samples, its output y_{dac} may also contain harmonic and nonharmonic spurious tones, which is shown in Fig. 1 by e_{dac}. Analogously, e_H models the error contribution introduced by an analog low-pass filter with transfer function $H(z)$ used for signal smoothing.

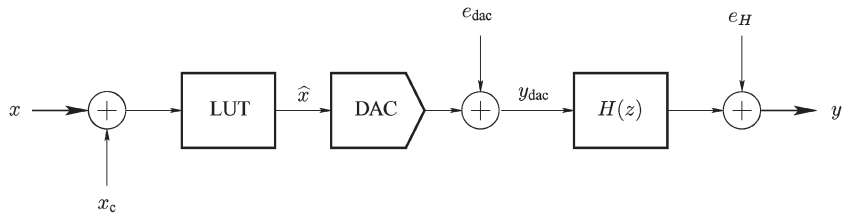

Fig. 1. Discrete-time model of a signal generation improved through a predistortion of the LUT content.

The discrete-time version of the resulting analog signal can be written as

$$Y(z) = H(z)X(z) + H(z)E_{\rm dac}(z) + E_H(z) \qquad (2)$$

where, as in the rest of this paper, capital letters represent the z-transforms of the corresponding sequences. Various solutions have been proposed in the literature to mitigate this effect. The approach considered in this paper consists of compensating the unwanted components by feeding the DAC input with a modified sequence $\widehat{x}[\cdot]$ (Fig. 1) that is suitably quantized to fit the DAC resolution and is obtained by superimposing it on the fundamental sinewave of other C sinewaves, whose frequencies coincide with the terms to be corrected

$$\widehat{x}[\cdot] = x[\cdot] + x_{\rm c}[\cdot], \quad x_{\rm c}[n] = \sum_{i=1}^{C} A_i \sin\left(\frac{2\pi k_i n}{N} + \varphi_i\right). \qquad (3)$$

The core of this method is the estimation of the amplitude A_i and phase φ_i of the various unwanted components. To this aim, a spectrum analyzer can be used [12]. This approach guarantees good performances but has the following disadvantages:

1) The phase information is usually lost, thus requiring multistep estimations [12].
2) The analysis is time-consuming and, presumably, must be performed offline.
3) No BIST strategies can be implemented.

As shown in the following sections, the proposed closed-loop compensation technique overcomes these problems and may be used for BIST purposes.

III. Closed-Loop Compensation

A. Models and Stability Analysis of the Loop

The methodology proposed in [14] relies on a Σ–Δ-like topology (Fig. 2), including a DAC, an ADC, and an analog low-pass filter $H(z)$ [16]. At first, in order to improve the DAC output spectrum, the ADC output $y_{\rm adc}[\cdot]$ is stored, and its spectrum is estimated using DFT techniques to identify the required cancellation terms for updating the LUT, as shown in Fig. 2 by the branch derived from the dashed line. The ADC output is then added to the LUT content $\widehat{x}[\cdot]$ and quantized to feed the DAC. Once all the significant unwanted components have been removed, the LUT is no longer updated.

Since high-resolution data converters are assumed in the following, in order to analyze the stability of the proposed feedback topology, a unitary gain quantizer has been considered. Moreover, both the ADC and the DAC may introduce latencies between the input and output sequences, whose effect can be taken into account by using the discrete-time constant delays $d_{\rm adc}$ and $d_{\rm dac}$ shown in Fig. 2. In the same figure, $e_{\rm adc}$, $e_{\rm dac}$, and e_H model the ADC error, the DAC error, and the error introduced by the analog low-pass filter that was not considered in [14]. In [14], the properties of $|H(z)| \gg 1$ were exploited to desensitize $y_{\rm adc}$ with respect to $e_{\rm adc}$. The capability of the system to discriminate between ADC and DAC error contributions increases with the magnitude of $H(z)$. However, this analog gain cannot be arbitrarily raised, as the feedback loop may become unstable. Such behavior was observed during experimental verifications, because the delays $d_{\rm adc}$ and $d_{\rm dac}$, apparently, also reduce the phase margin and force the reduction of the loop gain.

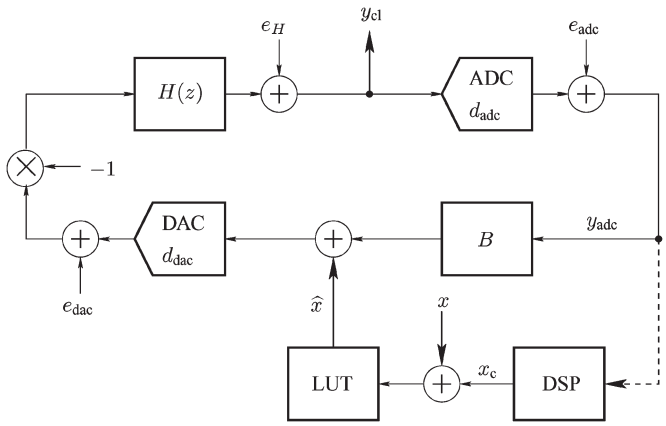

Fig. 2. Discrete-time model of the architecture used for closed-loop compensation.

To this aim, the stability of the considered system has been analyzed using the root-locus technique [9] as a function of a digital gain B inserted after the ADC to improve system stability [17]. Fig. 3 shows the root locus for the system in Fig. 2, assuming an ideal integrator

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \qquad (4)$$

with two different sets of converter delays. In the first considered case, $d_{\rm adc} = d_{\rm dac} = 0$, and the pole is on the unitary circle for $B = 2$. In the second one, $d_{\rm adc} = d_{\rm dac} = 2$, and the dominant poles cross the circle for $B \simeq 0.34$. Therefore, the stability may become critical even for relatively small delays. However, to achieve the stability of the system independently of the variations of the analog and mixed hardware, the digital attenuation B shown in Fig. 2, and not included in [14], can be

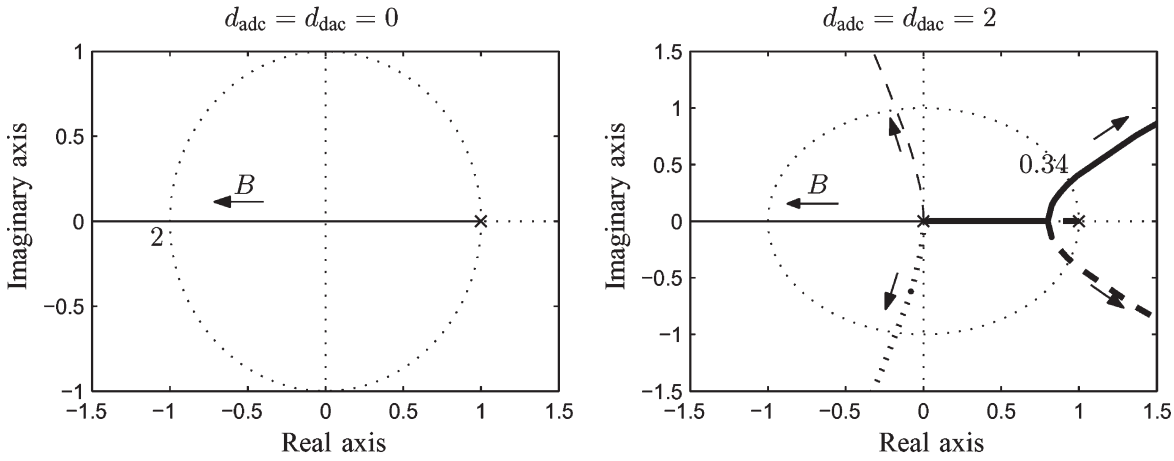

Fig. 3. Root locus of the closed-loop system assuming $H(z)$ equal to the ideal integrator [see (4)] and different delays for the data converters.

changed, even after a free evolution of the system presenting an unstable behavior. For example, B may be fixed, after an estimation of the low-frequency gain H_0, to satisfy the empirically determined condition

$$B \simeq \frac{1}{|H(j\omega)|} \simeq \frac{1}{H_0} \ll 1, \qquad \omega \quad \text{in the filter pass-band} \tag{5}$$

which is also expected to prevent ADC and DAC overloading.

B. Modified Procedure

The z-transform of the ADC output sequence can be modeled as follows:

$$Y_{\rm adc}(z) = -\frac{H(z)}{1+H(z)B}\widehat{X}(z) - \frac{H(z)}{1+H(z)B}E_{\rm dac}(z) + \frac{1}{1+H(z)B}E_H(z) + \frac{1}{1+H(z)B}E_{\rm adc}(z). \tag{6}$$

The analog signal generated at the output of the analog filter is

$$Y_{\rm cl}(z) = -\frac{H(z)}{1+H(z)B}\widehat{X}(z) - \frac{H(z)}{1+H(z)B}E_{\rm dac}(z) + \frac{1}{1+H(z)B}E_H(z) - \frac{H(z)B}{1+H(z)B}E_{\rm adc}(z). \tag{7}$$

Instead of estimating the unwanted components and the relative correction terms in (3) by processing the analog sequence $y_{\rm cl}[\cdot]$, the analysis is applied to the only available quantity: the digital sequence $y_{\rm adc}[\cdot]$. Nevertheless, when $|H(z)| \gg 1$ and (5) are verified, it can be observed that

$$|H(z)B| \to 1, \qquad \left|\frac{H(z)}{1+H(z)B}\right| \gg 1. \tag{8}$$

Therefore, due to the amplification by a factor $|H(z)|$, the contribution of $e_{\rm adc}$ on the measured signal $y_{\rm adc}$ is negligible with respect to $e_{\rm dac}$, thus relaxing the ADC linearity requirements. The same consideration applies for the contribution of e_H. Moreover, the insertion of the digital attenuation B in the structure proposed in [14] also reduces the influence of the ADC on the analog output.

The procedure proposed in [14] was modified as shown in the following. The algorithm operates on an iterative basis, updating the LUT after an appropriate evolution of the loop, by identifying and removing each time of only the most powerful undesired component of $y_{\rm adc}[\cdot]$

$$k_i = \arg\max_{\substack{k\in\mathcal{I}\\ k\neq k_0}} |Y_{\rm adc}[k]| \tag{9}$$

where $Y_{\rm adc}[\cdot]$ represents the DFT of $y_{\rm adc}[\cdot]$, and $\mathcal{I}$ is the interval of digital frequency bins on which the procedure is applied, corresponding to the band characterized by high values of $|H(j\omega)|$, i.e., $|H(j\omega)| \gg 1$. This restriction ensures that, provided that the unwanted harmonic components are comparable, only the DAC contribution is identified and compensated. Furthermore, since only a few low-order harmonics are usually significant, the number of iterations is expected to be reasonably low.

Once k_i has been selected according to (9), the amplitude A_i and phase φ_i of the corresponding component can be estimated from $Y_{\rm adc}[k_i]$ and corrected using the frequency response relating $\widehat{x}[\cdot]$ and $y_{\rm adc}[\cdot]$. Observe that the condition $|H(j\omega_i)| \gg 1$, with ω_i corresponding to the selected bin k_i, may be used to avoid the online estimation of the parameters in (3). In fact, in this case, the transfer function relating $\widehat{x}[\cdot]$ and $e_{\rm dac}[\cdot]$ to $y_{\rm cl}[\cdot]$ reduces to $H(j\omega_i)/2$.

The compensation term is able to change the magnitude and the phase of each spectral component $Y_{\rm adc}(j\omega)$ of $y_{\rm adc}[\cdot]$ and then allows one to cancel an unwanted component introduced by $e_{\rm dac}[\cdot]$. Equations (6) and (7) show that both the ADC output $Y_{\rm adc}(j\omega)$ and the analog output $Y_{\rm cl}(j\omega)$ are desensitized to the ADC harmonics in the high-gain bandwidth of $H(j\omega)$, because the transfer functions relating the LUT content $\widehat{X}(z)$ and the DAC error $E_{\rm dac}(z)$ to such outputs are magnified by $|H(z)|$ with respect to the corresponding transfer functions associated with the ADC error $E_{\rm adc}(z)$. Notice that the correction algorithm, based on the spectral analysis of the ADC output, does not select an ADC harmonic component for removal, unless it exceeds the highest DAC harmonic by at least $|H(j\omega)|$. Consequently, for each considered harmonic frequency ω_i, two

cases are possible, summarized by the expression in (10a) and (10b), shown at the bottom of this page, which relate the analog output $Y_{\rm cl}(j\omega_i)$ to $E_{\rm adc}(j\omega_i)$, depending on whether the correction algorithm ignores or erroneously selects the ADC harmonic for cancellation. In particular, (10a) is the transfer function reported in (7), while (10b) takes into account the correction term erroneously introduced in the LUT. Canceling an unwanted component at the ADC output corresponds to a performance improvement on the analog output. Analogously, the proposed solution removes harmonics and spurious terms introduced by the analog filter and described by $e_H[\cdot]$, which are treated by the algorithm like the DAC nonlinearities. By neglecting this further positive effect and by considering (10a) and (10b) for each removed harmonic component, the reduction in the total harmonic distortion (THD) [2] of the signal $y_{\rm cl}[\cdot]$ with respect to the original signal $y[\cdot]$, which is generated using a filter whose spectral influence on the considered components can be approximated with H_0, may be expressed as the expression in (11a) and (11b), shown at the bottom of the page. Thus, the procedure improves the spurious-free dynamic range (SFDR) [2] of the generated analog signal, provided that the ADC distortion does not dominate the DAC one. Since the error sequence $e_{\rm adc}[\cdot]$ is not magnified by the filter gain as $e_{\rm adc}[\cdot]$ in (2), under the hypothesis that the characteristics of the two data converters are similar, the improvement is at least equal to H_0. Such a hypothesis is reasonable in practical systems, as shown in next section, but it is necessary to consider that the two converters' THDs in (11) refer to different amplitudes and, in some cases, full scales (FS).

At the end of the correction procedure, it may be useful to open the loop to reduce the influence of the ADC or, for example, to reuse the disconnected ADC in another generation channel. This can be accomplished by setting $B = 0$ in the feedback loop and in the preceding equations, but further considerations on this operation must be addressed. First, opening the loop is not expected to remove from $y_{\rm cl}[\cdot]$ any ADC harmonic component that was erroneously identified as a DAC contribution. This event corresponds to the detrimental introduction of an unneeded component in the LUT, which persists even if the loop is opened, as described by (10b), which actually does not depend on B. Conversely, when the ADC does not influence the LUT, (10a) and (11a) apply, and consequently, opening the loop may significantly improve the spectral purity of the generated signal. However, to still use the closed-loop compensation results in the open-loop configuration, the dynamic range and initial phase of the DAC input should not significantly change when the system topology is modified, because the amount of DAC nonlinearities depends on the excited DAC output levels. For a given frequency ω_0, this leads to the necessary condition

$$\frac{1}{1+H(j\omega_0)B_1}X_1(j\omega_0) \simeq \frac{1}{1+H(j\omega_0)B_2}X_2(j\omega_0) \quad (12)$$

where $x_1[\cdot]$ and $x_2[\cdot]$ are the ideal sinewaves inserted in the LUT for each considered topology. Thus, when the topology is altered by replacing B_1 with B_2, the new LUT content is expected to excite the same DAC output levels than the former case. In particular, when (5) applies and the loop is opened $(B = 0)$, (12) requires the LUT content obtained with the closed-loop compensation algorithm to be halved, as reported in [15]. However, modifying the entire LUT content $\widehat{x}[\cdot]$ rather than just $x[\cdot]$ may reduce the effectiveness of the closed-loop compensation, because (5) also leads to the neglecting of the phase requirements in (12).

IV. Analysis of a Simulated System

In this section, the proposed procedure is illustrated and optimized on a simulated system reproducing the architecture in Fig. 2. An 8-b DAC is assumed to be affected by INL that is randomly generated in a ± 0.3 least significant bit (LSB) and having FS equal to one. The simulated ADC has also 8 b, FS $= 1$, and, to stress the robustness of the technique, is affected by INL that is randomly generated in ± 0.5 LSB. Since the analog filter is the ideal integrator [see (4)], the system is stable, and a digital attenuation in the feedback part of the loop is not required $(B = 1)$.

A preliminary indication about the performance achievable by the compensation can be obtained by comparing the initial errors produced by the converters at the closed-loop operative conditions (Fig. 4). The spectra are evaluated from $y_{\rm cl}[\cdot]$ because, according to (7), the corresponding error transfer functions are identical. Since $e_{\rm adc}[\cdot]$ does not dominate $e_{\rm dac}[\cdot]$, the $\rm THD_{adc}/THD_{dac}$ ratio is not expected to be higher than one. Thus, (11) suggests that the compensation algorithm may be profitably applied to improve the spectral purity of the analog signal.

The positive effect of the analog gain can be viewed in Fig. 5, where the power spectrum estimated at the output of the simulated ADC is compared to the spectrum that would

$$Y_{\rm cl}(j\omega_i) \simeq Y_{\rm adc}(j\omega_i) - E_{\rm adc}(j\omega_i) \simeq \begin{cases} -\frac{H(j\omega_i)B}{1+H(j\omega_i)B}E_{\rm adc}(j\omega_i), & \text{for ignored ADC components} \quad (10a) \\ -E_{\rm adc}(j\omega_i), & \text{for erroneously corrected components} \quad (10b) \end{cases}$$

$$\frac{\rm THD_{Y_{cl}}}{\rm THD_Y} \simeq \begin{cases} \left(\frac{B}{1+H_0B}\right)\frac{\rm THD_{adc}}{\rm THD_{dac}}, & \text{if only the DAC harmonics are corrected} \quad (11a) \\ \left(\frac{1}{H_0}\right)\frac{\rm THD_{adc}}{\rm THD_{dac}}, & \text{if all the ADC harmonics are erroneously corrected} \quad (11b) \end{cases}$$

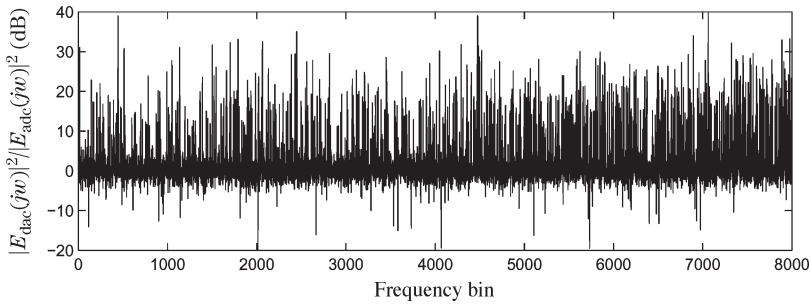

Fig. 4. Comparison between the power spectra of the initial errors $e_{\rm dac}[\cdot]$ and $e_{\rm adc}[\cdot]$ evaluated from $y_{\rm cl}[\cdot]$ at the closed-loop operative conditions.

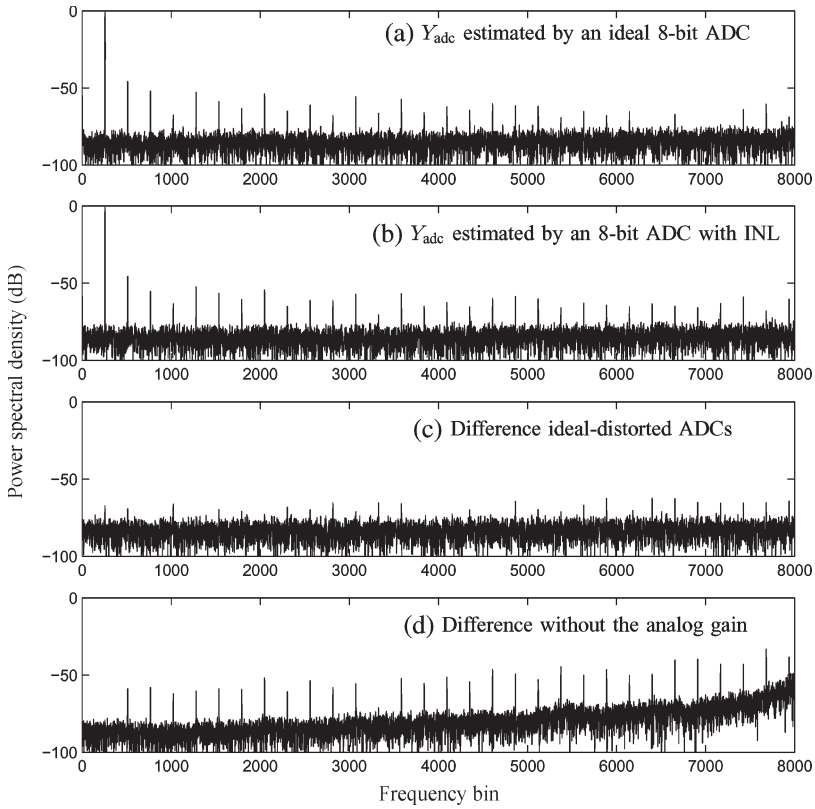

Fig. 5. Comparison between (a) the power spectrum measured by an ideal ADC and (b) the spectrum measured by an ADC with INL randomly generated in ± 0.5 LSB when inserted in a loop along with a nonideal DAC and a filter $H(z) = z^{-1}/(1 - z^{-1})$. (c) The third graph shows their difference. (d) The bottom graph shows the same difference when the ADCs operate in a loop with $H(z) = 1$, namely, without an analog gain.

be measured by an ideal ADC (zero INL) inserted in the loop under the same conditions. The differences introduced by the ADC nonlinearity are more evident when they are derived for a loop with $H(z) = 1$, as shown in Fig. 5(d). This example also shows a noise-shaping effect similar to that exploited in [18]. However, as shown in Section V, in practical cases, the undesired components are limited to the first harmonics.

Fig. 6 shows both the open-loop and closed-loop signal spectra at the output of the low-pass filter before and after applying the correction procedure. Simulation results show that inserting the DAC in the proposed Σ–Δ topology has a positive effect on the sinewave SFDR, even before applying the harmonic-removal procedure [Fig. 6(b)], possibly due to the change in the bandwidth/gain product and to a mutual interaction between the nonidealities induced by the feedback topology. The residual harmonics of the corrected $Y_{\rm cl}$ are presumably due to the $e_{\rm adc}[\cdot]$ contribution in (10), because most of them are also in the low-gain-frequency region of the analog filter, where both $Y_{\rm adc}(j\omega)$ and $Y_{\rm cl}(j\omega)$ are desensitized to the DAC harmonics. Thus, the obtained results of Fig. 6(c) may not be improved by further iterating the compensation algorithm. Such residual harmonics can be deleted by reopening the loop [Fig. 6(d)], even if the integrated low-frequency disturb limits the advantages obtained with compensation. The entire digital bandwidth $[0, N/2 - 1]$ with $N = 2^{14}$ was considered as suggested by the error rate in Fig. 4. Otherwise, better results can be achieved by reducing the search region $\mathcal{I}$ in (9) to the analog filter's high-gain band and producing a consequent attenuation of the higher order harmonics [15].

Fig. 7 compares a time window of some sequences generated in the same simulations to the desired output sinewave. The signal at the DAC output is remarkably smaller than its FS,

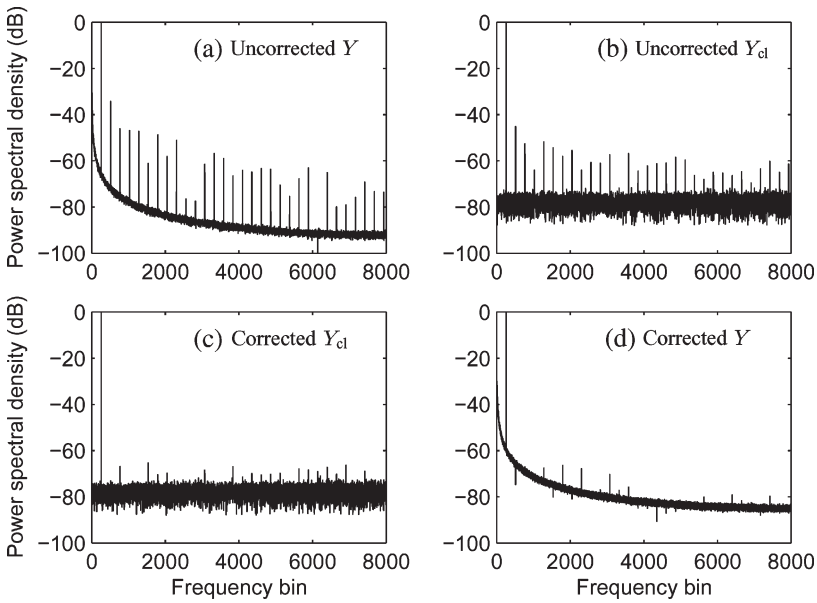

Fig. 6. Power spectrum of the signals synthesized by a simulated 8-b DAC affected by a nonlinearity randomly generated in ± 0.3 LSB and conditioned by the ideal integrator (4). (a) The uncorrected open-loop spectrum Y refers to the DAC not yet inserted in the loop. (b) The $Y_{\rm cl}$ spectra are reported, respectively, before starting the LUT optimization and (c) after the compensation over the whole digital bandwidth. (d) The last graph was obtained by reopening the loop after the closed-loop compensation.

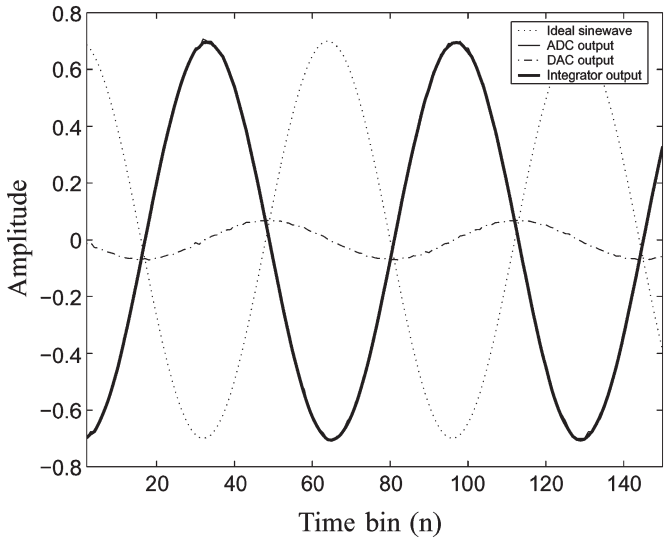

Fig. 7. Typical sequences generated during the closed-loop simulations.

and therefore, the DAC uses only a limited number of levels, corresponding to a 3–4-b reduction of the DAC effective resolution. Accordingly, it can be inferred that a good accuracy may still be obtained using also a low-resolution DAC, as the presented results rely on the feedback topology rather than on the DAC resolution.

Finally, to investigate the influence of the ADC resolution, the same simulations were repeated without modifying the other conditions but by simulating an ADC characterized by a number of bits lower than that of the DAC. Some results are showed in Fig. 8 for resolutions reduced to 7 b. Although the introduction of the correction terms produces an apparent deletion of the harmonics in $Y_{\rm adc}(j\omega)$, such an effect is not extended to $Y_{\rm cl}(j\omega)$, and hence, the performance obtained for 8 b, as in Fig. 6(c), cannot be reached. Nevertheless, the improvement is still appreciable for a 7-b ADC (Fig. 8), whereas the simulations showed that the compensation is almost ineffective when it is applied to a 6-b ADC.

V. Experimental Results

The described algorithm has been tested on a DSP C6713, operating at a clock frequency of 225 MHz and integrated on a DSK6713 development board in order to improve a 1.53-kHz sinewave generated by a 16-b Burr Brown/Texas Instrument DAC8831 and measured by a 16-b Texas ADS8402. An almost simultaneous generation and acquisition is ensured by controlling the converters through two independent fast interfaces: A serial peripheral interface port for the DAC, programmed to operate at a data rate of about 14 Mb/s, and a parallel port for the ADC that is able to operate with a clock of 100 MHz. The high gain has been obtained by an active op-amp-based low-pass filter with $|H(j\omega)| = 20$ over a 7-kHz band and assuming $B = 1/20$. Each component has been estimated by averaging 50 DFT-based periodograms of $y_{\rm adc}[\cdot]$ with $N = 1024$. As signal generation and sampling are both coherent, no windowing has been used, and the selected sinewave digital amplitude, exciting 12 of the 16 DAC bits, is the maximum allowed value which prevents ADC overloading. The analysis has been limited to the region that includes the first four harmonics, and the algorithm has been iterated 30 times.

Fig. 9 compares the open-loop spectra measured at the filter's output by a Stanford SR770 network analyzer, before and after applying the compensation algorithm. The proposed setup is able to correct the harmonic present in the low-frequency range. It can be observed that the SFDR has increased by about 10 dB. Moreover, the power spectrum of Fig. 9(b) shows an increased phase noise on the fundamental component. Such an effect can

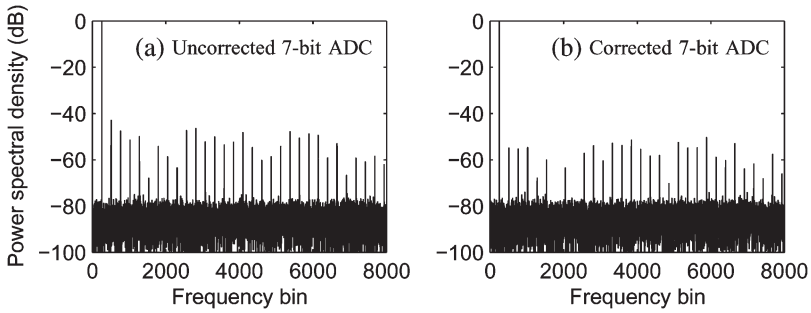

Fig. 8. Results of the technique when the simulated 8-b DAC is associated with an ADC characterized by a lower resolution. The closed-loop spectra Y_{cl} refer to a 7-b ADC (a) before and (b) after applying the correction procedure.

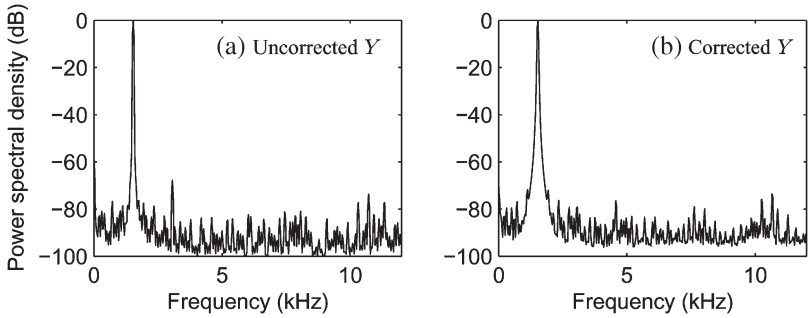

Fig. 9. Spectral characteristics of the signals generated by a 16-b DAC and conditioned by an active filter with low-frequency gain $H_0 = 20$ (a) before and (b) after a closed-loop compensation over a band corresponding to the first four harmonics.

be explained by observing that the phase noise in Fig. 9(a) is mostly due to the DAC sampling jitter and network-analyzer asynchronous sampling. Conversely, the correction algorithm is affected also by the ADC, whose sampling rate may be slightly different from the DAC one and may also be influenced by its own jitter and DSP parallel bus latency. This can reduce the accuracy of the estimation of the unwanted components and introduce noise at fundamental frequency when the LUT is updated. Simulation results obtained by improving the SFDR of an incoherently sampled sinewave show a similar effect, with a slightly increased phase noise affecting the corrected signal.

Finally, the obtained results have been compared with some examples reported in literature. The most similar approach [12] reports a similar SFDR improvement but using external instruments and offline algorithms. Moreover, the results in [12] refer to an initial distortion level higher than the one of the DAC8831 considered in this paper, which may be easier to correct. Comparable performances have been obtained in [7] and [10], while better accuracy can be reached by limiting the signal band [8], [18]. However, it is important to consider that the cited techniques require preventive analysis and optimizations [9], [10], whereas the architecture proposed in this paper offers a full agility in terms of both frequency and amplitude.

VI. Conclusion

The presented technique allows one to improve the dynamic range of a DAC-based sinewave generator. By exploiting a feedback topology, the spurious components introduced by the DAC are effectively removed, after an estimation scarcely sensitive to the nonlinearity of the ADC and of the analog circuitry used to this purpose. The closed-loop structure and the choices simplify the onboard identification of the correction parameters. If the distortions of the data converters are comparable, the performance improvement is related to the characteristics of an analog filter. Theoretical, simulation, and experimental results have been presented to validate the proposed approach.

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