



SC13: Ultrasound system design: Analog front end circuits, in-probe electronics and imaging systems

3rd September 2023

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Part 2: In-Probe Electronics

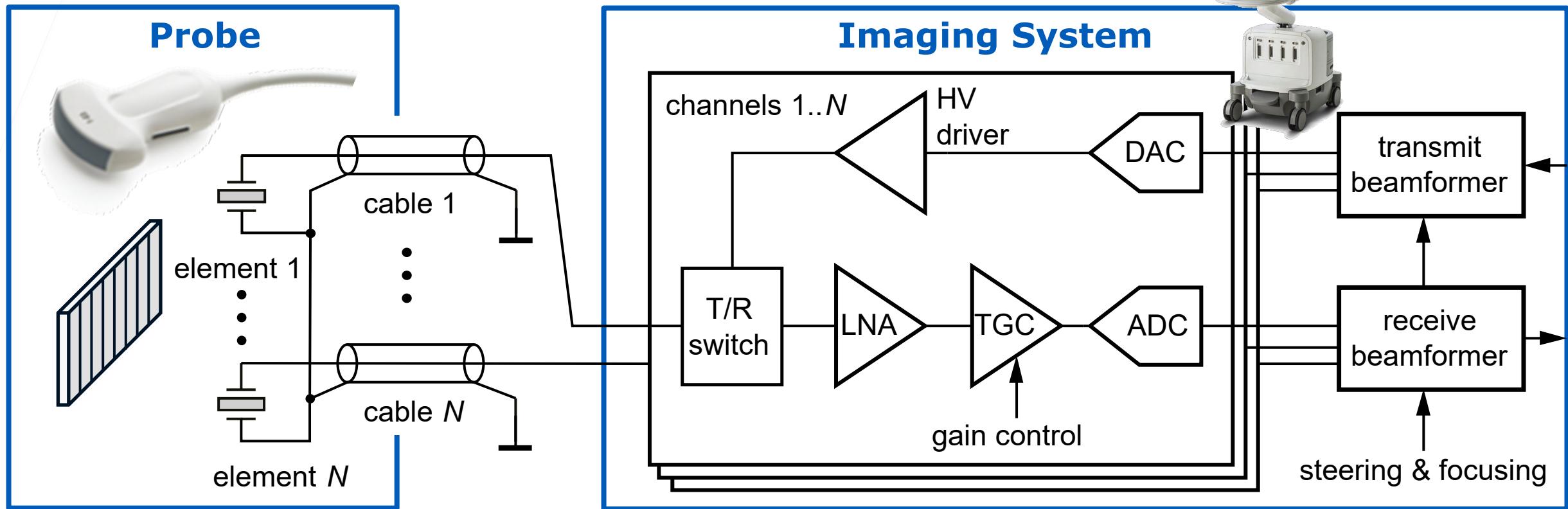
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3rd September 2023

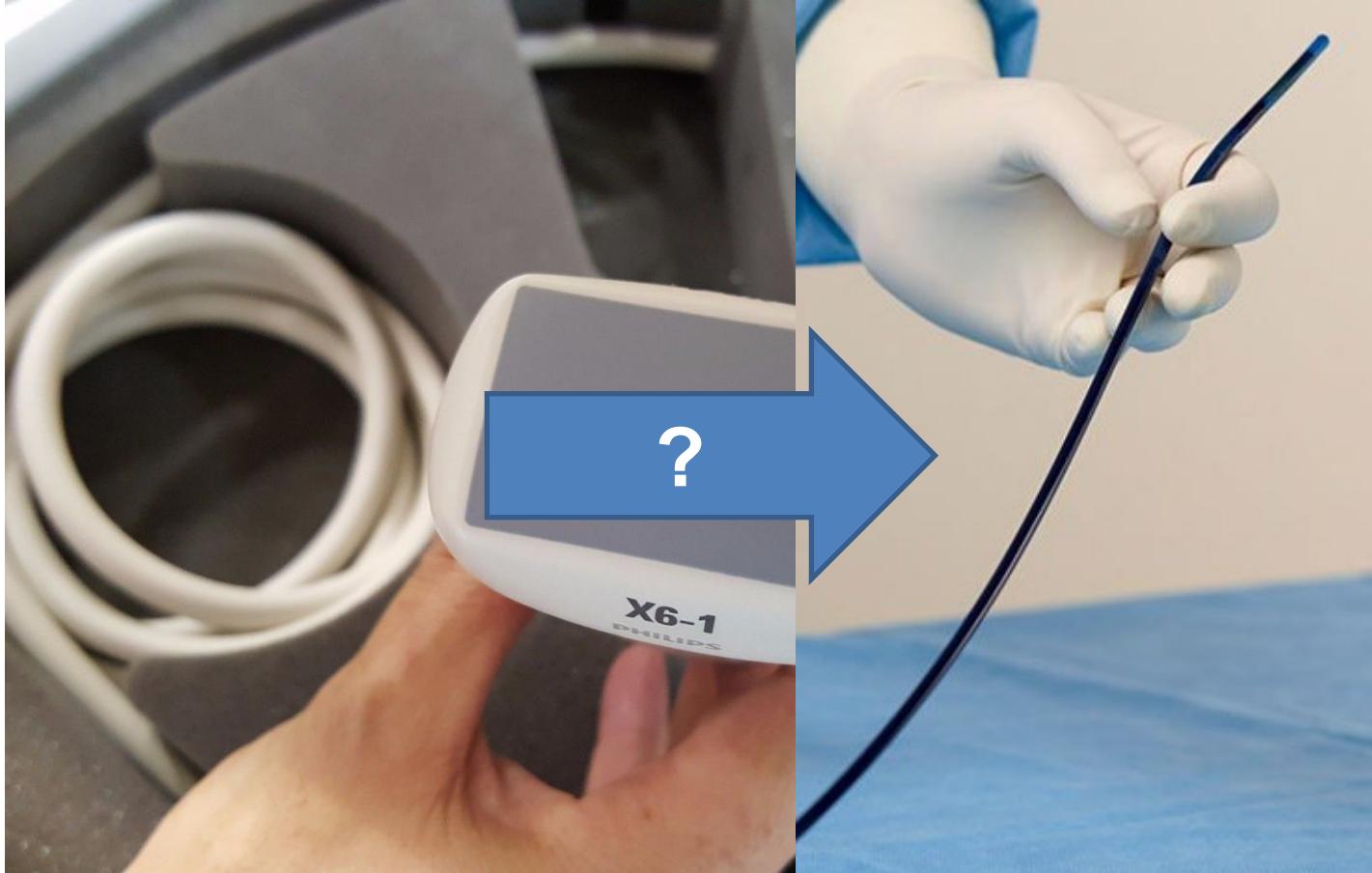


Ultrasound Imaging System



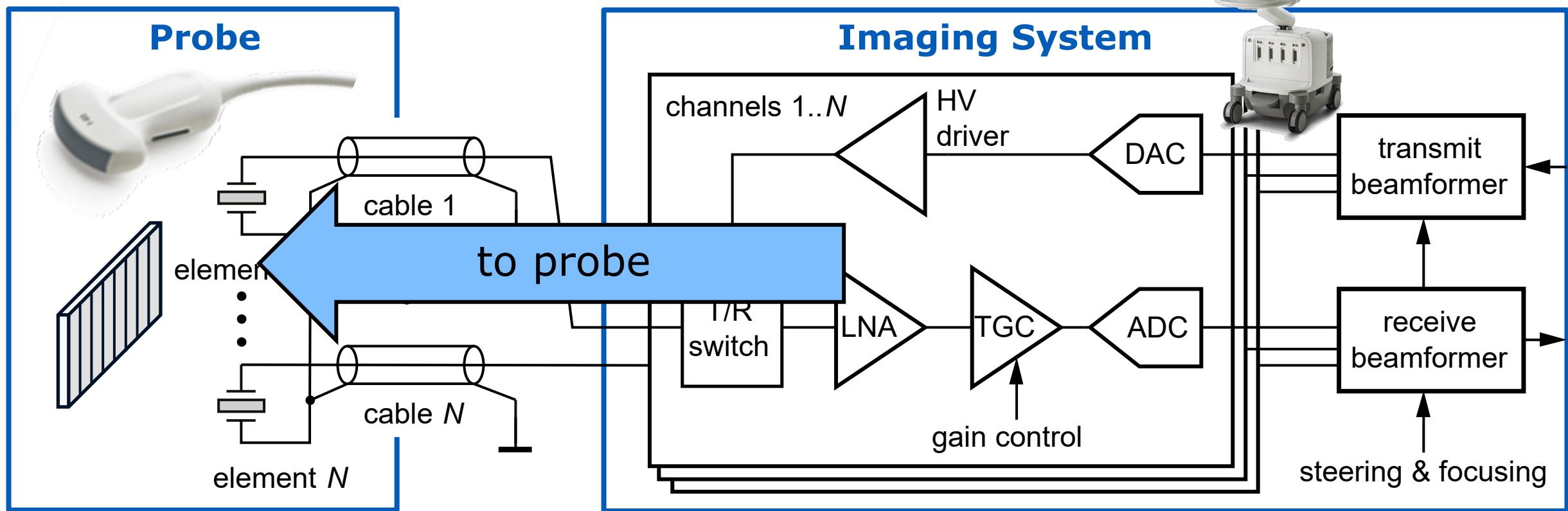
- One cable and one system channel per transducer element
- Practical systems typically 128, max 256 channels

Miniaturization is Challenging



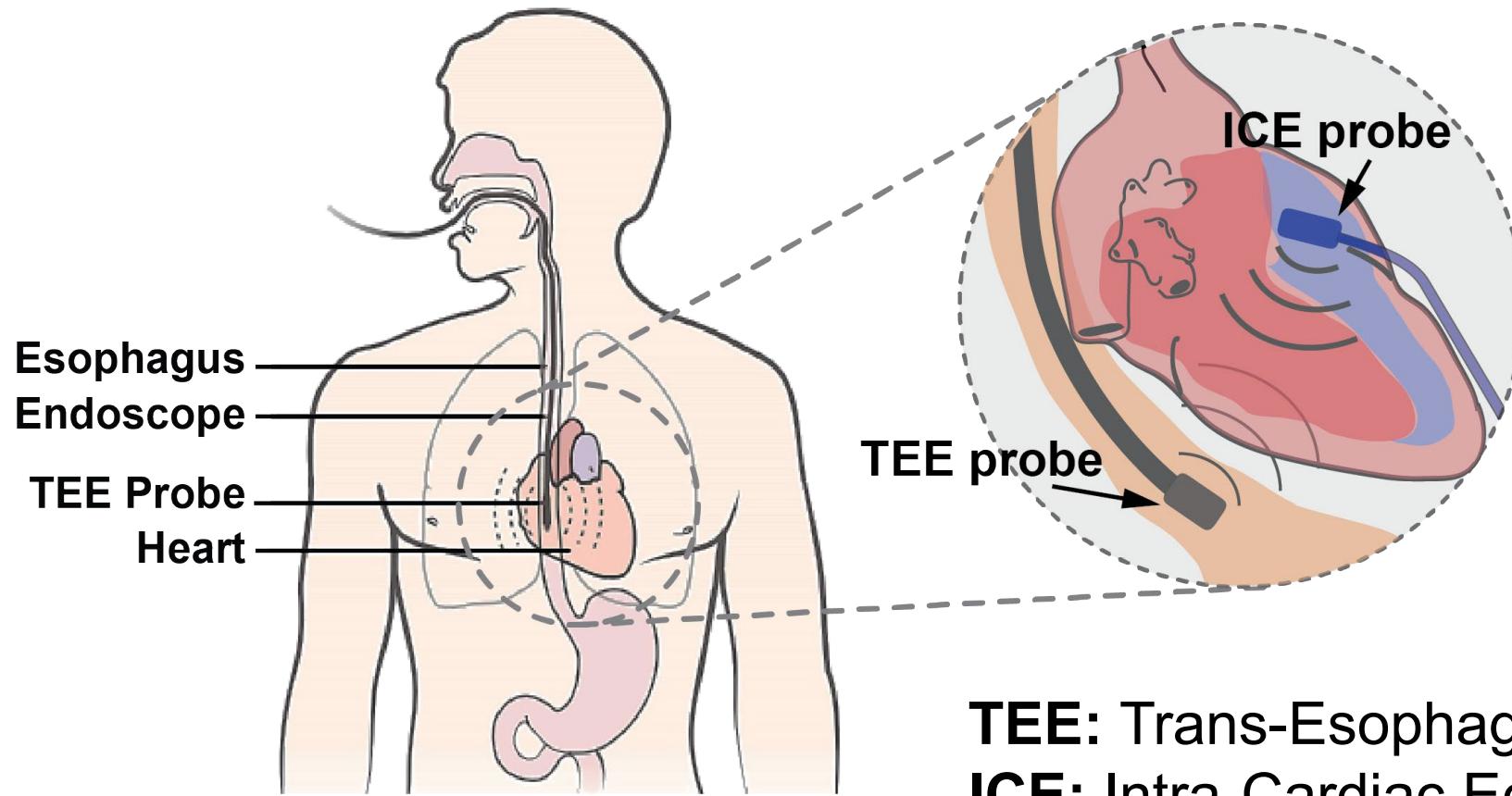
Sources: www.usa.philips.com
www.siemens-healthineers.com

Solution: Electronics into the Probe



- Local amplification \Rightarrow improved SNR
- Local channel-count reduction \Rightarrow enabler for 3D imaging

Use Case: Smart 3D Imaging Catheters



[Chen JSSC'17]

Challenges

- Size
- Interconnect
- Power consumption

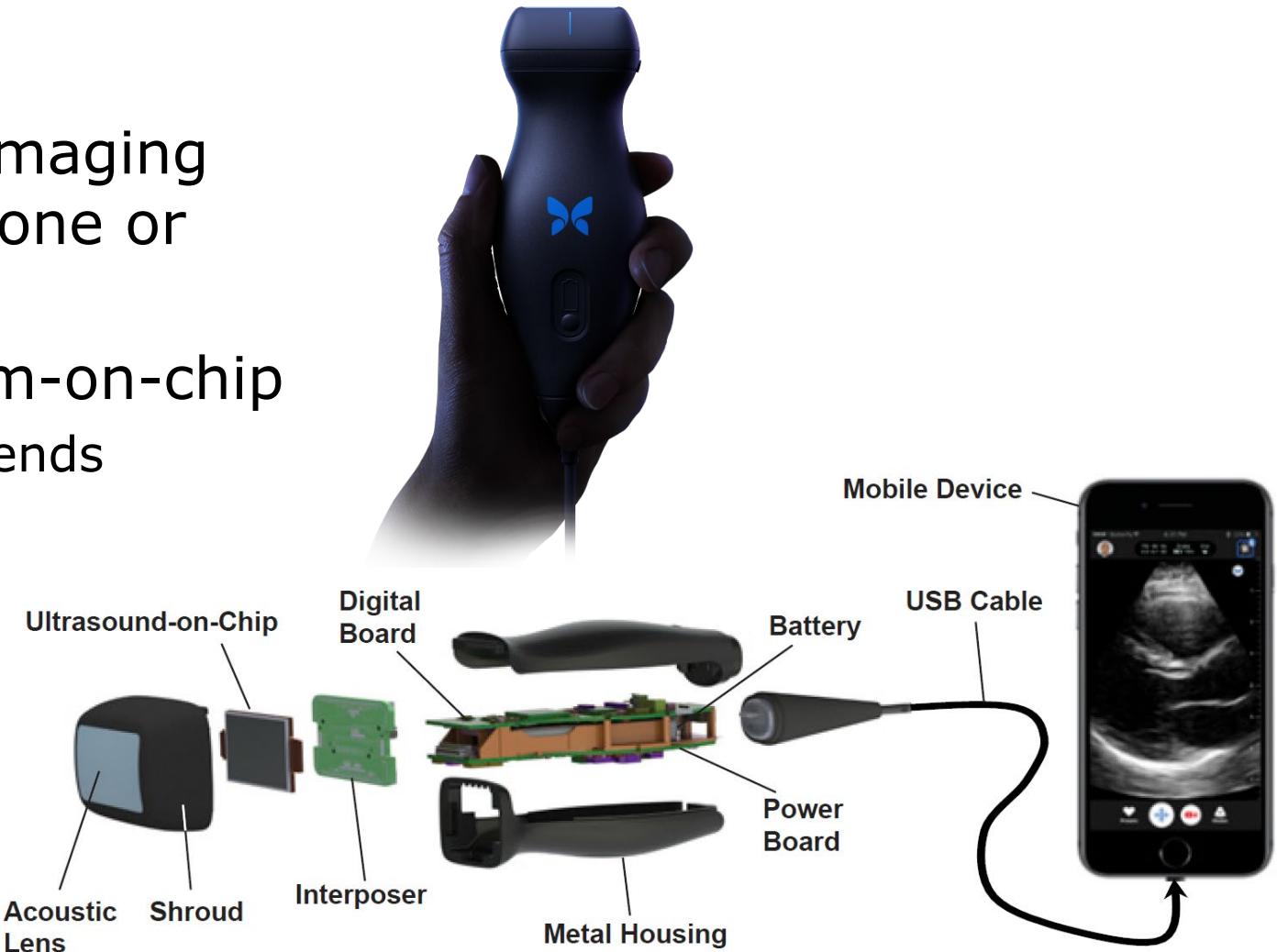
TEE: Trans-Esophageal Echo $\sim 10 \text{ mm } \varnothing$

ICE: Intra-Cardiac Echo $\sim 3 \text{ mm } \varnothing$

IVUS: Intra-Vascular Ultrasound $\sim 1 \text{ mm } \varnothing$

Use Case: Point-of-Care Imaging Devices

- “Ultrasound stethoscope”
- No longer tethered to an imaging system, but to a smart phone or tablet!
- Calls for ultrasound-system-on-chip
 - Pitch-matched TX/RX front-ends
 - Full digitization
 - Data pre-processing

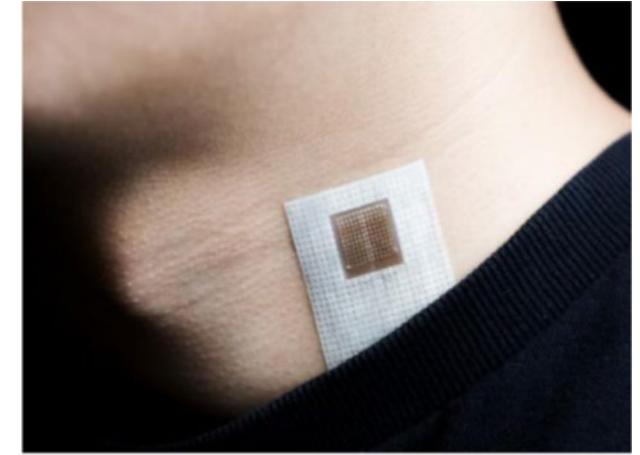


[Rothberg PNAS'21]

ButterflyIQ (www.butterflynetwork.com)

Use Case: Wearable Ultrasound Patches

- Wearable, stretchable, conformal patches for diagnosis and monitoring
- Devices so far employ
 - rigid single-element transducers and discrete electronics, or
 - arrays wired to an imaging system
- True wearability will require co-integrated electronics and wireless data transmission
- Challenges
 - Size (embedded in a patch)
 - Power (from a thin battery)
 - Data rate (suitable for wireless TX)



Univ. of California, San Diego
[Wang Nature BME'21]



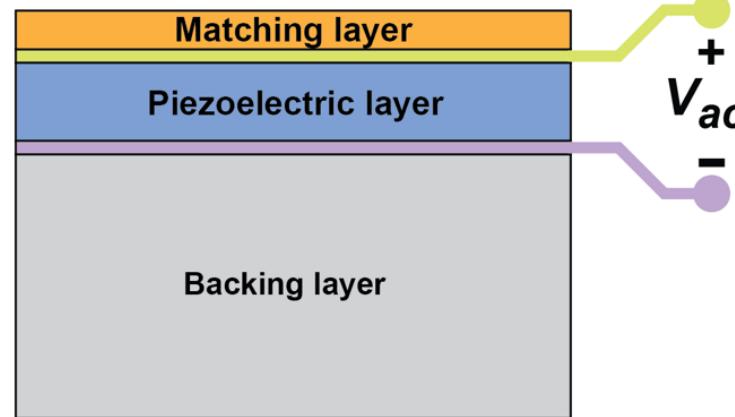
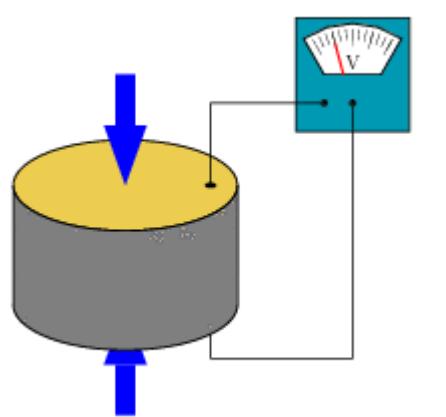
ULIMPIA project
<http://ulimpia-project.eu/>

Outline

- Introduction
- **Transducer-ASIC integration schemes**
- In-probe front-end circuitry
- Channel-count reduction schemes
- Sub-array beamforming
- In-probe digitization
- Conclusions and outlook

Ultrasound Transducers

Bulk piezo-electric transducers

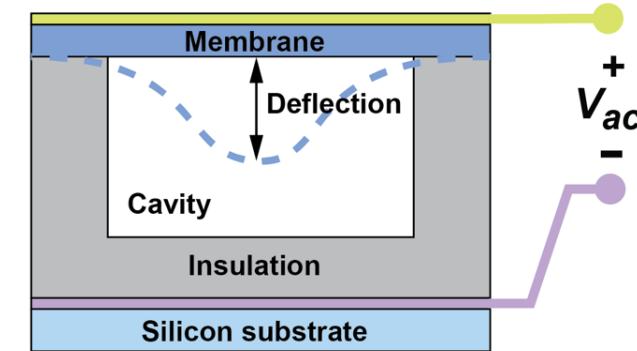


[Safari Springer'08]

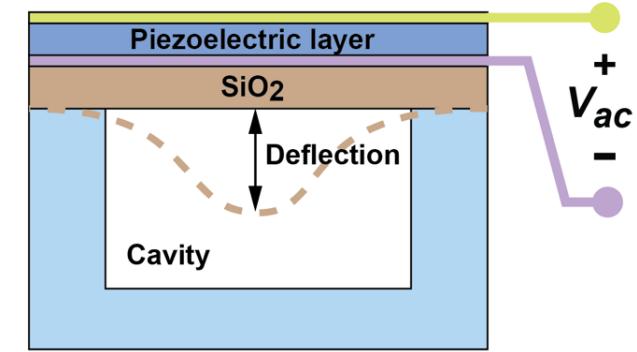
- Bulk piezo still dominant technology
- MEMS offers cost and integration advantages
- All can be integrated with ASICs

MEMS transducers

CMUTs

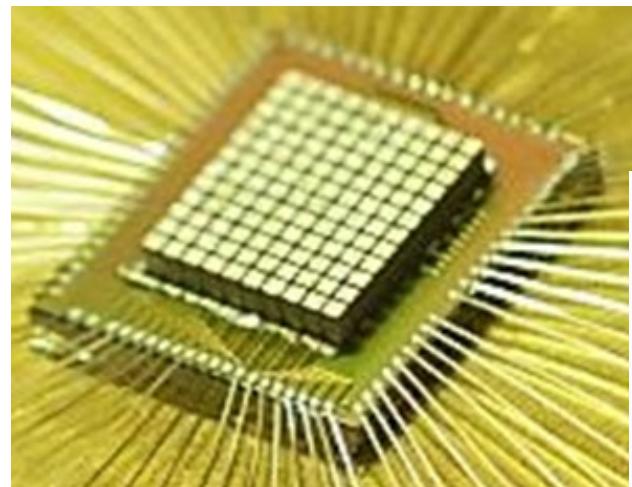


PMUTs

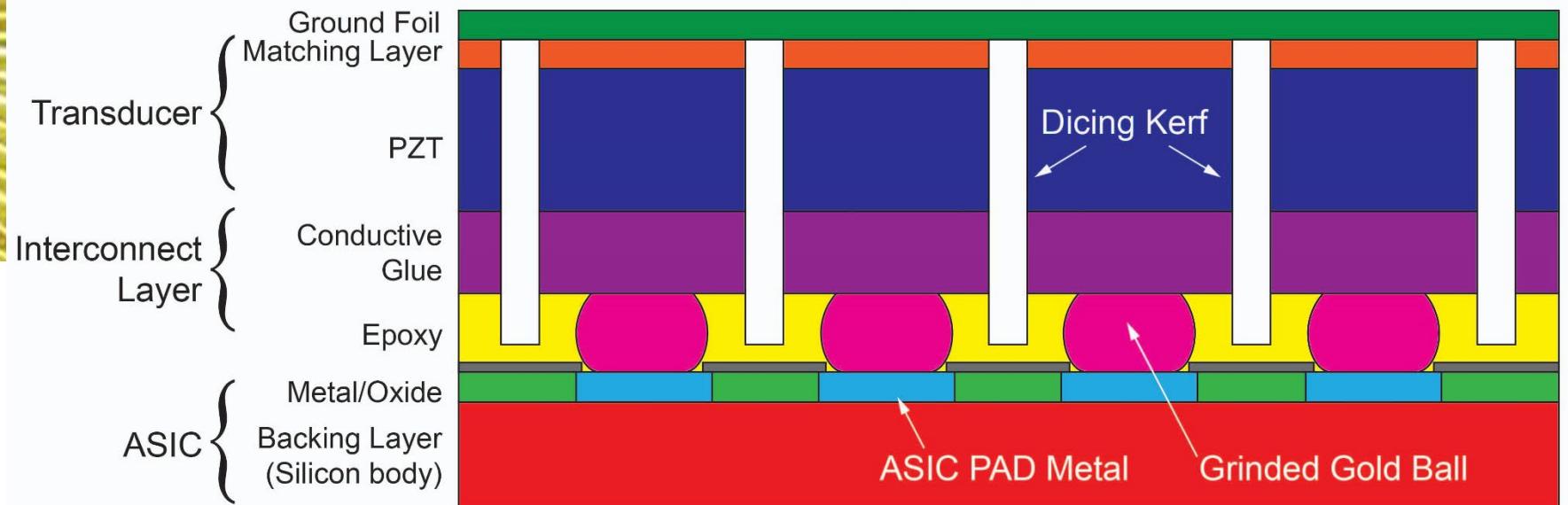
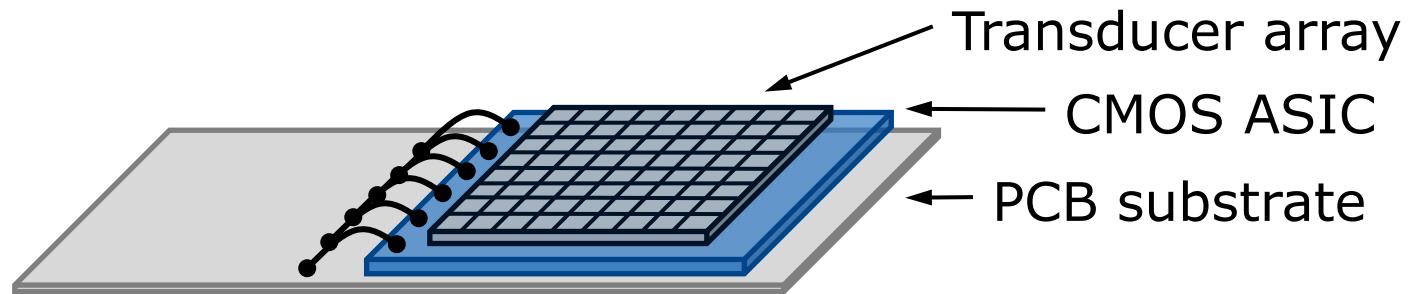


[Brenner MicroMachines'19] [Qiu Sensors'15]

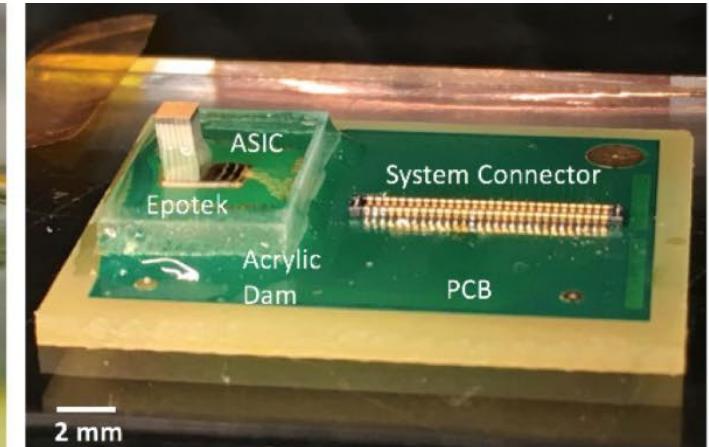
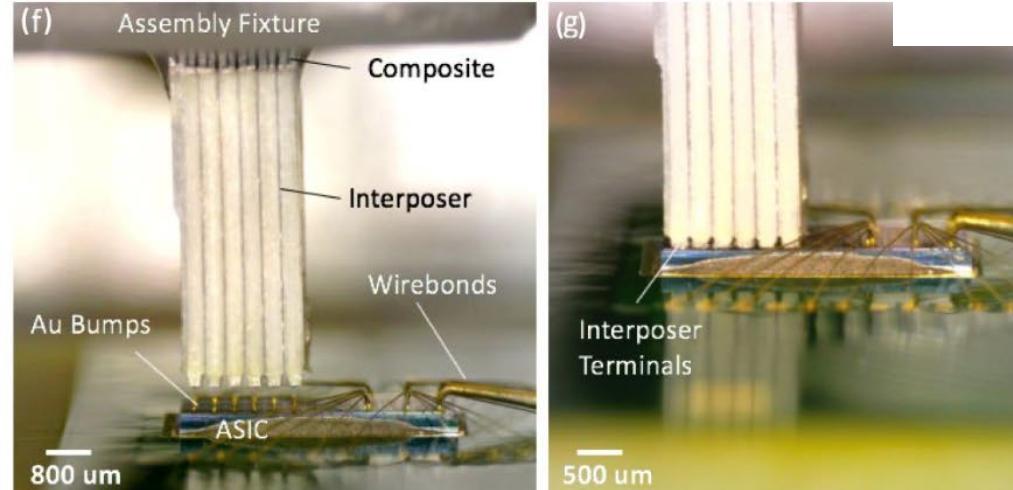
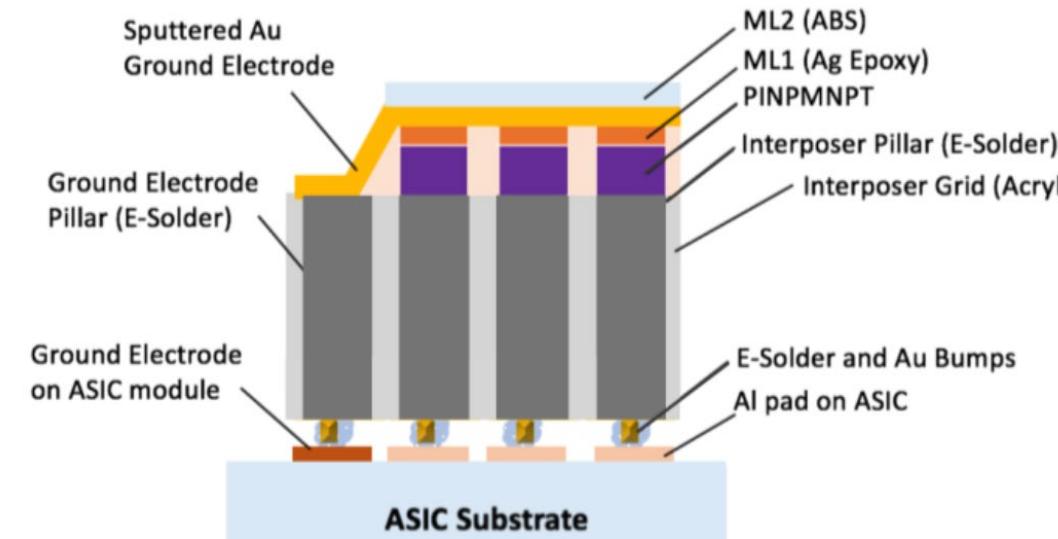
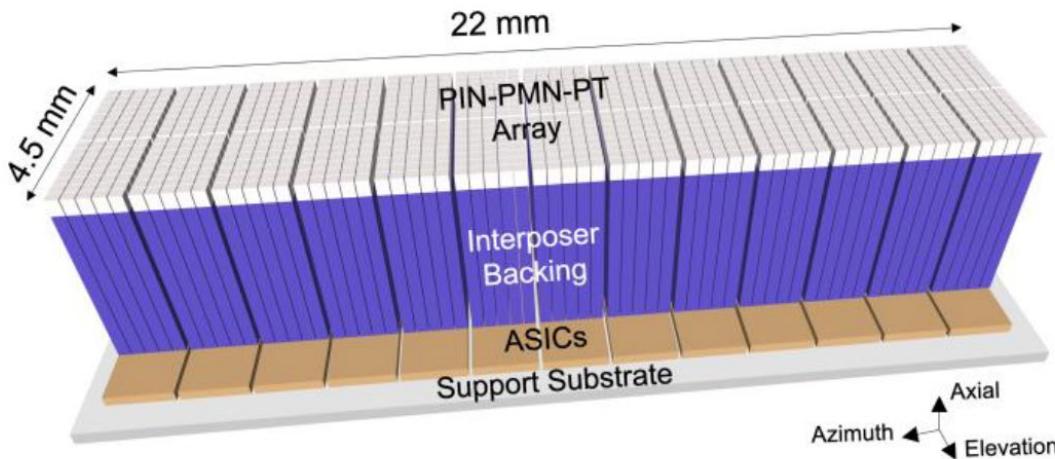
Piezo-on-ASIC Integration



[Chen TUFFC'16]

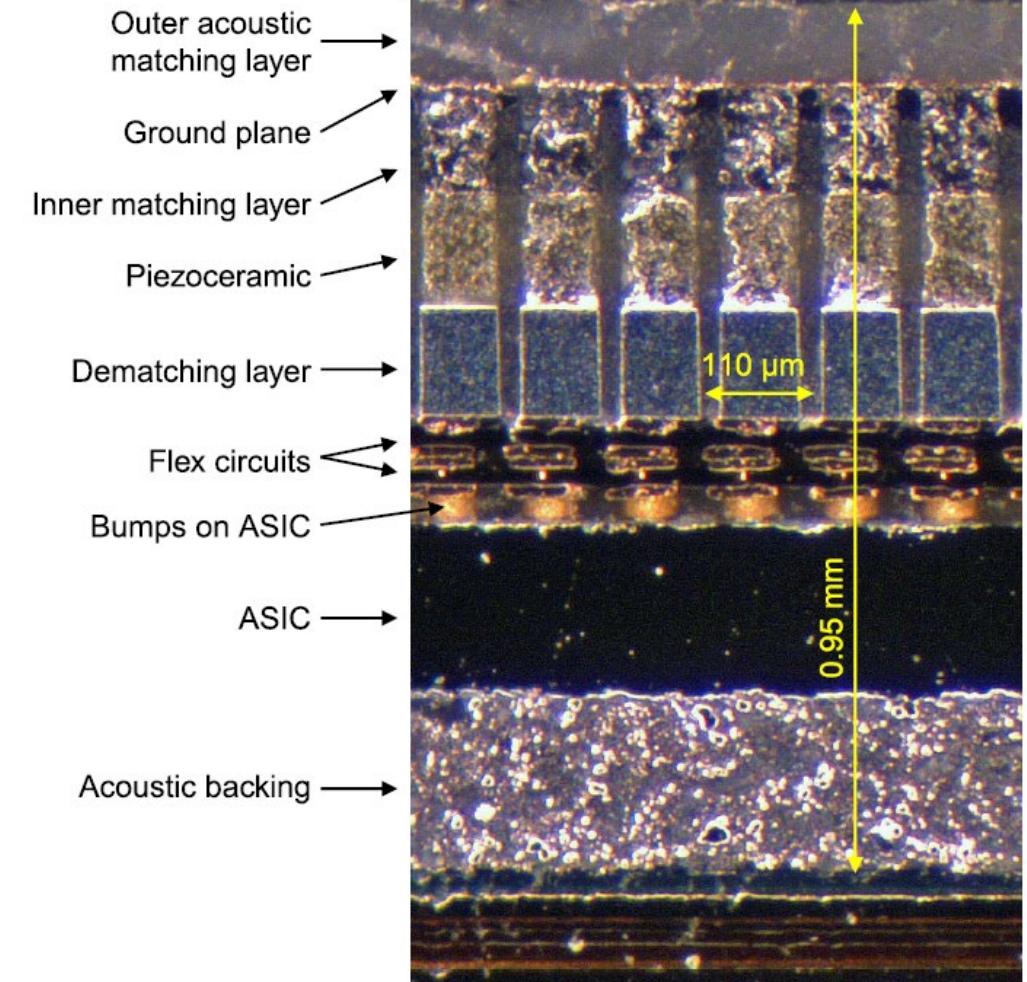
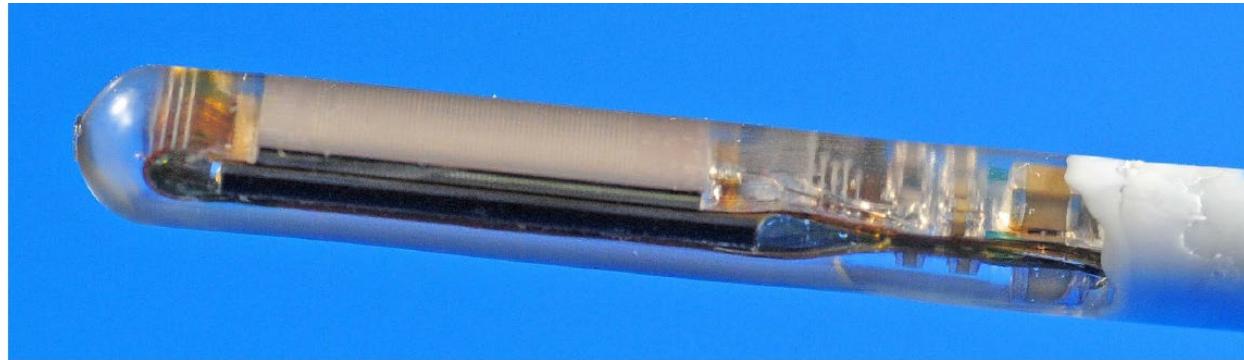
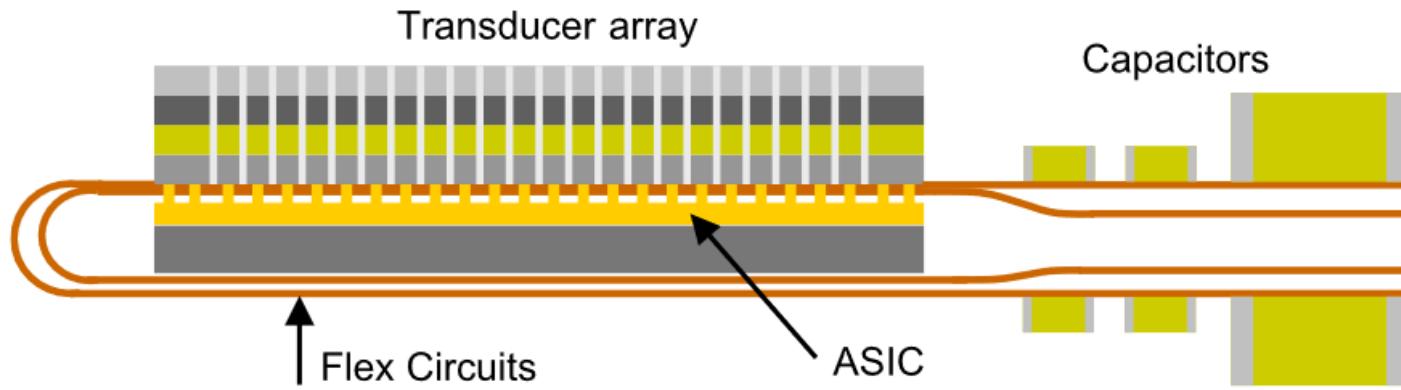


Piezo-on-ASIC Integration with Interposer



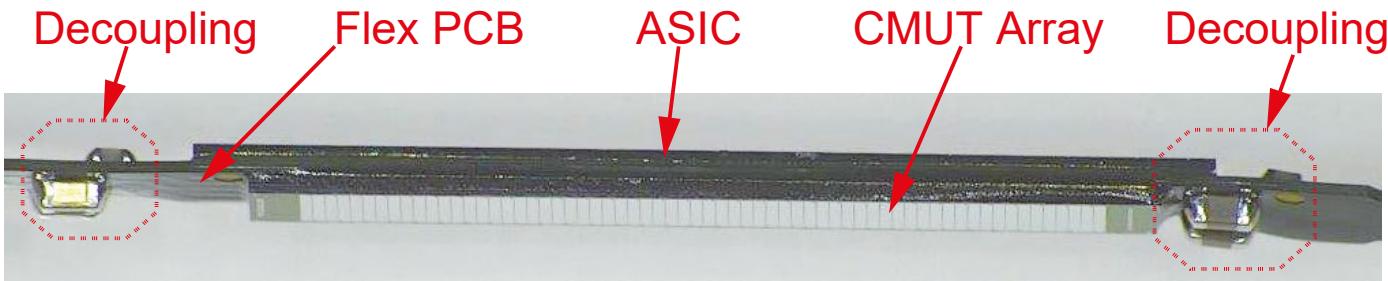
[Wodnicki TUFFC'20,
Kang TUFFC'22]

Piezo-ASIC-Flex Integration



[Wildes TUFFC'16]

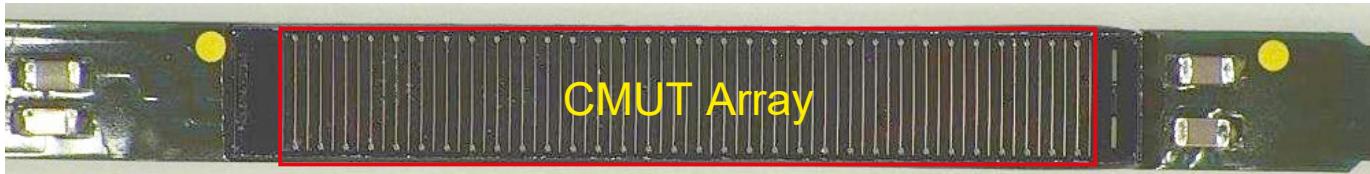
CMUT-ASIC-Flex PCB Integration



Side View



Bottom View

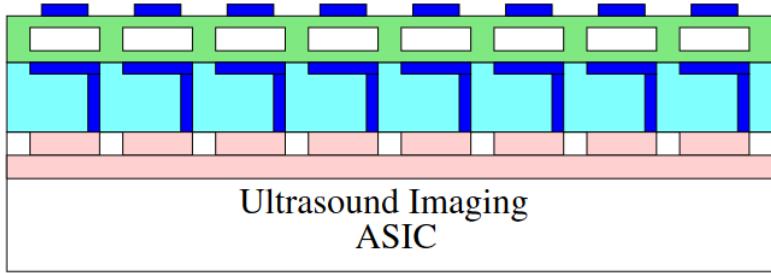


Top View

[Kang JSSC'20]

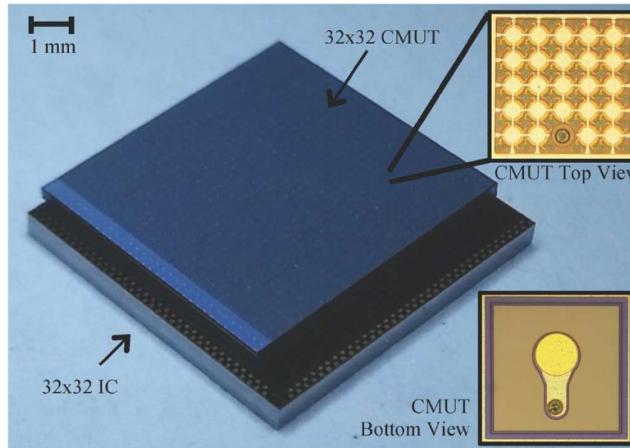
Direct CMUT-ASIC Integration

Monolithic integration

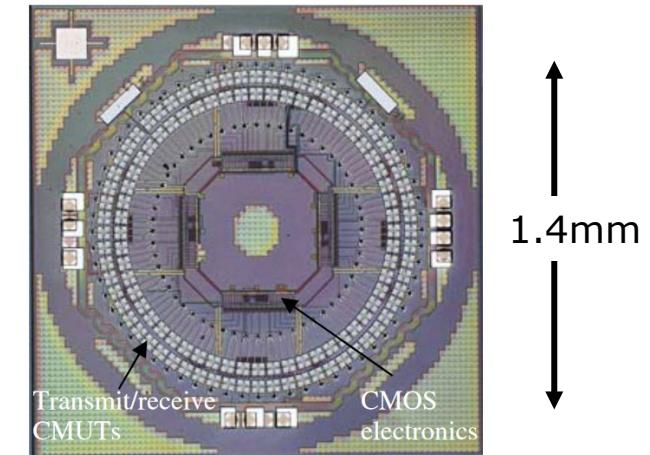


CMUT array
planarization layer

Ultrasound Imaging
ASIC

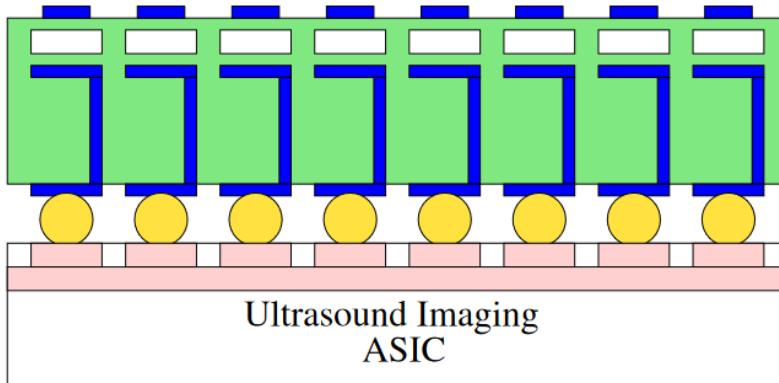


[Bhuyan TBCAS'13]



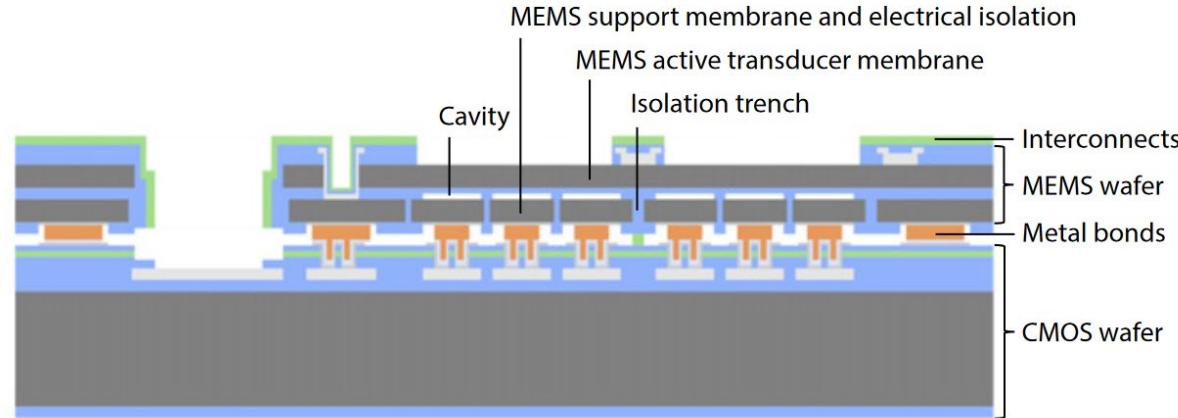
[Degertekin Transducers'17]

Chip-to-chip or wafer-to-wafer bonding



CMUT array
with through-wafer
interconnects
flip-chip bonding

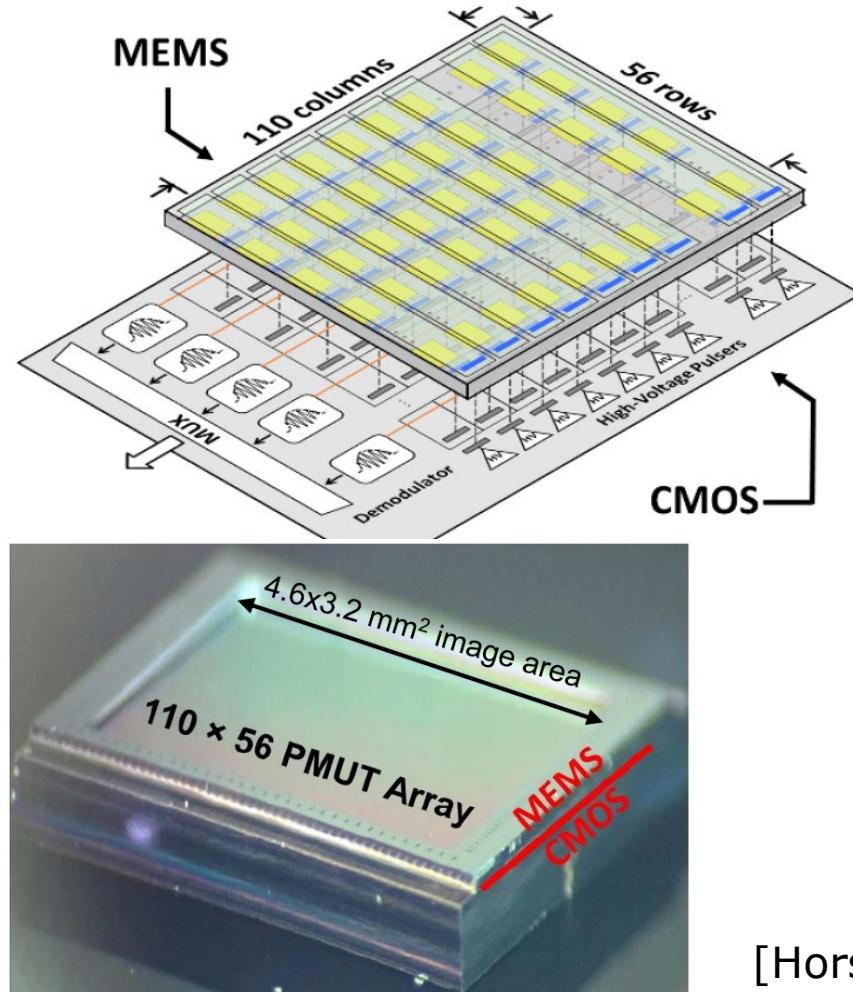
Ultrasound Imaging
ASIC



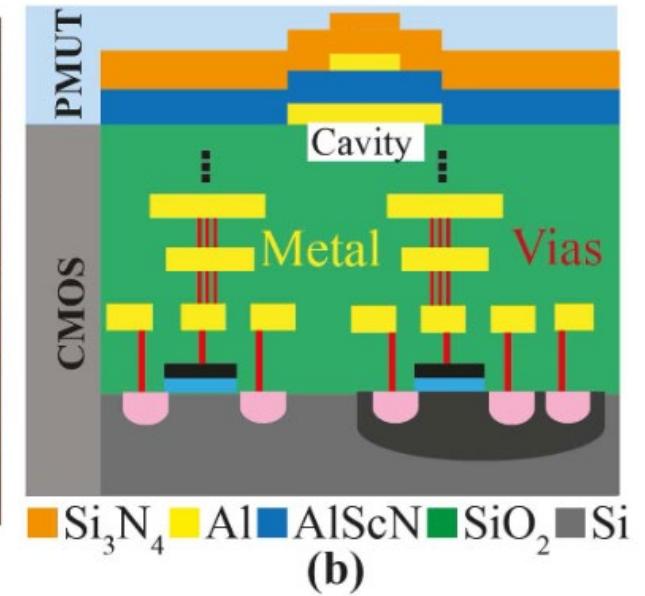
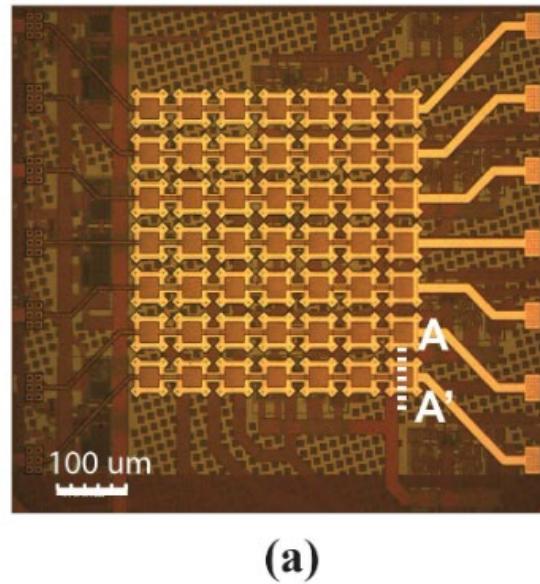
[Brenner MicroMachines'19]

Butterfly [Rothberg PNAS'21]

Direct PMUT-ASIC Integration



[Horsley IUS'16]



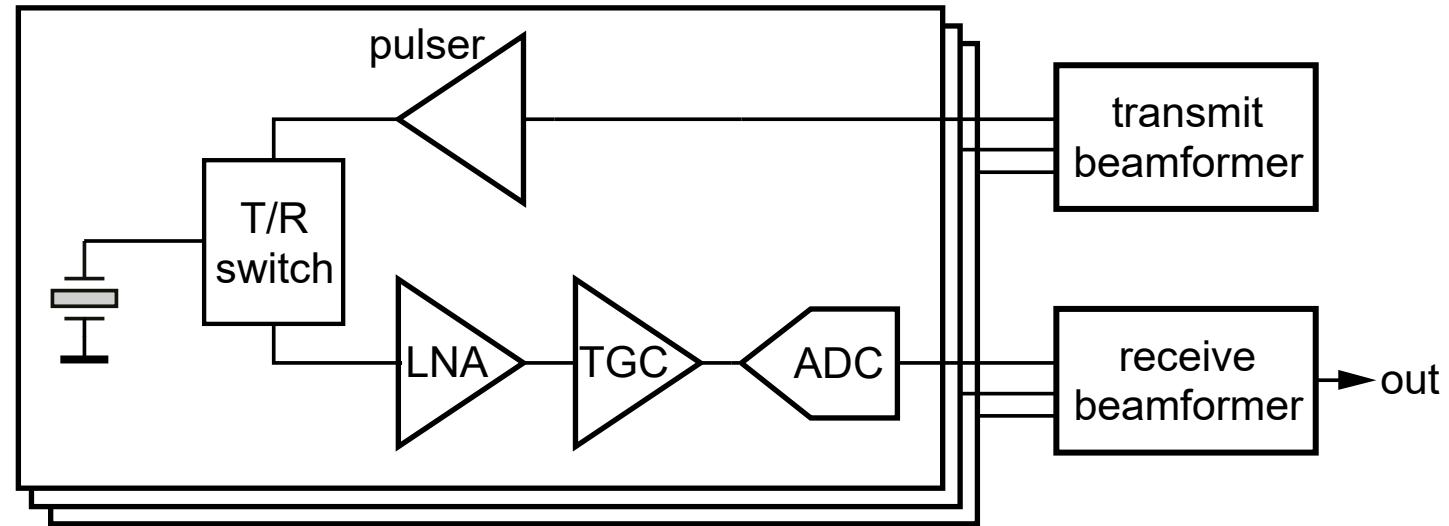
SilTerra [Zamora EDL'22]

Outline

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- **In-probe front-end circuitry**
- Channel-count reduction schemes
- Sub-array beamforming
- In-probe digitization
- Conclusions and outlook

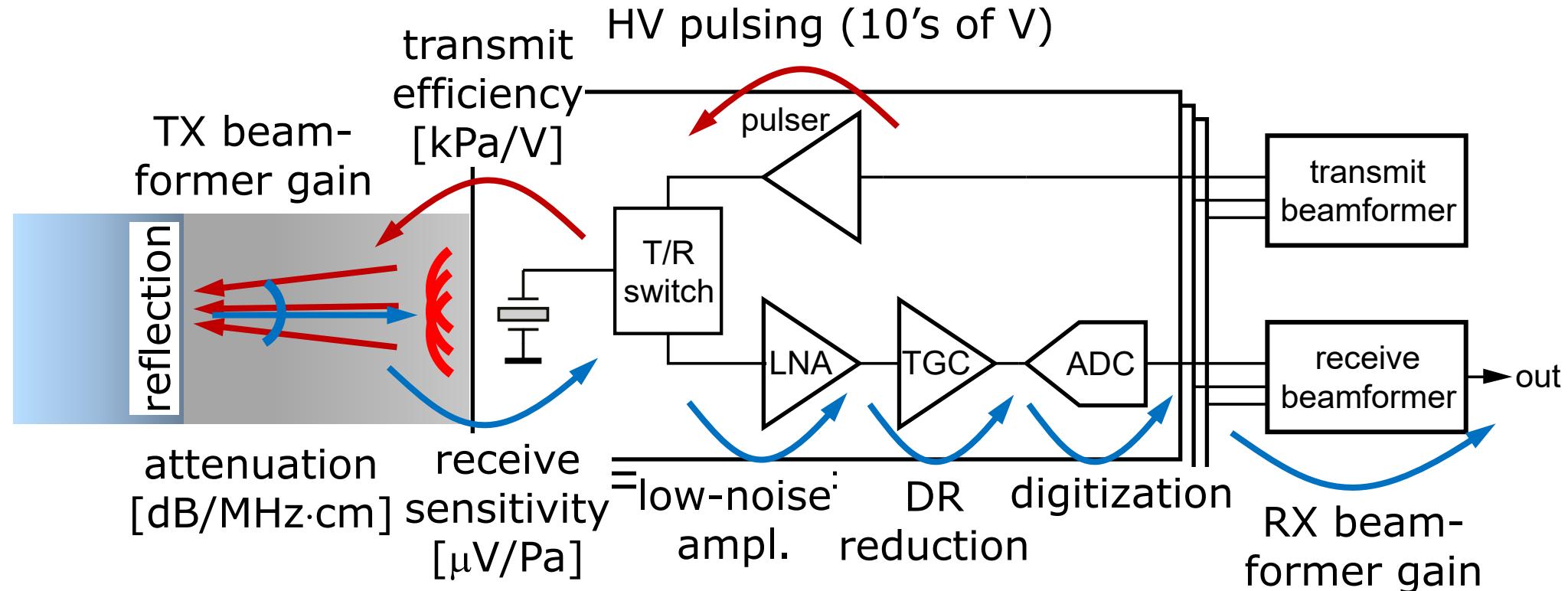
Ultrasound Front-End Circuits

Electrical domain

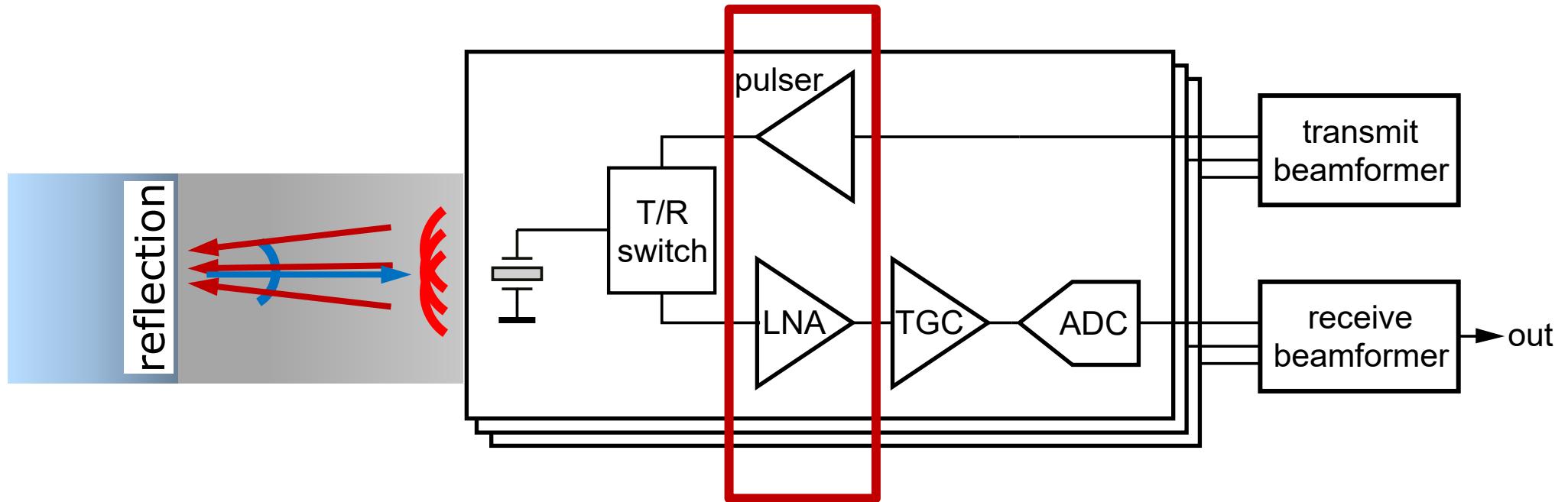


- Overall goal: achieve sufficient SNR_{out} at minimal power
- Signal: echo amplitude
- Noise: acoustic noise, transducer noise, electronics noise (thermal, quantization)
- Complex system optimization!

Ultrasound Front-End Circuits

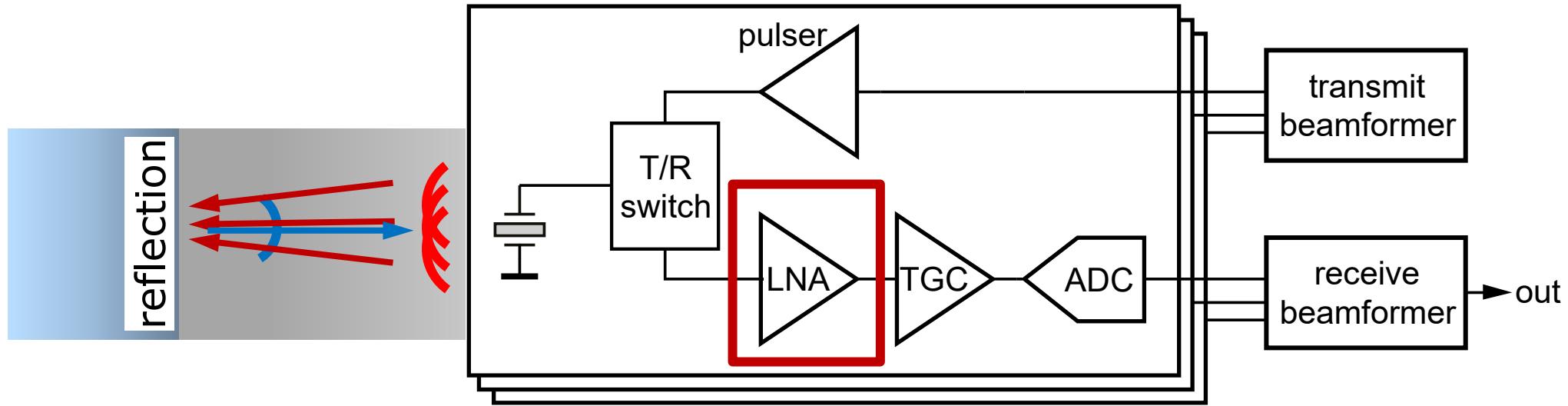


Ultrasound Front-End Circuits



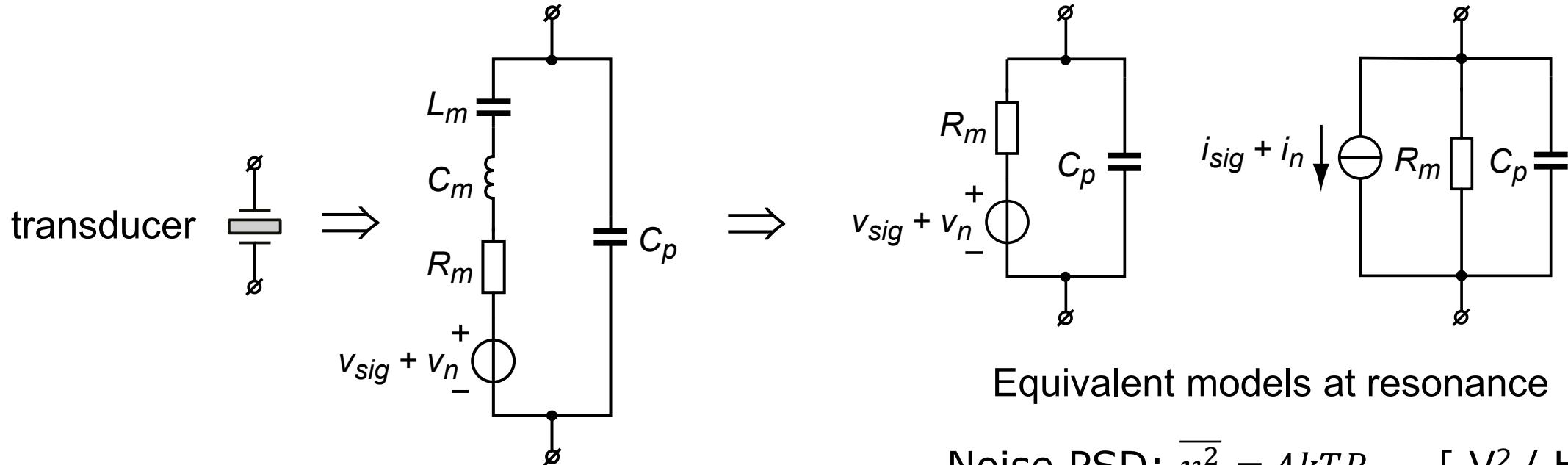
tend to dominate
power consumption
and limit performance

Low-noise amplifiers – requirements



- **Good noise figure:** noise < transducer noise (and uncorrelated between channels!)
- Sufficient **bandwidth:** > transducer bandwidth
- Sufficient **dynamic range:** handle nearby echoes ($\sim V$) up to deep echoes ($\sim \mu V$)
 - Programmable gain, built-in TGC can help
- Price to pay: **power!**

Butterworth-Van Dyke model



Butterworth-Van Dyke
model

$$f_{res} = 1/2\pi\sqrt{L_m C_m}$$

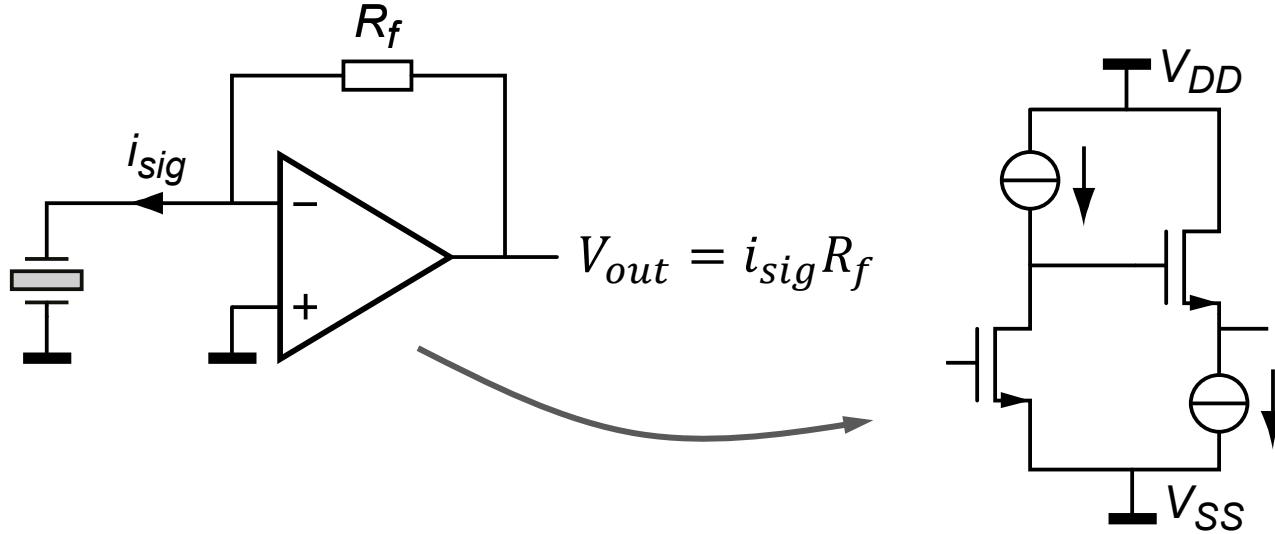
Equivalent models at resonance

$$\text{Noise PSD: } \overline{v_n^2} = 4kT R_m \quad [\text{V}^2 / \text{Hz}]$$

$$\overline{i_n^2} = 4kT/R_m \quad [\text{A}^2 / \text{Hz}]$$

Models work for bulk piezo, CMUTs, PMUTs
(with different model parameters)

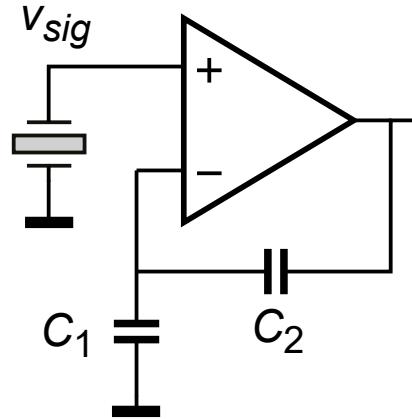
LNA - transimpedance amplifiers



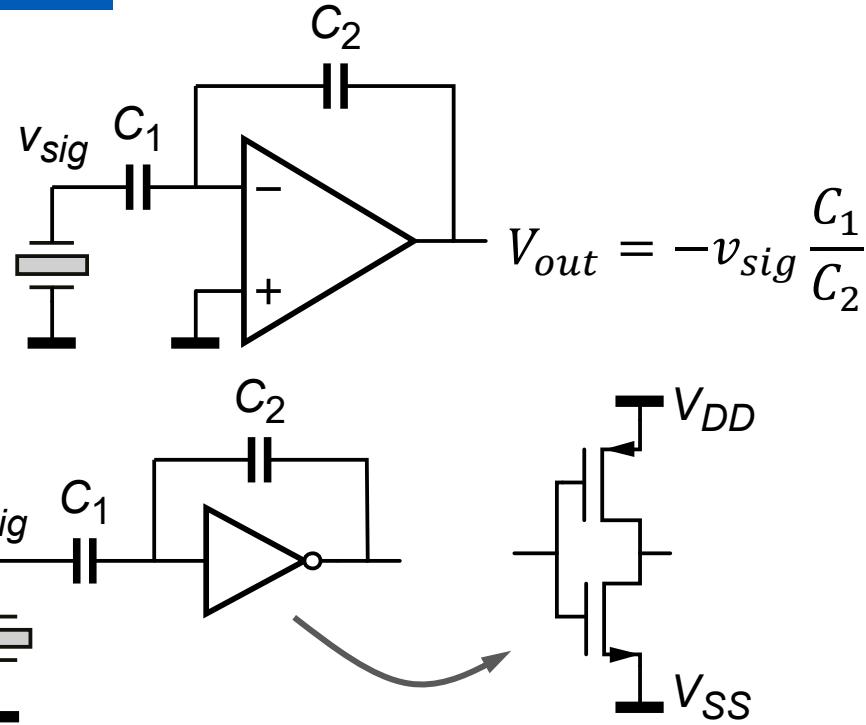
[Wygant TUFFC'09]
[Chen JSSC'13]
[Sautto ESSCIRC'14]

- Senses motional current (i_{sig}) of the transducer
- Power-efficient for relatively high-impedance transducers (e.g. CMUTs)

LNA - voltage amplifiers



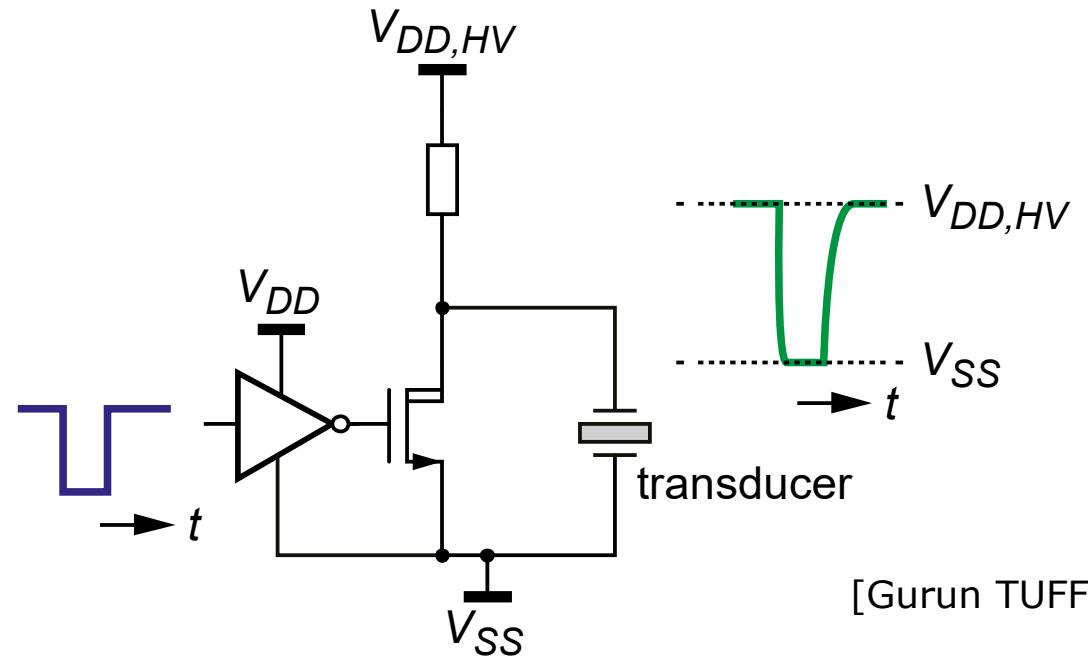
$$V_{out} = v_{sig} \frac{C_1 + C_2}{C_2}$$



- Senses voltage across the transducer
- Power-efficient for relatively low-impedance transducers (e.g. bulk PZT)

Transmit circuits – pulsers

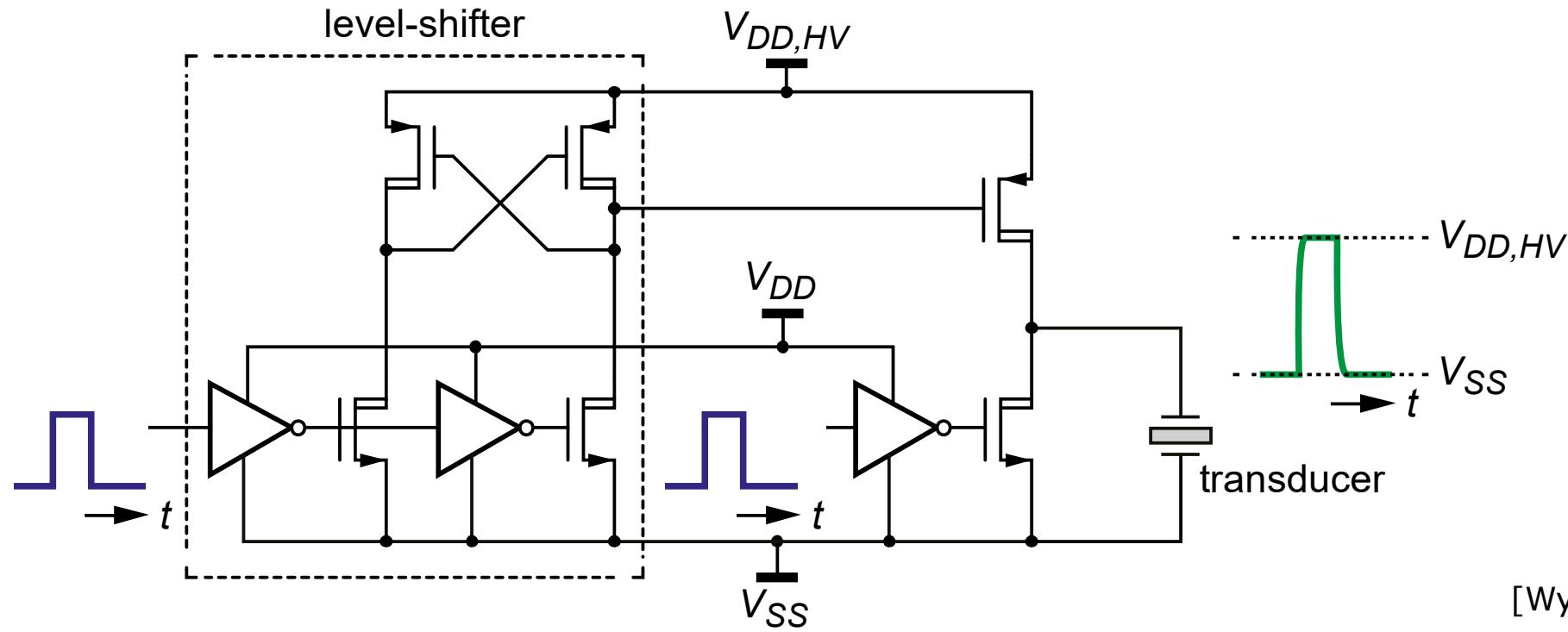
- Pulse voltage typically tens of V
⇒ need HV CMOS process
- Excite transducer at resonance
⇒ pulse width $t_{pulse} = 1/2f_{res}$
- Often sequence of multiple pulses at f_{res}
 - more pulses ⇒ better SNR but poorer axial resolution



[Gurun TUFFC'14]

- Resistive pull-up is simple and compact, but power hungry

Transmit circuits – push-pull topology

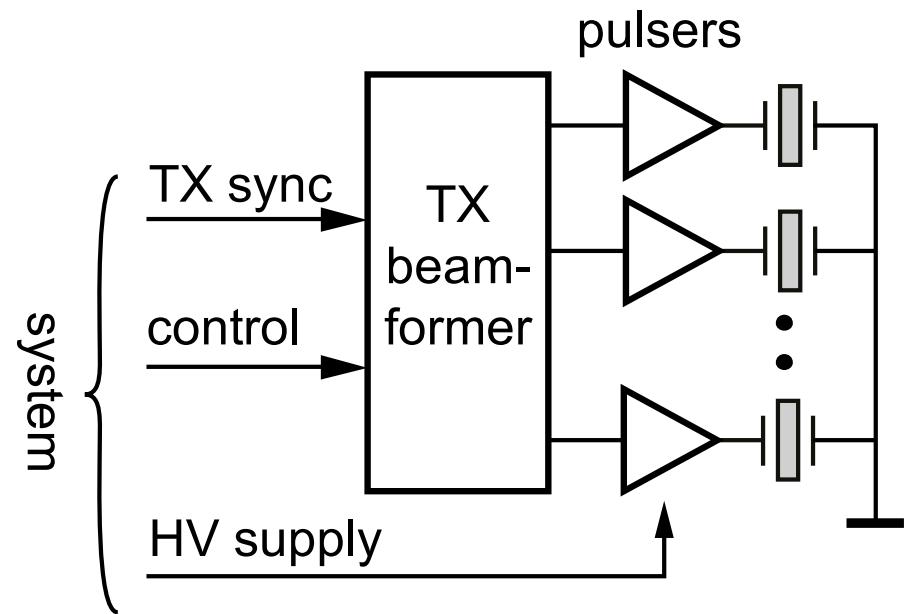


[Wygant TUFFC'08]

- More efficient, but tends to require HV level-shifters
- Power limited by (dis)charging of transducer capacitance: $f_{PRF}CV^2$ [Tang TBioCAS'15]
- More efficient but also more complex: bipolar pulsers, multi-level pulsers

In-Probe Transmit Beamformers

- Determine pulse timing using on-chip logic
 - Programmable counters
 - Programmable delay lines
 - Synchronized to a master clock that defines the timing resolution
- Moves transmit functionality fully into the probe, system provides configuration and trigger/sync
- Delay profile can be calculated on chip, or programmed into the chip
 - Often via a serial interface
 - Delay programming takes time
 - In-probe memory can help to quickly switch between beam profiles



[Bhuyan ISSCC'13,
KChen JSSC'16, Katsume ISSCC'17]

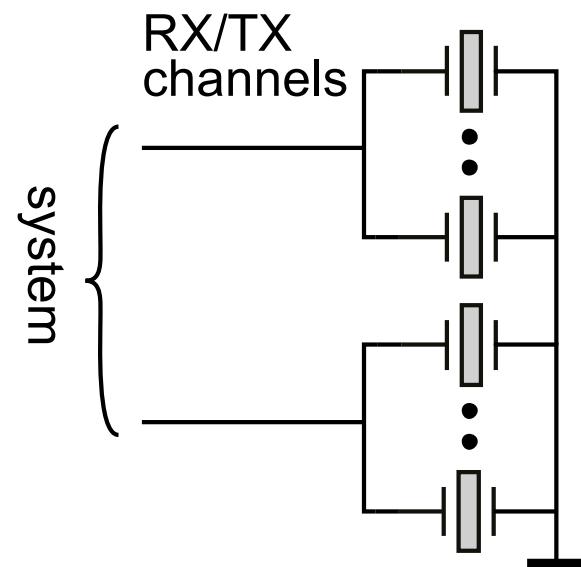
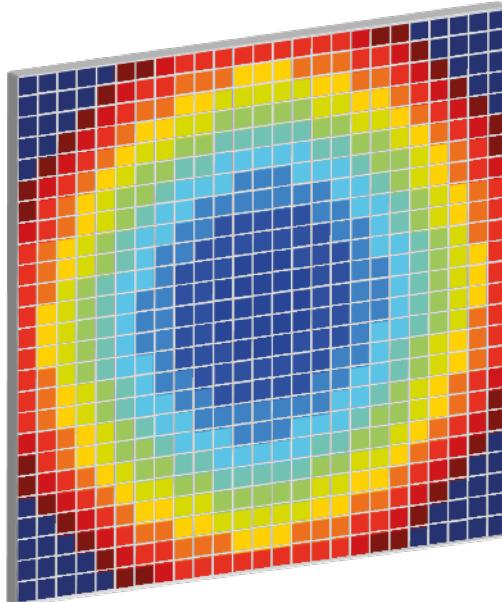
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Approaches to Channel-Count Reduction

□ Iso-phase element grouping

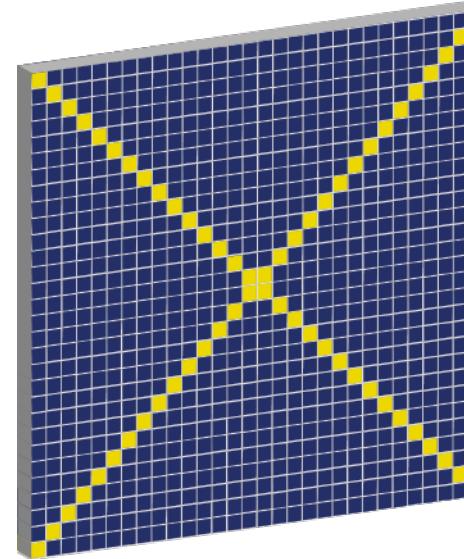
- Can be made reconfigurable using in-probe switches



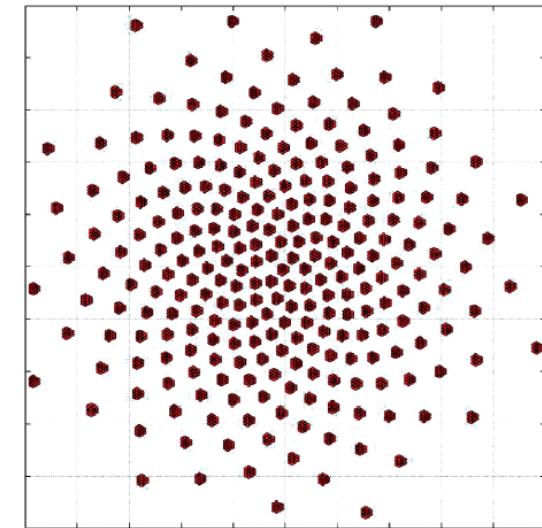
[Savord IUS'03, Tamano IUS'04, Fisher IUS'05]

□ Sparse arrays

- Receive on diagonals
- Spiral array patterns



[Wygant TUFFC'09]

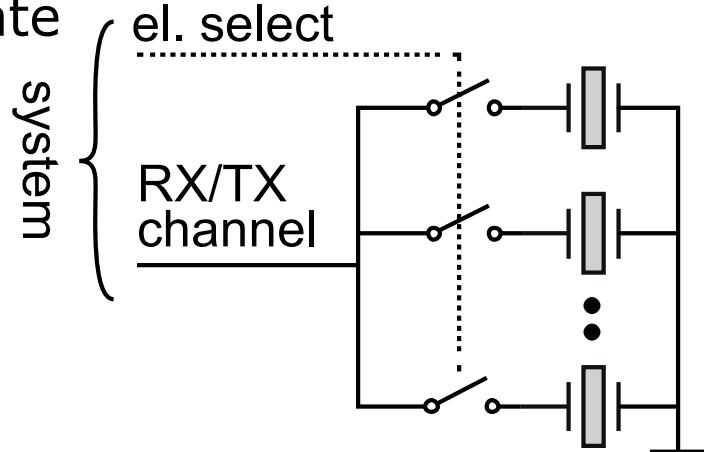
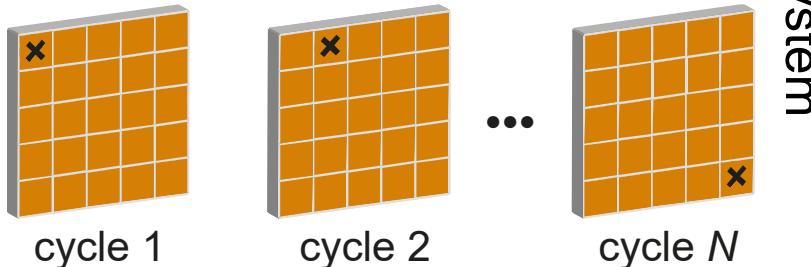


[Ramalli TUFFC'15]

Approaches to Channel-Count Reduction

□ Multiplexing

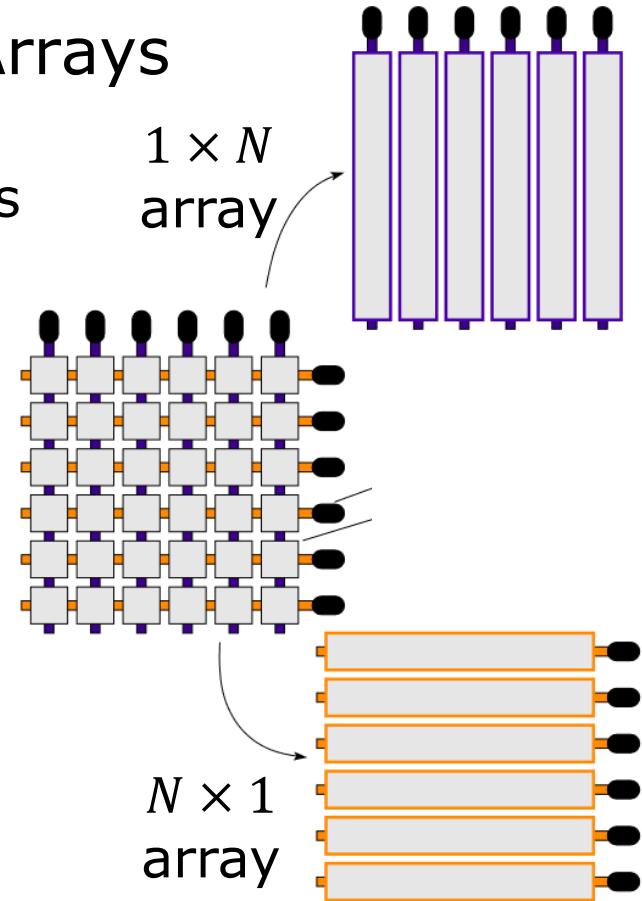
- Employ in-probe switches to connect N elements to one system channel
- “synthetic aperture” acquisition
- Reduces frame rate



[Kim IUS'12, KChen JSSC'16, Carpenter TUFFC'16,
Rezvanitabar TBCAS'22]

□ Row/Column Arrays

- $N \times N$ array
 $\rightarrow 2N$ channels

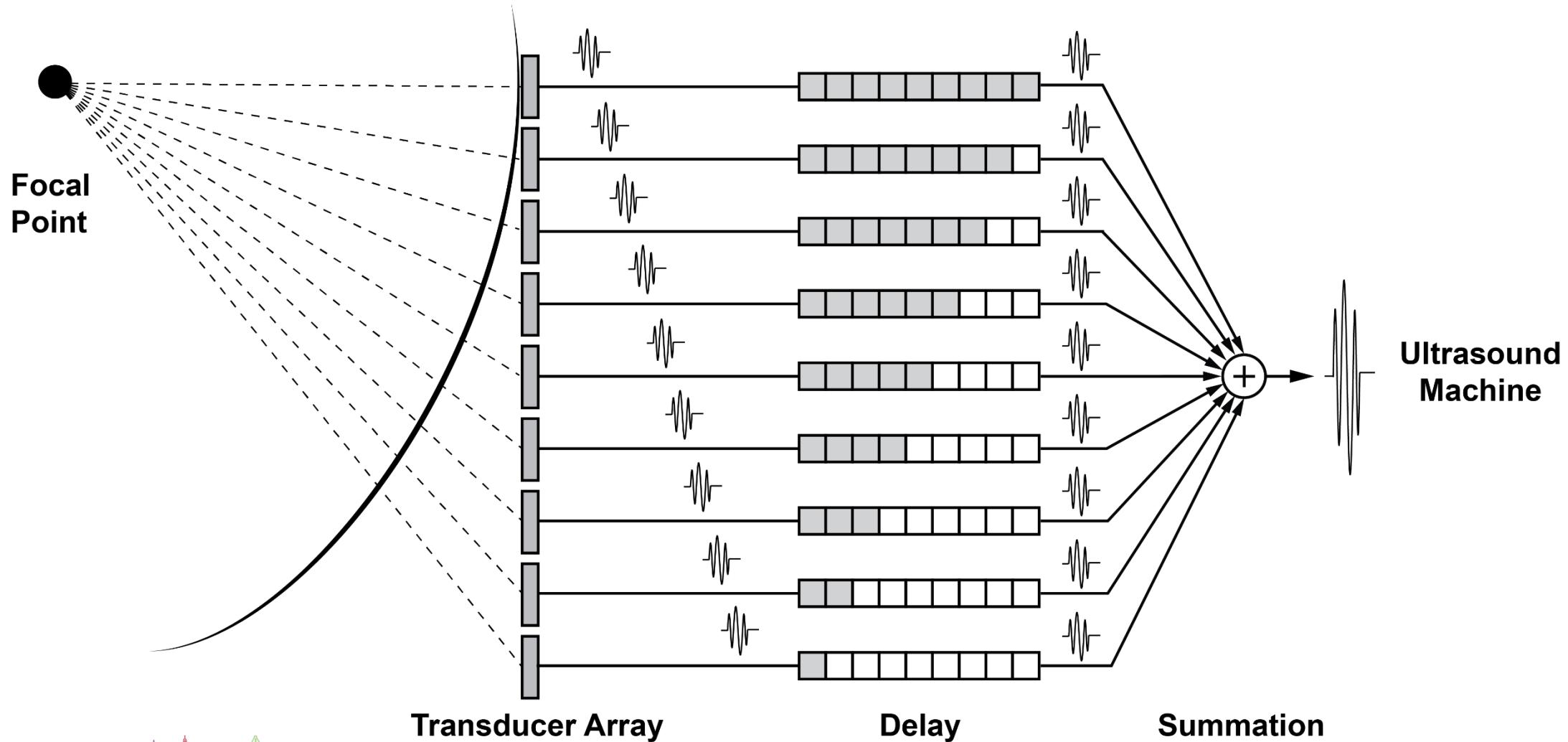


[Jensen TUFFC'22]

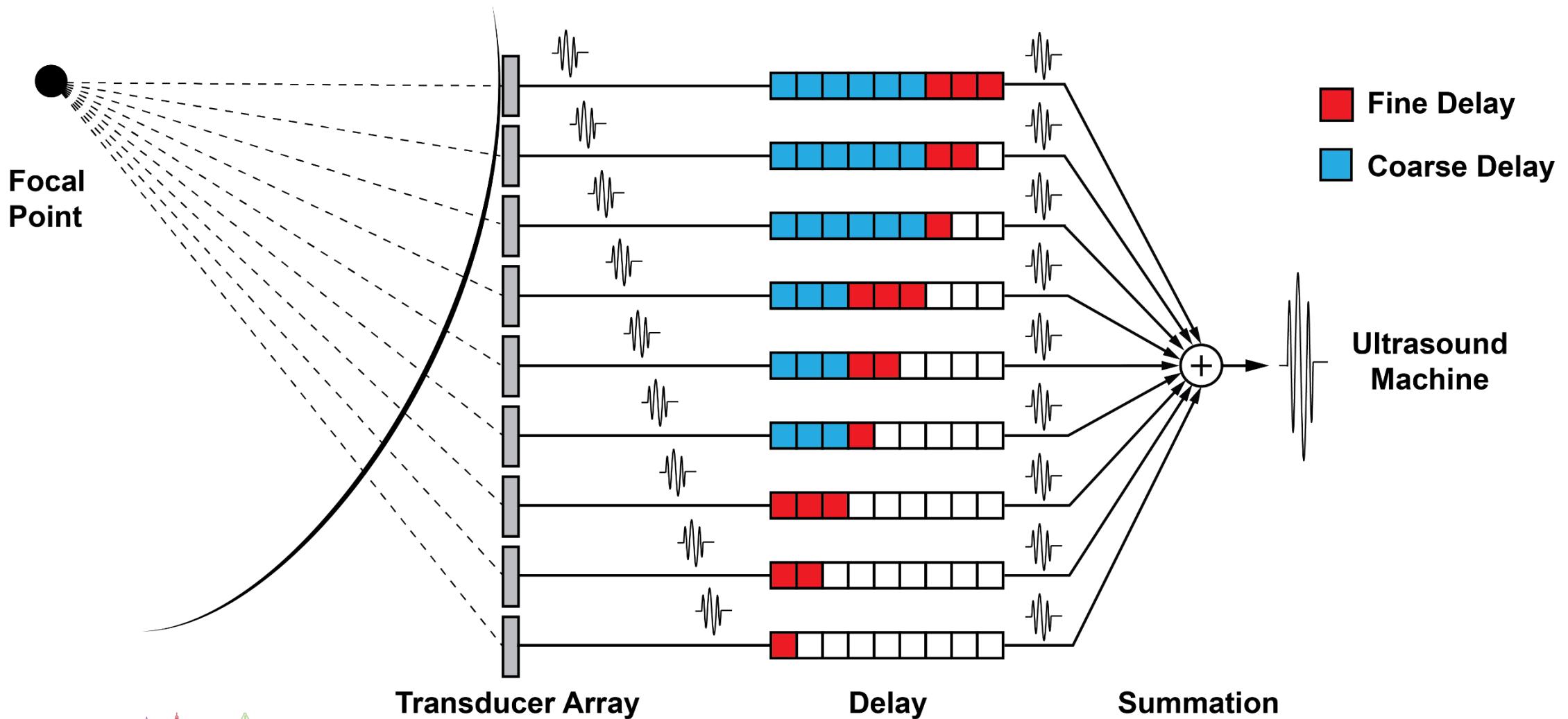
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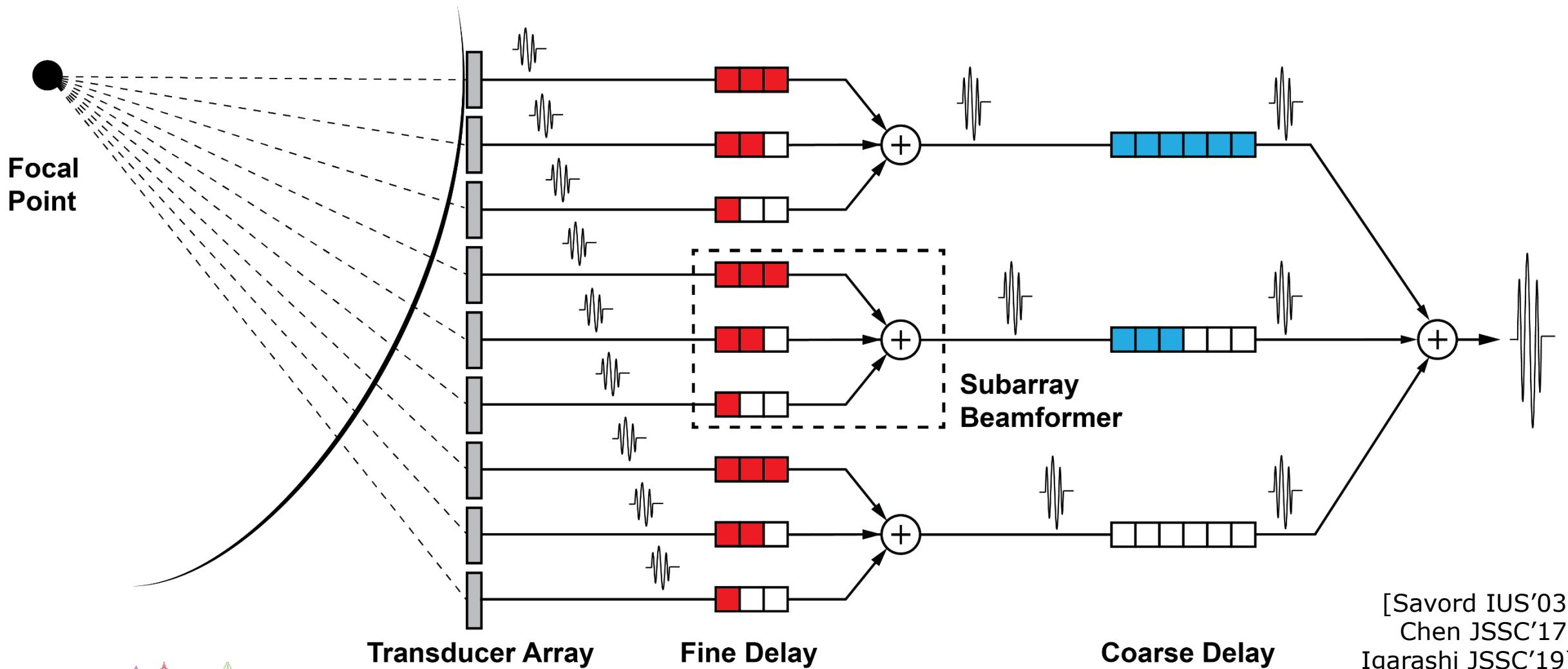
Sub-array Beamforming



Sub-array Beamforming

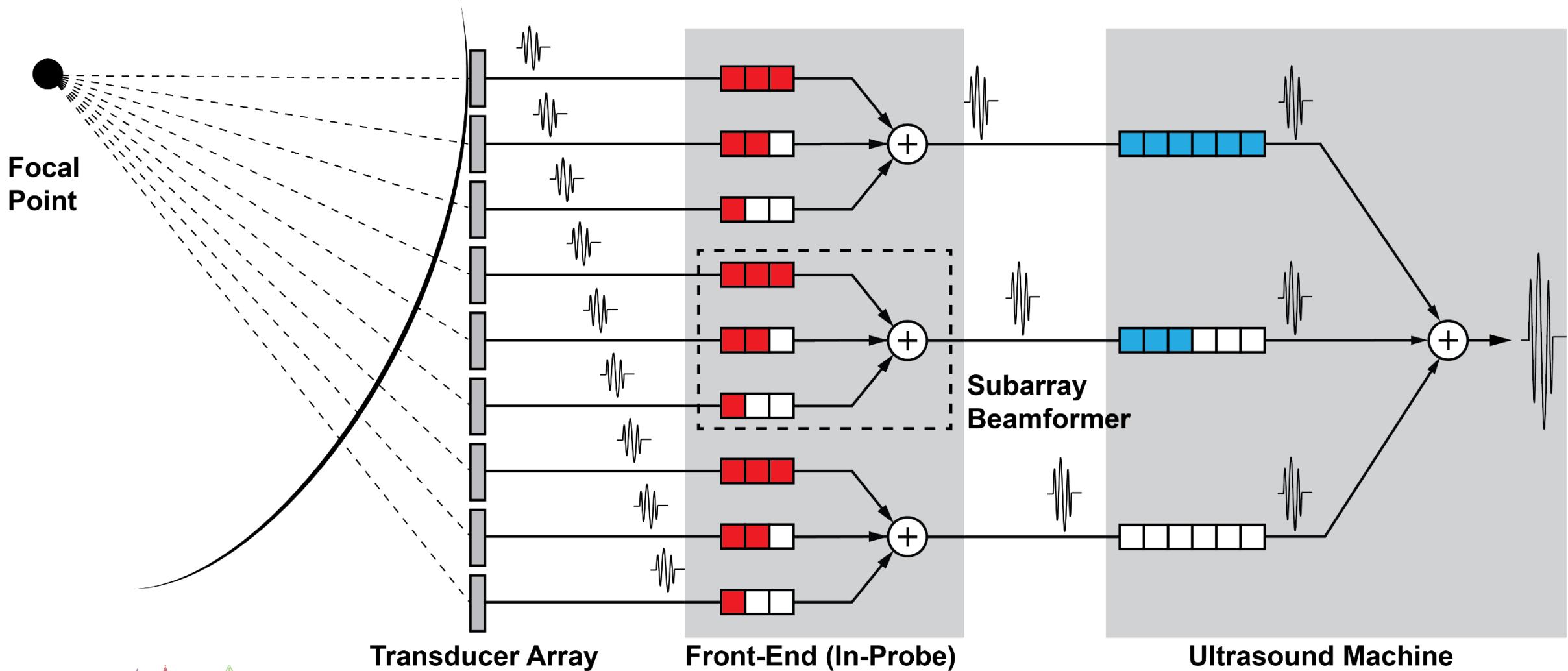


Sub-array Beamforming

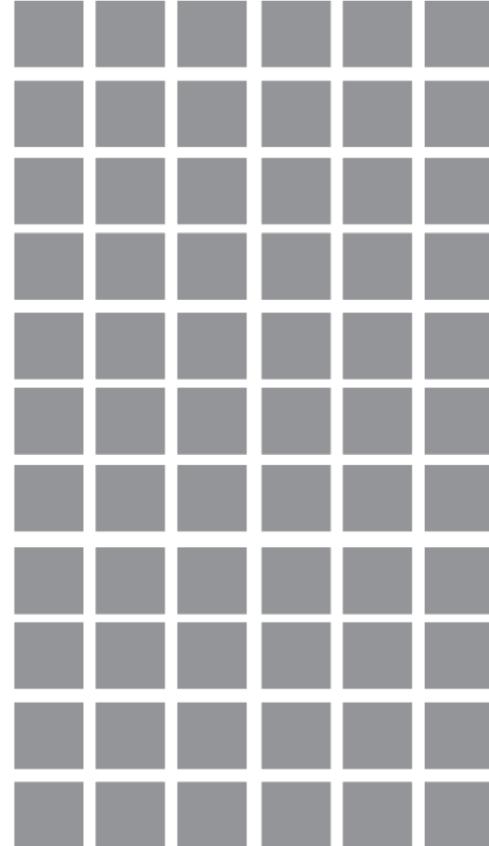


[Savord IUS'03,
Chen JSSC'17,
Igarashi JSSC'19]

Sub-array Beamforming

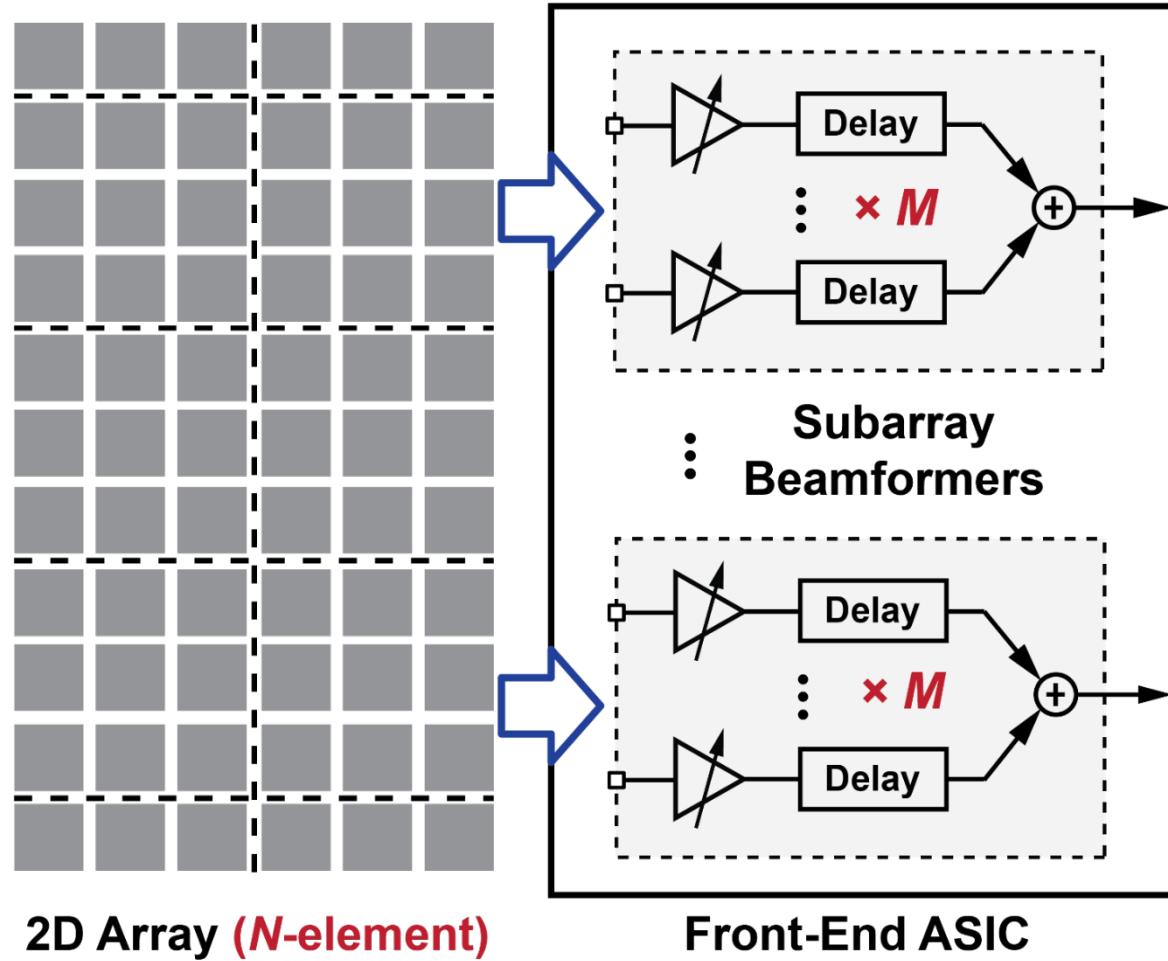


Sub-array Beamforming on a 2D Array

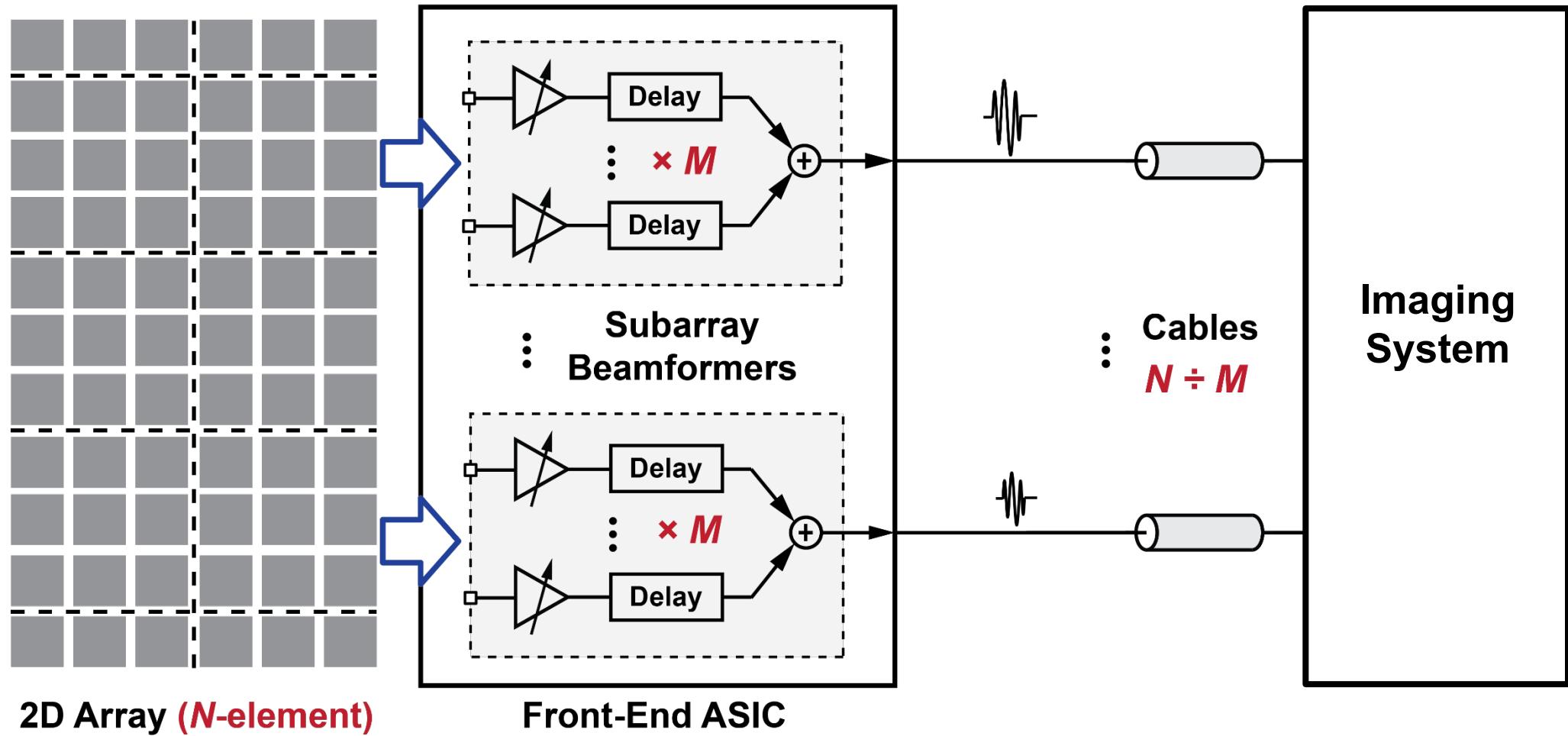


2D Array (N -element)

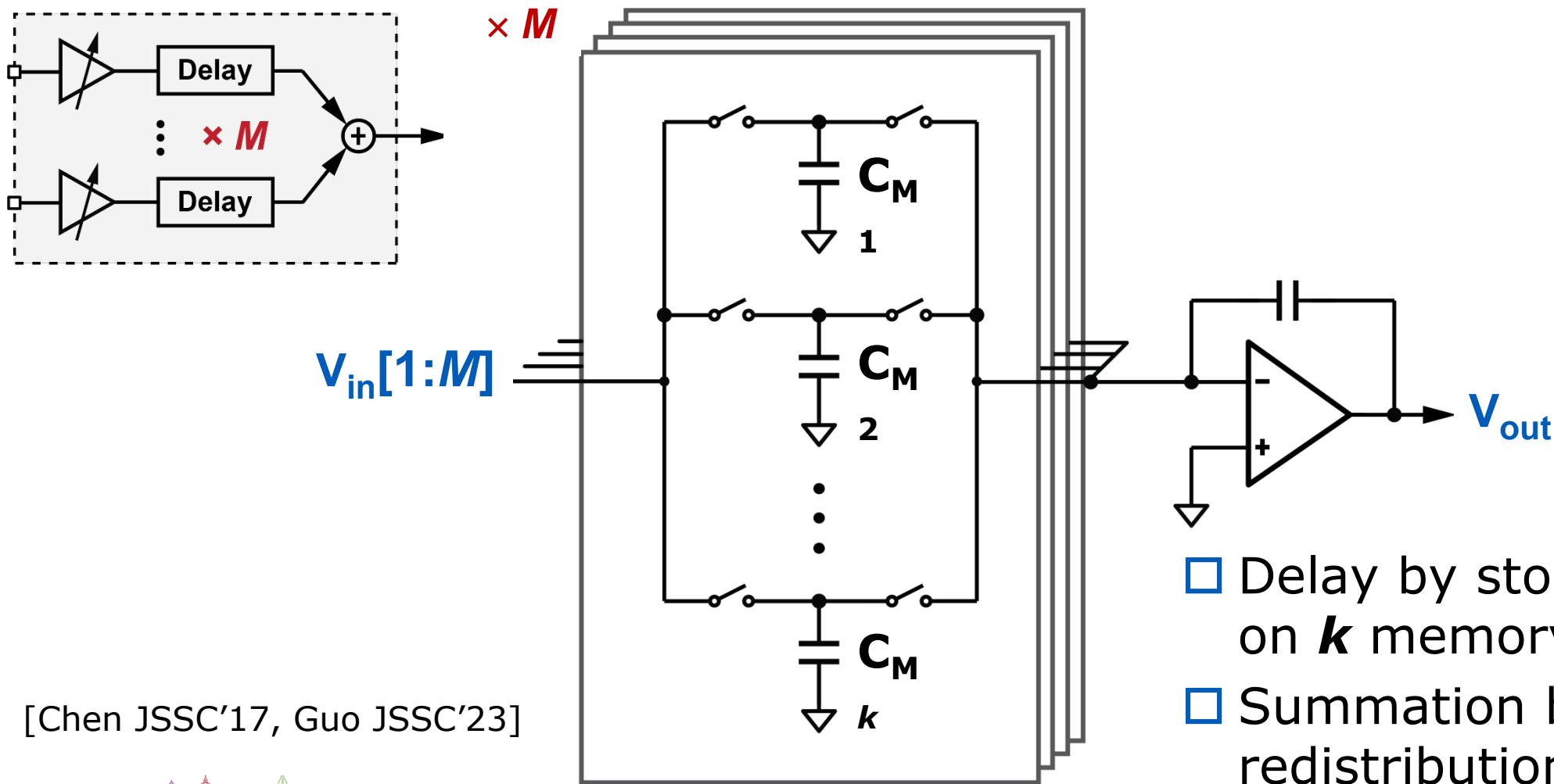
Sub-array Beamforming on a 2D Array



Sub-array Beamforming on a 2D Array



Analog Beamformer based on S&H delay lines

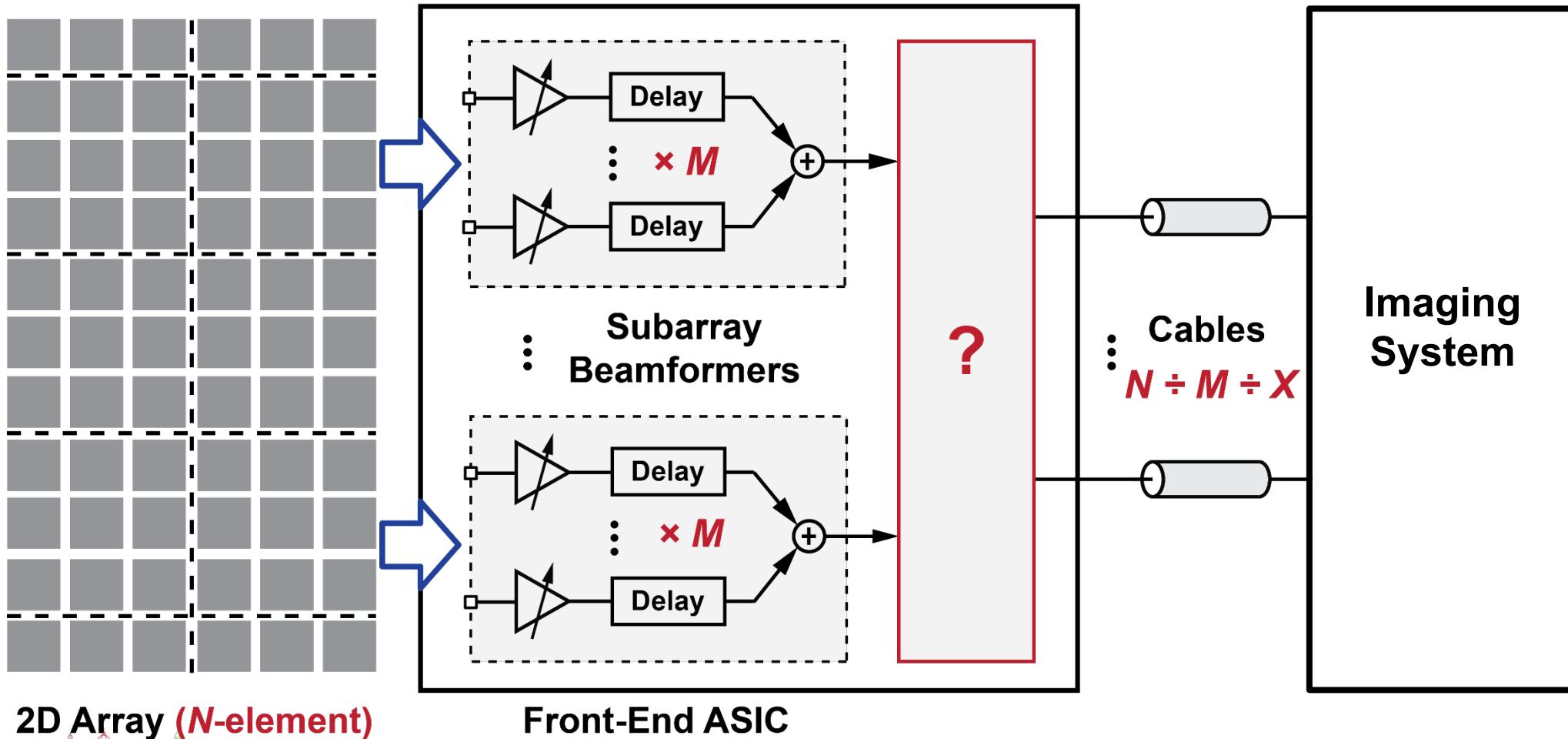


[Chen JSSC'17, Guo JSSC'23]

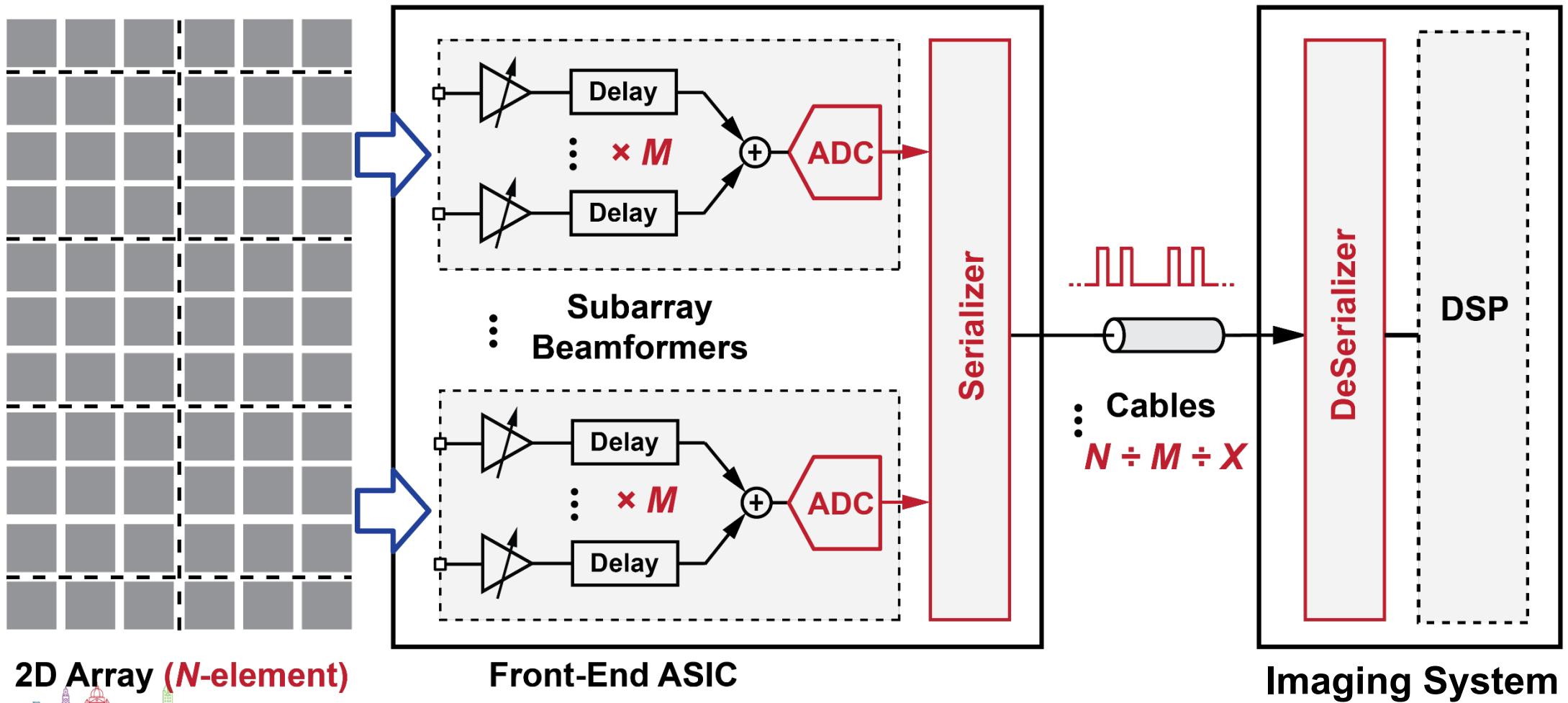
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Further Channel Reduction?



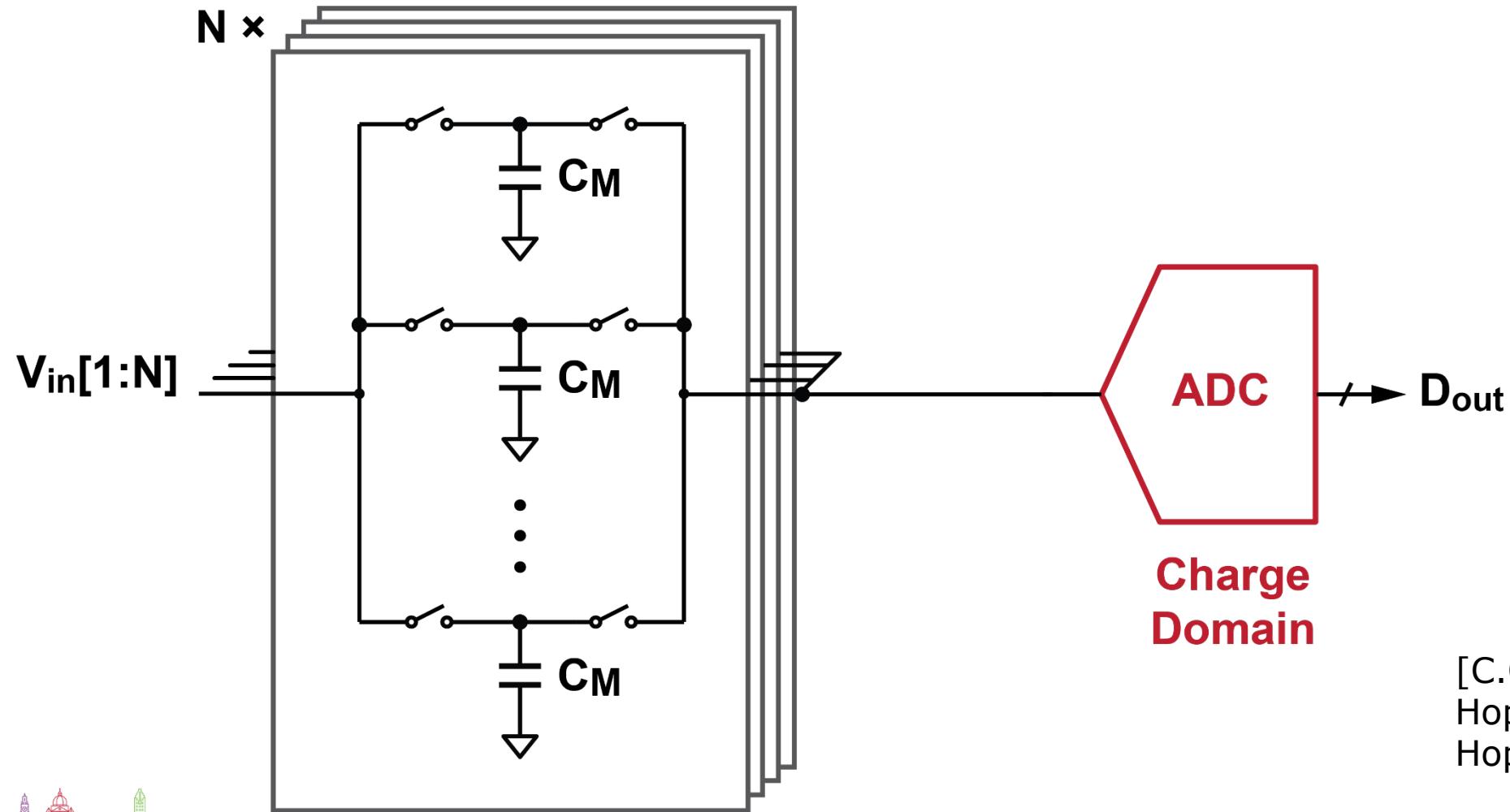
Go Digital !



In-probe digitization

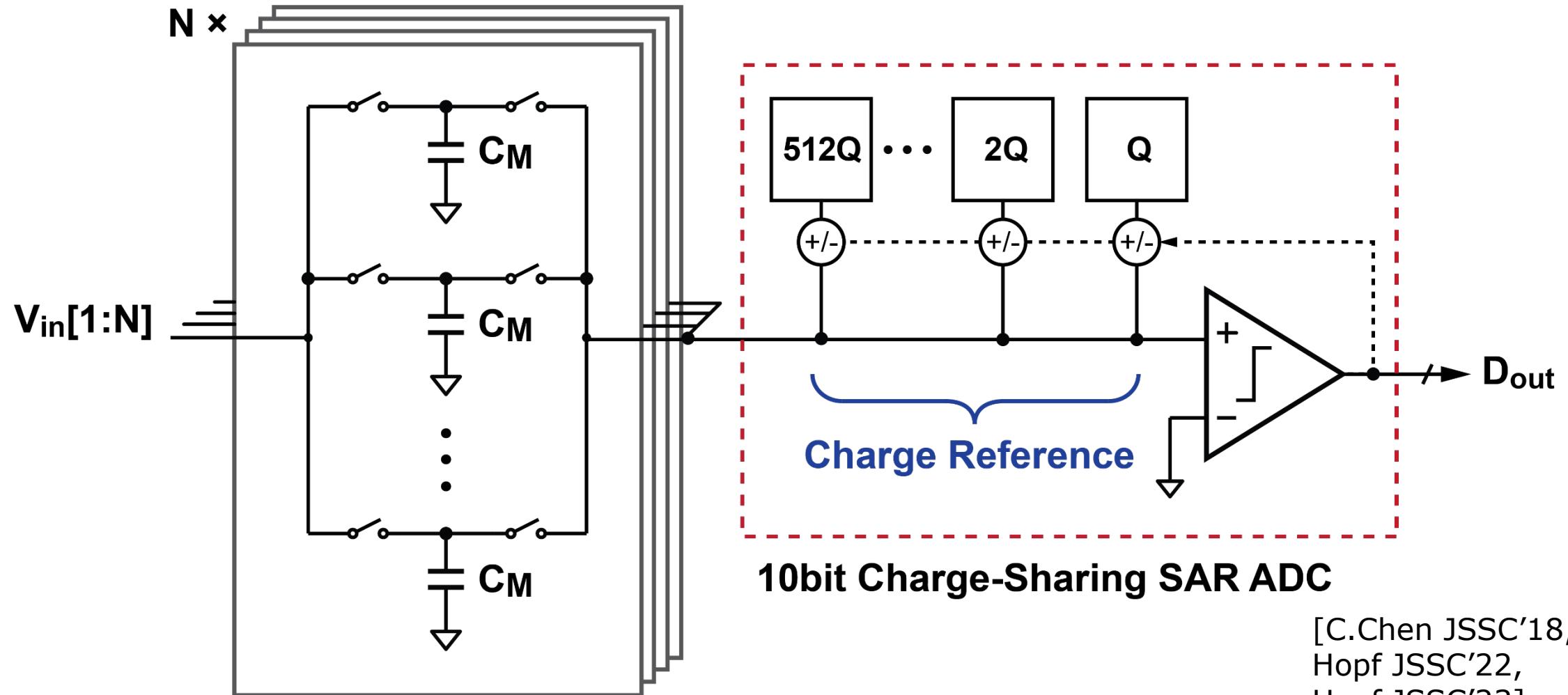
- Sampled >> Nyquist
 - Typically $\geq 4x$ transducer center frequency to enable accurate pulse timing
- Resolution typically 8..14 bits
 - Quantization noise should be lower than AFE noise to prevent SNR degradation
 - PGA/TGC prior to ADC helps to reduce dynamic range
 - Linearity / distortion not critical for fundamental imaging, but can be for harmonic
 - Jitter critical for Doppler imaging
- Various suitable architectures
 - Pipeline ADCs
 - Delta-sigma ADCs
 - SAR ADCs
 - Hybrids (e.g. SAR/slope, noise-shaping SAR)

Sub-Array Beamformer + Charge-Domain ADC



[C.Chen JSSC'18,
Hopf JSSC'22,
Hopf JSSC'23]

Charge Domain Beamforming SAR ADC



[C.Chen JSSC'18,
Hopf JSSC'22,
Hopf JSSC'23]

Datalink

- Digitized data needs to be sent to imaging system
 - Data rates can be very high
 - Example: 40 Mb/s 10-bit ADC → 400 Mb/s per RX channel
 - Standards like LVDS, JESD204B allow directly interfacing to FPGAs, but can be power hungry
- Custom designs, like load-modulation and multi-level signalling, can strongly reduce power
 - Can benefit from the high bit-error tolerance of ultrasound signals
 - BER up to 10^{-4} can be tolerated
 - $>10x$ less power than LVDS



Conclusions and Outlook

- **In-probe electronics** are key for advanced ultrasound probes
 - Provide SNR improvement
 - Channel-count reduction → enable 3D probes
- **In-probe digitization** is the next step
 - Enabler for in-probe data processing / compression
 - Further cable count reduction using high-speed digital data links
- Ultrasound devices will become **portable, wearable, disposable**
 - Integrated circuits will be essential for size, power and cost reduction
- Calls for **out-of-the-box solutions** and **multi-disciplinary collaboration**

References

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Integrated Transceivers for Emerging Medical Ultrasound Imaging Devices: A Review

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Abstract- As medical ultrasound imaging moves from conventional cart-based scanners to new form factors such as imaging catheters, hand-held point-of-care scanners and ultrasound patches, there is an increasing need for integrated transceivers that can be closely integrated with the transducer to provide channel-count reduction, improved signal quality and even full digitization. This paper reviews compact and power-efficient circuit solutions for such transceivers. It starts with a brief overview of ultrasound transducer technologies and the operating principles of the ultrasound transmit-receive signal path. For transmission, high-voltage pulser are reviewed, from compact unipolar pulsers to multi-level pulsers that provide amplitude control and improved power efficiency. The review of receive circuits starts with low-noise amplifiers as the power- and performance-limiting building block. Solutions for time-gain compensation are discussed, which are essential to reduce signal dynamic range by compensating for the decaying echo-signal amplitude associated with propagation attenuation. Finally, the option of direct digitization of the echo signal at the transducer is discussed. The paper ends with a reflection on future opportunities and challenges in the area of integrated circuits for ultrasound applications.

Index Terms— Ultrasound imaging, high-voltage pulsers, analog front-ends, low-noise amplifiers, time-gain compensation, in-probe digitization

I. INTRODUCTION

ULTRASOUND imaging is widely used to assist diagnosis and guide treatments in a broad range of medical applications, such as obstetrics and cardiology. Although ultrasound imaging has been around for decades, new developments are poised to radically change the way ultrasound is used. First, the form factor is changing. While ultrasound imaging is still mostly based on hand-held probes connected to a bulky imaging system, it is now becoming available in the form of pocket-size handheld scanners [1], endoscopes [2], catheters [3], pills [4] and patches [5] (Fig. 1). Second, ultrasound imaging is moving from 2D to 3D. While conventionally a 1D transducer array is used to produce 2D cross-sectional images, 2D arrays that can generate 3D images become increasingly common, not only in hand-held probes, but also in miniature probes like endoscopes and imaging catheters [2, 3]. Third, ultrasound is moving out of the hands of an expert sonographer into more widespread use by clinicians in general and, eventually, by the general public, calling for cost reduction and increased user-friendliness [1].

Integrated circuits play a key role in these developments. The electronics architecture of conventional imaging systems, based on commercial off-the-shelf components, is not scalable to the mentioned new form factors in terms of size and power consumption. Moreover, in terms of channel

Fig. 1. Examples of emerging medical ultrasound imaging devices (clockwise from the left): a hand-held point-of-care ultrasound scanner (image courtesy of Butterfly Network) [1]; a 3D intra-cardiac imaging catheter [2]; an artist's impression of a 3D transesophageal ultrasound probe [3]; a pill-shaped ultrasonic endoscopy device (image courtesy of Univ. of Glasgow) [4]; an artist's impression of a wearable ultrasound patch (image courtesy of UCLMPDA project) [5].

count, these architectures are not scalable to 3D imaging. Integrated transceiver circuits, closely integrated with the ultrasound transducer array, can solve these problems, e.g. [2, 7, 8]. Combined with the move from conventional labour-intensive and expensive bulk-piezoelectric transducer technology to micro-machined transducers, integrated circuits pave the way to the cost reduction needed for more widespread use [1].

This paper reviews recent advances in the design of integrated ultrasound transceivers. Section II starts with a

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References

Our website: <http://ei.ewi.tudelft.nl/>

- [1] C. Chen *et al.*, "A Front-End ASIC With Receive Sub-array Beamforming Integrated With a 32 x 32 PZT Matrix Transducer for 3-D Transesophageal Echocardiography," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 994–1006, Apr. 2017, doi: 10.1109/JSSC.2016.2638433.
- [2] J. M. Rothberg *et al.*, "Ultrasound-on-chip platform for medical imaging, analysis, and collective intelligence," *Proc. Natl. Acad. Sci. U.S.A.*, vol. 118, no. 27, p. e2019339118, Jul. 2021, doi: 10.1073/pnas.2019339118.
- [3] C. Wang *et al.*, "Continuous monitoring of deep-tissue haemodynamics with stretchable ultrasonic phased arrays," *Nat Biomed Eng*, vol. 5, no. 7, pp. 749–758, Jul. 2021, doi: 10.1038/s41551-021-00763-4.
- [4] A. Safari and E. K. Akdoğan, Eds., *Piezoelectric and Acoustic Materials for Transducer Applications*. Boston, MA: Springer US, 2008. doi: 10.1007/978-0-387-76540-2.
- [5] K. Brenner, A. Ergun, K. Firouzi, M. Rasmussen, Q. Stedman, and B. Khuri-Yakub, "Advances in Capacitive Micromachined Ultrasonic Transducers," *Micromachines*, vol. 10, no. 2, p. 152, Feb. 2019, doi: 10.3390/mi10020152.
- [6] Y. Qiu *et al.*, "Piezoelectric Micromachined Ultrasound Transducer (PMUT) Arrays for Integrated Sensing, Actuation and Imaging," *Sensors*, vol. 15, no. 4, pp. 8020–8041, Apr. 2015, doi: 10.3390/s150408020.

References

Our website: <http://ei.ewi.tudelft.nl/>

- [7] C. Chen *et al.*, "A Prototype PZT Matrix Transducer With Low-Power Integrated Receive ASIC for 3-D Transesophageal Echocardiography," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 63, no. 1, pp. 47–59, Jan. 2016, doi: 10.1109/TUFFC.2015.2496580.
- [8] R. Wodnicki *et al.*, "Co-Integrated PIN-PMN-PT 2-D Array and Transceiver Electronics by Direct Assembly Using a 3-D Printed Interposer Grid Frame," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 67, no. 2, pp. 387–401, Feb. 2020, doi: 10.1109/TUFFC.2019.2944668.
- [9] H. Kang *et al.*, "2-D Array Design and Fabrication With Pitch-Shifting Interposer at Frequencies From 4 MHz up to 10 MHz," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 69, no. 12, pp. 3382–3391, Dec. 2022, doi: 10.1109/TUFFC.2022.3216602.
- [10] D. Wildes *et al.*, "4-D ICE: A 2-D Array Transducer With Integrated ASIC in a 10-Fr Catheter for Real-Time 3-D Intracardiac Echocardiography," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 63, no. 12, pp. 2159–2173, Dec. 2016, doi: 10.1109/TUFFC.2016.2615602.
- [11] E. Kang *et al.*, "A Variable-Gain Low-Noise Transimpedance Amplifier for Miniature Ultrasound Probes," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3157–3168, Dec. 2020, doi: 10.1109/JSSC.2020.3023618.

References

Our website: <http://ei.ewi.tudelft.nl/>

- [12] F. L. Degertekin, "Microscale systems based on ultrasonic MEMS — CMOS integration," in *2017 19th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, Kaohsiung: IEEE, Jun. 2017, pp. 397–401. doi: 10.1109/TRANSDUCERS.2017.7994071.
- [13] A. Bhuyan *et al.*, "Integrated Circuits for Volumetric Ultrasound Imaging With 2-D CMUT Arrays," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 6, pp. 796–804, Dec. 2013, doi: 10.1109/TBCAS.2014.2298197.
- [14] I. Zamora, E. Ledesma, A. Uranga, and N. Barniol, "Phased Array Based on AlScN Piezoelectric Micromachined Ultrasound Transducers Monolithically Integrated on CMOS," *IEEE Electron Device Lett.*, vol. 43, no. 7, pp. 1113–1116, Jul. 2022, doi: 10.1109/LED.2022.3175323.
- [15] D. A. Horsley *et al.*, "Ultrasonic fingerprint sensor based on a PMUT array bonded to CMOS circuitry," in *2016 IEEE International Ultrasonics Symposium (IUS)*, Tours, France: IEEE, Sep. 2016, pp. 1–4. doi: 10.1109/ULTSYM.2016.7728817.
- [16] I. O. Wygant *et al.*, "Integration of 2D CMUT arrays with front-end electronics for volumetric ultrasound imaging," *IEEE Trans. Ultrason., Ferroelectr., Freq. Contr.*, vol. 55, no. 2, pp. 327–342, Feb. 2008, doi: 10.1109/TUFFC.2008.652.

References

Our website: <http://ei.ewi.tudelft.nl/>

- [17] K. Chen, H.-S. Lee, A. P. Chandrakasan, and C. G. Sodini, "Ultrasonic Imaging Transceiver Design for CMUT: A Three-Level 30-Vpp Pulse-Shaping Pulser With Improved Efficiency and a Noise-Optimized Receiver," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2734–2745, Nov. 2013, doi: 10.1109/JSSC.2013.2274895.
- [18] M. Sutto *et al.*, "A CMUT transceiver front-end with 100-V TX driver and 1-mW low-noise capacitive feedback RX amplifier in BCD-SOI technology," in *ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC)*, Venice Lido, Italy: IEEE, Sep. 2014, pp. 407–410. doi: 10.1109/ESSCIRC.2014.6942108.
- [19] C. Chen, Z. Chen, Z. Chang, and M. A. P. Pertijs, "A compact 0.135-mW/channel LNA array for piezoelectric ultrasound transducers," in *ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference (ESSCIRC)*, Graz, Austria: IEEE, Sep. 2015, pp. 404–407. doi: 10.1109/ESSCIRC.2015.7313913.
- [20] G. Gurun *et al.*, "Single-chip CMUT-on-CMOS front-end system for real-time volumetric IVUS and ICE imaging," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 61, no. 2, pp. 239–250, Feb. 2014, doi: 10.1109/TUFFC.2014.6722610.
- [21] I. O. Wygant *et al.*, "An integrated circuit with transmit beamforming flip-chip bonded to a 2-D CMUT array for 3-D ultrasound imaging," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 56, no. 10, pp. 2145–2156, Oct. 2009, doi: 10.1109/TUFFC.2009.1297.

References

Our website: <http://ei.ewi.tudelft.nl/>

- [22] H.-Y. Tang *et al.*, "Miniaturizing Ultrasonic System for Portable Health Care and Fitness," *IEEE Trans. Biomed. Circuits Syst.*, pp. 1–1, 2016, doi: 10.1109/TBCAS.2015.2508439.
- [23] A. Bhuyan *et al.*, "3D volumetric ultrasound imaging with a 32x32 CMUT array integrated with front-end ICs using flip-chip bonding technology," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA: IEEE, Feb. 2013, pp. 396–397. doi: 10.1109/ISSCC.2013.6487786.
- [24] K. Chen, H.-S. Lee, and C. G. Sodini, "A Column-Row-Parallel ASIC Architecture for 3-D Portable Medical Ultrasonic Imaging," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 738–751, Mar. 2016, doi: 10.1109/JSSC.2015.2505714.
- [25] Y. Katsume *et al.*, "27.6 Single-chip 3072ch 2D array IC with RX analog and all-digital TX beamformer for 3D ultrasound imaging," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA: IEEE, Feb. 2017, pp. 458–459. doi: 10.1109/ISSCC.2017.7870459.
- [26] B. Savord and R. Solomon, "Fully sampled matrix transducer for real time 3D ultrasonic imaging," in *IEEE Symposium on Ultrasonics, 2003*, Honolulu, HI, USA: IEEE, 2003, pp. 945–953. doi: 10.1109/ULTSYM.2003.1293556.

References

Our website: <http://ei.ewi.tudelft.nl/>

- [27] S. Tamano, T. Kobayashi, S. Sano, K. Hara, J. Sakano, and T. Azuma, “3D ultrasound imaging system using fresnel ring array & high voltage multiplexer IC,” in *IEEE Ultrasonics Symposium, 2004*, Montreal, Canada: IEEE, 2004, pp. 782–785. doi: 10.1109/ULTSYM.2004.1417838.
- [28] R. Fisher *et al.*, “Reconfigurable arrays for portable ultrasound,” in *IEEE Ultrasonics Symposium, 2005.*, Rotterdam, The Netherlands: IEEE, 2005, pp. 495–499. doi: 10.1109/ULTSYM.2005.1602899.
- [29] A. Ramalli, E. Boni, A. S. Savoia, and P. Tortoli, “Density-tapered spiral arrays for ultrasound 3-D imaging,” *IEEE Trans. Ultrason., Ferroelectr., Freq. Contr.*, vol. 62, no. 8, pp. 1580–1588, Aug. 2015, doi: 10.1109/TUFFC.2015.007035.
- [30] B.-H. Kim, Y. Kim, S. Lee, K. Cho, and J. Song, “Design and test of a fully controllable 64x128 2-D CMUT array integrated with reconfigurable frontend ASICs for volumetric ultrasound imaging,” in *2012 IEEE International Ultrasonics Symposium*, Dresden, Germany: IEEE, Oct. 2012, pp. 77–80. doi: 10.1109/ULTSYM.2012.0019.
- [31] T. M. Carpenter, M. W. Rashid, M. Ghovanloo, D. M. J. Cowell, S. Freear, and F. L. Degertekin, “Direct Digital Demultiplexing of Analog TDM Signals for Cable Reduction in Ultrasound Imaging Catheters,” *IEEE Trans. Ultrason., Ferroelectr., Freq. Contr.*, vol. 63, no. 8, pp. 1078–1085, Aug. 2016, doi: 10.1109/TUFFC.2016.2557622.

References

Our website: <http://ei.ewi.tudelft.nl/>

- [32] A. Rezvanitabar *et al.*, "Integrated Hybrid Sub-Aperture Beamforming and Time-Division Multiplexing for Massive Readout in Ultrasound Imaging," *IEEE Trans. Biomed. Circuits Syst.*, vol. 16, no. 5, pp. 972–980, Oct. 2022, doi: 10.1109/TBCAS.2022.3205024.
- [33] J. A. Jensen *et al.*, "Anatomic and Functional Imaging Using Row–Column Arrays," *IEEE Trans. Ultrason., Ferroelectr., Freq. Contr.*, vol. 69, no. 10, pp. 2722–2738, Oct. 2022, doi: 10.1109/TUFFC.2022.3191391.
- [34] Y. Igarashi *et al.*, "Single-Chip 3072-Element-Channel Transceiver/128-Subarray-Channel 2-D Array IC With Analog RX and All-Digital TX Beamformer for Echocardiography," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2555–2567, Sep. 2019, doi: 10.1109/JSSC.2019.2921697.
- [35] C. Chen *et al.*, "A Pitch-Matched Front-End ASIC With Integrated Subarray Beamforming ADC for Miniature 3-D Ultrasound Probes," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3050–3064, Nov. 2018, doi: 10.1109/JSSC.2018.2864295.
- [36] Y. M. Hopf *et al.*, "A Pitch-Matched Transceiver ASIC With Shared Hybrid Beamforming ADC for High-Frame-Rate 3-D Intracardiac Echocardiography," *IEEE J. Solid-State Circuits*, vol. 57, no. 11, pp. 3228–3242, Nov. 2022, doi: 10.1109/JSSC.2022.3201758.

References

Our website: <http://ei.ewi.tudelft.nl/>

- [37] Y. M. Hopf *et al.*, “A Pitch-Matched High-Frame-Rate Ultrasound Imaging ASIC for Catheter-Based 3-D Probes,” *IEEE J. Solid-State Circuits*, pp. 1–16, 2023, doi: 10.1109/JSSC.2023.3299749.
- [38] P. Guo *et al.*, “A 1.2-mW/Channel Pitch-Matched Transceiver ASIC Employing a Boxcar-Integration-Based RX Micro-Beamformer for High-Resolution 3-D Ultrasound Imaging,” *IEEE J. Solid-State Circuits*, pp. 1–12, 2023, doi: 10.1109/JSSC.2023.3271270.
- [39] Z. Chen *et al.*, “Impact of Bit Errors in Digitized RF Data on Ultrasound Image Quality,” *IEEE Trans. Ultrason., Ferroelectr., Freq. Contr.*, vol. 67, no. 1, pp. 13–24, Jan. 2020, doi: 10.1109/TUFFC.2019.2937462.
- [40] P. Guo *et al.*, “A Pitch-Matched Transceiver ASIC for 3D Ultrasonography with Micro-Beamforming ADCs based on Passive Boxcar Integration and a Multi-Level Datalink,” in *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Kyoto, Japan: IEEE, Jun. 2023, pp. 1–2. doi: 10.23919/VLSITechnologyandCir57934.2023.10185159.



Thank you for your attention!

Questions?