Ultrasound system design:
Analog front end circuits, in-probe electronics and imaging systems

15th September 2025

David Cowell, School of Electronic and Electrical Engineering, University of Leeds, UK

Enrico Boni, Department of Information Engineering, University of Florence, Italy

Michiel Pertijs, Electronic Instrumentation Laboratory, Delft University of Technology, The Netherlands

Part 2: In-Probe Electronics

Michiel Pertijs
Electronic Instrumentation Laboratory
Delft University of Technology, The Netherlands
M.A.P.Pertijs@tudelft.nl

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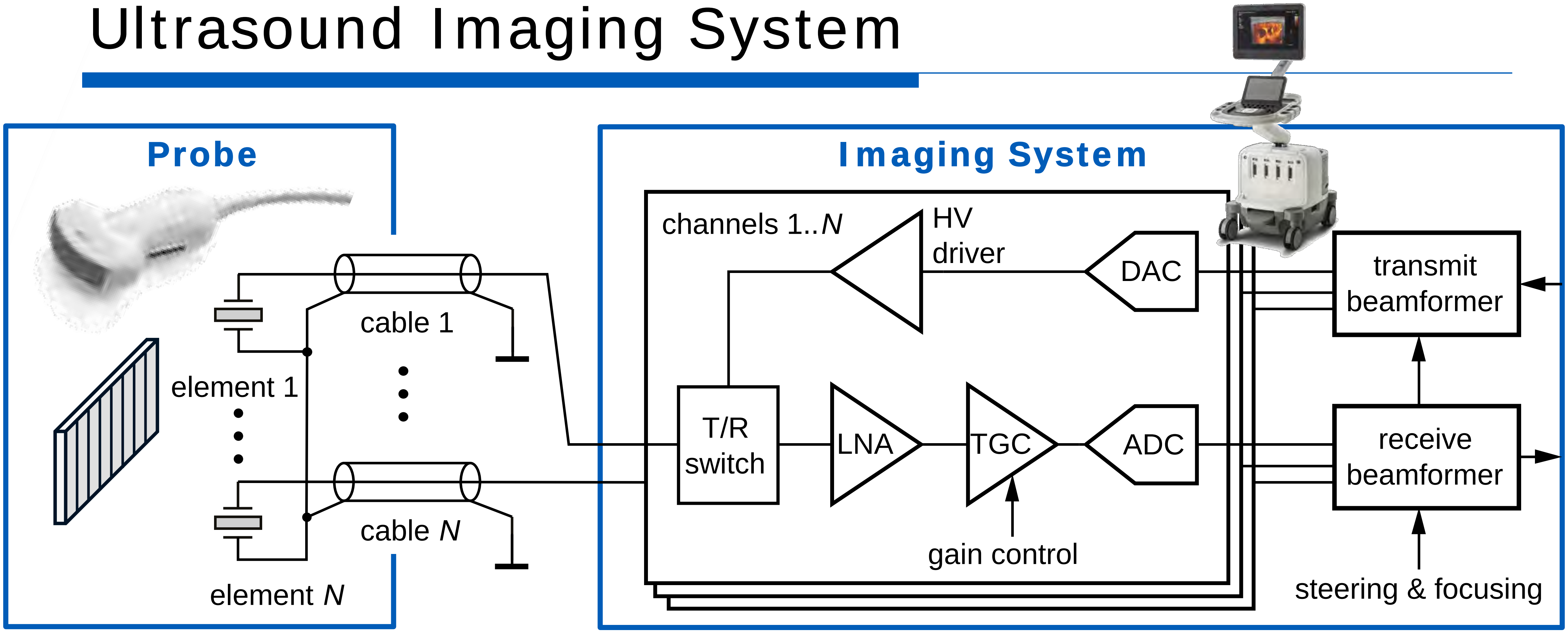
TU Delft

Ultrasound Imaging System



- One cable and one system channel per transducer element
- Practical systems typically 128, max 256 channels

Need for In-Probe Electronics

Point-of-Care Probes

High-end 3D Probes

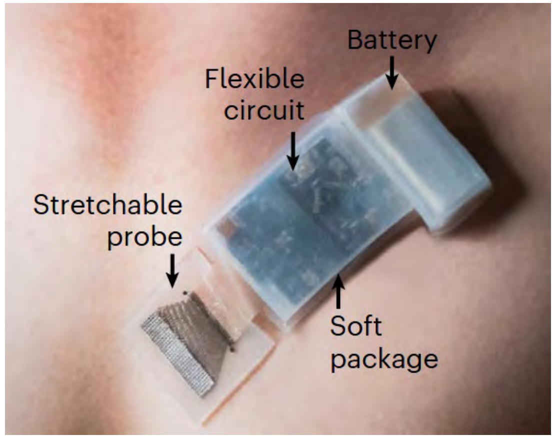
Philips X6-1

3D Imaging Catheters and Endoscopes

Oldelft Ultrasound mini 4D TEE

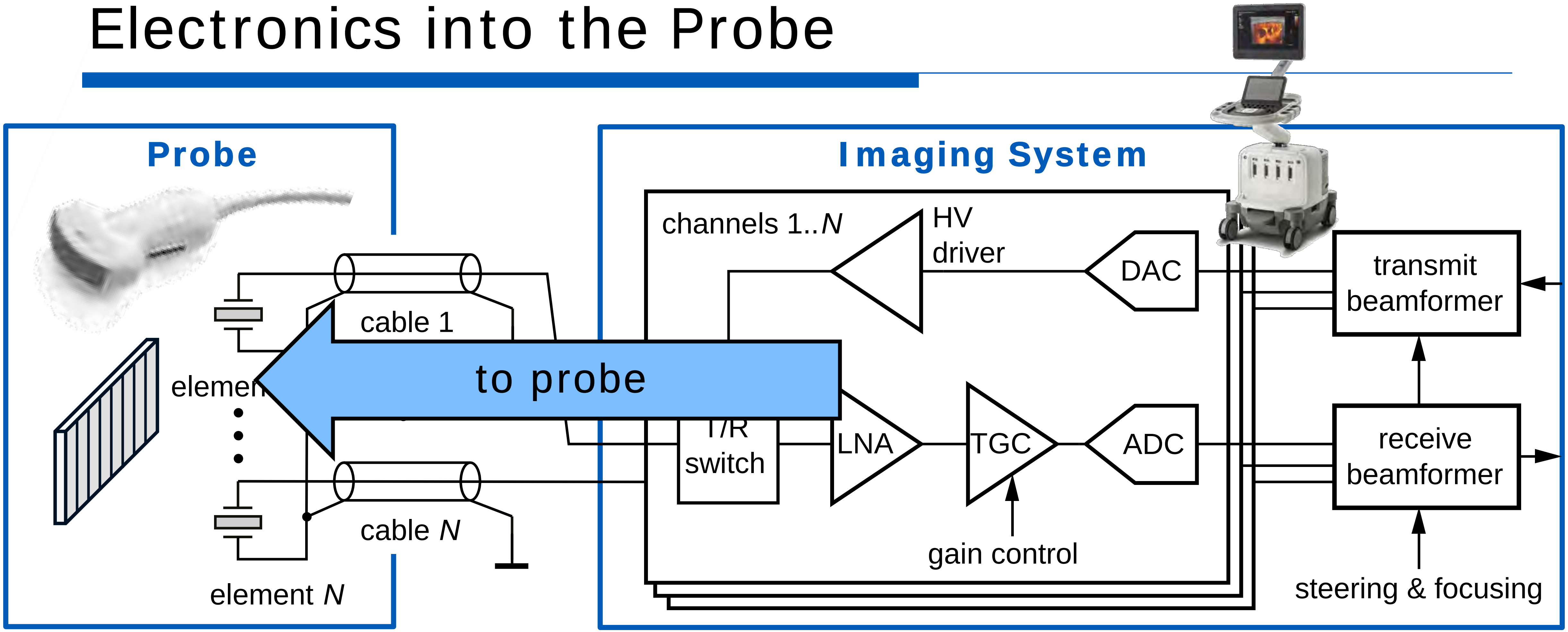
Butterfly IQ
[Rothberg PNAS'21]

Wearable Ultrasound



Univ. of California, San Diego
[Lin Nature BioTech'24]

Electronics into the Probe



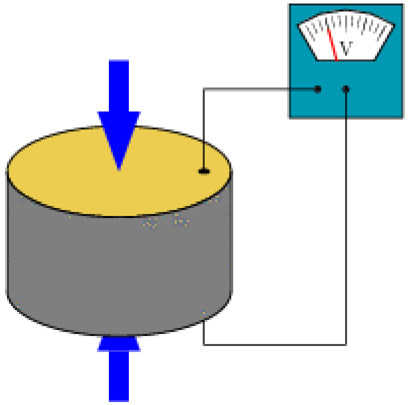
- Local amplification ⇒ improved SNR
- Local channel-count reduction ⇒ enabler for 3D imaging

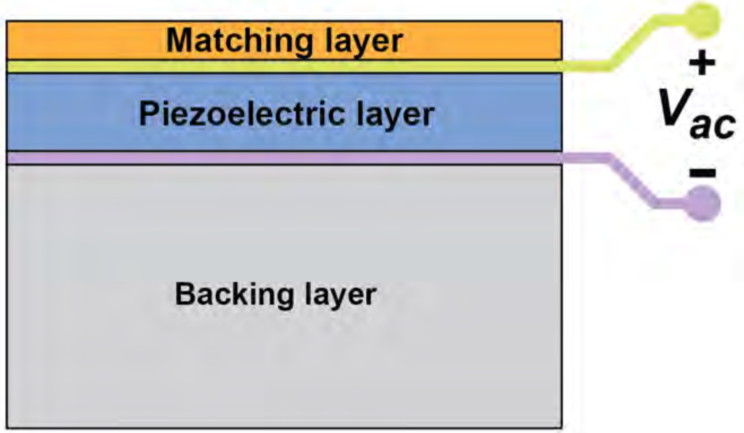
Outline

- Introduction
- **Transducer-ASIC integration schemes**
- In-probe front-end circuitry
- Channel-count reduction schemes
- Sub-array beamforming
- In-probe digitization
- Conclusions and outlook

Ultrasound Transducers

Bulk piezo-electric transducers



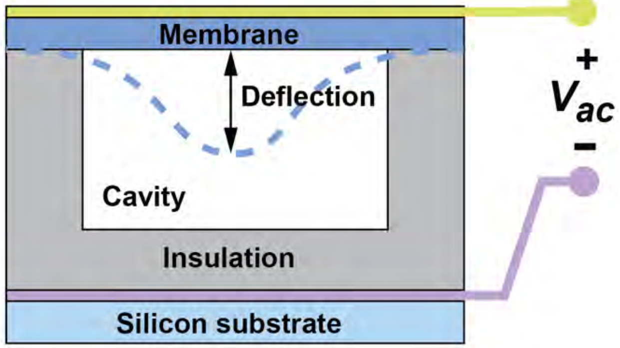


[Safari Springer'08]

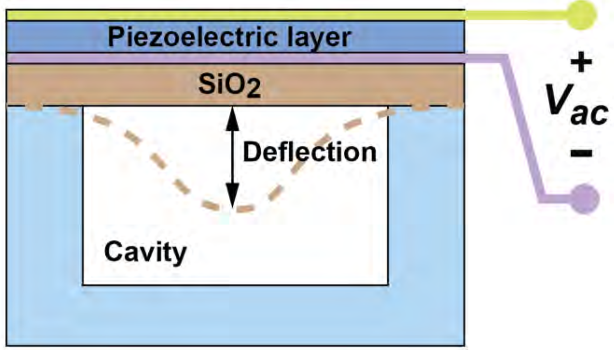
- Bulk piezo still dominant technology
- MEMS offers cost and integration advantages
- All can be integrated with ASICs

MEMS transducers

CMUTs

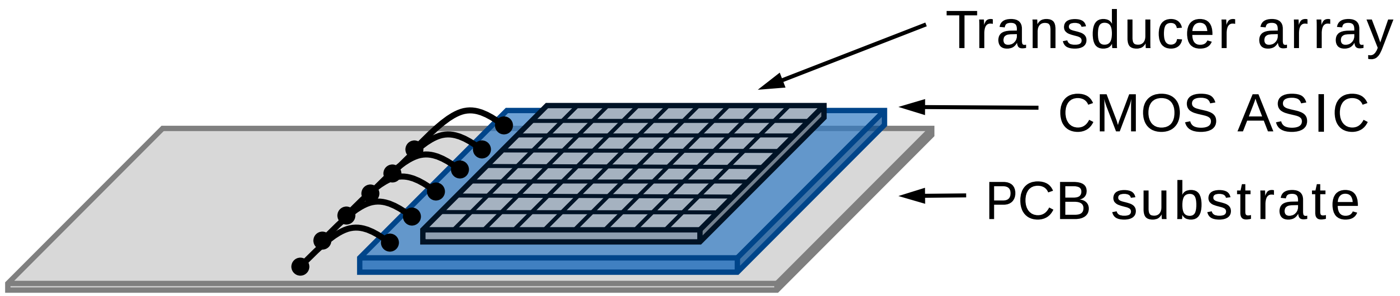


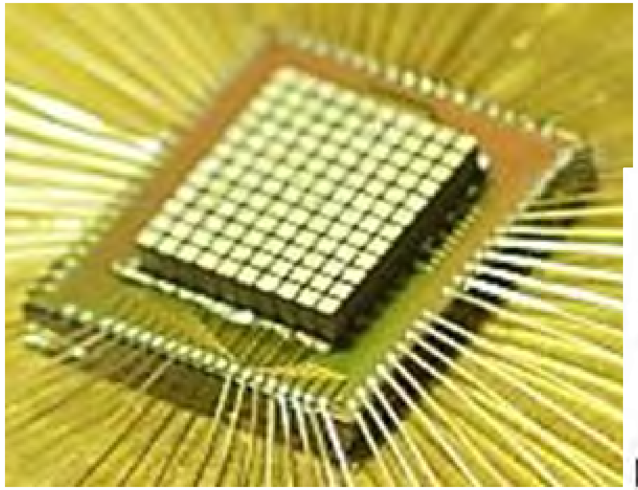
PMUTs

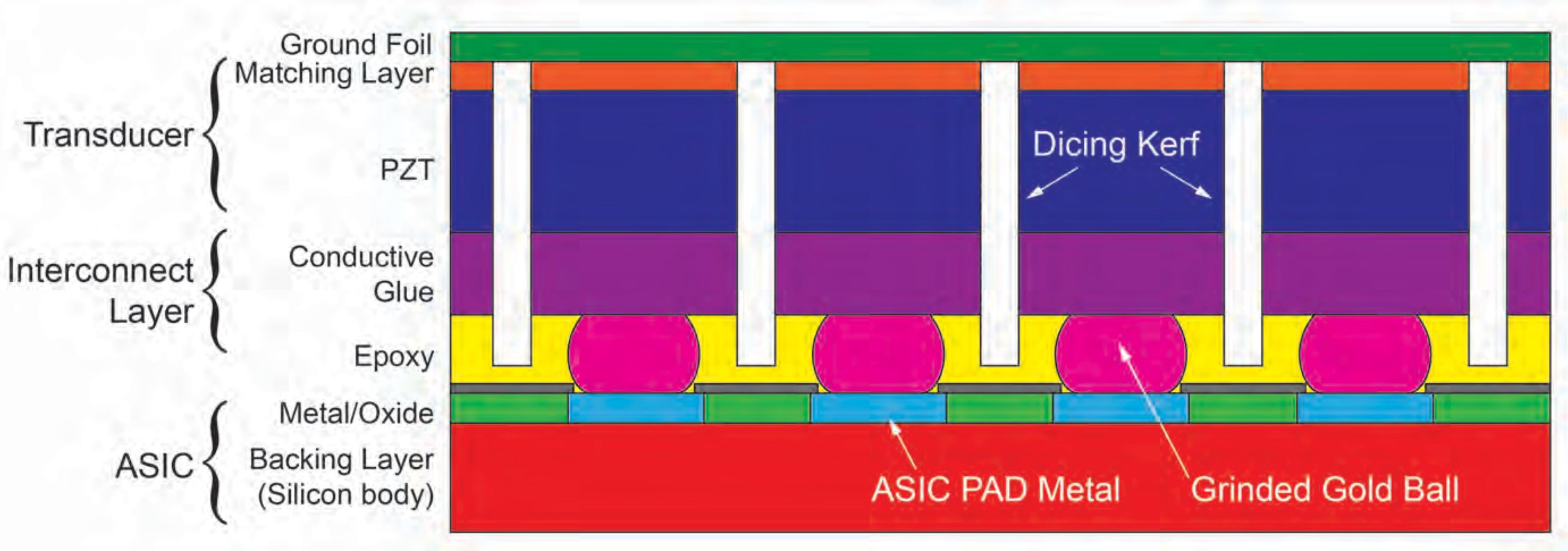


[Brenner MicroMachines'19] [Qiu Sensors'15]

Piezo-on-ASIC Integration

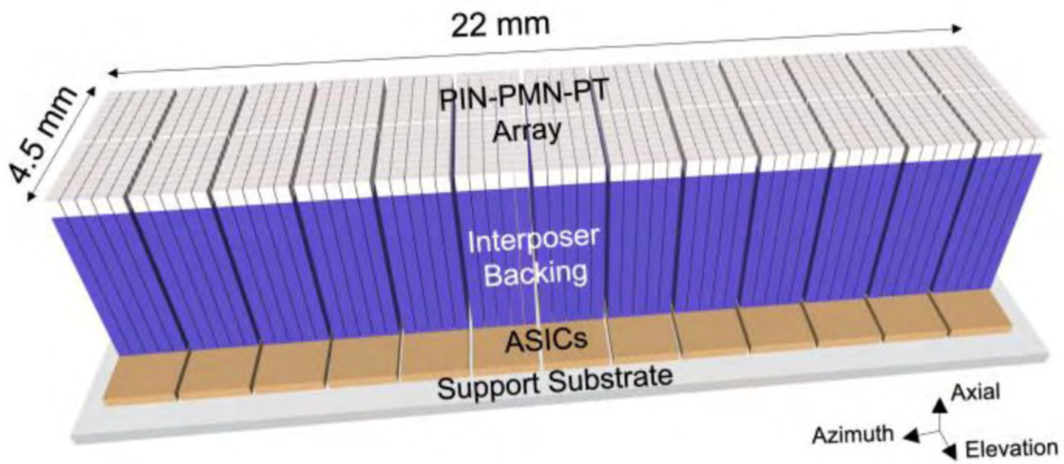


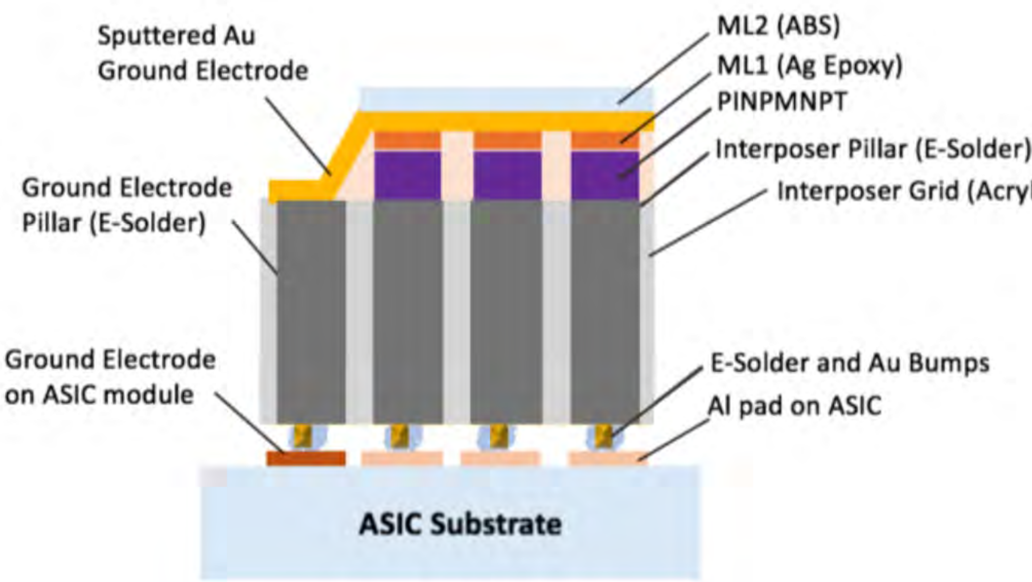




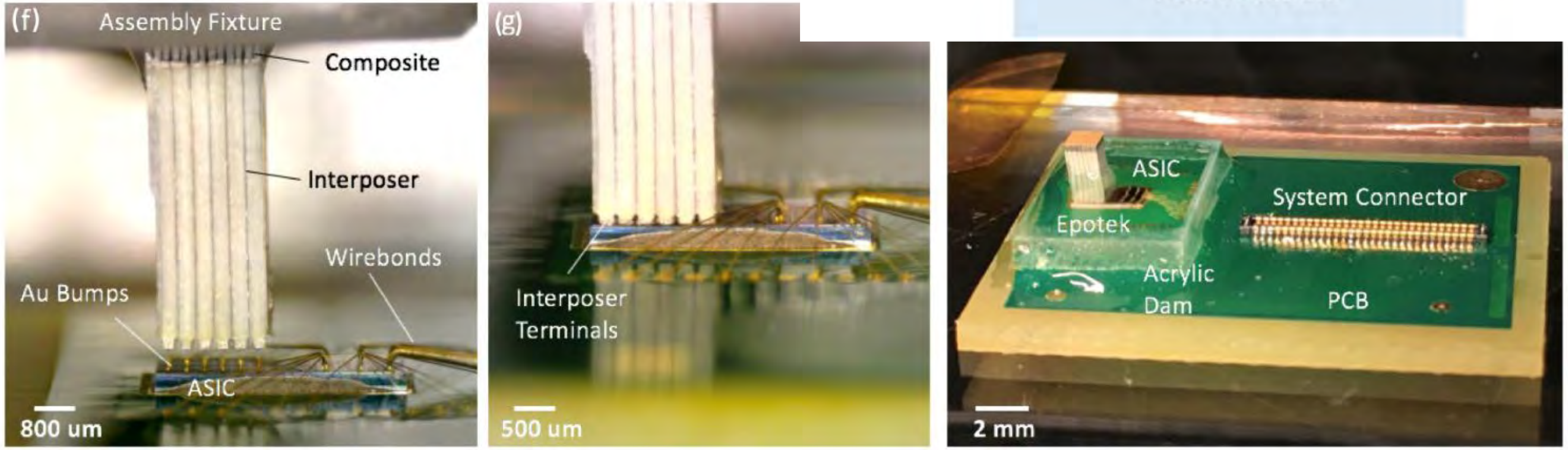
[Chen TUFFC'16]

Piezo-on-ASIC Integration with Interposer

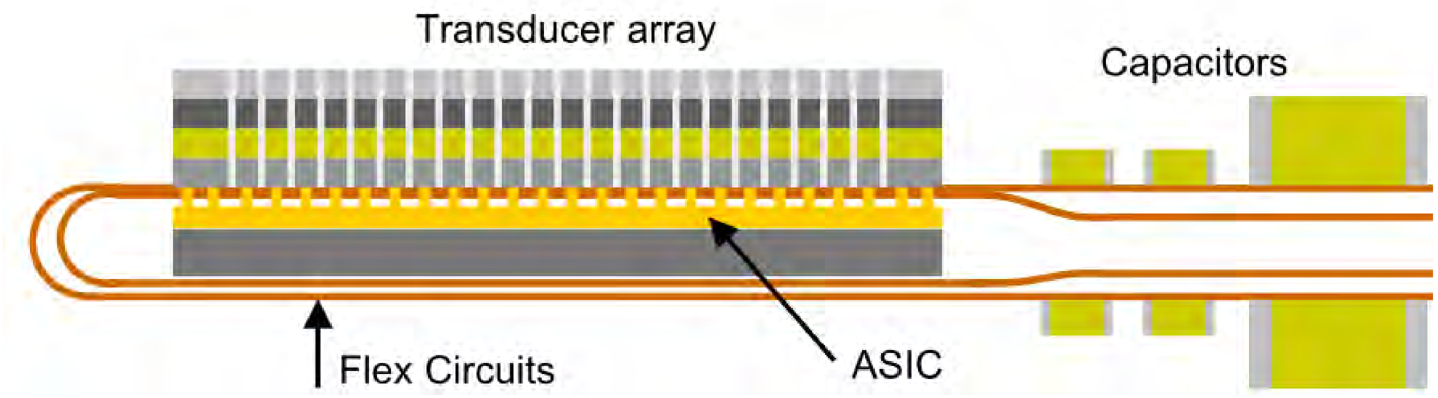


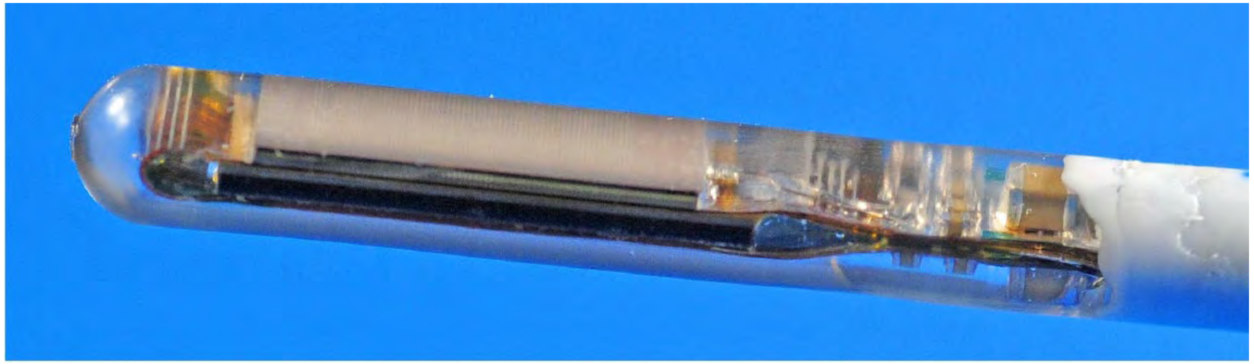


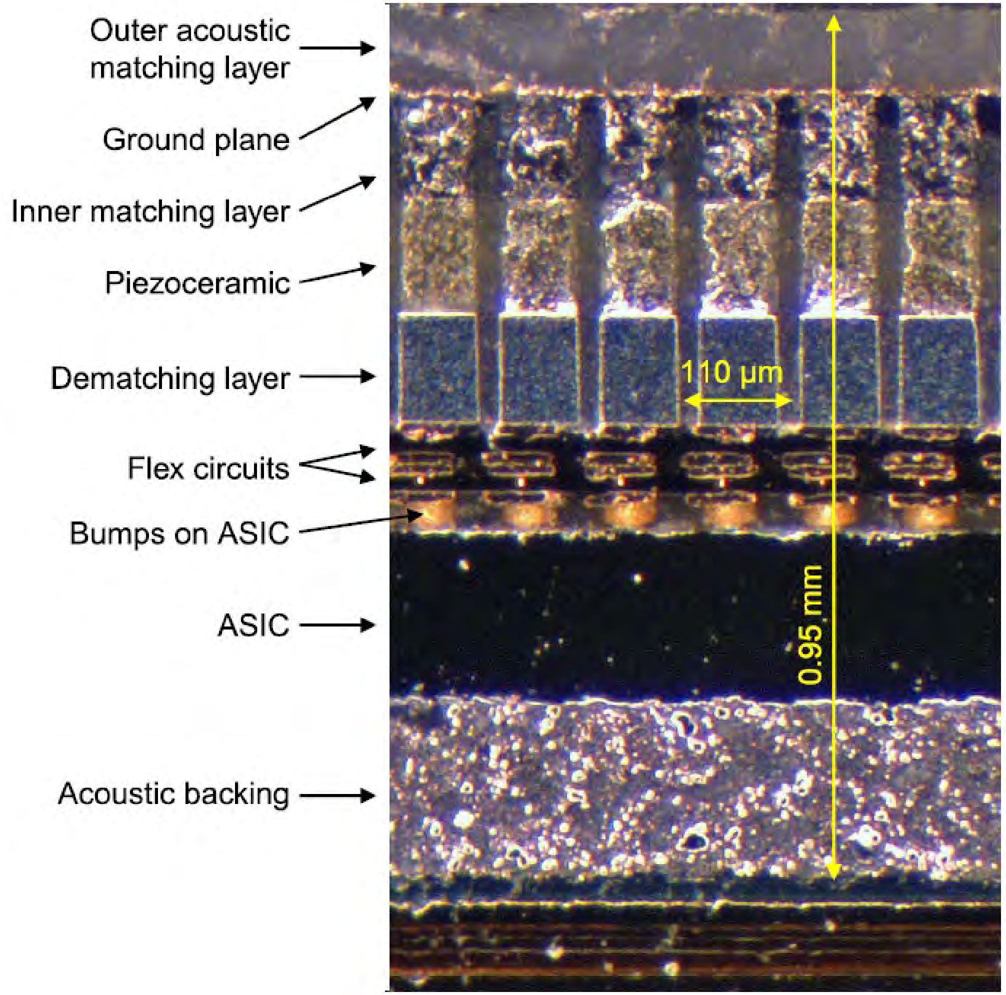
Univ. of S. California [Wodnicki TUFFC'20, Kang TUFFC'22]



Piezo-ASIC-Flex Integration

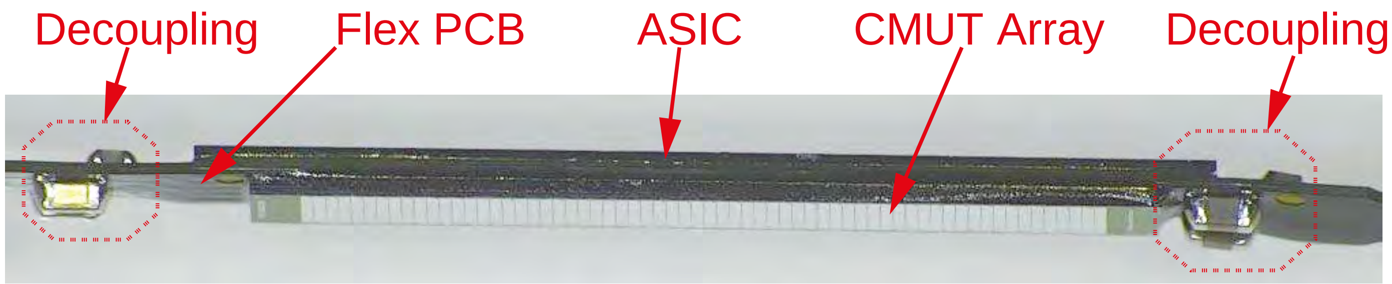




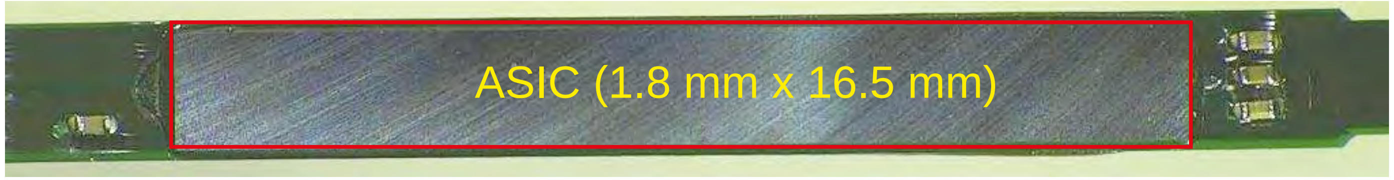


[Wildes TUFFC'16]

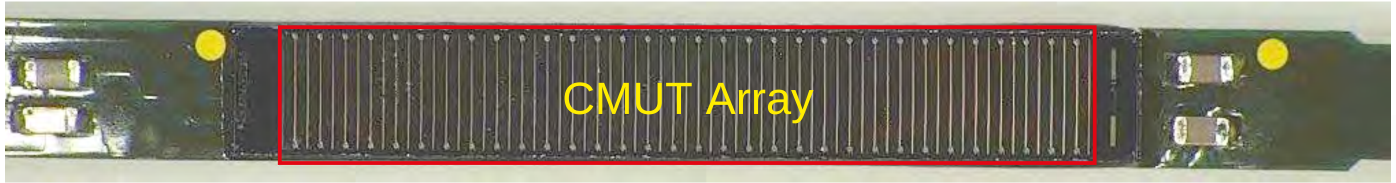
CMUT-ASIC-Flex PCB Integration



Side View



Bottom View



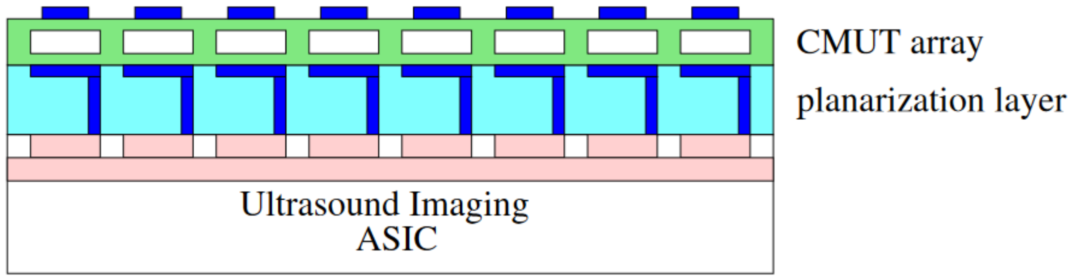
Top View

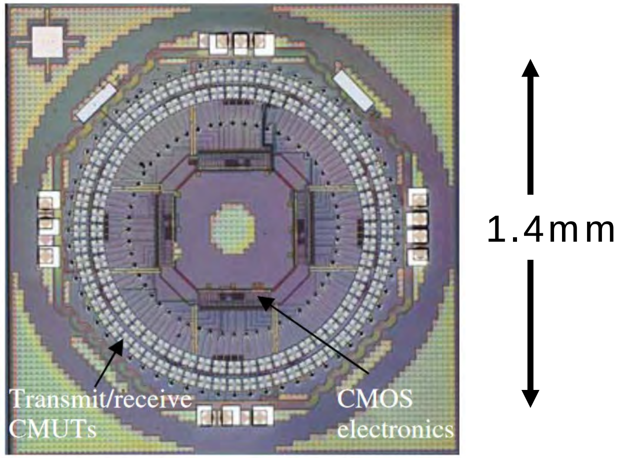
[Kang JSSC'20, Matéo IUS'20]

vermon

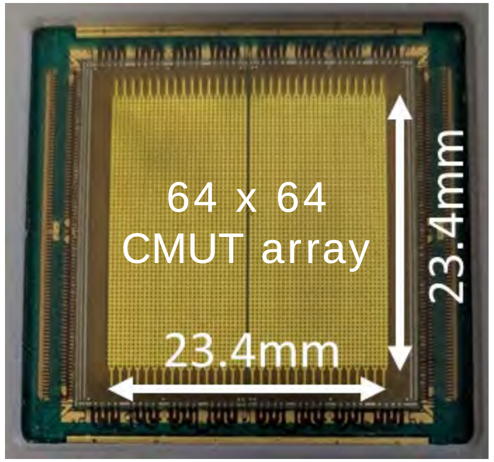
Direct CMUT-ASIC Integration

Monolithic integration



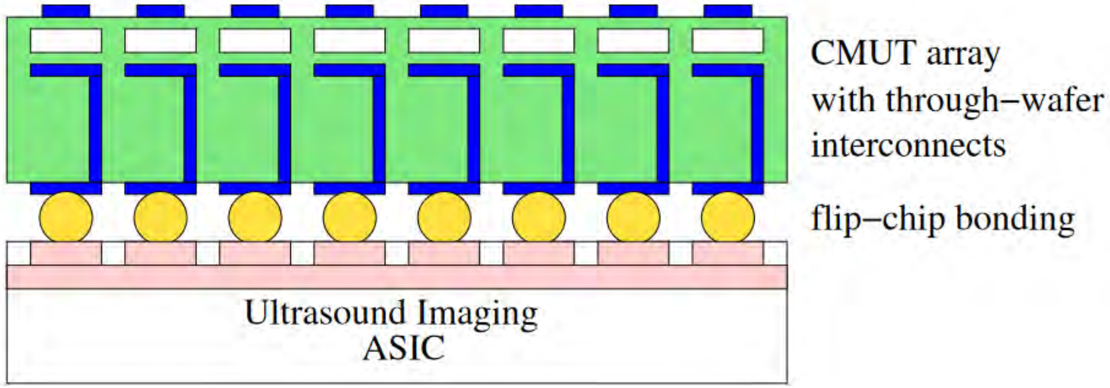


[Degertekin Transducers’17]

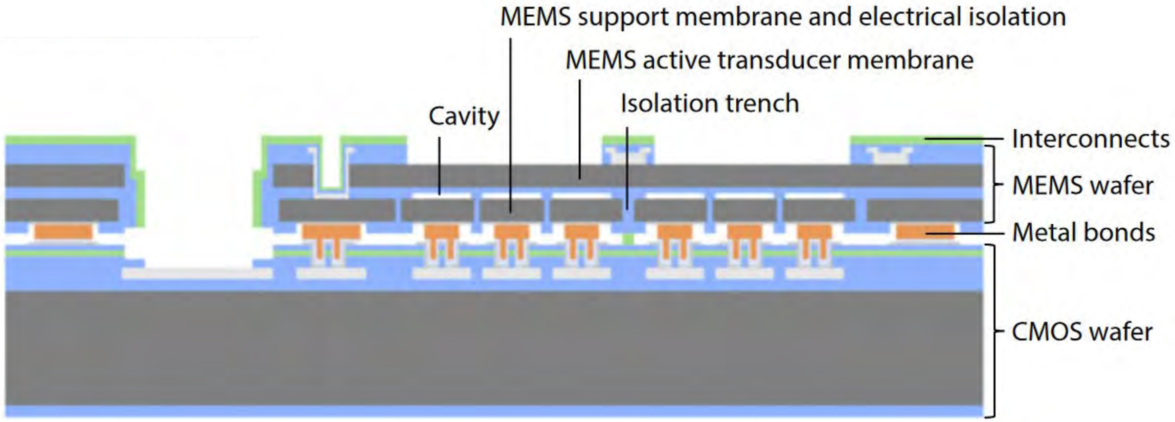


[Rozsa JSSC’25]

Chip-to-chip or wafer-to-wafer bonding

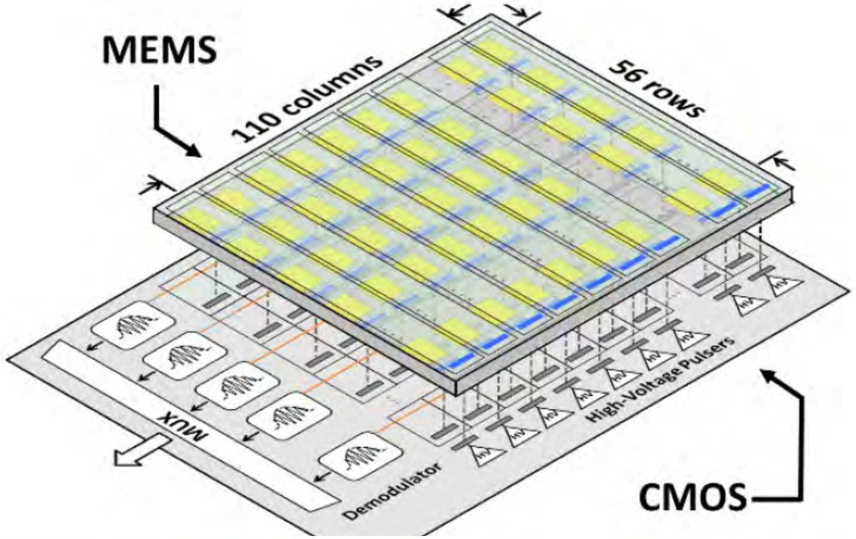


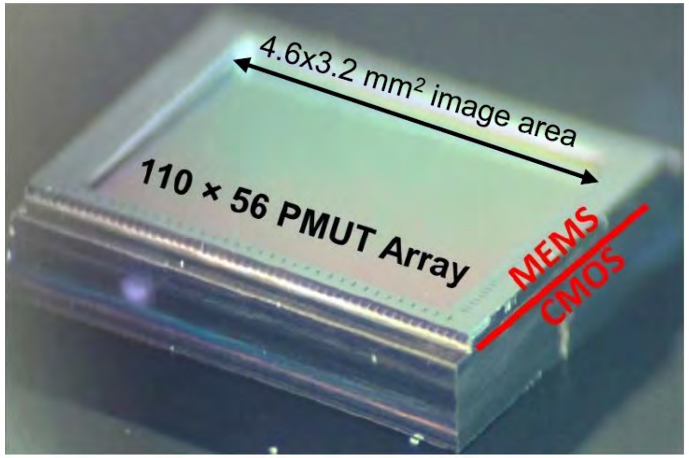
[Brenner MicroMachines’19]



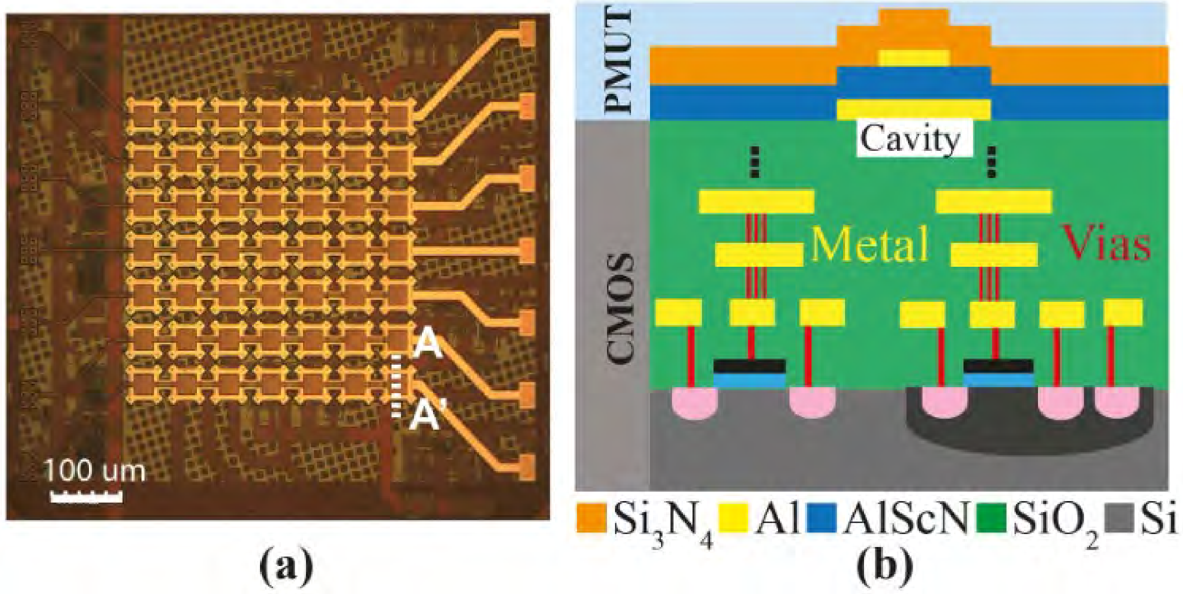
Butterfly [Rothberg PNAS’21]

Direct PMUT-ASIC Integration





[Horsley IUS'16]



SilTerra [Zamora EDL'22]

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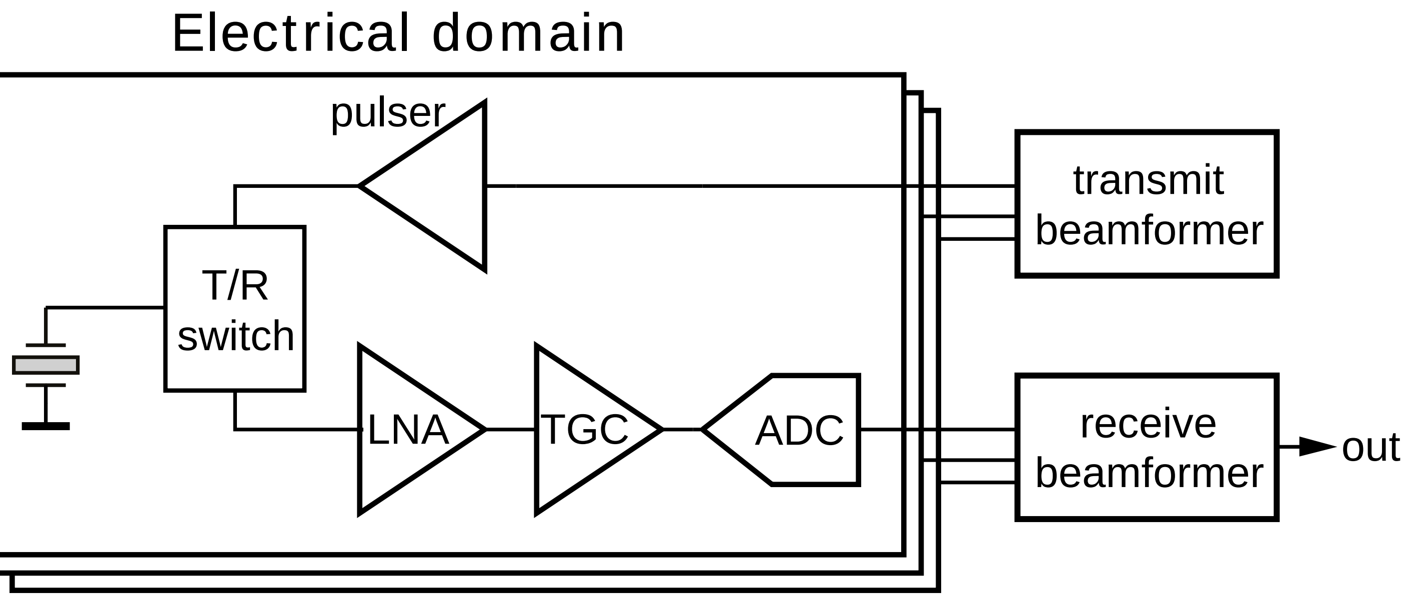
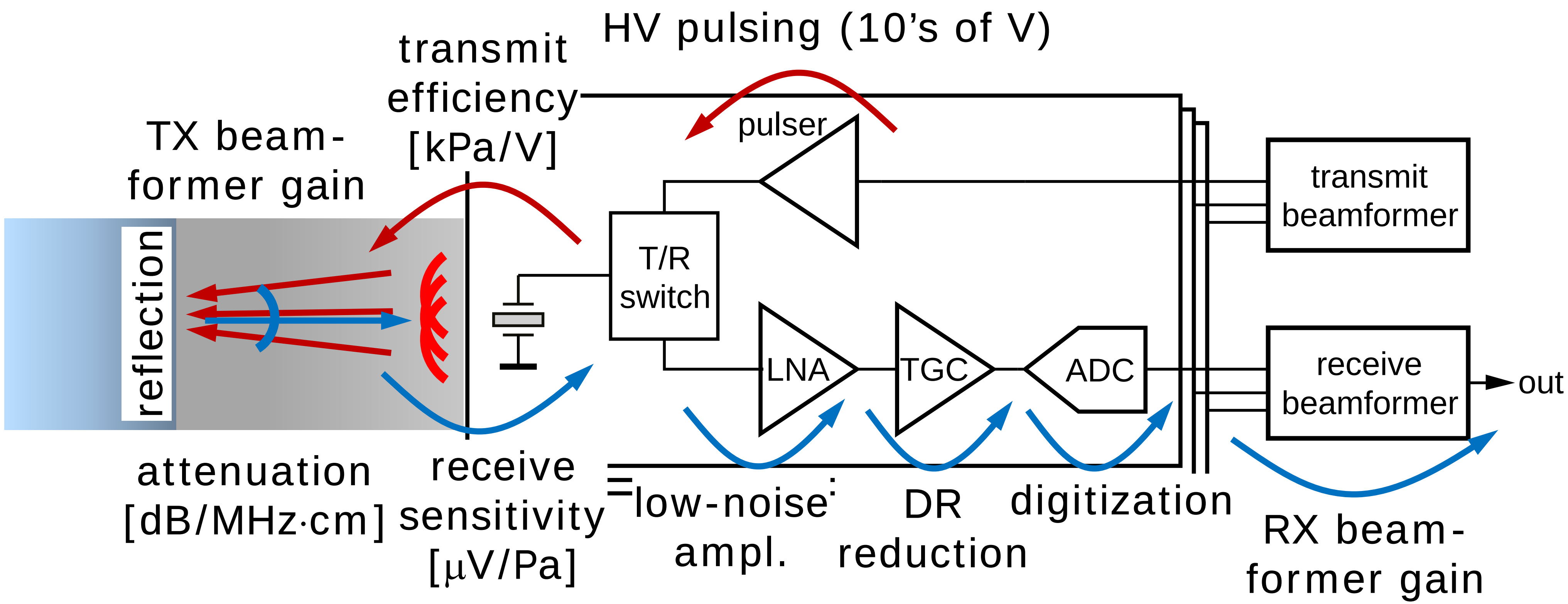
Ultrasound Front-End Circuits

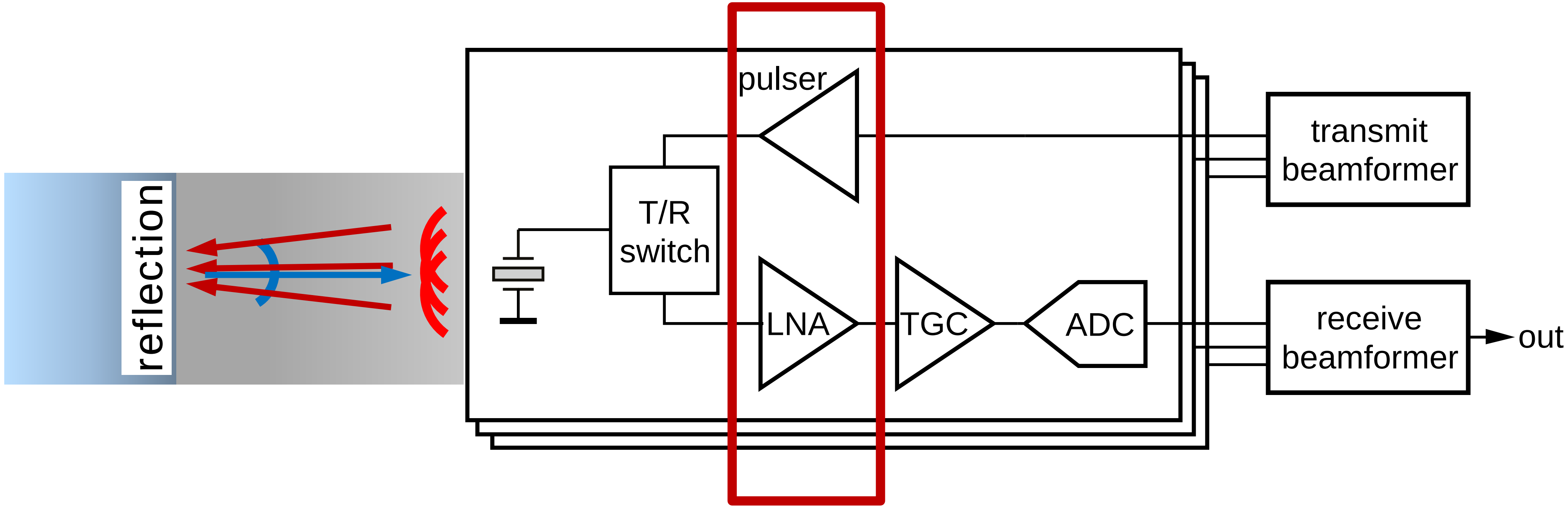


- Overall goal: achieve sufficient SNR_{out} at minimal power
- Signal: echo amplitude
- Noise: acoustic noise, transducer noise, electronics noise (thermal, quantization)
- Complex system optimization!

Ultrasound Front-End Circuits



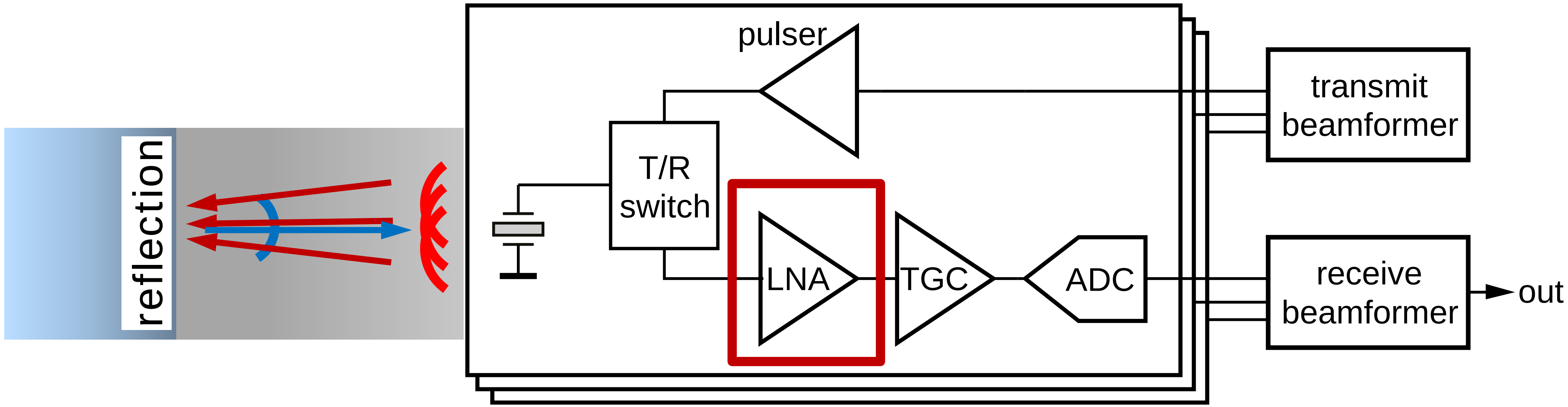
Ultrasound Front-End Circuits



tend to dominate
power consumption
and limit performance

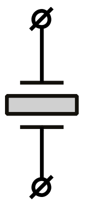
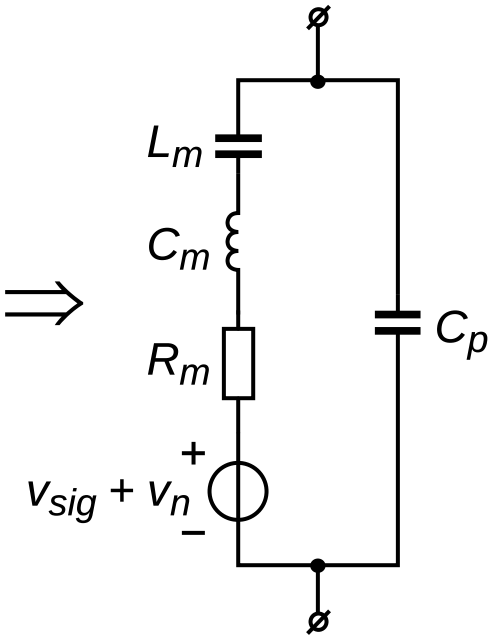
[Chen OJSSC’21]

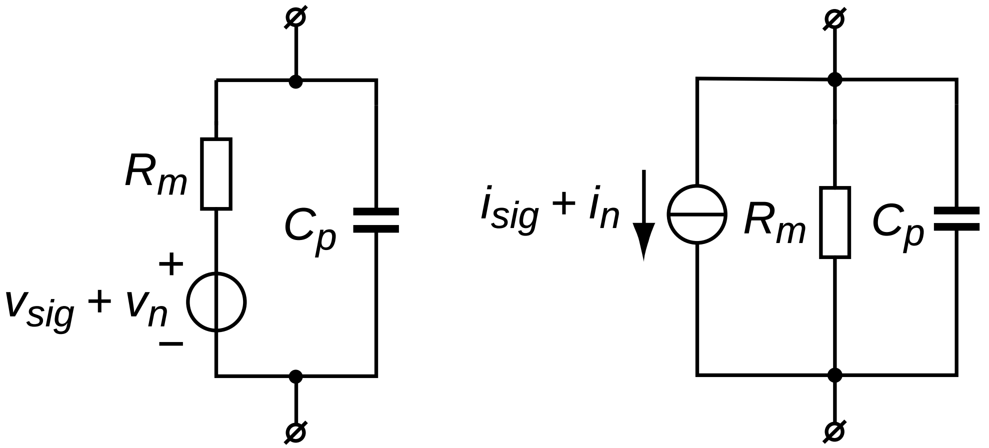
Low-noise amplifiers – requirements



- **Good noise figure**: noise < transducer noise (and uncorrelated between channels!)
- Sufficient **bandwidth**: > transducer bandwidth
- Sufficient **dynamic range:** handle nearby echoes (~V) up to deep echoes (~ µV)
  - Programmable gain, built-in TGC can help
- Price to pay: **power!**

Butterworth-Van Dyke model

transducer  ⇒ 

⇒ 

Butterworth-Van Dyke model

$$f_{res} = 1/2\pi\sqrt{L_m C_m}$$

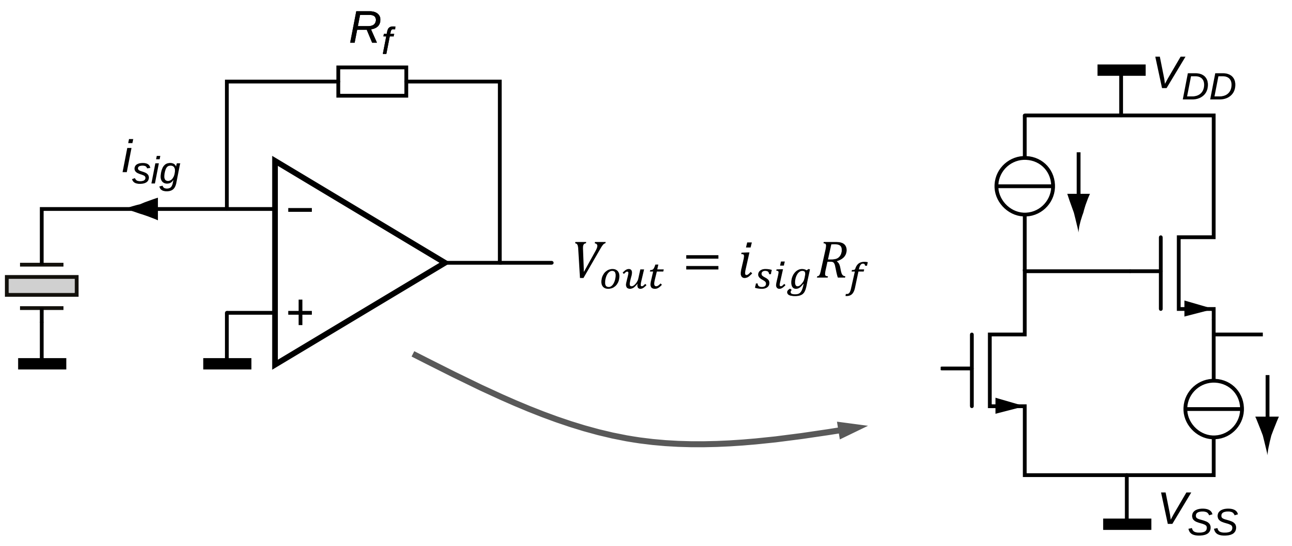
Equivalent models at resonance

Noise PSD: $\overline{v_n^2} = 4kTR_m$ [V^2 / Hz]

$\overline{i_n^2} = 4kT/R_m$ [A^2 / Hz]

Works for bulk piezo, CMUTs, PMUTs
(with different model parameters)

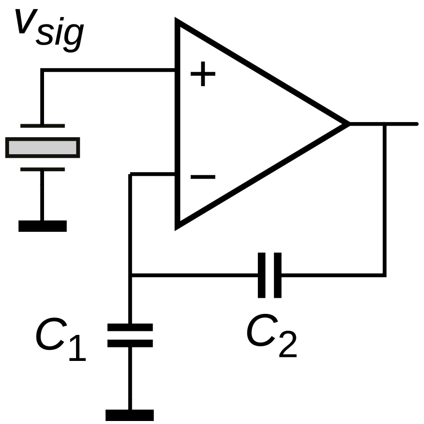
LNAs – transimpedance amplifiers



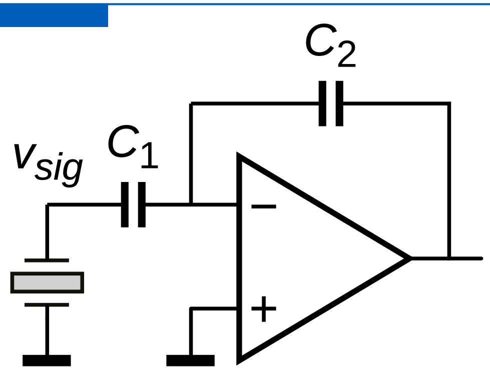
[Wygant TUFFC’09]
[Chen JSSC’13]
[Sautto ESSCIRC’14]

- Senses motional current (i_{sig}) of the transducer
- Power-efficient for relatively high-impedance transducers (e.g. CMUTs)

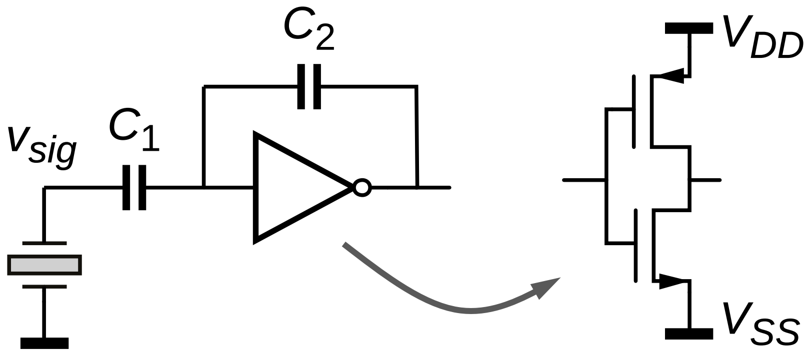
LNAs – voltage amplifiers



$$V_{out} = v_{sig}\frac{C_1 + C_2}{C_2}$$



$$V_{out} = -v_{sig}\frac{C_1}{C_2}$$

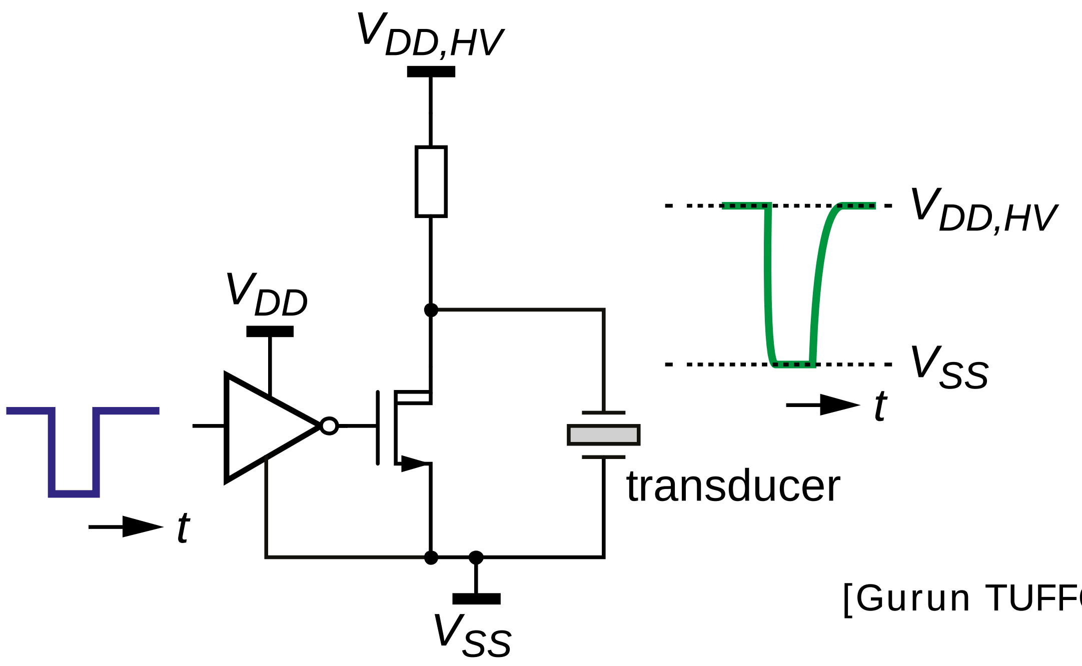


- Senses voltage across the transducer
- Power-efficient for relatively low-impedance transducers (e.g. bulk PZT)

[Chen ESSCIRC'15]

Transmit circuits – pulsers

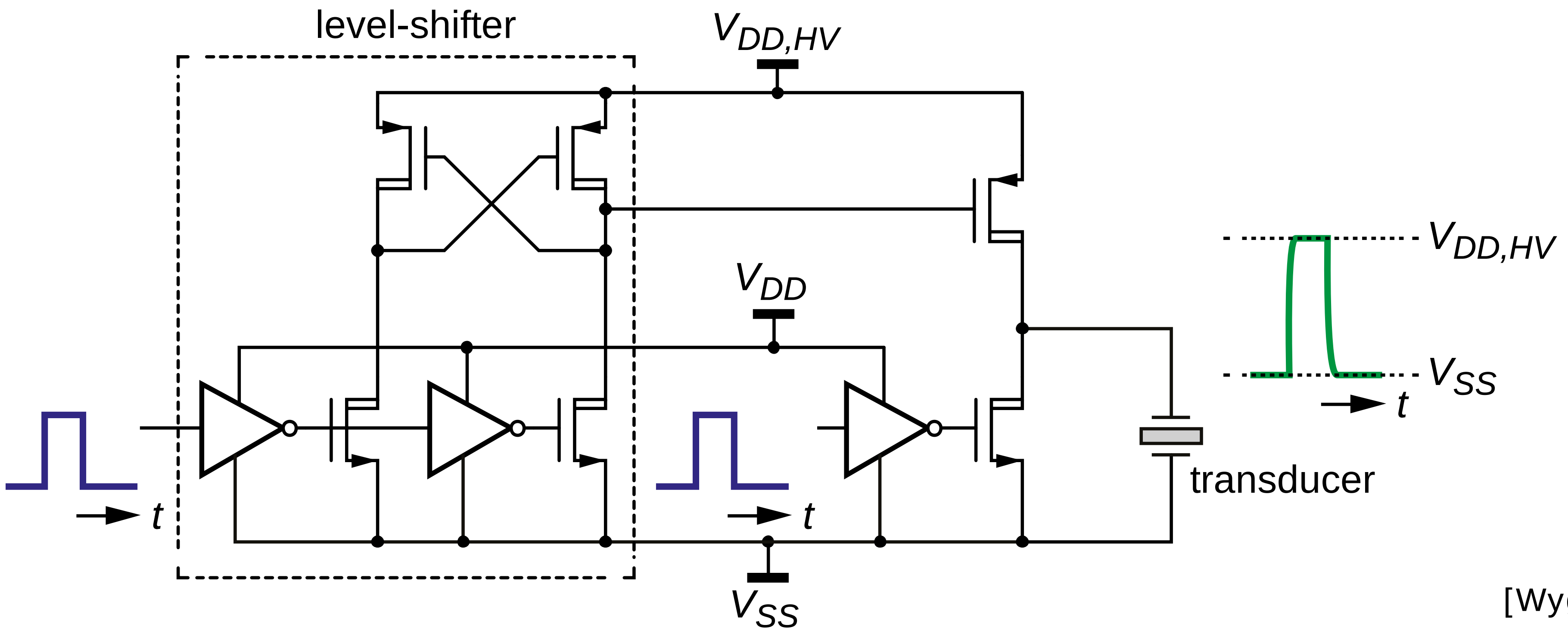
- Pulse voltage typically tens of V
  $\Rightarrow$ need HV CMOS process
- Excite transducer at resonance
  $\Rightarrow$ pulse width $t_{pulse} = 1/2f_{res}$
- Often sequence of multiple pulses at f_{res}
  - more pulses $\Rightarrow$ better SNR but poorer axial resolution



[Gurun TUFFC’14]

- Resistive pull-up is simple and compact, but power hungry

Transmit circuits – push-pull topology



[Wygant TUFFC'08]

- More efficient, but tends to require HV level-shifters
- Power limited by (dis)charging of transducer capacitance: $f_{PRF}CV^2$ [Tang TBioCAS'16]
- More efficient but also more complex: bipolar pulsers, multi-level pulsers

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- Sub-array beamforming
- In-probe digitization
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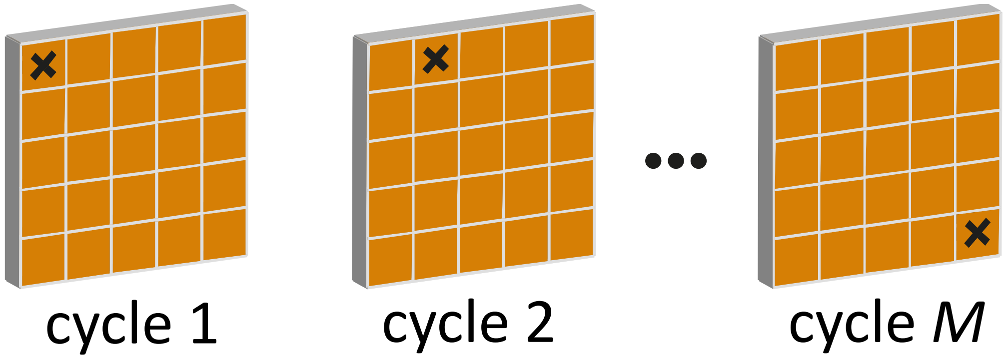
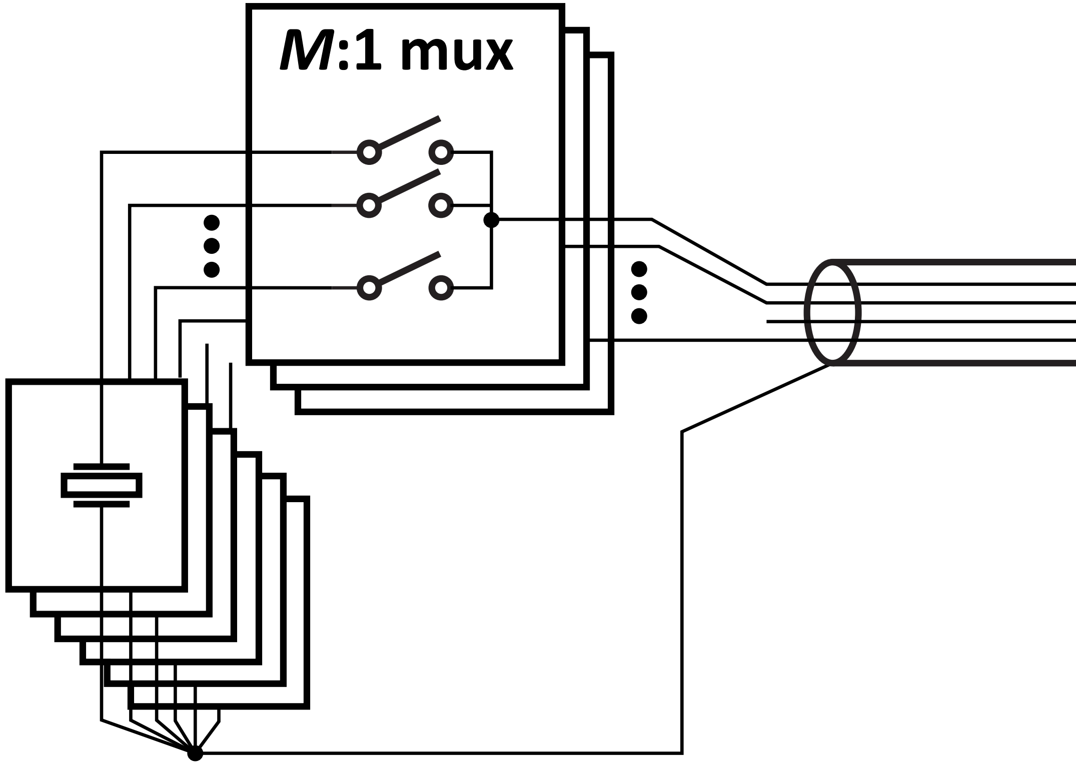
Reducing Channel Count: Multiplexing

- In-probe switches to connect *M* elements to one system channel
- *M*-fold cable-count reduction
- "Synthetic aperture" acquisition



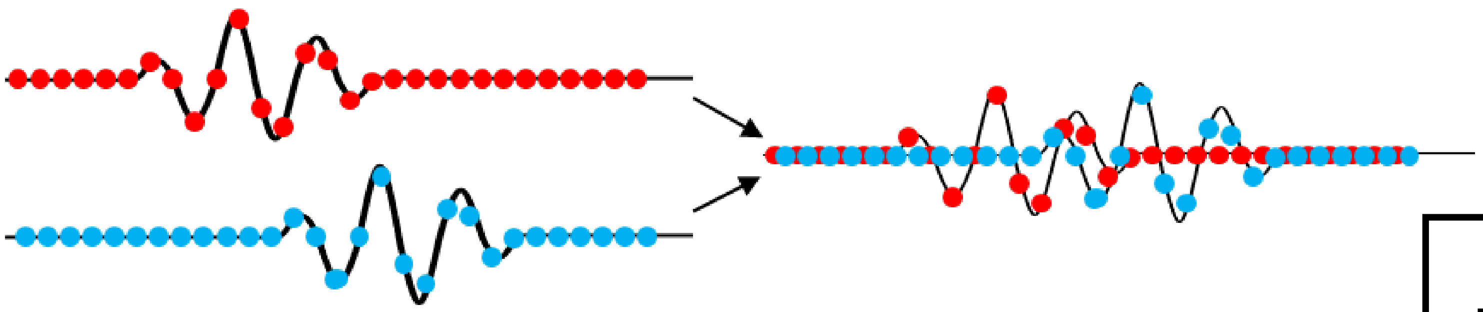


- Penalty: lower frame rate!

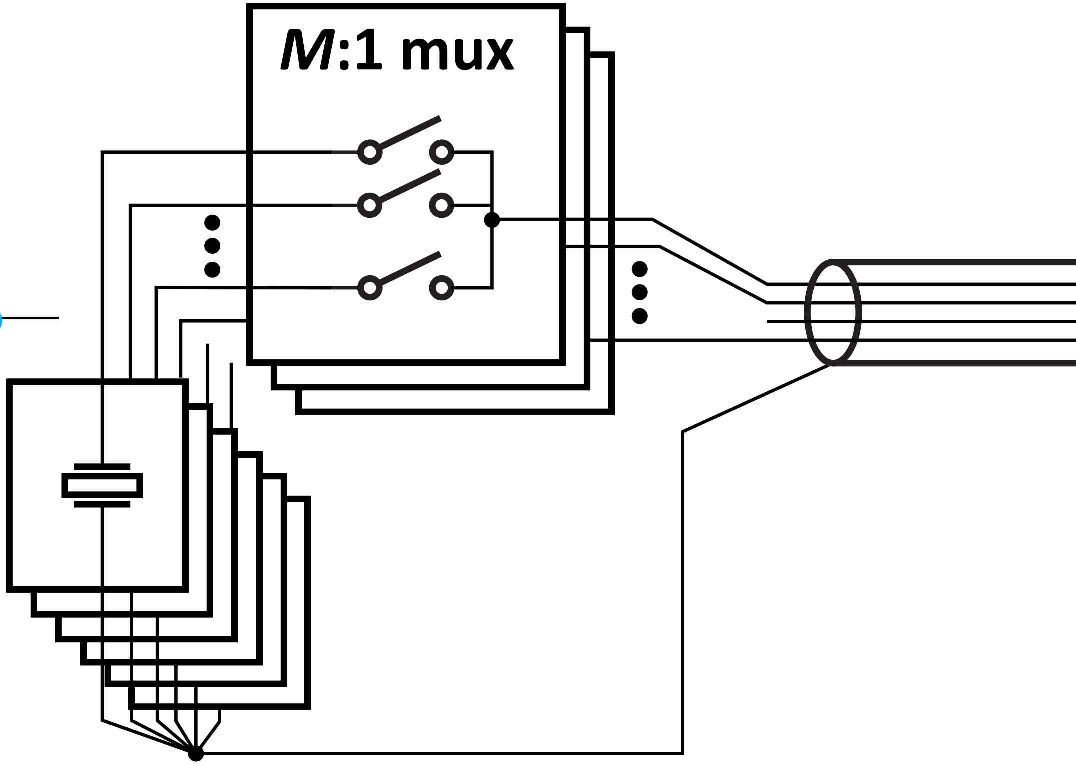
[Savord IUS'03 , Kim IUS'12, KChen JSSC'16, Carpenter TUFFC'16, Rezvanitabar TBCAS'22]

Reducing Channel Count: TDMA

- Time-Division Multiple Access:
  fast switching to time-interleave signals



- One channel acquires RF signals of multiple elements simultaneously
  → no framerate penalty!
- But: requires higher channel BW, introduces channel-to-channel crosstalk



[Carpenter TUFFC'16, Rezvanitabar TBCAS'22, Rozsa JSSC'25]

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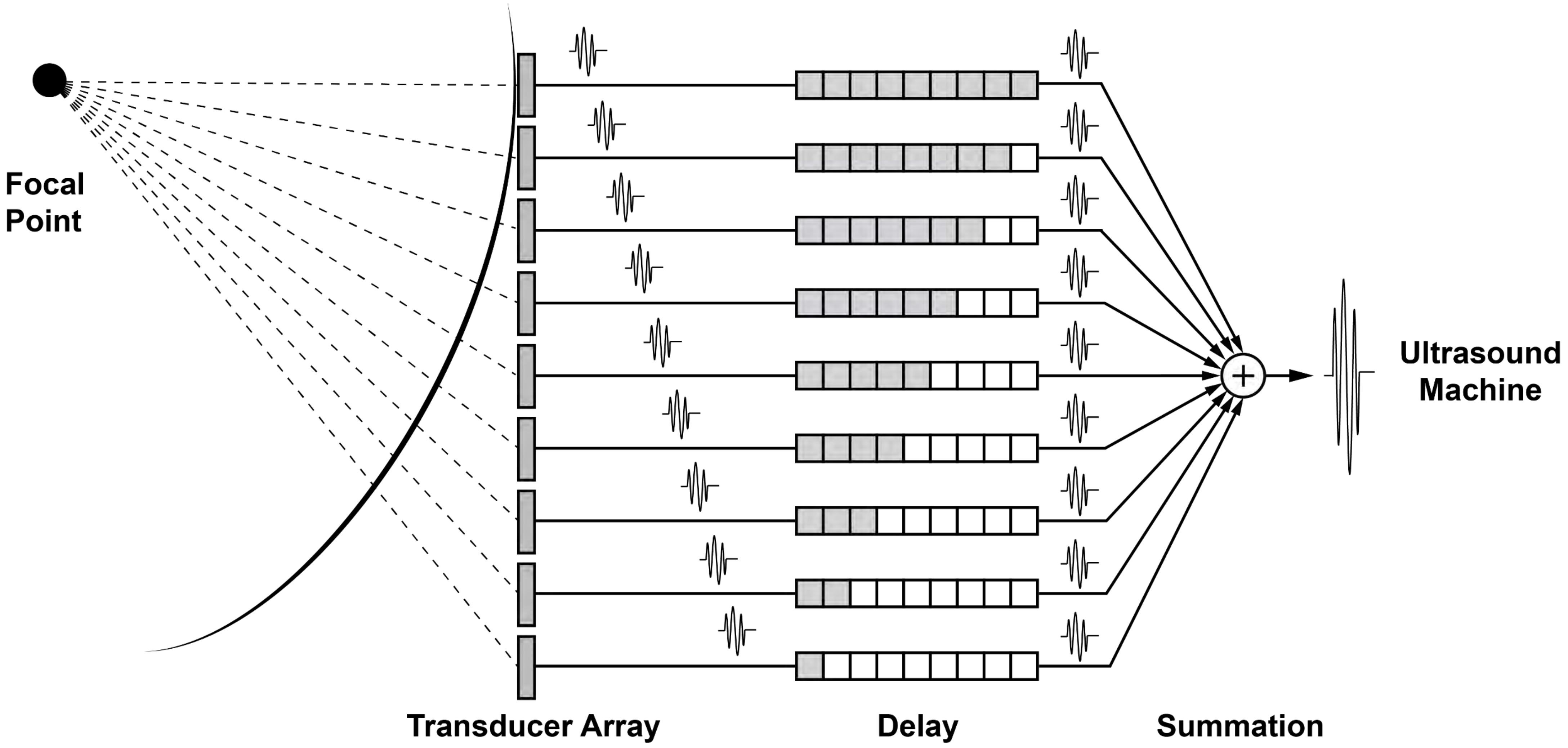
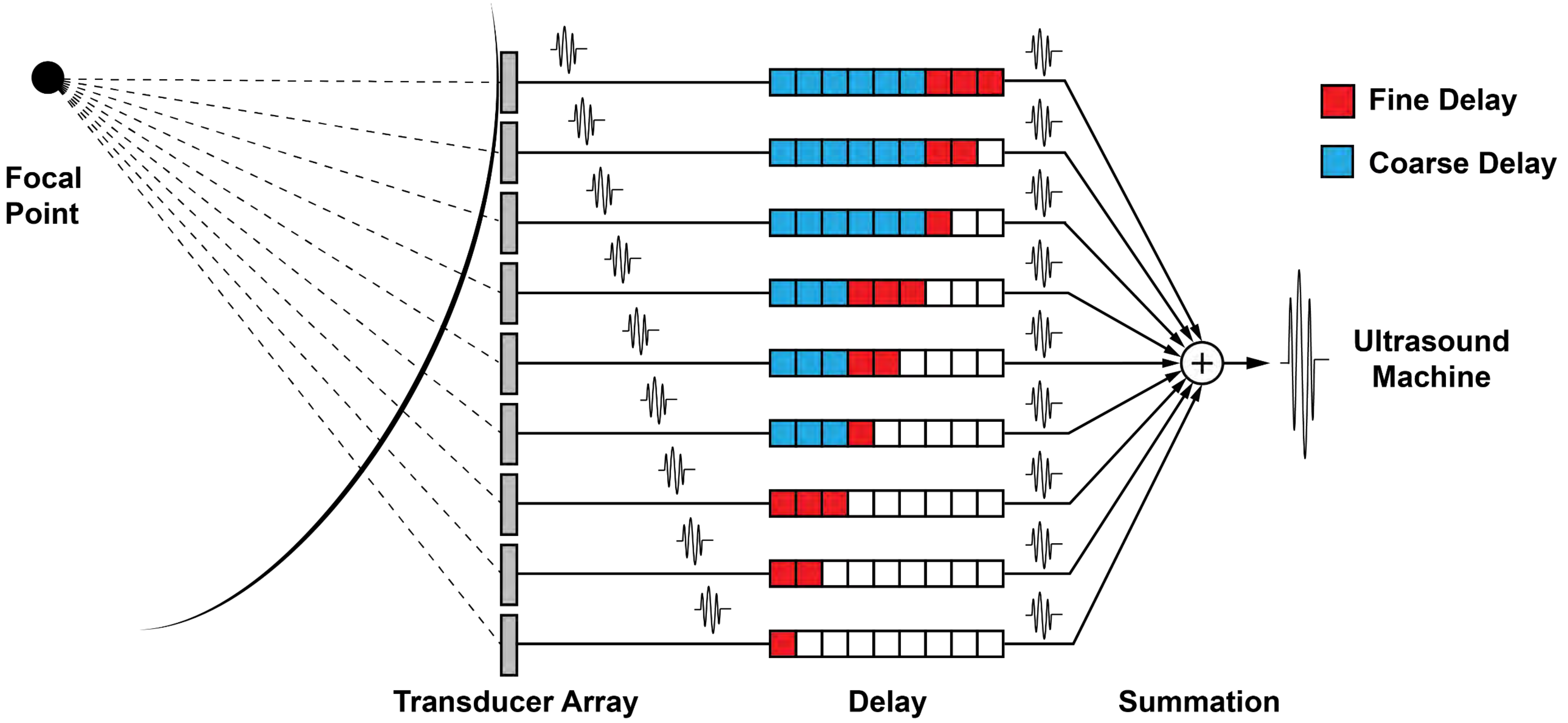
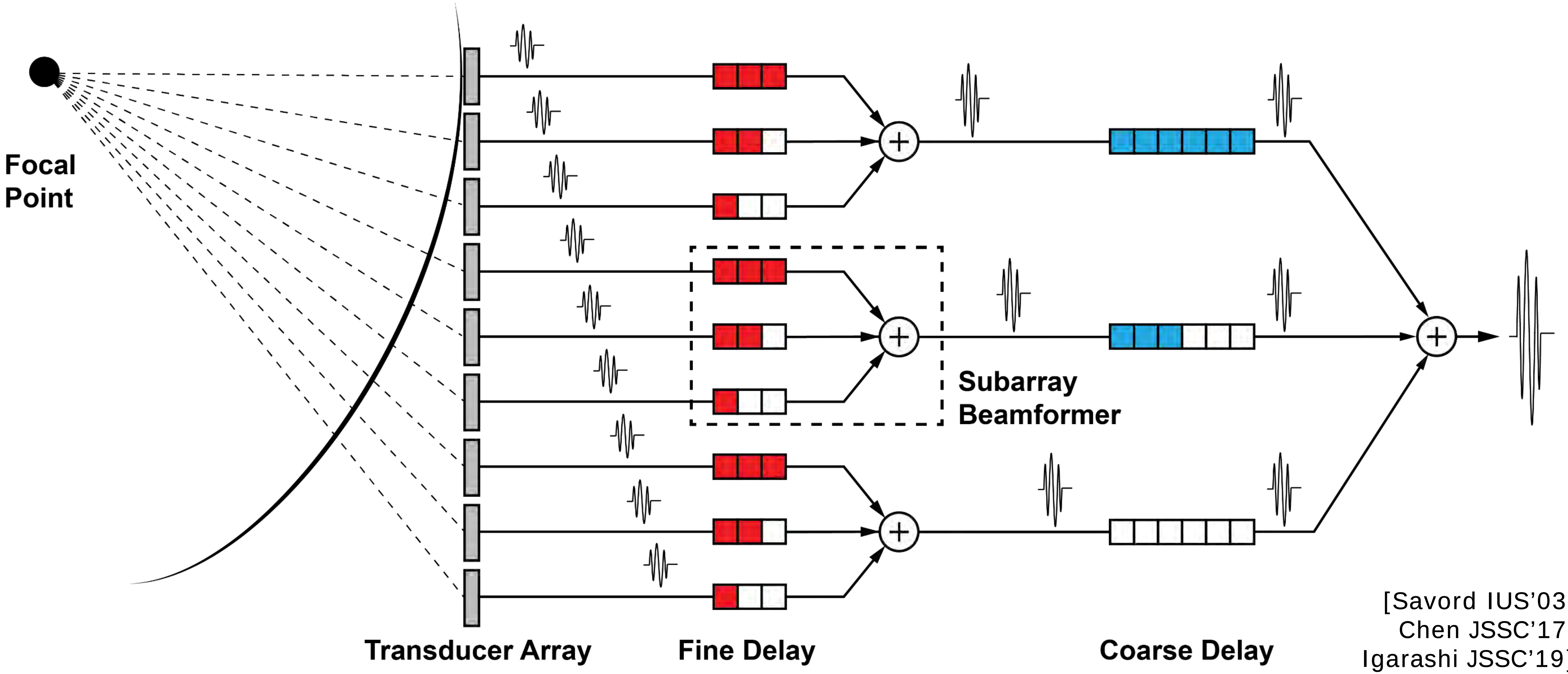
Sub-array Beamforming



Sub-array Beamforming

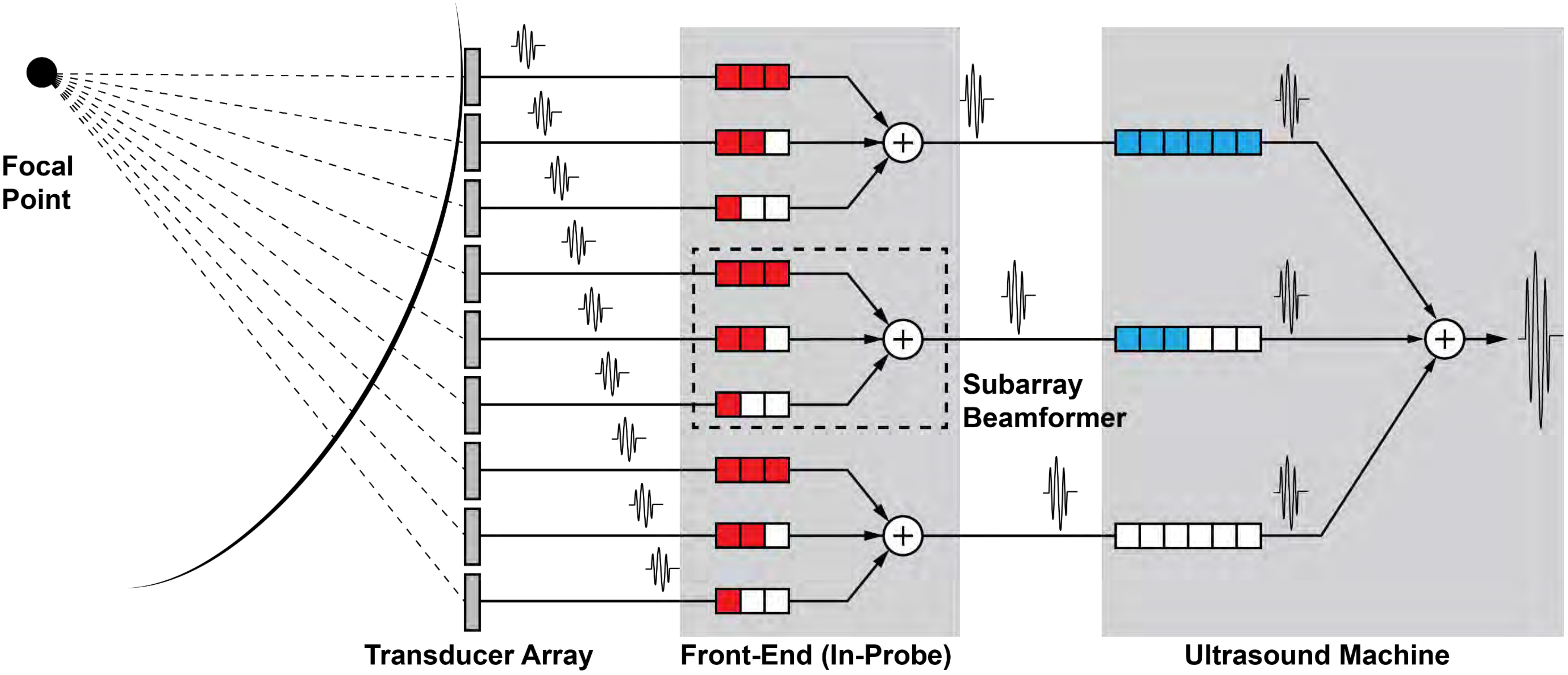


Sub-array Beamforming

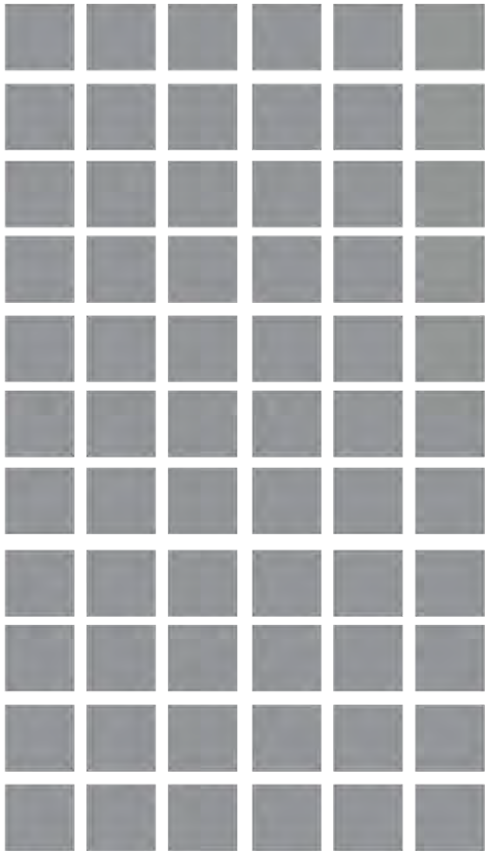


[Savord IUS'03, Chen JSSC'17, Igarashi JSSC'19]

Sub-array Beamforming

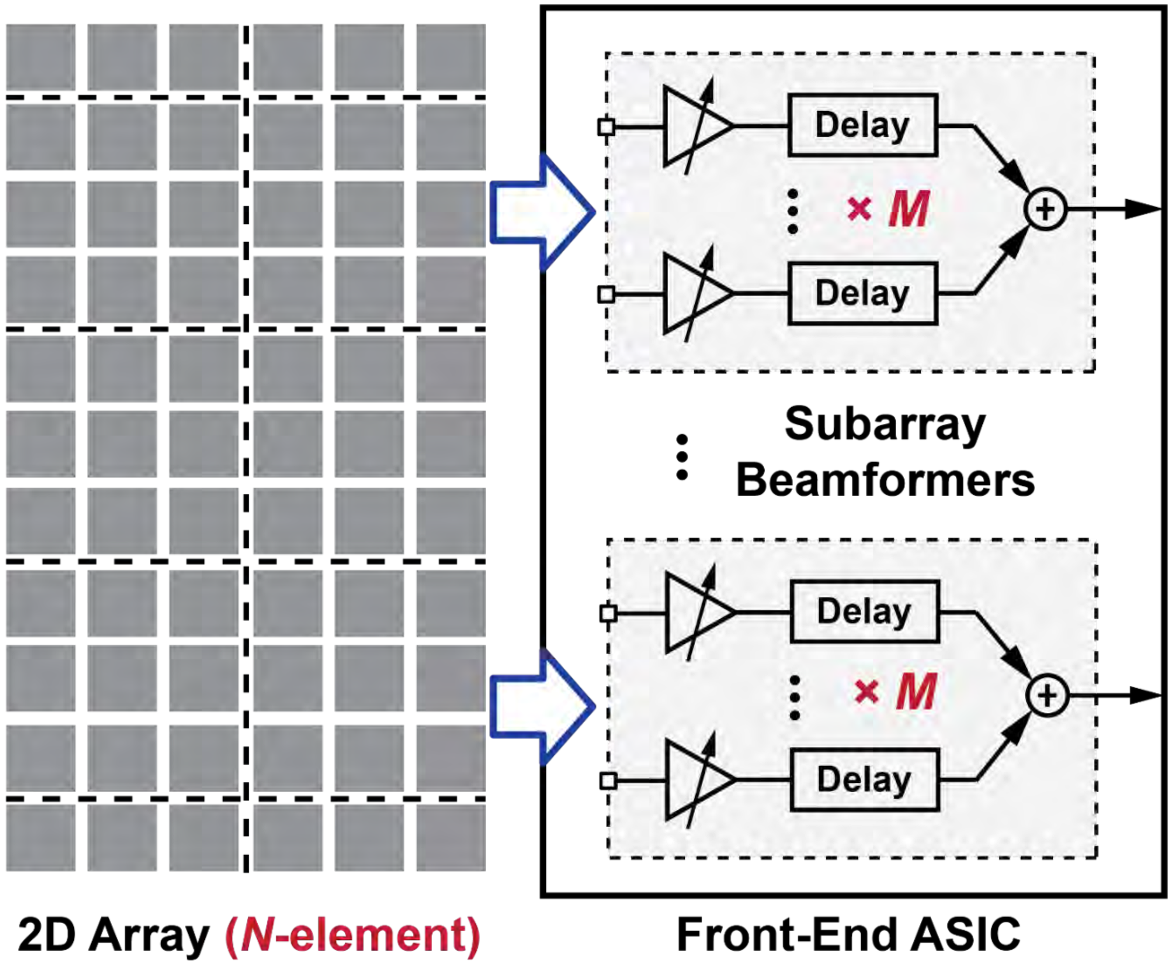


Sub-array Beamforming on a 2D Array

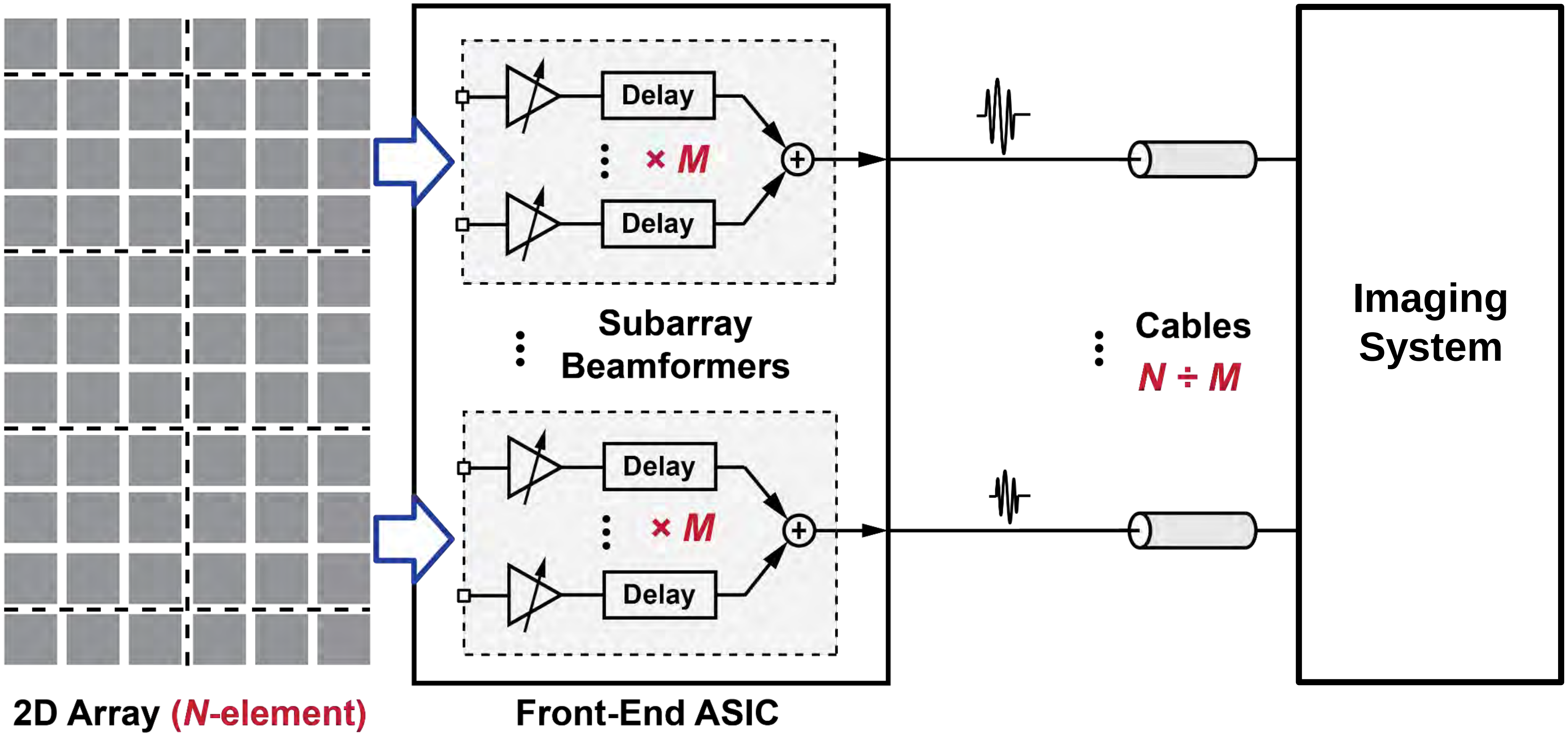


2D Array (*N*-element)

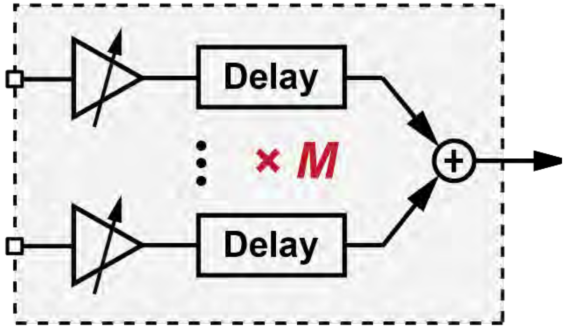
Sub-array Beamforming on a 2D Array

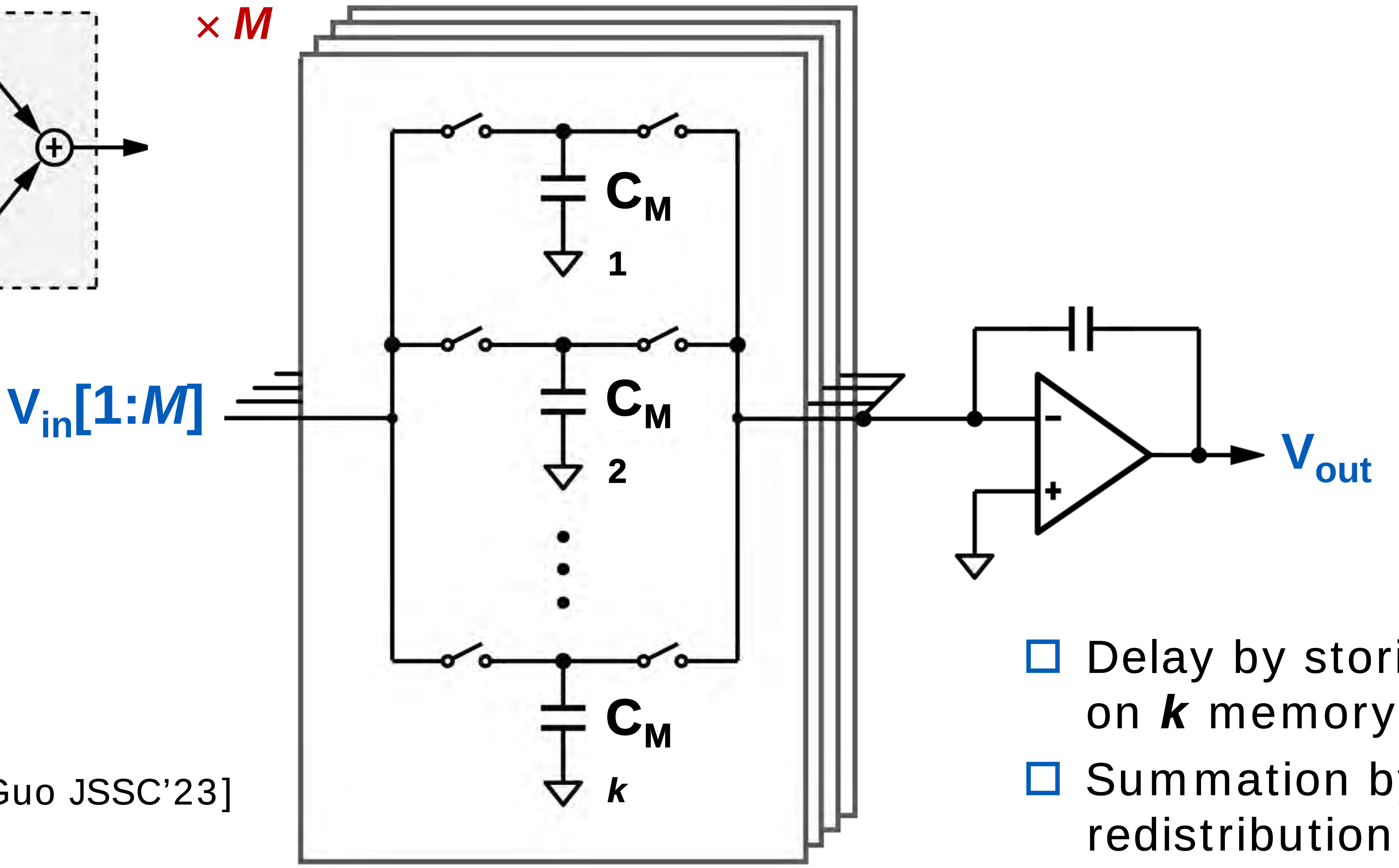


Sub-array Beamforming on a 2D Array



Analog Beamformer based on S&H delay lines





[Chen JSSC'17, Guo JSSC'23]

- Delay by storing input on ***k*** memory capacitors
- Summation by charge redistribution at the output

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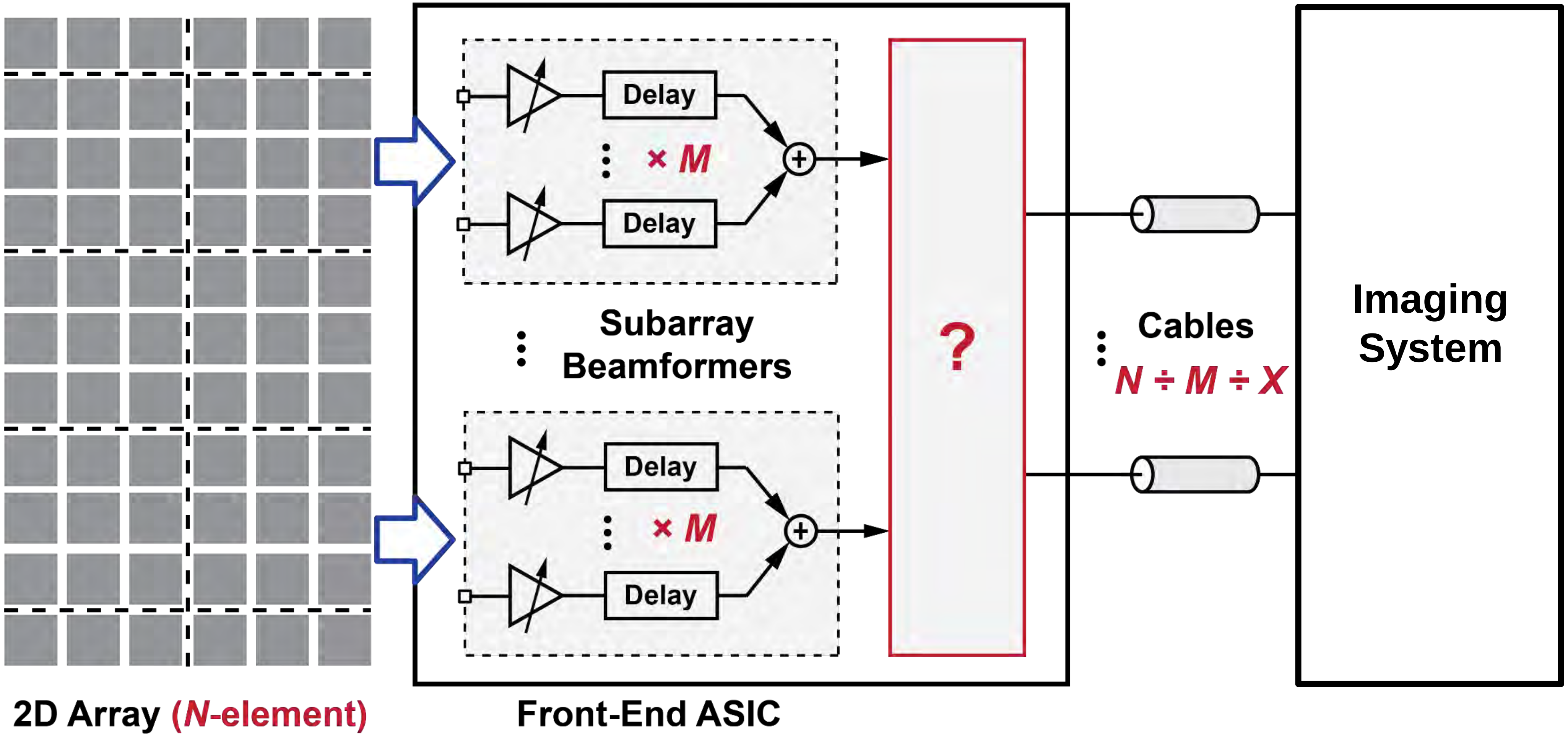
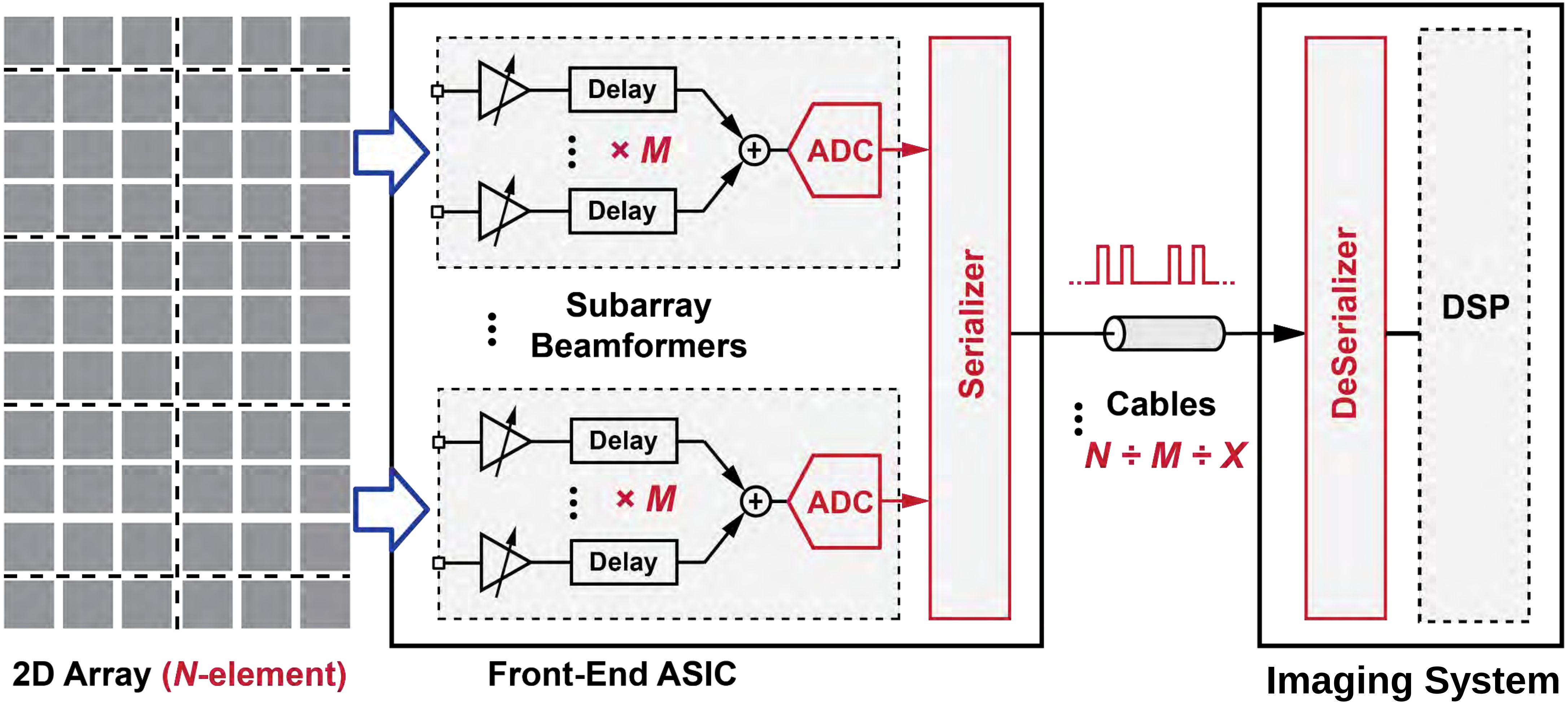
Further Channel Reduction?



Go Digital !



Delay
× M
Delay
ADC
Subarray
Beamformers
Delay
× M
Delay
ADC
Serializer
Cables
N ÷ M ÷ X
DeSerializer
DSP
2D Array (N-element)
Front-End ASIC
Imaging System

In-probe digitization

- Sampled >> Nyquist
  - Typically ≥ 4x transducer center frequency to enable accurate pulse timing
  - Jitter critical for Doppler imaging
- Resolution typically 8..14 bits
  - Quantization noise should be lower than AFE noise to prevent SNR degradation
  - PGA/TGC prior to ADC helps to reduce dynamic range
- Linearity / distortion not critical for fundamental imaging
  - Can be strongly relaxed compared to “conventional” ADCs [Radeljic-Jakic TUFFC’25]
- Various suitable architectures
  - Pipeline ADCs
  - Delta-sigma ADCs
  - SAR ADCs
  - Hybrids (e.g. SAR/slope, noise-shaping SAR)

Datalink

- Digitized data needs to be sent to imaging system
  - Data rates can be very high
  - Example: 40 Mb/s 10-bit ADC → 400 Mb/s per RX channel
  - Standards like LVDS, JESD204B allow directly interfacing to FPGAs, but can be power hungry
- Custom designs, like load-modulation and multi-level signalling, can strongly reduce power
  - Can benefit from the high bit-error tolerance of ultrasound signals
  - BER up to 10^{-4} can be tolerated
  - >10x less power than LVDS

[Hopf JSSC'23, Guo JSSC'24]

[Chen TUFFC'20]

Conclusions and Outlook

- **In-probe electronics** are key for advanced ultrasound probes
  - Provide SNR improvement
  - Channel-count reduction $\rightarrow$ enable 3D probes
- **In-probe digitization** is the next step
  - Further cable count reduction using high-speed digital data links
  - Enabler for in-probe data processing / compression
  - Key for point-of-care and wearable devices
- **Key challenges**: size, power consumption, data rate
  - Order-of-magnitude gaps to be bridged to make ultrasound wearable
- Solutions lie in **new architectures** and transducer-circuit-system **co-design**

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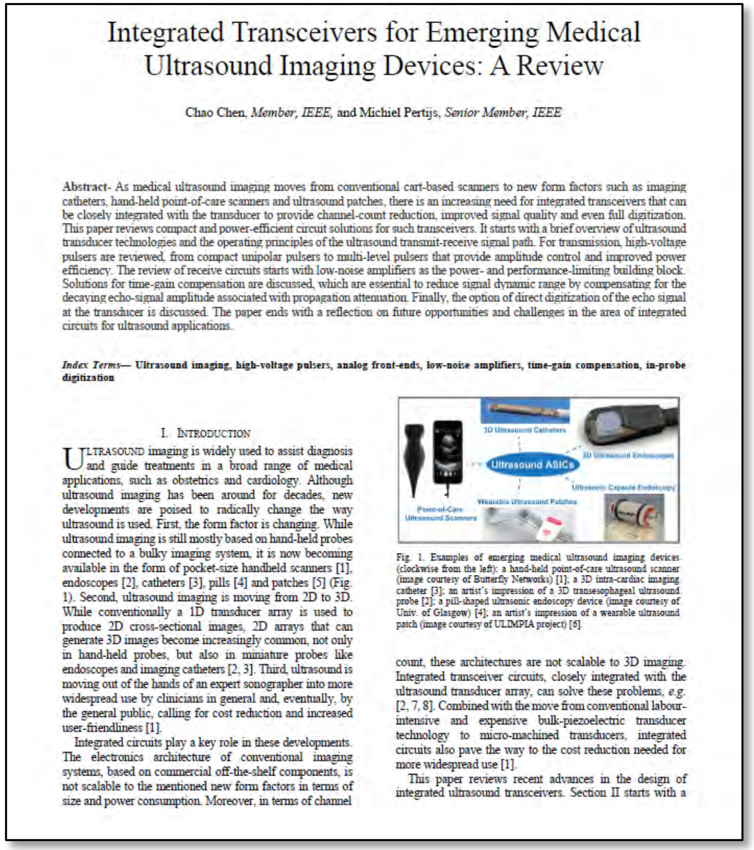

Integrated Transceivers for Emerging Medical Ultrasound Imaging Devices: A Review

Chao Chen, *Member, IEEE,* and Michiel Pertijs, *Senior Member, IEEE*

Abstract- As medical ultrasound imaging moves from conventional cart-based scanners to new form factors such as imaging catheters, hand-held point-of-care scanners and ultrasound patches, there is an increasing need for integrated transceivers that can be closely integrated with the transducer to provide channel-count reduction, improved signal quality and even full digitization. This paper reviews compact and power-efficient circuit solutions for such transceivers. It starts with a brief overview of ultrasound transducer technologies and the operating principles of the ultrasound transmit-receive signal path. For transmission, high-voltage pulsers are reviewed, from compact unipolar pulsers to multi-level pulsers that provide amplitude control and improved power efficiency. The review of receive circuits starts with low-noise amplifiers as the power- and performance-limiting building block. Solutions for time-gain compensation are discussed, which are essential to reduce signal dynamic range by compensating for the decaying echo-signal amplitude associated with propagation attenuation. Finally, the option of direct digitization of the echo signal at the transducer is discussed. The paper ends with a reflection on future opportunities and challenges in the area of integrated circuits for ultrasound applications.

Index Terms— **Ultrasound imaging, high-voltage pulsers, analog front-ends, low-noise amplifiers, time-gain compensation, in-probe digitization**

I. INTRODUCTION

ULTRASOUND imaging is widely used to assist diagnosis and guide treatments in a broad range of medical applications, such as obstetrics and cardiology. Although ultrasound imaging has been around for decades, new developments are poised to radically change the way ultrasound is used. First, the form factor is changing. While ultrasound imaging is still mostly based on hand-held probes connected to a bulky imaging system, it is now becoming available in the form of pocket-size handheld scanners [1], endoscopes [2], catheters [3], pills [4] and patches [5] (Fig. 1). Second, ultrasound imaging is moving from 2D to 3D. While conventionally a 1D transducer array is used to produce 2D cross-sectional images, 2D arrays that can generate 3D images become increasingly common, not only in hand-held probes, but also in miniature probes like endoscopes and imaging catheters [2, 3]. Third, ultrasound is moving out of the hands of an expert sonographer into more widespread use by clinicians in general and, eventually, by the general public, calling for cost reduction and increased user-friendliness [1].

Integrated circuits play a key role in these developments. The electronics architecture of conventional imaging systems, based on commercial off-the-shelf components, is not scalable to the mentioned new form factors in terms of size and power consumption. Moreover, in terms of channel count, these architectures are not scalable to 3D imaging. Integrated transceiver circuits, closely integrated with the ultrasound transducer array, can solve these problems, *e.g.* [2, 7, 8]. Combined with the move from conventional labour-intensive and expensive bulk-piezoelectric transducer technology to micro-machined transducers, integrated circuits also pave the way to the cost reduction needed for more widespread use [1].

This paper reviews recent advances in the design of integrated ultrasound transceivers. Section II starts with a

Fig. 1. Examples of emerging medical ultrasound imaging devices (clockwise from the left): a hand-held point-of-care ultrasound scanner (image courtesy of Butterfly Networks) [1]; a 3D intra-cardiac imaging catheter [3]; an artist's impression of a 3D transesophageal ultrasound probe [2]; a pill-shaped ultrasonic endoscopy device (image courtesy of Univ. of Glasgow) [4]; an artist's impression of a wearable ultrasound patch (image courtesy of ULIMPIA project) [6].

Further reading?

See our open-access review paper in the *IEEE Open Journal of the Solid-State Circuits Society*

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