



## **Ultrasound system design: Analog front end circuits, in-probe electronics and imaging systems**

15<sup>th</sup> September 2025

**<https://github.com/dcowell/IUS2025-UltrasoundSystemDesign>**

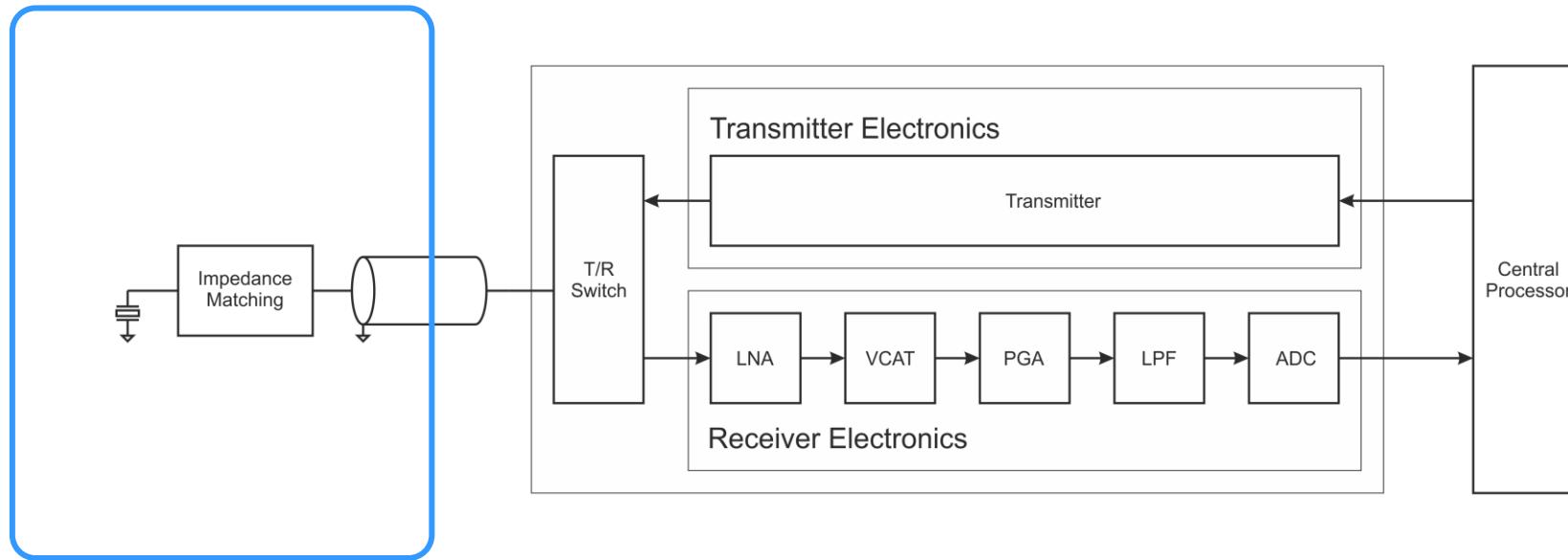
**David Cowell**, School of Electronic and Electrical Engineering, University of Leeds, UK

**Enrico Boni**, Department of Information Engineering, University of Florence, Italy

**Michiel Pertijs**, Electronic Instrumentation Laboratory, Delft University of Technology, The Netherlands

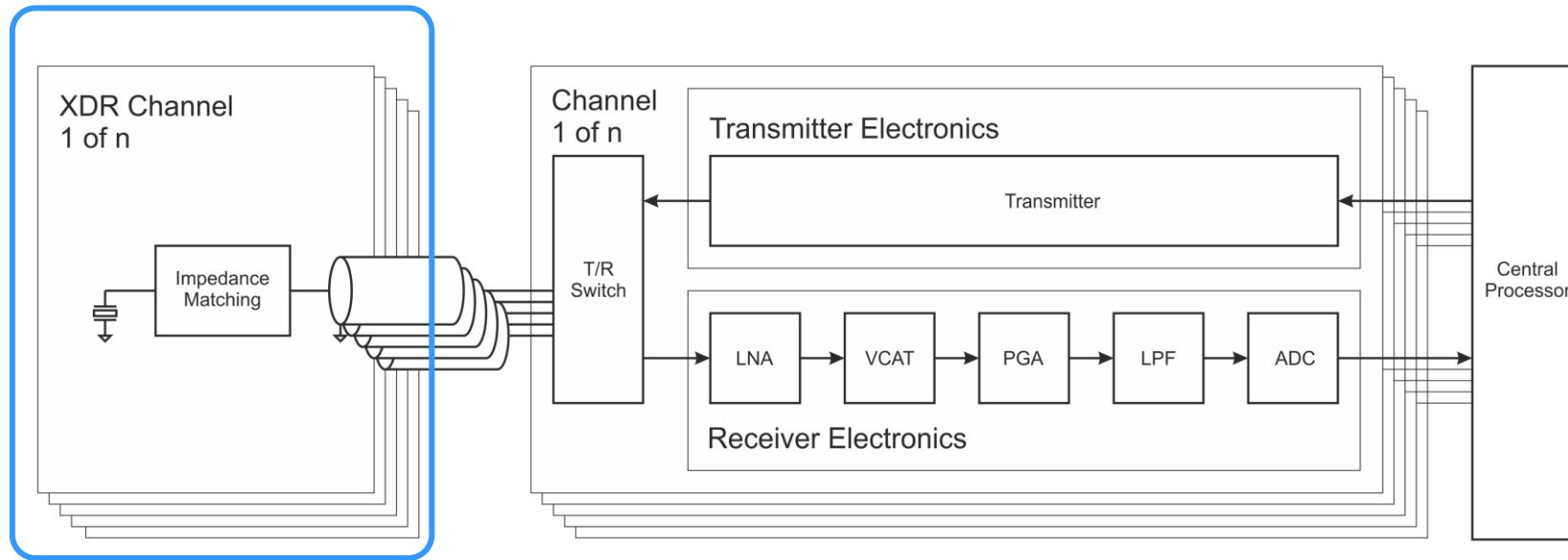
# Electronics Overview

## Transducer



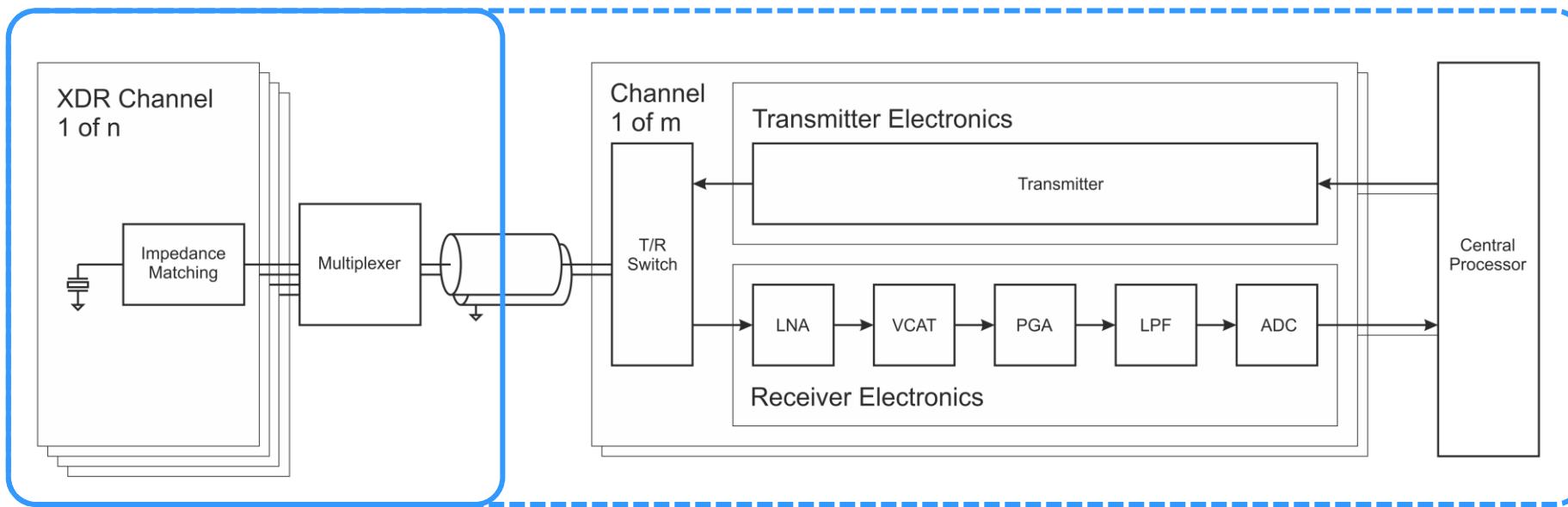
# Electronics Overview

## Transducer



# Electronics Overview

## Transducer



# Impedance, Resistance and Reactance

Acoustic Impedance =  $\frac{\text{Pressure}}{\text{Velocity}}$

$$Z = \frac{p}{v}$$

$$Z = R + jX$$

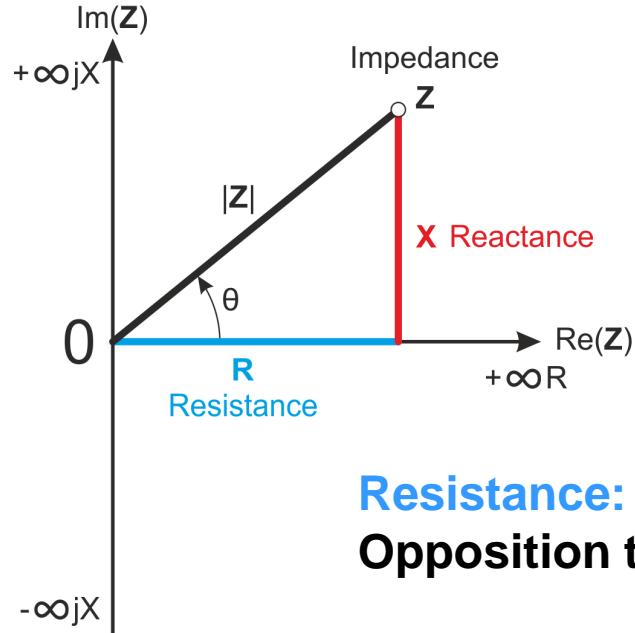
$$|Z| = \sqrt{R^2 + X^2}$$

$$\theta = \tan^{-1} \left( \frac{X}{R} \right)$$

versus

Electrical Impedance =  $\frac{\text{Voltage}}{\text{Current}}$

$$Z = \frac{V}{I}$$



**Reactance:**  
**Opposition to the change**  
**of electric current**

**Resistance:**  
**Opposition to the passage** of electric current

# Impedance and Admittance of Ideal Lumped Components



**Resistor**

**Impedance**

**Z**

$$Z = R$$

**Admittance**

$$Y = \frac{1}{Z}$$

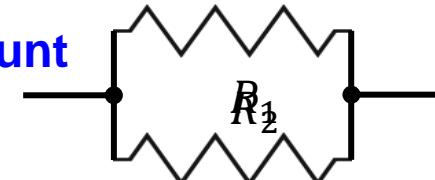
$$Y = \frac{1}{R}$$

**Series**



$$R_T = R_1 + R_2$$

**Parallel / Shunt**



$$\frac{1}{R_T} = \frac{1}{R_1} + \frac{1}{R_2}$$

$$Y_T = Y_1 + Y_2$$

# Impedance and Admittance of Ideal Lumped Components

## Impedance

$Z$



**Resistor**

$$Z = R$$



**Inductor**

$$Z = j\omega L$$



**Capacitor**

$$Z = \frac{1}{j\omega C} = \frac{-j}{\omega C}$$

## Admittance

$$Y = \frac{1}{Z}$$

$$Y = \frac{1}{R}$$

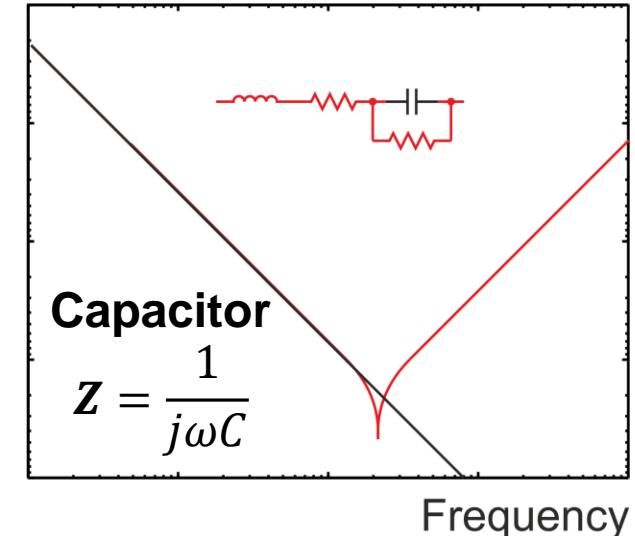
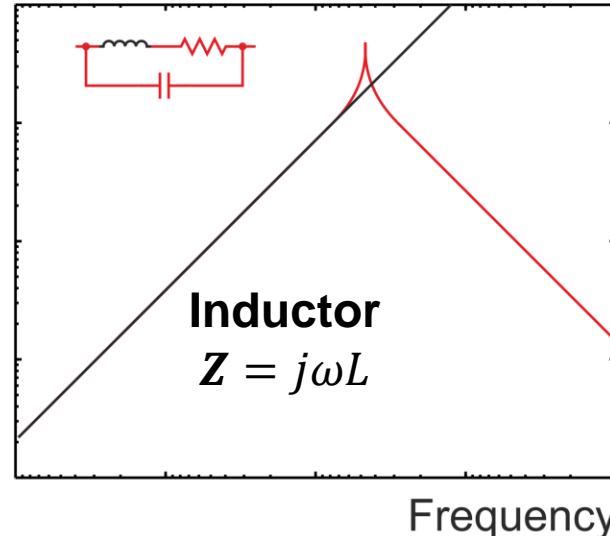
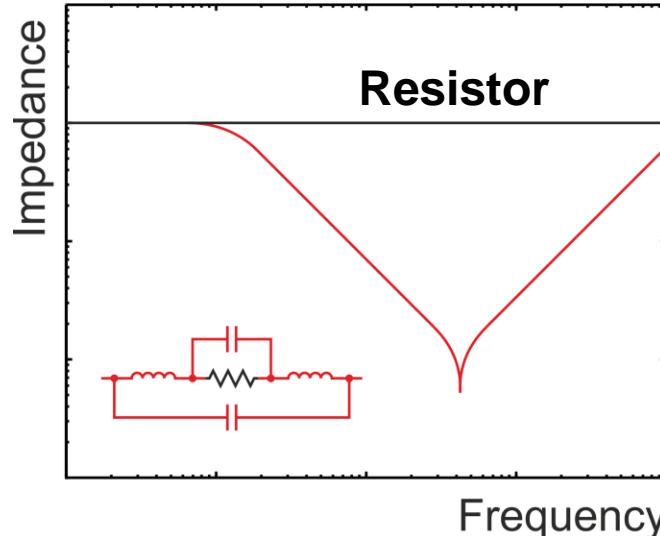
$$Y = \frac{1}{j\omega L} = \frac{-j}{\omega L}$$

$$Y = j\omega C$$

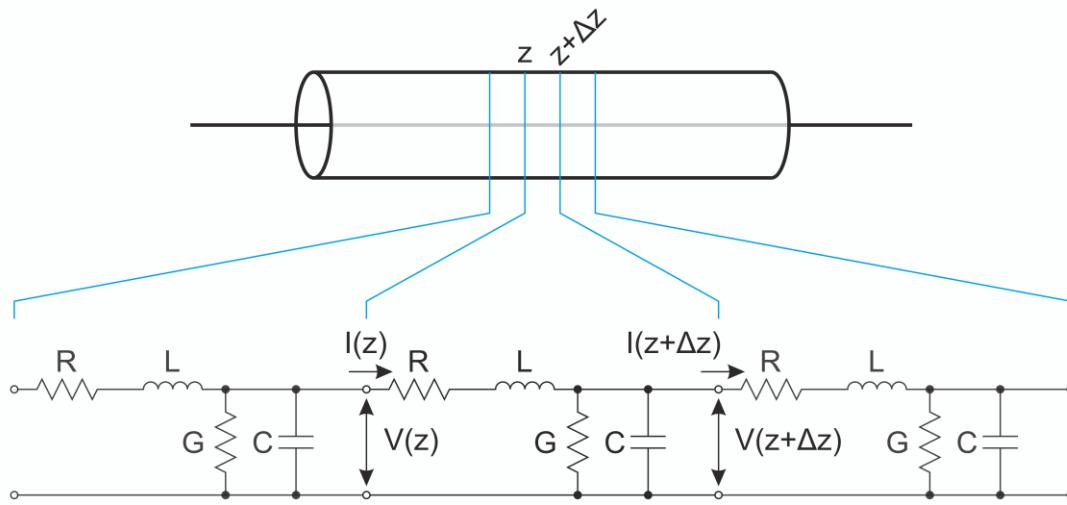
# Impedance of Real Lumped Components

- Real components have parasitic effects from leads or terminals and internal construction etc.
- Parasitic effects can be reduced by selecting small component package size.
- Parasitic effects high frequencies i.e. MHz region - specific high frequency components.
- Parasitic effects will alter matching circuits or filters designs from specification.
  - Always simulate circuits with actual component models not ideal models.

Ideal (black) and typical real response (red) for R, L, & C's.



# Micro-coaxial cable



$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$



- Increase characteristic impedance – decrease capacitance
  - $50\Omega - 110 \text{ pF/m}$ ,  $60\Omega - 90 \text{ pF/m}$ ,  $75\Omega - 60 \text{ pF/m}$ ,  $85\Omega - 50 \text{ pF/m}$ .
- Typical one way signal attenuation  $\sim 0.1 \text{ dB/foot}$  ( $< 10 \text{ MHz}$ )
- Application will define the coaxial cable.
- Coaxial cable will define the characteristic impedance.
- Measure cable frequency dependent characteristics on a network or impedance analyser.
- Mechanical damage (twisting, kinking etc) will cause an impedance mismatch and degrade signal.

# Why is Characteristic Impedance so important?

Acoustic impedance  
Reflection Coefficient

$$R_p = \frac{Z_{o2} - Z_{o1}}{Z_{o2} + Z_{o1}}$$

Electrical impedance  
Voltage Reflection Coefficient

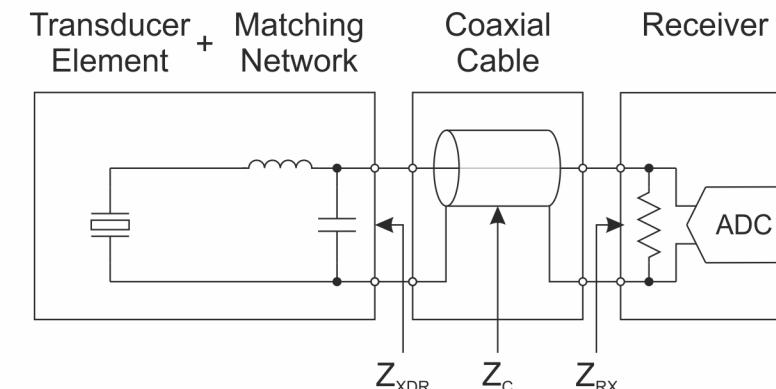
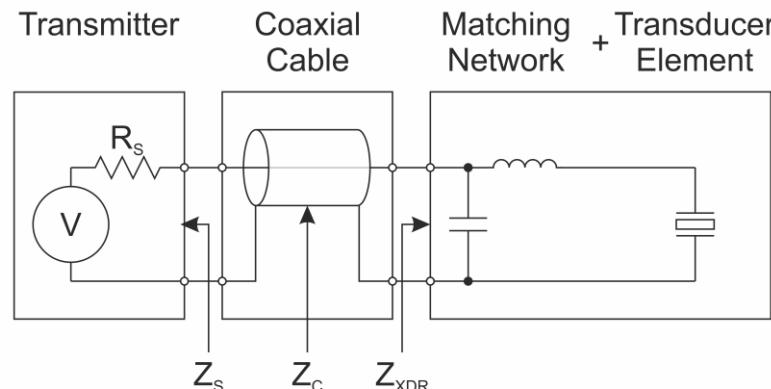
$$\Gamma_{12} = \frac{Z_2 - Z_1}{Z_2 + Z_1}$$

To minimize reflection and maximize transmission...

**Minimize Impedance Mismatch!**  
**Result? – Improved SNR**

# Impedance Matching

- $Z_s$  and  $Z_c$  equal to Characteristic Impedance
- $Z_{ELEMENT}$  not equal to Characteristic Impedance
- Adding a Matching Network of passive components between the coaxial cable and the transducer element allows impedance transformation
- When  $Z_s = Z_c = Z_{XDR}$ 
  - Maximum transmission of energy from transmitter to transducer
- When  $Z_{XDR} = Z_c = Z_{RX}$ 
  - Maximum transmission of energy from transducer to receiver



# Noise Factor and Noise Figure

*Noise Factor is noise added by a component!*

## Noise Factor

$$F = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}}$$

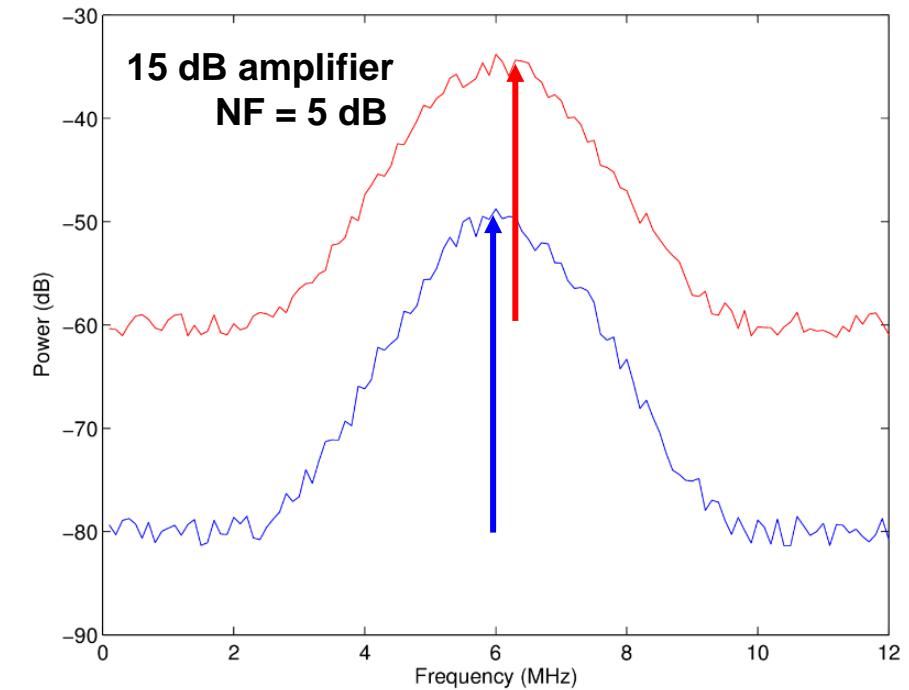
## Noise Figure

$$\text{NF} = 10 \log F$$

$$\text{NF} = \text{SNR}_{\text{in},\text{dB}} - \text{SNR}_{\text{out},\text{dB}}$$

$$\text{NF} = (-50 - -80) - (-35 - -60)$$

$$\text{NF} = 30 - 25 = 5 \text{ dB}$$



- **Friis' Formula**  $F = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1 G_2} + \frac{F_4-1}{G_1 G_2 G_3} + \dots + \frac{F_n-1}{G_1 G_2 G_3 \dots G_{n-1}}$

where **F** is Noise Factor and **G** is Power Gain (both linear units)

- The first component,  $F_1$ , has the most significant effect in a chain.
  - Effort should be paid to improving input SNR and reducing the Noise Figure of the first component.

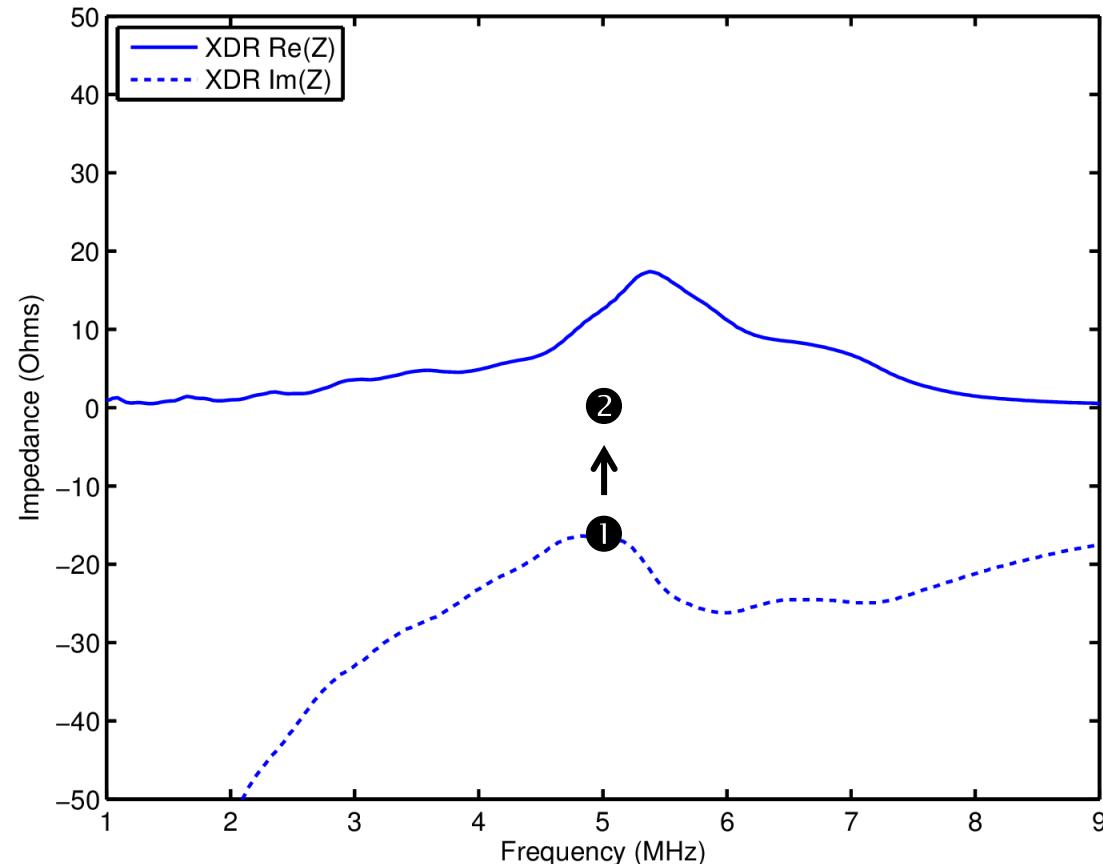
# Single component Impedance Matching

Aim

With a single component reduce reactance to zero at 5 MHz  
Calculate required change in reactance from ① to ② -j16.6 Ω to j0Ω

Real ——————

Resistive  $Z = R$



Imaginary -----

Inductive  $Z = j\omega L$

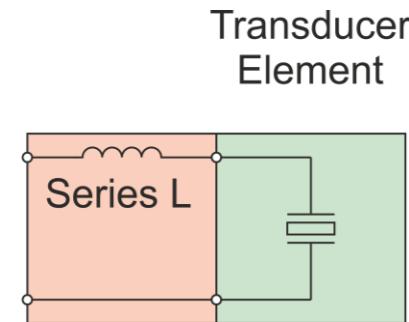
Capacitive  $Z = \frac{1}{j\omega C} = \frac{-j}{\omega C}$

# Single component Impedance Matching

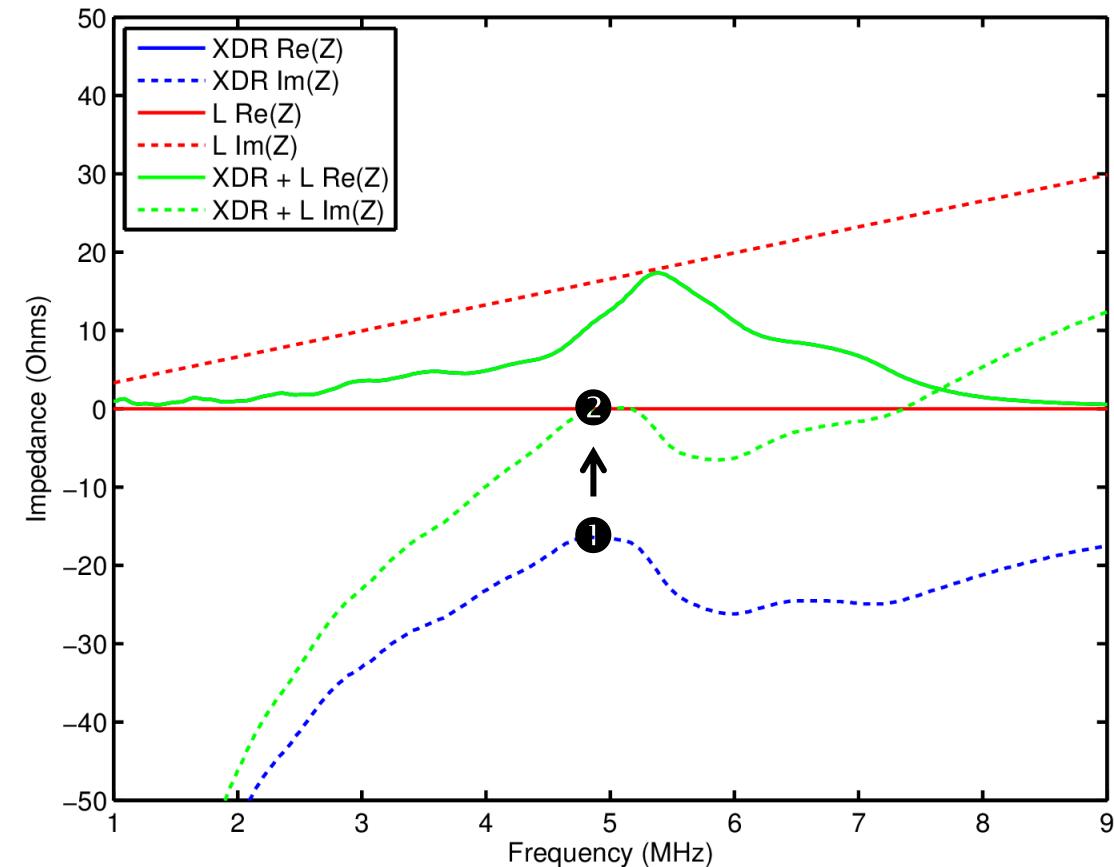
- Calculate required component to add  $j16.6 \Omega$  at 5MHz

$$L_S = \frac{Z}{j\omega} = \frac{16.6j}{j2\times\pi\times5\times10^6} = 0.528 \mu\text{H}$$

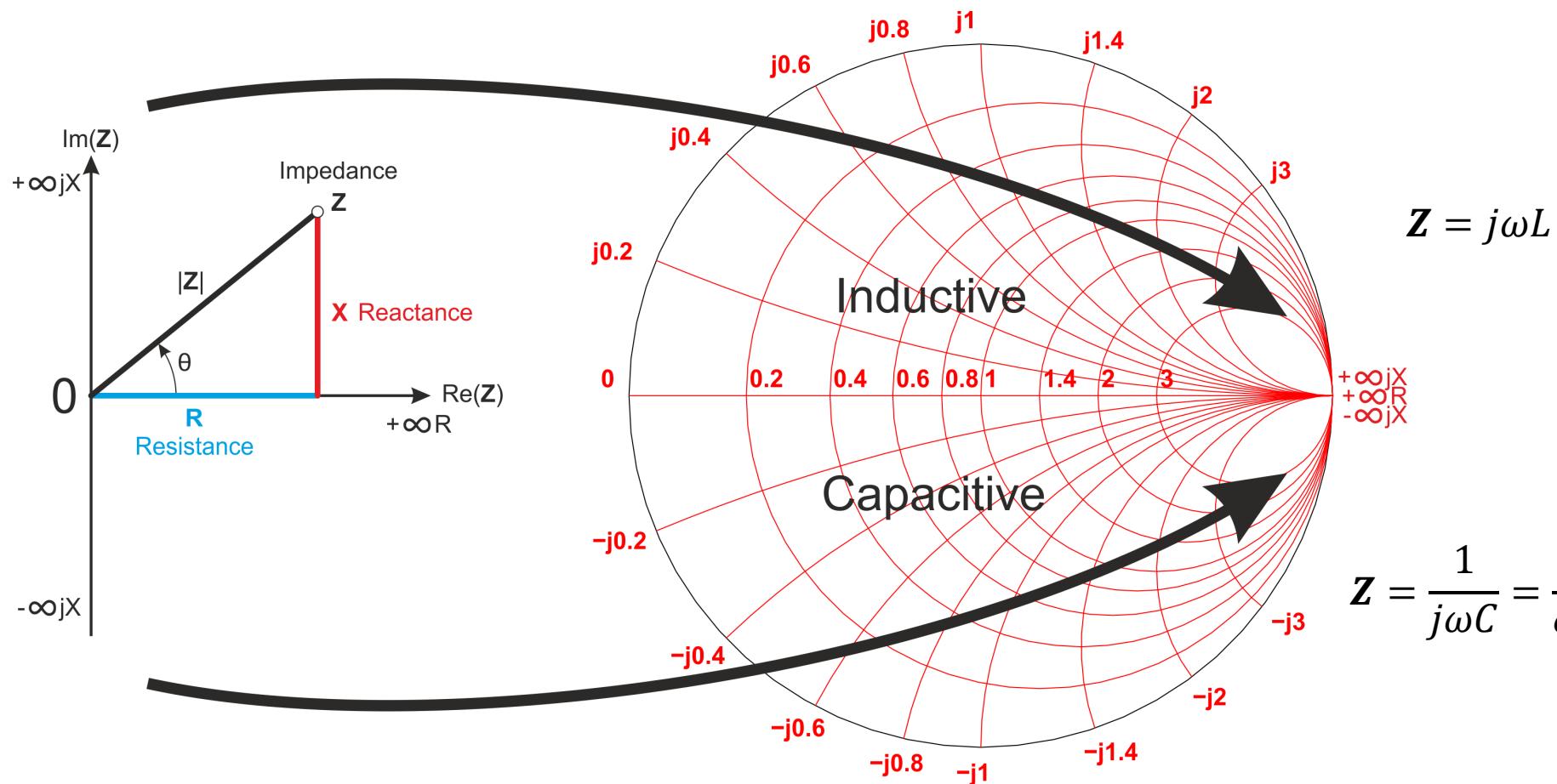
- Add series inductor to complex impedance of transducer element.



- Reactance cancelled at 5 MHz with no change in resistance.
- However, impedance changed from 20.8 ohms to 12.5 ohms!



# Impedance Visualisation Smith Charts



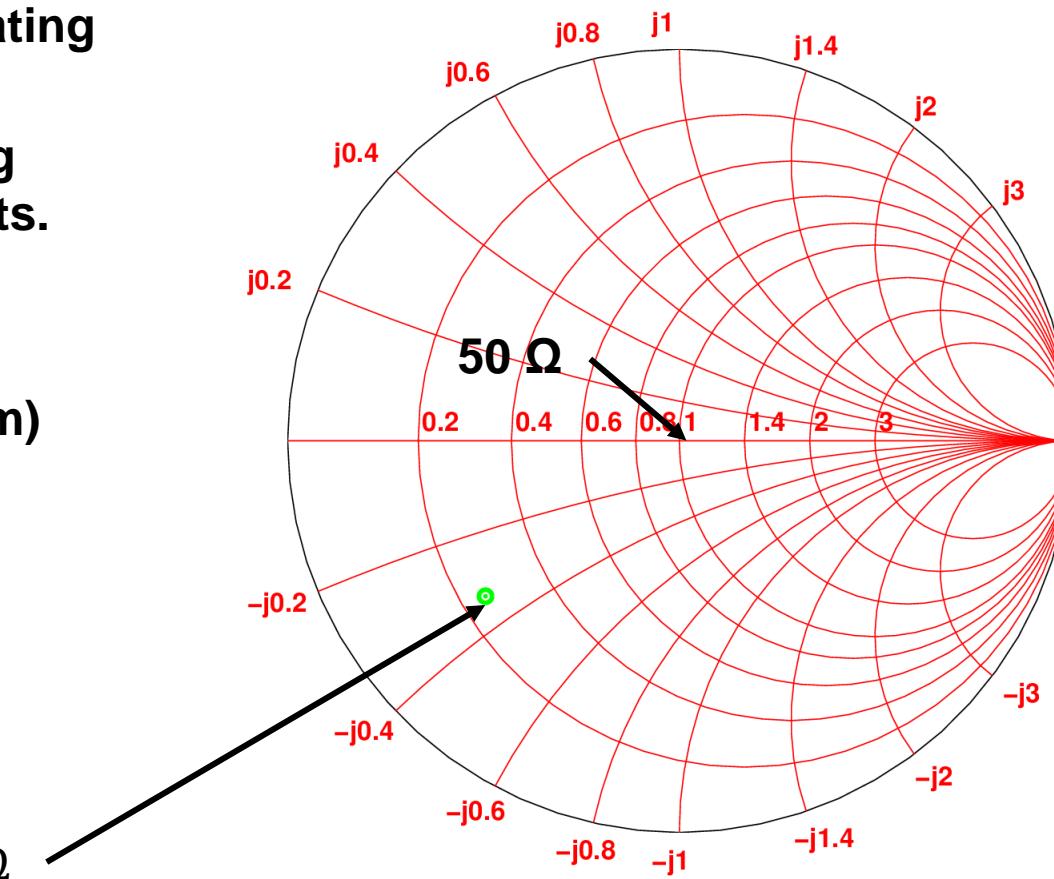
# Smith Chart - Impedance

- Graphical tool for displaying and manipulating impedances.
- Extensively used in Electronic Engineering for calculating impedance matching circuits.
- Often found on impedance or network analyser instruments.
- Typically matched to characteristic (system) impedance.

- $Z_n = Z/Z_o$  e.g. ( $Z_o = 50$ )

- Example XDR at 5 MHz

$$Z_n = \frac{12.5 - j16.6\Omega}{50} = 0.25 - j0.33 \Omega$$



# Smith Chart - Admittance

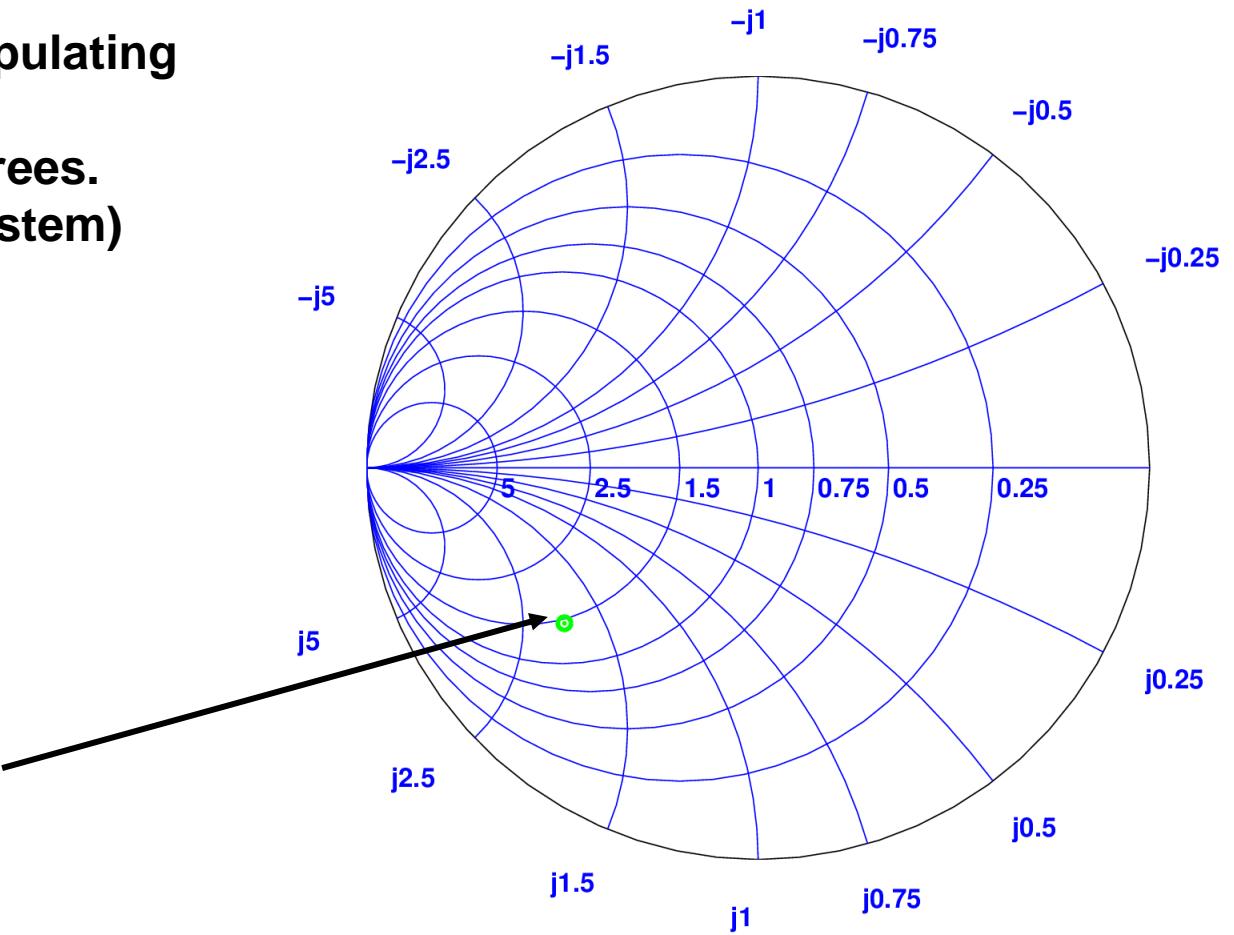
- Graphical tool for displaying and manipulating admittances.
- Rotation of the smith chart by 180 degrees.
- Typically matched to characteristic (system) impedance.

- $Y_o = \frac{1}{Z_o}$  e.g.  $Y_o = \frac{1}{50} = 0.02$

- $Y_n = \frac{Y}{Y_o} = Y \times Z_o$

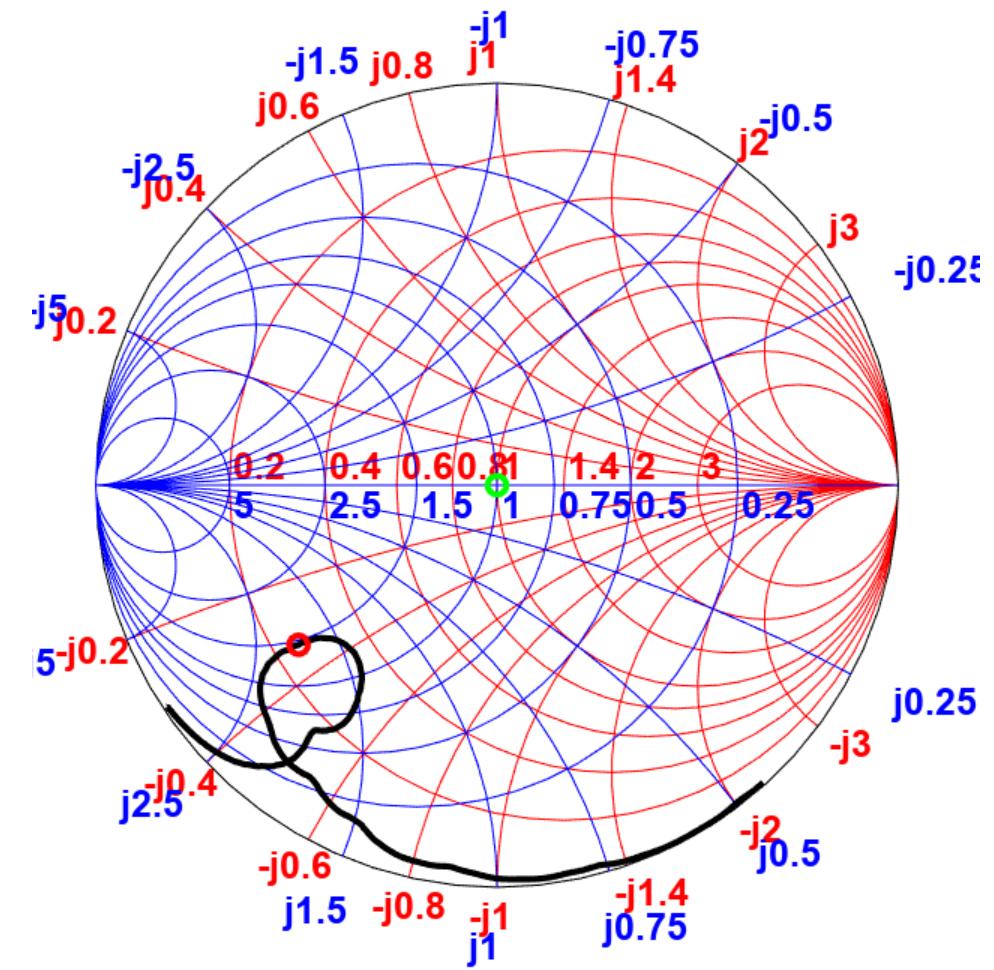
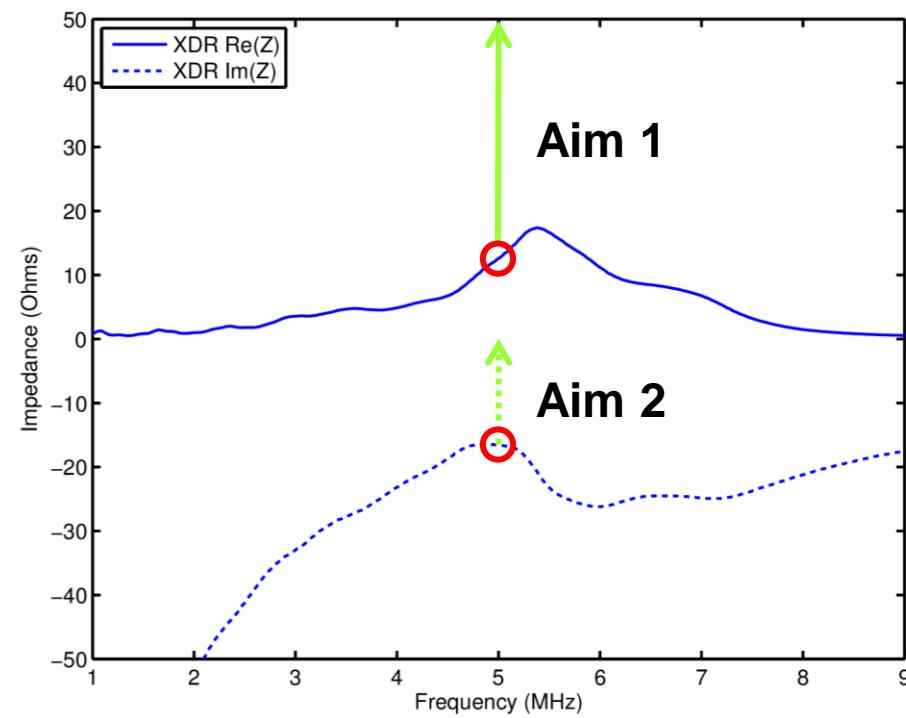
- Example XDR at 5 MHz

$$Y_n = \frac{50}{12.5 - j16.6} = 1.45 + j1.9 \text{ S}$$

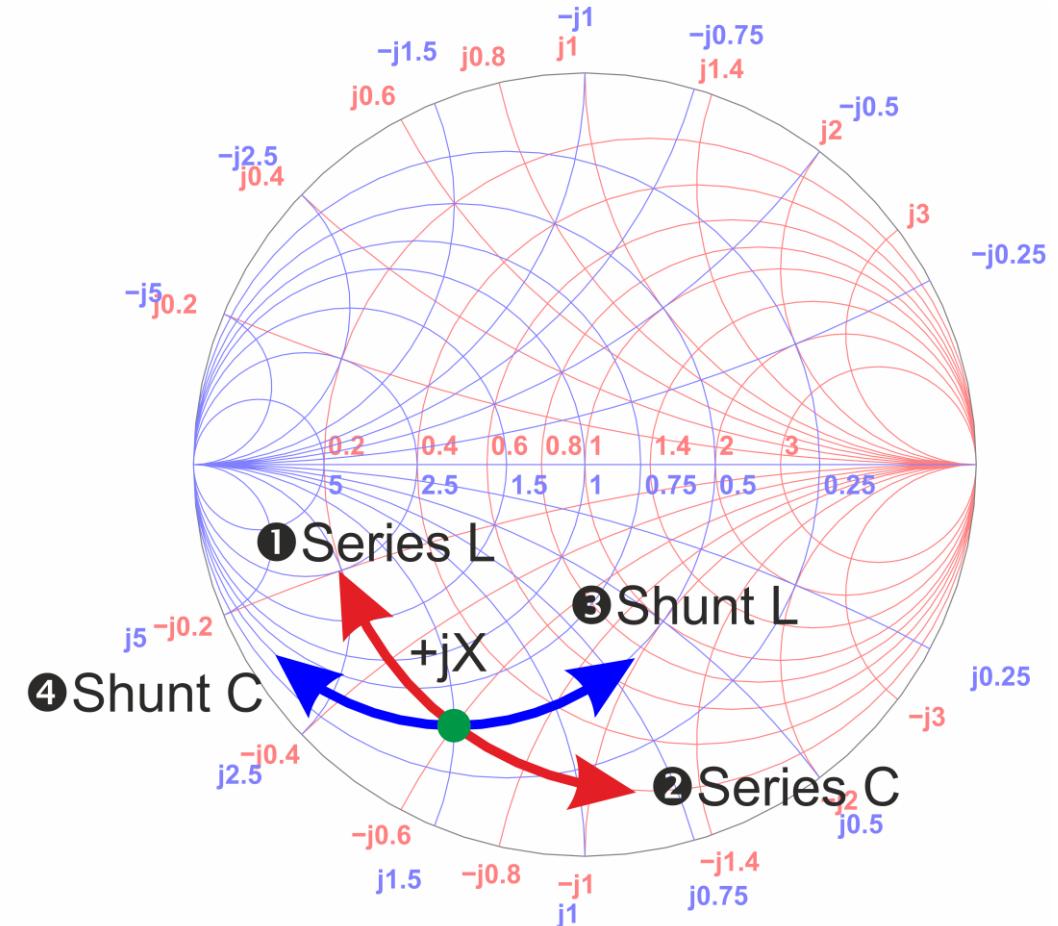
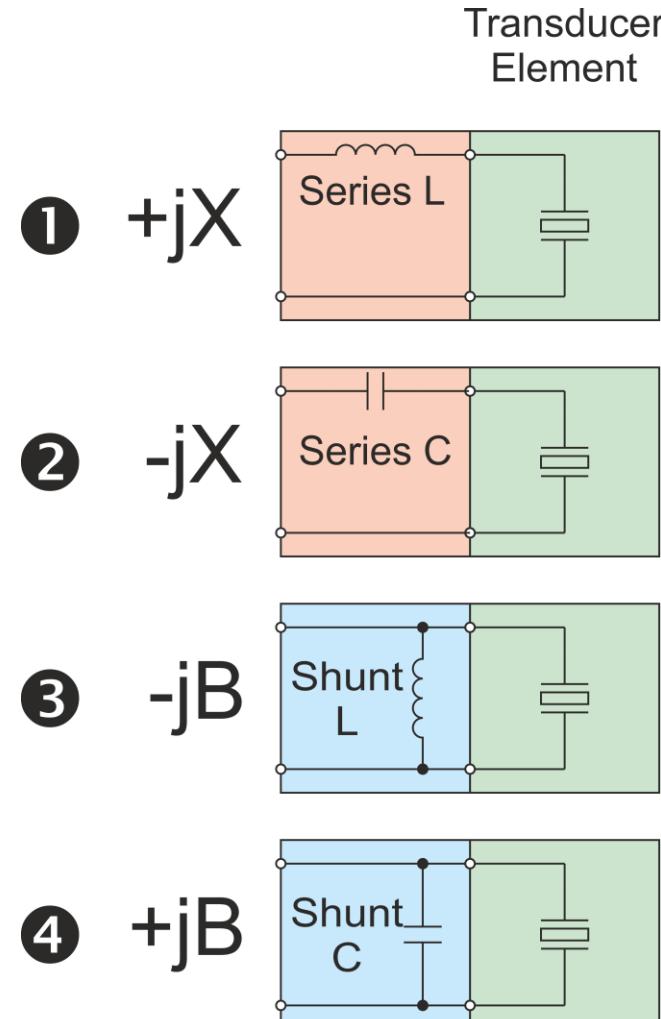


# Smith Chart Impedance Matching

Aim 1 Resistance of 50 ohms at 5 MHz  
Aim 2 Reactance of 0 ohms at 5 MHz



# Smith Chart – Impedance-Admittance



# Smith Chart Impedance Matching Series Inductor

Unmatched transducer impedance shown in BLACK

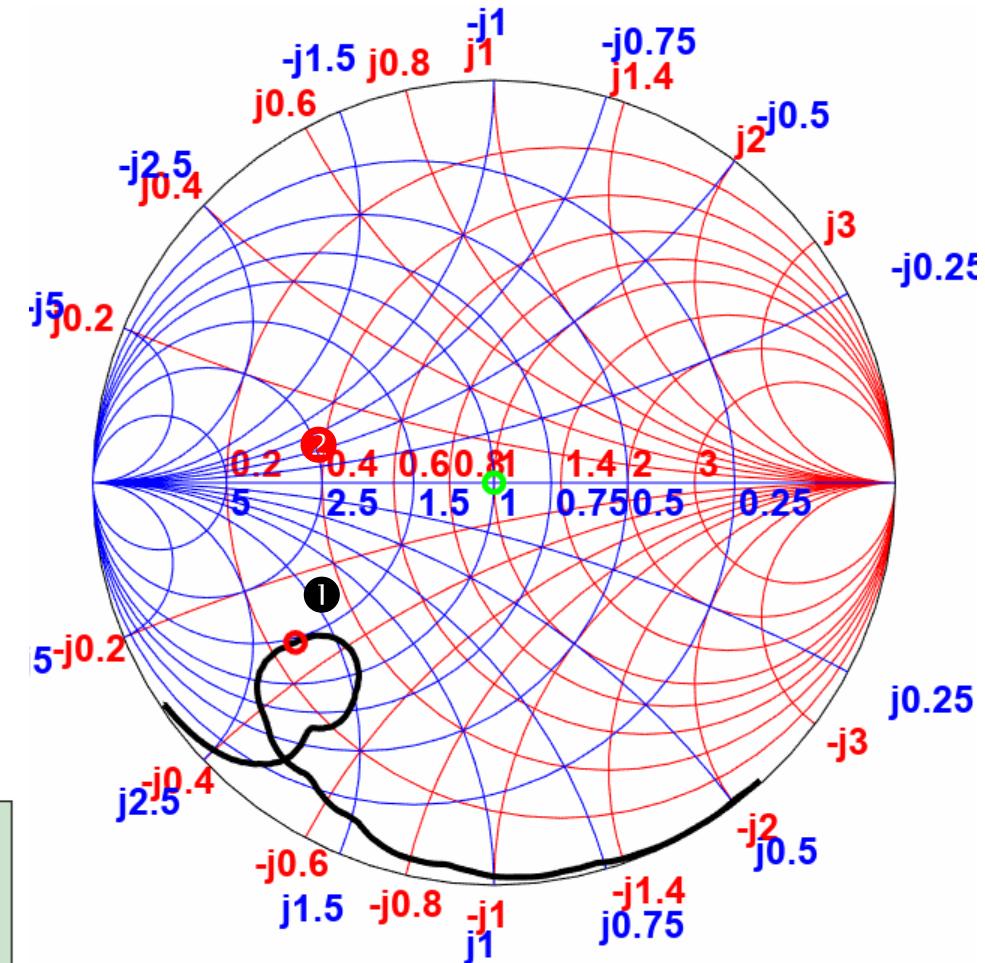
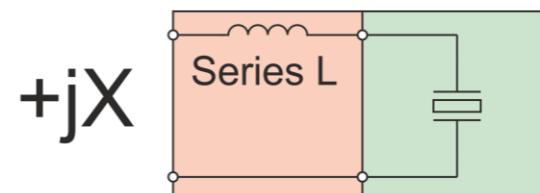
At nominal frequency of 5 MHz:  $Z_{XDR} = 12.5 - j16.6\Omega$

① On smith chart:  $Z_n = \frac{12.5 - j16.6\Omega}{50} = 0.25 - j0.33\Omega$

Therefore, add  $j16.6\Omega$  at 5 MHz  
to cancel capacitive impedance.

$$L_S = \frac{Z}{j\omega} = \frac{16.6j}{j2\pi\times5\times10^6} = 0.528\mu H$$

Adding a series inductor of value of  $0.528\mu H$   
rotates ① anticlockwise around Inductance Smith Chart  
to  $12.5\Omega$  (zero phase) ②.



# Smith Chart Impedance Matching Shunt Inductor

Unmatched transducer impedance shown in BLACK

At nominal frequency of 5 MHz:

Convert impedance to admittance:

$$Y_{XDR} = \frac{1}{12.5 - j16.6} = 0.029 + j0.038 \text{ S}$$

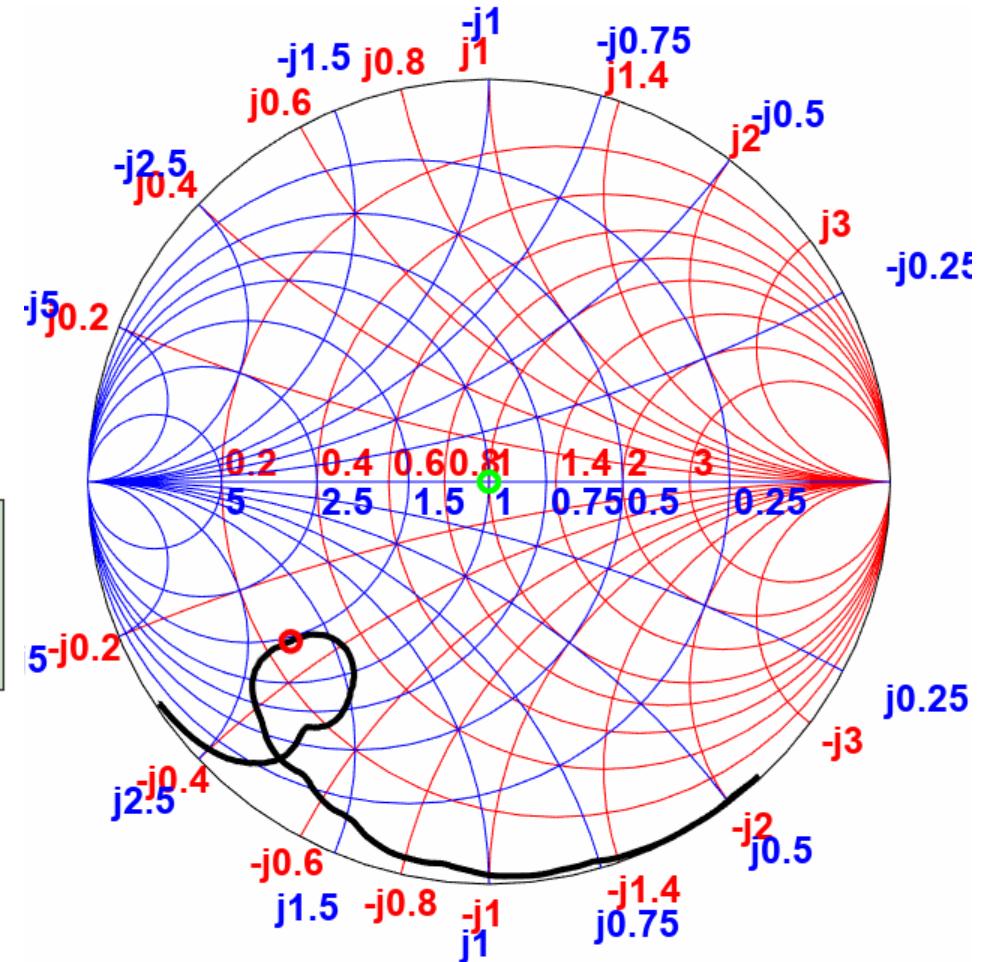
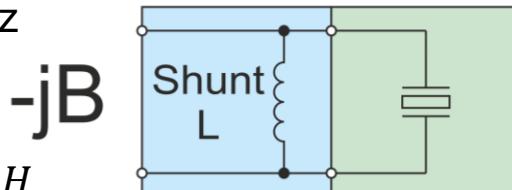
① On smith chart:  $Y_n = 50 \times Y_{XDR} = 1.45 + j1.9 \text{ S}$

Therefore, subtract  $j0.038 \text{ S}$  at 5 MHz  
to cancel capacitive impedance.

$$L_P = \frac{1}{j\omega Y} = \frac{1}{j2\pi \times 5 \times 10^6 \times j0.038} = 0.837 \mu\text{H}$$

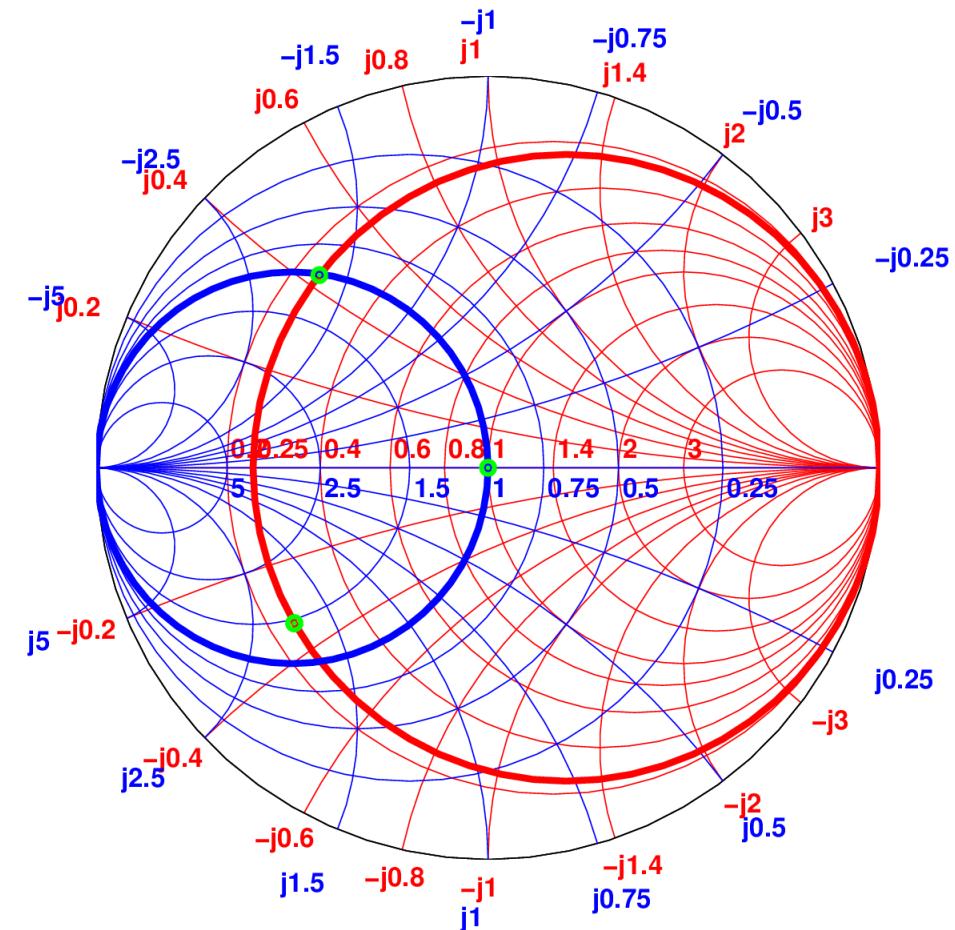
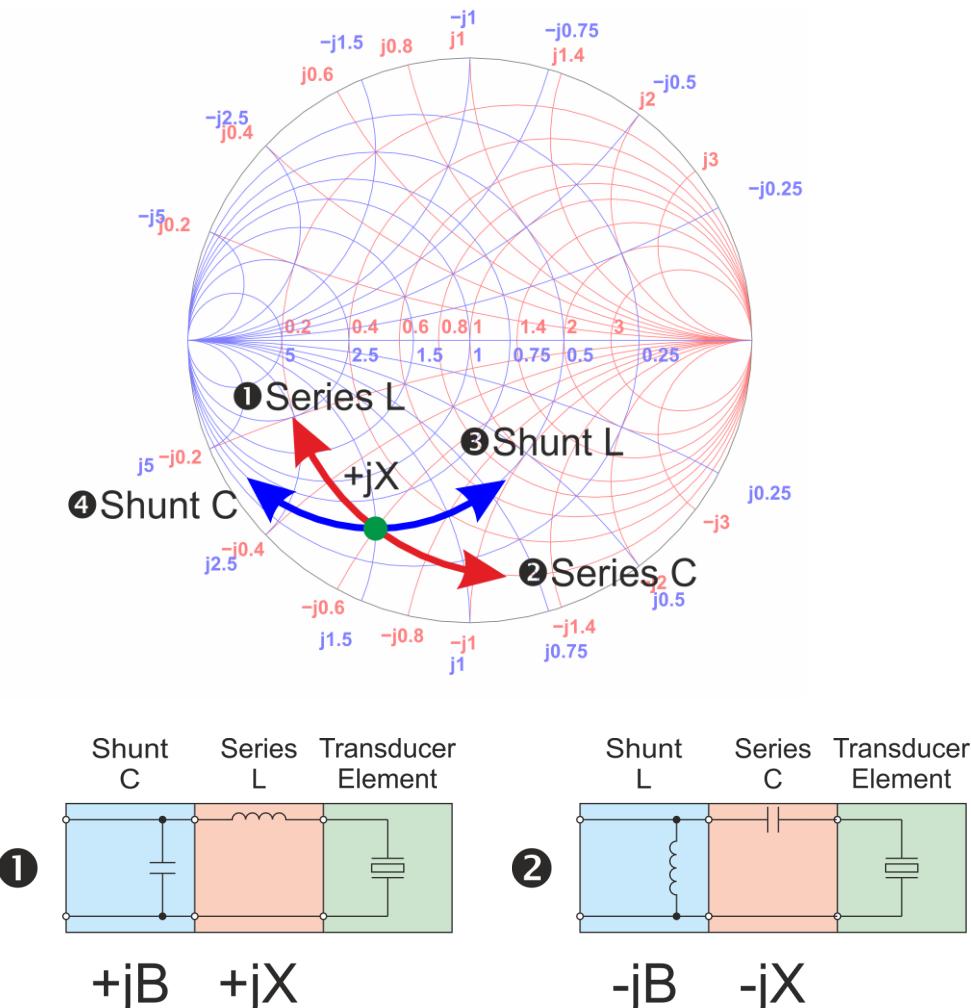
Adding a shunt (parallel) inductor of value  $0.837 \mu\text{H}$   
rotates ① anticlockwise around Admittance Smith Chart  
to  $34.5 \Omega$  ( $0.029 \text{ S}$ ) ③.

Note: Impedance circles  $50 \Omega$  indicating good matching  
over a broad bandwidth.



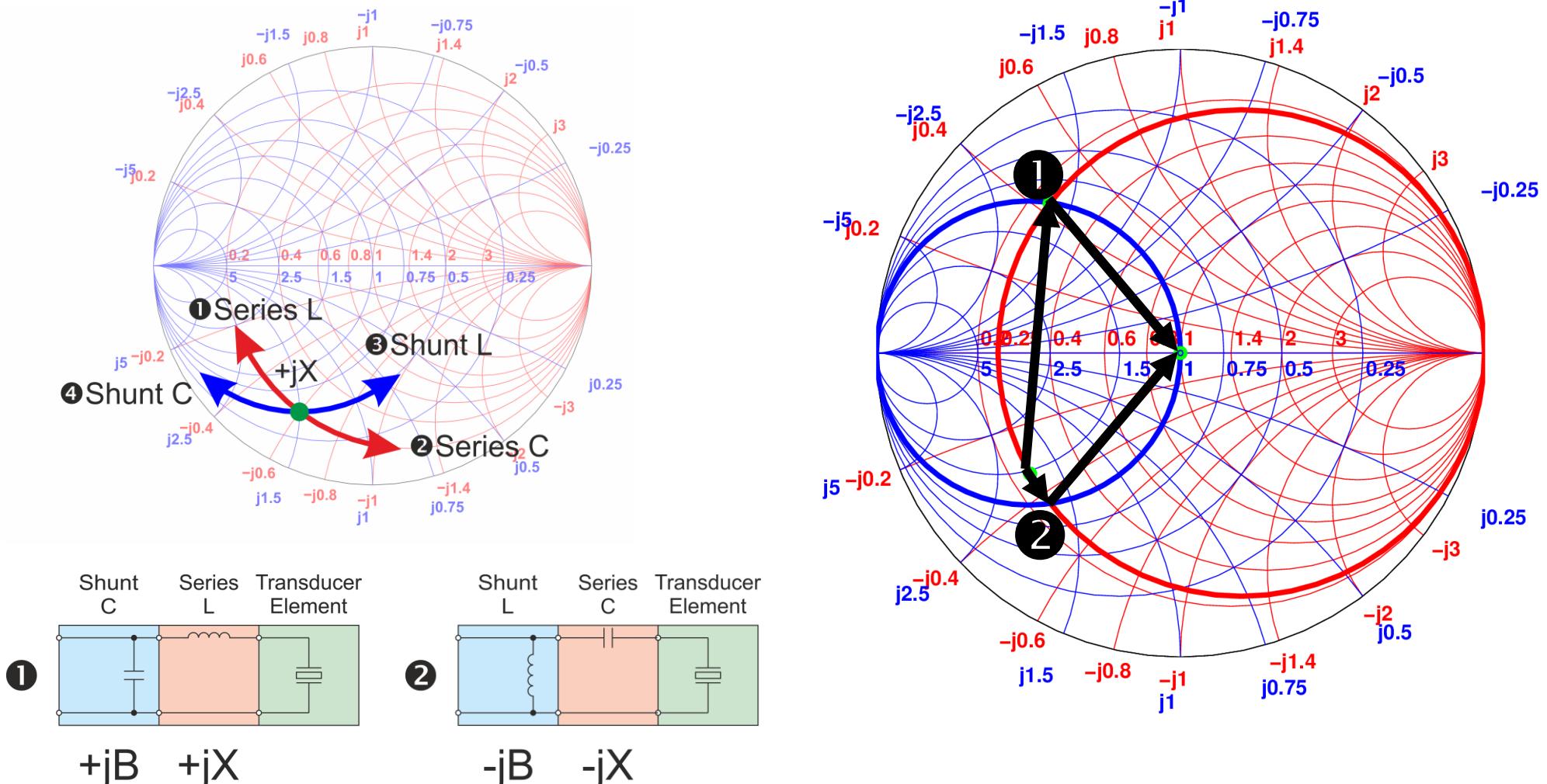
# Multi-component Smith Chart

## Impedance Matching

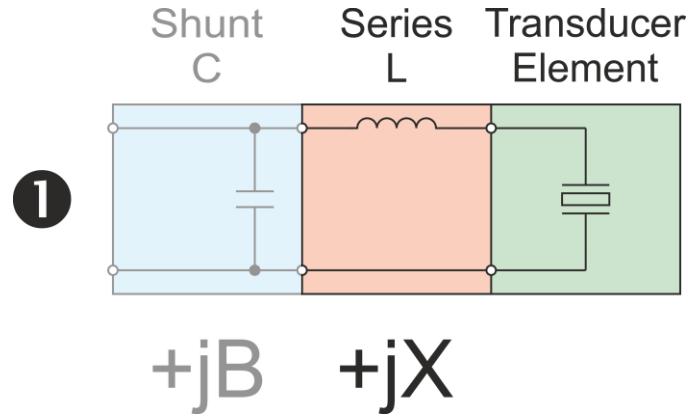


# Multi-component Smith Chart

## Impedance Matching



# ① Multi-component Smith Chart Impedance Matching



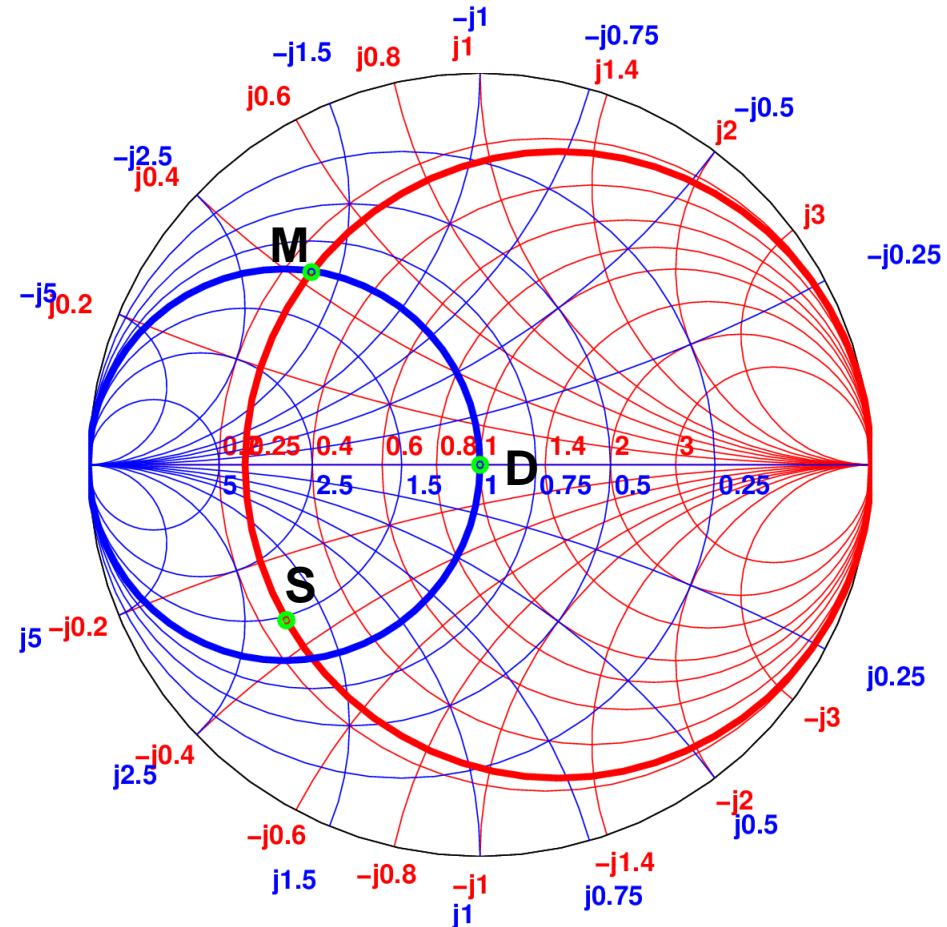
**S:**  $Z_{XDR} = 12.5 - j16.6$

**S:**  $Z_{XDRn} = 0.25 - j0.33$

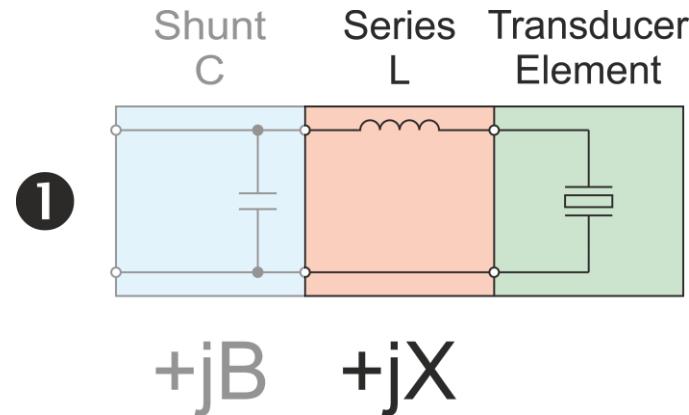
**M:**  $Z_{(XDR+L)n} = 0.25 + j0.43$

**M-S:**  $Z_{Ln} = 0 + j0.76 \therefore Z_L = j38$

At 5 MHz  $L = \frac{j38}{j2\pi \times 5e6} = 1.2\mu H$



# ① Multi-component Smith Chart Impedance Matching



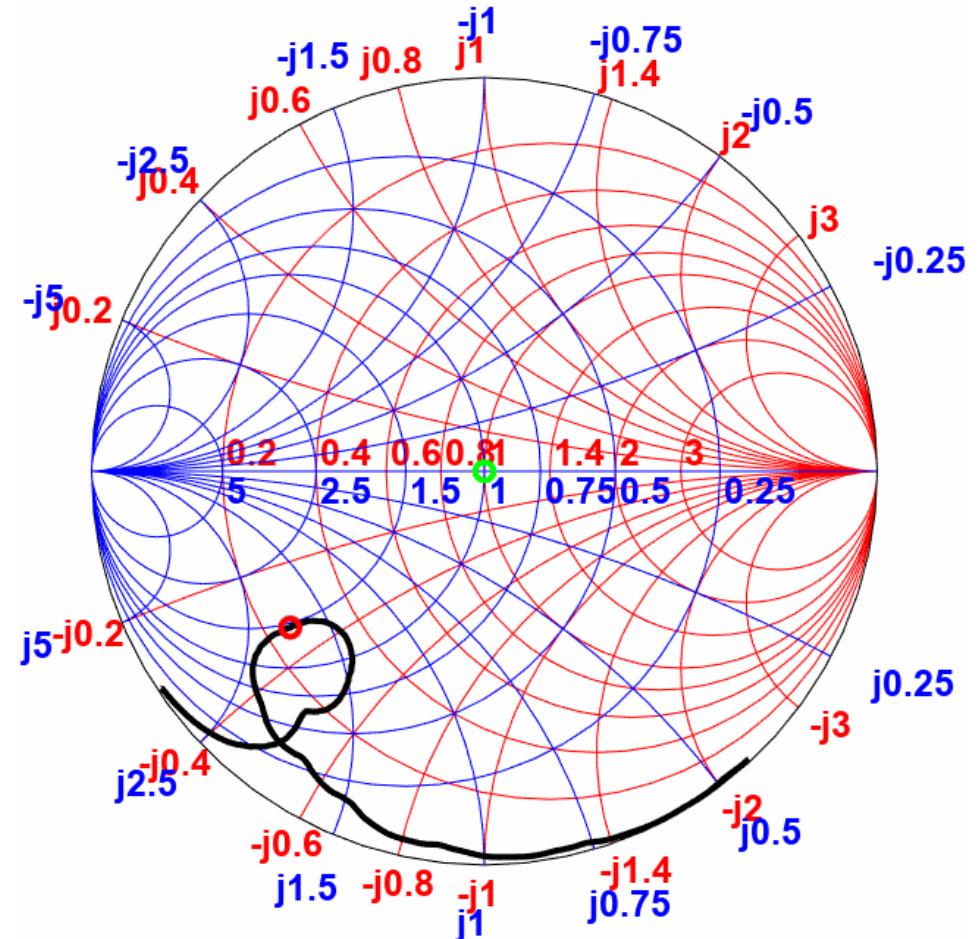
**S:**  $Z_{XDR} = 12.5 - j16.6$

**S:**  $Z_{XDRn} = 0.25 - j0.33$

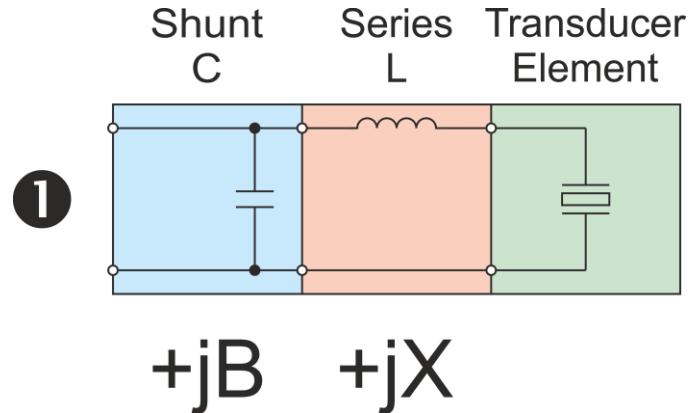
**M:**  $Z_{(XDR+L)n} = 0.25 + j0.43$

**M-S:**  $Z_{Ln} = 0 + j0.76 \therefore Z_L = j38$

At 5 MHz  $L = \frac{j38}{j2\pi \times 5e6} = 1.2\mu H$



# I Multi-component Smith Chart Impedance Matching



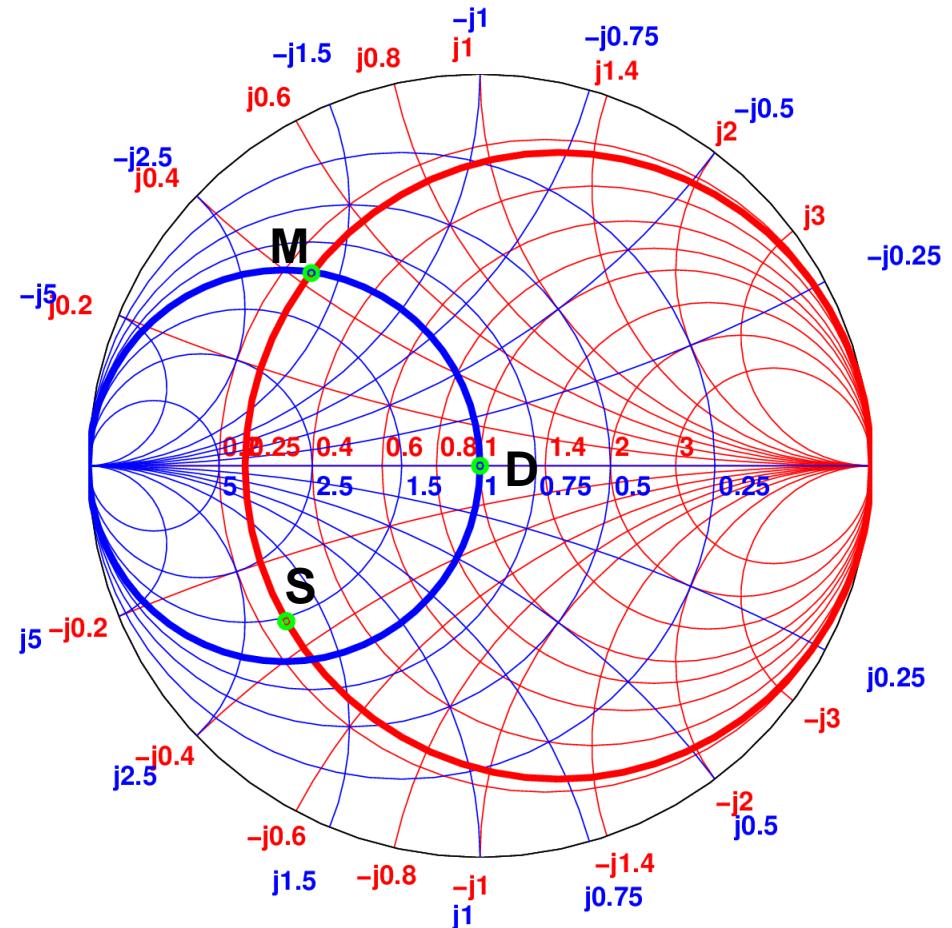
M:  $Z_{(XDR+L)n} = 0.25 + j0.43$

M:  $Y_{(XDR+L)n} = 1 - j1.74$

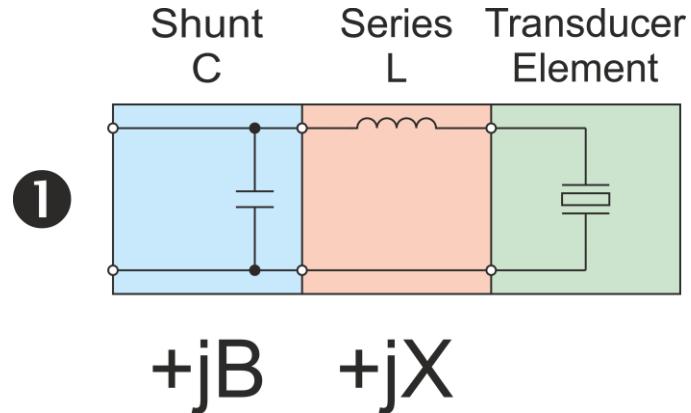
D:  $Y_{(XDR+L)n||Cn} = 1 - j0$

D-M:  $Y_{Cn} = 0 + j1.74 \quad \therefore \quad Y_C = j0.0348$

At 5 MHz  $C = \frac{j0.0348}{j2\pi \times 5e6} = 1.1nF$



# 1 Multi-component Smith Chart Impedance Matching



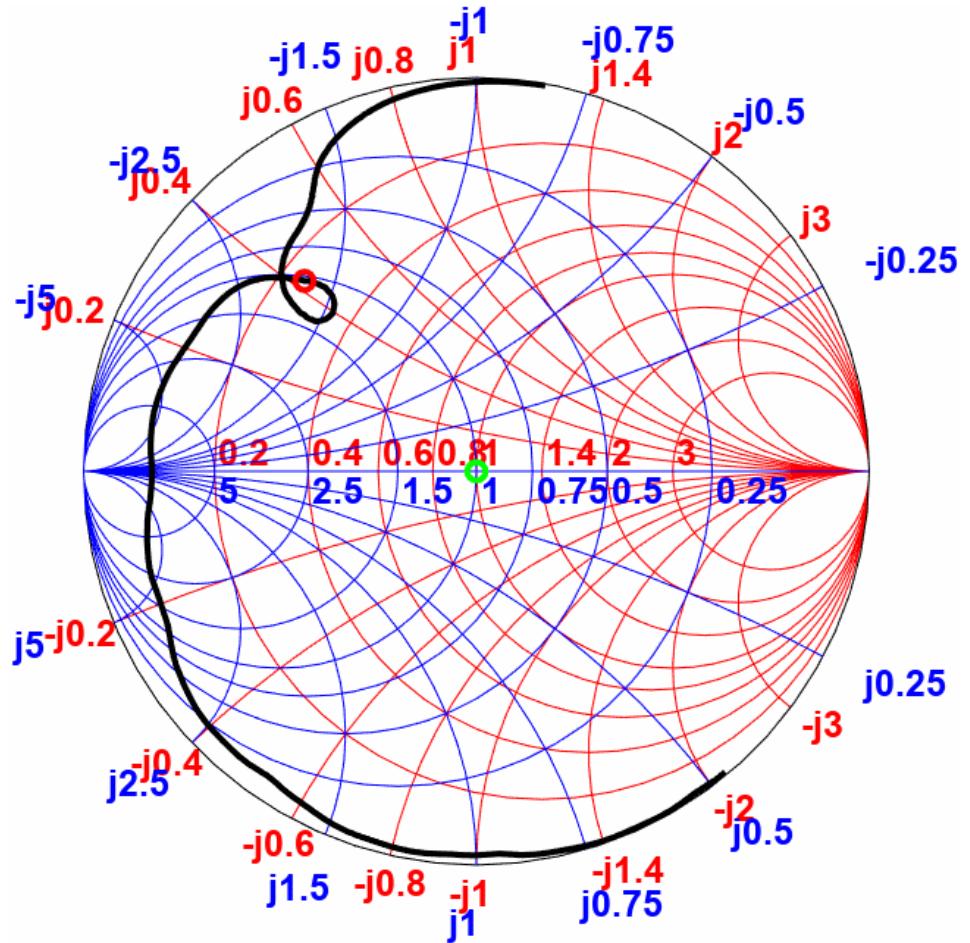
M:  $Z_{(XDR+L)n} = 0.25 + j0.43$

M:  $Y_{(XDR+L)n} = 1 - j1.74$

D:  $Y_{(XDR+L)n||Cn} = 1 - j0$

D-M:  $Y_{Cn} = 0 + j1.74 \quad \therefore \quad Y_C = j0.0348$

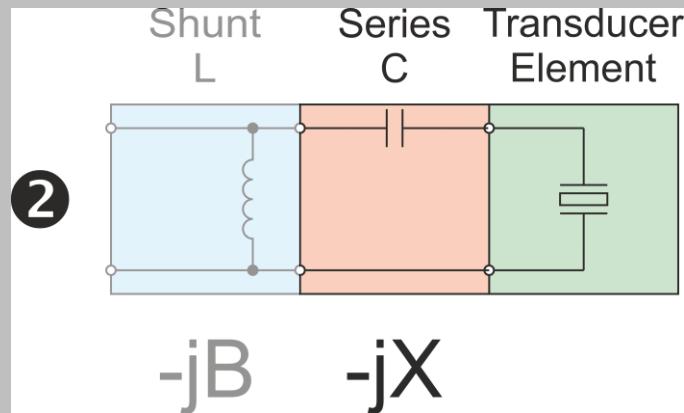
At 5 MHz  $C = \frac{j0.0348}{j2\pi \times 5e6} = 1.1nF$



②

# Multi-component Smith Chart

## Impedance Matching



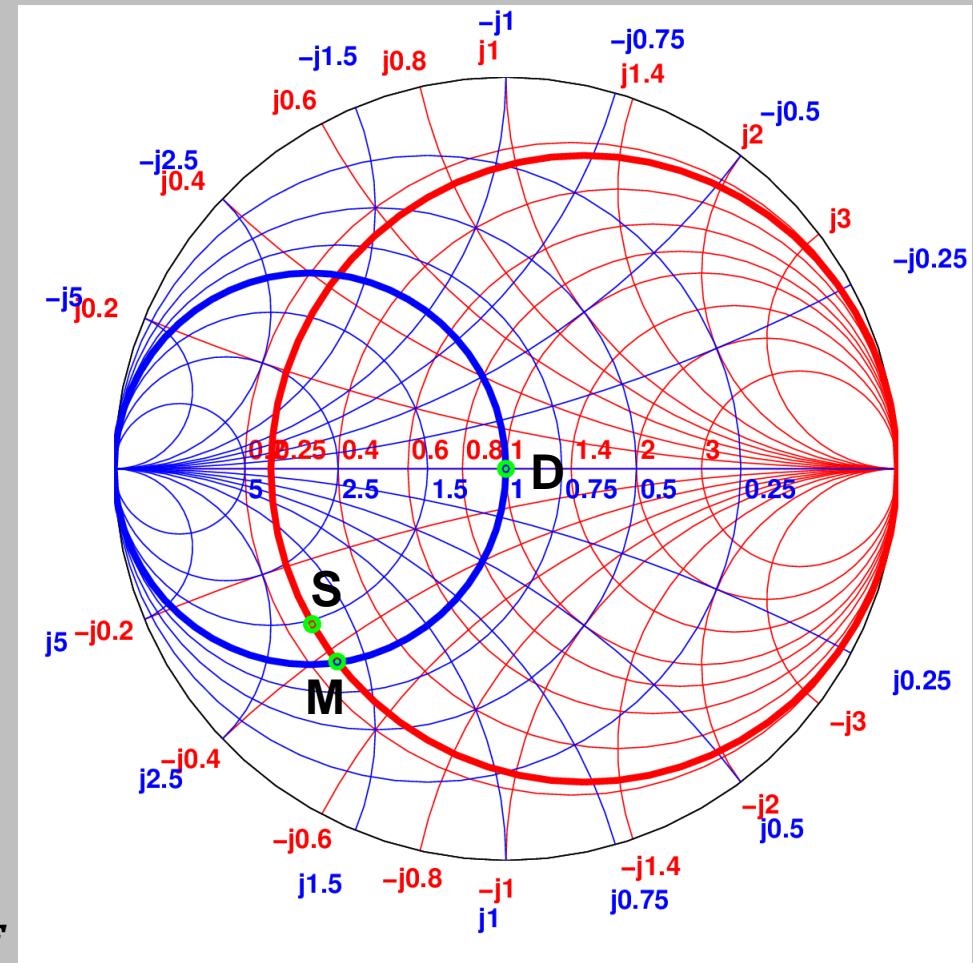
**S:**  $Z_{XDR} = 12.5 - j16.6$

**S:**  $Z_{XDRn} = 0.25 - j0.33$

**M:**  $Z_{(XDR+C)n} = 0.25 - j0.43$

**M-S:**  $Z_{Cn} = 0 - j0.10 \therefore Z_C = -j5$

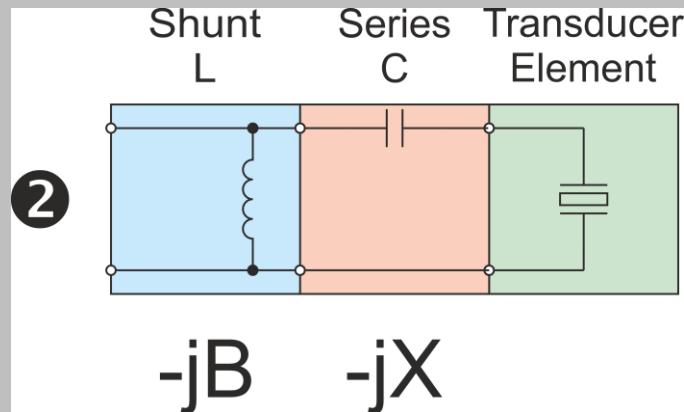
At 5 MHz  $C = \frac{1}{j2\pi \times 5e6 \times (-j5)} = 6.36nF$



②

# Multi-component Smith Chart

## Impedance Matching



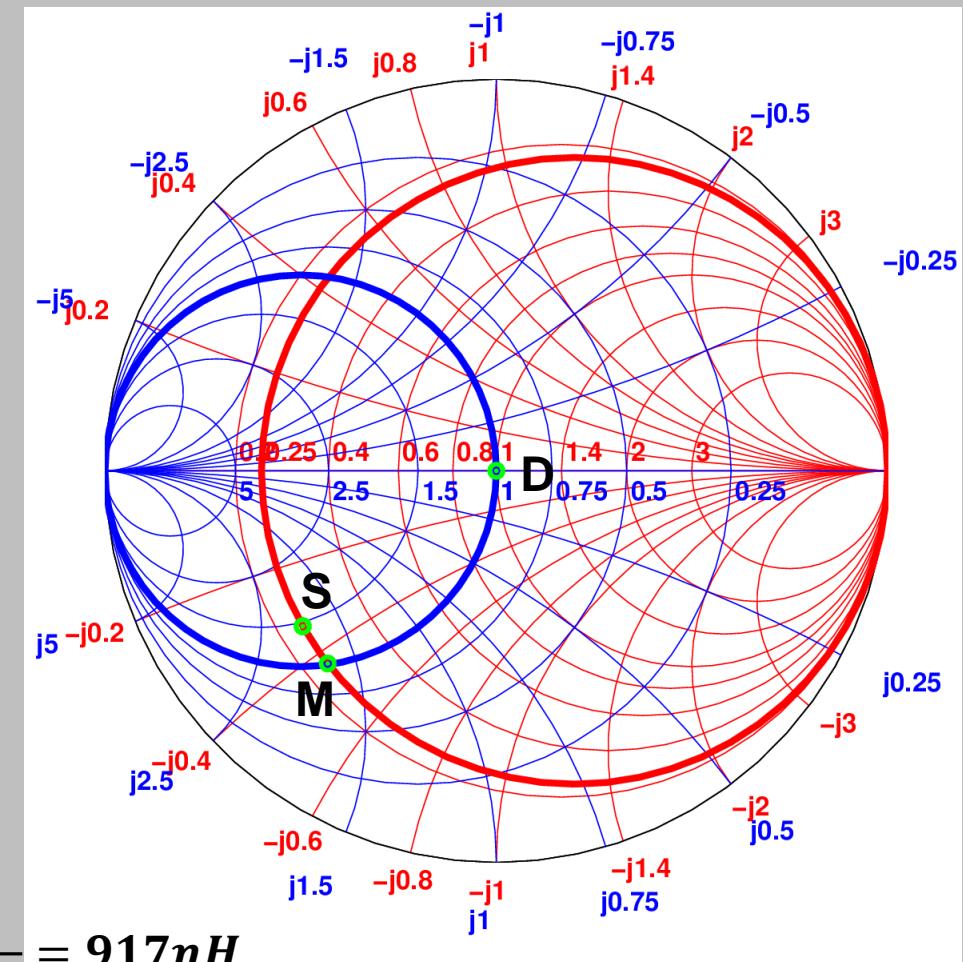
$$\mathbf{M}: Z_{(XDR+C)n} = 0.25 - j0.43$$

$$\mathbf{M}: Y_{(XDR+C)n} = 1 + j1.73$$

$$\mathbf{D}: Y_{(XDR+C)n||Ln} = 1 + j0$$

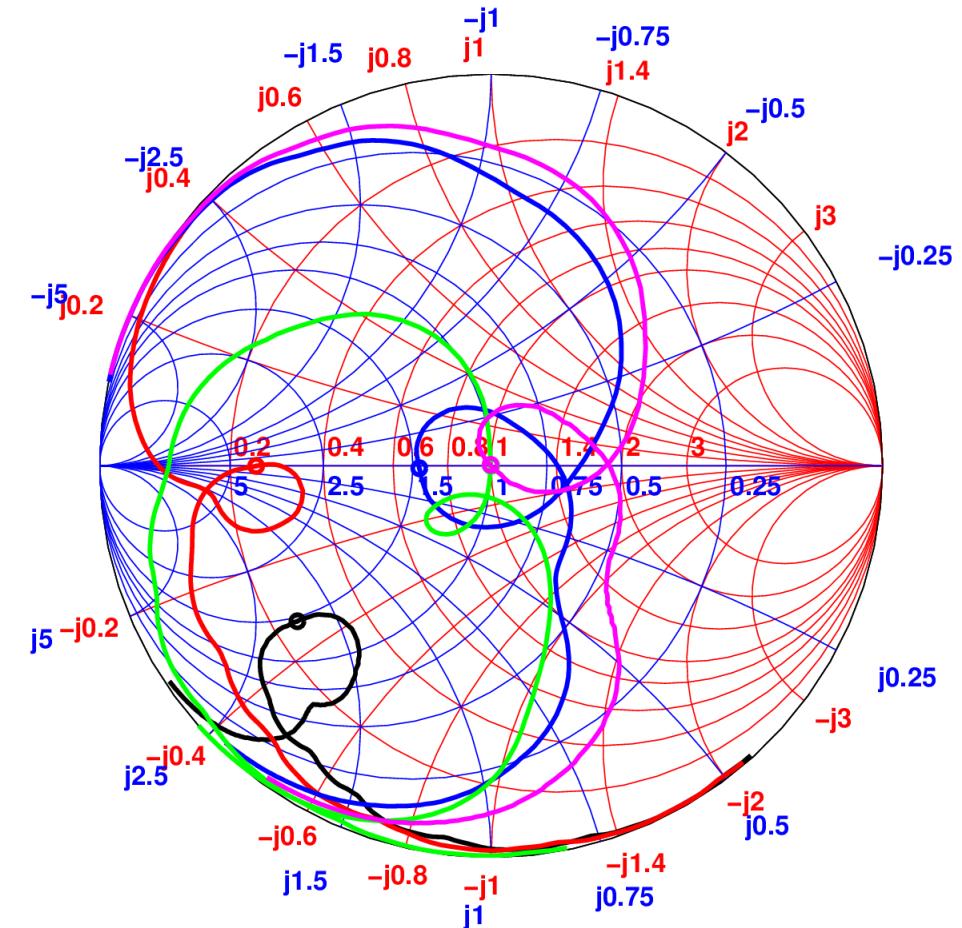
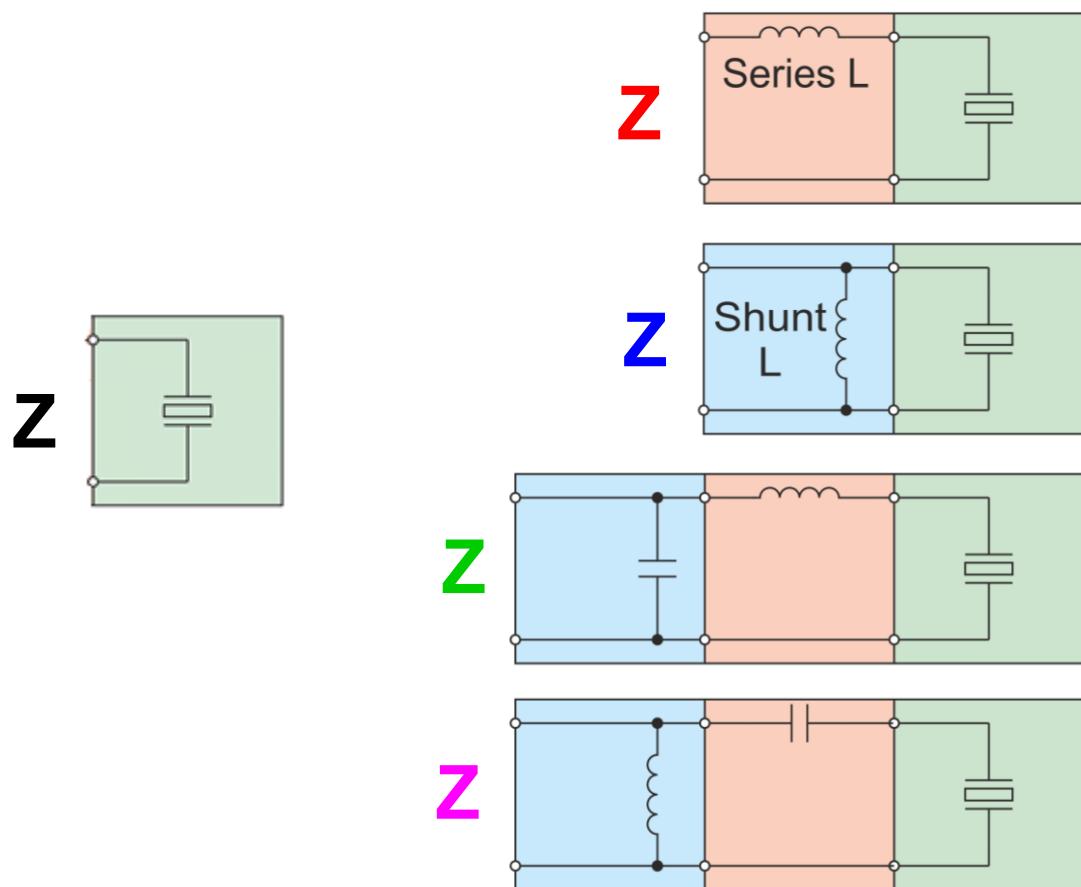
$$\mathbf{D-M}: Y_{Ln} = 0 - j1.73 \quad \therefore \quad Y_L = -j0.035$$

$$\text{At } 5 \text{ MHz} \quad L = \frac{1}{j\omega Y} = \frac{1}{j2\pi \times 5e6 \times (-j0.035)} = 917nH$$

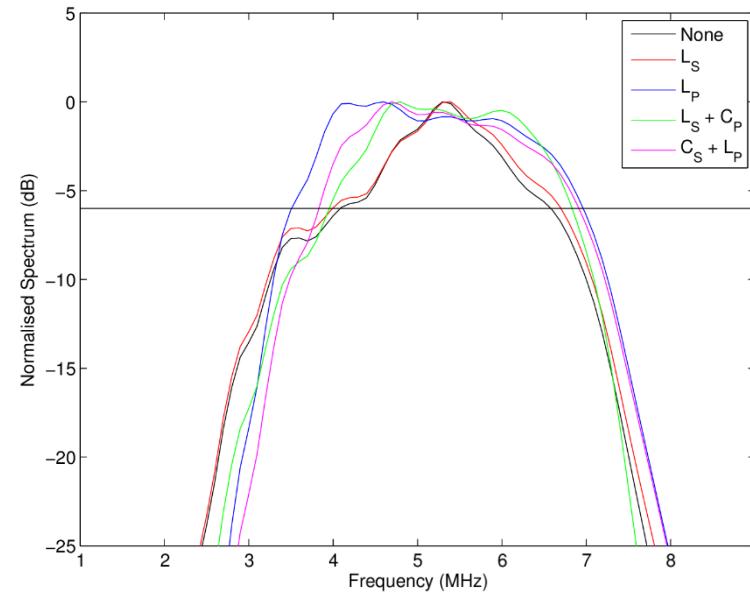
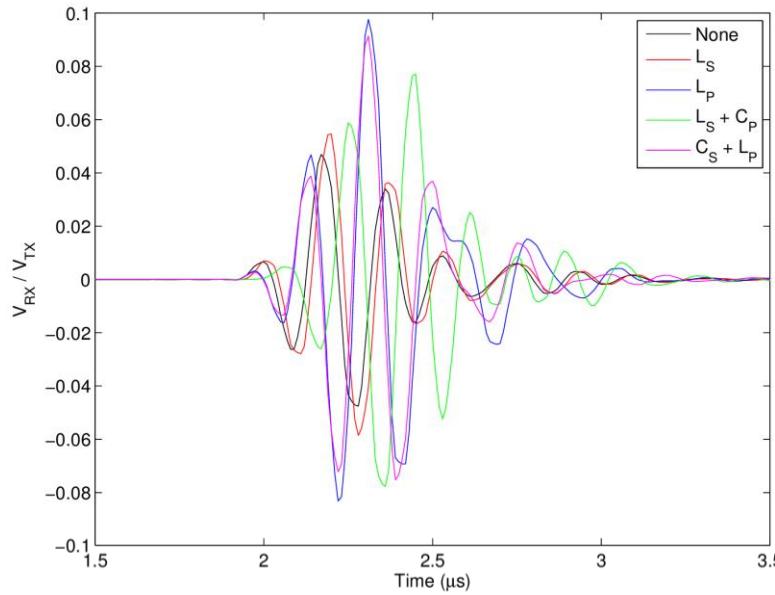


# Multi-component Smith Chart

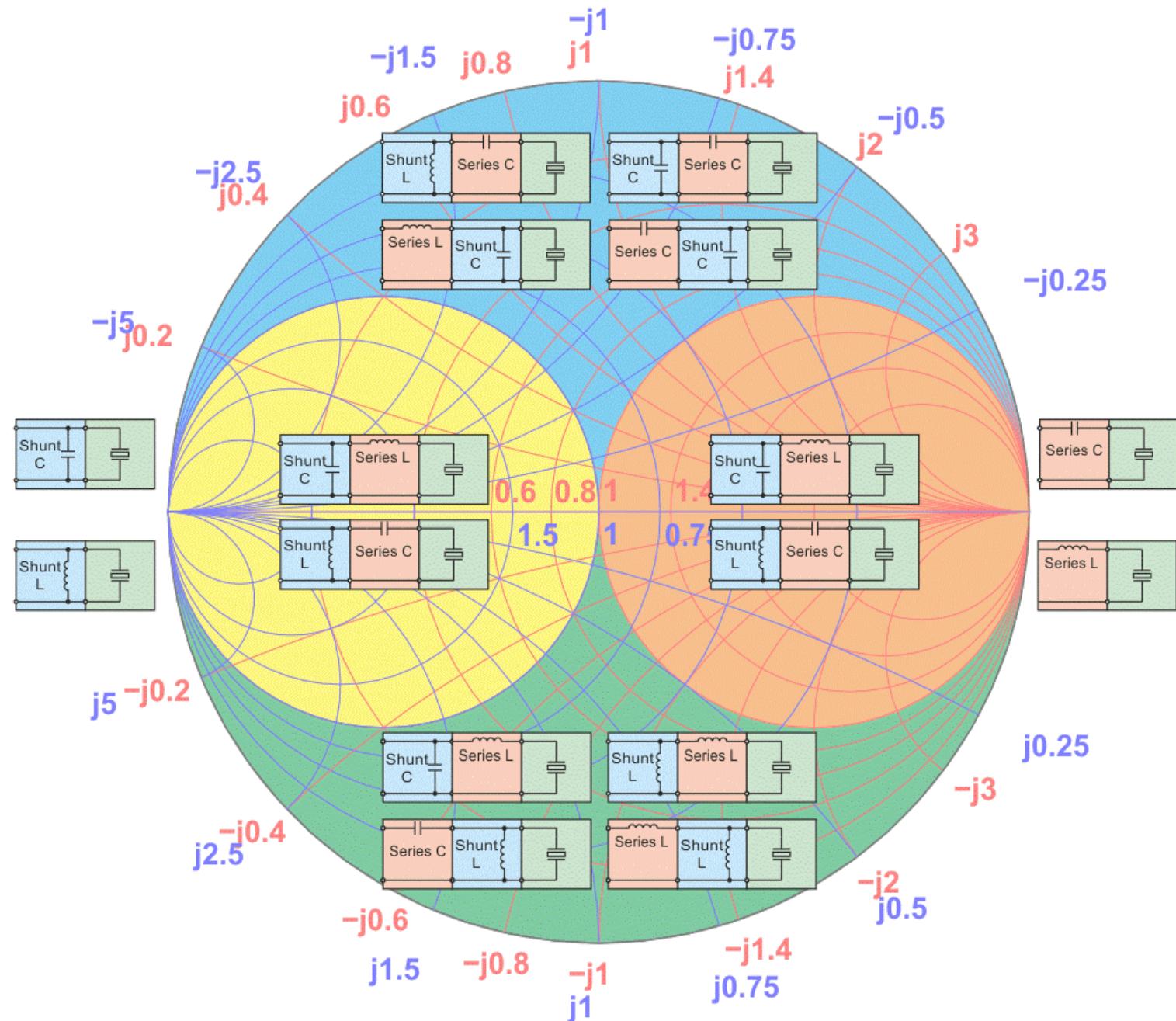
## Impedance Matching



# Effect of matching circuits on Pulse Echo response

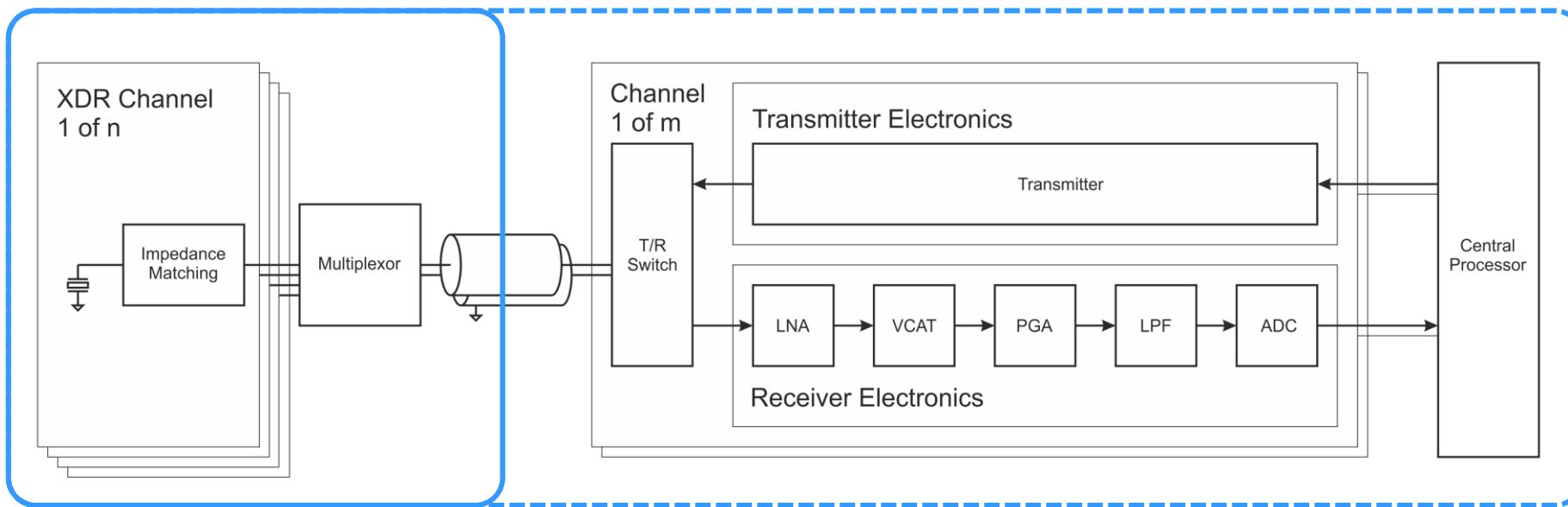


- **Pulse echo time response**
- Improvement in sensitivity
  - $9.4 \text{ mV}_{RX}/\text{V}_{TX}$  (No matching)
  - $18.2 \text{ mV}_{RX}/\text{V}_{TX}$  (Parallel Inductor)
- **Pulse echo frequency response**
- Improved -6dB bandwidth
  - 2.5 MHz (No matching)
  - 3.5 MHz (Parallel Inductor)
  - Flatter bandwidth above -6dB

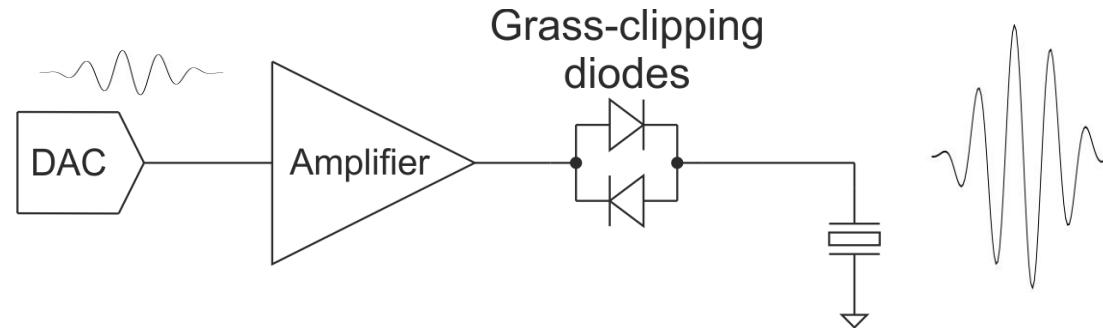


# Electronics Overview

## Transducer



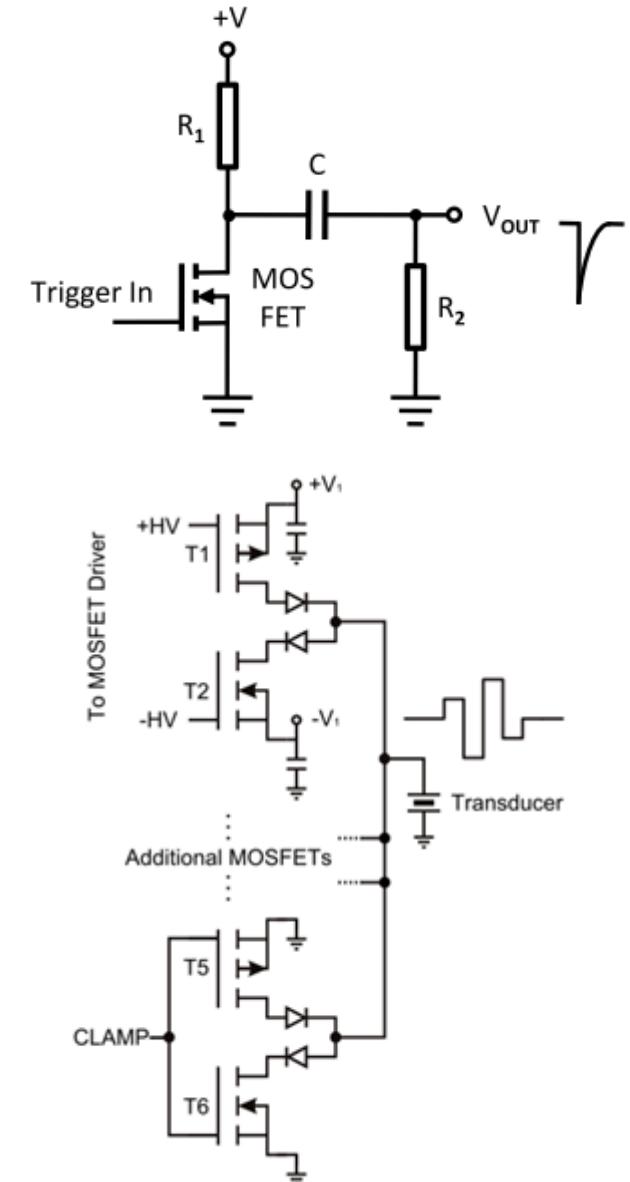
# Arbitrary Excitation



- True arbitrary excitation allows control of frequency/phase and amplitude.
- Arbitrary control required for apodization across an array aperture.
- Significant implementation complexity of digital to analog converter (DAC) and amplifier, plus digital control and waveform storage/generation requirements.
- Amplifier requires a linear, high current, high voltage, high slew rate response.
- Amplifier Slew rate (SR) defines frequency-voltage operating space:  
$$2 \pi f V_{\text{pk}} \leq \text{SR} \leq \max \left( \left| \frac{d v_{\text{out}}(t)}{dt} \right| \right)$$
- Low output impedance of amplifier must be disconnected from transducer during receive mode using either a high voltage switch or grass-clipping diodes.

# Pulsed & Switched Excitation

- Switching between discrete voltage levels to generate short pulses or ‘square wave’ signals.
- Potential for high voltages and currents to be switched at high freq.
- With decreasing rise and fall time signal approaches an impulse.
- Broadband pulse generation is limited by switching speed of MOSFET.
  - Performance limited by device parasitics
  - e.g. gate inductance, drain-source capacitance etc
- In negative ‘Shock Excitation’ the positive plate of charged capacitor switch to ground producing a negative pulse on transducer (top)
- Complex excitation modulation schemes (e.g. approximate to arbitrary excitation) can be implemented by direct switching between discrete supply voltages using multiple MOSFETs (bottom).



# Commercial Chipsets

## TX & T/R – Maxim – MAX14808

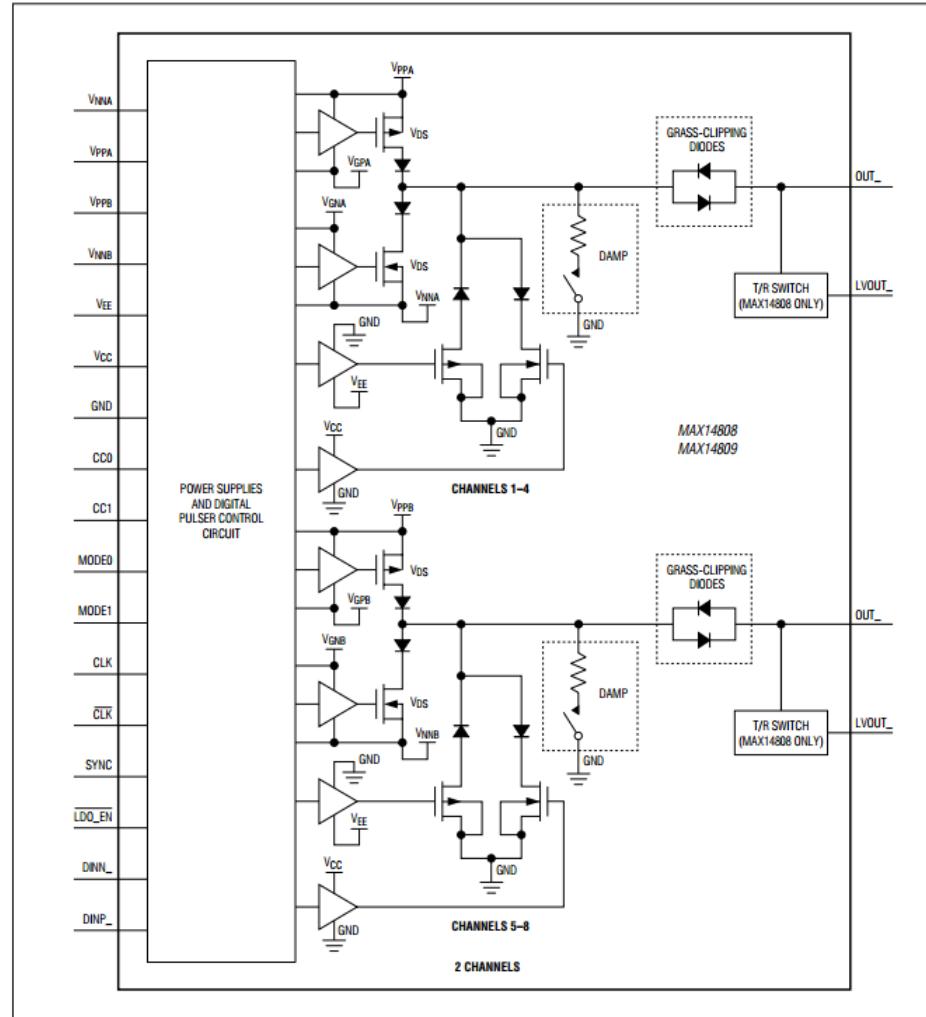
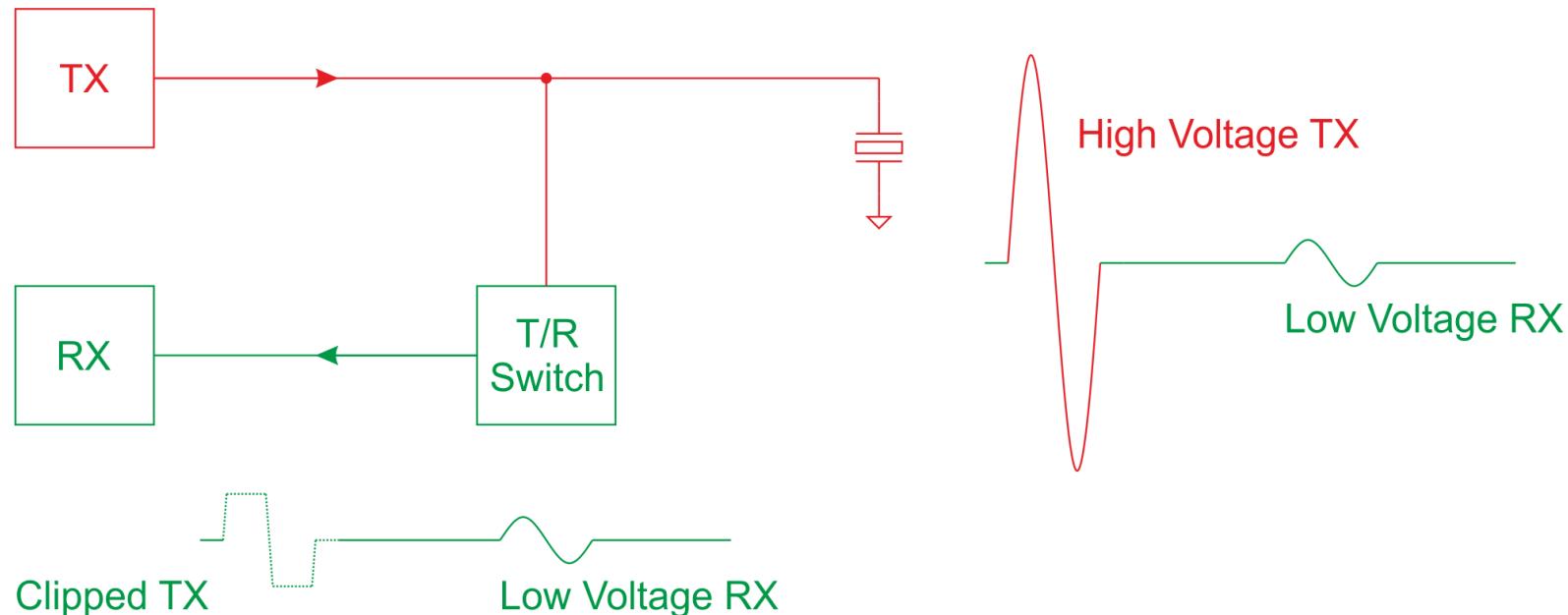


Image copyright Maxim Integrated (Source: MAX14808 Datasheet)

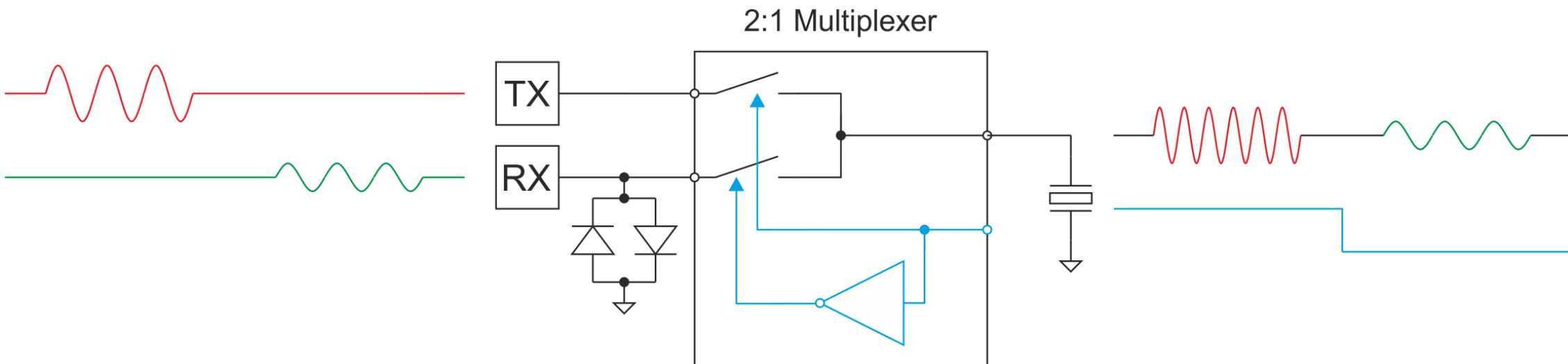
# Transmit/Receive Switch

- RX electronics are typically tolerant of input voltages in the order of  $\pm 1$  V.
- High voltages in the order of  $\pm 100$  V are common in excitation waveforms.
- Transmit/Receive (T/R) Switches are used to protect RX electronics from high TX voltages whilst allowing low voltage signals to RX electronics.
- T/R switch must be designed to minimise distortion to the RX signals.



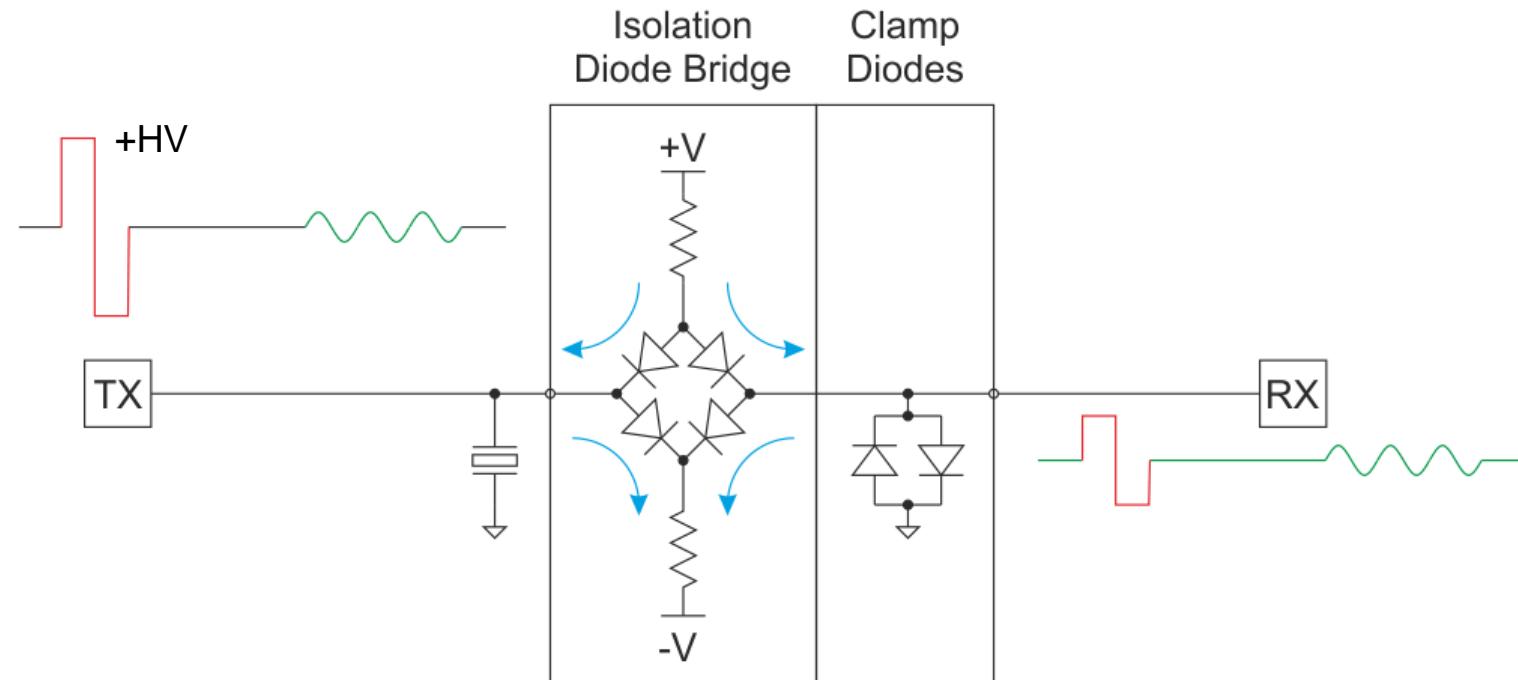
# Transmit/Receive Switch

- A multiplexer switch may be used as a T/R switch due to its inherent high voltage and low distortion.
- The switchover time between inputs must be very fast, ideally sub microsecond.
- Additional protection placed between T/R switch and receiver to protect sensitive electronics from high voltages that may present on transducer during switchover. Typically, back-to-back *grass clipping* diodes.



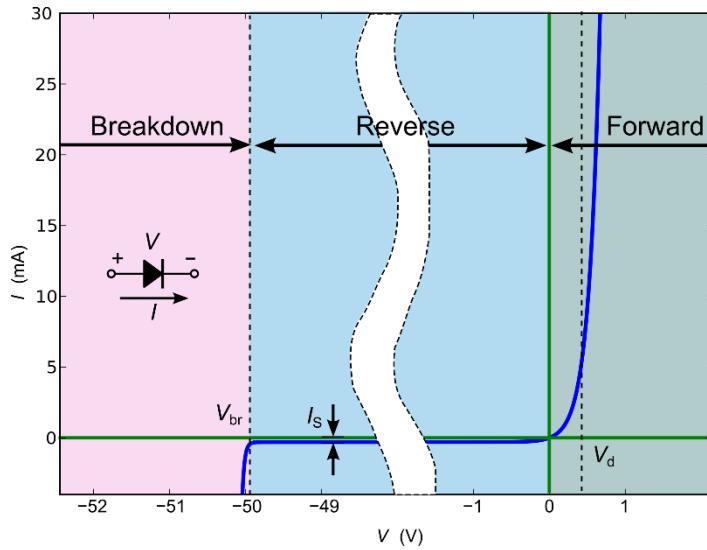
# Diode Bridge T/R Switch

- Diode bridge provides isolation of input and output voltages.
- Passive clamping of output voltage during transmit (or when high voltages present).
- Output mirrors input voltage during receive (or when low voltages present).
- Glass clipping clamping diodes provide further protection of output voltage.

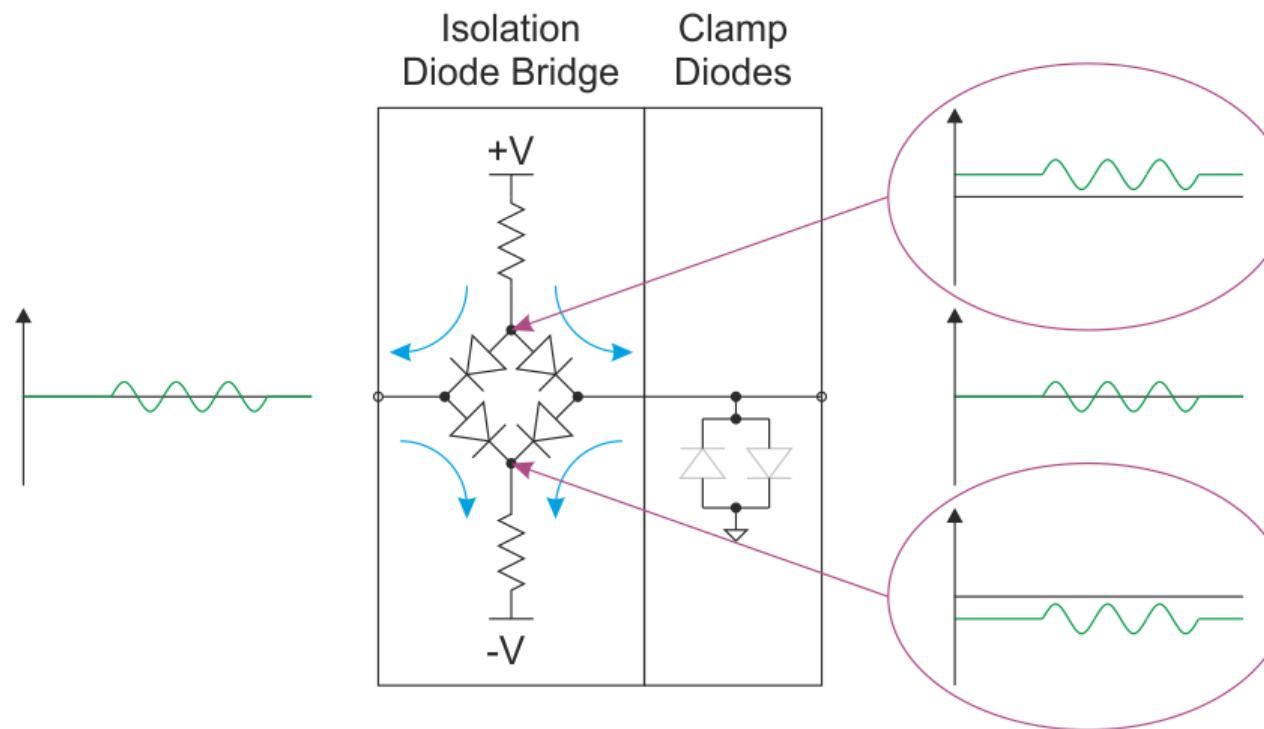


# Diode Bridge T/R Switch: RX

- All isolation bridge diodes are **forward biased**.
- Clamp diodes are less than forward voltage – nominally non-conducting.
- Output voltage mirrors input voltage.

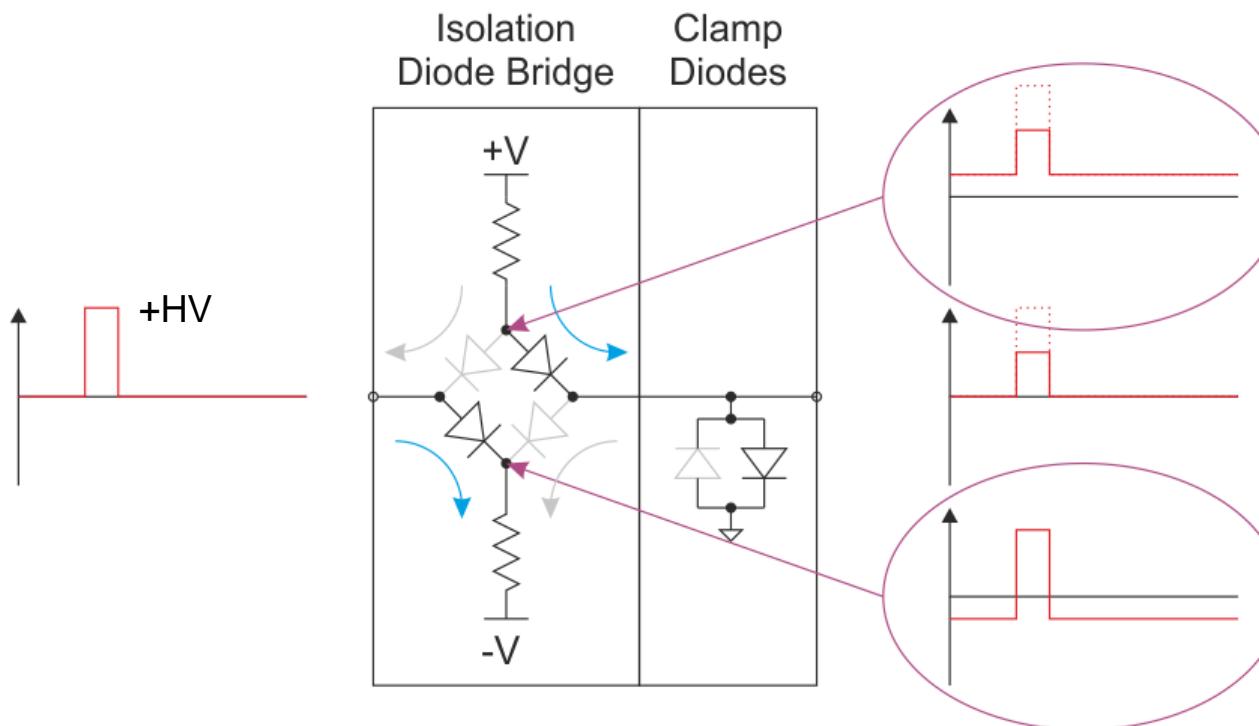
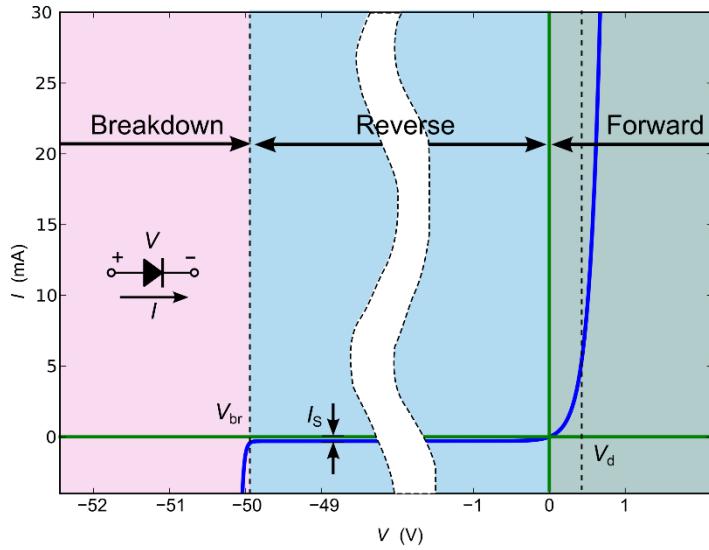


By User:Hldsc - Own work, CC BY-SA 4.0  
<https://commons.wikimedia.org/w/index.php?curid=27168067>



# Diode Bridge T/R Switch: +TX

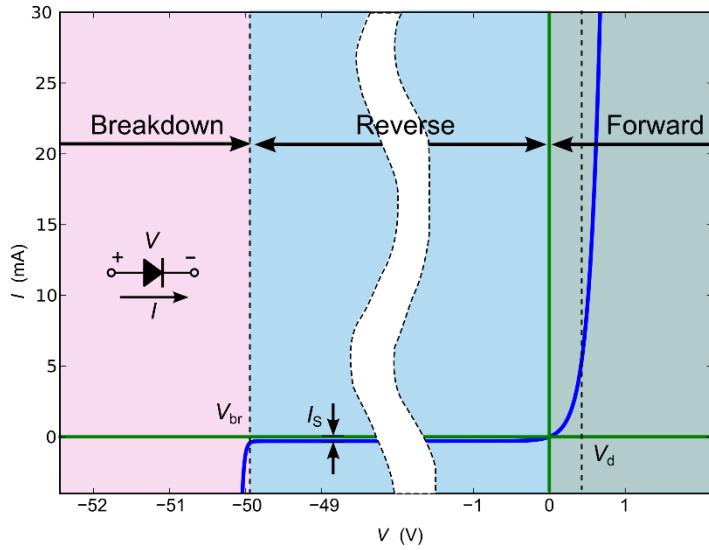
- Input voltage high enough to **reverse bias** bridge diodes.
- Positive supply drives output positive.
- Clamp diodes restrict output voltage to safe level.



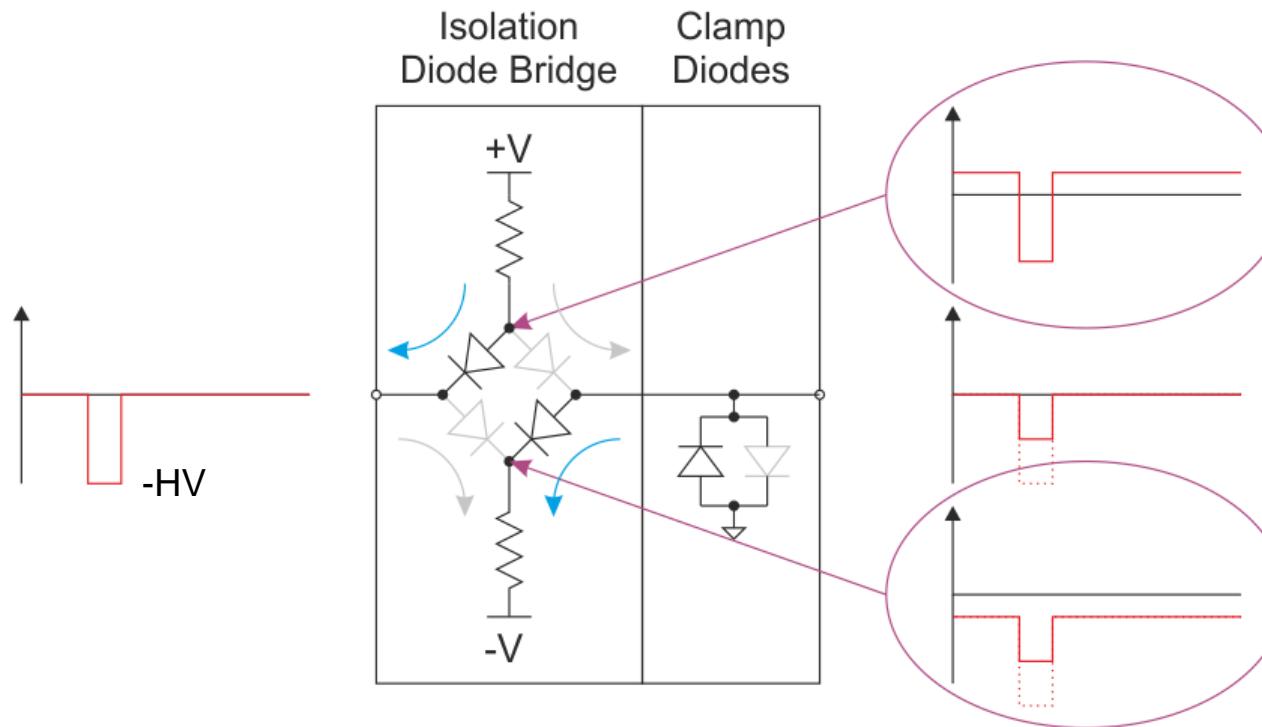
By User:Hldsc - Own work, CC BY-SA 4.0  
<https://commons.wikimedia.org/w/index.php?curid=27168067>

# Diode Bridge T/R Switch: -TX

- Input voltage low enough to **reverse bias** bridge diodes.
- Negative supply drives output negative.
- Clamp diodes restrict output voltage to safe level.

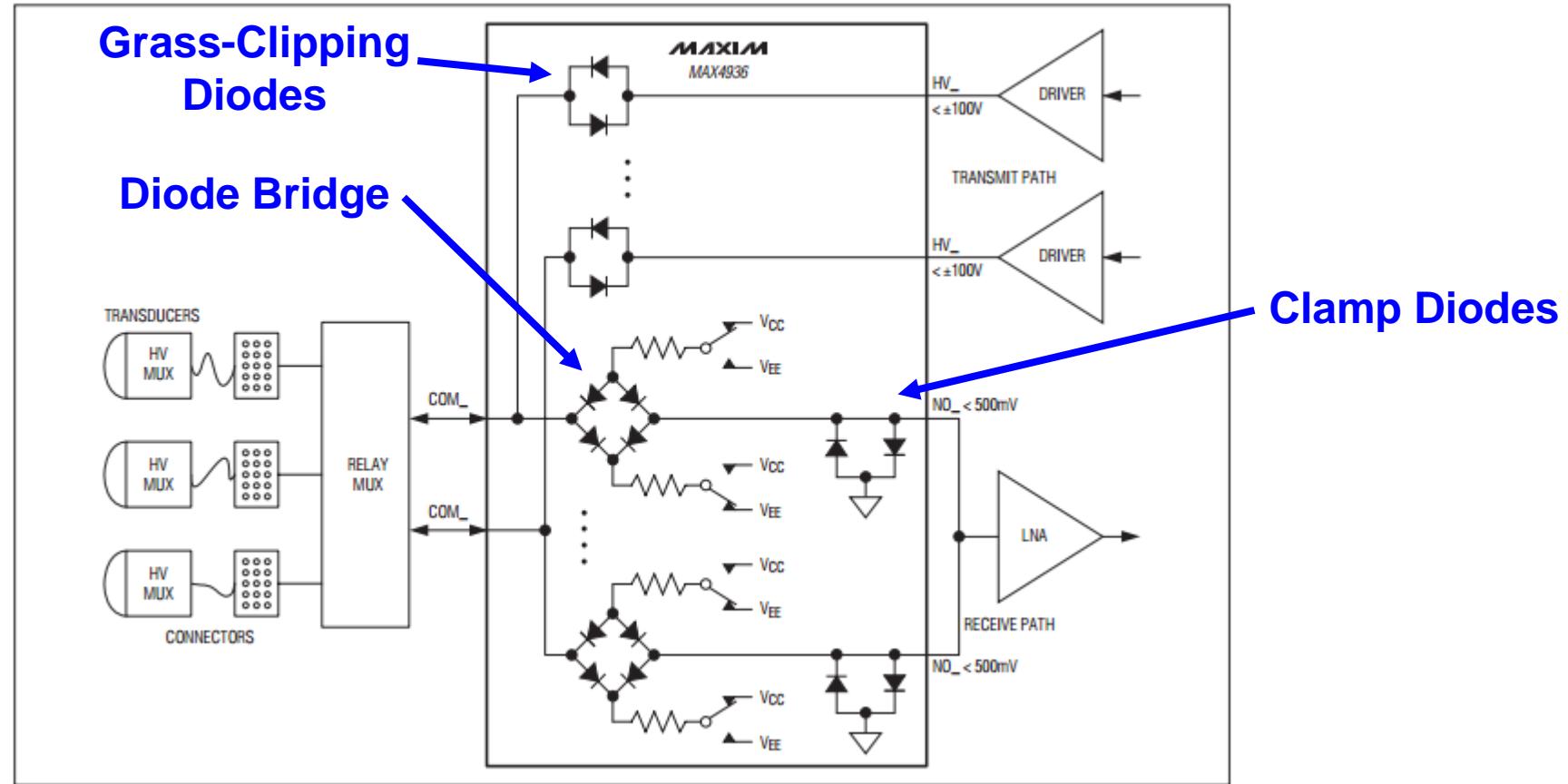


By User:Hldsc - Own work, CC BY-SA 4.0  
<https://commons.wikimedia.org/w/index.php?curid=27168067>



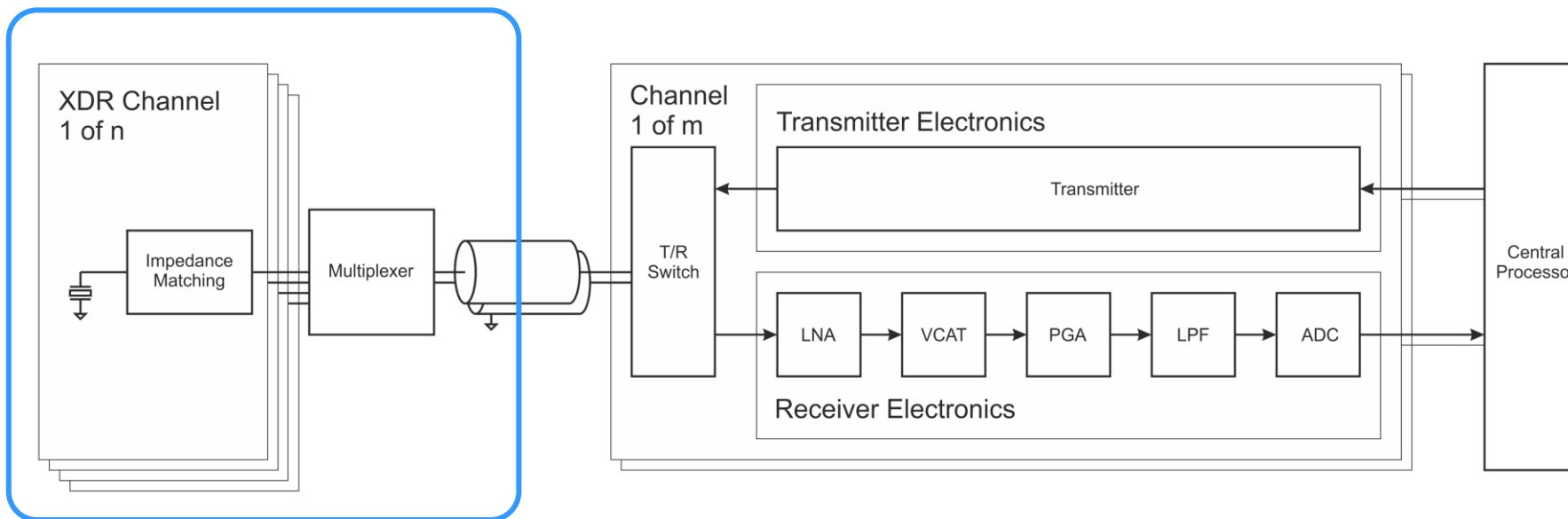
# Commercial Chipsets

## Octal T/R – Maxim – MAX4936



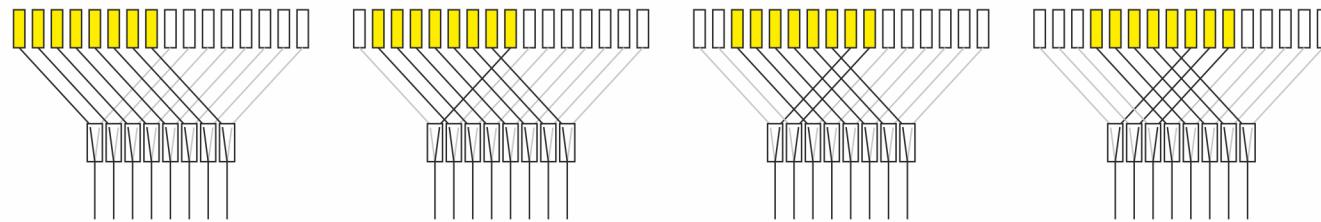
# Multiplexers

## Transducer



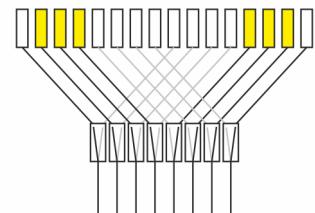
# Multiplexers

- Example 256 element commercial linear probe.
- Multiplex [1 128], [2 129]... [127 255], [128 256]
- Any single aperture up to 128 consecutive channels.

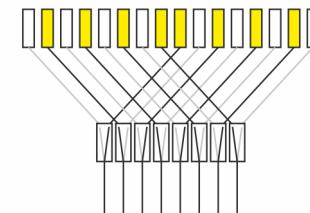


- Within mapping limitations it is also possible to create:

**Multiple apertures**



**Sparse arrays**

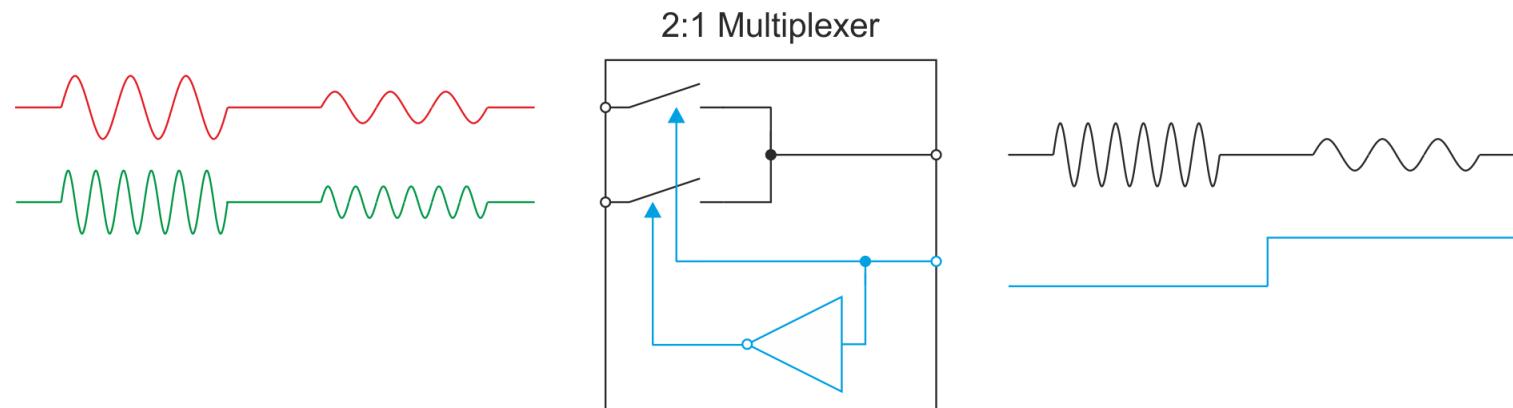


# Time domain multiplexers

- Allow transducer elements to connect to a reduced number of TX/RX channels/cables
- Time domain switching of active elements between measurements.

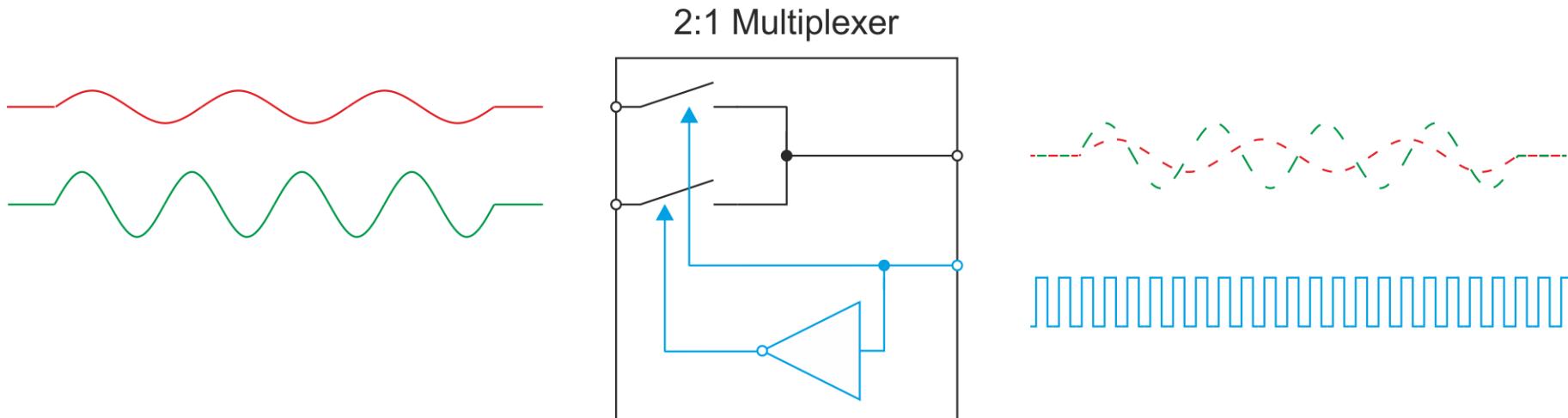
**Switching frequency < Pulse Repetition Frequency**

- Limits techniques like full matrix capture as only a subset of elements can be concurrently addressed.
- A multiplexer switch must exhibit high voltage tolerance, high bandwidth, low distortion and low jitter characteristics.

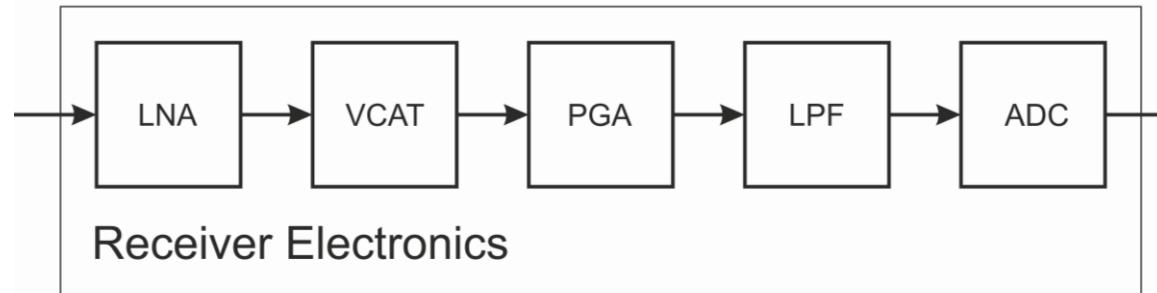


# HF time domain multiplexer

- High frequency time domain modulation (TDM).
- Concurrent sampling of multiple signals.
- Increased signal bandwidth down a single coax cable.
- Requires high speed analog to digital converter in receiver.
- ‘Moving the ADC sample and hold buffer into the handle’.



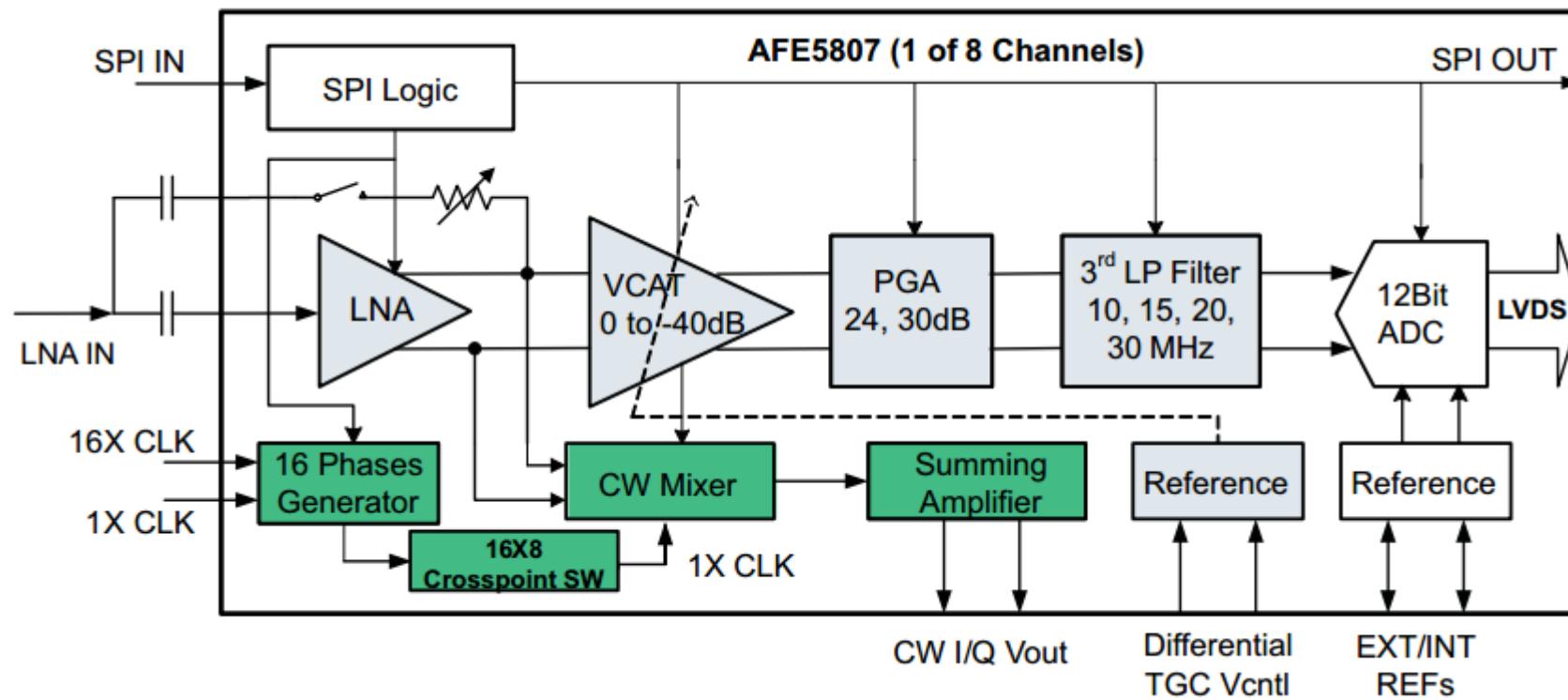
# Analog Front End (AFE)



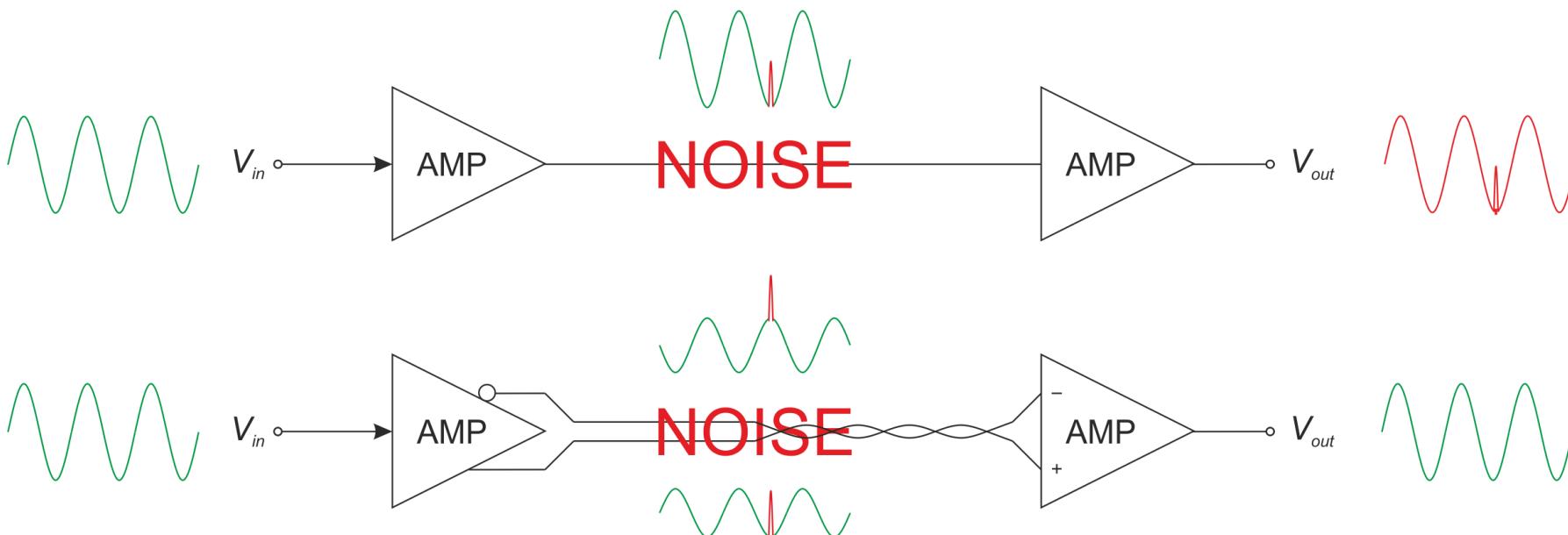
- **LNA** Low Noise Amplifier
- **VCAT** Voltage Controlled Attenuator (Time Gain Compensation)
- **PGA** Programmable Gain Amplifier
- **LPF** Low Pass Filter (Anti-aliasing filter)
- **ADC** Analog to Digital Converter

# Commercial AFE Chipsets

## Texas Instruments - AFE5807



# Differential signalling



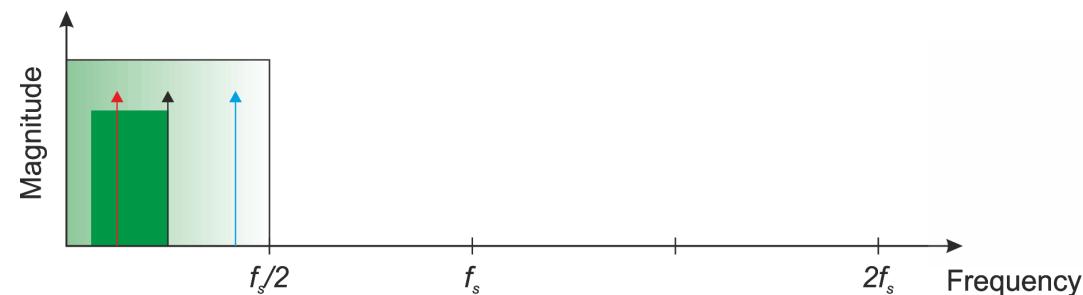
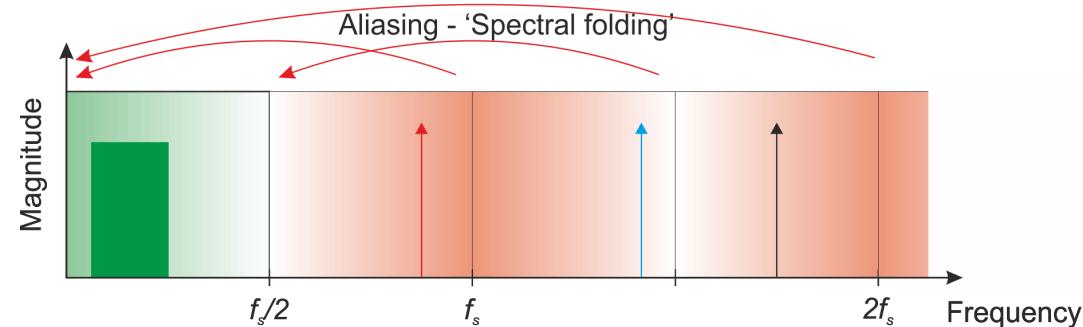
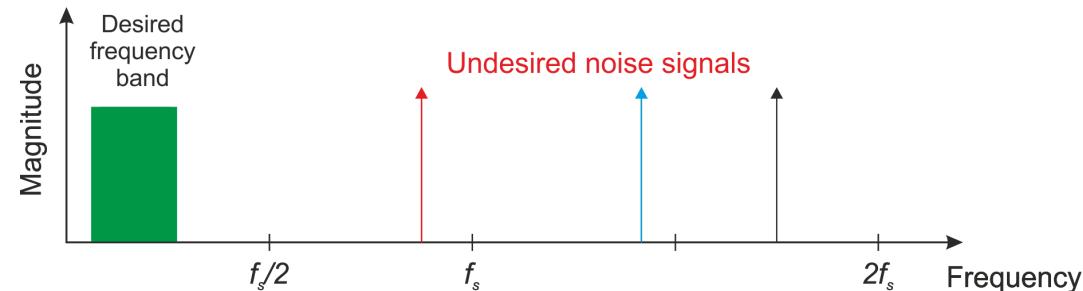
- Differential signalling reduces noise in transmission of signals in electrically noisy environments.
- A signal is transmitted along with its inverse signal through a close couple path (IC, PCB trace, twisted pair cable) where signals on both paths are subjected to equal additive noise.
- Original signal is recovered at receiver by subtracting the negative signal from the positive signal.
- $\text{Signal} - \text{negative Signal} = 2 \times \text{Signal.}$        $\text{Noise} - \text{Noise} = 0$

# Sampling Theory

- Nyquist frequency  $f_n$
- Sampling frequency  $f_s$

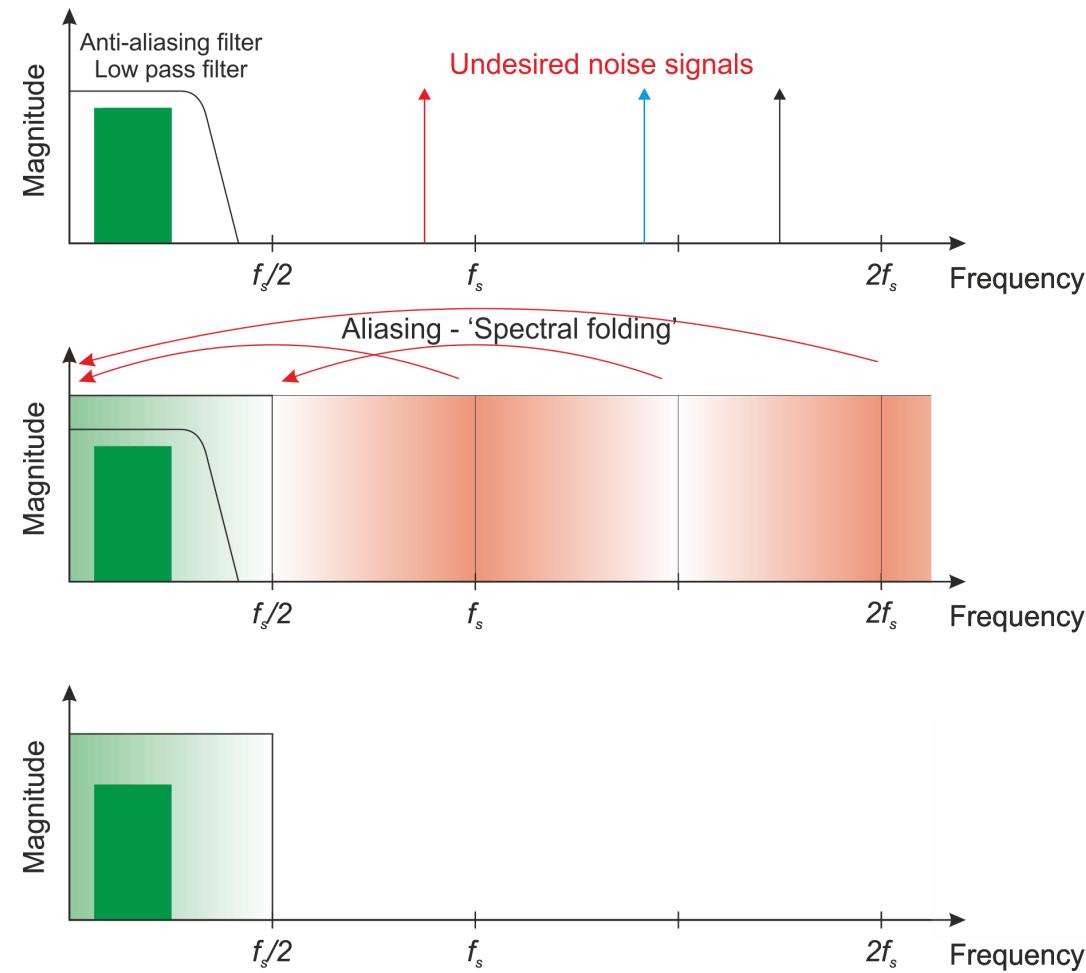
$$f_n = \frac{f_s}{2}$$

- Beyond  $f_n$  frequencies alias of fold into the region zero to  $f_n$ .
- Digital filtering cannot be used to remove aliased frequencies.



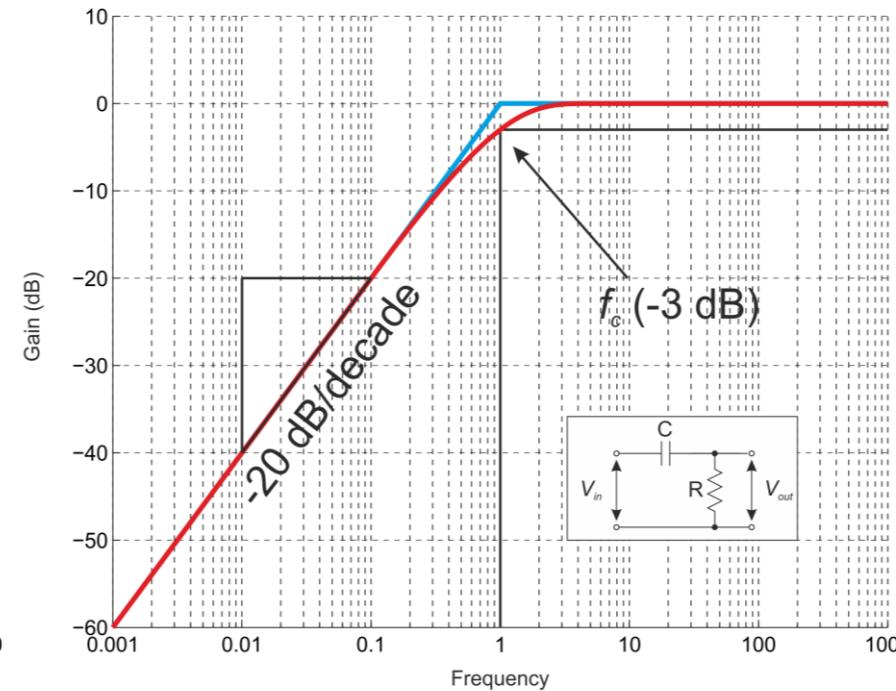
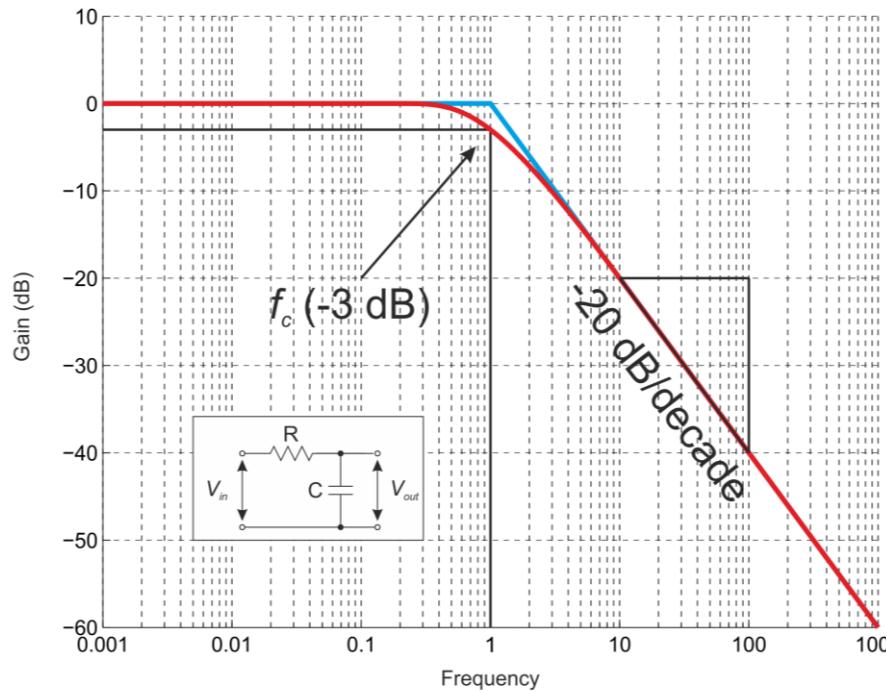
# Anti-aliasing filter

- Prevention of aliasing requires analog filtering to be performed before the input to the ADC.
- The filter should be designed such that undesired frequencies are sufficiently suppressed before sampling.
- Sampling where the frequencies of interest are below the Nyquist frequency is termed oversampling
- Give consideration to parasitics when designing analog filters.



# Passive Filtering

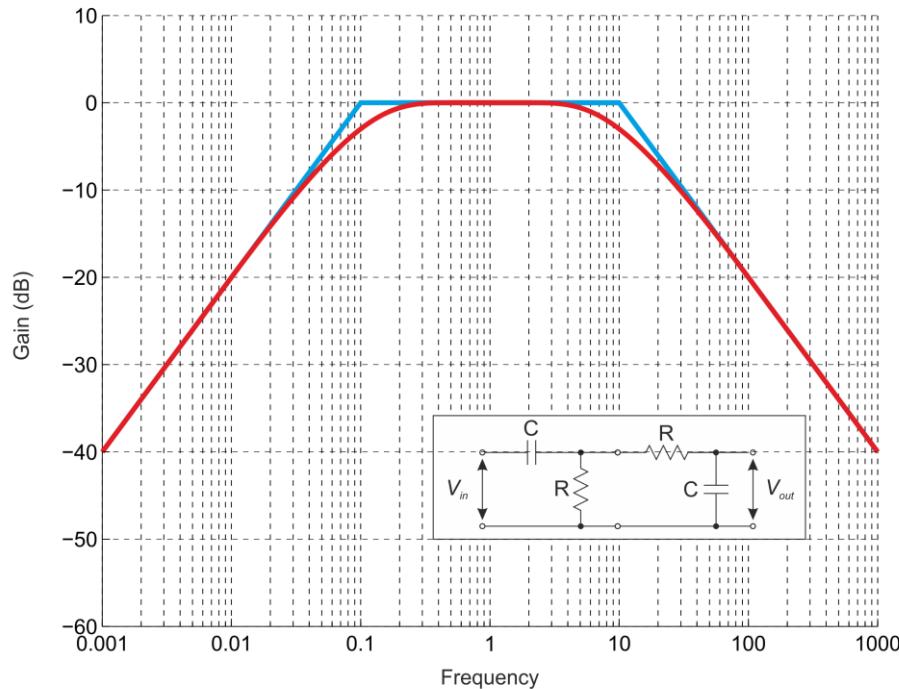
## Low Pass, High Pass



- The cut-off frequency,  $f_c = \frac{1}{2\pi RC}$ , defines the point of -3dB gain.
- Beyond the -3dB point, attenuation of -20 dB per decade frequency (roll-off)
- Cascade multiple stages for increased roll-off or bandpass and bandstop responses.
- Be aware of parasitic in lumped components – especially at high frequencies.

# Analog Passive Filtering

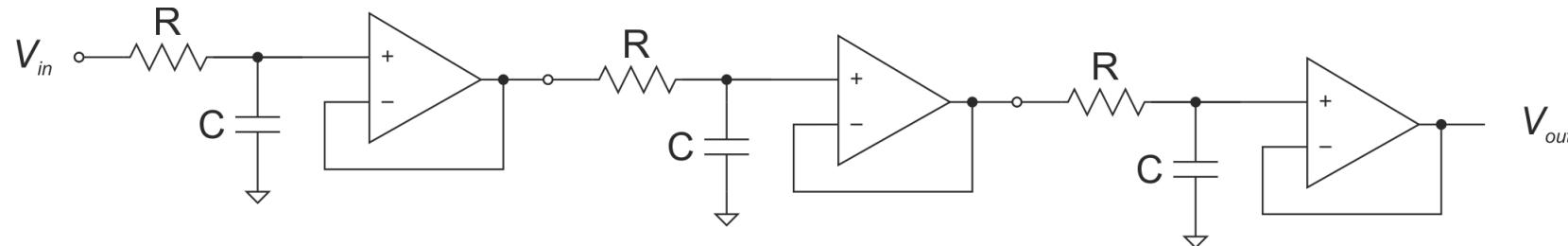
## Cascaded Band Pass



- Multiple filter stages can be cascaded to form more complex filters.
- A band pass filters can be constructed by combining a low and high pass filter.
- Multiple cascaded low or high pass filters may result in a steeper roll-off.
- Beware of loading effects due to impedance of passive filters in series.
- Amplifier buffers may be required between stages to maintain desired impedance characteristics.

# Active Filtering

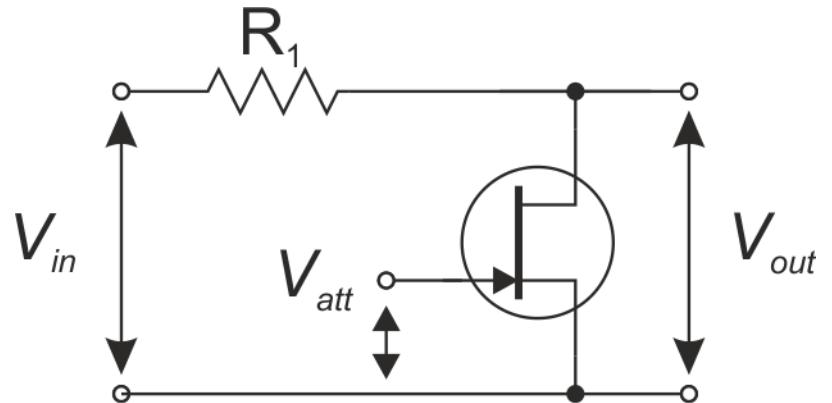
## 3<sup>rd</sup> Order Low Pass



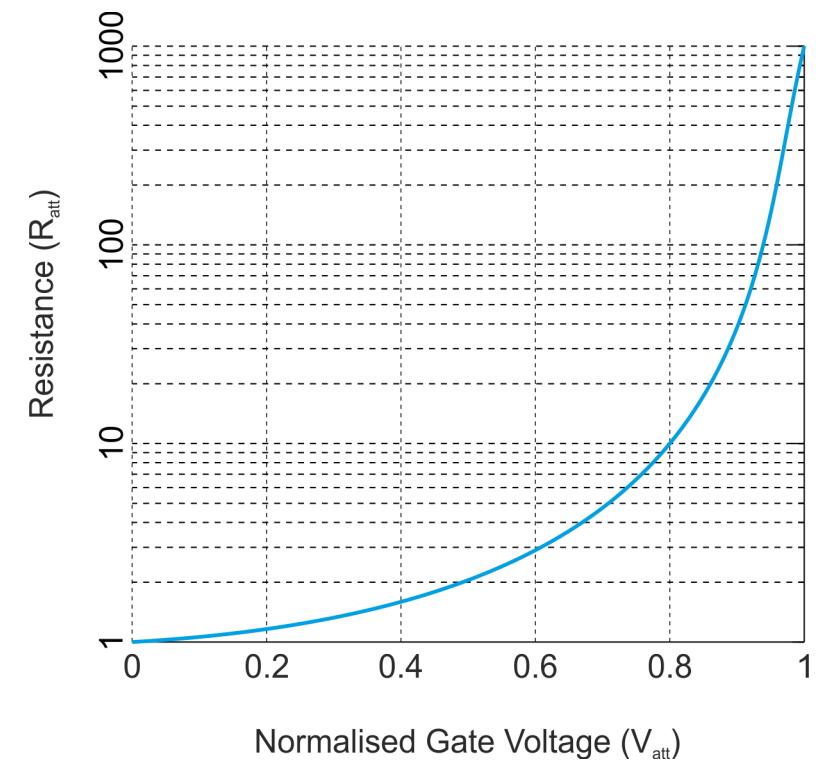
- Op-amps configured as unity gain buffers
- Are voltage followers:  $V_{out} = V_{in}$
- High input impedance at the non-inverting input (+)
- Low output impedance to drive successive filter stages
- Input impedance is that of first the first stage RC filter

# Time Gain Compensation (TGC) Voltage Controlled Attenuator (VCA)

- Typically implemented as a combination of fixed gain amplifier and time varying attenuation
- Voltage Controlled Attenuator (VGA) created using a voltage divider.
- Resistance between drain and source terminals of a Field Effect Transistor ( $R_{att}$ ) can be controlled by varying gate voltage - Voltage Controlled Resistor (VCR)
- Control signal manipulated to produce controlled voltage-attenuation profile.
- Digital to analog converter used to control VGA and perform TGC.



$$V_{out} = V_{in} \frac{R_{att}}{R_1 + R_{att}}$$



# Simplified ADC Input

## Sample

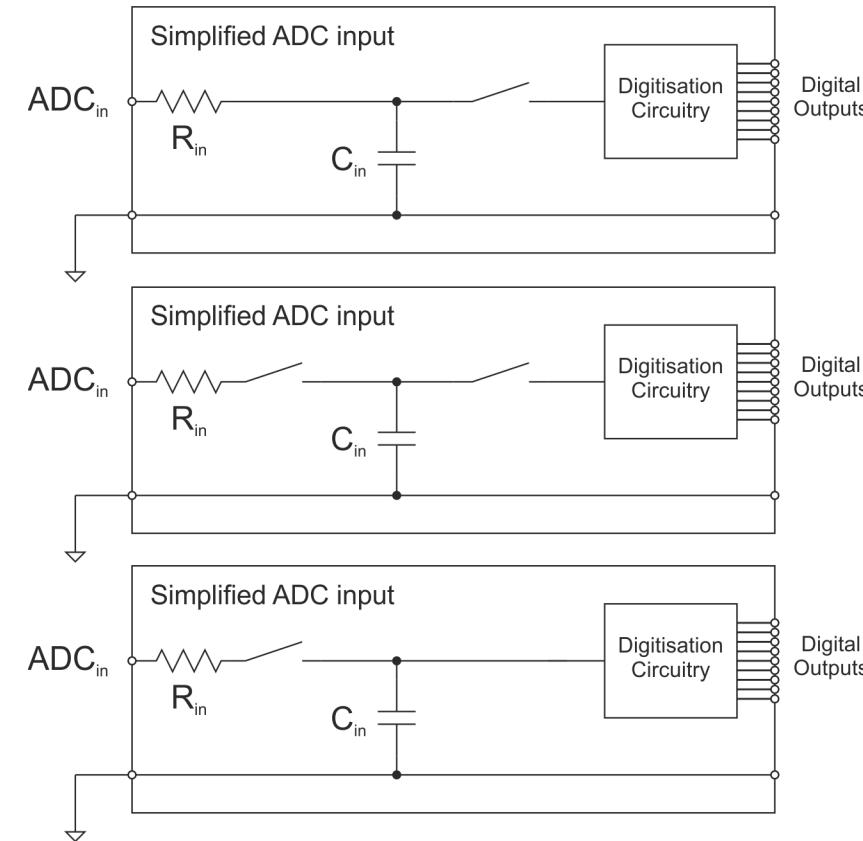
Charge input capacitor via input resistor  
and wait for voltage to stabilise

## Hold

Disconnect input resistor

## Convert

Connect input capacitor to digitisation circuitry



- **Input resistor typically kilohms ( $k\Omega$ ), Input capacitor typically picofarads ( $pF$ ).**
- **Input typically acts as a low pass filter with very high cut off frequency.**
- **Input not matched to characteristic impedance - Buffering or matching required!**

# Sampling theory

## Ideal Signal to Noise Ratio (SNR)

$$\text{SNR} = 6.02n + 1.76$$

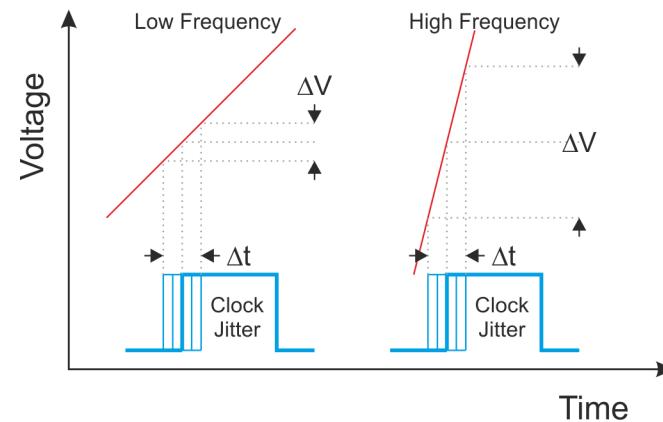
where  $n$  is the number of bits

$n$ (bits)	Ideal SNR (dB)
8	49.92
10	61.96
12	74.00
14	86.04
16	98.08

- SNR should be greater than the desired dynamic range of the imaging system.
- **Ideal SNR can never be achieved in a practical system**

# Sampling clock jitter and SNR

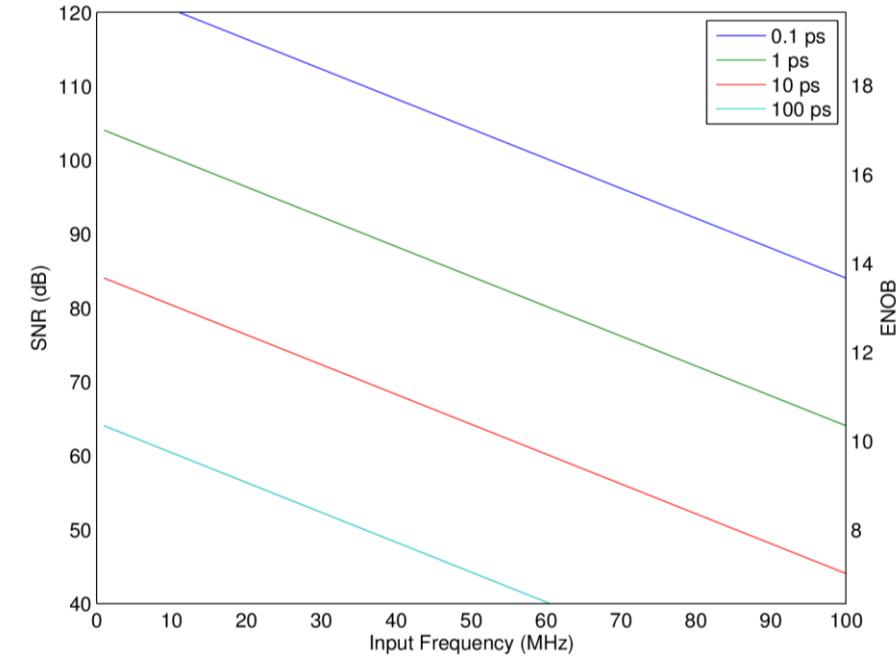
- SNR should be greater than the desired dynamic range of the system.
- Ideal SNR can never be achieved in a practical system.
- Clock jitter is a time deviation for the ideal period clock crossing point



$$\text{SNR} = -20 \log_{10}(2\pi f_{in} t_j)$$

$f_{in}$  Input frequency (Hz)

$t_j$  Sampling Clock Jitter (s)



e.g. 50 MHz input to 14 bit ADC requires clock jitter <1 ps – 16 bit requires 100 fs!

**Jitter is not dependent on sampling frequency!**

# Thank you!

