Dante Crescenzi

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Education

University of Toronto Toronto, ON
B.A.Sc Computer Engineering *Sept 2020 – June 2025*

- Achieved a *3.99/4.0* Cumulative GPA and *94%* Cumulative average
- Awarded Dept. of Electrical and Computer Engineering *Top Student Award* (2020/21, 2021/22, 2022/23)
- Received Charles Edwin Trim (2022), 2 x Wallberg Undergraduate (2021, 2022) *Scholarships*

Experience

Incoming Hardware Engineer August 2025
IMC Trading *Chicago, IL*

Hardware Engineer Intern June 2024 – August 2024
IMC Trading *Chicago, IL*

- Implemented elements of low-latency trading systems, improving performance, reliability and flexibility.
- Contributed to the development of both software, hardware, and their integration.

FPGA Software Engineer Intern May 2023 – June 2024
Intel *Toronto, ON*

- Worked within the Synthesis team of the Quartus Prime compiler developing high-performance C++ to contribute to increasing Fmax and lowering area through the application of diverse netlist optimization techniques.
- Identified and resolved a 5% runtime increase on the synthesis stage of the Quartus Prime compiler by conducting in-depth analysis and implementing different optimization strategies.
- Developed an internal testing tool aimed at generating randomized designs to rigorously stress test Synthesis optimizations, significantly enhancing the reliability and performance of Synthesis results.

Software Developer Intern May 2022 – Sept 2022
Oracle *Remote*

- Contributed to the successful development and launch of Oracle's new ERP service, NetSuite Next, by playing a key role in various aspects of its construction.
- Helped design and implement document transformation flows between various financial records as a member of the Order-To-Cash team at NetSuite.

Software Engineer Intern May 2021 – Sept 2021
PointClickCare *Remote*

- Led a comprehensive refactoring initiative to streamline the connection interface between testing infrastructure and relevant databases, resulting in a significant simplification of 120+ unit tests and improved code readability.
- Collaborated with a team of testing automation engineers to elevate the team's test coverage from 81% to 97%.

Projects

Custom Pipelined Processor - *Verilog, Quartus*
FPGA CNN Accelerator Utilities - *SystemVerilog, Verilator, Quartus*
SmallC Compiler - *C++, ANTLR4, LLVM*
User-Level Thread Package - *C, Linux*
Hashtable library for C with Custom Testing Framework - *C, Linux, Python*
Raft Consensus Algorithm Implementation - *Go*
Random HDL design generator for Synthesis stress testing - *Modern C++, Various HDLs, Python, Quartus*
Geographic Information System - *Modern C++, Gtk, Linux*

Technical Skills

Languages: Modern C++, C, SystemVerilog, Go, Python, x86 & ARM v7 Assembly, Java, SQL
Software/Hardware Courses: Algorithms & Data Structures, Operating Systems, Computer Architechture, Computer Networking, Compilers & Interpreters, Software Design, High Performance Computing, Digital Systems
Math Courses: Probability, Multivariable Calculus, Linear Algebra, Complex Analysis & Differential Equations