Derek C. **Welty**

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Summary

Senior Electrical Engineer with over 12 years of experience in the electronics industry working in all phases of the product development life cycle. Possesses a Master's degree in Electrical Engineering and a broad set of skills and experiences ranging from early prototyping to PCB design to system architecture to validation and mass production. Highly self-motivated and solution-oriented team player with a growth mindset and passion for technical problem solving and process improvements.

Experience

Systems Engineering Lead
San Francisco, CA

eero LLC
June 2025 – Present

- Led system-level architecture and electrical design for multi-SKU wired networking platforms, defining platform tenets across performance, integration, and scalability
- Partnered with product teams and cross-functional engineering groups to shape system requirements, evaluate architecture options, and drive high-impact trade-off decisions across cost, schedule, and performance
- Directed NPI engagement with a newly onboarded contract manufacturer, shaping the engagement model, build-readiness expectations, and cross-team technical workflows

Senior Display Electrical Engineer
Cupertino, CA

Apple Inc.
Nov 2023 – Feb 2025

- Implemented electrical designs for displays through BOM component selection, schematic creation, directing layout, simulation, and bring-up/debugging circuits in the lab
- Collaborated with a large number of cross-functional groups including PD, DFM, RF, SW, HW Test, System, and EPM to bring a product from concept to mass production
- Defined test criteria and executed test plans on functional prototypes to demonstrate design robustness
- Led external vendors through NPI including build readiness, quality improvements, and root cause FACA analysis

Senior Electrical Engineer
Redmond, WA

Microsoft Corporation
Jan 2022 – Oct 2023

- Led and managed high volume product design decisions, team members, vendors, and partners
- Motherboard PCBA lead driving sound technical solutions through large cross-disciplinary teams including Power/Thermal, Power Delivery, Silicon, HSIO, LSIO, RF, Wireless, Desense, AV, ME, SW/FW, DFM, Memory, Storage, and HW test
- Led the successful integration of a critical piece of custom silicon from tapeout to full system validation
- Responsible for XBOX console schematic integration, board layout design, and BOM management
- Drove system definition, validation, and bug triage to ensure quality, cost, schedule targets are all met

Senior Design Verification Engineer
Redmond, WA

Microsoft Corporation
Sept 2019 – Jan 2022

- Owned targeted verification of XBOX systems and subsystems including SoC power management firmware
- Designed, integrated, and maintained automated test systems (Python, PowerShell, C++)
- Performed hardware prototype bring-up, debugging, failure analysis, and telemetry forensics
- Formulated statistical techniques to analyze large data sets and design experiments
- Triaged and diagnosed countless high priority issues leading to increased customer experience and factory yield

Senior Design Engineer
Olathe, KS

Garmin International
Mar 2017 – Sept 2019

- Conceptualized and delivered automotive mass production consumer infotainment electronics
- Designed schematics and developed complex rigid/flex printed circuit boards with analog, digital, high-speed, audio, display, camera, wireless, DC-DC power, capacitive multi-touch and RF circuitry
- Project Engineer leading system design and coordinating interdisciplinary collaboration across teams
- Researched components for ideal part selection and BOM management while balancing performance and cost
- Directed and collaborated with factory team in Taiwan to design for testing and manufacturability
- Tested and debugged field hardware/software issues for technical root cause and corrective actions

Electrical Engineer I/II/III
Kansas City, MO

DOE National Security Campus, Managed by Honeywell
Jan 2013 – Mar 2017

- Lead test engineer architecting/implementing hardware/software solutions for scalable test infrastructure
- Defined test plans and electrical verification methodologies for board level and top-level systems
- Integrated FPGA and CPLD designs into motherboard designs for embedded control and testing
- Interfaced with government customers and supported earned value management project planning

Network Engineer Intern *Overland Park, KS*

Sprint Nextel Corporation *May 2012 – Aug 2012*

- Designed and implemented a VoIP Android IMS client using Java
- Debugged client/server communications by analyzing network packets and protocols
- Utilized network and streaming protocols such as UDP, SIP, and RTP

Education

MS in Electrical Engineering ***GPA: 4.00/4.00***

Missouri University of Science & Technology *Aug 2013 – May 2018*

Digital Network Design, Wireless Networks, Resilient Networks, Network Performance Analysis and Modeling, Stochastic Signal Analysis, Power Electronics, Advanced Electromagnetics, Microwave Engineering, Analog CMOS Design

BS in Electrical Engineering, Minor in Mathematics ***GPA: 3.93/4.00***

Missouri University of Science & Technology *Aug 2008 – Dec 2012*

IEEE, Eta Kappa Nu, Missouri Miner Photo Editor, Student Union Board Promotions Director

Skills

Protocols Ethernet, USB, WiFi, BT, I2C, SPI, HDMI, MIPI, GPS, UART, PCIe, CAN, LCD/XGA

Programming Python, PowerShell, VB.NET, Java, MATLAB, Arduino, Git, Subversion, TestStand, ADB, VISA

Lab Equipment Oscilloscopes, multimeters, spectrum/network/logic analyzers, power supplies, Raspberry Pi, Arduino, PXI, DAQ

Software Tools Schematic capture, PCB layout, Mentor Graphics, CADSTAR, OrCad, Cadence, Allegro, SPICE, Solidworks

Extra Training Advanced GNSS/GPS, Radar Systems Certificate, MIL-STD 1553, Six Sigma Green Belt

Graphic Design Adobe Photoshop, Adobe Illustrator, LaTeX, HTML, CSS, Bootstrap

Miscellaneous MS Office, Android, Linux, Windows, Atlassian suite, Azure DevOps

Awards & Patents

2016 **Outstanding Engineer Award**, Honeywell Aerospace

2019 **US10447297B1**, Electronic Device and Method for Compressing Sampled Data