A 1.29GHz 251.16fJ
6-bit Absolute-Value Detector

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Design Summary

- **Circuit topology:** (Multiplexors/Invertors) followed by a Carry-Propagate Comparator
- **Circuit Style: all static CMOS**
- **C) WHY:**

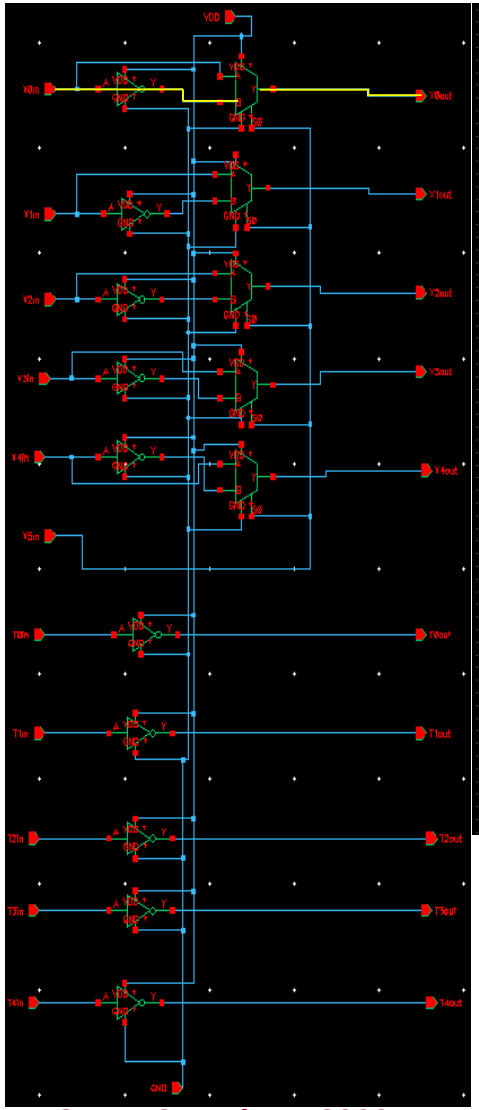
  -use of carry-propagate as comparator reduces the total number of gates and transistors, making better use of area and using less power (compared to the normal comparator)

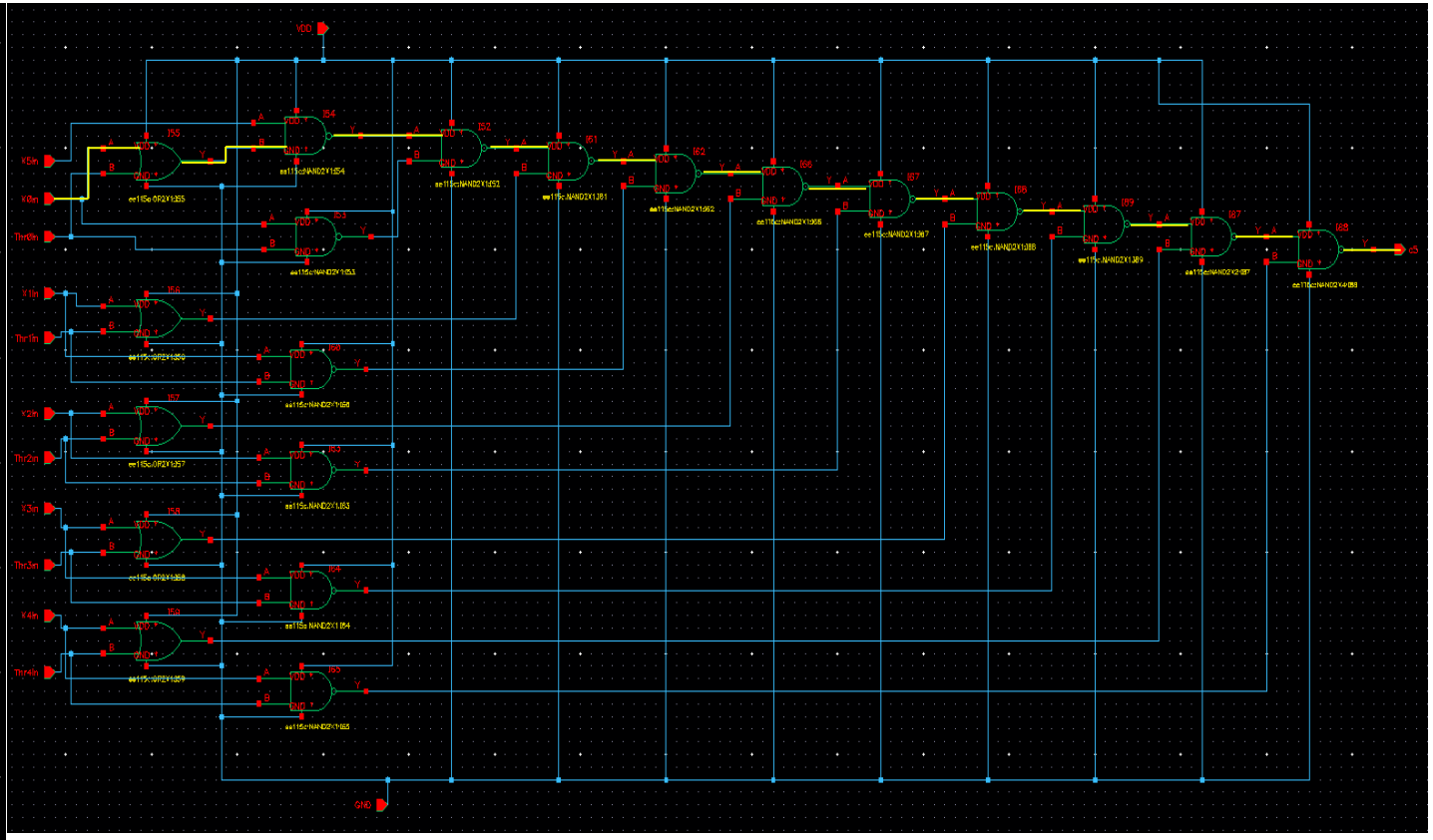
  -carry-propagate comparator allows for regular design (repeated use of NAND gates)

Delay	Layout size	Energy	Verification
Sch. t_p = 772.95ps	X= 15.815µm, Y= 26.965µm	Sch. E = 187.22fJ	Func: Y
Lay. t_p = 749.95ps	A = 426.45µm^2	Lay. E = 251.16fJ	DRC: Y
Critical Input = X_0	AR = 1.7	Lay. V_{DD} = 0.69V	LVS: Y

*(assuming Vdd is fully optimized for a delay of ~775ps)

Critical Path Analysis





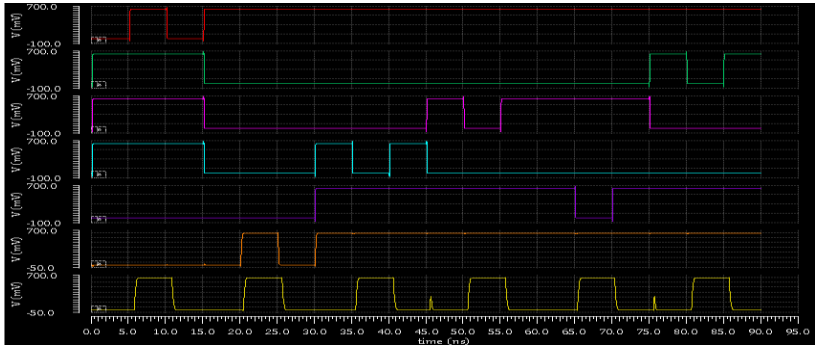
$$T_{crit} = T_{INV} + T_{MUX} + T_{OR} + 10T_{NAND}$$

Design Optimization

- Gate level critical path:
  -propagation from X_0 (if it changes) to C_5 (out)
  -majority of delay come from the chain of NAND gates
- MOS detail of gates, sizing, and optimization strategy:
  -mainly used standard cells from gsclib090
  -optimization strategies:
    -use of NANDs over NORs
      (however, standard cells have same logical effort)
      (lower T_{LH} than T_{HL}, and less energy in testbench)
    -buffering electrical fanout over last few gates
      (experimented and found it best to size last 2 NANDs x2 and x4)
  -note: if threshold were to change frequently, then power consumption would increase due to unconditional inversion of the threshold

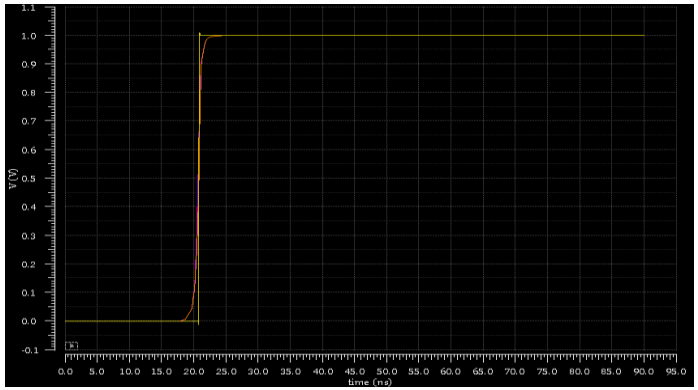
Functionality Check

- **Functionality (testbench)**



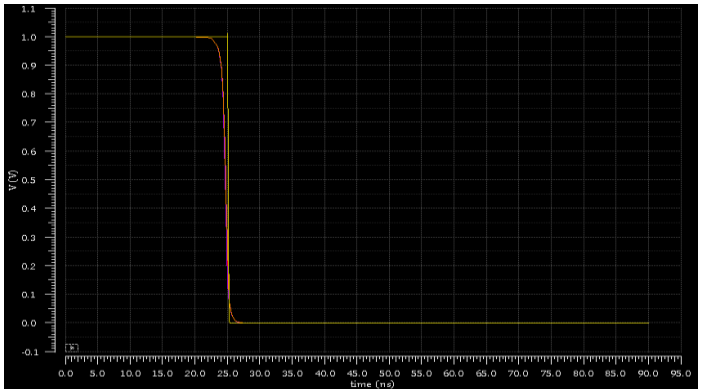
- **Worst-Case Delays (V_{dd} = 1)**

(T_{LH})



(X: 000000→111111)
(T = 000000)
(delay = 418ns)

(T_{HL})



(X: 111111→000000)
(T = 000000)
(delay = 458ns)

(Note: because of the use of NAND gates, T_{LH} is less than T_{HL})

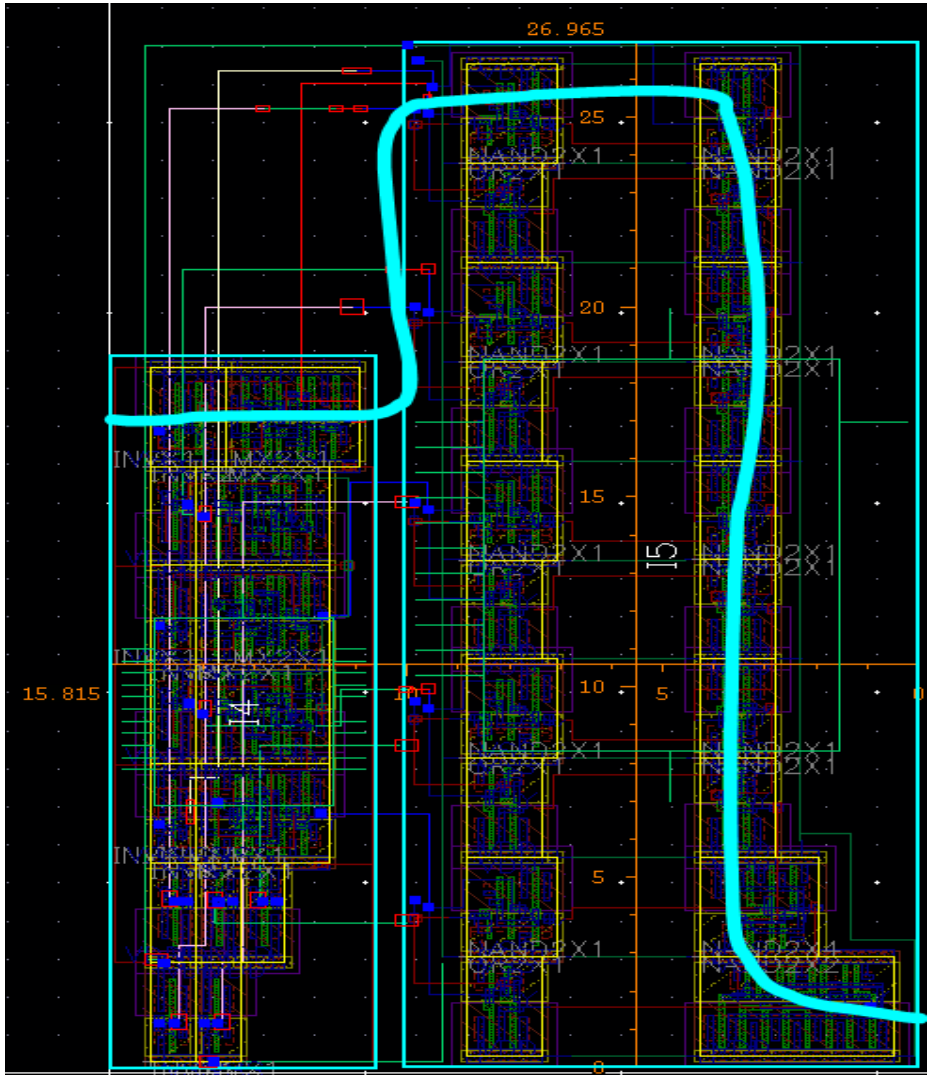
Absolute-Value Detector Layout

Size: X = 26.965µm
Y = 15.815µm

Area: 426.45µm²

Aspect Ratio: 1.7

Density: 60%



Discussion

Most Important Features of Our Design:

- Sizing of last few logic gates to better buffer the electrical fanout
- Highly regular use of NAND gates in comparator
- Minimal use of non-(invertor/NAND/NOR) logic gates to minimize number of transistors, power, and area in layout

Potential Improvements:

- Resizing gates
  (just halving the gate sizes cut down the energy by ~20fJ)
- Redo the layout of the comparator
  (much wasted space)
- Try to redesign the logic so that we can remove the invertors in the first stage
  (not much energy consumption since threshold has low switching frequency)
  (NOR-implemented comparator has higher energy consumption in current testbench)
  (would save some area for the layout by removing invertor logic gates)