

## ECE115C – Digital Electronic Circuits Project Testbench

This provides a method for you to test your design in Cadence. “ ” denotes a blank space explicitly.

1. Copy the test file **tb\_project.tar** to your working directory (default: ~/ee115c)

```
>cp /w/class.1/ee/ee115v/ee115vta/ee115c_w20/tb_project.tar  
~/ee115c
```

2. From your ~/ee115c directory, extract the archive with the following command:

```
>tar -xvf tb_project.tar
```

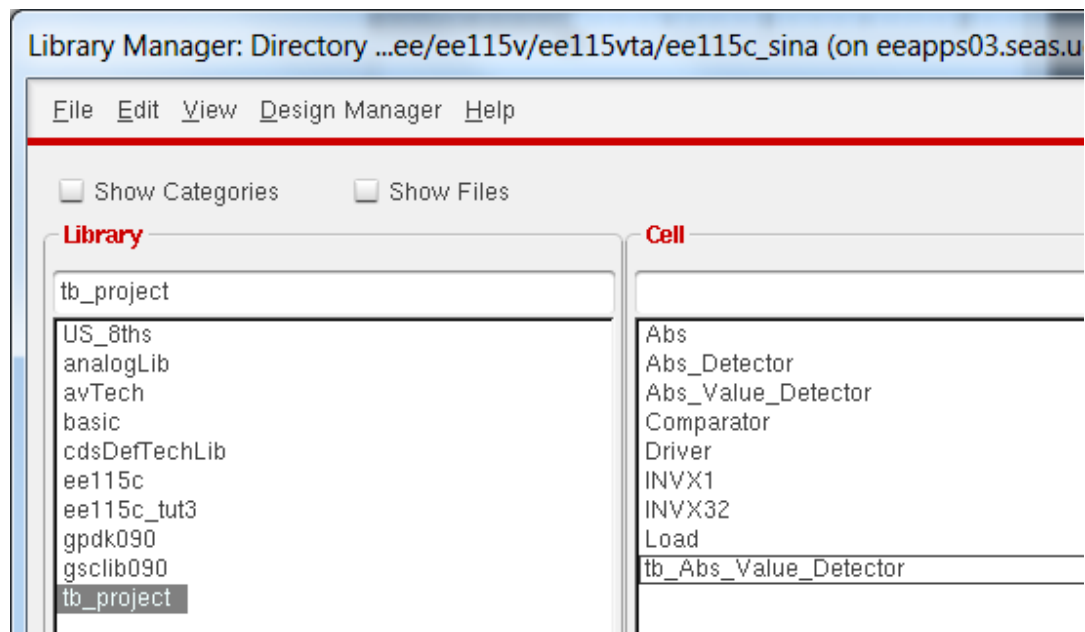
This would create a directory “**tb\_project**” under your working directory.

3. Edit **cds.lib** file in your working directory to add the following line at the end.

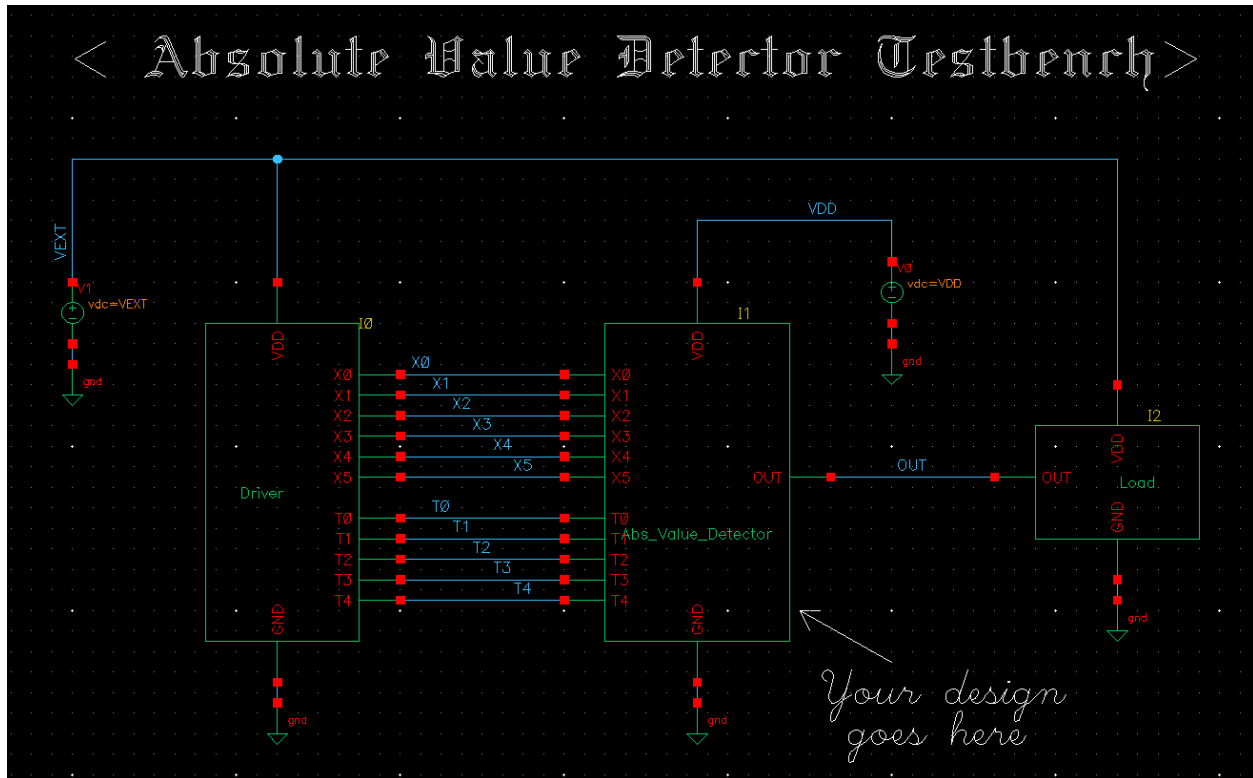
```
DEFINE tb_project ~/ee115c/tb_project
```

This tells Cadence to consider the directory we just copied as a Cadence library.

4. Now launch Cadence as usual. You should now see a new library test\_project.



Open the schematic “**tb\_Abs\_Value\_Detector**”.



Replace the “**Abs\_Value\_Detector**” (this is an example design) in the library “tb\_project” with your own absolute value detector design. Please make sure that your design is named “**Abs\_Value\_Detector**”. Also make sure that you have the following pins on your design:

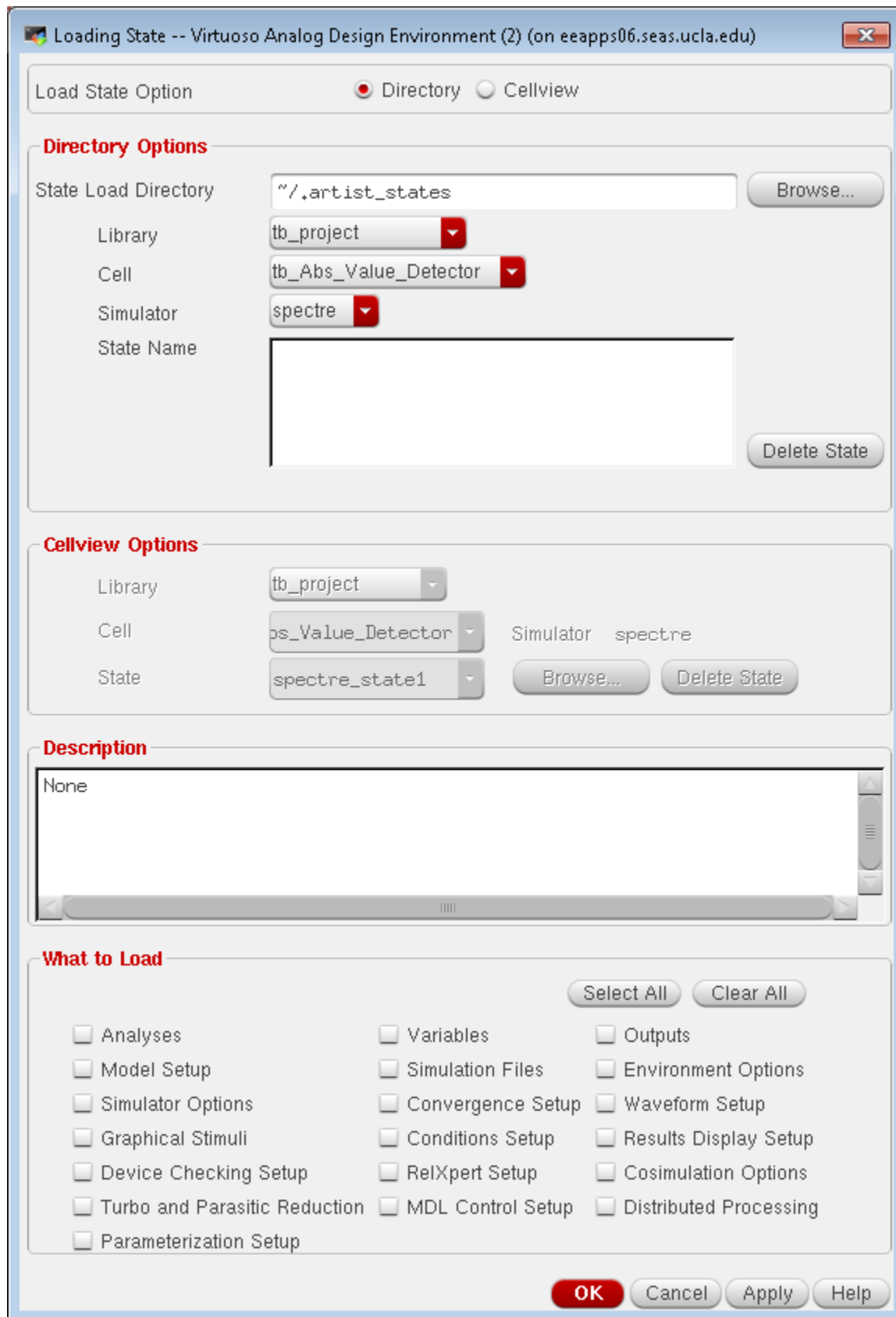
**X0, X1, X2, X3, X4, X5, T0, T1, T2, T3, T4, VDD, GND, and OUT.**

The above pins are case sensitive. It is important to maintain this consistency in your design name and pin names of the design, for the verification steps to be posted later. Please check the port names in the sample design provided with this testbench to verify that your design and port names are correct.

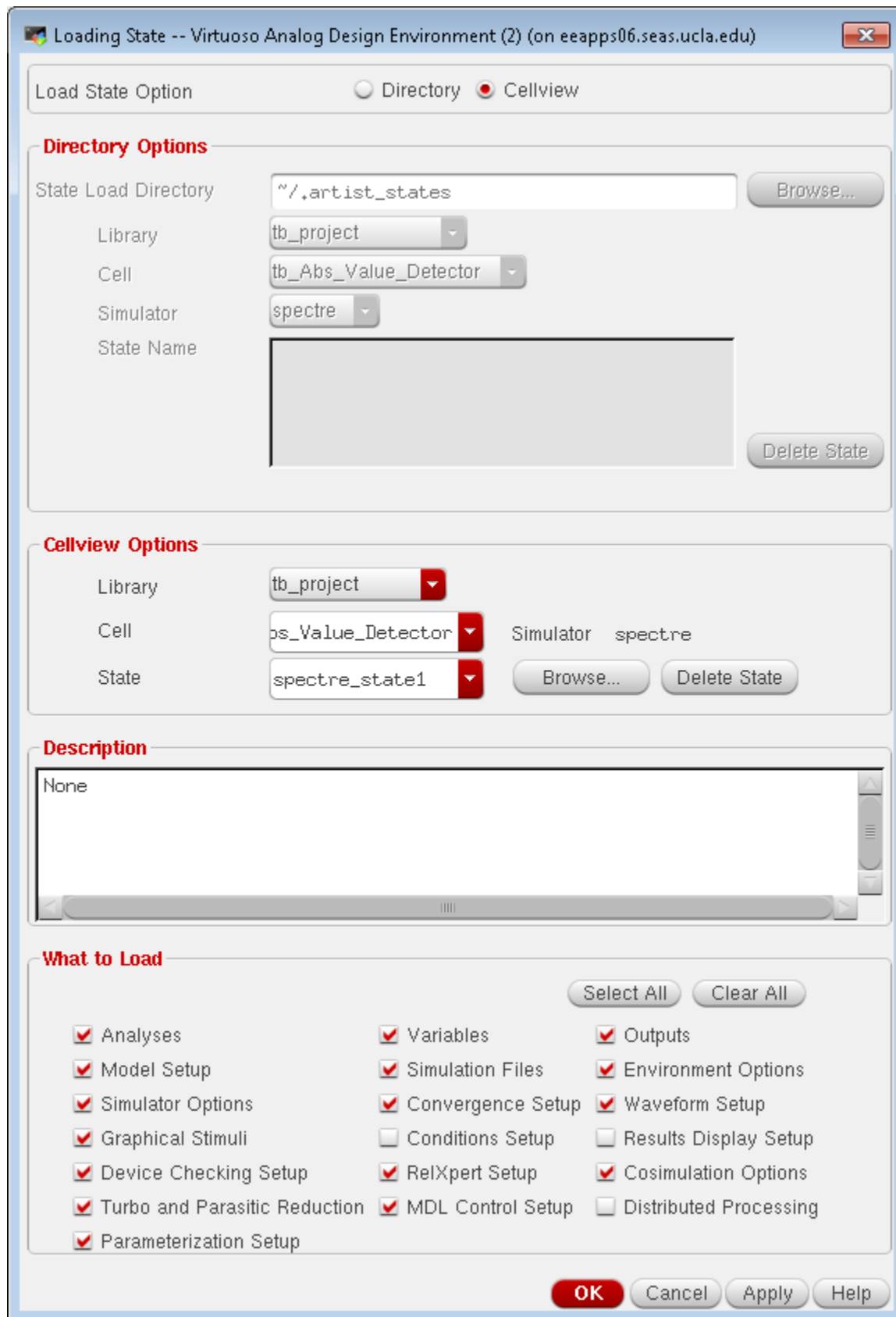
Note: Once you make sure that the pins names and design name is consistent, you can copy the schematic view of your Absolute Value Detector design to the “tb\_project” library. **You can still retain the symbol view** that you have been provided, to allow very easy replacement of the adder in the testbench schematic.

**Save** the schematic for “tb\_Abs\_Value\_Detector” after your design has been replaced.

Now in the schematic window of tb\_Abs\_Value\_Detector click “Launch → ADE I”. When Analog Design Environment opens, go to: “Session → Load State...”. The following window shows up.



Choose "Cellview" in "Load State Option", the window becomes:



The state “spectre\_state1” is just the simulation settings we need, click “OK”.

This will set the variables needed for the testbench, the outputs to be evaluated and the analysis to be performed.

The inputs include 16 transitions with input pattern changes due to the probability distribution given earlier in the project description. Another pattern due to the same probability distribution would be used to check your final submission later.

Now you can run the simulation. For the sample design given to you, operating at 1V, you will see an output as follows: (VDD and VEXT have to always match).

The screenshot shows the Cadence Virtuoso Analog Design Environment interface. The title bar indicates the project is 'tb\_project tb\_Abs\_Value\_Detector schematic (...)'. The menu bar includes Launch, Session, Setup, Analyses, Variables, Outputs, Simulation, and Results. The toolbar shows various icons for file operations and simulation control.

**Design Variables**

Name	Value
VDD	1
VEXT	1

**Analyses**

Type	Enable	Arguments
1 tran	<input checked="" type="checkbox"/>	0 90.1n moderate
2 dc	<input checked="" type="checkbox"/>	t

**Outputs**

Name/Signal/Expr	Value	Plot	Save	Save Options
1 X0		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	allv
2 X1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
3 X2		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
4 X3		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	allv
5 X4		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
6 X5		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	allv
7 OUT		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	allv
8 V0/MINUS		<input type="checkbox"/>	<input checked="" type="checkbox"/>	yes
9 V0/PLUS		<input type="checkbox"/>	<input checked="" type="checkbox"/>	yes
10 tpih_X0_OUT	428.292p	<input type="checkbox"/>	<input checked="" type="checkbox"/>	
11 tphi_X0_OUT	350.088p	<input type="checkbox"/>	<input checked="" type="checkbox"/>	
12 tpih_X1_OUT	560.136p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
13 tphi_X1_OUT	446.366p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
14 tpih_X2_OUT	573.45p	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
15 tphi_X2_OUT	455.49p	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
16 tpih_X3_OUT	584.01p	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
17 tphi_X3_OUT	461.39p	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
18 tpih_X4_OUT	475.5p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
19 tphi_X4_OUT	466.088p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
20 tpih_X5_OUT	415.436p	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
21 tphi_X5_OUT	398.198p	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
22 Delay_X5_OUT	406.817p	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
23 Delay_X4_OUT	470.794p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
24 Delay_X3_OUT	522.7p	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
25 Delay_X2_OUT	514.47p	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
26 Delay_X1_OUT	504.251p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
27 Delay_X0_OUT	389.18p	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
28 Energy	688.487f	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	

Plot after simulation: **Auto** Plotting mode: **Replace**

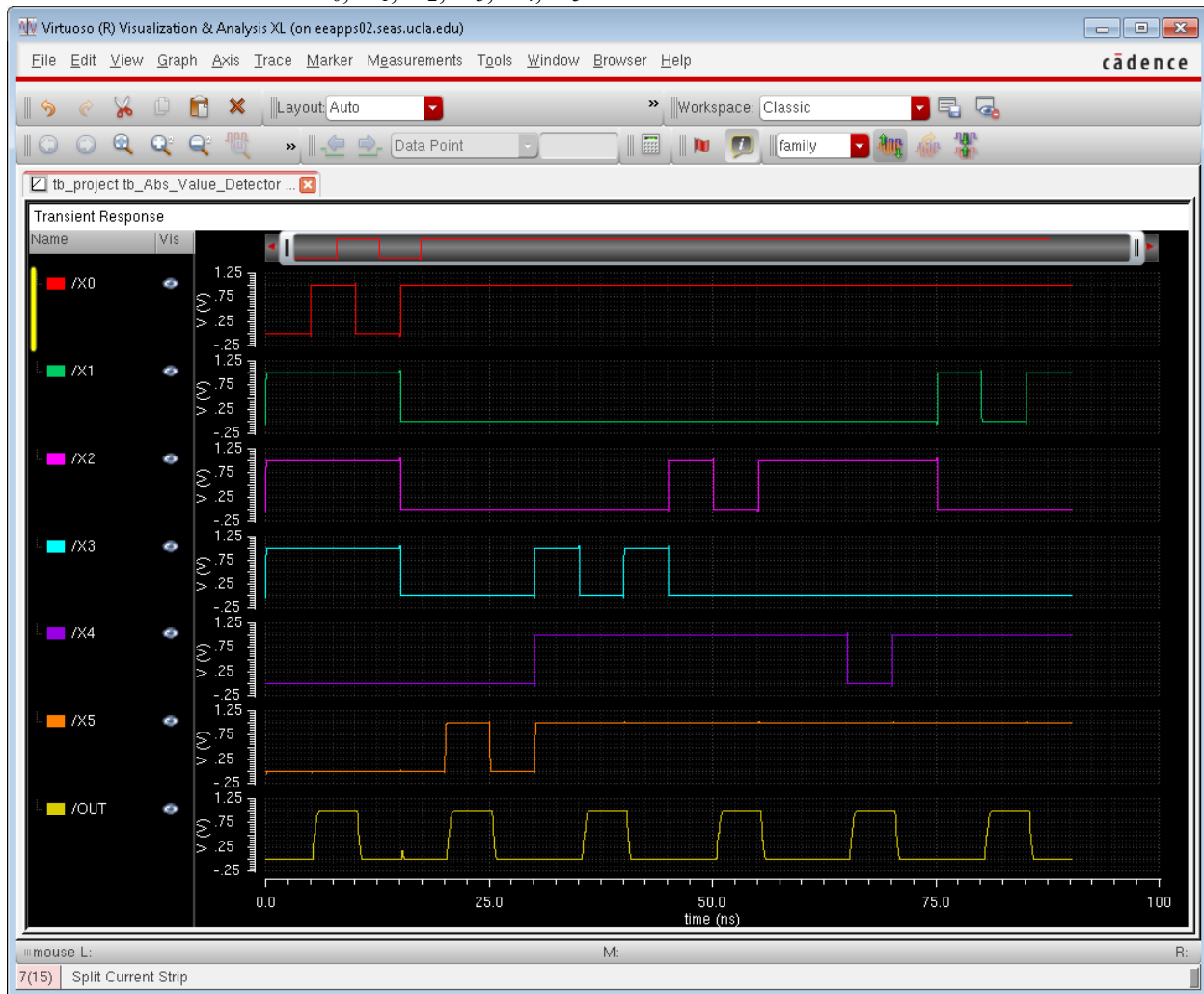
5(11) Stimuli ... Status: Ready T=27 C Simulator: spectre State: spectre\_state1

This shows the delay of this design from  $X_0$ ,  $X_1$ ,  $X_2$ ,  $X_3$ ,  $X_4$  and  $X_5$  to OUT.

Energy Consumption in this example is 688.487fJ.

Delay is the average of  $t_{pLH}$  and  $t_{pLH}$  in each case (Maximum delay and maximum  $t_{pLH}$  or  $t_{pLH}$ , should all be less than 1ns). In the example shown above Delay\_X3\_OUT is the critical path.

Transient waveforms of  $X_0$ ,  $X_1$ ,  $X_2$ ,  $X_3$ ,  $X_4$ ,  $X_5$  and OUT are shown below:



While only a few input combinations are plotted here, you have to make sure that your design functions for all combinations (even the ones that are not tested in this testbench).

**GOOD LUCK!**