CS152B Lab 0 – Binary Coded Decimal System

Required Equipment

VHDL modeling, simulation will require the use of Mentor Graphics Modelsim tool

Introduction to Binary Coded Decimal (BCD)

In the BCD numbering system, a decimal number is separated into four bits for each decimal digit within the number. Each decimal digit is represented by its weighted binary value performing a direct translation of the number. So a 4-bit group represents each displayed decimal digit from 0000 for a zero to 1001 for a nine.
For example, 369_{10} (three hundred and sixty nine) in decimal would be presented in Binary Coded Decimal as:

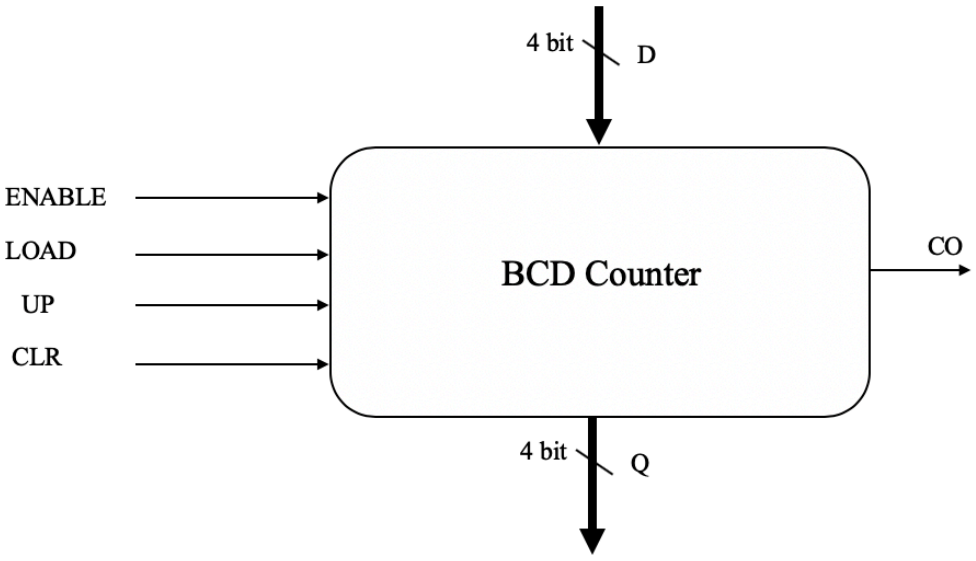
$$369_{10} = 0011\ 0110\ 1001\ (BCD)$$

The main advantage of binary coded decimal is that it allows easy conversion between decimal (base-10) and binary (base-2) form. However, the disadvantage is that BCD code is wasteful as the states between 1010 (decimal 10), and 1111 (decimal 15) are not used. Nevertheless, binary coded decimal has many important applications especially using digital displays.

Part 1: Sequential circuit
BCD Counter

Implement a 1-digit BCD (binary coded decimal) counter. It should be a synchronous (4-bit) up/down decade counter with output Q that works as follows: All state changes occur on the rising edge of the CLK input, except the asynchronous clear (CLR). When CLR = 0, the counter is reset regardless of the values of the other inputs.

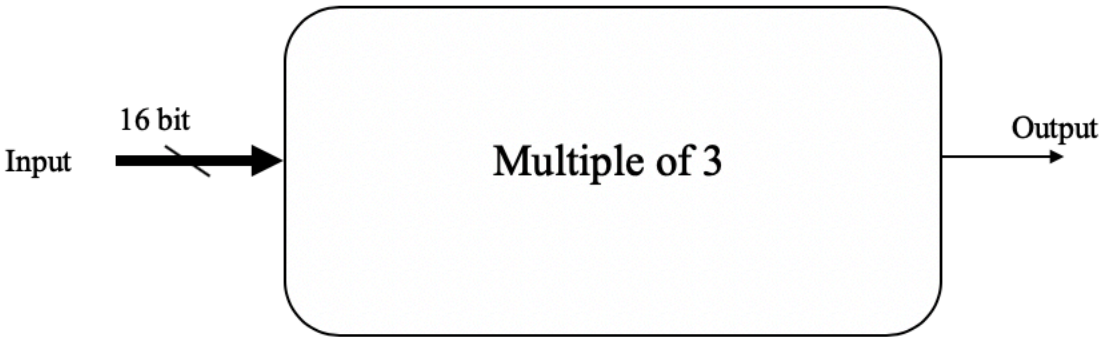
- If the LOAD = ENABLE = 1, the data input D is loaded into the counter.
- If LOAD = 0 and ENABLE = UP = 1, the counter is incremented.
- If LOAD = 0, ENABLE = 1, and UP = 0, the counter is decremented.
- If ENABLE = 1 and UP = 1, the carry output (CO) = 1 when the counter's value is 9.
- If ENABLE = 1 and UP = 0, the carry output (CO) = 1 when the counter's value is 0.



Part 2: Combinational circuit
4-digit BCD divisible by 3 and 11

Implement a circuit that has a four-digit BCD input and one-bit output.

- The output=1 only if the four-digit BCD input is divisible by 3.



Repeat the same experiment for division by 11.
In designing this circuit you are only allowed to use basic gates.
Hint:
N is divisible by:

- 3 if the sum of digits of N is a multiple of 3.
- 11 if the difference of the alternating sum of digits of N is a multiple of 11 (e.g. 7249 is divisible by 11 because 7 - 2 + 4 - 9 = 0, which is a multiple of 11).

Checking Syntax and Simulating
The steps taken to design and implement are as follows: Add Code, Check Syntax, Synthesize, and Simulate.

In order to simulate, you have to design a Verilog test bench to drive the design under test.

Then create a stub waveform where you can drive the input signals and check the output signals.
Please write comprehensive and well written test benches for your modules that covers all the possible inputs and outputs and demo it to TA.
Take a screenshot from waveforms and add it to your report.

Please submit a lab report (see syllabus for details) describing your experience with this lab, any problems you encountered, etc.