LAC Performance on ARM-Cortex M4

No Author Given

No Institute Given

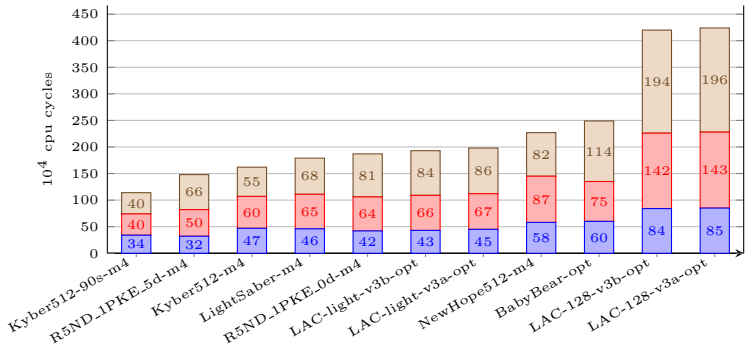

Fig. 1. Performance of 128-bits security level (ARM-Cortex M4)

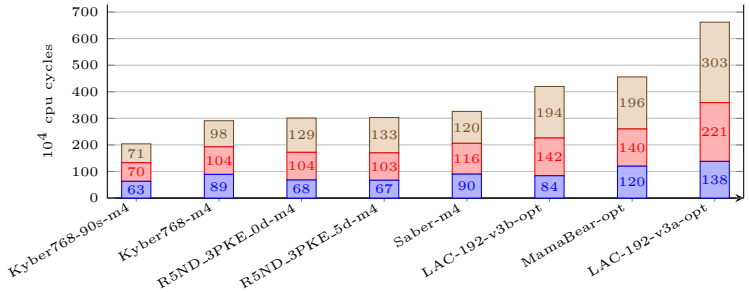

Fig. 2. Performance of 192-bits security level (ARM-Cortex M4)

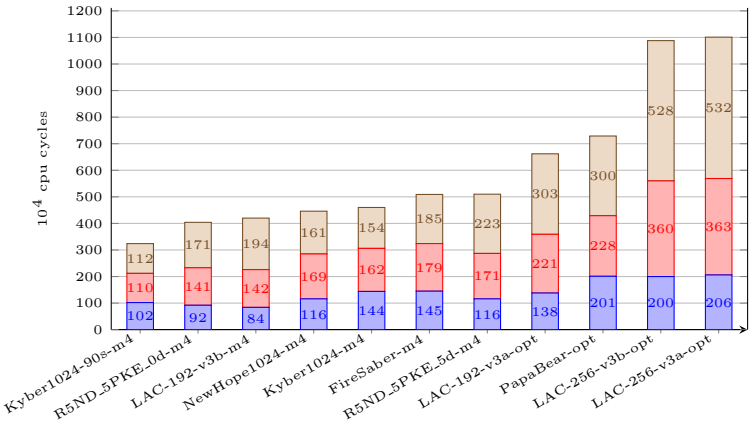

Fig. 3. Performance of 256-bits security level (ARM-Cortex M4)