Product Specification

( ) **Preliminary Specifications**

(V) **Final Specifications**

Module	13.3"(13.26") FHD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B133HTN01.4 (H/W:0A)
Note ( )	*LED Backlight with driving circuit design*

Customer	Date	Approved by	Date
Checked & Approved by	Date	Prepared by	Date

Note: This Specification is subject to change without notice.

NBBU Marketing Division
AU Optronics corporation

Product Specification

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2015/11/09	All	First Edition for Customer		
0.2 2015/12/04	5	Power		
	16	Backlight power		
	26,27	LCM Outline Dimension		
0.2 2016/02/16	28	Label		
	30	EDID		
0.3 2016/05/03	6	Color / Chromaticity Coodinates	Update Color / Chromaticity Coodinates	
1.0 2016/05/18		Final Spec.		
1.1 2016/05/24	13	VDD=272	VDD=257	
	18	MSAK24025P30 or Compatible	MSAK24025P30	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.

7) Do not open nor modify the Module Assembly.

8) Do not press the reflector sheet at the back of the module to any directions.

9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.

11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.

13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B133HTN01.4 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x1080(V) screen and 262K colors (RGB 6-bits) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B133HTN01.4 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	336.7			
Active Area	[mm]	293.472x165.078			
Pixels H x V		1920x3(RGB) x1080			
Pixel Pitch	[mm]	0.15285x0.15285			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (I_{LED}=25mA) (Note: ILED is LED current)	[cd/m^2]	250 typ. (5 points average) 212 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		500 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.0 max. (Include Logic and Blu power)			
Weight	[Grams]	230 max.			
Physical Size **Include bracket**	[mm]		Min.	Typ.	Max.
		Length	304.85	305.35	305.85
		Width	192.96	193.46	193.96
		Thickness	-	-	2.6
Electrical Interface		2 Lane eDP (eDP w/o PSR)			
Glass Thickness	[mm]	0.3			
Surface Treatment		Anti-Glare, Hardness 3H,			
Support Color		262K colors (RGB 6-bits)			

| Temperature Range			
Operating	[^{o}C]	0 to +50	
Storage (Non-Operating)	[^{o}C]	-20 to +60	
RoHS Compliance		RoHS Compliance	

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I$_{LED}$=25mA			5 points average	212	250	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10 (Left)	40	45	-	degree	4, 9
		θ_L		40	45	-		
		ϕ_H	Vertical (Upper) CR = 10 (Lower)	10	15	-		
		ϕ_L		30	35	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.6		2, 3, 4
Contrast Ratio		CR		400	500	-		4, 6
Cross talk		%				4		4, 7
Response Time		T$_{RT}$	Rising + Falling	-	8	16	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.605	0.635	0.665		4
		Ry		0.310	0.340	0.370		
	Green	Gx		0.295	0.325	0.355		
		Gy		0.580	0.610	0.640		
	Blue	Bx		0.122	0.152	0.182		
		By		0.017	0.047	0.077		
	White	Wx		0.275	0.305	0.335		
		Wy		0.29	0.320	0.35		
NTSC		%		62	72	-		

Note 1: 5 points position (Ref: Active area)
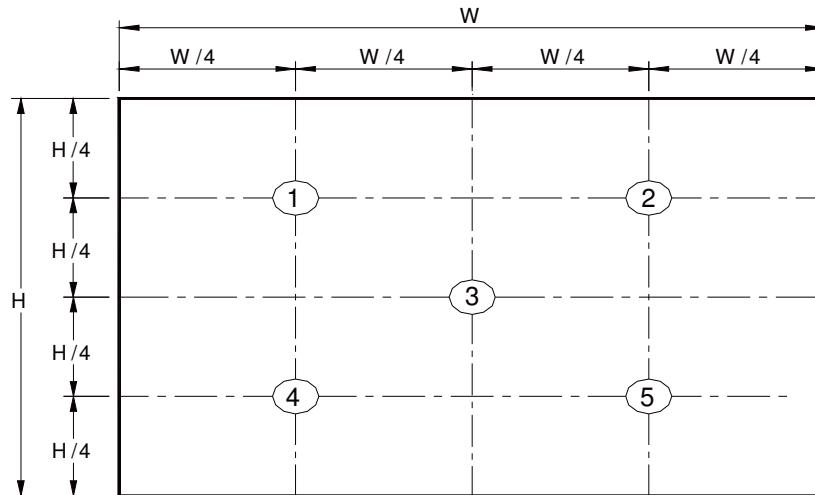
Note 2: 13 points position (Ref: Active area)
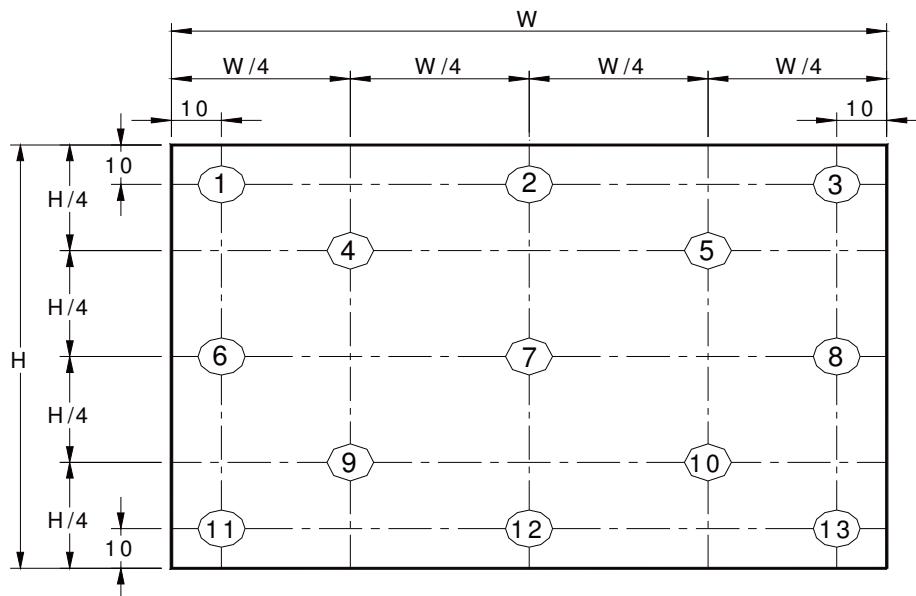
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.

Photo detector

Field=2°

50 cm

LCD Panel

TFT-LCD Module

Center of the screen
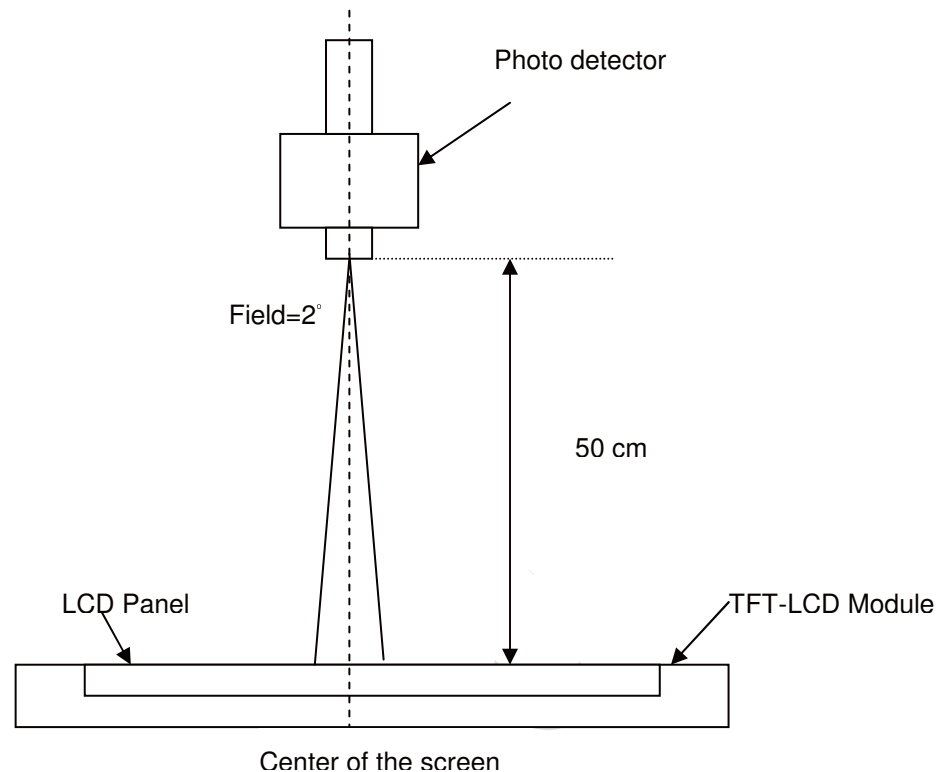
Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

Note 7： Definition of Cross Talk (CT)

CT = | $Y_B - Y_A$ | / Y_A × 100 (%)

Where

Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)
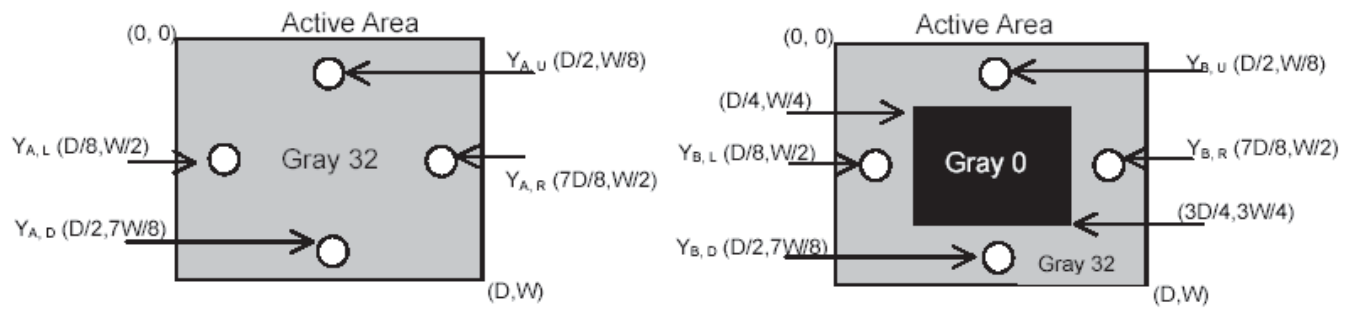
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.

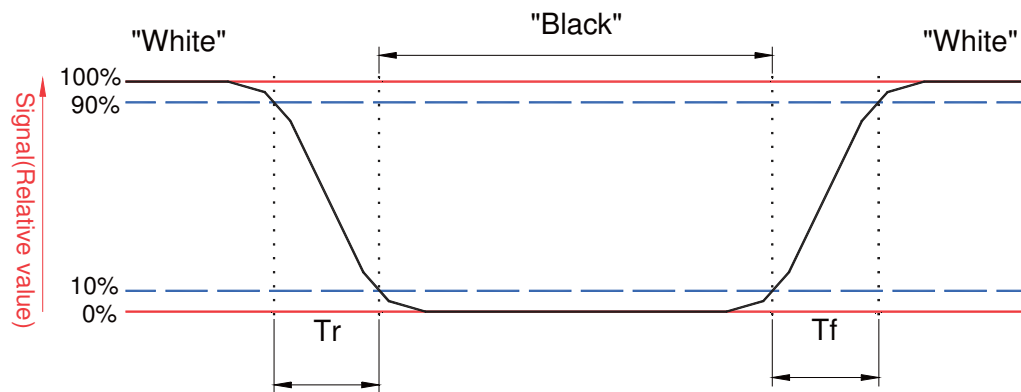**Note 9**. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.
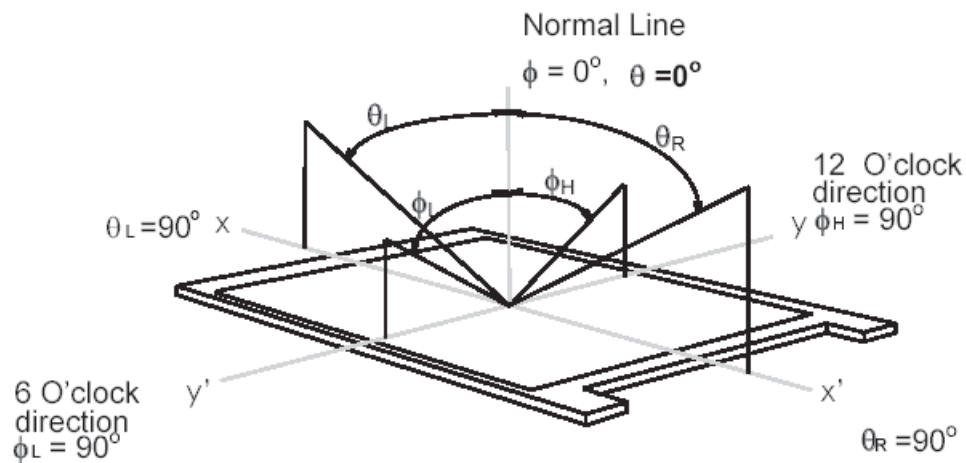
3. Functional Block Diagram

The following diagram shows the functional block of the 13.3 inches wide Color TFT/LCD 30 Pin
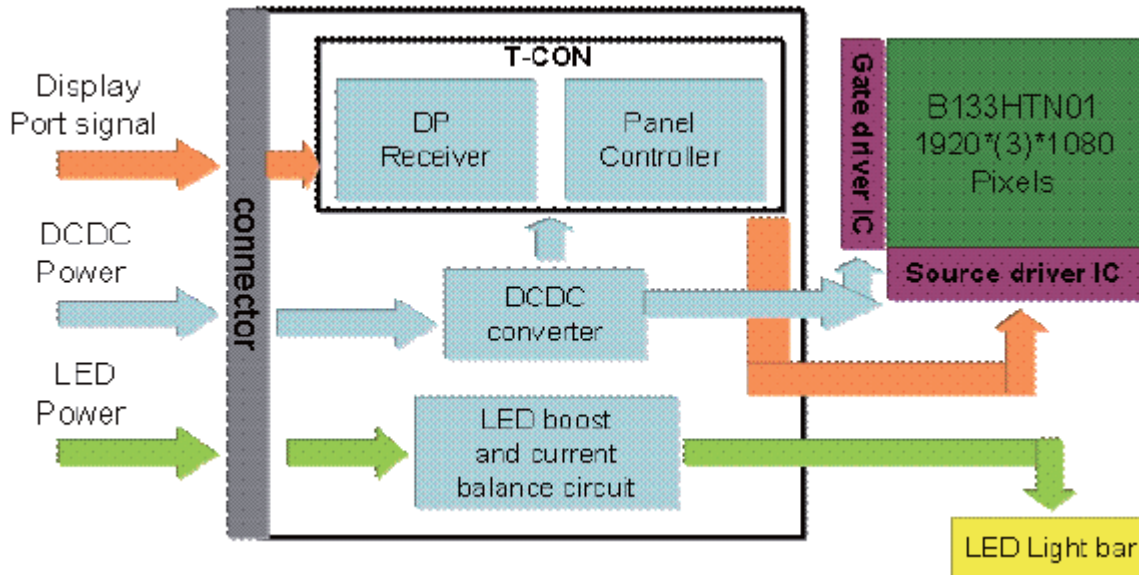
4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[^{o}C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[^{o}C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).
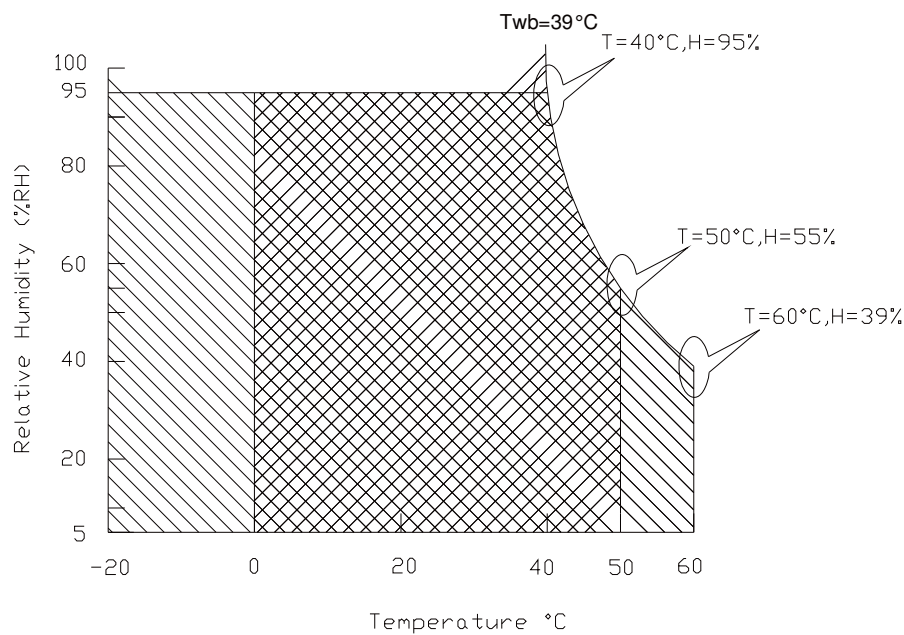
Operating Range   Storage Range

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.85	[Watt]	Note 1
IDD	IDD Current	-	-	257	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3}$ x I_{black})

    Typical Measurement Condition : Mosaic Pattern

Note 2：Measure Condition
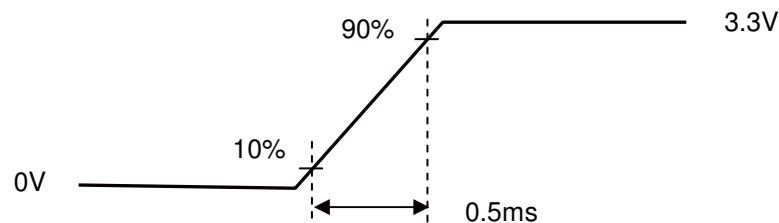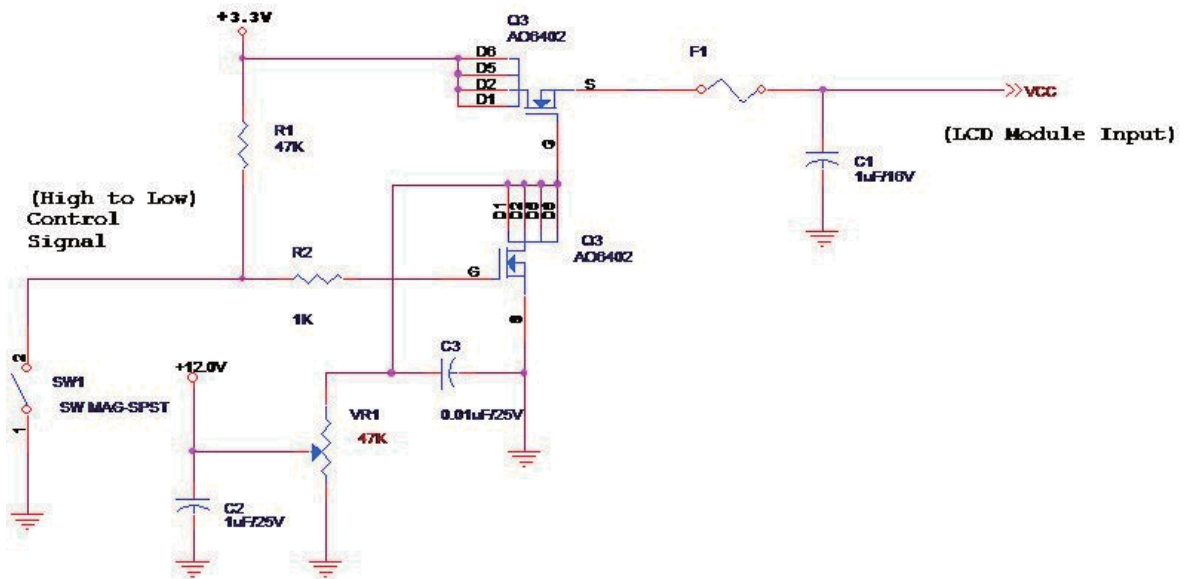
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Display Port main link signal:

Differential pair VD+ , VD-
Which is one Display port
Main link

VCM of Display port
Main link

VD+

VCM

VDiff

VD-

$Vdiff_{P-P} = [(VD+) - (VD-)] \times 2$

$V_{D+} - V_{D-}$
0V
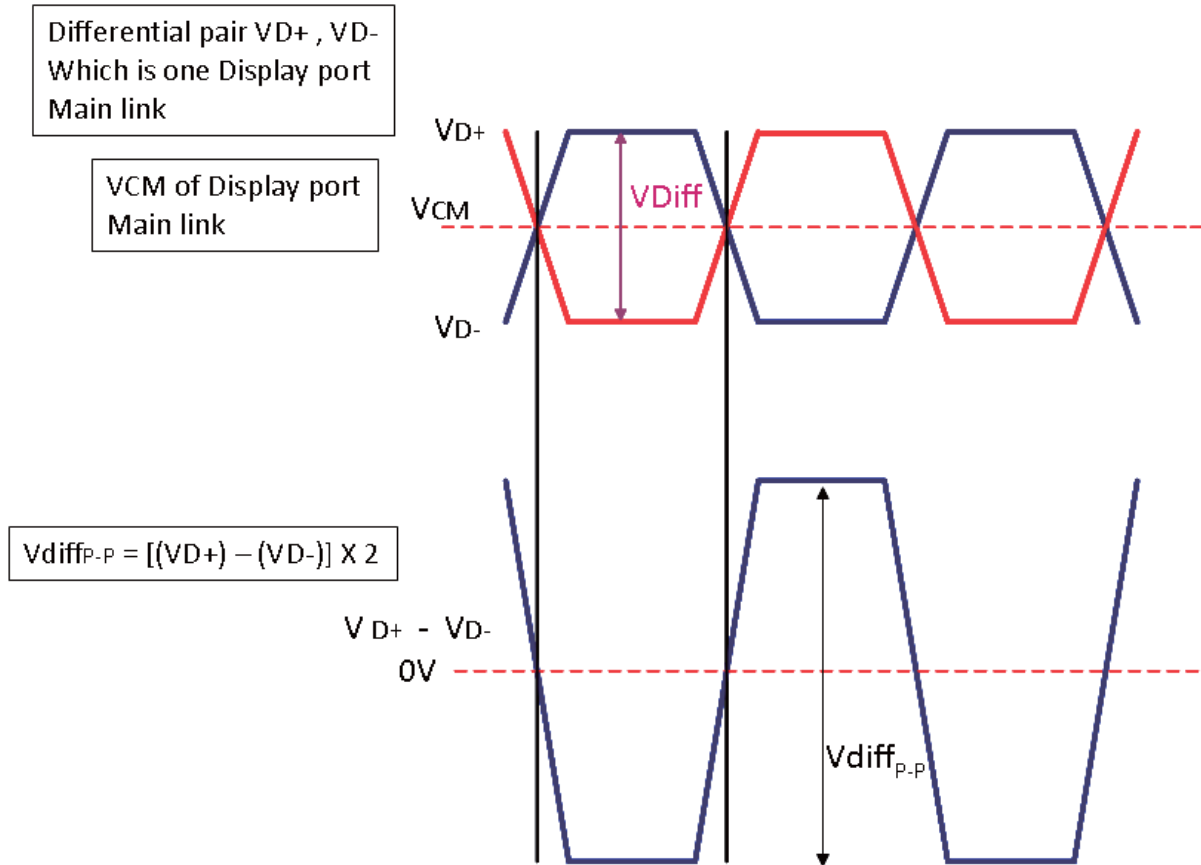
$Vdiff_{P-P}$

Display port main link		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff$_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Follow as VESA display port standard V1.2

Display Port AUX_CH signal:

Differential AUX+ , AUX-
Which is Display pot AUX_CH
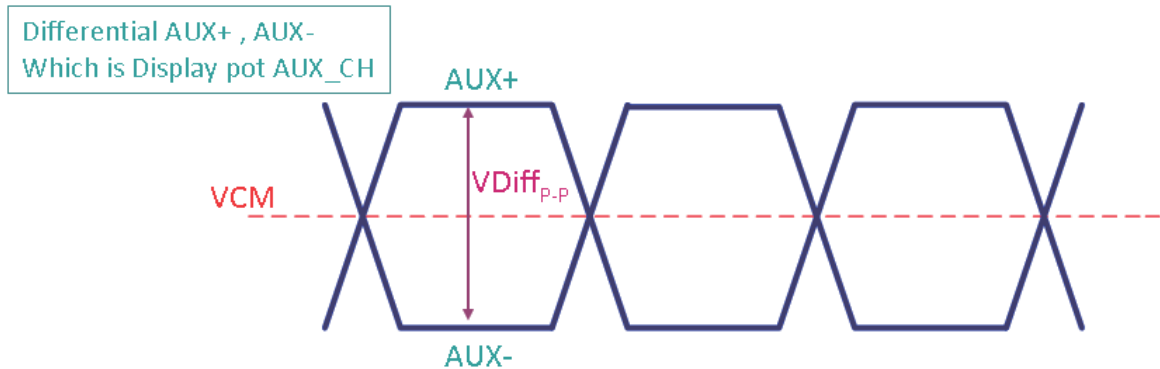
Display port AUX_CH		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff$_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Follow as VESA display port standard V1.2.

Display Port V$_{HPD}$ signal:

Display port V$_{HPD}$		Min	Typ	Max	unit
V$_{HPD}$	HPD Voltage	2.25		3.6	V

Follow as VESA display port standard V1.2.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	3.15	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=19 mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5	12.0	21.0	[Volt]	
LED Enable Input High Level	VLED_EN	2.2	-	5.5	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.2	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.
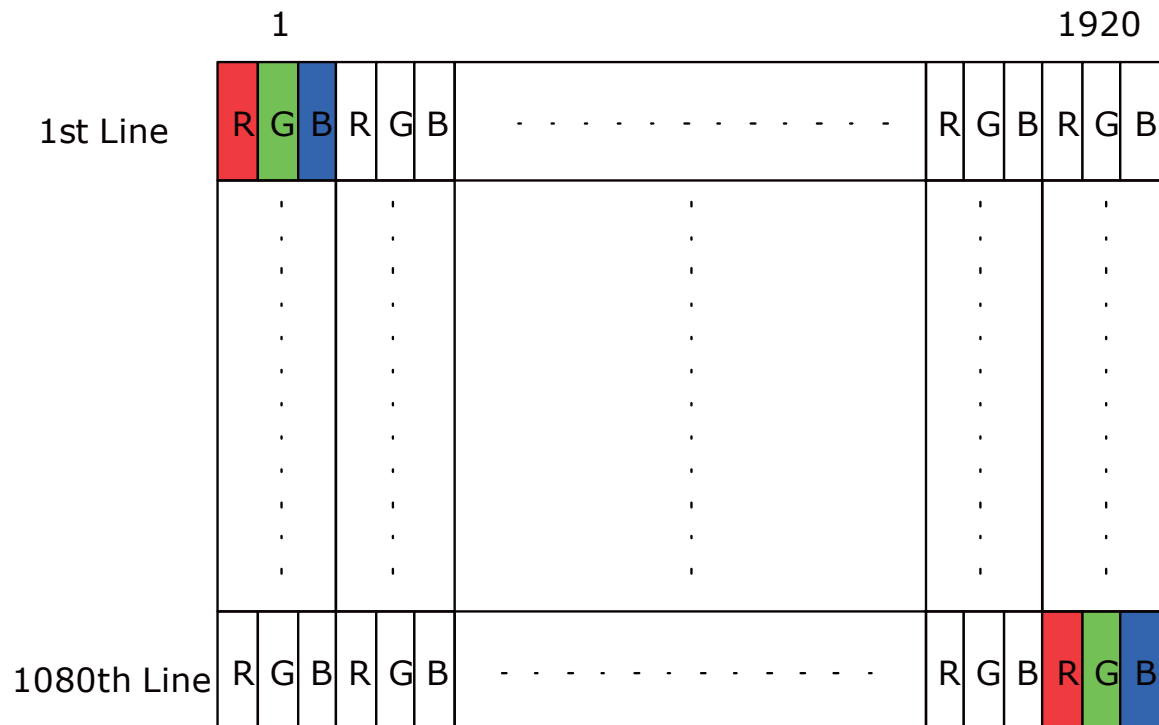
6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	STM
Type / Part Number	MSAK24025P30
Mating Housing/Part Number	IPEX 20353-030T-11 or Compatible

6.2.2 Pin Assignment (2 Lane)

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

| PIN NO	Symbol	Function
1	NC	No Connect
2	H_GND	High Speed Ground
3	Lane1_N	Comp Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	NC	Reverse for AUO TEST only
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signale pin
18	BL_GND	Backlight ground
19	BL_GND	Backlight ground
20	BL_GND	Backlight ground
21	BL_GND	Backlight ground
22	BL_Enable	Backlight On / Off
23	BL_PWM_DIM	System PWM signal Input
24	NC	Reversed
25	NC	Reversed
26	BL_PWR	Backlight power
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	NC	No connect

Pin 30   **Pin 1**

Connector
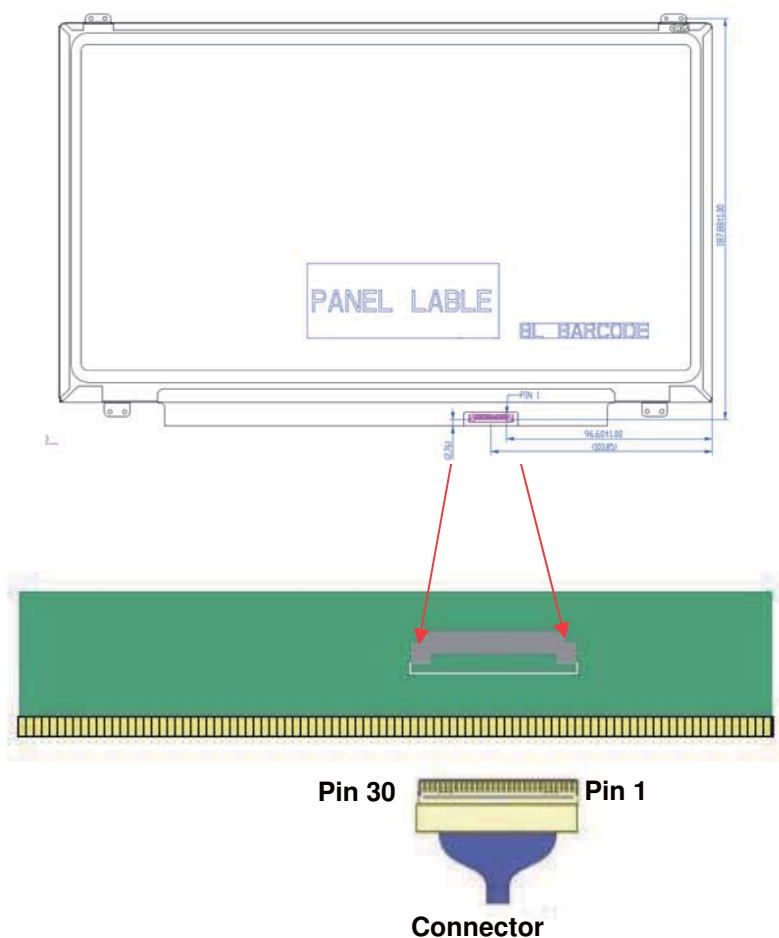
Note1: Start from right side.
Note2: Input signals shall be low or High-impedance state when VDD is off.
     Internal circuit of **eDP inputs** are as following.
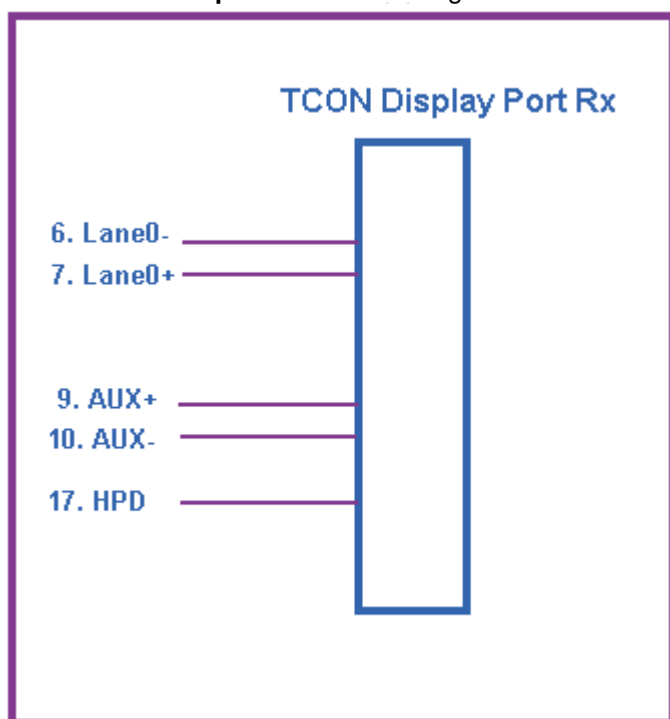
6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	**Hz**
Clock frequency		$1/T_{Clock}$	66.6	72	80	**MHz**
Vertical Section	**Period**	T_V	1100	1130	1080+A	T_{Line}
	Active	T_{VD}		1080		
	Blanking	T_{VB}	20	50	A	
Horizontal Section	**Period**	T_H	1010	1050	960+B	T_{Clock}
	Active	T_{HD}		960		
	Blanking	T_{HB}	50	90	B	

Note 1 : DE mode only
Note 2 : The maximum clock frequency = (1920+B)*(1080+A)*60<180MHz

6.4 Power ON/OFF Sequence

Display Port panel power sequence:
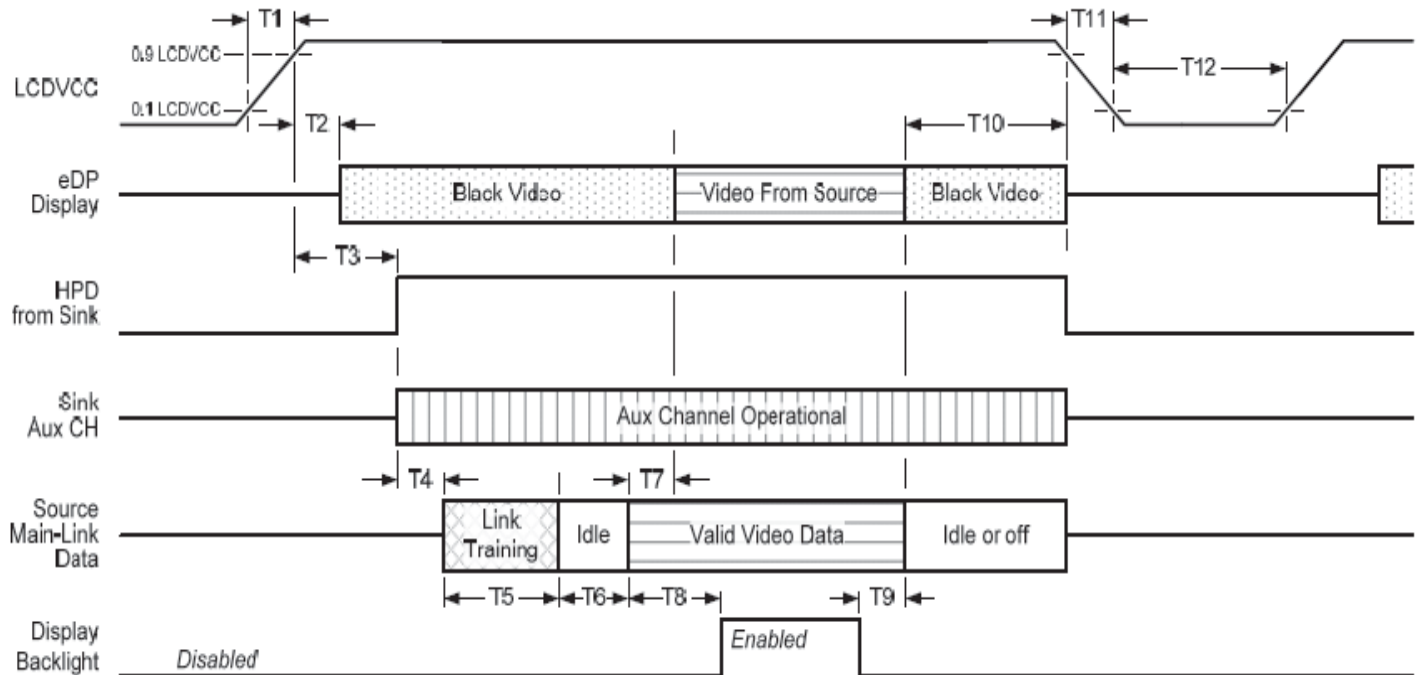
Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:

Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

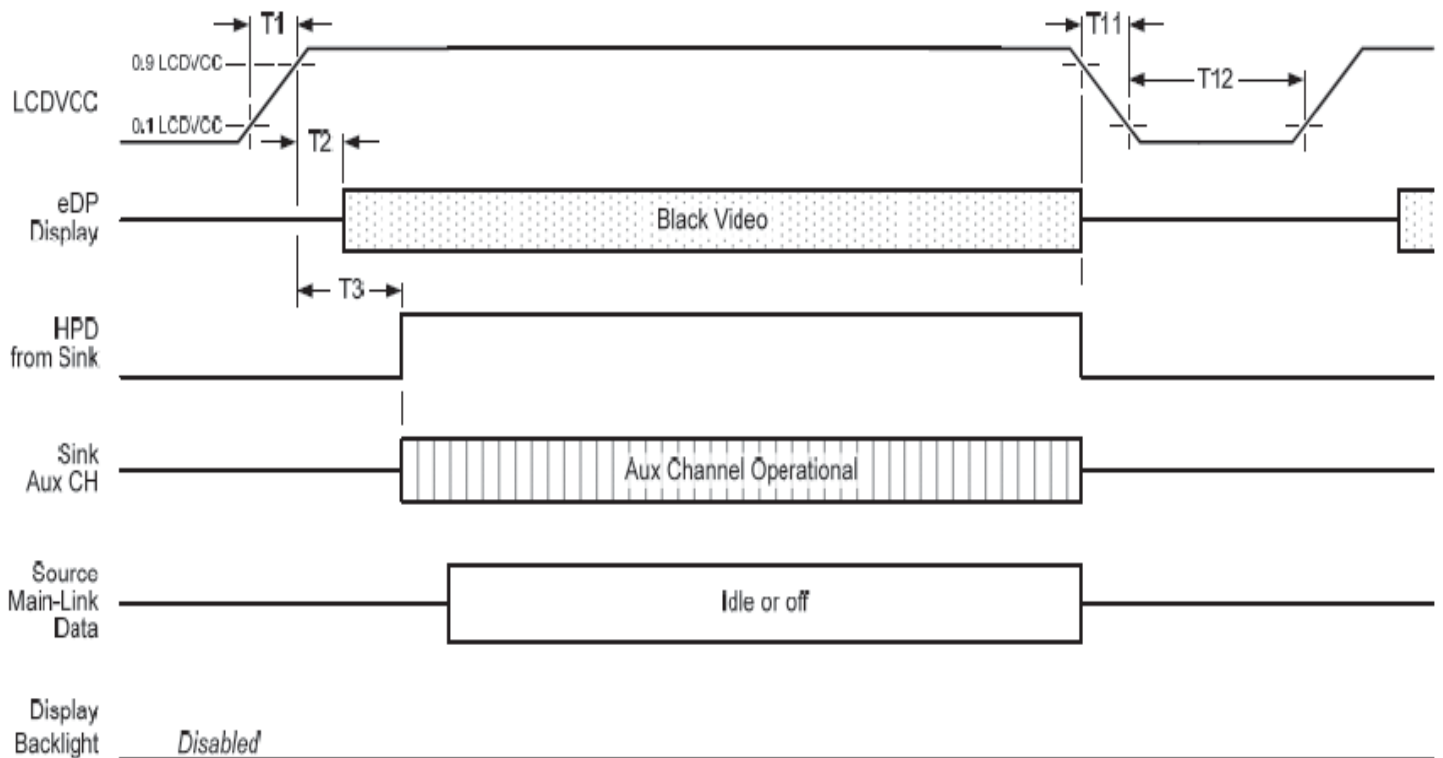| Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
  -upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
  -when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:
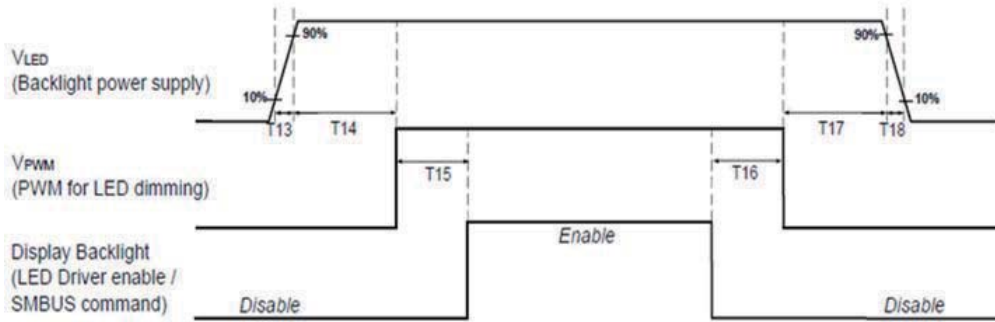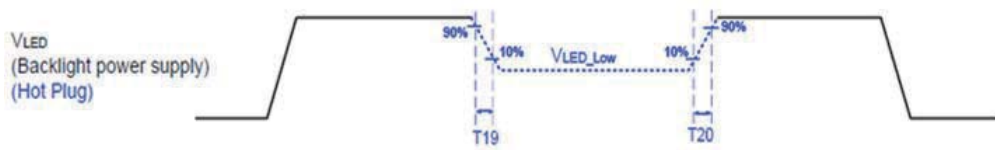
	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT$_{PWM}$*

*T$_{PWM}$= 1/PWM Frequency

Note 1 : If T14,T15,T16,T17<10ms，The display garbage may occur. We suggest T14,T15,T16,T17>10ms to avoid the display garbage.

Note 2 : If T13 or T18<0.5ms，the inrush current may cause the damage of fuse. If T13 or T18<0.5ms，the inrush current I²t is under typical melt of fuse Spec.，there is no mentioned problem.

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable.

No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

Product Specification

AU OPTRONICS CORPORATION

8. Mechanical Characteristics

8.1 LCM Outline Dimension

Product Specification

AU OPTRONICS CORPORATION

BARCODE

DON'T TOUNCH

196.77±1.00 (OUTLINE TO CONNECTOR PIN 1)

422±1.00

SHIPPING

2.60 MAX (LCM SIDE)

1.10 ±0.50 (TOP POLARIZER TO BRACKET BOTTOM SURFACE)

2.60 MAX (PCB SIDE)

XX XX XXXX
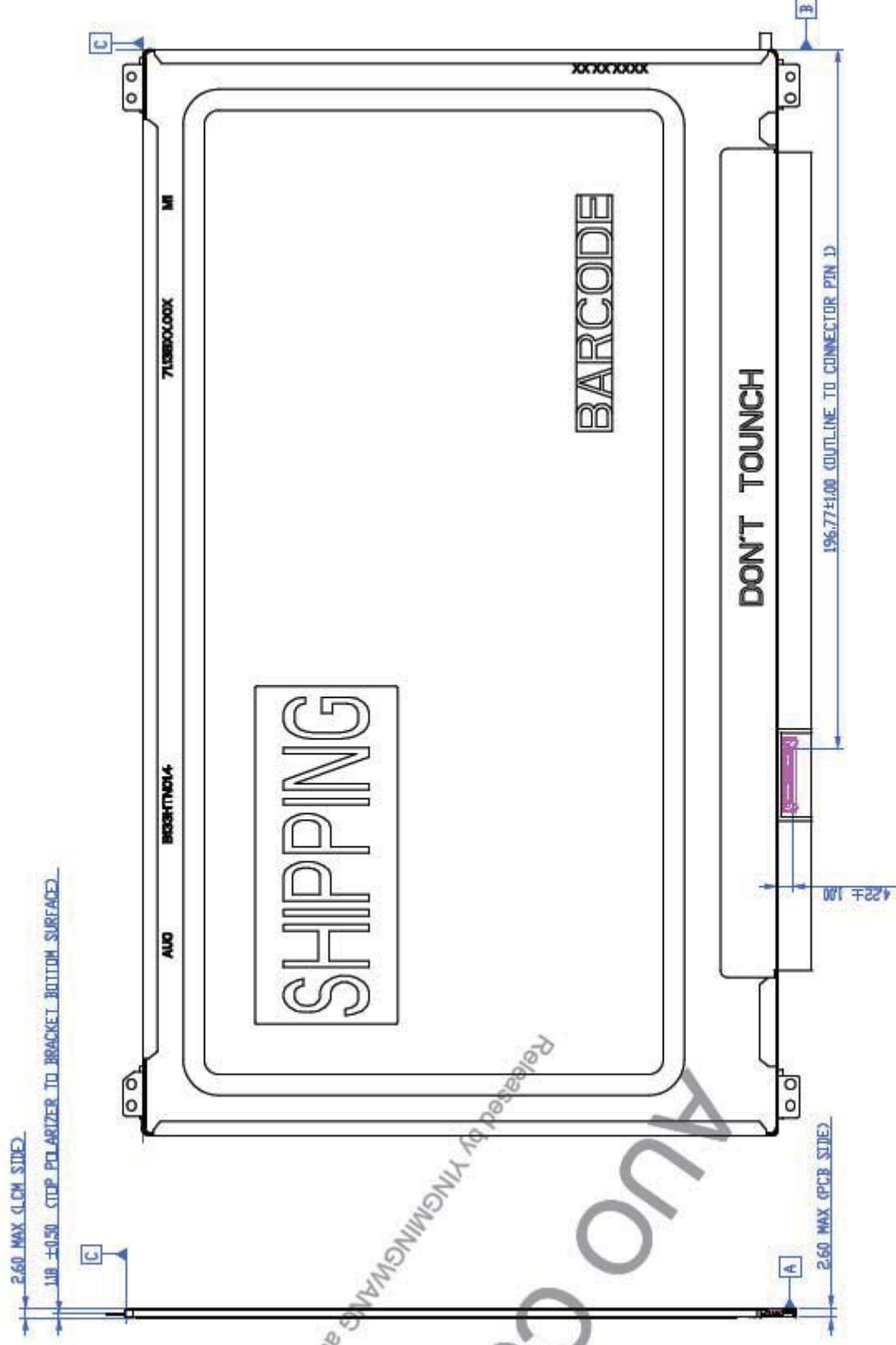
Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

9. Shipping and Package

9.1 Shipping Label Format

9.2 Carton Package

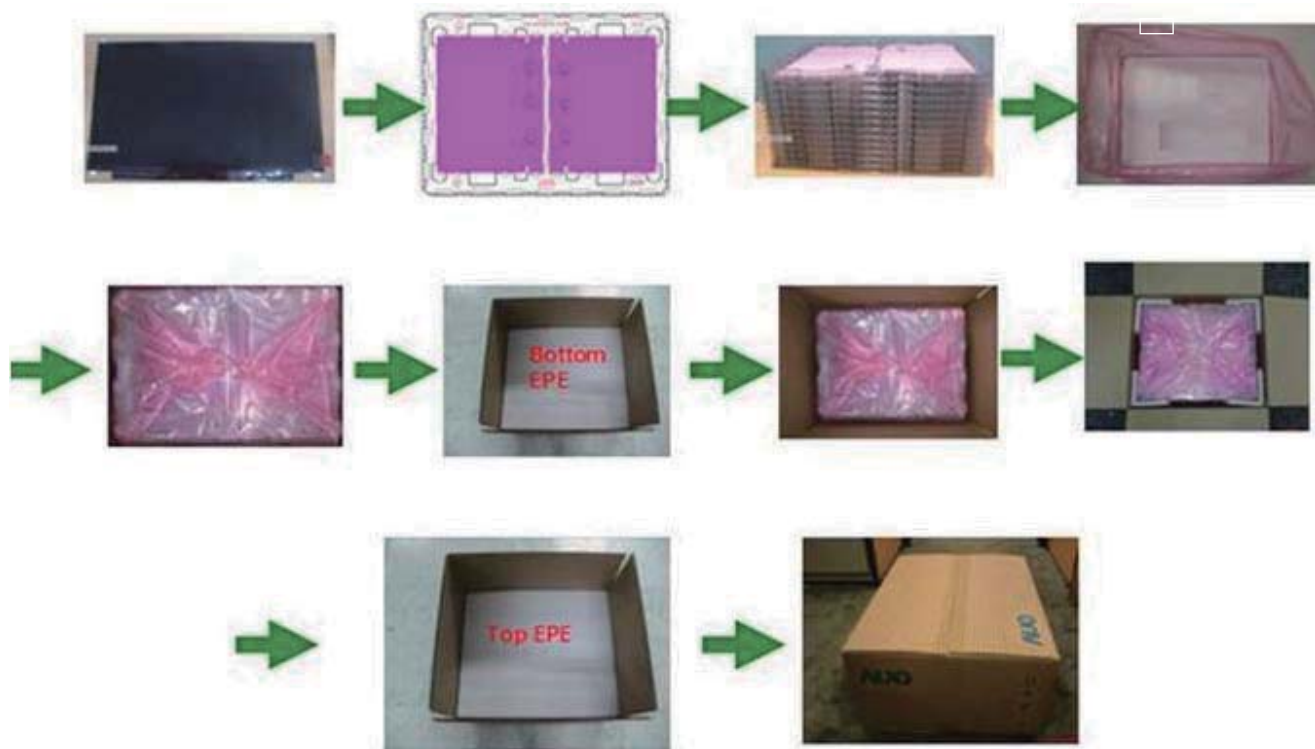## 9.3 Shipping Package of Palletizing Sequence
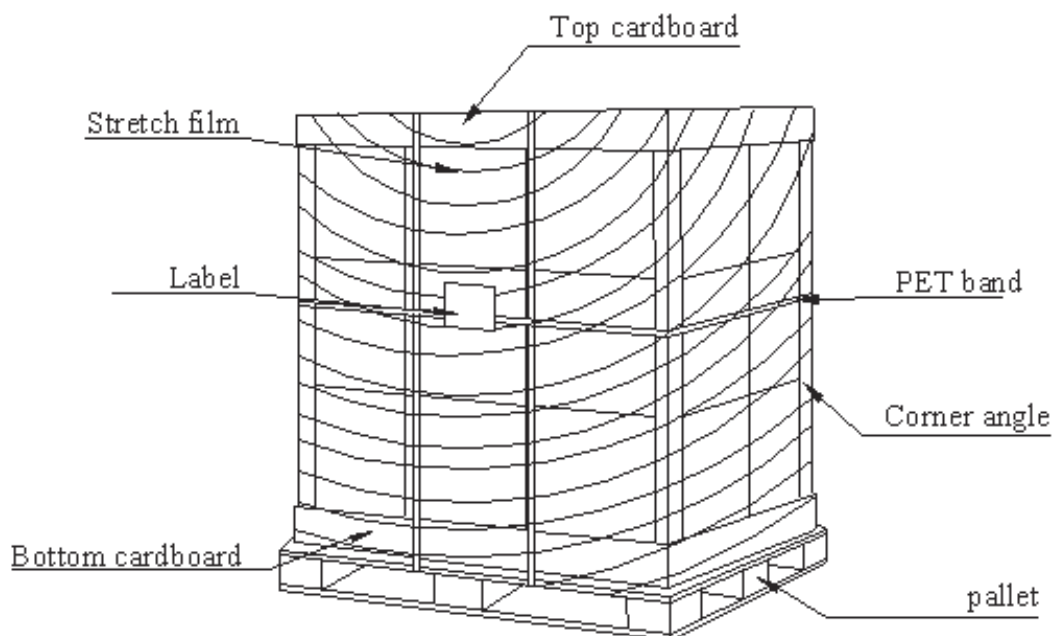
10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	2D	00101101	45	
0B	hex, LSB first	14	00010100	20	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	02	00000010	2	
11	Year of manufacture	1A	00011010	26	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def.** (digital I/P, non-TMDS, CRGB)	95	10010101	149	
15	**Max H image size** (rounded to cm)	1D	00011101	29	
16	**Max V image size** (rounded to cm)	11	00010001	17	
17	**Display Gamma** (=(gamma*100)-100)	78	01111000	120	
18	**Feature support** (no DPMS, Active OFF, RGB, tmg Blk#1)	02	00000010	2	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	BB	10111011	187	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	F5	11110101	245	
1B	Red x **(Upper 8 bits)**	94	10010100	148	
1C	Red y/ highER 8 bits	55	01010101	85	
1D	Green x	54	01010100	84	
1E	Green y	90	10010000	144	
1F	Blue x	27	00100111	39	
20	Blue y	23	00100011	35	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	

24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	3C	00111100	60	
37	Pixel Clock/10000 USB	37	00110111	55	
38	Horz active **Lower 8bits**	80	10000000	128	
39	Horz blanking **Lower 8bits**	C0	11000000	192	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	70	01110000	112	
3B	Vertical Active **Lower 8bits**	38	00111000	56	
3C	Vertical Blanking **Lower 8bits**	20	00100000	32	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40	01000000	64	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	64	01100100	100	
40	VertSync.Offset : VertSync.Width	8E	10001110	142	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	25	00100101	37	
43	Vertical Image Size **Lower 8bits**	A5	10100101	165	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	

4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B

72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	33	00110011	51	3
74	Manufacture P/N	33	00110011	51	3
75	Manufacture P/N	48	01001000	72	H
76	Manufacture P/N	54	01010100	84	T
77	Manufacture P/N	4E	01001110	78	N
78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	31	00110001	49	1
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	34	00110100	52	4
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	7E	01111110	126	