

# **AMOLED MODULE SPECIFICATION**

	<b>Customer:</b>						
	Module No.	-					
	Date:	2024-09-	27				
	Version:	2.0		-			
	<ul> <li>□ Pre-Specification for parameter checking</li> <li>■ Final-Specification for sample approval</li> </ul>						
Approved	<b>-</b>	arice.	Comment				

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## **Record of Revision**

Rev.	Date	Description	Editor
1.0	2024-09-06	First release	Zaiping.Yang
2.0	2024-09-27	Update brightness and color coordinate parameters.	Zaiping.Yang



## 1 General Specifications

No.	Item	Specification	Remark
1	OLED Size	5.44 inch (Diagonal)	
2	Driver Element	AMOLED active matrix	
3	Resolution	1080 (RGB) ×1920	
4	Display Mode	AMOLED	
5	Pixel Pitch(mm)	0.0314(H) × 0.0628 (V)	
6	Display Colors	16.7M	
7	Surface Treatment		
8	Color Arrangement	Rendering	
9	Interface	MIPI	
10	Viewing Direction	All	
11	Gray Scale Inversion Direction	1	Note 1
12	Outline Dimension (mm)	81.0 (W) ×138.2 (H) × 1.67 (T)	
13	Active Area (mm)	67.824 (W) × 120.58 (H)	
14	Touch Screen	On-cell with Cover Lens	
15	Display Driver IC	SH8801A	
16	Touch Driver IC	GT9886	

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180°shift.

Note 2: RoHS compliant.



## 2 Pin Assignment

## 2.1 OLED Pin assignment

Match connector: 0.3mm contact pitch FPC,39pin,T=0.2mm.

Type of connector on FPC: FH26-39S-0.3SHW( Hirose)or equivalent.

PIN	Symbol	I/O	Description	Remark
1	GND1	Р	Ground	
2	GND2	Р	Ground	
3	GND3	Р	Ground	
4	VBAT1	Р	power supply (4.2V)	
5	VBAT2	Р	power supply (4.2V)	
6	VBAT3	Р	power supply (4.2V)	
7	VBAT4	Р	power supply (4.2V)	
8	VBAT5	Р	power supply (4.2V)	
9	GND4	Р	Ground	
10	VPP		Power supply for OTP. Float it for normal	
			operation.	
11	NC1		NC	
12	GND5	Р	Ground	
13	D3P	1	MIPI DSI differential data pair (Data lane 3)	
14	D3N	I	MIPI DSI differential data pair (Data lane 3)	
15	GND6	Р	Ground	
16	D0P	1/0	MIPI DSI differential data pair (Data lane 0)	
17	D0N	1/0	MIPI DSI differential data pair (Data lane 0)	
18	GND7	Р	Ground	
19	CLKP	I	MIPI DSI differential clock pair	
20	CLKN	1	MIPI DSI differential clock pair	
21	GND8	Р	Ground	
22	D1P	I	MIPI DSI differential data pair (Data lane 1)	
23	D1N	I	MIPI DSI differential data pair (Data lane 1)	
24	GND9	Р	Ground	
25	D2P	I	MIPI DSI differential data pair (Data lane 2)	
26	D2N	I	MIPI DSI differential data pair (Data lane 2)	
27	GND10	Р	Ground	
28	RESX	I	Reset Signal ,Active Low.	
29	VDDIO	Р	Digital circuit I/O power supply	



30	VCI	Р	Power supply for Analog circuit.
31	TE	0	Tearing effect.
32	GND11	Р	Ground
33	TSP_AVDD_3.3V	Р	Touch IC analog power supply (3.3V)
34	TSP_DVDD_1.8V	Р	Touch IC Digital circuit I/O power supply
35	TSP_SDA	1/0	Touch IIC Data signal(1.8V)
36	TSP_SCL	I	Touch IIC Clock signal(1.8V)
37	TSP_RESET	I	Touch Reset Signal(1.8V)
38	TSP_ATTN	I	Touch Interrupt(1.8V)
39	ID		ID Signal. (not connect)

I---Input, O---Output, P--- Power/Ground

# 3 Absolute Maximum Ratings

Ta = 25 ℃

Item	Symbol	Min.	Max.	Unit	Remark
	VBAT	2.5	5.0	٧	
	VCI	-0.30	+4.0	V	
	VDDIO	-0.30	+2.6	V	
Power Voltage	TSP_AVDD_3.3 V	-0.30	+4.2	V	
	TSP_DVDD_1.8 V	-0.30	+3.6	V	
Operating Temperature	Тор	-20.0	70.0	$^{\circ}\!\mathbb{C}$	
Storage Temperature	T <sub>st</sub>	-30.0	80.0	$^{\circ}\!\mathbb{C}$	
Operating and Storage Humidity	H <sub>stg</sub>	10%	90%	%(RH)	



## 4. Electrical Characteristics

## **4.1 Recommended Operating Condition**

VCI=3.3V, GND=0V, Ta =  $25^{\circ}$ C

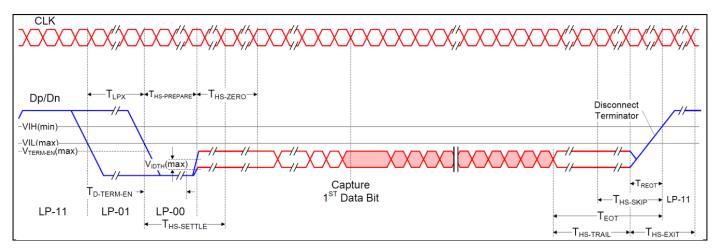
l'	tem	Symbol	Min.	Тур.	Max.	Unit	Remark
Power V	oltage/	VBAT	2.9	4.2	4.5	V	
Digital s Voltage	upply	VDDIO	1.65	1.8	1.98	>	
Analog s Voltage	supply	VCI	2.7	2.8	3.3	٧	
TD Dowe		TSP_AVDD_3.3	2.7	3.0	3.4	<b>V</b>	
TP Powe	er .	TSP_DVDD_1.8V	1.65	1.8	1.95	<b>V</b>	
Input	Low Level	$V_{IL}$	0	-	0.3 x VDDIO	٧	
Signal Voltage	High Level	V <sub>IH</sub>	0.7 x VDDIO	-	VDDIO	V	
Current Voltage	of Power	VBAT	ı	205	380	mA	350 nits @Gray 255
Current supply v	of digital oltage	Ivddio	ı	ı	10	mA	
Current supply v	of analog oltage	I <sub>VCI</sub>	-	50	60	mA	VCI=3.3V, @Gray 255

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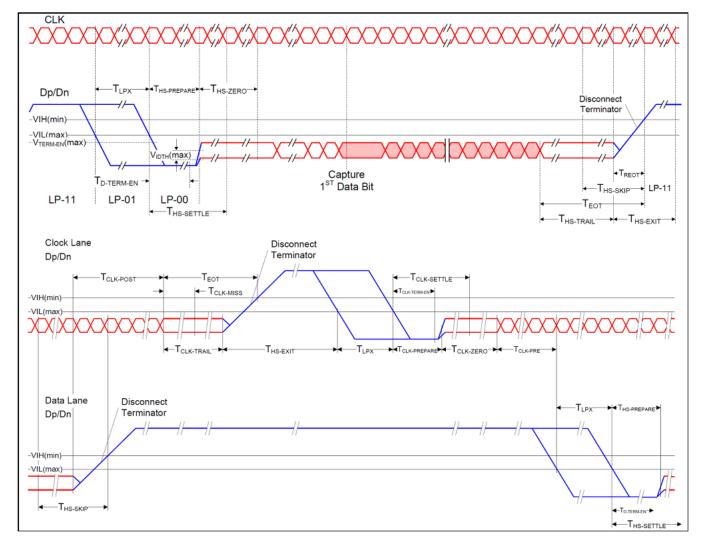


## 5 Timing Chart

## 5.1 DSI Interface Timing Characteristics



**High-Speed Data Transmission in Bursts** 



**High Speed Clock and Data timing** 



Symbol	Description	Min.	Тур.	Max.	Unit	Note
Tolk-miss	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-Rx.	-	-	60		(1) (6)
Tolk-post	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60 ns + 52 × UI	-	-	ns	
Tolk-pre	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	_	UI	<u>(5)</u>		
T <sub>CLK-PREPARE</sub>	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95		
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95	-	300		9
Tolk-term-en	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.	Time for Dn to reach VTERM-EN	-	38	ns	<u>(6)</u>
T <sub>CLK</sub> -TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-		3
Tolk-prepare + Tolk-zero	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-		<u>(5)</u>
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.	Time for Dn to reach VTERM-EN	-	35 ns + 4 × UI	_	<u>(6)</u>
Теот	Transmitted time interval from the start of THS-TRAIL OF TCLK-TRAIL, to the start of the LP-11 state following a HS burst.	-	-	105 ns + n × 12 × UI	_	(3) (5)
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100	-	-		
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4 × UI	-	85 ns + 6 × UI	ns	<u>(5)</u>
THS-PREPARE + THS-ZERO	The HS-Prepare + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10 × UI	_	-		
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions,	85 ns + 6 × UI	_	145 ns + 10 × UI		<u>(6)</u>



Symbol	Description	Min.	Тур.	Max.	Unit	Note
	starting from the beginning of THS-PREPARE.					
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	ore any transitions on the Data ving a HS burst. The end point of is defined as the beginning of 55 ns + 4 × UI				
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max (n × 8 × UI, 60 ns + n × 4 × UI)	_	-		(2) (3) (5)
T <sub>LPX</sub>	Transmitted length of any Low-Power state period	-	56.6	_	ns	( <u>4</u> ) ( <u>5</u> )
Ratio TLPX	Ratio of T <sub>LPX</sub> (MASTER)/ T <sub>LPX</sub> (SLAVE) between Master and Slave side	2/3	_	3/2	_	
TTA-GET	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	5 × T <sub>LPX</sub>				
TTA-GO	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	4 × T <sub>LPX</sub>			ns	<u>(5)</u>
TTA-SURE	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T <sub>LPX</sub> – 2 × T <sub>LPX</sub>				
TWAKEUP	Time that a transmitter drivers a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms	<u>(5)</u>

#### NOTE:

- 1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
- 2. If a > b then Max. (a, b) = a, otherwise Max. (a, b) = b
- 3. Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode
- 4. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
- 5. Transmitter-specific parameter
- 6. Receiver-specific parameter
- 7. The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.



### 5.2 Recommended Timing Setting of TCON

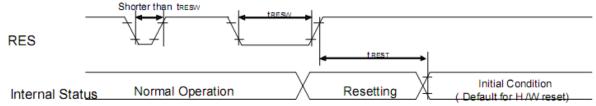
TCON (Embedded in Source IC) Input Timing (DCLK, HS, VS, DE)

DVDD=3.3V, GND=0V, Ta=25  $^{\circ}$ C

Parameter	Symbol	Min.	Тур.	Max.	Unit	Remark
D CL IV	Fclk	-	138	-	MHz	
DCLK	tclk	-	7.24	-	ns	
	thd	-	1080	-	tclk	
HCD	thpw	-	2	-	tclk	
HSD	thb	-	36	-	tclk	
	thfp	-	26	-	tclk	
	tvd	-	1920	-	th	
VSD	tvpw	-	4	-	th	
VSD	tvb	-	16	-	th	
	tvfp	-	8	-	th	

Note: For reference only, it needs to be adjusted according to the actual display effect.

## 5.3 Reset Input timing



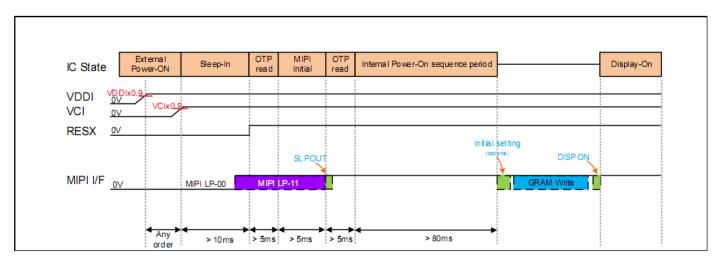
Reset input timing:

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t <sub>RESW</sub>	*1) Reset low pulse width	RESX	10	-	-	-	μS
t <sub>REST</sub>	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

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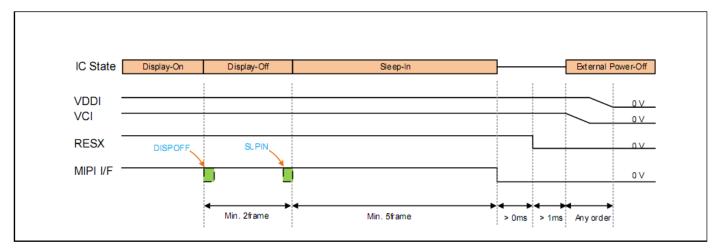


### 5.4 Power On Timing



**Power-On Sequence** 

### 5.5 Power Off Timing



**Power-Off Sequence** 



# **6 Optical Characteristics**

Ta=25 ℃

Item		Symbol	Condition	Min.	Тур.	Max.	Unit	Remark
View Angles		θТ	- CR ≥ 1000	80	-	-	Degree	
		θВ		80	-	-		Note 2
		θL		80	-	-		Note 2
		θR		80	-	-		
Contrast Ratio		CR	θ=0°	60000	-	-		Note1 Note3
Response Time		T <sub>ON</sub>	25℃	-	-	2	ms	Note1 Note4
Chromaticity	White	х	Backlight is on	0.275	0.295	0.315		
		У		0.285	0.305	0.325		
	Red	х		0.66	0.69	0.72		
		У		0.28	0.31	0.34		Note1
	Green	х		0.195	0.235	0.275		Note5
		У		0.68	0.72	0.760		
	Blue	х		0.113	0.143	0.173		
		У		0.014	0.044	0.074		
Uniformity		U		75	-	-	%	Note1 Note6
NTSC				90	109	-	%	Note 5
Luminance		L		-	280	-	cd/m <sup>2</sup>	Note1 Note7

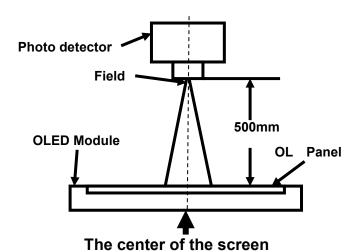
### **Test Conditions:**

- 1. The ambient temperature is 25±3 ℃.humidity is 65±20%RH, Dark Room.
- 2. The test systems refer to Note 1 and Note 2.



#### Note 1: Definition of optical measurement system.

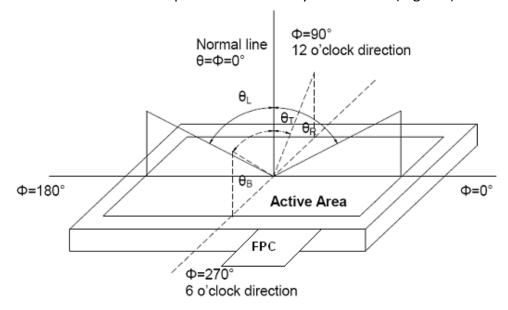
Properties are measured at the center point of the OLED screen. All input terminals OLED panel must be ground when measuring the center area of the panel.



	1		
ltem	Photo detector	Field	
Contrast Ratio			
Luminance	BM-7 or similar	1°	
Chromaticity	equipment		
Lum Uniformity			
Response Time	BM-7A	2°	

Note 2: Definition of viewing angle range and measurement system.

Viewing angle is measured at the center point of the OLED by CONOSCOPE(ergo-80).



Note 3: Definition of contrast ratio

Contrast ratio (CR) = Luminance measured when OLED is on the "White" state

Luminance measured when OLED is on the "Black" state

"White state ": The state is that the OLED should drive by Vwhite.

"Black state": The state is that the OLED should drive by Vblack.

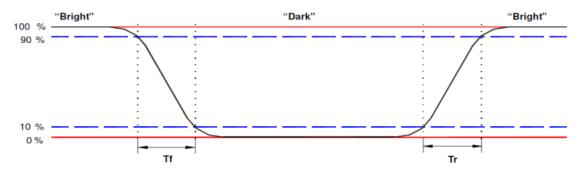
Vwhite: To be determined Vblack: To be determined.

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### Note 4: Definition of response time

The response time is defined as the OLED optical switching time interval between "White" state and "Black" state. Rise time ( $T_{ON}$ ) is the time between photo detector output intensity changed from 90% to 10%. And fall time ( $T_{OFF}$ ) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

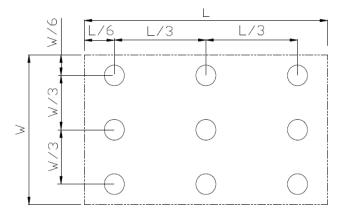
Color coordinates measured at center point of OLED.

#### Note 6: Definition of luminance uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/Lmax

L----- Active area length W---- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

#### Note 7: Definition of luminance:

Measure the luminance of white state at center point.

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# 6 Environmental / Reliability Test

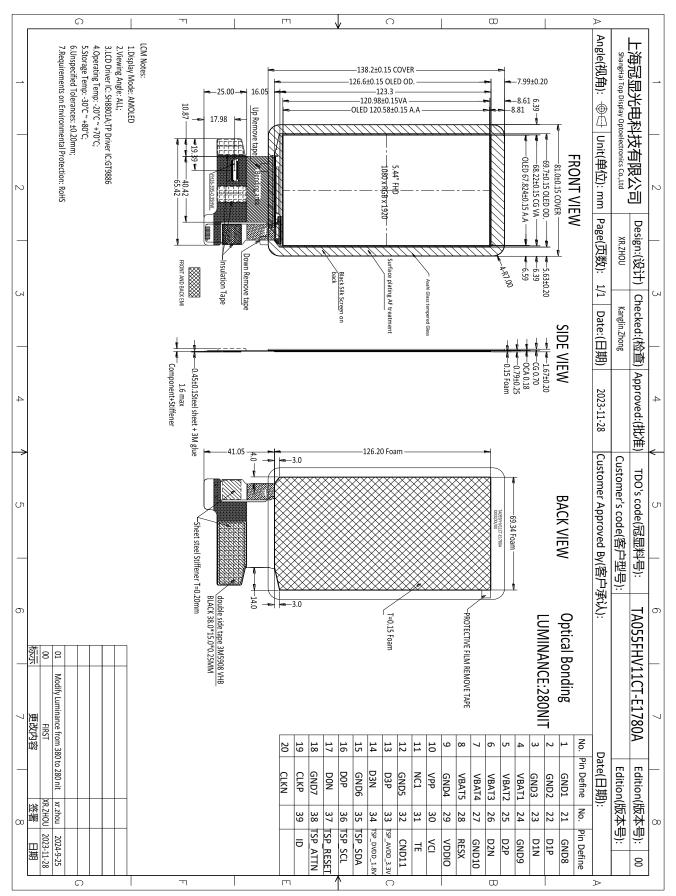
No	Test Item	Condition	Remarks		
1	High Temperature Operation	Ts = +70℃, 120 hours	No abnormalities in functions		
2	Low Temperature Operation	Ta = -20°C, 120 hours	No abnormalities in functions		
3	High Temperature Storage	Ta = +85 °C , 120 hours	No abnormalities in functions		
4	Low Temperature Storage	Ta = -40°C, 120 hours	No abnormalities in functions		
5	Storage at High Temperature and Humidity	Ta = +60 °C, 93% RH max,120hours	No abnormalities in functions		
6	Thermal Shock (non-operating)	-40 °C 30 min~ +85 °C 30 min, Change time: 0.5 hour ← 5 min $\rightarrow$ 0.5 hour.32 Cycle	Start with cold temperature, End with high temperature,		
7	ESD	C=150pF, R=330 $\Omega$ ,5point/panel Air: $\pm$ 6Kv, 20times; Contact: $\pm$ 4Kv,20times (Environment:15 $^{\circ}$ C $^{\circ}$ 35 $^{\circ}$ C, 30% $^{\circ}$ 60%.86Kpa $^{\circ}$ 106Kpa)	No abnormalities in functions		

Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of samples.



## 8 Mechanical Drawing





#### 9 Precautions for Use of OLED Modules

#### **Handling Precautions**

- 9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- 9.1.2 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- 9.1.3 The polarizer covering the display surface of the OLED module is soft and easily scratched. Handle this polarizer carefully.
- 9.1.4 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:
  - Isopropyl alcohol
  - Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents
- 9.1.6 Do not attempt to disassemble the OLED Module.
- 9.1.7 If the logic circuit power is off, do not apply the input signals.
- 9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  - 9.1.8.1 Be sure to ground the body when handling the OLED Modules.
  - 9.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.
- 9.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
- 9.1.8.4 The OLED Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

#### **Storage Precautions**

- 9.2.1 When storing the OLED modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.
- 9.2.2 The OLED modules should be stored under the storage temperature range. If the OLED modules will be stored for a long time, the recommend condition is: Temperature : 0  $^{\circ}$ C  $\sim$  40  $^{\circ}$ C Relatively humidity:  $\leq$ 80%
  - 9.2.3 The OLED modules should be stored in the room without acid, alkali and harmful gas.

#### **Transportation Precautions**

9.3.1 The OLED modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

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