



() Preliminary Specifications
(v) Final Specifications

Module	15.6" (15.55) FHD 16:9 Color TFT-LCD with LED Backlight design
Model Name	G156HTN01.0

<table><tr><td>Customer</td><td>Date</td></tr><tr><td><hr/></td><td><hr/></td></tr><tr><td>Checked & Approved by</td><td></td></tr><tr><td><hr/></td><td><hr/></td></tr></table>	Customer	Date	<hr/>	<hr/>	Checked & Approved by		<hr/>	<hr/>	<table><tr><td>Approved by</td><td>Date</td></tr><tr><td><hr/>Crystal Hsieh</td><td><hr/>2015/01/29</td></tr><tr><td>Prepared by</td><td></td></tr><tr><td><hr/>Sandy Su</td><td><hr/>2015/01/29</td></tr></table>	Approved by	Date	<hr/> Crystal Hsieh	<hr/> 2015/01/29	Prepared by		<hr/> Sandy Su	<hr/> 2015/01/29
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Note: This Specification is subject to change without notice.	Audio-Video Business Unit / AU Optronics corporation																

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Record of Revision

Version and Date	Page	Old description	New Description
0.0 2014/02/20	All	Preliminary Edition for Customer	
0.1 2014/02/24	5	Temperature Range Operating: 0 to +50	-10 to +60 (Surface)
0.2 2014/04/11	5	Contrast Ratio 400:1 Response Time 8 Typ / 16 Max. Weight TBD Width Thickness TBD	700:1 9 Typ / 16 Max. 390 Max 217.28 Max 3.35 Max
	6	Uniformity TBD Contrast Ratio 400:1 Response Time 8 Typ.	65 Min. 80 Typ. 700:1 9 Typ.
	14	Backlight Power Consumption 3.2 Max.	4.3 Max
	24	LCM Outline Dimension (Front View)	Update
	25	LCM Outline Dimension (Rear View)	Update
0.3 2014/05/08	5	Weight 390 Max. Thickness 3.35 Max.	400 Max. 3.55 Max.
	24	LCM Outline Dimension (Front View)	Update
	25	LCM Outline Dimension (Rear View)	Update
1.0 2014/08/14	5	Physical Size--Width: Min. 216.28 Typ. 216.78 Max. 217.28	Update for cell tape adhesive tolerance Min. 216.45 Typ. 216.95 Max.217.75
	6	Optical Characteristics: TBD	Update TBD→ Measuring data
	15	Scanning Direction	Remove reverse scan
	26	Carton Package	Update
1.1 2014/10/15	26	Carton Package	Update Pallet info for MP
1.2 2015/01/29	16	Timing Characteristics	Update for eDP interface timing

1. Operating Precautions

- 1) Since front polarizer is easily damaged, please be cautious and not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or soft cloth.
- 5) Since the panel is made of glass, it may be broken or cracked if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the module assembly.
- 8) Do not press the reflector sheet at the back of the module to any direction.
- 9) In case if a module has to be put back into the packing container slot after it was taken out from the container, do not press the center of the LED Reflector edge. Instead, press at the far ends of the LED Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) TFT-LCD Module is not allowed to be twisted & bent even force is added on module in a very short time. Please design your display product well to avoid external force applying to module by end-user directly.
- 12) Small amount of materials without flammability grade are used in the TFT-LCD module. The TFT-LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950-1 or UL60950-1), or be applied exemption.
- 13) Severe temperature condition may result in different luminance, response time.
- 14) Continuous operating TFT-LCD Module under high temperature environment may accelerate LED light bar exhaustion and reduce luminance dramatically.
- 15) The data on this specification sheet is applicable when TFT-LCD module is placed in landscape position.
- 16) Continuous displaying fixed pattern may induce image sticking. It's recommended to use screen saver or moving content periodically if fixed pattern is displayed on the screen.

2. General Description

G156XTN01.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT-LCD display, a driver circuit, and LED backlight system. The screen format is intended to support 16:9 FHD, 1920(H) x1080(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP (Embedded DisplayPort) interface compatible. All design rules of this module can correspond to PSWG standard.

G156XTN01.0 is designed for industrial display applications.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	15.6" (15.55)			
Active Area	[mm]	344.16 x 193.59			
Pixels H x V		1920 x 3(RGB) x 1080			
Pixel Pitch	[mm]	0.17925 x 0.17925			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance ($I_{LED} = 22 \text{ mA}$) (Note: I_{LED} is LED current)	[cd/m ²]	300 Typ. (5 points average) 240 Min. (5 points average)			
Luminance Uniformity		1.25 Max. (5 points)			
Contrast Ratio		700 :1 Typ			
Response Time	[ms]	9 Typ / 16 Max.			
Nominal Input Voltage VDD	[Volt]	+3.3 Typ.			
Power Consumption	[Watt]	5.3 Max. (Include Logic and BLU Power)			
Weight	[Grams]	400 Max.			
Physical Size Without bracket.	[mm]		Min.	Typ.	Max.
		Length	359.0	359.5	360.0
		Width	216.45	216.95	217.75
		Thickness			3.55
Electrical Interface		2 Lane eDP			
Glass Thickness	[mm]	0.4			
Surface Treatment		Anti-glare (Haze=25%)			
Support Color		262K colors (RGB 6-bit)			
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 -10 to +60 (Surface) -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25 (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance	[cd/m2]	100% Dimming (center point)	240	300	-	1
Uniformity	%	9 Points	65	80	-	1, 2, 3
Contrast Ratio			400	700	-	4
Cross talk	%		-	1.2	1.5	5
Response Time	[msec]	Rising	-	6		6
	[msec]	Falling	-	3		
	[msec]	Raising + Falling	-	9	16	
Viewing Angle	[degree]	Horizontal (Right)	70	80	-	7
	[degree]	CR = 10 (Left)	70	80	-	
	[degree]	Vertical (Upper)	60	70	-	
Color / Chromaticity Coordinates (CIE 1931)		CR = 10 (Lower)	60	70	-	
		Red x	0.590	0.620	0.650	
		Red y	0.320	0.350	0.380	
		Green x	0.290	0.320	0.350	
		Green y	0.570	0.600	0.630	
		Blue x	0.120	0.150	0.180	
		Blue y	0.090	0.120	0.150	
		White x	0.283	0.313	0.343	
Color Gamut		White y	0.299	0.329	0.359	
	%		-	60	-	
Gamma Value			-	2.2	-	8

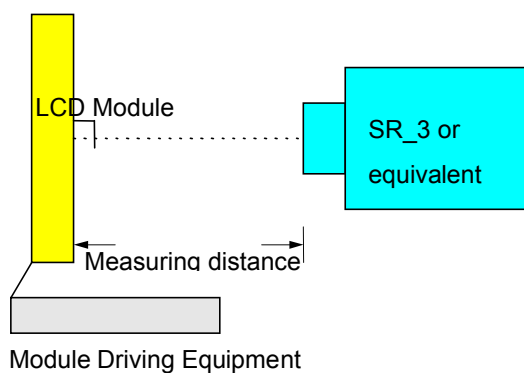
Note 1: Measurement method

Equipment Pattern Generator, Power Supply, Digital Voltmeter, Luminance meter (SR_3 or equivalent)

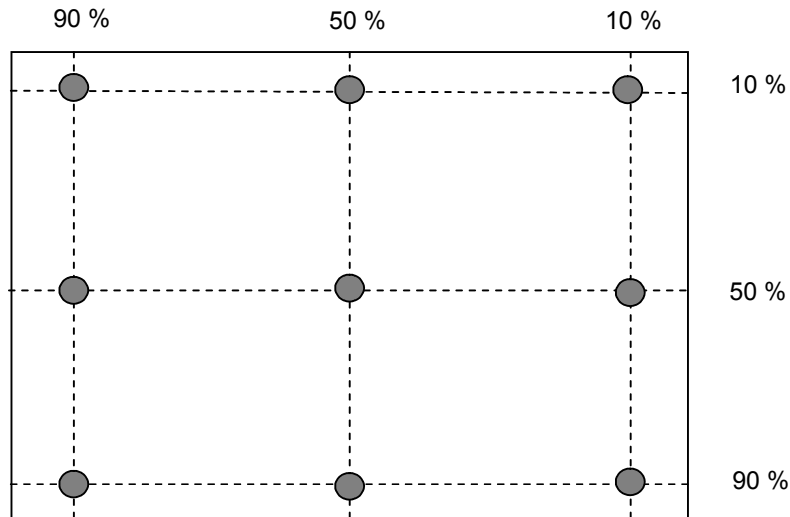
Aperture 1° with 50cm viewing distance

Test Point Center

Environment < 1 lux



Note 2: Definition of 9 points position (Display active area : 304.128(H) x 228.096(V))



Note 3: The luminance uniformity of 9 points is defined by dividing the minimum luminance values by the maximum test point luminance

$$w_9 = \frac{\text{Minimum Brightness of nine points}}{\text{Maximum Brightness of nine points}}$$

Note 4 : Definition of contrast ratio (CR):

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

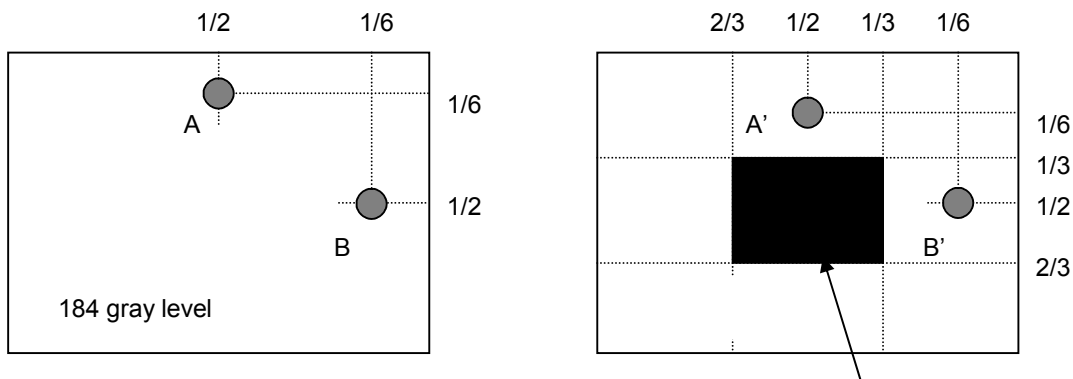
Note 5 : Definition of cross talk (CT)

$$CT = |YB - YA| / YA \times 100 (\%)$$

Where

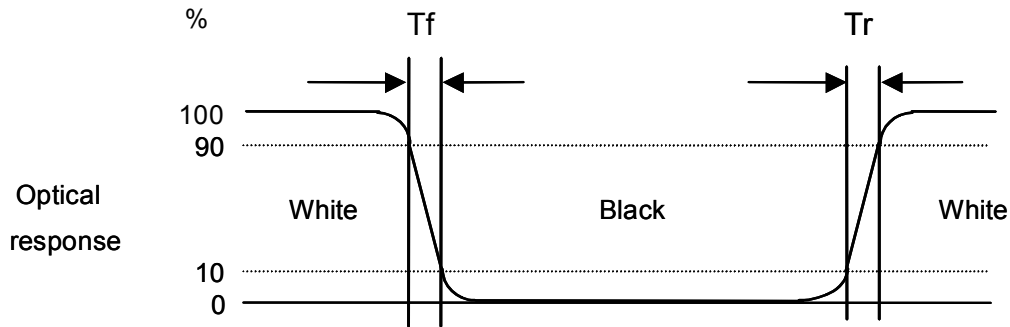
YA = Luminance of measured location without gray level 0 pattern (cd/m²)

YB = Luminance of measured location with gray level 0 pattern (cd/m²)



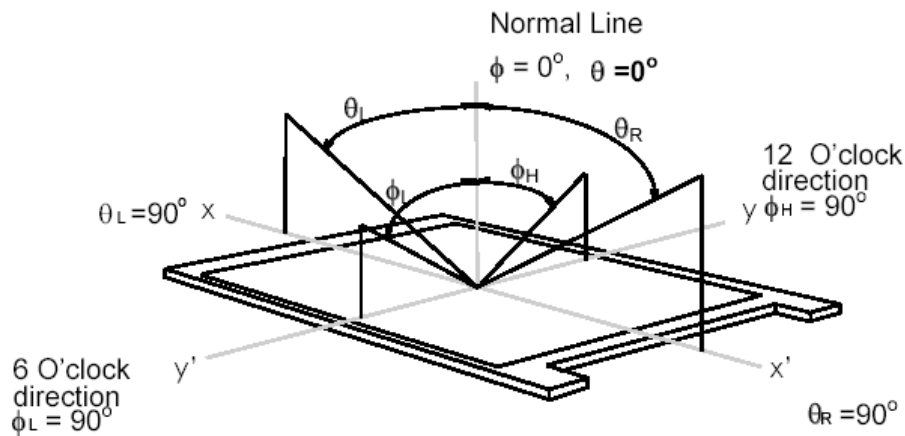
Note 6: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “White” to “Black” (falling time) and from “Black” to “White” (rising time), respectively. The response time interval is between 10% and 90% of amplitudes. Please refer to the figure as below.



Note 7: Definition of viewing angle

Viewing angle is the measurement of contrast ratio 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as below: 90° (θ) horizontal left and right, and 90° (ϕ) vertical high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated to its center to develop the desired measurement viewing angle.



Note 8: Note 8: Definition of Gamma Value

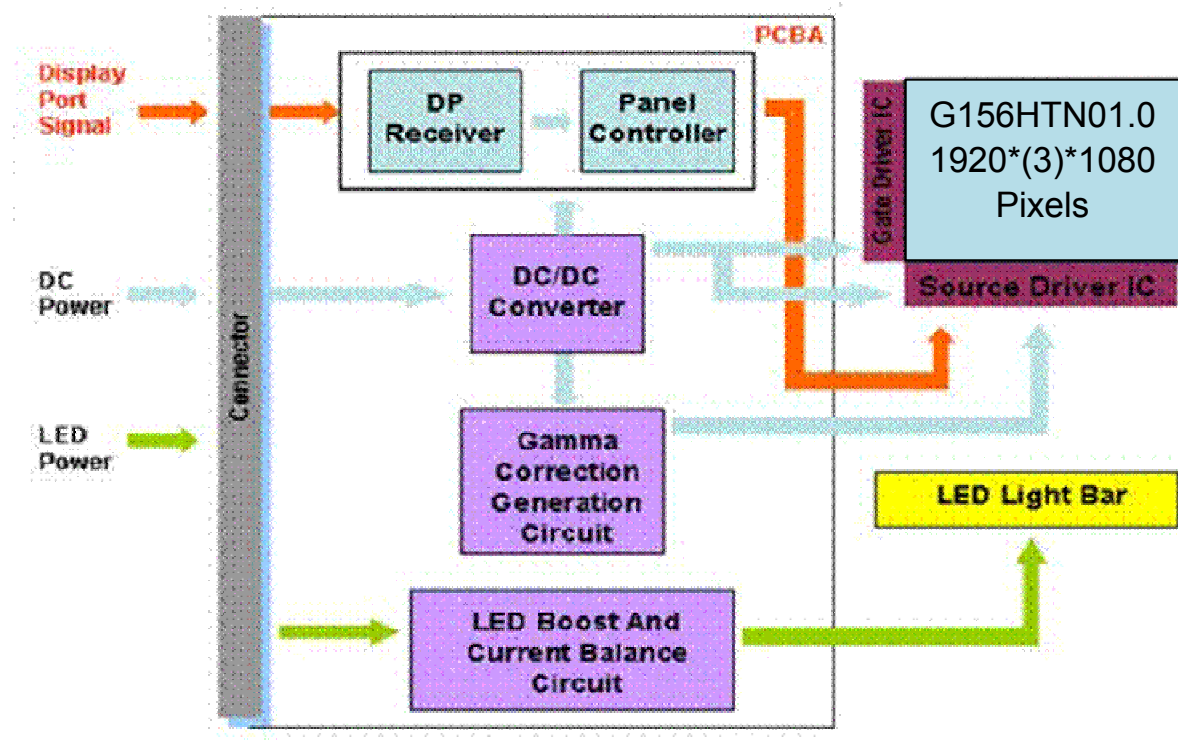
Generally, Gamma Value is defined as the slope of a Gray Level – Luminance curve in log-log space, that is

$$= d \log(\text{Luminance}) / d \log(\text{Gray Level})$$

The Gamma Value defined in this spec is Linear Regression (1, 2, 3..., 16). 1 to 16 are the section gamma of the following 17 sampling points, GL(0), GL(16), GL(32), GL(48), GL(64), GL(80), GL(96), GL(112), GL(128), GL(144), GL(160), GL(176), GL(192), GL(208), GL(224), GL(240) and GL(255), in 8 bits input.

3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 30 Pin.



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

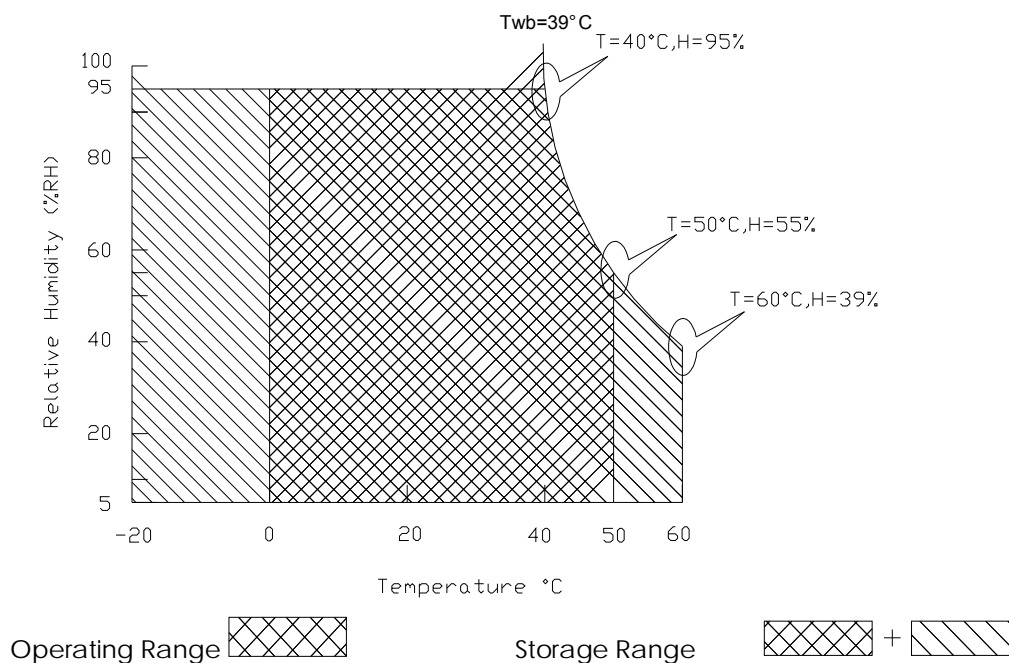
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	-10	+60	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



5. Electrical Characteristics

5.1 TFT LCD Module

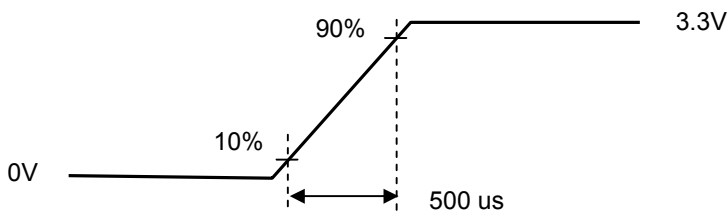
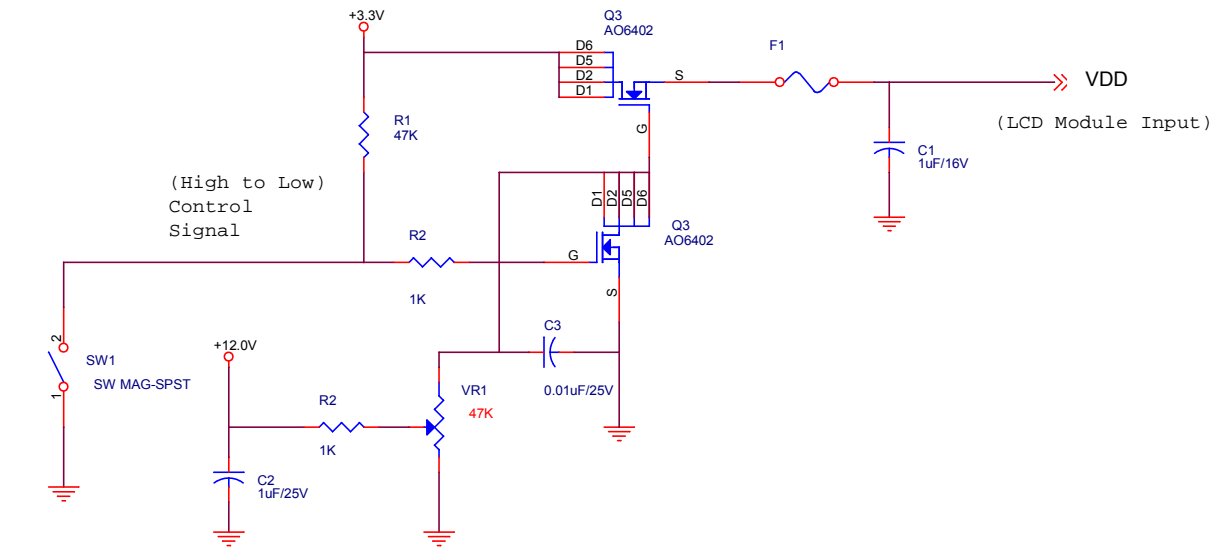
5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25 °C and frame frequency under 60Hz.

Symbol	Parameter	Min	Typ	Max	Units	Remark
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	± 10%
IDD	IDD Current	-	-	606	[mA]	64 Gray Bar Pattern (VDD=3.3V, at 60Hz)
Irush	LCD Inrush Current	-	-	2000	[mA]	Note 1
PDD	VDD Power	-	-	1.0	[Watt]	64 Gray Bar Pattern (VDD=3.3V, at 60Hz)
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1: Measurement condition:



VDD rising time



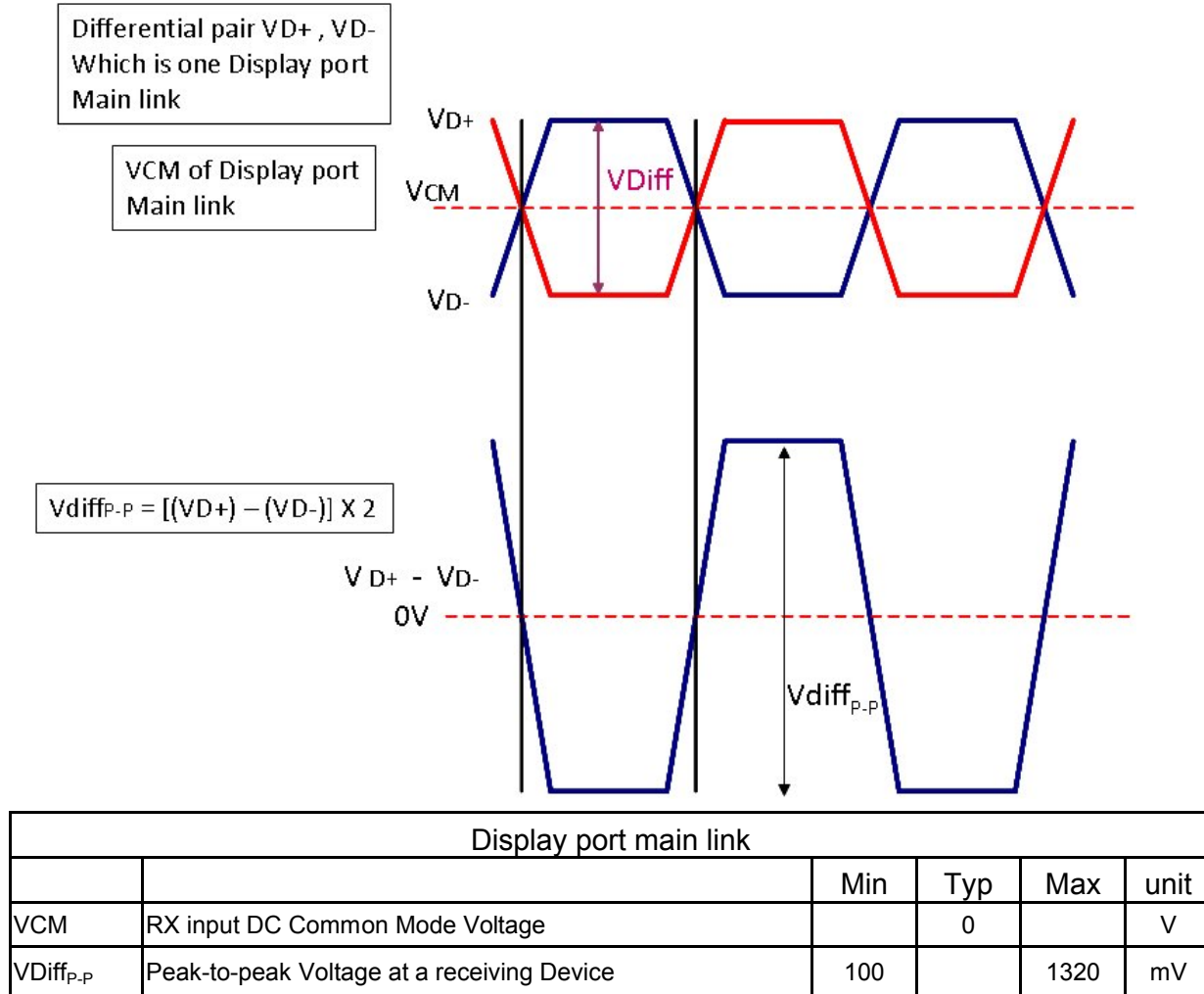
64 Gray pattern

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

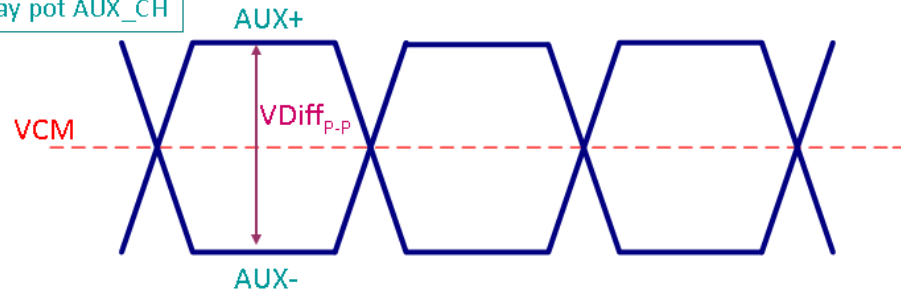
Display Port main link signal:



Fallow as VESA display port standard V1.1a

Display Port AUX_CH signal:

Differential AUX+ , AUX-
Which is Display port AUX_CH



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff _{P-P}	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Fallow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

Fallow as VESA display port standard V1.1a.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	4.3	[Watt]	(Ta=25 °C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25 °C), Note 2 IF=22 mA

Note 1: Calculator value for reference $P_{LED} = V_F \text{ (Normal Distribution)} * I_F \text{ (Normal Distribution)} / \text{Efficiency}$

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

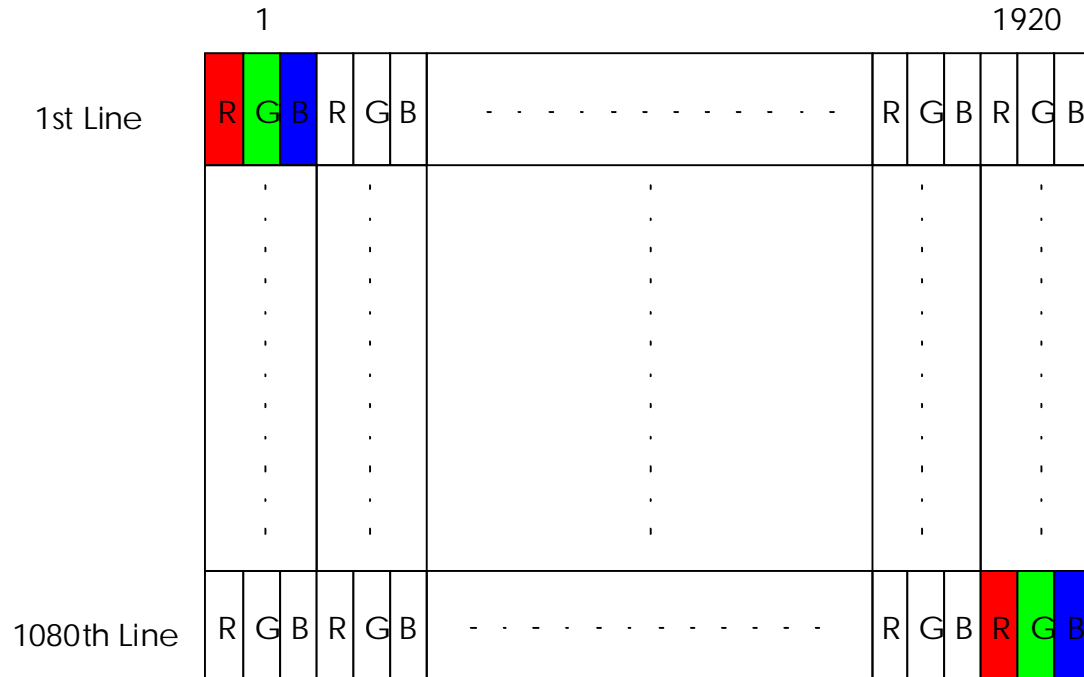
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25 °C)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level	*Note 1	-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level	*Note 1	-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10k	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommended system pull up/down resistor no bigger than 10kohm.

6. Signal Characteristic

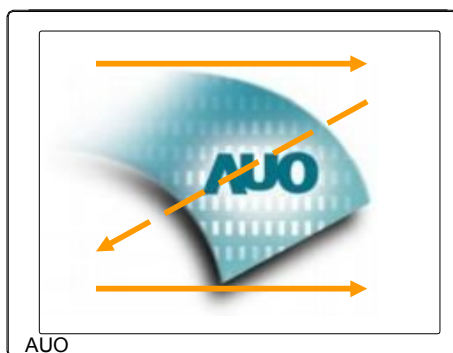
6.1 Pixel Format Image

Following figure shows the relationship between input signal and LCD pixel format.



6.2 Scanning Direction

The following figures show the image seen from the front view. The arrow indicates the direction of scan.



6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

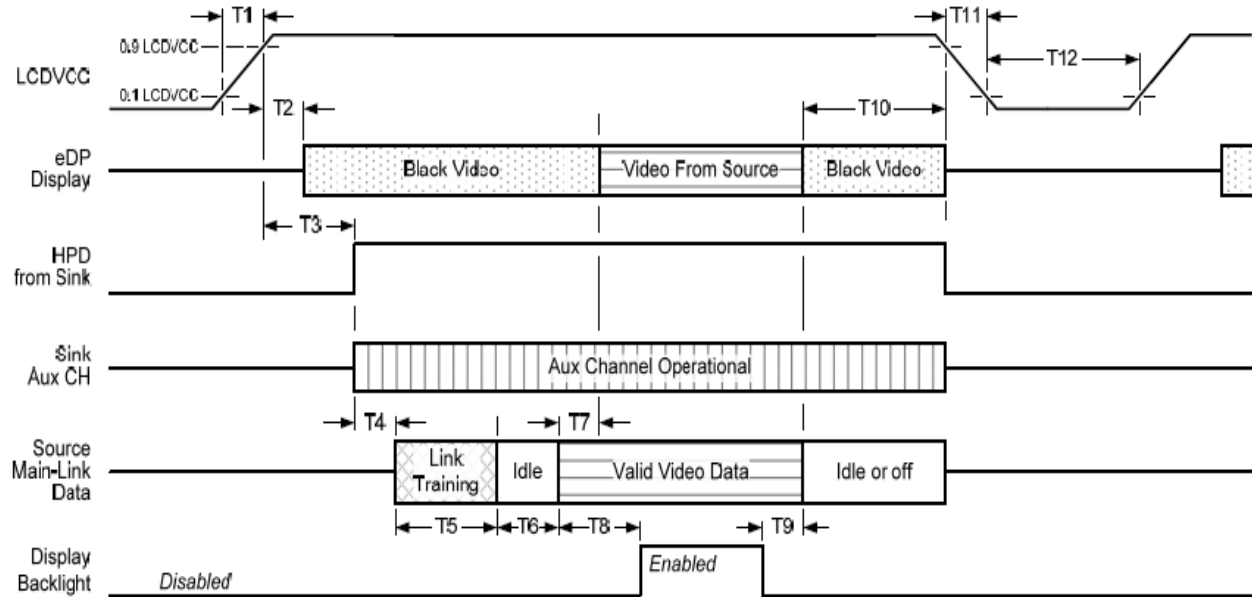
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-		60	-	Hz
Clock frequency		1/ T _{Clock}		141		MHz
Vertical Section	Period	T _V	1090	1116	1080+A	T _{Line}
	Active	T _{VD}	1080			
	Blanking	T _{VB}	10	36	A	
Horizontal Section	Period	T _H	2070	2104	1920+B	T _{Clock}
	Active	T _{HD}	1920			
	Blanking	T _{HB}	150	184	B	

Note 1 : DE mode only

Note 2 : The maximum clock frequency = (1920+B)*(1080+A)*60 < 148MHz

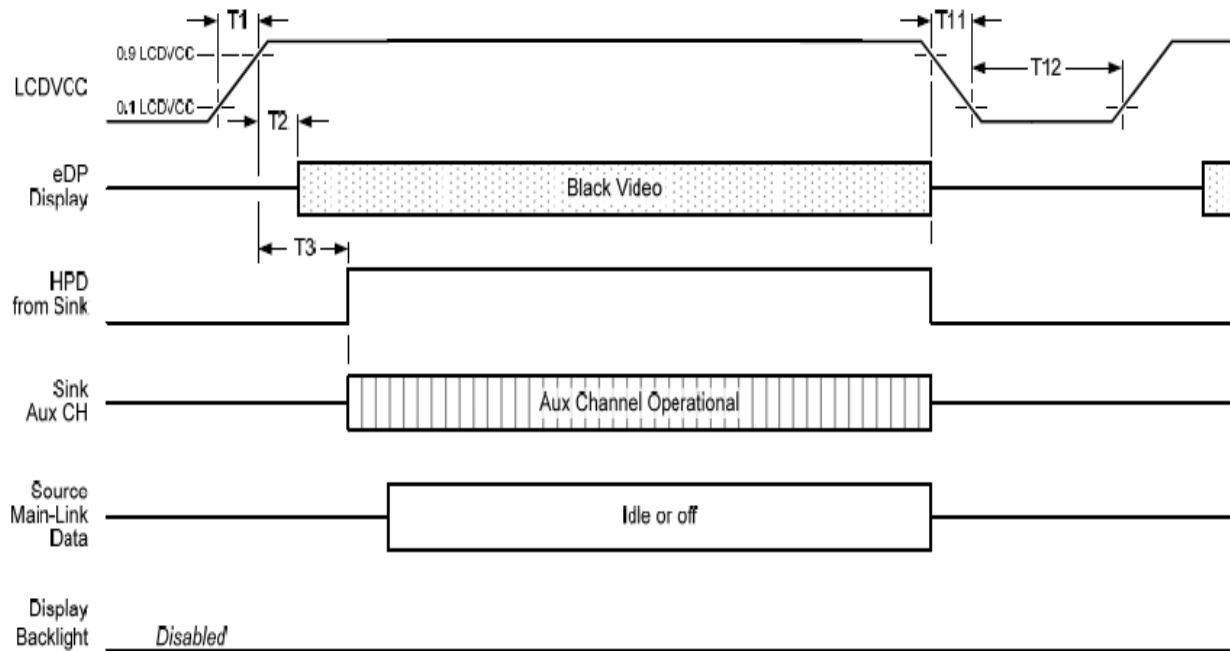
6.4 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

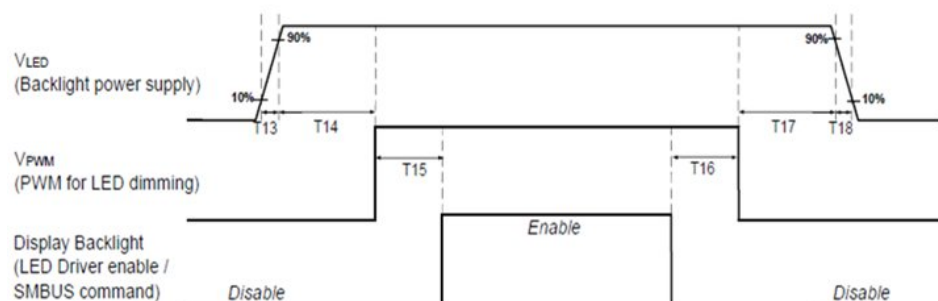
- upon LCDVDD power on (within T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).

- when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

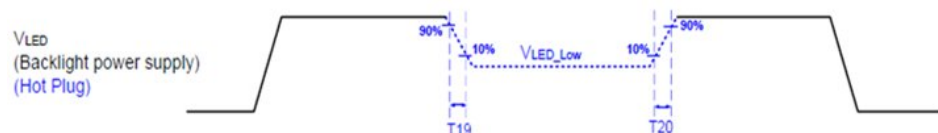
Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: $T19/T20 = 5 \times T_{PWM}^*$

* $T_{PWM} = 1/PWM \text{ Frequency}$

7. Integration Interface Requirement

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

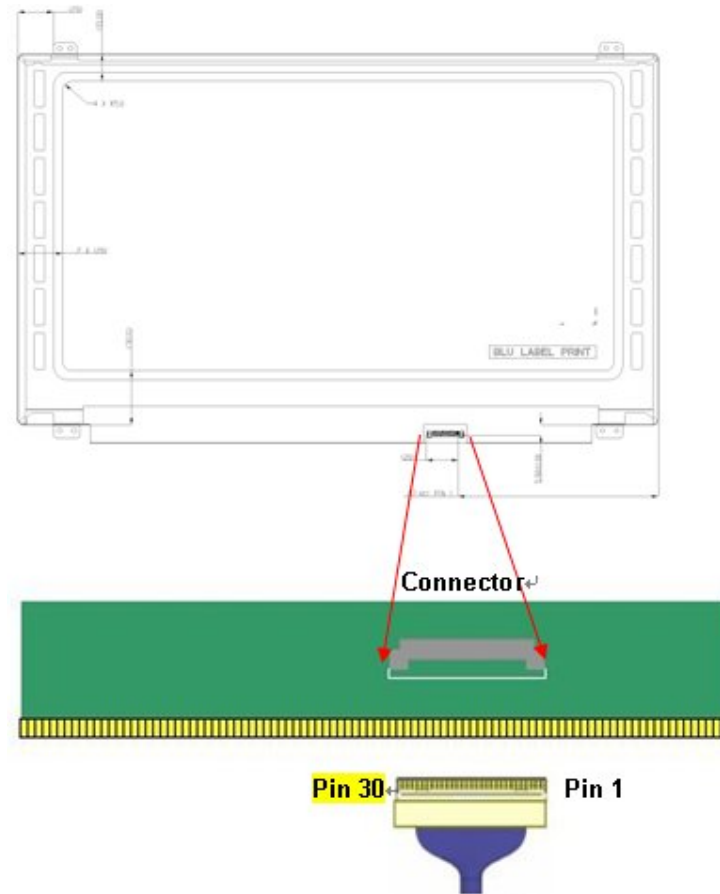
7.1 Connector Description

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or Compatible
Type / Part Number	IPEX 20455-030E-12 or Compatible
Mating Housing/Part Number	IPEX 20353-030T-11 or Compatible

7.2 Pin Assignment (2 Lane)

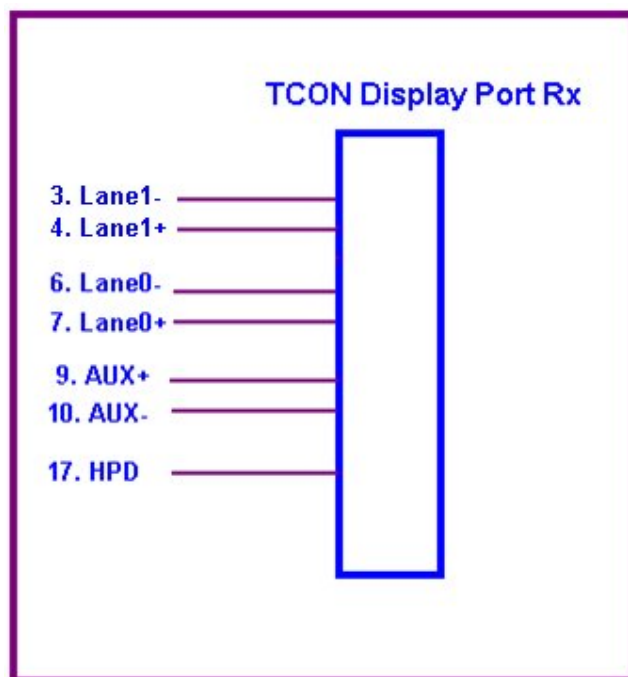
eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	No Connect
2	H_GND	High Speed Ground
3	Lane 1_N	Comp Signal Link Lane 1
4	Lane 1_P	Comp Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL_PWM_DIM	System PWM signal Input
24	NC	Reverse for AUO TEST only
25	NC	Reverse for AUO TEST only
26	BL_PWR	Backlight power (6V~21V)
27	BL_PWR	Backlight power (6V~21V)
28	BL_PWR	Backlight power (6V~21V)
29	BL_PWR	Backlight power (6V~21V)
30	NC	No Connect



Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



8. Reliability Test Criteria

8.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 200 - 10 Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 50 G , Half sine wave
- Active time: 20ms
- Pulse: X,Y,Z .one time for each side

8.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40 , 90%RH, 300h	
High Temperature Operation	Ta= 60 , Dry, 300h for panel surface temp.	
Low Temperature Operation	Ta= -10 , 300h	
High Temperature Storage	Ta= 60 , 35%RH, 300h	
Low Temperature Storage	Ta= -20 , 50%RH, 250h	
Thermal Shock Test	Ta=-20 to 60 , Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed.

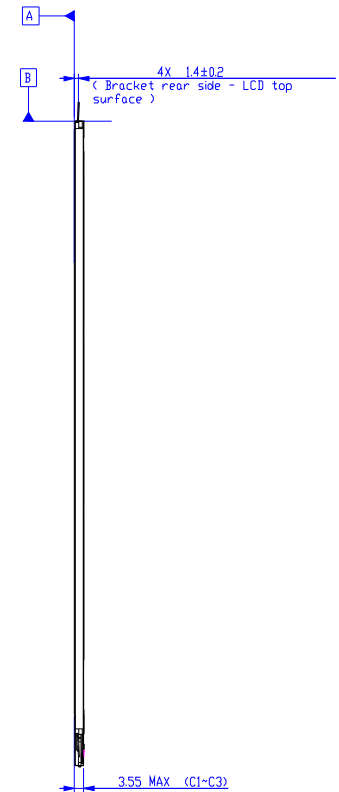
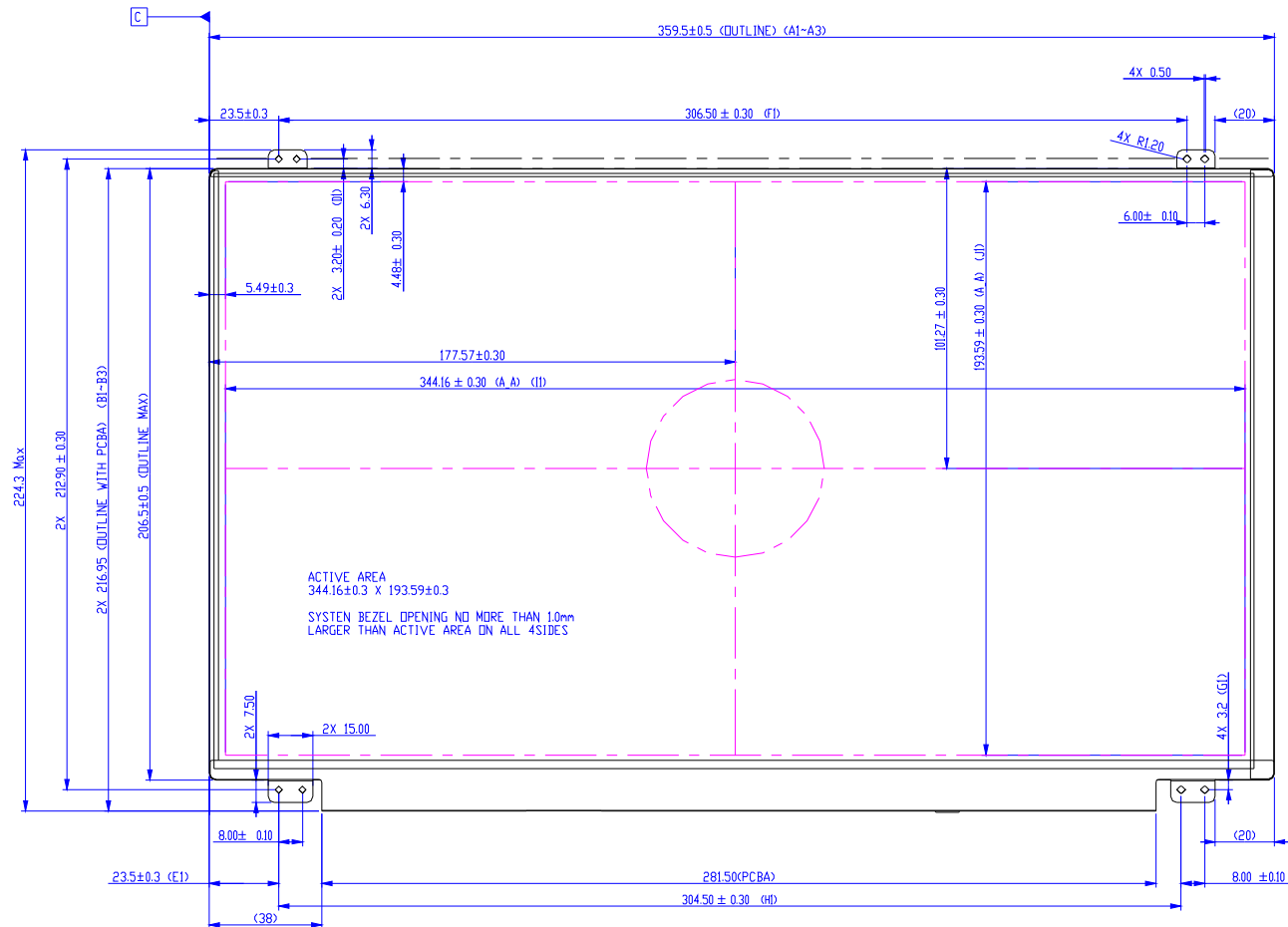
Self-recoverable. No data lost, No hardware failures. Mura shall be ignored after high temperature reliability test.



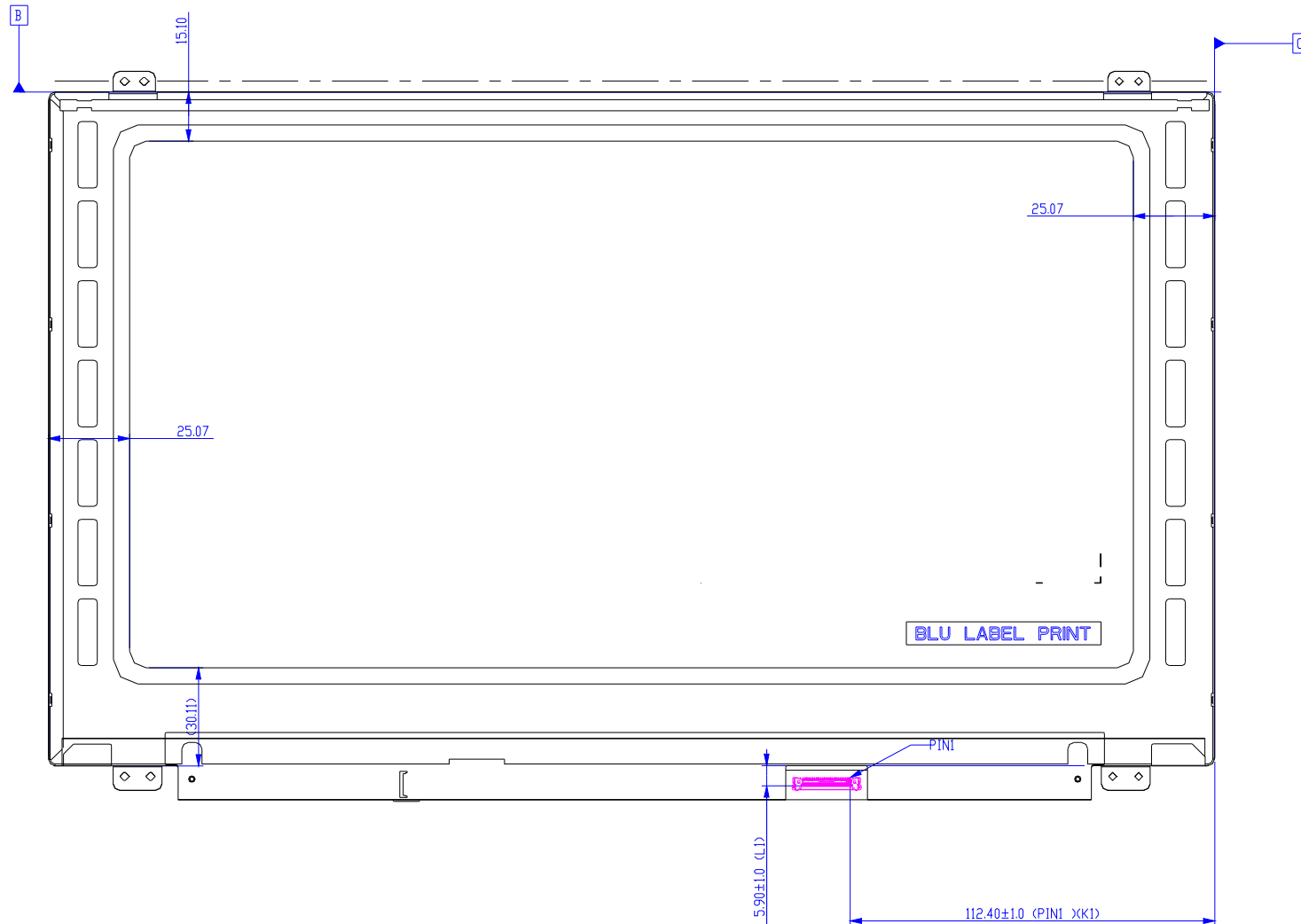
G156HTN01.0

9. Mechanical Characteristics

9.1 LCM Outline Dimension (Front View)



9.2 LCM Outline Dimension (Rear View)



Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

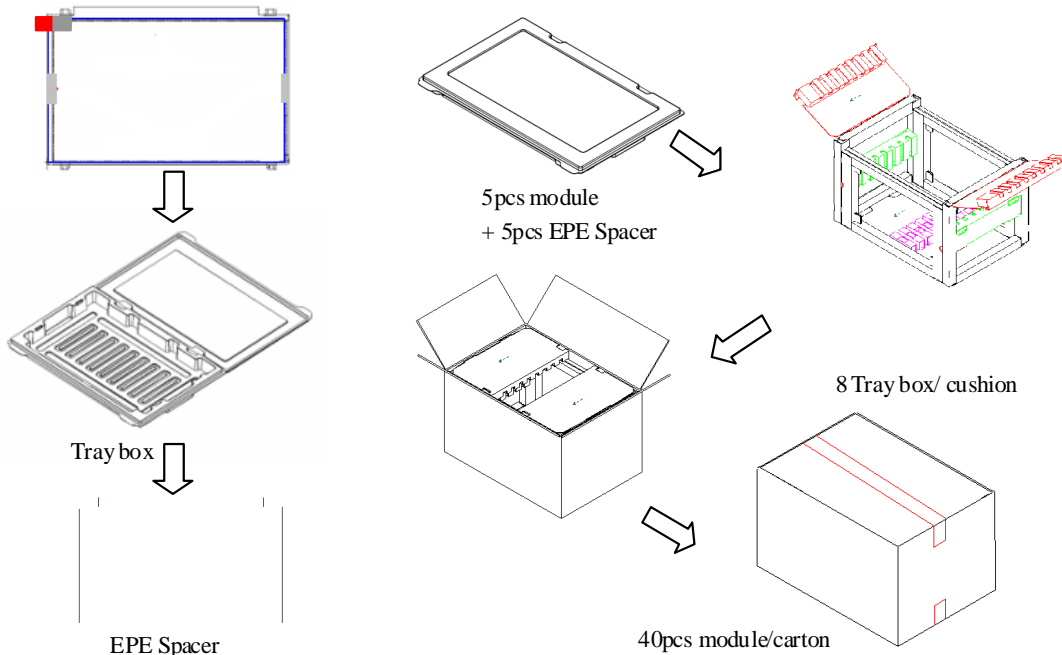
10. Label and Packaging

10.1 Shipping Label (on the rear side of TFT-LCD display)



10.2 Carton Package

Max capacity: 40 pcs TFT-LCD module per carton
Max weight: 19 kg per carton
Outside dimension of carton: 480mm*341mm*302mm
Pallet size: 1140mm*980mm*138mm



Palletizing

Module by air : (2 *3) *4 layers , one pallet put 24 boxes , total 960pcs module

Module by sea : (2 *3) *4 layers+(2 *3) *2 layers , two pallet put 36 boxes , total 1440pcs module

Module by sea_HQ : (2 *3) *4 layers+(2 *3) *3 layers , two pallet put 42 boxes , total 1680 pcs module

11. Safety

11.1 Sharp Edge Requirements

There will be no sharp edges or comers on the display assembly that could cause injury.

11.2 Materials

11.2.1 Toxicity

There will be no carcinogenic materials used anywhere in the display module. If toxic materials are used, they will be reviewed and approved by the responsible AUO toxicologist.

11.2.2 Flammability

All components including electrical components that do not meet the flammability grade UL94-V1 in the module will complete the flammability rating exception approval process.

The printed circuit board will be made from material rated 94-V1 or better. The actual UL flammability rating will be printed on the printed circuit board.

11.3 Capacitors

If any polarized capacitors are used in the display assembly, provisions will be made to keep them from being inserted backwards.

11.4 National Test Lab Requirement

The display module will satisfy all requirements for compliance to:

UL 60950-1, Second Edition

U.S.A. Information Technology Equipment

12. Appendix: EDID description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	ED	11101101	237	
0B	hex, LSB first	35	00110101	53	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	17	00010111	23	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	Video input def. <i>(digital I/P, non-TMDS, CRGB)</i>	95	10010101	149	
15	Max H image size <i>(rounded to cm)</i>	22	00100010	34	
16	Max V image size <i>(rounded to cm)</i>	13	00010011	19	
17	Display Gamma <i>(=(gamma*100)-100)</i>	78	01111000	120	
18	Feature support <i>(no DPMS, Active OFF, RGB, tmg Blk#1)</i>	02	00000010	2	
19	Red/green low bits (Lower 2:2:2:2 bits)	D1	11010001	209	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	15	00010101	21	
1B	Red x (Upper 8 bits)	9E	10011110	158	
1C	Red y/ highER 8 bits	59	01011001	89	
1D	Green x	53	01010011	83	
1E	Green y	9B	10011011	155	
1F	Blue x	27	00100111	39	
20	Blue y	1E	00011110	30	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	

2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	78	01111000	120	
37	Pixel Clock/10000 USB	37	00110111	55	
38	Horz active Lower 8bits	80	10000000	128	
39	Horz blanking Lower 8bits	B4	10110100	180	
3A	HorzAct:HorzBlink Upper 4:4 bits	70	01110000	112	
3B	Vertical Active Lower 8bits	38	00111000	56	
3C	Vertical Blanking Lower 8bits	2E	00101110	46	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	40	01000000	64	
3E	HorzSync. Offset	6C	01101100	108	
3F	HorzSync.Width	30	00110000	48	
40	VertSync.Offset : VertSync.Width	AA	10101010	170	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
42	Horizontal Image Size Lower 8bits	58	01011000	88	
43	Vertical Image Size Lower 8bits	C1	11000001	193	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16	
45	Horizontal Border <i>(zero for internal LCD)</i>	00	00000000	0	
46	Vertical Border <i>(zero for internal LCD)</i>	00	00000000	0	
47	Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i>	18	00011000	24	
48	Pixel Clock/10,000 (LSB)	FB	11111011	251	40Hz frame rate
49	Pixel Clock/10,000 (MSB)	24	00100100	36	
4A	Horizontal Addressable Pixels, lower 8 bits	80	10000000	128	
4B	Horizontal Blanking Pixels, lower 8 bits	B4	10110100	180	
4C	H Pixels, upper nibble : H Blanking, upper nibble	70	01110000	112	
4D	Vertical Addressable Lines, lower 8 bits	38	00111000	56	
4E	Vertical Blanking Lines, lower 8 bits	2E	00101110	46	
4F	V lines, upper nibble : V blanking, upper nibble	40	01000000	64	
50	Horizontal Front Porch, lower 8 bits	6C	01101100	108	
51	Horizontal Sync Pulse, lower 8 bits	30	00110000	48	
52	V Front Porch, lower nibble : V Sync Pulse, lower nibble	AA	10101010	170	
53	VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits	00	00000000	0	
54	Horizontal Image Size in mm, lower 8 bits	58	01011000	88	
55	Vertical Image Size in mm, lower 8 bits	C1	11000001	193	
56	H Image Size, upper nibble : V Image Size, upper nibble	10	00010000	16	

57	Horizontal Border	00	00000000	0	
58	Vertical Border	00	00000000	0	
59	Bit Encode Sync Information	18	00011000	24	
5A	DC	00	00000000	0	nVDPS Reserved 00
5B	HTOTAL	00	00000000	0	
5C	HA	00	00000000	0	
5D	HBL	00	00000000	0	
5E	HFP	00	00000000	0	
5F	HFPe	00	00000000	0	
60	HBP	00	00000000	0	
61	HB	00	00000000	0	
62	HSO	00	00000000	0	
63	HS	00	00000000	0	
64	VTOTAL	00	00000000	0	
65	VA	00	00000000	0	
66	VBL	00	00000000	0	
67	VFP	00	00000000	0	
68	VBP	00	00000000	0	
69	VB	00	00000000	0	
6A	VSO	00	00000000	0	Header
6B	VS	00	00000000	0	
6C	Detail Timing Description #4	00	00000000	0	
6D	Flag	00	00000000	0	
6E	Reserved	00	00000000	0	Brightness Table
6F	For Brightness Table and Power Consumption	02	00000010	2	
70	Flag	00	00000000	0	
71	PWM % [7:0] @ Step 0	0C	00001100	12	
72	PWM % [7:0] @ Step 5	33	00110011	51	
73	PWM % [7:0] @ Step 10	FF	11111111	255	
74	Nits [7:0] @ Step 0	0E	00001110	14	Power Consumption
75	Nits [7:0] @ Step 5	3C	00111100	60	
76	Nits [7:0] @ Step 10	96	10010110	150	
77	Panel Electronics Power @ 32x32 Chess Pattern =	1B	00011011	27	
78	Backlight Power @ 60 nits =	0D	00001101	13	
79	Backlight Power @ Step 10 =	1C	00011100	28	
7A	Nits @ 100% PWM Duty =	96	10010110	150	
7B	Flag	20	00100000	32	
7C	Flag	20	00100000	32	
7D	Flag	20	00100000	32	
7E	Extension Flag	00	00000000	0	
7F	Checksum	41	01000001	65	