Product Functional Specification

15 inch SXGA+ Color TFT LCD Module
Model Name: B150PG03 V0

(◆) Preliminary Specification
( ) Final Specification

Note: This Specification is subject to change without notice.

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I. Contents

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II Record of Revision

<table>
<tr><th>Version and Date</th><th>Page</th><th>Old description</th><th>New Description</th><th>Remark</th></tr>
<tr><td>0.0. 2004/4/7</td><td>All</td><td>First Edition for Customer</td><td>All</td><td></td></tr>
<tr><td rowspan="7">0.1. 2004/5/25</td><td>7</td><td>Physical Size [mm]
317.3 x 242.0 x 6.0 (typ)</td><td>Physical Size [mm]
317.3 x 242.0 x 6.5 (max)</td><td>Modification is under “section 2.1”</td></tr>
<tr><td>9</td><td>N/A</td><td>Add “Wet bulb temperature chart”</td><td></td></tr>
<tr><td>10</td><td>
<table>
<tr><th>Conditions</th><th>Min.</th><th>Typ.</th><th>Max.</th></tr>
<tr><td>Red x</td><td>0.549</td><td>0.564</td><td>0.578</td></tr>
<tr><td>Red y</td><td>0.326</td><td>0.330</td><td>0.335</td></tr>
<tr><td>Green x</td><td>0.303</td><td>0.308</td><td>0.314</td></tr>
<tr><td>Green y</td><td>0.526</td><td>0.537</td><td>0.548</td></tr>
<tr><td>Blue x</td><td>0.149</td><td>0.153</td><td>0.157</td></tr>
<tr><td>Blue y</td><td>0.129</td><td>0.136</td><td>0.143</td></tr>
</table>
</td><td>
<table>
<tr><th>Conditions</th><th>Min.</th><th>Typ.</th><th>Max.</th></tr>
<tr><td>Red x</td><td>0.538</td><td>0.568</td><td>0.598</td></tr>
<tr><td>Red y</td><td>0.312</td><td>0.342</td><td>0.372</td></tr>
<tr><td>Green x</td><td>0.276</td><td>0.306</td><td>0.336</td></tr>
<tr><td>Green y</td><td>0.529</td><td>0.559</td><td>0.589</td></tr>
<tr><td>Blue x</td><td>0.123</td><td>0.153</td><td>0.183</td></tr>
<tr><td>Blue y</td><td>0.111</td><td>0.141</td><td>0.171</td></tr>
</table>
</td><td>Modification of “section 4.0”: Color / Chromaticity Coordinates (CIE 1931) : Modifications of R/G/B parts only</td></tr>
<tr><td>11</td><td>N/A</td><td>Add “5 points position”</td><td></td></tr>
<tr><td>16</td><td>
LVDS Macro AC characteristics are as follows
<table>
<tr><th></th><th>Min.</th><th>Max.</th></tr>
<tr><td>Clock Frequency (T)</td><td>TBD</td><td>TBD</td></tr>
<tr><td>Data Setup Time (Tsu)</td><td>TBD</td><td></td></tr>
<tr><td>Data Hold Time (Thd)</td><td>TBD</td><td></td></tr>
</table>
</td><td>
LVDS Macro AC characteristics are as follows
<table>
<tr><th></th><th>Min.</th><th>Max.</th></tr>
<tr><td>Clock Frequency (T)</td><td>25MHz</td><td>115MHz</td></tr>
<tr><td>Data Setup Time (Tsu)</td><td>600ps</td><td></td></tr>
<tr><td>Data Hold Time (Thd)</td><td>600ps</td><td></td></tr>
</table>
</td><td>Modifications of “section 5.4”: update “TBD”s to actual values</td></tr>
<tr><td>19</td><td>
8.1 Timing Characteristics
<table>
<tr><th>Symbol</th><th>Description</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>fdck</td><td>DTCLK Frequency</td><td></td><td>54.00</td><td></td><td>[MHz]</td></tr>
<tr><td>tck</td><td>DTCLK cycle time</td><td></td><td>18.5</td><td></td><td>[nsec]</td></tr>
<tr><td>tx</td><td>X total time</td><td>TBD</td><td>844</td><td>TBD</td><td>[tck]</td></tr>
<tr><td>tacx</td><td>X active time</td><td>TBD</td><td>700</td><td></td><td>[tck]</td></tr>
<tr><td>tblkx</td><td>X blank time</td><td></td><td>144</td><td></td><td>[tck]</td></tr>
<tr><td>Hsync</td><td>H frequency</td><td></td><td>63.98</td><td></td><td>[KHz]</td></tr>
<tr><td>Hsw</td><td>H-Sync width</td><td>TBD</td><td>56</td><td></td><td>[tck]</td></tr>
<tr><td>Hbp</td><td>H back porch</td><td>TBD</td><td>64</td><td></td><td>[tck]</td></tr>
<tr><td>Hfp</td><td>H front porch</td><td>TBD</td><td>24</td><td></td><td>[tck]</td></tr>
<tr><td>ty</td><td>Y total time</td><td>TBD</td><td>1066</td><td>TBD</td><td>[tx]</td></tr>
<tr><td>tacy</td><td>Y active time</td><td></td><td>1050</td><td></td><td>[tx]</td></tr>
<tr><td>Vsync</td><td>Frame rate</td><td>(55)</td><td>60</td><td>61</td><td>[Hz]</td></tr>
<tr><td>Vw</td><td>V-sync Width</td><td>1</td><td>3</td><td></td><td>[tx]</td></tr>
<tr><td>Vfp</td><td>V-sync front porch</td><td>1</td><td>1</td><td></td><td>[tx]</td></tr>
<tr><td>Vbp</td><td>V-sync back porch</td><td>7</td><td>12</td><td>63</td><td>[tx]</td></tr>
</table>
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<tr><th>Symbol</th><th>Description</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>fdck</td><td>DTCLK Frequency</td><td></td><td>54.00</td><td></td><td>[MHz]</td></tr>
<tr><td>tck</td><td>DTCLK cycle time</td><td></td><td>18.5</td><td></td><td>[nsec]</td></tr>
<tr><td>tx</td><td>X total time</td><td>740</td><td>844</td><td>1000</td><td>[tck]</td></tr>
<tr><td>tacx</td><td>X active time</td><td>700</td><td>700</td><td></td><td>[tck]</td></tr>
<tr><td>tblkx</td><td>X blank time</td><td></td><td>144</td><td></td><td>[tck]</td></tr>
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<tr><td>Hfp</td><td>H front porch</td><td>C</td><td>24</td><td></td><td>[tck]</td></tr>
<tr><td>ty</td><td>Y total time</td><td>1054</td><td>1066</td><td>2048</td><td>[tx]</td></tr>
<tr><td>tacy</td><td>Y active time</td><td></td><td>1050</td><td></td><td>[tx]</td></tr>
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<tr><td>Vw</td><td>V-sync Width</td><td>1</td><td>3</td><td>8</td><td>[tx]</td></tr>
<tr><td>Vfp</td><td>V-sync front porch</td><td>1</td><td>1</td><td></td><td>[tx]</td></tr>
<tr><td>Vbp</td><td>V-sync back porch</td><td>7</td><td>12</td><td>63</td><td>[tx]</td></tr>
</table>
</td><td>Modifications of “section 8.1”: update “TBD”s to actual values</td></tr>
<tr><td>20</td><td>
9.0 Power Consumption
Input power specifications are as followed,
<table>
<tr><th>Symbol</th><th>Parameter</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th><th>Condition</th></tr>
<tr><td>VDD</td><td>Logic/LCD Drive Voltage</td><td>3.0</td><td>3.3</td><td>3.6</td><td>[Volt]</td><td>Load Capacitance 20uF</td></tr>
<tr><td>PDD</td><td>VDD Power</td><td></td><td>TBD</td><td></td><td>[Watt]</td><td>All Black Pattern</td></tr>
<tr><td>PDD Max</td><td>VDD Power max</td><td></td><td></td><td>TBD</td><td>[Watt]</td><td>Max Pattern Note</td></tr>
<tr><td>IDD</td><td>IDD Current</td><td></td><td>TBD</td><td></td><td>mA</td><td>All Black Pattern</td></tr>
<tr><td>IDD Max</td><td>IDD Current max</td><td></td><td></td><td>TBD</td><td>mA</td><td>Max Pattern Note</td></tr>
<tr><td>VDDrp</td><td>Allowable Logic/LCD Drive Ripple Voltage</td><td></td><td></td><td>100</td><td>[mV] p-p</td><td></td></tr>
<tr><td>VDDns</td><td>Allowable Logic/LCD Drive Ripple Noise</td><td></td><td></td><td>100</td><td>[mV] p-p</td><td></td></tr>
</table>
</td><td>
9.0 Power Consumption
Input power specifications are as followed,
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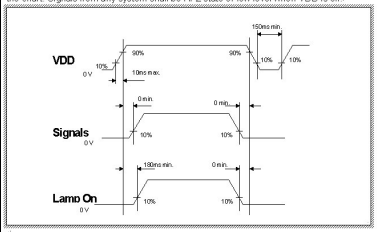
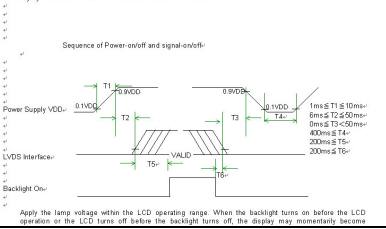
<tr><th>Symbol</th><th>Parameter</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th><th>Condition</th></tr>
<tr><td>VDD</td><td>Logic/LCD Drive Voltage</td><td>3.0</td><td>3.3</td><td>3.6</td><td>[Volt]</td><td>Load Capacitance 20uF</td></tr>
<tr><td>PDD</td><td>VDD Power</td><td></td><td>1.8</td><td></td><td>[Watt]</td><td>All Black Pattern</td></tr>
<tr><td>PDD Max</td><td>VDD Power max</td><td></td><td></td><td>1.93</td><td>[Watt]</td><td>Max Pattern (Note)</td></tr>
<tr><td>IDD</td><td>IDD Current</td><td></td><td>550</td><td></td><td>mA</td><td>All Black Pattern</td></tr>
<tr><td>IDD Max</td><td>IDD Current max</td><td></td><td></td><td>585</td><td>mA</td><td>Max Pattern (Note)</td></tr>
<tr><td>VDDrp</td><td>Allowable Logic/LCD Drive Ripple Voltage</td><td></td><td></td><td>100</td><td>[mV] p-p</td><td></td></tr>
<tr><td>VDDns</td><td>Allowable Logic/LCD Drive Ripple Noise</td><td></td><td></td><td>100</td><td>[mV] p-p</td><td></td></tr>
</table>
</td><td>Modifications of “section 9.0”: update “TBD”s to actual values</td></tr>
<tr><td>21</td><td>
10. Power ON/OFF Sequence
VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.


</td><td>
10. Power ON/OFF Sequence
VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.


</td><td>Modification of “section 10.0”</td></tr>
<tr><td>22</td><td>N/A</td><td>Add ”11.0 Reliability / Safety Requirement”</td><td></td></tr>
</table>

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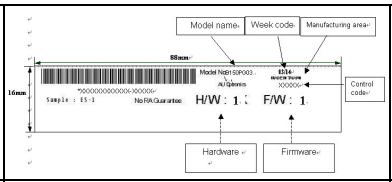
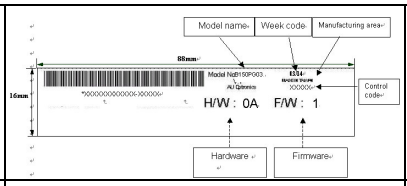
<table>
<tr><td></td><td>25</td><td> 
</td><td> 
</td><td>Modification of “section 13.0”</td></tr>
<tr><td></td><td>26</td><td>N/A</td><td>Add “14.0 Screw Hole Depth and Center Position”</td><td></td></tr>
<tr><td>0.2. 2004/7/21</td><td>7</td><td>
<table>
<tr><td>Typical White Luminance (ICFL=5.5mA)</td><td>[cd/m²]</td><td>200 (5-point average)</td></tr>
<tr><td>Typical Power Consumption (VDD line + VCFL line)</td><td>[Watt]</td><td>5.5W</td></tr>
</table>
</td><td>
<table>
<tr><td>Typical White Luminance (ICFL=6mA)</td><td>[cd/m²]</td><td>200 (5-point average)</td></tr>
<tr><td>Typical Power Consumption (VDD line + VCFL line)</td><td>[Watt]</td><td>5.9W @ all black pattern</td></tr>
</table>
</td><td>Modification of “section 2.1”</td></tr>
<tr><td></td><td>12</td><td>5.2 Signal Pin
<table>
<tr><th>Pin#</th><th>Signal Name</th><th>Pin#</th><th>Signal Name</th></tr>
<tr><td>1</td><td>GND</td><td>2</td><td>VDD</td></tr>
<tr><td>3</td><td>VDD</td><td>4</td><td>Reserved</td></tr>
<tr><td>5</td><td>Reserved</td><td>6</td><td>Reserved</td></tr>
<tr><td>7</td><td>Reserved</td><td>8</td><td>RoIN0-</td></tr>
<tr><td>9</td><td>RoIN0+</td><td>10</td><td>GND</td></tr>
<tr><td>11</td><td>RoIN1-</td><td>12</td><td>RoIN1+</td></tr>
<tr><td>13</td><td>GND</td><td>14</td><td>RoIN2-</td></tr>
<tr><td>15</td><td>RoIN2+</td><td>16</td><td>GND</td></tr>
<tr><td>17</td><td>RoCLKIN-</td><td>18</td><td>RoCLKIN+</td></tr>
<tr><td>19</td><td>GND</td><td>20</td><td>ReIN0-</td></tr>
<tr><td>21</td><td>ReIN0+</td><td>22</td><td>GND</td></tr>
<tr><td>23</td><td>ReIN1-</td><td>24</td><td>ReIN1+</td></tr>
<tr><td>25</td><td>GND</td><td>26</td><td>ReIN2-</td></tr>
<tr><td>27</td><td>ReIN2+</td><td>28</td><td>GND</td></tr>
<tr><td>29</td><td>ReCLKIN-</td><td>30</td><td>ReCLKIN+</td></tr>
</table>
</td><td>5.2 Signal Pin
<table>
<tr><th>Pin#</th><th>Signal Name</th><th>Pin#</th><th>Signal Name</th></tr>
<tr><td>1</td><td>GND</td><td>2</td><td>VDD</td></tr>
<tr><td>3</td><td>VDD</td><td>4</td><td>VEDID</td></tr>
<tr><td>5</td><td>Reserved</td><td>6</td><td>CLKEDID</td></tr>
<tr><td>7</td><td>DATAEDID</td><td>8</td><td>RoIN0-</td></tr>
<tr><td>9</td><td>RoIN0+</td><td>10</td><td>GND</td></tr>
<tr><td>11</td><td>RoIN1-</td><td>12</td><td>RoIN1+</td></tr>
<tr><td>13</td><td>GND</td><td>14</td><td>RoIN2-</td></tr>
<tr><td>15</td><td>RoIN2+</td><td>16</td><td>GND</td></tr>
<tr><td>17</td><td>RoCLKIN-</td><td>18</td><td>RoCLKIN+</td></tr>
<tr><td>19</td><td>GND</td><td>20</td><td>ReIN0-</td></tr>
<tr><td>21</td><td>ReIN0+</td><td>22</td><td>GND</td></tr>
<tr><td>23</td><td>ReIN1-</td><td>24</td><td>ReIN1+</td></tr>
<tr><td>25</td><td>GND</td><td>26</td><td>ReIN2-</td></tr>
<tr><td>27</td><td>ReIN2+</td><td>28</td><td>GND</td></tr>
<tr><td>29</td><td>ReCLKIN-</td><td>30</td><td>ReCLKIN+</td></tr>
</table>
</td><td>Modification of “section 5.2”: “Pin#4,#6 and #7”</td></tr>
<tr><td></td><td>13</td><td>5.3 Signal Description
The module uses a LVDS receiver. LVDS is a differential signal technology for LCD interface and high-speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.
<table>
<tr><th>Signal Name</th><th>Description</th></tr>
<tr><td>RoIN0-, RoIN0+</td><td>LVDS differential Odd data input(Red0-Red5, Green0)</td></tr>
<tr><td>RoIN1-, RoIN1+</td><td>LVDS differential Odd data input(Green1-Green5, Blue0-Blue1)</td></tr>
<tr><td>RoIN2-, RoIN2+</td><td>LVDS differential Odd data input(Blue2-Blue5, Hsync, Vsync, DSPTMG)</td></tr>
<tr><td>RoCLKIN-, RoCLKIN0+</td><td>LVDS Odd differential clock input</td></tr>
<tr><td>ReIN0-, ReIN0+</td><td>LVDS differential Even data input(Red0-Red5, Green0)</td></tr>
<tr><td>ReIN1-, ReIN1+</td><td>LVDS differential Even data input(Green1-Green5, Blue0-Blue1)</td></tr>
<tr><td>ReIN2-, ReIN2+</td><td>LVDS differential Even data input(Only Blue2-Blue5)</td></tr>
<tr><td>ReCLKIN-, ReCLKIN0+</td><td>LVDS Even differential clock input</td></tr>
<tr><td>VDD</td><td>+3.3V Power Supply</td></tr>
<tr><td>GND</td><td>Ground</td></tr>
</table>
Note: Input signals shall be low or Hi-Z state when VDD is off.
Internal circuit of LVDS inputs are as following.</td><td>5.3 Signal Description
The module uses a LVDS receiver. LVDS is a differential signal technology for LCD interface and high-speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.
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<tr><td>RoIN0-, RoIN0+</td><td>LVDS differential Odd data input(Red0-Red5, Green0)</td></tr>
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<tr><td>RoIN2-, RoIN2+</td><td>LVDS differential Odd data input(Blue2-Blue5, Hsync, Vsync, DSPTMG)</td></tr>
<tr><td>RoCLKIN-, RoCLKIN0+</td><td>LVDS Odd differential clock input</td></tr>
<tr><td>ReIN0-, ReIN0+</td><td>LVDS differential Even data input(Red0-Red5, Green0)</td></tr>
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<tr><td>ReCLKIN-, ReCLKIN0+</td><td>LVDS Even differential clock input</td></tr>
<tr><td>VDD</td><td>+3.3V Power Supply</td></tr>
<tr><td>GND</td><td>Ground</td></tr>
<tr><td>VEDID</td><td>DDC 3.3V Power</td></tr>
<tr><td>CLKEDID</td><td>DDC Clock</td></tr>
<tr><td>DATAEDID</td><td>DDC Data</td></tr>
</table>
Note: Input signals shall be low or Hi-Z state when VDD is off.
Internal circuit of LVDS inputs are as following.</td><td>Modification of “section 5.3”: “Add VEDID, CLKEDID and DATAEDID”</td></tr>
<tr><td></td><td>17</td><td>7.0 Parameter guideline for CFL Inverter
<table>
<tr><th>Parameter</th><th>Min</th><th>DP-1</th><th>Max</th><th>Units</th><th>Condition</th></tr>
<tr><td>White Luminance 5 points average</td><td>170</td><td>200</td><td>—</td><td>[cd/m²]</td><td>(Ta=25℃)</td></tr>
<tr><td>CCFL current(ICFL)</td><td>3.0</td><td>6</td><td>7.0</td><td>[mA] rms</td><td>(Ta=25℃) Note 2</td></tr>
<tr><td>CCFL Frequency(FCFL)</td><td>50</td><td>60</td><td>70</td><td>[KHz]</td><td>(Ta=25℃) Note 3</td></tr>
<tr><td>CCFL Ignition Voltage(Vs)</td><td></td><td>—</td><td>1,150</td><td>[Volt] rms</td><td>(Ta= 0℃) Note 4</td></tr>
<tr><td>CCFL Voltage (Reference) (VCFL)</td><td>—</td><td>700</td><td>—</td><td>[Volt] rms</td><td>(Ta=25℃) Note 5</td></tr>
<tr><td>CCFL Power consumption (PCFL)</td><td>—</td><td>3.9</td><td>—</td><td>[Watt]</td><td>(Ta=25℃) Note 5</td></tr>
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<tr><td>CCFL Frequency(FCFL)</td><td>50</td><td>55</td><td>60</td><td>[KHz]</td><td>(Ta=25℃) Note 3</td></tr>
<tr><td>CCFL Ignition Voltage(Vs)</td><td>1,560</td><td>1,600</td><td>1,800</td><td>[Volt] rms</td><td>(Ta= 0℃) Note 4</td></tr>
<tr><td>CCFL Voltage (Reference) (VCFL)</td><td>—</td><td>650</td><td>—</td><td>[Volt] rms</td><td>(Ta=25℃) Note 5</td></tr>
<tr><td>CCFL Power consumption (PCFL)</td><td>—</td><td>3.9</td><td>—</td><td>[Watt]</td><td>(Ta=25℃) Note 5</td></tr>
</table>
</td><td>Modification of “section 7.0”</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
</table>

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1.0 Handing Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(2.11, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit(2.4, IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

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2.0 General Description

This specification applies to the 15.0 inch Color TFT/LCD Module B150PG03 V0.

This module is designed for a display unit of notebook style personal computer.

The screen format is intended to support the SXGA+ (1400(H) x 1050(V)) screen and 262k colors (RGB 6-bits data driver).

All input signals are LVDS interface compatible.

This module does not contain an inverter card for backlight.

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2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	381
Active Area	[mm]	304.5 X 228.375
Pixels H x V		1400(x3) x 1050
Pixel Pitch	[mm]	0.2175X0.2175
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance (ICFL=6mA)	[cd/m^2]	200 (5-point average)
Contrast Ratio		300:1 (typ.)
Optical Rise Time/Fall Time	[msec]	10/15
Nominal Input Voltage VDD	[Volt]	+3.3 (typ.)
Typical Power Consumption (VDD line + VCFL line)	[Watt]	5.9W @ all black pattern
Weight	[Grams]	575 (typ.)
Physical Size	[mm]	317.3 x 242.0 x 6.5(max)
Electrical Interface		2 channel LVDS
Support Color		Native 262K colors (RGB 6-bit data driver)
Temperature Range Operating Storage (Shipping)	 [^{o}C] [^{o}C]	 0 to +50 -20 to +60

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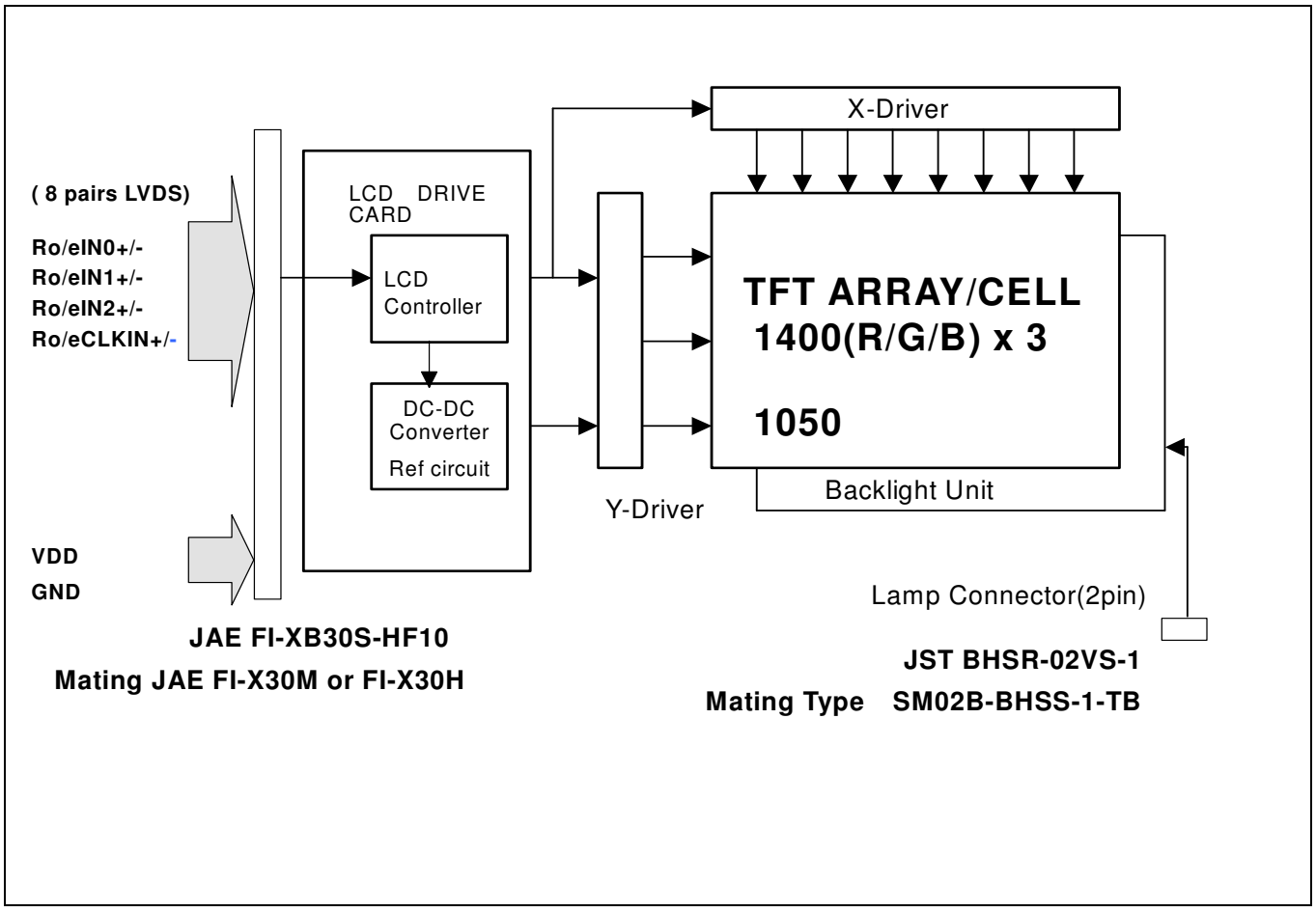
2.2 Functional Block Diagram

The following diagram shows the functional block of the 15.0 inches Color TFT/LCD Module:



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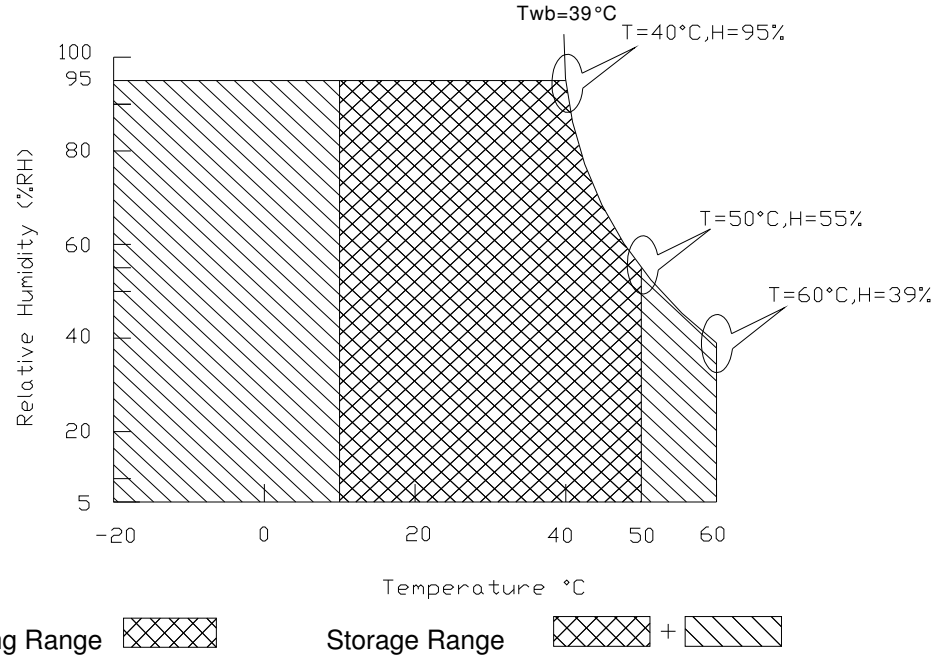
3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	[Volt]	
Input Voltage of Signal	Vin	-0.3	VDD+0.3	[Volt]	
CCFL Current	ICFL	-	7	[mA] rms	
CCFL Ignition Voltage	Vs	-	1200	Vrms	
Operating Temperature	TOP	0	+50	[°C]	Note 1
Operating Humidity	HOP	8	95	[%RH]	Note 1
Storage Temperature	TST	-20	+60	[°C]	Note 1
Storage Humidity	HST	5	95	[%RH]	Note 1
Vibration			1.5 10-500 (random)	G Hz	2hr/axis, X,Y,Z
Shock			220 , 2	G ms	Half sine wave

Note 1 : Maximum Wet-Bulb should be 39℃ and No condensation.

Wet bulb temperature chart



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4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25℃ condition:

Item	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	40 40	- -	- -	
CR: Contrast Ratio	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	10 30	- -	- -	
Uniformity		5 Points			1.2	
Uniformity		13 Points			1.5	
Contrast ratio			250	300	-	
Response Time	[msec]	Rising	-	10	15	
	[msec]	Falling	-	15	20	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.538	0.568	0.598	
		Red y	0.312	0.342	0.372	
		Green x	0.276	0.306	0.336	
		Green y	0.529	0.559	0.589	
		Blue x	0.123	0.153	0.183	
		Blue y	0.111	0.141	0.171	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	
White Luminance CCFL 6.0mA	[cd/m^2]	5 points average	170	200	-	
Cross talk	%	θ=0°, Φ=0° Viewing Normal Angle			4.0	

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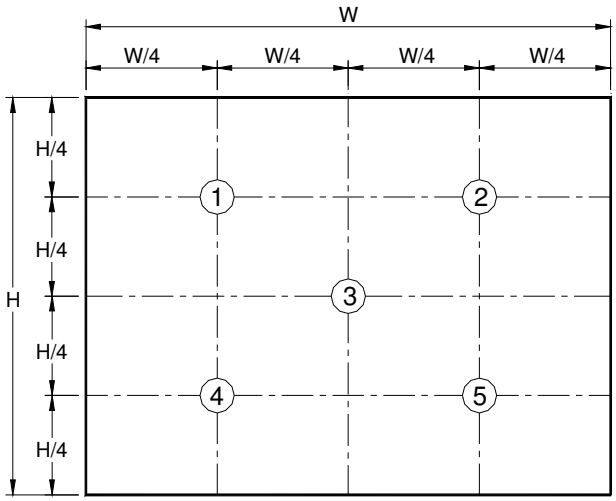
Note 1: 5 points position (Display area : 304.5mm x 228.375mm)



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5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XB30S-HF10
Mating Housing/Part Number	FI-X30M, FI-X30H
Mating Contact/Part Number	FI-C3-A1

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

5.2 Signal Pin

Pin#	Signal Name	Pin#	Signal Name
1	GND	2	VDD
3	VDD	4	V_{EDID}
5	Reserved	6	CLK_{EDID}
7	$DATA_{EDID}$	8	RoIN0-
9	RoIN0+	10	GND
11	RoIN1-	12	RoIN1+
13	GND	14	RoIN2-
15	RoIN2+	16	GND
17	RoCLKIN-	18	RoCLKIN+
19	GND	20	ReIN0-
21	ReIN0+	22	GND
23	ReIN1-	24	ReIN1+
25	GND	26	ReIN2-
27	ReIN2+	28	GND
29	ReCLKIN-	30	ReCLKIN+

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5.3 Signal Description

The module uses a LVDS receiver. LVDS is a differential signal technology for LCD interface and high-speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.

Signal Name	Description
RoIN0-, RoIN0+	LVDS differential Odd data input(Red0-Red5, Green0)
RoIN1-, RoIN1+	LVDS differential Odd data input(Green1-Green5, Blue0-Blue1)
RoIN2-, RoIN2+	LVDS differential Odd data input(Blue2-Blue5, Hsync, Vsync, DSPTMG)
RoCLKIN-, RoCLKIN0+	LVDS Odd differential clock input
ReIN0-, ReIN0+	LVDS differential Even data input(Red0-Red5, Green0)
ReIN1-, ReIN1+	LVDS differential Even data input(Green1-Green5, Blue0-Blue1)
ReIN2-, ReIN2+	LVDS differential Even data input(Only Blue2-Blue5)
ReCLKIN-, ReCLKIN0+	LVDS Even differential clock input
VDD	+3.3V Power Supply
GND	Ground
V_{EDID}	DDC 3.3V Power
CLK_{EDID}	DDC Clock
$DATA_{EDID}$	DDC Data

Note: Input signals shall be low or Hi-Z state when VDD is off.

Internal circuit of LVDS inputs are as following.

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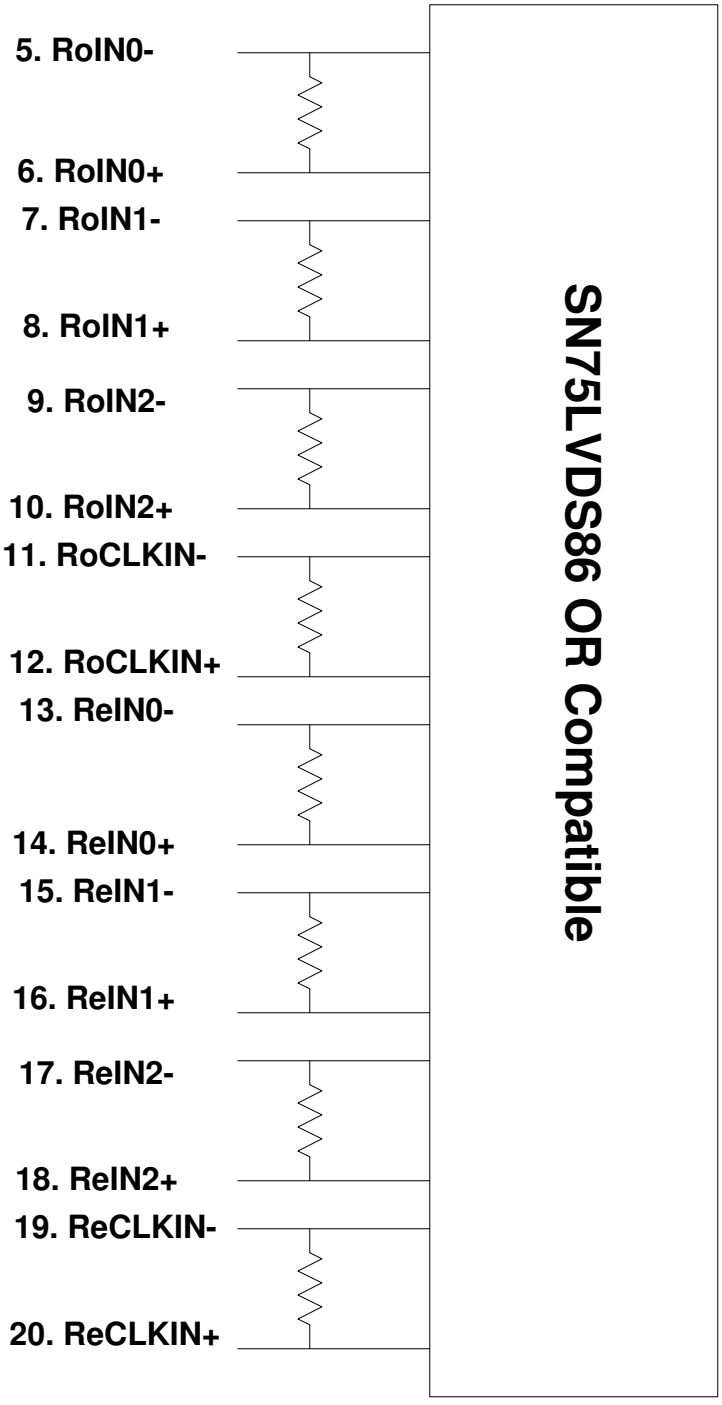
Signal Input



The module uses a 100ohm resistor between positive and negative data lines of each receiver input

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Signal Name	Description	
+RED5 +RED4 +RED3 +RED2 +RED1 +RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK	Data Clock	The typical frequency is 54.0 MHZ.. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	Display Timing	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync	The signal is synchronized to -DTCLK .
HSYNC	Horizontal Sync	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

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5.4 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

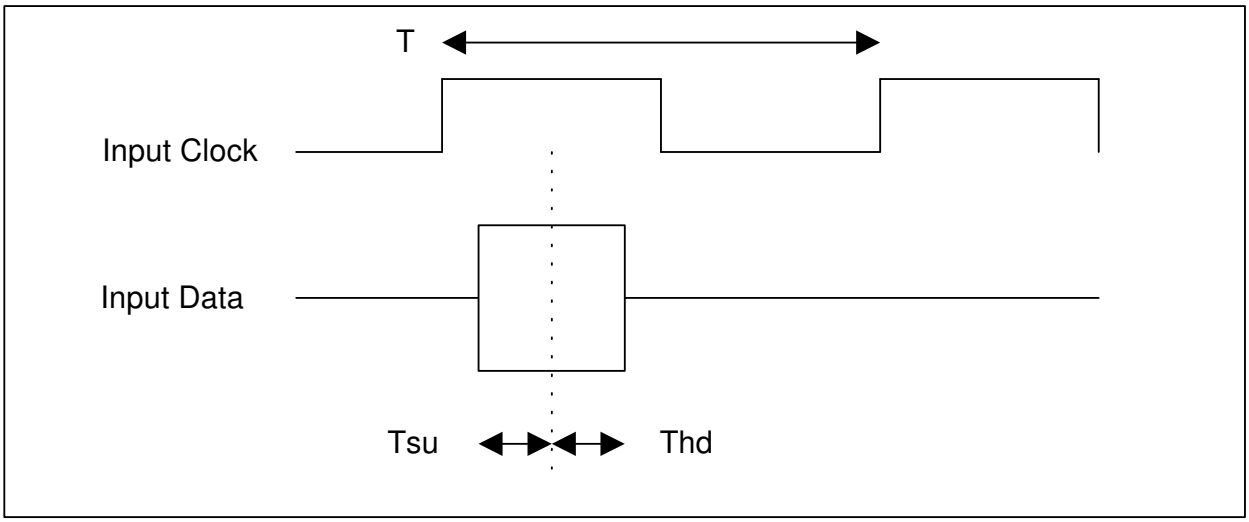
It is recommended to refer the specifications of SN75LVDS86DGG(Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Voltage(Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Voltage(Vcm=+1.2V)	-100		[mV]

LVDS Macro AC characteristics are as follows:

	Min.	Max.
Clock Frequency (T)	25MHz	115MHz
Data Setup Time (Tsu)	600ps	
Data Hold Time (Thd)	600ps	



5.5 Signal for Lamp connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

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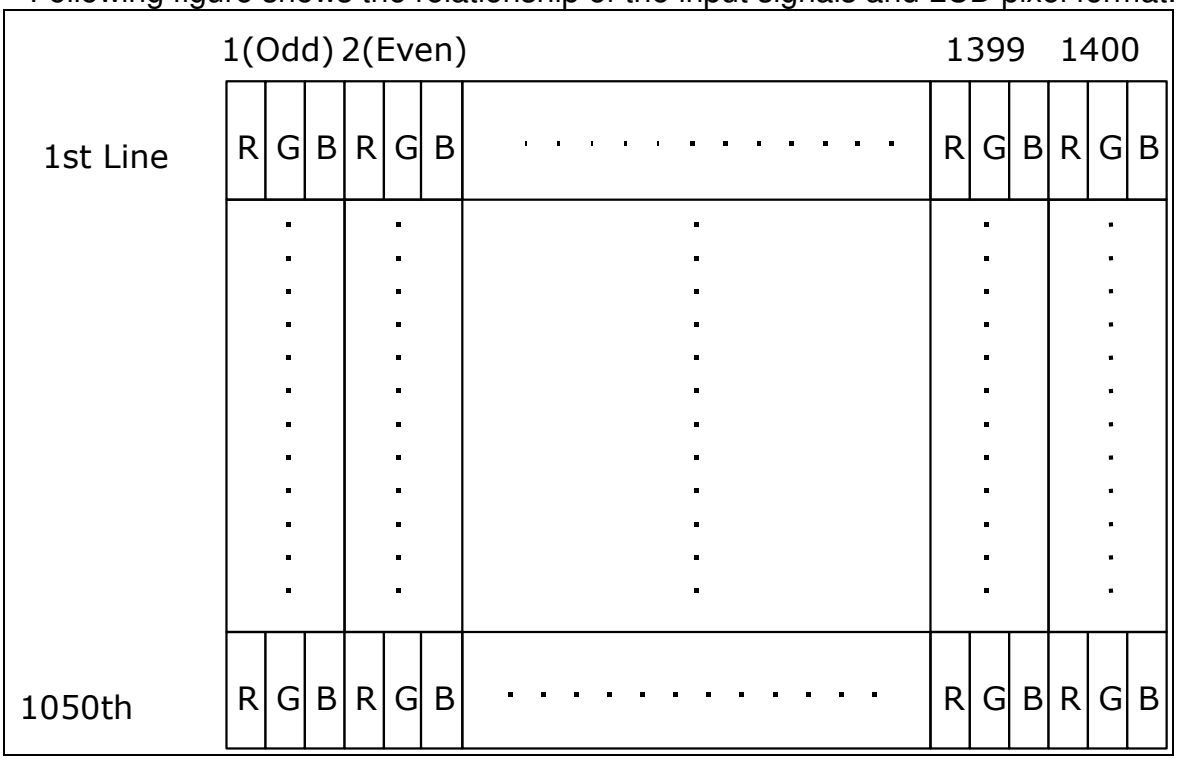
6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



7.0 Parameter guideline for CFL Inverter

Parameter	Min	DP-1	Max	Units	Condition
White Luminance 5 points average	170	200	—	[cd/m^2]	(Ta=25℃)
CCFL current(ICFL)	3.0	6.0	7.0	[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(FCFL)	50	55	60	[KHz]	(Ta=25℃) Note 3
CCFL Ignition Voltage(Vs)	1,560	1,600	1,800	[Volt] rms	(Ta= 0℃) Note 4
CCFL Voltage (Reference) (VCFL)	—	650	—	[Volt] rms	(Ta=25℃) Note 5
CCFL Power consumption (PCFL)	—	3.9	—	[Watt]	(Ta=25℃) Note 5

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Note 1: DP-1 is AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the ADT Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has “Duty Dimming”, if ICFL is less than 4mA.

Note 3: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: CFL inverter should be able to give out a power that has a generating capacity of over 1,400 voltages. Lamp units need 1,400 voltages minimum for ignition.

Note 5: Calculator value for reference (ICFL×VCFL=PCFL)

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8.0 Interface Timings

Basically, interface timings should match the VESA 1400x1050 /60Hz (VG901101) manufacturing guideline timing.

8.1 Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
fdck	DTCLK Frequency		54.00		[MHz]
tck	DTCLK cycle time		18.5		[nsec]
tx	X total time	740	844	1000	[tck]
tacx	X active time	700	700		[tck]
tbkx	X blank time		144		[tck]
Hsync	H frequency		63.98		[KHz]
Hsw	H-Sync width	A	56		[tck]
Hbp	H back porch	B	64		[tck]
Hfp	H front porch	C	24		[tck]
ty	Y total time	1054	1066	2048	[tx]
tacy	Y active time		1050		[tx]
Vsync	Frame rate	(55)	60	61	[Hz]
Vw	V-sync Width	1	3	8	[tx]
Vfp	V-sync front porch	1	1		[tx]
Vbp	V-sync back porch	7	12	63	[tx]

Note: A+B+C=39

Note: Hsw(H-sync width) + Hbp(H-sync back porch) should be less than 515 tck.

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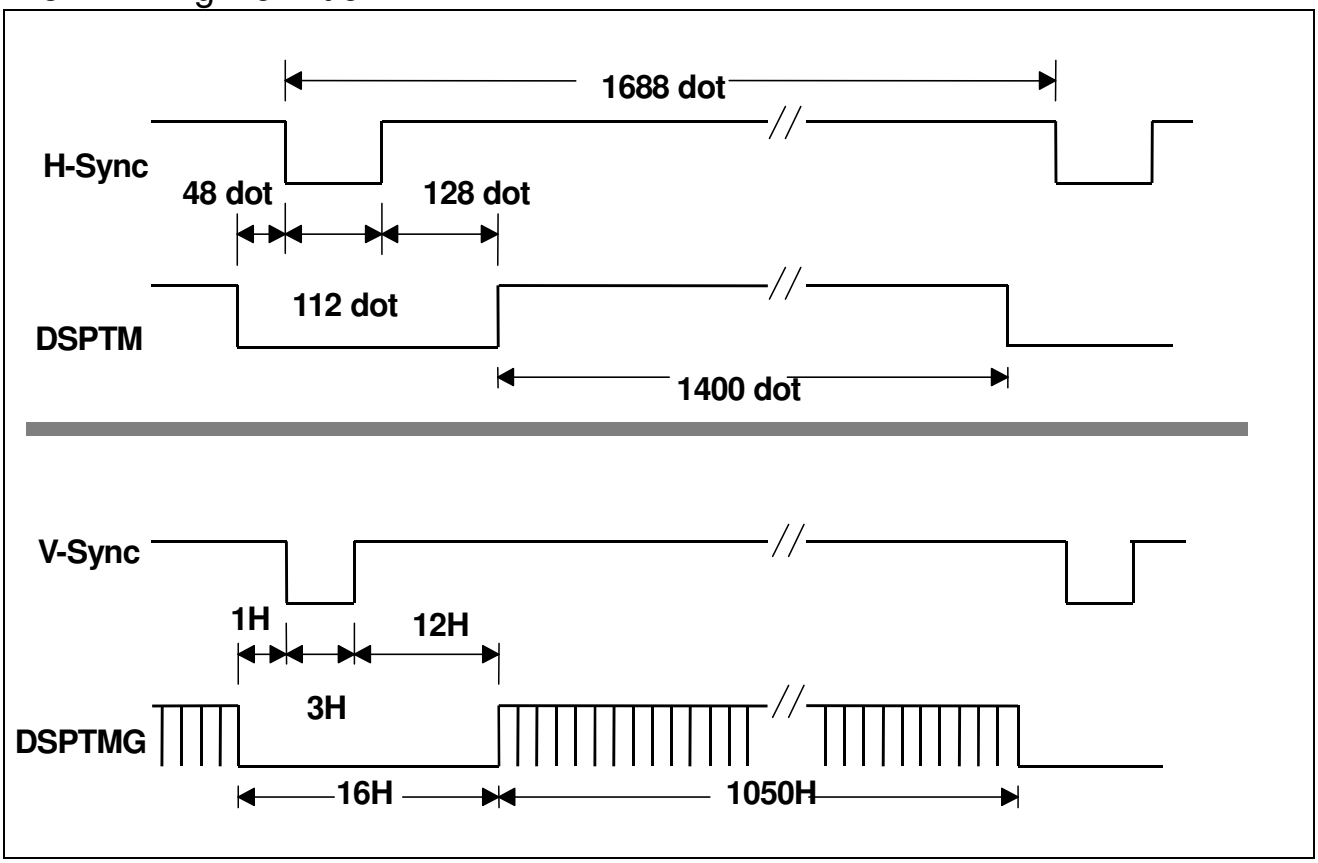
8.2 Timing Definition



9.0 Power Consumption

Input power specifications are as followed;

Symbol	Parameter	Min	Typ	Max	Unit	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		1.8		[Watt]	All Black Pattern
PDD Max	VDD Power max			1.93	[Watt]	Max Pattern (Note)
IDD	IDD Current		550		mA	All Black Pattern
IDD Max	IDD Current max			585	mA	Max Pattern (Note)
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mV] p-p	

Note: VDD=3.3V

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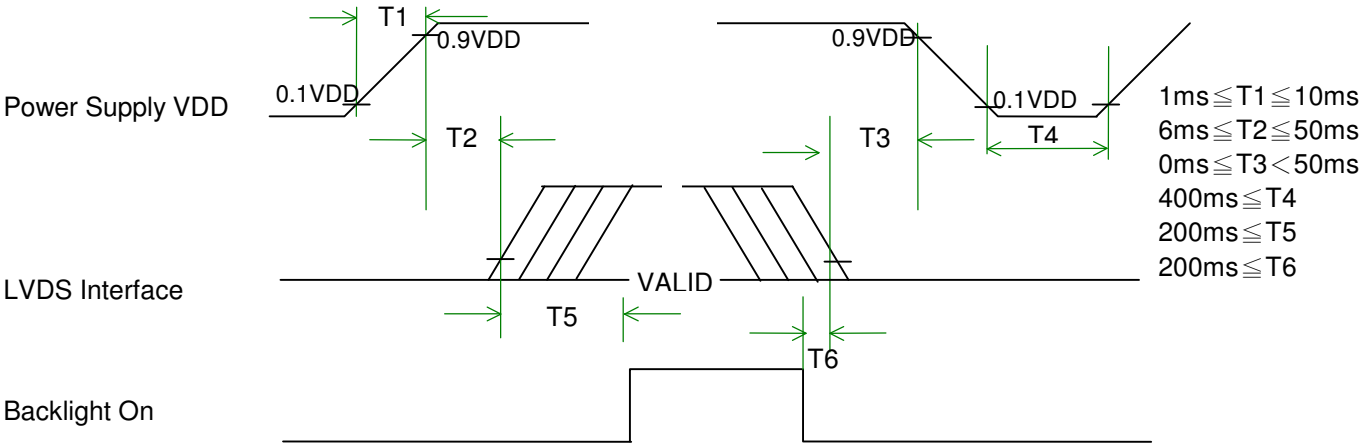
10. Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.

Sequence of Power-on/off and signal-on/off



Apply the lamp voltage within the LCD operating range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal.

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11.0 Reliability / Safety Requirement

11.1 Reliability Test Conditions

Items	**Required Condition**
Temperature Humidity Bias	40℃/90%,300Hr
High Temperature Operation	50℃/Dry,300Hr
Low Temperature Operation	0℃,500Hr
Continuous Life	25℃,2000 hours
On/Off Test	ON/30 sec. OFF/30sec., 14,000 cycles
Hot Storage	60℃/40% RH ,240 hours
Cold Storage	-20℃/50% RH ,240 hours
Thermal Shock Test	-20℃/30 min ,60℃/30 min 100cycles
Hot Start Test	50℃/1 Hr min. power on/off per 5 minutes, 5 times
Cold Start Test	0℃/1 Hr min. power on/off per 5 minutes, 5 times
Shock Test (Non-Operating)	220G, 2ms, Half-sine wave
Vibration Test (Non-Operating)	Sinusoidal vibration, 1.5G zero-to-peak, 10 to 500 Hz, 0.5 octave/minute; 0.5hr in each of three mutually perpendicular axes.
ESD	Contact : operation ±8KV / non-operation ± 10KV Air : operation ±15KV / non-operation ± 20KV
Altitude Test	10000 ft / operation / 8Hr 30000ft / non-operation / 24r
Maximum Side Mount Torque	2.5kgf.cm .

11.2 Safety

UL1950

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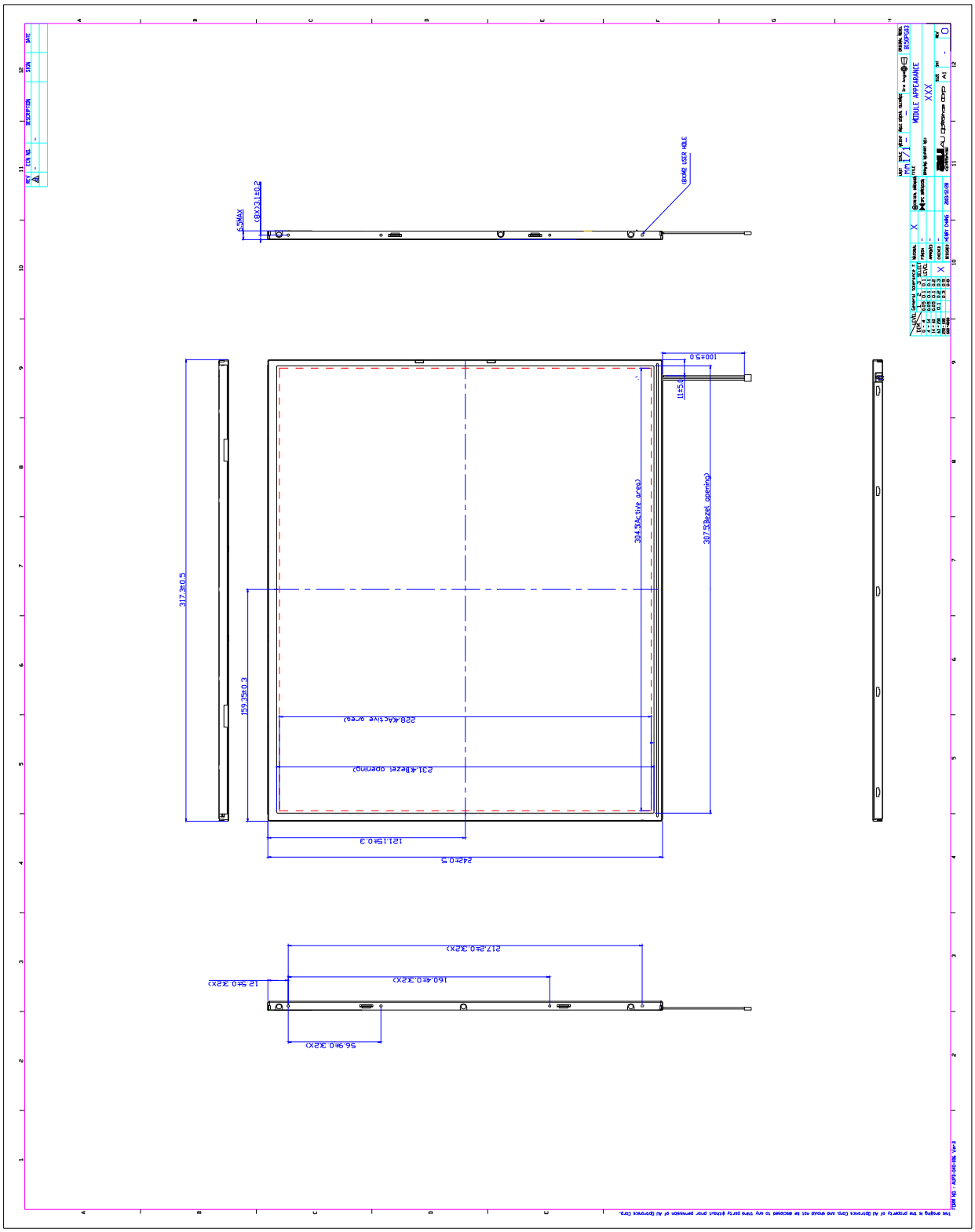
12.0 Mechanical Characteristics



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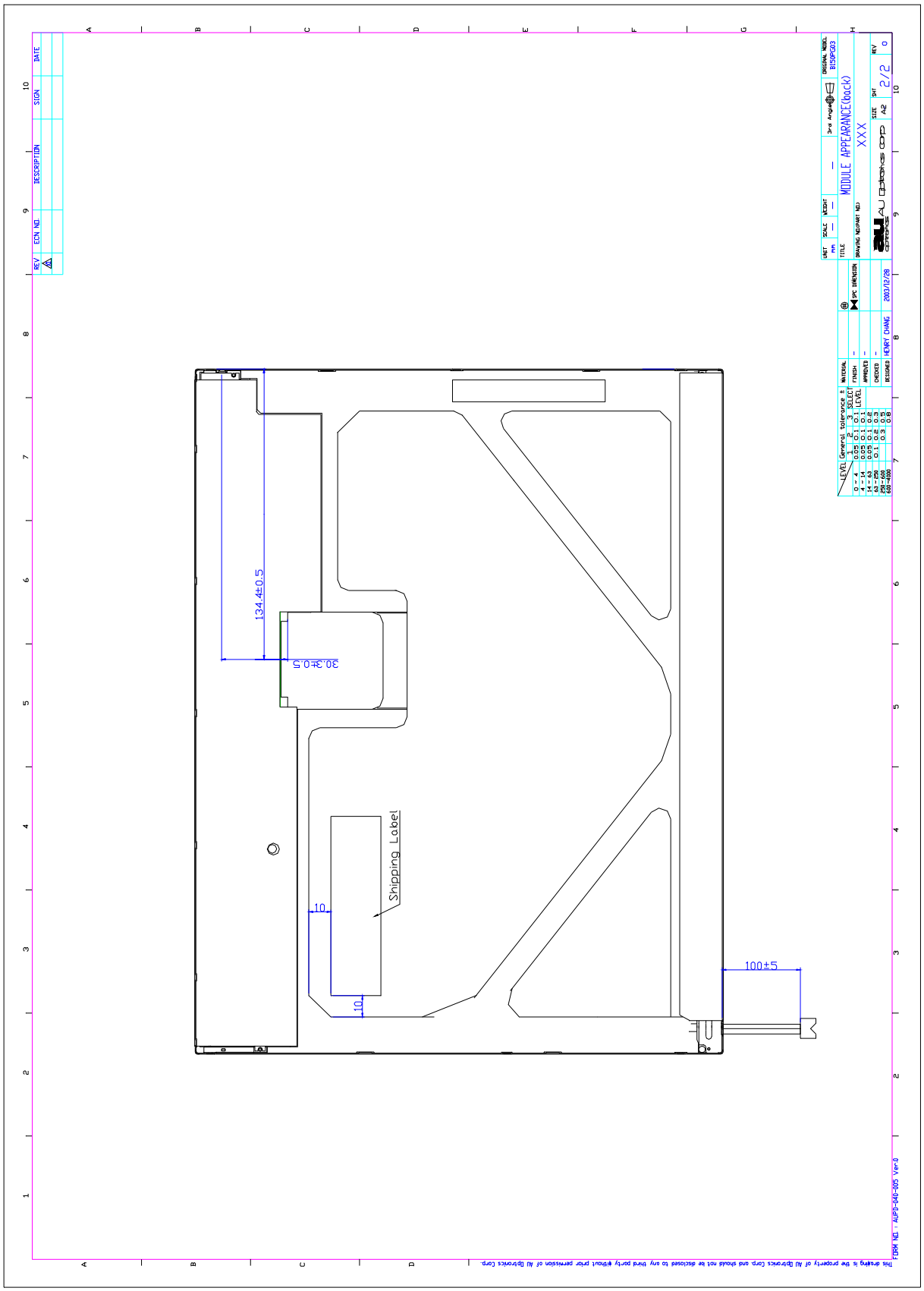

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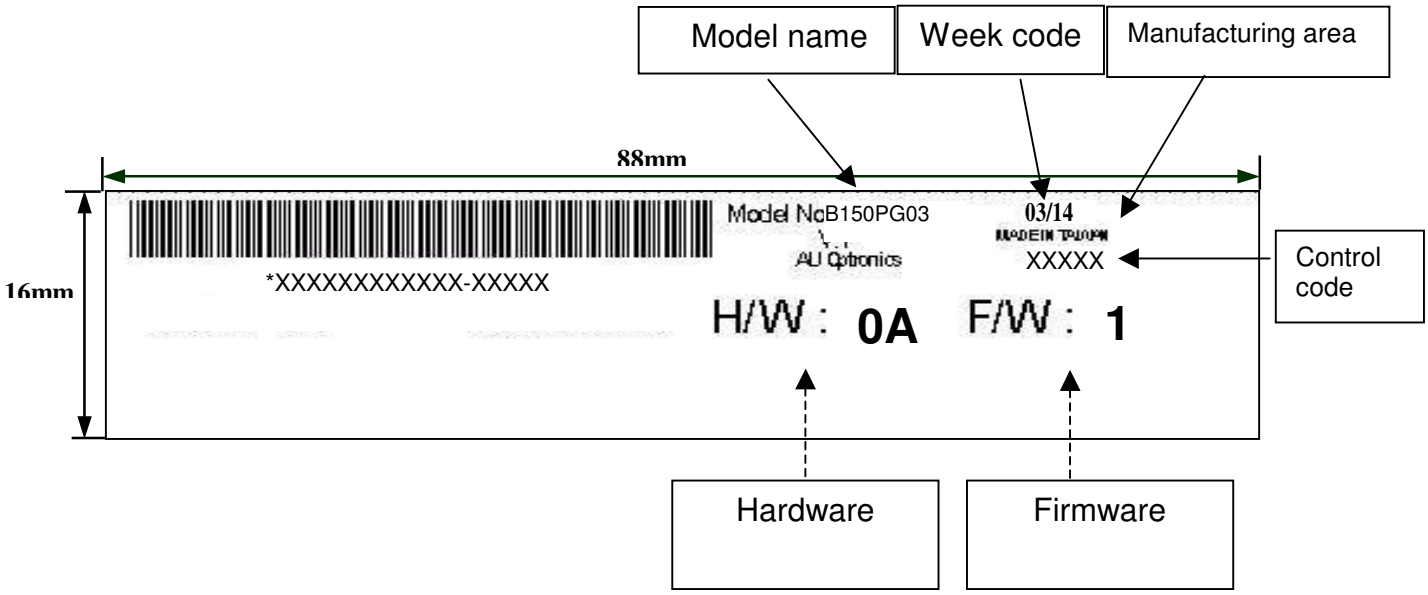
13.0 Shipping Label Format



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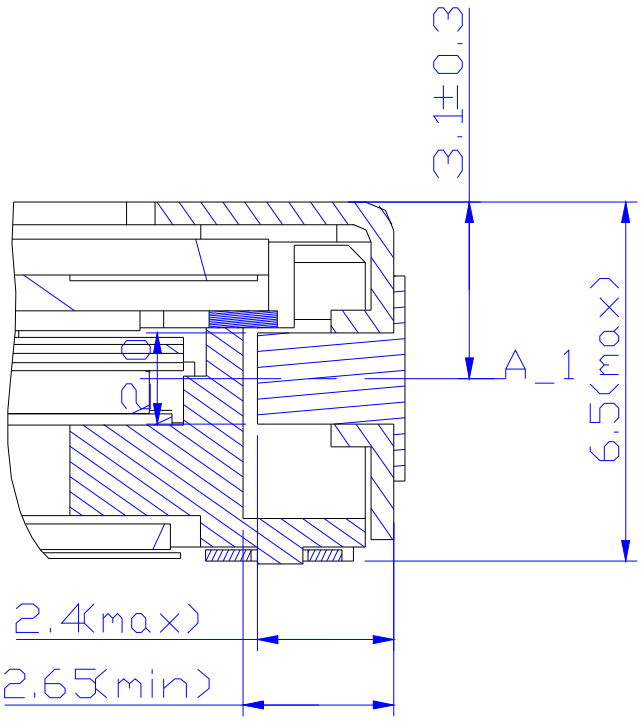
14.0 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface =2.65 mm (See drawing)
Screw hole center location, from front surface = 3.1 ± 0.3mm (See drawing)
Screw maximum length = 2.4 mm (See drawing)
Screw Torque: Maximum2.0 kgf-cm



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