

()	Preliminary Specifications
(V) Final Specifications

Module	13.3" WXGA Color TFT-LCD with LED Backlight design			
Model Name	B133EW05 V0 (H/W:0A)			
Note (🗭)	LED Backlight with driving circuit design			

Customer	Date	Approved by	Date
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Note: This Specification is subject notice.	to change without	NBBU Marketi AU Optronics	



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Record of Revision

Version and Date		Page	Old description	New Description	Remark
0.1	2007/12/14	All	First Edition for Customer		
0.2	2007/12/24	27	11.1 Shipping Label Format	11.1 Shipping Label Format	
0.3	2008/01/16	18	Pin11: 5V , Pin12: GND	Pin11: GND , Pin12: NC	
		29-32	EDID check sum 34	EDID check sum 7E	
0.4	2008/02/01	5	Physical Size: T 3.05	Physical Size: T 3.35	
		26	Label position on rear frame	Label position on BLU sheet	
		28	TBD	Add Carton and shipping Packing	
0.5	2008/03/25	5	ILED=19mA	ILED=20mA	
0.6	2008/6/12	29	EDID check sum 7E	EDID check sum CF	
0.7	2008/7/7	29	EDID check sum CF	EDID check sum 63	
0.8	2008/7/7	26	Label position on rear frame	Label position on BLU sheet	
0.9	2008/7/7	27	Non Green Label Format	Green Label Format	
0.10	2008/7/16	6	White Luminance min 240	White Luminance min 250	
0.11	2008/7/16	6	Contrast Ratio typ 600	Contrast Ratio typ 550	
0.12	2008/7/16	6	By 0.090 / 0.120 / 0.150	By 0.120 / 0.150 / 0.180	
0.13	2008/7/16	6	Viewing Angle(Vertical) (Upper) 15 / 15(min/typ) (Lower) 30 / 35	Viewing Angle(Vertical) (Upper) 15 / 20(min/typ) (Lower) 30 / 40	



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1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11)After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



2. General Description

B133EW05 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B133EW05 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 $^{\circ}\mathrm{C}$ condition:

Items	Unit		Specifications				
Screen Diagonal	[mm]	337.8 (13.3W")					
Active Area	[mm]	286.08 (H) X 178.8 (V)					
Pixels H x V		1280x3(RG	iB) x 800				
Pixel Pitch	[mm]	0.2235 x 0.	2235				
Pixel Format		R.G.B. Ver	tical Stripe				
Display Mode		Normally W	/hite				
White Luminance (ILED=20mA) Note: ILED is lamp current	[cd/m ²]	300 typ.(5 points average) 240 min.(5 points average) (Note1)					
Luminance Uniformity		1.25 max. (5 points)				
Contrast Ratio		600 typ					
Response Time	[ms]	16 typ					
Nominal Input Voltage VDD	[Volt]	+3.3 typ.					
Power Consumption	[Watt]	4.85 max.					
Weight	[Grams]	245 max.					
Physical Size without inverter,	[mm]		L	W	Т		
bracket.		Max	296.5	203.0	3.35		
		Typical			-		
		Min -					
Electrical Interface	one channel LVDS						
Surface Treatment		Anti-Glare, Hardness 3H,					
Support Color		262K colors (RGB 6-bit)					



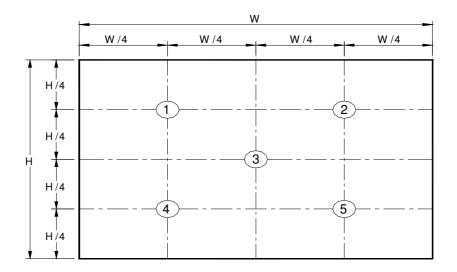
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -25 to +65
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

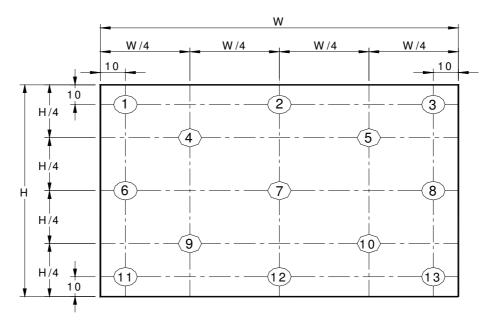
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Unit	Conditions	Min.	Тур.	Max.	Note
White Luminance ILED=20mA	[cd/m ²]	5 points average	250	300	-	1, 4, 5.
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	40 40	45 45		0
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	15 30	20 40		8
Luminance Uniformity		5 Points	-	-	1.25	1
Luminance Uniformity		13 Points	-	-	1.6	2
CR: Contrast Ratio			400	550	-	6
Cross talk	%				4	7
	[msec]	Rising	-	4	8	
Response Time	[msec]	Falling	-	12	17	8
	[msec]	Rising + Falling	-	16	25	
		Red x	0.570	0.600	0.630	
		Red y	0.315	0.345	0.375	
		Green x	0.290	0.320	0.350	
Chromaticity of color Coordinates		Green y	0.525	0.555	0.585	
(CIE 1931)		Blue x	0.120	0.150	0.180	2,8
, ,		Blue y	0.120	0.150	0.180	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	
NTSC	%	CIE 1931	-	45	-	

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



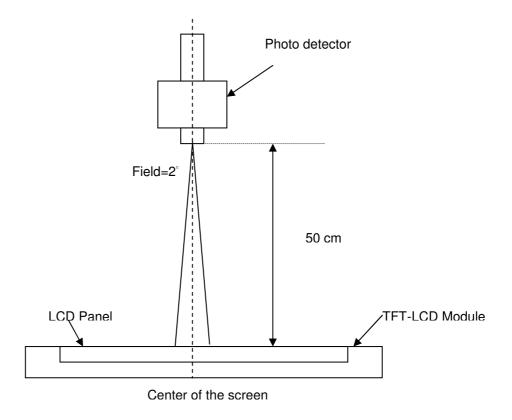
Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

2		Maximum Brightness of five points
δ _{W5}	=	Minimum Brightness of five points
2		Maximum Brightness of thirteen points
δ w13	=	Minimum Brightness of thirteen points



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The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5: Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points \cdot $Y_L = [L (1) + L (2) + L (3) + L (4) + L (5)] / 5 L (x) is corresponding to the luminance of the point X at Figure in Note (1).$

Note 6: Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

Note 7: Definition of Cross Talk (CT)

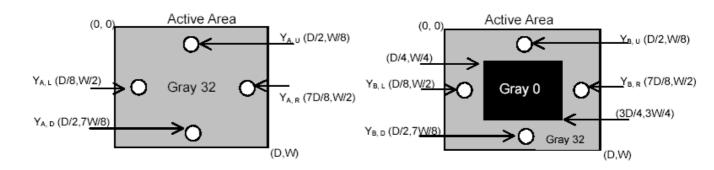


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Where

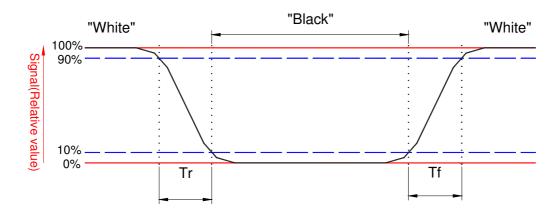
Y_A = Luminance of measured location without gray level 0 pattern (cd/m₂)

 Y_B = Luminance of measured location with gray level 0 pattern (cd/m₂)



Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.

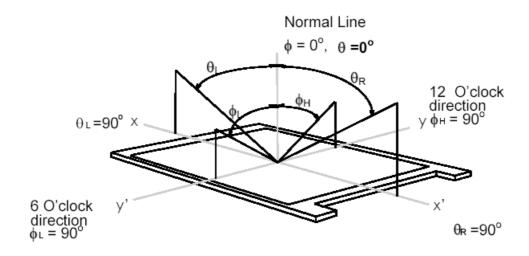




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Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio \geq 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.

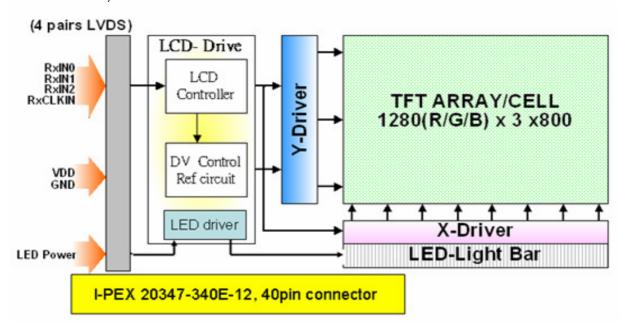




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3. Functional Block Diagram

The following diagram shows the functional block of the 13.3 inches wide Color TFT/LCD 40 Pin (One CH/connector Module)





4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

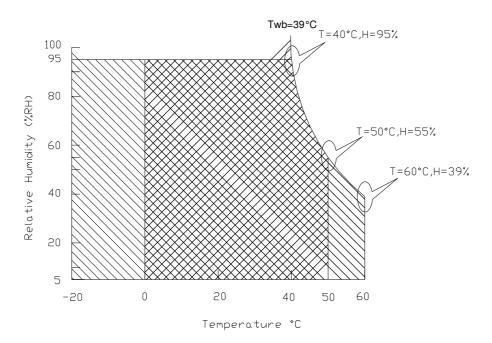
Item	Symbol	Min	Max	Unit	Conditions			
Operating Temperature	TOP	0	+50	[°C]	Note 4			
Operation Humidity	HOP	5	95	[%RH]	Note 4			
Storage Temperature	TST	-20	+60	[°C]	Note 4			
Storage Humidity	HST	5	95	[%RH]	Note 4			

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range

Storage Range

+

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

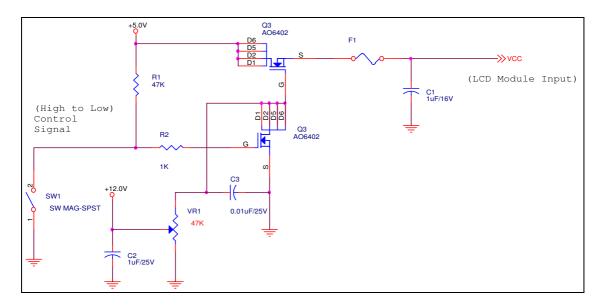
The power specification are measured under 25°C and frame frenquency under 60Hz

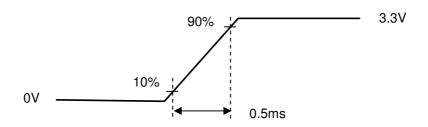
Symble	Parameter	Min	Тур	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	0.75	0.85	[Watt]	Note 1/2
IDD	IDD Current	-	230	290	[mA]	Note 1/2
IRush	Inrush Current	-	0.7	1.5	[A]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1: Maximum Measurement Condition: Black Pattern

Note 2: Typical Measurement Condition: Mosaic Pattern

Note 3: Measure Condition







5.1.2 Signal Electrical Characteristics

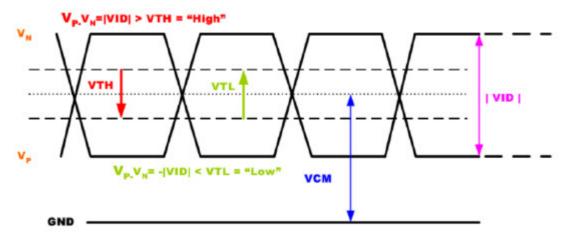
Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)	-	+100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
Vcm	Differential Input Common Mode Voltage	0.8	2.0	[V]

Note: LVDS Signal Waveform

Single-end Signal



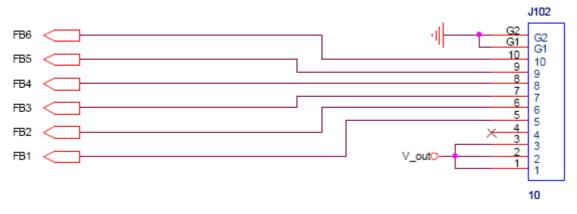


5.2 Backlight Unit

LED Parameter guideline for LED driving selection (Ref. Remark 1)

Parameter	Min	Тур	Maz	Units	Units
White Luminance 5 points average	240	300	-	[cd/m ²]	Ta=25 °C
LED current (ILED)	-	20	-	[mA]	Ta=25 °C
LED Power consumption	-	4.07	-	[Watt]	Ta=25 °C

Light bar PIN assignment:



PIN NO.	Pin assignment	Function
1	VOUT	LED Anode (Positive)
2	VOUT	LED Anode (Positive)
3	VOUT	LED Anode (Positive)
4	NC	NC
5	FB1	LED Cathode (Negative)
6	FB2	LED Cathode (Negative)
7	FB3	LED Cathode (Negative)
8	FB4	LED Cathode (Negative)
9	FB5	LED Cathode (Negative)
10	FB6	LED Cathode (Negative)



6. Signal Characteristic

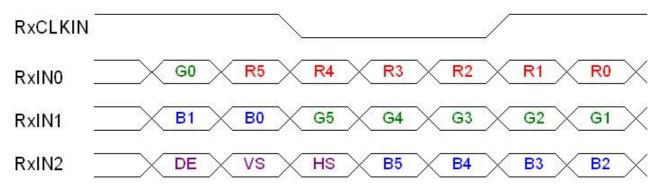
6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

	1						12	80)
1st Line	R G B	R G B		R	G	В	R	G	В
					•			•	
					•				
			•					•	
	•		•		•				
			•		•				
800th Line	R G B	R G B		R	G	В	R	G	В



6.2 The input data format



Signal Name	Description
VEEDID (3.3V)	+3.3V EDID Power
CLK EEDID	EDID Clock Input
DATA EEDID	EDID Data Input
RXIN0-, RXIN0+	LVDS differential data input(Red0-Red5, Green0)
RXIN1-, RXIN1+	LVDS differential data input(Green1-Green5, Blue0-Blue1)
RXIN2-, RXIN2+	LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DE)
RXCLKIN-, RXCLKIN+	LVDS differential clock input
VDD	+3.3V Power Supply
VSS	Ground

Note: Output signals from any system shall be low or High-impedance state when VDD is off.



6.3 Integration Interface and Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Pin Signal			Description
2 CONNTST Connector test 3 VDD Logic power 3.3V (Panel logic, BL logic) 4 VDD Logic power 3.3V (Panel logic, BL logic) 5 VDD Logic power 3.3V (Panel logic, BL logic) 6 VEDID EDID 3.3V power 7 TEST Panel Self Test 8 CLK EDID clock 9 DATA EDID data 10 VSS Ground 11 VSS Ground 11 VSS Ground 12 NC no connection 13 RINO- LVDS differential data input (R0-R5, G0) 14 RINO+ LVDS differential data input (R0-R5, G0) 15 VSS Ground 16 RIN1- LVDS differential data input (G1-G5, B0-B1) 17 RIN1+ LVDS differential data input (G1-G5, B0-B1) 18 VSS Ground 19 RIN2- LVDS differential data input (B2-B5,HS,VS, DE) 20 RIN2+ LVDS differential data input (B2-B5,HS,VS, DE) 21 VSS Ground 22 CLK- LVDS differential clock input 23 CLK+ LVDS differential clock input 24 VSS Ground 25 INV PWM PWM brightness control 26 VBL- LED power return 27 VBL- LED power return 29 VBL- LED power return 30 VBL- LED power return 31 NC no connection 32 VBL+ 7V - 20V LED power source 33 VBL+ 7V - 20V LED power source 34 VBL+ TV - 20V LED power source 35 VBL+ TV - 20V LED power source 36 VBL+ TV - 20V LED power source 37 CONNTST Connector test 38 SMB CLK SMBus Data			
3			
4 VDD Logic power 3.3V (Panel logic, BL logic) 5 VDD Logic power 3.3V (Panel logic, BL logic) 6 VEDID EDID 3.3V power 7 TEST Panel Self Test 8 CLK EDID clock 9 DATA EDID data 10 VSS Ground 11 VSS Ground 12 NC no connection 13 RIN0- - LVDS differential data input (R0-R5, G0) 14 RIN0+ + LVDS differential data input (G1-G5, B0-B1) 15 VSS Ground 16 RIN1- - LVDS differential data input (G1-G5, B0-B1) 17 RIN1+ + LVDS differential data input (B2-B5,HS,VS, DE) 20 RIN2- - LVDS differential data input (B2-B5,HS,VS, DE) 21 VSS Ground 22 CLK- + LVDS differential clock input 23 CLK- + LVDS differential clock input 24 VSS Ground 25 INV PWM			
5 VDD Logic power 3.3V (Panel logic, BL logic) 6 VEDID EDID 3.3V power 7 TEST Panel Self Test 8 CLK EDID clock 9 DATA EDID data 10 VSS Ground 11 VSS Ground 12 NC no connection 13 RIN0- - LVDS differential data input (R0-R5, G0) 14 RIN0+ + LVDS differential data input (R0-R5, G0) 15 VSS Ground 16 RIN1- - LVDS differential data input (G1-G5, B0-B1) 17 RIN1+ + LVDS differential data input (B2-B5,HS,VS, DE) 20 RIN2- - LVDS differential data input (B2-B5,HS,VS, DE) 21 VSS Ground 22 CLK- - LVDS differential clock input 23 CLK- - LVDS differential clock input 24 VSS Ground 25 INV_PWM PWM brightness control 26 VBL- LED power return <			0 1 0 7
6 VEDID EDID 3.3V power 7 TEST Panel Self Test 8 CLK EDID clock 9 DATA EDID data 10 VSS Ground 11 VSS Ground 12 NC no connection 13 RIN0- - LVDS differential data input (R0-R5, G0) 14 RIN0+ + LVDS differential data input (R0-R5, G0) 15 VSS Ground 16 RIN1- - LVDS differential data input (G1-G5, B0-B1) 17 RIN1+ + LVDS differential data input (G1-G5, B0-B1) 18 VSS Ground 19 RIN2- - LVDS differential data input (B2-B5,HS,VS, DE) 20 RIN2+ + LVDS differential clock input (B2-B5,HS,VS, DE) 21 VSS Ground 22 CLK- - LVDS differential clock input 23 CLK- + LVDS differential clock input 24 VSS Ground 25 INV PWM PWM brightness control			
7 TEST Panel Self Test 8 CLK EDID clock 9 DATA EDID data 10 VSS Ground 11 VSS Ground 12 NC no connection 13 RIN0- - LVDS differential data input (R0-R5, G0) 14 RIN0+ + LVDS differential data input (G1-G5, B0-B1) 15 VSS Ground 16 RIN1- - LVDS differential data input (G1-G5, B0-B1) 17 RIN1+ + LVDS differential data input (B2-B5,HS,VS, DE) 19 RIN2- - LVDS differential data input (B2-B5,HS,VS, DE) 20 RIN2+ + LVDS differential clock input (B2-B5,HS,VS, DE) 21 VSS Ground 22 CLK- - LVDS differential clock input 23 CLK+ + LVDS differential clock input 24 VSS Ground 25 INV_PWM PWM brightness control 26 VBL- LED power return 27 VBL- LED power return </td <td></td> <td></td> <td></td>			
8 CLK EDID clock 9 DATA EDID data 10 VSS Ground 11 VSS Ground 11 VSS Ground 12 NC no connection 13 RIN0 LVDS differential data input (R0-R5, G0) 14 RIN0+ + LVDS differential data input (R0-R5, G0) 15 VSS Ground 16 RIN1 LVDS differential data input (G1-G5, B0-B1) 17 RIN1+ + LVDS differential data input (G1-G5, B0-B1) 18 VSS Ground 19 RIN2 LVDS differential data input (B2-B5,HS,VS, DE) 20 RIN2+ + LVDS differential data input (B2-B5,HS,VS, DE) 21 VSS Ground 22 CLK LVDS differential clock input 23 CLK+ + LVDS differential clock input 24 VSS Ground 25 INV PWM PWM brightness control 26 VBL- LED power return 27 VBL- LED power return 28 VBL- LED power return 30 VBL- LED power return 31 NC no connection 32 VBL+ 7V - 20V LED power source 33 VBL+ 7V - 20V LED power source 34 VBL+ 7V - 20V LED power source 35 VBL+ 7V - 20V LED power source 36 VBL+ 7V - 20V LED power source 37 CONNTST Connector test 38 SMB CLK SMBus Clock 39 SMB DAT SMBus Data			
9 DATA			
10		_	
11			
12 NC no connection 13 RIN0- - LVDS differential data input (R0-R5, G0) 14 RIN0+ + LVDS differential data input (R0-R5, G0) 15 VSS Ground 16 RIN1- - LVDS differential data input (G1-G5, B0-B1) 17 RIN1+ + LVDS differential data input (G1-G5, B0-B1) 18 VSS Ground 19 RIN2- - LVDS differential data input (B2-B5,HS,VS, DE) 20 RIN2+ + LVDS differential data input (B2-B5,HS,VS, DE) 21 VSS Ground 22 CLK- - LVDS differential clock input 23 CLK+ + LVDS differential clock input 24 VSS Ground 25 INV_PWM PWM brightness control 26 VBL- LED power return 27 VBL- LED power return 28 VBL- LED power return 30 VBL- LED power return 31 NC no connection 32 VBL+ 7V - 20V LE			
13 RINO LVDS differential data input (R0-R5, G0) 14 RINO+ + LVDS differential data input (R0-R5, G0) 15 VSS Ground 16 RIN1 LVDS differential data input (G1-G5, B0-B1) 17 RIN1+ + LVDS differential data input (G1-G5, B0-B1) 18 VSS Ground 19 RIN2 LVDS differential data input (B2-B5,HS,VS, DE) 20 RIN2+ + LVDS differential data input (B2-B5,HS,VS, DE) 21 VSS Ground 22 CLK LVDS differential clock input 23 CLK+ + LVDS differential clock input 24 VSS Ground 25 INV_PWM PWM brightness control 26 VBL- LED power return 27 VBL- LED power return 28 VBL- LED power return 29 VBL- LED power return 30 VBL- LED power return 31 NC no connection 32 VBL+ 7V - 20V LED power source 33 VBL+ 7V - 20V LED power source 34 VBL+ 7V - 20V LED power source 35 VBL+ 7V - 20V LED power source 36 VBL+ 7V - 20V LED power source 37 CONNTST Connector test 38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data			
14 RIN0+ + LVDS differential data input (R0-R5, G0) 15 VSS Ground 16 RIN1 LVDS differential data input (G1-G5, B0-B1) 17 RIN1+ + LVDS differential data input (G1-G5, B0-B1) 18 VSS Ground 19 RIN2 LVDS differential data input (B2-B5,HS,VS, DE) 20 RIN2+ + LVDS differential data input (B2-B5,HS,VS, DE) 21 VSS Ground 22 CLK LVDS differential clock input 23 CLK+ + LVDS differential clock input 24 VSS Ground 25 INV PWM PWM brightness control 26 VBL- LED power return 27 VBL- LED power return 28 VBL- LED power return 29 VBL- LED power return 30 VBL- LED power return 31 NC no connection 32 VBL+ 7V - 20V LED power source 33 VBL+ 7V - 20V LED power source 34 VBL+ 7V - 20V LED power source 35 VBL+ 7V - 20V LED power source 36 VBL+ 7V - 20V LED power source 37 CONNTST Connector test 38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data			
15 VSS Ground 16 RIN1- - LVDS differential data input (G1-G5, B0-B1) 17 RIN1+ + LVDS differential data input (G1-G5, B0-B1) 18 VSS Ground 19 RIN2- - LVDS differential data input (B2-B5,HS,VS, DE) 20 RIN2+ + LVDS differential data input (B2-B5,HS,VS, DE) 21 VSS Ground 22 CLK- - LVDS differential clock input 23 CLK+ + LVDS differential clock input 24 VSS Ground 25 INV PWM PWM brightness control 26 VBL- LED power return 27 VBL- LED power return 28 VBL- LED power return 29 VBL- LED power return 30 VBL- LED power source 31 NC no connection 32 VBL+ 7V - 20V LED power source 34 VBL+ 7V - 20V LED power source 35 VBL+ 7V - 20V LED power source	_		
16 RIN1 LVDS differential data input (G1-G5, B0-B1) 17 RIN1+ + LVDS differential data input (G1-G5, B0-B1) 18 VSS Ground 19 RIN2 LVDS differential data input (B2-B5,HS,VS, DE) 20 RIN2+ + LVDS differential data input (B2-B5,HS,VS, DE) 21 VSS Ground 22 CLK LVDS differential clock input 23 CLK+ + LVDS differential clock input 24 VSS Ground 25 INV_PWM PWM brightness control 26 VBL- LED power return 27 VBL- LED power return 28 VBL- LED power return 29 VBL- LED power return 30 VBL- LED power return 31 NC no connection 32 VBL+ 7V - 20V LED power source 33 VBL+ 7V - 20V LED power source 34 VBL+ 7V - 20V LED power source 35 VBL+ 7V - 20V LED power source 36 VBL+ 7V - 20V LED power source 37 CONNTST Connector test 38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data			
17 RIN1+ + LVDS differential data input (G1-G5, B0-B1) 18 VSS Ground 19 RIN2 LVDS differential data input (B2-B5,HS,VS, DE) 20 RIN2+ + LVDS differential data input (B2-B5,HS,VS, DE) 21 VSS Ground 22 CLK LVDS differential clock input 23 CLK+ + LVDS differential clock input 24 VSS Ground 25 INV_PWM PWM brightness control 26 VBL- LED power return 27 VBL- LED power return 28 VBL- LED power return 29 VBL- LED power return 30 VBL- LED power return 31 NC no connection 32 VBL+ 7V - 20V LED power source 33 VBL+ 7V - 20V LED power source 34 VBL+ 7V - 20V LED power source 35 VBL+ 7V - 20V LED power source 36 VBL+ 7V - 20V LED power source 37 CONNTST Connector test 38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data			
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28 VBL- LED power return 29 VBL- LED power return 30 VBL- LED power return 31 NC no connection 32 VBL+ 7V - 20V LED power source 33 VBL+ 7V - 20V LED power source 34 VBL+ 7V - 20V LED power source 35 VBL+ 7V - 20V LED power source 36 VBL+ 7V - 20V LED power source 37 CONNTST Connector test 38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data	26	VBL-	LED power return
29 VBL- LED power return 30 VBL- LED power return 31 NC no connection 32 VBL+ 7V - 20V LED power source 33 VBL+ 7V - 20V LED power source 34 VBL+ 7V - 20V LED power source 35 VBL+ 7V - 20V LED power source 36 VBL+ 7V - 20V LED power source 37 CONNTST Connector test 38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data	27	VBL-	LED power return
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31 NC no connection 32 VBL+ 7V - 20V LED power source 33 VBL+ 7V - 20V LED power source 34 VBL+ 7V - 20V LED power source 35 VBL+ 7V - 20V LED power source 36 VBL+ 7V - 20V LED power source 37 CONNTST Connector test 38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data	29	VBL-	LED power return
32 VBL+ 7V - 20V LED power source 33 VBL+ 7V - 20V LED power source 34 VBL+ 7V - 20V LED power source 35 VBL+ 7V - 20V LED power source 36 VBL+ 7V - 20V LED power source 37 CONNTST Connector test 38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data	30	VBL-	LED power return
33 VBL+ 7V - 20V LED power source 34 VBL+ 7V - 20V LED power source 35 VBL+ 7V - 20V LED power source 36 VBL+ 7V - 20V LED power source 37 CONNTST Connector test 38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data	31	NC	no connection
34 VBL+ 7V - 20V LED power source 35 VBL+ 7V - 20V LED power source 36 VBL+ 7V - 20V LED power source 37 CONNTST Connector test 38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data	32	VBL+	7V - 20V LED power source
35 VBL+ 7V - 20V LED power source 36 VBL+ 7V - 20V LED power source 37 CONNTST Connector test 38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data	33	VBL+	7V - 20V LED power source
36 VBL+ 7V - 20V LED power source 37 CONNTST Connector test 38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data	34	VBL+	7V - 20V LED power source
37 CONNTST Connector test 38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data	35	VBL+	7V - 20V LED power source
38 SMB_CLK SMBus Clock 39 SMB_DAT SMBus Data	36	VBL+	7V - 20V LED power source
39 SMB_DAT SMBus Data	37	CONNTST	Connector test
39 SMB_DAT SMBus Data	38	SMB_CLK	SMBus Clock
			SMBus Data
	40	VSS	Ground

Note1: Start from right side

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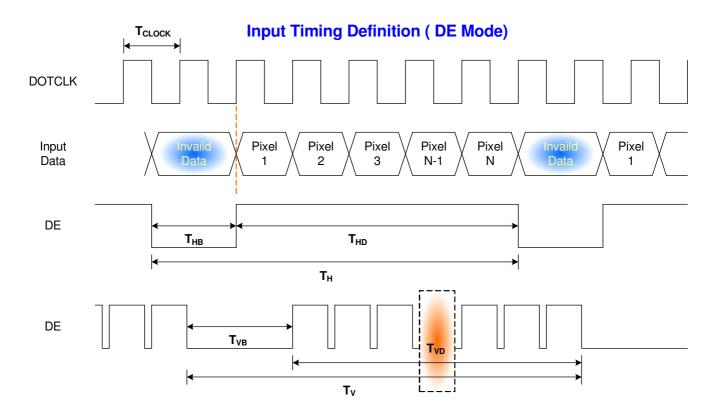
6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parai	meter	Symbol	Min.	Тур.	Max.	Unit
Frame	e Rate	-	50	60	-	Hz
Clock from	equency	1/ T _{Clock}	-	68.9	72	MHz
	Period	T _V	808	816	1023	
Vertical	Active	T _{VD}		800		T_Line
Section	Blanking	T _{VB}	8	16	-	
	Period	T _H	1320	1408	2047	
Horizontal	Active	T _{HD}		1280		T _{Clock}
Section	Blanking	T _{HB}	30	128		

Note: DE mode only

6.4.2 Timing diagram

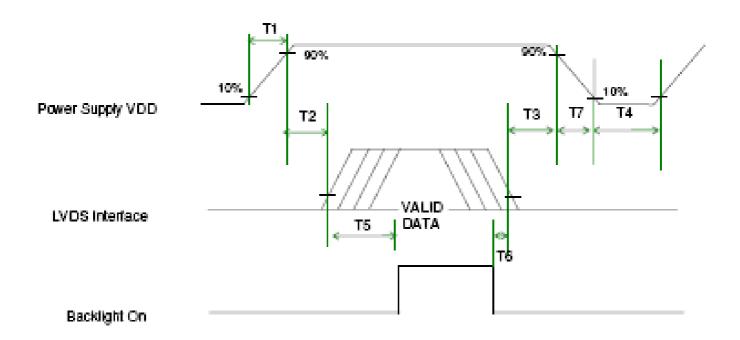




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6.5 Power ON/OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Power Sequence Timing

		Value		
Parameter	Min.	Тур.	Max.	Units
T1	0.5	-	10	
T2	0	-	50	
Т3	0	-	50	
T4	400	_	-	ms
T5	200	_	-	
T6	200			
10	200	-	-	
T7	0	-	10	



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7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	20347-340E-12 or compatible
Mating Housing/Part Number	20346-040T-02 or compatible

8. LED Driving Specification

8.1 Connector Description

It is a intergrative interface and comibe into LVDS connector. The type and mating refer to section 7.

8.2 Pin Assignment

Ref. to 6.3



9. Vibration and Shock Test

9.1 Vibration Test

Test condition(Non-OP):

Acceleration: 1.3 G

Frequency: 10 - 500Hz Random

Sweep: 30 Minutes each Axis (X, Y, Z)

9.2 Shock Test Spec:

Test condition (Non-OP):

Acceleration: 220 G, Half sine wave

Active time: 2 ms

Pulse: +/-X,+/-Y,+/-Z, one time for each side

Remark:

Ambient condition is $25 \pm 5^{\circ}$ C, Relative humidity : $40\% \sim 70\%$

Non-packaged and Non-operation



10. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 95%RH, 250h	
High Temperature Operation	Ta= 50℃, Dry, 250h	
Low Temperature Operation	Ta= 0℃, 250h	
High Temperature Storage	Ta= 65℃/20%, 250h	
Low Temperature Storage	Ta= -25℃, 50%RH, 250h	
Thermal Shock Test	Ta=-40℃to 65℃, Duration at 30 min, 50 cycles	
ESD	Contact : ±8 KV	Note 1
LSD	Air: ±15 KV	

Note1: According to EN 61000-4-2, ESD class B: Some performance degradation allowed. No data lost

. Self-recoverable. No hardware failures.

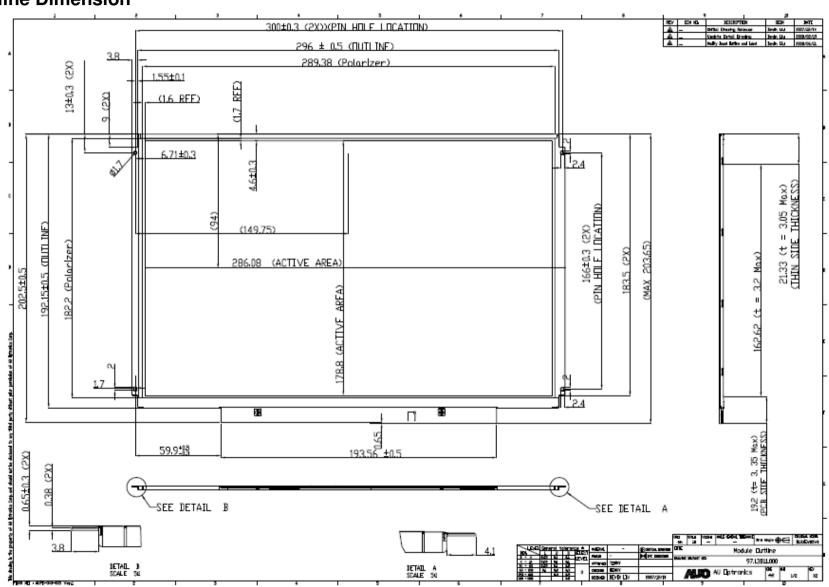
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%



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11. Mechanical Characteristics

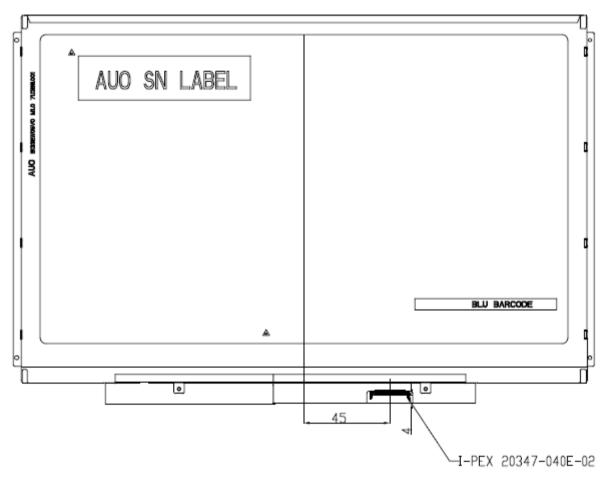
11.1 LCM Outline Dimension



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Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

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12. Shipping and Package

12.1 Shipping Label Format



Manufactured 05/52

Model No: B133EW05 V0

AU Optronics 0AXXG

MADE IN China (S1) H/W: 0A F/W:1



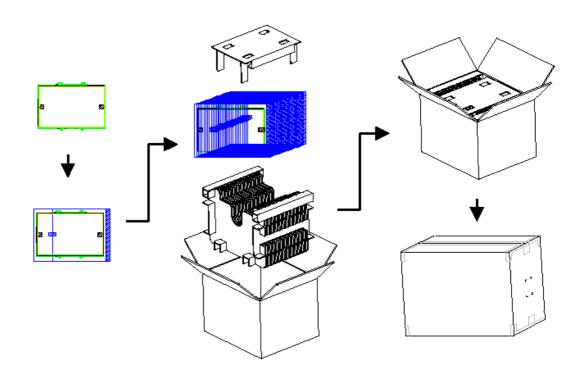




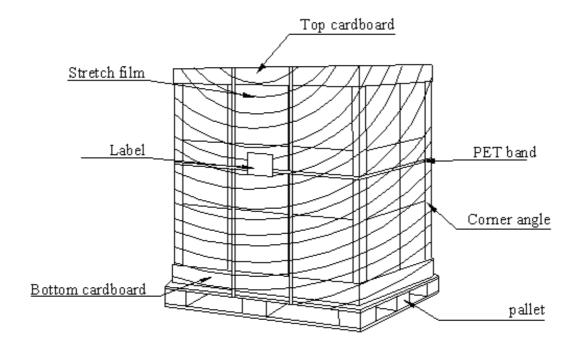


12.2 Carton package

The outside dimension of carton is 430 (L)mm x 378 (W)mm x 341 (H)mm



12.3 Shipping package of palletizing sequence





13. Appendix: EDID description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
80	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	24	00100100	36	
0B	hex, LSB first	50	01010000	80	
ОС	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	01	00000001	1	
11	Year of manufacture	12	00010010	18	
12	EDID Structure Ver.	01	0000001	1	
13	EDID revision #	03	00000011	3	
14	Video input def. (digital I/P, non-TMDS, CRGB)	80	10000000	128	
15	Max H image size (rounded to cm)	1D	00011101	29	
16	Max V image size (rounded to cm)	12	00010010	18	
17	Display Gamma (=(gamma*100)-100)	78	01111000	120	
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	0A	00001010	10	
19	Red/green low bits (Lower 2:2:2:2 bits)	90	10010000	144	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	B5	10110101	181	
1B	Red x (Upper 8 bits)	99	10011001	153	
1C	Red y/ highER 8 bits	58	01011000	88	
1D	Green x	52	01010010	82	
1E	Green y	8E	10001110	142	
1F	Blue x	26	00100110	38	
20	Blue y	1E	00011110	30	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	



	l l		Ì
	01	0000001	1
Standard timing #2	01	0000001	1
	01	00000001	1
Standard timing #3	01	00000001	1
	01	0000001	1
Standard timing #4	01	0000001	1
	01	0000001	1
Standard timing #5	01	0000001	1
	01	0000001	1
Standard timing #6	01	0000001	1
	01	00000001	1
Standard timing #7	01	0000001	1
	01	00000001	1
Standard timing #8	01	0000001	1
	01	0000001	1
Pixel Clock/10000 LSB	58	01011000	88
Pixel Clock/10000 USB	1B	00011011	27
Horz active Lower 8bits	00	00000000	0
Horz blanking Lower 8bits	8A	10001010	138
HorzAct:HorzBlnk Upper 4:4 bits	50	01010000	80
Vertical Active Lower 8bits	20	00100000	32
Vertical Blanking Lower 8bits			23
Vert Act : Vertical Blanking (upper 4:4 bit)	30		48
HorzSync. Offset	30		48
HorzSync.Width	20	00100000	32
VertSync.Offset : VertSync.Width	36	00110110	54
Horz‖ Sync Offset/Width Upper 2bits			0
Horizontal Image Size Lower 8bits	1E	00011110	30
Vertical Image Size Lower 8bits			178
Horizontal & Vertical Image Size (upper 4:4 bits)			16
Horizontal Border (zero for internal LCD)			0
Vertical Border (zero for internal LCD)			0
Signal (non-intr, norm, no stero, sep sync, neg pol)			24
Detailed timing/monitor			0
-			0
			0
			15
			0
			0
			0
			0
			0
	00	0000000	0
	Standard timing #3 Standard timing #4 Standard timing #5 Standard timing #6 Standard timing #7 Standard timing #8 Pixel Clock/10000 LSB Pixel Clock/10000 USB Horz active Lower 8bits Horz blanking Lower 8bits HorzAct:HorzBlnk Upper 4:4 bits Vertical Active Lower 8bits Vertical Blanking Lower 8bits Vertical Flanking Lower 8bits Vertical Flanking Lower 8bits Vertical Blanking Lower 8bits Vertical Flanking Upper 4:4 bits Vertical Blanking Upper 4:4 bits HorzSync. Offset HorzSync. Width VertSync. Offset : VertSync. Width Horz‖ Sync Offset/Width Upper 2bits Horizontal Image Size Lower 8bits Vertical Image Size Lower 8bits Horizontal & Vertical Image Size (upper 4:4 bits) Horizontal Border (zero for internal LCD) Vertical Border (zero for internal LCD)	Standard timing #2	Standard timing #2



52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	0000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	Α
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	0
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	В
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	33	00110011	51	3
74	Manufacture P/N	33	00110011	51	3
75	Manufacture P/N	45	01000101	69	Е
76	Manufacture P/N	57	01010111	87	W
77	Manufacture P/N	30	00110000	48	0
78	Manufacture P/N	35	00110101	53	5
79	Manufacture P/N	20	00100000	32	
7 A	Manufacture P/N	56	01010110	86	V
7B	Manufacture P/N	30	00110000	48	0
7C		20	00100000	32	
B133EW05 V0 _D	Occument Version : 0.5			31 (of 32



7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	71	01110001	113	
			SUM		