(V) Preliminary Specifications
( ) Final Specifications

Module	16.4” HD+ - Color TFT-LCD
Model Name	B164RW01 V0 (H/W:0A)

Customer	**Date**
Checked & Approved by	**Date**
Note: This Specification is subject to change without notice.	

Approved by	**Date**
Beyond Yang	09/12/2008
Prepared by	**Date**
Jeff Hou	09/12/2008
NBBU Marketing Division / AU Optronics corporation	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2008/07/29	All	First Edition for Customer		
0.2 2008/08/21	15		Update 5.2 Blacklight Unit Spec.	
0.3 2008/9/12	19,20		Update LVDS AC characteristics	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CCFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp (CCFL) in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit (IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

2. General Description

B164RW01 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the HD+ (1600(H) x 900(V)) screen and 262k colors (RGB 6-bits data driver) without backlight inverter. All input signals are LVDS interface compatible.

B164RW01 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

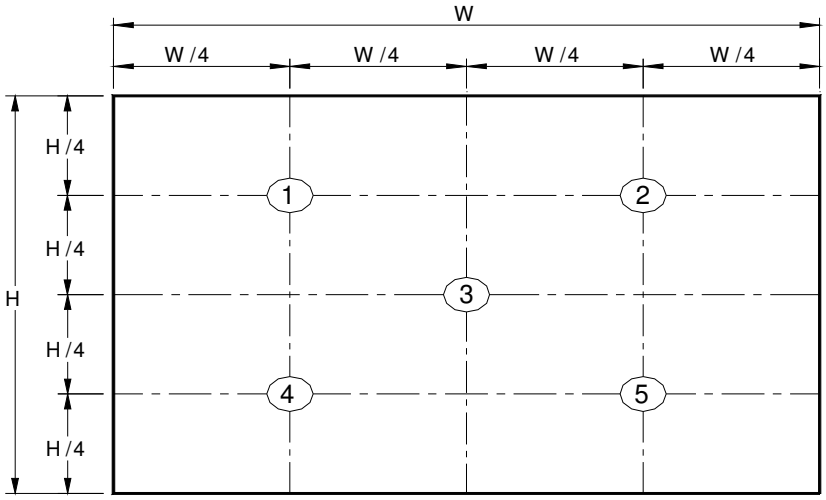
Items	Unit	Specifications			
Screen Diagonal	[mm]	415.798 (16.37W")			
Active Area	[mm]	362.4 X 203.85			
Pixels H x V		1600x3(RGB) x 900			
Pixel Pitch	[mm]	0.2265X0.2265			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance **(I_{CCFL}=6.0mA)** Note: I_{CCFL} is lamp current	[cd/m^2]	210 typ. (5 points average) 180 min. (5 points average) (Note1)			
Luminance Uniformity		1.25 max. (5 points) 1.42 max. (13 points)			
Contrast Ratio		500 typ			
Response Time	[ms]	8 typ / 15 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	1.85 max. – TFT 4.84 max. – Backlight			
Weight	[Grams]	610 max.			
Physical Size **without inverter, bracket**	[mm]		Min.	Typ.	Max.
		Length	374.5	375.0	375.5
		Width	218.6	219.1	219.6
		Thickness	-	-	6.5
Electrical Interface		2 channel LVDS			
Surface Treatment		Glare, Hardness 3H,			
Support Color		262K colors (RGB 6-bit)			
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

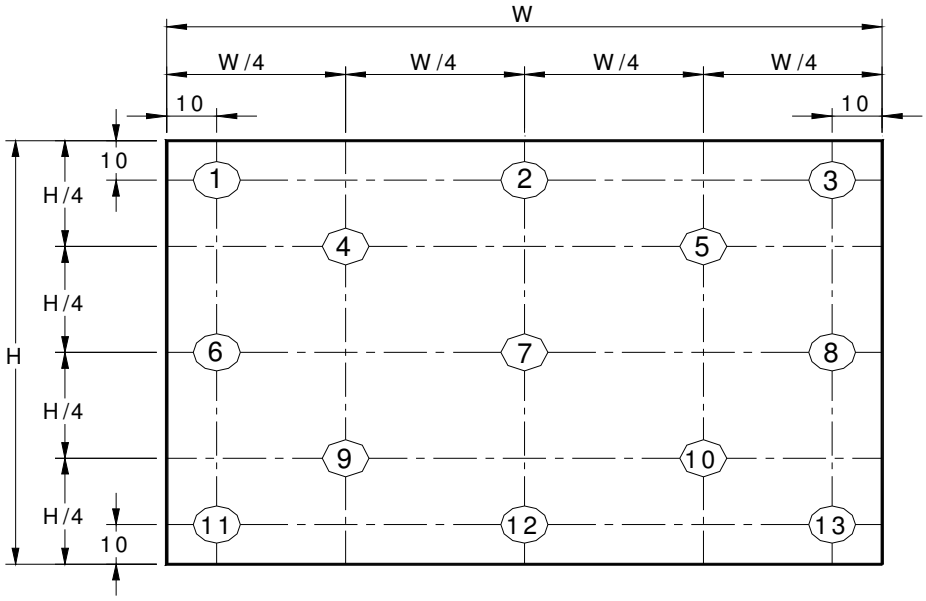
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{CCFL}=6.0mA			5 points average	180	210	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10 (Left)	-	45	-	degree	4, 9
		θ_L		-	45	-		
		ϕ_H	Vertical (Upper) CR = 10 (Lower)	-	20	-		
		ϕ_L		-	40	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
		δ_{13P}	13 Points	-	-	1.42		2, 3, 4
Contrast Ratio		CR		400	500	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_r	Rising	-	-	-	msec	4, 8
		T_f	Falling	-	-	-		
		T_{RT}	Rising + Falling	-	8	15		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.571	0.601	0.631		4
		Ry		0.319	0.349	0.379		
	Green	Gx		0.278	0.308	0.338		
		Gy		0.539	0.569	0.599		
	Blue	Bx		0.121	0.151	0.181		
		By		0.100	0.130	0.160		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	50	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



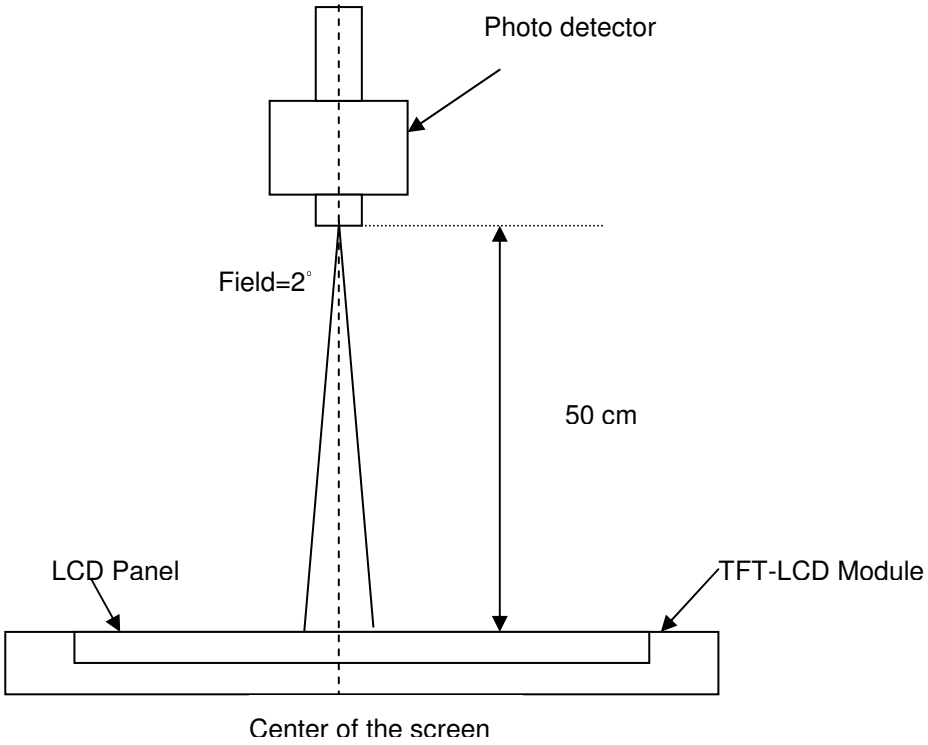
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

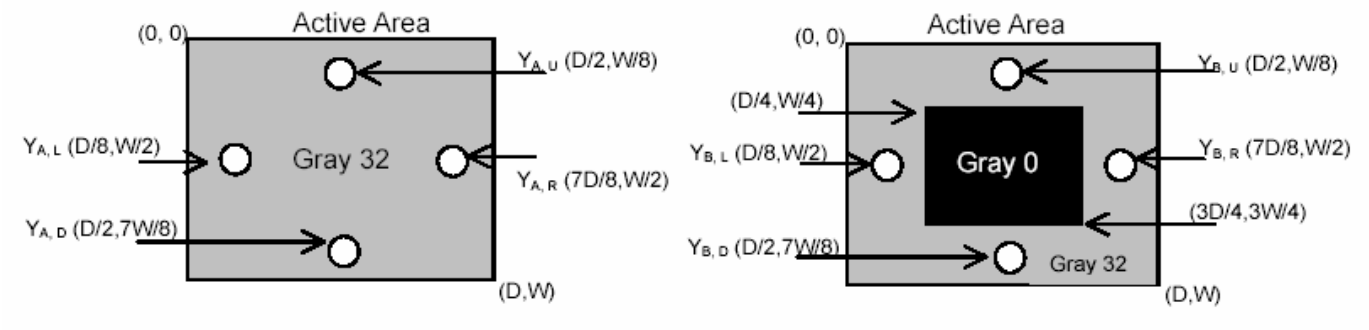
Note 7： Definition of Cross Talk (CT)

$CT = |Y_B - Y_A| / Y_A \times 100\ (\%)$

Where

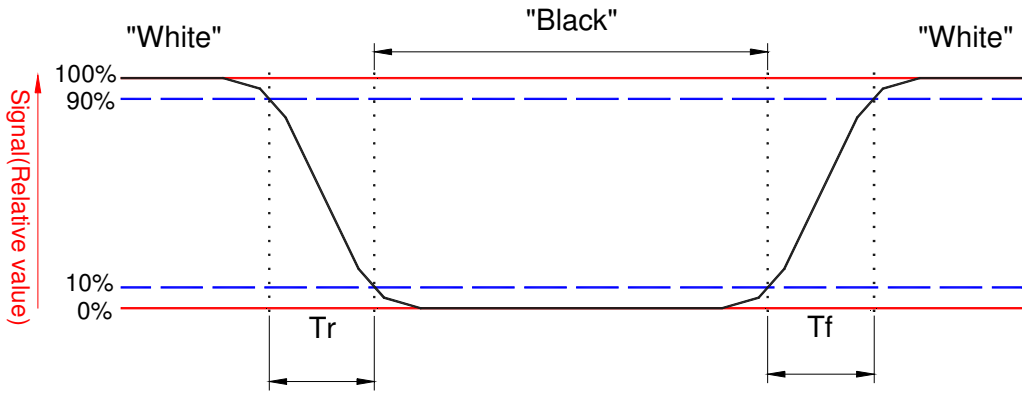
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



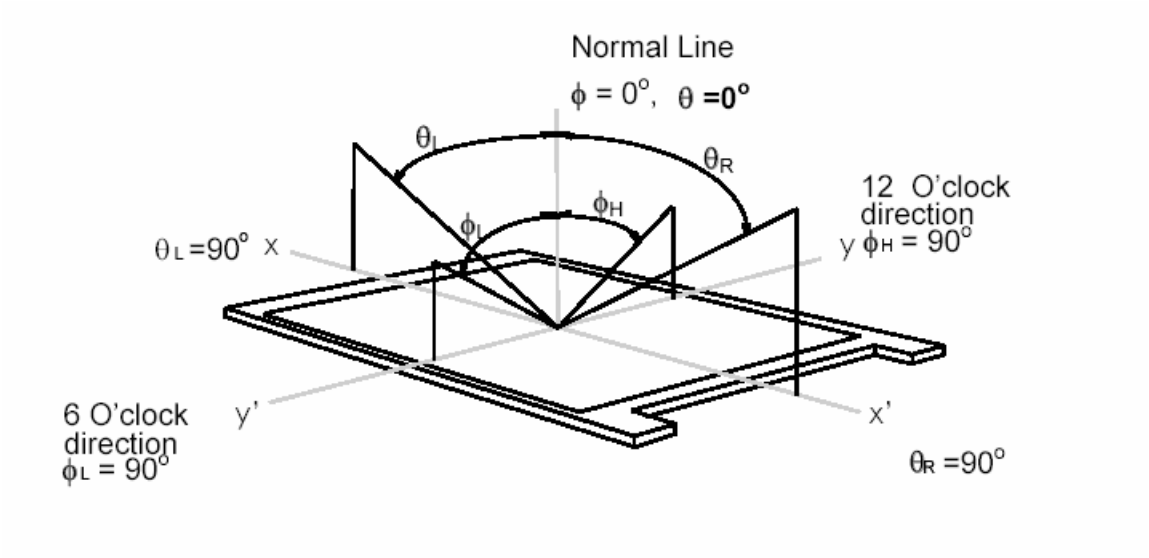
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



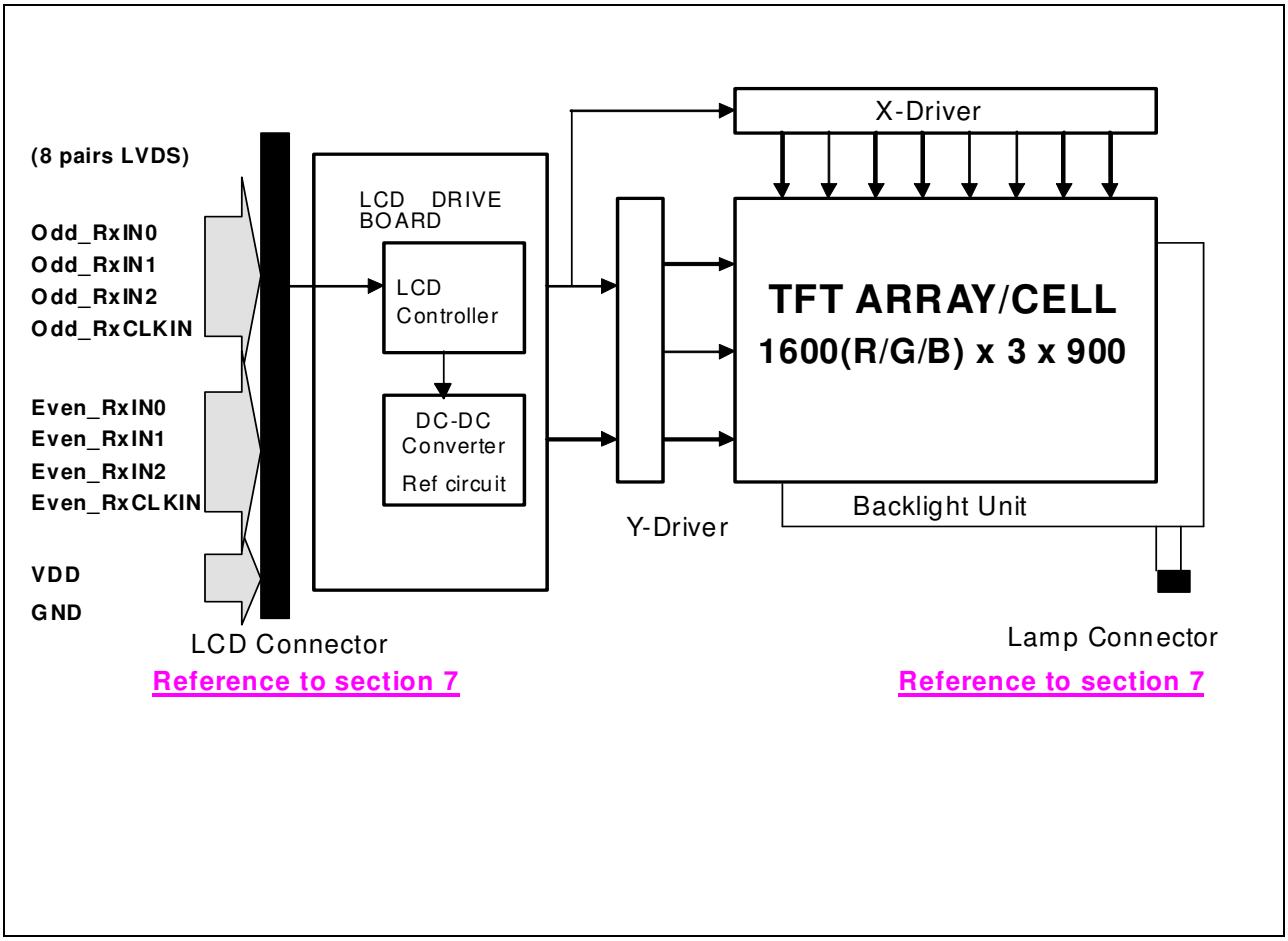
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 16.4 inches wide Color TFT/LCD Module:



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	-	7.0	[mA] rms	Note 1,2

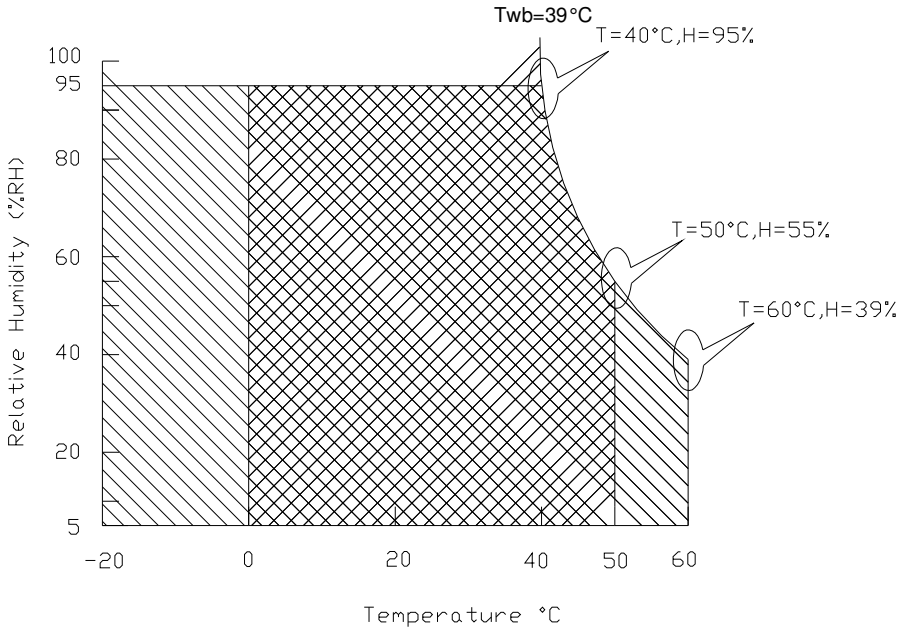
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

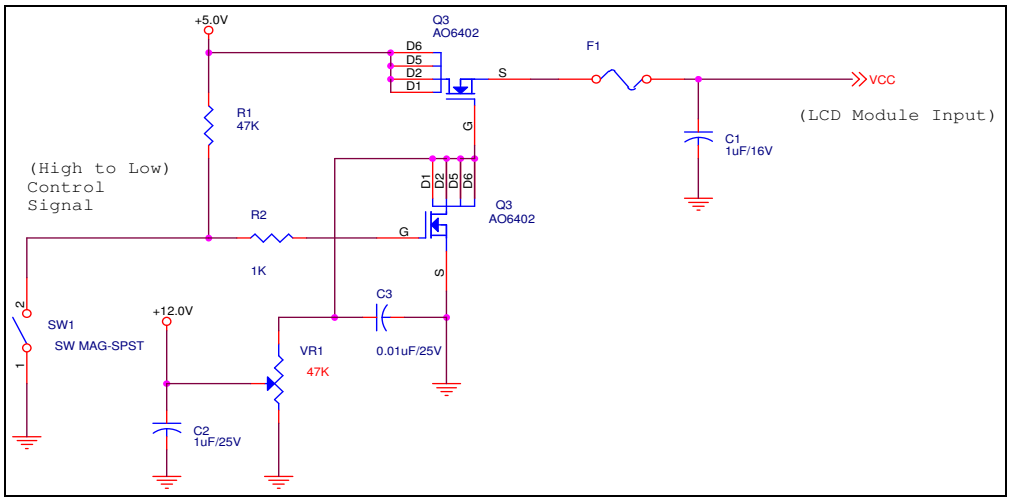
The power specification are measured under 25℃ and frame frenquency under 60Hz

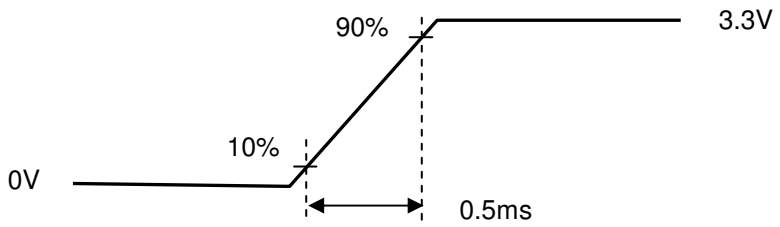
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	1.5	1.85	[Watt]	Note 1/2
IDD	IDD Current	-	450	560	[mA]	Note 1/2
IRush	Inrush Current	-	-	1500	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern

Note 2：Typical Measurement Condition: Mosaic Pattern

Note 3：Measure Condition





Vin rising time

5.1.2 Signal Electrical Characteristics

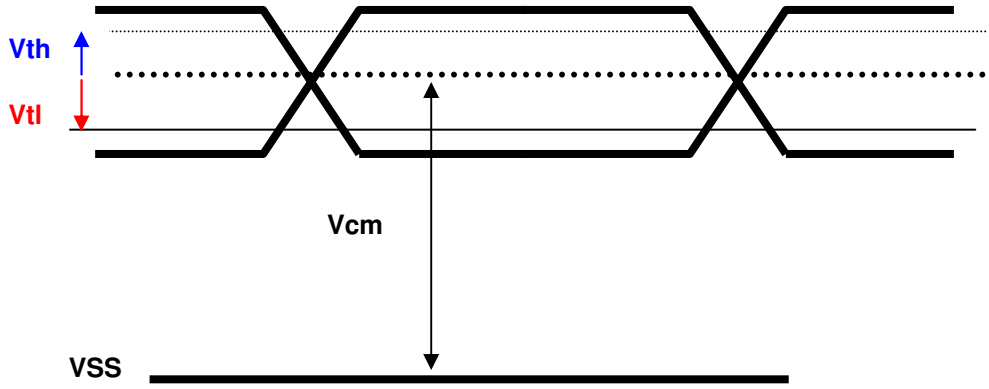
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A (Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)	-	100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

CCFL Parameter guideline for CCFL Inverter selection (Ref. Remark 1)

Parameter	Min	Typ	Max	Units	Condition
CCFL current(I_{CCFL})	2.0	6.0	7.0	[mA] rms	(Ta=25℃) Note 1, 6
CCFL Frequency(F_{CCFL})	44	55	62	[KHz]	(Ta=25℃) Note 2,3
CCFL startup Voltage(Vs)			1500	[Volt] rms	(Ta= 0℃) Note 4
CCFL startup Voltage(Vs)			1200	[Volt] rms	(Ta= 25℃) Note 4
CCFL Voltage (Reference) (V_{CCFL})	703	740	777	[Volt] rms	(Ta=25℃) Note 5
CCFL Power consumption (P_{CCFL})	-	4.4	4.84	[Watt]	(Ta=25℃) Note 5
CCFL Life-Time	10,000	-	-	Hour	(Ta=25℃) Note 7

To optimun TFT LCD performance, the LAMP inverter PWM Frequesncy define as:210 +/-5 Hz

Remark 1: Typ are AUO recommended Design Points.

1-1 All of characteristics listed are measured under the condition using the AUO Test inverter.

1-2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

1-3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CCFL is damaged.

1-4 Generally, CCFL has some amount of delay time after applying starting voltage. It is recommended to keep on applying starting voltage for **1 [Sec]** until discharge.

1-5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

1-6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 1: It should be employed the inverter which has “Duty Dimming”, if ICCFL is less than 4mA.

Note 2: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 3: The frequency range will not affect to lamp life and reliability characteristics.

Note 4: The output voltage of inverter should be able to give out a power after ballast capacitor , the generating capacity has to be larger than a lamp startup voltage, otherwise backlight may has blinking for a moment after turns on or can not be turned on.

Note 5: Calculator value for reference ($I_{CCFL} \times V_{CCFL} = P_{CCFL}$)

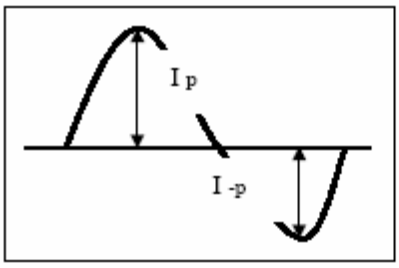
Note 6: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.

b. The distortion rate of the waveform should be within √2 ±10%.

* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

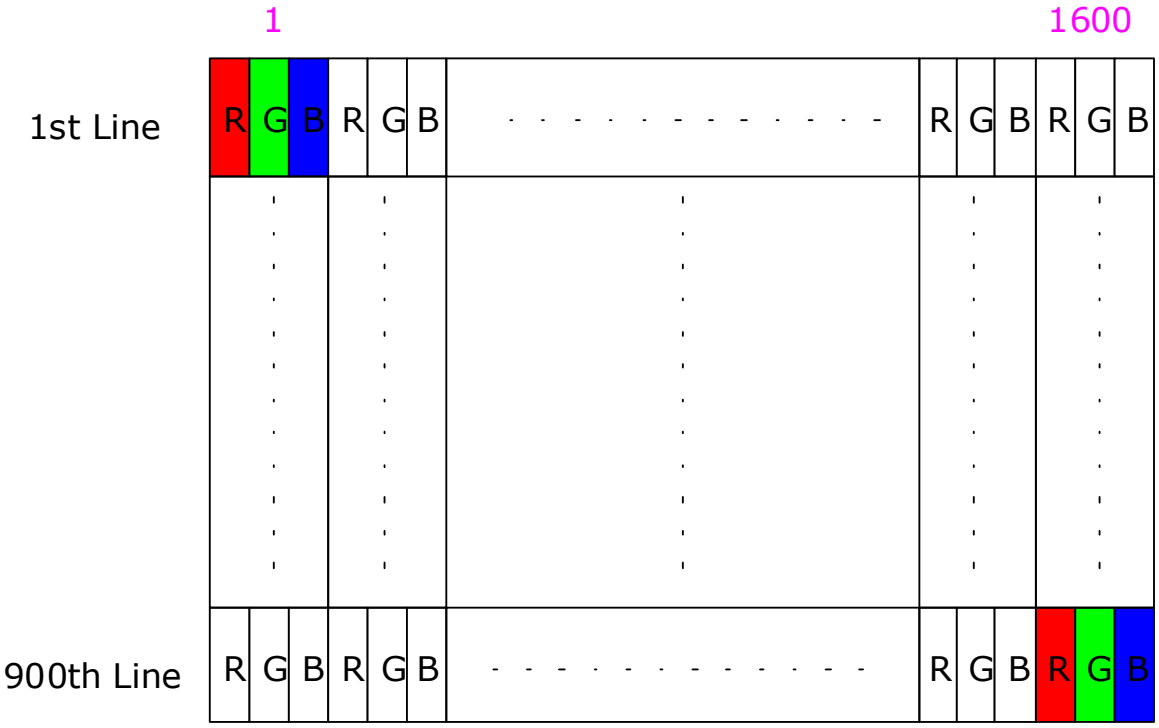
I_p (or I_{-p}) / I_{rms}

Note 7: It is an edge-type BLU with single CCFL, the life-time define as the brightness decay to 50% of original value and under normal operation.

6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format

Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.

DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

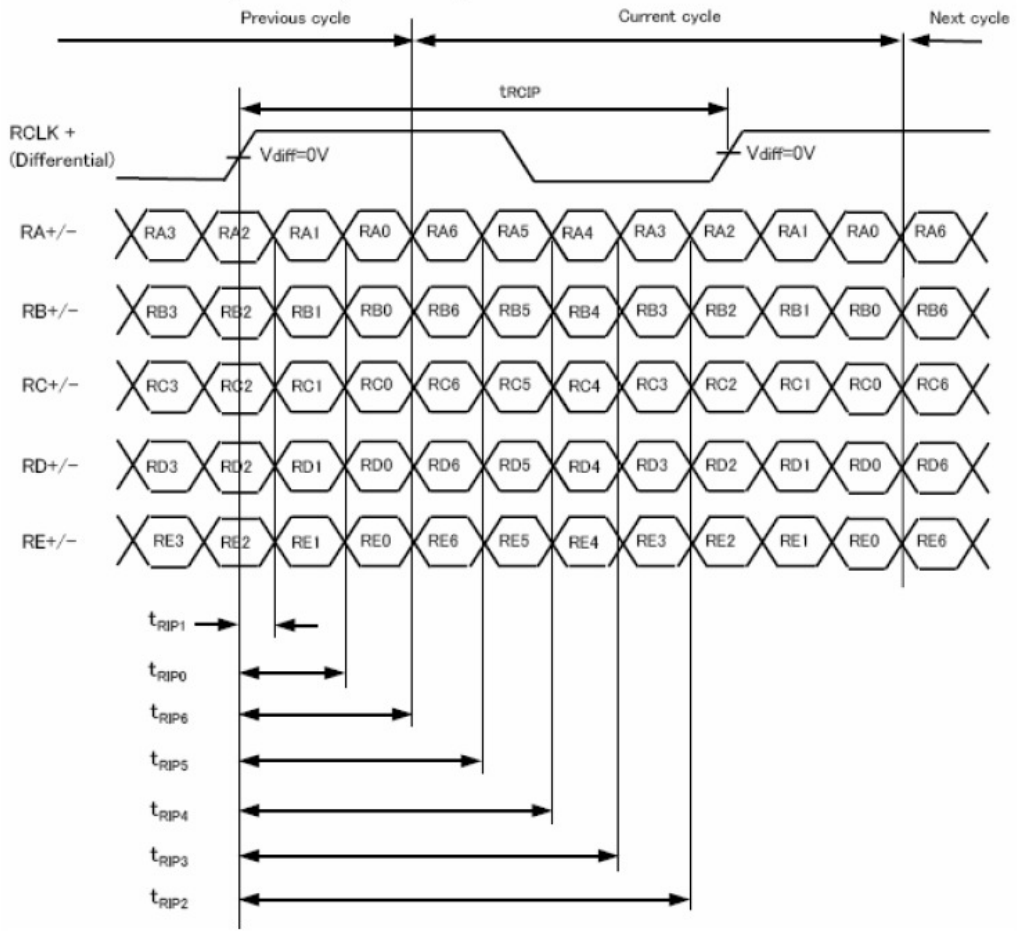
Note 1: Output signals from any system shall be low or High-impedance state when VDD is off.

Note 2: LVDS AC characteristics: (f=53MHz)

Symbol	Item	Value			Unit
		Min.	Typ.	Max.	
t_{RIP0}	Input data position0	0-0.45	0	0+0.45	ns
t_{RIP1}	Input data position1	tRCIP /7-0.45	tRCIP /7	tRCIP /7+0.45	ns
t_{RIP2}	Input data position2	2 tRCIP /7-0.45	2 tRCIP /7	2 tRCIP /7+0.45	ns
t_{RIP3}	Input data position3	3 tRCIP /7-0.45	3 tRCIP /7	3 tRCIP /7+0.45	ns
t_{RIP4}	Input data position4	4 tRCIP /7-0.45	4 tRCIP /7	4 tRCIP /7+0.45	ns
t_{RIP5}	Input data position5	5 tRCIP /7-0.45	5 tRCIP /7	5 tRCIP /7+0.45	ns
t_{RIP6}	Input data position6	6 tRCIP /7-0.45	6 tRCIP /7	6 tRCIP /7+0.45	ns

tRCIP=1/f

Note 3: LVDS Data, Clock Input Timing

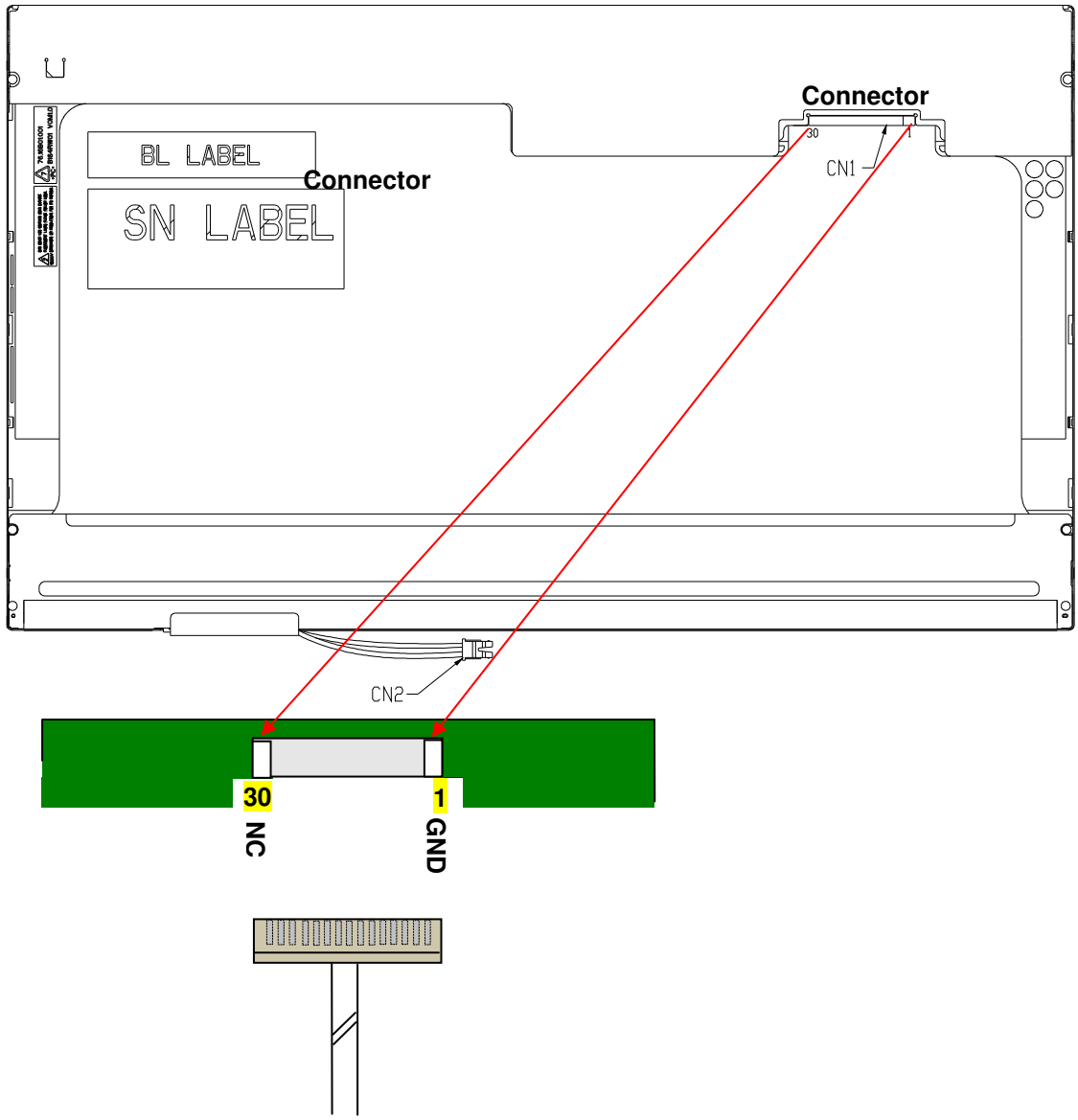


6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

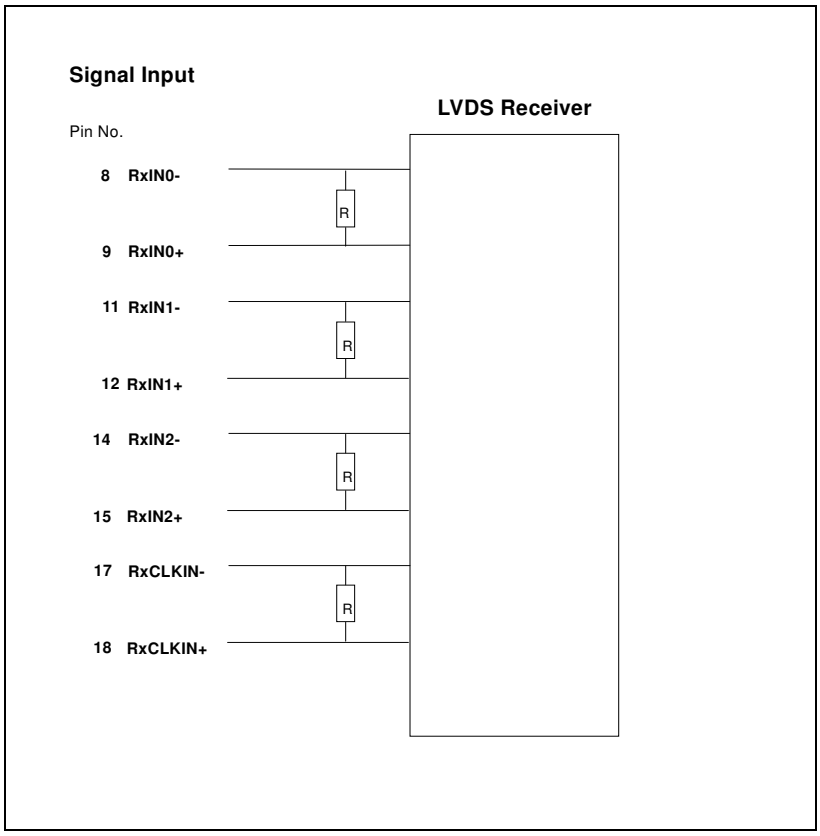
PIN #	SIGNAL NAME	DESCRIPTION
1	VSS	Power Ground
2	VDD	+ 3.3V Power Supply
3	VDD	+ 3.3V Power Supply
4	VEDID	+ 3.3V EDID Power
5	AGING (N.C. for Sony)	Aging Mode Power Supply
6	CLKEDID	EDID Clock Input
7	DATAEDID	EDID Data Input
8	Odd_Rin0-	-LVDS Differential Data Input
9	Odd_Rin0+	+LVDS Differential Data Input
10	VSS	Power Ground
11	Odd_Rin1-	-LVDS Differential Data Input
12	Odd_Rin1+	+LVDS Differential Data Input
13	VSS	Power Ground
14	Odd_Rin2-	-LVDS Differential Data Input
15	Odd_Rin2+	+LVDS Differential Data Input
16	VSS	Power Ground
17	Odd_ClkIN-	-LVDS Differential Clock Input
18	Odd_ClkIN+	+LVDS Differential Clock Input
19	VSS	Power Ground
20	Even_Rin0-	-LVDS Differential Data Input
21	Even_Rin0+	+LVDS Differential Data Input
22	VSS	Power Ground
23	Even_Rin1-	-LVDS Differential Data Input
24	Even_Rin1+	+LVDS Differential Data Input
25	VSS	Power Ground
26	Even_Rin2-	-LVDS Differential Data Input
27	Even_Rin2+	+LVDS Differential Data Input
28	VSS	Power Ground
29	Even_ClkIN-	-LVDS Differential Clock Input
30	Even_ClkIN+	+LVDS Differential Clock Input

Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.

internal circuit of LVDS inputs are as following.
The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

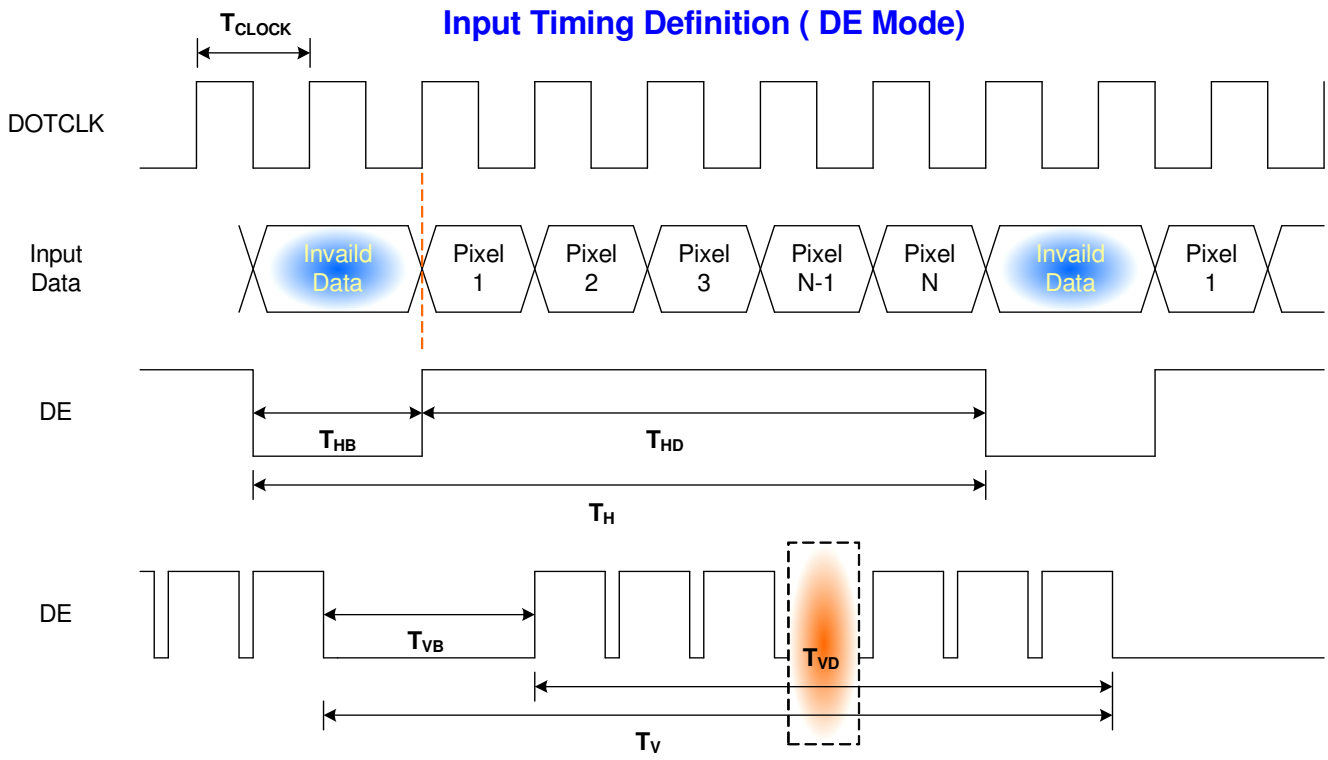
6.4.1 Timing Characteristics

Basically, interface timings should match the 1600x900 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-		60	-	Hz
Clock frequency		1/ T_{Clock}	50	53	80	MHz
Vertical Section	Period	T_V	908	912	2047	T_{Line}
	Active	T_{VD}	900	900	900	
	Blanking	T_{VB}	8	12	-	
Horizontal Section	Period	T_H	830	965	1024	T_{Clock}
	Active	T_{HD}	800	800	800	
	Blanking	T_{HB}	30	165	-	

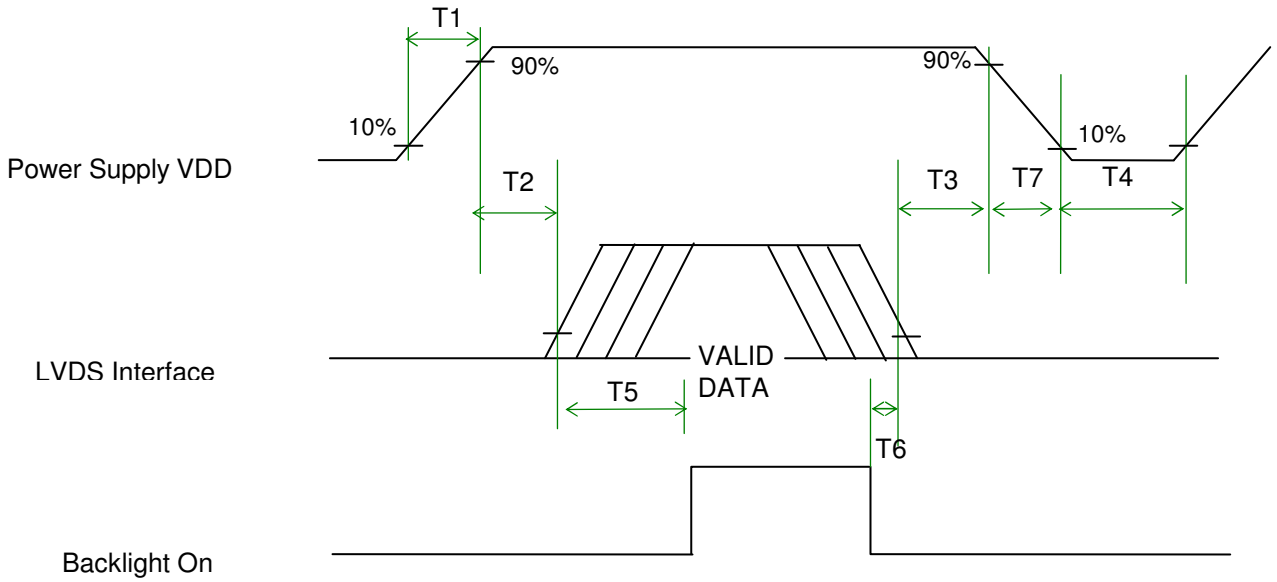
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SL-HF10 or compatible
Mating Housing/Part Number	FI-X30H or compatible

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage

8. Dynamic Test

8.1 Vibration Test

Test condition:

- Acceleration: 1.5 G , sine wave
- Frequency: 10 - 500Hz
- Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test condition:

- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: +/-X,+/-Y,+/-Z , one time for each side

Remark:

1. Ambient condition is 25 ± 5℃, Relative humidity : 40% ~ 70%
2. Non-packaged and Non-operation

9. Reliability

This Panel is also compliance with SONY RA criteria.

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 300h	
Low Temperature Storage	Ta= -20℃, 300h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

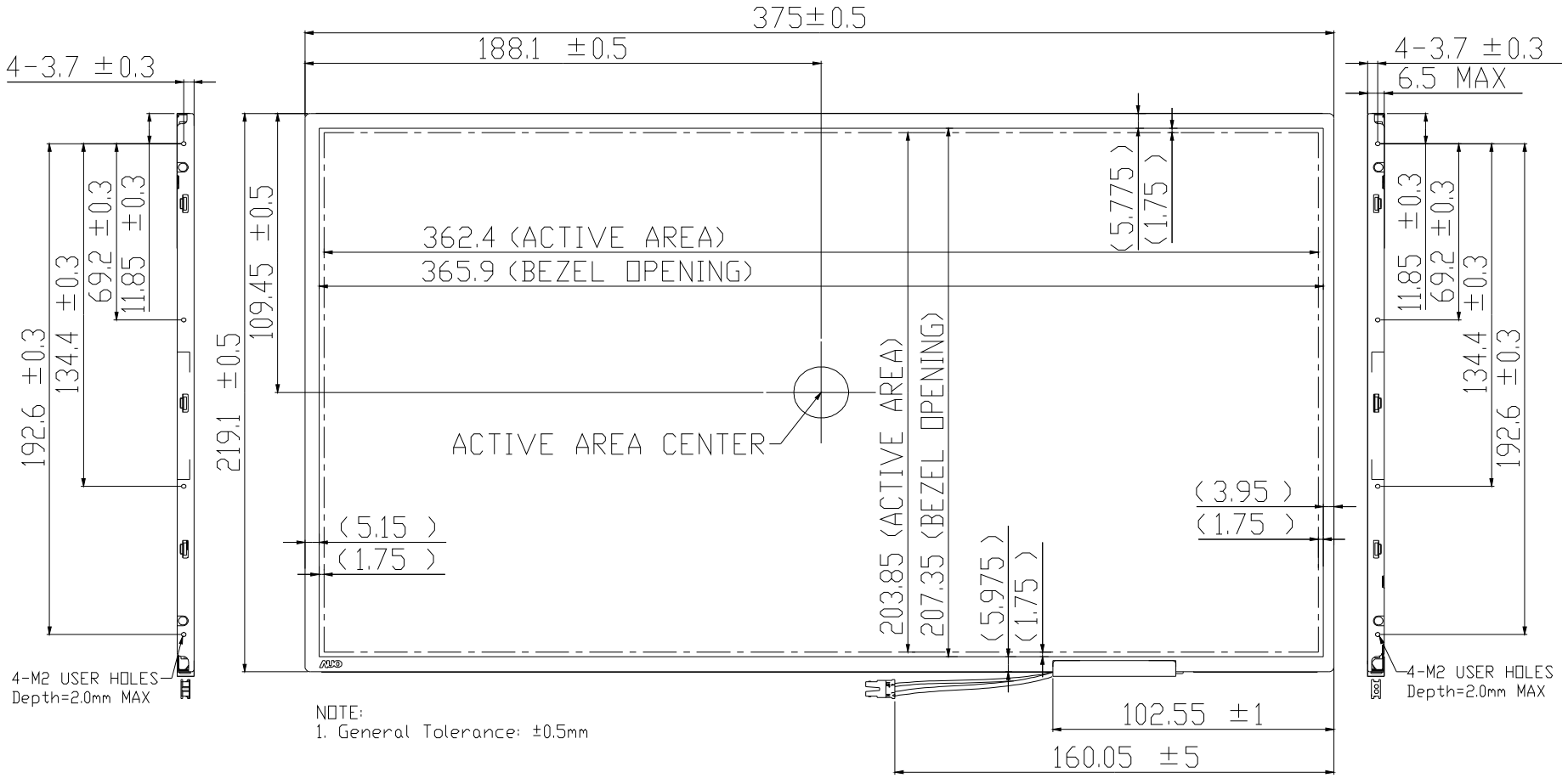
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

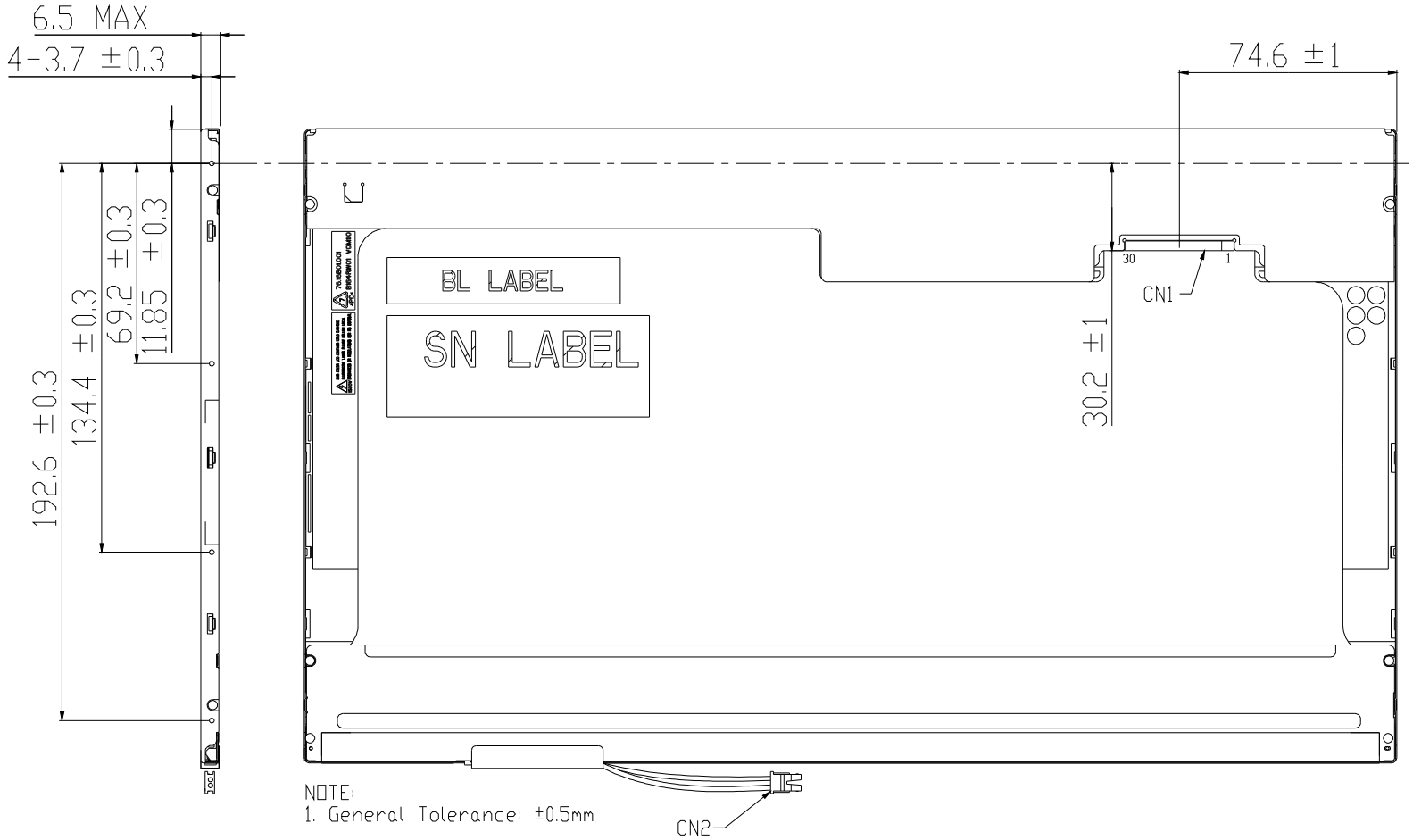
. Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the CCFL): 50,000 hours with a confidence level 90%

10. Mechanical Characteristics

10.1 LCM Outline Dimension

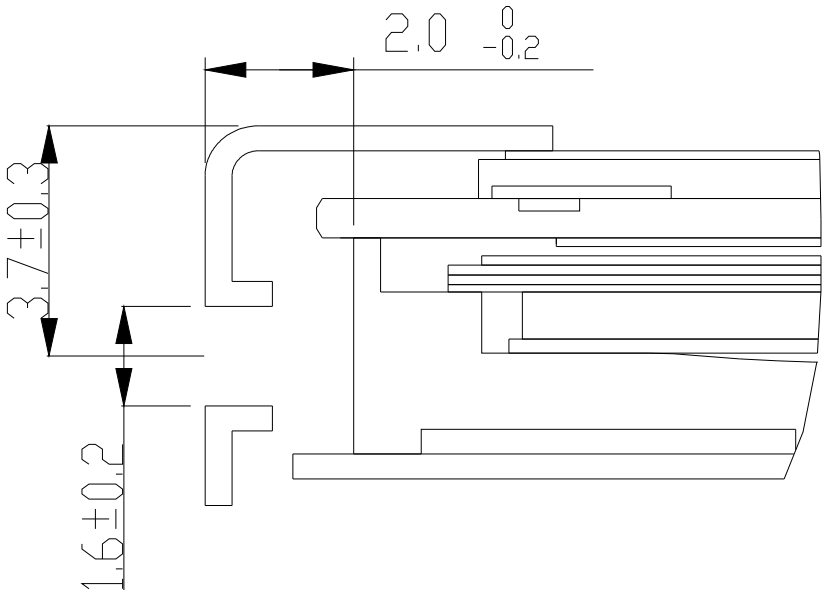




Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

10.2 Screw Hole Depth and Center Position

Screw hole center location, from front surface = 3.7 ± 0.3mm (Ref. drawing)
Screw Torque: Maximum 2.0 kgf-cm

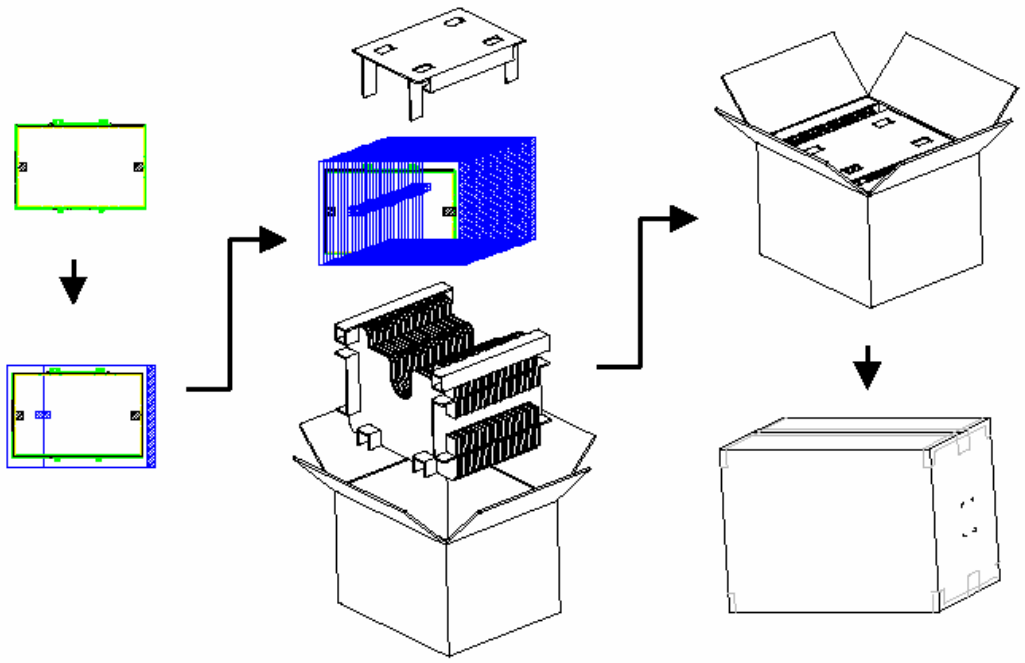


11. Shipping and Package

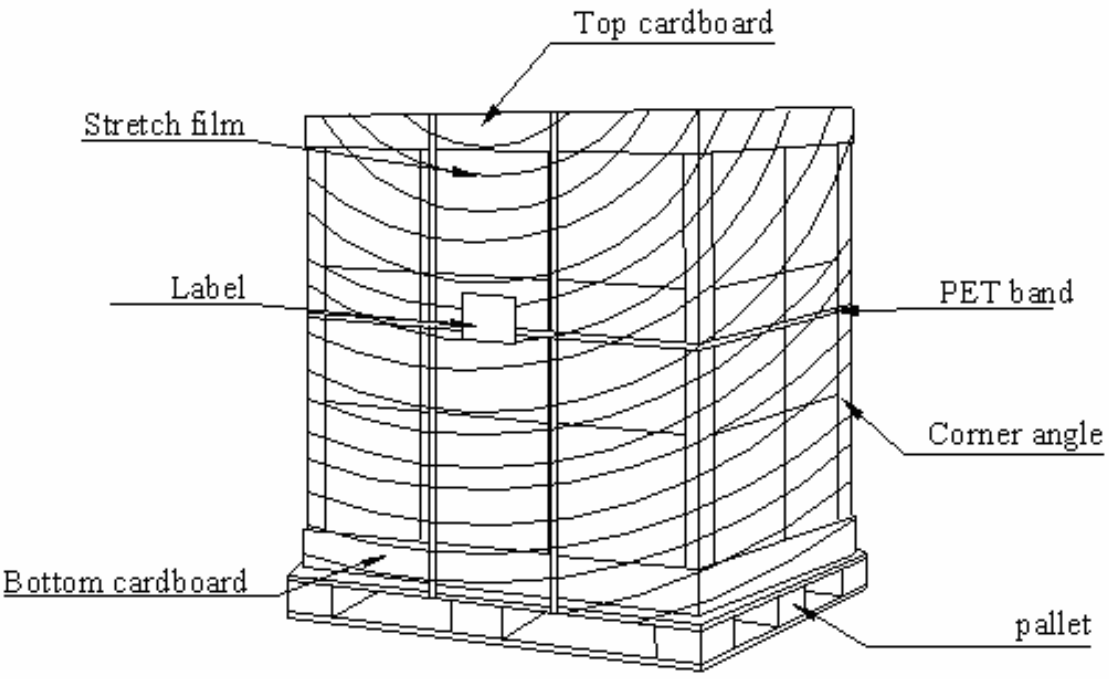
11.1 Shipping Label Format

11.2 Carton package

The outside dimension of carton is 469 (L)mm x 369 (W)mm x 328 (H)mm



11.3 Shipping package of palletizing sequence



12. Appendix: EDID description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	BE	10111110	190	
0B	hex, LSB first	10	00010000	16	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	01	00000001	1	
11	Year of manufacture	12	00010010	18	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	03	00000011	3	
14	**Video input def. (digital I/P, non-TMDS, CRGB)**	80	10000000	128	
15	**Max H image size (rounded to cm)**	24	00100100	36	
16	**Max V image size (rounded to cm)**	14	00010100	20	
17	**Display Gamma (=(gamma*100)-100)**	78	01111000	120	
18	**Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)**	0A	00001010	10	
19	Red/green low bits (Lower 2:2:2:2 bits)	AA	10101010	170	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	15	00010101	21	
1B	Red x (Upper 8 bits)	A6	10100110	166	
1C	Red y/ highER 8 bits	56	01010110	86	
1D	Green x	48	01001000	72	
1E	Green y	9C	10011100	156	
1F	Blue x	25	00100101	37	
20	Blue y	0D	00001101	13	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	

26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	68	01101000	104	
37	Pixel Clock/10000 USB	29	00101001	41	
38	Horz active Lower 8bits	40	01000000	64	
39	Horz blanking Lower 8bits	4A	01001010	74	
3A	HorzAct:HorzBlnk Upper 4:4 bits	61	01100001	97	
3B	Vertical Active Lower 8bits	84	10000100	132	
3C	Vertical Blanking Lower 8bits	0C	00001100	12	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	00110000	48	
3E	HorzSync. Offset	40	01000000	64	
3F	HorzSync.Width	2A	00101010	42	
40	VertSync.Offset : VertSync.Width	33	00110011	51	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
42	Horizontal Image Size Lower 8bits	6A	01101010	106	
43	Vertical Image Size Lower 8bits	CB	11001011	203	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16	
45	Horizontal Border (zero for internal LCD)	00	00000000	0	
46	Vertical Border (zero for internal LCD)	00	00000000	0	
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	

50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	36	00110110	54	6
74	Manufacture P/N	34	00110100	52	4
75	Manufacture P/N	52	01010010	82	R
76	Manufacture P/N	57	01010111	87	W
77	Manufacture P/N	30	00110000	48	0
78	Manufacture P/N	31	00110001	49	1
79	Manufacture P/N	20	00100000	32	
7A	Manufacture P/N	56	01010110	86	V

7B	Manufacture P/N	30	00110000	48	0
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	86	10000110	134	