## () Preliminary Specification(V) Final Specification

Module	32.0" Color TFT-LCD
Model Name	M320QAN01.2

Customer Date	Approved by	Date
Approved by	Prepared by	Date
<b>\</b>		Apr. 25, 2016
Note: This Specification is subject to change without notice.	AU Optronics	s corporation

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## **Record of Revision**



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Versio n	Date	Page	Old description New Description		Remark
0.1	2015/12/2	All	First version release	-	
0.2	2016/01/19	14	Connector PN :187034-3009	Connector PN :187034-4112	
0.3	2016/04/19	14	Connector PN :187034-4112	Connector PN :187060-4122	
0.3	2016/04/19	22	Symbols   Description:   Him.   Typ.:   Hins.   Unit:   Remark:	Symbol   Description   Plin.   Typ.   Hes.   Unit   Remark	
0.3	2016/04/19	22	old note : Note 3-4	add new note : Note 3-5,Note 3-6,Note 3-7	
0.3	2016/04/21	7	Ref	R <sub>c</sub>	
0.3	2016/04/25	5	Weight = 3950	Weight = 3900	
0.3	2016/04/25	34			



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#### 1 Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case a TFT-LCD Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lightbar edge. Otherwise the TFT-LCD Module may be damaged.
- 10) Insert or pull out the interface connector, be sure not to rotate nor tilt it of the TFT-LCD Module.
- 11) Do not twist nor bend the TFT -LCD Module even momentary. It should be taken into consideration that no bending/twisting forces are applied to the TFT-LCD Module from outside. Otherwise the TFT-LCD Module may be damaged.
- 12) Please avoid touching COF position while you are doing mechanical design.
- 13) When storing modules as spares for a long time, the following precaution is necessary: Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5 and 35 at normal humidity.



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### **2 General Description**

This specification applies to the 32.0 inch wide Color a-Si TFT-LCD Module M320QAN01.2. The display supports the UHD - 3840(H) x 2160(V) screen format and 1.07B colors (10bits data input). The input interface is 8-lanes eDP and this module doesn't contain an driver board for backlight.

### 2.1 Display Characteristics

The following items are characteristics summary on the table under 25 \, condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	812.8 (32.0")
Active Area	[mm]	708.48 (H) x 398.52 (V)
Pixels H x V	-	3840(x3) x 2160
Pixel Pitch	[um]	184.5 (per one triad) × 184.5
Pixel Arrangement	-	R.G.B. Vertical Stripe
Display Mode	-	Normally Black
White Luminance ( Center )	[cd/m²]	300 (Typ.)
Contrast Ratio	-	1000 (Typ.)
Response Time	[msec]	12 (Typ., Gray to Gray)
Power Consumption (LCD Module + Backligh unit)	[Watt]	53W (Typ.) LCD module : PDD(Typ.)=10.8W @white pattern, 60Hz, 12V Backlight unit : PBLU (Typ.) =42.2W @ls=100mA
Weight	[Grams	3,900
Outline Dimension	[mm]	721.88 (H) x 417.93 (V) × 16.37 (D) Typ.
Electrical Interface	-	8-lanes eDP , 10bits RGB data input
Support Color	-	1.07B colors
Surface Treatment	-	Anti-Glare, 3H
Temperature Range Operating Storage (Shipping)	[°C]	0 to +50 -20 to +60
RoHS Compliance	-	RoHS Compliance
TCO Compliance	-	TCO 7.0 Compliance

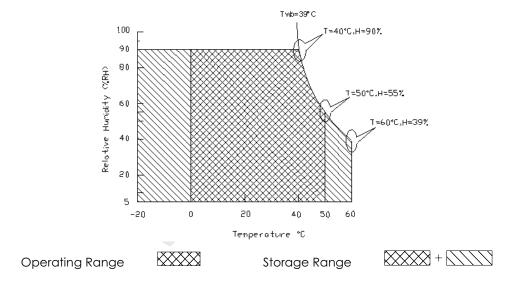
### 2.2 Absolute Maximum Rating of Environment

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	Note 2-1
TGS	Glass surface temperature	0	+68	[°C]	Note 2-1 Function judged
HOP	Operation Humidity	5	90	[%RH]	Note 2-1
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-1: Temperature and relative humidity range are shown as the below figure.

- 1. 90% RH Max ( Ta  $\leq$ 39°C)
- 2. Max wet-bulb temperature at 39°C or less. (Ta  $\leq$  39°C)
- 3. No condensation





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### 2.3 Optical Characteristics

The optical characteristics are measured on the following test condition.

### **Test Condition:**

1. Equipment setup: Please refer to Note 2-2.

2. Panel Lighting time: 30 minutes

3. VDD=12.0V, Fv=60Hz, Is=100mA, Ta=25□

Symbol	Description		Min.	Тур.	Max.	Unit	Remark
L <sub>w</sub>	White Luminance (Center of screen)		240	300	-	[cd/m2]	<b>Note 2-2</b> By SR-3
L <sub>uni</sub>	Luminance Uniformity	(9 points)	75	80	-	[%]	<b>Note</b> <b>2-3</b> By SR-3
CR	Contrast Ratio (Center	of screen)	600	1000	-	-	<b>Note 2-4</b> By SR-3
$\theta_{R}$	Horizontal Viewing Angle	Right	75	89	-		
$\Theta_{L}$	(CR=5)	Left	75	89	-	[degree	Note 2-5
Фн	Vertical Viewing Angle	Up	75	89	-	]	2-3 By SR-3
ФL	(CR=5)	Down	75	89	-		Бу 3К-3
T <sub>GTG</sub>	Response Time	Gray to Gray	-	12	-	[msec]	<b>Note 2-6</b> By TRD-100
R <sub>x</sub>		Red x	0.655	0.685	0.715		
R <sub>y</sub>		Red y	0.279	0.309	0.339	-	
G <sub>x</sub>		Green x	0.180	0.210	0.340		
Gy	Color Coordinates	Green y	0.680	0.710	0.740	-	By SR-3
B <sub>x</sub>	(CIE 1931)	Blue x	0.120	0.150	0.180		b) on o
Ву		Blue y	0.030	0.060	0.090		
W <sub>x</sub>		White x	0.283	0.313	0.343		
Wy		White y	0.299	0.329	0.359		
	Adobe RGB coverage ro	atio		100		[%]	By SR-3
СТ	Crosstalk		-	-	1.5	[%]	<b>Note 2-7</b> By SR-3



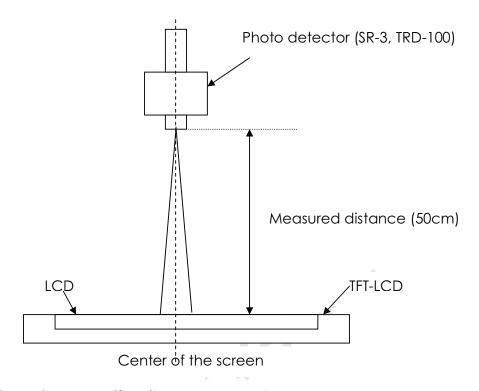
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						Note
F <sub>dB</sub>	Flicker (Center of screen)	-	-	-20	[dB]	2-8
						By SR-3



### Note 2-2: Equipment setup:

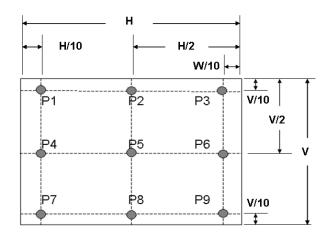


Note 2-3: Luminance Uniformity Measurement

### **Definition:**

 $Luminance\ Uniformity = \frac{Minimum\ Luminance\ of\ 9\ Points\ (P1 \sim P9)}{Maximum\ Luminance\ of\ 9\ Points\ (P1 \sim P9)}$ 

a. Test pattern: White Pattern





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Note 2-4: Contrast Ratio Measurement

### **Definition:**

Contrast Ratio = Luminance of White pattern

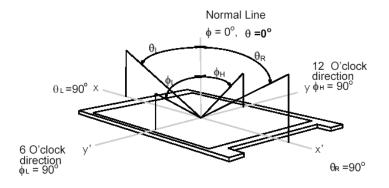
Luminance of Black pattern

a. Measured position: Center of screen (P5) & perpendicular to the screen ( $\theta$ = $\Phi$ =0°)

### Note 2-5: Viewing angle measurement

**Definition:** The angle at which the contrast ratio is greater than 10 & 5.

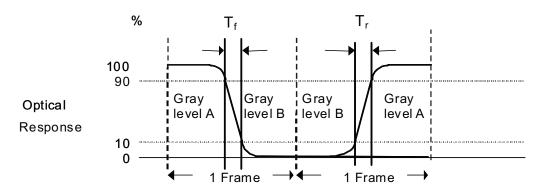
a. Horizontal view angle: Divide to left & right ( $\theta_L \& \theta_R$ ) Vertical view angle: Divide to up & down ( $\Phi_H \& \Phi_L$ )



**Note 2-6:** Response measurement

time

The output signals of photo detector are measured when the input signals are changed from "Gray level A" to "Gray level B" (falling time,  $T_f$ ), and from "Gray level B" to "Gray level A" (rising time,  $T_r$ ), respectively. The response time is interval between the 10% and 90% of optical response.



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The gray to gray response time is defined as the following table.

Cray Loyal to Cray Loyal		Target gray level					
Glay Level 10 (	Gray Level to Gray Level		L255	L511	L767	L1023	
	LO					-	
	L255						
Start gray level	L511						
	L767						
	L1023						

■ T<sub>GTG\_typ</sub> is the total average time at rising time and falling time of gray to gray.

### Note 2-7: Crosstalk measurement

#### **Definition:**

 $CT = Max. (CT_H, CT_V);$ 

#### Where

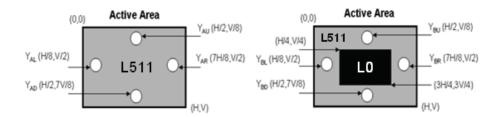
a. Maximum Horizontal Crosstalk:

$$CT_H = Max. (| Y_{BL} - Y_{AL} | / Y_{AL} \times 100 \%, | Y_{BR} - Y_{AR} | / Y_{AR} \times 100 \%);$$

Maximum Vertical Crosstalk:

$$CT_V = Max. (| Y_{BU} - Y_{AU} | / Y_{AU} \times 100 \%, | Y_{BD} - Y_{AD} | / Y_{AD} \times 100 \%);$$

b.  $Y_{AU}$ ,  $Y_{AD}$ ,  $Y_{AL}$ ,  $Y_{AR}$  = Luminance of measured location without Black pattern  $Y_{BU}$ ,  $Y_{BD}$ ,  $Y_{BL}$ ,  $Y_{BR}$  = Luminance of measured location with Black pattern



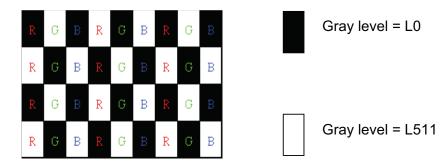


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### Note 2-8: Flicker measurement

a. Test pattern: It is listed as following.



R: Red, G: Green, B:Blue

b. Measured position: Center of screen (P5) & perpendicular to the screen ( $\theta$ = $\Phi$ = $0^{\circ}$ )

#### 2.4 Mechanical Characteristics

Symbol	Description	Min.	Max.	Unit	Remark
P <sub>bc</sub>	Backside Compression	2.5	-	[Kgf]	Note 2-9

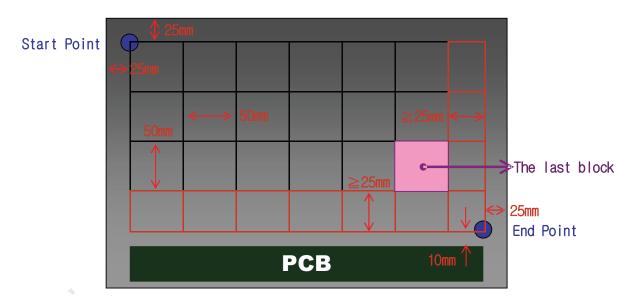
### Note 2-9: a. Test Method:

The point is at a distance from right-downside 25mm x 25mm defined as the Start Point of Measure Points, and the point is at a distance 25mm from left-side & around 10mm from PCB defined as the End Point.

Align 50mm x 50mm block from Start Point on the Bezel Back, and the corners of each block are Measure Points.

If the distance from the last block to each side of the End Point  $\geq$  25mm, add other blocks to make sure that most area of Bezel Back can be measured.

b. Test pattern: It is listed as following.



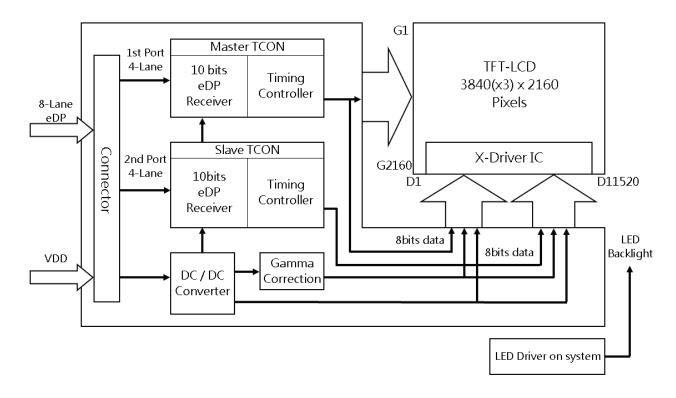
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### 3 TFT-LCD Module

### 3.1 Block Diagram

The following shows the block diagram of the 32.0 inch Color TFT-LCD Module.





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### 3.2 Interface Connection

3.2.1 Connector Type

TFT-LCD	Manufacturer	P-TWO	JAE	
Connector	Part Number	187060-4122	FI-RE41S-HF	
Mating	Manufacturer	JAE or compatible		
Connector	Part Number	FI-RE41CL		

### 3.2.2 Connector Pin Assignment

PIN#	Symbol	Description	Remark
1	1st Lane3_N	Negative eDP differential data input	
2	1st Lane3_P	Positive eDP differential data input	
3	GND	Ground	
4	1st Lane2_N	Negative eDP differential data input	
5	1st Lane2_P	Positive eDP differential data input	
6	GND	Ground	
7	1st Lane1_N	Negative eDP differential data input	
8	1st Lane1_P	Positive eDP differential data input	
9	GND	Ground	
10	1st Lane0_N	Negative eDP differential data input	
11	1st Lane0_P	Positive eDP differential data input	
12	GND	Ground	
13	1st AUX_CH_P	Positive AUX Channel differential data input	
14	1st AUX_CH_N	Negative AUX Channel differential data input	
15	1st HPD	Hot plug detection	
16	2nd Lane3_N	Negative eDP differential data input	
17	2nd Lane3_P	Positive eDP differential data input	
18	GND	Ground	
19	2nd Lane2_N	Negative eDP differential data input	
20	2nd Lane2_P	Positive eDP differential data input	

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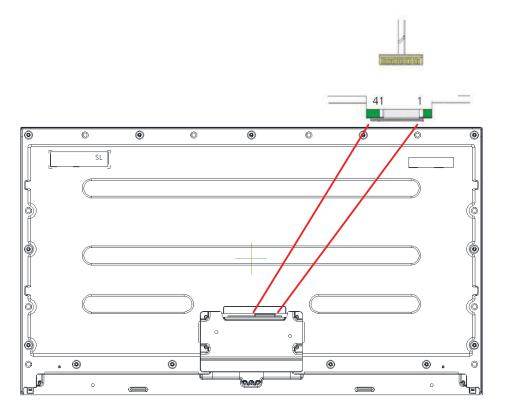
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21	GND	Ground
22	2nd Lane1_N	Negative eDP differential data input
23	2nd Lane1_P	Positive eDP differential data input
24	GND	Ground
25	2nd Lane0_N	Negative eDP differential data input
26	2nd Lane0_P	Positive eDP differential data input
27	GND	Ground
28	2nd AUX_CH_P	Positive AUX Channel differential data input
29	2nd AUX_CH_N	Negative AUX Channel differential data input
30	2nd HPD	Hot plug detection
31	NC	No connection (for AUO test only. Do not connect)
32	NC	No connection (for AUO test only. Do not connect)
33	NC	No connection (for AUO test only. Do not connect)
34	NC	No connection (for AUO test only. Do not connect)
35	GND	Ground
36	GND	Ground
37	GND	Ground
38	NC	No connection
39	VDD	Power +12V
40	VDD	Power +12V
41	VDD	Power +12V

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Note 3-1: Input signals of port 1 to port 4 clocks shall be the same timing.

### 3.3 Electrical Characteristics

### 3.3.1 Absolute Maximum Rating

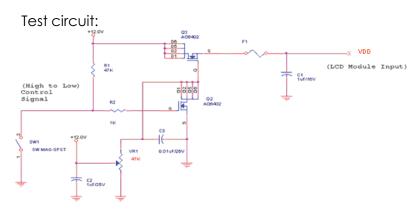
Permanent damage may occur if exceeding the following maximum rating.

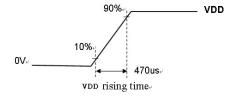
Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14	[Volt	Ta=25□

### 3.3.2 Recommended Operating Condition

Symbol	Description	Min	Тур	Max	Unit	Remark
VDD	Power supply Input voltage	10.8	12.0	13.2	[Volt]	
IDD	Power supply Input Current (RMS)	-	0.9	1.1	[A]	VDD= 12.0V, White pattern, Fv=60Hz
PDD	VDD Power Consumption	-	10.8	13.2	[Watt]	VDD= 12.0V , White pattern, Fv=60Hz
IRush	Inrush Current	-	-	3	[A]	Note 3-2
VDDrp	Allowable VDD Ripple Voltage	-	-	VDD*5%	[mV]	VDD= 12.0V, White pattern, Fv=60Hz

### Note 3-2: Inrush Current measurement:





The duration of VDD rising time: 470us.



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### 3.4 Signal Characteristics

### 3.4.1 LCD Pixel Format

Following figure shows the relationship between the input signals and LCD pixel format.

	1	st	Lar ↓	ie0	1s	t La	ne1	1	Lst 1	Lan ↓	ie2	1st	Lar ↓	ne3			192	20	2		Lan ↓ 921	ie0		l La: ↓ 1922			d La ↓ 192	me2		d La ↓ 1924				3840	
1	Г	, T	C.	D	ъ	T <sub>C</sub>	Тъ	Т	Т	3 G ]	D	D	- -	ъ	_	 $\overline{}$	_	_	T	$\overline{}$	$\overline{}$	D			_		_	$\overline{}$	_		_		_		
	R	8.1		В	R		В		R		В	K		В		 R		B		R		В	R	· · · · ·	B	R		В	R	· · · · ·	IB		R		В
↓	l																		l																
2160	R	2	G	В	R	G	В	I	R	G	В	R	G	В		 R	G	В	I	R	G	В	R	G	В	R	G	В	R	G	В		R	G	В

Note 3-3: The module use 8-Lanes eDP interface.

1<sup>st</sup> port:

1st Lane0: 1+4n pixel 1st Lane1: 2+4n pixel 1st Lane2: 3+4n pixel 1st Lane3: 4+4n pixel

2<sup>nd</sup> port:

2<sup>nd</sup> Lane0: 1921+4n pixel 2<sup>nd</sup> Lane1: 1922+4n pixel 2<sup>nd</sup> Lane2: 1923+4n pixel 2<sup>nd</sup> Lane3: 1924+4n pixel

n=0~479



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### 3.4.2 eDP Data Format

1st Lane0	lst Lanel	1st Lane2	1st Lane3			
R1-9:2	R2-9:2	R3-9:2	R4-9:2			
R1-1:0IG1-9:4	R2-1:0IG2-9:4	R3-1:0IG3-9:4	R4-1:0lG4-9:4			
G1-3:0IB1-9:6	G2-3:0IB2-9:6	G3-3:0IB3-9:6	G4-3:0IB4-9:6			
B1-5:0IR5-9:8	B2-5:0IR6-9:8	B3-5:0IR7-9:8	B4-5:0IR8-9:8			
R5-7:0	R6-7:0	R7-7:0	R8-7:0			
G5-9:2	G6-9:2	G7-9:2	G8-9:2			
GS-1:0IBS-9:4	G6-1:0IB6-9:4	G7-1:0IB7-9:4	G8-1:0IB8-9:4			
B5-3:0IR9-9:6	B6-3:0IR10-9:6	B7-3:0IR11-9:6	B8-3:0IR12-9:6			
R9-5:01G9-9:8	R10-5:0IG10-9:8	R11-5:0IG11-9:8	R12-5:0IG12-9:8			
G9-7:0	G10-7:0	G11-7:0	G12-7:0			
B9-9:2	B10-9:2	B11-9:2	B12-9:2			
B9-1:0IR13-9:4	B10-1:0IR14-9:4	B11-1:0IR15-9:4	B12-1:0IR16-9:4			
R13-3:0IG13-9:6	R14-3:0IG14-9:6	R15-3:0IG15-9:6	R16-3:0IG16-9:6			
G13-5:0IB13-9:8	G14-5:0IB14-9:8	G15-5:0IB15-9:8	G16-5:0IB16-9:8			
B13-7:0	B14-7:0	B15-7:0	B16-7:0			
		l .				

2nd Lane0	2nd Lanel	2nd Lane2	2nd Lane3
R1921-9:2	R1922-9:2	R1923-9:2	R1924-9:2
R1921-1:0IG1921-9:4	R1922-1:0IG1922-9:4	R1923-1:0IG1923-9:4	R1924-1:0lG1924-9:4
G1921-3:0IB1921-9:6	G1922-3:0IB1922-9:6	G1923-3:0IB1923-9:6	G1924-3:0IB1924-9:6
B1921-5:0IR1925-9:8	B1922-5:0IR1926-9:8	B1923-5:0IR1927-9:8	B1924-5:0IR1928-9:8
R1925-7:0	R1926-7:0	R1927-7:0	R1928-7:0
G1925-9:2	G1926-9:2	G1927-9:2	G1928-9:2
G1925-1:0IB1925-9:4	G1926-1:0IB1926-9:4	G1927-1:0IB1927-9:4	G1928-1:0IB1928-9:4
B1925-3:0IR1929-9:6	B1926-3:0IR1930-9:6	B1927-3:0IR1931-9:6	B1928-3:0IR1932-9:6
R1929-5:0IG1929-9:8	R1930-5:0IG1930-9:8	R1931-5:0IG1931-9:8	R1932-5:0IG1932-9:8
G1929-7:0	G1930-7:0	G1931-7:0	G1932-7:0
B1929-9:2	B1930-9:2	B1931-9:2	B1932-9:2
B1929-1:0IR1933-9:4	B1930-1:0IR1934-9:4	B1931-1:0IR1935-9:4	B1932-1:0IR1936-9:4
R1933-3:0IG1933-9:6	R1934-3:0IG1934-9:6	R1935-3:0IG1935-9:6	R1936-3:0IG1936-9:6
G1933-5:0IB1933-9:8	G1934-5:0IB1934-9:8	G1935-5:0IB1935-9:8	G1936-5:0IB1936-9:8
B1933-7:0	B1934-7:0	B1935-7:0	B1936-7:0

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### 3.4.3 Color versus Input Data

The following table is for color versus input data (10bit). The higher the gray level, the brighter the color.

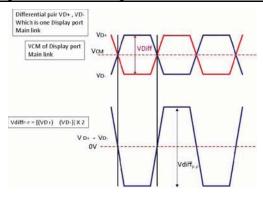
															Col	or In	out C	)ata														
Color	Gary Level					RED B:R9										REEI B:G9									E (MS	B:B9						Remark
		R9	R8	R7	R6	R5	R4	R3	R2	R1	RO	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	В9	В8	В7	В6	В5	В4	ВЗ	В2	В1	ВО	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
L511	-	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	
	LO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
Red	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L1023	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	LO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
Green	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L1023	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
	LO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
Blue	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L1023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	



### 3.4.4 eDP Specification (Follow as VESA DisplayPort Standard Version 1.2)

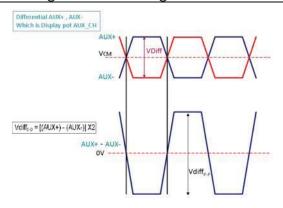
### a. DisplayPort main link signal:

	DisplayPort main link				
		Min	Тур	Max	unit
VCM	RX input DC Common Mode Voltage	-	0	<b>/</b> -	٧
VDiff <sub>P-P</sub>	Peak-to-peak Voltage at a receiving Device	120	- *	-	mV



### b. DisplayPort AUX\_CH signal:

	DisplayPort AUX CH				
	, , =	Min	Тур	Max	unit
VCM	AUX DC Common Mode Voltage		0.5		٧
VDiff <sub>P-P</sub>	AUX Peak-to-peak voltage at a receiving device	0.32	0.6	1.32	٧



### c. DisplayPort VHPD signal:

	DisplayPort VHPD				
		Min	Тур	Max	unit
VHPD	HPD Voltage	2.25	-	3.6	V

### 3.4.5 Input Timing Specification

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The input timing is shown as the following table.

Symbol	Descri	ption	Min.	Тур.	Max.	Unit	Remark
Tv		Period	2180	2200	5260	Th	
Tdisp (v)	Vertical	Active	2160	2160	2160	Th	
Tblk (v)	Section	Blanking	20	40	3100	Th	
Fv		Frequency	29	60	65	Hz	Note 3-6
							Note 3-7
Th		Period	2026	2100	2300	Tclk	
Tdisp (h)	Horizontal	Active	1920	1920	1920	Tclk	
Tblk (h)	Section	Blanking	106	180	380	Tclk	
Fh		Frequency	109	132.00	142.20	kHz	Note 3-4
Tclk	Pixel Clock	Period	4.53	3.61	3.47	ns	1/Fclk
Fclk	010 OK	Frequency	220.83	277.20	288.00	MHz	Note 3-5
	Link Rate per La	ne		2.7		Gbps	

Note 3-4: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = Fclk (Min.) / Th (Min.)

Fh (Typ.) = Fclk (Typ.) / Th (Typ.)

Fh (Max.)= Fclk (Max.) / Th (Min.)

Note 3-5: The equation is listed as following. Please don't exceed the above recommended value.

1st Lane N & 2nd Lane N skew < 200ns

Fclk (Typ.) = Fv (Typ.) x Th (Typ.) x Tv (Typ.)

Fclk (Min.) $\leq$ Fv x Th x Tv  $\leq$  Fclk (Max.)

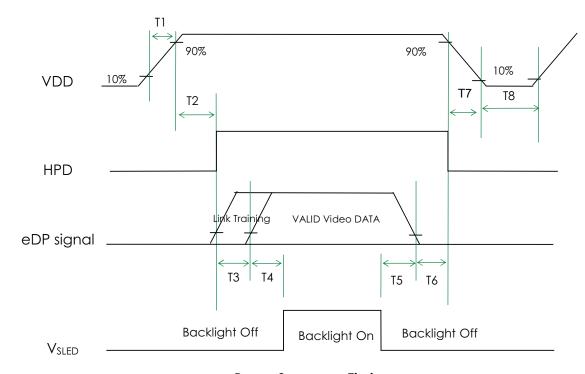
Note 3-6: The equation is listed as following. Please don't exceed the above recommended value.

Fv = Fclk(Typ.) / (Tv x Th)

*Note 3-7:* The optimal Vertical Frequency is 50~65 Hz for best picture quality.

### 3.5 Power ON/OFF Sequence

VDD power,eDP signal and backlight on/off sequence are as following. eDP signals from any system tshall be Hi-Z state when VDD is off.



### **Power Sequence Timing**

Symbol		Value		11	Remark
Symbol	Min.	Тур.	Max.	Unit	
T1	0.5	-	10	[ms]	
T2	0	-	200	[ms]	
Т3	0	-	-	[ms]	Note 3-5
T4	500	-	-	[ms]	
T5	100		-	[ms]	
T6	0	-	50	[ms]	Note 3-6 Note 3-7
Т7	0		200	[ms]	Note 3-8
Т8	1000	-	-	[ms]	

Note 3-5: During T3 period, eDP link training time by customer's system.

**Note 3-6:** Recommend setting T6 = 0ms to avoid electronic noise when VDD is off.

Note 3-7: During T6 period, please keep the level of input eDP signals with Hi-Z state.

Note 3-8: Voltage of VDD must decay smoothly after power-off.(customer system decide this value)



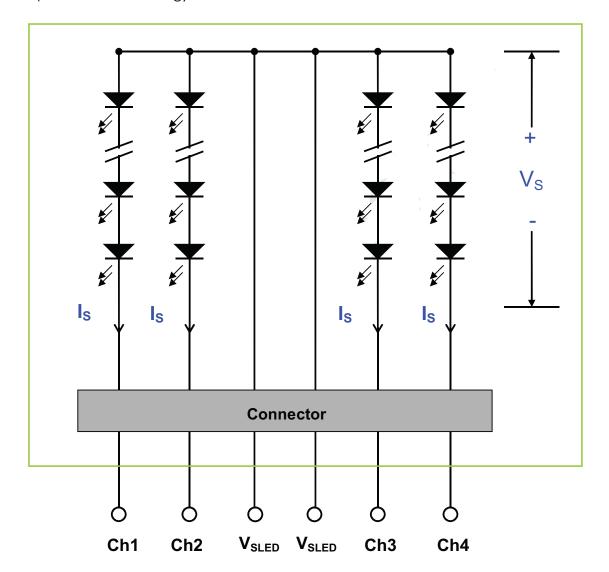
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### 4 Backlight Unit

### 4.1 Block Diagram

The following shows the block diagram of the 32.0 inch Backlight Unit. And it includes 2 pcs LED light bar in Backlight Unit. Each LED light bar includes 68 pcs LED package. (4 strings and 17 pcs LED of one string).



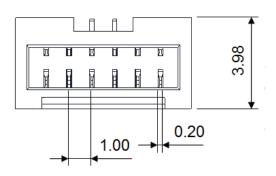
### **4.2 Interface Connection**

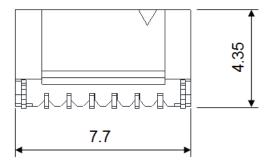
### 4.2.1 Connector Type

Backlight Connector	Manufacturer	Cvilux
	Part Number	CI1406M1VLD-NH
	Manufacturer	ENTERY
Mating Connector	Part Number	H112K-P06N-00B (Non-Locking type) H112K-P06N-11B(White) (Locking type) H112K-P06N-13B(Black) (Locking type)

### **Backlight Connector dimension:**

 $H \times V \times D = 13.9 \times 3.00 \times 4.25$ , Pitch = 1.0(unit = mm)



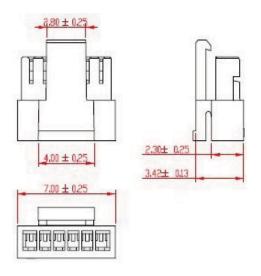


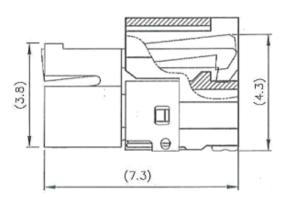


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### **Mating Connector dimension:**





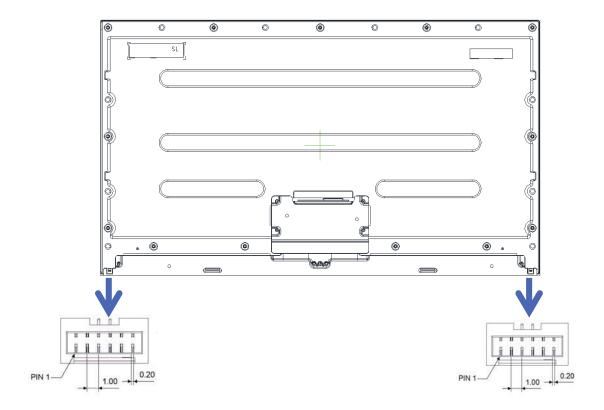


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### 4.2.2 Connector Pin Assignment

Pin#	Symbol	Description	Remark
1	Ch1	LED Current Feedback Terminal (Channel 1)	
2	Ch2	LED Current Feedback Terminal (Channel 2)	
3	$V_{SLED}$	LED Power Supply Voltage Input Terminal	
4	$V_{SLED}$	LED Power Supply Voltage Input Terminal	
5	Ch3	LED Current Feedback Terminal (Channel 3)	
6	Ch4	LED Current Feedback Terminal (Channel 4)	





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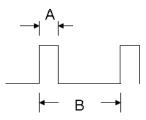
### 4.3 Electrical Characteristics

### 4.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

(Ta=25□)

Symbol	Description	Min	Max	Unit	Remark
		0	150	[mA]	100% duty ratio
ls	LED String Current		300	[mA]	Duty ratio□ 10% Pulse time=10 ms



Duty ratio= (A / B) X 100%; (A: Pulse time, B: Period)

### 4.3.2 Recommended Operating Condition

(Ta=25□)

Symbol	Description	Min.	Тур.	Max.	Unit	Remark
Is	LED String Current	-	100	110	[mA]	100% duty ratio of LED chip <b>Note 4-6</b>
Vs	LED String Voltage	47.6	52.7	57.8	[Volt]	Is=100mA @ 100% duty ratio; <b>Note 4-1&amp; Note</b> <b>4-5</b>
ΔVs	Maximum Vs Voltage Deviation of light bar	-	-	3.4	[Volt]	ls=100mA @ 100% duty ratio; <b>Note 4-2</b>
P <sub>BLU</sub>	LED Light Bar Power Consumption	-	42.2	46.2	[Watt]	Note 4-3
LT <sub>LED</sub>	LED Life Time	30,000	-	-	[Hour]	Note 4-4
OVP	Over Voltage Protection in system board	110% Vs (max)	-	-	[Volt]	Note 4-5

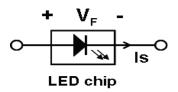
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- **Note 4-1:** Vs (Typ.) =  $V_F$  (Typ.) X LED No. (one string);
  - a. V<sub>F</sub>: LED chip forward voltage, V<sub>F</sub> (Min.)=2.8V, V<sub>F</sub>(Typ.)=3.1V, V<sub>F</sub>(Max.)=3.4V
  - b. The same eugation to calculate Vs(Min.) & Vs (Max.) for respective V<sub>F</sub> (Min.)
  - &  $V_F(Max.)$ ;



- **Note 4-2:**  $\Delta Vs$  (Max.) =  $\Delta V_F X$  LED No. (one string);
  - a.  $\Delta V_{F:}$  LED chip forward voltage deviation (0.2V, each Bin of LED  $V_F$ )
- Note 4-3:  $P_{BLU}$  (Typ.) = Vs (Typ.) X Is (Typ.) X 8 (8 is total String No. of BLU)  $P_{BLU}$  (Max.) = Vs (Max.) X Is (Typ.) X 8
- Note 4-4: Definition of life time:
  - a. Brightness of LED becomes to 50% of its original value
  - b. Test condition: Is = 100mA and 25□ (Room Temperature)
- **Note 4-5:** Recommendation for LED driver power design:

Due to there are electrical property deviation in LED & monitor set system component after long time operation. AUO strongly recommend the design value of LED driver board OVP (over voltage protection) should be 10% higher than max. value of LED string voltage (Vs) at least.

**Note 4-6:** AUO strongly recommend "Analog Dimming" method for backlight brightness control for Wavy Noise Free. Otherwise, recommend that Dimming Control Signal (PWM Signal) should be synchronized with Frame Frequency



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### **5 Reliability Test**

AUO reliability test items are listed as following table. (Bare Panel only)

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50□, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50□, 50%RH, 300hours	
Low Temperature Operation	Ta= 0□, 300hours	
High Temperature Storage (HTS)	Ta= 60□, 300hours	
Low Temperature Storage (LTS)	Ta= -20□, 300hours	
Vibration Test (Non-operation)	Frequency:10~57Hz/Vibration width(one side):0.075mm : 58~500Hz/Acceleration:9.8 m/s2 Sweep time: 11minutes Test period: 3 hours(1h for each direction of X,Y,Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Thermal Shock Test (TST)	-20□/30min, 60□/30min, 100 cycles	Note 5-1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: $\pm$ 15KV, 150pF(330 $\Omega$ ) 1sec, 8 points, 25 times/ point.	Note 5-2
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	NOIE 3-2
Altitude Test	Operation:18,000 ft Non-Operation:40,000 ft	

- **Note 5-1**: a. A cycle of rapid temperature change consists of varying the temperature from -20 to 60 and back again. Power is not applied during the test.
  - b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.
- **Note 5-2**: EN61000-4-2, ESD class B: Certain performance degradation allowed No data lost Self-recoverable

No hardware failures.

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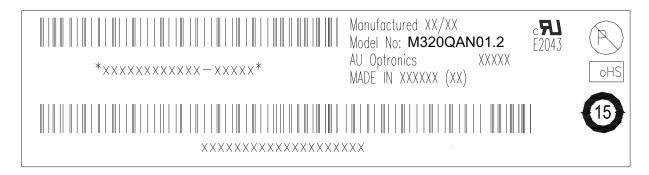


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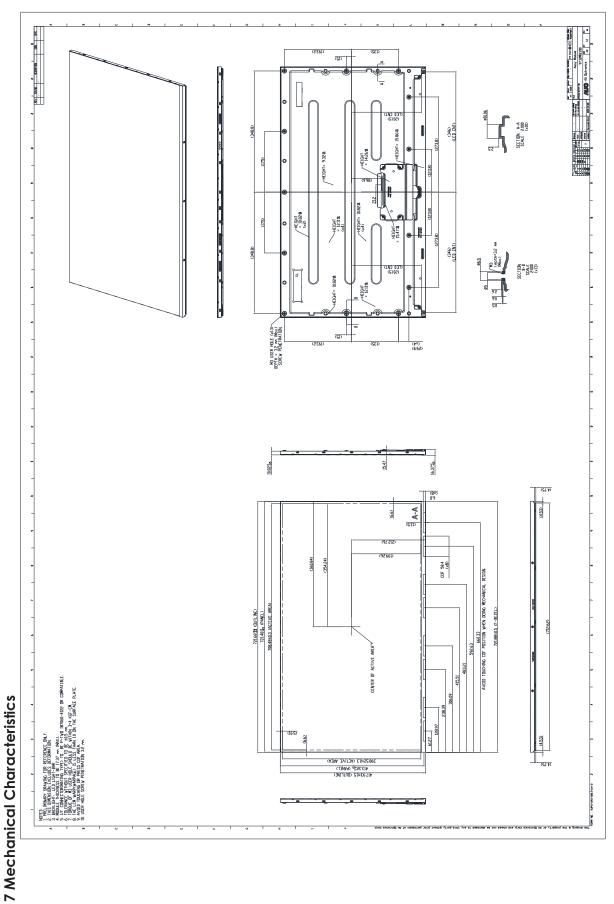
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### 6 Shipping Label

The label is on the panel as shown below:



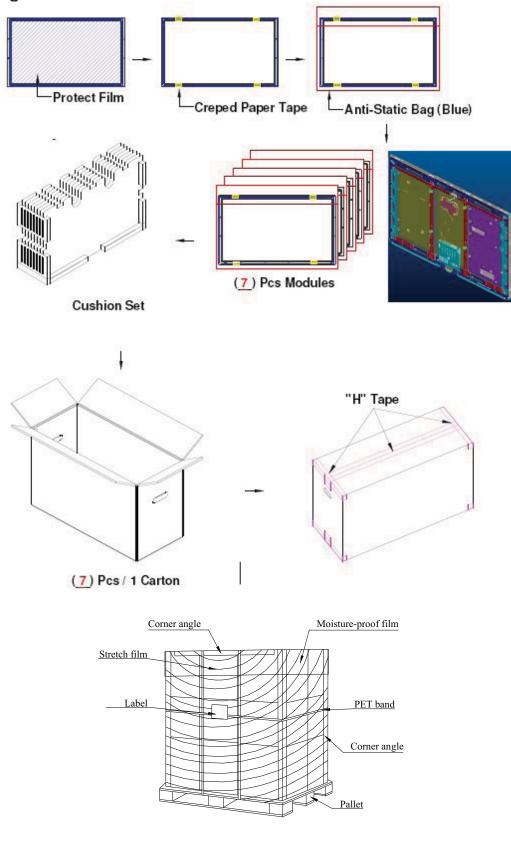
- Note 6-1: For Pb Free products, AUO will add 🕲 for identification.
- Note 6-2: For RoHS compatible products, AUO will add RoHS for identification.
- Note 6-3: For China RoHS compatible products, AUO will add 19 for identification.
- **Note 6-4:** The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.



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### **8 Packing Specification**

### 8.1 Packing Flow



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### 8.2 Pallet and shipment information

Item		D a ma and c		
nem	Q'ty	Dimension	Weight(kg)	Remark
Panel	1	721.88(H)mm x 417.93(V)mm x 16.37(D)mm	3.90	
Cushion	1	-		
Вох	1	805(L)mm x 280(W)mm x 512(H)mm	6.88	without Panel
Packing Box	7 pcs/Box	805(L)mm x 280(W)mm x 512(H)mm	34.53	with panel & cushion & Box
Pallet	1	1150(L)mm x 840(W)mm x 132(H)mm	13.8	
Pallet after Packing	8 boxes/pallet	1150(L)mm x 840(W)mm x 1156(H)mm	290.04	