

M170EG01 VB

AU OPTRONICS CORPORATION

(۷)	Preliminary	Specification
()	١	Final Specifi	ication

Module	17.0" SXGA Color TFT-LCD
Model Name	M170EG01 VB

Customer Date	Checked & Date Approved by
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Approved by	Prepared by
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Note: This Specification is subject to change without notice.	Desktop Display Business Group / AU Optronics corporation

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Record of Revision

Version & Date		Page	Old Description	New Description	Remark
0.1	.1 2005/10/05 All		First Edition for Customer		

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1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL reflector edge. Instead, press at the far ends of the CCFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit (IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

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2. General Description

M170EG01 VB is a Color Active Matrix Liquid Crystal Display composed of a TFT-LCD panel, a driver circuit, and backlight system. The screen format is intended to support the SXGA (1280(H) x 1024(V)) screen and 16.2M colors (RGB 6-bits + FRC data). All input signals are LVDS interface compatible. Inverter card of backlight is not included. M170EG01 VB is designed for a display unit of personal computer.

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2.1 Display Characteristics

The following items are characteristics summary on the table under 25 condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	432 (17.0")
Active Area	[mm]	337.920(H) × 270.336(V)
Pixels H x V		1280 × 3(RGB) × 1024
Pixel Pitch	[mm]	0.264(per one triad) × 0.264
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance	[cd/m ²]	300 (center,Typ)@7.5 mA
Contrast Ratio		500 : 1 (Typ)
Optical ResponseTime	[msec]	8 (Typ)
Nominal Input Voltage VDD	[Volt]	+5.0 (Typ)
Power Consumption	[Watt]	25.8 W (Typ) (PDD=6W, PCFL=19.8W @Lamp=7.5mA)
Weight	[Grams]	1900 (Typ)
Physical Size (H x V x D)	[mm]	358.5(H) x 296.5(V) x 17.0(D) (Typ)
Electrical Interface		Dual Channel LVDS
Surface Treatment		Anti-glare type, Hardness 3H
Support Color		16.2M colors (RGB 6-bits + FRC data)
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

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2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25 (Room Temperature):

Item	Unit	Cond	Conditions		Тур.	Max.	Note	
Viewing Angle	[dograp]	Horizontal CR = 10	(Right) (Left)	60 60	70 70	-	1	
Viewing Angle	[degree]	Vertical CR = 10	(Up) (Down)	60 50	70 60	-	1	
Luminance Uniformity	[%]	9 Points		75	80	-	2, 3	
		Rising		-	6	9		
Optical Response Time	[msec]	Falling		-	2	4	4, 6	
		Rising + Fall	-	8	13			
		Red x		0.61	0.64	0.67		
		Red y		0.31	0.34	0.37		
		Green x		0.26	0.29	0.32		
Color / Chromaticity		Green y Blue x Blue y White x		0.58	0.61	0.64	4	
Coordinates (CIE 1931)				0.11	0.14	0.17		
				0.04	0.07	0.10		
				0.28	0.31	0.34		
		White y		0.30	0.33	0.36		
White Luminance (At CCFL= 7.5mA)	[cd/m ²]			240	300	-	4	
Contrast Ratio				300	500	-	4	
Cross Talk (At 75Hz)	[%]			-	-	1.5	5	
Flicker	[dB]			-	-	-20	7	

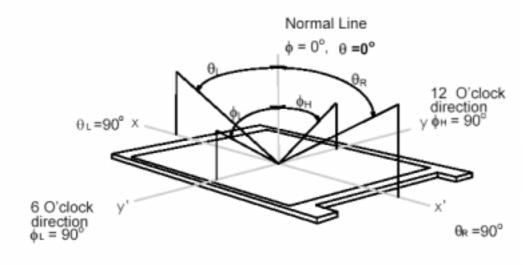
Optical Equipment: BM-5A, BM-7, PR880, or equivalent

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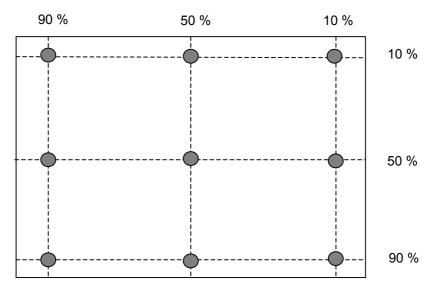


Note 1: Definition of viewing angle

Viewing angle is the measurement of contrast ratio 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° () horizontal left and right and 90° () vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



Note 2: 9 points position



Note 3: The luminance uniformity of 9 points is defined by dividing the maximum luminance values by the minimum test point luminance

W9 = Minimum Luminance of 9 points

Maximum Luminance of 9 points

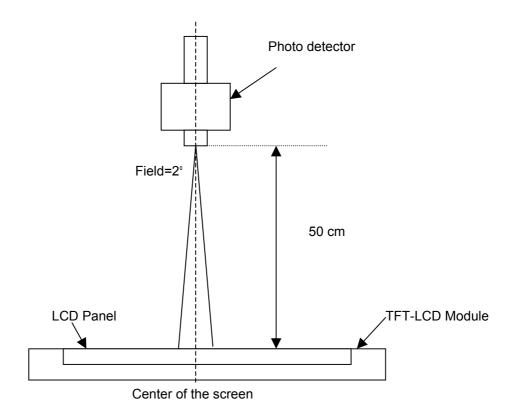
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Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.

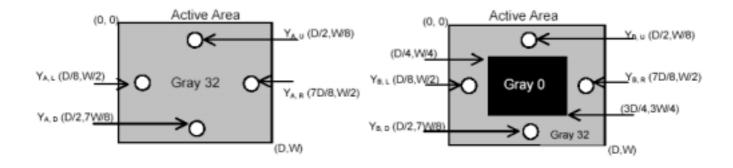


Note 5: Definition of Cross Talk (CT) $CT = |YB - YA|/YA \times 100 (\%)$

Where

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

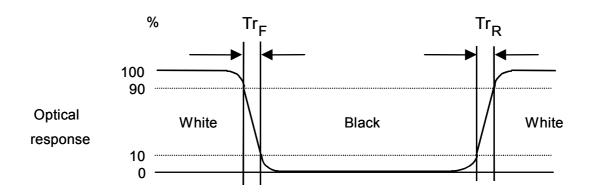
YB = Luminance of measured location with gray level 0 pattern (cd/m2)



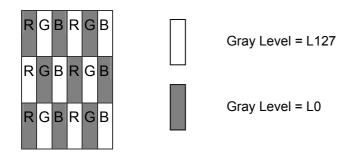
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Note 6: Definition of response time:

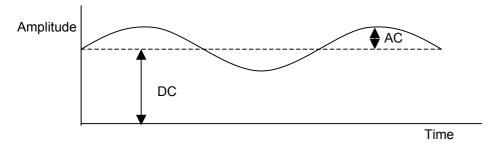
The output signals of photo detector are measured when the input signals are changed from "Full Black" to "Full White" (rising time), and from "Full White" to "Full Black" (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 7: Subchecker Pattern



Method: Record dBV & DC value with (WESTAR)TRD-100



Flicker (dB) =
$$20 \log \frac{AC \text{ Level(at 30 Hz)}}{DC \text{ Level}}$$

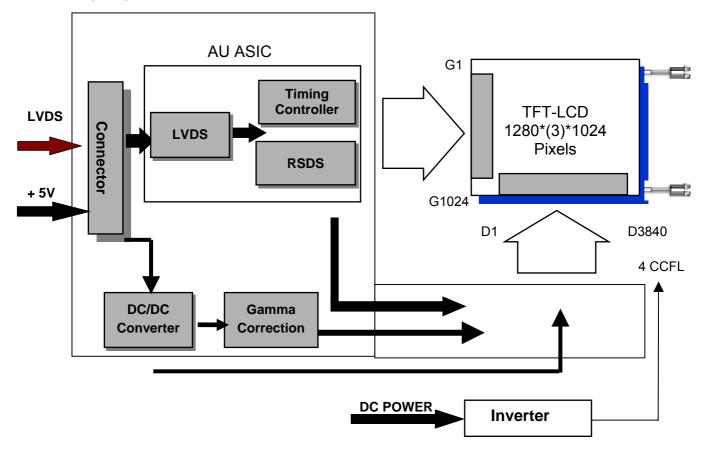
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3. Functional Block Diagram

The following diagram shows the functional block of the 17.0 inches Color TFT-LCD Module:



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4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min.	Max.	Unit	Conditions
Logic/LCD Drive	VDD	-0.3	+6	[Volt]	Note 1, 2
Voltage	۷۵۵	-0.5	10	[voit]	Note 1, 2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min.	Max.	Unit	Conditions
CCFL Current	ICFL	-	8.5	[mA] rms	Note 1, 2

4.3 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	
Operation Humidity	HOP	5	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	90	[%RH]	

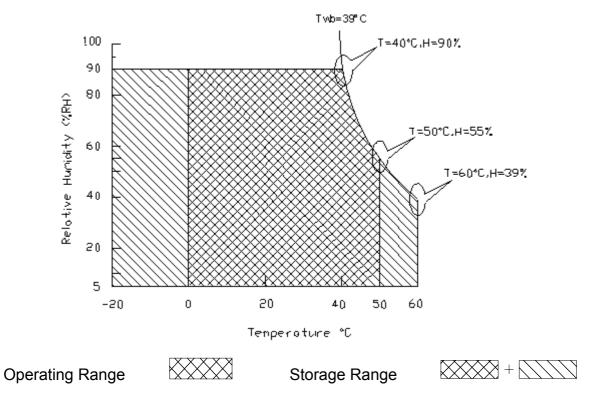
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Note 1: With in Ta= 25

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



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5. Electrical characteristics

5.1 TFT LCD Module

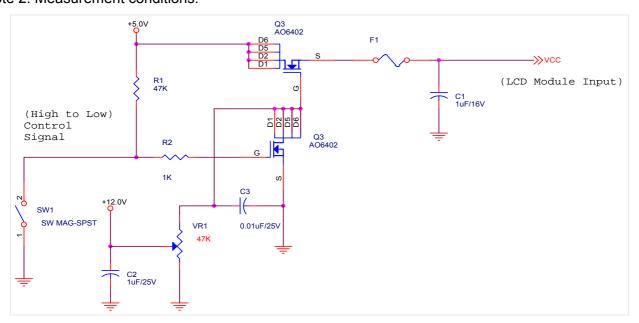
5.1.1 Power Specification

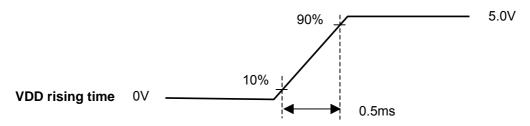
Input power specifications are as follows:

Symble	Parameter	Min.	Тур.	Max.	Unit	Condition
VDD	Logic/LCD Drive Voltage	4.5	5.0	5.5	[Volt]	Load Capacitance 20uF
IDD	Input Current	-	1.2	1.56	[A]	VDD= 5.0V, All Black Pattern At 75Hz
PDD	VDD Power	-	6	7.8	[Watt]	VDD= 5.0V, All Black Pattern At 75Hz , Note 1
IRush	Inrush Current	-	-	3.0	[A]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	VDD= 5.0V, All Black Pattern At 75Hz

Note 1: The variance of VDD power consumption is ±10%.

Note 2: Measurement conditions:





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5.2 Backlight Unit

Parameter guideline for CCFL Inverter is under stable conditions at 25 (Room Temperature):

Parameter	Min.	Тур.	Max.	Unit	Condition
CCFL Standard Current(ISCFL)	7.0	7.5	8.0	[mA] rms	Note 2
CCFL Operation Current(IRCFL)	3.0	7.5	8.0	[mA] rms	Note 2
CCFL Frequency(FCFL)	40	60	80	[KHz]	Note 3,4
CCFL Ignition Voltage(ViCFL, Ta= 0)	1500	-	-	[Volt] rms	Note 5
CCFL Ignition Voltage(ViCF, Ta= 25)	1150	-	-	[Volt] rms	Note 5
CCFL Operation Voltage (VCFL)	1	660 (@ 7.5mA)	700 (@ 3.0mA)	[Volt] rms	Note 6
CCFL Power Consumption(PCFL)	-	19.8	21.8	[Watt]	Note 6
CCFL Life Time(LTCFL)	40,000	50,000	-	[Hour]	

Note 1: Typ. are AUO recommended design points.

- *1 All of characteristics listed are measured under the condition using the AUO test inverter.
- *2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
- *3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CCFL is damaged.
- *4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
- *5 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.
- Note 2: It should be employed the inverter which has "Duty Dimming", if IRCFL is less than 4mA.
- Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.
- Note 4: The frequency range will not affect to lamp life and reliability characteristics.
- Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,500 voltage. Lamp units need 1,500 voltage minimum for ignition.
- Note 6: The variance of CCFL power consumption is ±10%. Calculator value for reference (ISCFL × VCFL × 4 = PCFL)

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6. Signal Characteristic

6.1 Pixel Format Image

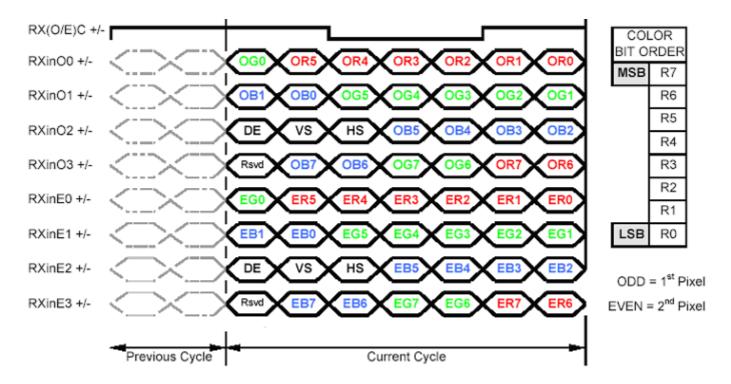
Following figure shows the relationship of the input signals and LCD pixel format.

		1		2			1:	27	9	12	280	Э
1st Line	R	G E	3 F	G	В		R	G	В	R	G	В
						•						
				•								
				•		•		•			•	
				•		•		•				
		'		•							•	
1024th Line	R	G E	3 F	G	В		R	G	В	R	G	В

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6.2 The Input Data Format



Note1: Normally, DE, VS, HS on EVEN channel are not used.

Note2: Please follow PSWG.

Note3: 8-bit in

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6.3 Signal Description

The module using a pair of LVDS receiver SN75LVDS82(Texas Instruments) or compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS83(negative edge sampling) or compatible. The first LVDS port(RxOxxx) transmits odd pixels

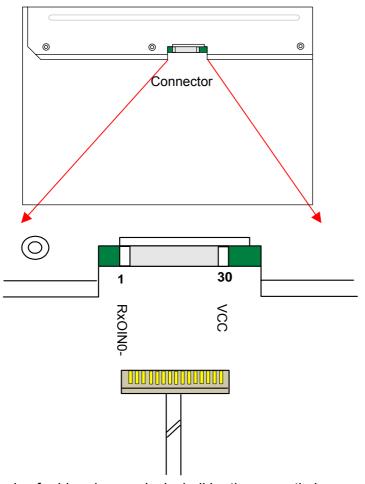
while the second LVDS port(RxExxx) transmits even pixels.

PIN # SIGNAL NAME	hile the	second LVDS p	port(RxExxx) transmits even pixels.
2 RXOIN0+ Positive LVDS differential data input (Odd data) 3 RXOIN1- Negative LVDS differential data input (Odd data) 4 RXOIN1+ Positive LVDS differential data input (Odd data) 5 RXOIN2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 6 RXOIN2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 7 VSS Power Ground 8 RXOCLKIN- Negative LVDS differential clock input (Odd clock) 9 RXOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RXOIN3- Negative LVDS differential data input (Odd data) 11 RXOIN3+ Positive LVDS differential data input (Odd data) 12 RXEIN0- Negative LVDS differential data input (Even data) 13 RXEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RXEIN1- Positive LVDS differential data input (Even data) 16 RXEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RXEIN2- Negative LVDS differential data input (Even data) 19 RXEIN2+ Positive LVDS differential data input (Even data) 20 RXECLKIN- Negative LVDS differential data input (Even data) 21 RXECLKIN- Negative LVDS differential data input (Even data) 22 RXEIN3- Negative LVDS differential data input (Even data) 23 RXEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	PIN#	SIGNAL NAME	DESCRIPTION
RXOIN1- Negative LVDS differential data input (Odd data) RXOIN2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) RXOIN2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) RXOIN2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) RXOCLKIN- Negative LVDS differential clock input (Odd clock) RXOCLKIN- Positive LVDS differential clock input (Odd clock) RXOIN3- Negative LVDS differential data input (Odd data) RXOIN3- Negative LVDS differential data input (Odd data) RXOIN3- Negative LVDS differential data input (Odd data) RXOIN3- Negative LVDS differential data input (Even data) RXEIN0- Negative LVDS differential data input (Even data) RXEIN0- Positive LVDS differential data input (Even data) RXEIN1- Positive LVDS differential data input (Even data) RXEIN1- Positive LVDS differential data input (Even data) RXEIN1- Negative LVDS differential data input (Even data) RXEIN2- Negative LVDS differential data input (Even data) RXEIN2- Negative LVDS differential data input (Even data) RXEIN2+ Positive LVDS differential clock input (Even clock) RXECLKIN- Negative LVDS differential clock input (Even clock) RXECLKIN- Positive LVDS differential data input (Even data) RXEIN3- Negative LVDS diff	1	RxOIN0-	Negative LVDS differential data input (Odd data)
4 RXOIN1+ Positive LVDS differential data input (Odd data) 5 RXOIN2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 6 RXOIN2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 7 VSS Power Ground 8 RXOCLKIN- Negative LVDS differential clock input (Odd clock) 9 RXOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RXOIN3- Negative LVDS differential data input (Odd data) 11 RXOIN3+ Positive LVDS differential data input (Odd data) 12 RXEIN0- Negative LVDS differential data input (Even data) 13 RXEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RXEIN1- Positive LVDS differential data input (Even data) 16 RXEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RXEIN2- Negative LVDS differential data input (Even data) 19 RXEIN2+ Positive LVDS differential data input (Even data) 20 RXECLKIN- Negative LVDS differential clock input (Even clock) 21 RXEIN3- Negative LVDS differential clock input (Even data) 22 RXEIN3- Negative LVDS differential data input (Even data) 23 RXEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	2	RxOIN0+	Positive LVDS differential data input (Odd data)
5 RxOIN2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 6 RxOIN2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 7 VSS Power Ground 8 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 9 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RxOIN3- Negative LVDS differential data input (Odd data) 11 RxOIN3+ Positive LVDS differential data input (Odd data) 12 RxEIN0- Negative LVDS differential data input (Even data) 13 RxEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Positive LVDS differential data input (Even data) 16 RxEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN- Positive LVDS differential clock input (Even data) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	3	RxOIN1-	Negative LVDS differential data input (Odd data)
6 RxOIN2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 7 VSS Power Ground 8 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 9 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RxOIN3- Negative LVDS differential data input (Odd data) 11 RxOIN3+ Positive LVDS differential data input (Odd data) 12 RxEIN0- Negative LVDS differential data input (Even data) 13 RxEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Positive LVDS differential data input (Even data) 16 RxEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN- Positive LVDS differential clock input (Even data) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3- Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	4	RxOIN1+	Positive LVDS differential data input (Odd data)
7 VSS Power Ground 8 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 9 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RxOIN3- Negative LVDS differential data input (Odd data) 11 RxOIN3+ Positive LVDS differential data input (Odd data) 12 RxEIN0- Negative LVDS differential data input (Even data) 13 RxEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Positive LVDS differential data input (Even data) 16 RxEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	5	RxOIN2-	Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
8 RXOCLKIN- Negative LVDS differential clock input (Odd clock) 9 RXOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RxOIN3- Negative LVDS differential data input (Odd data) 11 RXOIN3+ Positive LVDS differential data input (Odd data) 12 RXEIN0- Negative LVDS differential data input (Even data) 13 RXEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RXEIN1- Positive LVDS differential data input (Even data) 16 RXEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RXEIN2- Negative LVDS differential data input (Even data) 19 RXEIN2+ Positive LVDS differential data input (Even data) 20 RXECLKIN- Negative LVDS differential clock input (Even clock) 21 RXECLKIN+ Positive LVDS differential clock input (Even data) 22 RXEIN3- Negative LVDS differential data input (Even data) 23 RXEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	6	RxOIN2+	Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
9 RXOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RxOIN3- Negative LVDS differential data input (Odd data) 11 RXOIN3+ Positive LVDS differential data input (Odd data) 12 RXEIN0- Negative LVDS differential data input (Even data) 13 RXEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RXEIN1- Positive LVDS differential data input (Even data) 16 RXEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RXEIN2- Negative LVDS differential data input (Even data) 19 RXEIN2+ Positive LVDS differential data input (Even data) 20 RXECLKIN- Negative LVDS differential clock input (Even clock) 21 RXECLKIN+ Positive LVDS differential clock input (Even data) 22 RXEIN3- Negative LVDS differential data input (Even data) 23 RXEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	7	VSS	Power Ground
10 RxOIN3- Negative LVDS differential data input (Odd data) 11 RxOIN3+ Positive LVDS differential data input (Odd data) 12 RxEIN0- Negative LVDS differential data input (Even data) 13 RxEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Positive LVDS differential data input (Even data) 16 RxEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	8	RxOCLKIN-	Negative LVDS differential clock input (Odd clock)
11 RxOIN3+ Positive LVDS differential data input (Odd data) 12 RxEIN0- Negative LVDS differential data input (Even data) 13 RxEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Positive LVDS differential data input (Even data) 16 RxEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	9	RxOCLKIN+	Positive LVDS differential clock input (Odd clock)
12 RxEIN0- Negative LVDS differential data input (Even data) 13 RxEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Positive LVDS differential data input (Even data) 16 RxEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	10	RxOIN3-	Negative LVDS differential data input (Odd data)
13 RxEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Positive LVDS differential data input (Even data) 16 RxEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	11	RxOIN3+	Positive LVDS differential data input (Odd data)
14 VSS Power Ground 15 RxEIN1- Positive LVDS differential data input (Even data) 16 RxEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	12	RxEIN0-	Negative LVDS differential data input (Even data)
15 RxEIN1- Positive LVDS differential data input (Even data) 16 RxEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	13	RxEIN0+	Positive LVDS differential data input (Even data)
16 RxEIN1+ Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	14	VSS	Power Ground
17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	15	RxEIN1-	Positive LVDS differential data input (Even data)
18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	16	RxEIN1+	Negative LVDS differential data input (Even data)
19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	17	VSS	Power Ground
20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	18	RxEIN2-	Negative LVDS differential data input (Even data)
21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	19	RxEIN2+	Positive LVDS differential data input (Even data)
22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	20	RxECLKIN-	Negative LVDS differential clock input (Even clock)
23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	21	RxECLKIN+	Positive LVDS differential clock input (Even clock)
24 VSS Power Ground 25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	22	RxEIN3-	Negative LVDS differential data input (Even data)
25 VSS Power Ground 26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	23	RxEIN3+	Positive LVDS differential data input (Even data)
26 NC No Connection (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	24	VSS	Power Ground
27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	25	VSS	Power Ground
28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	26	NC	No Connection (for AUO test)
29 VCC +5.0V Power Supply	27	VSS	Power Ground
	28	vcc	+5.0V Power Supply
30 VCC +5.0V Power Supply	29	VCC	+5.0V Power Supply
	30	VCC	+5.0V Power Supply

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Note1: Start from left side



Note2: Input signals of odd and even clock shall be the same timing.

Note3: Please follow PSWG.

6.4 Interface Timing

6.4.1 Timing Characteristics

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS82DGG (Texas Instruments) or equivalent.

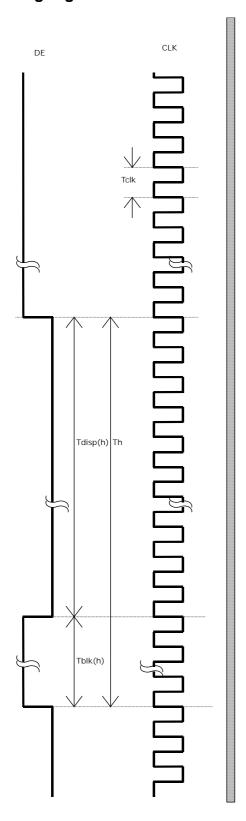
ŀ	tem	Symbol	Min	Тур	Max	Unit
Dat	ta CLK	Tclk	40	54	70	MHz
Llocation	Period	Th	685	844	1024	Tclk
H-section	Display Area	Tdisp(h)	640	640	640	Tclk
\/ apation	Period	Tv	1036	1066	2048	Th
V-section	Display Area	Tdisp(v)	1024	1024	1024	Th
Frame Rate		F	49	60	76	Hz

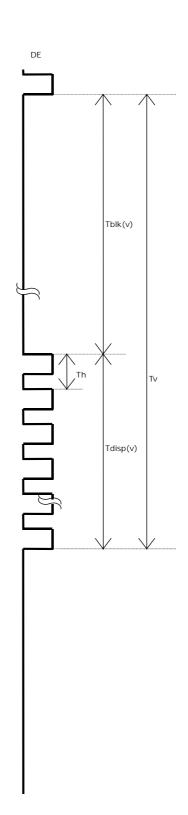
Note: DE mode only

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6.4.2 Timing Digram





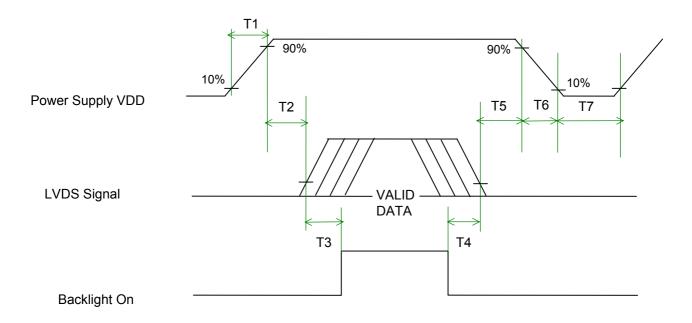
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6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter		Value	Unit	
Parameter	Min.	Тур.	Max.	Offic
T1	0.5	-	10	[ms]
T2	0	-	10	[ms]
Т3	200	-	-	[ms]
T4	100	-	-	[ms]
T5	0	16	50	[ms]
T6	-	-	10	[ms]
T7	1000	_	-	[ms]

Note: The values of the table are follow PSWG.

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7. Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

7.1.1 Connector

Connector Name / Designation	Interface Connector / Interface card
Manufacturer	P2 / JAE or compatible
Type Part Number	AL2307-A0G1D-P / FI-XB30SSRL-HF16
Mating Housing Part Number	JAE FI-X30HL

7.1.2 Pin Assignment

Pin#	Signal Name	Pin#	Signal Name
1	RxOIN0-	2	RxOIN0+
3	RxOIN1-	4	RxOIN1+
5	RxOIN2-	6	RxOIN2+
7	VSS	8	RxOCLKIN-
9	RxOCLKIN+	10	RxOIN3-
11	RxOIN3+	12	RxEIN0-
13	RxEIN0+	14	VSS
15	RxEIN1-	16	RxEIN1+
17	VSS	18	RxEIN2-
19	RxEIN2+	20	RxECLKIN-
21	RxECLKIN+	22	RxEIN3-
23	RxEIN3+	24	VSS
25	VSS	26	NC
27	VSS	28	VCC
29	VCC	30	VCC

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7.2 Backlight Unit

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	Lamp Connector / Backlight lamp
Manufacturer	JST
Type Part Number	BHSR-02VS-1
Mating Type Part Number	SM02B-BHSS-1-TB

7.2.1 Signal for Lamp connector

	Connector No.	Pin No.	Input	Color	Function
CN1	1	Hot1	Pink	High Voltage	
	CIVI	2	Cold1	White	Low Voltage
Upper	CNIO	1	Hot2	Blue	High Voltage
	CN2	2	Cold2	Black	Low Voltage

	Connector No.	Pin No.	Input	Color	Function
CN3	1	Hot1	Pink	High Voltage	
	CNS	2	Cold1	White	Low Voltage
Lower	CNIA	1	Hot2	Blue	High Voltage
	CN4	2	Cold2	Black	Low Voltage

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8. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50 , 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50 , 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0 , 300hours	
High Temperature Storage (HTS)	Ta= 60 , 300hours	
Low Temperature Storage (LTS)	Ta= -20 , 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 G Wave: Random Frequency: 10 - 200 - 10 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20 /30min, 60 /30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	2
ESD (ElectroStatic Discharge)	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:10,000 ft Non-Operation:30,000 ft	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20 to 60, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2, ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

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9. Shipping Label

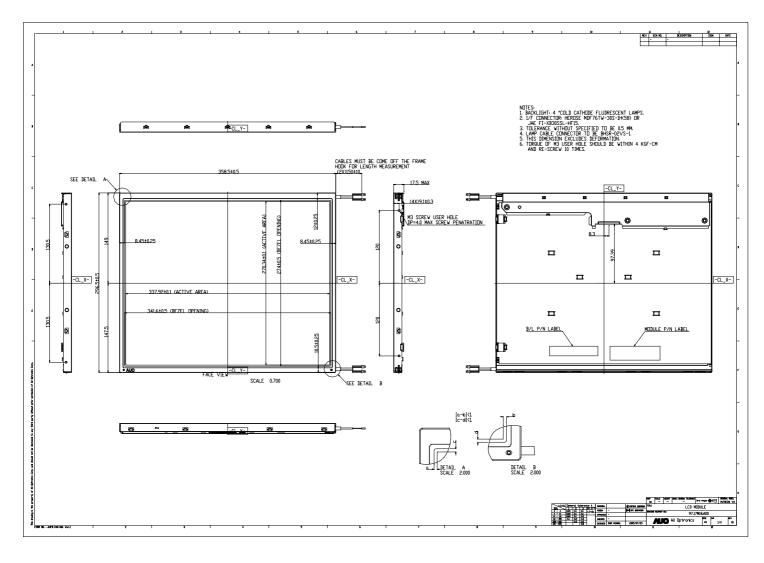
The shipping label format is shown as below.



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10. Mechanical Characteristics



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