



TO

DATE : Jan. 22, 2007

SAMSUNG TFT-LCD

MODEL NO.: LTN141W1-L06

NOTE: Extension code [-1]

LTN141W1-L06-1

Surface type [Anti-Glare]

Green product (Complied with RoHS requirement)

Any Modification of Spec is not allowed without SEC' permission

APPROVED BY:

PREPARED BY: LCD Product Planning Group 1

SAMSUNG ELECTRONICS CO., LTD.



Samsung Secret

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K. H. Shin

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REVISION HISTORY

Approval

Date F	Revision No.	Page	Summary
Feb. 8. 2006	P00	All	LTN141W1-L06 Model spec was issued first.
Apr.24, 2006	A00	All	LTN141W1-L06 Model spec was approved
Apr.24, 2006 May 29, 2006	A00 A01	All 23	The extension code was changed from 00X3 to 10X3. LTN141W1-L06-0003(Cheonan) → LTN141W1-L06-1003 LTN141W1-L06-00A3(SESL) → LTN141W1-L06-10A3

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GENERAL DESCRIPTION

DESCRIPTION

LTN141W1-L06 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching devices. This model is composed of a TFT LCD panel, a driver circuit and a backlight unit. The resolution of a 14.1" contains 1,280 x 800 pixels and can display up to 262,144 colors. 6 O'clock direction is the Optimum viewing angle.

FEATURES

- Thin and light weight
- High contrast ratio, high aperture structure
- Wide XGA (1280x800 pixels) resolution
- Fast Response Time
- Low power consumption
- Single CCFL
- DE (Data enable) only mode.
- 3.3V LVDS Interface
- On board EDID chip
- RoHS Compliance

APPLICATIONS

- Notebook PC
- If the usage of this product is not for PC application, but for others, please contact SEC.

GENERAL INFORMATION

Item	Specification	Unit	Note
Display area	303.36(H) x 189.6(V) (14.1" diagonal)	mm	
Driver element	a-Si TFT active matrix		
Display colors	262,144		
Number of pixel	1280 x RGB(3) x 800	pixel	16 : 10
Pixel arrangement	RGB vertical stripe		
Pixel pitch	0.2370(H) x 0.2370(V) (TYP.)	mm	
Display Mode	Normally white		
Surface treatment	Haze 25, Hard-Coating 3H		

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Mechanical Information

Item		Min.	Тур.	Max.	Unit	Note
	Horizontal (H)	319.0	319.5	320.0	mm	
Module size	Vertical (V)	205.0	205.5	206.0	mm	
size	Depth (D)	-	-	5.5	mm	
	Weight		400	420	g	

Note (1) Measurement condition of outline dimension

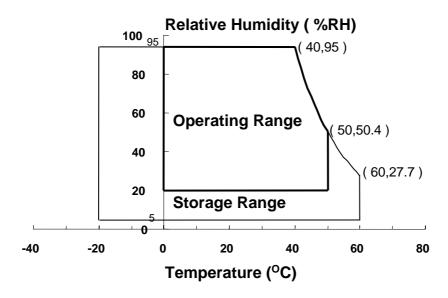
. Equipment : Bernier Calipers . Push Force : 500g ·f (minimum)

1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENTAL ABSOLUTE RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Storage temperate	TSTG	-20	60	°C	(1)
Operating temperate (Temperature of glass surface)	TOPR	0	50	°C	(1)
Shock (non-operating)	Snop	-	240	G	(2),(4)
Vibration (non-operating)	Vnop	-	2.41	G	(3),(4)

Note (1) Temperature and relative humidity range are shown in the figure below. 95 % RH Max. (40 $^{\circ}$ C \geq Ta) Maximum wet - bulb temperature at 39 $^{\circ}$ C or less. (Ta > 40 $^{\circ}$ C) No condensation



- (2) 2ms, half sine wave, one time for $\pm X$, $\pm Y$, $\pm Z$.
- (3) 5 500 Hz, random vibration, 30min for X, Y, Z.
- (4) At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard and rigid enough so that the Module would not be twisted or bent by the fixture.

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1.2 ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

 $V_{DD} = 3.3V$, $V_{SS} = GND = 0V$

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V _{DD}	V _{DD} - 0.3	V _{DD} + 0.3	V	(1)
Logic Input Voltage	Vin	V _{DD} - 0.3	V _{DD} + 0.3	V	(1)

NOTE (1) Within Ta (25 ± 2 °C)

(2) BACK-LIGHT UNIT

Ta = 25 ± 2 °C

Item	Symbol	Min.	Max.	Unit	Note
Lamp Current	IL	3.0	7.0	mArms	(1)
Lamp frequency	F _L	40	80	kHz	(1)

NOTE (1) Permanent damage to the device may occur if maximum values are exceeded.

Functional operation should be restricted to the conditions described under Normal Operating Conditions.

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2. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (5). Measuring equipment: TOPCON SR-3

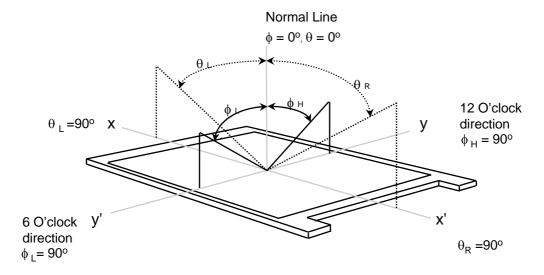
* Ta = 25 ± 2 °C, Vdd=3.3V, fv= 60Hz, fdclk = 68.9MHz, IL = 6.0 mArms

Item		Symbol	Condition	Min.	Тур.	Max	Unit	Note
Contrast F (5 Poin		CR		200	300	-	-	(1), (2), (5)
Response	Rising	T _R +T _f		_	25	35	msec	(1), (3)
Time at 25	Falling	IKTII		_	25	33	IIISEC	(1), (3)
Average Lum of White (5		YL,AVE	Normal	140	170	-	cd/m ²	I∟=6.0mA (1), (4)
	Dad	Rx	Viewing	0.562	0.590	0.618		
Color	Red	Ry	Angle $\phi = 0$ $\theta = 0$	0.320	0.340	0.360	- - - -	(1), (5) SR-3
	0	Green Gx		0.292	0.320	0.348		
	Green	G _Y		0.530	0.550	0.570		
Chromaticity (CIE)	Dive	Вх		0.124	0.152	0.180		
	Blue	Вү		0.110	0.130	0.150		
	White	Wx		0.285	0.313	0.341		
	vvnite	WY		0.309	0.329	0.349		
	Llav	θι		-	45	-		
Viewing	Hor.	θн	OD > 40	-	45	-	Degree	(1), (5)
Angle	Ver.	фн	CR ≥ 10	-	20	-	S	SR-3
		фь		-	45	-		
13 Poin White Vari		δι		-	-	1.65	-	(6)

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Note 1) Definition of Viewing Angle : Viewing angle range($10 \le C/R$)

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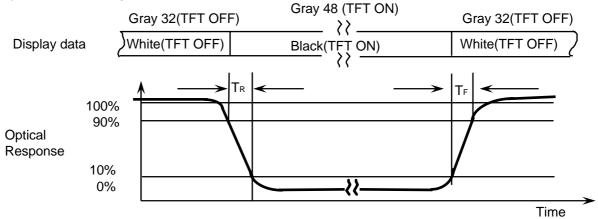


Note 2) Definition of Contrast Ratio (CR): Ratio of gray max (Gmax) ,gray min (Gmin) at 5 points(4, 5, 7, 9, 10)

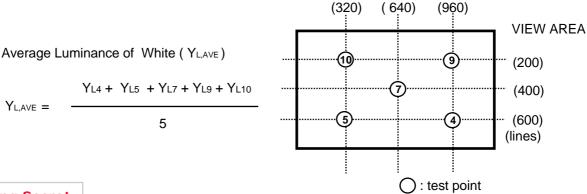
$$CR = \frac{CR(4) + CR(5) + CR(7) + CR(9) + CR(10)}{5}$$

Points : (4), (5), (7), (9), (10) at the figure of Note (6).

Note 3) Definition of Response time:



Note 4) Definition of Average Luminance of White: measure the luminance of white at 5 points.



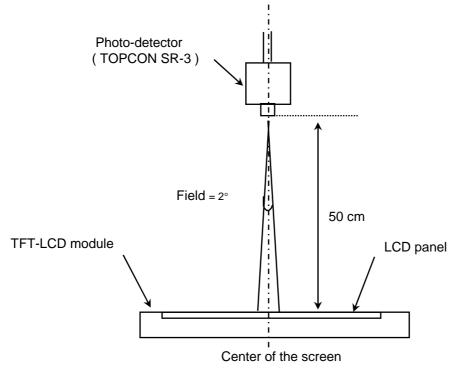
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Note 5) After stabilizing and leaving the panel alone at a given temperature for 30 min , the measurement should be executed. Measurement should be executed in a stable, windless, and dark room.

30 min after lighting the backlight. This should be measured in the center of screen.

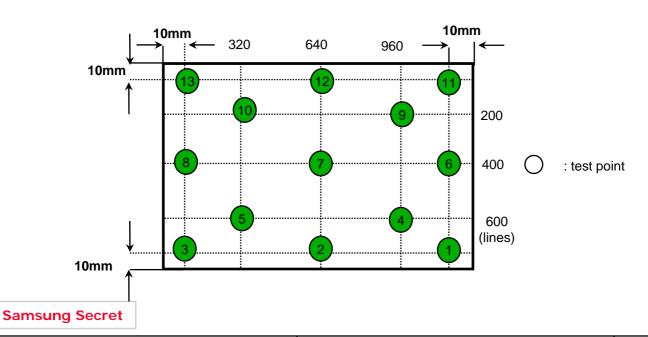
Lamp current: 6.0mA

Environment condition : Ta = 25 ± 2 °C



[Optical characteristics measurement setup]

Note 6) Definition of 13 points white variation (δ L), CR variation (CVER) [1 ~ 13] δ L = $\frac{\text{Maximum luminance of 13 points}}{\text{Minimum luminance of 13 points}}$



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3. ELECTRICAL CHARACTERISTICS

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3.1 TFT LCD MODULE

Ta= 25 ± 2°C

Item	Item		Min.	Тур.	Max.	Unit	Note
Voltage of Power Supply		V _{DD}	3.0	3.3	3.6	V	
Differential Input Voltage for LVDS Receiver Threshold	High	ViH	-	-	+100	mV	V 14 2V
	Low	VIL	-100	1	-	mV	V _{CM} = +1.2V
Vsync Frequency		fv	-	60	-	Hz	
Hsync Freque	Hsync Frequency		-	48.96	-	KHz	fv*816
Main Frequer	псу	fock	-	68.93	-	MHz	fh*1408
Rush Currer	nt	Irush	-	-	1.5	Α	(4)
	White		-	360	-	mA	(2),(3)*a
Current of Power Supply	Mosaic	ldd	-	400	-	mA	(2),(3)*b
	Max.PT		-	465	485	mA	(2),(3)*c

Note (1) Display data pins and timing signal pins should be connected.(GND = 0V)

- (2) $f_V = 60 Hz$, $f_{DCLK} = 68.93 MHZ$, $V_{DD} = 3.3 V$, DC Current.
- (3) Power dissipation pattern



VIEW AREA

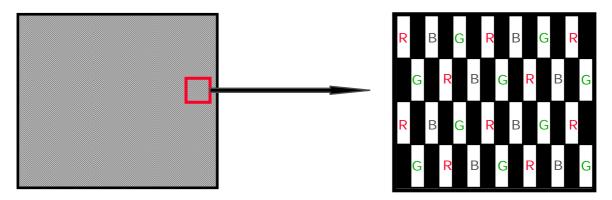
Display Brightest Gray Level

Display Darkest Gray Level

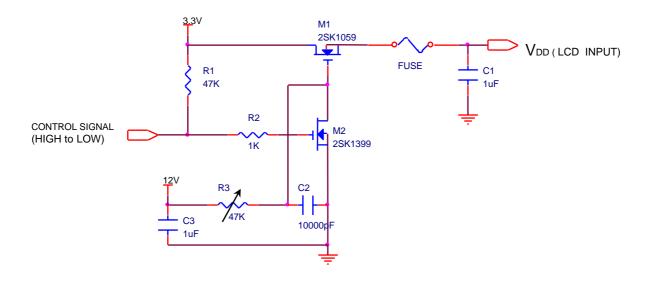
*b) Mosaic Pattern

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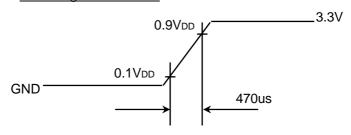
*d) 1dot Inversion Pattern



4) Rush current measurement condition



VDD rising time is 470us



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3.2 BACK-LIGHT UNIT

The backlight system is an edge-lighting type with a single CCFT (Cold Cathode Fluorescent Tube). The characteristics of a single lamp are shown in the following table.

- INVERTER: SEC SIC 130T

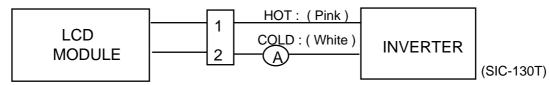
Ta= 25 ± 2 °C

Item	Symbol	Min.	Тур.	Max.	Unit	Note
Lamp Current	Iι	3.0	6.0	6.5	mArms	(1)
Lamp Voltage	VL	-	665	-	Vrms	I∟= 6.0mA
Frequency	f∟	50	60	65	KHz	(2)
Power Consumption	P∟	-	4.0	-	W	(3) IL = 6.0mA
Operating Life Time	Hr	10,000	-	-	Hour	(4)
Startup Valtage	V ₂			1200	Vrms	25°C, (5)
Startup Voltage	Vs	-	-	1400	Vrms	0°C, (5)

Note) The waveform of the inverter output voltage must be area symmetric and the design of the inverter must have specifications for the modularized lamp.

The performance of the backlight, for example life time or brightness, is much influenced by the characteristics of the DC-AC inverter for the lamp. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter. When you design or order the inverter, please make sure that a poor lighting caused by the mismatch of the backlight and the inverter(miss lighting, flicker, etc.) never occur. When you confirm it, the module should be operated in the same condition as it is installed in your instrument.

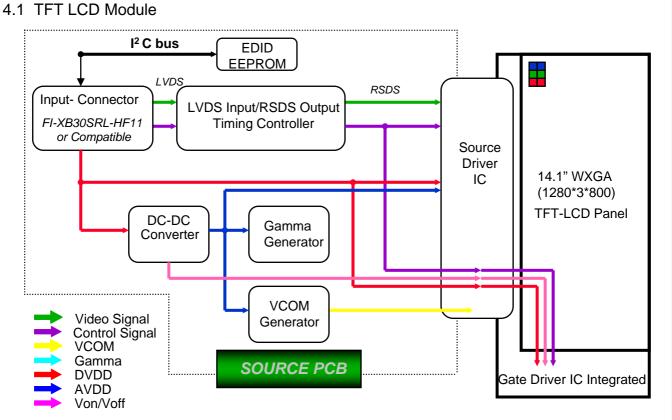
Note (1) Lamp current is measured with a high frequency current meter as shown below.



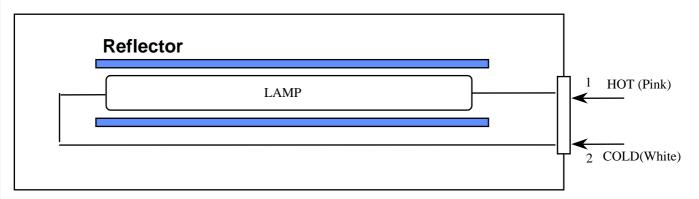
- (2) Lamp frequency may produce interference with horizontal synchronous frequency and this may cause line flow on the display. Therefore lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible in order to avoid interference.
- (3) Refer to I_L×V_L to calculate.
- (4) Life time (Hr) of a lamp can be defined as the time in which it continues to operate under the condition Ta= 25 ± 2 °C and IL = 6.0 mArms until one of the following event occurs.
 - 1. When the brightness becomes 50% or lower than the original.
 - 2. When the Effective ignition length becomes 80% or lower than the original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)
 - 3. Lamp unit only.
- (5) The inverter open voltage this voltage should be measured after ballast capacitor- have to be larger than the lamp startup voltage, otherwise backlight may has blinking for a moment after turns on or not be turned on.
 - If an inverter has shutdown function it should keep its open voltage for longer than 1 second even if lamp connector open.

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4. BLOCK DIAGRAM



4.2 BACK-LIGHT UNIT



Connector: BHSR-02VS-1

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Note) The output of the inverter may change according to the material of the reflector.

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5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power LVDS, Connector : JAE FI-XB30SRL-HF11 or compatible Mating Connector : JAE FI-X30M or compatible

No.	Symbol	Function	Polarity	Remarks
1	VSS	Ground		
2	VDD	POWER SUPPLY +3.3V		
3	VDD	POWER SUPPLY +3.3V		
4	VEEDID	DDC 3.3V Power		
5	BIST	Panel BIST enable		
6	CLKEDID	DDC Clock		
7	DATAEDID	DDC data		
8	RxIN0-	LVDS Differential Data INPUT (R0-R5,G0)	Negative	
9	RxIN0+	LVDS Differential Data INPUT (R0-R5,G0)	Positive	
10	GND	Ground		
11	RxIN1-	LVDS Differential Data INPUT (G1-G5,B0-B1)	Negative	
12	RxIN1+	LVDS Differential Data INPUT (G1-G5,B0-B1)	Positive	
13	GND	Ground		
14	RxIN2-	LVDS Differential Data INPUT (B2-B5,Sync,DE)	Negative	
15	RxIN2+	LVDS Differential Data INPUT (B2-B5,Sync,DE)	Positive	
16	Vss	Ground		
17	ClkIN-	LVDS Differential Clock INPUT	Negative	
18	ClkIN+	LVDS Differential Clock INPUT	Positive	
19	Vss	Ground		
20	NC	No connect		
21	NC	No connect		
22	NC	No connect		
23	NC	No connect		
24	NC	No connect		
25	NC	No connect		
26	NC	No connect		
27	NC	No connect		
28	NC	No connect		
29	NC	No connect		
30	NC	No connect		

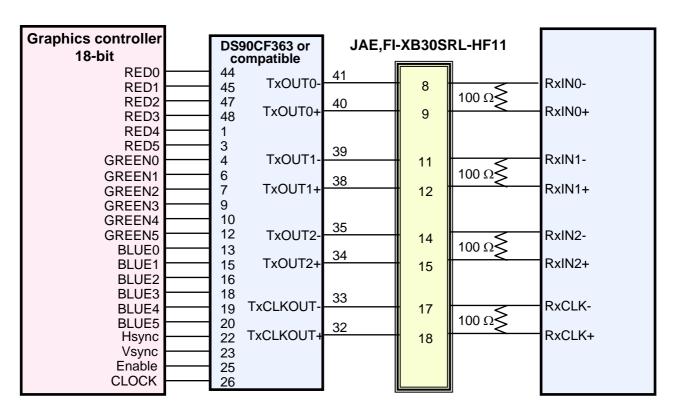
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5.2 LVDS Interface: Transmitter DS90CF363 or Compatible

LVDS

Pin No.	Name	RGB Signal	Pin No.	Name	RGB Signal
44	TxIN0	RO0	12	TxIN11	GO5
45	TxIN1	RO1	13	TxIN12	BO0
47	TxIN2	RO2	15	TxIN13	BO1
48	TxIN3	RO3	16	TxIN14	BO2
1	TxIN4	RO4	18	TxIN15	воз
3	TxIN5	RO5	19	TxIN16	BO4
4	TxIN6	GO0	20	TxIN17	BO5
6	TxIN7	GO1	22	TxIN18	Hsync
7	TxIN8	GO2	23	TxIN19	Vsync
9	TxIN9	GO3	25	TxIN20	DE
10	TxIN10	GO4	26	TxCLK IN	Clock

LVDS Interface



Note: The LCD Module uses a 100ohm resistor between positive and negative lines of each receiver input.

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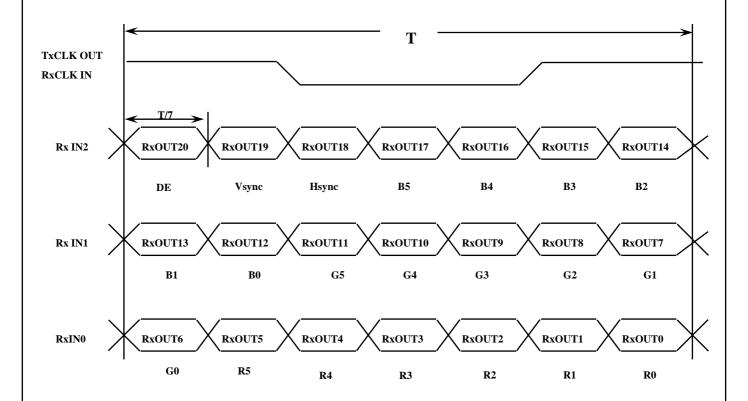
5.3 BACK LIGHT UNIT

Connector : JST BHSR - 02VS -1 Mating Connector : SM02B-BHSS-1(JST)

Pin NO.	Symbol	Color	Function			
1	НОТ	Pink	High Voltage			
2	COLD	White	Low Voltage			

5.4 Timing Diagrams of LVDS For Transmission

LVDS Receiver: Integrated T-CON



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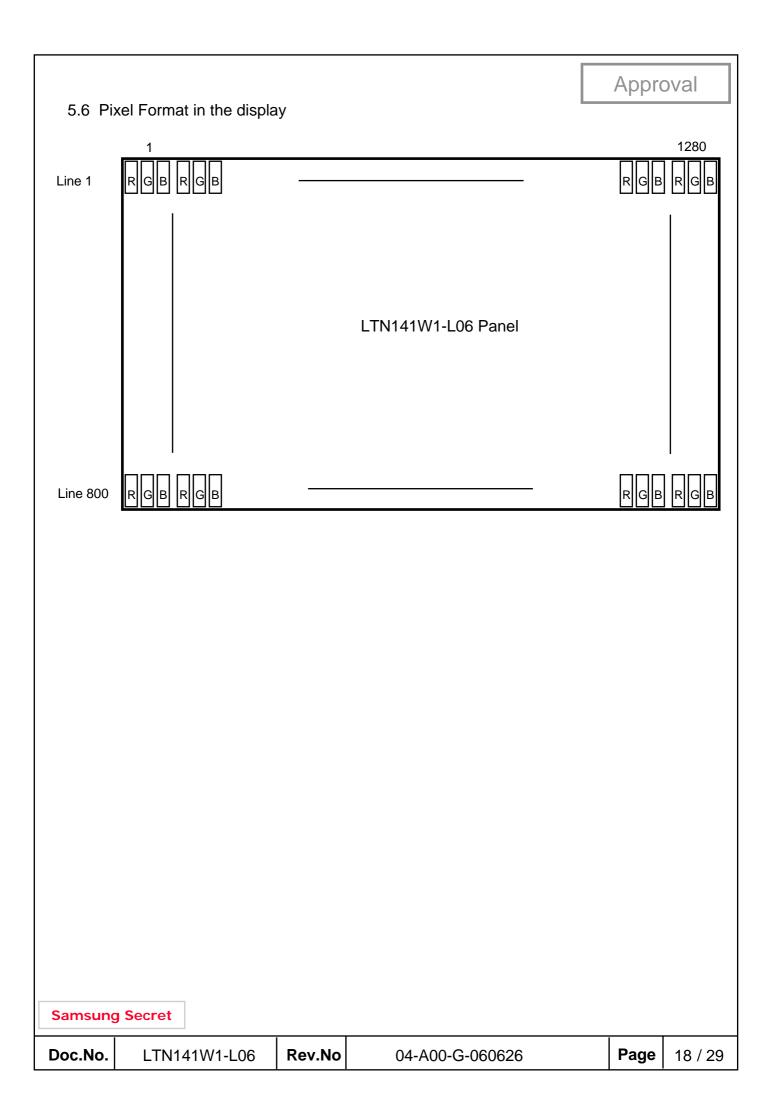
5.5 Input Signals, Basic Display Colors and Gray Scale of Each Color

										Data	Sign	al								Gray
Color	Display			R	ed					Gre	een					BI	ue			Scale
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	В0	B1	B2	ВЗ	45	B5	Level
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	-
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	-
Basic	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	-
Colors	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	-
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	-
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	-
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	Dark	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
Gray	↑	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
Scale	:		• •	:		:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3~R60
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	K3~K00
Red	\downarrow	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R61
	Light	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R62
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R63
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	Dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	G1
Gray	↑	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G2
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~G60
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~G00
Green	↓	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	G61
	Light	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	G62
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	G63
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	B1
Gray	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B2
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~B60
Of	:	:	•	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	D0~D00
Blue	↓	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	B61
	Light	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B62
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	B63

Note 1) Definition of gray:

Rn: Red gray, Gn: Green gray, Bn: Blue gray (n=gray level) Note 2)Input signal: 0 =Low level voltage, 1=High level voltage

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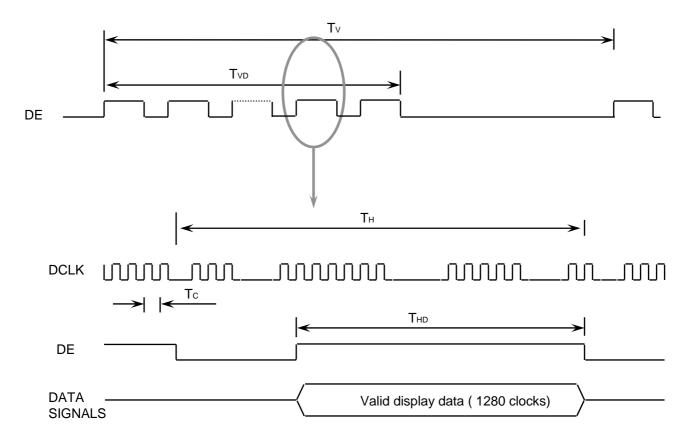


6. INTERFACE TIMING

6.1 Timing Parameters

Signal	Item	Symbol	Min.	Тур.	Max.	Unit	Note
Frame Frequency	Cycle	TV	806	816	833	Lines	-
Vertical Active Display Term	Display Period	TVD	-	800	-	Lines	-
One Line Scanning Time	Cycle	TH	1320	1408	1500	Clocks	-
Horizontal Active Display Term	Display Period	THD	-	1280	-	Clocks	-

6.2 Timing diagrams of interface signal

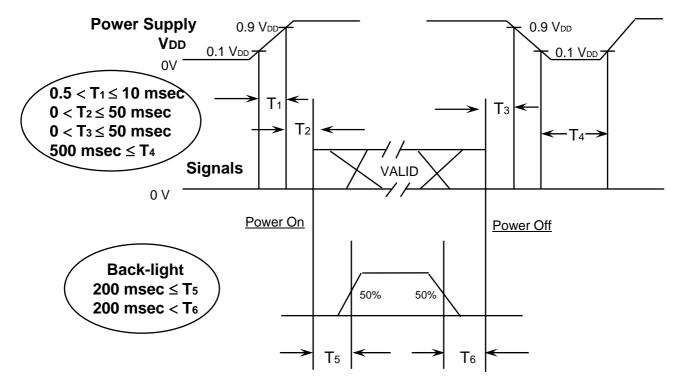


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6.3 Power ON/OFF Sequence

: To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

T1: Vdd rising time from 10% to 90%

T2: The time from Vdd to valid data at power ON.

T3: The time from valid data off to Vdd off at power Off.

T4: Vdd off time for Windows restart

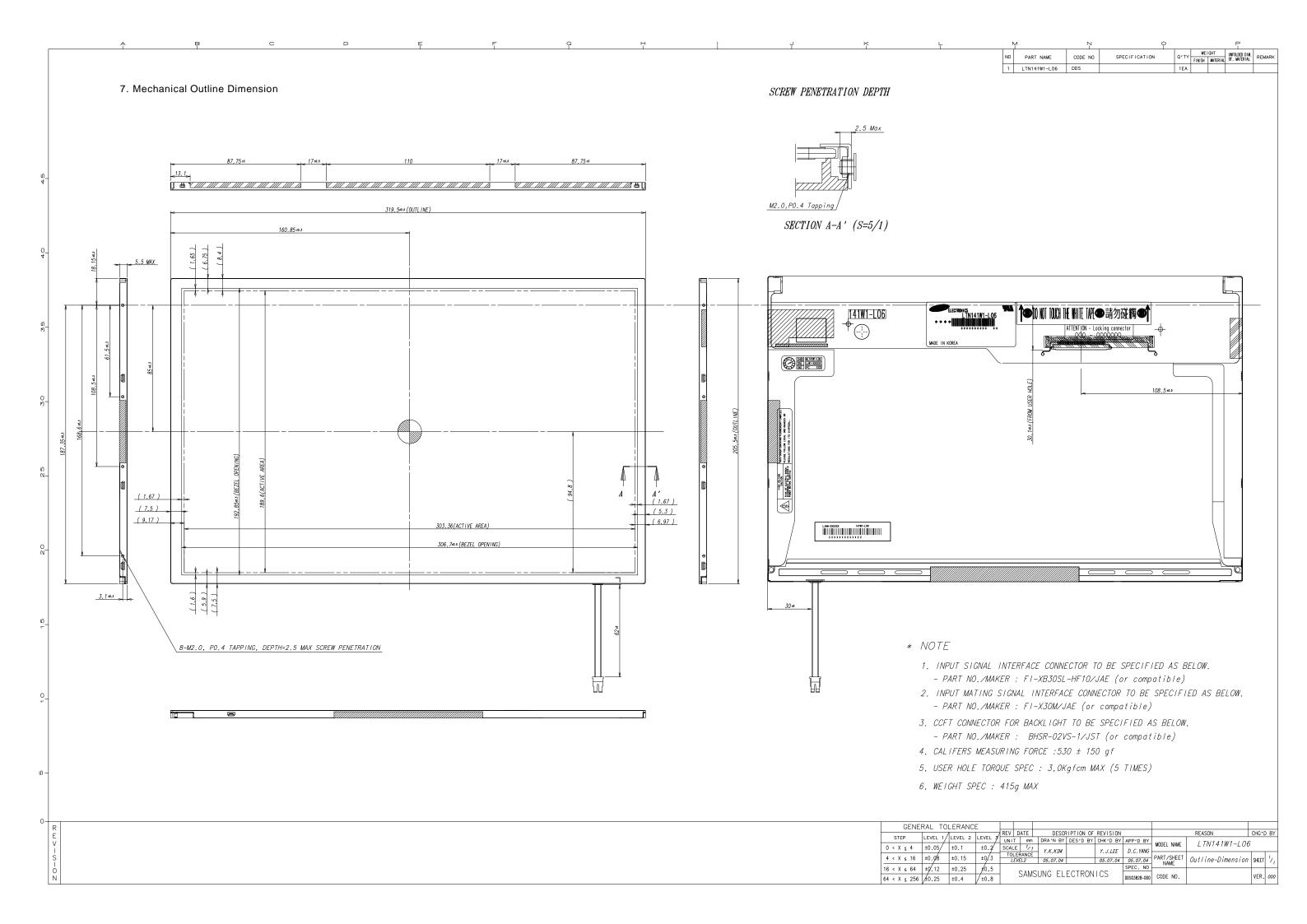
T5: The time from valid data to B/L enable at power ON.

T6: The time from valid data off to B/L disable at power Off.

NOTE.

- (1) The supply voltage of the external system for the module input should be the same as the definition of VDD.
- (2) Apply the lamp voltage within the LCD operation range. When the back-light turns on before the LCD operation or the LCD turns off before the back-light turns off, the display may momentarily become white.
- (3) In case of VDD = off level, please keep the level of input signals on the low or keep a high impedance.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

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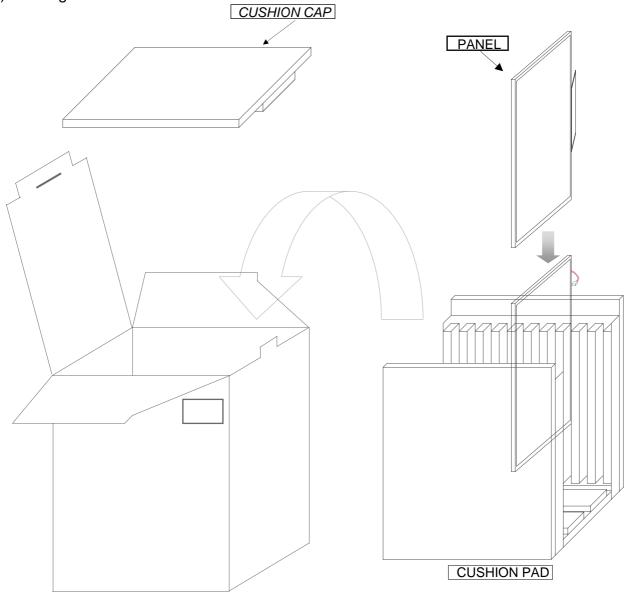


8. PACKING

Approval

- 1. CARTON(Internal Package)
 - (1) Packing Form
 Corrugated Cardboard box and Corrupad form as shock absorber

(2) Packing Method



Note 1)Total Weight: Approximately 10 kg 2) Acceptance number of piling: 10 sets 3) Carton size: 376(W)×326(D)×404(H)

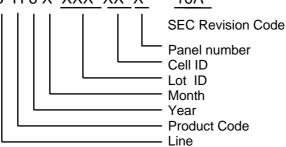
No	Part name	Quantity
1	Static electric protective sack	10
2	Packing case (Inner box) included shock absorber	1 set
3	Pictorial marking	2 pcs
4	Carton	1 set

9. MARKINGS & OTHERS

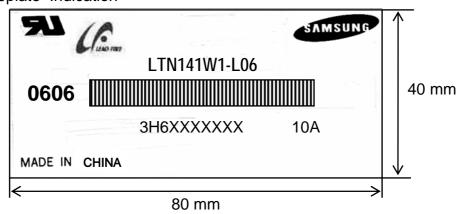
A nameplate bearing followed by is affixed to a shipped product at the specified location on each product.

(1) Parts number: LTN141W1-L06(2) Revision: Three letters(3)Control code: One letter

(4) Lot number : 3 H 6 X XXX XX X 10A



(5) Nameplate Indication



Parts name : LTN141W1 - L06 Lot number : 3H6GXXXXXX

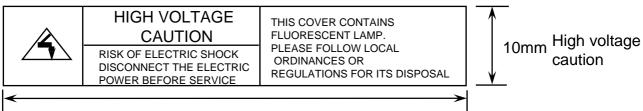
Inspected work week : 0606(2006 year, 6th week)

Product Revision Code: 10A

Production Site : CHINA (SESL)

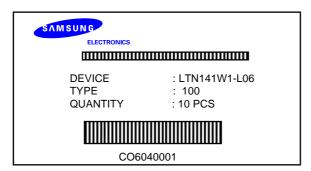
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This HIGH VOLTAGE CAUTION is carved in mold frame



70mm

(6) Packing small box attach



(7) Packing box Marking: Samsung TFT-LCD Brand Name



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10. GENERAL PRECAUTIONS

1. Handling

- (a) When the module is assembled, It should be attached to the system firmly using selected mounting holes. Be careful not to twist and bend the modules.
- (b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and CCFT backlight.
- (c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.
- (d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.
- (e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (f) The desirable cleaners are water, IPA(Isoprophyl Alcohol) or Hexane.

 Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
- (h) Protect the module from static, it may cause damage to the C-MOS Gate Array IC.
- (i) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (j) Do not disassemble the module.
- (k) Do not pull or fold the lamp wire.
- (I) Do not adjust the variable resistor which is located on the back side.
- (m) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (n) Pins of I/F connector shall not be touched directly with bare hands.

Samsun	g Secret
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2. STORAGE

- (a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C and relative humidity of less than 70%.
- (b) Do not store the TFT-LCD module in direct sunlight.
- (c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

3. OPERATION

- (a) Do not connect, disconnect the module in the "Power On" condition.
- (b) Power supply should always be turned on/off by following item 6.3 "Power on/off sequence ".
- (c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (d) The cable between the backlight connector and its inverter power supply shall be a minimized length and be connected directly. The longer cable between the backlight and the inverter may cause lower luminance of lamp(CCFT) and may require higher startup voltage(Vs).

4. OTHERS

- (a) Ultra-violet ray filter is necessary for outdoor operation.
- (b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.
- (c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.
- (d) If the module displays the same pattern continuously for a long period of time, it can be the situation when the image "sticks" to the screen.
- (e) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

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11. EDID

Address		Value			ASCII	
	FUNCTION		BIN	DEC	or	Notes
(HEX)		HEX			Data	
00		00	00000000	0		
01		FF	11111111	255		
02		FF	11111111	255		
03		FF	11111111	255		
04	Header	FF	11111111	255		EDID Header
05		FF	11111111	255		
06		FF	11111111	255		
07		00	00000000	0		
08		4C	01001100	76	S	3 character ID
	ID Manufacturer Name				E	
09		A3	10100011	163	c	"SEC"
0A		42	01000010	66	[B]	
0B	ID Product Code	41	01000001	65	[A]	
0C		00	00000000	0	F 3	
0D		00	00000000	0		
0E	32-bit serial no.	00	00000000	0		
0F		00	00000000	0		
10	Week of manufacture	00	00000000	0		
11	Year of manufacture	10	00010000	16	2006	2006
12	EDID Structure Ver.	01	00000001	1	1	EDID Ver. 1.0
13	EDID revision #	03	00000011	3	3	EDID Rev. 3
14	Video input definition	80	10000000	128		
15	Max H image size	1E	00011110	30	30	30 cm(approx)
16	Max V image size	13	00010011	19	19	19 cm(approx)
17	Display Gamma	78	01111000	120	2.2	Gamma 2.2
18	Feature support	0A	00001010	10		
19	Red/green low bits	87	10000111	135		10000111
1A	Blue/white low bits	F5	11110101	245		1111110
					0.580	Red x 0.580=
1B	Red x/ high bits	94	10010100	148	0.000	1001010010
_					0.340	Red y 0.340=
1C	Redy	57	01010111	87	0.010	0101011100
	_				0.310	Green x 0.310=
1D	Green x	4F	01001111	79	0.0.0	0100111101
	_				0.550	Green y 0.550=
1E	Green y	8C	10001100	140	0.000	1000110011
					0.155	Blue x 0.155=
1F	Blue x	27	00100111	39	0.100	001001111
					0.155	Blue y 0.155=
20	Blue y	27	00100111	39	0.100	001001111
					0.313	White x 0.313=
21	White x	50	01010000	80	0.010	0101000001
		_		_	0.329	White y 0.329=
22	White y	54	01010100	84	0.020	0101010001
23	Established timing 1	00	00000000	0		2.3.0.000.
24	Established timing 2	00	0000000	0		
25	Established timing 3	00	00000000	0		
20	Lotabilotica tittiilig o		0000000	U		

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27	26		01	00000001	1		
28 Standard timing #2 01 000000001 1 not used 2A Standard timing #3 01 00000001 1 not used 2C Standard timing #4 01 00000001 1 not used 2D Standard timing #5 01 00000001 1 not used 2E Standard timing #6 01 00000001 1 not used 30 Standard timing #7 01 00000001 1 not used 32 Standard timing #8 01 00000001 1 not used 34 Standard timing #8 01 00000001 1 not used 36 EE 1110110 238 68.94 Main clocke 68.94 MHz 37 14 00011010 28 68.94 Main clocke 68.94 MHz 38 10 00000000 1 10 not used 39 14 00011010 28 8.94 Min clocke 68.94 MHz 30 10 00000		Standard timing #1		II .			not used
29							
2A 2B 2B 2C 2C 2D 31 30 31 31 32 32 33 33 34 44 35 36 36 36 36 36 37 37 38 39 39 39 39 39 39 39 39 39 30 30 30 30 30 30 30 30 30 30 30 30 30		Standard timing #2		II .	•		not used
28		Otana da ad timaina a 110	01		1		
2D	2B	Standard timing #3	01	00000001	1		not used
25	2C	Standard timing #4	01	00000001	1		notunod
Standard timing #6	2D	Standard tirriing #4	01	00000001	1		not used
2F		Standard timing #5	01		1		notused
31	2F	Standard tirring #5	01	00000001	1		not useu
31		Standard timing #6			1		not used
33		Ciandara anning #0					1101 0000
33		Standard timing #7					not used
Standard timing #8							
35		Standard timing #8					not used
1A							
1A	36		EE	11101110		68.94	Main clock= 68.94 MHz
Section Sect	37		1A	00011010	26		
SA 3B 3B 3C 2D 00100000 32 300 Vertical blanking=16 lines 2D 00100000 32 300 Vertical blanking=16 lines 30 00110000 48 4bit : 4bit 4bit : 4bit 30 00110000 48 4bit : 4bit 4bit : 4bit 4D 4bit : 4bit 4D 4D 4D 4D 4D 4D 4D 4	38		00	00000000	0	1280	•
38 3C 3D 3C 3D 3D 3C 3D 3D	39		80		128	128	
10				01010000			
3D 3E 3D 3E 3D 3D 3D 3D							
Detailed timing/monitor 40			I			16	_
3F							
40							
41	3F		40	01000000	64		
41	40	descriptor #1	33	00110011	51		
BE	41		00	00000000	0		2bit : 2bit :2bit :2bit
BE	12		2F	00101111	47	303	H image size= 303 mm(approx)
10							
Manufacturer Specified (Timing)						100	1age 6:25 1 00(app. 6/4)
Manufacturer Specified (Timing)							No Horizontal Border
19							
Manufacturer Specified (Timing)	47						
Manufacturer Specified (Timing)	48		00	00000000			
Manufacturer Specified (Timing)							
4B 4C 4D 00 00000000 0 4E 00 00000000 0 Value=HSPWmin / 2 4F Detailed timing/monitor 00 00000000 0 Value=Thbpmin / 2 50 descriptor #2 00 00000000 0 Value=Thbpmax/2 51 00 00000000 0 Value=VSPWmin / 2 52 00 00000000 0 Value=VSPWmax/2 53 00 00000000 0 Value=Tvbpmin / 2 54 00 00000000 0 Value=Tvbpmax / 2 55 00 00000000 0 Value=Tvbpmax / 2 23 00100011 35 Thpmin=value*2 + HA pixelclks 56 87 10000111 135 Thpmax=value*2 + HA pixelclks 57 00 00000010 2 Tvpmin=value*2 + VA lines							Manufacturer Specified (Timina)
4C 4D 4D 00 00000000 0 Value=HSPWmin / 2 4E 00 00000000 0 Value=HSPWmax / 2 4F Detailed timing/monitor 00 00000000 0 Value=Thbpmin / 2 50 descriptor #2 00 00000000 0 Value=Thbpmax / 2 51 00 00000000 0 Value=VSPWmin / 2 52 00 00000000 0 Value=VSPWmax / 2 53 00 00000000 0 Value=Tvbpmin / 2 54 00 00000000 0 Value=Tvbpmin / 2 55 00 00000000 0 Value=Tvbpmin / 2 23 00100011 35 Thpmin=value*2 + HA pixelclks 56 87 10000111 135 Thpmax=value*2 + HA pixelclks 57 00 00000010 2 Tvpmin=value*2 + VA lines							
4D 4E Detailed timing/monitor							
4E 00 00000000 0 Value=HSPWmax/2 50 descriptor #2 00 00000000 0 Value=Thbpmin /2 51 00 00000000 0 Value=Thbpmax/2 52 00 00000000 0 Value=VSPWmin /2 53 00 00000000 0 Value=Tvbpmin / 2 54 00 00000000 0 Value=Tvbpmax / 2 55 23 00100011 35 Thpmin=value*2 + HA pixelclks 56 87 10000111 135 Thpmax=value*2 + HA pixelclks 57 00 00000010 2 Tvpmin=value*2 + VA lines							Value_HSD\//min / 2
4F Detailed timing/monitor 00 00000000 0 Value=Thbpmin /2 50 descriptor #2 00 00000000 0 Value=Thbpmax/2 51 00 00000000 0 Value=VSPWmin /2 52 00 00000000 0 Value=VSPWmax/2 53 00 00000000 0 Value=Tvbpmin / 2 54 00 00000000 0 Value=Tvbpmax / 2 55 23 00100011 35 Thpmin=value*2 + HA pixelclks 56 87 10000111 135 Thpmax=value*2 + HA pixelclks 57 00 00000010 2 Tvpmin=value*2 + VA lines							
50 descriptor #2 00 00000000 0 Value=Thbpmax/2 51 00 00000000 0 Value=VSPWmin /2 52 00 00000000 0 Value=VSPWmax/2 53 00 00000000 0 Value=Tvbpmin / 2 54 00 00000000 0 Value=Tvbpmax / 2 55 23 00100011 35 Thpmin=value*2 + HA pixelclks 56 87 10000111 135 Thpmax=value*2 + HA pixelclks 57 02 00000010 2 Tvpmin=value*2 + VA lines		Detailed timing/monitor					
51 00 000000000 0 Value=VSPWmin/2 52 00 00000000 0 Value=VSPWmax/2 53 00 00000000 0 Value=Tvbpmin/2 54 00 00000000 0 Value=Tvbpmax/2 55 23 00100011 35 Thpmin=value*2 + HA pixelclks 56 87 10000111 135 Thpmax=value*2 + HA pixelclks 57 02 00000010 2 Tvpmin=value*2 + VA lines							
52 00 00000000 0 Value=VSPWmax/2 53 00 00000000 0 Value=Tvbpmin / 2 54 00 00000000 0 Value=Tvbpmax / 2 55 23 00100011 35 Thpmin=value*2 + HA pixelclks 56 87 10000111 135 Thpmax=value*2 + HA pixelclks 57 02 00000010 2 Tvpmin=value*2 + VA lines		ασοσιρισι πΖ					
53 00 000000000 0 Value=Tvbpmin / 2 54 00 00000000 0 Value=Tvbpmax / 2 55 23 00100011 35 Thpmin=value*2 + HA pixelclks 56 87 10000111 135 Thpmax=value*2 + HA pixelclks 57 02 00000010 2 Tvpmin=value*2 + VA lines							
54 00 000000000 0 Value=Tvbpmax/2 55 23 00100011 35 Thpmin=value*2 + HA pixelclks 56 87 10000111 135 Thpmax=value*2 + HA pixelclks 57 02 00000010 2 Tvpmin=value*2 + VA lines							
55 23 00100011 35 Thpmin=value*2 + HA pixelclks 56 87 10000111 135 Thpmax=value*2 + HA pixelclks 57 02 00000010 2 Tvpmin=value*2 + VA lines							•
56 87 10000111 135 Thpmax=value*2 + HA pixelclks 57 02 00000010 2 Tvpmin=value*2 + VA lines			-				•
57 02 00000010 2 Tvpmin=value*2 + VA lines							
			I				
58 64 01100100 100 Tvpmax= value *2 + VA lines							
59 00 00000000 0 Module revision							•

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SB SC SC SD SC SD SC SD SE SC SD SD SD SD SD SD SD	5A		00	00000000	0		
SC SD FE 11111110 254					_		
FE							100115 . 0.: -
SE SF 60 Detailed timing/monitor 60 61 Detailed timing/monitor 62 63 64 65 66 66 66 66 66 66							ASCII Data String Tag
SF 60 Detailed timing/monitor 41 01000001 65 [A]	5D		FE	111111110	254		
A			00	00000000	0		
61 Detailed timing/monitor 62 descriptor #3 53 01010011 83 [S] 55 0101010 85 [U] 4E 01001110 78 [N] 66 66 67 67 68 69 69 69 60 20 00100000 32 [] 20 00100000 32 [] 20 00100000 32 [] 60 60 60 60 60 60 60 60 60 60 60 60 60 6							
62 descriptor #3 63							
63							
AE		descriptor #3					
A7							
66 67 67 68 69 20 00100000 32 [] 69 6A 6B 20 00100000 32 [] 6C 6B 6C 0 00000000 0 0 6E 0 00000000 0 0 0 6F 0 00000000 0 0 0 0 71 72 0 00000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0							
67 68 69 69 6A 6B 6C 6D 6E 6F 70 71 72 73 Detailed timing/monitor 4E 01001110 74 4C 01001100 76 77 77 78 78 79 7A 7B 7C 7C 68 69 20 00100000 32 [] 20 00100000 32 [] 20 00100000 32 [] 20 00100000 32 [] 20 00100000 32 [] 00 00000000 0 0 00000000 0 0 00000000							
68 69 6A 6B 6C 6C 6D 6F 70 71 72 73 Detailed timing/monitor 4E 01001110 75 76 76 77 78 78 79 7A 7B 7C 7C 6A 6B 20 00100000 32 [] 20 00100000 32 [] 00 00000000 0 0 00 00000000 0 0 00 0000							
69 6A 6B 6B 20 00100000 32 [] 6C 6C 6D 6E 6F 70 71 72 73 Detailed timing/monitor 4E 0101110 75 76 77 78 78 79 7A 7B 7C 7C 20 00100000 32 [] 00 00000000 0 0 00000000 0 0 0 0000000							
6A 6B 20 00100000 32 [] 6B 20 00100000 32 [] 6C 6C 6D 6E 6E 6E 70 000000000 0 0 00000000 0 0 0 0000000							
6B							
6C 6D 6E 6F 70 71 72 73 Detailed timing/monitor 4E 01001110 74 descriptor #4 4E 01001110 75 76 77 78 79 7A 7B 7C 00 00000000 0 0 00000000 0 0 0 0 00000							
6D 6E 6F 70 71 72 73 Detailed timing/monitor	6B		20	00100000	32	[]	
6E 6F 70 71 72 73 Detailed timing/monitor 4E 01001110 78 [N] 75 76 77 78 78 79 7A 78 78 77 78 78 76 77 78 78 77 78 78 77 78 78 78 77 78 78	6C		00	00000000	0		
6F 70 70 71 71 4C 01001100 76 [L] 72 54 01010100 84 [T] 73 Detailed timing/monitor 4E 01001110 78 [N] 74 descriptor #4 31 00110001 49 [1] 75 34 00110001 49 [1] 76 31 00110001 49 [1] 77 57 01010111 87 [M] 78 31 00110001 49 [1] 7A 4C 01001100 76 [L] 7B 30 00110000 48 [0] 7C 36 00110110 54 [6]	6D		00	00000000	0		
70 71 71 72 73 Detailed timing/monitor 4E 01010100 84 [T] 74 descriptor #4 31 00110001 49 [1] 75 34 00110100 52 [4] 76 31 00110001 49 [1] 77 78 31 00110001 49 [1] 78 31 00110001 49 [1] 79 31 00110001 45 [-] 7A 4C 01001100 76 [L] 7B 30 00110000 48 [0] 7C 36 00110110 54 [6]	6E		00	00000000	0		Monitor Name Tag (ASCII)
71 72 54 01001100 76 [L] 73 Detailed timing/monitor 4E 01001110 78 [N] 74 descriptor #4 31 00110001 49 [1] 75 34 00110001 49 [1] 76 31 00110001 49 [1] 77 57 01010111 87 [W] 78 31 00110001 49 [1] 79 2D 00101101 45 [-] 7A 4C 01001100 76 [L] 7B 30 00110000 48 [0] 7C 36 00110110 54 [6]	6F		FE	11111110	254		
72 Detailed timing/monitor 54 01010100 84 [T] 73 Detailed timing/monitor 4E 01001110 78 [N] 74 descriptor #4 31 00110001 49 [1] 75 34 00110100 52 [4] 31 00110001 49 [1] 57 01010111 87 [W] 78 31 00110001 49 [1] 2D 00101101 45 [-] 7A 4C 01001100 76 [L] 7B 30 00110000 48 [0] 7C 36 00110110 54 [6]	70		00	00000000	0		
72 54 01010100 84 [T] 73 Detailed timing/monitor 4E 01001110 78 [N] 74 descriptor #4 31 00110001 49 [1] 75 34 00110100 52 [4] 31 00110001 49 [1] 57 01010111 87 [W] 78 31 00110001 49 [1] 79 2D 00101101 45 [-] 7A 4C 01001100 76 [L] 7B 30 00110000 48 [0] 7C 36 00110110 54 [6]	71		4C	01001100	76	[L]	
73	72		54	01010100	84		
75 76 77 78 79 7A 7B 7C 30 30 30 30 30 31 32 33 34 34 35 36 37 36 37 37 38 39 30 30 31 <td>73</td> <td>Detailed timing/monitor</td> <td>4E</td> <td>01001110</td> <td>78</td> <td></td> <td></td>	73	Detailed timing/monitor	4E	01001110	78		
76 77 78 78 79 7A 7B 7C 7C 31 00110001 49 [1] 87 [W] 87 [V] 9 [1]	74	descriptor #4	31	00110001	49	[1]	
77 57 01010111 87 [W] 78 31 00110001 49 [1] 79 2D 00101101 45 [-] 7A 4C 01001100 76 [L] 7B 30 00110000 48 [0] 7C 36 00110110 54 [6]	75		34	00110100	52	[4]	
78 79 7A 7B 30 30 31 31 45 6 6 7B 36 36 37 38 39 30	76		31	00110001	49	[1]	
79 7A 7B 7C 2D 00101101 45 [-] 4C 01001100 76 [L] 30 00110000 48 [0] 7C	77		57	01010111	87	[W]	
7A	78						
7B 30 00110000 48 [0] 7C 36 00110110 54 [6]							
7C 36 00110110 54 [6]							
7D 00004040 40 M							
	7D		0A	00001010	10	[^]	
7E Extension Flag 00 00000000 0	7E	Extension Flag	00	00000000	0		
7F Checksum 64 01100100 100	7F	Checksum	64	01100100	100		

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