( ) Preliminary Specifications
(V) Final Specifications

Module	**14.0" HD+ Color TFT-LCD with LED Backlight Displayport interface design**
Model Name	B140RW01 V2 (H/W:1A)
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
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Note: This Specification is subject to change without notice.		**NBBU Marketing Division / AU Optronics corporation**	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2008/12/26	ALL	First Edition for Customer		
0.2 2009/02/09	ALL		Create display port interface	
0.3 2009/02/09	ALL		Create display port interface	
	18		Increase signal cable impedance request	
	32	H/W: 0A	H/W: 1A	
0.4 2009/09/15	32		Revise shipping label	
0.5 2009/10/ 07	35		Revise EDID	
0.6 2010/03/02	17		Revise T2 T3 T9	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electronic breakdown.

2. General Description

B140RW01 V2 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the HD (1600(H) x 900(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B140RW01 V2 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

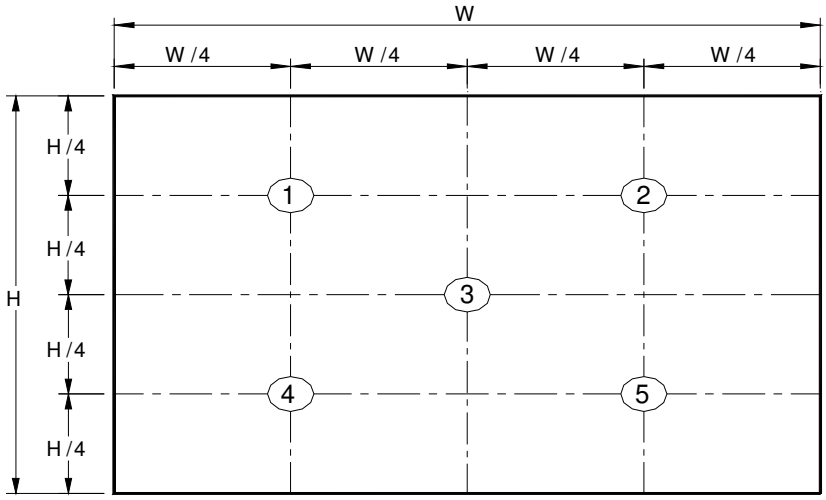
Items	Unit	Specifications			
Screen Diagonal	[mm]	354.95 (14.0W")			
Active Area	[mm]	309.60 X 174.15			
Pixels H x V		1600x3(RGB) x 900			
Pixel Pitch	[mm]	0.1935X0.1935			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (ILED=20mA) (Note: ILED is LED current)	[cd/m^2]	200 typ. (5 points average) 170 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		400 typ			
Response Time	[ms]	8 typ / 12 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	5.5 max. (Include Logic and Blu power)			
Weight	[Grams]	375 max.			
Physical Size without inverter, bracket.	[mm]		Min.	Typ.	Max.
		Length	323	323.5	324
		Width	191.5	192	192.5
		Thickness			5.2
Electrical Interface		eDP 1 Main Link Differential Pair			
Surface Treatment		Anti-Glare, Hardness 3H,			
Support Color		262K colors (RGB 6-bit)			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

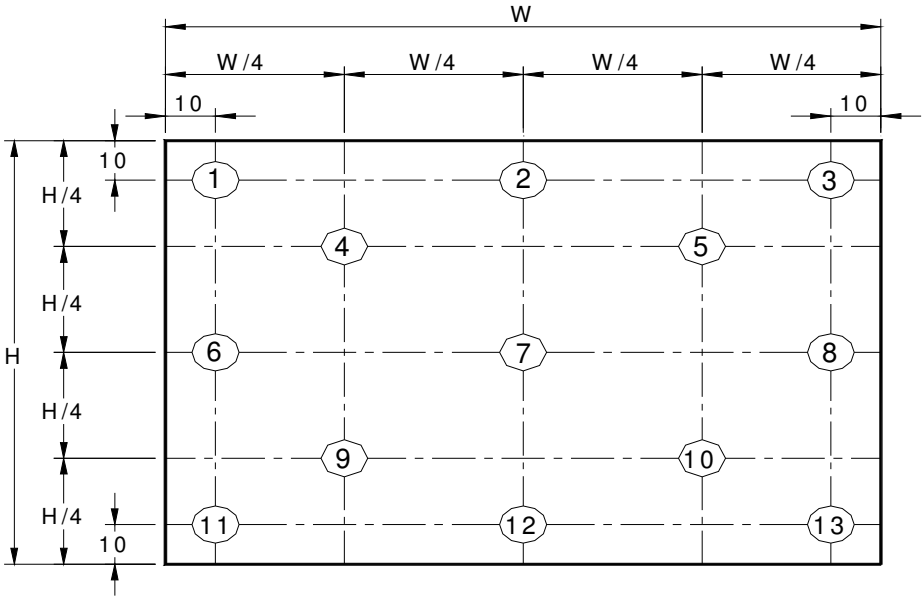
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=20mA			5 points average	170	200	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	40 40	45 45	- -	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	10 30	15 35	- -		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.50		2, 3, 4
Contrast Ratio		CR		300	400	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_r	Rising	-		-	msec	4, 8
		T_f	Falling	-		-		
		T_{RT}	Rising + Falling	-	8	12		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.590	0.620	0.650		4
		Ry		0.310	0.340	0.370		
	Green	Gx		0.300	0.330	0.360		
		Gy		0.540	0.570	0.600		
	Blue	Bx		0.120	0.150	0.180		
		By		0.030	0.060	0.090		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	45	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

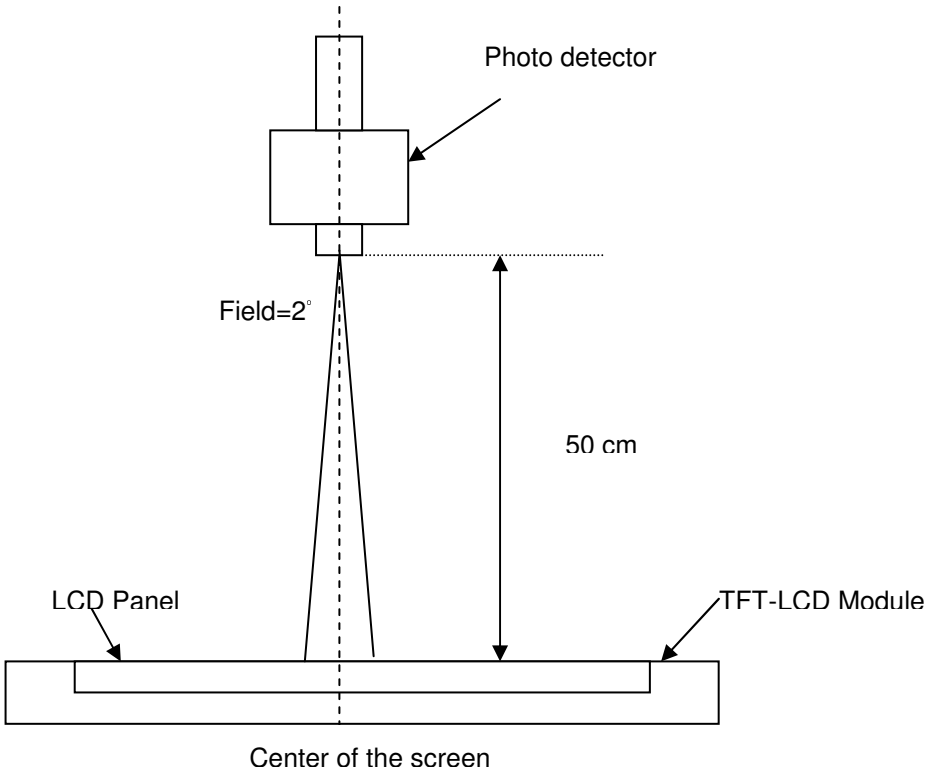
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

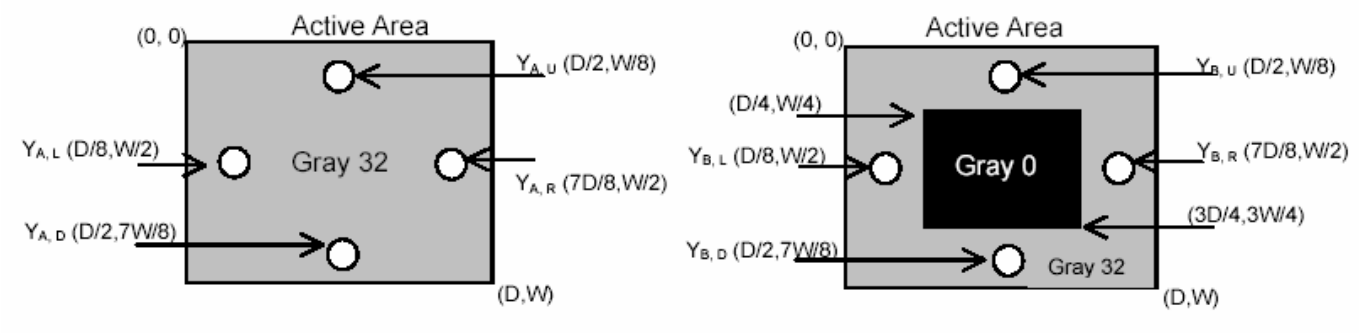
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where

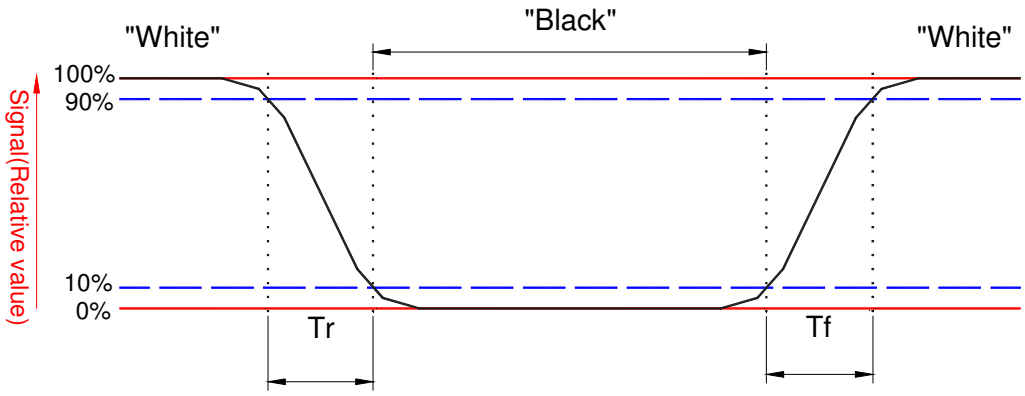
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



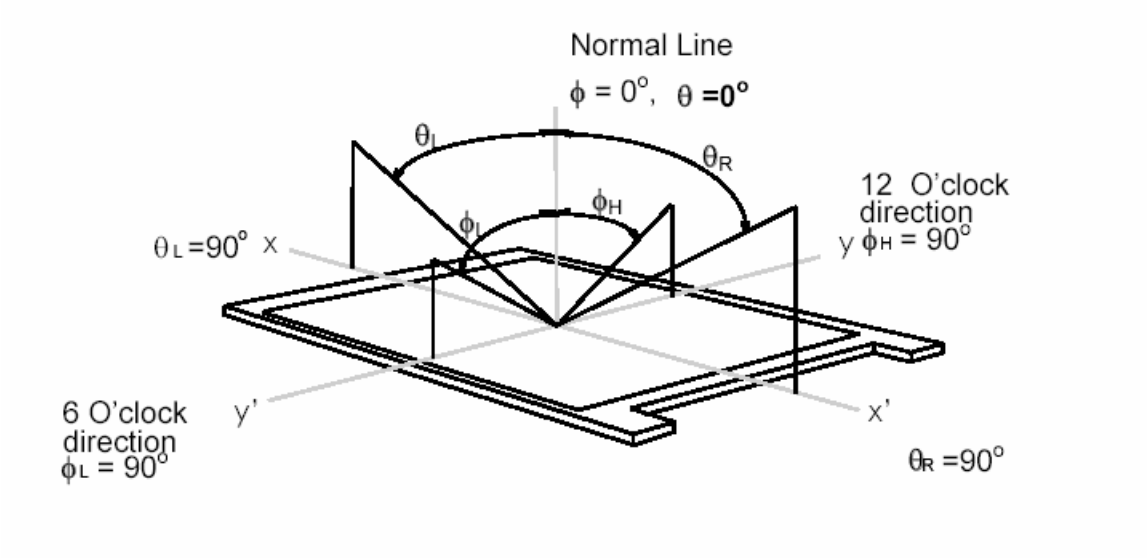
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



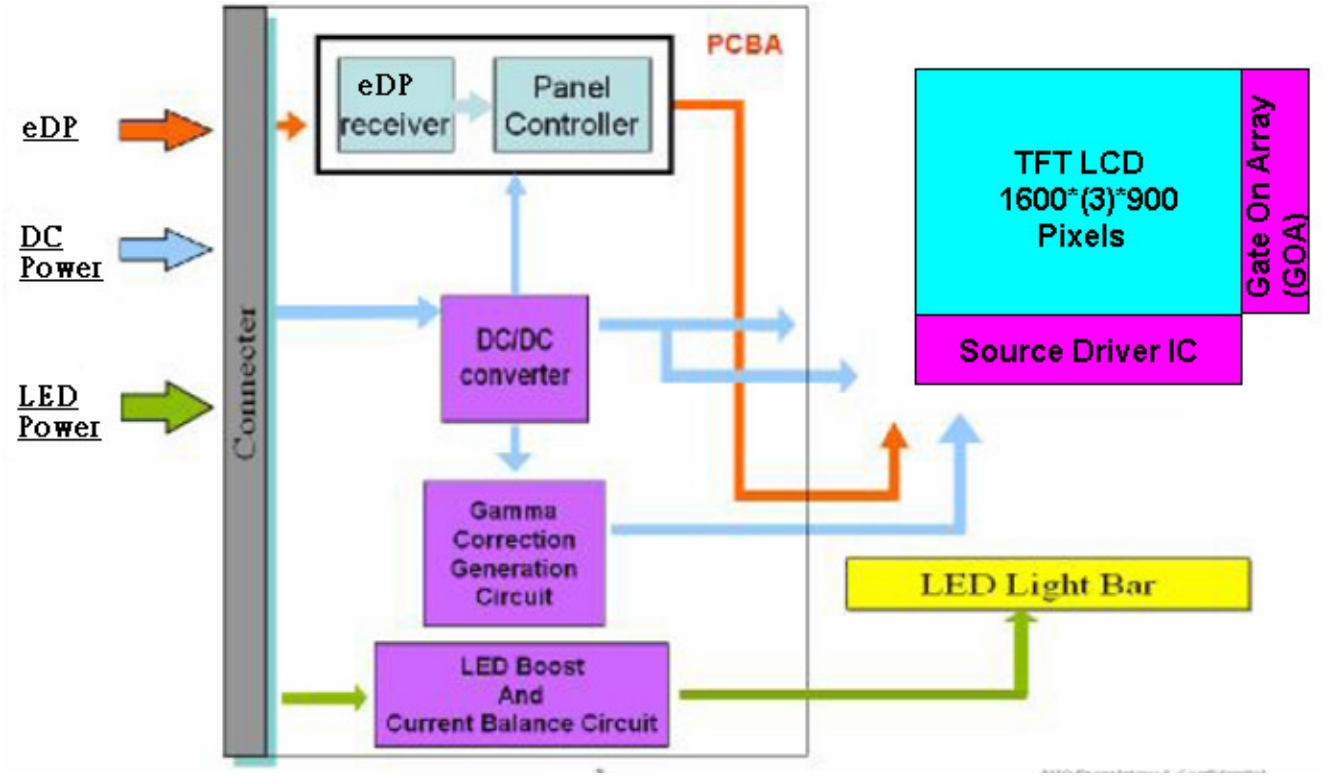
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 30 Pin (**1 main link differential pair** / connector Module)



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

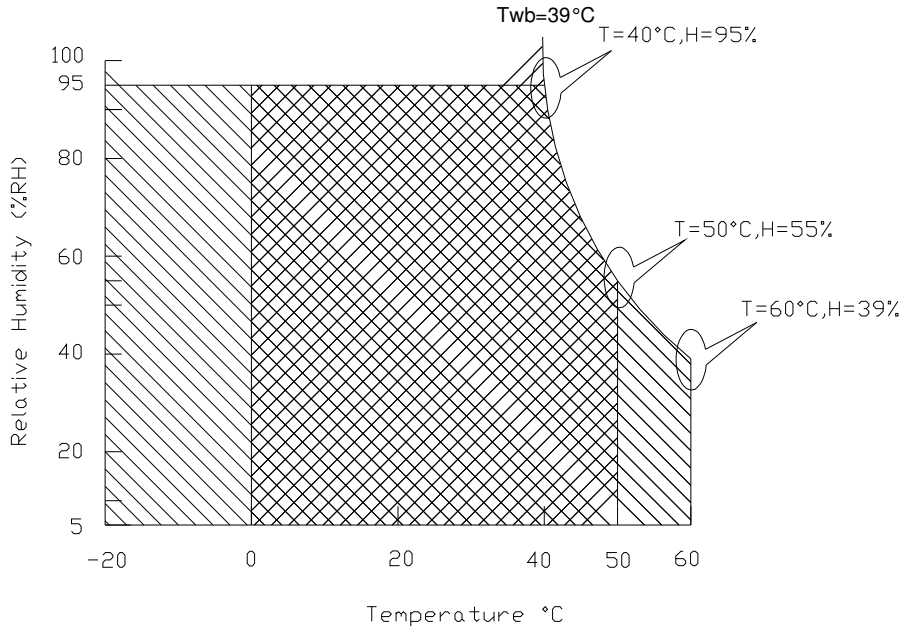
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	10	90	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	10	90	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

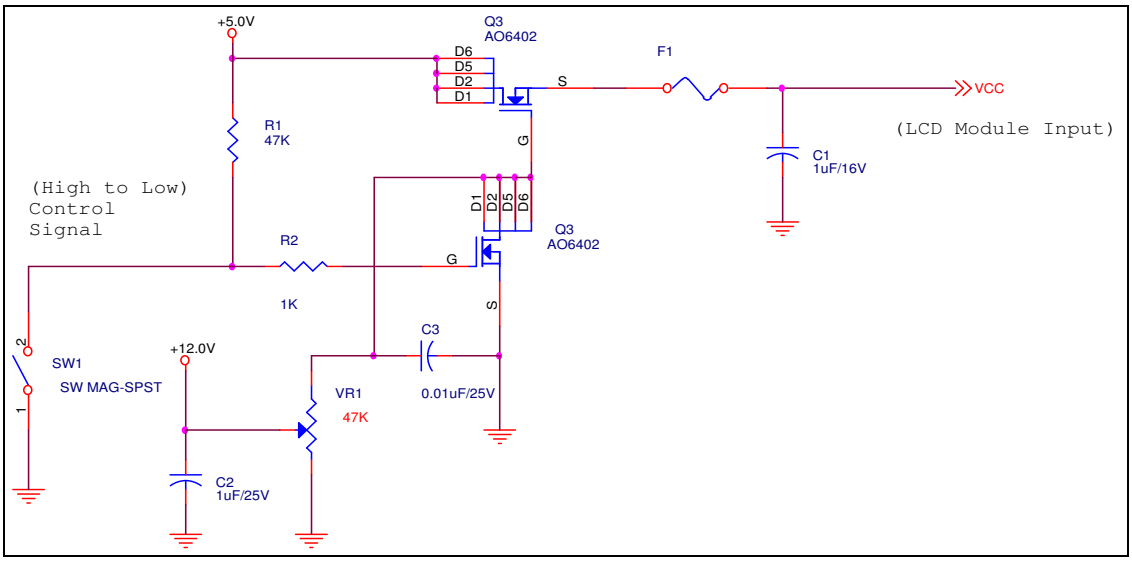
The power specification are measured under 25℃ and frame frenquency under 60Hz

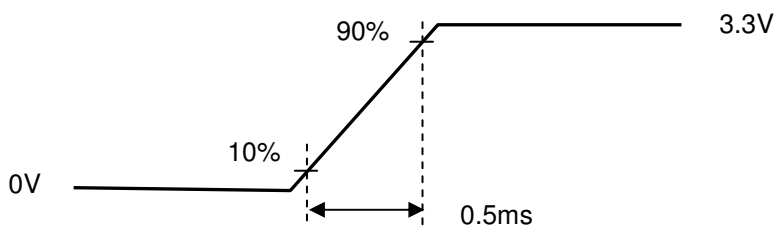
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	2		[Watt]	Note 1/2
IDD	IDD Current	-	364	467	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Typical Measurement Condition: Mosaic Pattern

Note 3 : Measure Condition





Vin rising time

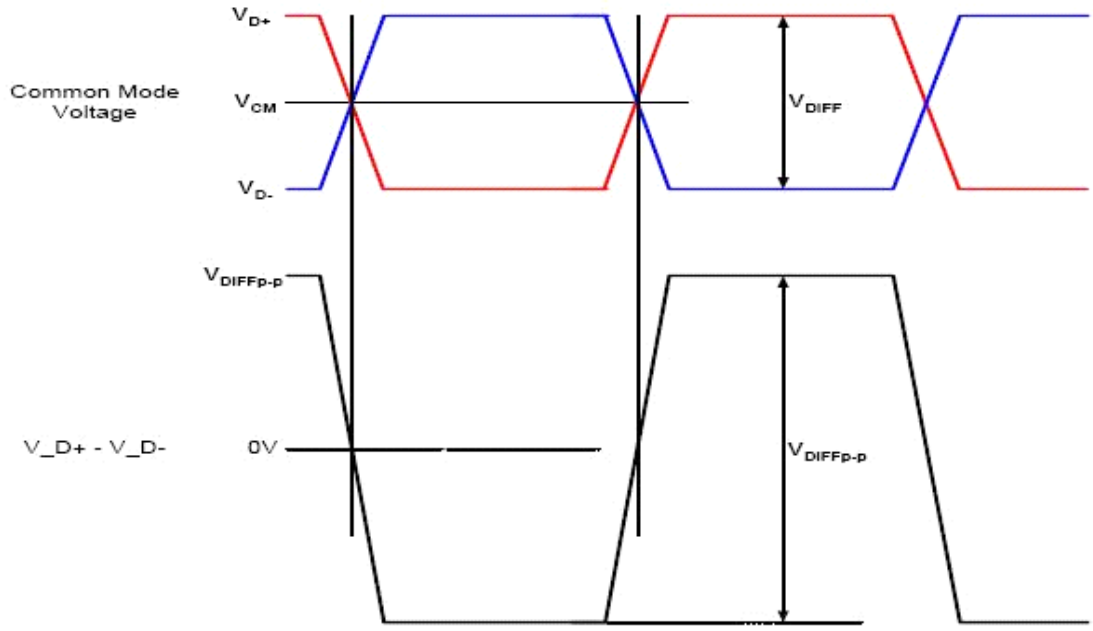
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of VESA Display Port Standard V1.1a in detail.

Signal electrical characteristics are as follows;

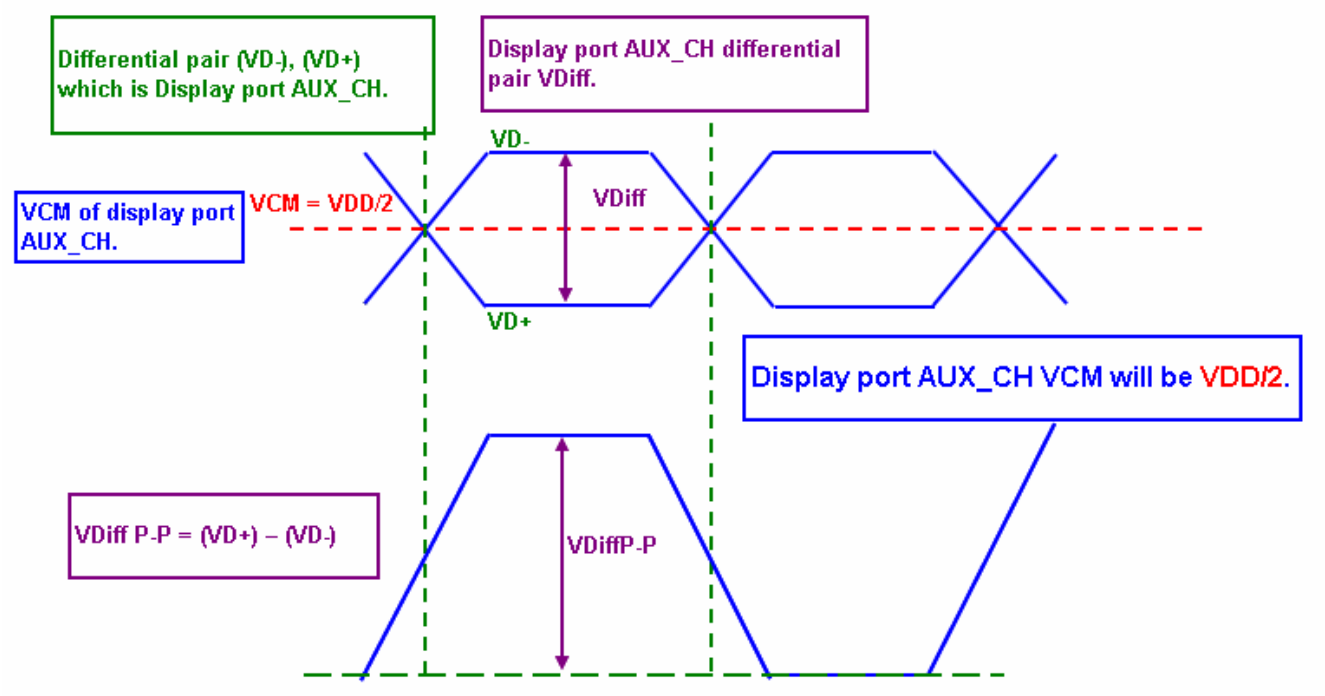
Display Port main link signal:



Display Port main link					
		Min	Typ	Max	unit
VCM	Differential common mode voltage	---	0	---	V
VDiffP-P level1	Differential peak to peak voltage level1	0.34	0.4	0.46	V
VDiffP-P level2	Differential peak to peak voltage level2	0.51	0.6	0.68	V
VDiffP-P level3	Differential peak to peak voltage level3	0.69	0.8	0.92	V
VDiffP-P level4	Differential peak to peak voltage level4	1.02	1.2	1.38	V

Fallow as VESA display port standard V1.1a at both 1.62 and 2.7Gbps link rates.

Display Port AUX_CH signal:



Display Port AUX_CH					
		Min	Typ	Max	unit
VCM	Differential common mode voltage	0	VDD/2	2	V
VDiffP-P	Differential peak to peak voltage	0.39		1.38	V

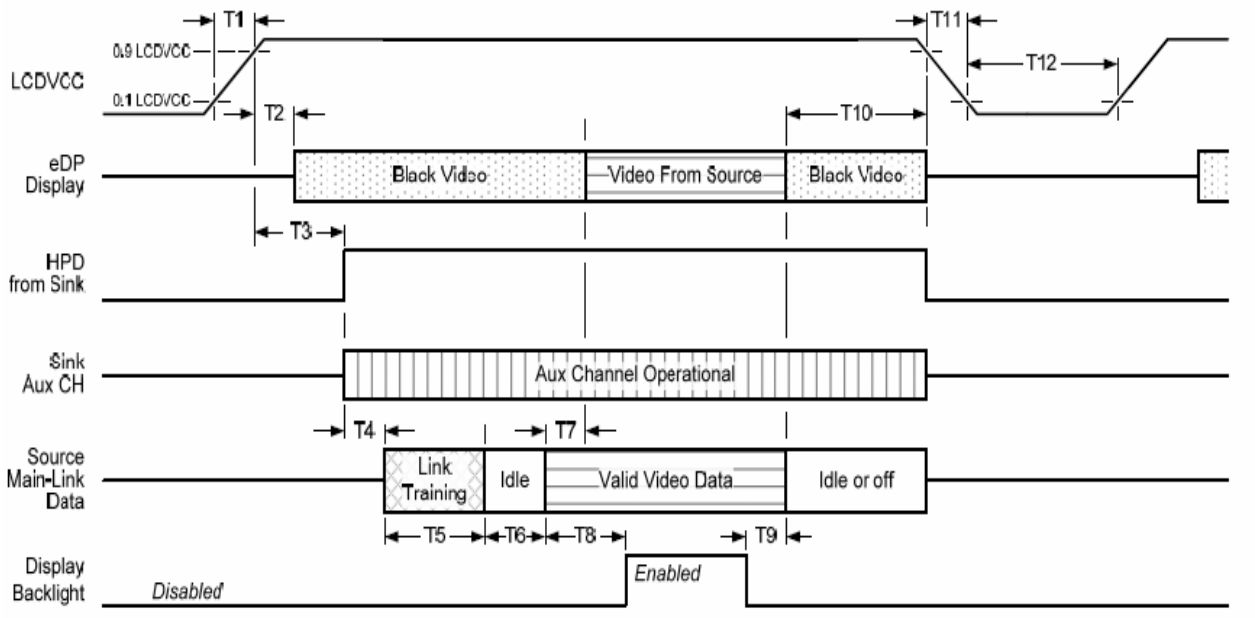
Fallow as VESA display port standard V1.1a.

Display Port V_{HPD} signal:

Display Port V_{HPD}					
		Min	Typ	Max	unit
V_{HPD}	HPD voltage	2.25		3.6	V

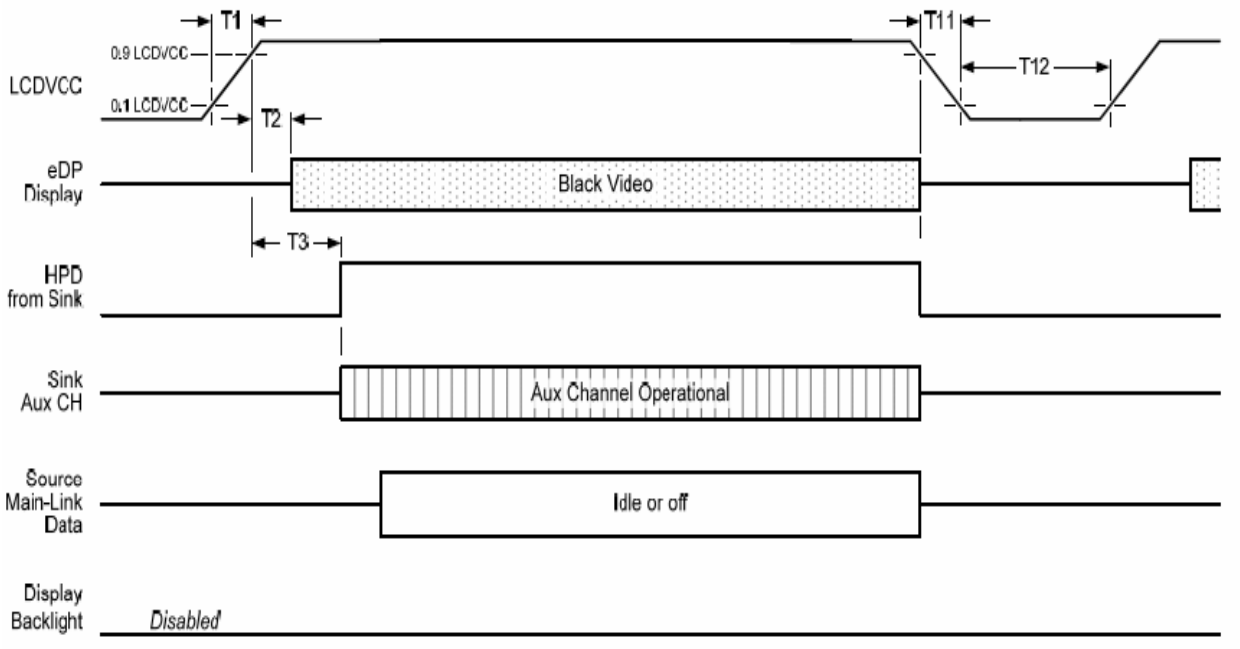
Fallow as VESA display port standard V1.1a.

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note 1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)
-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 50ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

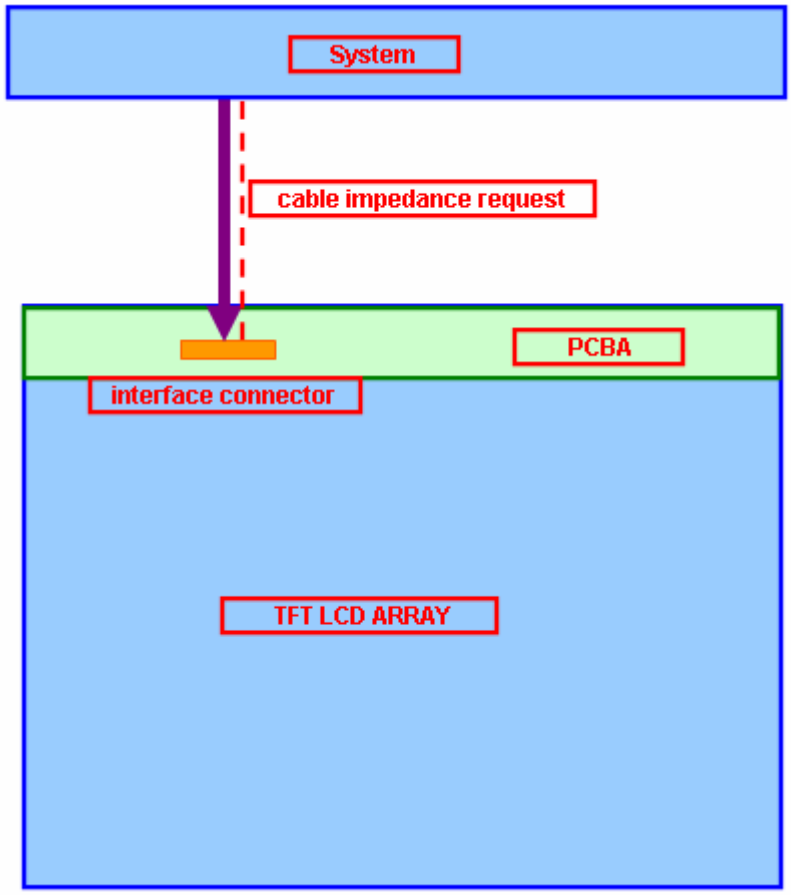
Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port signal cable impedance request:

Signal cable impedance:

The variation of the cable impedance must be within 100ohms +/-15% from a system to a panel connector.

Parameter	Condition	Min.	Typ.	Max.	Unit
Cable impedance	System to panel connector	85	100	115	Ohm



5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	3.21	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	10000	-	-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

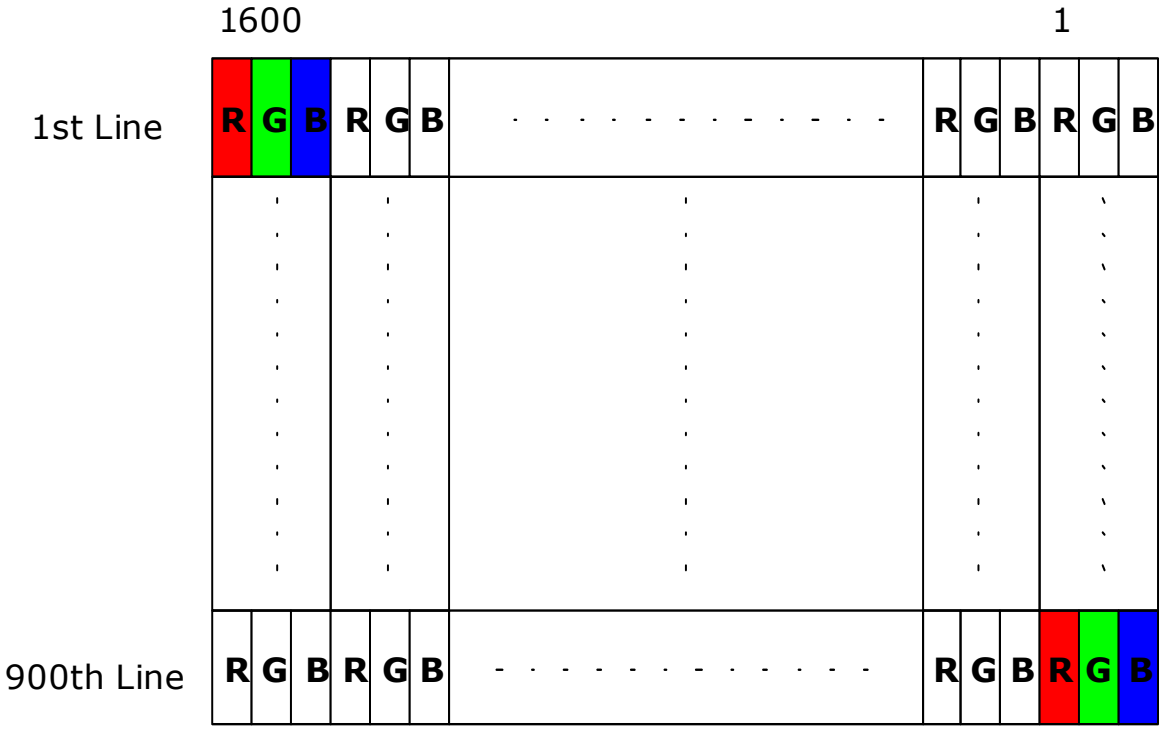
5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	100	-	20K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

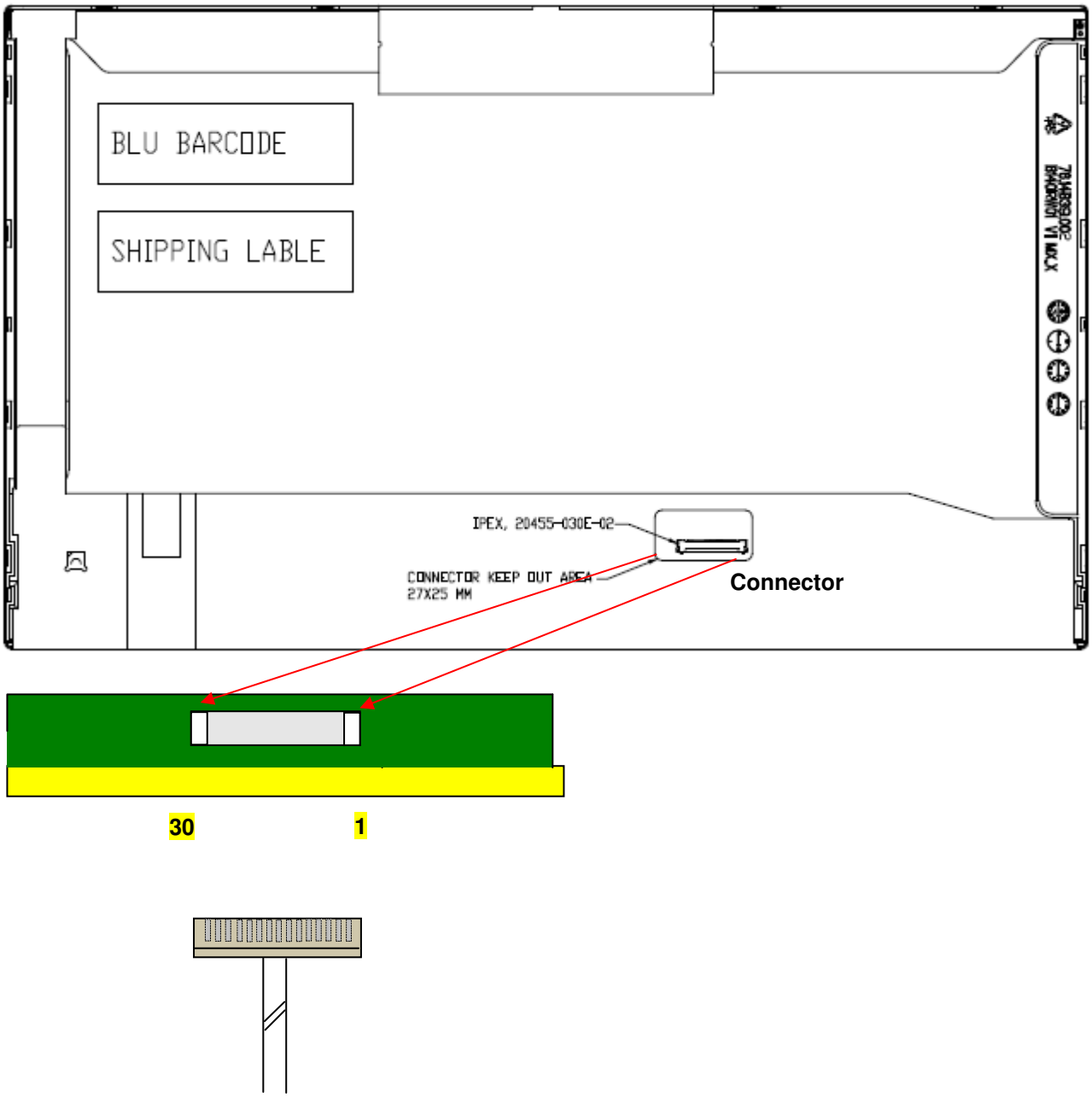


6.2 Integration Interface and Pin Assignment

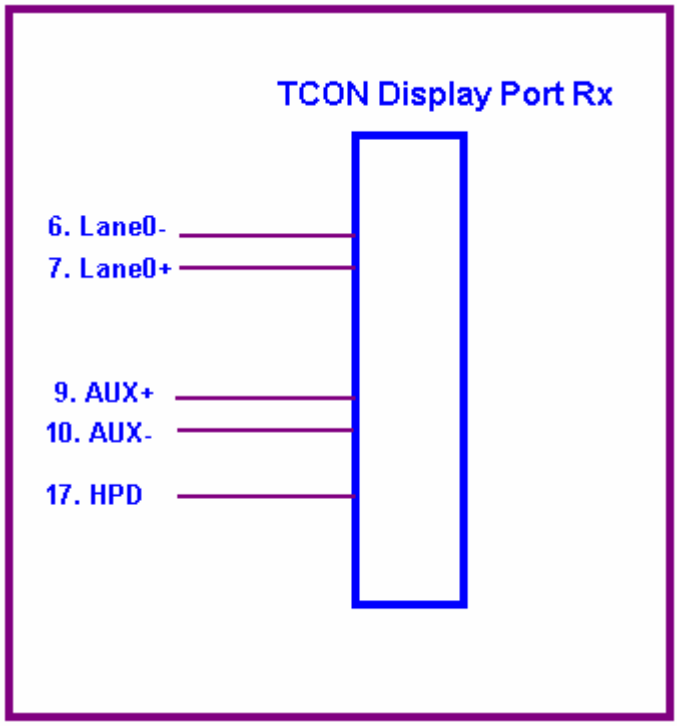
eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	No Connection
2	NC	No Connection
3	NC	No Connection
4	NC	No Connection
5	H_GND	High Speed Ground
6	Lane0_N	Complement Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Complement Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	Self Test (BIST)	Built-In Self Test (active high)
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	HPD	HPD signal pin (Hot Plug Detect)
18	BL_GND	Back light_ground
19	BL_GND	Back light_ground
20	BL_GND	Back light_ground
21	BL_GND	Back light_ground
22	BL_ENABLE	Backlight On/off
23	BL PWM DIM	System PWM signal input for dimming
24	NC-Reserved	Reserved for LCD manufacture's use
25	NC-Reserved	Reserved for LCD manufacture's use
26	BL_PWR	Backlight power
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	NC	No Connection

Note1: Start from right side

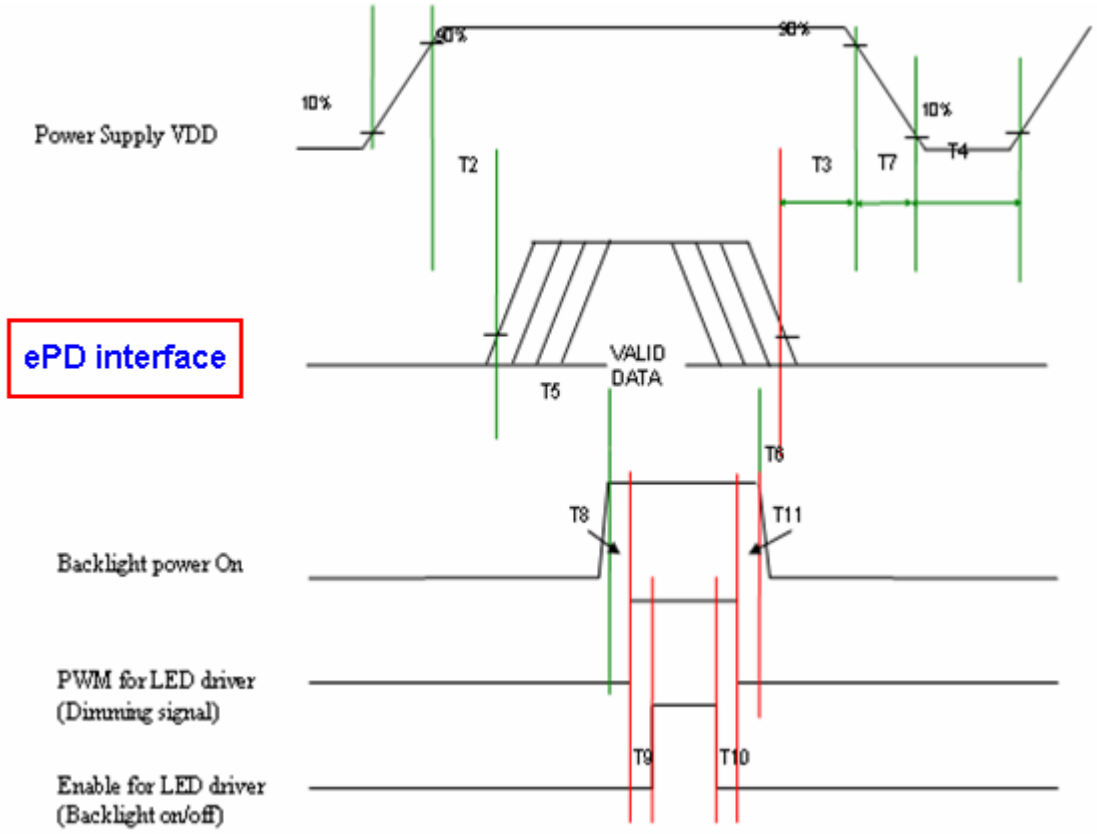


Note2: Input signals shall be low or High-impedance state when VDD is off.
internal circuit of eDP inputs are as following.


TCON Display Port Rx
6. Lane0-
7. Lane0+
9. AUX+
10. AUX-
17. HPD

6.3 Power ON/OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	5	-	50	(ms)
T3	0.5	-	50	(ms)
T4	400	-	-	(ms)
T5	300	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)
T8	10	---	---	(ms)
T9	10	---	---	(ms)
T10	0	---	---	(ms)
T11	10	---	---	(ms)

6.4 Interface Timing

6.4.1 Timing Characteristics

Basically, interface timings should match the 1600X900 / 60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		$1/T_{Clock}$	25	53.9	208	MHz
Vertical Section	Period	T_V	902	-	-	T_{Line}
	Active	T_{VD}	900			
	Blanking	T_{VB}	2	-	-	
Horizontal Section	Period	T_H			4095	T_{Clock}
	Active	T_{HD}	1600			
	Blanking	T_{HB}	10	370	2495	

Note : DE mode only

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX
Type / Part Number	**IPEX 20455-030E-12R or compatible**
Mating Housing/Part Number	IPEX 20453-030T-01 or compatible

8. LED Driving Specification

8.1 Connector Description

It is a intergrative interface and comibe into eDP connector. The type and mating refer to section 7.

8.2 Pin Assignment

Ref. to 6.3

9. Vibration and Shock Test

9.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

9.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

10. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 300h	
Low Temperature Storage	Ta= -20℃, 250h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

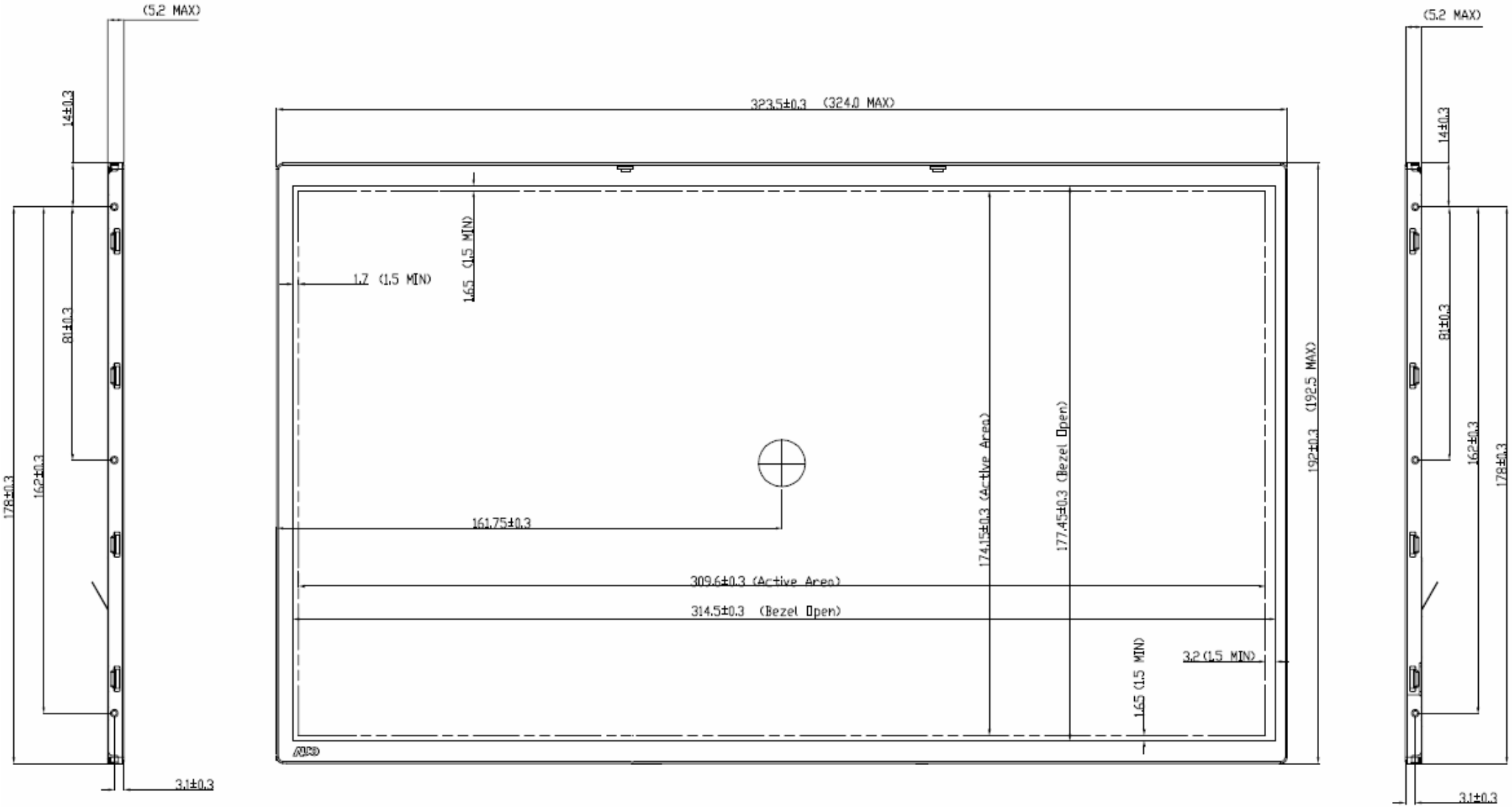
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

. Self-recoverable. No hardware failures.

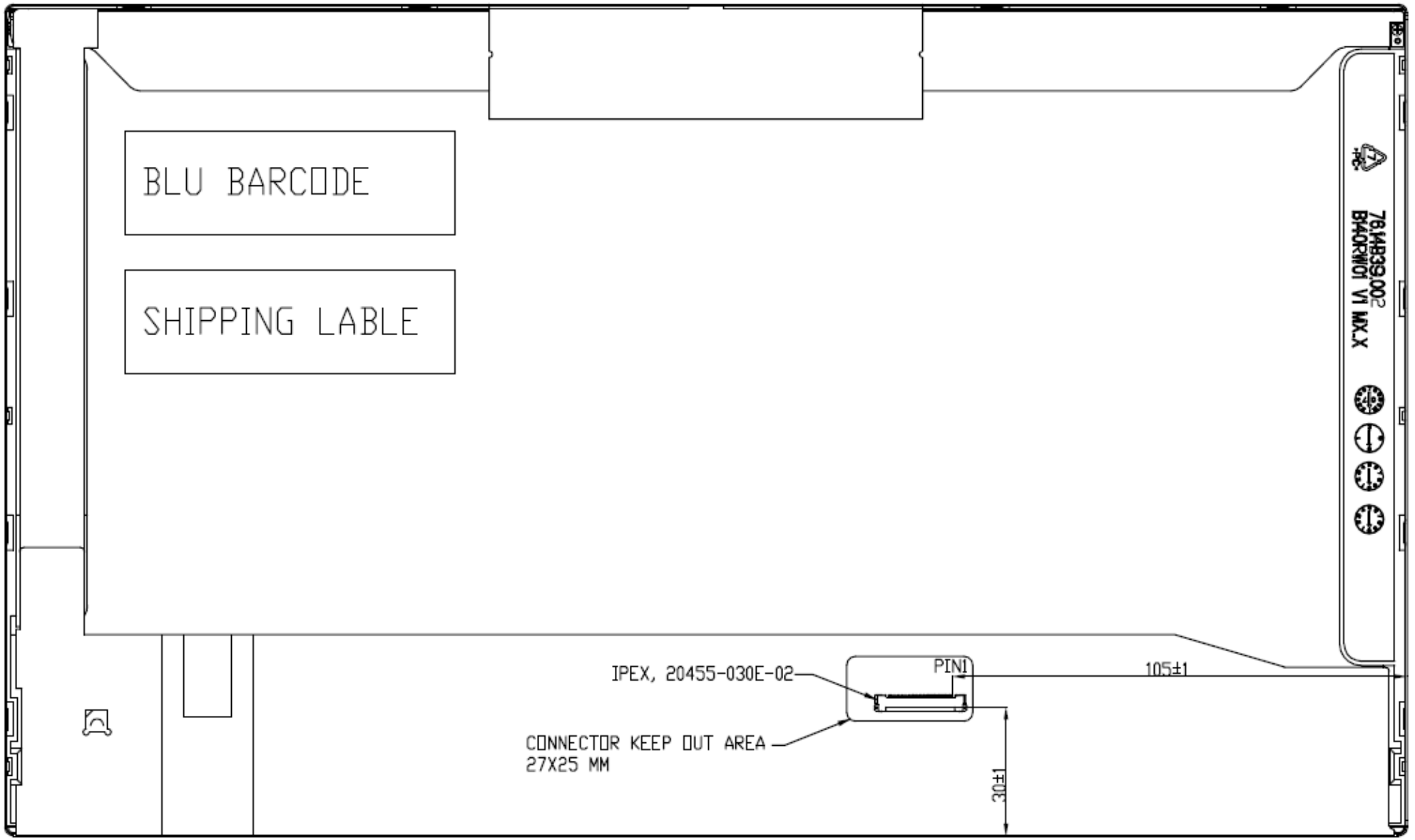
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

11. Mechanical Characteristics

11.1 LCM Outline Dimension



Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

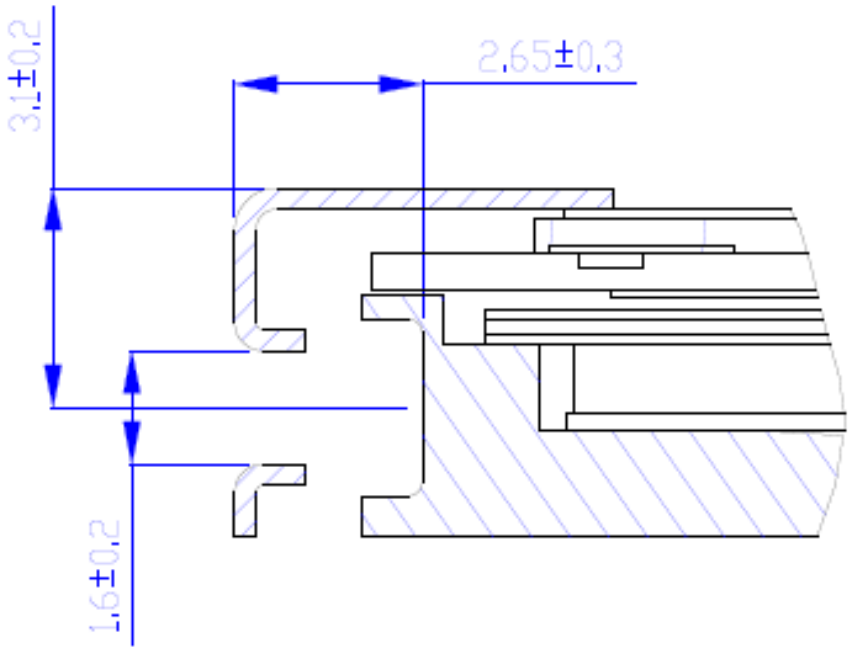


Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

11.2 Screw Hole Depth and Center Position

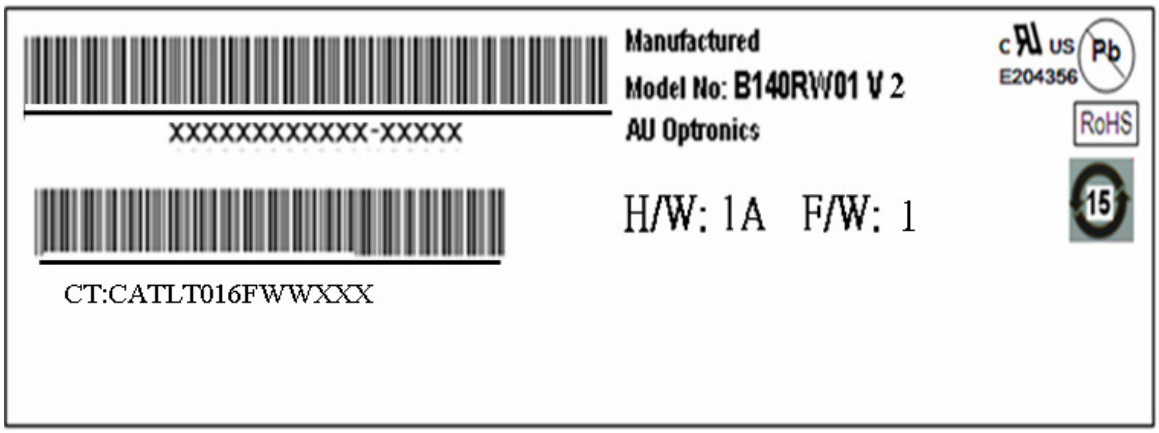
Screw hole maximum depth, from side surface = 2.65 mm (see drawing)

Screw hole center location, from front surface = 3.1 ± 0.2mm (See drawing)
Screw Torque: Maximum 2.5 kgf-cm

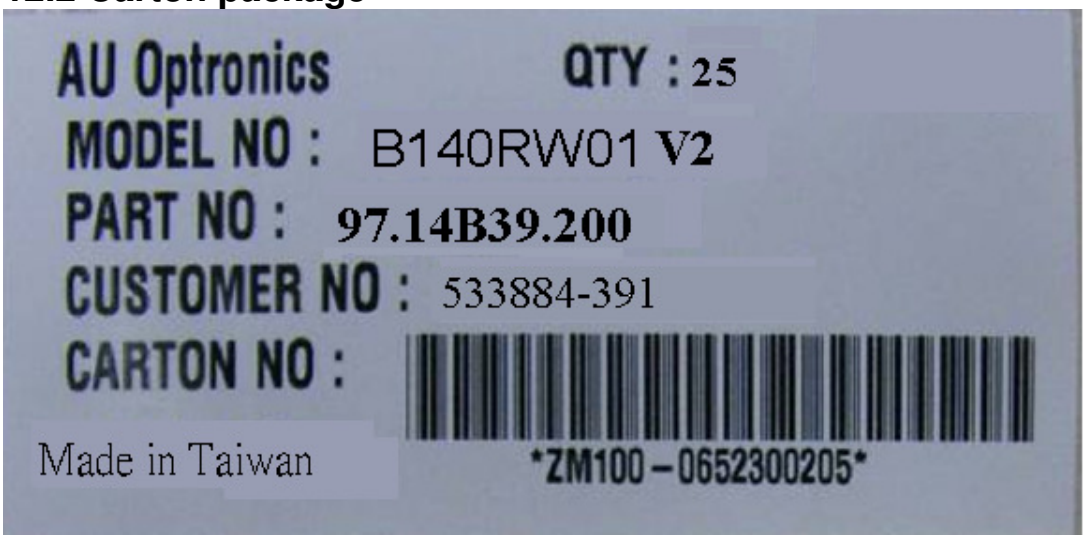


12. Shipping and Package

12.1 Shipping Label Format



12.2 Carton package



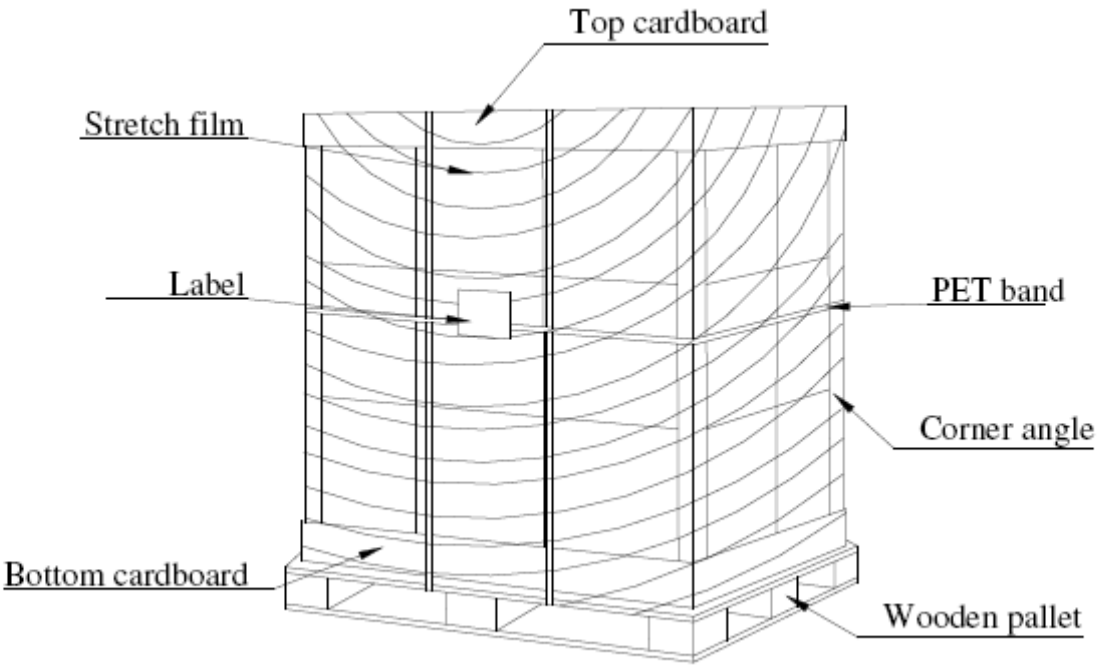
The outside dimension of carton is 405(L)mm* 376(W)mm* 302(H)mm, carton and cushion weight are 2200g.

12.3 Shipping package of palletizing sequence

The outside dimension of Pallet is 114(L)mm* 83(W)mm* 13.8(H)mm

By air：6 * 4 layers, one pallet put 24 boxes, total 600 pcs module.

By sea：6 * 6 layers, one pallet put 36 boxes, total 900 pcs module.



13. Appendix: EDID description 0928 Checksum = C1

B140RW01 V2 EDID Code

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	3E	00111110	62	
0B	hex, LSB first	12	00010010	18	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	13	00010011	19	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	95	10010101	149	
15	**Max H image size** *(rounded to cm)*	1F	00011111	31	
16	**Max V image size** *(rounded to cm)*	11	00010001	17	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	C8	11001000	200	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	95	10010101	149	
1B	Red x **(Upper 8 bits)**	9E	10011110	158	
1C	Red y/ highER 8 bits	57	01010111	87	
1D	Green x	54	01010100	84	
1E	Green y	92	10010010	146	
1F	Blue x	26	00100110	38	
20	Blue y	0F	00001111	15	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	

29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	1C	00011100	28	
37	Pixel Clock/10000 USB	2A	00101010	42	
38	Horz active **Lower 8bits**	40	01000000	64	
39	Horz blanking **Lower 8bits**	72	01110010	114	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	61	01100001	97	
3B	Vertical Active **Lower 8bits**	84	10000100	132	
3C	Vertical Blanking **Lower 8bits**	0C	00001100	12	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30	00110000	48	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	DC	11011100	220	
40	VertSync.Offset : VertSync.Width	44	01000100	68	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	35	00110101	53	
43	Vertical Image Size **Lower 8bits**	AE	10101110	174	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Pixel Clock/10,000 (LSB)	13	00010011	19	
49	Pixel Clock/10,000 (MSB)	1C	00011100	28	40Hz frame rate
4A	Horizontal Addressable Pixels, lower 8 bits	40	01000000	64	
4B	Horizontal Blanking Pixels, lower 8 bits	72	01110010	114	
4C	H Pixels, upper nibble : H Blanking, upper nibble	61	01100001	97	
4D	Vertical Addressable Lines, lower 8 bits	84	10000100	132	
4E	Vertical Blanking Lines, lower 8 bits	0C	00001100	12	
4F	V lines, upper nibble : V blanking, upper nibble	30	00110000	48	
50	Horizontal Front Porch, lower 8 bits	30	00110000	48	
51	Horizontal Sync Pulse, lower 8 bits	DC	11011100	220	
52	V Front Porch, lower nibble : V Sync Pulse, lower nibble	44	01000100	68	
53	VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits	00	00000000	0	
54	Horizontal Image Size in mm, lower 8 bits	35	00110101	53	

55	Vertical Image Size in mm, lower 8 bits	AE	10101110	174	
56	H Image Size, upper nibble : V Image Size, upper nibble	10	00010000	16	
57	Horizontal Border	00	00000000	0	
58	Vertical Border	00	00000000	0	
59	Bit Encode Sync Information	18	00011000	24	
5A	DC	00	00000000	0	
5B	HTOTAL	00	00000000	0	
5C	HA	00	00000000	0	
5D	HBL	00	00000000	0	
5E	HFP	00	00000000	0	
5F	HFPe	00	00000000	0	
60	HBP	00	00000000	0	
61	HB	00	00000000	0	
62	HSO	00	00000000	0	
63	HS	00	00000000	0	
64	VTOTAL	00	00000000	0	
65	VA	00	00000000	0	
66	VBL	00	00000000	0	
67	VFP	00	00000000	0	
68	VBP	00	00000000	0	
69	VB	00	00000000	0	
6A	VSO	00	00000000	0	
6B	VS	00	00000000	0	
6C	Detailed time decription #4	00	00000000	0	
6D	Flags	00	00000000	0	
6E	Reserved	00	00000000	0	
6F	For Brightness table and Power consumption	02	00000010	2	
70	Flags	00	00000000	0	
71	PWM % [7:0] @ STEP 0	0C	00001100	12	5%
72	PWM % [7:0] @ STEP 5	3F	00111111	63	25%
73	PWM % [7:0] @ STEP 10	CC	11001100	204	80%
74	Nits [7:0] @ STEP 0	0A	00001010	10	10nits
75	Nits [7:0] @ STEP 5	3C	00111100	60	60nits
76	Nits [7:0] @ STEP 10	64	01100100	100	200nits
77	Panel Electronics Power @ 32X32 Chess Pattern	21	00100001	33	1320mW
78	Backlight Power @ 60nits	12	00010010	18	720mW
79	Backlight Power @ step10	24	00100100	36	2880mW
7A	Nits @ 100% PWM duty	7D	01111101	125	250nits
7B	Flags	20	00100000	32	
7C	Flags	20	00100000	32	
7D	Flags	20	00100000	32	
7E	Extension Flag	00	00000000	0	
7F	Checksum	C1	11000001	193	
			SUM	6400	

SUM to HEX	1900