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# **Product Specification**

Color TFT-LCD module MODEL NAME: <u>A085FW01 V7</u>

( ◆ ) Preliminary Specification( ..... ) Final Specification

Note: The content of this specification is subject to change.

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## Record of Revision

Version	Revise Date	Page	Content
0.0	25/Jan/2007		First draft.
0.1	16/Mar/2007	6	Add max. and min. LED lightbar voltage
0.2	4/Jun/2007	6	Update the figure of LED serial/parallel connection
		14	Update outline drawing(back side)
0.3	11/Jul/2007	8	Add a note for power off sequence
		<u> </u>	



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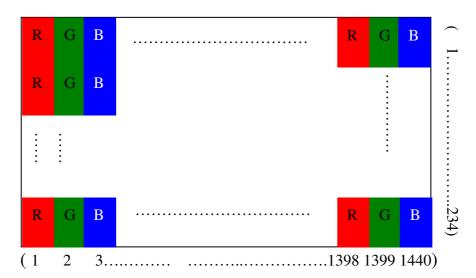


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A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution(dot)	480RGB(W)×234(H)	
2	Active area(mm)	187.2(W)×105.3(H)	
3	Dot pitch(mm)	0.130(W)×0.450(H)	
4	Color configuration	R. G. B. stripe	Note 1
5	Overall dimension(mm)	199.0(W)×119.0(H)×5.8(D)	Note 2
6	Weight(g)	232 ±10	
7	Surface treatment	Anti-Glare	
8	Backlight unit	LED	

Note 1: Below figure shows the dot stripe arrangement.



Note 2: Refer to Fig. 1



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## **B.** Electrical specifications

1.Pin assignment

a. TFT-LCD panel driving section

Pin no	Symbol	I/O	Description	Remark
1	GND	-	Ground for logic circuit	
2	$V_{CC}$	I	Supply voltage of logic control circuit for scan driver	
3	$V_{GL}$	I	Negative power for scan driver	
4	$V_{GH}$	I	Positive power for scan driver	
5	STVD	I/O	Vertical start pulse	Note 1
6	STVU	I/O	Vertical start pulse	Note 1
7	CKV	I	Shift clock input for scan driver	
8	U/D	I	UP/DOWN scan control input	Note 1,2
9	OEV	I	Output enable input for scan driver	
10	VCOM	I	Common electrode driving signal	
11	VCOM	I	Common electrode driving signal	
12	L/R	I	LEFT/RIGHT scan control input	Note 1,2
13	MOD	I	Sequential sampling and simultaneous sampling setting	Note 3
14	OEH	I	Output enable input for data driver	
15	STHL	I/O	Start pulse for horizontal scan line	Note 1
16	STHR	I/O	Start pulse for horizontal scan line	Note 1
17	CPH3	I	Sampling and shifting clock pulse for data driver	
18	CPH2	I	Sampling and shifting clock pulse for data driver	
19	CPH1	I	Sampling and shifting clock pulse for data driver	
20	$V_{CC}$	I	Supply voltage of logic control circuit for data driver	
21	GND	-	Ground for logic circuit	
22	VR	I	Alternated video signal input(Red)	
23	VG	I	Alternated video signal input(Green)	
24	VB	I	Alternated video signal input(Blue)	
25	$AV_DD$	I	Supply voltage for analog circuit	
26	$AV_SS$	-	Ground for analog circuit	

Note 1: Selection of scanning mode (please refer to the following table)

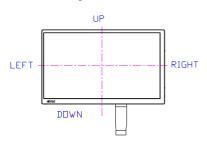
			•			,
Setting of scan control input				T state t pulse		Scanning direction
U/D	L/R	STVD	STVU	STHR	STHL	Journal of the state of the sta
GND	V <sub>cc</sub>	OUT	IN	OUT	IN	From up to down, and from left to right.
V <sub>CC</sub>	GND	IN	OUT	IN	OUT	From down to up, and from right to left.
GND	GND	OUT	IN	IN	OUT	From up to down, and from right to left.
V <sub>CC</sub>	V <sub>CC</sub>	IN	OUT	OUT	IN	From down to up, and from left to right.



IN: Input; OUT: Output.

Note 2: Definition of scanning direction.

Refer to figure as below:



Note 3: MOD = H: Simultaneous sampling.

MOD = L: Sequential sampling.

Please set CPH2 and CPH3 to GND when MOD = H.

#### b. Backlight driving section (Refer to Figure 1)

No.	Symbol	I/O	Description	Remark
1	HI	I	Power supply for backlight unit (High voltage)	
2	GND	-	Ground for backlight unit	

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#### 2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
	$V_{CC}$	GND=0	-0.3	7	V	
	$AV_DD$	AV <sub>SS</sub> =0	-0.3	7	V	
Power voltage	$V_{GH}$	0110 0	-0.3	18	V	
	$V_{GL}$	GND=0	-15	0.3	V	
	$V_{GH} - V_{GL}$		1	33	V	
	$V_{i}$		-0.3	AV <sub>DD</sub> +0.3	V	Note 1
Input signal voltage	VI		-0.3	V <sub>CC</sub> +0.3	V	Note 2
	VCOM		-2.9	5.2	V	

Note 1: VR, VG, VB.

Note 2: STHL, STHR, OEH, L/R, CPH1~CPH3, STVD, STVU, OEV, CKV, U/D.



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#### 3. Electrical characteristics

a. Typical operating conditions (GND=AVss=0V, Note 3)

Item		Symbol	Min.	Тур.	Max.	Unit	Remark
		V <sub>CC</sub>	3	5	5.5	V	
		$AV_DD$	4.5	5	5.5	V	
Power	supply	$V_{GH}$	14.3	15	15.7	V	
		$V_{GL}$	-10.5	-10	-9.5	V	
Video signal		V <sub>iA</sub>	0.4	-	AV <sub>DD</sub> -0.4	V	Note 1
•	itude	$V_{iAC}$	-	3	-	V	AC component
(VH,V	G,VB)	$V_{iDC}$	-	AV <sub>DD</sub> /2	-	V	DC component
V/O	OM	$V_{CAC}$	5.3	5.6	5.9	Vp-p	AC component
VCOM		V <sub>CDC</sub>	1.6	1.9	2.2	V	DC component
Input H Leve		V <sub>IH</sub>	0.8 V <sub>CC</sub>		V <sub>CC</sub>	V	Note 0
signal voltage	L Level	V <sub>IL</sub>	0	-	0.2 V <sub>CC</sub>	V	Note 2

Note 1: Refer to Fig.4- (a).

Note 2: STHL, STHR, OEH, L/R, CPH1~CPH3, STVD, STVU, OEV, CKV, U/D.

Note 3: Be sure to apply GND,  $V_{CC}$  and  $V_{GL}$  to the LCD first, and then apply  $V_{GH}$ .

#### b. Current consumption (GND=AVss=0V)

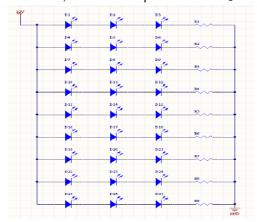
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit	Remark
Current	$I_{GH}$	V <sub>GH</sub> =15V	-	0.20	0.5	mA	
for	I <sub>GL</sub>	V <sub>GL</sub> =-10V	-	0.20	0.5	mA	
driver	I <sub>CC</sub>	V <sub>CC</sub> =5V	-	3.0	6.0	mA	
	I <sub>DD</sub>	AV <sub>DD</sub> =5V	-	15.0	30	mA	

#### c. Backlight driving conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit	Remark
LED lightbar voltage	$V_{L}$	10	12	12	V	Note 1, 2
LED Lightbar current	ΙL	-	225		mA	Note 1, 2
LED Lightbar life time		10,000	-	-	Hr	Note 1, 2, 3

Note 1: LED backlight is 27 pcs of LED lightbar type.

Note 2: Definition of "LED Lifetime": brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25°ℂ and LED voltage = 12V



Note 3: The value is only for reference.

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#### 4. AC Timing

### a. Timing conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit.	Remark
Rising time	t <sub>r</sub>	-	-	10	ns	Note 1
Falling time	$t_f$	-	-	10	ns	Note 1
High and low level pulse width	t <sub>CPH</sub>	99	103	107	ns	CPH1~CPH3
CPH pulse duty	t <sub>cwh</sub>	40	50	60	%	CPH1~CPH3
CPH pulse delay	t <sub>C12</sub> t <sub>C23</sub> t <sub>C31</sub>	30	t <sub>CPH</sub> /3	t <sub>CPH</sub> /2	ns	CPH1~CPH3
STH setup time	t <sub>suh</sub>	20	-	-	ns	STHR, STHL
STH hold time	t <sub>HDH</sub>	20	-	-	Ns	STHR, STHL
STH pulse width	t <sub>STH</sub>	-	1	-	t <sub>CPH</sub>	STHR, STHL
STH period	$t_H$	61.5	63.5	65.5	$\mu$ s	STHR, STHL
OEH pulse width	t <sub>OEH</sub>	-	1.22	-	$\mu$ s	OEH
Sample and hold disable time	t <sub>DIS1</sub>	-	8.28	-	$\mu$ s	
OEV pulse width	$t_{OEV}$	1	5.40	-	$\mu$ s	OEV
CKV pulse width	$t_{\text{CKV}}$	-	4.18	-	$\mu$ s	CKV
Clean enable time	t <sub>DIS2</sub>	-	3.74	-	$\mu$ s	
Horizontal display start	t <sub>SH</sub>	-	0	-	T <sub>CPH</sub> /3	
Horizontal display timing range	t <sub>DH</sub>	-	1440	-	T <sub>CPH</sub> /3	
STV setup time	$t_{\text{SUV}}$	400	-	-	ns	STVU, STVD
STV hold time	$t_{HDV}$	400	-	-	ns	STVU, STVD
STV pulse width	$t_{\text{STV}}$	1	-	1	t <sub>H</sub>	STVU, STVD
Horizontal lines per field	$t_V$	256	262	268	t <sub>H</sub>	Note 2
Vertical display start	$t_{SV}$		3	-	t <sub>H</sub>	
Vertical display timing range	$t_{DV}$		234	-	t <sub>H</sub>	
VCOM rising time	$t_{rCOM}$		-	5	$\mu$ s	
VCOM falling time	t <sub>fCOM</sub>		-	5	$\mu$ s	
VCOM delay time	t <sub>DCOM</sub>		-	3	$\mu$ s	
RGB delay time	t <sub>DRGB</sub>		-	1	$\mu$ s	

Note 1: For all of the logic signals.

Note 2: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

#### b. Timing diagram

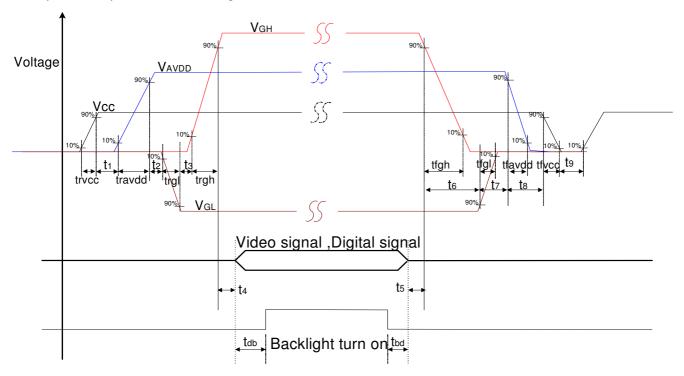
Please refer to the attached drawing, from Fig.2 to Fig.6.



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#### 5. Power Sequence

Sequence for power on/off and Signal on/off



trvcc□15ms(From 10%VCC to 90%VCC ,when VCC is low to high)

travdd ☐ 15ms(From 10%VAVDD to 90%VAVDD ,when VAVDD is low to high)

trgh 15ms(From 10%VGH to 90%VGH ,when VGH is low to high)

trgl□15ms(From 10%VGL to 90%VGL ,when VGL is low to high)

tfvcc 20ms(From 90%VCC to 10%VCC ,when VCC is high to low)

tfavdd 20ms(From 90%VAVDD to 10%VAVDD, when VAVDD is high to low)

tfgh 20ms(From 90%VGH to 10%VGH, when VGH is high to low)

tfgl 20ms(From 90%VGL to 10%VGL, when VGL is high to low)

0 □ t1 □ 10ms(From 90%Vcc to 10% VAVDD, when VCC is low to high)

0 □ t2 □ 10ms(From 90% VAVDD to 10% VGL , when VCC is low to high)

0 □ t3 □ 10ms(From 90% VGL to 10% VGH, when VCC is low to high)

0 □ t4 □ 10ms(From 90% VGH to video signal start ,when VGH is low to high)

0 □ t5 □ 10ms(From video signal end to 90% VGH, when VGH is low to high)

t6□10ms(From 10%VGH to 90% VGL ,when VCC is high to low)

t7□10ms(From 10%VGL to 90% VAVDD, when VCC is high to low)

 $t8 \square 10 ms (From \ 10\% VAVDD \ to \ 90\% \ VCC$  , when VCC is high to low)

t9 □ 0.4s(From 10% VCC is H  $\rightarrow$  L to 10% VCC is L  $\rightarrow$  H)

0 db 10ms(From video signal start to backlight on)

0 □ tbd □ 10ms(From backlight off to video signal end)

Note: Please follow above power off sequence or turn off all power simultaneously.



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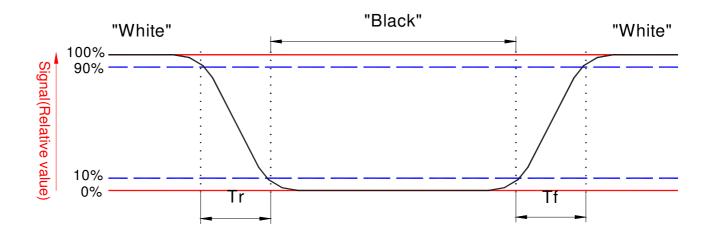
### C. Optical specification (Note 1, Note 2)

Item		Symbol	Condition	Min.	Тур.	Max.	Unit	Remark
Response time	Rise Fall	Tr Tf	$\theta = 0^{\circ}$	-	12 18	24 36	ms ms	Note 3,5
Contrast ra	tio	CR	At optimized Viewing angle	200	300	-		Note 4, 5
Viewing angle	Top Bottom Left Right		CR≧10	40 55 55 55	50 65 65 65	- - -	deg.	Note 5, 6
Brightnes	S	Y <sub>L</sub>	V <sub>L</sub> =12V, 25°℃	180	220	-	cd/m <sup>2</sup>	Note 7
White chromaticity		Х	<i>θ</i> =0°	0.26	0.31	0.36		Note 7
		Υ	$\theta$ =0 $^{\circ}$	0.28	0.33	0.38		

- Note 1 : To be measured in the dark room. Ambient temperature =25 $^{\circ}$ C, and LED lightbar current I<sub>L</sub> = 225 mA.
- Note 2 :To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-7, after 15 minutes operation.
- Note 3. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (falling time) and from "white" to "black" (rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

Contrast ratio (CR)=

Photo detector output when LCD is at "White" state

Photo detector output when LCD is at "Black" state



Note 5. White  $Vi=V_{i50} + 1.5V$ 

Black Vi=V<sub>i50</sub> ± 2.0V

" $\pm$ " means that the analog input signal swings in phase with  $V_{\text{COM}}$  signal.

" $\overline{+}$ " means that the analog input signal swings out of phase with  $V_{COM}$  signal.

 $V_{\text{i50}}$ : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

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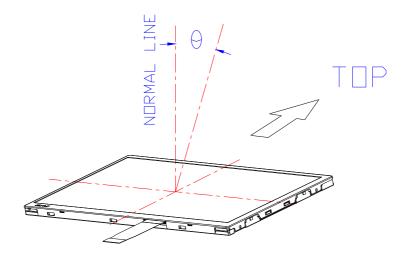
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Note 6. Definition of viewing angle, Refer to figure as below.



Note 7. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.



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## D. Reliability test conditions (Note 2):

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70°C 200Hrs	
2	Low temperature storage	Ta= -20°C 200Hrs	
3	High temperature operation	Tp= 60°C 200Hrs	
4	Low temperature operation	Ta= -10°C 200Hrs	
5	High temperature and high humidity	Tp= 50°C , 80% RH 200Hrs	Operation
6	Heat shock	-30°C∼70°C / 50 cycles 1Hrs/cycle	Non-operation
7	Electrostatic discharge	$\pm$ 200V,200pF(0 $\Omega$ ), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz  Stoke : 1.5mm  Sweep : 10 ~ 55 ~ 10Hz  2 hours for each direction of X,Y,Z  (6 hours for total)	JIS C7021, A-10 Condition A
9	Mechanical shock	100G, 6ms, ±X,±Y,±Z 3 times for each direction	JIS C7021, A-7 Condition C
10	Vibration (with carton)	Random vibration: 0.015G <sup>2</sup> /Hz from 5~200Hz -6dB/octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	JIS Z0202

Note1: Ta: Ambient Temperature.

Note2: Tp: Panel Surface Temperature

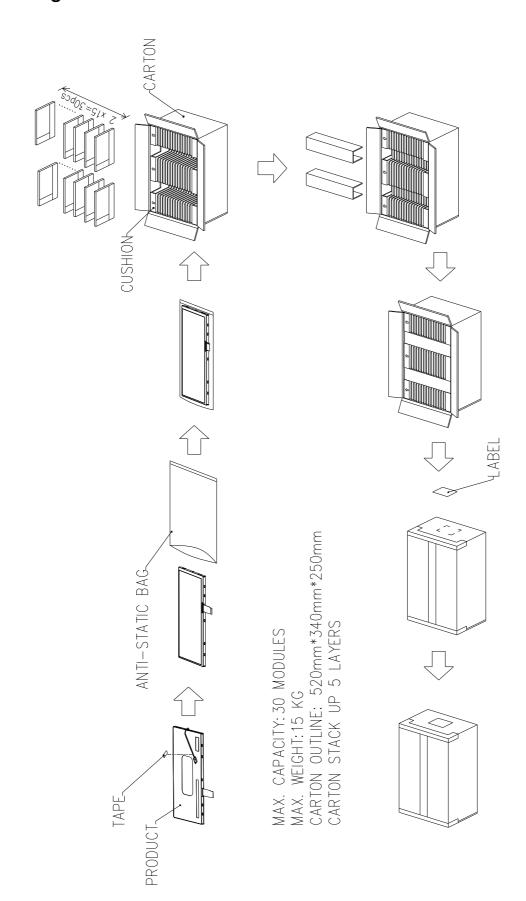
Note3: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.



E. Packing form

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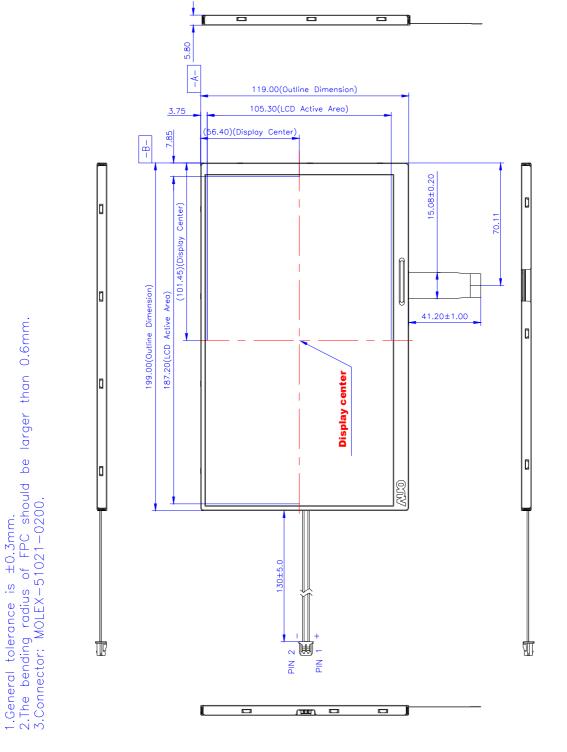


Fig.1-(a) Outline dimension of TFT-LCD module (Front side)



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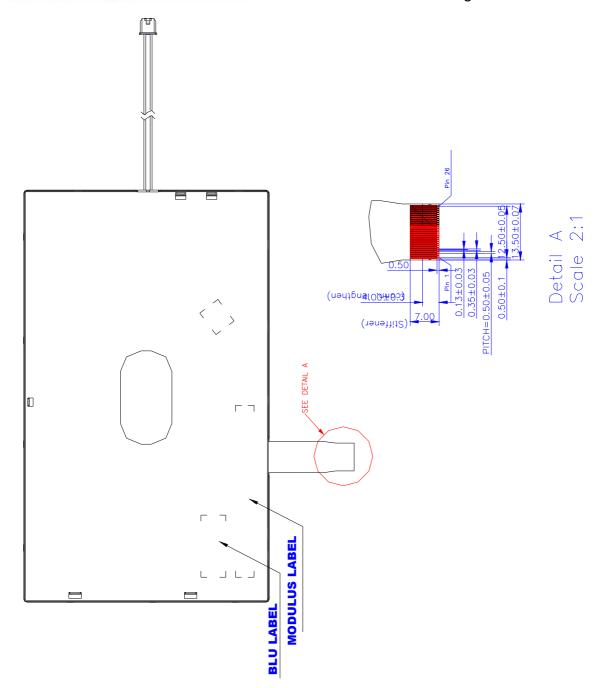
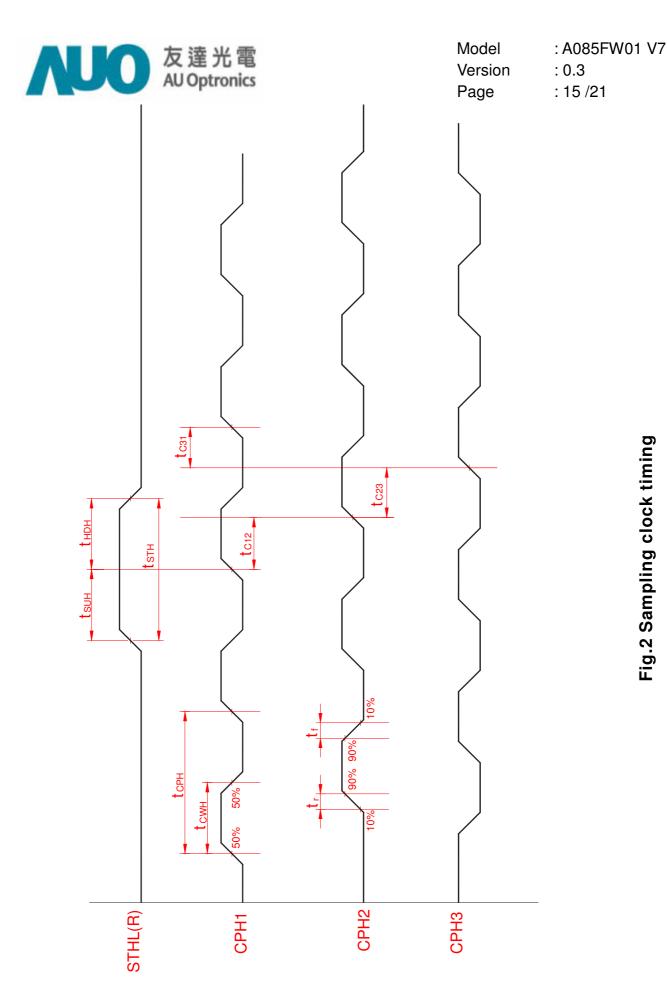


Fig.1-(b) Outline dimension of TFT-LCD module (Back side)





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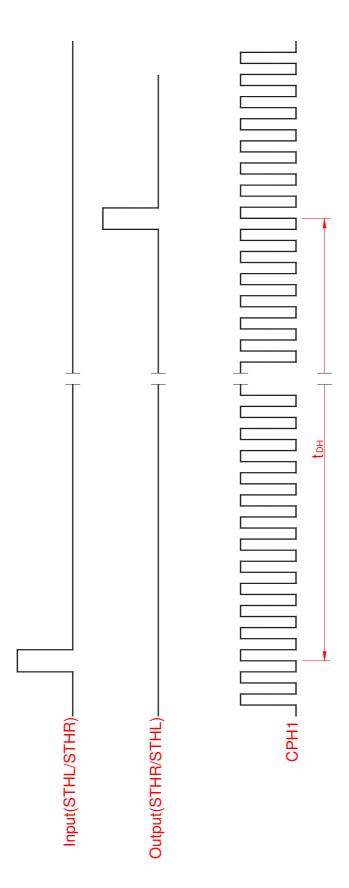
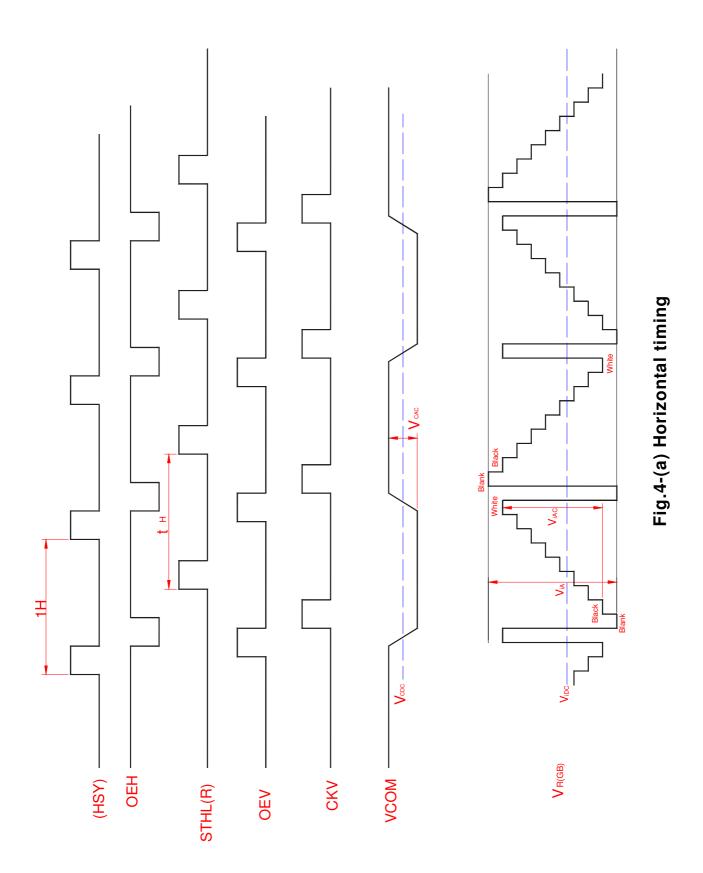


Fig.3 Horizontal display timing range



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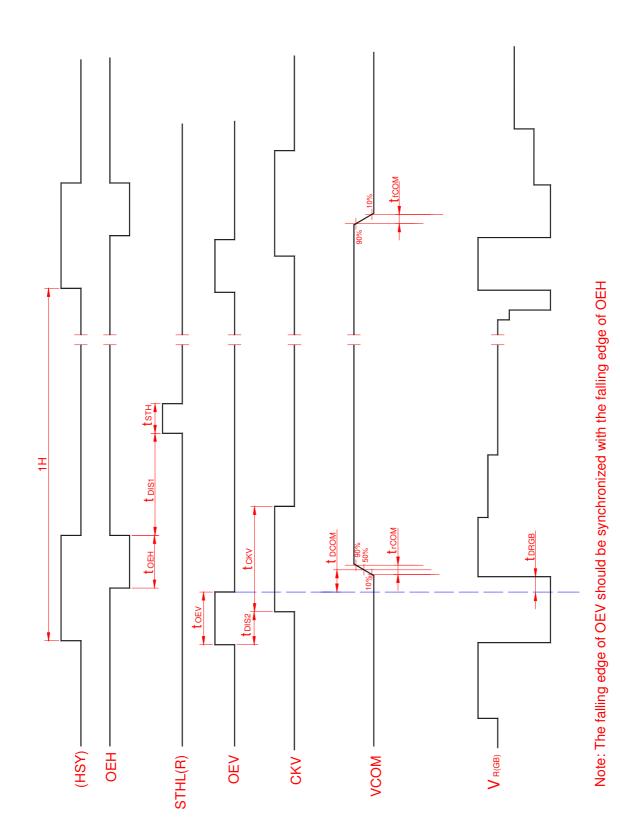


Fig.4-(b) Detail horizontal timing



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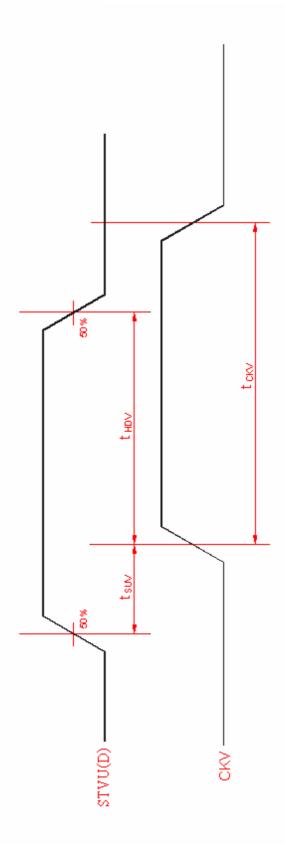


Fig.5 Vertical shift clock timing



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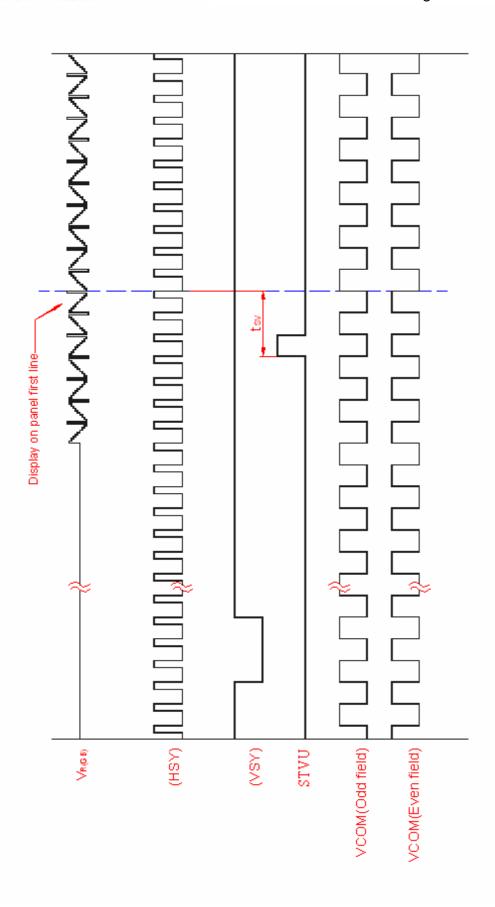


Fig.6-(a) Vertical timing (From up to down)



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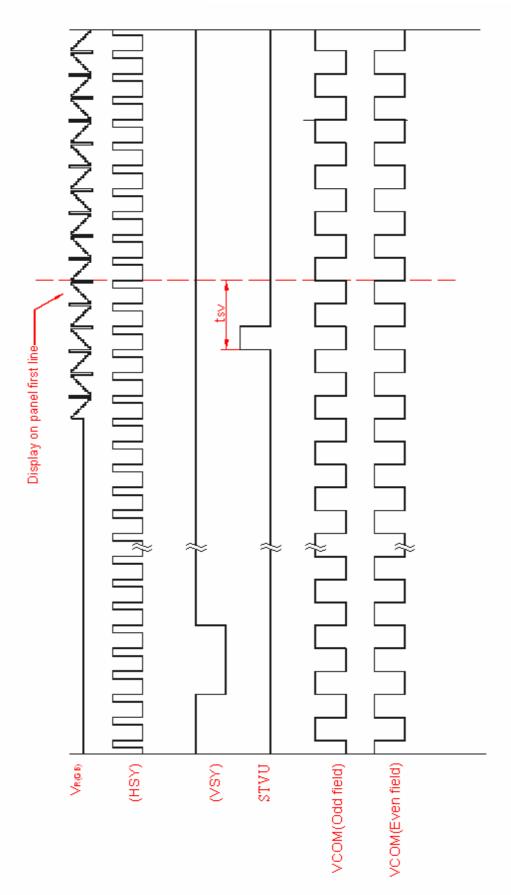


Fig.6-(b) Horizontal timing (From down to up)