上海冠显光电科技有限公司
Shanghai Top Display Optoelectronics Co., LTD

PRODUCTION SPECIFICATION OF AMOLED MODULE

MODULE NO.：TA027SVH01

Customer Name:			
Customer Part Number:			
Approved By:		**Date:**	

Prepared By	Checked By	Approved By

Version History			
Version. No	Date	Contents	Remark
01	2019-05-28	Preliminary Specification	

Contents

1 Scope

This Specification defines AMOLED manufactured by Shanghai Top Display Optoelectronics Limited, from here on refer as TDO. In the case of any unspecified item, it may require both TDO and the party designs this module into its product to work out a solution.

2 Features

2.1 Product Applications

Smart Mobile Phone

2.2 Product Features

1) Display color：16.7M (RGB x8bits)
2) Displayformat：2.69”(800RGBx600)
3) Pixel arrangement：Real RGBarrangement
4) Interface：DSI 2-Lane
5) Driver IC: RM69700

3 Maximum Rating

Parameter	Symbol	Spec			Unit	Note
		Min.	Typ.	Max.		
Analog/boost power voltage	VCI	-	-	6.6	V	-
I/O voltage	VDDIO	-	-	6.6	V	-
Operating temperature	Top	-40	-	85	℃	-
Storage temperature	Tstg	-55	-	125	℃	-

4 Mechanical Specifications

Item	Specification	unit
Dimension outline	56.6(V) x 47.25(W) x 0.505(T)	mm
Number of dots	800RGB*600	dots
Active area	54.6(W) ×40.95(H)	mm
Diagonal size	2.69	inch
Pixel pitch	68.25(W) ×68.25(H)	μm
Glass thickness （LTPS/encapsulation glass）	0.3 / 0.2	mm
Weight	TBD	g

5 Electrical Specifications

5.1 Electrical Characteristics

Test Condition: Temp=25±2℃

Item	Min.	Typ.	Max.	Unit	Remark
Logic Power		TBD		W	
ELVDD	4.6	4.6	4.6	V	
ELVSS	-3	-2.0	-1.4	V	100mV Step
AVDD	6.8	6.8	7.8	V	
VCI	2.7	3.0	3.6	V	
VDDIO	1.62	1.8	1.98	V	
Logic Current		TBD		mA	
Freq	58	60	62	Hz	
VGH	5.7	6	7	V	
VGL	-7	-6	-5.4	V	

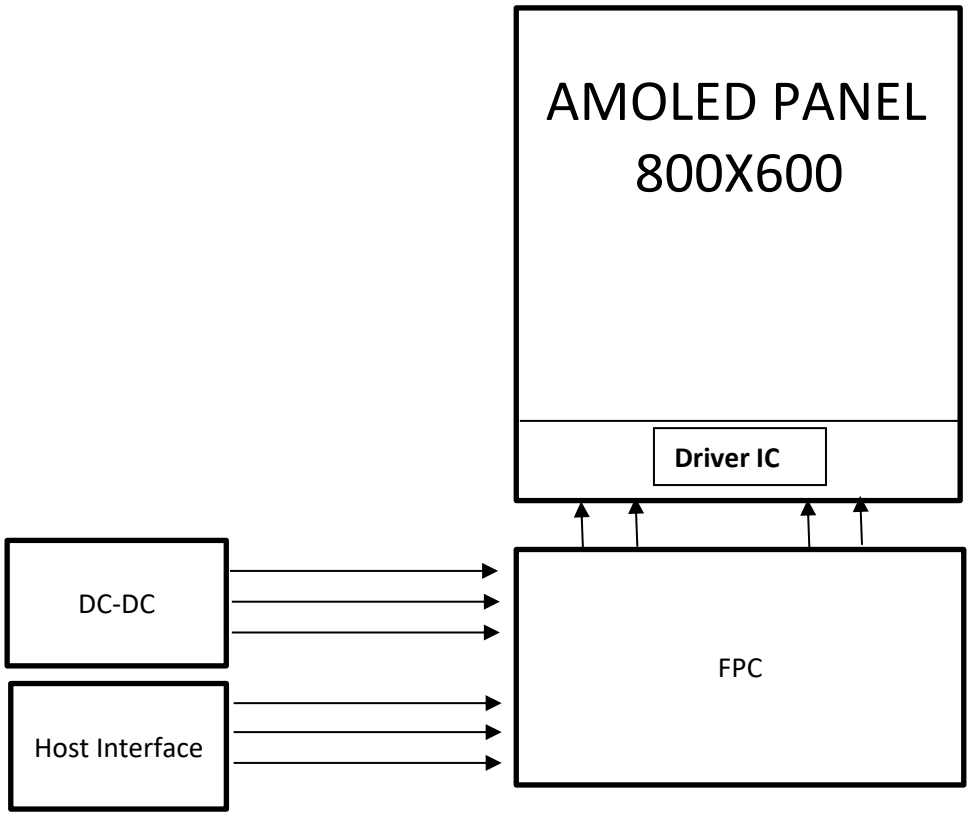
5.2 I/O Connection and Block Diagrams

5.2.1 FPC Pin Assignment

No.	Name	No.	Name
1	NC	2	GND
3	NC	4	ELVDD
5	NC	6	ELVDD
7	NC	8	ELVSS
9	GND	10	ELVSS
11	D1N	12	AVDD
13	D1P	14	GND
15	GND	16	VDDIO
17	CLKN	18	VCI
19	CLKP	20	GND
21	GND	22	SWIRE
23	D0N	24	OLED_EN
25	D0P	26	ERR_FG
27	GND	28	TE
29	MTP_PWR	30	RESX

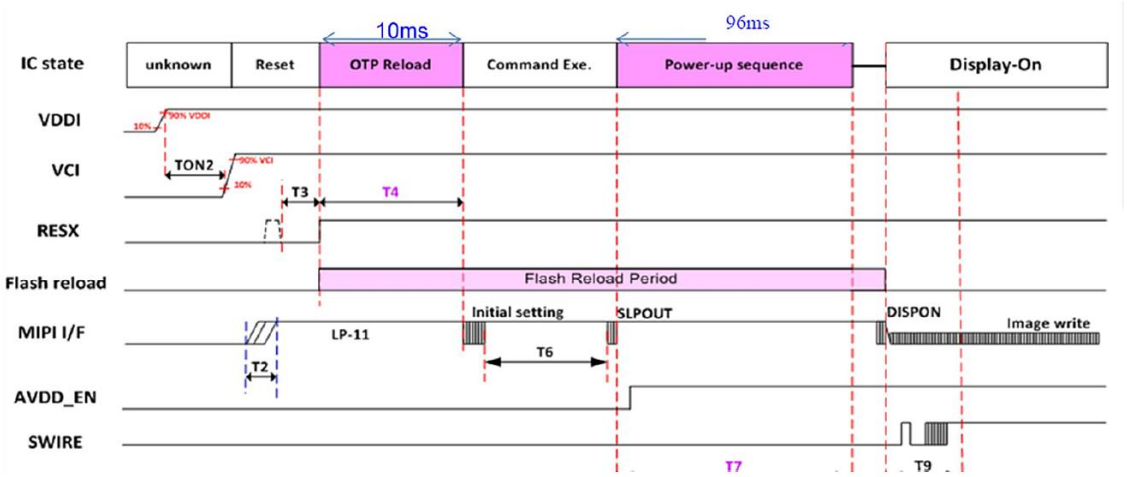
5.3 Block Diagrams

TBD

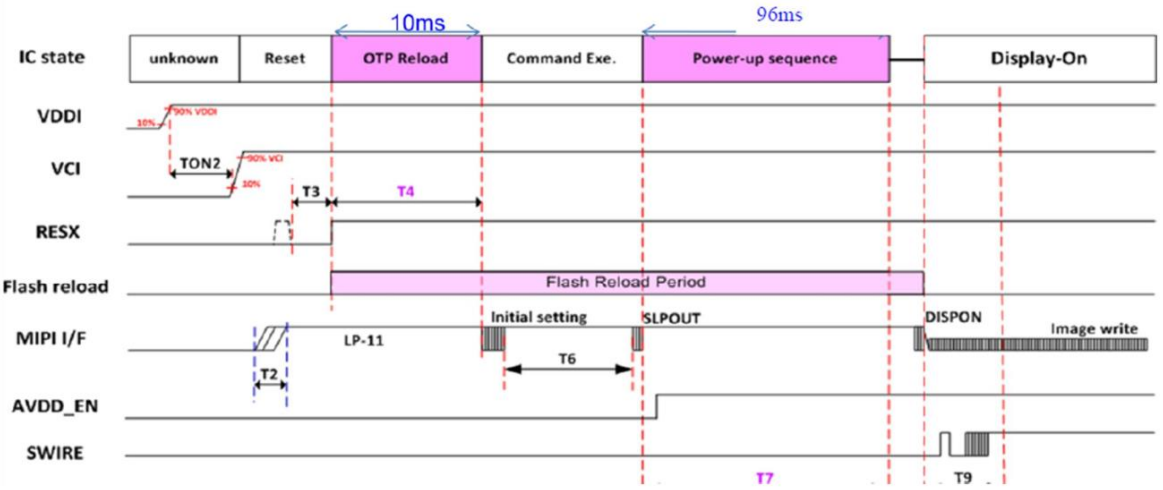


5.4 Recommended Operating Sequence

5.4.1 Power on sequence

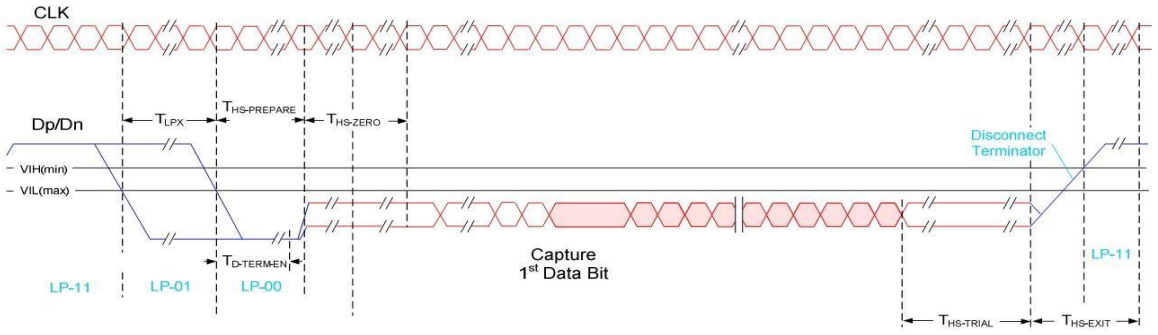


5.4.2 Power off sequence

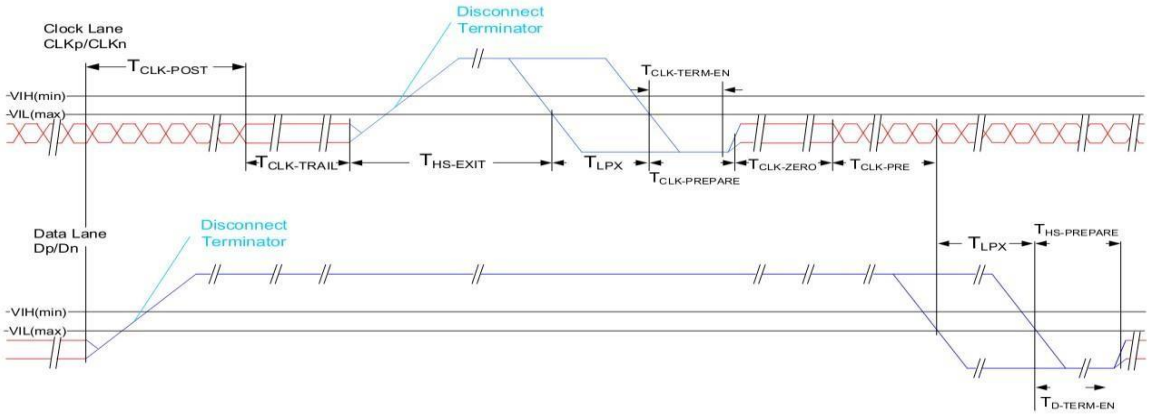


5.5 DSI Timing Characteristics

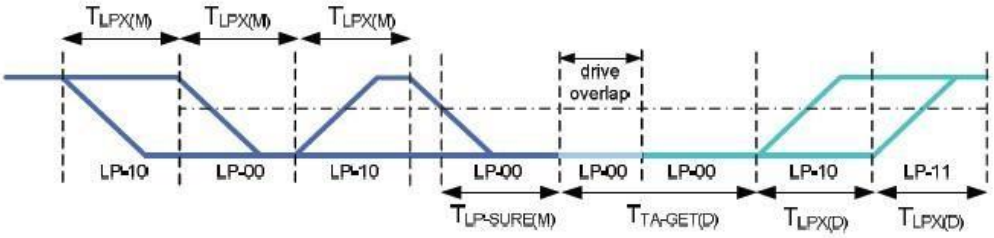
5.5.1 HS Data TransmissionBurst



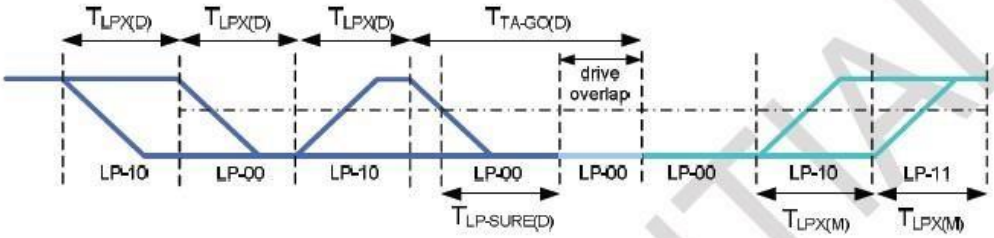
5.5.2 HS Clock Transmission



5.5.3 Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

5.5.4 Timing Parameters

Parameter	Description	MIN	MAX	Unit
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRIAL to the beginning of TCLK-TRAIL.	60ns+52×UI		ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60		ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	300		ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, Starting from the time point when Dn crosses VIL, MAX.	Time for Dn to reach VTERM-EN	38	ns
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	95	ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8		UI
TCLK-PREPARE +TCLK-ZERO	TCLK-PREPARE+ time that the transmitter drives the HS-0 state prior to starting the Clock.	300		ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL, MAX.	Time for Dn to reach VTERM-EN	35ns+4×UI	ns
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	40ns+4×UI	85ns+6×UI	ns
THS-PREPARE +THS-ZERO	THS-PREPARE+ time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns+10×UI		ns
THS-TRIAL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	60ns+4×UI		ns

5.5.5 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(Test condition: VDDIO=1.65V~1.98V,VSSA=DVSS= VSSI=0V,T_A=-40℃~+85℃)

Parameter	Symbol	Conditions	Spec			Unit
			Min.	Typ.	Max.	
Reset low pulse width	Trst	-	15	-	-	μs

Table: Reset timing

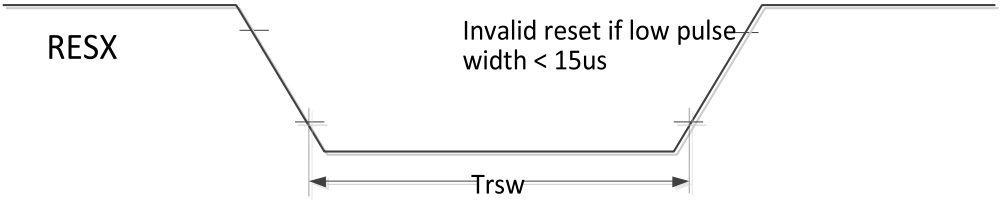


Figure: Reset timing

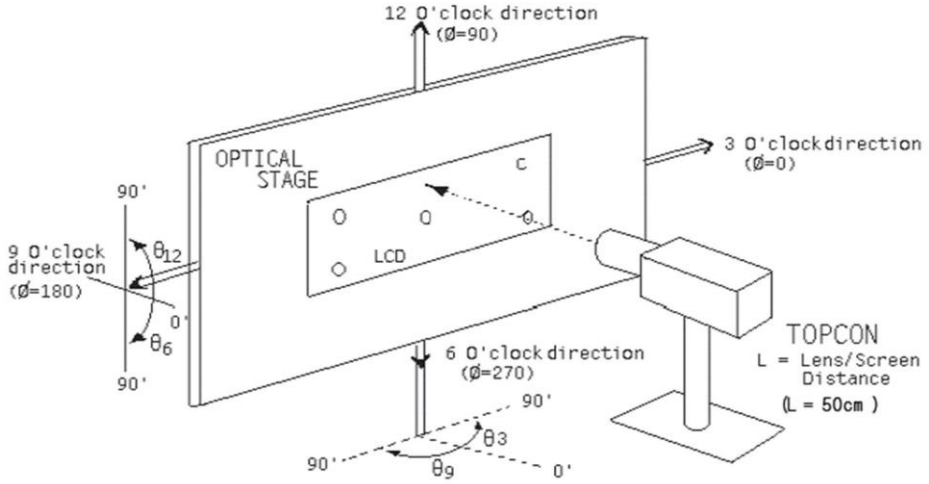
6 Electro-Optical Specification

The test of optical specifications shall be measured in a dark room (ambient luminance ≤1lux and temperature= 25±2℃) with the equipment of Luminance meter. We refer to θ, Ø=0º (=θ_3) as the 3 o'clock direction (the"right"), θ, Ø=90º (= θ_{12}) as the 12 o'clock direction ("upward"), θ, Ø=180º (= θ_9) as the 9 o'clock direction ("left") and θ, Ø=270º (= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle	Horizontal	θ_3	CR ratio≥1600	80	-	-	°	Note1
		θ_9						
	Vertical	θ_6						
		θ_{12}						
Brightness			θ=0° At Center	380	420	460	nit	
Contrast ratio		CR	θ=0°	100,000:1	-	-	-	Note2
Brightness Uniformity		LRU	W255	75	80	-	%	Note3
Color of CIE coordinate	White	x_W	θ=0°	0.2790	0.2990	0.3190	CIE 1931	Note4
		y_W		0.2949	0.3149	0.3349		
	Red	x_R		0.638	0.668	0.698		
		y_R		0.302	0.332	0.362		
	Green	x_G		0.191	0.226	0.261		
		y_G		0.684	0.719	0.754		
	Blue	x_B		0.108	0.138	0.168		
		y_B		0.025	0.055	0.085		
Color Gamut			θ=0° vs. NTSC	-	100	-	%	
Response Time			G To G			1	ms	
Cross Talk(5nit)			Window: black Background: gray127	-	3.5	5	%	Note5
Cross Talk(100nit&420nit)					-	3		
Colorshift			W255	3(30°)	4(45°)	5(60°)	JNCD	
Gamma			Subsection Control	1.9	2.2	2.5	-	-
Life time	LT93 B10		Room temperature	-	240	-	hrs	
	LT93 B10		50℃		72		hrs	

Notes :

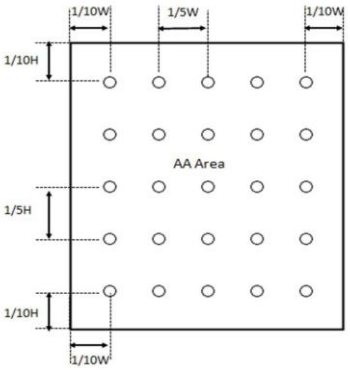
1. Viewing angle is the angle at which the contrast ratio is greater than 1600:1. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the panel surface.



2. Contrast measurements shall be made at viewing angle of θ= 0º and at the center of the panel surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (see Figure 3) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Uniformity. LRU Refer to figure as below：



Uniformity measurements shall be made atθ=0° and at the different points of the panel surface. Luminance shall be measured with all pixels in the view field set to W/R/G/B at 255 Gary level, respectively.
Luminance uniformity=Lmin/Lmax ×100%

4. The color chromaticity coordinates specified in Table 4 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

5. Crosstalk measurement shall be done at the center of the different pattern and the result shall be calculated as follow formula.
   a. measure luminance at the center.
   b. calculate cross talk as below equation:

$$\text{Crosstalk(V)} = \left| \frac{L_{Vinf} - L_{ref}}{L_{ref}} \right| \times 100\%$$

$$\text{Crosstalk(H)} = \left| \frac{L_{hinf} - L_{ref}}{L_{ref}} \right| \times 100\%$$

7 Reliability

7.1 Environmental Test

No.	Item	Condition	Qnty	Result	Judgment Criterion
1	HTS	80℃, 240hr	5 ea	OK	1. In the process of the test sample to work properly, no dysfunction。 2. The test is finished, return to room temperature, the sample appearance, display function is normal, no new display abnormal。
2	LTS	-40℃, 240hr	5 ea	OK	
3	THS	60℃/90%RH,240hr	5 ea	OK	
4	HTO	70℃, 240hr	5 ea	OK	
5	LTO	-20℃, 240hr	5 ea	OK	
6	TST	-40℃~80℃, 60 Cycles	5 ea	OK	

7.2 Electrical Test

No.	Item		Condition	Qnty	Result	Judgment Criterion
1	ESD	Front on display	±4KV(Contact)/ ±8kV(Air), 150pF/330Ω	5 ea	OK	In the process of the test sample to work properly, no dysfunction。
		Ground on metal plane	±4KV(Contact)/ ±8kV(Air), 150pF/330Ω	5 ea	OK	
		HBM	±2.5KV 1.5KΩ/100pF	5 ea	OK	
		Front on touch	±8KV(Contact)/ ±15kV(Air), 150pF/330Ω	5 ea	OK	

8 Handling Precautions

8.1 Mounting Method

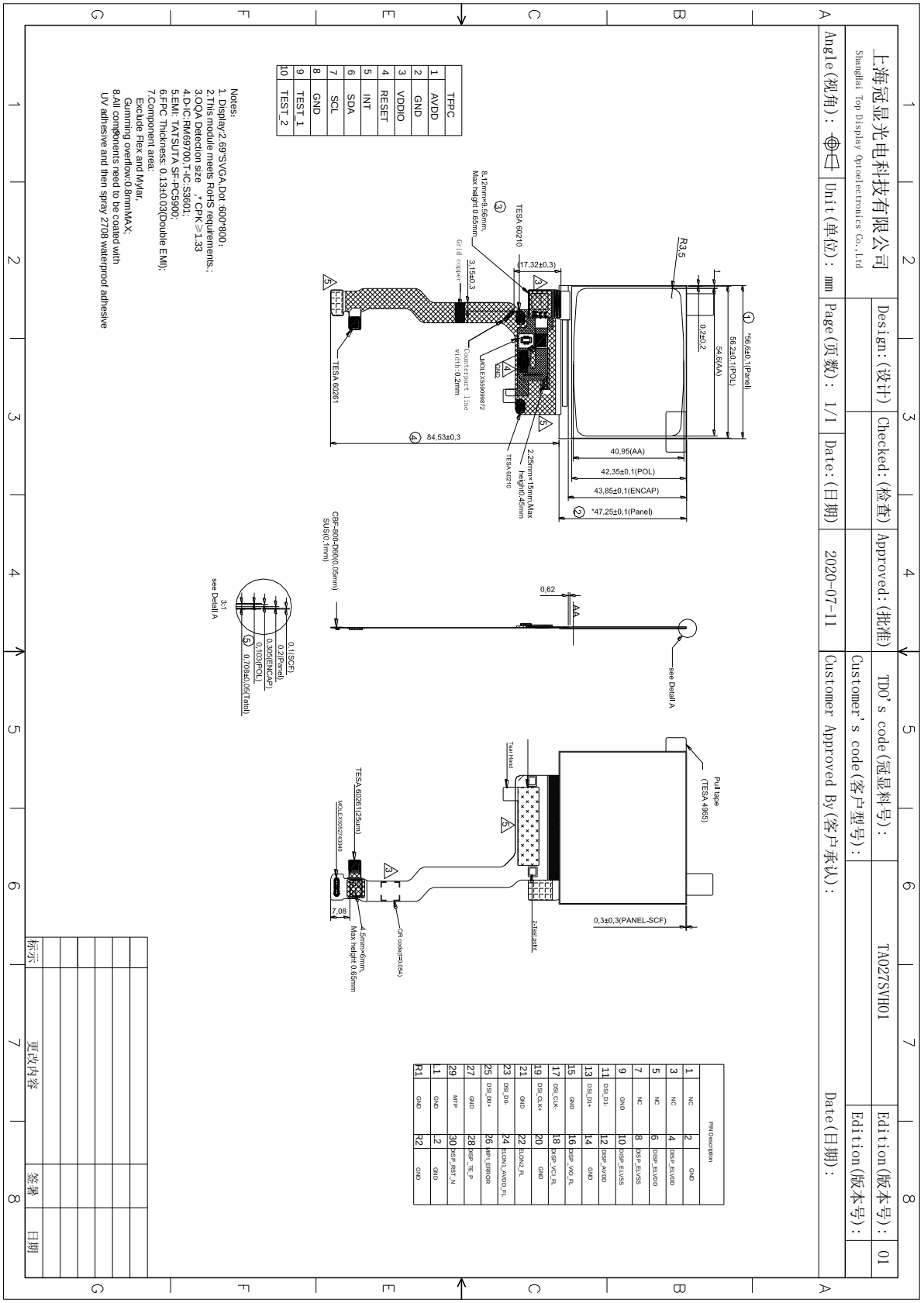
The AMOLED panel module consists of two slim glasses with polarizer which can easily get damaged. Since the module is constructed as to be fixed by utilizing fitting holes in the printed circuit board. Extreme care should be used when handling the AMOLED modules.

8.2 Caution of AMOLED Handling and Cleaning

When cleaning the display surface, use soft cloth solvent as recommended below and wipe gently.

1. Keep module away from direct sunlight or fluorescent light, and keep it at room temperature and humidity
2. Do not wipe the display surface with dry or hard materials that will damage the polarizer surface. Do not use the following solvent.
   - Water
   - Ketone
   - Aromatics
3. Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns. Do not use the following solvent on the pad and prevent it from being contaminated.
   - HCFC (Other area except ITO pad can use the HCFC for cleaning process)
   - Soldering flux
   - Chlorine(Cl), Sulfur(S)
   - Spittle, Fingerprint
4. Strong impact & pressure on module and packing is prohibited
5. Following normal power on/off sequence is necessary for preventing abnormal display or permanent damage to display
6. Optimal contrast ratio under ideal voltage is AMOLED module's characteristic, hence it is recommended a voltage control function available
7. Image sticking may occur if an image displays for an extended period of time
8. When interfered by system's overall mechanical design, an abnormal display may occur
9. Host side should place a surge-prevent circuit at power trace (ie: VCI, Vddi) to protect AMOLED module.

9 Outline Dimension Drawing



10 The Control of Hazardous substances

The Control of Hazardous substances refer toTDO document《有害物质管控标准书》(Standard document for the Control of Hazardous substances) TDO-IS-110, the latest version.