AUO

CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A116XTN02.0**
CUSTOMER APPROVED	Title : Name :

☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver._0.1)**

☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver._0.1)**

☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver._0.1)**

☐ **CUSTOMER REMARK :**

AUO

Doc. version :	0.0
Total pages :	28
Date :	2012/05/25

Product Specification

11.6" COLOR TFT-LCD PANEL

Model Name：	**A116XTN02.0**

Planned Lifetime:	From 2012/Mar To 2013/Dec
Phase-out Control:	From 2012/July To 2013/Dec
EOL Schedule:	2013/July

< □ >Preliminary Specification

<　　>Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2012/03/19		First Draft
0.1	2012/05/25	P.5	General Information

Contents

A. General Information

This product is for Netbook application. This product is include cell, POL, driver IC, and FPC.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	11.6 (Diagonal)	
2	Display Resolution	dot	1366x3(RGB) x 768	
3	Overall Dimension	mm	264.775 X154.705 X1.26	Note 1
4	Active Area	mm	256.125 X 144.0	
5	Pixel Pitch	mm	0.1875 x 0.1875	
6	Color Configuration	--	R.G.B. Vertical Stripe	Note 2
7	Color Depth	--	262K colors (RGB 6-bit)	Note 3
8	NTSC Ratio	%	45	
9	Display Mode	--	Normally White	
10	Panel surface Treatment	--	Hardness 3H, Reflection 4.3%	
11	Weight	g	115	
12	Panel Power Consumption	W	0.2	Note 4
13	Panel Transmittance	%	6.0	

Note 1: Not include blacklight cable and FPC. Refer next page to get further information.
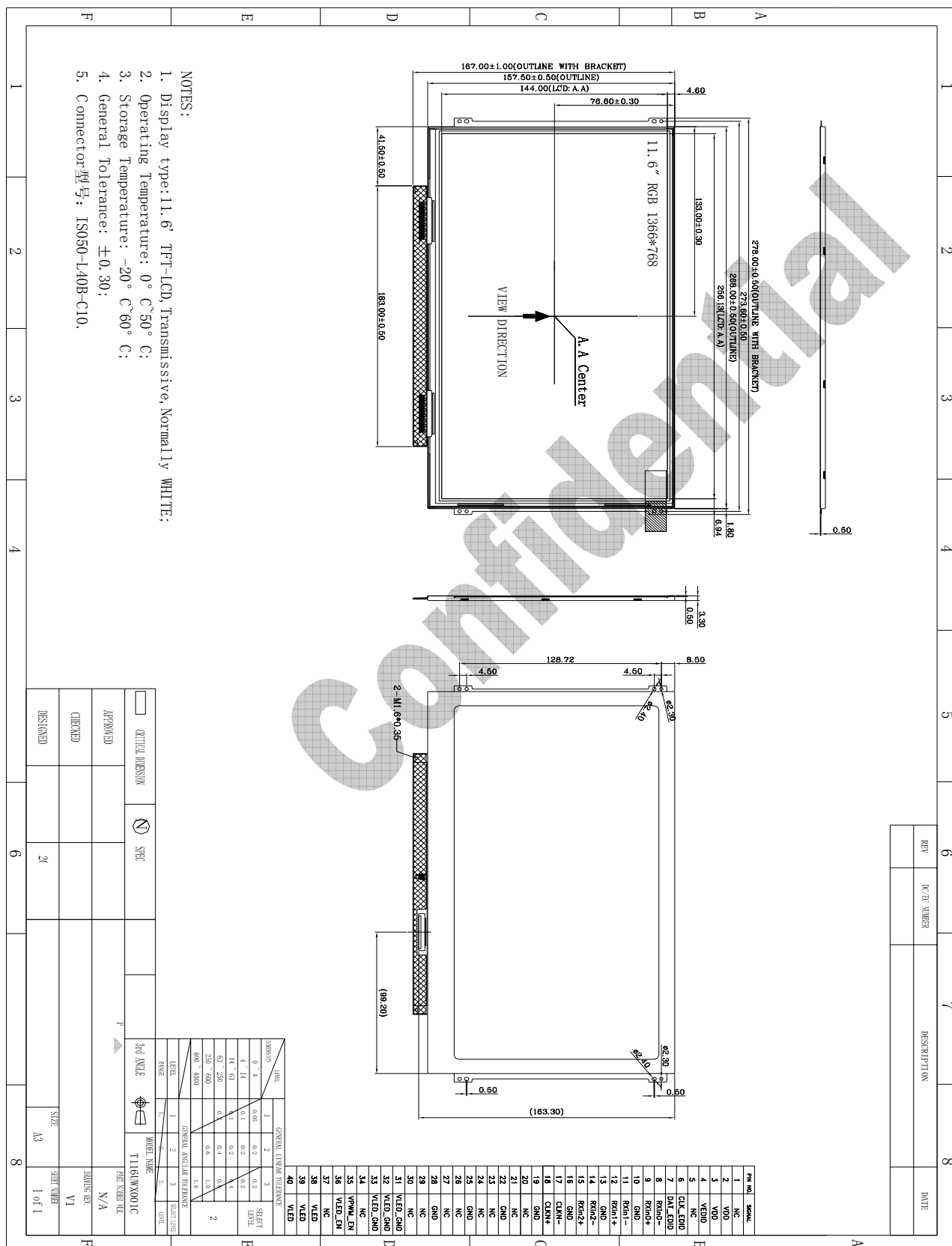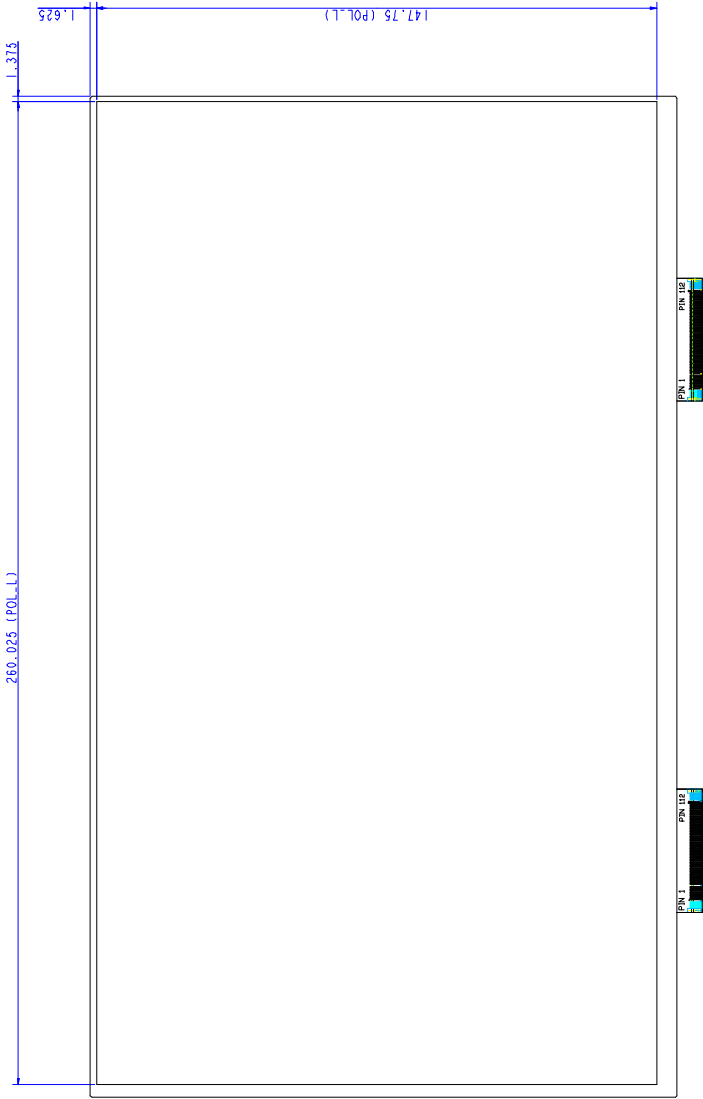
Note 2: Below figure shows dot stripe arrangement.

Note 3: The full color display depends on 18-bit data signal (pin 4~27).

Note 4: Please refer to Electrical Characteristics chapter.
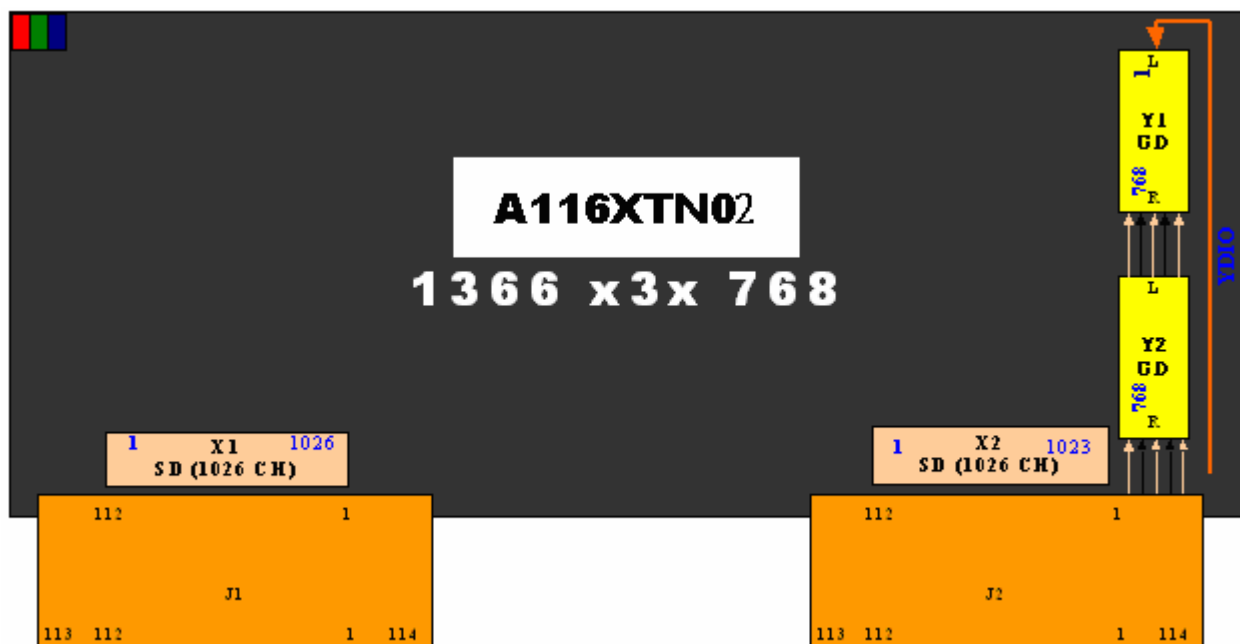
B. Outline Dimension
TFT-LCD Module

NOTES:
1. Display type:11.6" TFT-LCD, Transmissive, Normally WHITE;
2. Operating Temperature: 0°C~50°C;
3. Storage Temperature: -20°C~60°C;
4. General Tolerance: ±0.30;
5. Connector型号: IS050-L40B-C10.

11.6" RGB 1366*768

167.00±1.00(OUTLINE WITH BRACKET)
157.50±0.50(OUTLINE)
144.00(LCD: A.A)
76.60±0.30
4.60

278.00±0.50(OUTLINE WITH BRACKET)
268.00±0.50(OUTLINE)
273.60±0.50
256.19(LCD: A.A)
183.00±0.30

VIEW DIRECTION
A.A Center

41.50±0.50
183.00±0.50

0.50
6.94
1.80

3.30
0.60

128.72
4.50
4.50
8.50

(89.20)

(163.30)
0.50
0.50

ø2.30
ø2.30

2-M1.6*0.35

PIN NO.	SIGNAL
1	NC
2	NC
3	VDD
4	VDD
5	VEDID
6	CLK_EDID
7	DAT_EDID
8	GND
9	RXin0-
10	RXin0+
11	GND
12	RXin1-
13	RXin1+
14	GND
15	RXin2-
16	RXin2+
17	GND
18	CLKN-
19	CLKN+
20	GND
21	NC
22	NC
23	GND
24	NC
25	NC
26	NC
27	GND
28	GND
29	NC
30	NC
31	VLED_GND
32	VLED_GND
33	VLED_GND
34	NC
35	VPWM_EN
36	VLED_EN
37	NC
38	VLED
39	VLED
40	VLED

CRITICAL DIMENSION
SPEC
DESIGNED
CHECKED
APPROVED

MODEL NAME: T116WX01C
PART NUMBER: N/A
DRAWING REV: V1
SHEET NUMBER: 1 of 1
SIZE: A3
3rd ANGLE

REAR SIDE

147.75 (POL.L)

1.625

1.375

260.025 (POL.L)

PIN 212

PIN 1

PIN 112

PIN 1

FRONT SIDE

REAR SIDE

DETAIL B
SCALE 2/1

C. Electrical Specifications

FPC Pin Assignment

Front Side

FPC (J1 & J2) are differential signal definition for LCD interface and high speed data transfer device.

FPC J1 pin assignment:

PIN#	Signal Name	Description
114	DUMMY	No connection
1	GND	Ground
2	DUMMY	No connection
3	GND	Ground
4	DUMMY	No connection
5	GND	Ground
6	DUMMY	No connection
7	GND	Ground
8	DUMMY	No connection
9	GND	Ground
10	DUMMY	No connection
11	GND	Ground
12	DUMMY	No connection
13	GND	Ground
14	DUMMY	No connection
15	GND	Ground
16	DUMMY	No connection
17	DIO2	Start pulse signal output

18	STB	Latches the polarity of outputs and switches the new data to output
19	XPOL	Input the terminal of polarity signal
20	YDIO	Gate start pulse input
21	CS0	Charge sharing selection pin
22	CS1	Charge sharing selection pin
23	ODLY0	Output delay setting
24	ODLY1	Output delay setting
25	ODLY2	Output delay setting
26	SRC0	Slew Rate Control selection pin
27	SRC1	Slew Rate Control selection pin
28	PATH4	The internal connected bypass paths
29	PATH3	The internal connected bypass paths
30	DPSEL1	Selects mini-LVDS input mode
31	DPSEL0	Selects mini-LVDS input mode
32	DGND	Ground pin for digital circuit
33	DGND	Ground pin for digital circuit
34	DVDD	Power supply for digital circuit
35	DVDD	Power supply for digital circuit
36	AVDD	Power supply for analog circuit
37	AVDD	Power supply for analog circuit
38	VTOP	Power supply for analog circuit
39	VTOP	Power supply for analog circuit
40	VBOT	Power supply for analog circuit
41	VBOT	Power supply for analog circuit
42	AGND	Ground pin for analog circuit
43	AGND	Ground pin for analog circuit
44	DGND	Ground pin for digital circuit
45	DGND	Ground pin for digital circuit
46	DVDD	Power supply for digital circuit
47	DVDD	Power supply for digital circuit
48	MLV0P	LVDS input RGB data
49	MLV0N	LVDS input RGB data
50	SGND	Signal Ground
51	MLV1P	LVDS input RGB data
52	MLV1N	LVDS input RGB data
53	SGND	Signal Ground
54	MLV2P	LVDS input RGB data
55	MLV2N	LVDS input RGB data
56	SGND	Signal Ground

57	MLVCLKP	LVDS input CLK
58	MLVCLKN	LVDS input CLK
59	SGND	Signal Ground
60	MLV3P	LVDS input RGB data
61	MLV3N	LVDS input RGB data
62	SGND	Signal Ground
63	MLV4P	LVDS input RGB data
64	MLV4N	LVDS input RGB data
65	SGND	Signal Ground
66	MLV5P	LVDS input RGB data
67	MLV5N	LVDS input RGB data
68	DVDD	Power supply for digital circuit
69	DVDD	Power supply for digital circuit
70	DGND	Ground pin for digital circuit
71	DGND	Ground pin for digital circuit
72	AGND	Ground pin for analog circuit
73	AGND	Ground pin for analog circuit
74	VBOT	Power supply for analog circuit
75	VBOT	Power supply for analog circuit
76	VTOP	Power supply for analog circuit
77	VTOP	Power supply for analog circuit
78	AVDD	Power supply for analog circuit
79	AVDD	Power supply for analog circuit
80	DVDD	Power supply for digital circuit
81	DVDD	Power supply for digital circuit
82	DGND	Ground pin for digital circuit
83	DGND	Ground pin for digital circuit
84	D_CON	Selects control pin left or right shift
85	GMAEN	Gamma amplification control pin
86	PW_SEL	Static current control in half AVDD function
87	FRE_SEL	Mini-LVDS frequency range control function
88	AVSEL	Analog voltage selector
89	PRO1	The Structure of the line-repair amp is the same as that of the analog output
90	PATH2R	The internal connected bypass paths
91	PATH1R	The internal connected bypass paths
92	DIO1	Start pulse signal input
93	DUMMY	No connection
94	DUMMY	No connection

95	DUMMY	No connection
96	VGMA1	Gamma reference voltage
97	VGMA2	Gamma reference voltage
98	VGMA3	Gamma reference voltage
99	VGMA4	Gamma reference voltage
100	VGMA5	Gamma reference voltage
101	VGMA6	Gamma reference voltage
102	VGMA7	Gamma reference voltage
103	VGMA8	Gamma reference voltage
104	VGMA9	Gamma reference voltage
105	VGMA10	Gamma reference voltage
106	VGMA11	Gamma reference voltage
107	VGMA12	Gamma reference voltage
108	VGMA13	Gamma reference voltage
109	VGMA14	Gamma reference voltage
110	CST	Common voltage
111	RES1	Repair circuit
112	VCOM	VCOM signal
113	DUMMY	No connection

FPC J2 pin assignment:

PIN#	Signal Name	Description
114	DUMMY	No connection
1	VCOM	VCOM signal
2	RES2	Repair circuit
3	YDIO	Gate start pulse input
4	VGL	Gate drvier negative power supply
5	VGL	Gate drvier negative power supply
6	VGH	Gate drvier positive power supply
7	VGH	Gate drvier positive power supply
8	VBIAS	Switch driver outputs for discharge output loading
9	YVCCA	Gate driver digital power
10	GND	Ground
11	ADJ	Adjustable shading output control pin
12	YV1C_S	Power switch control pin
13	OE	Input/output pin for the output enable control
14	XON	Input/output pin for the output global on control
15	CPV	Gate clock signal for internal shift register
16	CST	Common voltage

17	DIO2	Start pulse signal output
18	STB	Latches the polarity of outputs and switches the new data to output
19	XPOL	Input the terminal of polarity signal
20	YDIO	Gate start pulse input
21	CS0	Charge sharing selection pin
22	CS1	Charge sharing selection pin
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50	SGND	Signal Ground
51	MLV1P	LVDS input RGB data
52	MLV1N	LVDS input RGB data
53	SGND	Signal Ground
54	MLV2P	LVDS input RGB data
55	MLV2N	LVDS input RGB data

56	SGND	Signal Ground
57	MLVCLKP	LVDS input CLK
58	MLVCLKN	LVDS input CLK
59	SGND	Signal Ground
60	MLV3P	LVDS input RGB data
61	MLV3N	LVDS input RGB data
62	SGND	Signal Ground
63	MLV4P	LVDS input RGB data
64	MLV4N	LVDS input RGB data
65	SGND	Signal Ground
66	MLV5P	LVDS input RGB data
67	MLV5N	LVDS input RGB data
68	DVDD	Power supply for digital circuit
69	DVDD	Power supply for digital circuit
70	DGND	Ground pin for digital circuit
71	DGND	Ground pin for digital circuit
72	AGND	Ground pin for analog circuit
73	AGND	Ground pin for analog circuit
74	VBOT	Power supply for analog circuit
75	VBOT	Power supply for analog circuit
76	VTOP	Power supply for analog circuit
77	VTOP	Power supply for analog circuit
78	AVDD	Power supply for analog circuit
79	AVDD	Power supply for analog circuit
80	DVDD	Power supply for digital circuit
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90	PATH2R	The internal connected bypass paths
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92	DIO1	Start pulse signal input
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94	DUMMY	No connection
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96	VGMA1	Gamma reference voltage
97	VGMA2	Gamma reference voltage
98	VGMA3	Gamma reference voltage
99	VGMA4	Gamma reference voltage
100	VGMA5	Gamma reference voltage
101	VGMA6	Gamma reference voltage
102	VGMA7	Gamma reference voltage
103	VGMA8	Gamma reference voltage
104	VGMA9	Gamma reference voltage
105	VGMA10	Gamma reference voltage
106	VGMA11	Gamma reference voltage
107	VGMA12	Gamma reference voltage
108	VGMA13	Gamma reference voltage
109	VGMA14	Gamma reference voltage
110	CST	Common voltage
111	RES1	Repair circuit
112	VCOM	VCOM signal
113	DUMMY	No connection

Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[^{o}C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[^{o}C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

Operating Range [graphic]   Storage Range   [graphic] + [graphic]
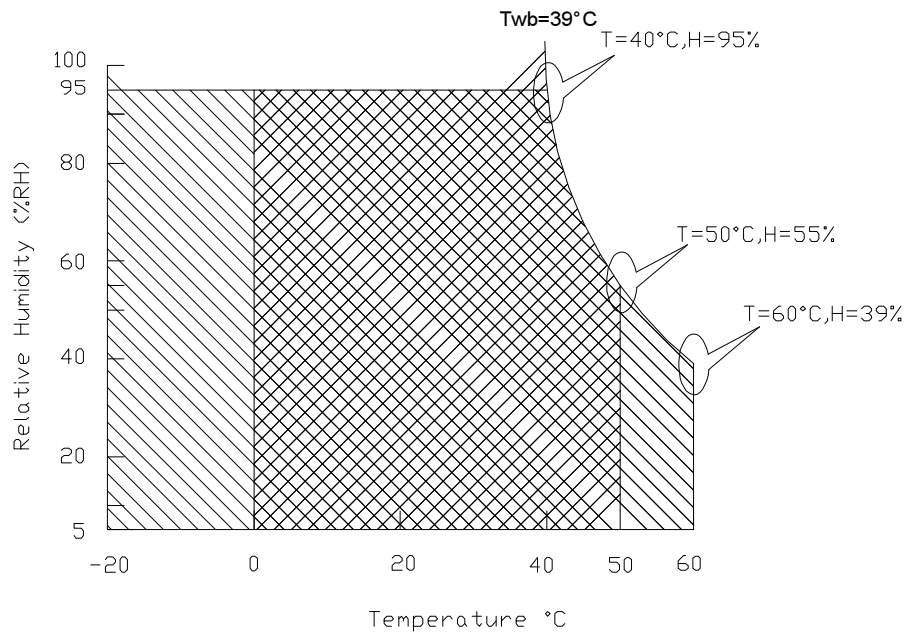
Electrical DC Characteristics
Typical Operation Condition (AGND =GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power voltage	XVCC	3.0	3.3	3.6	V	Source driver digital power supply
	YVCCA	3.0	3.3	3.6	V	Gate driver digital power supply
	AVDD, VTOP				V	Analog power supply
	VGL				V	Gate driver supply voltage
	VGH				V	
Gamma voltage	VGMA1				V	Gamma reference voltage (Preliminary only)
	VGMA2				V	
	VGMA4				V	
	VGMA6				V	
	VGMA7				V	
	VGMA8				V	
	VGMA9				V	
	VGMA11				V	
	VGMA13				V	
	VGMA14				V	
	V_{IH}	0.7*XVCC	-	XVCC	V	
	V_{IL}	0	-	0.3*XVCC	V	
	VCOM				V	
High level input voltage						Digital signals
Low level input voltage						
VCOM						

Electrical Characteristics

Please refer to Appendix A – Electrical characteristics.

Power On/Off Sequence

Please refer to Applendix A – Power on/off sequence

Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise + Fall		T_{RT}	θ=0°	--	8	16	ms	Note 2
Contrast ratio		CR	At optimized viewing angle	--	500	--		Note 3, 7
Viewing Angle	Top		CR□10	10	15	--	deg.	Note 4,5
	Bottom			30	35	--		
	Left			40	45	--		
	Right			40	45	--		
Transmittance		Y_L	θ=0°	6.0	6.1	--	%	Note 5

Note 1: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.

PHOTO DETECTOR
BM-5A
FIELD=1°
50 cm
LCD PANEL
TFT-LCD MODULE
CENTER OF THE SCREEN
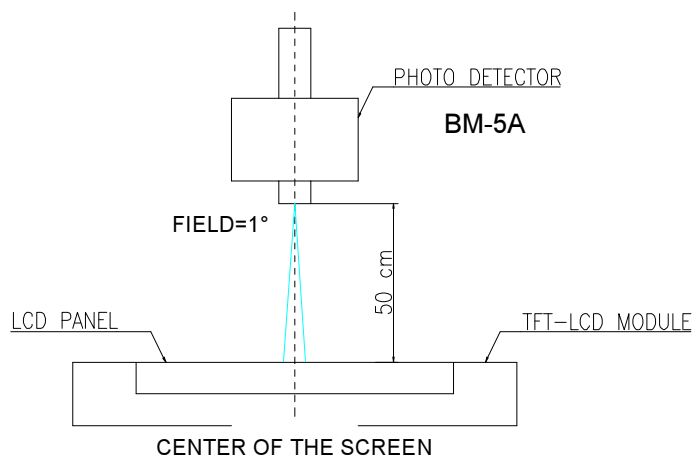
Note 2: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.
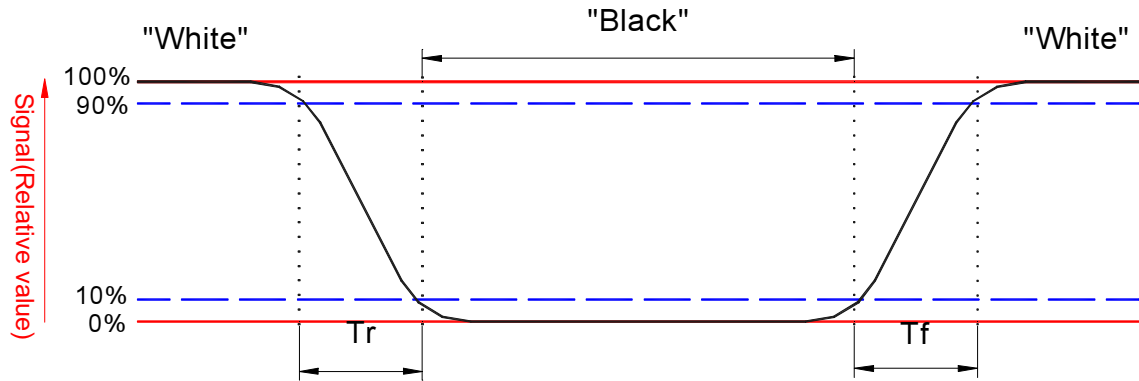
Note 3. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 4. Definition of viewing angle, θ, Refer to figure as below.
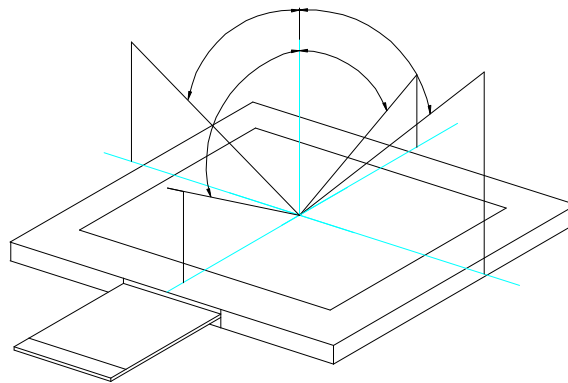
Note 5. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

D. Reliability Test Items

No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 60℃ 240Hrs	
2	Low Temperature Storage	Ta= -20℃ 240Hrs	
3	High Ttemperature Operation	Ta= 50℃ 240Hrs	
4	Low Temperature Operation	Ta= 0℃ 240Hrs	
5	High Temperature & High Humidity	Ta= 50℃. 80% RH 240Hrs	Operation
6	Heat Shock	-20℃(0.5h) ~60℃(0.5h), ,50Cycles	Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B	Note 5
8	Image Sticking	25℃, 4hrs	Note 6
9	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (With Carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

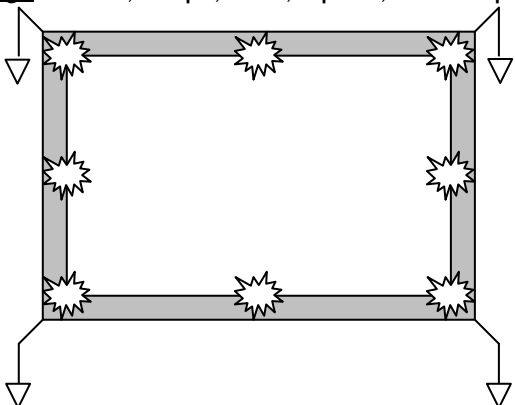Note 1: Ta: Ambient Temperature. Tp: Panel Surface Temperature

Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

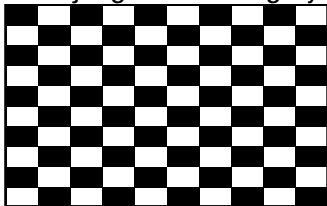Note 3: All the cosmetic specification is judged before the reliability stress.

Note 4: temperature and relative umidity range is shown in the figure below

Relative Humidity(%RH)

40℃ 95%

60℃ 90%

STORAGE RANGE

OPERATING RANGE

60℃ 15%

70℃ 10%

-30 -20   30   60   Temperature(℃)
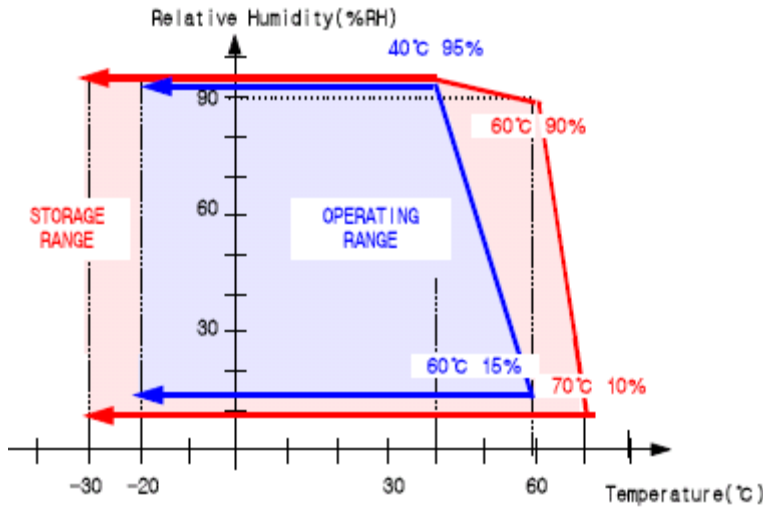
Note5 : All test techniques follow IEC6100-4-2 standard.

Test Condition		Note
Pattern		
Procedure And Set-up	Contact Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point Air Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point	
Criteria	B – Some performance degradation allowed. No data lost. Self-recoverable hardware failure.	
Others	1. Gun to Panel Distance 2. No SPI command, keep default register settings.	

Note 6: Operate with chess board pattern as figure and lasting time and temperature as the conditions. Then judge with 50% gray level, the mura is less than JND 2.5

Packing and Marking
Packing Form

PET Tray
84.11B05.001

Put 1pcs EPE Cushion FOR Left

Total Put 5 pcs SKD and 6 PCS EPE for Left

Put 5pcs SKD and 6 PCS EPE for Right

Put 6pcs Tray Stack

PP Board
84.11B07.001

Put one PP BOARD and put 6 pcs Tray Stack in the ANTI-STATIC bag

Packing ANTI-STATIC bag

84.11B07.004

Put EPE bottom Cushion into Carton

Put First Stack Package and EPE

Put Second Stack Package into Carton

84.11B07.004

Put TOP EPE Cushion into Carton

H Tape Fix

Panel Label Information

In the carton box, the panel (collectively called as the "Product") will be with a label of Shipping Number which represents the identification of the Product at a specific location.   The label is composed of a 22-digit serial number with the following definition:
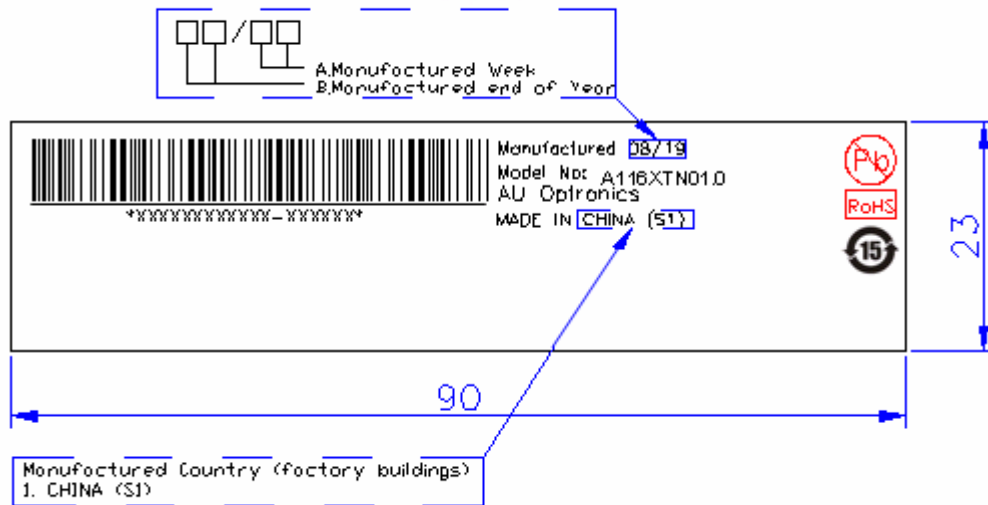
A. Manufactured end of year mark						B. Manufactured week mark			
Mark	08	09	10	11	…	Mark	01	02	…
Definition	2008	2009	2010	2011	…	Definition	1st Week	2nd Week	…

Shipping No. has 18 digits: for example: VW7400100001-PM0100

VW74001 00001-PM0100   => Lot number
VW74001 00001-PM0100   => Serial number
VW7400100001-PM0100   => Factory number

Carton Label Information

The packing carton will be attached with a carton label where packing Q'ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed.

AU Optronics

MODEL NO· A116XTN01.0
PART NO: 91.11A04.000
CUSTOMER NO:
CARTON NO:

Made in XXXXXX   *xxxxx—xxxxxxxxxx*

QTY: 100

RoHS Pb

15

40

80
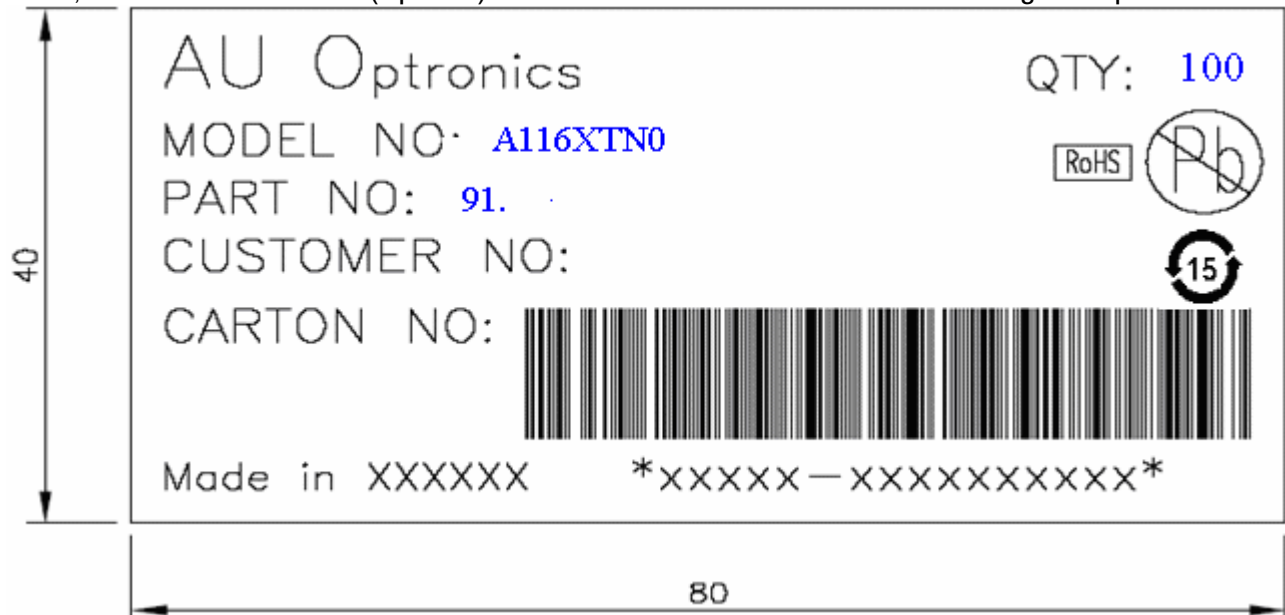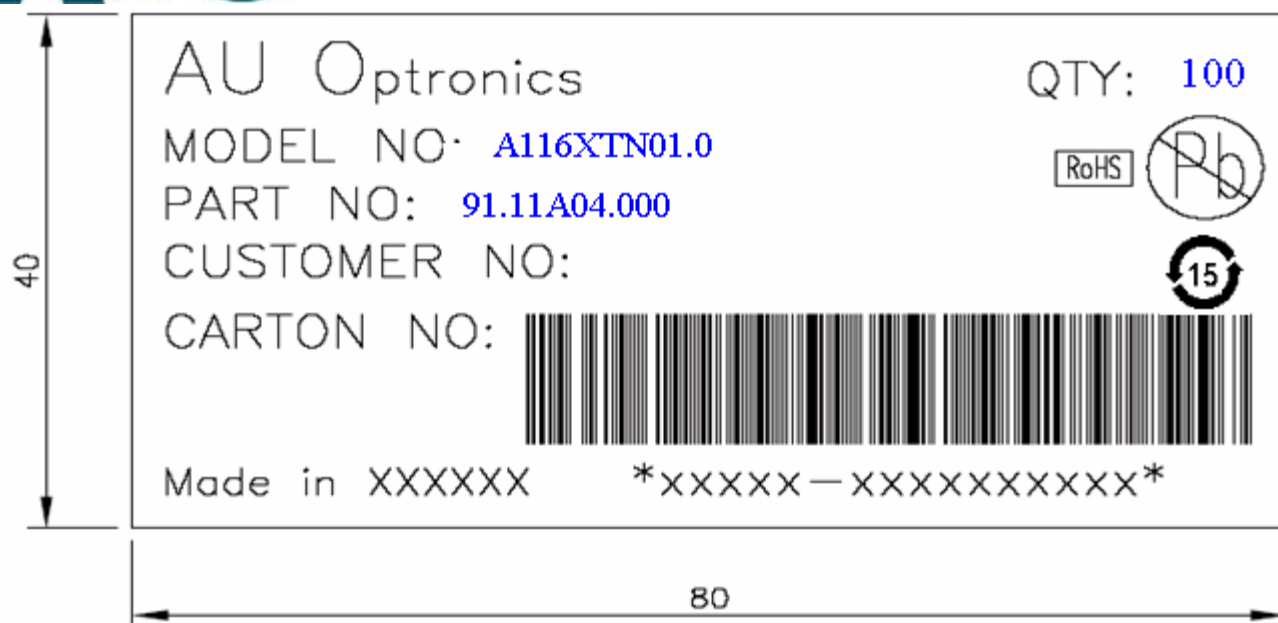
Refer to the above drawing of packing format for the location and size of the carton label.
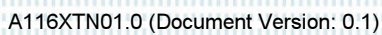
E. Application Note
Application Circuit
    Please refer to Appendix A – Electrical characteristics.
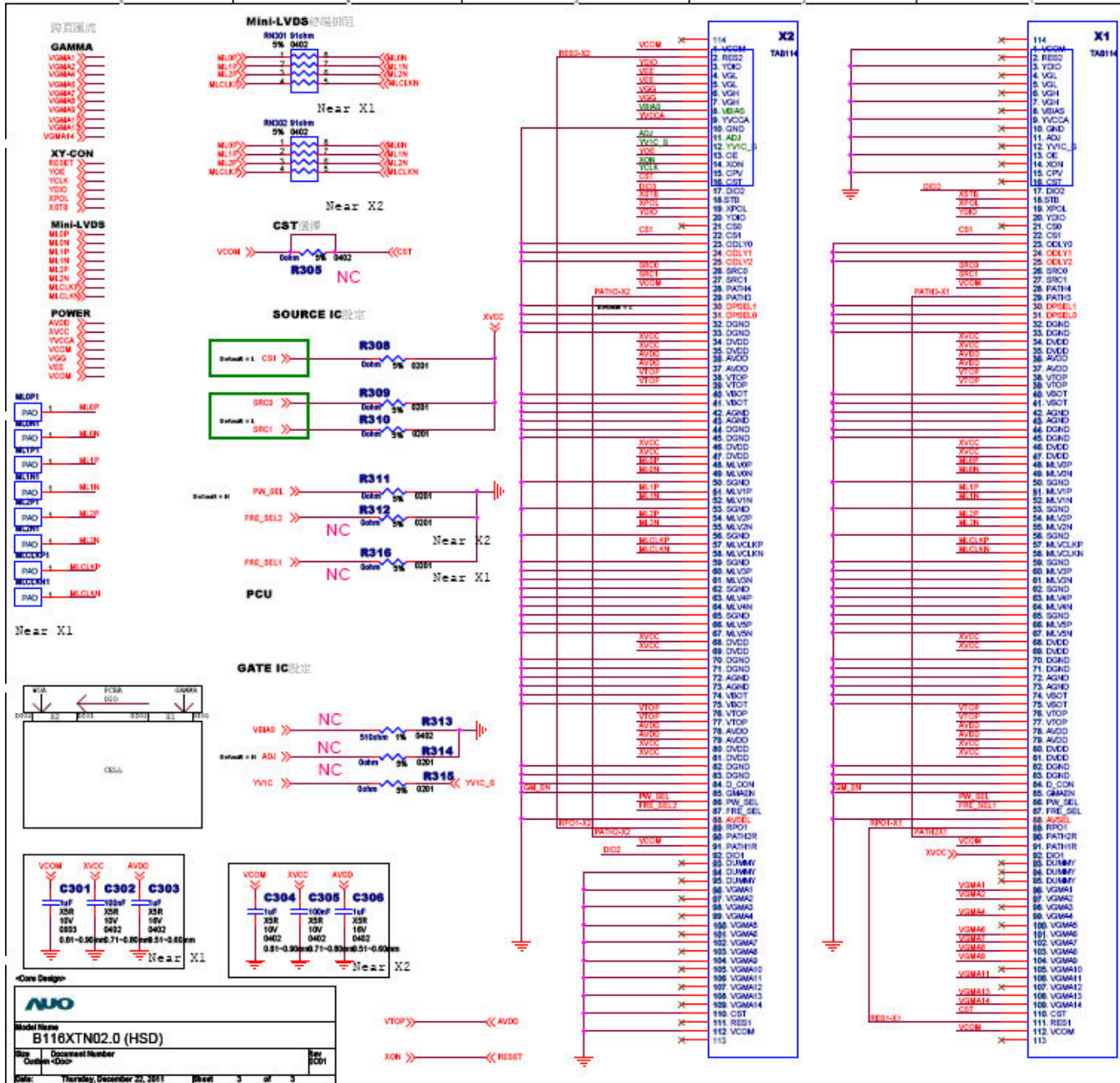
F. Precautions
1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.

Appendix A: Recommended Application Circuits with specifications

Application circuit (Bill of material is different to these schematics)

B116XTN02.0 (HSD)

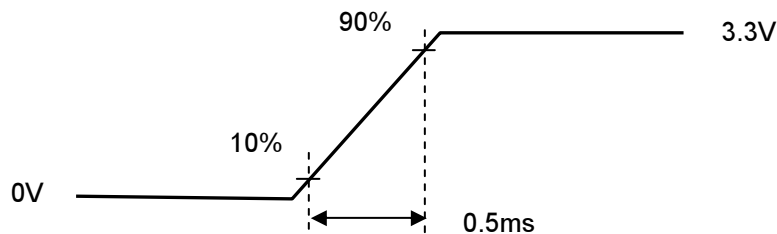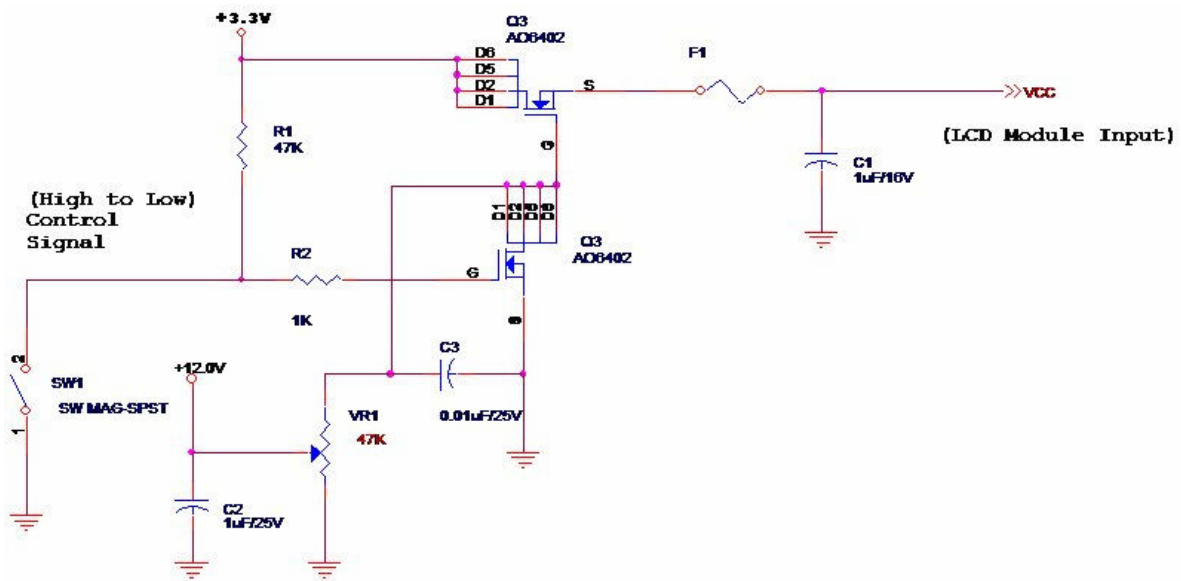## Electrical Characteristics
Power Specification

Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.8	[Watt]	Note 1
IDD	IDD Current	-	-	242	[mA]	Note 1
lRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3}$ x I_{black})

Note 2：Measure Condition

Vin rising time

Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{th}	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
V_{tl}	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
V_{ID}	Differential Input Voltage	100	600	[mV]
V_{cm}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform

Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off
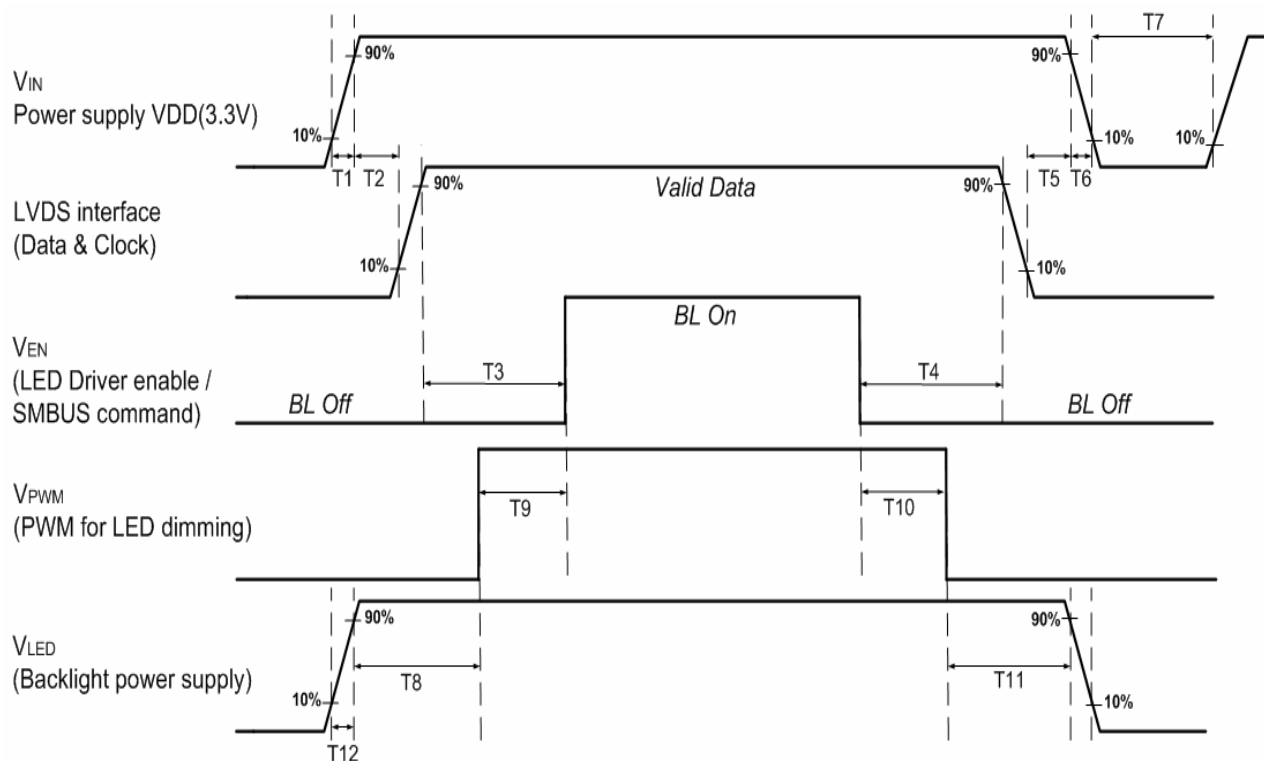
Parameter	Value	
	Min.(ms)	Max.(ms)
T1	0.5	10
T2	0	50
T3	200	-
T4	200	-
T5	0	50
T6	0	10
T7	500	-
T8	10	-
T9	10	180
T10	10	180
T11	10	-
T12	0.5	10