



## Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications

( V ) Final Specifications

Module	10.1"(10.07") WXGA 16:10 Color TFT-LCD with LED Backlight design
Model Name	B101EW05 V7 (H/W:0A )
Note	<i>LED Backlight with driving circuit design</i> ✓ <i>Dynamic Contrast Ratio (Power Saving Solution)</i>

Customer

Date

Checked &  
Approved by

Date

Note: This Specification is subject to change  
without notice.

Approved by

Date

Kevin Shen

06/23/2011

Prepared by

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06/23/2011

**NBBU Marketing Division**  
**AU Optronics corporation**



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## Record of Revision

Version and Date	Page	Old description	New Description	Remark										
0.1 2011/01/25	All	First Edition for Customer												
0.2 2011/01/26	20-21	6.3.2 LVDS PIN assignment as original B101EW05	6.3.2 LVDS PIN assignment as B101EB01											
0.3 2011/02/09	5	White Luminance	Change to 300nit,typ											
	5	Power Consumption	Change to 3.1W,max											
	6	Support Color	Change to 6bit + FRC											
	6	White Luminance	ILED = 18mA Brightness = 300nit, typ, 255nit, min											
	11	Functional Block Diagram	follow B101EB01 design w/o 3D function											
	18	The Input Data Format	Modify to 8bit NS mode											
	24-26	LCM 2D drawing	Addition											
	27	Shipping Label Format	TBD											
	29	EDID description	TBD											
0.4 2011/02/17	5	Phycisal size	Thickkness: from 5.2 to 5.3mm,max (Al foil addition @ PCBA protect film)											
	16	5.3.2 Backlight input signal characteristics	Alignment as B101EB01 spec											
	21	6.5.1 Timing Characteristics	Correction: blanking of Horizontal Section											
	24	8. Mechanical Characteristics	2D drawing update											
0.5 2011/02/17	21	6.5.1 Timing Characteristics	Clock frequency: change to 71.2MHz											
0.6 2011/02/22	21	6.5.1 Timing Characteristics	Clock frequency: change to 71.2MHz											
0.7 2011/02/22	6	Color / Chromaticity Coordinates	<table border="1"> <tr> <td>White:</td> <td>Wx:</td> <td>0.280</td> <td>0.310</td> <td>0.340</td> </tr> <tr> <td></td> <td>Wy:</td> <td>0.290</td> <td>0.320</td> <td>0.350</td> </tr> </table> White spec modification for MP stage	White:	Wx:	0.280	0.310	0.340		Wy:	0.290	0.320	0.350	
White:	Wx:	0.280	0.310	0.340										
	Wy:	0.290	0.320	0.350										
0.8 2011/02/23	30	Add "11.1 Precaution" description	Follow AUO CP model spec											
0.9 2011/03/18	22	6.4 Timing Characteristics	Modify the CLK frequency from 71.2 to 69.82 MHz											
	30	EDID description	Update all EDID											
	20	6.3.1 LVDS connector vendor	Change to I-PEX											



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	20	6.3.2 LVDS pin assignment	Update Pin 5 aging function	
	23	6.5 Power On/Off sequence	update	
	7	2.2 optical statistics	Flicker -20 dB	
1.0 2011/04/14	7	Cross talk	4% → 4% by AUO test cond. 5% by test cond.	
	17	LED characteristics	Add the description of LED & LB type	
1.1 2011/04/21	7, 11	LED color BIN definition	Add Note 10 for LED color BIN definition	
1.2 2011/06/10	7	2.2 I <sub>LED</sub> = 18 m A Luminance uniformity 5 points max 1.25	I <sub>LED</sub> = 17 m A Luminance uniformity 9 points max 1.42	
	14	5.1.1 VDD power 0.7 W IDD current 212 m A	VDD power 0.88 W current 293 m A	IDD
	16	5.1.3 DCR Mode Duty Index 70~100%	DCR Mode Duty Index 85~95%	
	17	5.2.1 Back light power 2.5 W	Back light power 2.32 W	
		I <sub>LED</sub> = 18 m A	I <sub>LED</sub> = 17 m A	
	22	6.4.1 clock frequency 68.92 MHz	clock frequency 71.1 MHz	
	32	10.1 EDID check sum AA	Check sum C2	
	6	I <sub>LED</sub> =18mA, 1.25 max. (5 points)	I <sub>LED</sub> =17mA, 1.42 max. (9 points)	
	8	Note1. 5 points, Note3. $\delta_{W5}$	Note1. 9 points, Note3. $\delta_{W9}$	
	9	Note 5. $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$	$Y_L = [L(1) + L(2) + L(3) + L(4) + L(5) + L(6) + L(7) + L(8) + L(9)] / 9$	
	25	8.1.1 Standard Front view	Update to latest version	
	24	7.3 Reliability test	Update to latest data	
1.3 2011/06/16	6	Physical Size without bracket / tape	Modify the Length / Width tolerance of LCM from +,-0.5mm to +,-0.3mm	
	16	DCR Mode Duty Index	Duty range changed to 85%~95%	
	22	6.4.1 Timing Characteristics	Parameter aligned with EDID: C2 ver	
	23	6.5 Power ON/OFF Sequence	Setting of power NO/OFF sequence	
	24	7.3 Reliability test	Referred by H429AL01, modify the spec	
1.4 2011/06/22	23	6.5 Power ON/OFF Sequence	Setting of power NO/OFF sequence	
1.5 2011/06/23	6	Power Consumption	3.10 max. (Include Logic and BLU power)	
	14	Power Specification	VDD Power: from 0.88W to 0.8W IDD Current: 242.4 mA	
	17	5.2.1 LED characteristics	Backlight Power Consumption: 2.3W,max	



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1.6 2011/07/04	32	9.2 Carton Package	Update the design of carton package : from TBD to actual OD	
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### 1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



## Product Specification

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### 2. General Description

B101EW05 V7 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 WXGA, 1280(H) x 800(V) screen and 16.7M colors (RGB 6-bits + FRC data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B101EW05 V7 is designed for a display unit of notebook style personal computer and industrial machine.

### 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	255.85 (10.07W")			
Active Area	[mm]	216.96(H) x 135.6(V)			
Pixels H x V		1280 x 3(RGB) x 800			
Pixel Pitch	[mm]	0.1695 X 0.1695			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (I <sub>LED</sub> =17mA) (Note: I <sub>LED</sub> is LED current)	[cd/m <sup>2</sup> ]	300 typ. (9 points average w/o touch panel) 255 min. (9 points average w/o touch panel)			
Luminance Uniformity		1.42 max. (9 points)			
Contrast Ratio		1300 typ, 1000 min.			
Response Time	[ms]	25 typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.10 max. (Include Logic and BLU power)			
Weight	[Grams]	180 max.			
Physical Size without bracket / tape	[mm]		Min.	Typ.	Max.
		Length	229.16	229.46	229.76
		Width	148.80	149.10	149.40
		Thickness	---	---	5.3
Electrical Interface		1 channel LVDS			
Glass Thickness	[mm]	0.3			



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Surface Treatment		Anti-Reflection $\leq 1.5\%$ , Hardness 3H
Support Color		16.7M colors ( RGB 6-bit + FRC)
Temperature Range Operating Storage (Non-Operating)	$^{\circ}\text{C}$ $^{\circ}\text{C}$	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

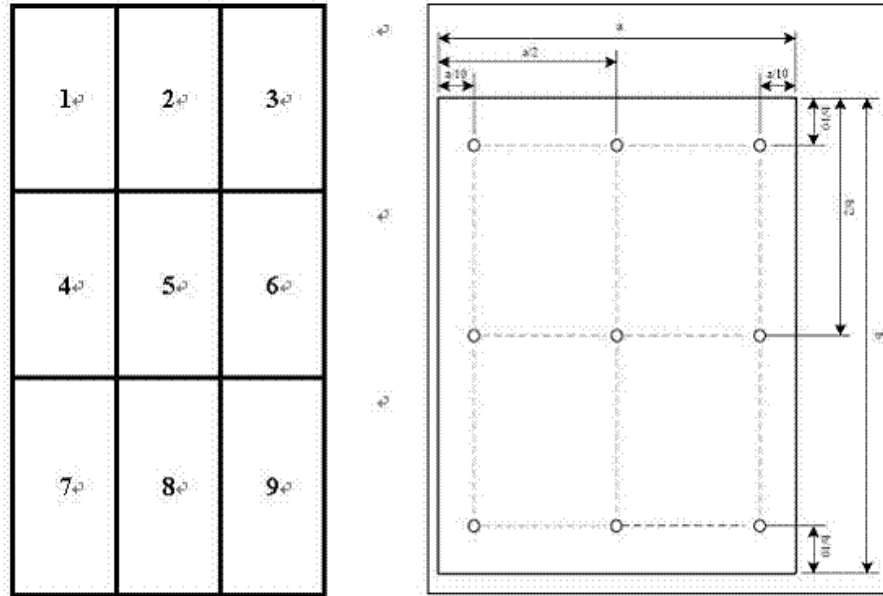
## 2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

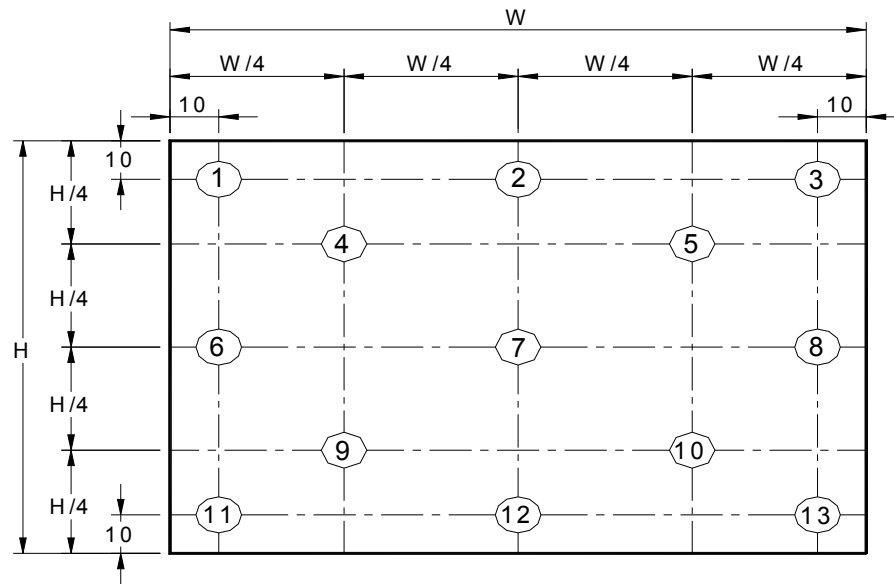
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance $I_{LED}=17\text{mA}$		9 points average	255	300	---	$\text{cd/m}^2$	1, 4, 5.
Viewing Angle	$\theta_R$	Horizontal (Right)	80	85	---	degree	4, 9
	$\theta_L$	CR = 10 (Left)	80	85	---		
	$\psi_H$	Vertical (Upper)	80	85	---		
	$\psi_L$	CR = 10 (Lower)	80	85	---		
Luminance Uniformity	$\Delta_{9P}$	9 Points	---	---	1.42		1, 3, 4
Luminance Uniformity	$\delta_{13P}$	13 Points	---	---	1.50		2, 3, 4
Contrast Ratio	CR		1000	1300	-		4, 6
Cross talk	%	[A] By AUO test cond. [B] By test cond.	---	---	[A] 4 [B] 5		4, 7
Flicker	dB				-20		
Response Time	$T_{RT}$	Rising + Falling	---	25	35	msec	4, 8
Color / Chromaticity Coordinates	Red	Rx	0.547	0.577	0.607		10
		Ry	0.306	0.336	0.366		
	Green	Gx	0.294	0.324	0.354		
		Gy	0.521	0.551	0.581		
	Blue	Bx	0.122	0.152	0.182		
		By	0.098	0.128	0.158		
	White	Wx	0.280	0.310	0.340		
		Wy	0.290	0.320	0.350		
NTSC	%		-	45	-		



**Note 1:** 9 points position (Ref: Active area)



**Note 2:** 13 points position (Ref: Active area)



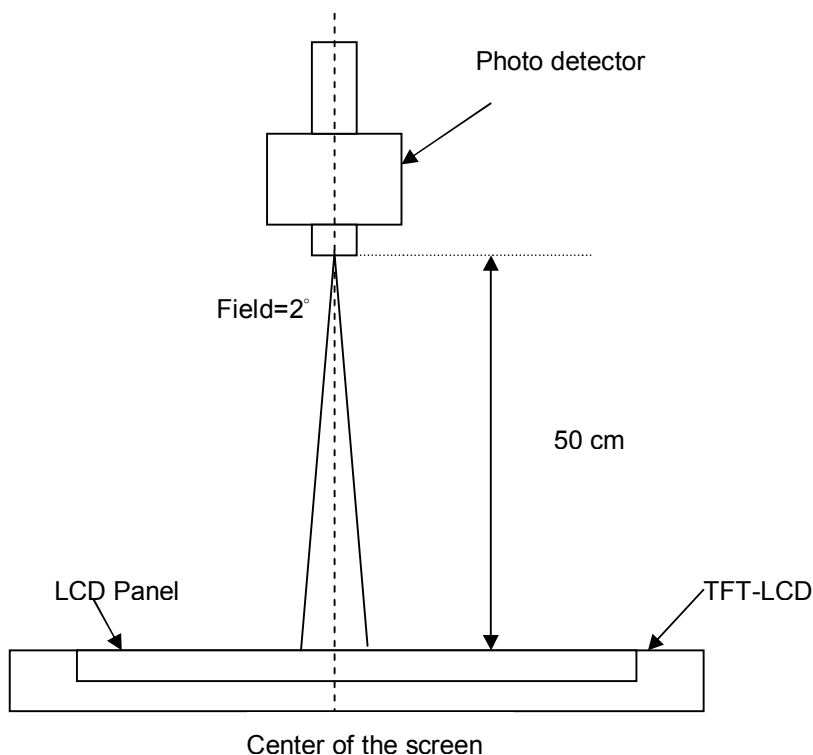
**Note 3:** The luminance uniformity of 9 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{w9} = \frac{\text{Maximum Brightness of nine points}}{\text{Minimum Brightness of nine points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

## Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



## Note 5 : Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 63 at 9 points ,

$$Y_L = [L(1) + L(2) + L(3) + L(4) + L(5) + L(6) + L(7) + L(8) + L(9)] / 9$$

$L(x)$  is corresponding to the luminance of the point X at Figure in Note (1).

## Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

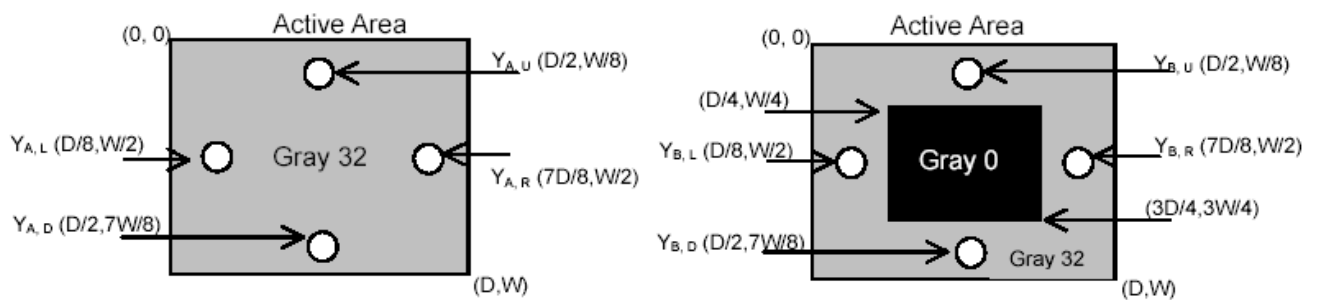
**Note 7 :** Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

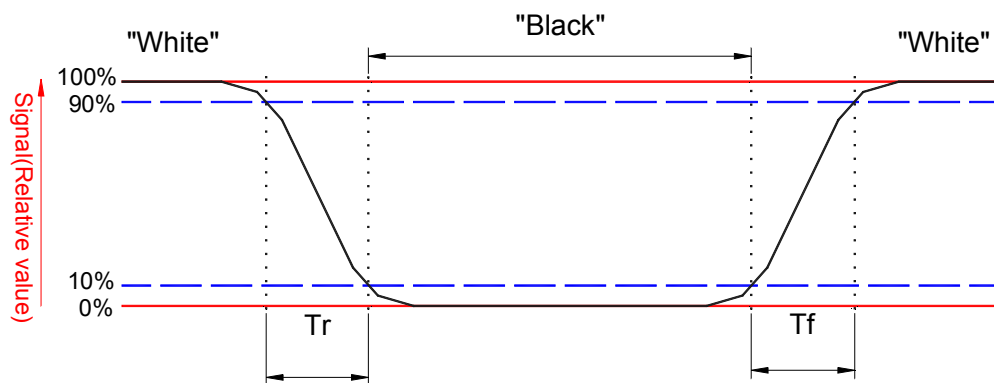
$Y_A$  = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

$Y_B$  = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)



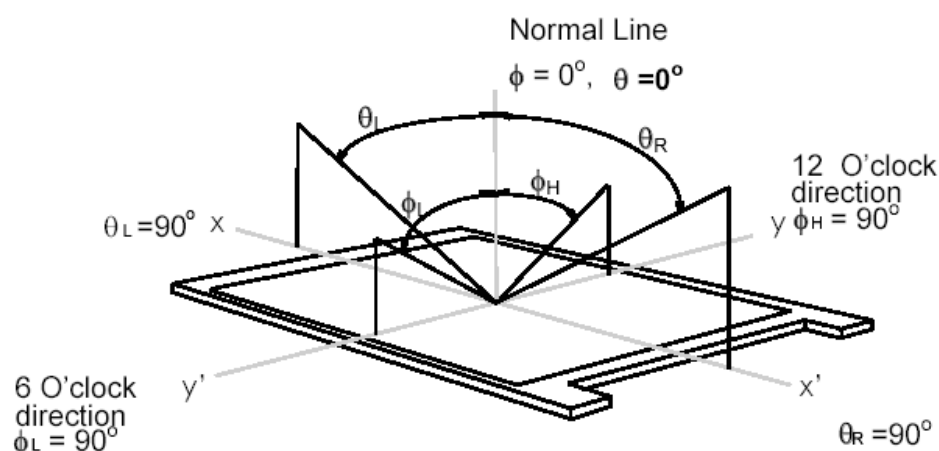
**Note 8:** Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



## Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a  $180^\circ$  horizontal and  $180^\circ$  vertical range (off-normal viewing angles). The  $180^\circ$  viewing angle range is broken down as follows;  $90^\circ$  ( $\theta$ ) horizontal left and right and  $90^\circ$  ( $\phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



## Note 10. LED BIN definition

1. The LED color BIN could be defined for Nichia 208 (0.8t)
2. B101EW05 V7:

(1). Below 20 LED BIN would be introduced to meet LCM color spec & recent MP demands –

Sa6265	Sa6266	Sbj255	Sbj256	Sbj265
Sa6267	Sa6268	Sbj257	Sbj258	Sbj267
Sa6285	Sa6286	Sbj275	sbj276	Sbj285
Sa6287	Sa6288	Sbj277	Sbj278	Sbj287

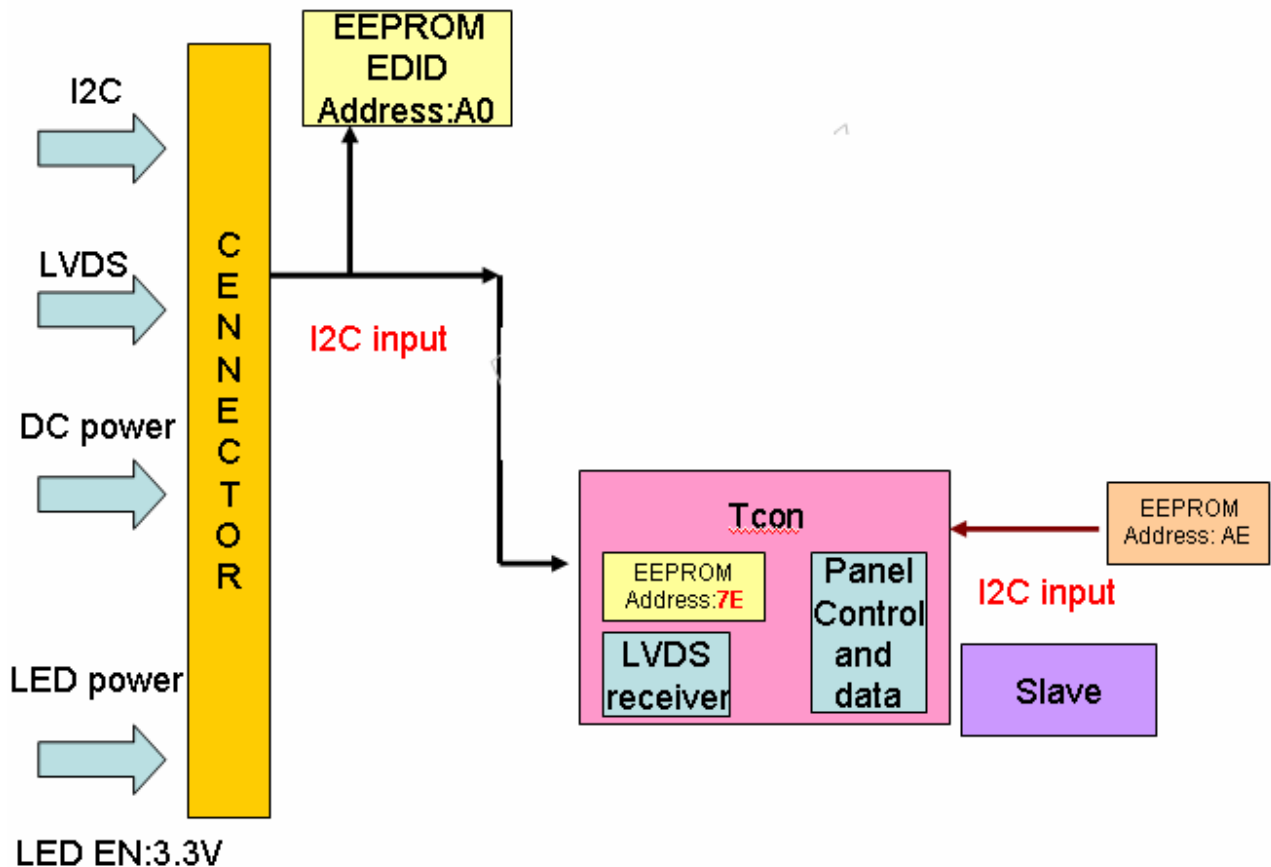
(2). If the MP demands would increase, below 40 LED BIN might be introduced after AUO RD verification

Sa5265	Sa5266	Sa6255	Sa6256	Sa6265	Sa6266	Sbj255	Sbj256	Sbj265	Sbj266
Sa5267	Sa5268	Sa6257	Sa6258	Sa6267	Sa6268	Sbj257	Sbj258	Sbj267	sbj268
Sa5285	Sa5286	Sa6275	Sa6276	Sa6285	Sa6286	Sbj275	sbj276	Sbj285	Sbj286
Sa5287	Sa5288	Sa6277	Sa6278	Sa6287	Sa6288	Sbj277	Sbj278	Sbj287	Sbj288

## 3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 40 Pin one channel Module

### 10.1" 2D LCM I2C Structure





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### 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

#### 4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

#### 4.2 Absolute Ratings of Environment

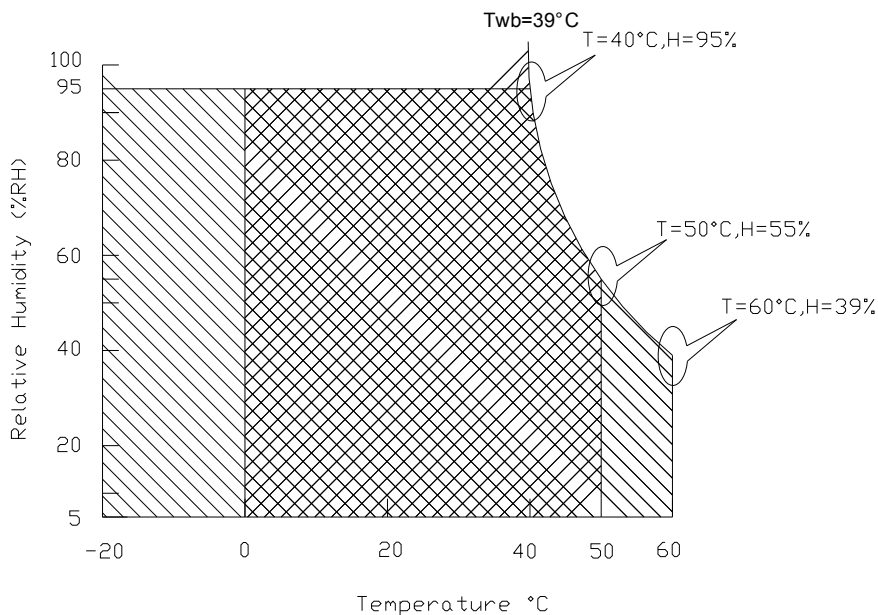
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C )



Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

## 5. Electrical Characteristics

## 5.1 TFT LCD Module

### 5.1.1 Power Specification

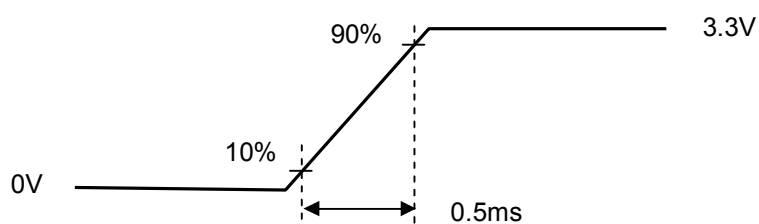
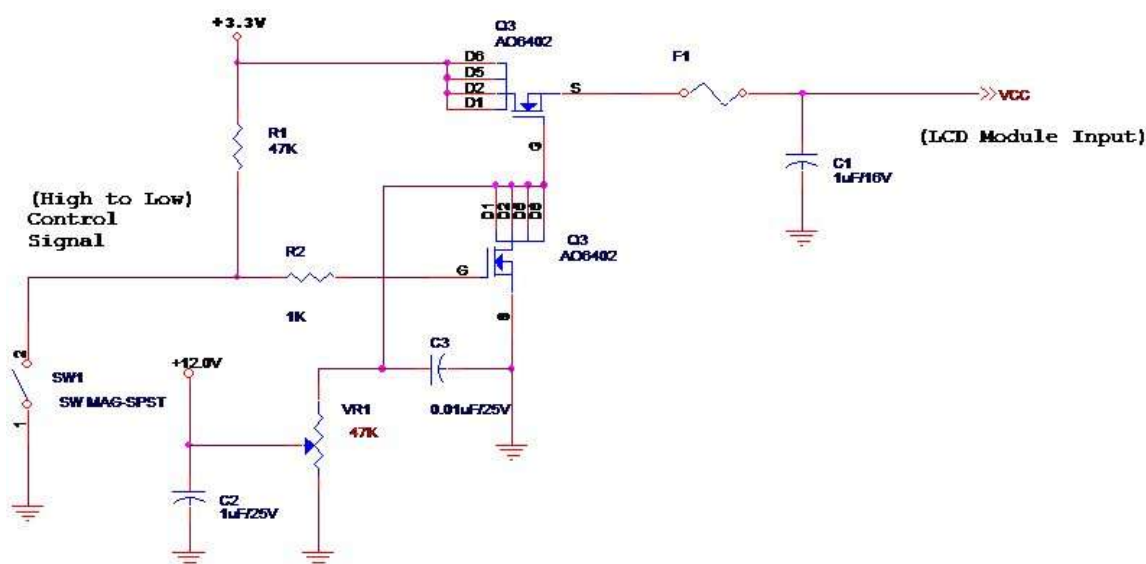
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.8	[Watt]	Note 1
IDD	IDD Current	-	-	242.4	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : White Pattern at 3.3V driving voltage. ( $P_{\max} = V_{3.3} \times I_{\text{black}}$ )

Note 2 : Measure Condition





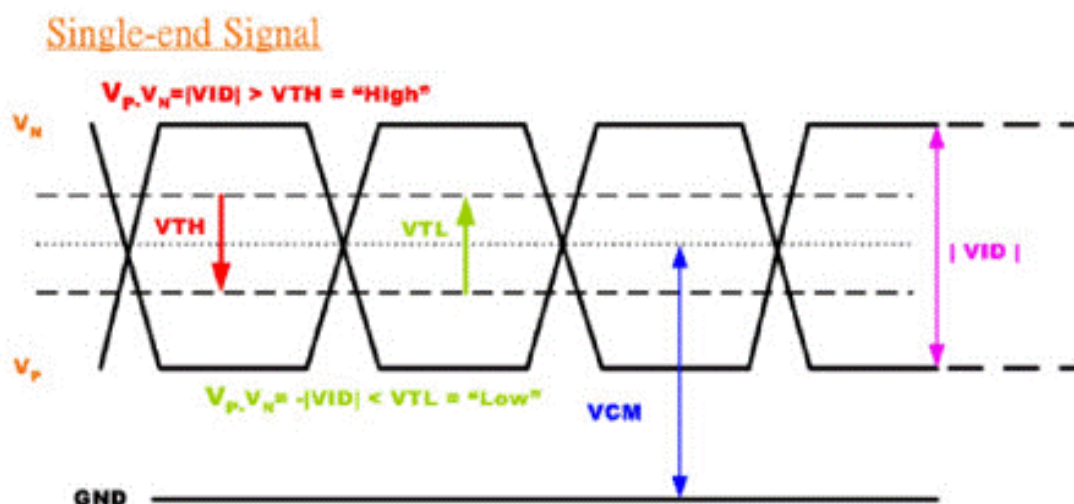
## 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
$V_{TH}$	Differential Input High Threshold ( $V_{cm}=+1.2V$ )	---	100	[mV]
$V_{TL}$	Differential Input Low Threshold ( $V_{cm}=+1.2V$ )	-100	---	[mV]
$ V_{ID} $	Differential Input Voltage	100	600	[mV]
$V_{CM}$	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform







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### 5.1.3 Dynamic contrast ratio Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
Dynamic contrast ratio(DCR) Input High Level	DCR_EN	2.5	-	5.5	[Volt]	Define as Connector Interface (Ta=25℃)
Dynamic contrast ratio(DCR) Input Low Level		-	-	0.8	[Volt]	
DCR Mode Duty Index	Duty	85	-	95	%	Note 1
L0 Gray level	Power	-	0.7P	-	Watt	Note 2
L63 Gray level	Power	-	1P	-	Watt	

**Note 1:** The minimums dynamic contrast ratio is setting at darkness, and a maximum is setting at brightness.

**Note 2:** The power saving capability refer to original Backlight power consumption (P)



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### 5.2 Backlight Unit

#### 5.2.1 LED characteristics

The LED lightbar is consisted of Nichia 208 (0.8t) x 36ea, and the circuit is 6 series and 6 parallel.

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.30	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 If=17mA

**Note 1:** Calculator value for reference  $P_{LED} = V_F \text{ (Normal Distribution)} * I_F \text{ (Normal Distribution)} / \text{Efficiency}$

**Note 2:** The LED life-time define as the estimated time to 50% degradation of initial luminous.

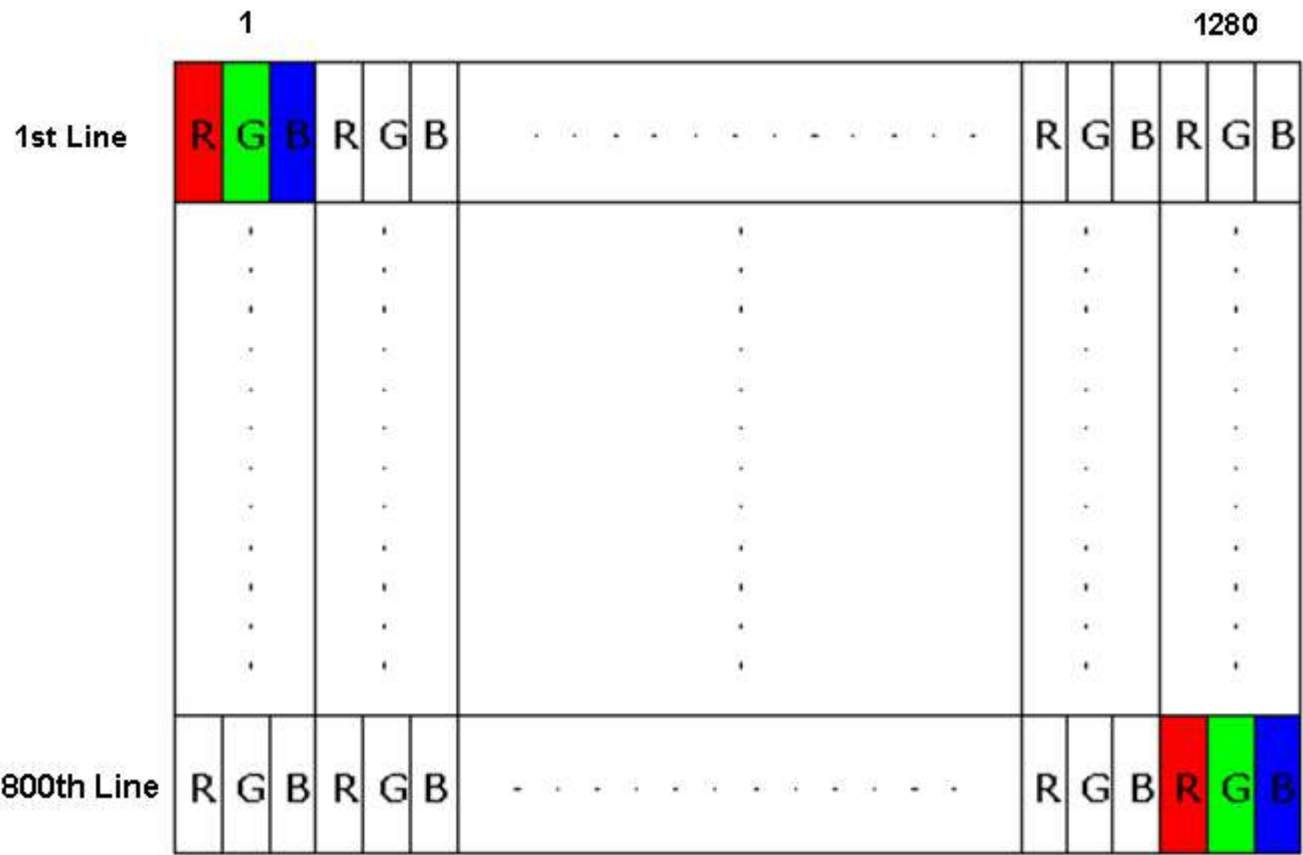
#### 5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.5	12.0	15.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	100	-	1K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

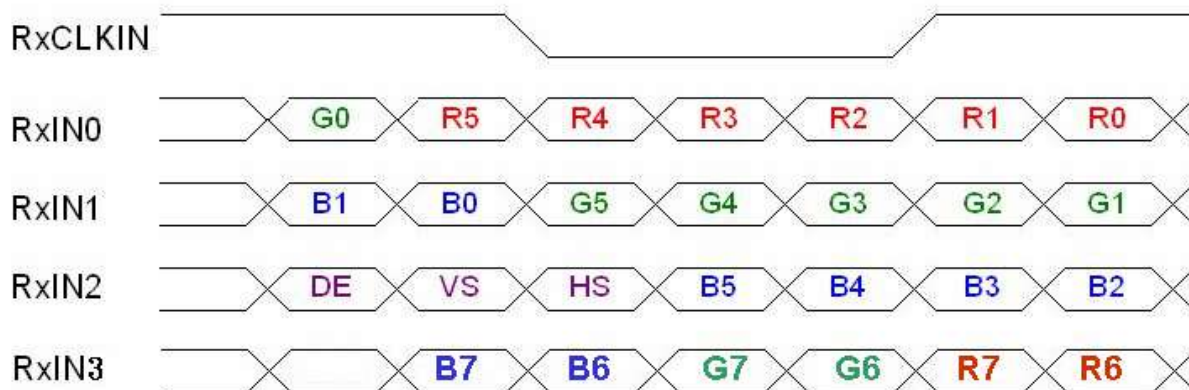
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



## 6.2 The Input Data Format



Signal Name	Description	
R7 R6 R5 R4 R3 R2 R1 R0	Red Data 7 (MSB) Red Data 6 Red Data 5 Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 8 bits pixel data.
G7 G6 G5 G4 G3 G2 G1 G0	Green Data 7 (MSB) Green Data 6 Green Data 5 Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 8 bits pixel data.
B7 B6 B5 B4 B3 B2 B1 B0	Blue Data 7 (MSB) Blue Data 6 Blue Data 5 Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 8 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off

## 6.3 Integration Interface Requirement

### 6.3.1 LVDS Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

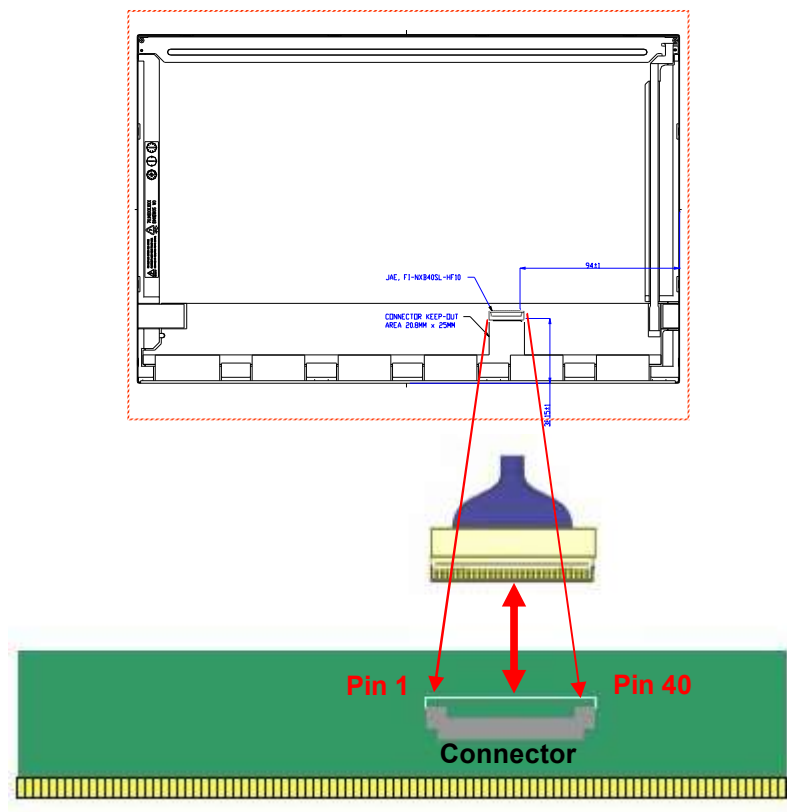
Connector Name / Designation	For Signal Connector
Manufacturer	I-PEX or Compatible
Type / Part Number	I-PEX 20455-040E-12R or Compatible
Mating Housing/Part Number	IPEX 20453-040T-11or Compatible

### 6.3.2 LVDS Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	NC	No Connection (Reserve)
2	VDD	Power Supply +3.3V
3	VDD	Power Supply +3.3V
4	VEDID	EDID +3.3V Power
5	AGING	Aging Mode Power Supply
6	CLK_EDID	EDID Clock Input (3.3V) note2
7	DAT_EDID	EDID Data Input (3.3V) note2
8	Rin0-	-LVDSdifferential data input(R0-R5,G0)
9	Rin0+	+LVDSdifferential data input(R0-R5,G0)
10	GND	Ground
11	Rin1-	-LVDSdifferential data input(G1-G5,B0-B1)
12	Rin1+	+LVDSdifferential data input(G1-G5,B0-B1)
13	GND	Ground
14	Rin2-	-LVDSdifferential data input(B2-B5,HS,VS,DE)
15	Rin2+	+LVDSdifferential data input(B2-B5,HS,VS,DE)
16	GND	Ground
17	CIKIN-	-LVDSdifferential clock input
18	CIKIN+	+LVDSdifferential clock input
19	NC	No Connection (Reserve)
20	Rin3-	-LVDSdifferential data input(R6,R7,G6,G7,B6,B7)
21	Rin3+	+LVDSdifferential data input(R6,R7,G6,G7,B6,B7)
22	GND	Ground–Shield
23	NC	No Connection (Reserve)
24	GND	Ground–Shield
25	NC	No Connection (Reserve)

26	GND	Ground–Shield
27	NC	No Connection (Reserve)
28	GND	Ground–Shield
29	NC	No Connection (Reserve)
30	NC	No Connection (Reserve)
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection (Reserve)
35	LED_PWM	System PWM Logic Input Level
36	VLED_EN	LED enable input level (5.0V)
37	DCR_EN	DCR enable input level (5.0V)
38	VLED	LED Power Supply (12V)
39	VLED	LED Power Supply (12V)
40	VLED	LED Power Supply (12V)



Note1: Input signals shall be low or High-impedance state when VDD is off.

## 6.4 LVDS Interface Timing

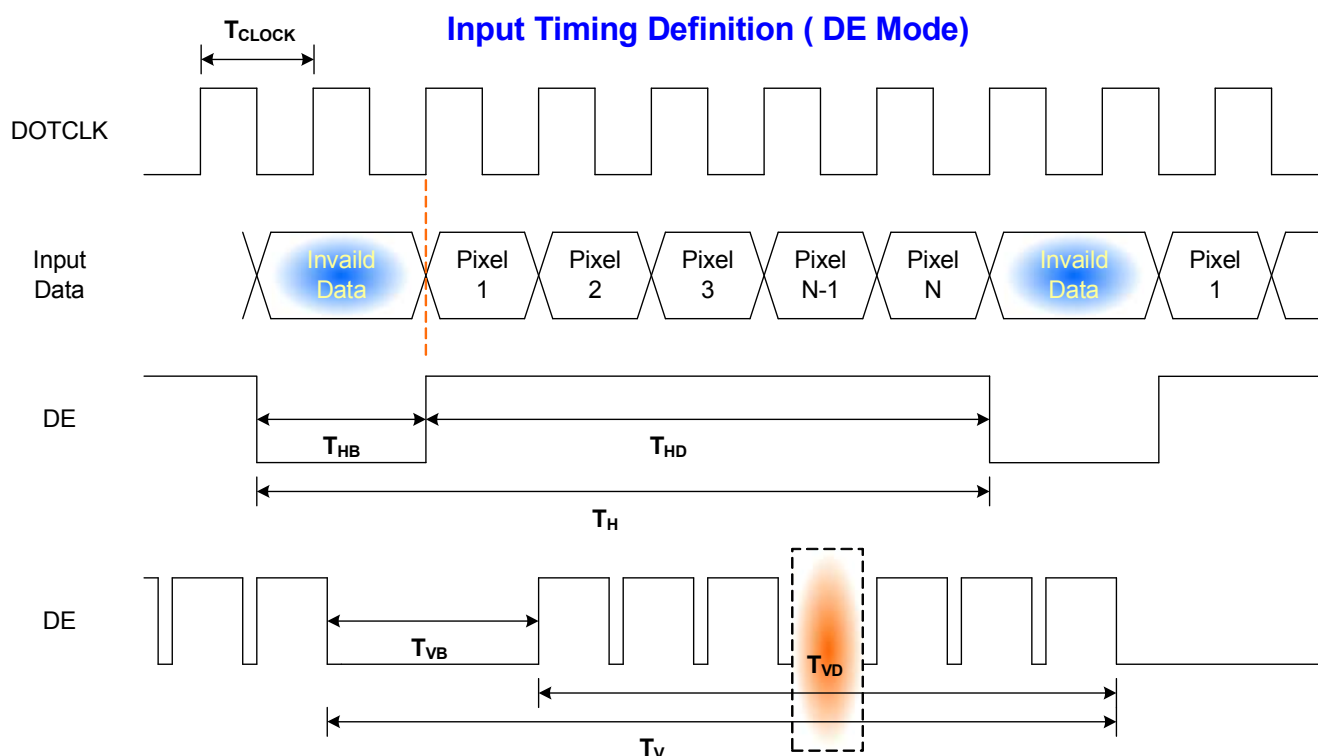
### 6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T <sub>Clock</sub>		71.1		MHz
Vertical Section	Period	T <sub>V</sub>	808	808	1023	T <sub>Line</sub>
	Active	T <sub>VD</sub>	800			
	Blanking	T <sub>VB</sub>	8	8	223	
Horizontal Section	Period	T <sub>H</sub>	1340	1466	2047	T <sub>Clock</sub>
	Active	T <sub>HD</sub>	1280			
	Blanking	T <sub>HB</sub>	60	186	767	

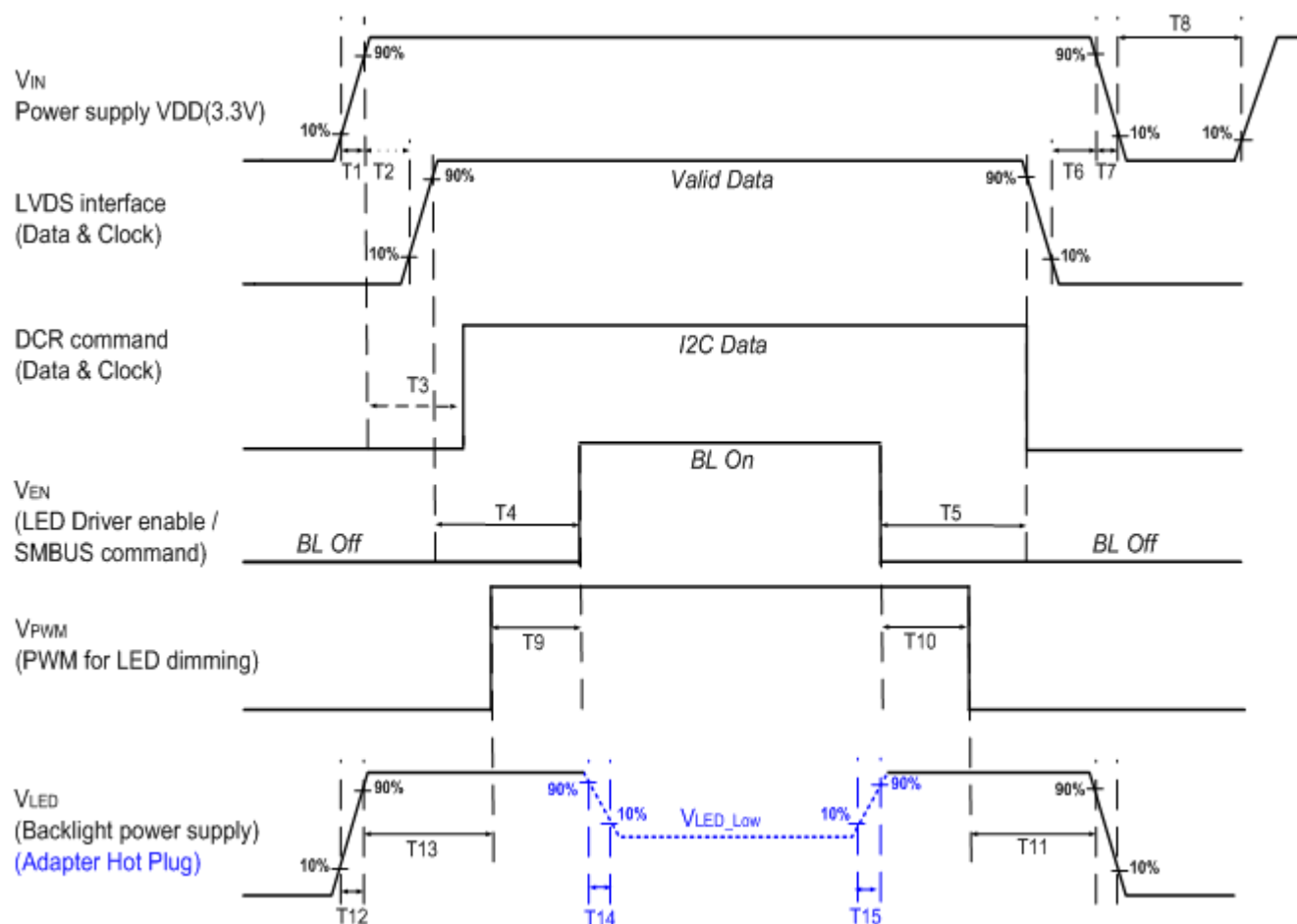
Note : DE mode only

### 6.4.2 Timing diagram



## 6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



	Min (ms)	Max (ms)
T1	0.5	10
T2	0	50
T3	150	-
T4	200	-
T5	0	-
T6	0	50
T7	0	10
T8	300	-
T9	10	-
T10	10	-
T11	10	-
T12	0.5	10
T13	10	-

	Min (ms)	Max (ms)
T14	1*	-
T15	1*	-

Seamless change:  $T14/T15 = 5 \times T_{PWM}^*$

\* $T_{PWM} = 1/PWM \text{ Frequency}$



## 7. Panel Reliability Test

### 7.1 Vibration Test

Test Spec:

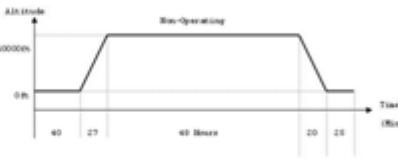
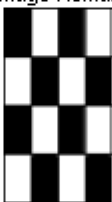
- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

### 7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

### 7.3 Reliability Test

Category	No.	Test items	Conditons	Remark
Reliability (Environment)	1	High Temp. Operation	Ta = + 60°C 240 hours	
	2	High Temp. Storage	Ta = + 70°C 240 hours	Non-operation
	3	Low Temp. Operation	Ta = - 20°C 240 hours	
	4	Low Temp. Storage	Ta = - 30°C 240 hours	Non-operation
	5	High Temp. / Humi. Operation	Ta = + 40°C , 95% RH 240 hours	
	6	High Temp. / Humi. Storage	Ta = + 60°C , 90% RH 240 hours	Non-operation <b>Note. 1</b>
	7	Thermal Shock	-30°C (30 min) ~ +70°C (30 min), 50 cycles	Non-operation
	8	Low Pressure Storage	40,000ft, room temperature, 48 hours 	Non-operation
Picture Quality	9	<b>Image Remaining (Sticking)</b>	<p>Image Remaining test</p>  <p>Condition 1: 40°C , 12 hours Black/white block interleave pattern (4X4). Criterion: The LCM cannot be found any image remaining on Middle Gray pattern (128/255) after 12 hour recovery.</p> <p>Condition 2: 25°C , 48 hours Black/white block interleave pattern. Criterion: 1. Cannot found any image remaining on Black /white interleave pattern 2. Cannot found any image remaining on Middle Gray pattern after 24 hour recovery.</p>	

Reliability (Mechanical)	10	Anti-Dust	First to perform thermal shock test before dust test. Temp. range: 15°C to 35°C Particle size: 50 micrometer Duration time: 8hrs BS EN 60529: IP5X degree of protection Including the test sequence 1~4	Non-operation																				
			The box files with enough talcum powder to cover up UUT and the box only contain 1 unit. Test shall be continued for a period of 1 minute. No dust or particle should appear on the display area and the gap between the backlight module and LCD housing or shielding frame.	Non-operation <b>Note. 2</b>																				
	11	Shock Test	Half sine 400G, duration time 2ms. One shock for each face, total 6 shocks.	Non-operation																				
	12	Random Vibration Test	0.025G <sup>2</sup> /Hz, 10 to 500Hz. Nominal 3.5Grms in each axis, 30 minutes each axis.	Non-operation																				
	13	Sinusoidal Vibration Test	5g Zero-to peak, 0.5 octave/minutes sweep rate. One sweep, 10 to 500 Hz, all 3 axes (X, Y, Z). Fixture used: Fasten the specimen to the vibration table. Power is OFF.	Non-operation																				
	14	LCM Connector Insert / Remove	Insert/Remove LCM connector for 15 cycles.																					
Reliability (LED)	15	LED Life	Luminance should be larger than half of initial luminance after 5,000 hrs operating at 25°C and ILED=20mA (If the rating current is not 20mA, vendor needs inform HTC.)																					
LED Forward Current	16	LED Forward Current	LED Forward Current limitation should not be less than 20mA when the ambient temperature is 60°C	<b>Note. 3</b>																				
ESD	17	IEC 6100-4-2 Air Discharge +/- 15KV Contact Discharge +/- 8KV	According to ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.																					
LED Rank	18	LED Color Rank	<table border="1"> <tr><td>Sa6265</td><td>Sa6266</td><td>Sb255</td><td>Sb256</td><td>Sb265</td></tr> <tr><td>Sa6267</td><td>Sa6268</td><td>Sb257</td><td>Sb258</td><td>Sb267</td></tr> <tr><td>Sa6285</td><td>Sa6286</td><td>Sb275</td><td>Sb276</td><td>Sb285</td></tr> <tr><td>Sa6287</td><td>Sa6288</td><td>Sb277</td><td>Sb278</td><td>Sb287</td></tr> </table>	Sa6265	Sa6266	Sb255	Sb256	Sb265	Sa6267	Sa6268	Sb257	Sb258	Sb267	Sa6285	Sa6286	Sb275	Sb276	Sb285	Sa6287	Sa6288	Sb277	Sb278	Sb287	
Sa6265	Sa6266	Sb255	Sb256	Sb265																				
Sa6267	Sa6268	Sb257	Sb258	Sb267																				
Sa6285	Sa6286	Sb275	Sb276	Sb285																				
Sa6287	Sa6288	Sb277	Sb278	Sb287																				
LED Model	19	LED Model	Maker: Nichia, Model: NNSV208A																					

#### Note 1:

About High temperature / Humidity (Non-OP) -- +60°C, 90%RH, 240 hours

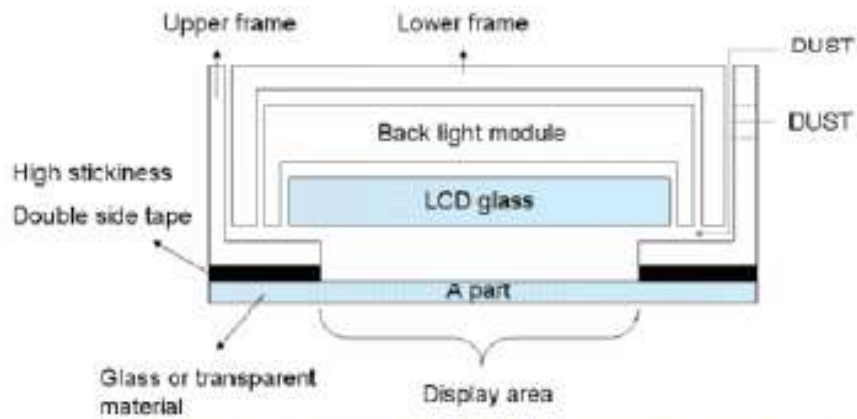
Verification results by AUO:

(1). T200 check: NO P mura, and all pass test criteria.

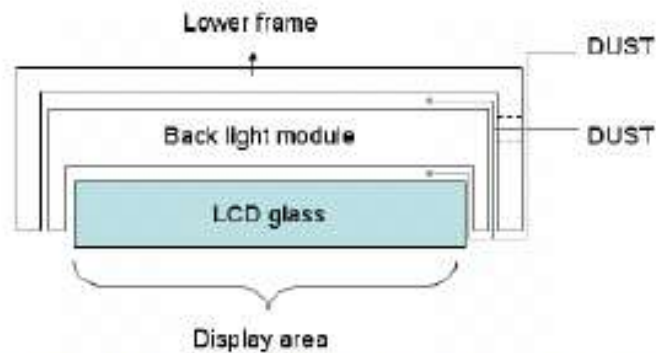
(2). T240 check: P mura occurred, but NON-visible after 3hrs re-check

#### Note 2:

Sequence 1: To add a glass or transparent material to cover the display area and fixed by high stickiness double side tape around the frame. Then do the dust test according above two conditions, if the LCM is without upper frame. It needn't pass a part during test.



Test Unit: With upper frame type have to add A part



Test Unit: Without upper frame type doesn't add A part.

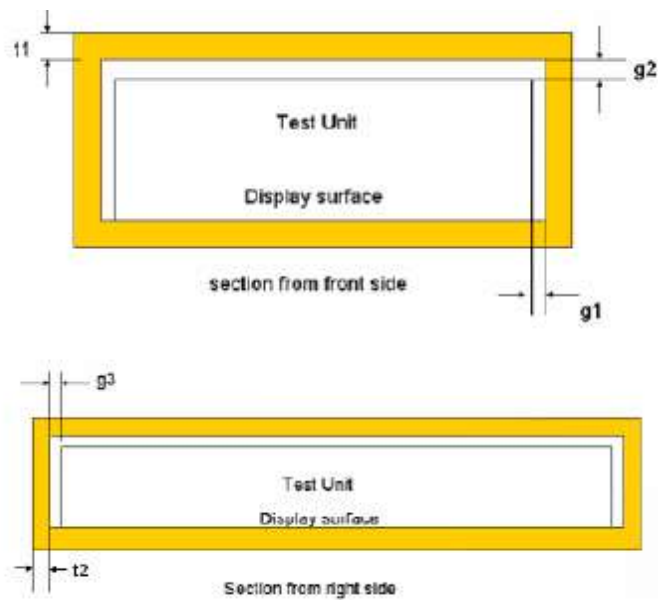
Sequence 2: after dust test, put the panel with A part in the jig. Jig dimension  $t_1$ ,  $t_2$ ,  $g_1$ ,  $g_2$  and  $g_3$  have to be defined (show as below picture).

$t_1 = t_2 = 1 \text{ mm}$

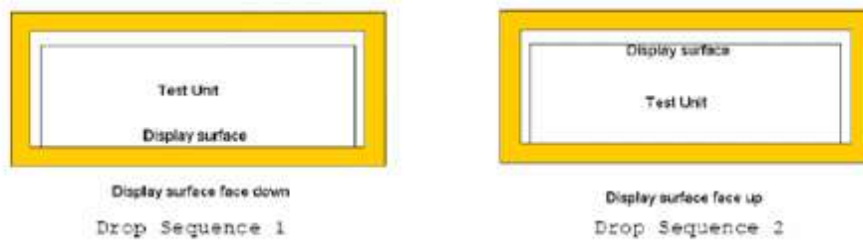
$g_1 = g_3 = 0.1 \text{ mm}$

$g_2 = 0.2 \text{ mm}$

if there has other concern, the dimensions of jig could be defined case by case

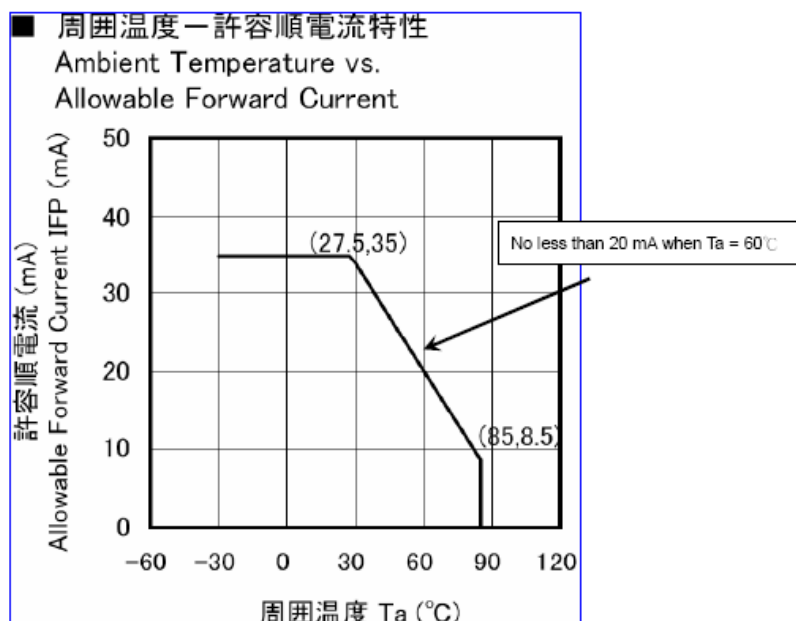


Sequence 3: Drop the jig for each ten cycle for front side and back side.  
 Drop height: 10cm  
 Drop cycle: ten cycles  
 Drop Sequence: 1 cycle means display surface face down then face up for each time.(show as below picture)

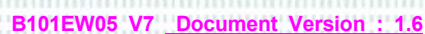


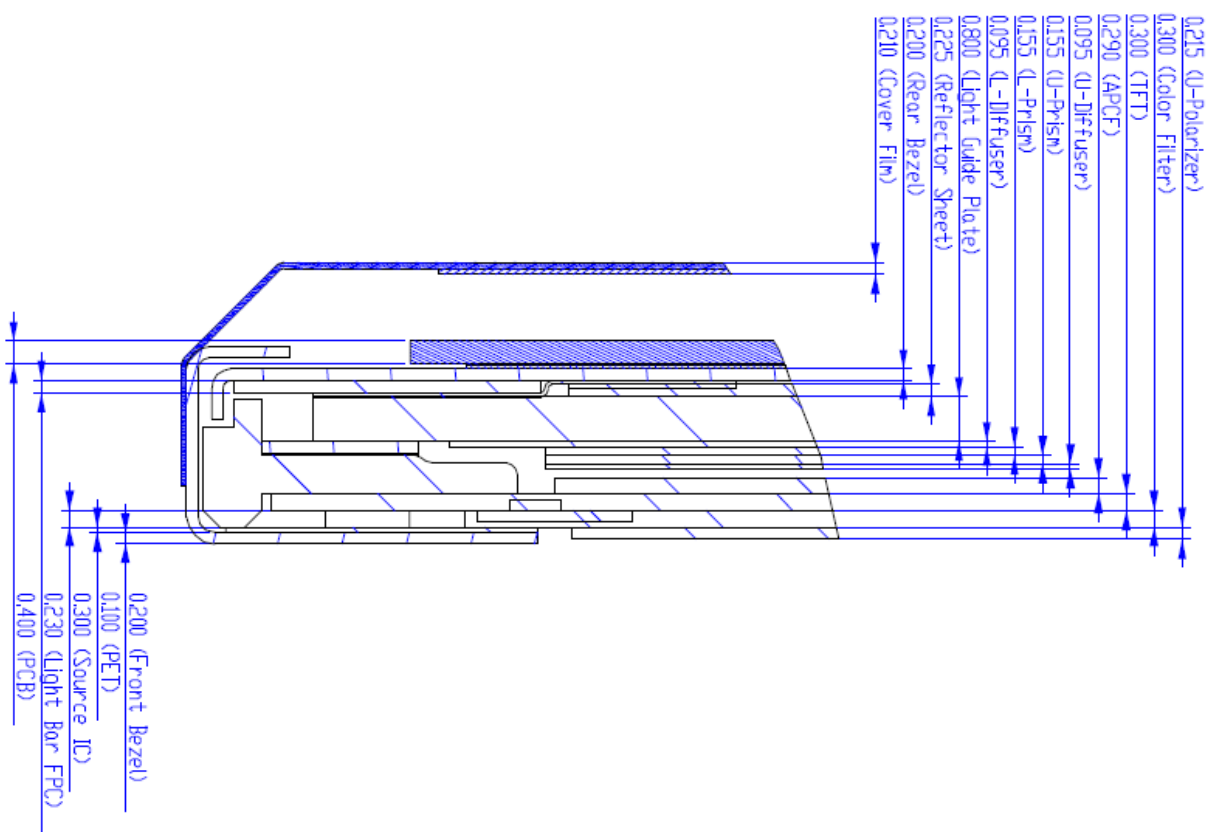
Sequence 4: Remove the dust on the A part or LCD polarizer and check the dust if appear on the display area.

### Note.3

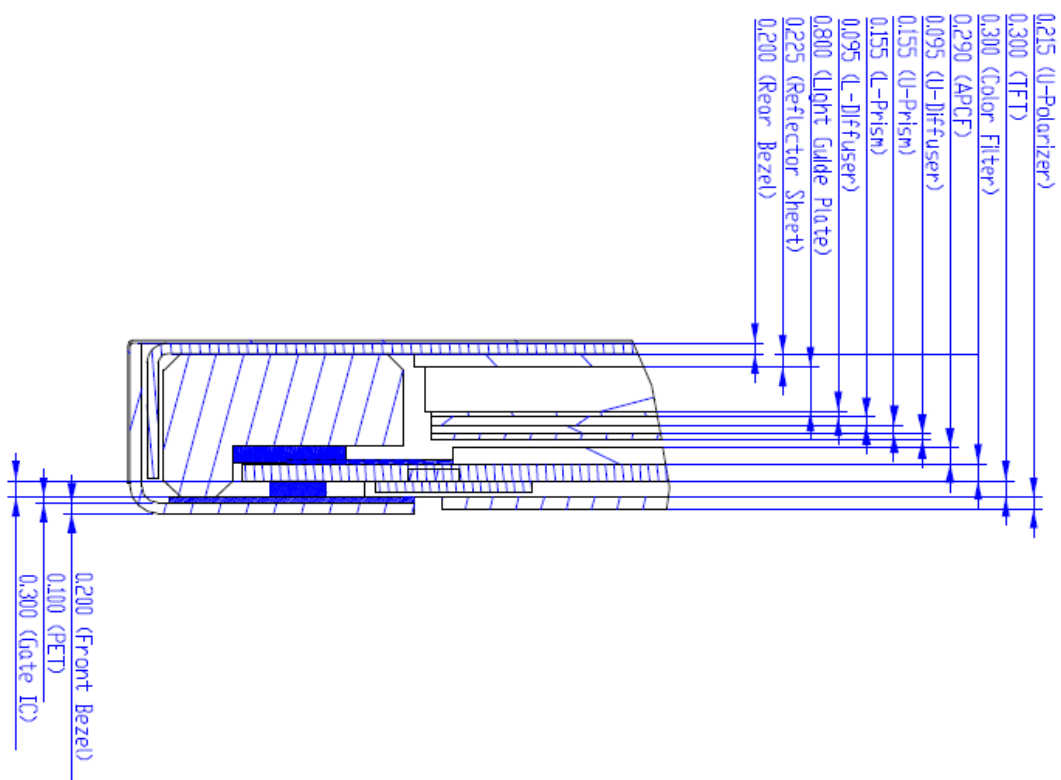


### 8.1.1 Standard Front View





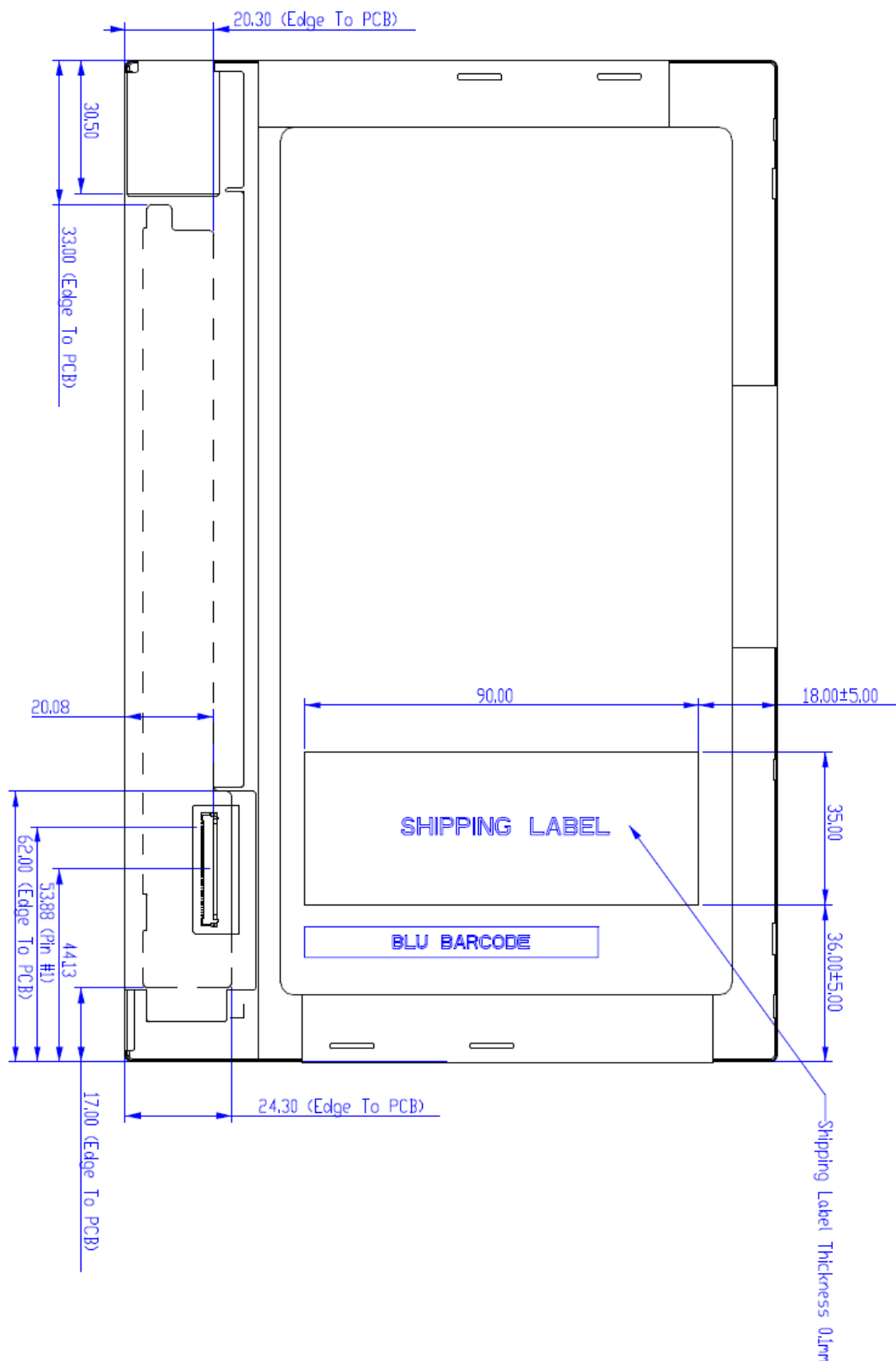
SECTION  
V\_CENTER-V\_CENTER  
SCALE 10.000



SECTION  
H\_CENTER-H\_CENTER  
SCALE 10.000

### 8.1.2 Standard Rear View & Key components remark and remind

Prevention damage the IC, connector, Capacitor...., we recommend your design (Ex: cable, rib, hardness parts) far away those section those have remarked at this



Note: Prevention IC damage, IC positions not allowed any overlap over these areas.



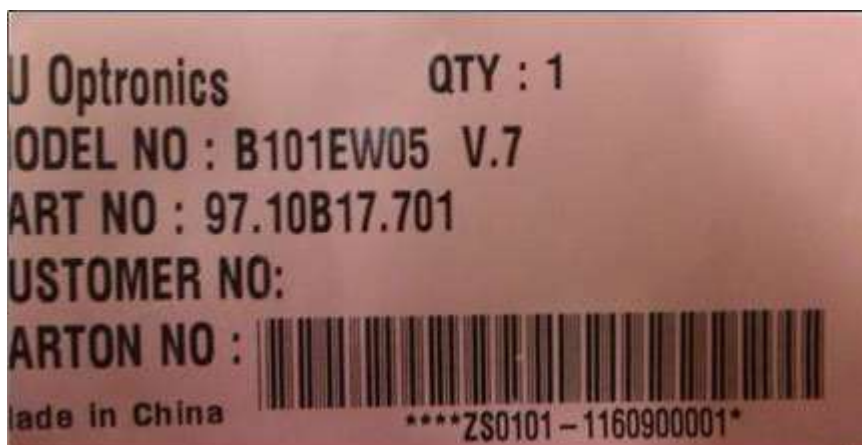
## 9. Shipping and Package

### 9.1 Shipping and carton Label Format

#### Shipping label



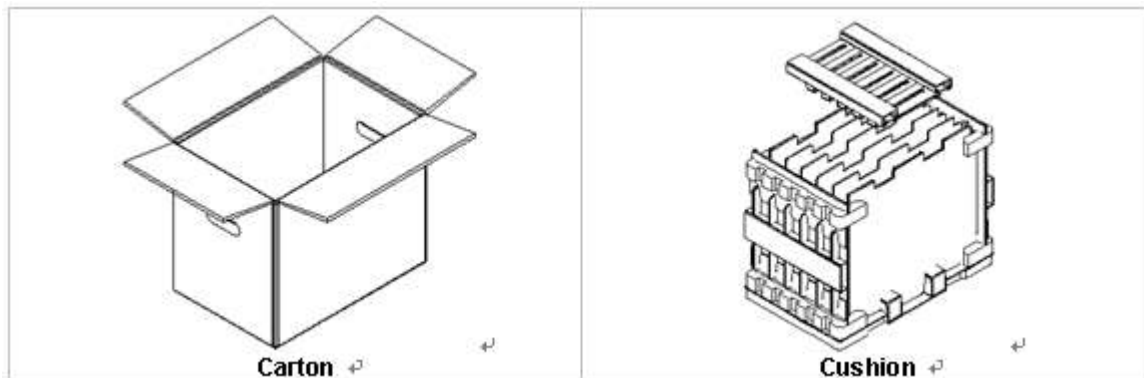
#### Carton label



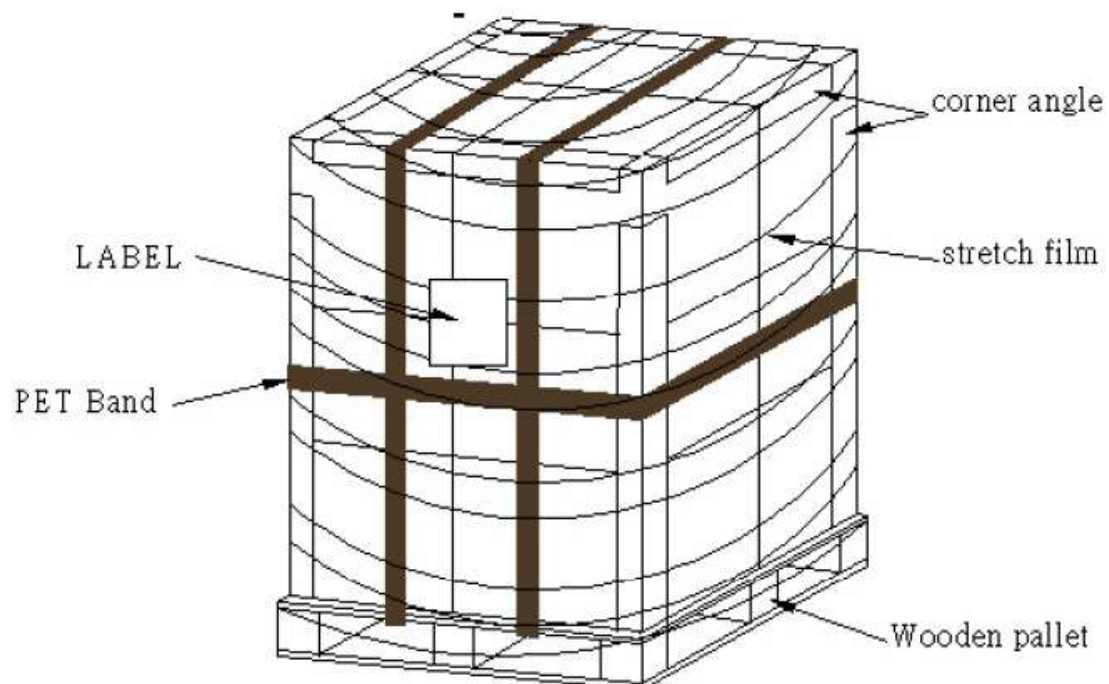


## 9.2 Carton Package

The outside dimension of carton is 445 (L)mm x 283 (W)mm x 373 (H)mm



## 9.3 Shipping Package of Palletizing Sequence



## 10. Appendix

### 10.1 EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	D4	11010100	212	
0B	hex, LSB first	57	01010111	87	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	08	00001000	8	
11	Year of manufacture	15	00010101	21	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	<b>Video input def.</b> <i>(digital I/P, non-TMDS, CRGB)</i>	A0	10100000	160	
15	<b>Max H image size</b> <i>(rounded to cm)</i>	16	00010110	22	
16	<b>Max V image size</b> <i>(rounded to cm)</i>	0E	00001110	14	
17	<b>Display Gamma</b> <i>(=<math>\gamma \times 100</math>)-100)</i>	96	10010110	150	
18	<b>Feature support</b> <i>(no DPMS, Active OFF, RGB, tmg Blk#1)</i>	02	00000010	2	
19	Red/green low bits <b>(Lower 2:2:2:2 bits)</b>	C0	11000000	192	
1A	Blue/white low bits <b>(Lower 2:2:2:2 bits)</b>	34	00110100	52	
1B	Red x <b>(Upper 8 bits)</b>	93	10010011	147	
1C	Red y/ highER 8 bits	56	01010110	86	
1D	Green x	53	01010011	83	
1E	Green y	8D	10001101	141	
1F	Blue x	27	00100111	39	
20	Blue y	20	00100000	32	
21	White x	4F	01001111	79	
22	White y	52	01010010	82	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	

2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	46	01000110	70	
37	Pixel Clock/10000 USB	1B	00011011	27	
38	Horz active <b>Lower 8bits</b>	00	00000000	0	
39	Horz blanking <b>Lower 8bits</b>	A0	10100000	160	
3A	HorzAct:HorzBlnk <b>Upper 4:4 bits</b>	50	01010000	80	
3B	Vertical Active <b>Lower 8bits</b>	20	00100000	32	
3C	Vertical Blanking <b>Lower 8bits</b>	08	00001000	8	
3D	Vert Act : Vertical Blanking <b>(upper 4:4 bit)</b>	30	00110000	48	
3E	HorzSync. Offset	08	00001000	8	
3F	HorzSync.Width	0A	00001010	10	
40	VertSync.Offset : VertSync.Width	31	00110001	49	
41	Horz&Vert Sync Offset/Width <b>Upper 2bits</b>	00	00000000	0	
42	Horizontal Image Size <b>Lower 8bits</b>	D8	11011000	216	
43	Vertical Image Size <b>Lower 8bits</b>	87	10000111	135	
44	Horizontal & Vertical Image Size <b>(upper 4:4 bits)</b>	00	00000000	0	
45	Horizontal Border <i>(zero for internal LCD)</i>	00	00000000	0	
46	Vertical Border <i>(zero for internal LCD)</i>	00	00000000	0	
47	Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i>	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	

5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	30	00110000	48	0
74	Manufacture P/N	31	00110001	49	1
75	Manufacture P/N	45	01000101	69	E
76	Manufacture P/N	57	01010111	87	W
77	Manufacture P/N	30	00110000	48	0
78	Manufacture P/N	35	00110101	53	5
79	Manufacture P/N	20	00100000	32	
7A	Manufacture P/N	56	01010110	86	V
7B	Manufacture P/N	37	00110111	55	7
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	C2	10101010	170	

## 11.1 Precaution

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.
22. Please pay attention for below matters at mounting design of touch panel of LCD module.
  - I. Do not lift the module by FPC to avoid peeling.
  - II. Do not strike the panel surface.
  - III. Please use dry cloth or soft cloth with neutral detergent (after wring dry) at cleaning.  
Do not use any organic solvent, acid or alkali solution.