BOE

TITLE ：NE135FBM-N41 V8.1

Customer: acer

Product Specification

Rev. 0

BOE Optoelectronics Technology Co., Ltd

REVISION HISTORY

( )Preliminary Specification

(√)Final Specification

Revision No.	Page	Description of Changes	Date	Prepared
0	-	Release	2020.05.18	He Xinxi
1	31&34 &35	Correct Lable&2D drawing	2020.05.18	He Xinxi
2	36&37 &38	EDID table update	2020.05.18	He Xinxi

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Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

NE135FBM-N41 V8.1 is a color active matrix TFT LCD module using oxide TFT's (Thin Film Transistors) as an active switching devices. This module has a 13.5 inch diagonally measured active area with 2K resolutions (2256 horizontal by 1504 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M(8bit) colors and color gamut 100%(SRGB). The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model.

All input signals are eDP1.4 interface compatible.

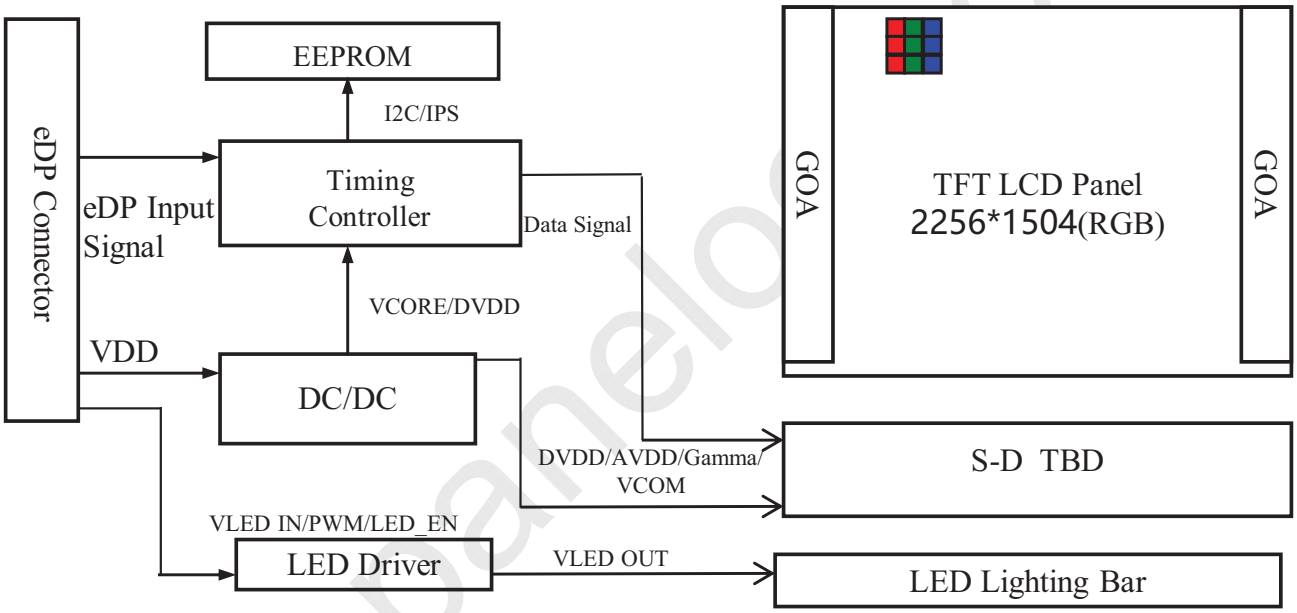


Figure 1. Drive Architecture

1.2 Features

- 4 lane eDP interface with 2.7 Gbps link rates
- Thin and light weight
- 16.7M(8bit) color depth
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Data enable signal mode
- Green product (RoHS & Halogen free product)
- On board LED driving circuit
- Low driving voltage and low power consumption
- On board EDID chip
- DPCD Version XX
- Function：PSR2

1.3 Application

- Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NE135FBM-N41 V8.1. (listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	284.933(H) ×189.955 (V)	mm	
Number of pixels	2256 (H) ×1504 (V)	pixels	
Pixel pitch	126.3(H) ×126.3(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	16.7M(8bit)		
Color gamut	sRGB 100%(TYP) 95% Min		Match比
Display mode	Normally black		
Dimensional outline	289.933±0.3 (H)*200.905±0.3(V) *2.0 (Max) (W/O PCB) 289.933±0.3(H)*212.28±0.5(V) *2.1(Max) (W/PCB)	mm	
Weight	200(max)	g	
Surface treatment	HC		
Surface hardness	2H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P_D : 0.6(Max)	W	@Mosaic
	P_{BL} : 2.9(Max)	W	
	P_{Total} : 3.5(Max)	W	@Mosaic

Notes : 1. LED Lighting Bar (54*LED Array)

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings>

Ta=25+/-2°C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V_{eDP}	0	2.0	V	
Logic Supply Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	+50	°C	Note 2
Storage Temperature	T_{ST}	-20	+60	°C	

Notes :
1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.
2. Temperature and relative humidity range are shown in the figure below.
90 % RH Max. (40 °C ≥ Ta) Maximum wet - bulb temperature at 39 °C or less. (Ta > 40 °C) No condensation.

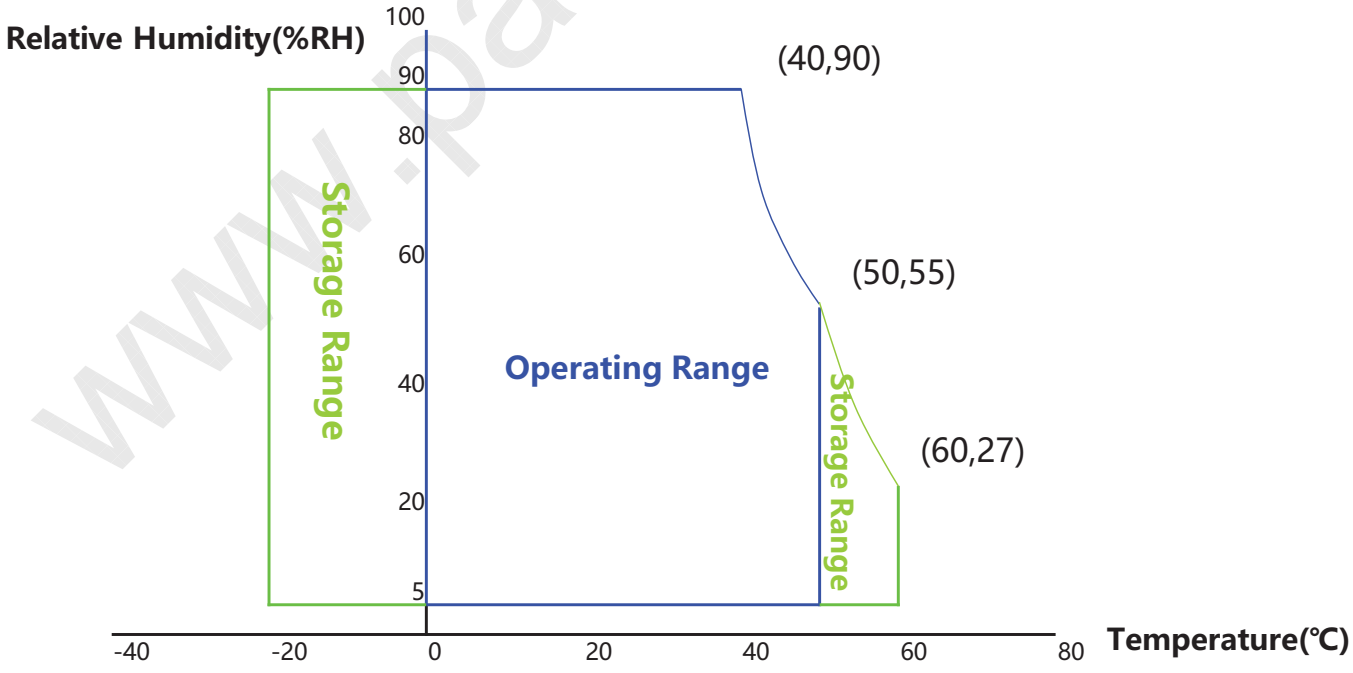


Figure 2. Temperature and Relative Humidity Range

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3. Electrical Specifications > Ta=25+/-2°C

Parameter			Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage		V_{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage		V_{RF}	-10% V_{DD}	-	+10% V_{DD}	V	@ V_{DD} = 3.3V
BIST Control Level		High Level	1.44	-	3.3	V	V_{DDIO}=1.8
		Low Level	0	-	0.27	V	
Power Supply Inrush Current		Inrush	-	-	2	A	Note3
Power Supply Current	Mosaic	I_{DD}	-	-	182	mA	Note 1
	R/G/B		-	-	202	mA	
Power Consumption	Mosaic	P_M	-	-	0.6	W	
	R/G/B	$P_{R/G/B}$	-	-	0.67	W	
	BLU	P_{BL}	-	-	2.9	W	Note 2
	Total	P_{Total}	-	-	3.5	W	@Mosaic

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

Notes :

1. The supply voltage is measured and specified at the interface connector of LCM.
   The current draw and power consumption specified is for 3.3V at 25 °C.
   a) Mosaic pattern 8*8
   b) R/G/B patterns

(a) (b)

Figure 3. Power Measure Patterns

2. Calculated value for reference ($V_{LED} \times I_{LED}$)
3. Measure condition (Figure 4)

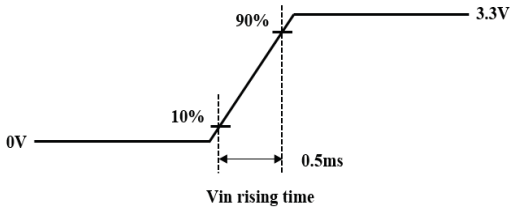


Figure 4. Inrush Measure Condition

3.2 Backlight Unit

< Table 4. LED Driving Guideline Specifications > Ta=25+/-2°C

Parameter			Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage		V_F	-	-	2.9	V	
LED Forward Current		I_F	-	15.8	-	mA	
LED Power Input Voltage		V_{LED}	5	12	21	V	
LED Power Input Current		I_{LED}	-	-	241	mA	Note 1
LED Power Consumption		P_{LED}	-	-	2.9	W	
Power Supply Voltage for LED Driver Inrush		Iled inrush	-	-	1.5	V	Note 3
LED Life-Time		N/A	15,000	-	-	Hour	I_F = 15.8mA Note 2
EN Control Level	Backlight On	V_{BL_EN}	1.2	-	5.0	V	
	Backlight Off		0	-	0.6	V	
PWM Control Level	High Level	V_{BL_PWM}	1.2	-	5.0	V	
	Low Level		0	-	0.6	V	
PWM Control Frequency		F_{PWM}	200	-	2K	Hz	
Duty Ratio			1	-	100	%	
PWM control resolution			0.4			%	@1Khz Note4

Notes :

1. Power supply voltage12V for LED driver.
   Calculator value for reference IF × VF ×54 /driver efficiency = PLED
2. The LED life-time define as the estimated time to 50% degradation of initial luminous.
3. Measure condition (Figure 5)
4. 0.4% PWM duty change can be detected when Fpwm is 1Khz.

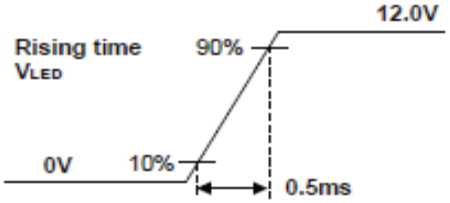


Figure 5. Inrush Measure Condition

3.3 LED Structure

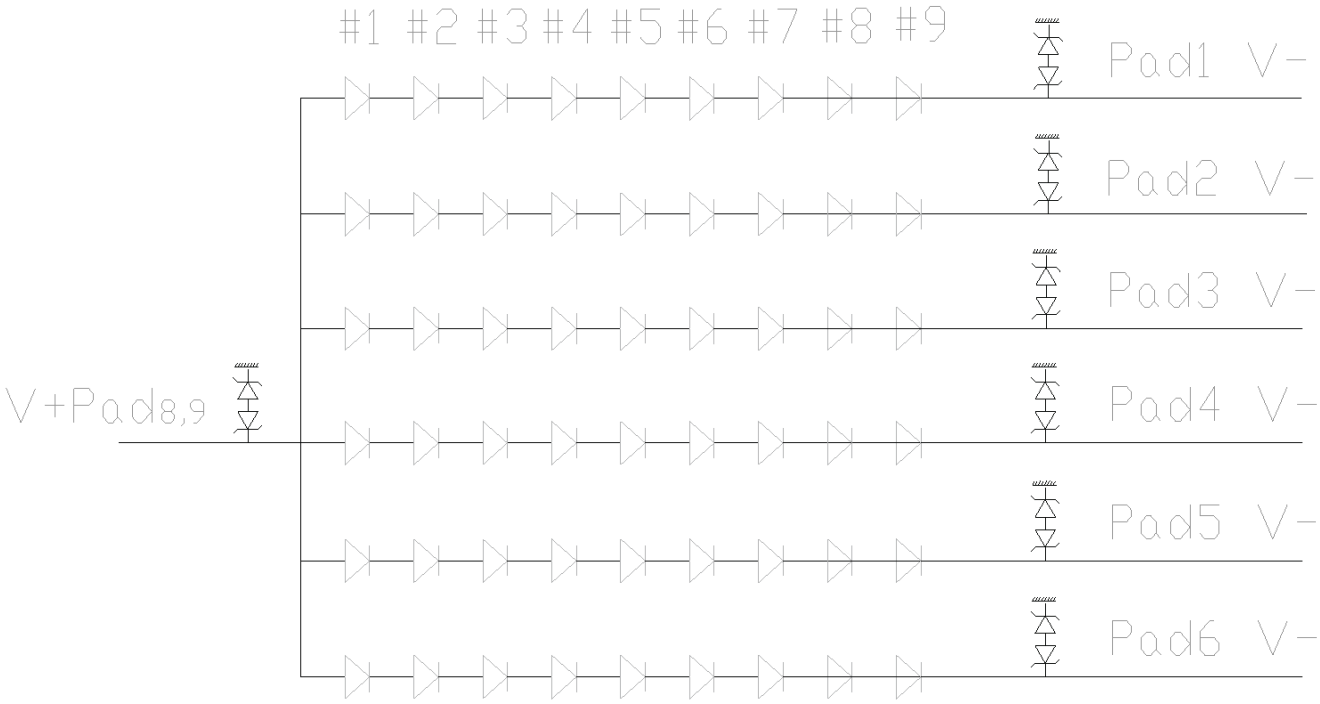


Figure 6. LED Structure

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2°C) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θØ=90 (= θ12) as the 12 o'clock direction ("upward"), θØ=180 (= θ9) as the 9 o'clock direction ("left") and θØ=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θand/or Ø, the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be 3.3+/- 0.3V at 25°C. Optimum viewing angle direction is 6 'clock.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note 1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Luminance Contrast Ratio		CR	Θ = 0°	1000	1500	-		Note 2
Luminance of White	5 Points	Y_w	Θ = 0° I_{LED} = 15.8mA	350	415	520	cd/m^2	Note 3
White Luminance Uniformity	5 Points	ΔY5		80	-	-	%	Note 4
	13 Points	ΔY13		62.5	-	-	%	
White Chromaticity		W_x	Θ = 0°	0.283	0.313	0.343		Note 5
		W_y		0.299	0.329	0.359		
Reproduction of Color	Red	R_x	Θ = 0°	Typ.-0.03	0.640	Typ.+0.03		
		R_y			0.330			
	Green	G_x			0.300			
		G_y			0.600			
	Blue	B_x			0.150			
		B_y			0.060			
Color Gamut				95	100	-	%	sRGB Matc h比
Response Time (Rising + Falling)		T_{RT}	Ta= 25°C Θ = 0°	-	30	35	ms	Note 6
Cross Talk		CT	Θ = 0°	-	-	2.0	%	Note 7

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).

2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.

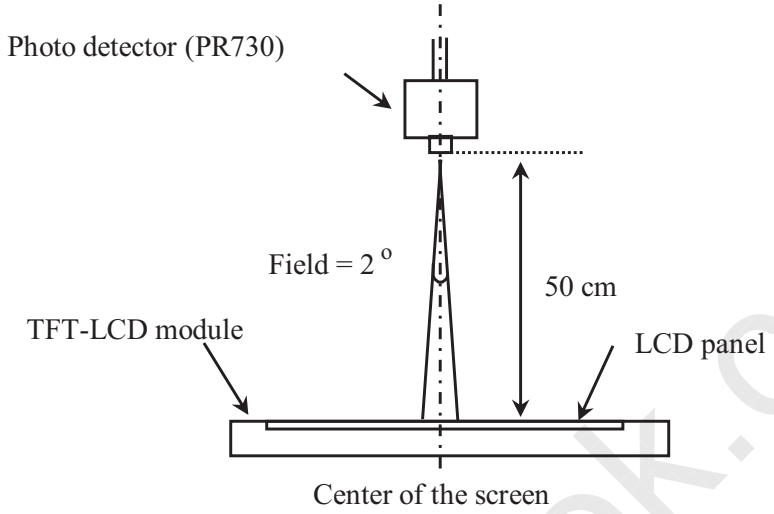
4. The White luminance uniformity on LCD surface is then expressed as : ΔY =Minimum Luminance of 5(or 13) points / Maximum Luminance of 5(or 13) points.(see Figure 8 and Figure 9).

5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The electro-optical response time measurements shall be made as Figure 10 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_f, and 90% to 10% is T_r.

7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark. (See Figure 11).

4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

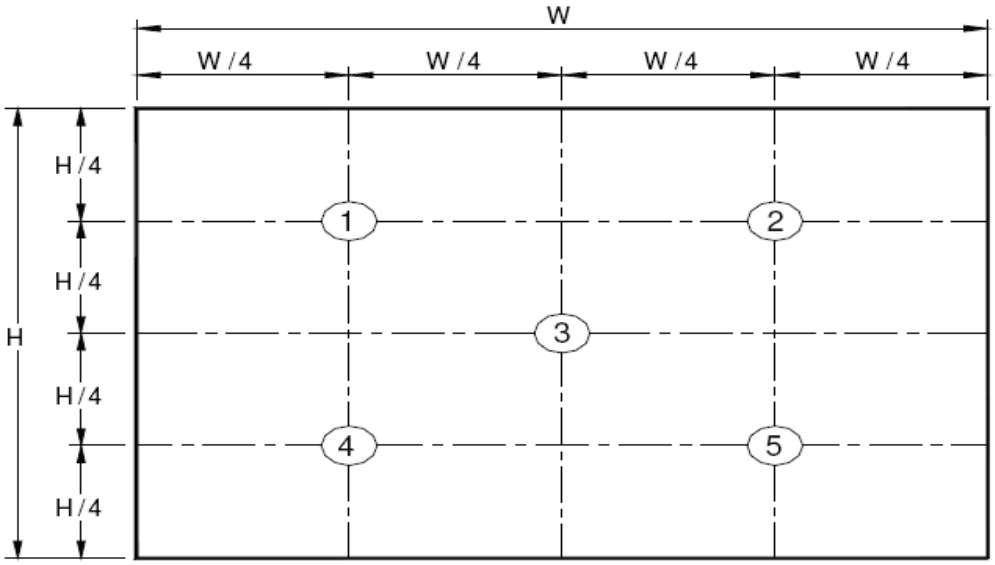


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

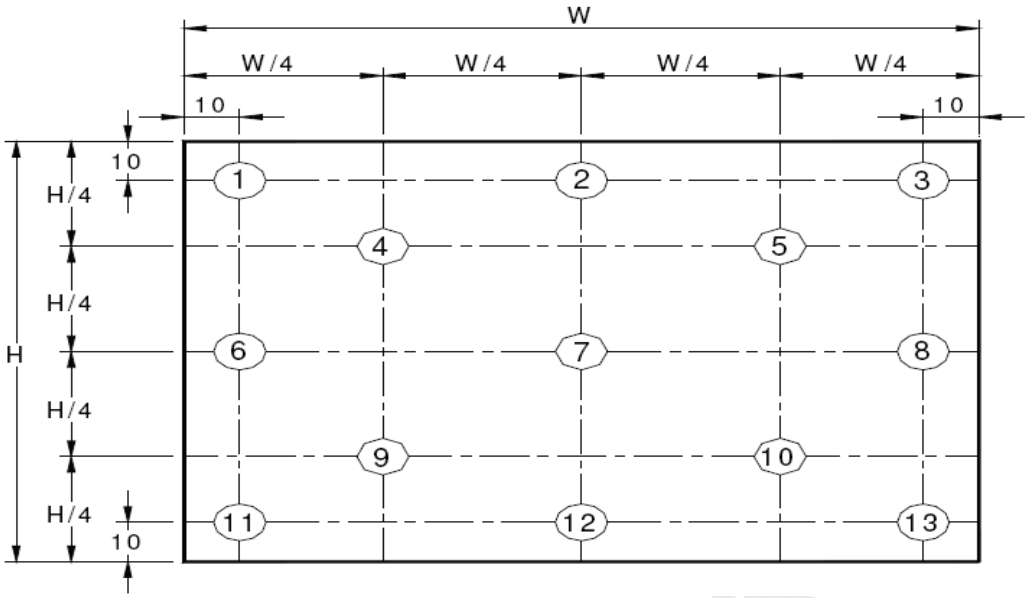


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as : ΔY5 = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8) , ΔY13 = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see Figure 9).

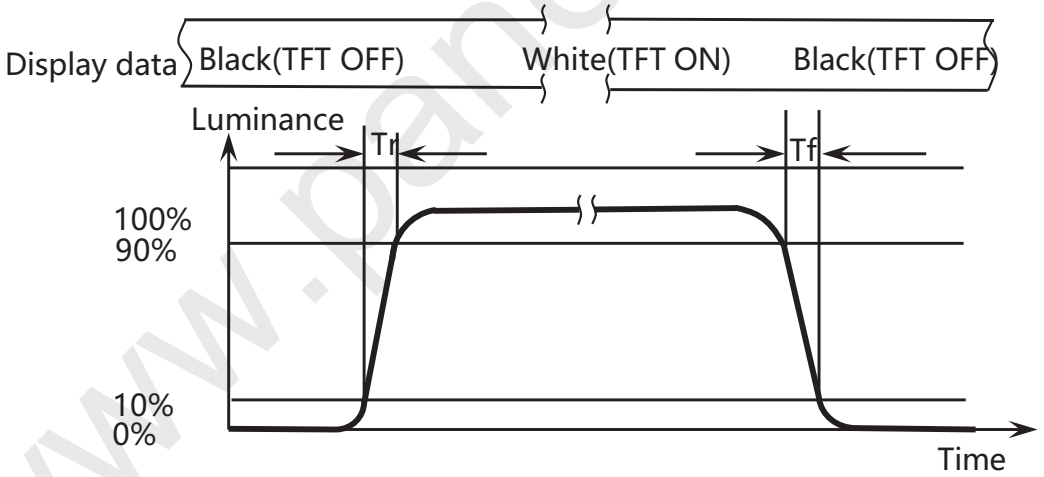
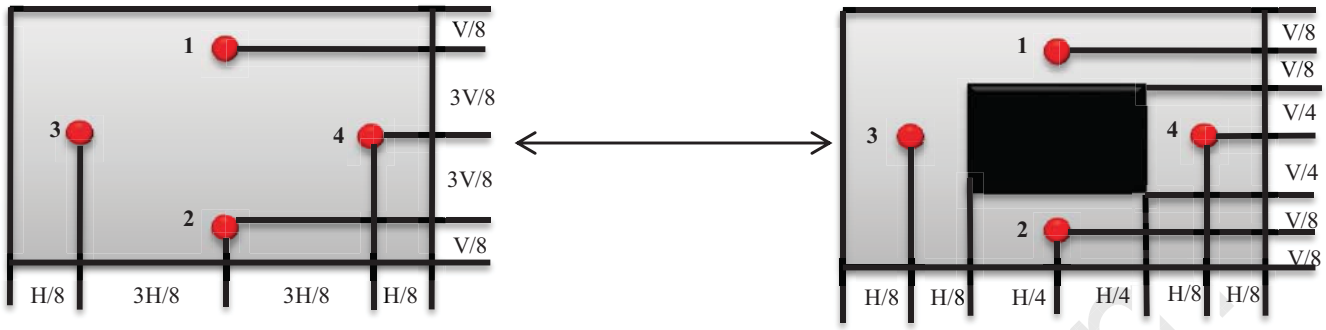


Figure 10. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the "data" input signal ON and OFF. Tr: The luminance to change from 10% to 90% ,Tf: The luminance to change from 90% to 10% .

The test system : LMS PR810



$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Figure 11. Cross Talk Modulation Test Description

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location 1/2/3/4 measured will be exactly the same in both patterns. The test background gray is from L64 to L192.Take the largest data as the result.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark.(Refer to Figure 11)

The test system: PR730

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is IPEX 20455-040E 0.5pitch.
The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	NC	No Connection	21	LCD_VCC	Power Supply, 3.3V (typ.)
2	H_GND	Ground	22	LCD Self Test	Panel Self Test Enable
3	Lane3_N	eDP RX Channel 3 Negative	23	LCD_GND	Ground
4	Lane3_P	eDP RX Channel 3 Positive	24	LCD_GND	Ground
5	H_GND	Ground	25	LCD_GND	Ground
6	Lane2_N	eDP RX Channel 2 Negative	26	LCD_GND	Ground
7	Lane2_P	eDP RX Channel 2 Positive	27	HPD	Hot Plug Detect Output
8	H_GND	Ground	28	BL_GND	LED Ground
9	Lane1_N	eDP RX Channel 1 Negative	29	BL_GND	LED Ground
10	Lane1_P	eDP RX Channel 1 Positive	30	BL_GND	LED Ground
11	H_GND	Ground	31	BL_GND	LED Ground
12	Lane0_N	eDP RX Channel 0 Negative	32	BL_Enable	LED Enable Pin(+3.3V Input)
13	Lane0_P	eDP RX Channel 0 Positive	33	BL_PWM_DIM	System PWM Signal Input
14	H_GND	Ground	34	NC	No Connection
15	AUX_CH_P	eDP AUX CH Positive	35	NC	No Connection
16	AUX_CH_N	eDP AUX CH Negative	36	BL_PWR	LED Power Supply 5V-21V
17	H_GND	Ground	37	BL_PWR	LED Power Supply 5V-21V
18	LCD_VCC	Power Supply, 3.3V (typ.)	38	BL_PWR	LED Power Supply 5V-21V
19	LCD_VCC	Power Supply, 3.3V (typ.)	39	BL_PWR	LED Power Supply 5V-21V
20	LCD_VCC	Power Supply, 3.3V (typ.)	40	NC	No Connection

5.2 eDP Interface

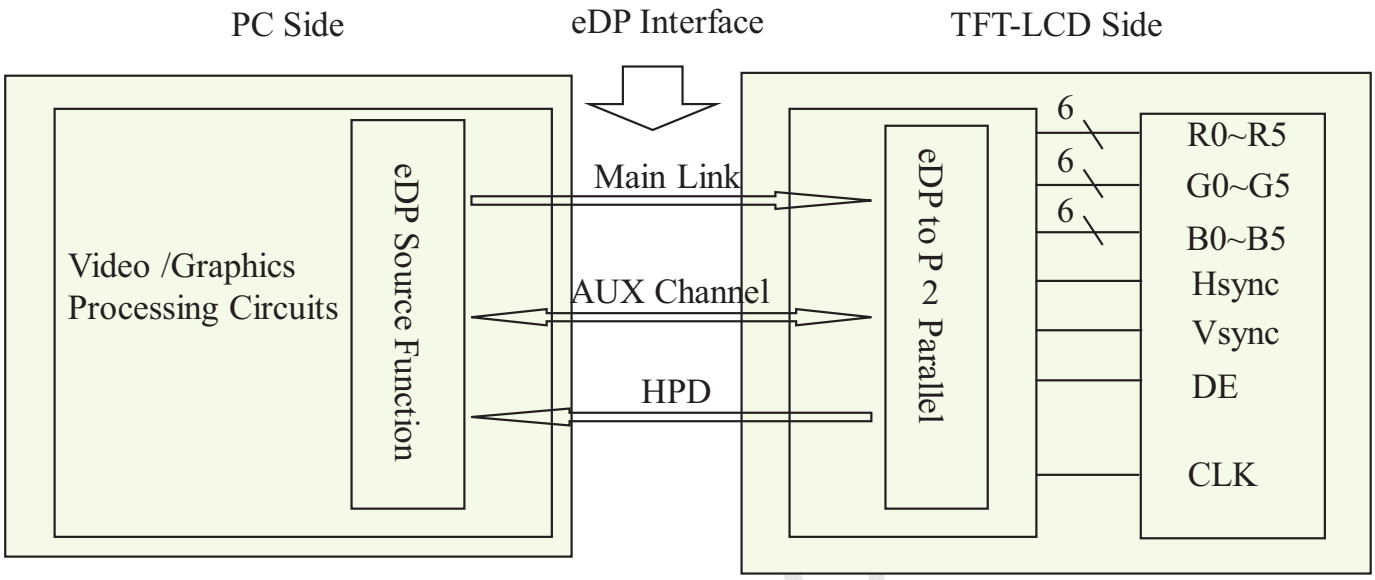
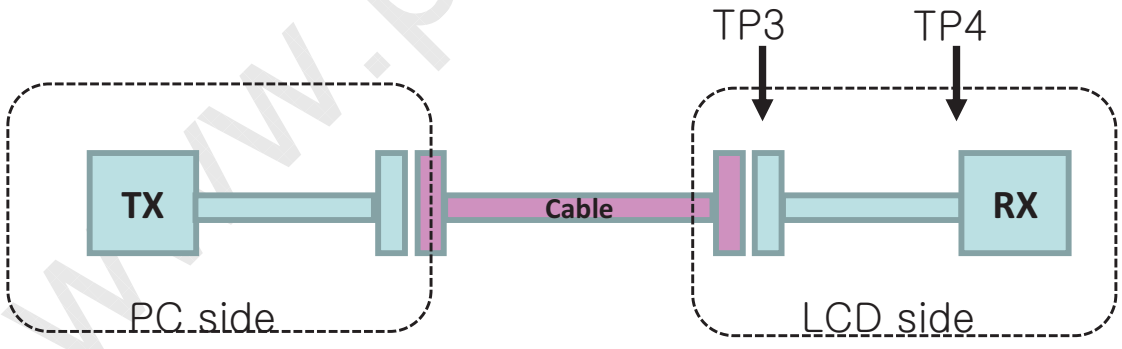


Figure 12. eDP Interface Architecture

Note:
Transmitter : Parade DP501 or equivalent.
Transmitter is not contained in module.

5.3 eDP Mainlink eye diagram test point



Mainlink eye diagram test point

Notes: Mainlink eye diagram at TP3 needs to be measured on the sink side(LCD Panel). The spec of sink eye vertices at TP3 should follow VESA DisplayPort™ Standard Version1. Revision 1a and Vesa Embedded DisplayPort Standard Version 1.2.

5.4 Data Input Format

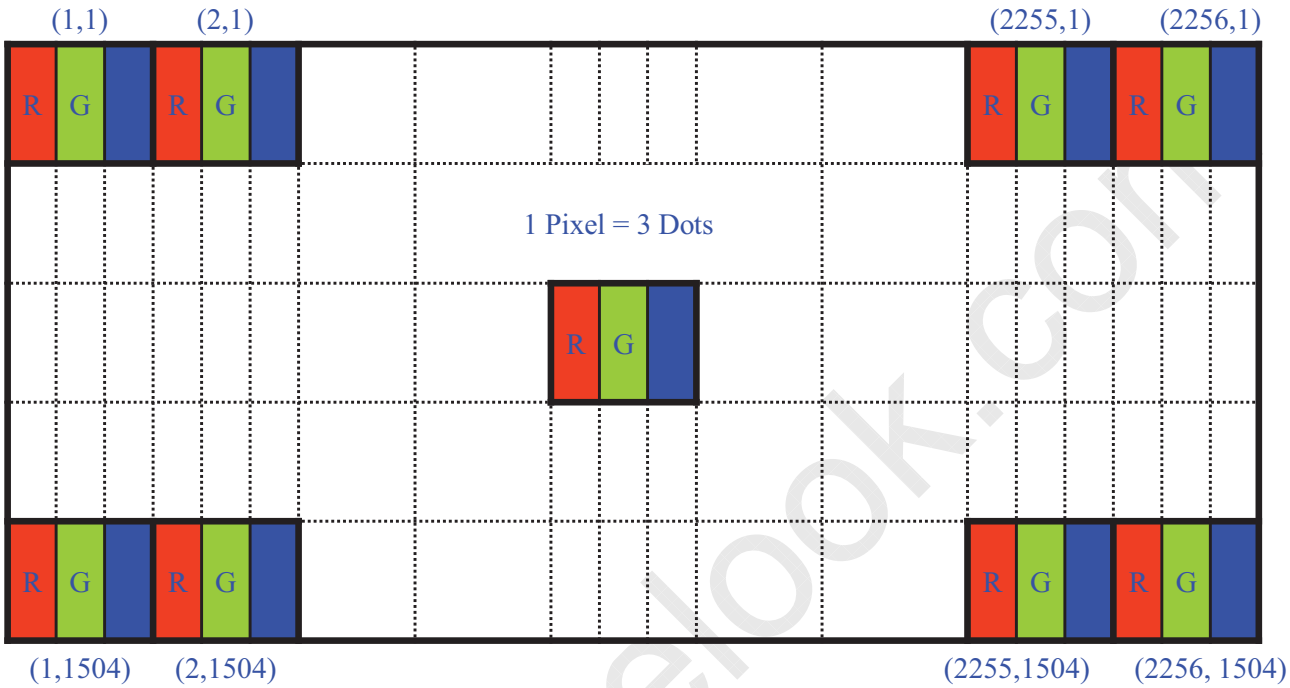


Figure 13. Display Position of Input Data (V-H)

5.5 Back-light & LCM Interface Connection

BLU Interface Connector: MSAK24037P9/PF040-B09B-C09/GF043-9S-E5000.

<Table 7. Pin Assignments for the BLU Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vout	LED anode connection	6	LED	LED cathode connection
2	Vout	LED anode connection	7	LED	LED cathode connection
3	NC	NC	8	LED	LED cathode connection
4	LED	LED cathode connection	9	LED	LED cathode connection
5	LED	LED cathode connection			

6.0 SIGNAL TIMING SPECIFICATION

6.1 The NE135FBM-N41 V8.1 Is Operated By The DE Only

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	228.6	235.7	242.8	MHz
Frame Period		Tv	1524	1552	1610	lines
			-	60	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	1504	-	lines
One line Scanning Period		Th	2479	2562	2594	clocks
Horizontal Display Period		Thd	-	2256	-	clocks

Note : The above is as optimized setting.

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	182.2	188.6	195.6	MHz
Frame Period		Tv	1524	1552	1610	lines
			-	48	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	1504	-	lines
One line Scanning Period		Th	2479	2562	2594	clocks
Horizontal Display Period		Thd	-	2256	-	clocks

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	ssc	-	-	0.5	%	
EYE width at package pins	V_{RX-EYE}	0.6			UI	
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	100	-	1320	mV	
Rx input DC common mode voltage	$V_{RX\_DC\_CM}$	0	-	2	V	
Differential termination resistance	$R_{RX-DIFF}$	80	-	120	Ω	
Single-ended termination resistance	R_{RX-SE}	40	-	60	Ω	
Rx short circuit current limit	I_{RX_SHORT}	-	-	20	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	$L_{RX\_SKEW\_INTRA\_PAIR}$	-	-	150	ps	
AC Coupling Capacitor	C_{SOURCE_ML}	75		200	nF	Source side

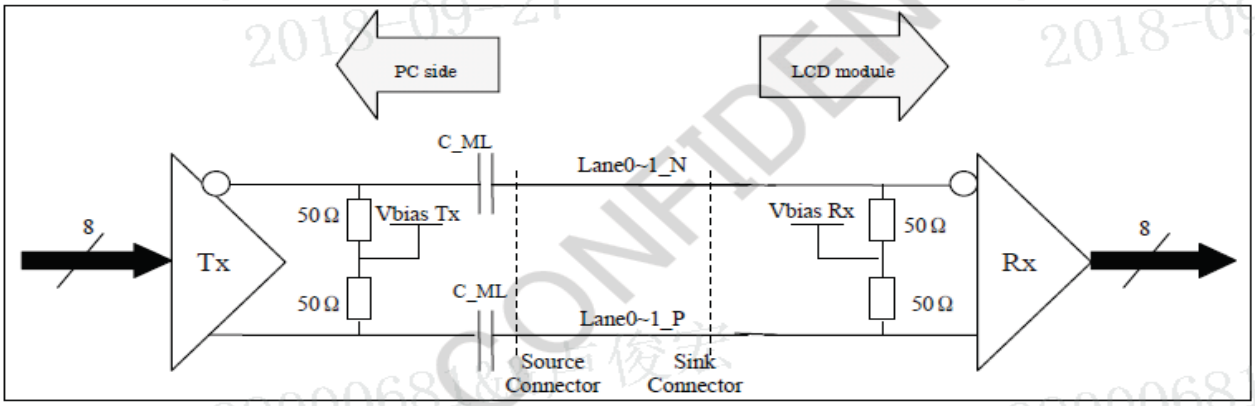


Figure 14. Main link differential pair

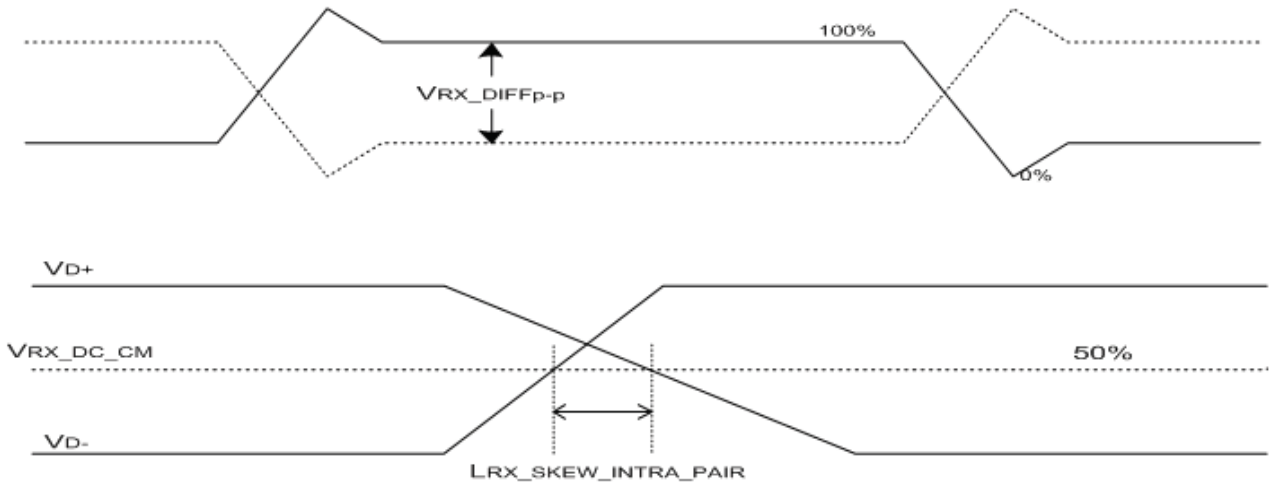


Figure 15. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

<Table 10. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	VHPD	2.25	-	3.6	V	
Hot Plug Detection Threshold	-	2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold	-	-	-	0.8V	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

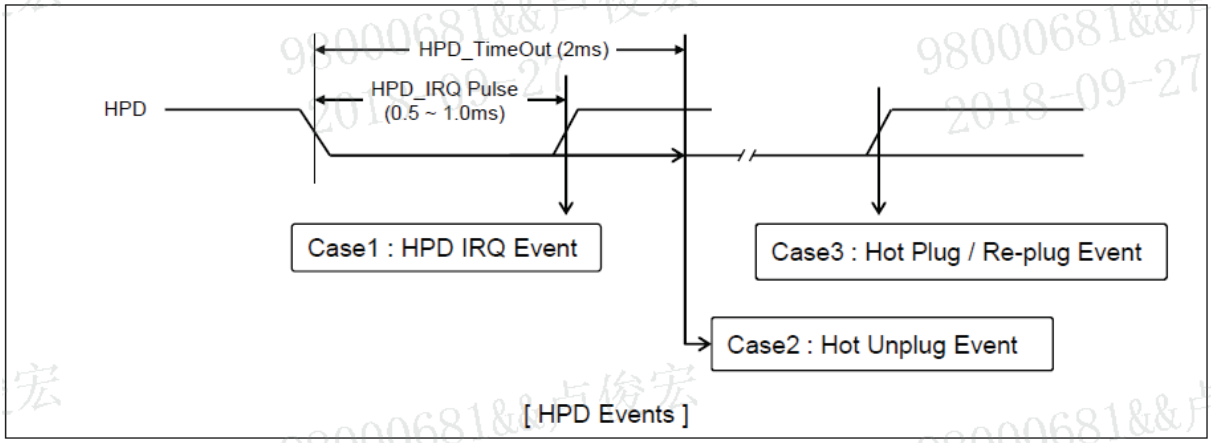


Figure 16. HPD Events

<Table 11. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	UIAUX	0.4	0.5	0.6	Us	
AUX peak-to-peak input differential voltage	VAUX-RX-DIFFp-p	0.29	-	1.38	V	
AUX CH termination DC resistance	RAUX-TERM	80	100	120	Ohm	
AUX DC common mode voltage	VAUX-DC-CM	0	-	2	V	
AUX turn around common mode voltage	VAUX-TURN-CM	-	-	0.3	V	
AUX short circuit current limit	IAUX-SHORT	-	-	90	mA	
AUX AC Coupling Capacitor	CSOURCE-AUX	75	-	200	nf	Source side

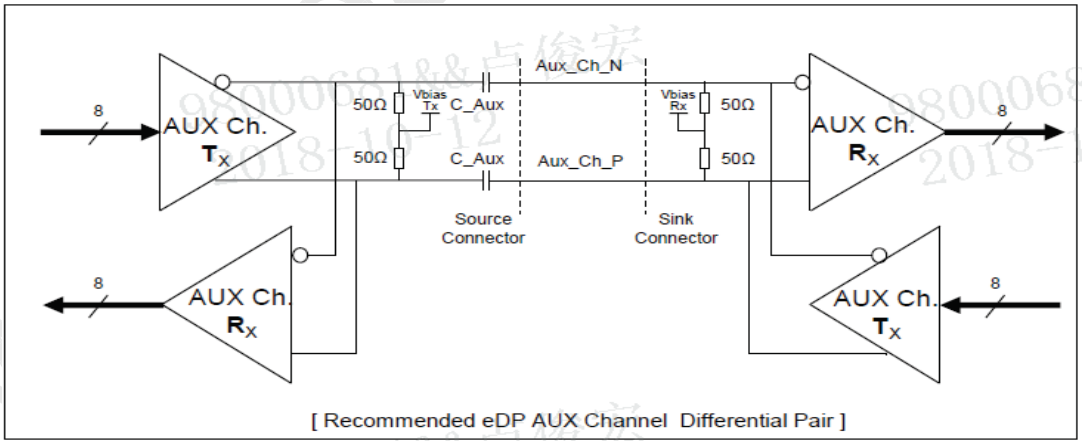


Figure 17. AUX differential pair

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 12. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal																			
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Light Blue	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Purple	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵					↑								↑								↑			
	▿					↓								↓								↓			
	Brighter	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▿	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵					↑								↑								↑			
	▿					↓								↓								↓			
	Brighter	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	▿	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	▵					↑								↑								↑			
	▿					↓								↓								↓			
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
	▿	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray scale of White& Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	▵					↑								↑								↑			
	▿					↓								↓								↓			
	Brighter	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1
	▿	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

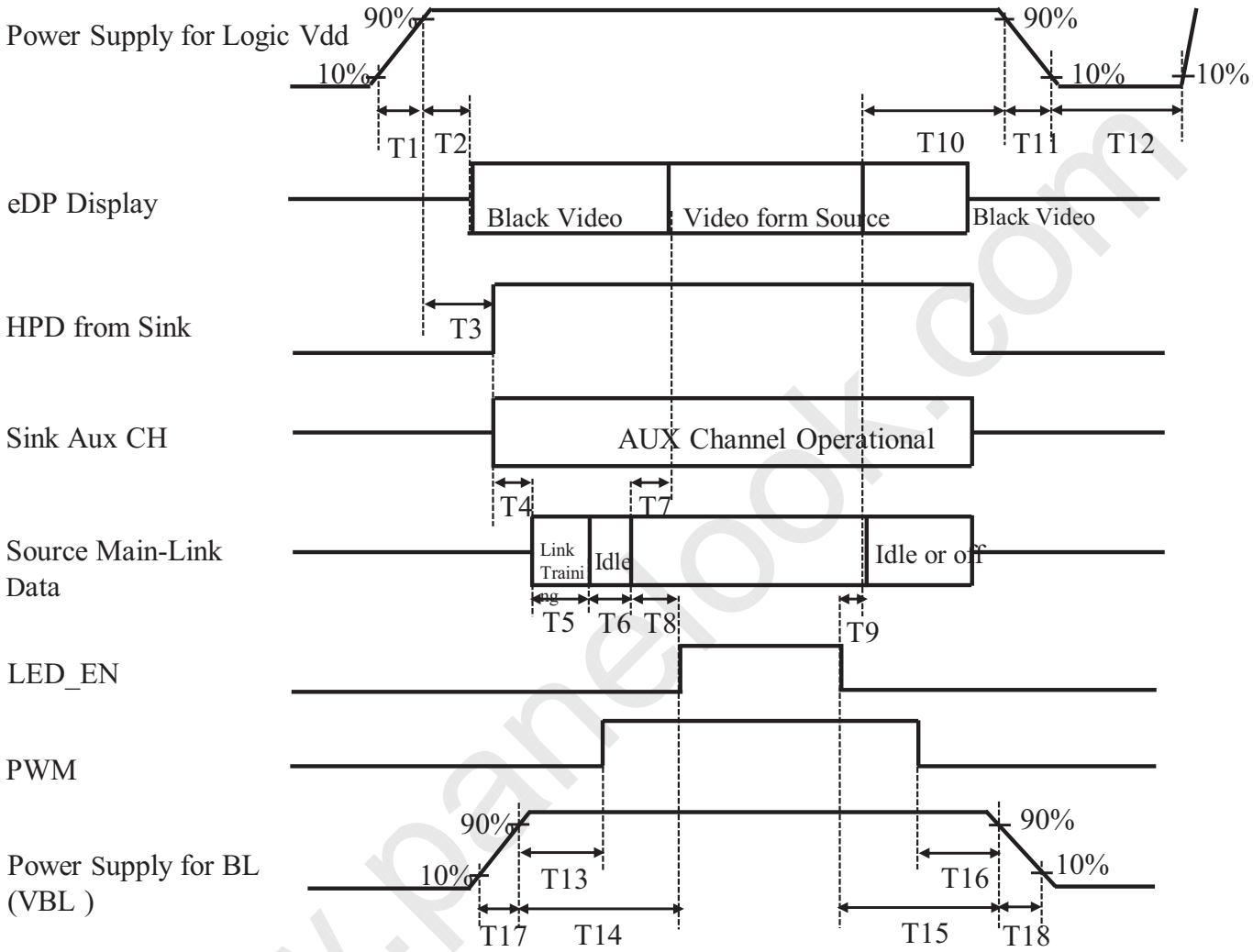


Figure 18. Power Sequence

- 0.5ms ≤ T1 ≤ 10 ms
- 0ms < T2 ≤ 200 ms
- 0ms < T3 ≤ 200 ms
- T3+T4+T5+T6+T8>200ms
- 0ms < T7 ≤ 50ms
- 50ms < T8
- 0ms < T9
- 0ms < T10 < 500 ms
- 0.5ms ≤ T11 ≤ 10 ms
- 500ms ≤ T12
- 0ms < T13
- 0ms < T14
- 0ms < T15
- 0ms < T16
- 0.5ms ≤ T17
- 0.5ms ≤ T18

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

9.0 Connector Description

Physical interface is described as for the connector on LCM.
These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

< Table 13. Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	IPEX
Type/ Part Number	20455-040E
Mating Housing/ Part Number	20454-30T

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 23shows mechanical outlines for the model NE135FBM-N41 V8.1.
Other parameters are shown in Table 14.

<Table 14. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	284.933 (H) ×189.955 (V)	mm
Number of pixels	2256 (H) X 1504 (V) (1 pixel = R + G + B dots)	pixels
Pixel pitch	126.3 (H) X 126.3 (V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	16.7M(8bit)	
Display mode	Normally black	
Dimensional outline	289.933±0.3 (H)*200.905±0.3(V) *2.0 (Max) (W/O PCB) 289.933±0.3(H)*212.28±0.5(V) *2.1(Max) (W/PCB)	mm
Weight	200 (max)	g

10.2 Mounting

See Figure 23.

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an hard coating Surface treatment with 2H hardness to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.

<Table 15. Reliability Test>

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 60°C , 60%RH, 240 hrs	
2	Low temperature storage test	Ta = -20°C , 240 hrs	
3	High temperature & high humidity operation test	Ta = 50°C , 80%RH, 240 hrs	
4	High temperature operation test	Ta = 50°C , 60%RH, 240 hrs	
5	Low temperature operation test	Ta = 0°C , 240 hrs	
6	Thermal shock	Ta = -20 °C ↔ 60 °C (0.5 hr), 60%±3%RH, 100 cycle	
7	Vibration test (non-operating)	Ta = 25°C , 60%RH, 1.5G, 10~500Hz, Sine X,Y,Z / Sweep rate : 1 hour	Note 1
8	Shock test (non-operating)	Ta = 25°C , 60%RH, 220G, Half Sine Wave 2msec ±X, ±Y, ±Z Once for each direction	Note 1
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ±15 KV Contact : 150 pF, 330Ω, ±8 KV Ta = 25°C , 60%RH,	Note 2

Notes :

1. The fixture must be hard enough , so that the module would not be twisted or bent.
2. Self- recovery and restart recovery is allowed. No hardware failures.

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 LABEL

(1) Product Label

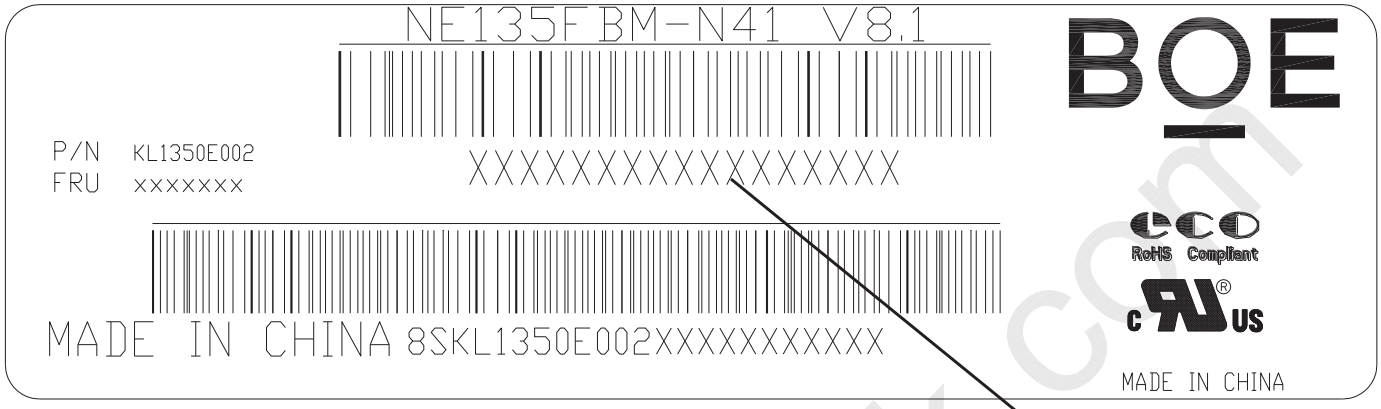


Figure 19. Product Label

Module ID Naming Rule:

<Table 16. Module ID Naming Rule>

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	B	9	A	F	1	7	8	8	D	3	1	0	0	0	0	6	8
Description	Product Name		Product Grade	B8	Year		Month	Model Extension Code (Last 4 Digits of FG CODE)				Serial No. 00001-ZZZZZZ					

(2) High voltage caution label

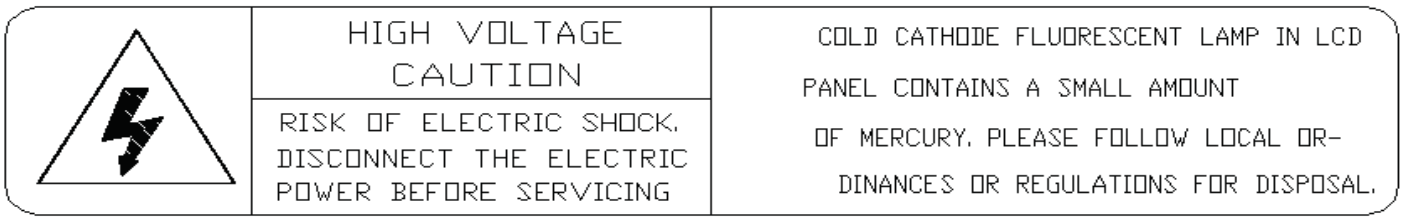


Figure 20. High Voltage Caution Label

(3) Box label

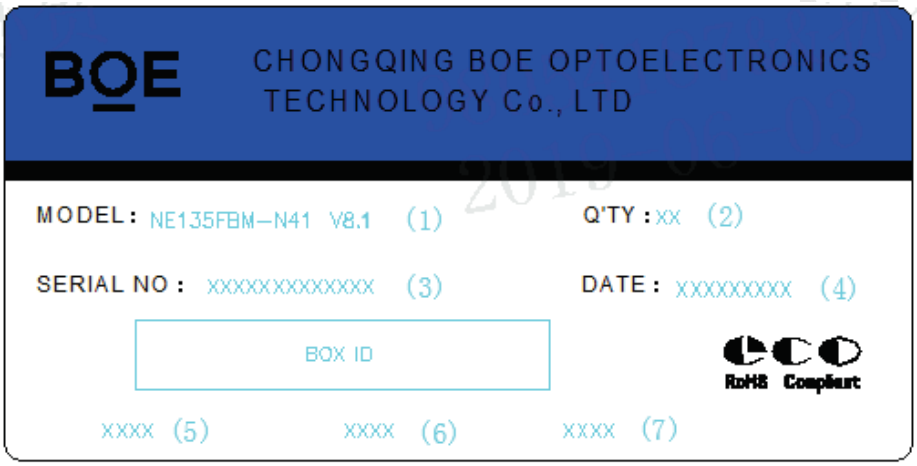


Figure 21. Box Label

Serial number marked part needs to print, show as follows:

1. FG-CODE(Before 12 bit)
2. Product quantity
3. Box ID
4. Date
5. The client section material number(The client)
6. FG-Code After four
7. The supplier code

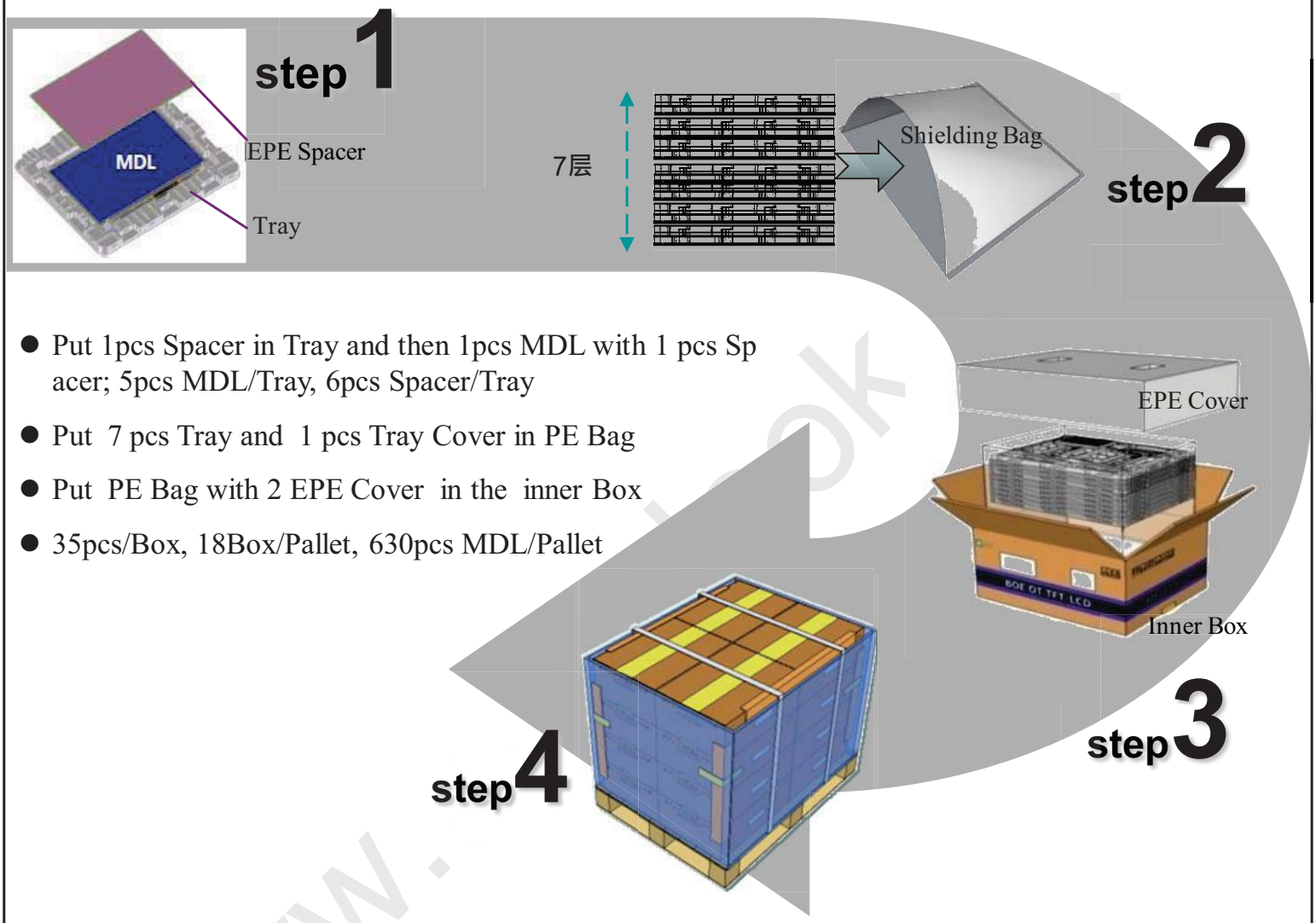
Total Size:100×50mm

<Table 17. Box Label Naming Rule >

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	B	9	A	F	1	7	8	N	0	0	3	2	7
Description	Product Name		Product Grade	B8	Year		Month	Revision	BOX Serial Number				

14.0 PACKING INFORMATION

14.1 Packing Order



- Put 1pcs Spacer in Tray and then 1pcs MDL with 1 pcs Spacer; 5pcs MDL/Tray, 6pcs Spacer/Tray
- Put 7 pcs Tray and 1 pcs Tray Cover in PE Bag
- Put PE Bag with 2 EPE Cover in the inner Box
- 35pcs/Box, 18Box/Pallet, 630pcs MDL/Pallet

Figure 22. Packing Order

14.2 Note

- Box dimension: 480mm*350mm*285mm
- Package quantity in one box: 35pcs
- Total weight: 9.2kg

15.0 MECHANICAL OUTLINE DIMENSION

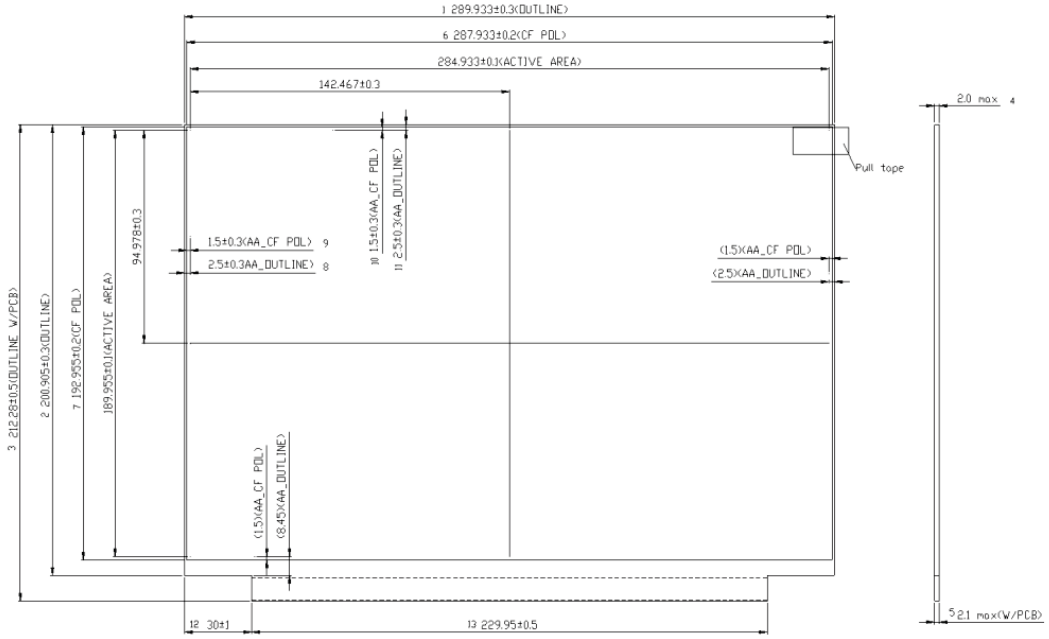


Figure 23. TFT-LCD Module Outline Dimension (Front View)

Note:

1. Top Polarizer is the highest part.
2. Curve Spec: 0<=d<=0.5mm.
3. No light leakage from all 4 corners of LCM.
4. Size Unit: mm.
5. General Tolerance: ±0.3mm.
6. The eDP connector is measured at pin 1 and mating line
7. Critical dimension:①- ⑯ CPK: ①-⑤
8. Measurement method refer to Appendix A
9. System matching refer to Appendix B
10. "()"marks the reference dimensions.
11. PCBA cover tape will bulge without external force due to the material character of the tape. The tolerance of PCBA cover tape thickness will not exceed 2 mm from surface of polarizer and thickness of PCBA side can be reformed to normal thickness by external force.
12. If system interfere with panel or twist panel while system operation, it may cause ripple or acoustic noise or other side effect. Please prevent such twist or interfere by system operation.
13. The system materials should contain no or less NH4+ ions.

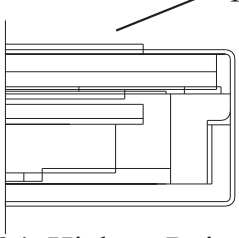


Figure 24. Highest Point Position

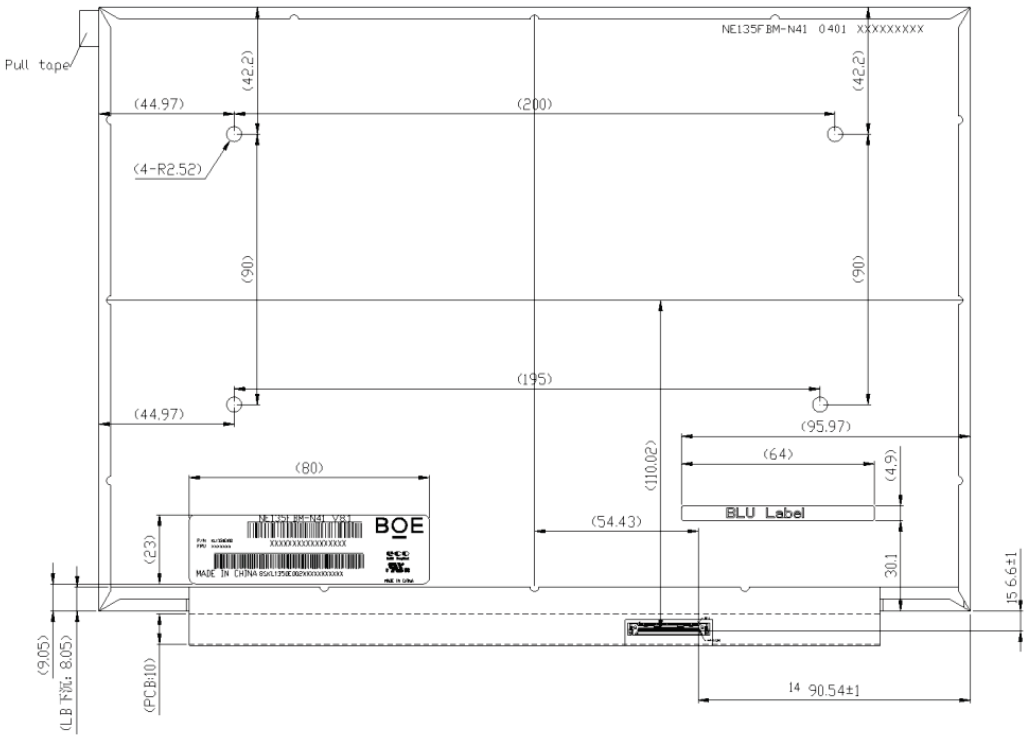


Figure 25. TFT-LCD Module Outline Dimensions (Rear view)

Note:

1. Top Polarizer is the highest part.
2. Curve Spec: 0<=d<=0.5mm.
3. No light leakage from all 4 corners of LCM.
4. Size Unit: mm.
5. General Tolerance: ±0.3mm.
6. The eDP connector is measured at pin 1 and mating line
7. Critical dimension:①- ⑯ CPK: ①-⑤
8. Measurement method refer to Appendix A
9. System matching refer to Appendix B
10. "()"marks the reference dimensions.
11. PCBA cover tape will bulge without external force due to the material character of the tape. The tolerance of PCBA cover tape thickness will not exceed 2 mm from surface of polarizer an d thickness of PCBA side can be reformed to normal thickness by external force.
12. If system interfere with panel or twist panel while system operation, it may cause ripple or acoustic noise or other side effect. Please prevent such twist or interfere by system operation.
13. The system materials should contain no or less NH4+ ions.

16.0 EDID Table

Check FAE	Check QE	Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
-	-	00	Header	00	0		0	EDID Header
-	-	01		FF	255		255	
-	-	02		FF	255		255	
-	-	03		FF	255		255	
-	-	04		FF	255		255	
-	-	05		FF	255		255	
-	-	06		FF	255		255	
-	-	07		00	0		0	
V		08	ID Manufacturer Name	09	9		BOE	ID = BOE
V		09		E5	229			
	V	0A	ID Product Code	5F	95		2399	ID = 2399
	V	0B		09	9			
V		0C	32-bit serial No.	00	0		0	
V		0D		00	0		0	
V		0E		00	0		0	
V		0F		00	0		0	
V		10	Week of manufacture	17	23		23	
V		11	Year of Manufacture	1D	29		2019	Manufactured in 2019
V		12	EDID Structure Ver.	01	1		1	EDID Ver 1.0
V		13	EDID revision #	04	4		4	EDID Rev. 0.4
V	V	14	Video input definition	A5	165		-	Refer to right table
	V	15	Max H image size	1C	28		28	28.4933 cm (Approx)
	V	16	Max V image size	13	19		19	18.9955 cm (Approx)
	V	17	Display Gamma	78	120		2.2	Gamma curve = 2.2
V		18	Feature support	03	3		-	Refer to right table
	V	19	Red/Green low bits	DE	222		-	Red / Green Low Bits
	V	1A	Blue/White low bits	50	80		-	Blue / White Low Bits
	V	1B	Red x high bits	A3	163	655	0.640	Red (x) = 10100011 (0.64)
	V	1C	Red y high bits	54	84	337	0.330	Red (y) = 01010100 (0.33)
	V	1D	Green x high bits	4C	76	307	0.300	Green (x) = 01001100 (0.3)
	V	1E	Green y high bits	99	153	614	0.600	Green (y) = 10011001 (0.6)
	V	1F	Blue x high bits	26	38	153	0.150	Blue (x) = 00100110 (0.15)
	V	20	BLue y high bits	0F	15	61	0.060	Blue (y) = 00001111 (0.06)
	V	21	White x high bits	50	80	320	0.313	White (x) = 01010000 (0.313)
	V	22	White y high bits	54	84	336	0.329	White (y) = 01010100 (0.329)
V		23	Established timing 1	00	0		-	Refer to right table
V		24	Established timing 2	00	0		-	
V		25	Established timing 3	00	0		-	
V		26	Standard timing #1	01	1			Not Used
V		27		01	1			
V		28	Standard timing #2	01	1			Not Used
V		29		01	1			
V		2A	Standard timing #3	01	1			Not Used
V		2B		01	1			
V		2C	Standard timing #4	01	1			Not Used
V		2D		01	1			

V		2E	Standard timing #5	01	1			Not Used
V		2F		01	1			
V		30	Standard timing #6	01	1			Not Used
V		31		01	1			
V		32	Standard timing #7	01	1			Not Used
V		33		01	1			
V		34	Standard timing #8	01	1			Not Used
V		35		01	1			
	V	36	Detailed timing/monitor descriptor #1	11	17		235.7	235.69584MHz Main clock
	V	37		5C	92			
	V	38		D0	208		2256	Hor Active = 2256
	V	39		18	24		280	Hor Blanking = 280
	V	3A		81	129		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
	V	3B		E0	224		1504	Ver Active = 1504
	V	3C		2D	45		45	Ver Blanking = 45
	V	3D		50	80		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
	V	3E		30	48		48	Hor Sync Offset = 48
	V	3F		20	32		32	H Sync Pulse Width = 32
	V	40		36	54		3	V sync Offset = 3 line
	V	41		00	0		6	V Sync Pulse width : 6 line
	V	42		1D	29		285	Horizontal Image Size = 284.933 mm (Low 8 bits)
	V	43		BE	190		190	Vertical Image Size = 189.955 mm (Low 8 bits)
	V	44		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
	V	45		00	0		0	Hor Border (pixels)
	V	46		00	0		0	Vertical Border (Lines)
	V	47		1A	26		-	Refer to right table
V		48	Detailed timing/monitor descriptor #2	A7	167		188.6	188.556672MHz Main clock
V		49		49	73			
V		4A		D0	208		2256	Hor Active = 2256
V		4B		18	24		280	Hor Blanking = 280
V		4C		81	129		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
V		4D		E0	224		1504	Ver Active = 1504
V		4E		2D	45		45	Ver Blanking = 45
V		4F		50	80		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
V		50		30	48		48	Hor Sync Offset = 48
V		51		20	32		32	H Sync Pulse Width = 32
V		52		36	54		3	V sync Offset = 3 line
V		53		00	0		6	V Sync Pulse width : 6 line
V		54		1D	29		285	Horizontal Image Size = 285 mm (Low 8 bits)
V		55		BE	190		190	Vertical Image Size = 190 mm (Low 8 bits)
V		56		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
V		57		00	0		0	Hor Border (pixels)
V		58		00	0		0	Vertical Border (Lines)
V		59		1A	26		-	Refer to right above table

V		5A	Detailed timing/monitor descriptor #3	00	0			Indicates descriptor #3 is a display Descriptor
V		5B		00	0			
V		5C		00	0			Reserved
V		5D		FE	254			Tag：ASCII String
V		5E		00	0			Reserved
V		5F		42	66		B	Manufacture name：BOECQ
V		60		4F	79		O	
V		61		45	69		E	
V		62		20	32			
V		63		43	67		C	
V		64		51	81		Q	
V		65		0A	10			
V		66		20	32			
V		67		20	32			
V		68		20	32			
V		69		20	32			
V		6A		20	32			
V		6B		20	32			
V		6C	Detailed timing/monitor descriptor #4	00	0			Indicates descriptor #4 is a display Descriptor
V		6D		00	0			
V		6E		00	0			Reserved
V		6F		FE	254			Tag：ASCII String
V		70		00	0			Reserved
V		71		4E	78		N	Model name：NE135FBM-N41
V		72		45	69		E	
V		73		31	49		1	
V		74		33	51		3	
V		75		35	53		5	
V		76		46	70		F	
V		77		42	66		B	
V		78		4D	77		M	
V		79		2D	45		-	
V		7A		4E	78		N	
V		7B		34	52		4	
V		7C		31	49		1	
V		7D		0A	10			
V	V	7E	Extension flag	00	0		1	
-	-	7F	Checksum	FB	251	251	-	

Appendix A

The Measurement Methods for the Dimensions of Module

Caliper:
a. Length of Outline
b. Width of Outline (Without/With PCB)
c. Thickness of Outline (Without/ With PCB)

Coordinate Measuring Machine:
CF Polarizer Size
Active Area Size
Active Area to Outline (Without Tape Wrinkle or Bulged)
Active Area to CF Polarizer
The Distance of Bracket Holes
P-Cover to Outline (Without Tape Wrinkle or Bulged)
Length of P-Cover
Connector Pin 1 to Outline (Without Tape Wrinkle or Bulged)

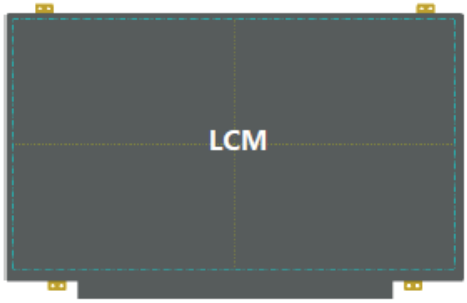
Height Gauge: The Different Height of Root and Top on the Bracket
(Need to Calculate From Bracket Angle Spec.)

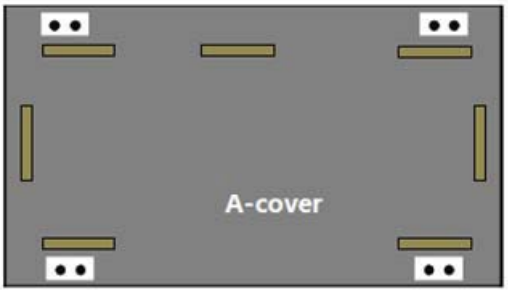
Feeler Gauge: The Warpage Spec. of Module

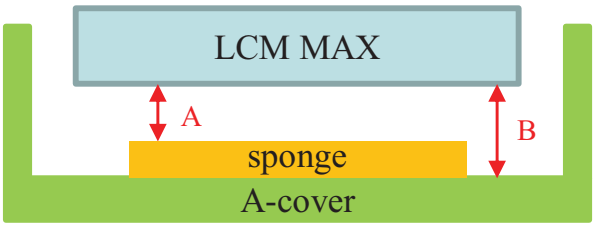
Notes:
Except the Critical Dimensions as Above, Other Dimensions are Measured by Coordinate Measuring Machine If Necessary.

Appendix B

LCM to A-Cover / sponges z-gap







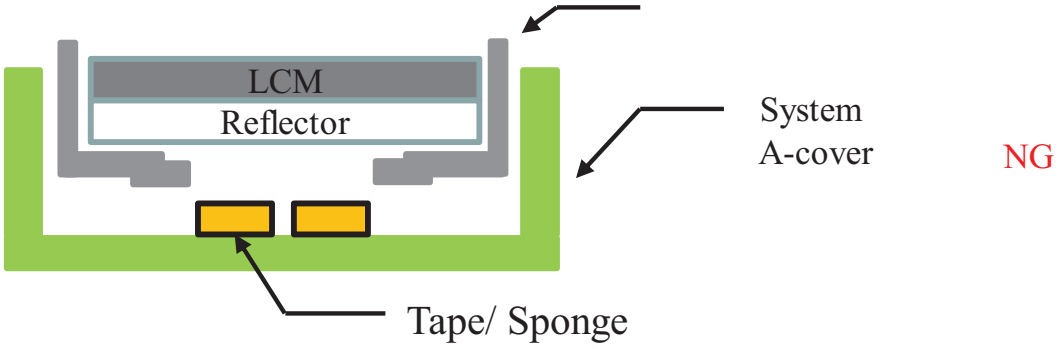
	Plastic Cover (LCM Thickness: Max)	Metal Cover (LCM Thickness: Max)
A	>0mm	>0mm
B	Min: 1.0mm	Min: 0.8mm
Without the open area of back cover		

Purpose	The reflector area is very sensitive, we suggest that design enough z-gap to decrease the risk of water ripple, white spot and other abnormal display

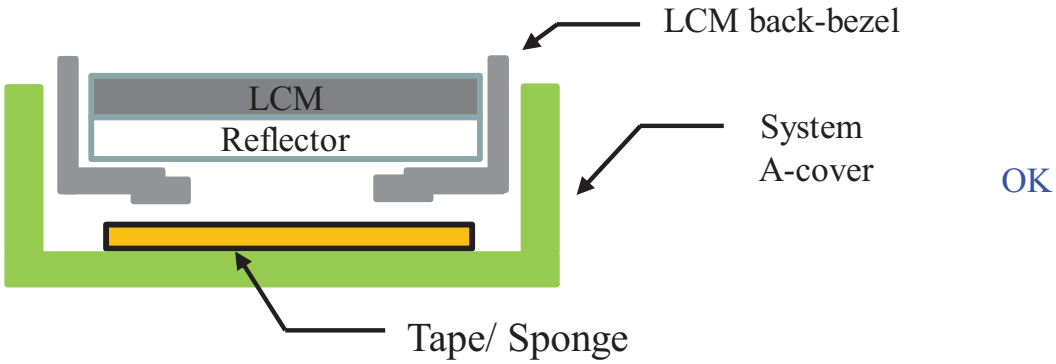
Appendix B

LCM to A-Cover / sponges z-gap

a



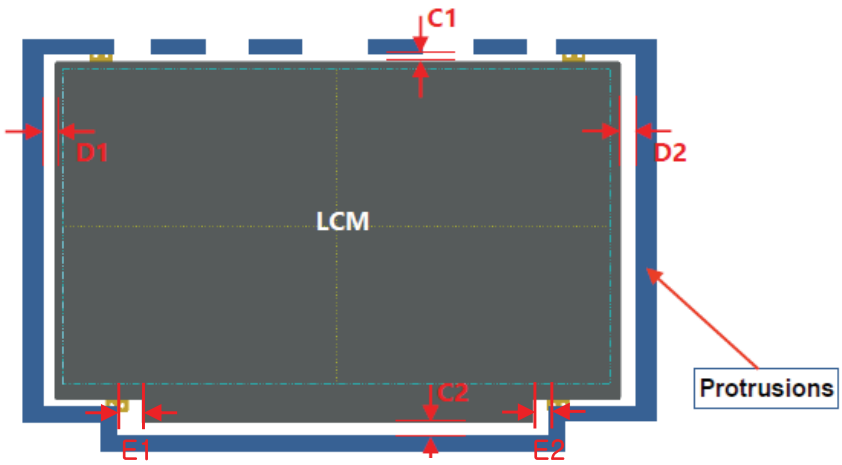
b



Purpose	If attach sponges or rubbers which correspond to white reflector area, it may cause white spot, pooling or other relate issues. We suggest that attach wide range sponges / rubbers which can cover the LCM back-bezel opening

Appendix B

LCM to side wall / protrusions



	Normal border	Narrow border
D1/D2	Min: 0.45mm	Min: 0.35mm
C1	Min: 0.50mm	
C2	Min: 0.50mm	
E1/E2	Min: 0.55mm	

Purpose	We suggest that design enough gap around LCM to prevent shock test failure, or interference, cell crack, abnormal display...etc. in the reliability test

Appendix B

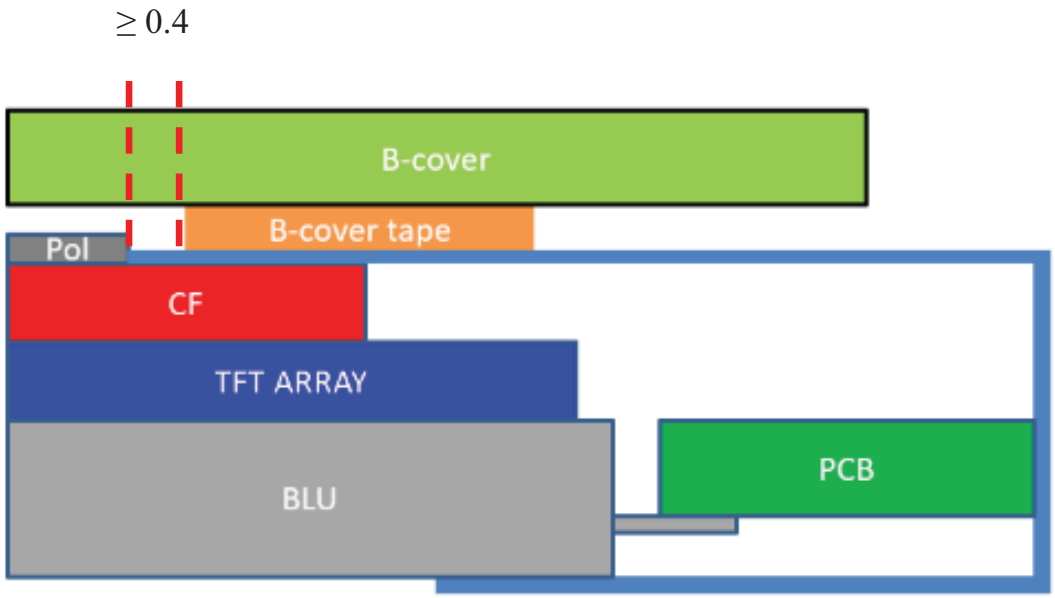
LCM to B-cover z-gap

B-cover Tape	Gap
Without	0.15 ~ 0.25mm
With	0.15 ~ 0.20mm

Purpose	Too less z-gap between system B-cover and LCM top pol has high risk to cause cell crack, pooling, light leakage and other issues

Appendix B

B-cover tape to top pol edge

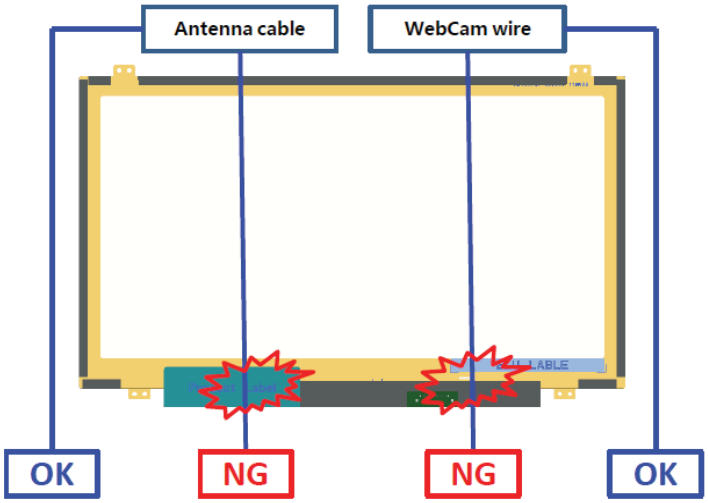


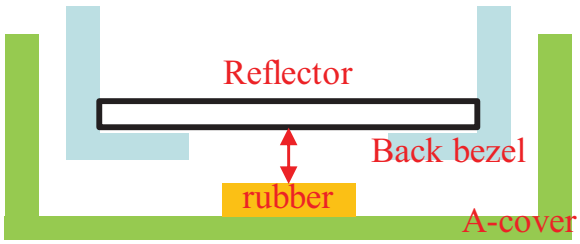
If attach b-cover and LCM with tapes,
Please let tapes to be located out of top pol edges 0.4mm away on 4 sides

Purpose	To avoid the B-cover tape override top pol and cause pooling or light leakage issue

Appendix B

Antenna Cable & Webcam wire



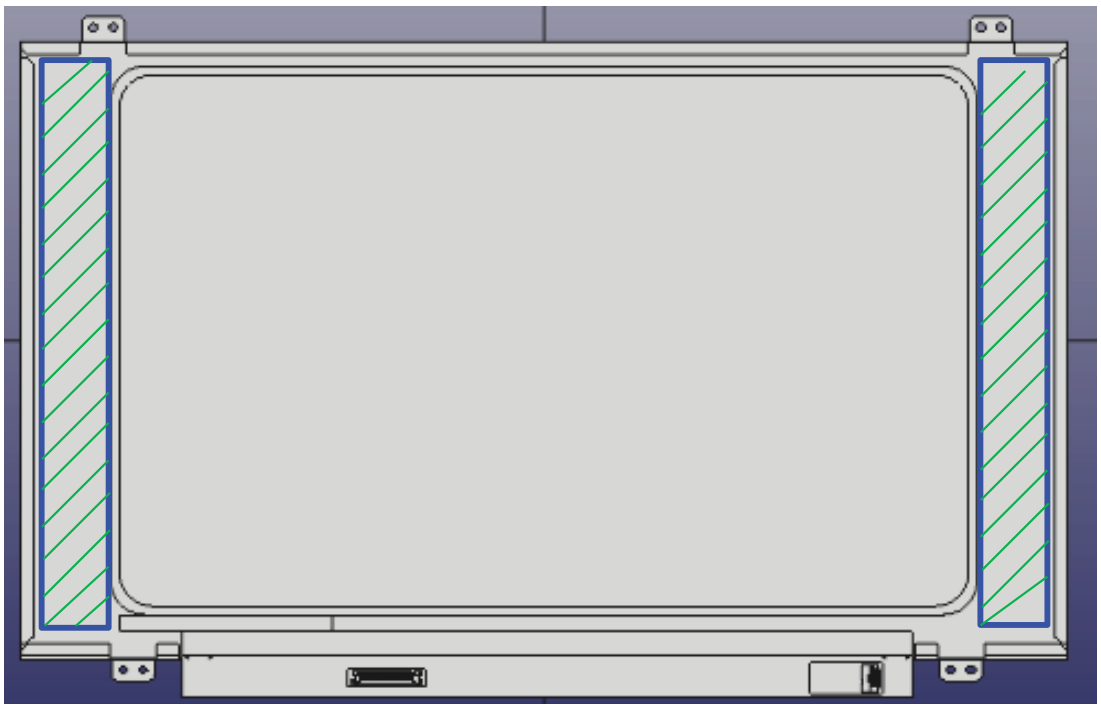


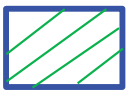
If sponge within the reflector area is necessary, we suggest that the gap between reflector and sponge is more than 0.5mm

Purpose	1. We suggest that do not set Antenna or WebCam cable / wire go behind LCM to avoid backpack test, hinge test ,twist test or pogo test with abnormal display 2. If the cable / wire is necessary to go behind LCM, please make a groove with rounds or chamfers to protect the cable / wire, or attach with higher sponge / rubbers adjacent to the cable / wire route 3. Suggest that attach the cable / wire with tapes to A-cover 4. Do not attach anything with LCM reflector area. If attach cable / wire with LCM reflector area, it may cause pooling, white spot, light leakage and other related issues

Appendix B

LCM paste area



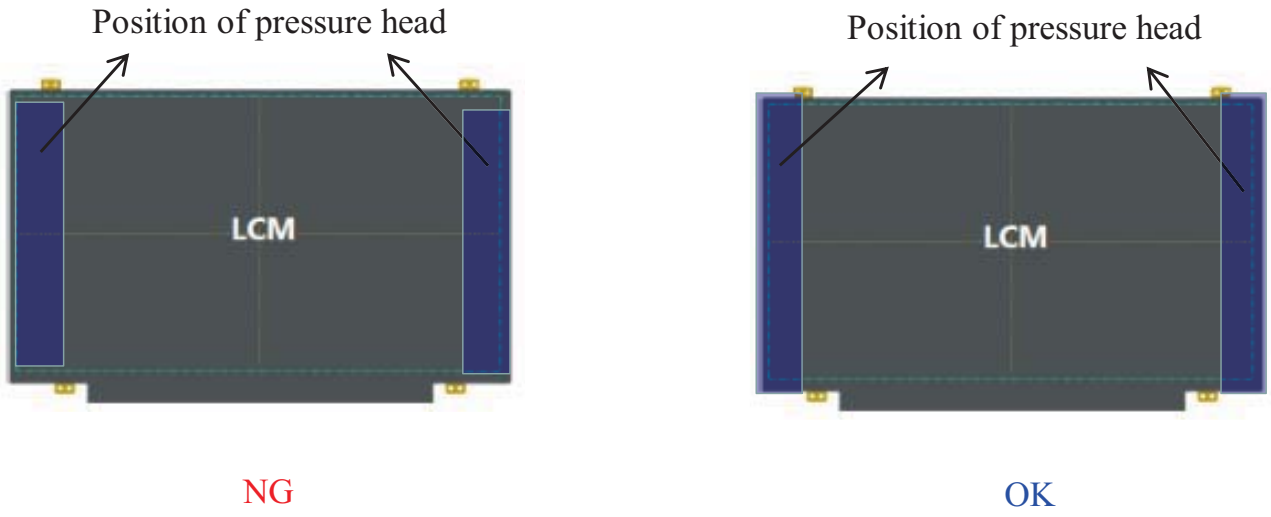


Attachment area

Purpose	If use the stretch remove tapes to fix LCM with A-cover, please set the stretch remove tapes correspond to the LCM back-bezel and do not let the tapes override the back-bezel's level step of opening

Appendix B

LCM pressable area

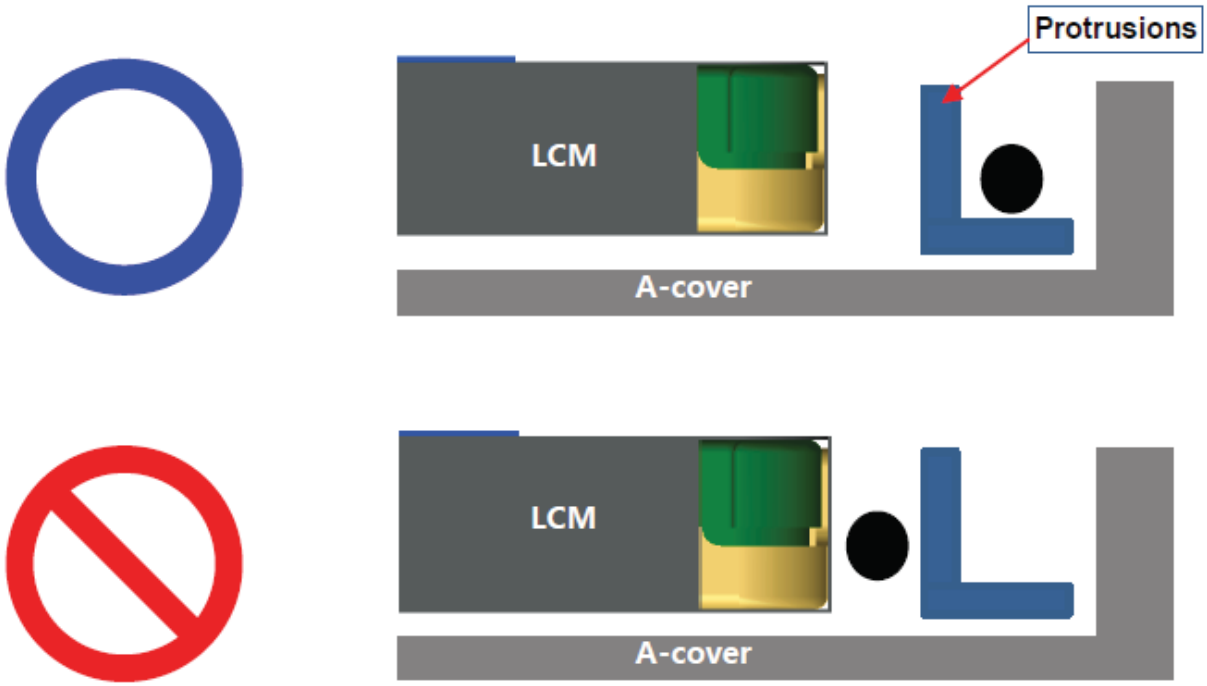


NG OK

Purpose	1. LCM is fixed on A-cover by double-sided tap which can stick LCM after using the press jig stress LCM during assembling. 2. To avoid panel broken the design of pressure head of press jig can not only pin on cell panel. The pressure head needs to pin on the LCM frame, which the LCM frame can share the pressure of the pressing head.

Appendix B

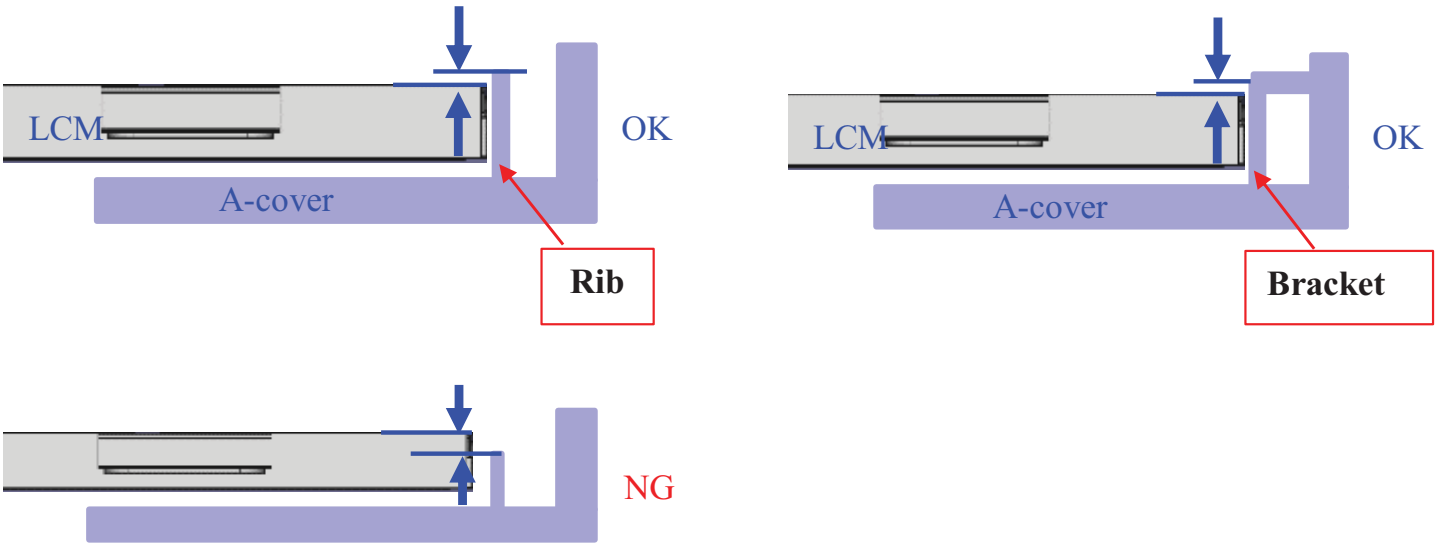
Wire setting



Purpose	Wire should be placed between Protrusions and A-cover. If place the wire between LCM and Protrusions, it may interfere with LCM when assembling B-covers, or even cause LCM breakage in reliability test.

Appendix B

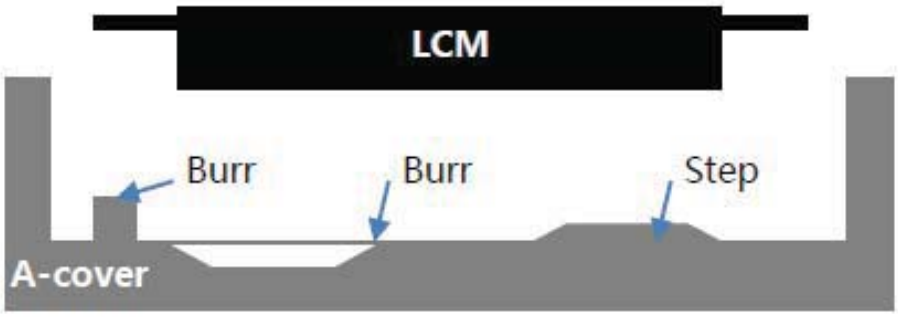
A-cover strength



Purpose	1. It is recommended that Rib height is higher than LCM, in order to avoiding press on LCM edge panels. 2. As for LCM is more stronger than Rib, the L Bracket is be recommended.

Appendix B

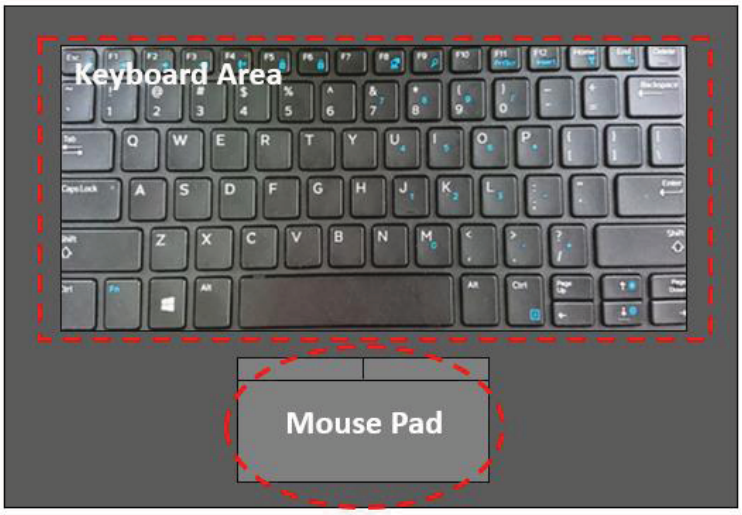
System A-cover Inner Surface

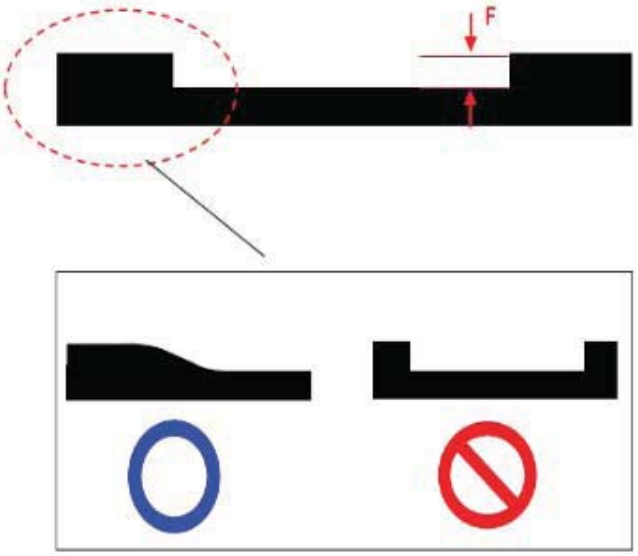


Purpose	There should not exist any burr, segment gap or protrusions beside Logo, which would cause White Spot or Glass Broken by stress concentration.

Appendix B

Keyboard area & Mouse pad



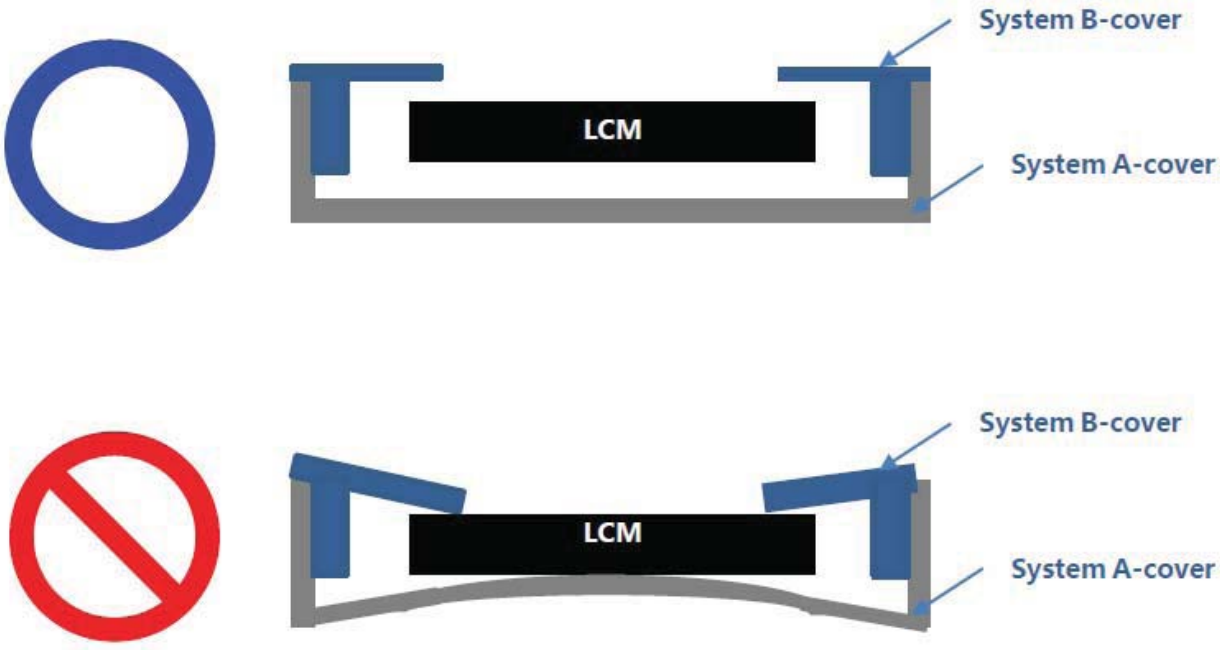


- F: max 0.3mm

Purpose	In order to avoiding LCM fragments in reliability test, the step surface of Keyboard and Mouse pad transmits smoothly, and should not be right-angle. For example, when Pogo testing, if the broken hole is done in this location, it is easy to produce fragments.

Appendix B

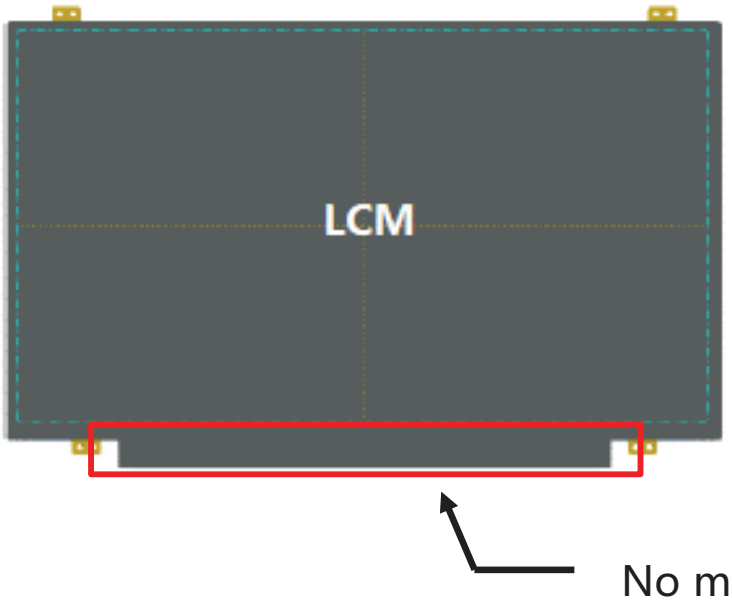
System cover reliability



Purpose	The permanent deformation part of System cover after the reliability test, including sponge and other structures or components, can not touch LCM.

Appendix B

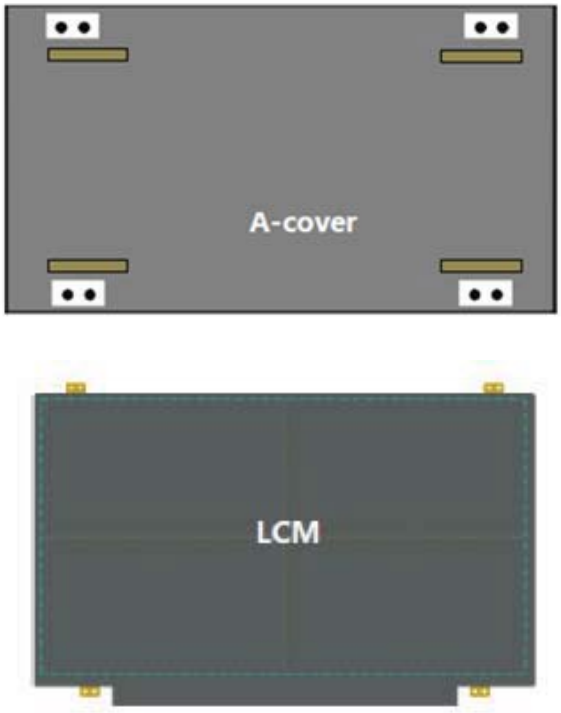
A/B-cover near LCD PCBA



Purpose	There should not have magnet object near LCM PCBA, which is prone to cause physical or electricity noise issue

Appendix B

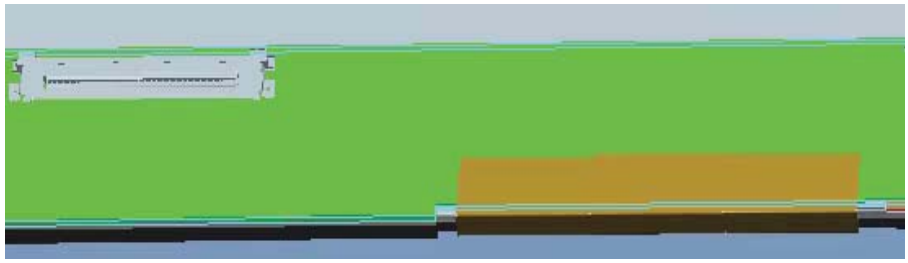
A-cover add sponges on Boss side wall

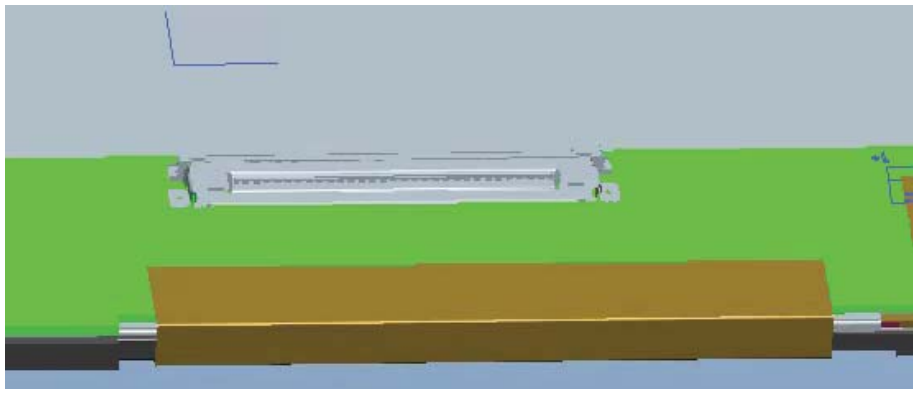


Purpose	We suggest to attach Sponges to the side of the Boss column of A-cover to reduce the panel broken possibility in assembly. It is recommended to this design synchronously.

Appendix B

LCM to A-Cover / sponges z-gap

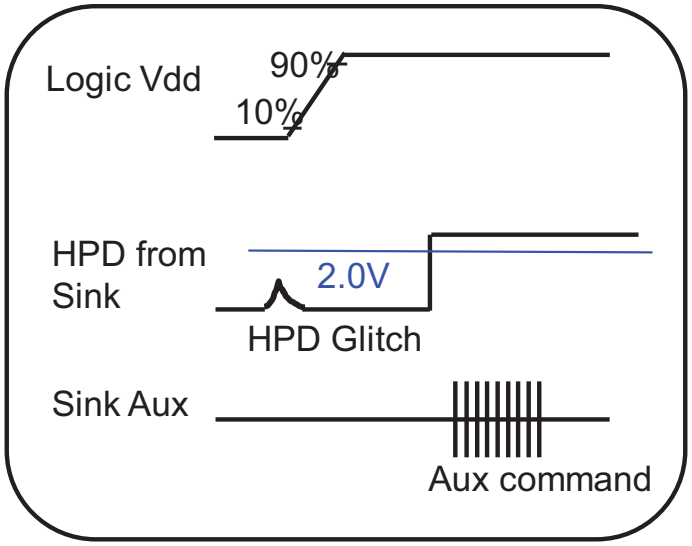




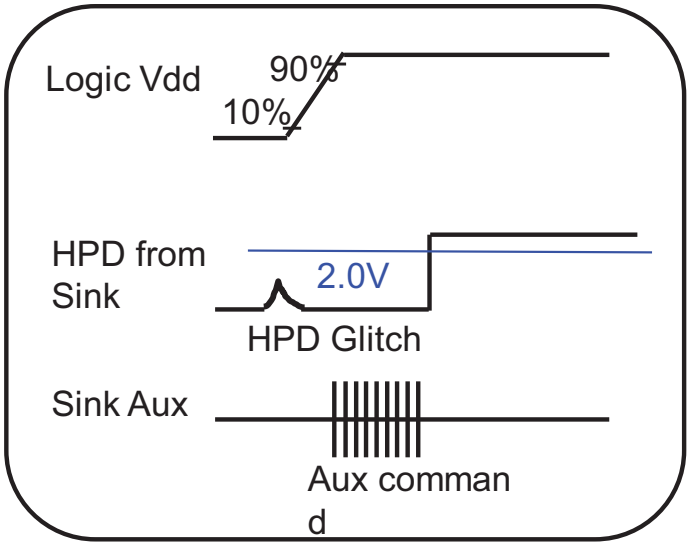
Purpose	Bent product: The position of system connector and FPC should be staggered in X direction. Otherwise, when testing, the system Cable line extrudes FPC, leading to FPC Crack; (Panel FPC Bonding location is related to Mask and can not be changed easily)

Appendix C

HPD Signal recognition



Normal Signal (Ignore HPD Glitch)

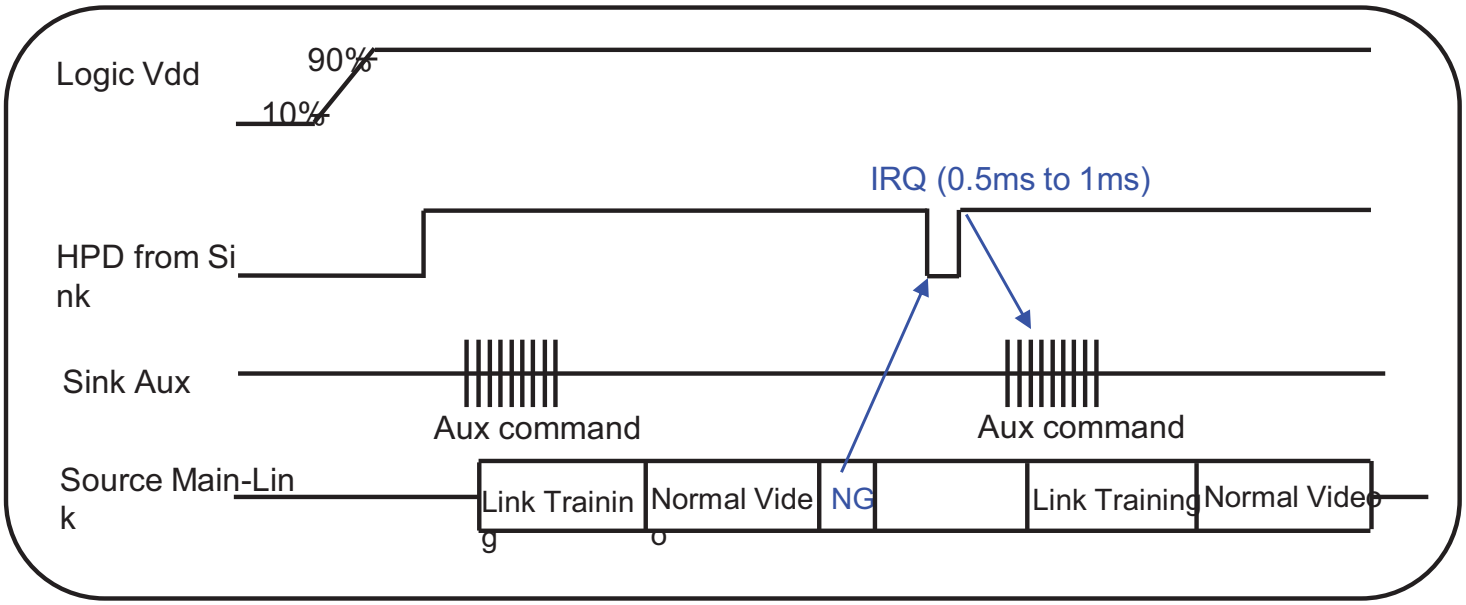


Abnormal Signal

Purpose	When HPD glitch of source device minimum is 2.0(V).

Appendix C

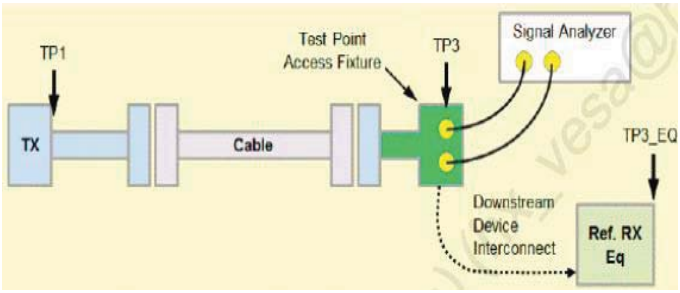
HPD Signal Definition IRQ (Interrupt Request)



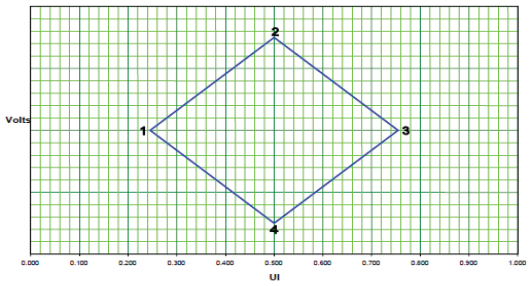
Purpose	When HPD signal low than 0.5ms to 1ms, the source device should check sink status field from the DPCD and take link training again.

Appendix C

Main link eye diagram of TP3



Measured TP3 on LCM connector.



Downstream Device Mask at TP3

	UI	Voltage
1	0.246	0
2	0.5	0.075
3	0.755	0
4	0.5	-0.075

Eye for TP3 at HBR

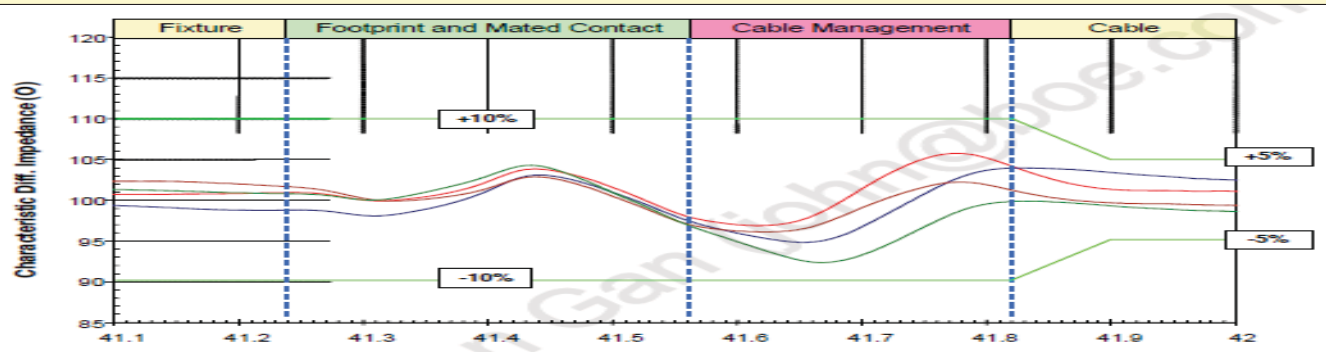
	UI	Voltage
1	0.375	0
2	0.5	0.023
3	0.625	0
4	0.5	-0.023

Eye for TP3 at RBR

Purpose	1. Main Link EYE Diagram should meet TP3 point of VESA. 2. The measure method is through access fixture.

Appendix C

Impedance Profile through a DP Connector



Differential Impedance Profile Measurement Data Example

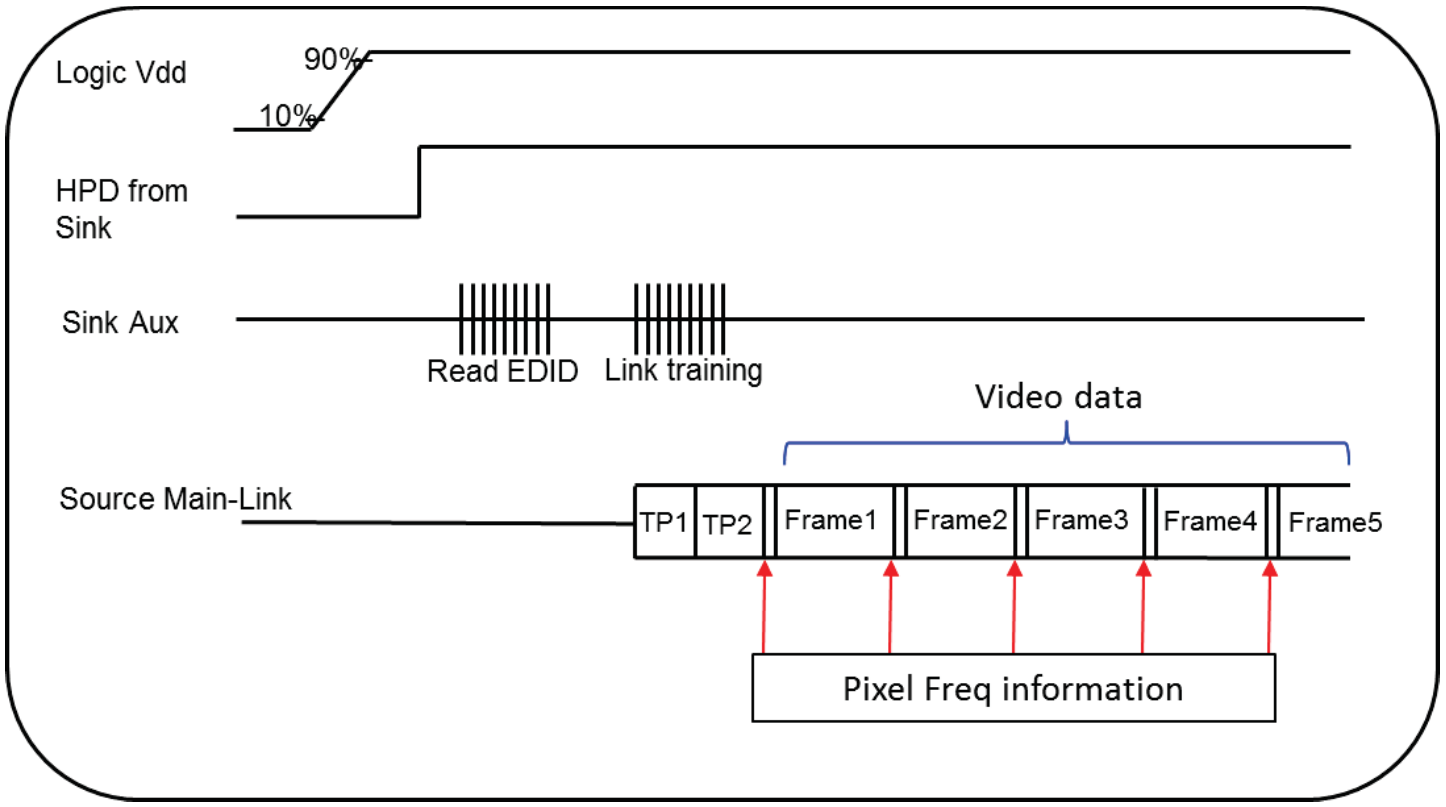
Segment	Differential Impedance Value	Maximum Tolerance
Fixture	100Ω/85Ω VESA	±10%
Connector	100Ω/85Ω VESA	±10%
Wire management	100Ω/85Ω VESA	±10%
Cable	100Ω/85Ω VESA	±5%

Impedance Profile Values for Cable Assembly

Purpose	Cable Impedance Profile 100ohm for Cable Assembly

Appendix C

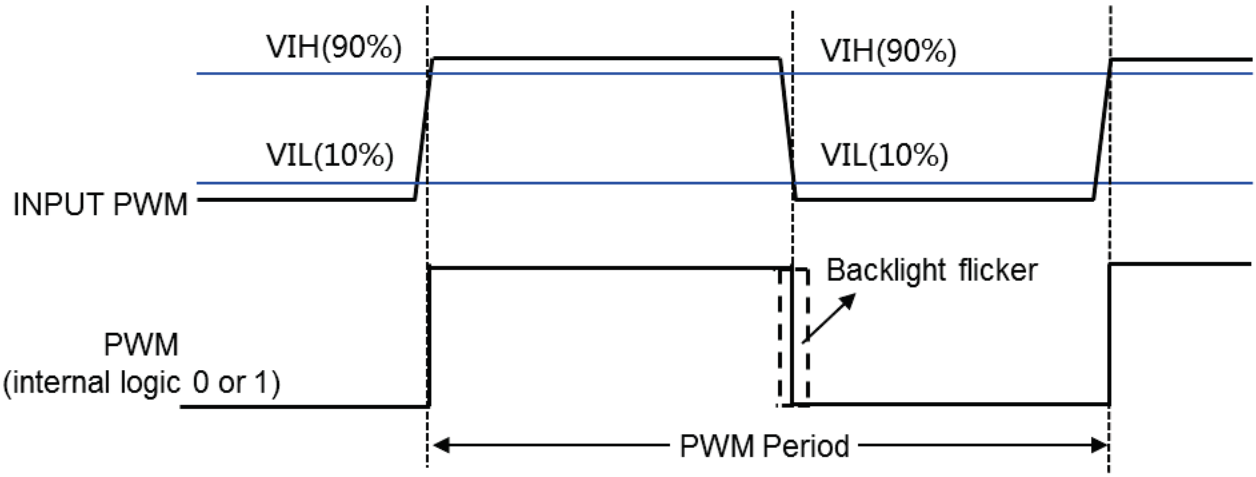
Main Link Pixel Freq information value of MSA data



Purpose	1. It need to fix pixel freq information value of MSA data output to prevent the initial abnormal pixel freq information value from incoming after power on. 2. BOE can read DPCD to check this value. Ex: BIOS is 1.62G , but into windows is 2.7G.

Appendix C

Main Link Pixel Freq information value of MSA data



Example:

Freq	Cycle Time	PWM Rising Time	PWM Falling Time
200Hz	5ms	≤1us	≤1us
1KHz	1ms	≤200ns	≤200ns

Purpose	1. LED driver need to calculate the duty cycle of input PWM signal. 2. To avoid backlight flicker visible on LCD, system input PWM suggest : PWM rising ≤ 200ppm*cycle time ; PWM falling ≤ 200ppm*cycle time.