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Product Specification

7" color TFT-LCD module

MODEL NAME: A070FW03 V3

(◆) Preliminary Specification

(.....) Final Specification

Note: The content of this specification is subject to change.

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Record of Revision

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A. Physical specifications

| NO. | Item | Specification | Remark |
|-----|-------------------------|-----------------------------|--------|
| 1 | Display resolution(dot) | 1440(W)×234(H) | |
| 2 | Active area(mm) | 154.08(W)×86.58(H) | |
| 3 | Screen size(inch) | 7.0(Diagonal) | |
| 4 | Dot pitch(mm) | 0.107(W)×0.370(H) | |
| 5 | Color configuration | R. G. B. stripe | |
| 6 | Overall dimension(mm) | 165.02(W)×100.12(H)×5.76(D) | |
| 7 | Weight(g) | TBD | |
| 8 | Surface treatment | AG(5.5%) | |
| 9 | Backlight unit | CCFL | |

B. Electrical specifications

1.Pin assignment

a. TFT-LCD panel driving section

| Pin no | Symbol | I/O | Description | Remark |
|--------|------------------|-----|---|----------|
| 1 | GND | - | Ground for logic circuit | |
| 2 | V _{CC} | I | Supply voltage of logic control circuit for scan driver | |
| 3 | V _{GL} | I | Negative power for scan driver | |
| 4 | V _{GH} | I | Positive power for scan driver | |
| 5 | STVR | I/O | Vertical start pulse | Note 1 |
| 6 | STVL | I/O | Vertical start pulse | Note 1 |
| 7 | CKV | I | Shift clock input for scan driver | |
| 8 | U/D | I | UP/DOWN scan control input | Note 1,2 |
| 9 | OE _V | I | Output enable input for scan driver | |
| 10 | V _{COM} | I | Common electrode driving signal | |
| 11 | V _{COM} | I | Common electrode driving signal | |
| 12 | L/R | I | LEFT/RIGHT scan control input | Note 1,2 |
| 13 | MOD | I | Sequential sampling and simultaneous sampling setting | Note 3 |
| 14 | OE _H | I | Output enable input for data driver | |
| 15 | STHL | I/O | Start pulse for horizontal scan line | Note 1 |
| 16 | STHR | I/O | Start pulse for horizontal scan line | Note 1 |
| 17 | CPH3 | I | Sampling and shifting clock pulse for data driver | |
| 18 | CPH2 | I | Sampling and shifting clock pulse for data driver | |
| 19 | CPH1 | I | Sampling and shifting clock pulse for data driver | |
| 20 | V _{CC} | I | Supply voltage of logic control circuit for data driver | |
| 21 | GND | - | Ground for logic circuit | |
| 22 | VR | I | Alternated video signal input(Red) | |
| 23 | VG | I | Alternated video signal input(Green) | |
| 24 | VB | I | Alternated video signal input(Blue) | |
| 25 | AV _{DD} | I | Supply voltage for analog circuit | |

| | | | | |
|----|------------------|---|---------------------------|--|
| 26 | AV _{SS} | - | Ground for analog circuit | |
|----|------------------|---|---------------------------|--|

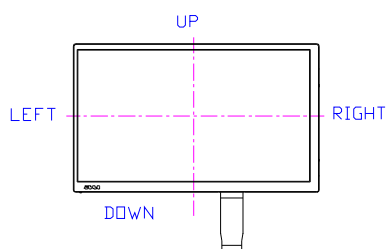
Note 1: Selection of scanning mode (please refer to the following table)

| Setting of scan control input | | IN/OUT state for start pulse | | | | Scanning direction |
|-------------------------------|-----------------|------------------------------|------|------|------|--|
| U/D | L/R | STVR | STVL | STHR | STHL | |
| GND | V _{CC} | OUT | IN | OUT | IN | From up to down, and from left to right. |
| V _{CC} | GND | IN | OUT | IN | OUT | From down to up, and from right to left. |
| GND | GND | OUT | IN | IN | OUT | From up to down, and from right to left. |
| V _{CC} | V _{CC} | IN | OUT | OUT | IN | From down to up, and from left to right. |

IN: Input; OUT: Output.

Note 2: Definition of scanning direction.

Refer to figure as below:



Note 3: MOD = H: Simultaneous sampling.

MOD = L: Sequential sampling.

Please set CPH2 and CPH3 to GND when MOD = H.

b. Backlight driving section (Refer to Figure 1)

| No. | Symbol | I/O | Description | Remark |
|-----|--------|-----|--|--------|
| 1 | HI | I | Power supply for backlight unit (High voltage) | -- |
| 2 | GND | - | Ground for backlight unit | -- |

2. Absolute maximum ratings

| Item | Symbol | Condition | Min. | Max. | Unit | Remark |
|--------------------------|-----------------|-------------|------|---------------|------|------------|
| Power voltage | V_{CC} | GND=0 | -0.3 | 7 | V | |
| | AV_{DD} | $AV_{SS}=0$ | -0.3 | 7 | V | |
| | V_{GH} | GND=0 | -0.3 | 18 | V | |
| | V_{GL} | | -15 | 0.3 | V | |
| | $V_{GH}-V_{GL}$ | | - | 33 | V | |
| Input signal voltage | V_i | | -0.3 | $AV_{DD}+0.3$ | V | Note 1 |
| | V_l | | -0.3 | $V_{CC}+0.3$ | V | Note 2 |
| | VCOM | | -2.9 | 5.2 | V | |
| Storage Temperature | Tstg | | -20 | +70 | °C | Note 3 |
| Operation Temperature | Top | Surface | -10 | +60 | °C | Note 3,4,5 |
| Lamp Max. Rating Voltage | V_L | | | 3000 | V | |

Note 1: VR, VG, VB.

Note 2: STHL, STHR, OEH, L/R, CPH1~CPH3, STVR, STVL, OEV, CKV, U/D.

Note 3: The temperature of panel surface must not exceed this rating

Note 4: Maximum wet-bulb temperature must be less than 58°C. No dew condensation.

Note 5: The operating temperature assure only driving. Contrast, response time, the other display quality is judgment at 25°C.

3. Electrical characteristics

a. Typical operating conditions (GND=AVss=0V, Note 4)

| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
|--------------------------------------|-----------|----------|--------------|---------------|--------------|----------------------|
| Power supply | V_{CC} | 3 | 5 | 5.5 | V | |
| | AV_{DD} | 4.5 | 5 | 5.5 | V | |
| | V_{GH} | 14.3 | 15 | 15.7 | V | |
| | V_{GL} | -10.5 | -10 | -9.5 | V | |
| Video signal amplitude (VR,VG,VB) | V_{iA} | 0.4 | - | $AV_{DD}-0.4$ | V | Note 1 |
| | V_{iAC} | - | 3 | - | V | AC component |
| | V_{iDC} | - | $AV_{DD}/2$ | - | V | DC component |
| VCOM | V_{CAC} | 3.5 | 5.6 | 6.5 | Vp-p | AC component, Note 2 |
| | V_{CDC} | 1.4 | 1.7 | 2.0 | V | DC component |
| Input signal | H Level | V_{IH} | $0.8 V_{CC}$ | - | V_{CC} | Note 3 |
| | L Level | V_{IL} | 0 | - | $0.2 V_{CC}$ | |

Note 1: Refer to Fig.4- (a).

Note 2: Adjusting the AC component of VCOM could change the brightness of LCD panel.

Note 3: STHL, STHR, OEH, L/R, CPH1~CPH3, STVR, STVL, OEV, CKV, U/D.

Note 4: Be sure to apply GND, V_{CC} and V_{GL} to the LCD first, and then apply V_{GH} .

b. Current consumption (GND=AVss=0V)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|--------------------|----------|---------------|------|------|------|------|--------|
| Current for driver | I_{GH} | $V_{GH}=15V$ | - | 0.20 | 0.5 | mA | |
| | I_{GL} | $V_{GL}=-10V$ | - | 0.80 | 1.5 | mA | |
| | I_{CC} | $V_{CC}=5V$ | - | 3.0 | 6.0 | mA | |
| | I_{DD} | $AV_{DD}=5V$ | - | 17.0 | 30 | mA | |

c. Backlight driving conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remark |
|-----------------------|--------|--------|------|-------|-------------------|-------------------------------|
| Lamp voltage | V_L | - | 538 | 591 | Vrms | $I_L=6mA$ |
| Lamp current | I_L | - | 6.0 | 7 | mA _{rms} | |
| Frequency | F_L | - | 70 | 80 | kHz | Note 3 |
| Lamp starting voltage | V_s | - | 844 | 1,070 | Vrms | $T_a = 25^{\circ}C$, Note 5 |
| | | - | | 1,540 | Vrms | $T_a = -10^{\circ}C$, Note 5 |
| Lamp life time | | 10,000 | - | - | Hr | Note 6 |

Note 1: The lamp frequency should be selected as different as possible from display horizontal synchronous signal to avoid interference.

Note 2: For starting the backlight unit, the output voltage of DC/AC's transformer should be larger than the maximum lamp starting voltage.

Note 3: The" Lamp life time" is defined as the module brightness decrease to 50% original brightness at $T_a=25^{\circ}C$, $I_L=6mA$.

4. AC Timing

a. Timing conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit. | Remark |
|---------------------------------|-------------------------------------|------|-------------|-------------|-------------|-----------|
| Rising time | t_r | - | - | 10 | ns | Note 1 |
| Falling time | t_f | - | - | 10 | ns | Note 1 |
| High and low level pulse width | t_{CPH} | 99 | 103 | 107 | ns | CPH1~CPH3 |
| CPH pulse duty | t_{CWH} | 40 | 50 | 60 | % | CPH1~CPH3 |
| CPH pulse delay | t_{C12} t_{C23} t_{C31} | 30 | $t_{CPH}/3$ | $t_{CPH}/2$ | ns | CPH1~CPH3 |
| STH setup time | t_{SUH} | 20 | - | - | ns | STHR,STHL |
| STH hold time | t_{HDH} | 20 | - | - | Ns | STHR,STHL |
| STH pulse width | t_{STH} | - | 1 | - | t_{CPH} | STHR,STHL |
| STH period | t_H | 61.5 | 63.5 | 65.5 | μs | STHR,STHL |
| OEH pulse width | t_{OEH} | - | 1.22 | - | μs | OEH |
| Sample and hold disable time | t_{DIS1} | - | 8.28 | - | μs | |
| OEV pulse width | t_{OEV} | - | 5.40 | - | μs | OEV |
| CKV pulse width | t_{CKV} | - | 4.18 | - | μs | CKV |
| Clean enable time | t_{DIS2} | - | 3.74 | - | μs | |
| Horizontal display start | t_{SH} | - | 0 | - | $T_{CPH}/3$ | |
| Horizontal display timing range | t_{DH} | - | 1440 | - | $T_{CPH}/3$ | |
| STV setup time | t_{SUV} | 400 | - | - | ns | STVL,STVR |
| STV hold time | t_{HDV} | 400 | - | - | ns | STVL,STVR |
| STV pulse width | t_{STV} | - | - | 1 | t_H | STVL,STVR |
| Horizontal lines per field | t_V | 256 | 262 | 268 | t_H | Note 2 |
| Vertical display start | t_{SV} | | 3 | - | t_H | |
| Vertical display timing range | t_{DV} | | 234 | - | t_H | |
| VCOM rising time | t_{rCOM} | | - | 5 | μs | |
| VCOM falling time | t_{fCOM} | | - | 5 | μs | |
| VCOM delay time | t_{DCOM} | | - | 3 | μs | |
| RGB delay time | t_{DRGB} | | - | 1 | μs | |

Note 1: The values herein are for all of the logic signals.

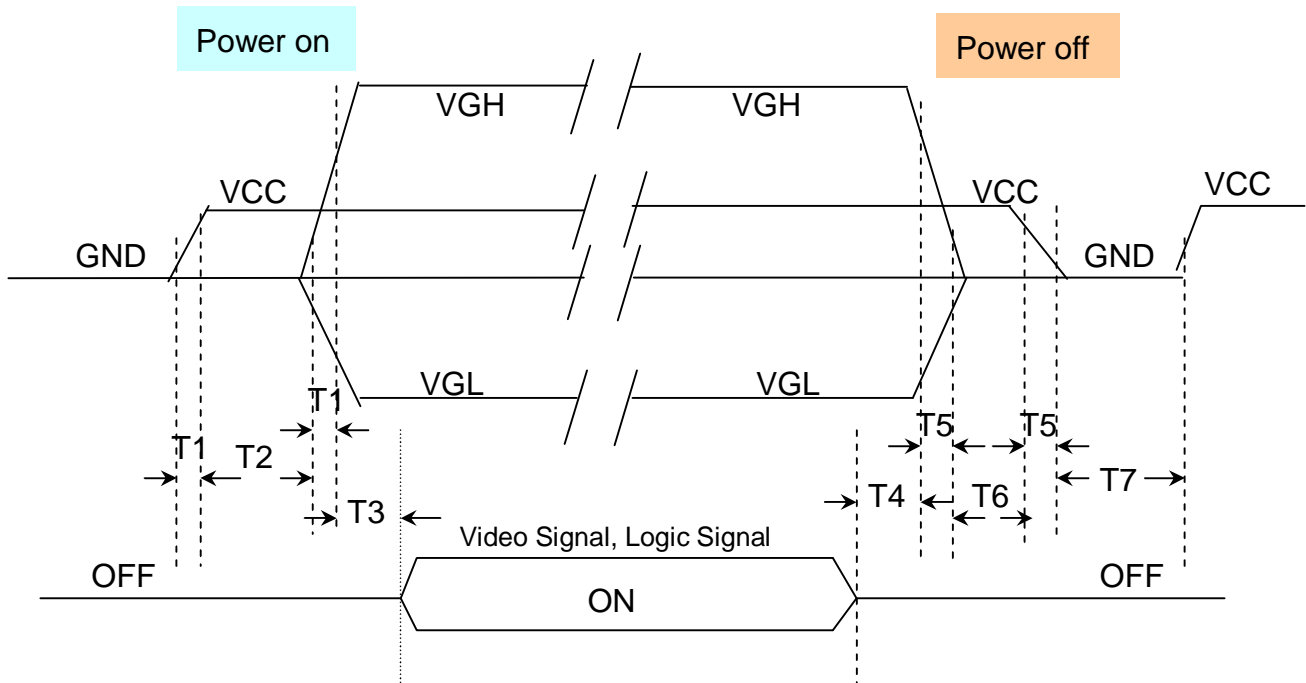
Note 2: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b. Timing diagram

Please refer to the attached drawing, from Fig.2 to Fig.6.

5. Power Sequence

Sequence for power on/off and Signal on/off



- T1 \cong 15ms (From 10%*VCC to 90%*VCC , when VCC is Low to High) ;
- T2 \cong 10ms (From 90%*VCC to 10%*VGH , when VCC is Low to High) ;
- T3 \cong 10ms (From 90%*VGH to Video signal , when VGH is Low to High) ;
- T4 \cong 10ms (From Video signal to 90%*VGH , when VGH is High to Low) ;
- T5 \cong 20ms (From 90%*VCC to 10%*VCC , when VCC is High to Low) ;
- T6 \cong 10ms (From 10%*VGH to 90%*VCC , when VCC is Low to High) ;
- T7 \cong 0.4s (From 10%*VCC is H→L to 10%*VCC is L→H) °

C. Optical specification (Note 1, Note 2)

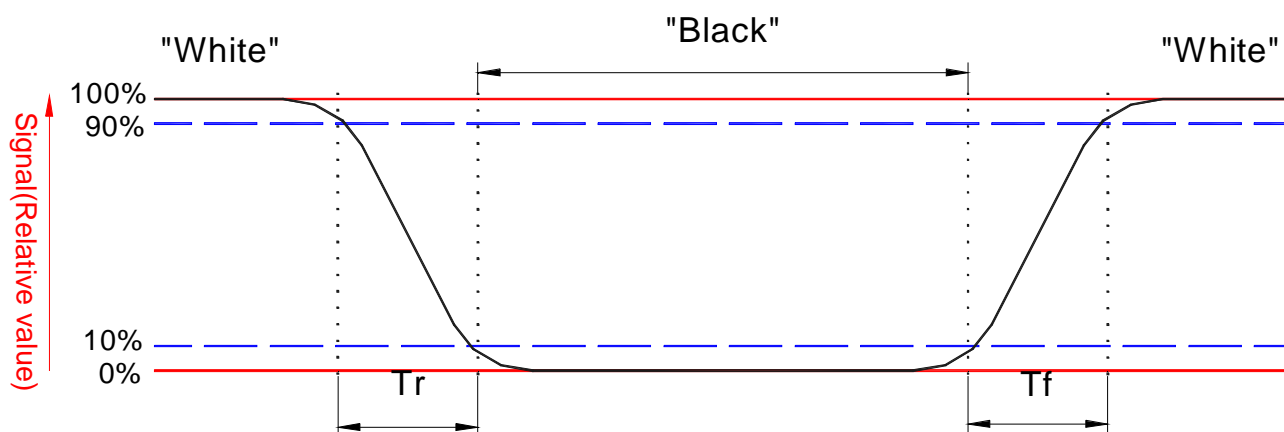
| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|--------------------|--------|--------|---|------|------|------|-----------------|-----------|
| Response time | Rise | Tr | $\theta = 0^\circ$ | - | 12 | 24 | ms | Note 3,5 |
| | Fall | Tf | | - | 18 | 36 | ms | |
| Contrast ratio | | CR | At optimized Viewing angle | 300 | 400 | - | | Note 4, 5 |
| Viewing angle | Top | | $CR \geq 10$ | 10 | 15 | - | deg. | Note 5, 6 |
| | Bottom | | | 30 | 35 | - | | |
| | Left | | | 45 | 50 | - | | |
| | Right | | | 45 | 50 | - | | |
| Brightness | | Y_L | $I_L = 6\text{mA}$, 25°C | 200 | 250 | - | cd/m^2 | Note 7 |
| | | | $I_L = 6.5\text{mA}$, 25°C | 250 | 300 | - | cd/m^2 | |
| White chromaticity | X | | $\theta = 0^\circ$ | 0.26 | 0.31 | 0.36 | | Note 7 |
| | Y | | $\theta = 0^\circ$ | 0.28 | 0.33 | 0.38 | | |

Note 1 : Ambient temperature $= 25^\circ\text{C}$, and lamp current $I_L = 6 \text{ mArms}$. To be measured in the dark room. DC/AC inverter driving frequency: 70 kHz.

Note 2 : To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5, after 15 minutes operation.

Note 3. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (falling time) and from "white" to "black" (rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 5. White $V_i = V_{i50} + 1.5V$

Black $V_i = V_{i50} \pm 2.0V$

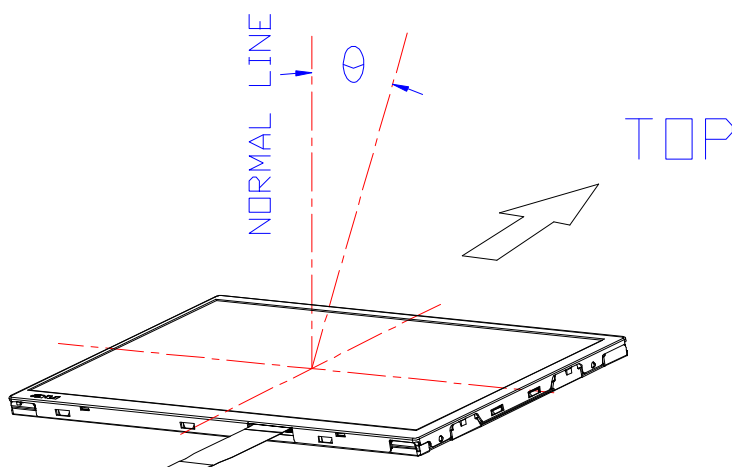
“ \pm ” means that the analog input signal swings in phase with V_{COM} signal.

“ \mp ” means that the analog input signal swings out of phase with V_{COM} signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6. Definition of viewing angle, details please refer to figure as below.



Note 7. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

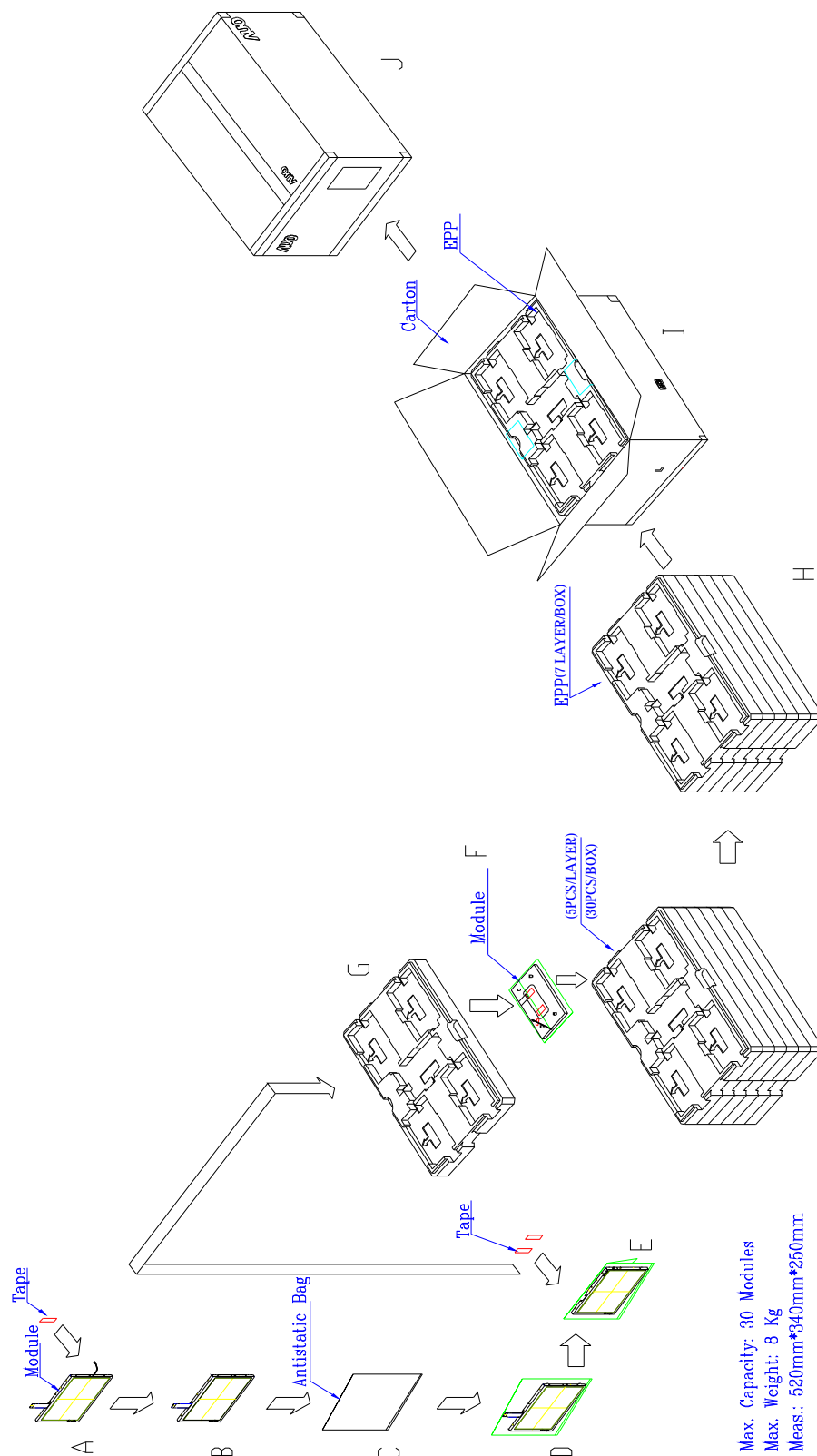
D. Reliability test items (Note 1):

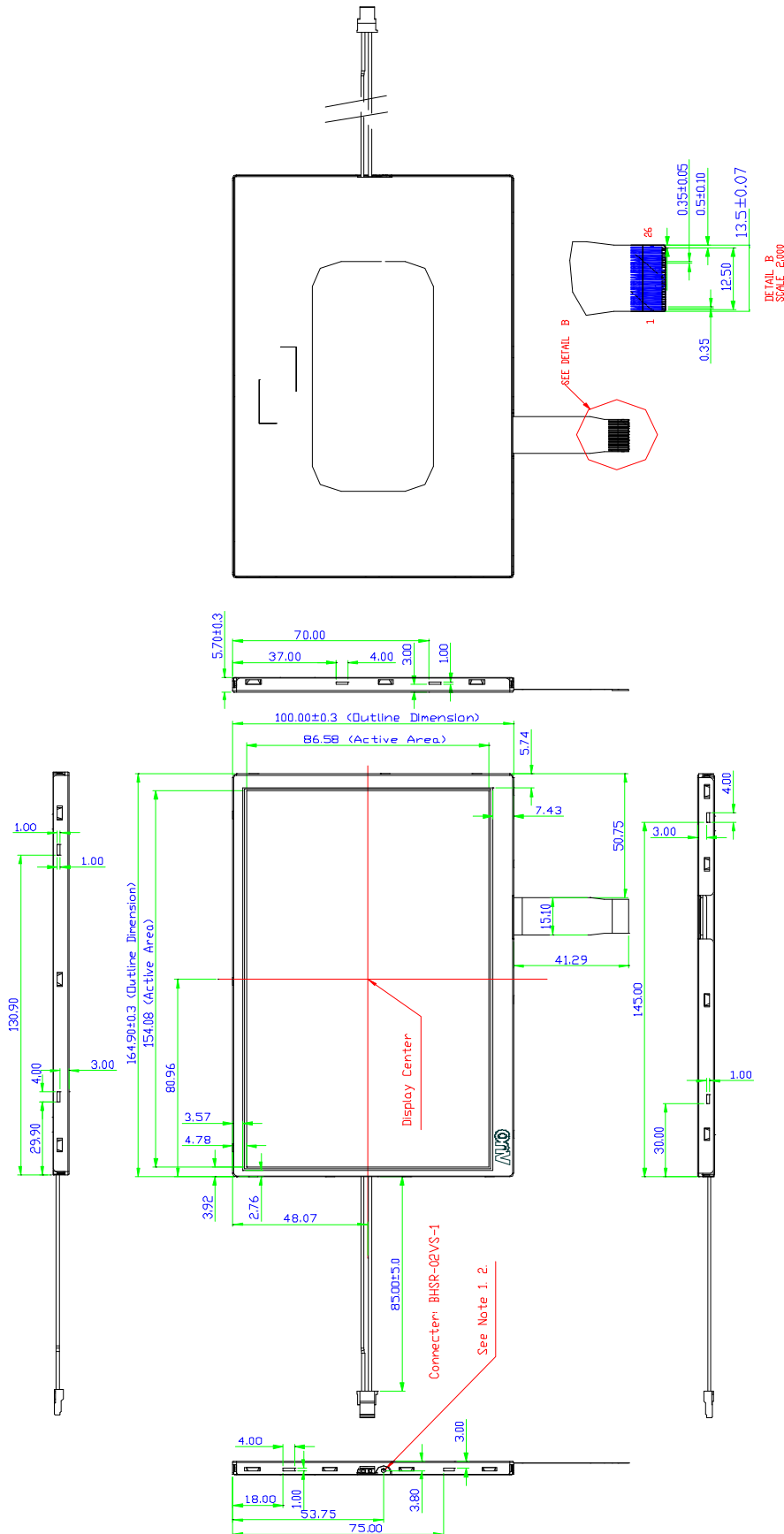
Following the below condition for test criteria. Each item needs 5 piece data.

| No. | Test items | Conditions | Remark |
|-----|------------------------------------|---|-----------------------------------|
| 1 | High temperature storage | Ta= 70℃ 240Hrs | |
| 2 | Low temperature storage | Ta= -20℃ 240Hrs | |
| 3 | High temperature operation | Tp= 60℃ 240Hrs | |
| 4 | Low temperature operation | Ta= -10℃ 240Hrs | |
| 5 | High temperature and high humidity | Tp= 40℃, 90% RH 240Hrs | Operation |
| 6 | Heat shock | -10℃~60℃/200 cycles 1Hrs/cycle | Non-operation |
| 7 | Electrostatic discharge | ±200V,200pF(0Ω), once for each terminal | Non-operation |
| 8 | Vibration | Frequency range : 8~33.3Hz Stoke : 1.3mm Sweep : 2.9G, 33.3 ~ 400Hz Cycle : 15 minutes 2 hours for each direction of X,Z 4 hours for Y direction | JIS D1601, A-10 Condition A |
| 9 | Mechanical shock | 100G, 6ms, ±X,±Y,±Z 3 times for each direction | JIS C0041, A-7 Condition C |
| 10 | Vibration (with carton) | Random vibration: 0.015G ² /Hz from 5~200Hz | IEC 68-34 |
| 11 | Drop (with carton) | Height: 60cm | JIS Z0202 |

Note1: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

E. Packing form





- Note: 1. The screw torque allowed 2kg-cm.
2. The screw size : M2.0x1.5mm(Pitch 0.4mm)
3. The Connector of lamp : BHSR-02VS-1
4. General tolerance is ±0.3
5. The bending radius of FPC should be larger than 0.6

Fig.1- Outline dimension of TFT-LCD module

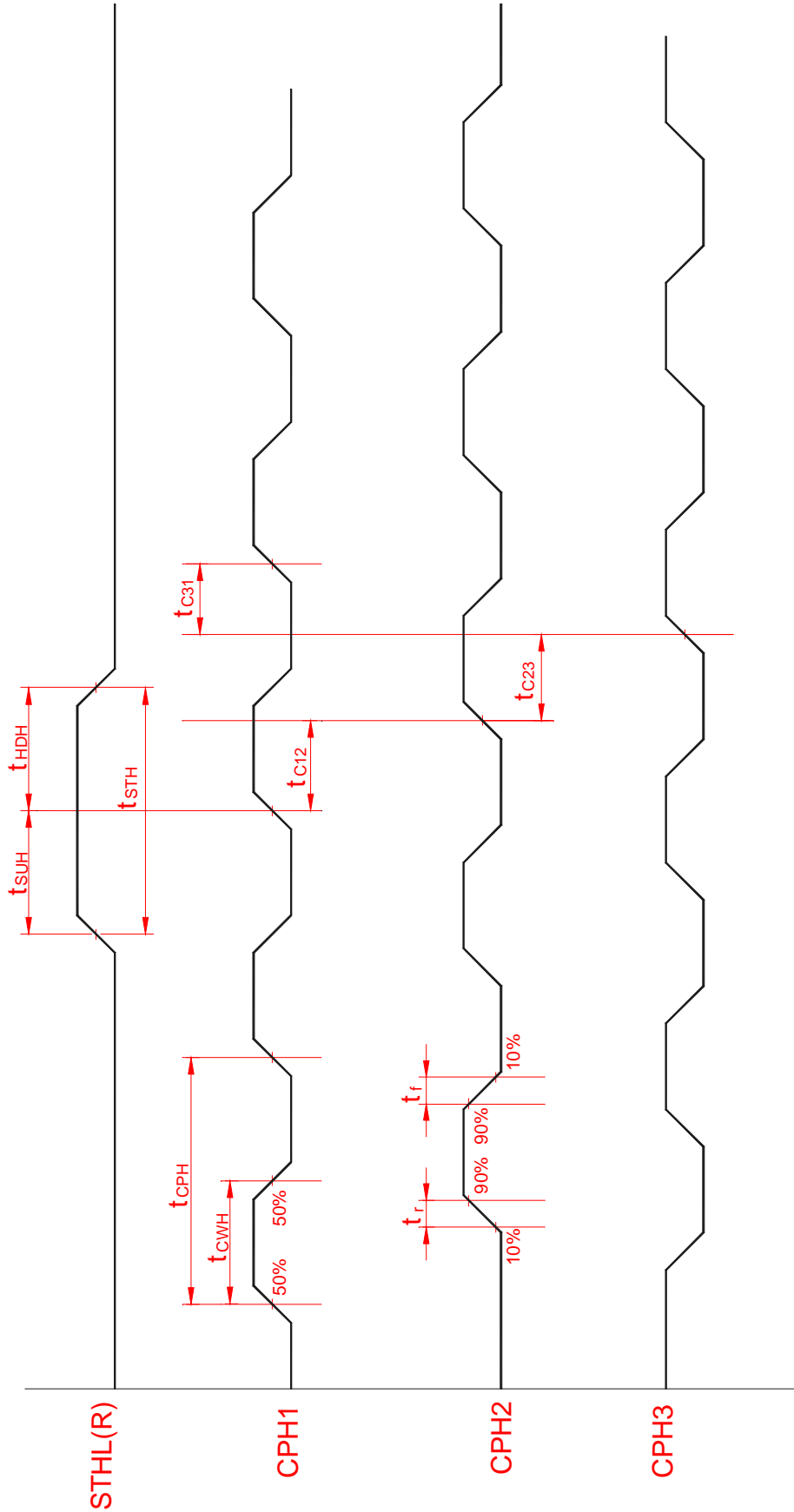


Fig.2 Sampling clock timing

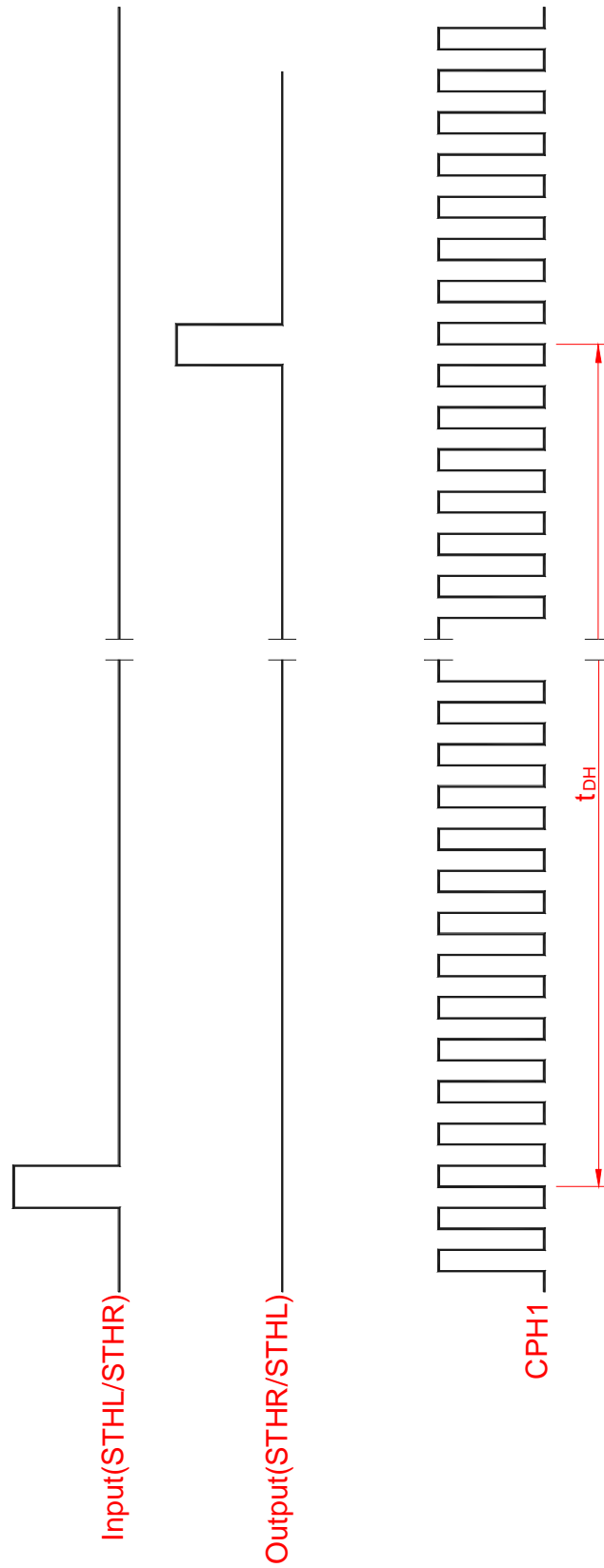


Fig.3 Horizontal display timing range

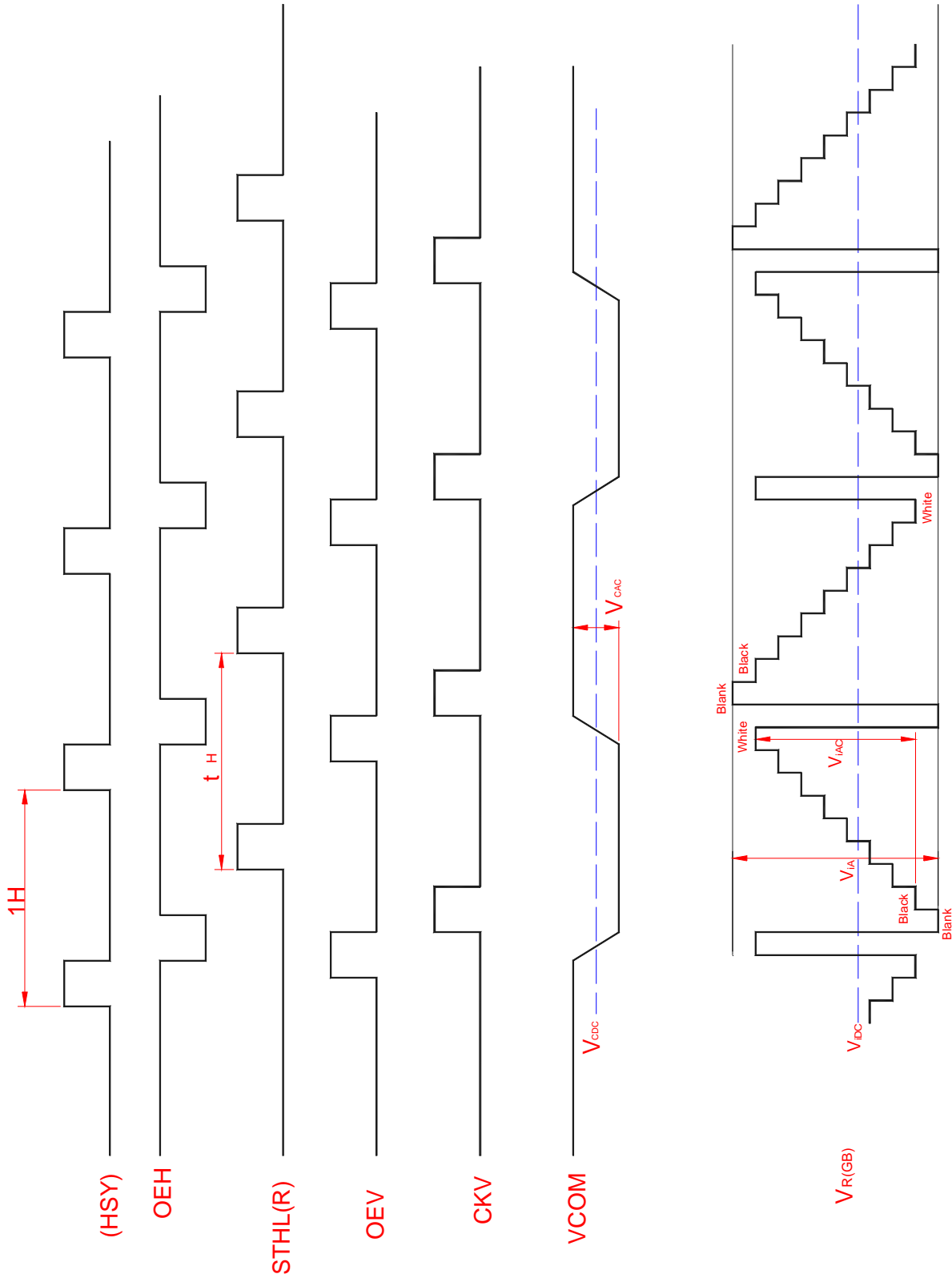


Fig.4-(a) Horizontal timing

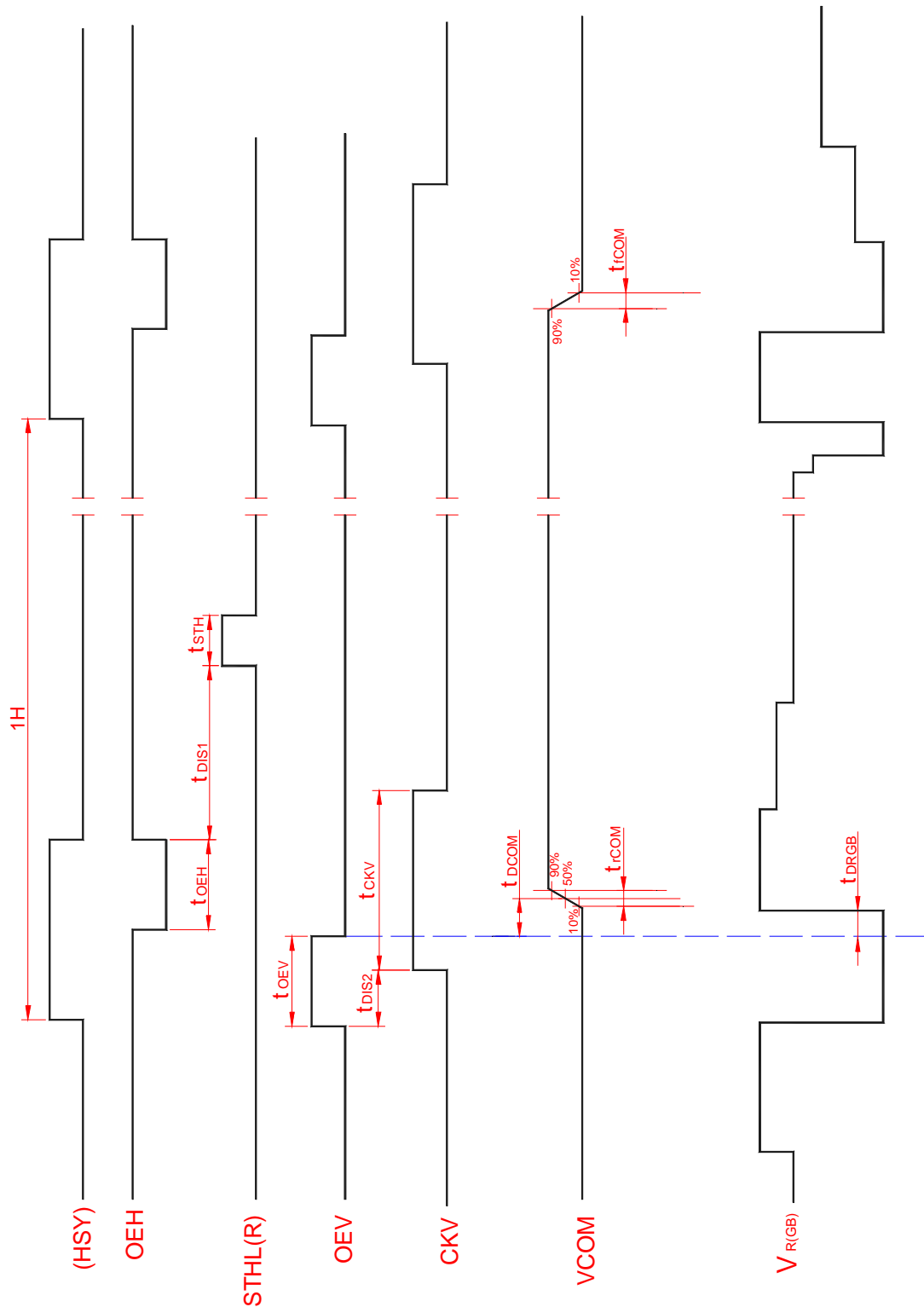


Fig.4-(b) Detail horizontal timing

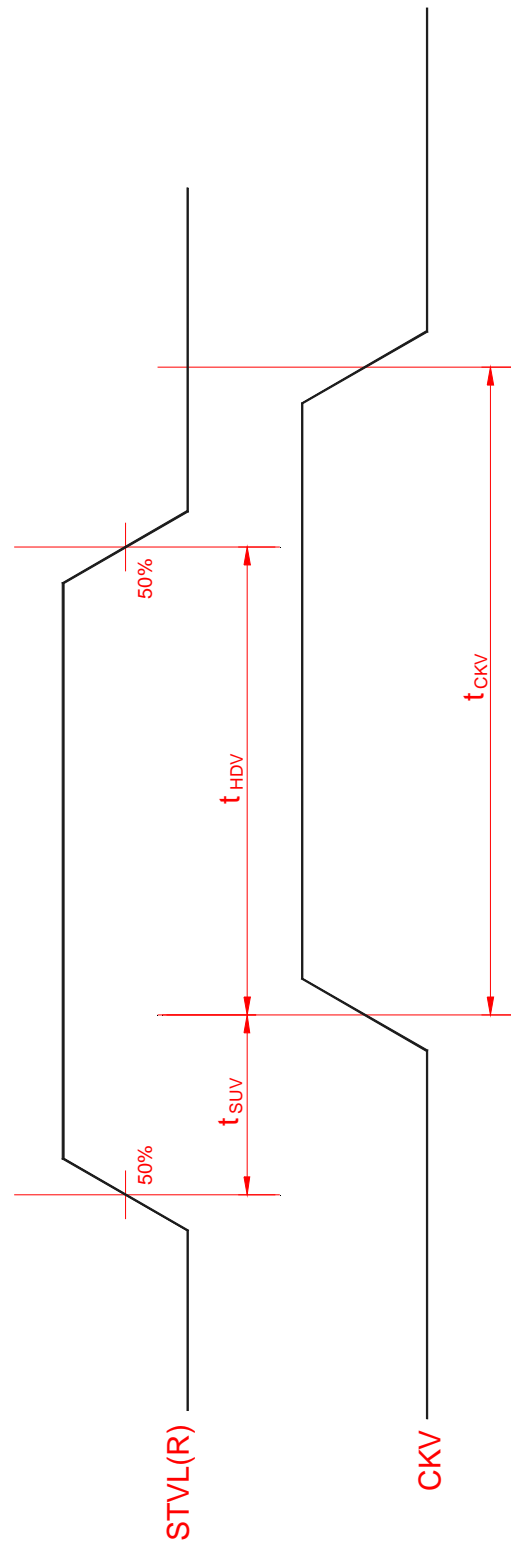


Fig.5 Vertical shift clock timing

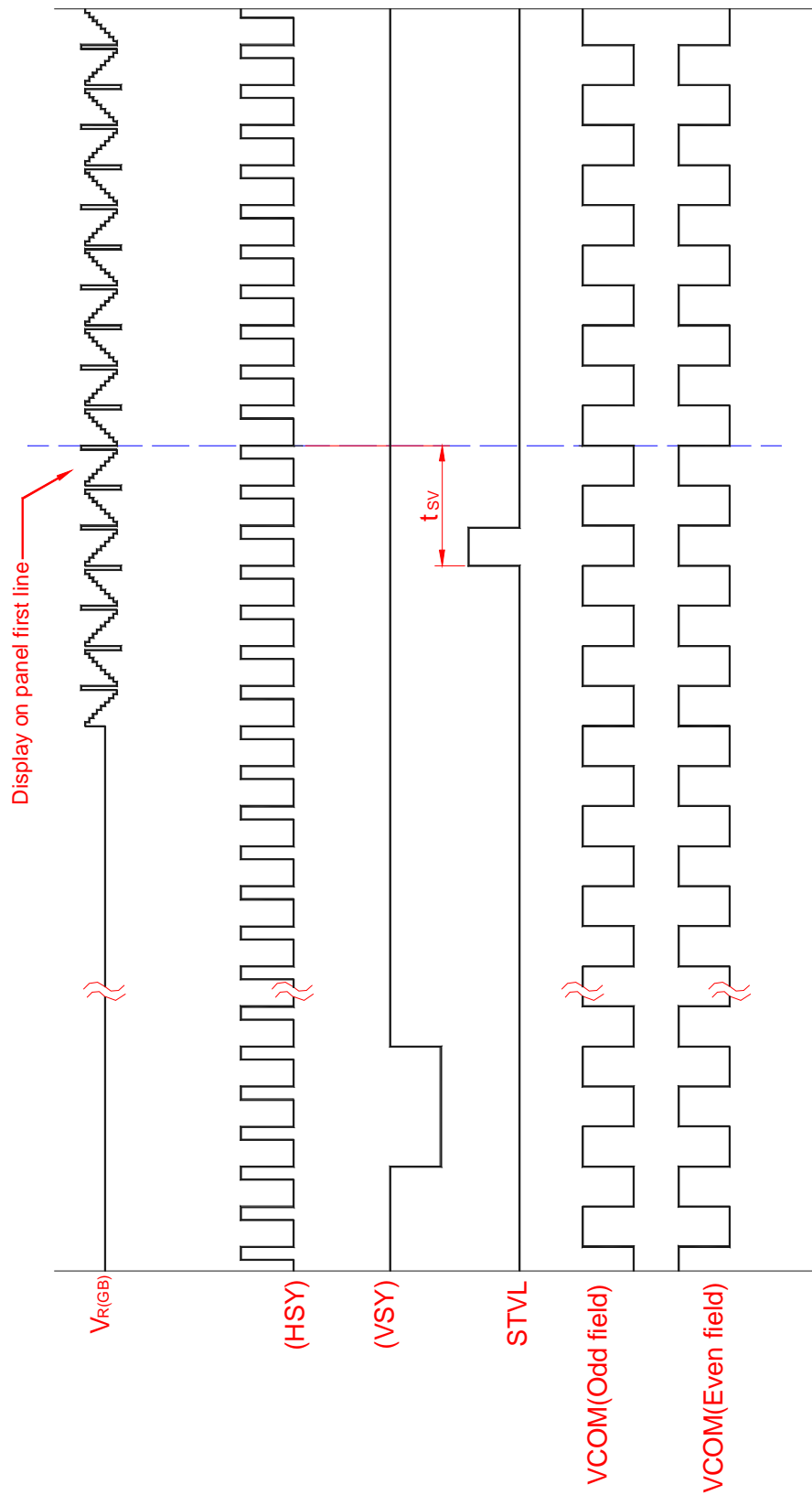


Fig.6-(a) Vertical timing (From up to down)

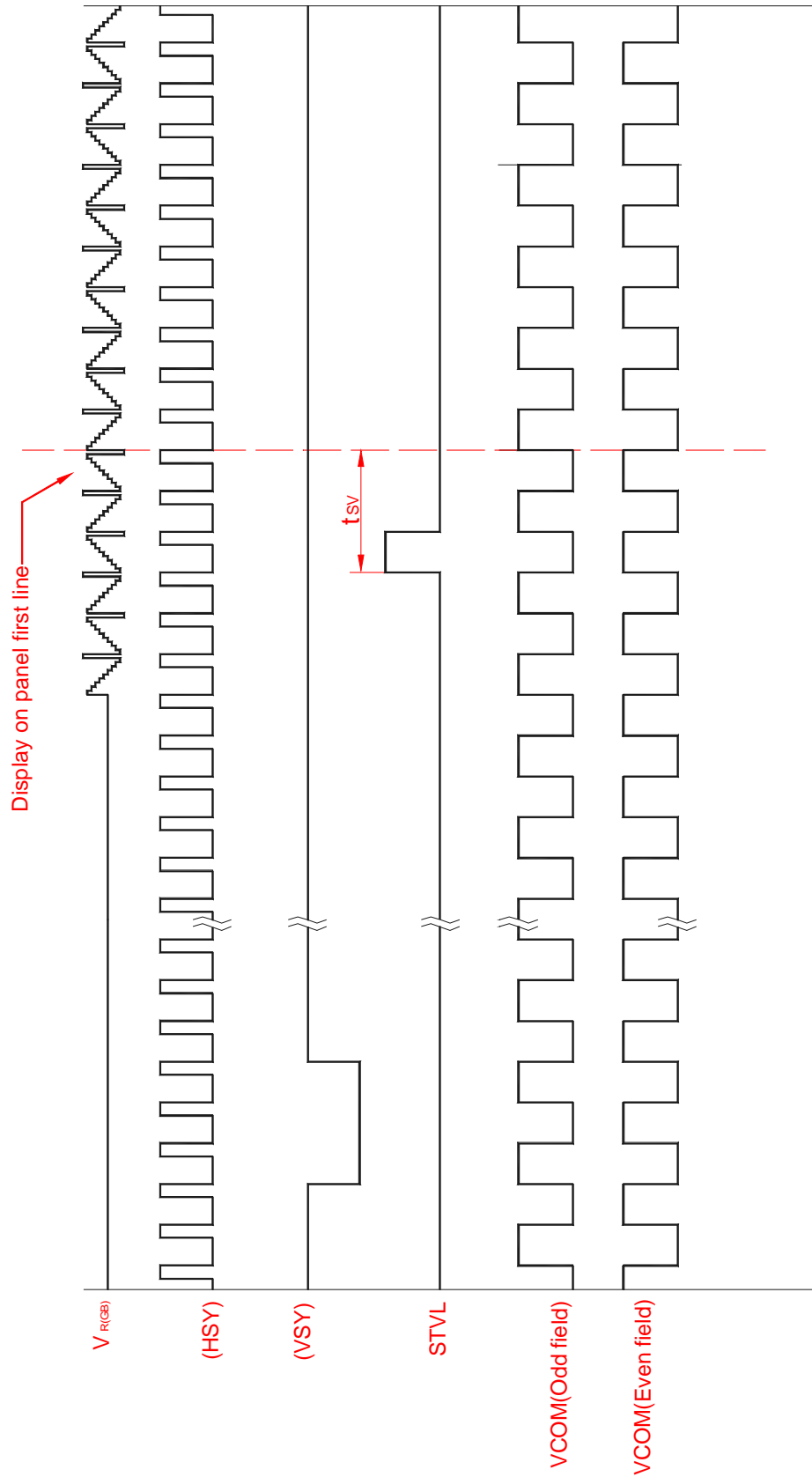


Fig.6-(b) Horizontal timing (From down to up)