Product Specification
AU OPTRONICS CORPORATION

(   ) Preliminary Specifications
(V) Final Specifications

Module	14.0" HD Color TFT-LCD with LED Backlight design
Model Name	B140XW01 V4
Note (🔌)	*LED Backlight with driving circuit design*

Customer	Date	Approved by	Date
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Note: This Specification is subject to change without notice.		NBBU Marketing Division / AU Optronics corporation	

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Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2009/01/23	All	First Edition for Customer		
0.2 2009/06/22	31	Shipping label H/W code: **4A**	Revise to H/W code: **1A**	
0.3 2009/07/14	34~37	TBD EDID	New EDID format.	
0.4 2009/07/17	34~37		Updated BRT value into EDID.	
0.5 2009/12/23	6	TBD Chromaticity	New Chromaticity.	
	34	Old EDID	New EDID.	
1.0 2010/02/26	1	Preliminary spec	Final spec	
	17	timing spec	Revised timing spec.	
	23		New added interface timing	

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1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.

7) Do not open nor modify the Module Assembly.

8) Do not press the reflector sheet at the back of the module to any directions.

9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.

11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.

13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breakdown.

2. General Description

B140XW01 V4 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the HD (1366(H) x 768(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are Display Port interface compatible.

B140XW01 V4 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	354.95 (14.0W")			
Active Area	[mm]	309.40 X 173.95			
Pixels H x V		1366x3(RGB) x 768			
Pixel Pitch	[mm]	0.2265X0.2265			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (I_{LED}=20mA) (Note: ILED is LED current)	[cd/m^2]	200 typ. (5 points average) 170 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		400 typ			
Response Time	[ms]	8 typ / 12 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.7 max. (Include Logic and Blu power)			
Weight	[Grams]	350 max.			
Physical Size **without inverter, bracket.**	[mm]		Min.	Typ.	Max.
		Length		323.5	324
		Width		192	192.5
		Thickness			5.2
Glass thickness	[mm]	TFT=0.5. CF=0.5			
Electrical Interface		1 channel Display Port			
Surface Treatment		Anti-Glare			

| Support Color		262K colors (RGB 6-bit)

Temperature Range
  Operating
  Storage (Non-Operating)
	[°C]
	[°C]
		0 to +50
		-20 to +60

RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=20mA			5 points average	170	200	-	cd/m²	1, 4, 5.
Viewing Angle		θ R θ L	Horizontal (Right) CR = 10 (Left)	40 40	45 45	- -	degree	4, 9
		Ψ H Ψ L	Vertical (Upper) CR = 10 (Lower)	10 30	15 35	- -		
Luminance Uniformity		δ 5P	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ 13P	13 Points	-	-	1.50		2, 3, 4
Contrast Ratio		CR		300	400	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_r	Rising	-	-	-	msec	4, 8
		T_f	Falling	-	-	-		
		T_{RT}	Rising + Falling	-	8	12		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.560	0.590	0.620	-	4
		Ry		0.315	0.345	0.375		
	Green	Gx		0.310	0.340	0.370		
		Gy		0.540	0.570	0.600		
	Blue	Bx		0.120	0.150	0.180		
		By		0.090	0.120	0.150		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	45	-		

Note 1: 5 points position (Ref: Active area)
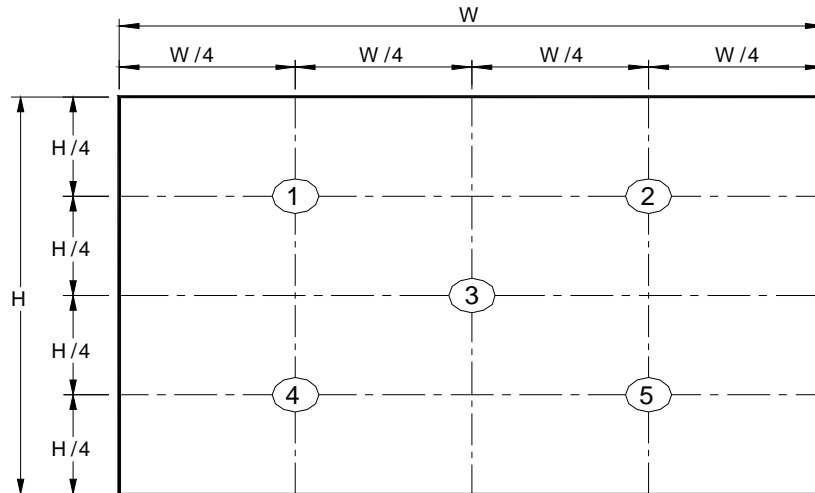
Note 2: 13 points position (Ref: Active area)
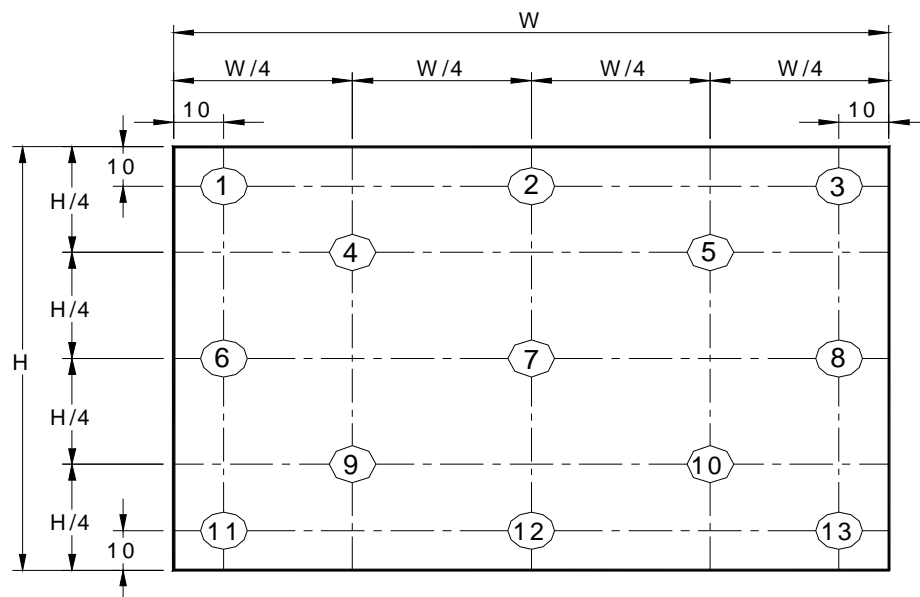
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature

change during measuring. In order to stabilize the luminance, the measurement should be executed after

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lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.

Center of the screen
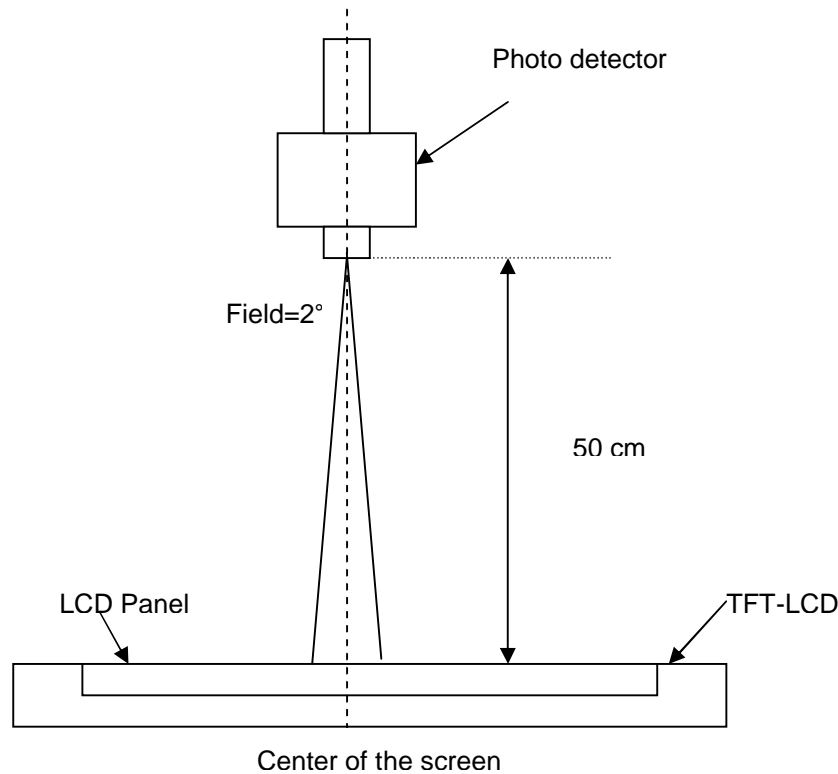
Note 5： Definition of Average Luminance of White (Y $_L$):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:
     Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

Note 7： Definition of Cross Talk (CT)

CT = | Y_B – Y_A | / Y_A ✕ 100 (%)

Where

Y_A = Luminance of measured location without gray level 0 pattern (cd/m$_2$)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m$_2$)

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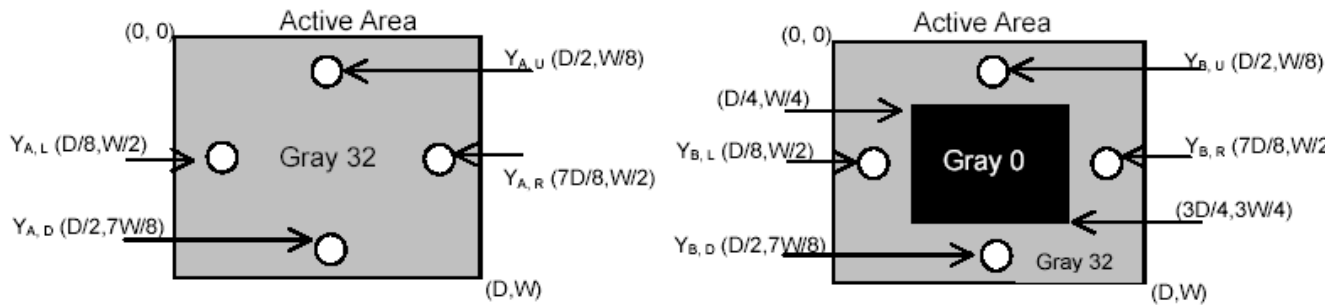
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.

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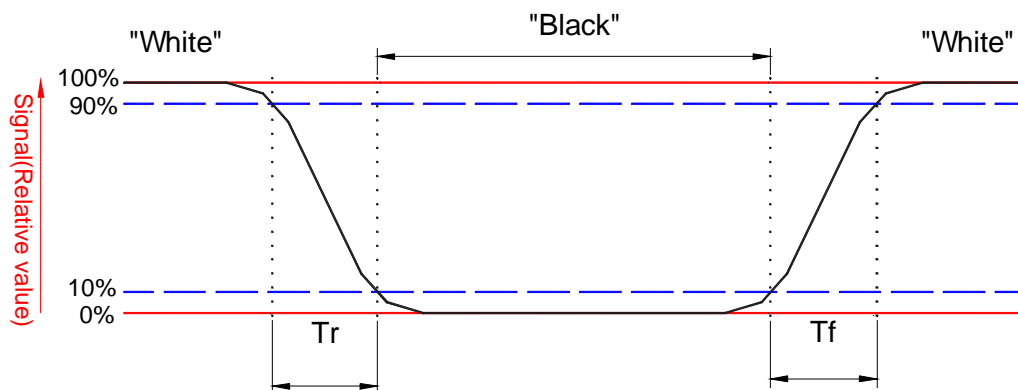
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.

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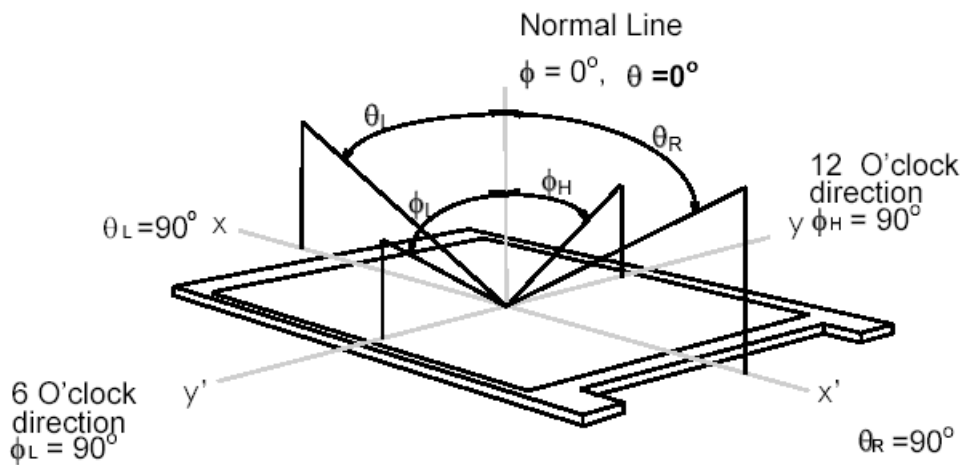
3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 40 Pin (One CH/connector Module)

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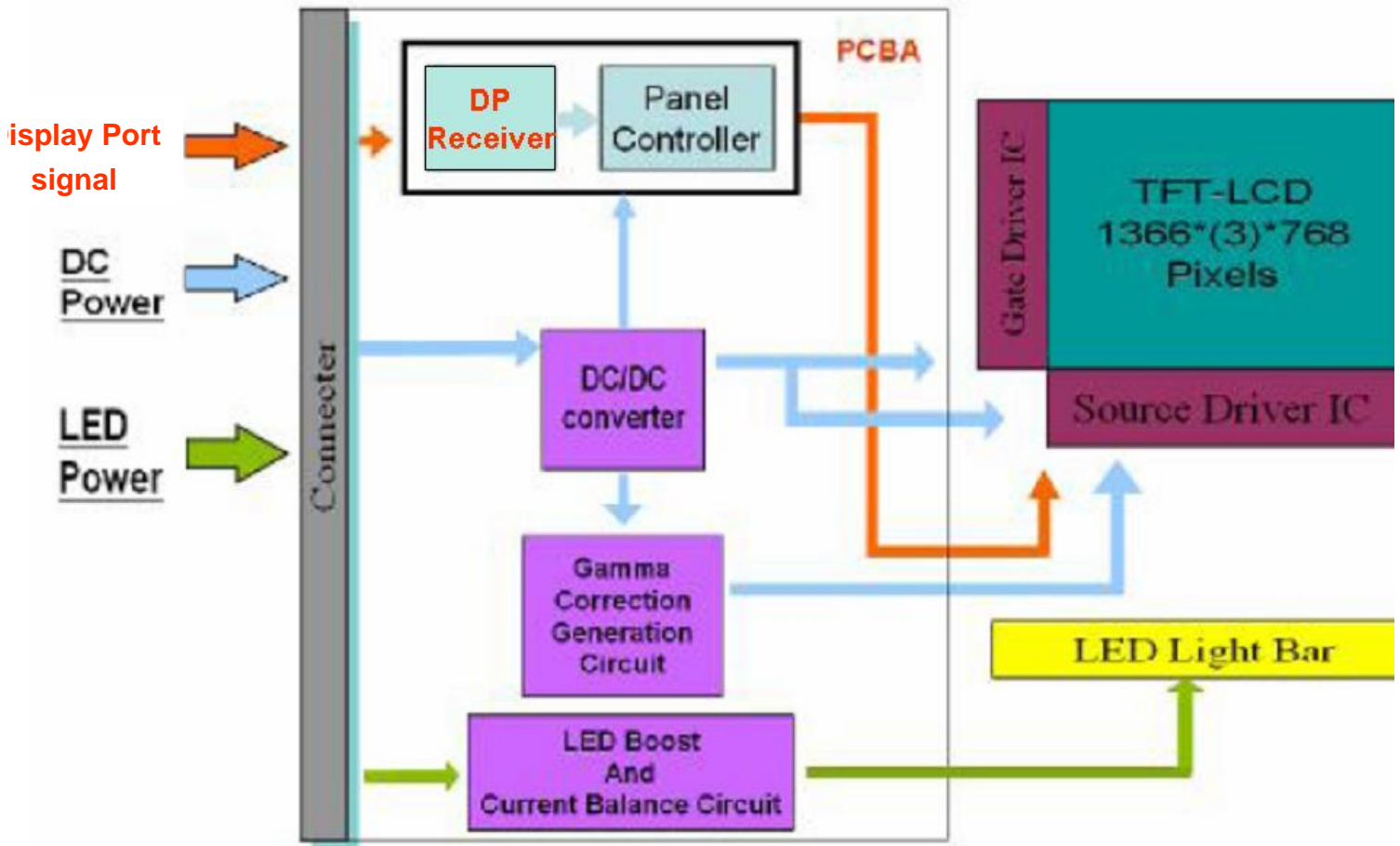
4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[^{o}C]	Note 4
Operation Humidity	HOP	10	90	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[^{o}C]	Note 4
Storage Humidity	HST	10	90	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).
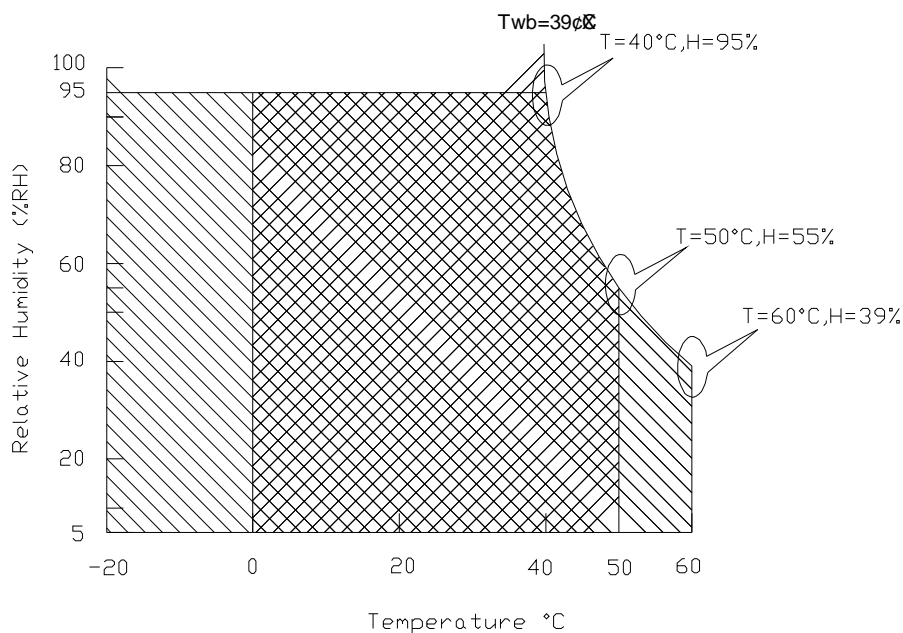
Operating Range   Storage Range

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5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	1.2	1.5	[Watt]	Note 1/2
IDD	IDD Current	-	333	364	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Typical Measurement Condition: Mosaic Pattern

Note 3 : Measure Condition
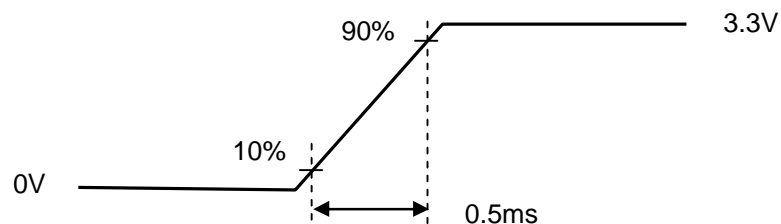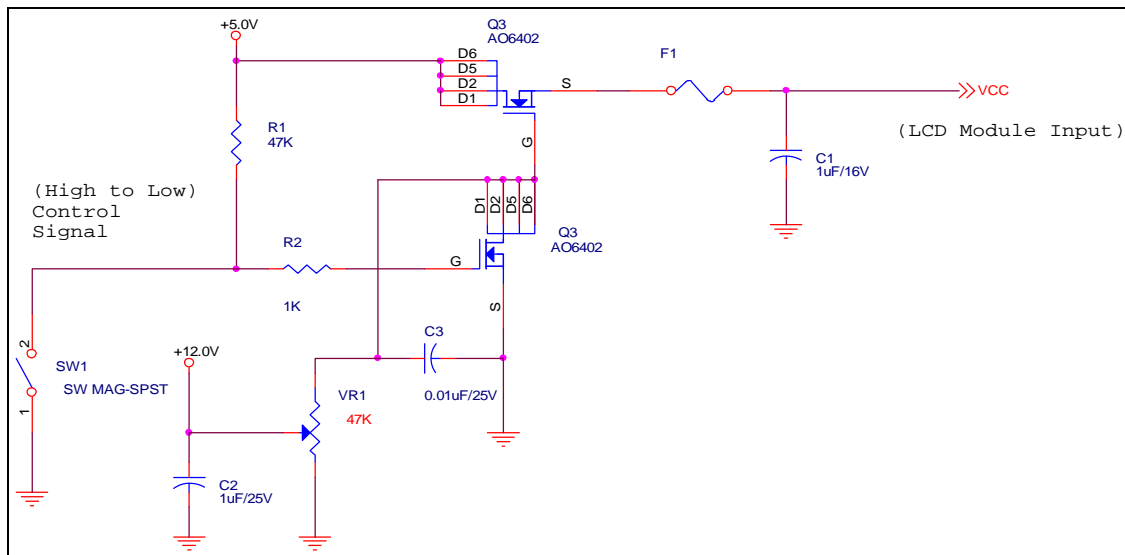
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Display Port main link signal:
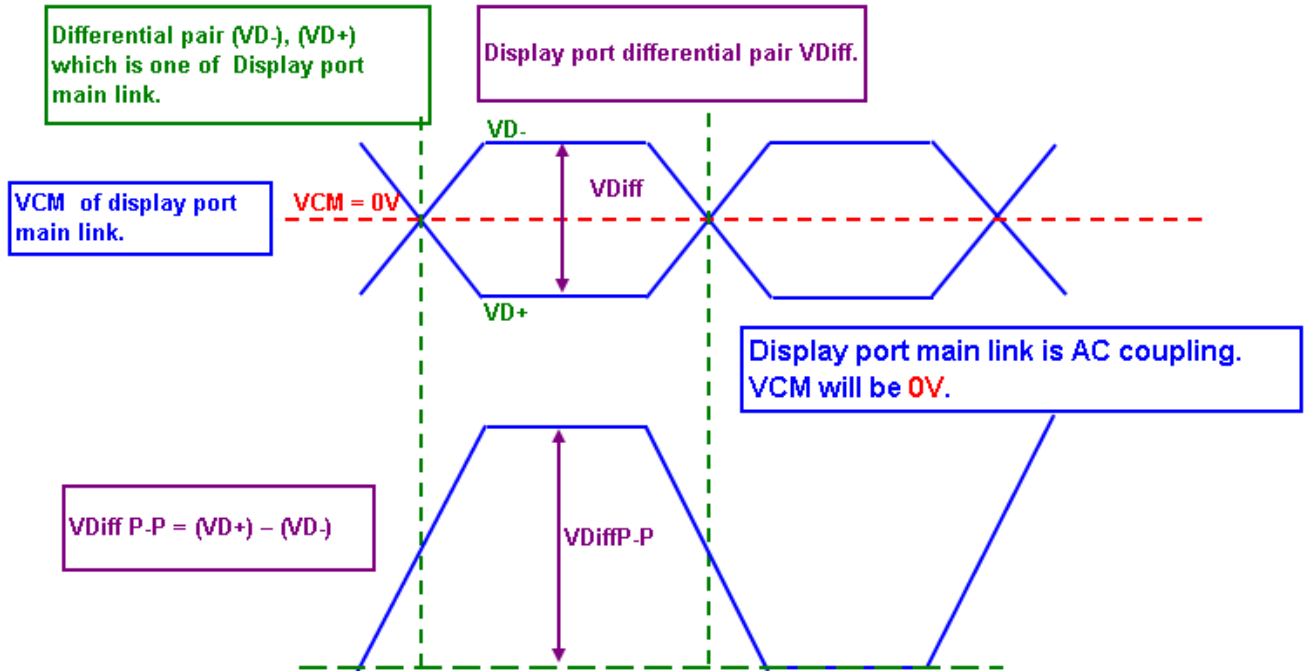
Display Port main link		Min	Typ	Max	unit
VCM	Differential common mode voltage	0.668	0.68	0.685	V
VDiffP-P level1	Differential peak to peak voltage level1	0.34	0.4	0.46	V
VDiffP-P level2	Differential peak to peak voltage level2	0.51	0.6	0.68	V
VDiffP-P level3	Differential peak to peak voltage level3	0.69	0.8	0.92	V
VDiffP-P level4	Differential peak to peak voltage level4	1.02	1.2	1.38	V

Fallow as VESA display port standard V1.1a.

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Display Port AUX_CH signal:
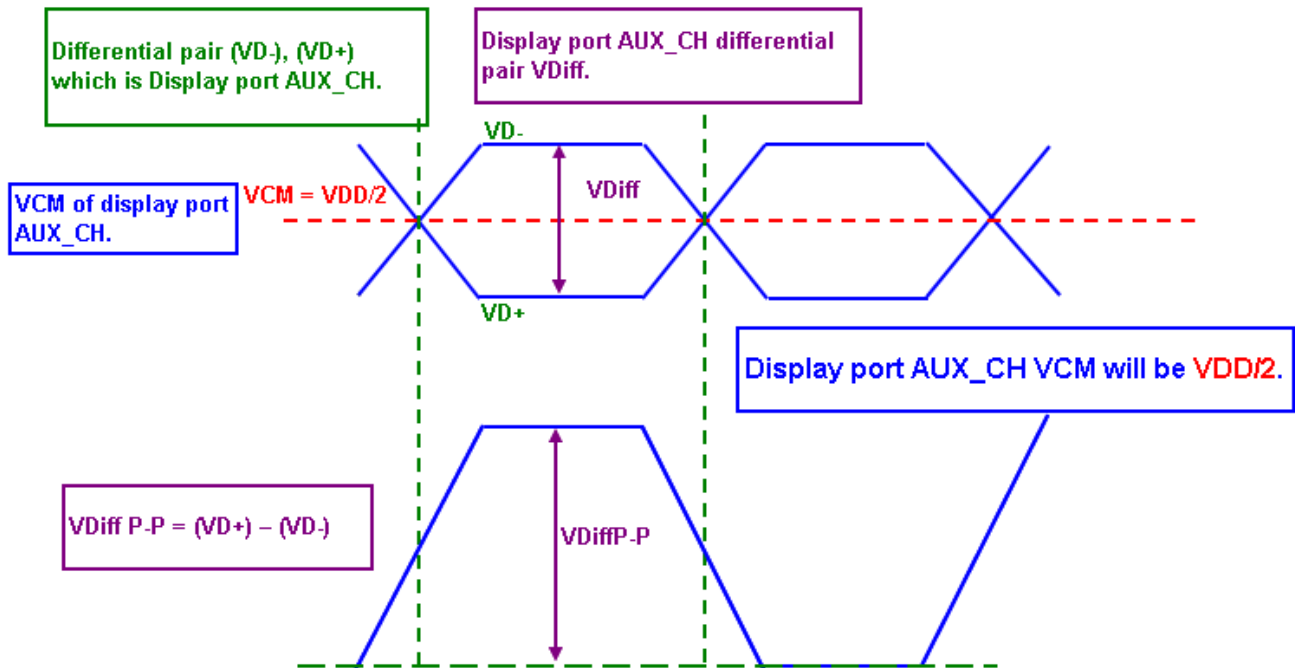
Display Port AUX_CH		Min	Typ	Max	unit
VCM	Differential common mode voltage	0	VDD/2	2	V
VDiffP-P	Differential peak to peak voltage	0.39		1.38	V

Fallow as VESA display port standard V1.1a.

Display Port VHPD **signal:**

Display Port VHPD		Min	Typ	Max	unit
VHPD	HPD voltage	2.25		3.6	V

Fallow as VESA display port standard V1.1a.

Display Port panel power sequence:
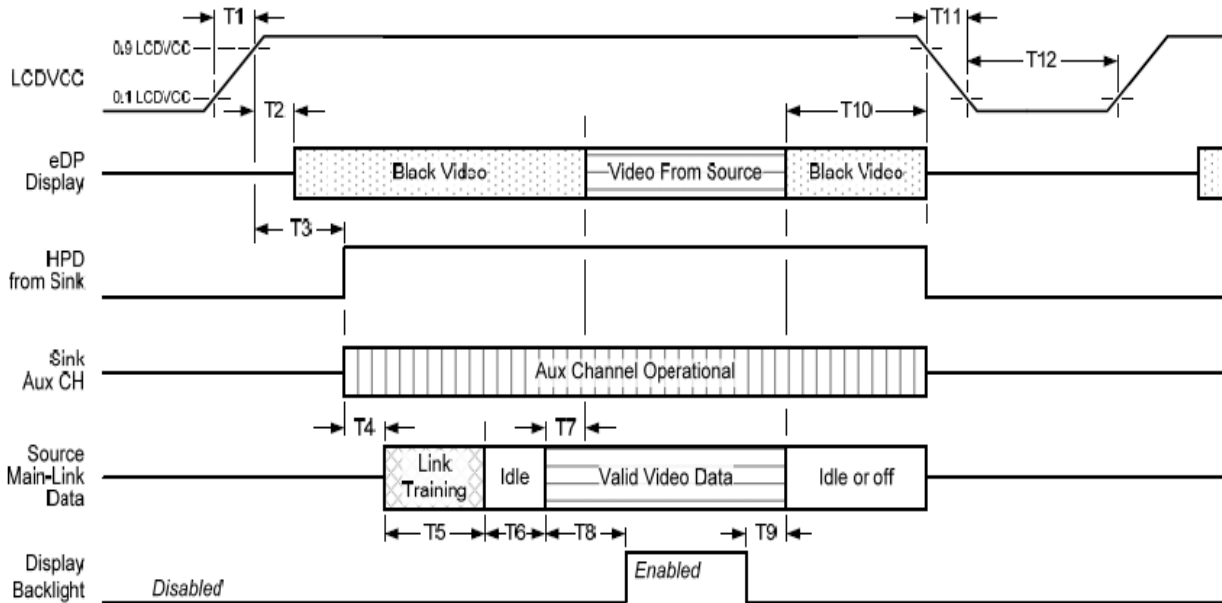
Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:

Display port interface power up/down sequence, AUX_CH transaction only

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Display Port panel power sequence timing parameter:

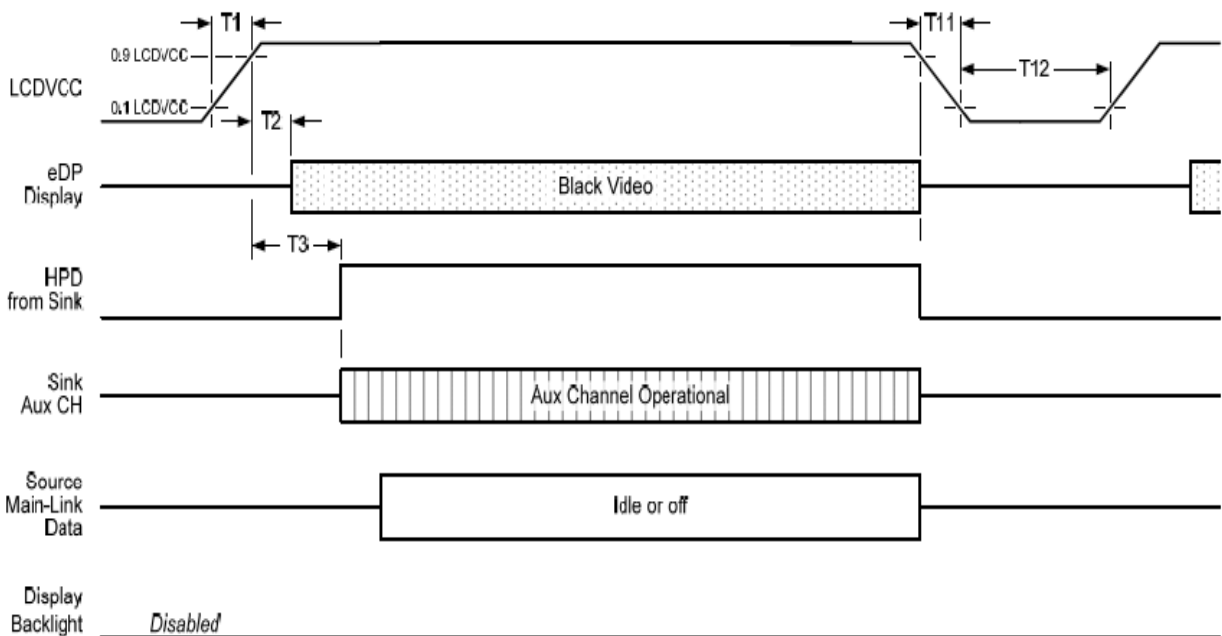| Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

5.2 Backlight Unit

LED Parameter guideline for LED driving selection (Ref. Remark 1)

Parameter	Symbol	Min	Typ	Max	Units	Condition
LED Forward Voltage	V_F	2.95	3.2	3.4	[Volt]	(Ta=25℃)
LED Forward Current	I_F		20	20.6	[mA]	(Ta=25℃)
LED Power consumption	P_{LED}		3.16	3.21	[Watt]	(Ta=25℃) Note 1
LED Driving Input Voltage	V_{LED}	6	12	21	[Volt]	
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25℃) I_F=20 mA Note 2
Output PWM frequency	F_{PWM}	100	200	20K	Hz	
Duty ratio	--	5	--	100	%	

Note 1: Calculator value for reference I_FxV_F =P

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

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6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

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6.3 Integration Interface and Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	Aging	LCD Panel Aging setting pin
2	NC	No Connection (reserved)
3	NC	No Connection (reserved)
4	NC	No Connection (reserved)
5	H_GND	High Speed Ground
6	Lane0_N	Complement Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Complement Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	Self Test or NC	Self Test (Optional in Sink device)
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	HPD or NC	HPD signal pin (Optional in Sink device)
18	BL_GND	Back light_ground
19	BL_GND	Back light_ground
20	BL_GND	Back light_ground
21	BL_GND	Back light_ground
22	BL_ENABLE	Backlight On/off
23	BL PWM DIM	System PWM signal input for dimming
24	NC-Reserved	Reserved for LCD manufacture's use
25	NC-Reserved	Reserved for LCD manufacture's use
26	BL_PWR	Backlight power (6V~21V)
27	BL_PWR	Backlight power (6V~21V)
28	BL_PWR	Backlight power (6V~21V)
29	BL_PWR	Backlight power (6V~21V)
30	NC	No Connection

Note1: Start from right side

SHIPPING LABEL

Connector IPEX20455-030-E2

30 ± 1

CONNECTOR KEEP OUT AREA
27 X 25mm

TBD

30

1
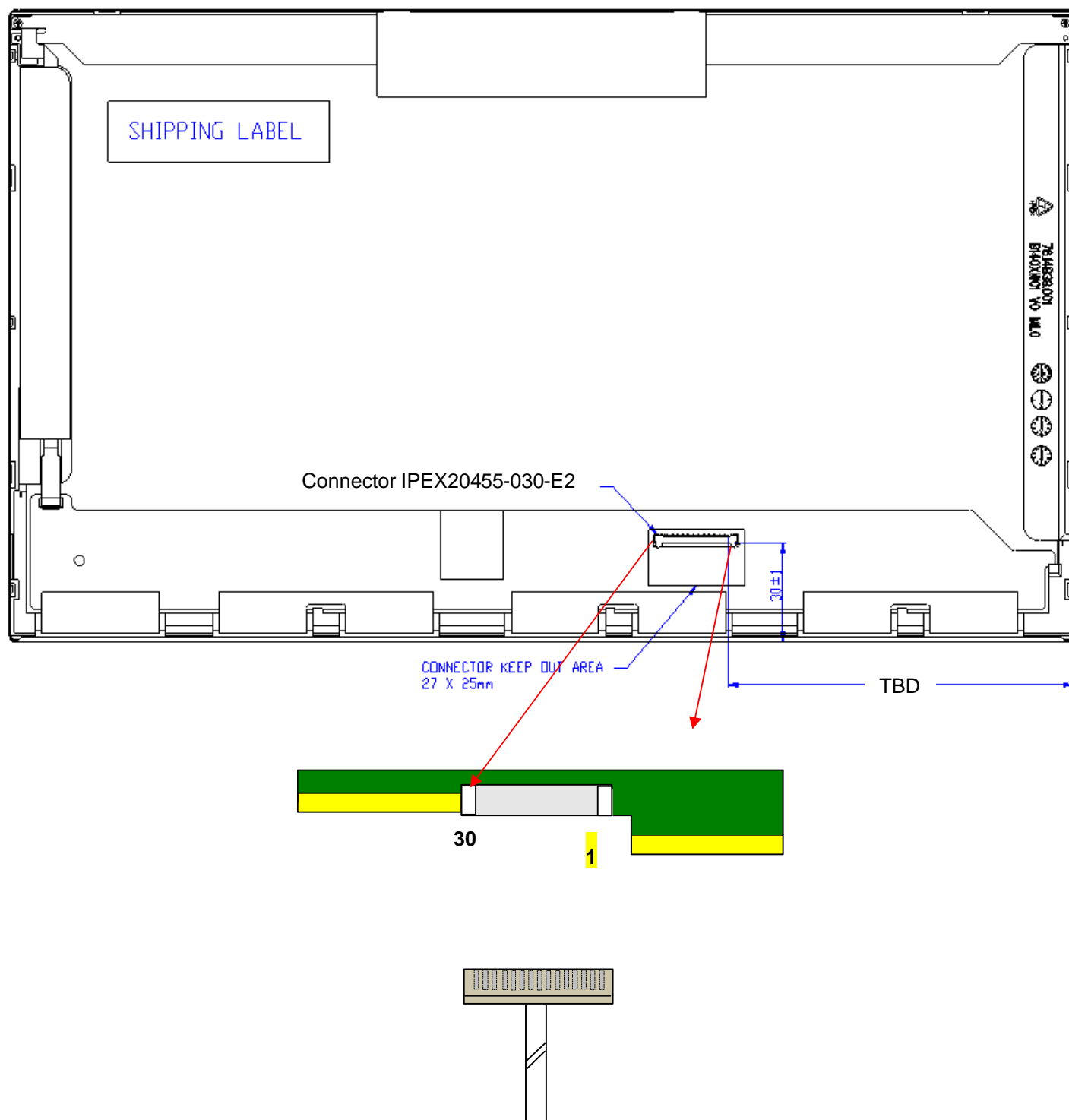
Note2: Input signals shall be low or High-impedance state when VDD is off.
internal circuit of **eDP inputs** are as following.

TCON Display Port Rx

6. Lane0-
7. Lane0+

9. AUX+
10. AUX-
17. HPD

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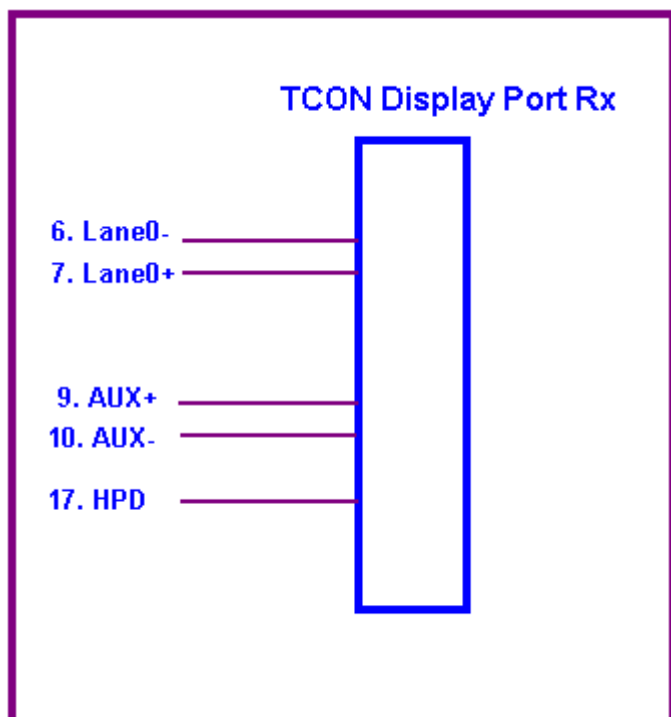
6.4 Interface Timing

6.4.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz   manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-50	60	-	Hz
Clock frequency		1/ T$_{Clock}$	-	69.3	-	MHz
Vertical Section	Period	T$_V$	776	808	1023	T$_{Line}$
	Active	T$_{VD}$		768		
	Blanking	T$_{VB}$	8	40	255	
Horizontal Section	Period	T$_H$	1396	1606	2047	T$_{Clock}$
	Active	T$_{HD}$		1366		
	Blanking	T$_{HB}$	30	240	681	

Note : DE mode only

6.4.2 Timing diagram

Input Timing Definition (DE Mode)

T$_{CLOCK}$

DOTCLK

Input Data

Invaild Data | Pixel 1 | Pixel 2 | Pixel 3 | Pixel N-1 | Pixel N | Invaild Data | Pixel 1

DE

T$_{HB}$ T$_{HD}$

T$_H$

DE

T$_{VB}$ T$_{VD}$

T$_V$
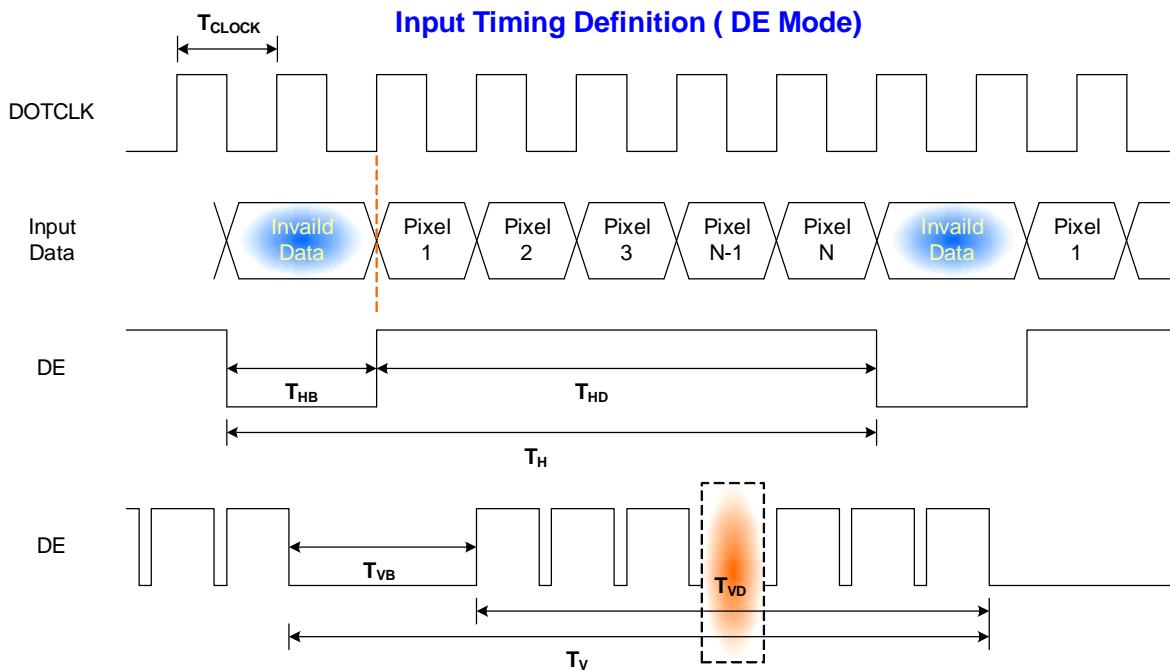
6.5 Power ON/OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off
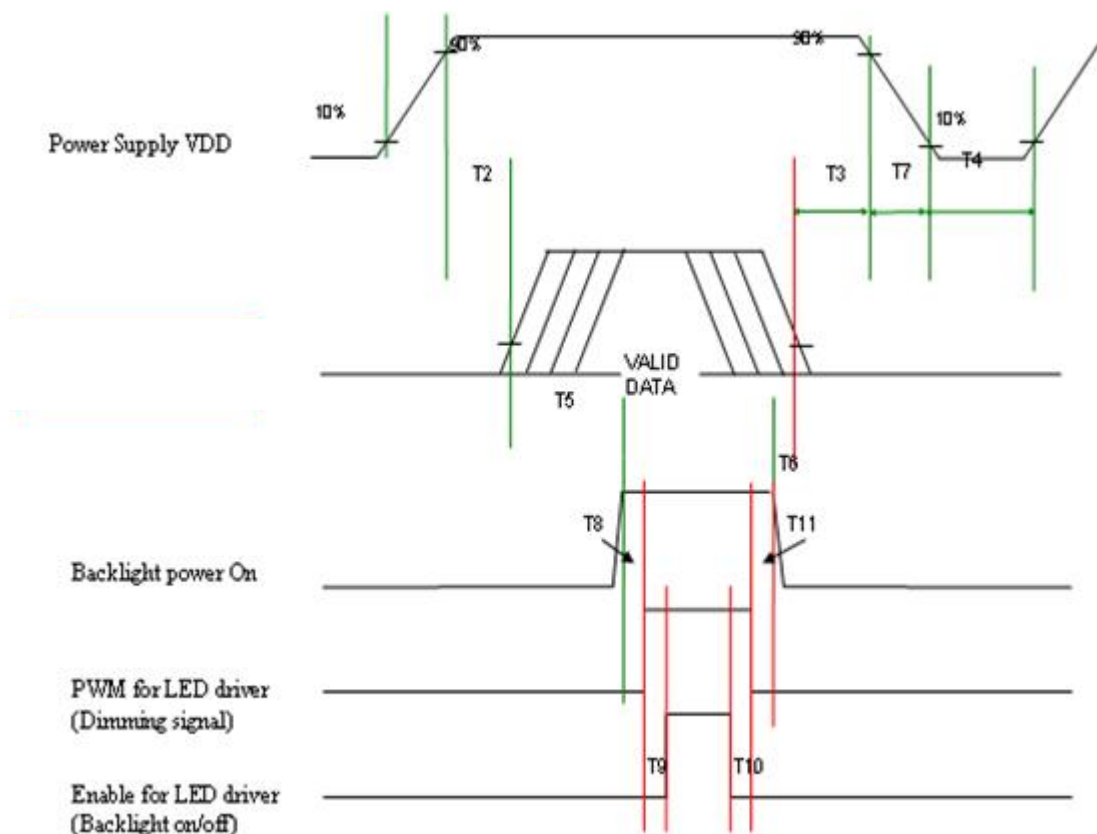
	Value			
Parameter	**Min.**	**Typ.**	**Max.**	**Units**
T1	0.5	-	10	(ms)
T2	5	-	50	(ms)
T3	0.5	-	50	(ms)
T4	400	-	-	(ms)
T5	300	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)
T8	10	---	---	(ms)
T9	10	---	---	(ms)
T10	0	---	---	(ms)
T11	10	---	---	(ms)

LED on/off sequence is as follows. Interface signals are also shown in the chart.
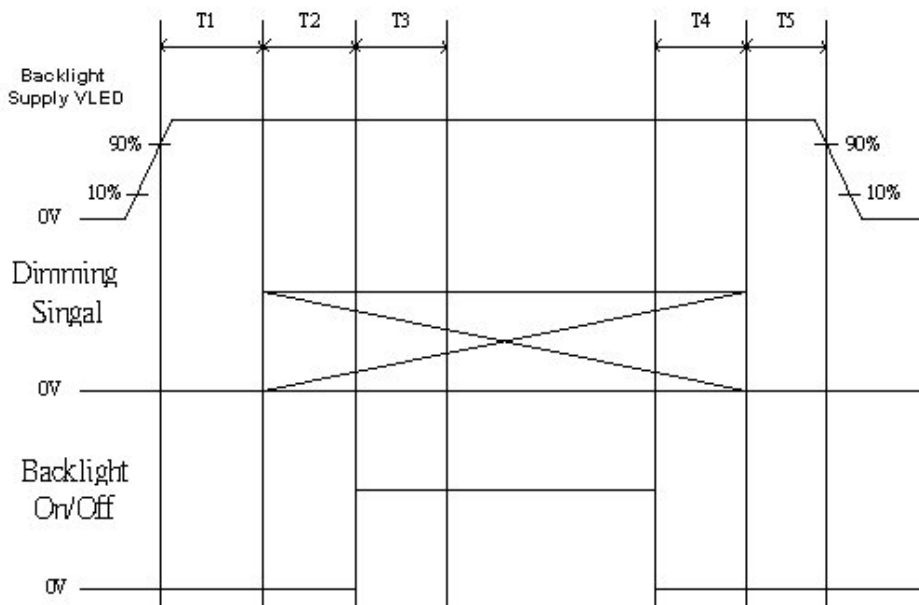
	Values			
Symbol	Min	Typ	Max	Unit
T1	10	---	---	
T2	10	---	---	
T3	50	---	---	ms
T4	0	---	---	
T5	10	---	---	

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	**IPEX**
Type / Part Number	**IPEX 20455-030E-02** or compatible
Mating Housing/Part Number	**IPEX 20453-030T-01** or compatible

8. LED Driving Specification

8.1 Connector Description

It is a intergrative interface and comibe into Display Port connector. The type and mating refer to section 7.

8.2 Pin Assignment

Ref. to 6.3

9. Vibration and Shock Test

9.1 Vibration Test

Test Spec:

- **l** Test method: Non-Operation
- **l** Acceleration: 1.5 G
- **l** Frequency: 10 - 500Hz Random
- **l** Sweep: 30 Minutes each Axis (X, Y, Z)

9.2 Shock Test Spec:

Test Spec:

- **l** Test method: Non-Operation
- **l** Acceleration: 220 G , Half sine wave
- **l** Active time: 2 ms
- **l** Pulse: X,Y,Z .one time for each side

10. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 300h	
Low Temperature Storage	Ta= -20°C, 250h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

. Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

11. Mechanical Characteristics

11.1 LCM Outline Dimension
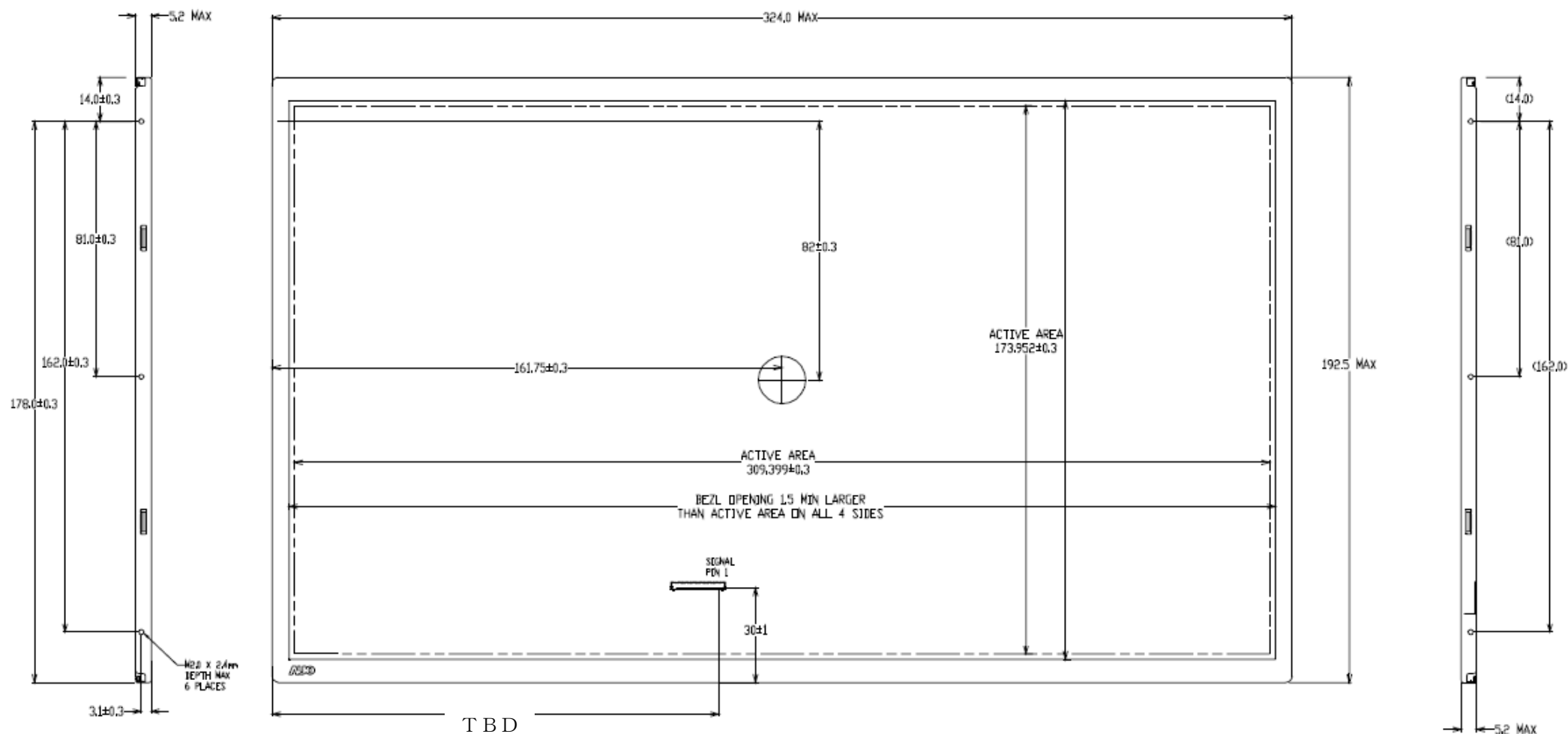
Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

11.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface = 2.35 mm (See drawing)

Screw hole center location, from front surface = 3.1 ± 0.2mm (See drawing)

Screw Torque: Maximum 2.5 kgf-cm
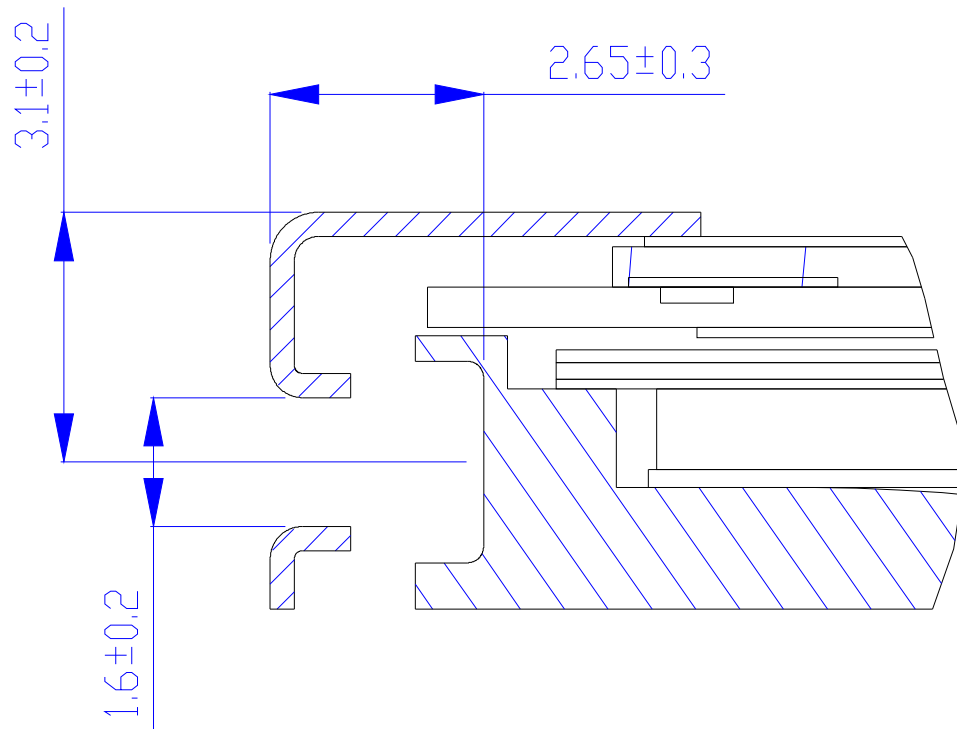
12. Shipping and Package

12.1 Shipping Label Format

Size :90 mm(length) ×35mm(width)

12.2 Carton package

Carton Label: 80mm * 40mm

AU Optronics   QTY: 25

MODEL NO: B140XW01V4   RoHS Pb

PART NO: 97.14B38.XXX

CUSTOMER NO: 533883-391

CARTON NO: [barcode]

Made in XXXXXX   *xxxxx−xxxxxxxxxx*

40

80
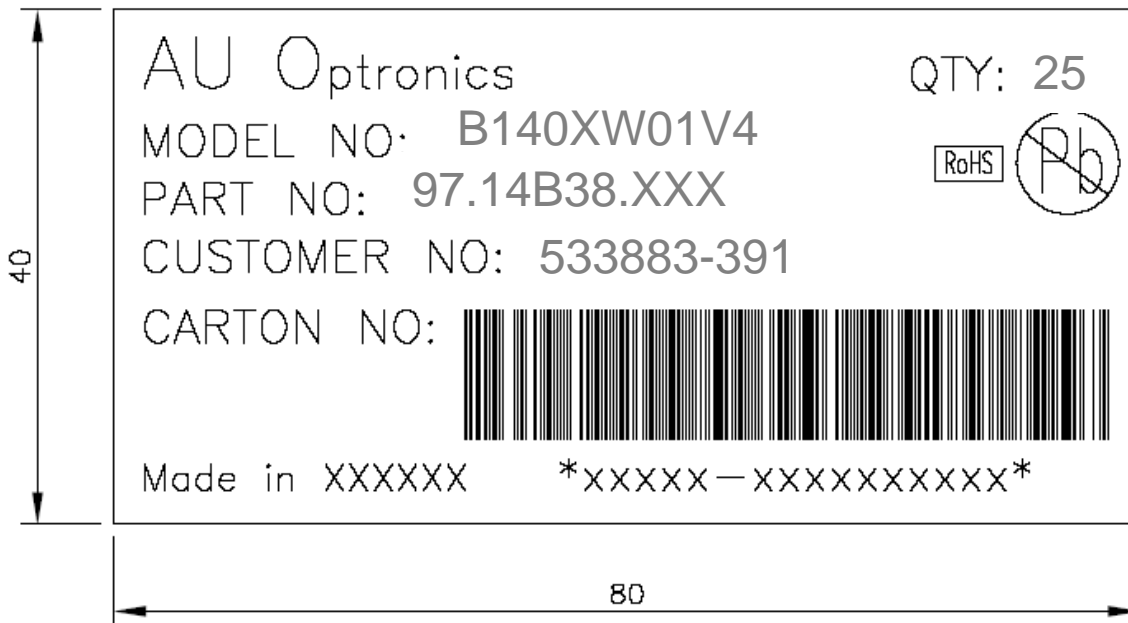
The outside dimension of carton is 454(L)mm* 376(W)mm* 302(H)mm, carton and cushion weight are 2200g

12.3 Shipping package of palletizing sequence

The outside dimension of Pallet is 114(L)mm* 83(W)mm* 13.8(H)mm

By air : 6 *4 layers, one pallet put 24 boxes, total 600 pcs module.

By sea : 6 *6 layers, one pallet put 36 boxes, total 900 pcs module.

Top cardboard

Stretch film

Label

PET band

Corner angle

Bottom cardboard

Wooden pallet

AU OPTRONICS CORPORATION

13. Appendix: EDID description

B140XW01 V4 EDID Code

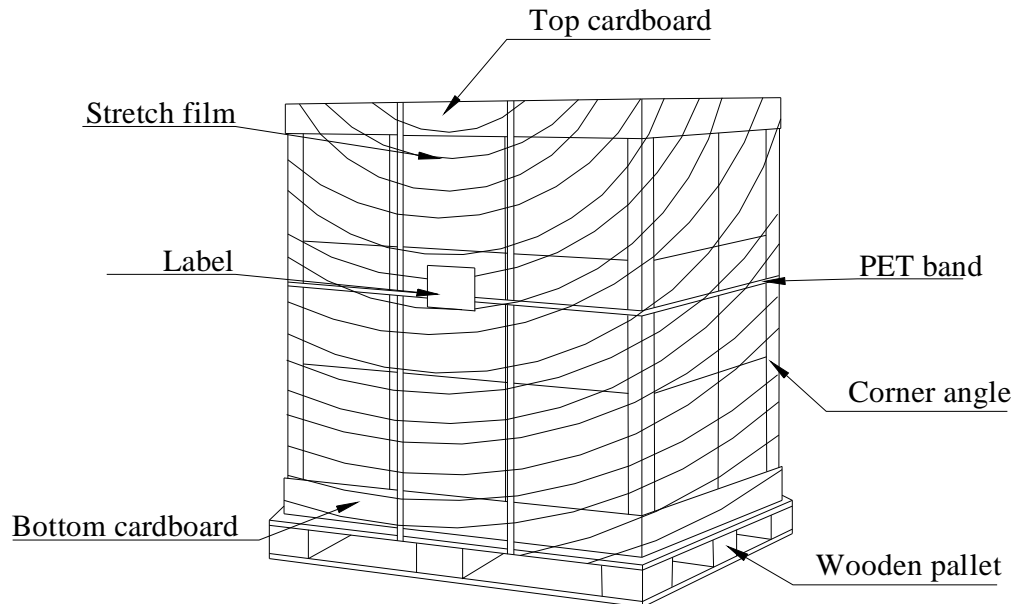| Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	3C	00111100	60
0B	hex, LSB first	14	00010100	20
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	00	00000000	0
11	Year of manufacture	13	00010011	19
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	04	00000100	4
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	95	10010101	149
15	**Max H image size** *(rounded to cm)*	1F	00011111	31
16	**Max V image size** *(rounded to cm)*	11	00010001	17
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2
19	Red/green low bits **(Lower 2:2:2:2 bits)**	45	01000101	69
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	25	00100101	37
1B	Red x **(Upper 8 bits)**	9C	10011100	156
1C	Red y/ highER 8 bits	5B	01011011	91
1D	Green x	55	01010101	85
1E	Green y	9C	10011100	156
1F	Blue x	27	00100111	39
20	Blue y	19	00011001	25
21	White x	50	01010000	80
22	White y	54	01010100	84

23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	12	00010010	18
37	Pixel Clock/10000 USB	1B	00011011	27
38	Horz active **Lower 8bits**	56	01010110	86
39	Horz blanking **Lower 8bits**	46	01000110	70
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	50	01010000	80
3B	Vertical Active **Lower 8bits**	00	00000000	0
3C	Vertical Blanking **Lower 8bits**	23	00100011	35
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30	00110000	48
3E	HorzSync. Offset	26	00100110	38
3F	HorzSync.Width	16	00010110	22
40	VertSync.Offset : VertSync.Width	36	00110110	54
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0
42	Horizontal Image Size **Lower 8bits**	35	00110101	53
43	Vertical Image Size **Lower 8bits**	AD	10101101	173
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0
46	Vertical Border *(zero for internal LCD)*	00	00000000	0
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24
48	Pixel Clock/10,000 (LSB)	0C	00001100	12
49	Pixel Clock/10,000 (MSB)	12	00010010	18

4A	Horizontal Addressable Pixels, lower 8 bits	56	01010110	86
4B	Horizontal Blanking Pixels, lower 8 bits	46	01000110	70
4C	H Pixels, upper nibble : H Blanking, upper nibble	50	01010000	80
4D	Vertical Addressable Lines, lower 8 bits	00	00000000	0
4E	Vertical Blanking Lines, lower 8 bits	23	00100011	35
4F	V lines, upper nibble : V blanking, upper nibble	30	00110000	48
50	Horizontal Front Porch, lower 8 bits	26	00100110	38
51	Horizontal Sync Pulse, lower 8 bits	16	00010110	22
52	V Front Porch, lower nibble : V Sync Pulse, lower nibble	36	00110110	54
53	VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits	00	00000000	0
54	Horizontal Image Size in mm, lower 8 bits	35	00110101	53
55	Vertical Image Size in mm, lower 8 bits	AD	10101101	173
56	H Image Size, upper nibble : V Image Size, upper nibble	10	00010000	16
57	Horizontal Border	00	00000000	0
58	Vertical Border	00	00000000	0
59	Bit Encode Sync Information	18	00011000	24
5A	DC	00	00000000	0
5B	HTOTAL	00	00000000	0
5C	HA	00	00000000	0
5D	HBL	00	00000000	0
5E	HFP	00	00000000	0
5F	HFPe	00	00000000	0
60	HBP	00	00000000	0
61	HB	00	00000000	0
62	HSO	00	00000000	0
63	HS	00	00000000	0
64	VTOTAL	00	00000000	0
65	VA	00	00000000	0
66	VBL	00	00000000	0
67	VFP	00	00000000	0
68	VBP	00	00000000	0
69	VB	00	00000000	0
6A	VSO	00	00000000	0
6B	VS	00	00000000	0
6C	Detail Timing Description #4	00	00000000	0
6D	Flag	00	00000000	0
6E	Reserved	00	00000000	0
6F	For Brightness Table and Power Consumption	02	00000010	2
70	Flag	00	00000000	0

71	PWM % [7:0] @ Step 0	0C	00001100	12
72	PWM % [7:0] @ Step 5	45	01000101	69
73	PWM % [7:0] @ Step 10	E8	11101000	232
74	Nits [7:0] @ Step 0	0B	00001011	11
75	Nits [7:0] @ Step 5	3C	00111100	60
76	Nits [7:0] @ Step 10	64	01100100	100
77	Panel Electronics Power @ 32x32 Chess Pattern =	12	00010010	18
78	Backlight Power @ 60 nits =	12	00010010	18
79	Backlight Power @ Step 10 =	1D	00011101	29
7A	Nits @ 100% PWM Duty =	6E	01101110	110
7B	Flag	20	00100000	32
7C	Flag	20	00100000	32
7D	Flag	20	00100000	32
7E	Extension Flag	00	00000000	0
7F	Checksum	AE	10101110	174
			SUM	5376