**Version: 0.7**

# Technical Specification

**MODEL NO: SA1452-FOA ( EC060KH1 )**

The content of this information is subject to be changed without notice.

Please contact E Ink or its agent for further information.

☐Customer's Confirmation

Customer

Date

By

☐E Ink's Confirmation

Approved By

Confirmed By

Prepared By

# Revision History

| Rev. | Issued Date | Revised Contents |
|---|---|---|
| 0.1 | 2019-07-30 | New |
| 0.2 | 2019-08-08 | 1. Re-layout FL FPC to keep same shape with ED060XH9<br>2. Modify item 7 description |
| 0.3 | 2019-11-22 | 1. Modify thickness due to structure<br>2. Modify figure<br>3. Modify LED number |
| 0.4 | 2020-01-09 | 1. Update model No<br>2. Correct some words |
| 0.5 | 2020-02-27 | 1. Add pixel arrangement, optical characteristics & reliability test |
| 0.6 | 2020-03-10 | 1. Modified TP description |
| 0.7 | 2020-04-16 | 1. Modified EE description<br>2. Modified TP description<br>3. Modified drawing<br>4. Combine TP & EE characteristic description |

# TECHNICAL SPECIFICATION

## CONTENTS

## 1. Application

SA1452-FOA is a color, reflective electrophoretic E Ink® technology display module. It is based on active matrix TFT substrate, featuring capacitive touch panel and front light and color component. It has 6" active area, the display is capable to display images at 2-16 gray levels (1-4 bits) depending on the display controller and the associated waveform file it used.

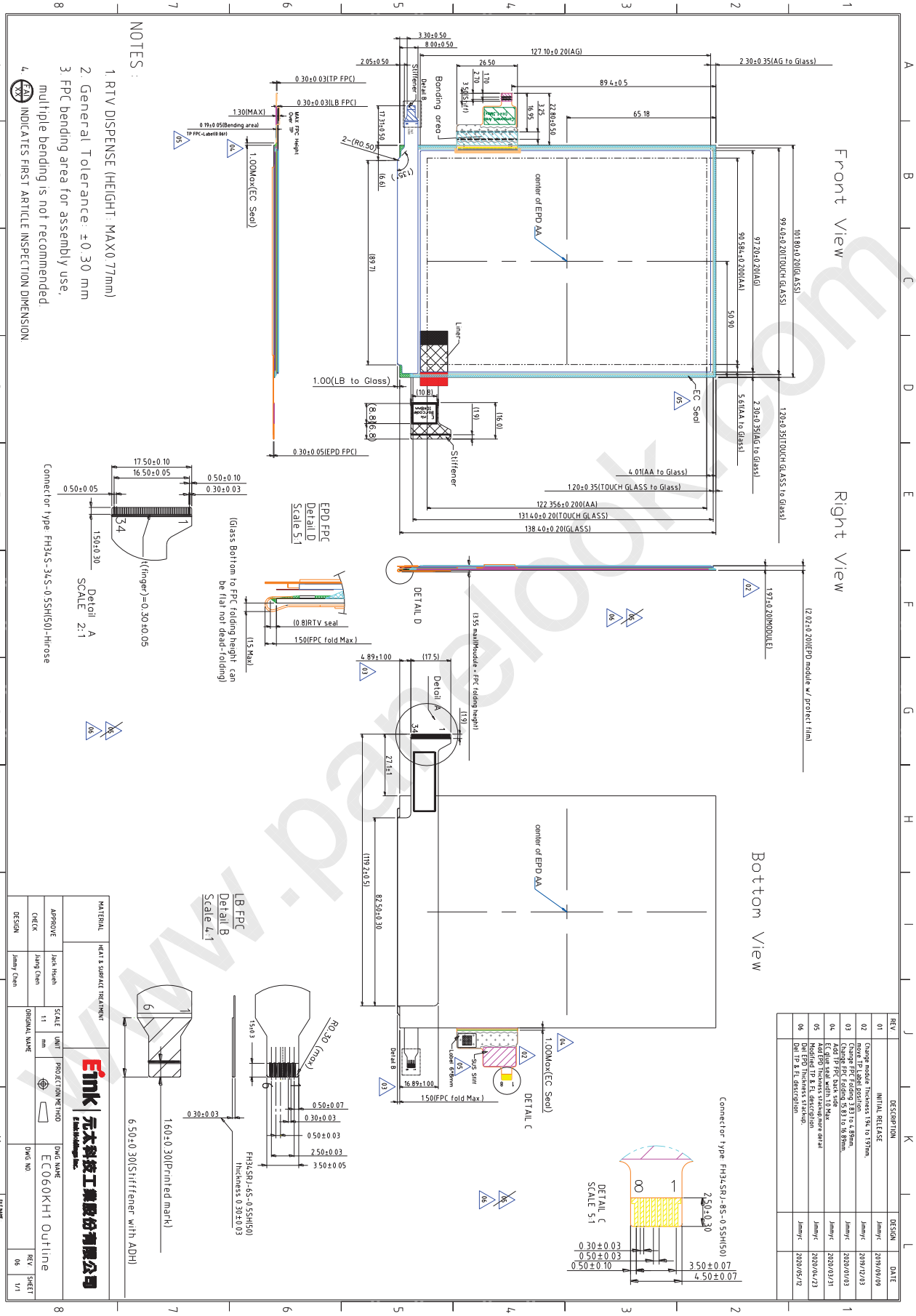
## 2. Features

- High contrast reflective/electrophoretic technology
- Color display
- Glass TFT
- Capacitive touch
- Front light module
- Bi-stable
- Portrait mode
- AG film surface
- Commercial temperature range

## 3. Mechanical Specifications

| Parameter | Specifications | Unit | Remark |
|---|---|---|---|
| Screen Size | 6 (3:4 diagonal) | Inch | |
| Display Resolution | 357 (H)×482 (V) color<br>1072 (H)×1448 (V) color | Pixel | 300dpi B/W<br>100dpi color |
| Display color | 4096 | - | |
| Active Area | 90.6(H)×122.4 (V) | mm | |
| Pixel Pitch | 0.0845(H)x0.0845(V) | mm | |
| Outline Dimension | 101.8 (W)×138.4 (H)×1.97 (D) | mm | |
| Module Weight | 47.0 ± 5 | g | |
| Number of Gray | 16 Gray Level (monochrome) | | |

## 4. Mechanical Drawing of EPD Module



## 5. Output Interface

### 5-1) Recommended Connector Type of Panel

FH34S-34S-0.5SH(50)

### 5-2) Pin Assignment of Panel

| Pin # | Signal | I/O | Description | Remark |
|---|---|---|---|---|
| 1 | VSL | P | Negative power supply source driver | Note1 |
| 2 | VGL | P | Negative power supply gate driver | Note1 |
| 3 | VSS | P | Ground | Note1 |
| 4 | NC | - | No Connection | |
| 5 | NC | - | No Connection | |
| 6 | VDD | P | Digital power supply drivers | Note1 |
| 7 | VSS | P | Ground | Note1 |
| 8 | CKH | I | Clock source driver | |
| 9 | VSS | P | Ground | Note1 |
| 10 | LEH | I | Latch enable source driver | |
| 11 | OEH | I | Output enable source driver | |
| 12 | SPH | I | Start pulse source driver | |
| 13 | D0 | I | Data signal source driver(LSB) | |
| 14 | D1 | I | Data signal source driver | |
| 15 | D2 | I | Data signal source driver | |
| 16 | D3 | I | Data signal source driver | |
| 17 | D4 | I | Data signal source driver | |
| 18 | D5 | I | Data signal source driver | |
| 19 | D6 | I | Data signal source driver | |
| 20 | D7 | I | Data signal source driver(MSB) | |
| 21 | VCOM | P | Common voltage | Note1 |
| 22 | NC | - | No Connection | |
| 23 | NC | - | No Connection | |
| 24 | NC | - | No Connection | |
| 25 | NC | - | No Connection | |
| 26 | VSS | P | Ground | Note1 |
| 27 | OEV | I | Output mode selection gate driver | |
| 28 | CKV | I | Clock gate driver | |
| 29 | SPV | I | Start pulse gate driver | |
| 30 | NC | - | No Connection | |
| 31 | Border | I | Border connection | |
| 32 | VSS | P | Ground | Note1 |
| 33 | VSH | P | Positive power supply source driver | Note1 |
| 34 | VGH | P | Positive power supply gate driver | Note1 |

**Note1: P Power pin**

**5-3) Recommended Connector Type of Front Light**

FH34SRJ-6S-0.5SH(50)

**5-4) Pin Assignment of Front Light**

| Pin # | Signal | I/O | Description | Remark |
|---|---|---|---|---|
| 1 | Anode | P | For circuit 01 | Note1 |
| 2 | Anode | P | For circuit 02 | Note1 |
| 3 | NC | - | No Connection | |
| 4 | NC | - | No Connection | |
| 5 | Cathode | P | For circuit 01 | Note1 |
| 6 | Cathode | P | For circuit 02 | Note1 |

**Note1: P Power pin**

**Circuit 01 :1/3/5/7/9/11(series)**

**Circuit 02:2/4/6/8/10/12(series)**

**5-5) Recommended Connector Type of Touch Panel**

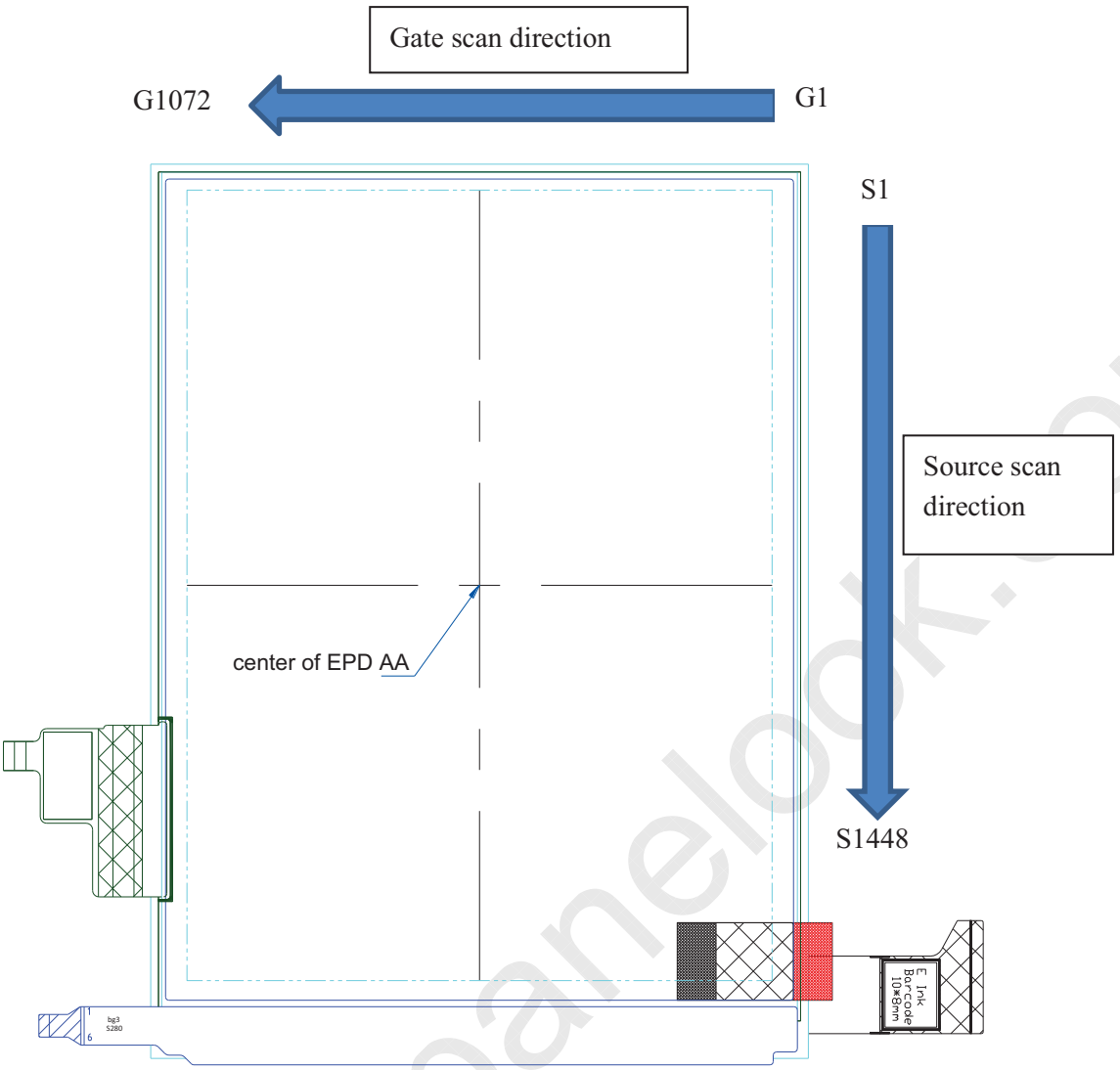
FH34SRJ-8S-0.5SH(50)

**5-6) Pin Assignment of Touch Panel**

| Pin# | Signal | I/O | Description | Remark |
|---|---|---|---|---|
| 1 | GND | P | Ground | Note1 |
| 2 | NC | - | No Connection | |
| 3 | XRES | I | Reset pin from mainboard to IC 3.3V digital I/O | Request pull high resistor 10K ohm for Reset by Host |
| 4 | INT | I/O | Interrupt pin from IC to mainboard 3.3V digital I/O | Pre-layout pull high resistor pad for INT by Host |
| 5 | SDA | I/O | I2C data pin to Parade touch IC 3.3V digital I/O | Request pull high resistor 4.7K ohm for SDA by Host |
| 6 | SCL | I/O | I2C clock pin to Parade touch IC 3.3V digital I/O | Request pull high resistor 4.7K ohm for SCL by Host |
| 7 | NC | - | No Connection | |
| 8 | $V_{DD}$_TP | P | Power Supply DC 2.8~3.4V | Note1 |

**Note1: P Power pin**

### 5-7) Panel Scan Directions




### 5-8)the relationship of input data and output

| Output | S1 | S2 | S3 | S4 |
|---|---|---|---|---|
| Data | D7 | D5 | D3 | D1 |
| | D6 | D4 | D2 | D0 |

## 6. Electrical Characteristics

### 6-1) Absolute Maximum Ratings of panel only:

| Parameter | Symbol | Rating | Unit | Remark |
|---|---|---|---|---|
| Logic Supply Voltage | VDD | -0.3 to +5.0 | V | -- |
| Positive Supply Voltage | $V_{SH}$ | -0.3 to +18.0 | V | -- |
| Negative Supply Voltage | $V_{SL}$ | +0.3 to -18.0 | V | -- |
| Max .Drive Voltage Range | $V_{SH} - V_{SL}$ | 36.0 | V | -- |
| Supply Voltage | VGH | -0.3 to VGL+50.0 | V | -- |
| Supply Voltage | VGL | -25.0 to +0.3 | V | -- |
| Supply Range | VGH-VGL | 10.0 to +45.0 | V | -- |
| Operating Temp. Range | TOTR | 0 to +50 | ℃ | -- |
| Storage Temperature | TSTG | TBD | ℃ | -- |

### 6-2) Panel DC Characteristics (Note. 1)

| Parameter | Symbol | Conditions | Min | Typ(Note 3) | Max(Note 2) | Unit |
|---|---|---|---|---|---|---|
| Signal ground | $V_{SS}$ | | - | 0.0 | - | V |
| Logic Voltage supply | $V_{DD}$ | | 1.7 | 1.8 | 2.1 | V |
| | $I_{VDD(B/W)}$ | $V_{DD}$=1.8V | - | 1.6 | 4.2 | mA |
| | $I_{VDD(COLOR)}$ | $V_{DD}$=1.8V | - | 3.4 | 4.2 | mA |
| | $V_{DD}$ | | 3.0 | 3.3 | 3.6 | V |
| | $I_{VDD(B/W)}$ | $V_{DD}$=3.3V | - | 6.2 | 8.2 | mA |
| | $I_{VDD(COLOR)}$ | $V_{DD}$=3.3V | | 6.5 | 8.2 | mA |
| Gate Negative supply | VGL | | -21.0 | -20.0 | -19.0 | V |
| | $I_{GL(B/W)}$ | VGL = -20V | - | 0.8 | 10.0 | mA |
| | $I_{GL(COLOR)}$ | VGL = -20V | | 4.5 | 10.0 | mA |
| Gate Positive supply | VGH | | 24.0 | 25.0 | 26.0 | V |
| | $I_{GH(B/W)}$ | VGH = 25V | - | 0.7 | 1.7 | mA |
| | $I_{GH(COLOR)}$ | VGH = 25V | | 1.1 | 1.7 | mA |
| Source Negative supply | $V_{SL}$ | | -15.4 | -15.0 | -14.6 | V |
| | $I_{SL(B/W)}$ | $V_{SL}$ = -15V | - | 1.7 | 113.0 | mA |
| | $I_{SL(COLOR)}$ | $V_{SL}$ = -15V | | 40.0 | 113.0 | mA |
| Source Positive supply | $V_{SH}$ | | 14.6 | 15.0 | 15.4 | V |
| | $I_{SH(B/W)}$ | $V_{SH}$ = 15V | - | 1.8 | 113.0 | mA |
| | $I_{SH(COLOR)}$ | $V_{SH}$ = 15V | | 48.0 | 113.0 | mA |
| Border supply | $V_{COM}$ | | -4.0 | Adjusted | -0.2 | V |
| Asymmetry source | $V_{Asym}$ | $V_{SH}$+VSL | -800.0 | 0.0 | 800.0 | mV |
| Common voltage | $V_{COM}$ | | -4.0 | Adjusted | -0.2 | V |
| | $I_{COM}$ | | - | 0.2 | - | mA |
| Panel Power | $P_{(B/W)}$ | $V_{DD}$=1.8V | - | 89.0 | 3640.0 | mW |

| | | | | | | |
|---|---|---|---|---|---|---|
| | $P_{(COLOR)}$ | $V_{DD}$=1.8V | | 1444.0 | 3640.0 | mW |
| | $P_{(B/W)}$ | $V_{DD}$=3.3V | | 107.0 | 3660.0 | mW |
| | $P_{(COLOR)}$ | $V_{DD}$=3.3V | | 1459.0 | 3660.0 | mW |
| Standby power panel (Note 4) | $P_{STBY}$ | | - | - | 1.3 | mW |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Maximum Currents (Note 5) | ISH | $V_{SH}$ = 15V | - | | 420.0 | mA |
| | ISL | $V_{SL}$ = -15V | - | | 388.0 | mA |
| | IGH | $V_{GH}$ = 25V | - | | 39.0 | mA |
| | IGL | $V_{GL}$ =-20V | - | | 293.0 | mA |
| | ICOM | -- | - | | 224.0 | mA |

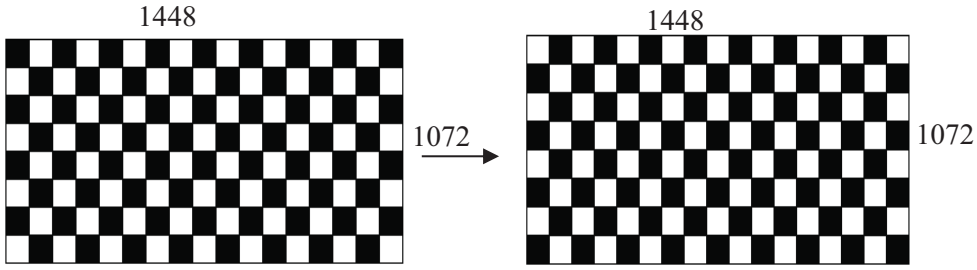
| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Digital Input “H” voltage | VIH | -- | 0.8VDD | | VDD | V |
| Digital Input “L” voltage | VIL | -- | GND | | 0.2VDD | V |

Note :

1. The power consumption in this field is provided for the purpose as the follows:
   1-1. The selection of suitable PMIC in the market to drive EPD normally.
   1-2. Estimation of voltage-drop at input side of PMIC for setting of threshold-voltage of battery.
2. The maximum average Currents for power consumption are measured using 85 Hz waveform with following pattern transition in both B/W and color condition: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
3. The Typical average current for power consumption is measured using 85 Hz waveform with following pattern transition:
   3-1. For displaying with grayscale image, it is from horizontal 4 gray scale pattern to vertical 4 gray scale pattern without dithering process. (Note 6-2)
   3-2. For displaying with color image, it is from horizontal 8 color pattern to vertical 8 color pattern without dithering process. (Note 6-3)
4. The standby power is the consumed power when the panel controller is in standby mode.
5. The Maximum Currents are measured using 85 Hz waveform with following pattern transition in both B/W and color condition: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
   - It is performed with decoupling capacitors on each power rail as below table (Note 6-4).
   - The minimum value in table of Maximum current is produced by charging mechanism between decoupling capacitors.
6. The listed electrical/optical characteristics are only guaranteed under the controller and waveform provided by E Ink.
7. Vcom is recommended to be set in the range of assigned value ± 0.1 V
8. Use of measuring instruments: Oscilloscope (Model: Tektronix MDO3054)

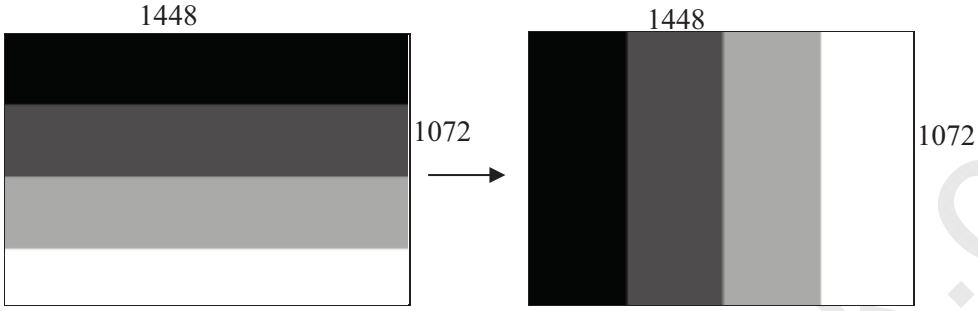
Note6-1

The maximum average current and Maximum Currents for B/W and Color displays



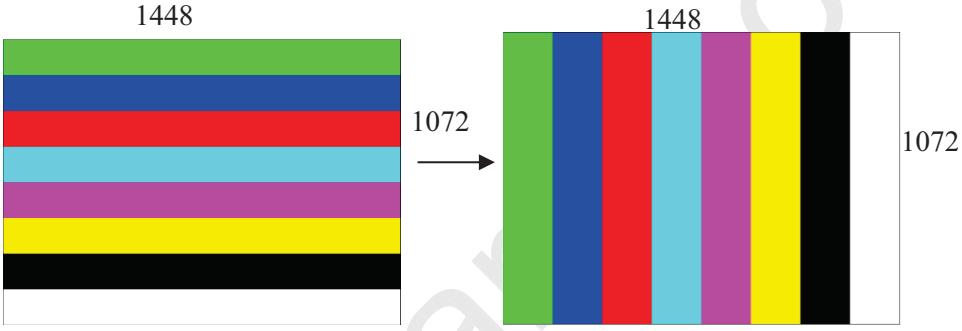

Note6-2

The typical power consumption for B/W display




Note6-3

The typical power consumption at color display




Note6-4

The decoupling capacitors on each power rail for Max. Currents

| Power rail | Capacitors suggested ( uF / Tolerance) |
|---|---|
| ISH | 4.7uF x 2pcs / ±10% |
| ISL | 4.7uF x 2pcs / ±10% |
| IGH | 2.2 uF x 1 pcs / ±10% |
| IGL | 4.7uF x 1 pcs / ±10% |
| IDD | 4.7uF x 1 pcs / ±10% |

**6-3) Panel DC Characteristics for Device Battery-Life Estimation (Note.1)**

| Parameter | Symbol | Conditions | Min | Typ(Note 3) | Max(Note 2) | Unit |
|---|---|---|---|---|---|---|
| Signal ground | $V_{SS}$ | | - | 0.0 | - | V |
| Logic Voltage supply | $V_{DD}$ | | 1.7 | 1.8 | 2.1 | V |
| | $I_{VDD(B/W)}$ | $V_{DD}$=1.8V | - | 0.8 | 4.0 | mA |
| | $I_{VDD(COLOR)}$ | $V_{DD}$=1.8V | | 3.6 | 4.0 | mA |
| | $V_{DD}$ | | 3.0 | 3.3 | 3.6 | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | $I_{VDD(B/W)}$ | $V_{DD}$= 3.3V | | 3.9 | 6.0 | mA |
| | $I_{VDD(COLOR)}$ | $V_{DD}$= 3.3V | - | 5.4 | 6.0 | mA |
| Gate Negative supply | VGL | | -21.0 | -20.0 | -19.0 | V |
| | $I_{GL(B/W)}$ | VGL = -20V | - | 2.0 | 9.6 | mA |
| | $I_{GL(COLOR)}$ | VGL = -20V | | 1.5 | 9.6 | mA |
| Gate Positive supply | VGH | | 24.0 | 25.0 | 26.0 | V |
| | $I_{GH(B/W)}$ | VGH = 25V | - | 0.7 | 0.8 | mA |
| | $I_{GH(COLOR)}$ | VGH = 25V | | 0.8 | 0.8 | mA |
| Source Negative supply | $V_{SL}$ | | -15.4 | -15.0 | -14.6 | V |
| | $I_{SL(B/W)}$ | $V_{SL}$ = -15V | - | 1.5 | 52.0 | mA |
| | $I_{SL(COLOR)}$ | $V_{SL}$ = -15V | | 37.0 | 52.0 | mA |
| Source Positive supply | $V_{SH}$ | | 14.6 | 15.0 | 15.4 | V |
| | $I_{SH(B/W)}$ | $V_{SH}$ = 15V | - | 1.5 | 53.0 | mA |
| | $I_{SH(COLOR)}$ | $V_{SH}$ = 15V | | 40.0 | 53.0 | mA |
| Border supply | $V_{COM}$ | | -4.0 | Adjusted | -0.2 | V |
| Asymmetry source | $V_{Asym}$ | $V_{SH}$+$V_{SL}$ | -800.0 | 0.0 | 800.0 | mV |
| Common voltage | $V_{COM}$ | | -4.0 | Adjusted | -0.2 | V |
| Standby power panel | $I_{COM}$ | | - | 0.21 | | mA |
| Panel Power | $P_{(B/W)}$ | $V_{DD}$=1.8V | - | 104.0 | 1795.0 | mW |
| | $P_{(COLOR)}$ | $V_{DD}$=1.8V | | 1212.0 | 1795.0 | mW |
| | $P_{(B/W)}$ | $V_{DD}$=3.3V | | 116.0 | 1807.0 | mW |
| | $P_{(COLOR)}$ | $V_{DD}$=3.3V | | 1223.0 | 1807.0 | mW |
| Standby power panel (Note 4) | $P_{STBY}$ | | - | - | 1.3 | mW |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Maximum Currents (Note 5) | ISH | $V_{SH}$ = 15V | - | | 420.0 | mA |
| | ISL | $V_{SL}$ = -15V | - | | 388.0 | mA |
| | IGH | $V_{GH}$ = 25V | - | | 39.0 | mA |
| | IGL | $V_{GL}$ =-20V | - | | 293.0 | mA |
| | ICOM | -- | - | | 224.0 | mA |

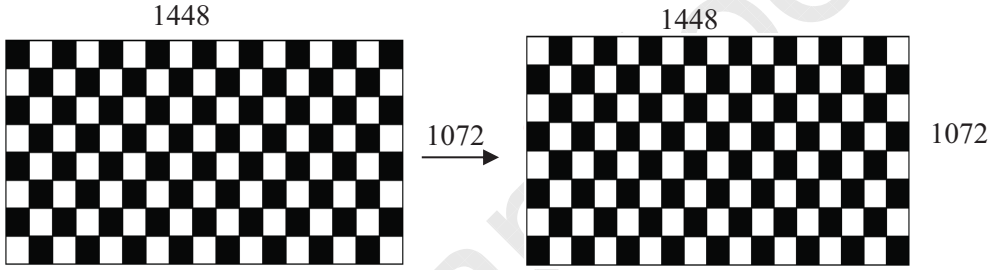
| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Digital Input “H” voltage | VIH | -- | 0.8VDD | | VDD | V |
| Digital Input “L” voltage | VIL | -- | GND | | 0.2VDD | V |

Note :

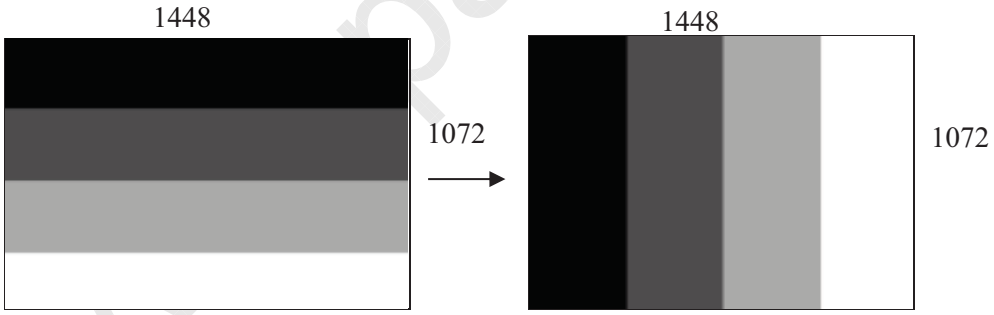
1. The power consumption in this field is measured in whole updated time by 350ms (at 25 degree C) for device battery life estimation.
2. The maximum average Currents for power consumption are measured using 85 Hz waveform with following pattern transition in both B/W and color condition: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)

3. The Typical average current for power consumption is measured using 85 Hz waveform with following pattern transition:
   3-1. For displaying with grayscale image, it is from horizontal 4 gray scale pattern to vertical 4 gray scale pattern without dithering process. (Note 6-2)
   3-2. For displaying with color image, it is from horizontal 8 color pattern to vertical 8 color pattern without dithering process. (Note 6-3)
4. The standby power is the consumed power when the panel controller is in standby mode.
5. The Maximum Currents are measured using 85 Hz waveform with following pattern transition in both B/W and color condition: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
   - It is performed with decoupling capacitors on each power rail as below table (Note 6-4).
   - The minimum value in table of Maximum current is produced by charging mechanism between decoupling capacitors.
6. The listed electrical/optical characteristics are only guaranteed under the controller and waveform provided by E Ink.
7. Vcom is recommended to be set in the range of assigned value ± 0.1 V
8. Use of measuring instruments: Oscilloscope (Model: Tektronix MDO3054)

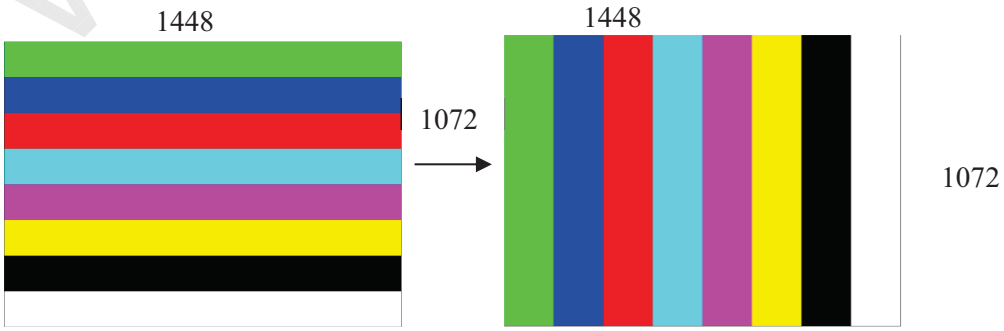
Note6-1
The maximum average current and Maximum Currents for B/W and Color displays




Note6-2
The typical power consumption for B/W display




Note6-3
The typical power consumption at color display



Note6-4

The decoupling capacitors on each power rail for Max. Currents

| Power rail | Capacitors suggested ( uF / Tolerance) |
|---|---|
| ISH | 4.7uF x 2pcs / ±10% |
| ISL | 4.7uF x 2pcs / ±10% |
| IGH | 2.2 uF x 1 pcs / ±10% |
| IGL | 4.7uF x 1 pcs / ±10% |
| IDD | 4.7uF x 1 pcs / ±10% |

**6-4) Front Light DC Characteristics:**

Circuit01 GND = 0 V， Ta = 25℃

| Parameter | LED driving current @ 20mA | | | | | Remark |
|---|---|---|---|---|---|---|
| | Symbol | Min | TYP | MAX | Unit | |
| Supply voltage of LED Front light | $V_{LED}$ | 16.2 | 17.1 | 18.0 | V | Serial 6 pcs |
| Front light Power Consumption | $P_{LED}$ | 324.0 | 342.0 | 360.0 | mW | |

Circuit02 GND = 0 V， Ta = 25℃

| Parameter | LED driving current @ 20mA | | | | | Remark |
|---|---|---|---|---|---|---|
| | Symbol | Min | TYP | MAX | Unit | |
| Supply voltage of LED Front light | $V_{LED}$ | 16.2 | 17.1 | 18.0 | V | Serial 6 pcs |
| Front light Power Consumption | $P_{LED}$ | 324.0 | 342.0 | 360.0 | mW | |

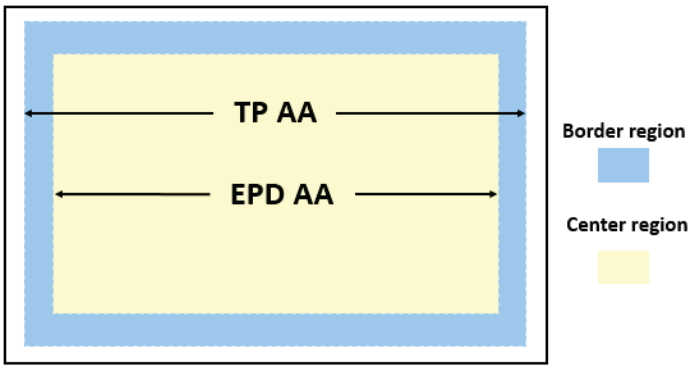
Note : LED L/B is tested at 0.1mA to make sure the LEDs can be driven normally at low current.

**6-5) Touch panel Characteristics**

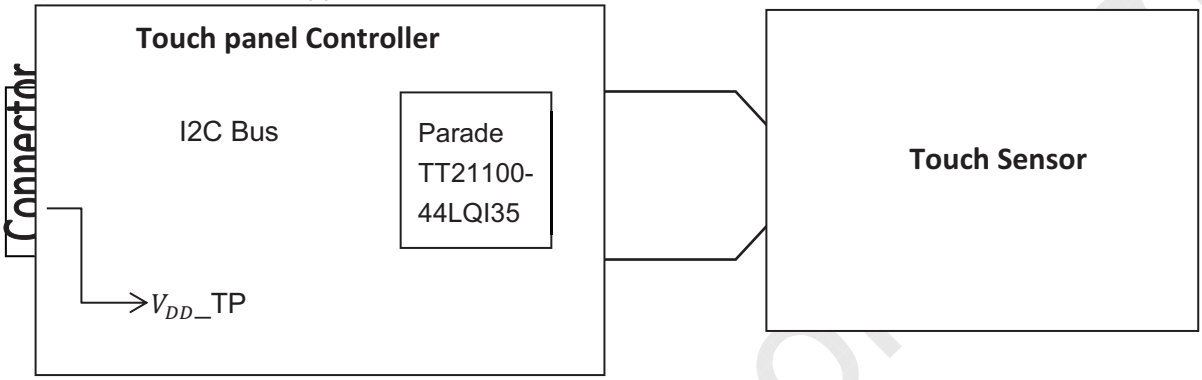
**6-5-1) Touch Panel Performance**

| Symbol | | Specification | Remark |
|---|---|---|---|
| Diameter finger | | 7mm | |
| Linearity | Center | ±1 | No display refresh |
| | Border | ±2 | |
| Accuracy | Center | ±1 | No display refresh |
| | Border | ±2 | |
| Jitter | Center | ±1 | No display refresh |
| | Border | ±2 | |

Reporting rate：80Hz




**6-5-2) Touch Panel circuit application**




**6-5-3) Touch driver IC DC Characteristics: (Note. 1)**

| Symbol | Description | Conditions | Min | Typ | Max | Units | Remark |
|---|---|---|---|---|---|---|---|
| $V_{DD}$_TP | Power supply voltage | - | 2.8 | 3.3 | 3.4 | V | - |
| $I_{DD\ ACT}$ | $V_{DD}$_$TP$ Active Current @ IC | - | - | 9 | 12 | mA | Note. 2 |
| $I_{DD\ DS}$ | $V_{DD}$_$TP$ Deep Sleep Current @ IC | - | - | 1 | - | uA | |
| $I_{DD\ ACT}$ | $V_{DD}$_$TP$ Active Current @ module | - | - | - | 18.2 | mA | |
| $I_{DD\ DS}$ | $V_{DD}$_$TP$ Deep Sleep Current @ module | - | - | - | 15.2 | uA | |

Note：

1. The final touch module consumption will be come out base on device firmware tune lockdown setting.
2. The power consumption is only for reference.

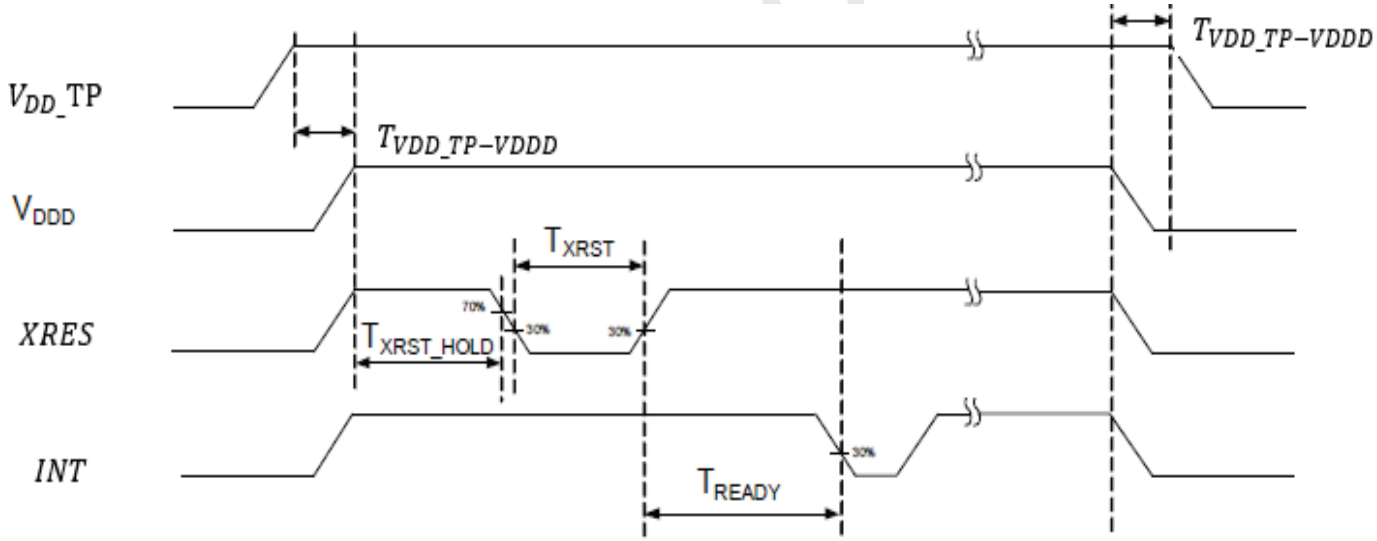
### 6-5-4) Touch driver IC AC Characteristics and Power Sequence: (Note.)

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $PSA_{RAMP}$ | $V_{DD\_TP}$ Ramp Up | - | - | - | 100 | mV/us |
| $PSD_{RAMP}$ | $V_{DDD}$ Ramp rate from ground to minimum voltage | - | 1 | - | 40 | V/ms |
| $T_{VDD\_TP-\_VDDD}$ | Time of $V_{DD\_TP}$ Ready time before $V_{DDD}$ ready time | - | 0 | - | - | ms |
| $T_{XRST\ HOLD}$ | Hold time berfore external reset(XRES) asserted | - | 2 | - | - | ms |
| $T_{XRST}$ | External reset(XRES) pulse width | After $V_{DDD}$ is valid | 10 | - | - | us |
| $T_{VDDD-\_VDD\_TP}$ | Time of $V_{DDD}$ discharge before $V_{DD\_TP}$ discharge time | - | 0 | - | - | ms |
| $T_{READY}$ | Time from XRES deassertion to INT | - | - | - | 10 | ms |
| $T_{CAL}$ | Calibration routine execution time | - | - | - | 1100 | ms |

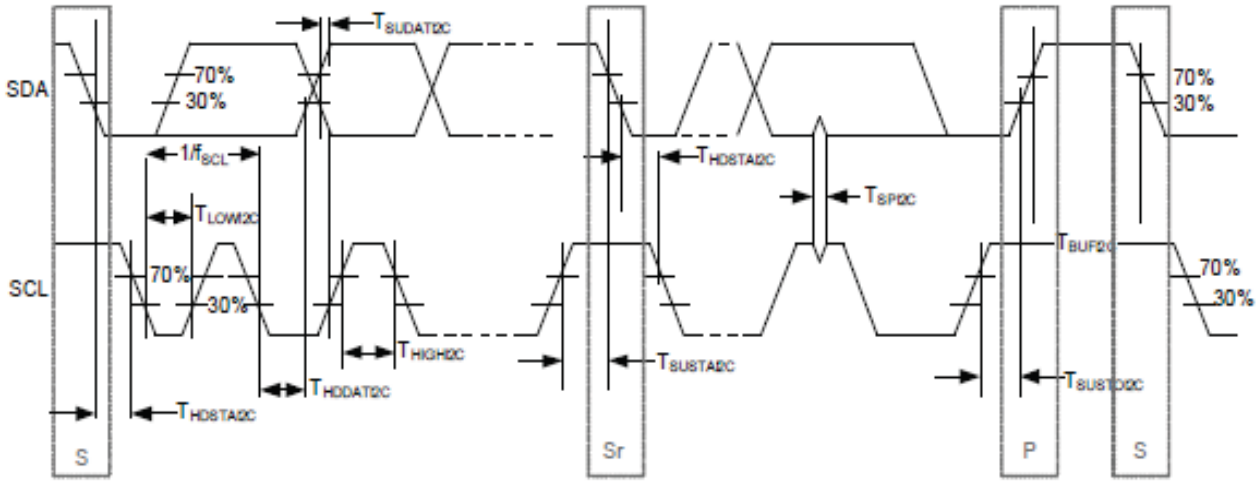
Note： $V_{DD}$_TP = $V_{DD}$_3.3V

$V_{DDD}$ ：Generated inside touch driver based on $V_{DD}$_3.3V

**Power sequence time diagram**



### 6-5-5) Touch Driver IC I2C Bus Timing Diagram for Fast/Standard Mode




**Legend**
S: I²C Start Condition
Sr: I²C Repeat Start Condition
P: I²C Stop Condition

### 6-5-6) Packet Interface Protocol (PIP) Communication

```
Code 1 - Register Pointer Example Write Code
w 24 04 00 05 00 2F 00 03
; Packet Length = 0x0050
; Packet ID     = 0x2F
```

```
Code 2 - Register Pointer Example Read Code
w 24 01 00
r 24 x x x
```

**Write Command Break-down**

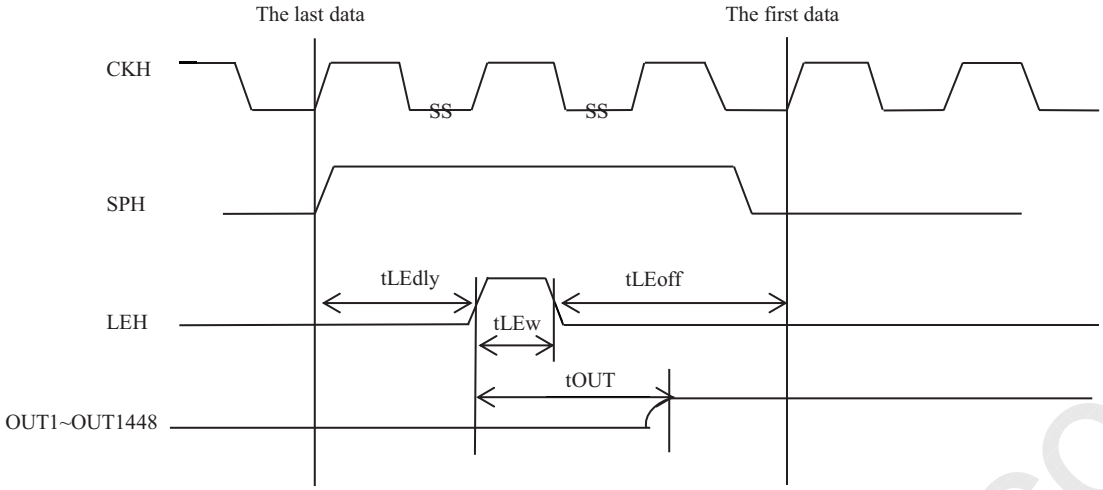
| Write | I²C Address | Buffer Offset LSB | Buffer Offset MSB | Packet Length LSB | Packet Length MSB | Report ID | Data[0] | Data[1] |
|---|---|---|---|---|---|---|---|---|
| W | 24 | 04 | 00 | 05 | 00 | 2F | 00 | 03 |

### 6-6), Panel AC characteristics:

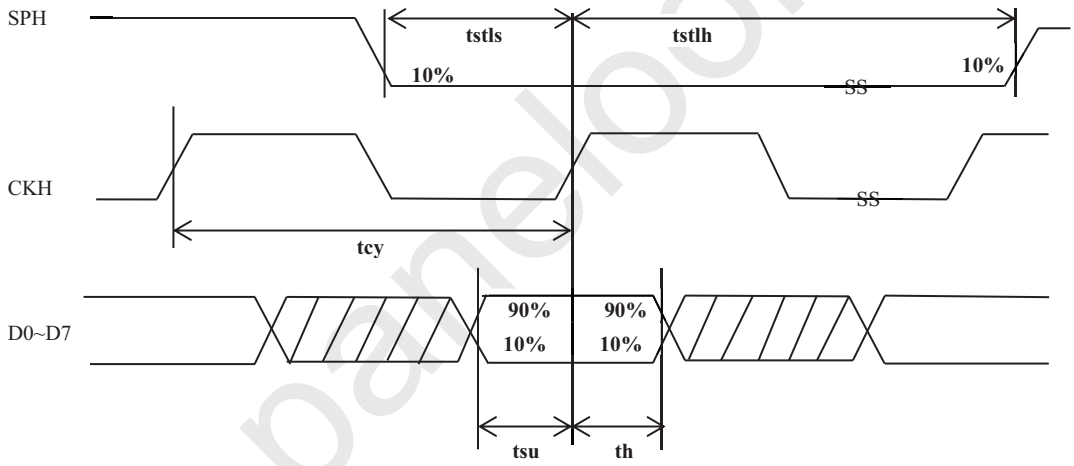
| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Clock frequency | fckv | - | - | 200 | kHz |
| Minimum “L” clock pulse width (for $V_{DD}$=1.8V) | twL | 1 | - | - | us |
| Minimum “H” clock pulse width (for $V_{DD}$=1.8V) | twH | 1 | - | - | us |
| Minimum “L” clock pulse width (for $V_{DD}$=3.3V) | twL | 0.5 | | | us |

| | | | | | |
|---|---|---|---|---|---|
| Minimum "H" clock pulse width (for $V_{DD}$=3.3V) | twH | 0.5 | | | us |
| Clock rise time | trckv | - | - | 100 | ns |
| Clock fall time | tfckv | - | - | 100 | ns |
| SPV setup time | tSU | 100 | - | twH-100 | ns |
| SPV hold time | tH | 100 | - | twH-100 | ns |
| Pulse rise time | trspv | - | - | 100 | ns |
| Pulse fall time | tfspv | - | - | 100 | ns |
| Clock XCL cycle time (for $V_{DD}$=1.8V) | tcy | 22.22 | - | - | ns |
| Clock XCL cycle time (for $V_{DD}$=3.3V) | tcy | 16.67 | - | - | ns |
| D0 .. D7 setup time (for $V_{DD}$=1.8V) | tsu | 11 | - | - | ns |
| D0 .. D7 setup time (for $V_{DD}$=3.3V) | tsu | 8 | - | - | ns |
| D0 .. D7 hold time (for $V_{DD}$=1.8V) | th | 11 | - | - | ns |
| D0 .. D7 hold time (for $V_{DD}$=3.3V) | th | 8 | - | - | ns |
| XSTL setup time | tstls | 0.5* tcy | - | 0.8* tcy | ns |
| XSTL hold time | tstlh | 0.5* tcy | - | | ns |
| XLE on delay time (for $V_{DD}$=1.8V) | tLEdly | 4.5* tcy | - | - | ns |
| XLE on delay time (for $V_{DD}$=3.3V) | tLEdly | 3.5* tcy | - | - | ns |
| XLE high-level pulse width (When VDD=1.7V to 2.5V) | tLEw | 400 | - | - | ns |
| XLE high-level pulse width (When VDD=2.5V to 3.6V) | tLEw | 300 | - | - | ns |
| XLE off delay time (for $V_{DD}$=1.8V) | tLEoff | 250 | - | - | ns |
| XLE off delay time (for $V_{DD}$=3.3V) | tLEoff | 200 | - | - | ns |
| Output setting time to +/- 30mV($C_{load}$=200pF) | tout | - | - | 20 | us |

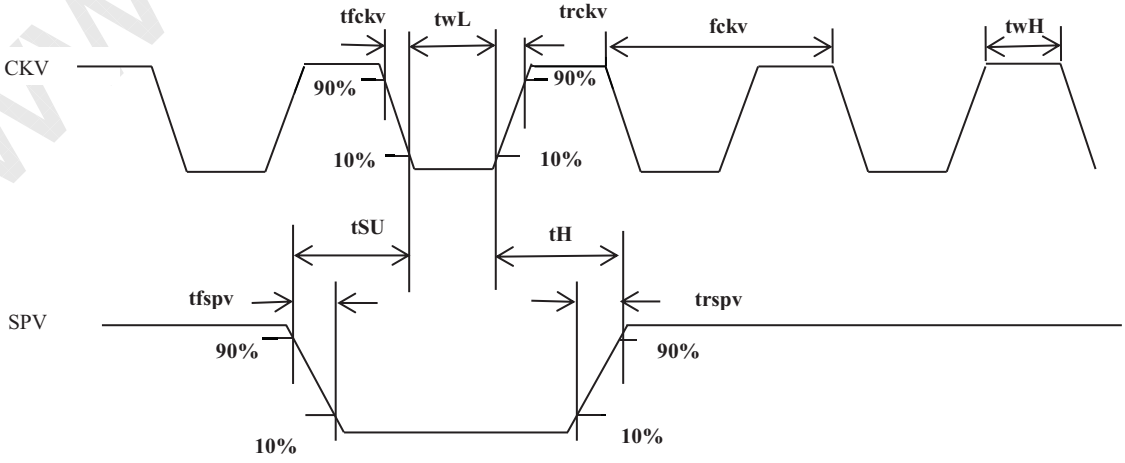
OUTPUT LATCH CONTROL SIGNALS



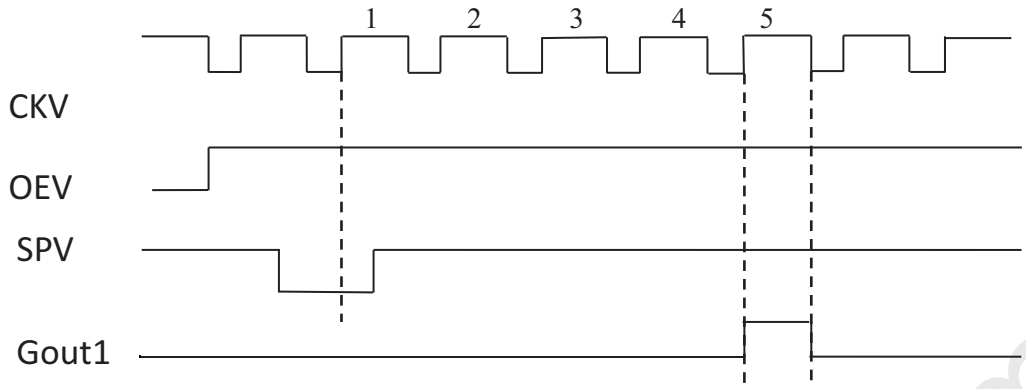

CLOCK & DATA TIMING




CKV & SPV TIMING



GATE OUTPUT TIMING




Note：The 1st Gate line(Gout1) is output based on above timing of "GATE OUTPUT TIMING"

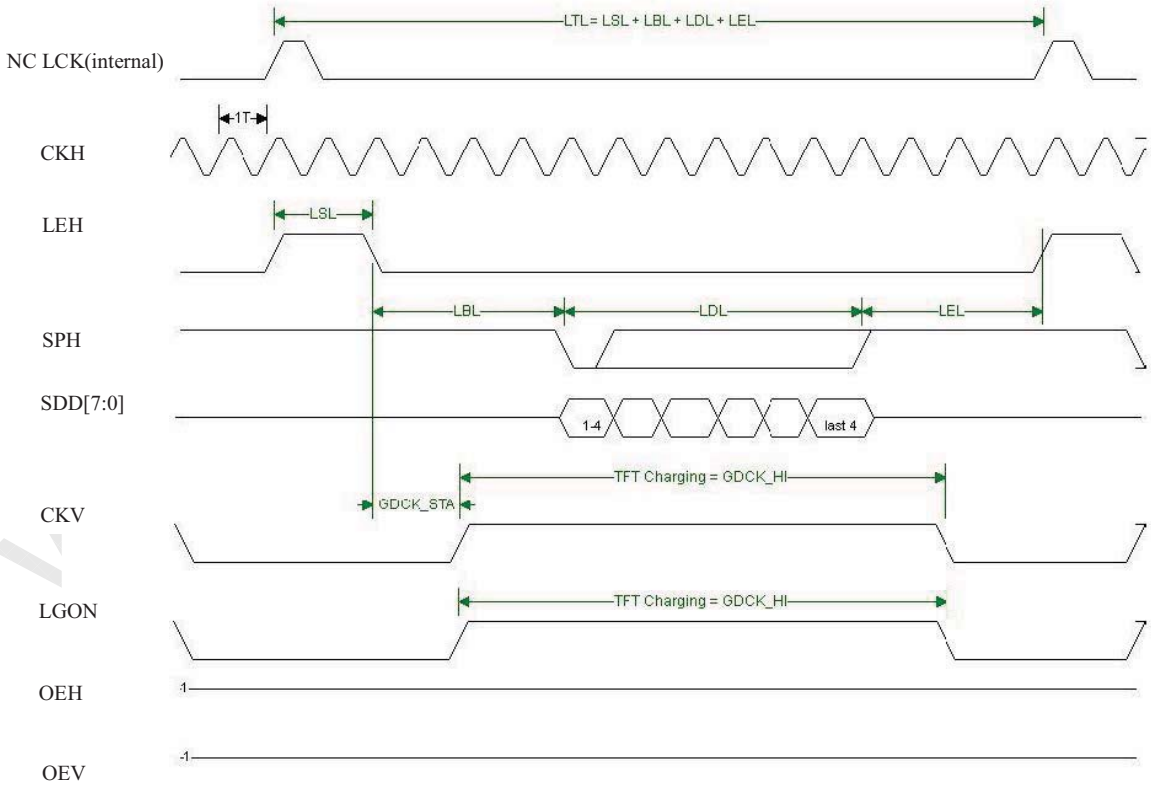
### 6-7) Refresh Rate

The module applied at a maximum refresh rate of 85 Hz.

| | Min | Max |
|---|---|---|
| **Refresh Rate** | - | 85 Hz |

### 6-8) Controller Timing

This timing mode is depicted on Figure 1 and Figure 2 and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, that in this mode LGON follows GDCK timing




Note: LCK is an internal signal and it is shown for reference only

Figure 1

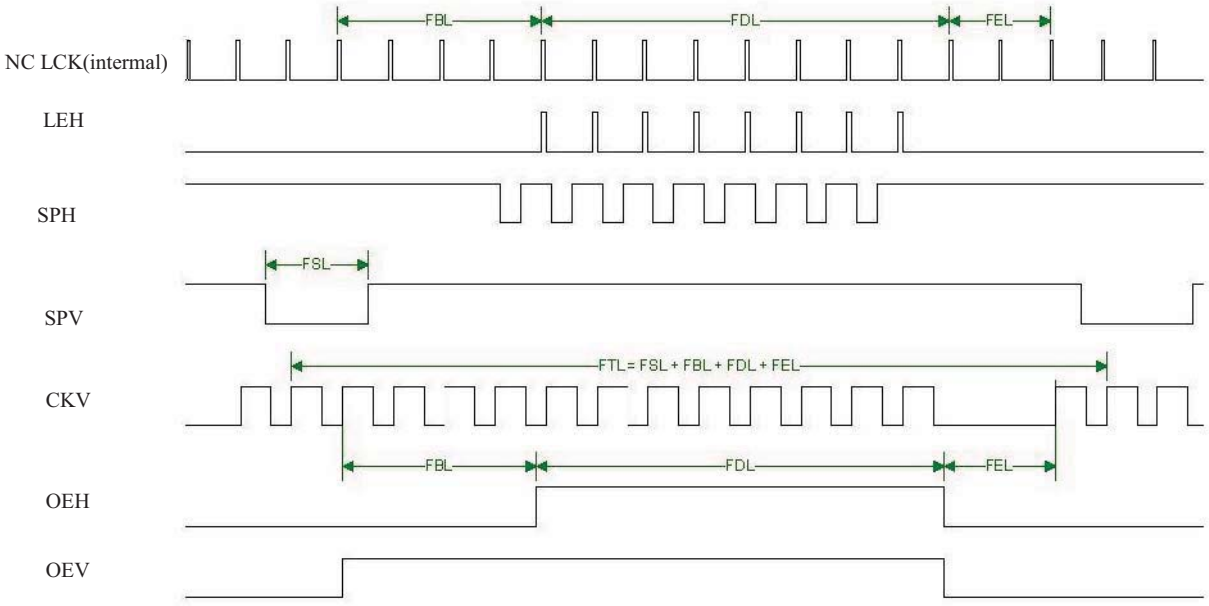



Figure 2

Timing Parameters Table

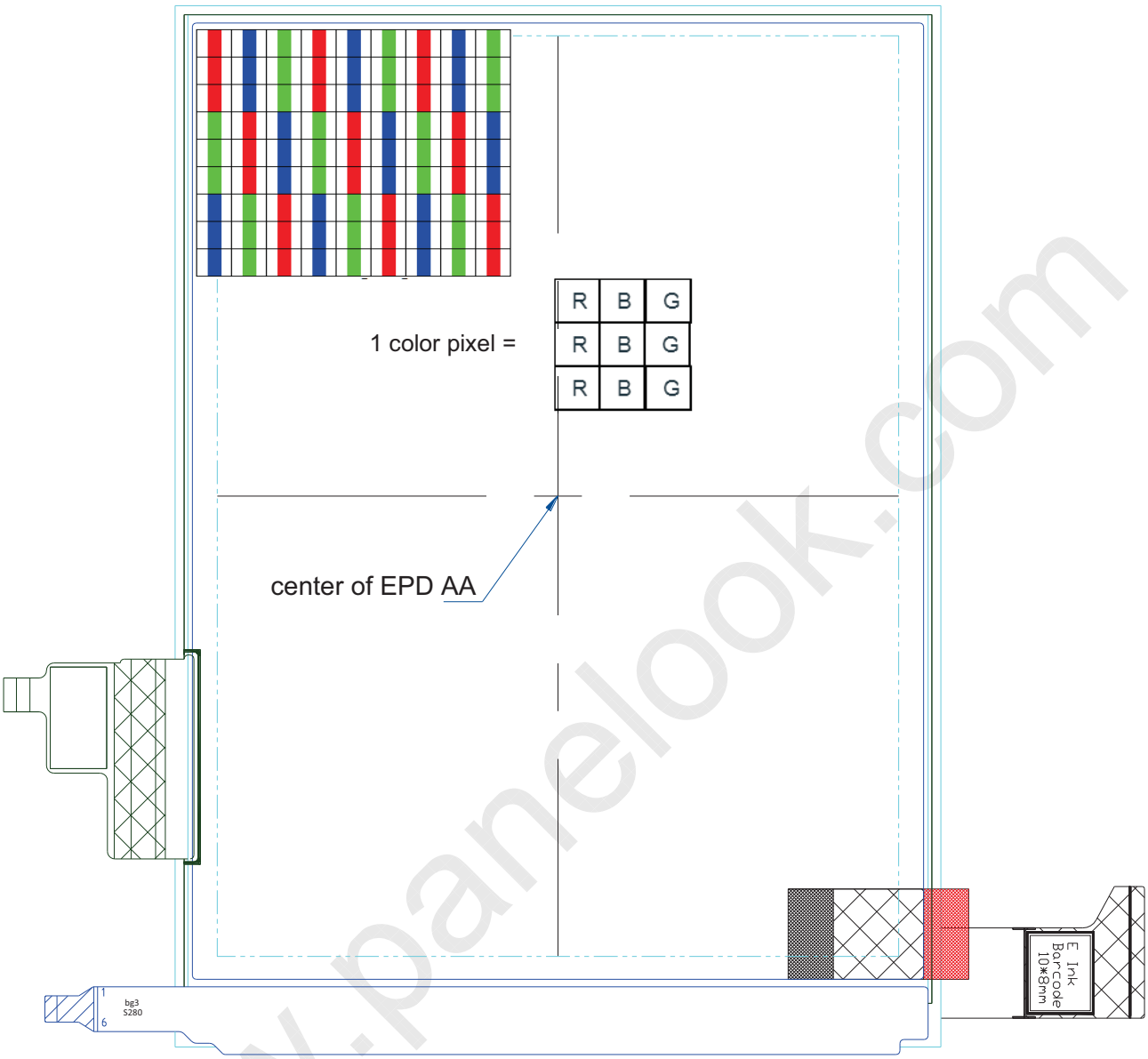
| | | | | | | |
|---|---|---|---|---|---|---|
| Mode | 3 | Resolution 1448*1072 | | | | |
| SDCK【MHz】 | 40 | | | | | |
| Pixels Per SDCK | 4 | | | | | |
| Line Parameters【SDCK】 | LSL | LBL | LDL | LEL | GDCK _STA | LGONL |
| | 18 | 12 | 362 | 40 | 84 | 288 |
| Line Parameters【us】 | - | - | - | - | - | - |
| | 0.45 | 0.30 | 9.05 | 1 | 2.1 | 7.2 |
| Frame Parameters【lines】 | FSL | FBL | FDL | FEL | - | FR【Hz】 |
| | 1 | 4 | 1072 | 12 | - | 85.03 |
| Frame Parameters【us】 | - | - | - | - | - | - |
| | 10.8 | 43.2 | 11577.6 | 129.6 | - | - |

Note:

1. For parameters definition, see above Figure 1 and Figure 2.
2. For NXP SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL
3. The mapping of pins between controller timing and pin-assignment of panel:

## 7 Pixel Arrangement

The Color EPD module pixel arrangement is stripe.

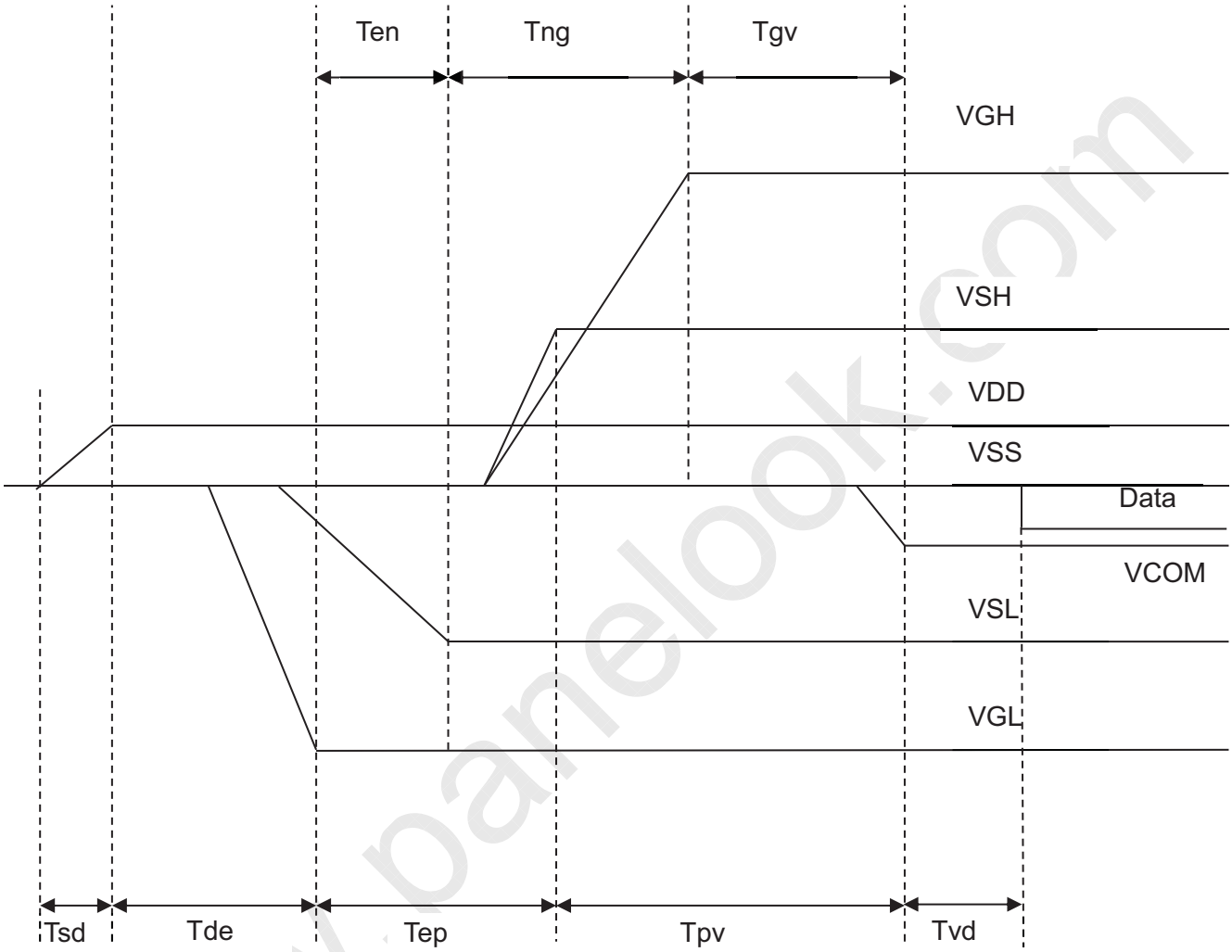


## 8. Power Sequence

Power Rails must be sequenced in the following order：

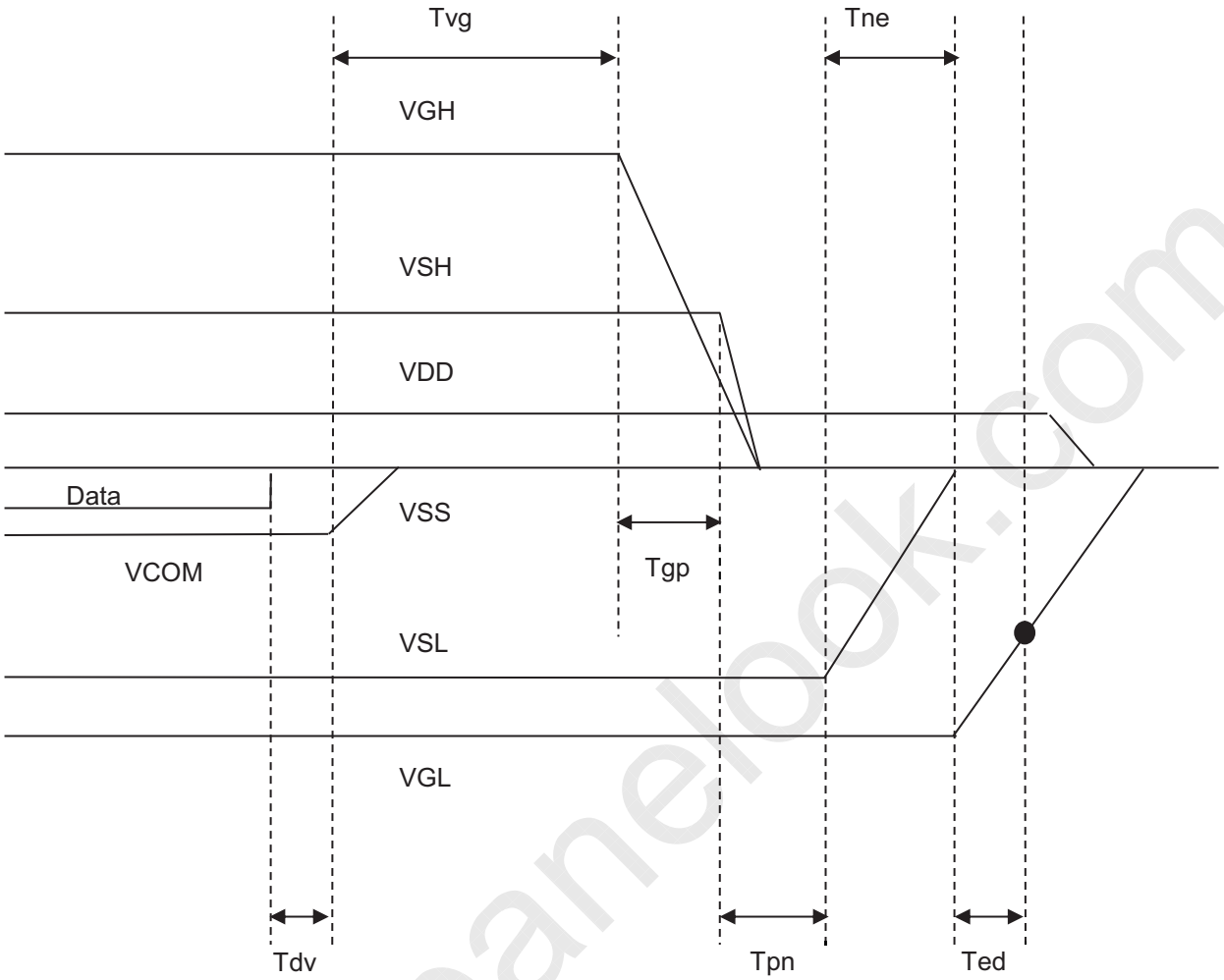
1. VSS → VDD → VSL → VSH (Source driver) → VCOM
2. VSS → VDD → VGL → VGH (Gate driver)

**POWER ON**




| | Min | Max |
|---|---|---|
| Tsd | 30us | - |
| Tde | 100us | - |
| Tep | 1000us | - |
| Tpv | 100us | - |
| Tvd | 100us | - |
| Ten | 0us | - |
| Tng | 1000us | - |
| Tgv | 100us | - |

**POWER OFF**




| | Min | Max | Remark |
|---|---|---|---|
| Tdv | 100µs | - | - |
| Tvg | 0µs | - | - |
| Tgp | 0µs | - | - |
| Tpn | 0µs | - | - |
| Tne | 0µs | - | - |
| Ted | 0.5s | - | Discharged point @ -7.4 Volt |

Note:

1. Supply voltages decay through pull-down resistors.
2. VGL must remain negative of Vcom during decay period

## 9. Optical Characteristics

### 9-1)Specifications

Measurements are made by PR655 with SL-1X or equivalent SpectraScan Colorimeter with that the illumination is from the 45°angle perpendicular to the center of while, and the detector is perpendicular unless otherwise specified.

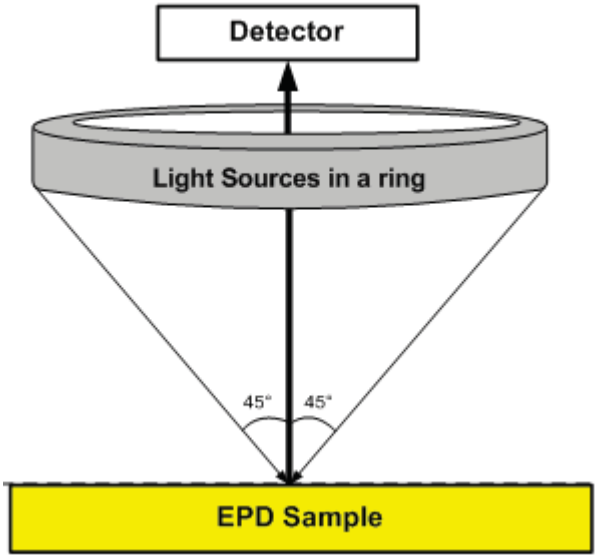
T = 25°C

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| R% | Reflectance | White | Front | 14 | 20 | - | % |
| CR | Contrast | WK | Light | 10 | 16 | - | |
| Color Gamut | | RGBCMYWK | Off | 2200 | 3200 | - | - |
| Y | Luminance | White | | 140 | 180 | - | cd/m$^2$ ($I_{LED}$ 20mA) |
| x | White Chromaticity | White | Front | 0.257 | 0.297 | 0.337 | |
| y | | White | Light | 0.283 | 0.323 | 0.363 | |
| Luminance Uniformity | | White | On | 60 | 75 | - | % |
| CR | Contrast | WK | | 9 | 12 | - | - |
| **SYMBOL** | **PARAMETER** | **CONDITIONS** | | **L*_TYP** | **a*_TYP** | **b*_TYP** | **UNIT** |
| R | Color coordinates (dE2000< 3) | Red | Front | 28.64 | 8.46 | 2.17 | - |
| G | | Green | Light | 33.47 | -13.36 | 7.08 | - |
| B | | Blue | Off | 28.78 | -5.92 | -10.82 | - |

*WS: White state , DS: Dark state, Gray state from Dark to White :DS、G1、G2…、Gn…、Gm-2、WS
m:4、8、16 when 2、3、4 bits mode
*C0 : Spec center of white chromaticity, B1~B4 : Boundary point of white chromaticity spec
* WK: W means white pattern and K means black pattern

### 9-2)Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):
CR = Rl/Rd




**9-3)Reflection Ratio**

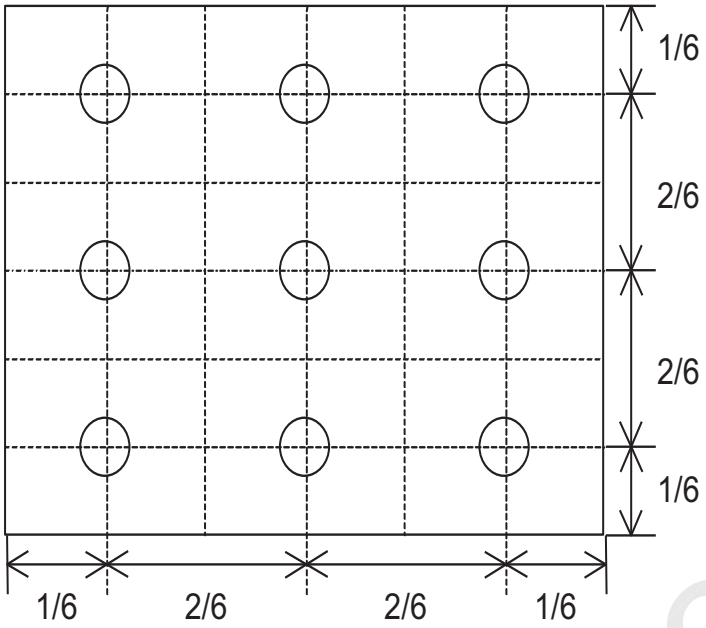
The reflection ratio is expressed as:
R = Reflectance Factor$_{\text{white board}}$ x ( $L_{\text{center}}$ / $L_{\text{white board}}$ )
$L_{\text{center}}$ is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

**9-4)Uniformity**

The uniformity is defined as:

$$U = \frac{The\ Minimum\ Brightness\ of\ the\ 9\ testing\ Points}{The\ Maximum\ Brightness\ of\ the\ 9\ testing\ Points}$$

Ambient illumination: < 1 Lux
Measuring direction: Perpendicular to the surface of module
The test pattern is white.




**9-5)Definition of contrast ratio for front light on mode**

$$CR = \frac{Luminance\ when\ Testing\ point\ is\ White}{Luminance\ when\ Testing\ point\ is\ Black}$$

## 10. Handling, Safety and Environmental Requirements and Remark

| WARNING |
|---|
| The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap. |

| CAUTION |
|---|
| The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. |
| Disassembling the display module can cause permanent damage and invalidate the warranty agreements. |
| IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed. |

| Mounting Precautions |
|---|
| (1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. |
| (2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force. |
| (3) You should adopt radiation structure to satisfy the temperature specification. |
| (4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction. |
| (5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS) |
| (6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS. |
| (7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading. |

| **Data sheet status** | |
|---|---|
| Product specification | This data sheet contains formal product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

| REMARK |
|---|
| All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation. |

## 11. Reliability Test

| | TEST | CONDITION | METHOD | REMARK |
|---|---|---|---|---|
| 1 | High-Temperature Operation | T = +50°C, RH = 30% for 240 hrs | IEC 60 068-2-2Be | -- |
| 2 | Low-Temperature Operation | T = 0°C for 240 hrs | IEC 60 068-2-1Ae | -- |
| 3 | High-Temperature, High-Humidity Operation | T = +40°C, RH = 90% for 168 hrs | IEC 60 068-2-78 | |
| 4 | High-Temperature Storage | T = +60°C, RH = 26% for 240 hrs<br>Test in white pattern | IEC 60 068-2-2 Bb | |
| 5 | Low-Temperature Storage | T = -25°C for 240 hrs<br>Test in white pattern | IEC 60 068-2-1Ab | |
| 6 | Temperature Cycle | -25℃→+60℃, 100 Cycles<br>30min 30min<br>Test in white pattern | IEC 68-2-14Nb | -- |
| 7 | Solar radiation test | 765 W/m$^2$ for 168hrs,40℃<br>Test in white pattern | IEC 60068-2-5Sa | -- |
| 8 | Package Vibration | 1.04G, Frequency: 10~500Hz<br>Direction: X,Y,Z<br>Duration: 1 hours in each direction | Full packed for shipment | -- |
| 9 | Package Drop Impact | Drop from height of 122 cm<br>on concrete surface.<br>Drop sequence: 1 corner,3 edges,6 faces<br>One drop for each. | Full packed for shipment | -- |
| 10 | Electrostatic Effect (non-operating) | (Machine model)+/- 250V<br>0Ω, 200pF | IEC 62179<br>IEC 62180 | -- |

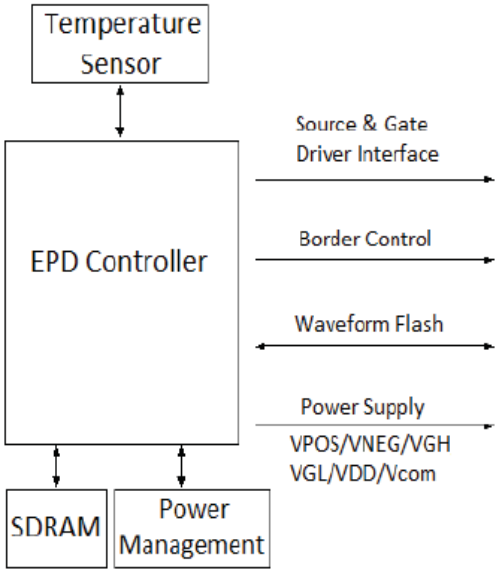
Actual EMC level to be measured on customer application

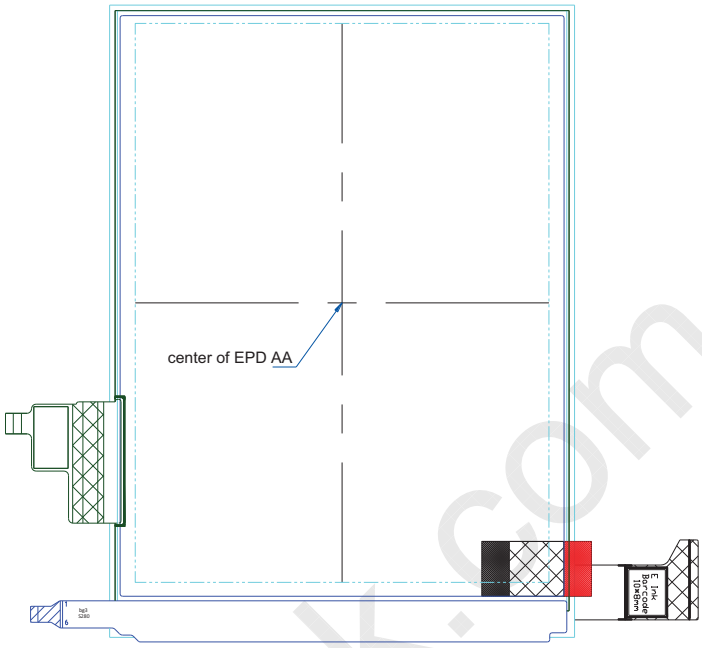
Note: The protective film must be removed before temperature test.

< Criteria >

In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image). All the cosmetic specification is judged before the reliability stress.

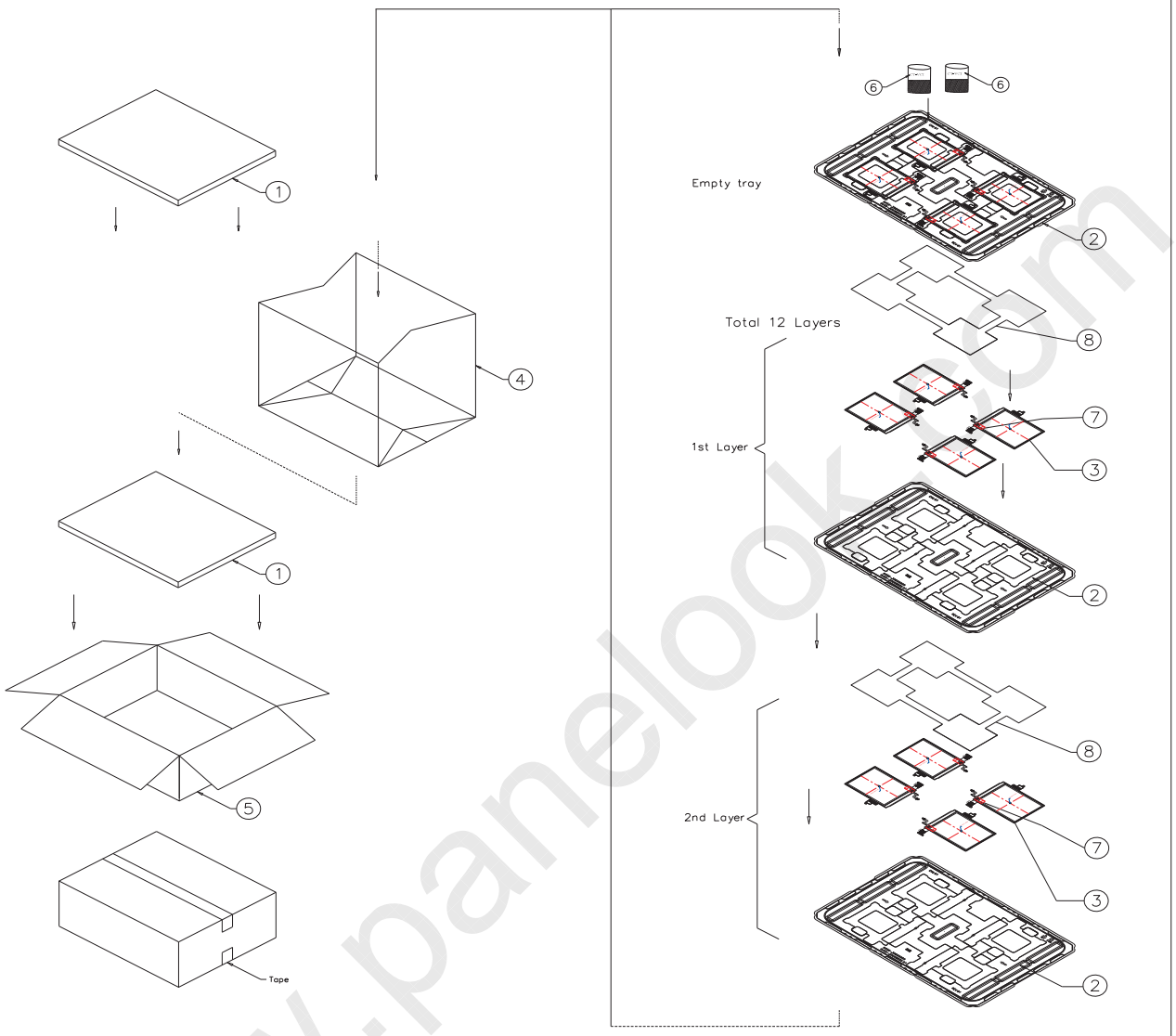
## 12. Block Diagram



## 13. Packing

| REV | DESCRIPTION | DESIGN | DATE |
|---|---|---|---|
| 01 | INITIAL RELEASE | Jimmy Chen | 2020/01/03 |
| | | | |




NOTE:
1. One layer include:
   10 pcs module & 1 piece of tray.
2. Q'TY: 120 pcs panel/carton.
3. Dimension: 445*365*170mm
4. Make sure tray stacked with 0° rotation.
   We can check this by lateral side view.

| ITEM | DESCRIPTION | Q'TY | REMARK |
|---|---|---|---|
| 8 | EPE_Cushion | 12 | |
| 7 | Peeling tape | 48 | |
| 6 | 30g加厚複合紙活礦乾燥劑73*95mm | 2 | |
| 5 | CARTON INTERNAL | 1 | |
| 4 | 摺口袋 Bag | 1 | 抗靜電 |
| 3 | EC060KH1 EPD | 48 | |
| 2 | TRAY | 13 | 抗靜電 |
| 1 | EPE FOAM | 2 | |

| MTL.SPEC. | UNSPECIFIED TOL'S ±5.0mm | REMARK |
|---|---|---|
| | ANGLE | |
| | ROUGHNESS | |

E Ink 元太科技工業股份有限公司 E Ink Holdings Inc.

| | | | SCALE | UNIT | SHEET | DWG.TITLE |
|---|---|---|---|---|---|---|
| APPROVE | Jiangbo Chen | 2020/01/03 | 1:1 | mm | 1 OF 1 | EC060KH1 PACKING |
| CHECK | Jiangbo Chen | 2020/01/03 | | | | |
| DESIGN | Jimmy Chen | 2020/01/03 | MTL.NO. | | DWG.NO. | A4 SIZE |