(V) Preliminary Specifications
( ) Final Specifications

Module	**11.6” 16:9 Color TFT-LCD with LED Backlight design**
Model Name	**B116XAN01.0 (H/W:2A)**
Note	***LED Backlight with New Digitizer Design***

Customer	**Date**
Checked & Approved by	**Date**

Approved by	**Date**
Kevin KH Shen	10/05/2012
Prepared by	
Erica YT Lin	10/05/2012

Note: This Specification is subject to change without notice.

DMPBU Marketing Division
AU Optronics corporation

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 07/27/2012			1st version	
0.2 08/28/2012	6		Update Chromaticity	
0.3 10/05/2012	4	Contrast ratio 800typ	Contrast ratio 800 min	
	32&33		Update 2D drawing	

Contents

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breakdown.

2. General Description

B116XAN01 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 WXGA, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit**.** All input signals are MIPI interface compatible.

B116XAN01 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

2.1.1 Panel General Specification

Items	Unit	Specifications	
Screen Diagona	[mm]	293.83 (11.6W")	
Active Area	[mm]	256.125 (H) x 144(V)	
Pixels H x V		1366 x 3(RGB) x 768	
Pixel Pitch	[mm]	0.1875 X 0.1875	
Pixel Format		R.G.B. Vertical Stripe	
Display Mode		Normally Black	
White Luminance (ILED=12mA/18.5mA) **(Note: I_{LED} is LED current)**	[cd/m^2]	450 typ. (5 points average)	
		700 typ. (5 points average)	
Luminance Uniformity		1.25 max. (5 points) 1.5 max (13 points)	
Contrast Ratio		800 min	
Response Time	[ms]	30 Max	
Nominal Input Voltage VDD	[Volt]	+3.3 typ.	
Power Consumption	[Watt]	Logic Power: 0.7W	450nit (typ)
		BLU Power: 1.69W	
		Logic Power: 0.7W	700nit (typ)
		BLU Power: 2.69W	
Weight	[Grams]	185 max (Base Panel)	Panel: 156 max
			Digitizer: 25 typ

Physical Size (panel only)	[mm]		Min.	Typ.	Max.
		Length	266.87	267.17	267.47
		Width	157.01	157.31	157.61
		Thickness (W/O PCBA)	---	---	2.91
		Thickness (W/ PCBA)	---	---	4.74
Support Color		16.7M colors (RGB 8-bit)			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	-20 to +60 -30 to +70			
RoHS Compliance		RoHS Compliance			

2.1.2 Digitizer General Specification

Technology	Electro-magnetic Resonance
Active Area	258.125×146mm
Resolution	0.01mm (2540 ppi)
Coordinate Accuracy	±0.4mm (see Note 1 and 2)
Coordinate Deviation When Tilting Pen	±3mm (tilted ±50° from vertical) (see Note 3)
Detectable Pen tilt	Up to 50° from vertical
Detectable Height	4 to 10mm above the Sensor Film (see Note 1)
Position Report Rate	133 pps
Pressure Resolution	1024 levels @ full scale (see Note 4)

Note 1: The Pen Digitizer Unit and pen only, at ordinary temperature.

Note 2: The pen held vertically at 7mm high from sensor film.

Note 3: The pen held in the center of the active area.

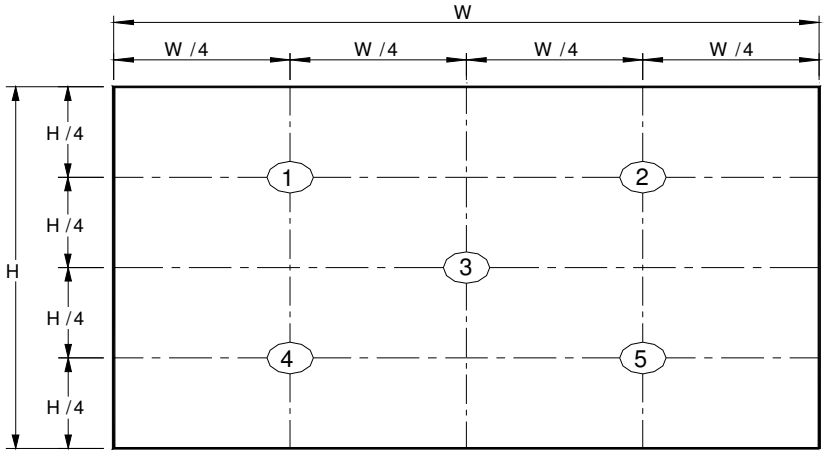
Note 4: UP pen only.

2.2 Optical Characteristics

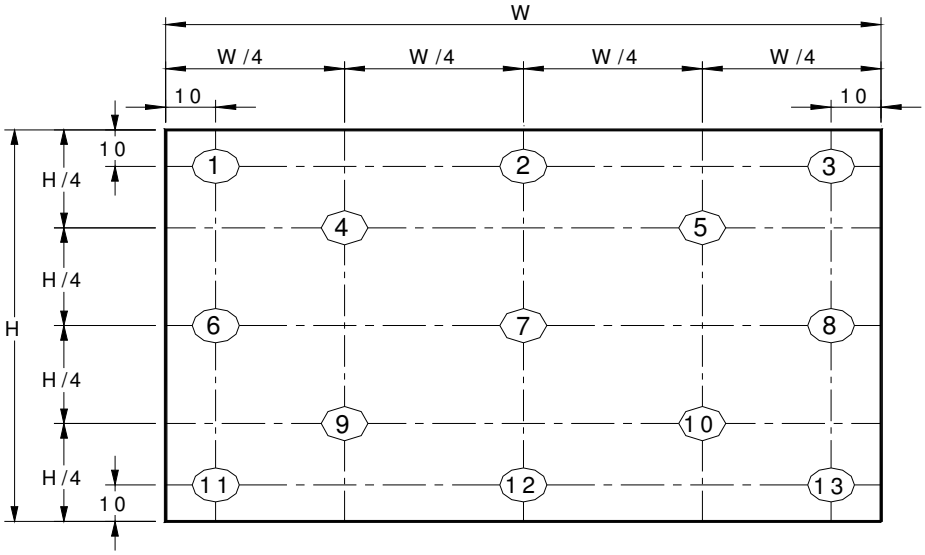
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=12mA			5 points average	405	450	---	cd/m^2	1, 4, 5.
White Luminance I_{LED}18.5mA			5 points average	616	700	---	cd/m^2	
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	---	89 89	---	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	---	89 89	---		
Luminance Uniformity		δ_{5P}	5 Points	---	---	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	---	---	1.5		2, 3, 4
Contrast Ratio		CR		800	---	---		4, 6
Cross talk		%		---	---	4		4, 7
Response Time		T_{RT}	Rising + Falling	---	--	30	msec	4, 8
Color / Chromaticity Coordinates	Red	Rx	CIE 1931	0.569	0.599	0.629		4
		Ry		0.316	0.346	0.376		
	Green	Gx		0.299	0.329	0.359		
		Gy		0.548	0.578	0.608		
	Blue	Bx		0.122	0.152	0.182		
		By		0.102	0.132	0.162		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	50	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



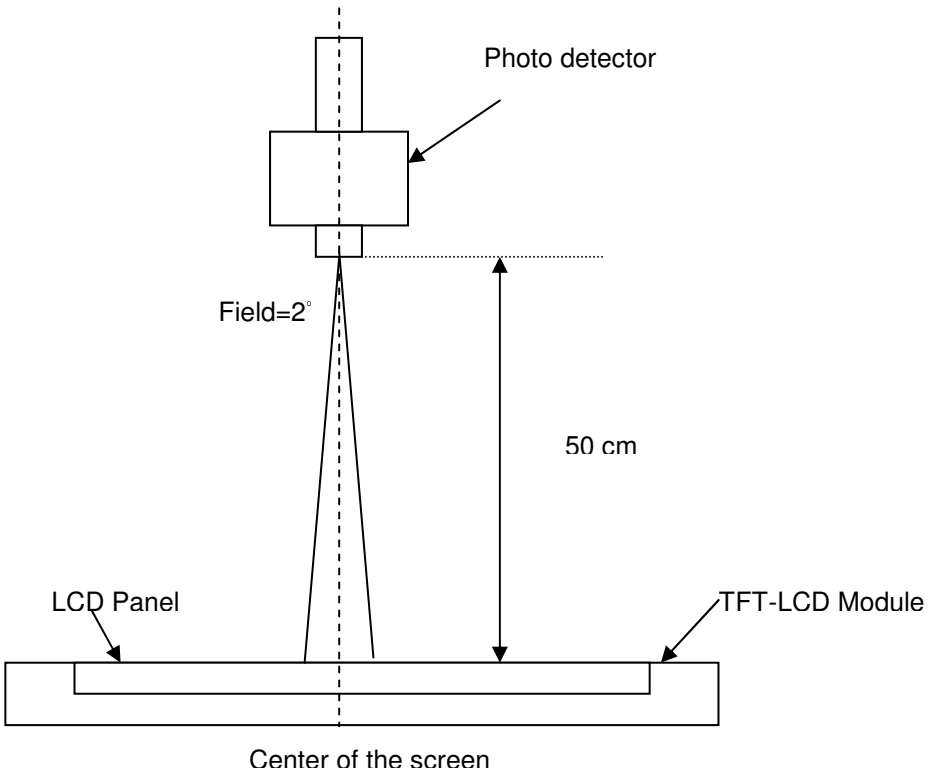
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

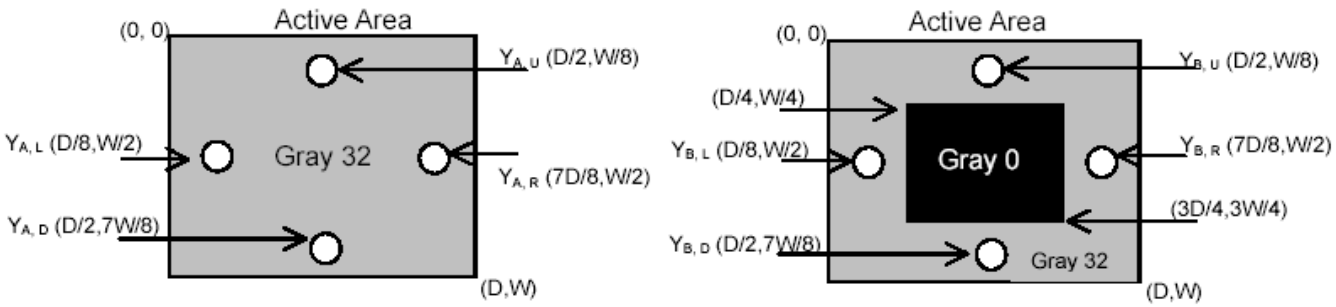
Note 7 : Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$

Where

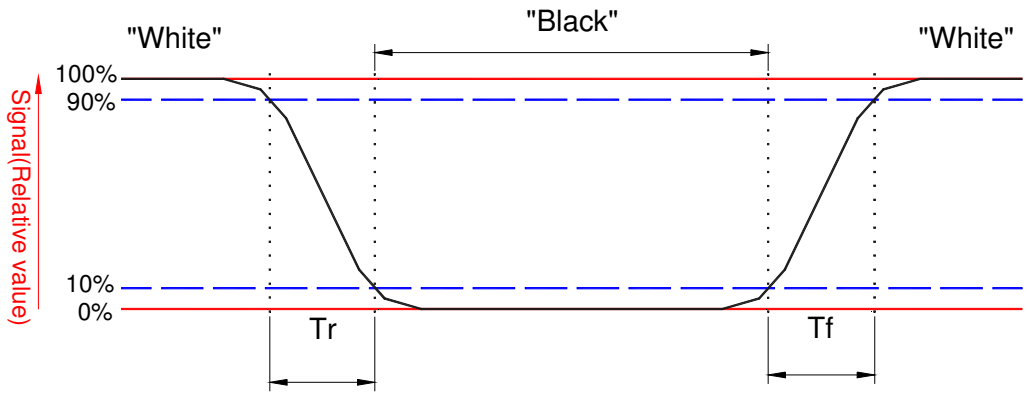
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



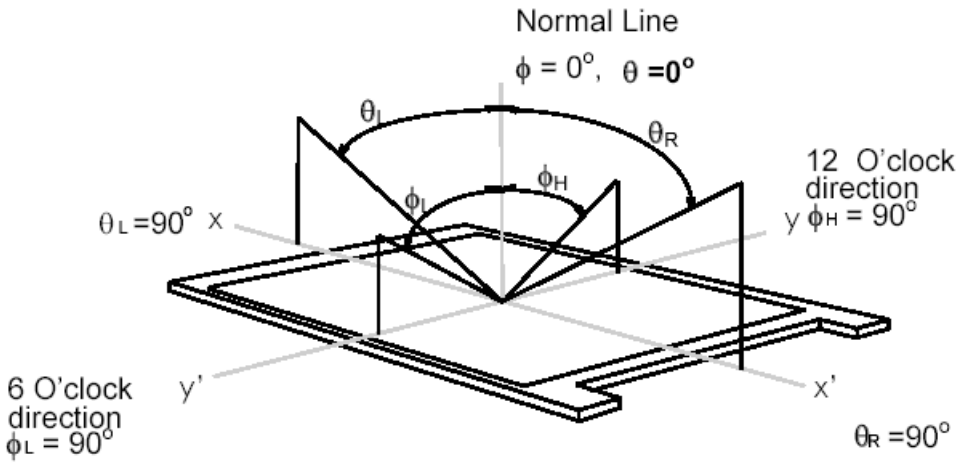
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



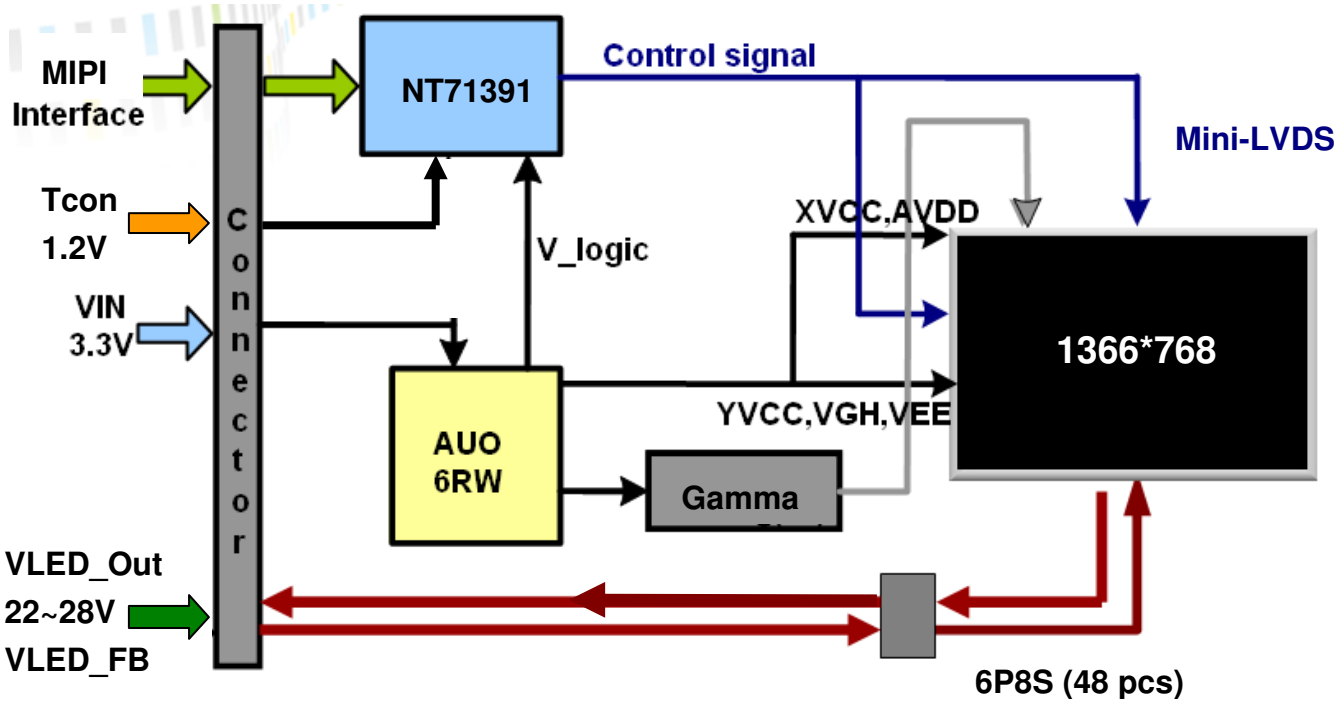
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 40 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Digitizer

Item	Symbol	Min	Max	Unit	Checked Terminal
Supply Voltage	V_{DD}	-0.3	+4.0	V	V_{DD} – GND
Input Voltage of Signals	V_{IN}	-0.3	V_{DD} +0.3	V	
High level output current	I_{OH}		-5	mA	
Low level output current	I_{OL}		-10	mA	
Operating Ambient Temperature	T_{OP}	0	+60	℃	
Operating Ambient Humidity	H_{OP}	20	90	%(RH)	No condensing
Storage Temperature	T_{STG}	-20	+75	℃	
Storage Humidity	H_{STG}	20	95	%(RH)	No condensing

Do not exceed the maximum rating values under any conditions including the variations in supply voltage, input voltage, part constants, ambient temperature and so on; it may damage the unit.

4.3 Absolute Ratings of Environment

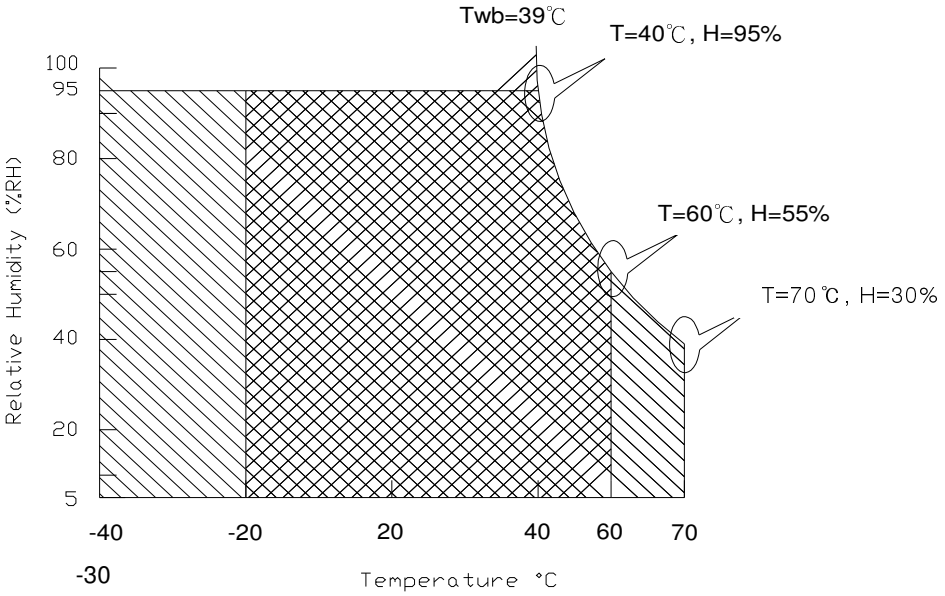
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	-20	+60	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-30	+70	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

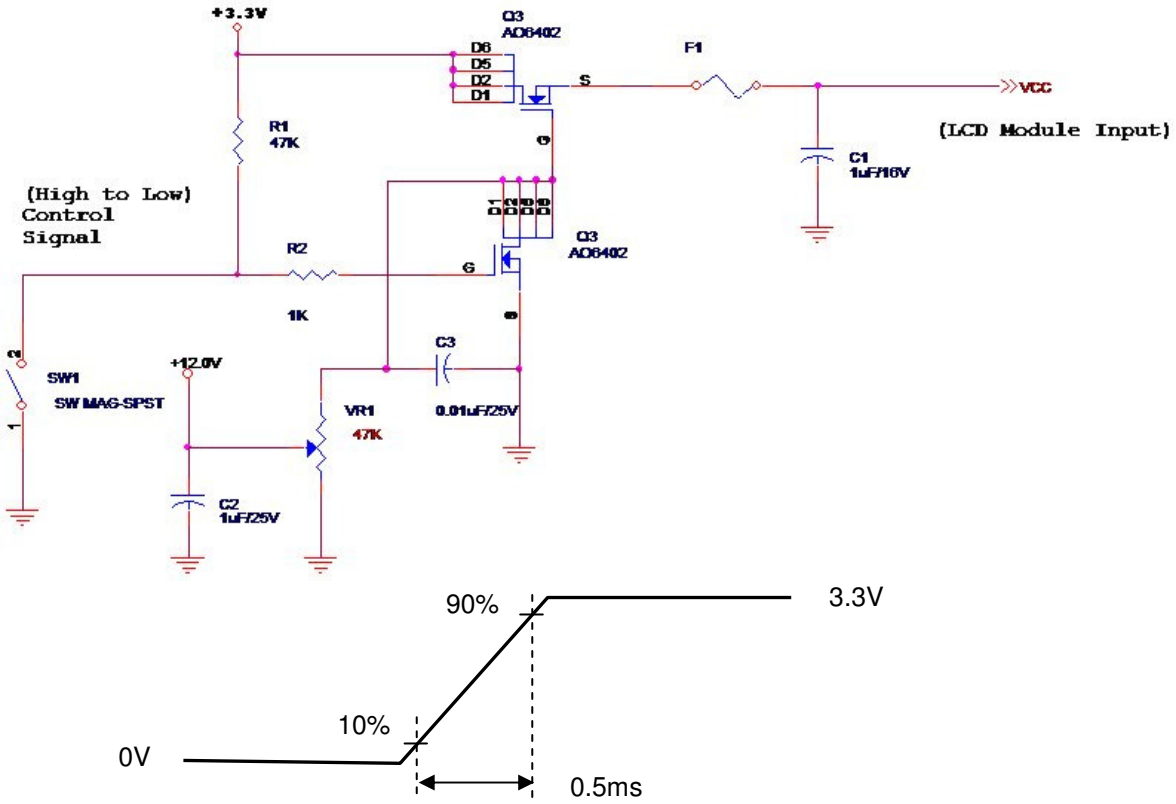
Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.7	[Watt]	Note 1
IDD	IDD Current	-	-	233	[mA]	Note 1
IRush	Inrush Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{white}$)

Note 2 : Measure Condition



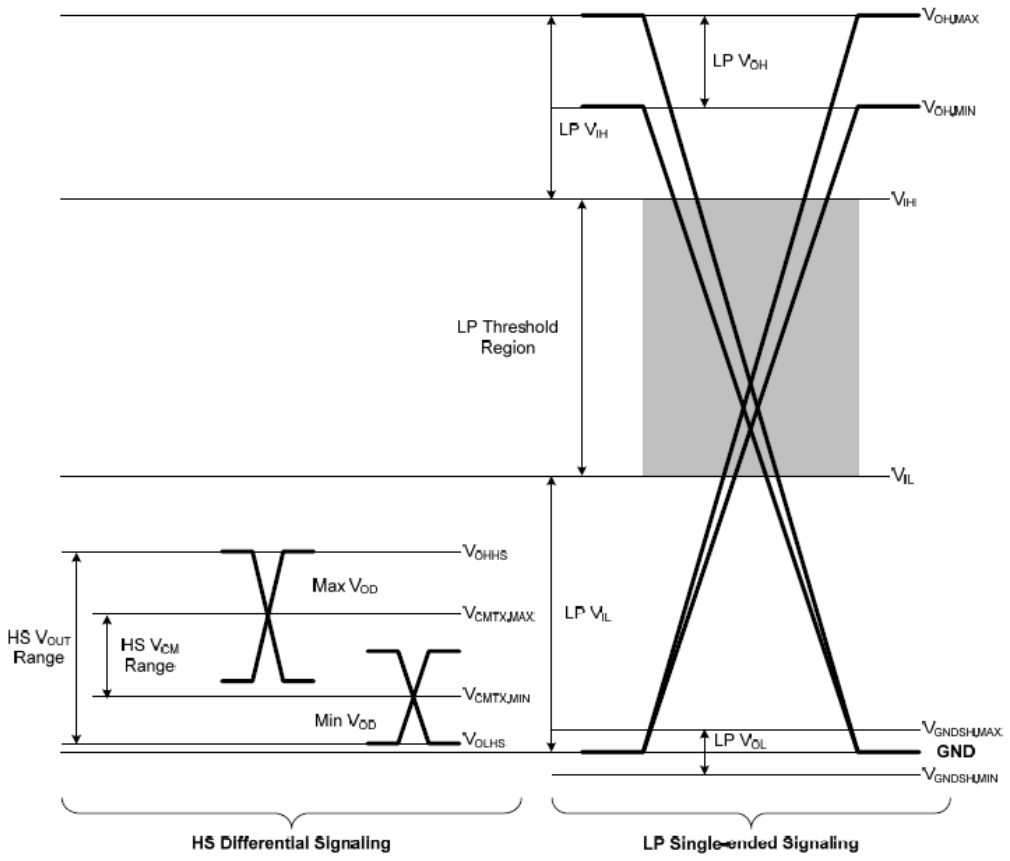
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

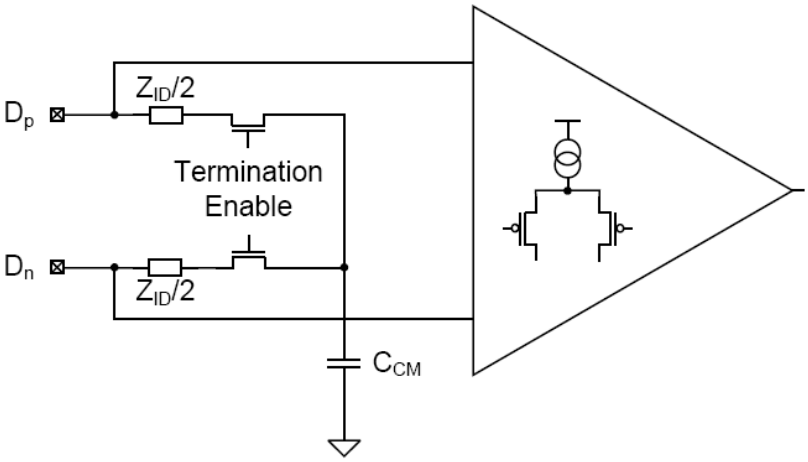
MIPI DC/AC Characteristics are as follows;

MIPI Receiver Differential Input (DC Characteristics)					
Symbol	Parameter	Min	Typ	Max	Unit
BR_{MIPI}	Input data bit rate	200	-	1000	Mbps
V_{CMRX}	Common-mode voltage(HS Rx mode)	70	-	330	mV
V_{IDTH}	Differential input high threshold (HS Rx mode)	-	-	70	mV
V_{IDTL}	Differential input low threshold (HS Rx mode)	-70	-	-	mV
$\lvert V_{IDM} \rvert$	Differential input voltage range (HS Rx mode)	70	-	500	mV
V_{IHHS}	Single-end input high voltage (HS Rx mode)	-	-	460	mV
V_{ILHS}	Single-end input low voltage (HS Rx mode)	-40	-	-	mV
Z_{ID}	Differential input impedance	80	100	125	Ω
V_{IHLP}	Logic 1 input voltage (LP Rx mode)	880			mV
V_{ILLP}	Logic 0 input voltage (LP Rx mode)			550	mV
V_{OH}	Output high level (LP Tx mode)	1.08	1.2	1.32	V
V_{OL}	Output low level (LP Tx mode)	-50		50	mV



MIPI Receiver Differential Input (AC Characteristics)						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz		-	-	100	mV
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz ~ 450MHz		-50	-	50	mV
C_{CM}	Common-mode termination		-	-	60	pF
UI_{INST}	UI instantaneous		1		12.5	ns

HS RX Scheme

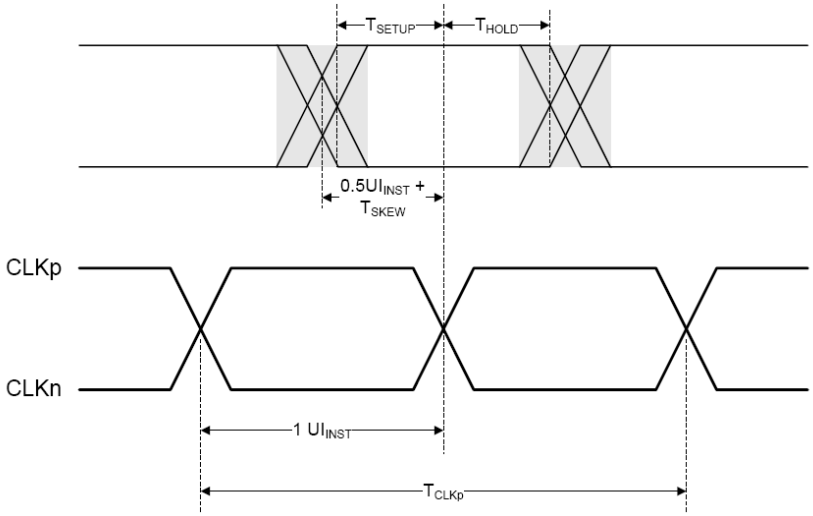


Symbol	Parameter	Min	Typ	Max	Unit	Notes
$T_{SKEW[TX]}$	Data to Clock Skew (mesured at transmitter)	-0.15		0.15	UI_{INST}	1
$T_{SETUP[RX]}$	Data to Clock Setup Time (receiver)	0.15			UI_{INST}	2
$T_{HOLD[RX]}$	Data to Clock Hold Time (receiver)	0.15			UI_{INST}	2

Note:

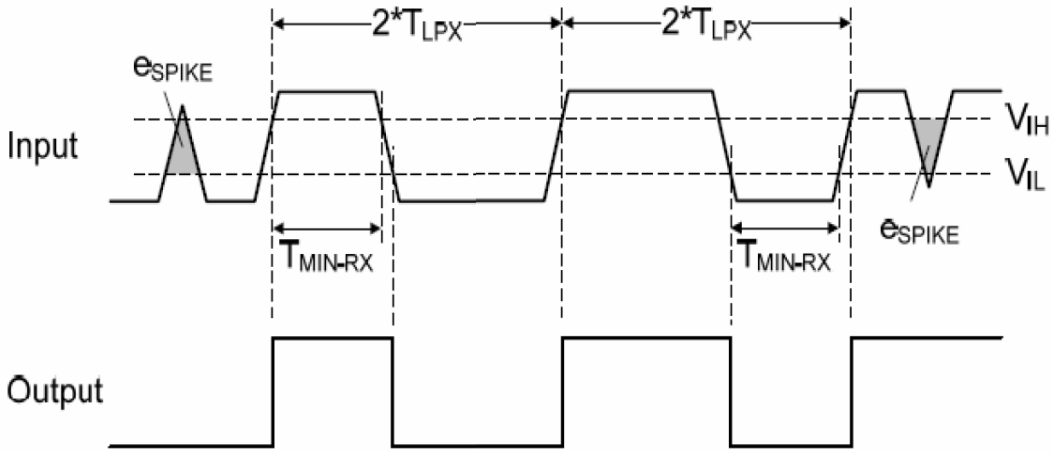
1. Total silicon and package delay budget of $0.3*UI_{INST}$
2. Total setup and hold window for receiver of $0.3*UI_{INST}$

High Speed Data Transmission: Data to Clock Timing

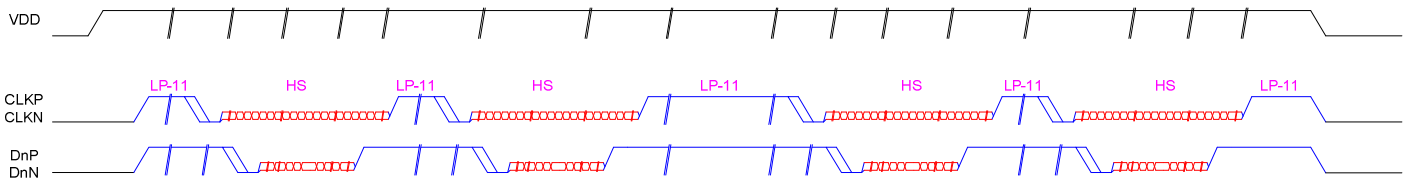


LP Receiver AC Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
e_{SPIKE}	Input pulse rejection		-	-	300	V · ps
T_{MIN-RX}	Minimum pulse width response		50	-	-	ns
V_{INT}	Peak interference amplitude		-	-	200	mV
f_{INT}	Interference frequency		450	-	-	MHz

Input Glitch Rejection of Low-Power Receivers



For MIPI data transmission from TX to TCON works properly in video mode, it is suggested that all of MIPI lanes status follow the scheme showed in below. When power is turned on, all lanes (include clock lane) are into LP-11 status first. When TX wants to start transmitting data to TCON, the clock lane is into HS and start toggling. Then data lanes are into HS and data are transmitted. After data transmissions are finished (ex. H-blanking, V-blanking), the data lanes are returned to LP-11, then clock lane, too. The transmission start from LP-11 and stop in LP-11 on all lanes (include clock lane) are the recommended proper operation sequence for MIPI video mode.



The timing definitions are listed in below,

Parameter	Description	Min	Typ	Max	Unit
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60 ns + 52*UI			ns

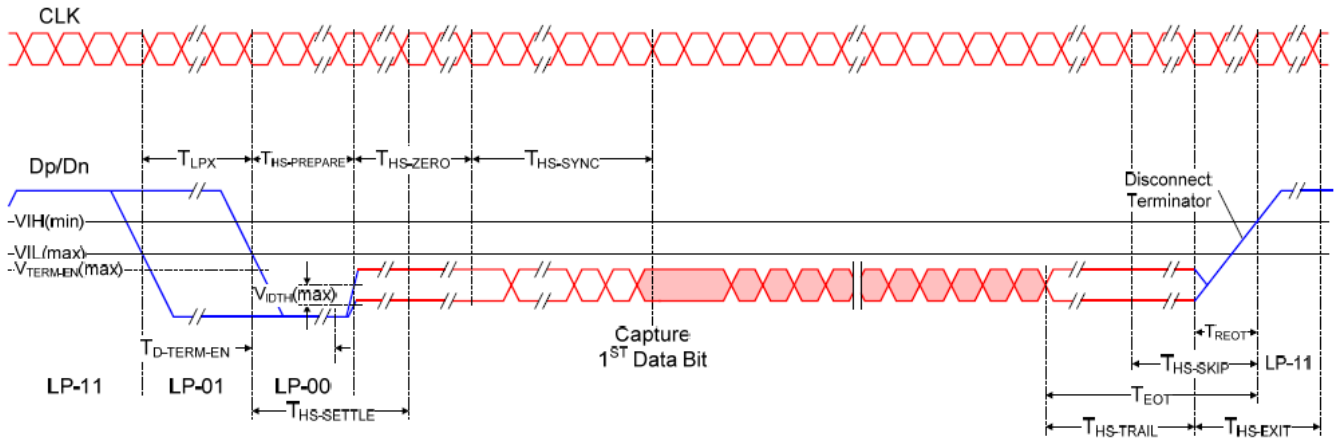
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			35 ns + 4*UI	ns
TEOT	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.			105 ns + 12*UI	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100			ns
THS-SYNC	HS Sync-Sequence '00011101' period		8		UI
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE.	85 ns + 6*UI		145 ns + 10*UI	ns
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60 ns + 4*UI			ns
TLPX	Transmitted length of any Low-Power state period	50			ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	2/3		3/2	
TTA-GET	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*TLPX		ns
TTA-GO	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*TLPX		ns
TTA-SURE	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX		2*TLPX	ns

Note:

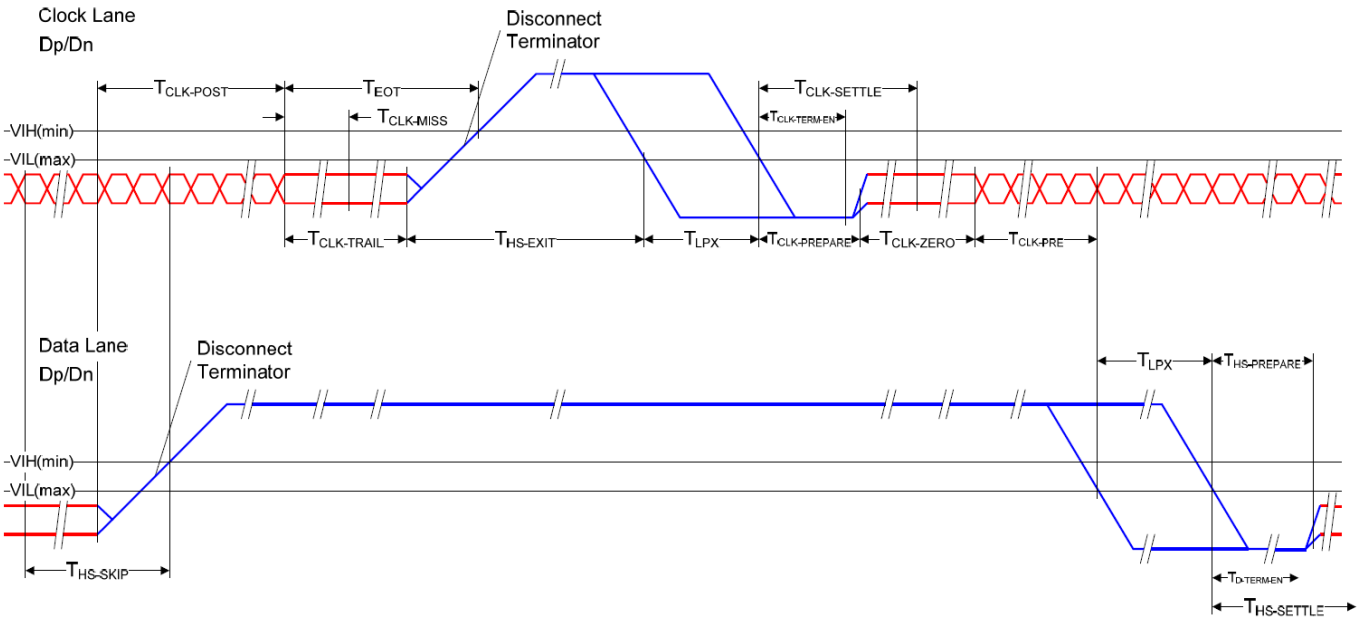
1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

2. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

High-Speed Data Transmission in Bursts



Switching the Clock Lane between Clock Transmission and Low-Power Mode



Turnaround Procedure

5.1.3 Digitizer Panel Power Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Ripple voltage	Vp-p				mV	
Ambient temperature		0	25	60	℃	
Ambient humidity		40	60	80	%	

Notes The Pen Digitizer Unit should always be operated within these ranges.

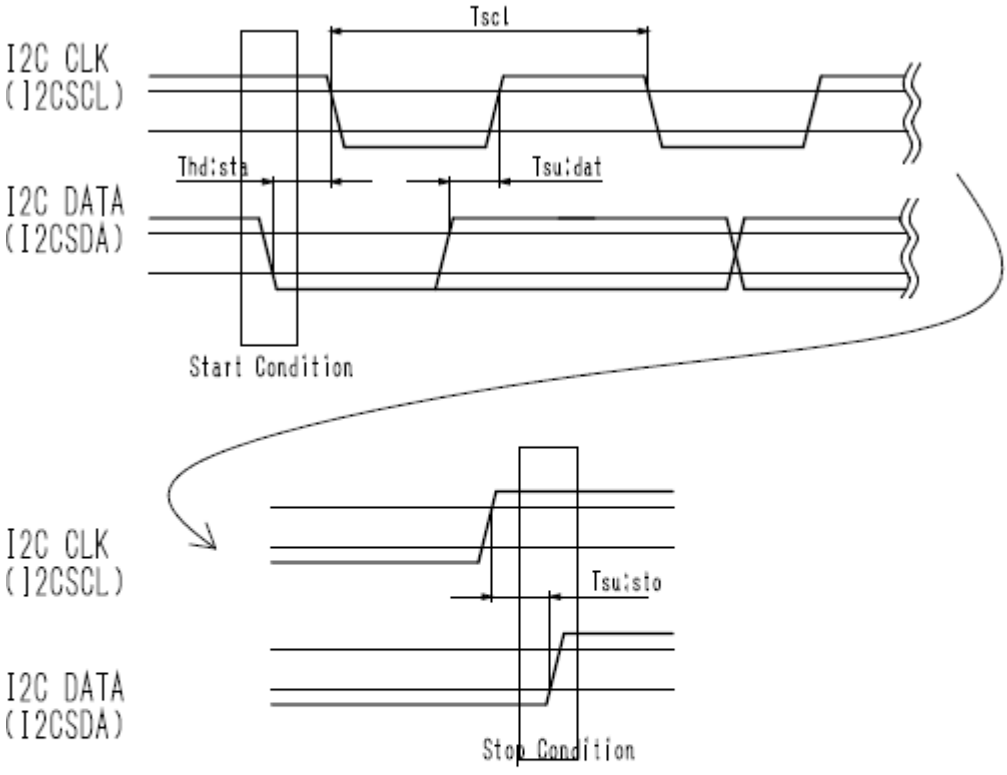
"Typ." Shows the recommended value.

5.1.4 Digitizer Signal Electrical Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit.	Remark
High level output current	I_{OH}			-1	mA	
Low level output current	I_{OL}			5	mA	
High level input voltage	V_{IH}	0.8 V_{DD}		V_{DD}	V	
Low level input voltage	V_{IL}	0	-	0.2 V_{DD}	V	
High level output voltage	V_{OH}	V_{DD} -0.5	-	V_{DD}	V	I_{OH} -100 μA
Low level output voltage	V_{OL}	0	-	0.5	V	I_{OL} 400 μA
High level input leak current				3	μA	$V_{IN} = V_{DD}$
Low level input leak current				-3	μA	V_{IN} = 0V

. Electrical Timing of I^2C signal

(fastmode)



Thd:sta(StartCondition Holdtime)
Tsu:dat(Data Setuptime))
Tsu:sto(StopiCondition Setuptime)

Name	Min	Typ	Max	Unit	Remark
Tscl			400	kHz	
sta			0.6	ms	
dat	100			ns	
sto	0.6			ms	

5.1.5 Dynamic contrast ratio Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
PWM_IN Input Frequecy	**PWM_IN**	200	--	16K	[Hz]	
PWM_IN Input High Level		1.8	--	--	[Volt]	
PWM_IN Input Low Level		--	--	0.5	[Volt]	
Input Duty Cycle		5	--	100	%	
PWM_OUT Output Frequency	**PWM_OUT**	200	--	16K	[Hz]	
PWM_OUT Output Voltage High Level		2	--	--	[Volt]	
PWM_OUT Output Voltage Low Level		--	--	0.5	[Volt]	
PWM_OUT Output Duty Cycle		5		100	%	**CABA disable**
PWM_OUT Output Duty Cycle		TBD*		100	%	**CABA enable**

*** Min. PWM_Out_Duty_Cycle = Min._System_Input_PWM_Duty * Min._DCR_Efficency.**

Ex. If Min._System_Input_PWM_Duty=5% and Min._DCR_Efficency=70%, Min. PWM_Out_Duty_Cycle=3.5%

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	**1.92**	[Watt]	(Ta=25℃@450nits)
Backlight Power Consumption	PLED	-	-	**3.26**	[Watt]	(Ta=25℃@700nits)
LED Life-Time	N/A	**10,000**	-	-	Hour	(Ta=25℃@450nit) Note1.
LED Forward Voltage	VF	**2.6**	**3.0**	**3.3**	[Volt]	(Ta=25℃)
LED Forward Voltage of every LED string	VF-string	-	**24**	**26.4**	[Volt]	(Ta=25℃) Note2.
LED Forward Current	IF	**12**	**-**	**18.5**	[mA]	(Ta=25℃)

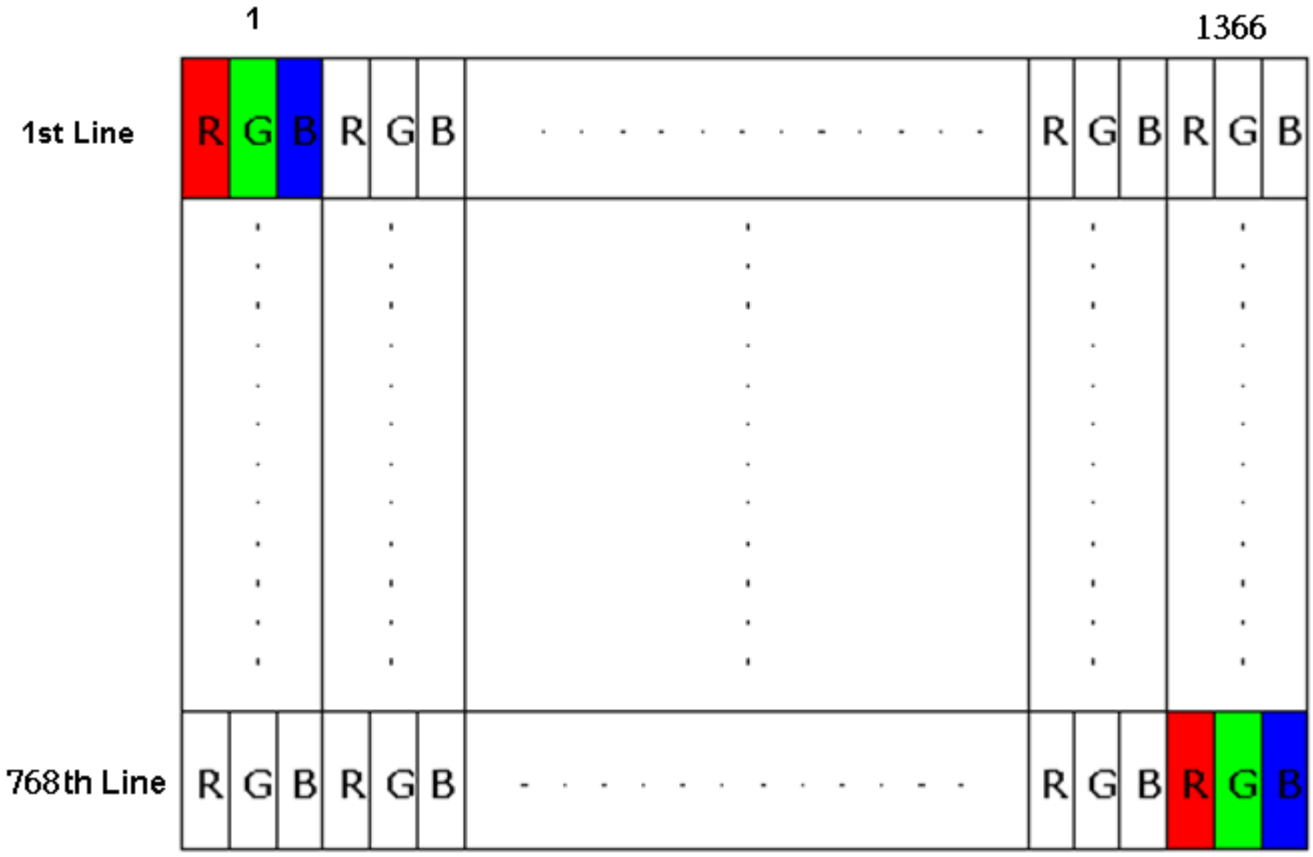
Note 1. The LED life-time define as the estimated time to 50% degradation of initial luminous.

Note 2. Every LED string consists of 8 pcs LED chip

6. Signal Interface Characteristic

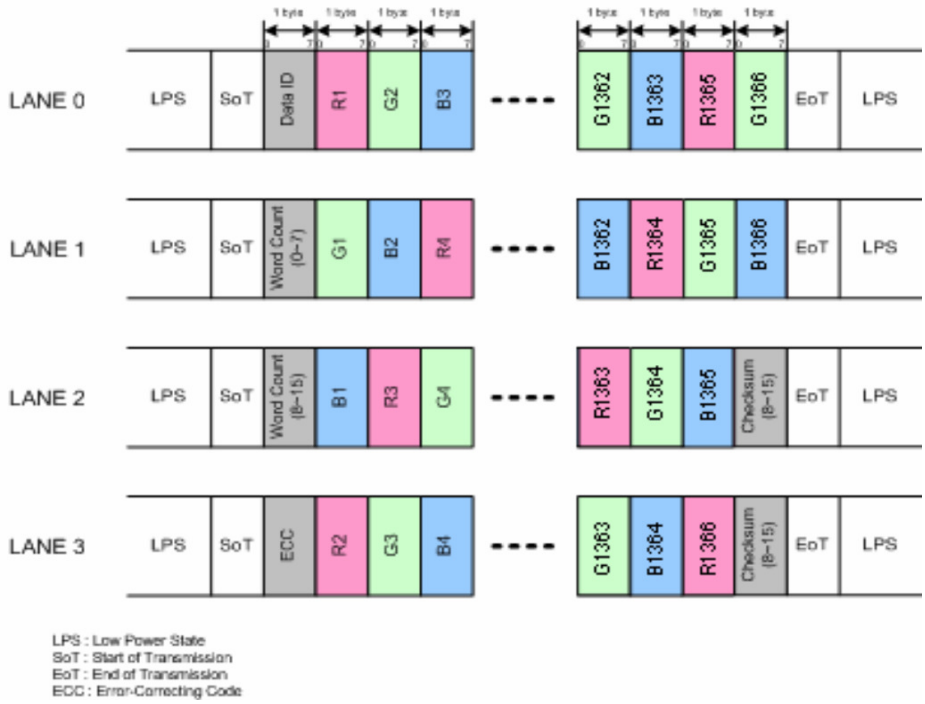
6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Panel Input Data Format

Input Pixel Stream Format (1366RGB in 4 Lanes with RGB 8-8-8 format)



6.3 Integration Interface Requirement

6.3.1 MIPI Connector Description

Physical interface is described as for the connector on module.

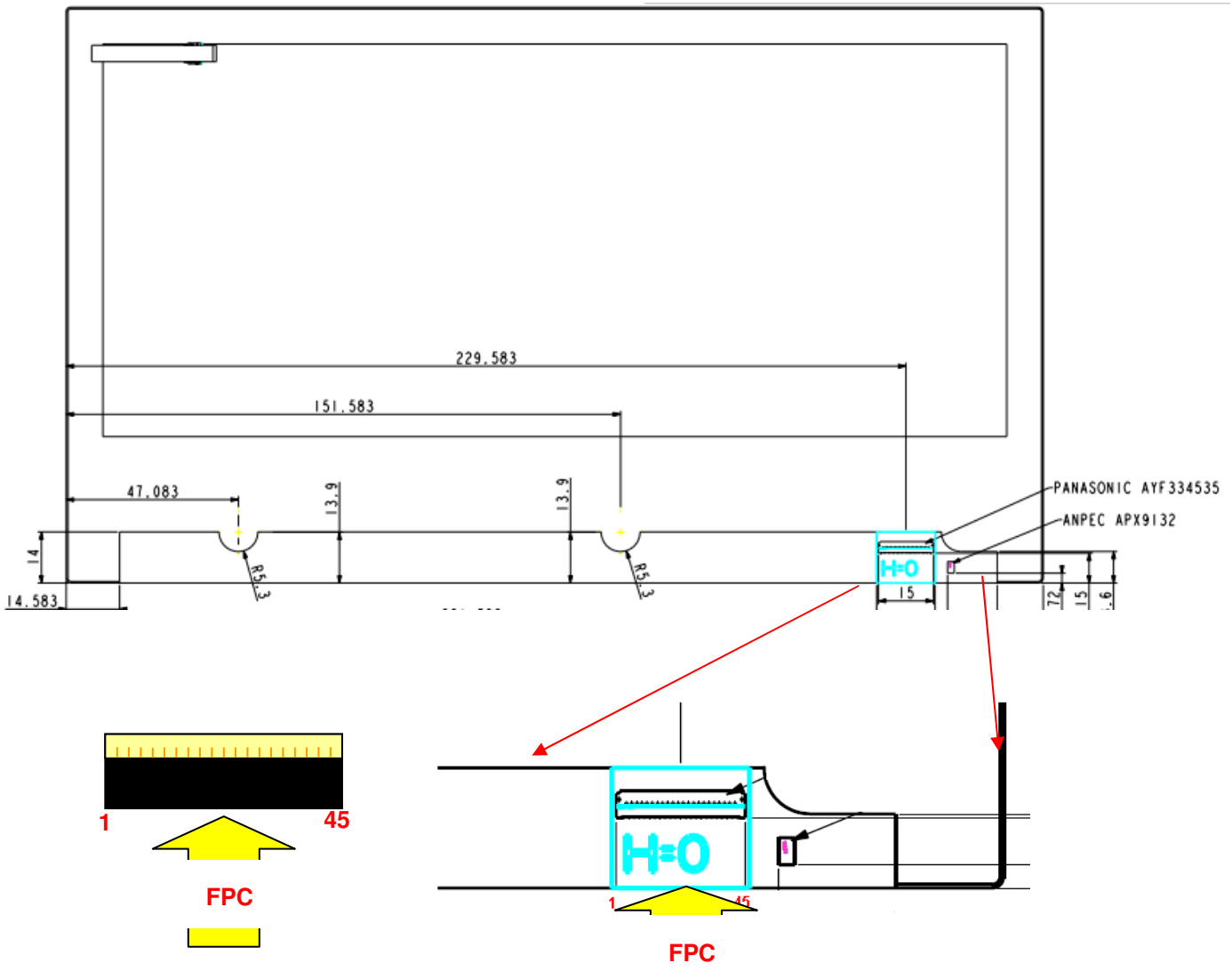
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	Panasonic
Type / Part Number	AYF334535
Mating Housing/Part Number	FPC

6.3.2 MIPI Pin Assignment

MIPI is a differential signal technology for LCD interface and high speed data transfer device.

	Signal Name	Description
1	VDD	Power Supply +3.3V
2	VDD	Power Supply +3.3V
3	VDD	Power Supply +3.3V
4	NC	No Connection (Reserve)
5	Tcon_VDD	Tcon +1.2 V Power
6	Tcon_VDD	Tcon +1.2 V Power
7	GND	Ground
8	BL_PWM_TCON_IN	System PWM signal input
9	GND	Ground
10	BL_PWM_TCON_OUT	Panel PWM signal output
11	GND	Ground
12	3V_VDD_EN	Power Supply +3.3V
13	PVID	Customer require
14	GND	Ground
15	SDA	EDID Data Input
16	SCL	EDID Clock Input
17	GND	Ground
18	DSI_D2P/Rx-IN2P	+MIPI differential data input
19	DSI_D2N/Rx-IN2N	-MIPI differential data input
20	GND	Ground
21	DSI_D1P/Rx-IN1P	+MIPI differential data input
22	DSI_D1N/Rx-IN1N	-MIPI differential data input
23	GND	Ground
24	DSI_CLKP/Rx-CLKP	+MIPI differential clock input
25	DSI_CLKN/Rx-CLKN	-MIPI differential clock input
26	GND	Ground
27	DSI_D0P/Rx-IN0P	+MIPI differential data input
28	DSI_D0N/Rx-IN0N	-MIPI differential data input
29	GND	Ground
30	DSI_D3P/Rx-IN3P	+MIPI differential data input
31	DSI_D3N/Rx-IN3N	-MIPI differential data input
32	GND	Ground
33	GND	Ground
34	NC/Aging	Auo test pin
35	VDD_H	Hall sensor power
36	INT_H	Hall sensor signal feedback
37	VLED-CH1	BL Feedback pin
38	VLED-CH2	BL Feedback pin
39	VLED-CH3	BL Feedback pin
40	VLED-CH4	BL Feedback pin
41	VLED-CH5	BL Feedback pin
42	VLED-CH6	BL Feedback pin
43	NC	No Connection (Reserve)
44	back light input power	LED Anode
45	back light input power	LED Anode



Note1: Input signals shall be low or High-impedance state when VDD is

6.3.3 Digitizer Connector Description

Connector on controller: 20397-008E-02 (i-PEX) or equivalent

6.3.4 Digitizer Pin Assignment

Pin	NAME	IN/OUT	FUNCTION
1	FWE	I	Flash ROM Compulsory Rewrite
2	I2CSCL	I / O	I^2C Clock Signal
3	I2CSDA	I / O	I^2C Data Signal
4	PDCT	O	Pen Detect Signal
5	I2CIRQ	I / O	I^2C Data Ready Signal
6	RES	I	Reset Signal
7	V_{DD}		Power Supply
8	GND		Ground

FWE Flash ROM Compulsory Rewrite
Must be grounded at the Host.
("Low" for normal operation.
When set to "High", Pen Digitizer Unit is in the compulsory rewrite mode.)

I2CSCL I^2C Clock Signal
Open drain. Must be inserted pull-up resister at the Host.

I2CSDA I^2C Data Signal
Open drain. Must be inserted pull-up resister at the Host.

PDCT Pen Detect Output Signal
This is set to "HIGH" while Pen Digitizer Unit detects pen.

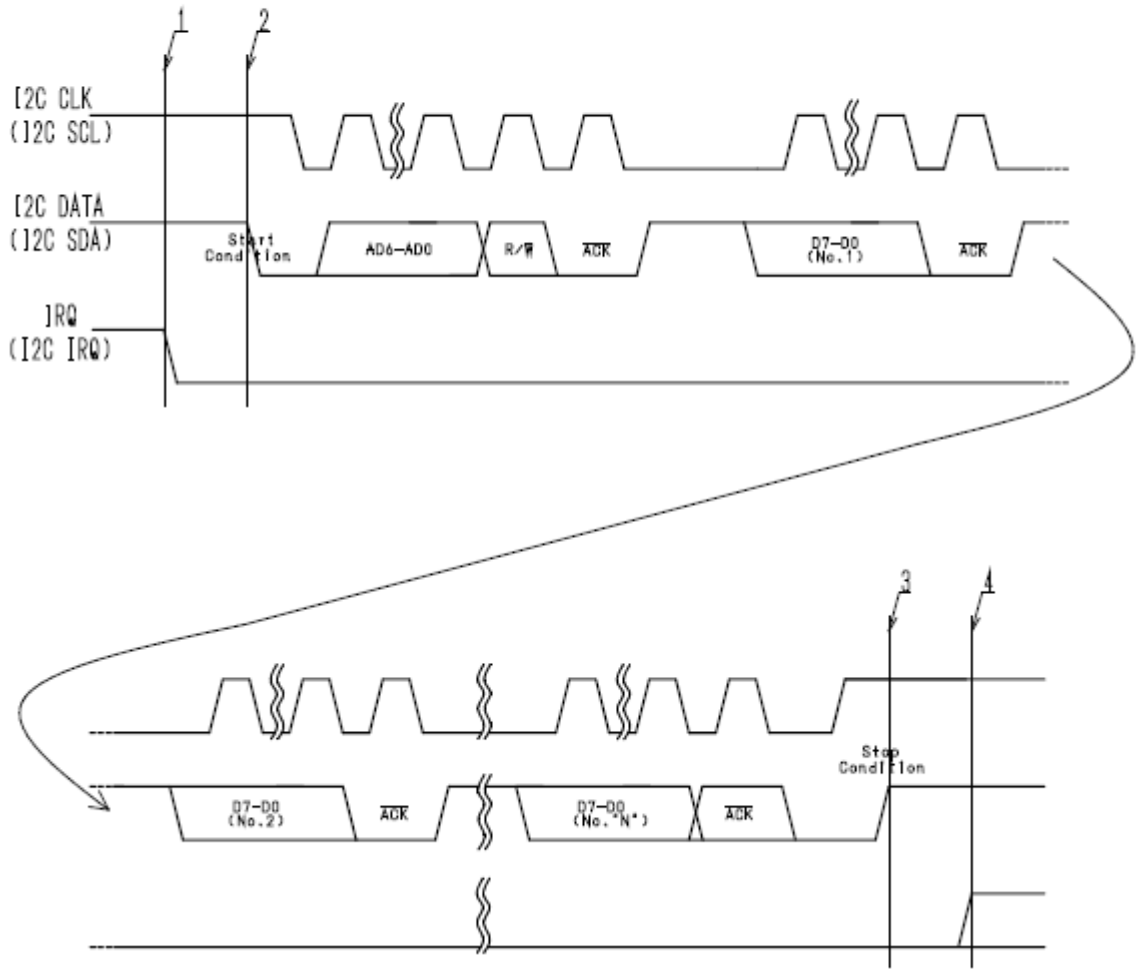
I2CIRQ I^2C Data Ready Signal (IRQ / ATTN)
This is set to "Low" when I^2C slave data ready to send.
Open drain. Must be inserted pull-up resiter at the Host.

RES Reset Signal
Pen Digitizer Unit stops operating when RES is set to "LOW".
Input "system power on reset" signal.

V_{DD} Power Supply.

Transfer Sequence

1. I²C coordinate data ready by Pen Digitizer.
2. Read coordinate data (= Max No."N") by master device.
3. Generate Stop Condition by master device.
4. IRQ control "L": coordinate data exists, "H":No coordinate data by Pen Digitizer.



ST	AD6-AD0	R	!ACK	D7-D0 (No.1)	!ACK	D7-D0 (No.2)	!ACK	…	D7-D0 (No."N")	SP

<Note 1> The 1st read data byte is always data No.1 after the I²C master device generated the start condition..

6.4 MIPI Interface Timing

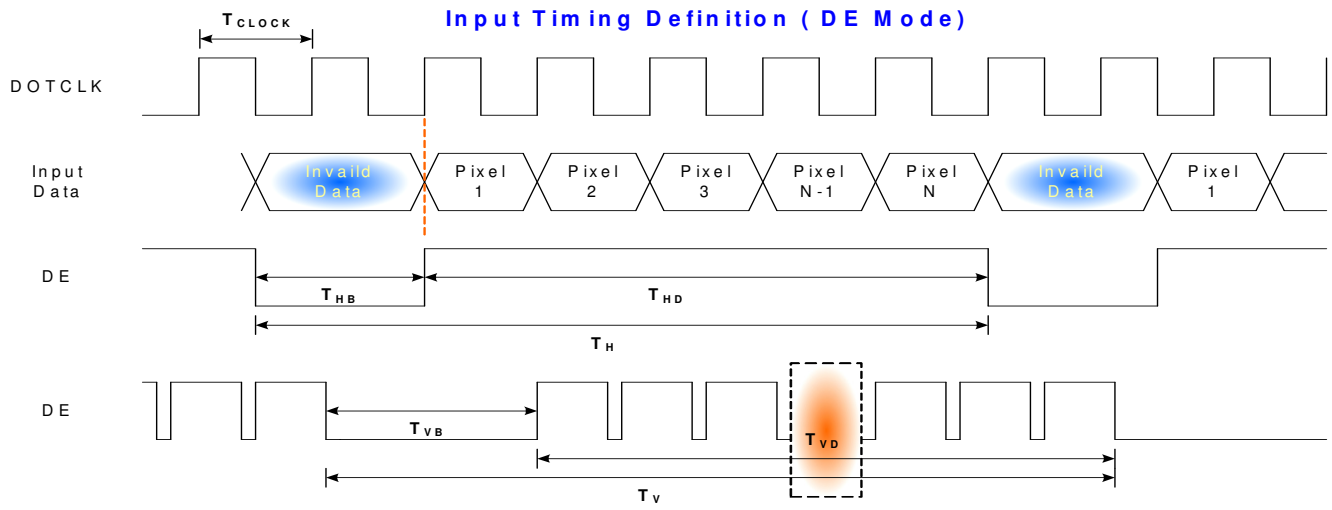
6.4.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T_{Clock}	67.3	69.3	80.5	MHz
Vertical Section	Period	T_V	784	793	862	T_{Line}
	Active	T_{VD}	768			
	Blanking	T_{VB}	16	25	94	
Horizontal Section	Period	T_H	1430	1454	1557	T_{Clock}
	Active	T_{HD}	1366			
	Blanking	T_{HB}	64	88	191	

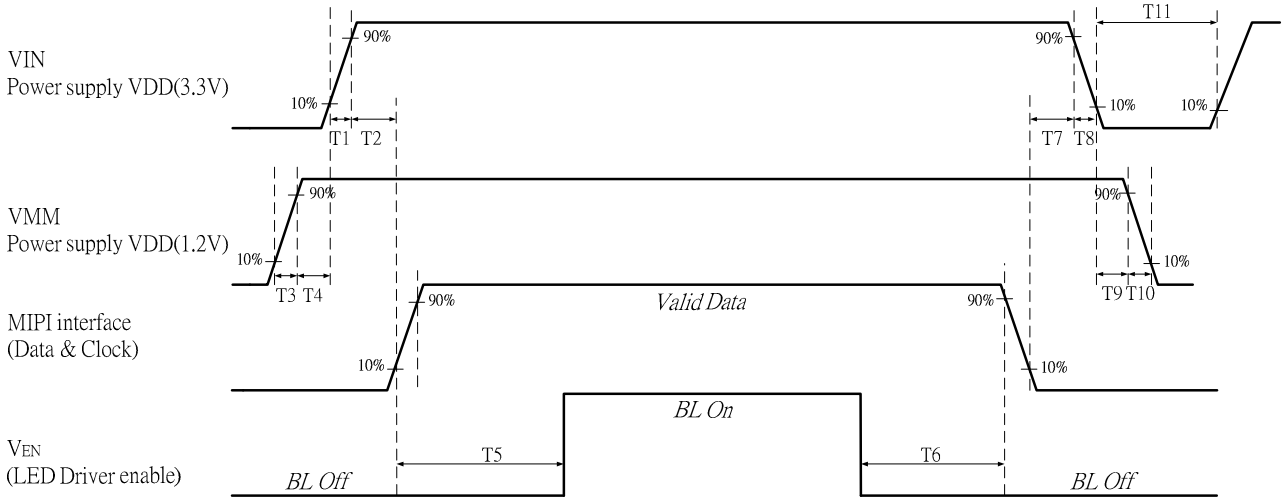
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.



Power Sequence Timing			
Parameter	Value		Units
	Min.	Max.	
T1	0.5	10	ms
T2	100	-	
T3	0.5	10	
T4	0	50	
T5	200	-	
T6	200	-	
T7	0	50	
T8	0	10	
T9	0	10	
T10	0	10	
T11	500	-	

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 95%RH, 240h	
High Temperature Operation	Ta= 60℃, Dry, 240h	
Low Temperature Operation	Ta=-20℃, 240h	
High Temperature Storage	Ta= 70℃, 240h	
Low Temperature Storage	Ta= -30℃, 240h	
Thermal Shock Test	Ta=-30℃to 70℃, Duration at 30 min, 20 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

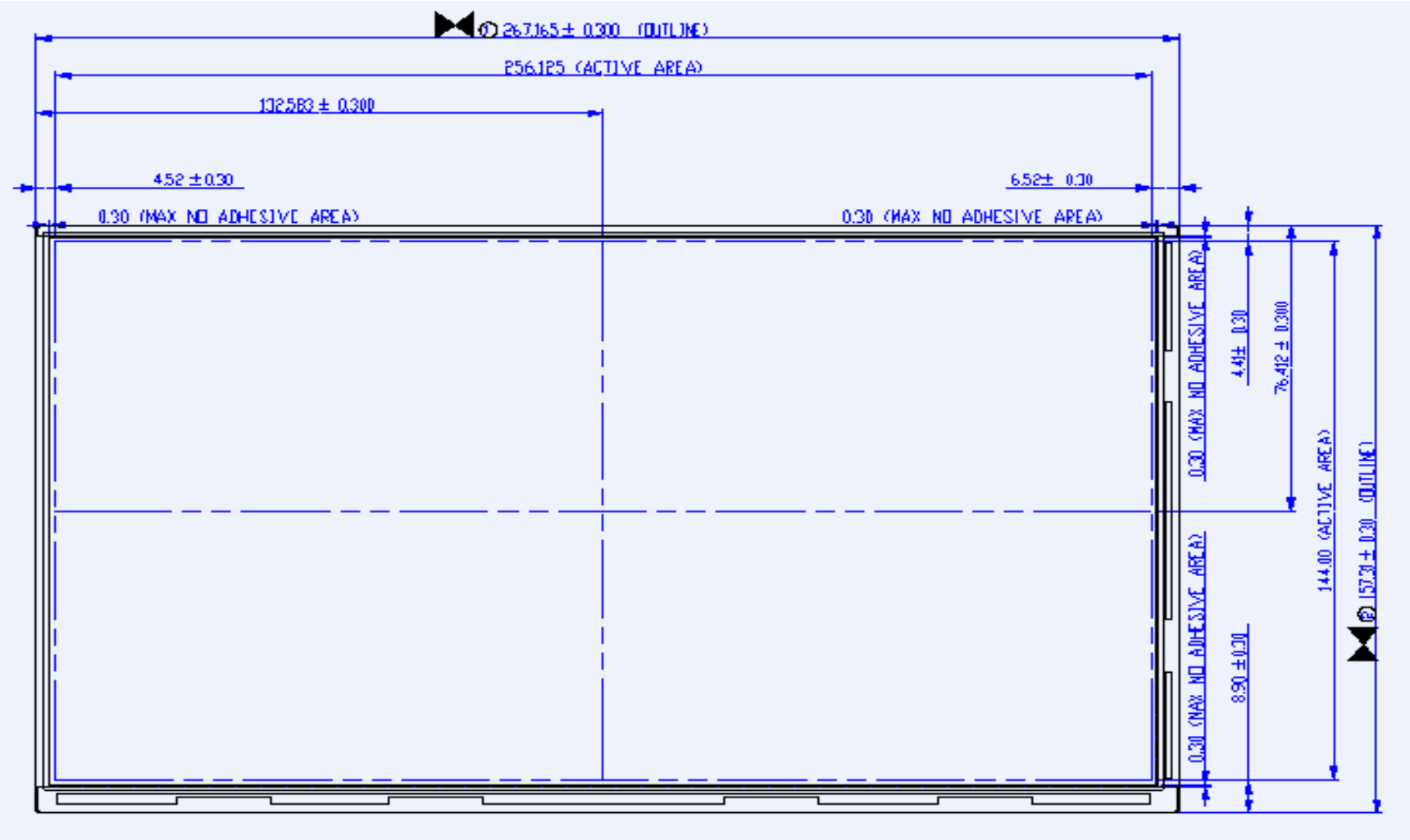
. Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

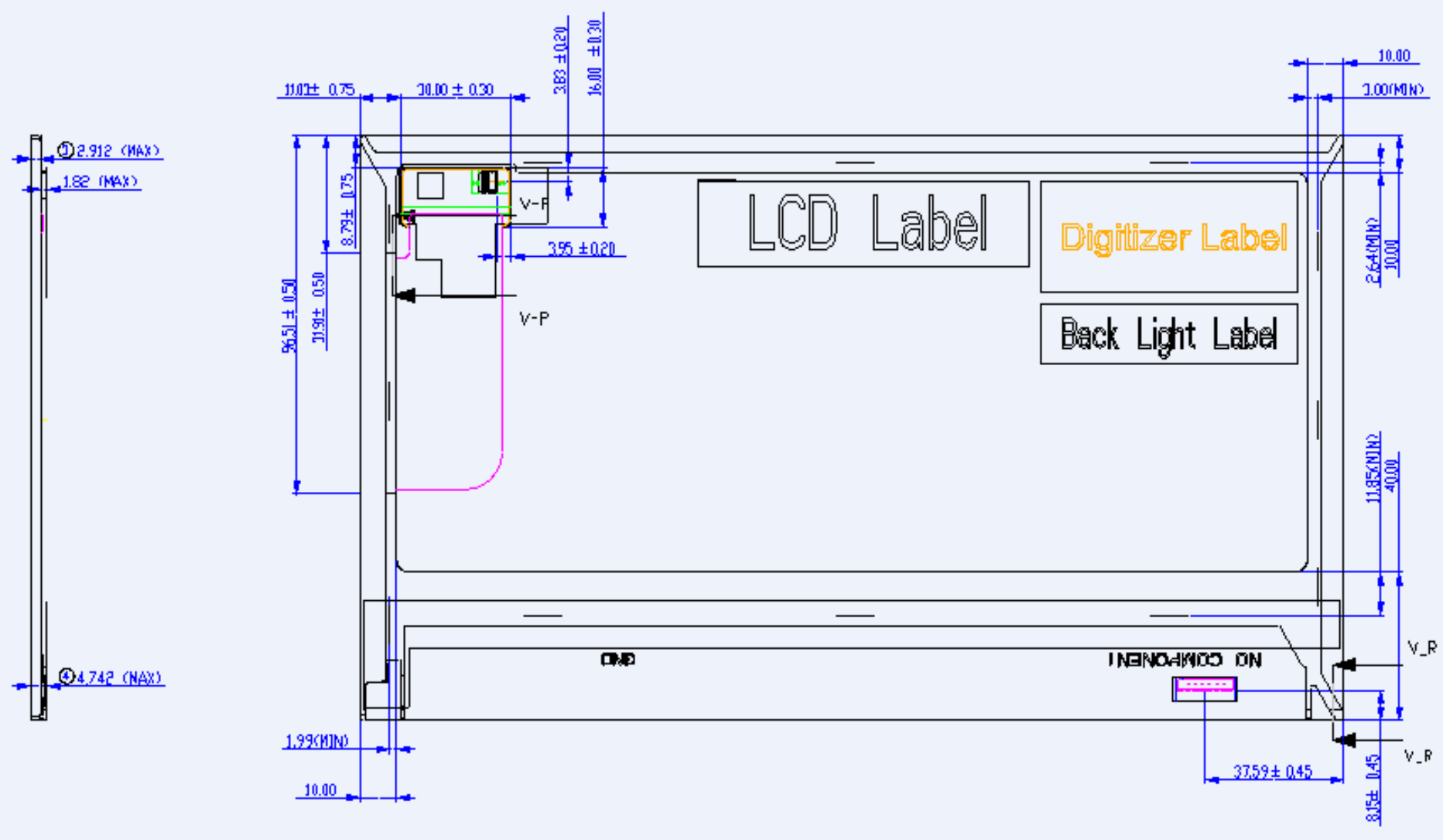
8.Mechanical Characteristics

LCM Outline Dimension

8.1 Standard Front View



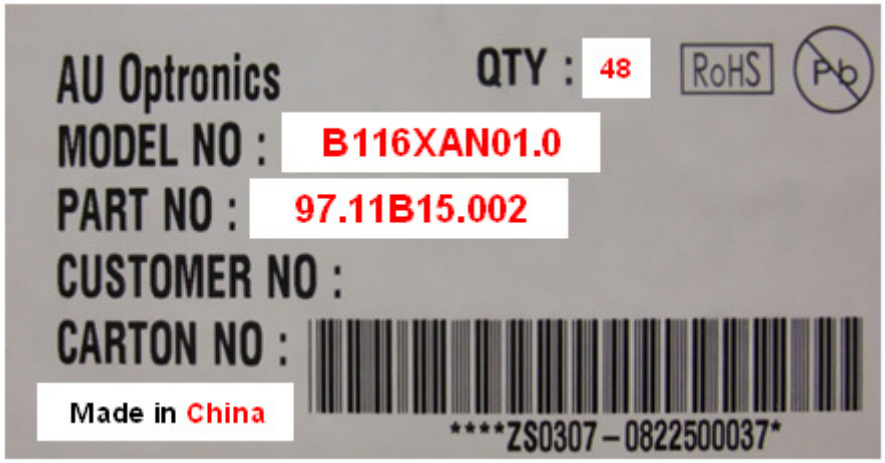
8.2 Standard Rear View



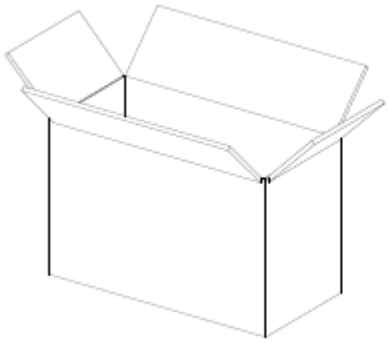
9. Shipping and Package

9.1 Shipping Label Format

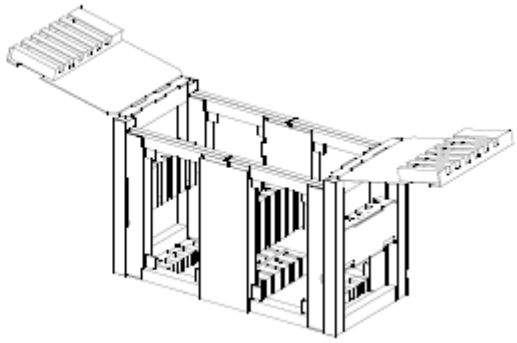
9.2 Carton Label Format



9.3 Carton Package



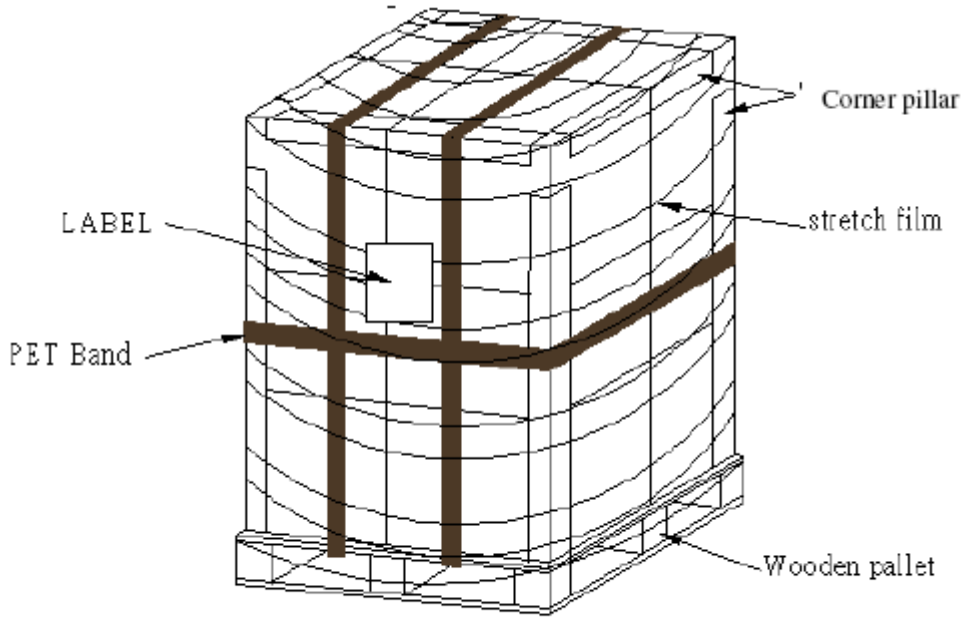
Carton P/N : 81.11B07.003



Cushion P/N : 83.11B05.001

- Pallet : 1150mm*840mm*132mm
- Stretch film : 500mm (W)*300M (L)
- Corner angle : L type fiber board
- PET band : 19mm (W)
- Label : 220mm* 200mm

9.4 Shipping Package of Palletizing Sequence



單層 pallet 打棧示意圖

10. Appendix

10.1 EDID Description

B116XAN01 0 EDID Code

Address	FUNCTION	Value	Value
HEX		HEX	BIN
00	Header	00	00000000
01		FF	11111111
02		FF	11111111
03		FF	11111111
04		FF	11111111
05		FF	11111111
06		FF	11111111
07		00	00000000
08	EISA Manuf. Code LSB	06	00000110
09	Compressed ASCII	AF	10101111
0A	Product Code	5C	01011100
0B	hex, LSB first	10	00010000
0C	32-bit ser #	00	00000000
0D		00	00000000
0E		00	00000000
0F		00	00000000
10	Week of manufacture	00	00000000
11	Year of manufacture	15	00010101
12	EDID Structure Ver.	01	00000001
13	EDID revision #	04	00000100
14	Video input def. (digital I/P, non-TMDS, CRGB)	A0	10100000
15	Max H image size (rounded to cm)	1A	00011010
16	Max V image size (rounded to cm)	0E	00001110
17	Display Gamma (=(gamma*100)-100)	78	01111000
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	02	00000010
19	Red/green low bits (Lower 2:2:2:2 bits)	1C	00011100
1A	Blue/white low bits (Lower 2:2:2:2 bits)	F5	11110101
1B	Red x (Upper 8 bits)	97	10010111
1C	Red y/ highER 8 bits	58	01011000
1D	Green x	50	01010000
1E	Green y	8E	10001110
1F	Blue x	27	00100111
20	Blue y	27	00100111
21	White x	50	01010000
22	White y	54	01010100

23	Established timing 1	00	00000000
24	Established timing 2	00	00000000
25	Established timing 3	00	00000000
26	Standard timing #1	01	00000001
27		01	00000001
28	Standard timing #2	01	00000001
29		01	00000001
2A	Standard timing #3	01	00000001
2B		01	00000001
2C	Standard timing #4	01	00000001
2D		01	00000001
2E	Standard timing #5	01	00000001
2F		01	00000001
30	Standard timing #6	01	00000001
31		01	00000001
32	Standard timing #7	01	00000001
33		01	00000001
34	Standard timing #8	01	00000001
35		01	00000001
36	Pixel Clock/10000 LSB	12	00010010
37	Pixel Clock/10000 USB	1B	00011011
38	Horz active Lower 8bits	56	01010110
39	Horz blanking Lower 8bits	58	01011000
3A	HorzAct:HorzBlnk Upper 4:4 bits	50	01010000
3B	Vertical Active Lower 8bits	00	00000000
3C	Vertical Blanking Lower 8bits	19	00011001
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	00110000
3E	HorzSync. Offset	30	00110000
3F	HorzSync.Width	20	00100000
40	VertSync.Offset : VertSync.Width	36	00110110
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000
42	Horizontal Image Size Lower 8bits	00	00000000
43	Vertical Image Size Lower 8bits	90	10010000
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000
45	Horizontal Border (zero for internal LCD)	00	00000000
46	Vertical Border (zero for internal LCD)	00	00000000
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000
48	Detailed timing/monitor	00	00000000
49	descriptor #2	00	00000000
4A		00	00000000
4B		0F	00001111
4C		00	00000000

4D		00	00000000
4E		00	00000000
4F		00	00000000
50		00	00000000
51		00	00000000
52		00	00000000
53		00	00000000
54		00	00000000
55		00	00000000
56		00	00000000
57		00	00000000
58		00	00000000
59		20	00100000
5A	Detailed timing/monitor	00	00000000
5B	descriptor #3	00	00000000
5C		00	00000000
5D		FE	11111110
5E		00	00000000
5F	Manufacture	41	01000001
60	Manufacture	55	01010101
61	Manufacture	4F	01001111
62		0A	00001010
63		20	00100000
64		20	00100000
65		20	00100000
66		20	00100000
67		20	00100000
68		20	00100000
69		20	00100000
6A		20	00100000
6B		20	00100000
6C	Detailed timing/monitor	00	00000000
6D	descriptor #4	00	00000000
6E		00	00000000
6F		FE	11111110
70		00	00000000
71	Manufacture P/N	42	01000010
72	Manufacture P/N	31	00110001
73	Manufacture P/N	31	00110001
74	Manufacture P/N	36	00110110
75	Manufacture P/N	58	01011000
76	Manufacture P/N	41	01000001

77	Manufacture P/N	4E	01001110
78	Manufacture P/N	30	00110000
79	Manufacture P/N	31	00110001
7A	Manufacture P/N	2E	00101110
7B	Manufacture P/N	30	00110000
7C		20	00100000
7D		0A	00001010
7E	Extension Flag	00	00000000
7F	Checksum	13	00010011
	SUM to HEX	1600	