Doc. version : **0.8c** (for ES7 or later)
Total pages : 32
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Product Specifications

8.1″ COLOR TFT-LCD Module

MODEL NAME: A081VW01

< ◆ > Preliminary Specification

< > Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0	2006/07/10		First draft.
0.1	2006/09/05	5 ~ 6	Update outline dimension
		7~9	Re-define pin assignment sequence
		20	Update suggested application circuit
		21	Update response time
0.2	2006/10/18	4~5	Update outline dimension and outline drawing
		9	Re-define pin assignment (57~60) sequence
0.3	2007/01/26	4~6	Updated outline dimension and outline drawing (LCD glass: T0.5)
		19	Updated brightness when w/ touch panel
		22~24	Added touch panel spec
0.4	2007/02/13	14~16	Updated recommended register setting
		26~27	Added recommended application circuit
0.4a	2007/03/01	23	Correct reliability test items
0.5	2007/03/13	4~6	Updated outline dimension and drawing (TP: glass:T1.8, DSA: 0.6)
0.6	2007/03/27	3	General Description modification.
		5~6	Updated outline drawing for touch panel FPC length
		7~9	Updated pin description.
		11	Updated dclk frequency and period.
		13 ~ 17	Updated SPI timing, register default esettings and description.
		18	Added Stand-by mode timing.
		28 ~ 29	Updated power on/off sequence.
		30	Added Recommend Register Settings.
0.6a	2007/04/01	5~6	Updated outline drawing for touch panel FPC dimension
0.6b	2007/05/15	5~6	Updated outline drawing for FPC outline
		15	Updated register table default value
		18	Updated register R6 description
		31	Updated recommend register settings
0.7	2007/08/10	10~11	Updated Pin Assignment

		12	Updated Typical Operation Condition
		18	Updated R1 description
		30	Updated application circuit
		33	Updated recommended register settings and sequence
		34	Updated Gamma2.2 Voltage
0.7a	2007/09/11	6	Updated outline drawing, the suggested customer housing design
		23~24	Updated touch panel electronic charistics and life test condition
0.7b	2007/09/27	19	Updated backlight LED driving voltage
0.8	2007/10/17	10	Updated Abolute Maximum Ratings
		19	Updated LED backlight by 4 LEDs serial type
		28	Updated application circuit
		31	Updated Recommand Register Settings
		32	Updated Gamma2.2 Voltage and recommanded resistors.
0.8a	2007/11/19	9	Updated DE mode description
		28	Updated register R516 from 10K to 0 ohm
		31	Updated Recommand Register Settings
0.8b	2008/03/31	20	Define min. to CR and Viewing Angle
0.8c	2008/04/02	7	Updated outline drawing due to BLU label shift

Contents

GENERAL DESCRIPTION

A081VW01 is a amorphous transmissive type TFT (Thin Film Transistor) LCD (Liquid crystal Display). This model is composed of TFT-LCD, drive IC, FPC (flexible printed circuit), backlight and touch panel. This model is the new driving type for 800RGBx300 application.The timing controller and one DCDC controller are integrated inside IC. It is easily to design for consumer product.

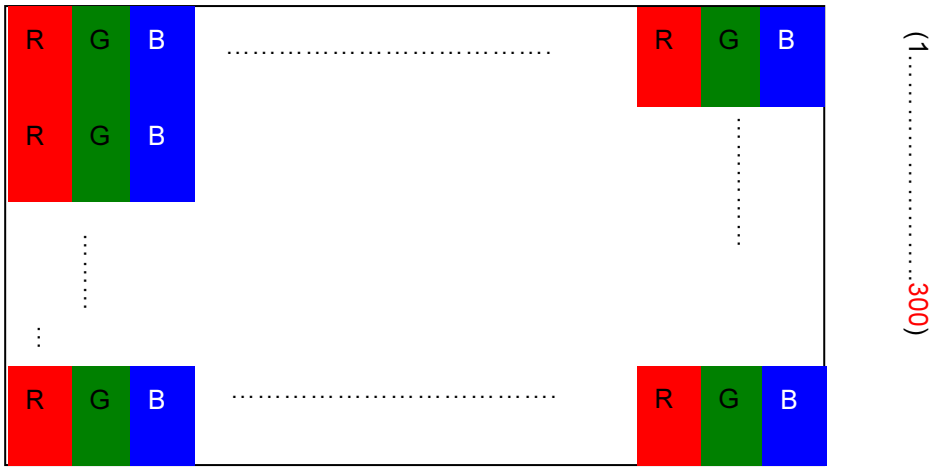
Features

- 8.1-inch display size with aspect ration of 8:3
- Resolution 800RGB x 300 in stripe dot arrangement
- 16.7M color supported
- Paralle 24 / 18-bit RGB interface
- SICC (**S**mart **I**ntegration **C**ascade **C**hip). Support below functions
  - VCOM DC value adjustable
  - SYNC timing adjustable
- Built in timing controller and one DC-DC controller
- Request 180mA for LED blacklight
- Standby mode supported
- 3-wire register setting
- Low power consumption
- RoHS compliant green design

1. General Information

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	800RGB(H)×300(V)	
2	Active Area	mm	192 (H)×72(V)	
3	Screen Size	inch	8.1” (Diagonal)	
4	Dot Pitch	mm	0.24(H)× 0.24(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	16.7M Colors	Note 2
7	Overall Dimension	mm	204.6(H)x 86.2(V)x 8.23(T)	Note 3
8	Weight	g	TBD (typ.)	
9	Panel surface treatment	--	Hard coating	
10	Display Mode	--	Normally White	

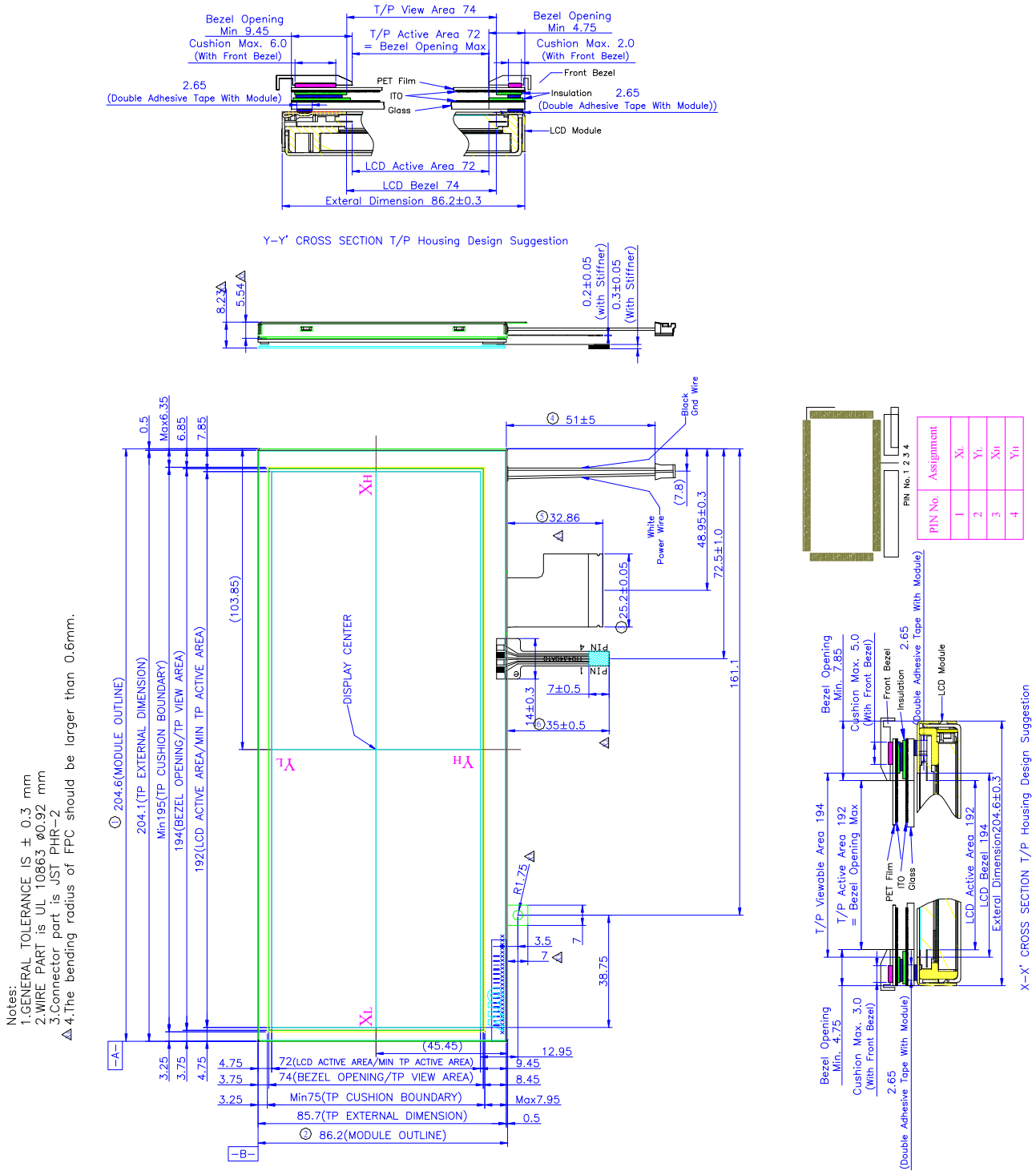
Note 1: Below figure shows dot stripe arrangement.



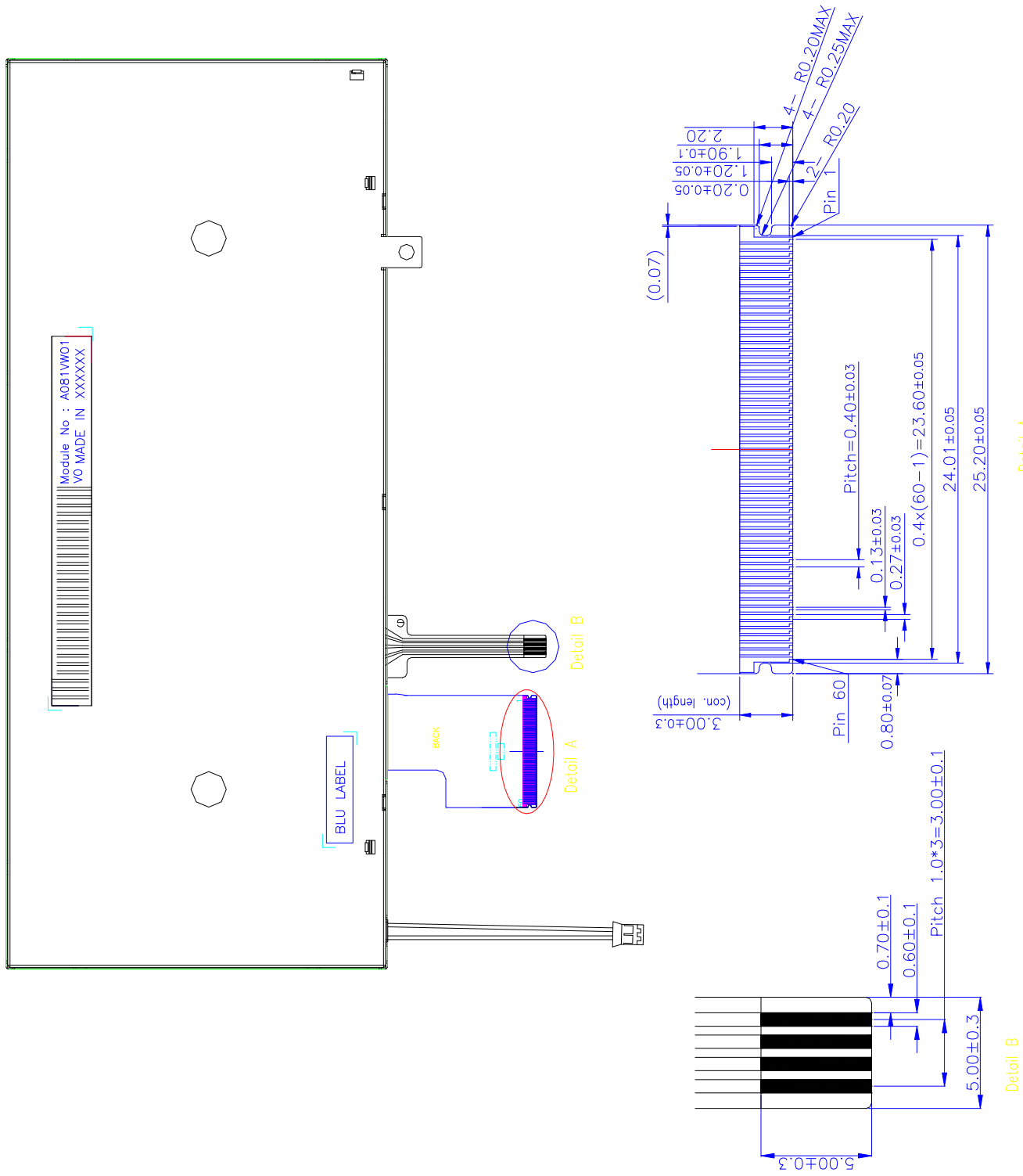
(1 2 3……2398 2399 2400)

Note 2: The full color display depends on 24-bit data signal (pin 4~27).

Note 3: Not include FPC. Refer next page to get further information.



8.1inch Module Outline Dimension – Front View



8.1inch Module Outline Dimension – Back View

2. Electrical Specifications

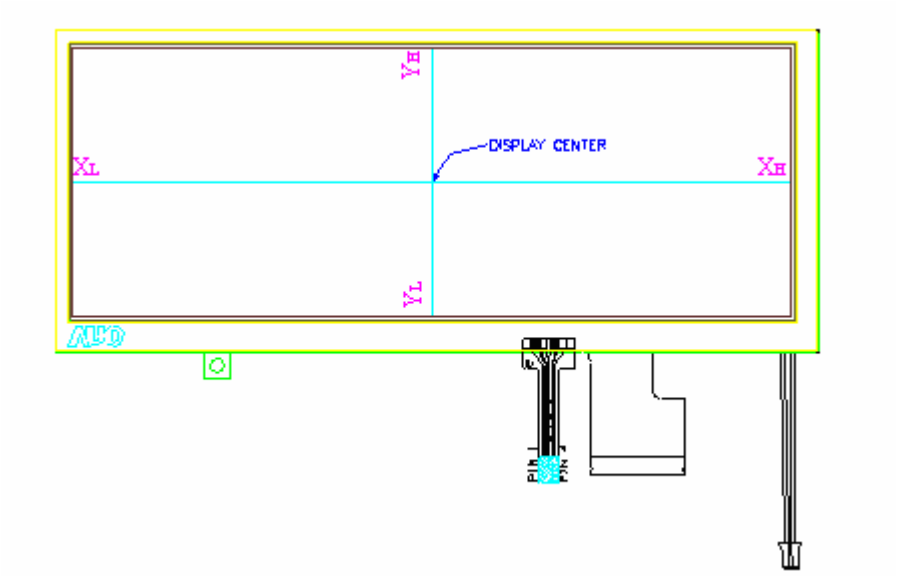
2.1 FPC Pin Assignment (HRS FH27-60H-0.4SH)

Pin no	Symbol	I/O	Description	Remark
1	AGND2	P	Analog Ground	
2	AVDD2	P	Analog Power	
3	VDD	P	Digital Power	
4	R0	I	Data input (LSB)	
5	R1	I	Data input	
6	R2	I	Data input	
7	R3	I	Data input	
8	R4	I	Data input	
9	R5	I	Data input	
10	R6	I	Data input	
11	R7	I	Data input (MSB)	
12	G0	I	Data input (LSB)	
13	G1	I	Data input	
14	G2	I	Data input	
15	G3	I	Data input	
16	G4	I	Data input	
17	G5	I	Data input	
18	G6	I	Data input	
19	G7	I	Data input (MSB)	
20	B0	I	Data input (LSB)	
21	B1	I	Data input	
22	B2	I	Data input	
23	B3	I	Data input	
24	B4	I	Data input	

25	**B5**	**I**	Data input	
26	**B6**	**I**	Data input	
27	**B7**	**I**	Data input (MSB)	
28	**DCLK**	**I**	Data Clock input	
29	**DE**	**I**	Data enable signal (DE mode is with higher prority than HV mode.)	
30	**HSYNC**	**I**	Horizontal sync input. Negative polarity	
31	**VSYNC**	**I**	Vertical sync input. Negative polarity	
32	**SCL**	**I**	Serial communication clock input	
33	**SDA**	**I**	Serial communication data input	
34	**CSB**	**I**	Serial communication chip select	
35	**NC**		Do not connect (Please leave it open)	
36	**VDD**	**P**	Digital Power	
37	**NC**		Do not connect (Please leave it open)	
38	**GND**	**P**	Digital ground	
39	**AGND**	**P**	Analog ground	
40	**AVDD**	**P**	Analog Power	
41	**VCOMin**	**I**	For external VCOM DC input (Optional)	Refer to R1(D7,D6)
42	**NC**		Do not connect (Please leave it open)	
43	**NC**		Do not connect (Please leave it open)	
44	**VCOM**	**I**	For external VCOM DC input (Optional)	Refer to R1(D7,D6)
45	**V10**	**P**	Gamma correction voltage reference	
46	**V9**	**P**	Gamma correction voltage reference	
47	**V8**	**P**	Gamma correction voltage reference	
48	**V7**	**P**	Gamma correction voltage reference	
49	**V6**	**P**	Gamma correction voltage reference	
50	**V5**	**P**	Gamma correction voltage reference	
51	**V4**	**P**	Gamma correction voltage reference	

52	**V3**	**P**	Gamma correction voltage reference	
53	**V2**	**P**	Gamma correction voltage reference	
54	**V1**	**P**	Gamma correction voltage reference	
55	**NC**		Do not connect (Please leave it open)	
56	**VGH**	**P**	Positive power for TFT	
57	**VGL**	**P**	Negative power for TFT	
58	**GVCC**	**P**	Digital Power	
59	**GGND**	**P**	Digital Ground	
60	**CAP**	**C**	Capacitor connect pin	

◆ I : Input, O : Output, P : Power, C: Capacitor



2.2 Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VDD	GND=0	-0.5	5	V	Note 1
	GVCC	GGND=0	-0.5	5	V	Note 1
	AVDD	AGND=0	-0.5	15	V	Note 1
Operating temperature	Topa	--	0	60	℃	Ambient Temperature
Storage temperature	Tstg	--	-25	80	℃	Ambient Temperature

Note 1: Functional operation should be restricted under normal ambient temperature.

2.3 Electrical Characteristics

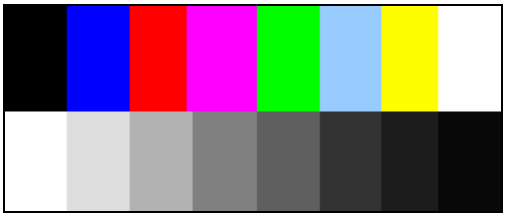
The following items are measured under stable condition and suggested application circuit.

2.3.1. TFT- LCD Typical Operation Condition

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.2	3.3	3.6	V	Pin3 and Pin36
		AVDD	(10.5)	(11)	(11.5)	V	Pin2 and Pin40
		GVCC	3.2	3.3	3.6	V	Pin58
		VGH	(14)	(15)	(16)	V	Pin56
		VGL	(-7.5)	(-7)	(-6.5)	V	Pin57
Input Signal	H Level	V_{IH}	$0.7V_{CC}$	-	V_{CC}	V	
	L Level	V_{IL}	GND	-	$0.3V_{CC}$	V	
VCOM		V_{CDC}	(4.3)	(4.5)	(4.7)	V	DC component
Input Current		I_{VDD}		11	20	mA	Pin3 + Pin36
		I_{AVDD}		8	15	mA	Pin2 + Pin40
		I_{GVCC}		0.02	0.1	mA	Pin58
		I_{VGH}		0.2	0.3	mA	Pin56
		I_{VGL}		0.2	0.3	mA	Pin57

Note: Above every operation range is based on stable operation from suggested application circuit

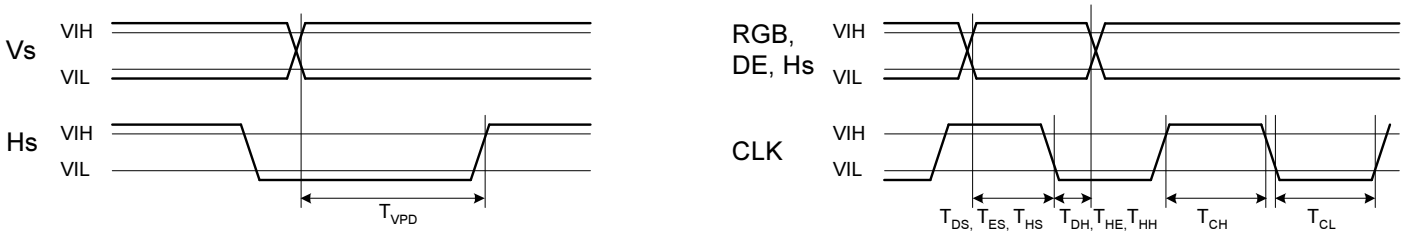
Note: Typical current test pattern



2.4 AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock High time	T_{WCL}		8	-	-	ns
Clock Low time	T_{WCH}		8	-	-	ns
Clock rising time	T_{RCLK}		-	-	1	ns
Clock falling time	T_{ACK}		-	-	1	ns
Hsync setup time	T_{HSU}		5			ns
Hsync hold time	T_{HHD}		10			ns
Vsync setup time	T_{VSU}		0			ns
Vsync hold time	T_{VHD}		2			ns
Data setup time	T_{DSU}		5			ns

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data hold time	T_{DHD}		10			ns
Data enable set-up time	T_{ESU}		4			ns
Data enable hold time	T_{EHD}		2			ns



2.5 RGB Parallel Input Timing

Horizontal Timing

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX	UNIT
DCLK frequency	F_{DCLK}		22	24	27.5	MHz
DCLK period	T_{DCLK}		36.4	41.7	45.5	ns
Hsync Period (= T_{HD} + T_{HBL})	T_H		986	1056	1183	DCLK
Active Area	T_{HD}		-	800	-	DCLK
Horizontal blanking (= T_{HF} + T_{HE})	T_{HBL}		186	256	383	CLK
Hsync front porch	T_{HF}			40	-	CLK
Delay from Hsync to 1st data input (= T_{HW} + T_{HB})	T_{HE}	Function of HDL[5..0] settings	146	216	343	DCLK
Hsync pulse width	T_{HW}		1	128	136	CLK
Hsync back porch	T_{HB}		10	88	342	CLK

Vertical Timing

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vsync period (= T_{VD} + T_{VBL})	T_V		372	380	387	Th
Active lines	T_{VD}			300		Th
Vertical blanking (= T_{VF} + T_{VE})	T_{VBL}		72	80	87	Th
Vsync front porch	T_{VF}		-	17	-	Th
GD start pulse delay	T_{VE}	Function of VDL[3..0] settings	55	63	70	HS
Vsync pulse width	T_{VW}		1	2	20	Th
Hsync/ Vsync phase shift	T_{VPD}		2	320	-	CLK

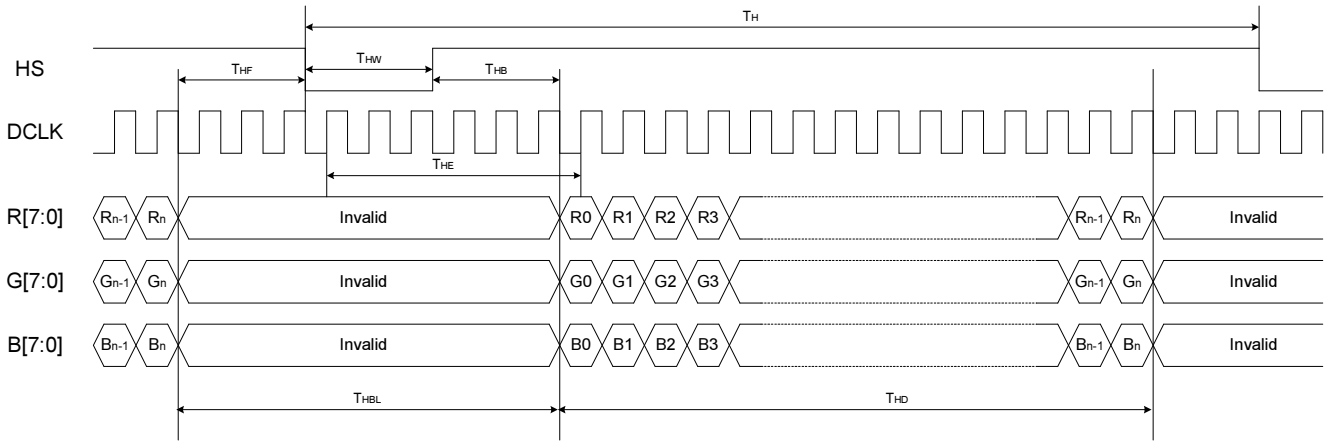


Figure 4 : Horizontal input timing. (HV mode)

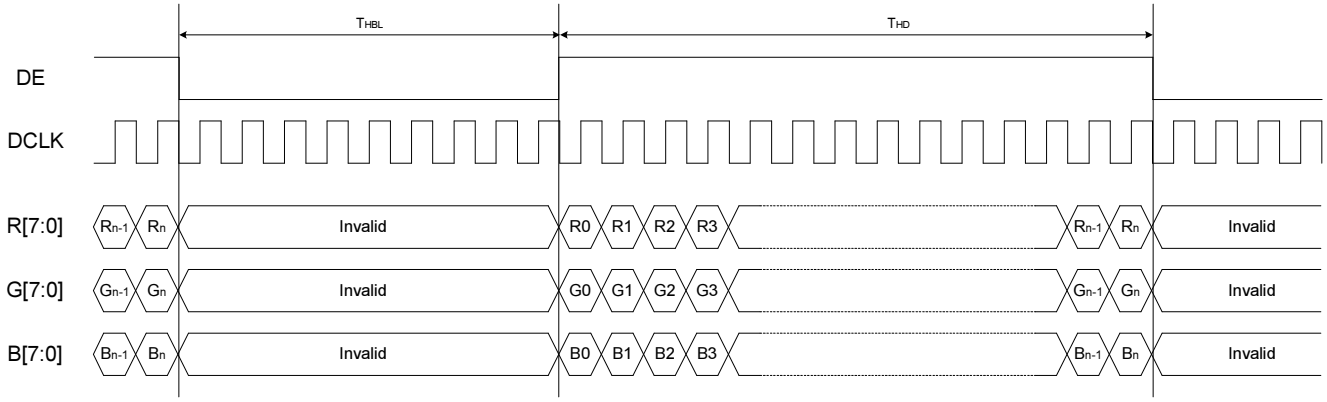


Figure 5 : Horizontal input timing. (DE mode)

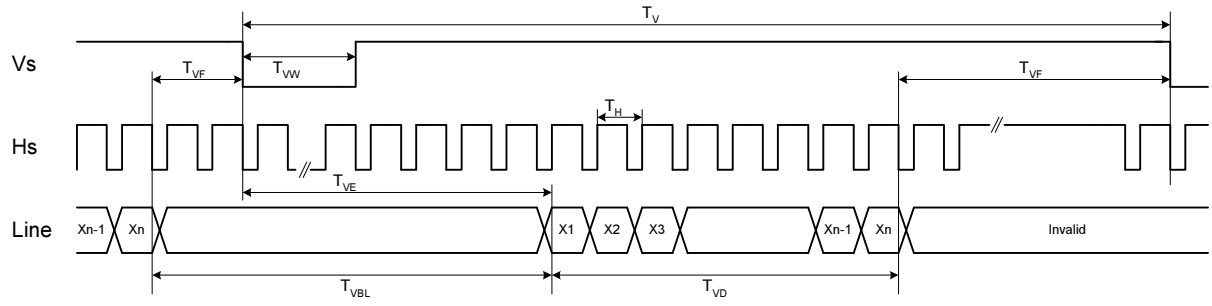


Figure 6 : Vertical timing. (HV mode)

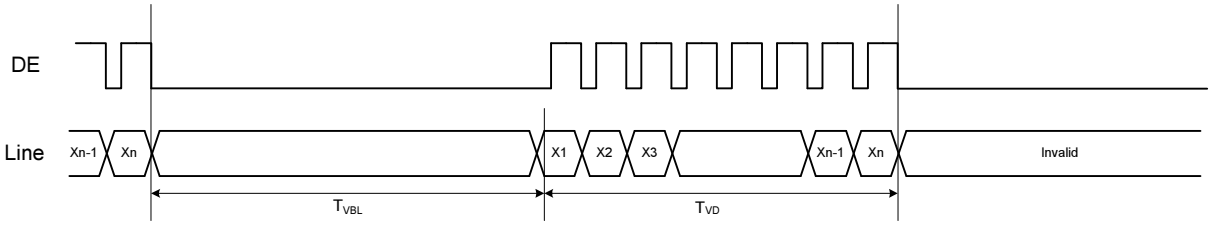


Figure 7 : Vertical timing. (DE mode)

2.6 Serial Control Interface AC characteristic

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial clock	T_{SCK}		320			ns
SCL pulse duty	T_{SCW}		40	50	60	%
Serial data setup time	T_{IST}		120			ns
Serial data hold time	T_{IHD}		120			ns
Serial clock high/low	T_{SSW}		120			ns
CSB setup time	T_{CST}		120			ns
CSB hold time	T_{CHD}		120			ns
Chip select distinguish	T_{CD}		1			us
Delay from CSB to VSYNC	T_{CV}		1			us

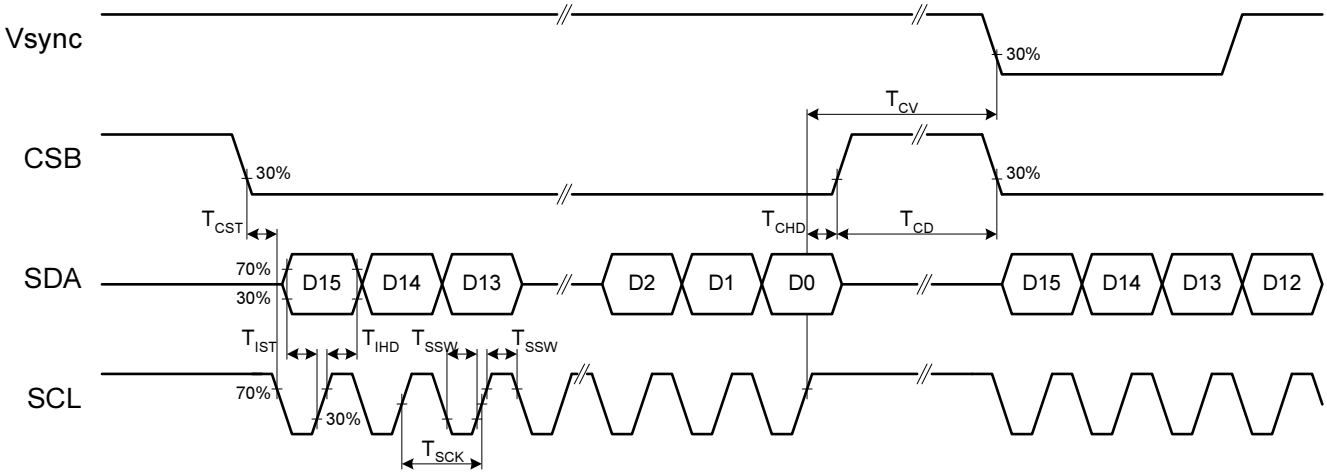


Figure 2 : AC serial interface write mode timing

2.7 Register Information

There is a total of 5 registers each containing several parameters. For a detailed description of the parameters refer to **Table 1**.The serial register has read/write function. D[15:12] are the register address, D[11] defines the read or write mode and D[10:0] are the data.

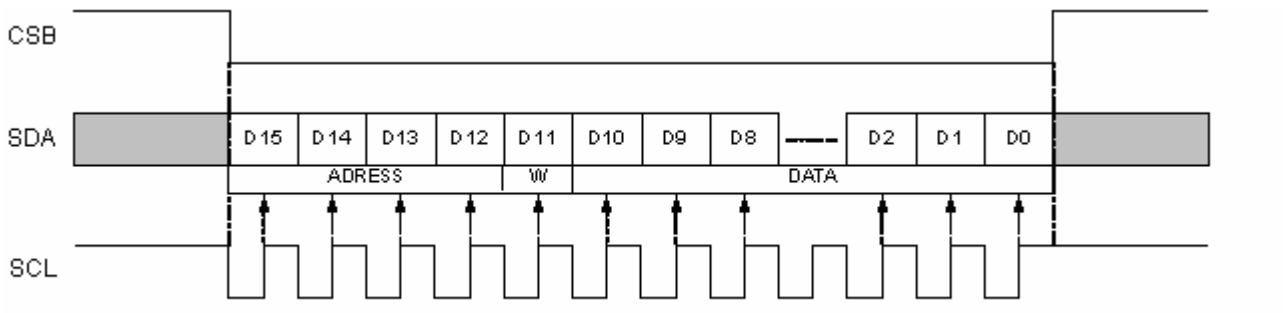


Figure 1: Serial interface write sequence

1. At power-on, the default values specified for each parameter (in **Table 1**) are taken.
2. If less than 16-bit data are read during the CS low time period, the data is cancelled.
   a. The write operation is cancelled.
3. All items are set at the falling edge of the vertical sync, except R0[1:0].
4. When GRB is activated through the serial interface, all registers are cleared, except the GRB value.
5. Register W setting: D11 = "L" → write mode;
6. The register setting values are valid when VCC already goes to high and after VSYNC starts.
7. It is suggested that VSYNC, HSYNC, DCLK always exists in the same time. But if HSYNC, DCLK stops, only VSYNC operating, the register setting is still valid.
8. If the chip goes to standby mode, the register value will still keep. MCU can wake up the chip only by changing standby mode value from low to high.
9. The register setting values are rewritten by the influence of static electricity, a noise, etc. to unsuitable value, incorrect operating may occur. It is suggested that the SPI interface will setup as frequently as possible.

2.7.1 Register Table (Default Register Settings)

Reg	ADDRESS				W	DATA										
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	01		01		1	U/D (0)	SHL (1)	SHDB1 (1)	X	GRB (1)	STB (1)
R1	0	0	0	1	0	X	01		VCOM_M (01)		VCOM_LVL (2Fh)					
R2	0	0	1	0	0	X	X	X	HDL (80h)							
R3	0	0	1	1	0	X	X	0	0	0	0	0	VDL (1000)			
R4	0	1	0	0	0	X	X	0	0	00		1	1111			
R6	0	1	1	0	0	X	0	EnGB12 (1)	EnGB11 (1)	EnGB10 (1)	0	0	EnGB5 (1)	EnGB4 (1)	EnGB3 (1)	0

※ R4 Should be set to "411Fh"

X : Reserved, please set to "0".

2.7.2

R0 Settings

Address	Bit	Description		Default
0000	[10..0]	Bits 10-9	AUO Internal Use	01
		Bits 7-8	AUO Internal Use	01
		Bit6	AUO Internal Use	1
		Bit5 (U/D)	Vertical shift direction selection.	0
		Bit4 (SHL)	Horizontal shift direction selection.	1

		Bit3 (SHDB1)	AVDD DC-DC converter shutdown setting.	1
		Bit2	AUO Internal Use	0
		Bit1 (GRB)	Global reset.	1
		Bit0 (STB)	Standby mode setting.	1

Bit5	**U/D function**
0	Scan down; First line=Gn→ Gn-1 →…→ G2 → Last line=G1. **(default)**
1	Scan up; First line=G1 → G2 → … → Gn-1 → Last line=Gn.

Bit4	**SHL function**
0	Shift left; First data=Y600 → Y601 → …→ Y2 → Last data=Y1.
1	Shift right: First data=Y1→ Y2 → …→ Y600 → Last data=Y600. **(default)**

Bit3	**SHDB1 function**
0	AVDD DC-DC converter is off.
1	AVDD DC-DC converter is on. **(default)**

Bit1	**GRB function**
0	The controller is reset. Reset all registers to default value.
1	Normal operation. **(default)**

Bit0	**STB function**
0	T-CON, source driver and DC-DC converters are off, and all outputs are High-Z.
1	Normal operation. (**default)**

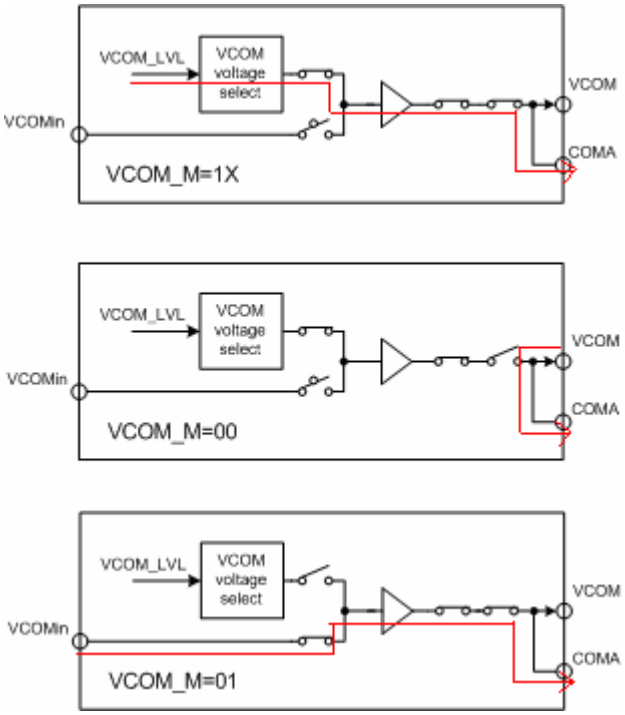
R1 settings

Address	**Bit**	**Description**		**Default**
0001	[8..0]	Bit9-8	AUO Internal Use	01
		Bit7-6 (VCOM_M)	VCOM mode signal.	01
		Bit5-0 (VCOM_LVL)	VCOM level adjustment. Step 31.25mV/LSB @AVDD=12.5V (AVDD/400)	2Fh

Bit7-6	**VCOM_M function.**
00	VCOM generator disabled. VCOM is generated externally.

01	VCOM internal reference disabled. DC voltage of VCOM follows VCOMin signal. (**default**)
1x	VCOM generator enabled. DC voltage of VCOM follows VCOM_LVL settings.

NOTE: Please refer to to following Figure. (COMA is panel internal signall)



Bit5-0	**VCOM_LVL function @V1=12.5V**
00h	VCOM_LVL = V1/2–47*31.25mV = 4.78125V
01h	VCOM_LVL = V1/2–46*31.25mV = 4.8125V
2Fh	VCOM_LVL = V1/2 = 6.25V (**default**)
3Eh	VCOM_LVL = V1/2+15*31.25mV = 6.71875V
3Fh	VCOM_LVL = V1/2+16*31.25mV = 6.75V

R2 settings

Address	**Bit**	**Description**		**Default**
0010	[7..0]	Bit7-0 (HDL)	Horizontal start pulse adjustment function	80h

Bit7-0	**HDL function.**
00h	$T_{HE} = T_{HEtyp}$ – 128 CLK period.
80h	$T_{HE} = T_{HEtyp}$. **(default)**
FFh	$T_{HE} = T_{HEtyp}$ + 127 CLK period.

R3 settings

Address	Bit	Description		Default
0011	6..0]	Bit6	AUO Internal Use	0
		Bit5	AUO Internal Use	0
		Bit4	AUO Internal Use	0
		Bit3-0 (VDL)	Vertical start pulse adjustment function	1000

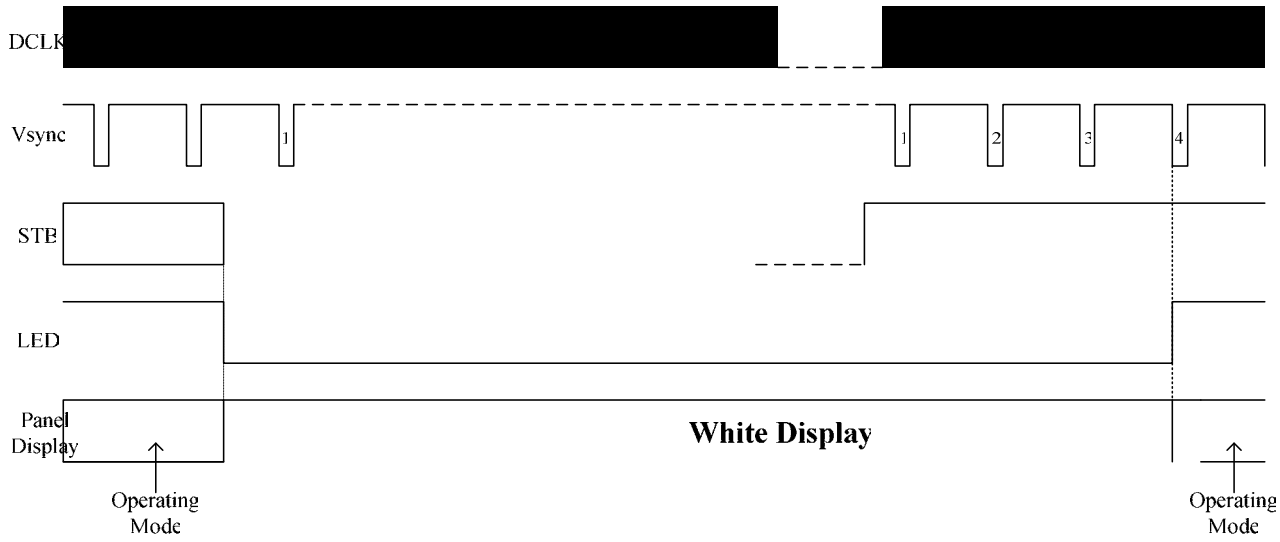
Bit3-0	VDL function.
0000	$T_{VE} = T_{VEtyp} – 8$ Hs period.
0001	$T_{VE} = T_{VEtyp} – 7$ Hs period.
0010	$T_{VE} = T_{VEtyp} – 6$ Hs period.
0011	$T_{VE} = T_{VEtyp} – 5$ Hs period.
0100	$T_{VE} = T_{VEtyp} – 4$ Hs period.
0101	$T_{VE} = T_{VEtyp} – 3$ Hs period.
0110	$T_{VE} = T_{VEtyp} – 2$ Hs period.
0111	$T_{VE} = T_{VEtyp} – 1$ Hs period.
1000	$T_{VE} = T_{VEtyp}$. **(default)**
1001	$T_{VE} = T_{VEtyp} + 1$ Hs period.
1010	$T_{VE} = T_{VEtyp} + 2$ Hs period.
1011	$T_{VE} = T_{VEtyp} + 3$ Hs period.
1100	$T_{VE} = T_{VEtyp} + 4$ Hs period.
1101	$T_{VE} = T_{VEtyp} + 5$ Hs period.
1110	$T_{VE} = T_{VEtyp} + 6$ Hs period.
1111	$T_{VE} = T_{VEtyp} + 7$ Hs period.

R6 settings

Address	Bit	Description		Default
0110	[9..0]	Bit9	AUO Internal Use	0
		Bit8(EnGB12)	Gamma buffer Enable for V9	1
		Bit7(EnGB11)	Gamma buffer Enable for V8	1
		Bit6(EnGB10)	Gamma buffer Enable for V7	1
		Bit5	AUO Internal Use	0
		Bit4	AUO Internal Use	0
		Bit3(EnGB5)	Gamma buffer Enable for V4	1
		Bit2(EnGB4)	Gamma buffer Enable for V3	1
		Bit1(EnGB3)	Gamma buffer Enable for V2	1
		Bit0	AUO Internal Use	0

Bitx	EnGBx function
0	Gamma buffer for VX is disable (High Z).
1	Gamma buffer is enable. VX must be connected externally.

2.8 Stand-by mode



2.9 Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	I_L	---	(180)	(200)	mA	---
LED Voltage	V_L	---	13.2	---	V	---
LED Life Time	L_L	10,000	---	---	Hr	Note 2, 3

Note 1: LED backlight is four LEDs serial type.

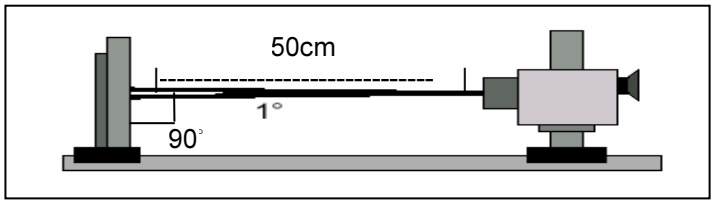
Note 2 :Define “LED Lifetime”: brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25℃ and LED current = 180mA.

Note 3: If it uses larger LED current I_L more than 200mA, it maybe decreases the LED lifetime.

3. Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	θ=0°	-	10	50	ms	Note 3
Fall	Tf		-	20	60	ms	
Contrast ratio	CR	At optimized viewing angle	250	300	-		Note 4
Viewing Angle							
Top			35	40	-		
Bottom		CR≧10	55	60	-	deg.	Note 5
Left			55	60	-		
Right			55	60	-		
Brightness (w/ TP)	Y_L	θ=0°	250	300	-	cd/m^2	Note 6
White Chromaticity	X	θ=0°	0.26	0.31	0.36		
	y	θ=0°	0.28	0.33	0.38		

Note 1 : Ambient temperature =25℃, and lamp current I_L = 180 mA. To be measured in the dark room.

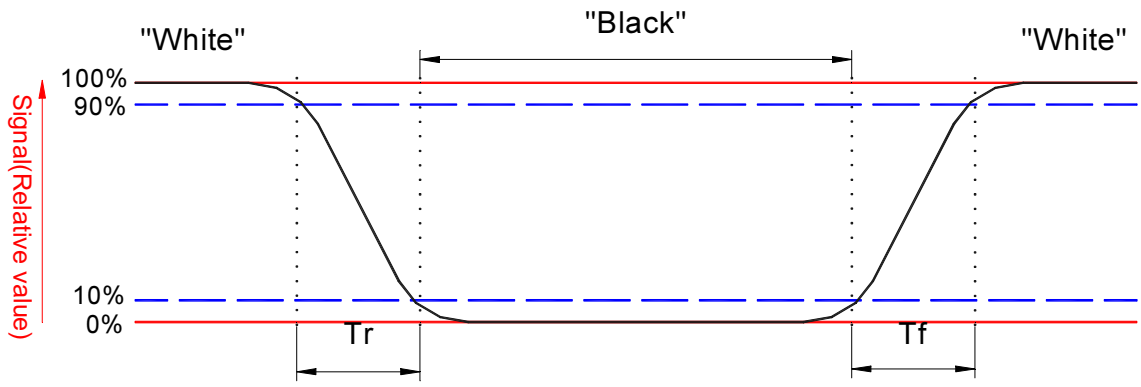


Note 2 :To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-7, after 15 minutes operation.

Note 3. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

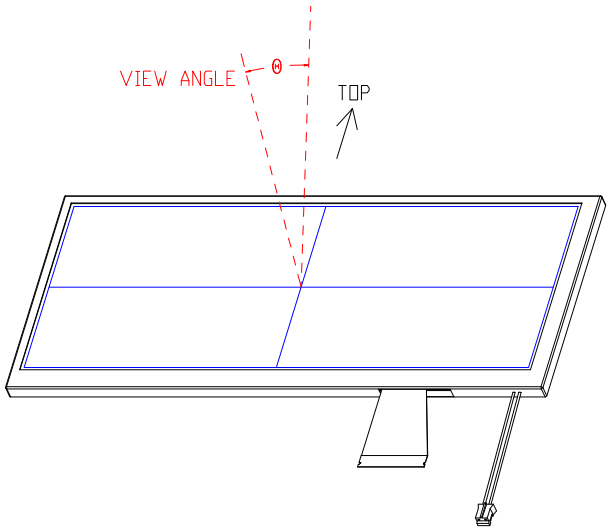


Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

4. Reliabiilty Test Items

No.	Test items	Conditions	Remark
1	High temperature storage	Ta = 80℃ 240Hrs	
2	Low temperature storage	Ta = -25℃ 240Hrs	
3	High temperature operation	Ta = 60℃ 240Hrs	
4	Low temperature operation	Ta = 0℃ 240Hrs	
5	High temperature and high humidity	Ta = 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃, 50 cycles, 2Hrs/cycle	Non-operation
7	Electrostatic discharge	± 200V,200pF (0Ω), once for each terminal	Non-operation
8	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz	IEC 68-34
9	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1: Ta: Ambient temperature.

5.Touch Screen Panel Specifications

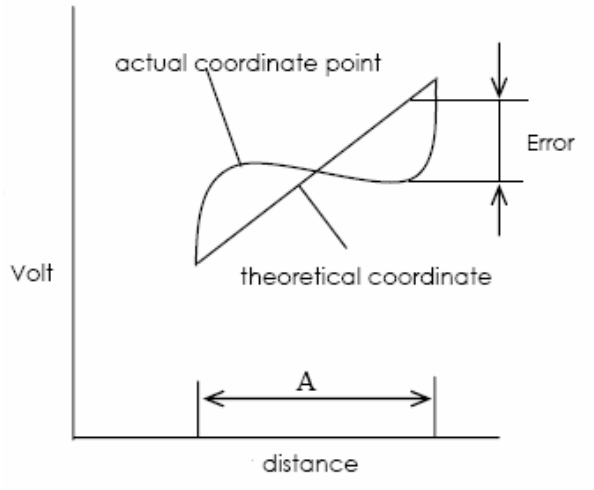
1. FPC Pin Assignment

Pin No.	Symbol	I/O
1	XL	O
2	YL	O
3	XH	O
4	YH	O

2. Electrical Characteristics

Item		Min.	Max.	Unit	Remark
Rate DC Voltage			7	V	Standard 5V
Resistance	X (Film)	400	1600	Ω	At connector
	Y (Glass)	100	400		
Linearity		-1.5%	1.5%	--	Note 1, test by 150 gf
Chattering			30	ms	At connector pin
Insulation Resistance		20M		Ω	DC 25V

Note 1: Measurement condition of Linearity: difference between actual voltage & theoretical voltage is an error at any points. Linearity is the value max. error voltage divided by voltage difference on active area.



3. Mechanical Characteristics

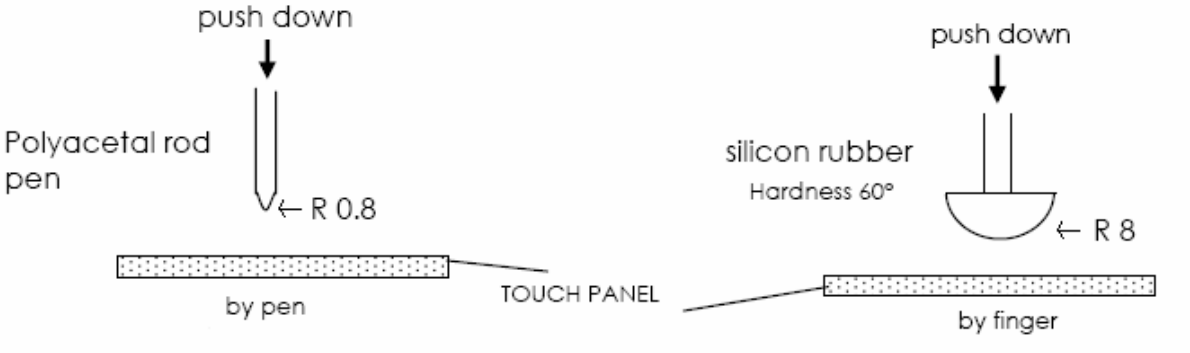
Item	Min.	Max.	Unit	Remark
Hardness of Surface	3	--	H	JIS K-5400
Operation Force (Pen or Finger)	--	80	gf	Note 1

Note 1: Within "guaranteed active area", but not on the edge and dot-spacer.

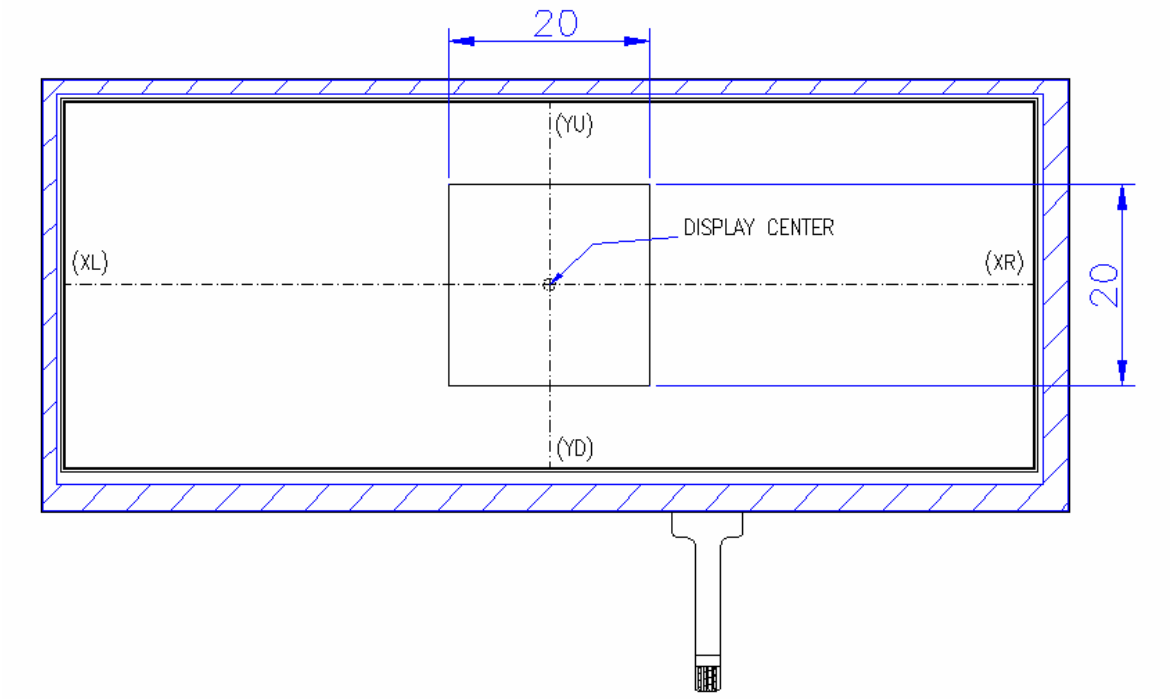
4. Life test Condition

Item	Min.	Max.	Unit	Remark
Sliding Life	10^5	--	times	Note 1, 2
Input Life	10^6	--	times	Note 1, 3

Note 1: Measurement condition of Operation Force: Within "guaranteed active area". Resistance, Insulation resistance, and operation force should be under 5.2 & 5.3 condition. When user pushes down on the film, resistance between X & Y axis must be equal or lower than 2kΩ. Below is test figure.



Note 2: Sliding Life test condition (by pen): Sliding area for pen sliding life test is the center of active area, 20x20 mm.Sliding speed is 100mm/s.



Note 3: Input Life test condition(by finger): By silicone rubber tapping at center of active area. Tapping Load is 250g, and tapping frequency is 3 Hz.

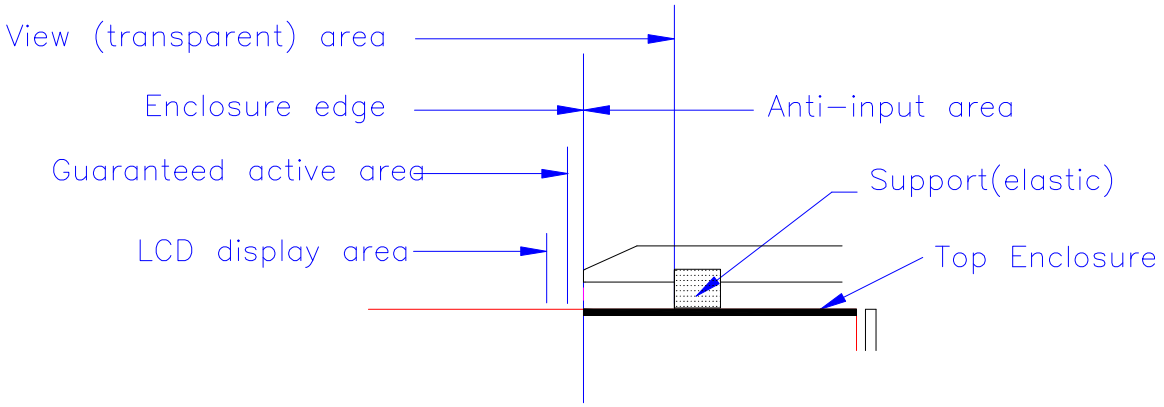
5. Attention

Please pay attention for below matters at mounting design of touch panel of LCD module.

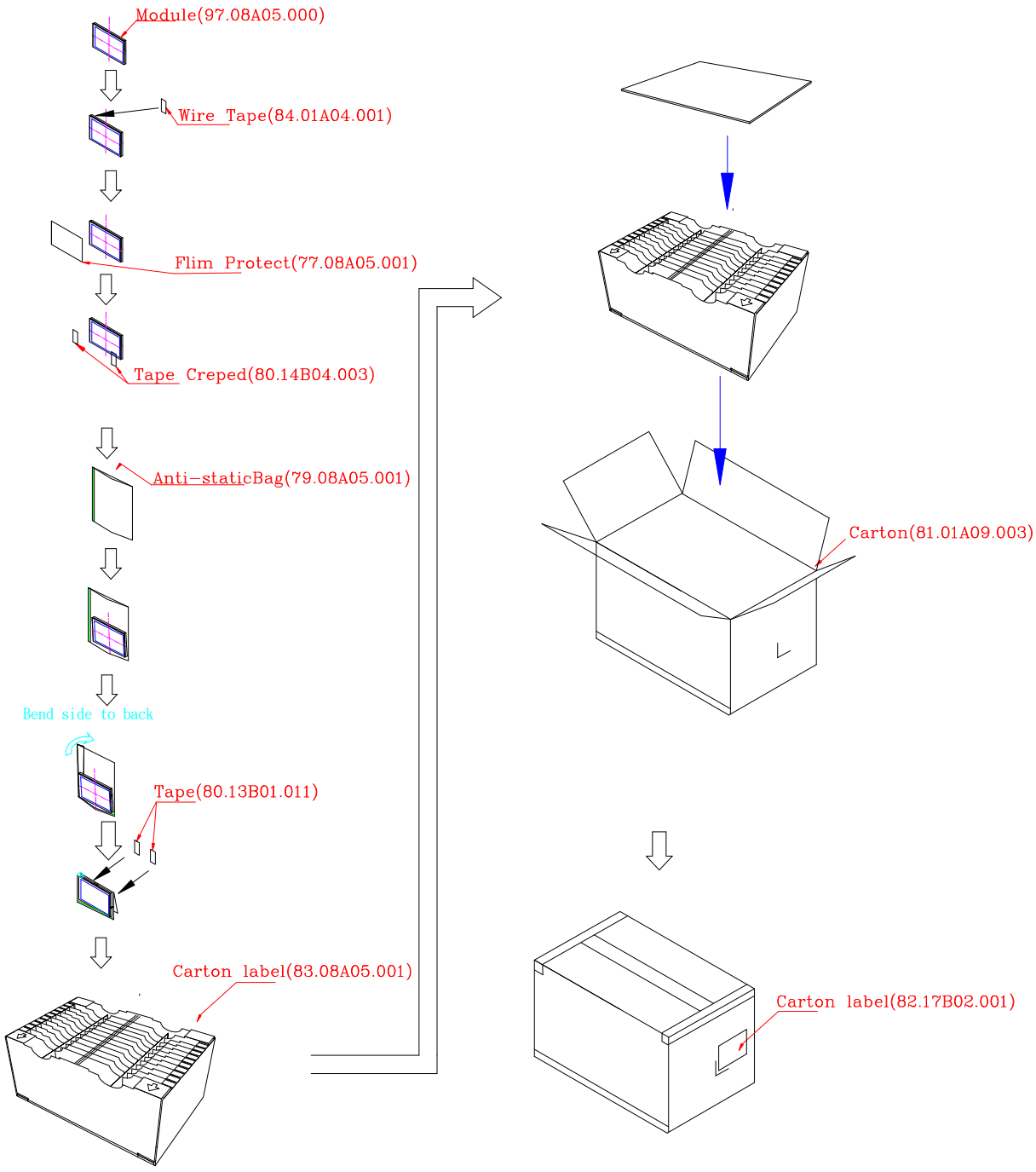
1. Do not design enclosure pressing the view area to prevent from miss input.
2. Enclosure support must not touch with view area.
3. Use elastic or non-conductive material to enclosure touch panel.
4. Do not bond film of touch panel with enclosure.
5. The touch panel edge is conductive. Do not touch it with any conductive part after mounting.
6. If user wants to cleaning touch panel by air gun, pressure 2kg/cm2 below is suggested. Not to blow glass from FPC site to prevent FPC peeled off.

7. Do not put a heavy shock or stress on touch panel and film surface. Ex. Don't lift the panel by film face with vacuum.
8. Do not lift LCD module by FPC.
9. Please use dry cloth or soft cloth with neutral detergent (after wring dry) or one with ethanol at cleaning. Do not use any organic solvent, acid or alkali liquor.
10. Do not pile touch panel. Do not put heavy goods on touch panel.

Recommendation of the cushion area:



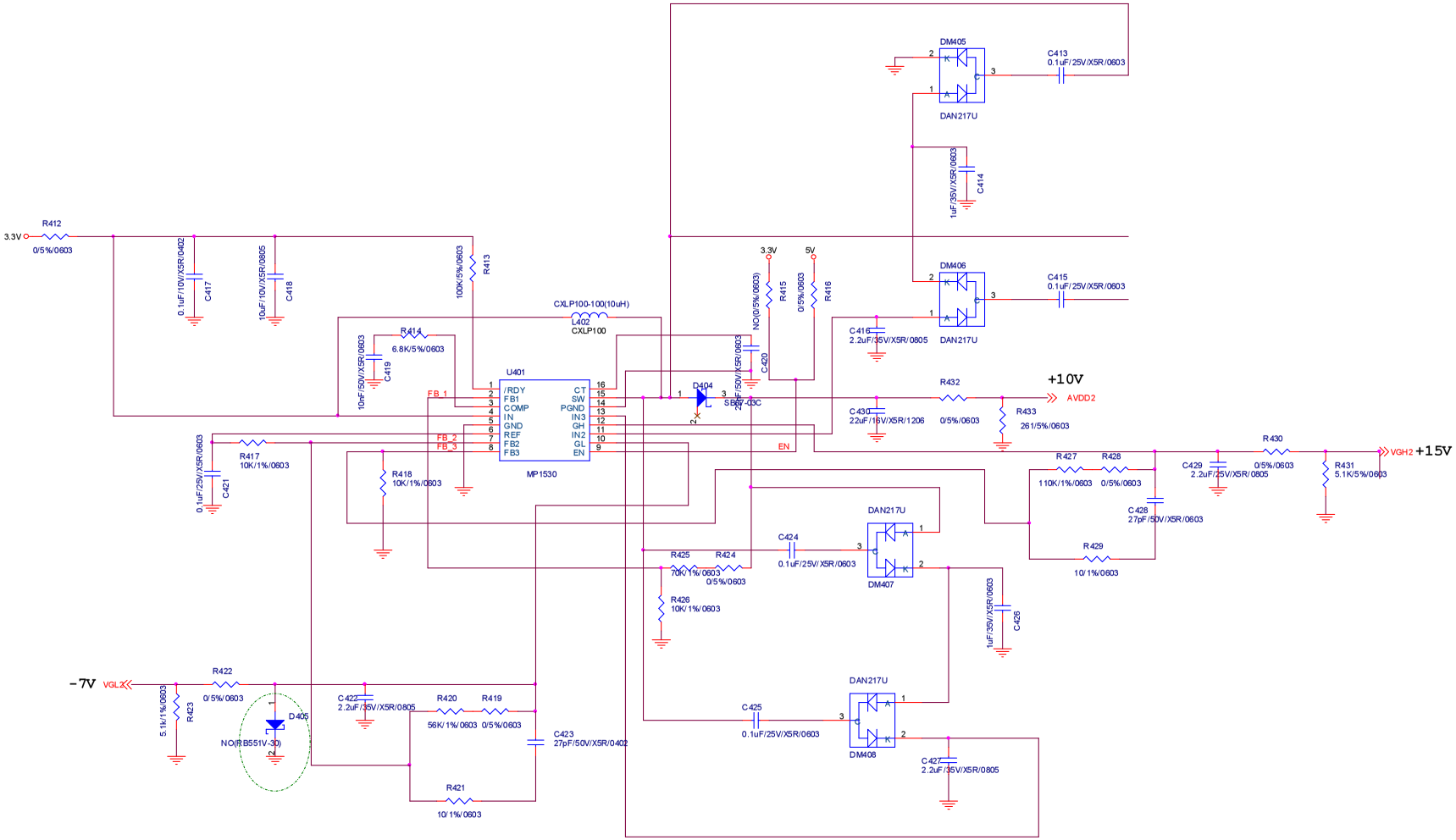
6. Packing Form

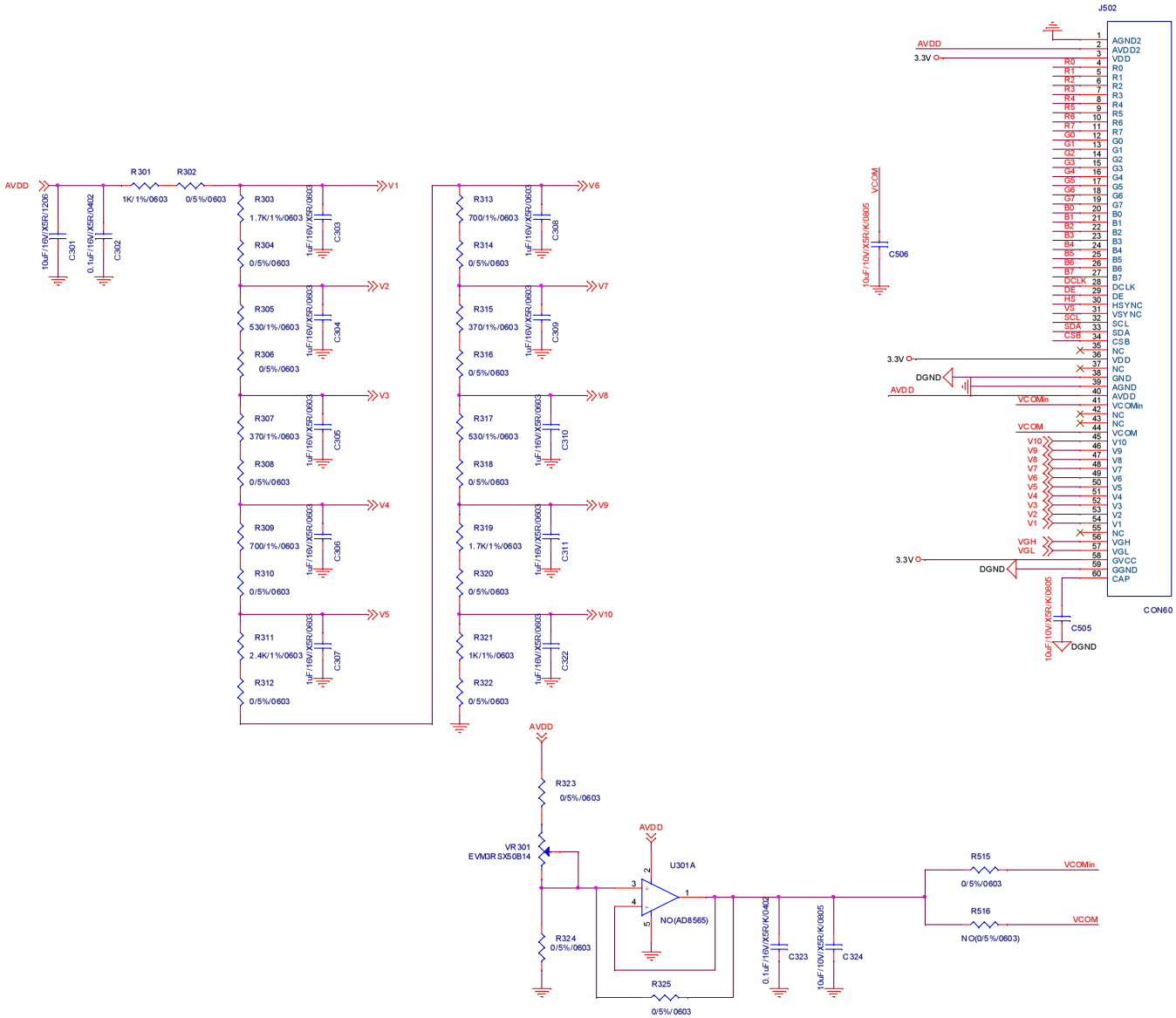


Max. Capacity: 40 Pcs Modules
Carton outline.: 520mm*340mm*250mm

7. Suggested Application Note

1. Application Circuit

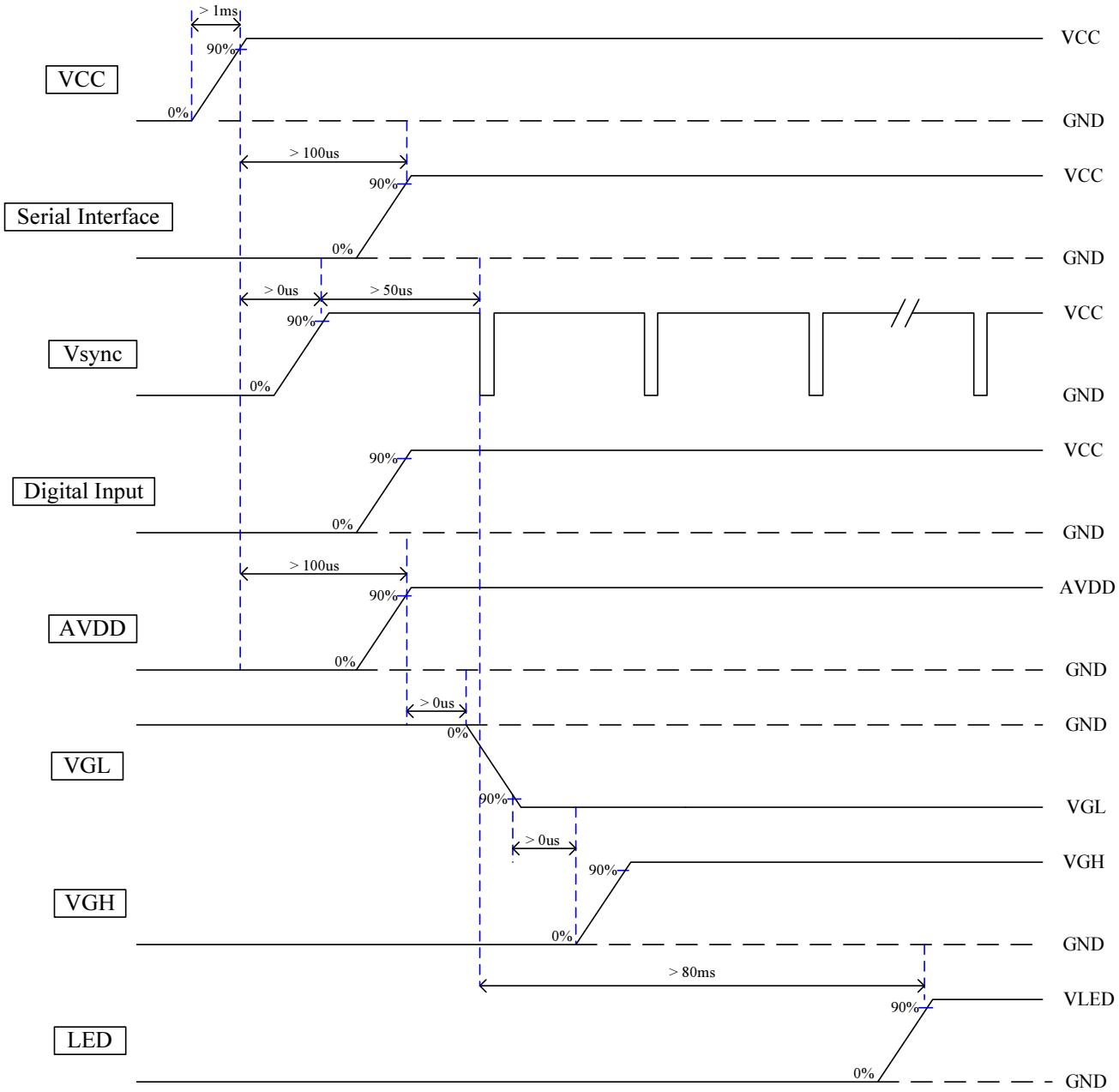




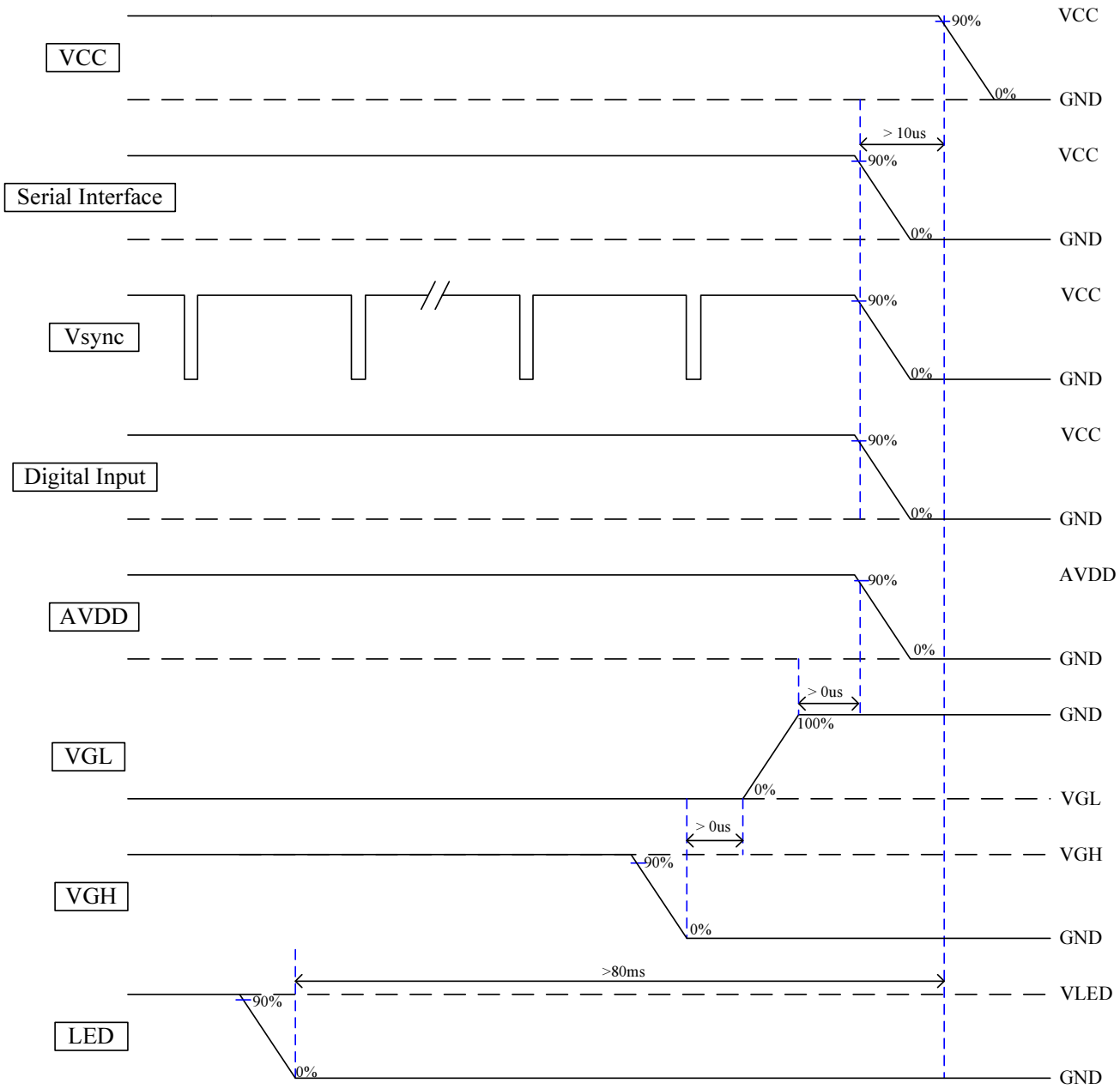
2. Power On/Off Sequence

This IC may be damaged by a large current flow when an incorrect power sequence is applied. The recommended power-on sequence is to first connect the logical power (VCC&GND), then the analog and driver powers (AVDD&AGND) and finally the references V1~14. When shutting off the power, the inverse sequence should be applied or all power should be turned off simultaneously.

Power On Sequence



Power Off Sequence



Note : Use external DCDC Controller for AVDD, VGL, and VGH.

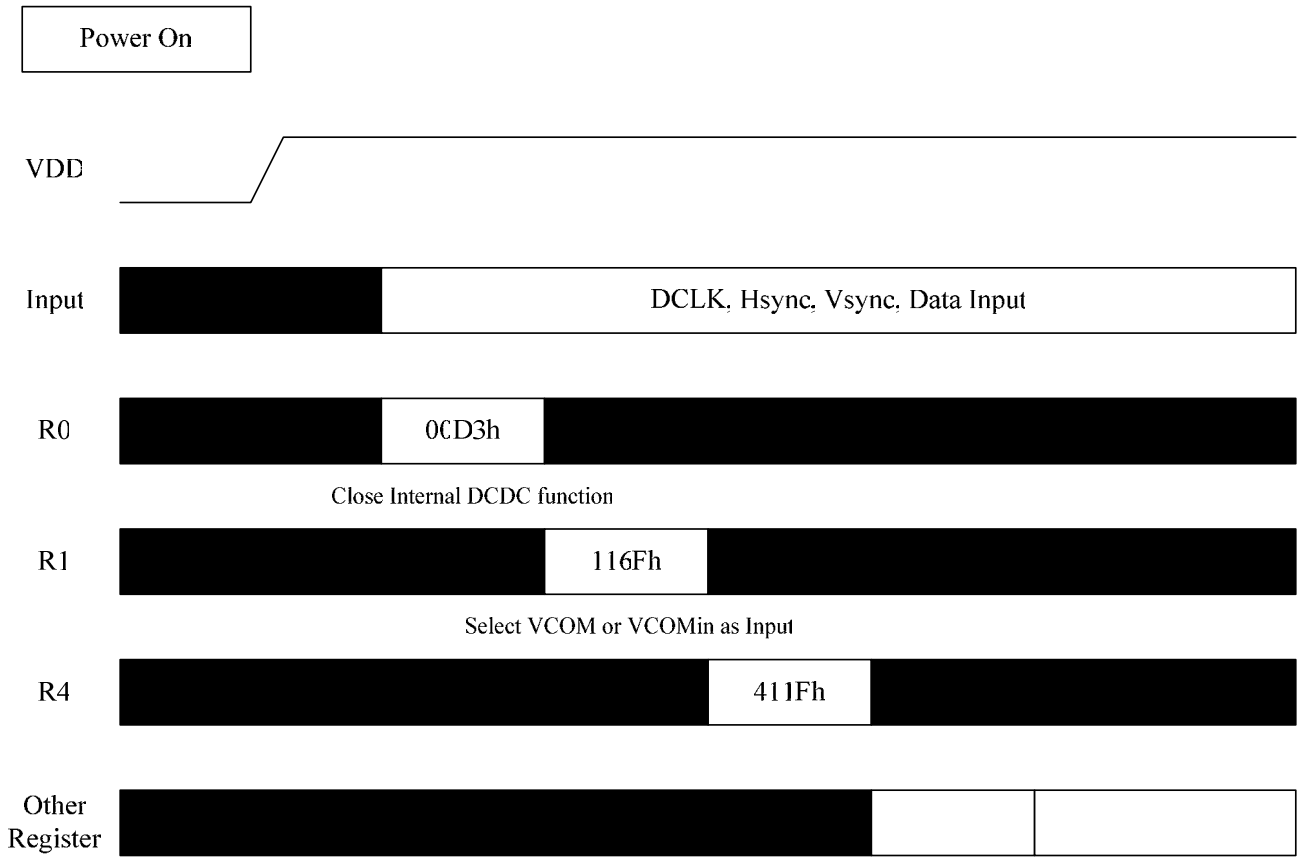
3. Recommended Register Setting

Reg	ADDRESS				W	DATA									
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	00		01		1	0	1	0	0	1	1
R1	0	0	0	1	0	0	01		01		2Fh					
R4	0	1	0	0	0	0	0	1	0	00		1	1111			

※ R4 Should be set to “411Fh”

※ Use VCOM(Pin44) as input , R1 should be setted to “112Fh”

※ Use VCOMin(Pin41) as input , R1 should be setted to “116Fh”



4. Gamma Voltage (TBD)

Gamma 2.2		
	AVDD	(11)
00H	V1	(10)
10H	V2	(8.3)
20H	V3	(7.77)
30H	V4	(7.4)
3FH	V5	(6.7)
3FH	V6	(4.3)
30H	V7	(3.6)
20H	V8	(3.23)
10H	V9	(2.7)
00H	V10	(1)