Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications
(V) Final Specifications

Module	**WXGA Color TFT-LCD with LED Backlight design**
Model Name	**B121EW09 V4 (H/W:0A)**
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
		Howard Lee	*2010/02/24*
Checked & Approved by	**Date**	**Prepared by**	
		Donna Yang	*2010/02/24*
Note: This Specification is subject to change without notice.		**NBBU Marketing Division / AU Optronics corporation**	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 04/13/2009	All	New version		
0.2 08/14/2009	15		Update signal electrical Charactistics	
0.2 08/14/2009	25		Update Power on-off sequence	
0.2 08/14/2009	34		Add Shipping Label Format	
0.3 10/01/2009	6		Update white luminance	
1.0 02/24/2010	18		Update Display Port panel power sequence timing parameter:	
1.0 02/24/2010	36		Add EDID information	
1.1 02/03/2010	15		Update VCM	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breakdown.

2. General Description

B121EW09 V4 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B121EW09 V4 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

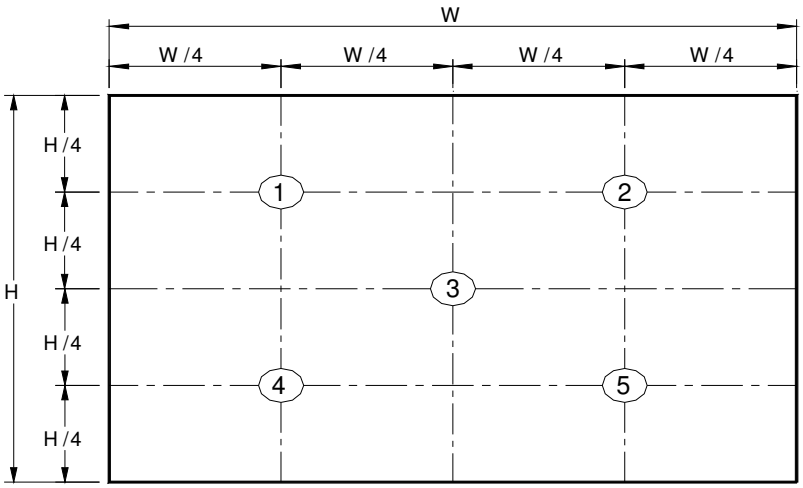
Items	Unit	Specifications
Screen Diagonal	[mm]	307.9 (W")
Active Area	[mm]	261.12(H) X 163.20(V)
Pixels H x V		1280x3(RGB) x 800
Pixel Pitch	[mm]	0.204X0.204
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (I_{LED}=20mA)	[cd/m^2]	220 typ. (5 points average) 187 min. (5 points average)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		400 typ
Response Time	[ms]	16 typ / 25 Max
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption	[Watt]	4.1 max. (Include Logic and Black Light power)
Weight	[Grams]	270 max.
Physical Size	[mm]	<table><tr><td></td><td>L</td><td>W</td><td>T</td></tr><tr><td>Max</td><td>276.3</td><td>178.6</td><td>5.5</td></tr><tr><td>Typical</td><td>275.8</td><td>178</td><td>-</td></tr><tr><td>Min</td><td>275.3</td><td>-</td><td>-</td></tr></table>
Electrical Interface		VESA eDP 30-pin
Surface Treatment		Anti-Glare
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +65
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

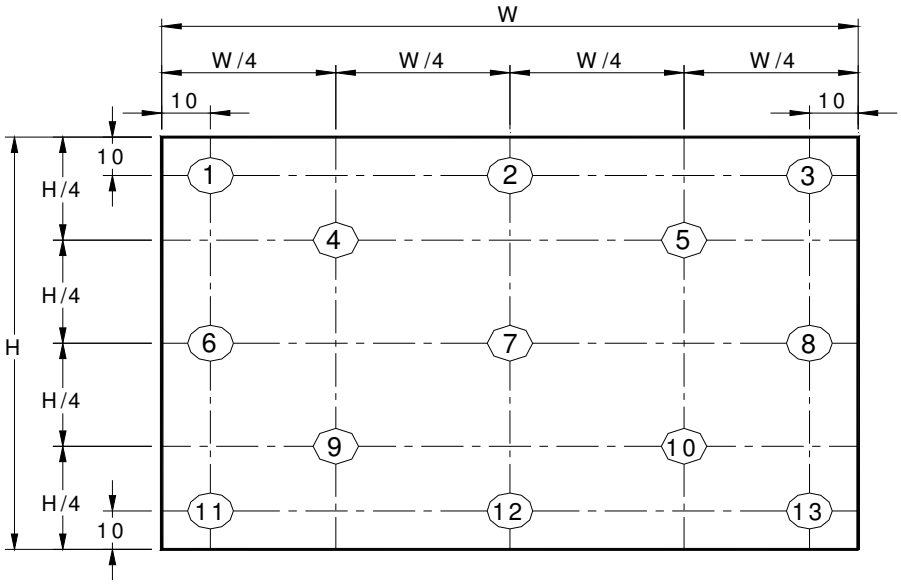
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=20mA			5 points average	187	220	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10 (Left)	40	45	-	degree	4, 9
		θ_L		40	45	-		
		Ψ_H	Vertical (Upper) CR = 10 (Lower)	10	15	-		
		Ψ_L		30	35	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.50		2, 3, 4
Contrast Ratio		CR			500	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_r	Rising	-	_	-	msec	4, 8
		T_f	Falling	-	_	-		
		T_{RT}	Rising + Falling	-	16	25		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.530	0.560	0.590		4
		Ry		0.320	0.350	0.380		
	Green	Gx		0.315	0.345	0.375		
		Gy		0.530	0.560	0.590		
	Blue	Bx		0.120	0.150	0.180		
		By		0.075	0.105	0.135		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	45	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



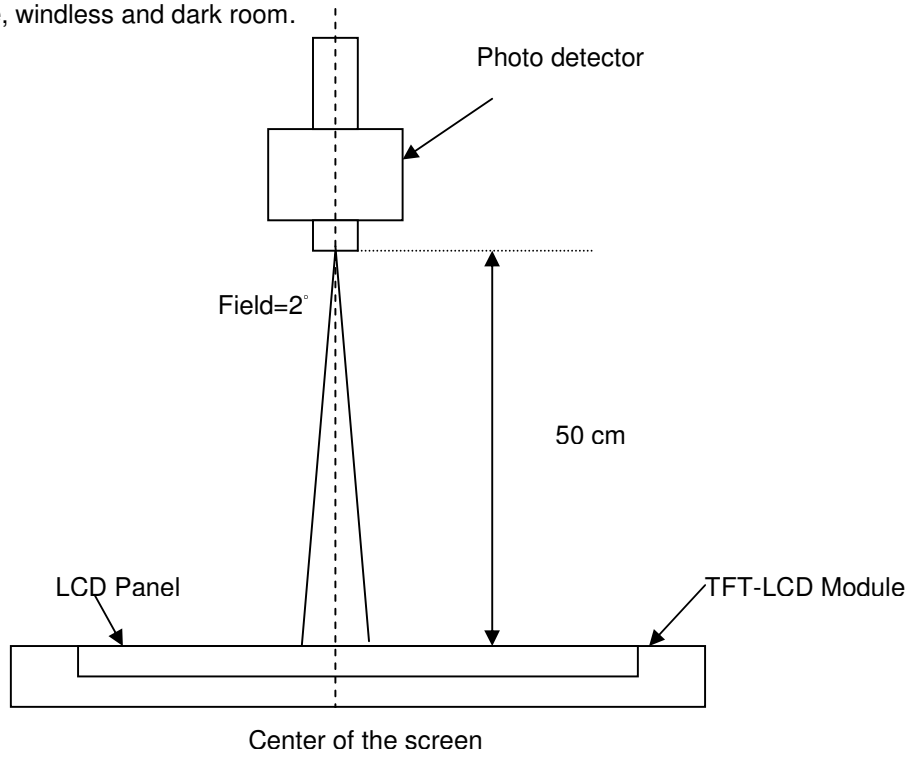
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

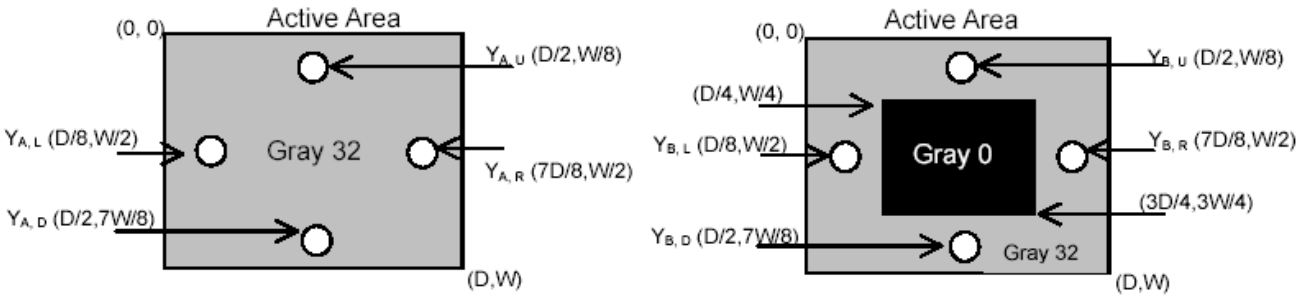
Note 7 : Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

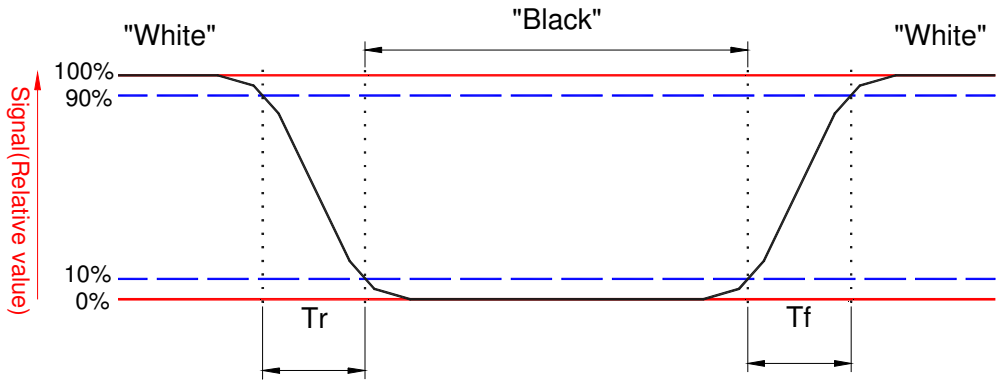
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



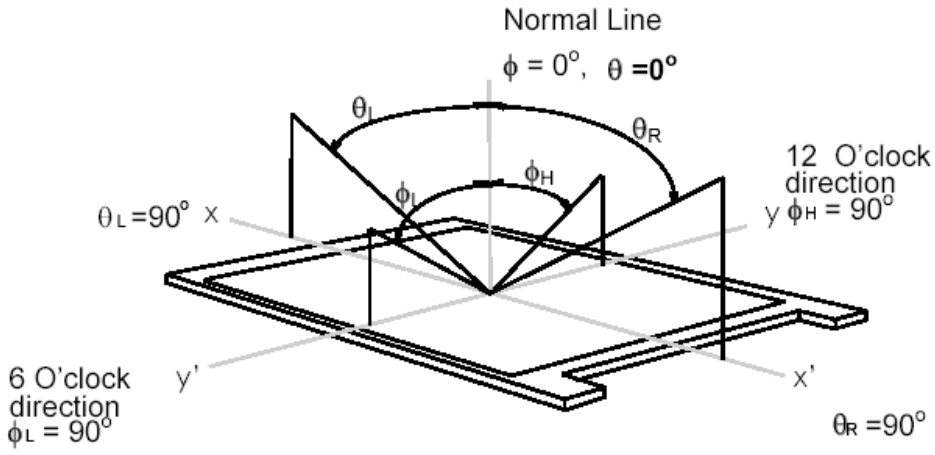
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



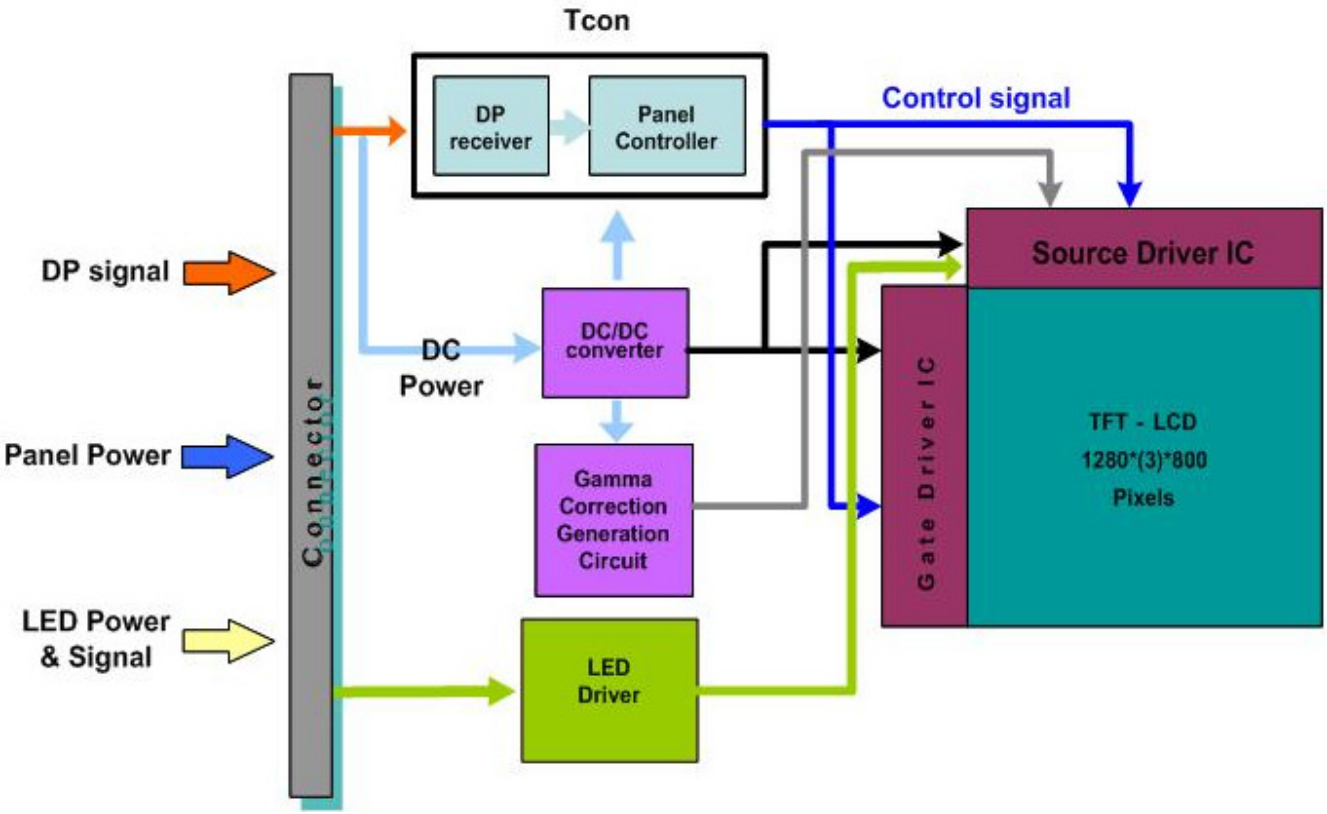
Note 8. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 12.1 inches wide Color TFT/LCD 30 Pin (One ch/connector Module:



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
LED Driving Voltage	V_{LED}	-	36 (Row Output)	[Volt]	Note 1,2,3
LED Driving Current	I_{LED}	-	30 (Row Output)	[mA] rms	Note 1,2,3

4.3 Absolute Ratings of Environment

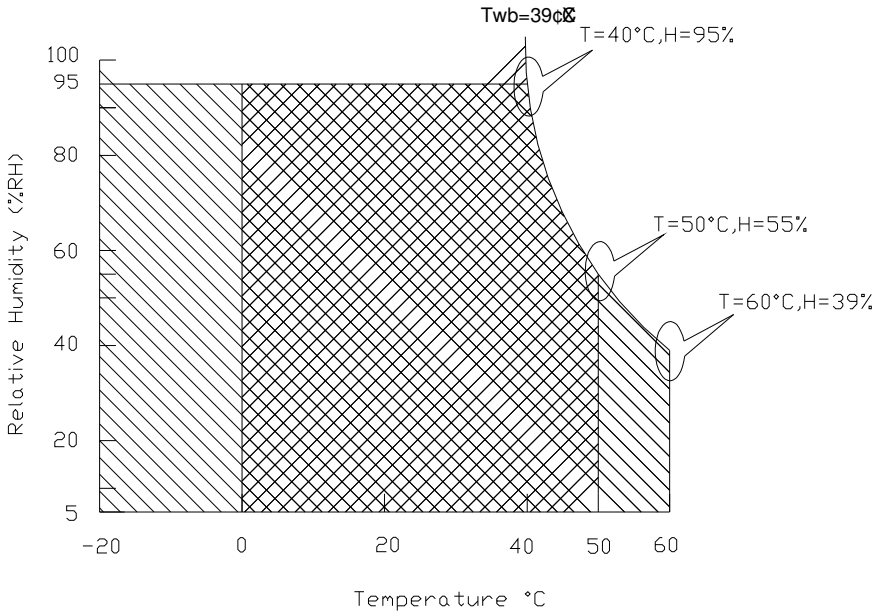
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	10	90	[%RH]	Note 4
Storage Temperature	TST	-20	+65	[°C]	Note 4
Storage Humidity	HST	10	90	[%RH]	Note 4

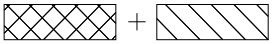
Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range  Storage Range 

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

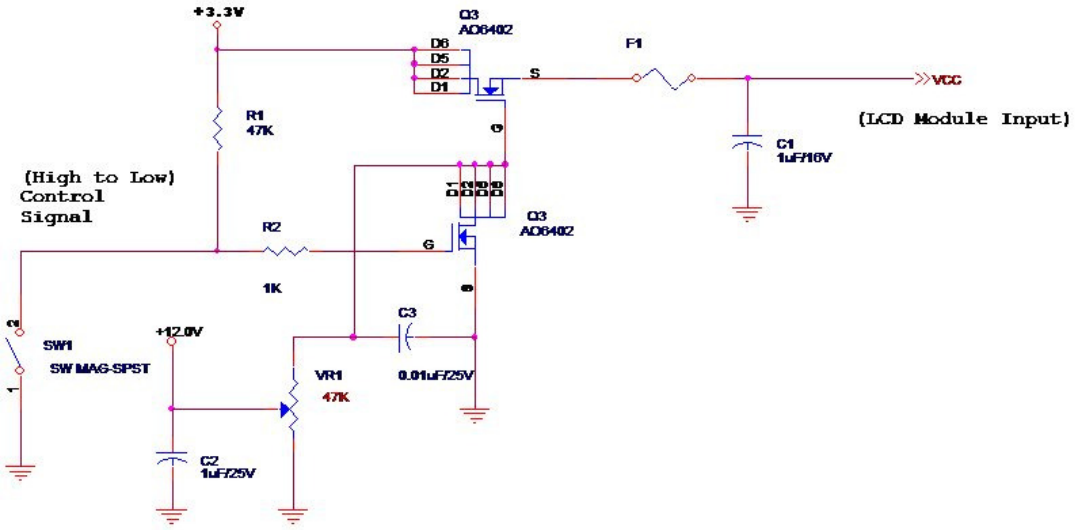
Input power specifications are as follows;

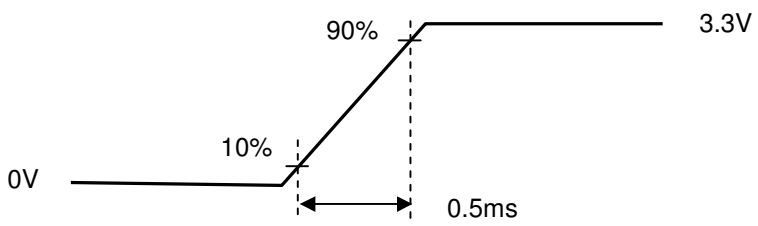
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-		0.9	[Watt]	Note 1/2
IDD	IDD Current	-	-	250	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Typical Measurement Condition: Mosaic Pattern

Note 3 : Measure Condition





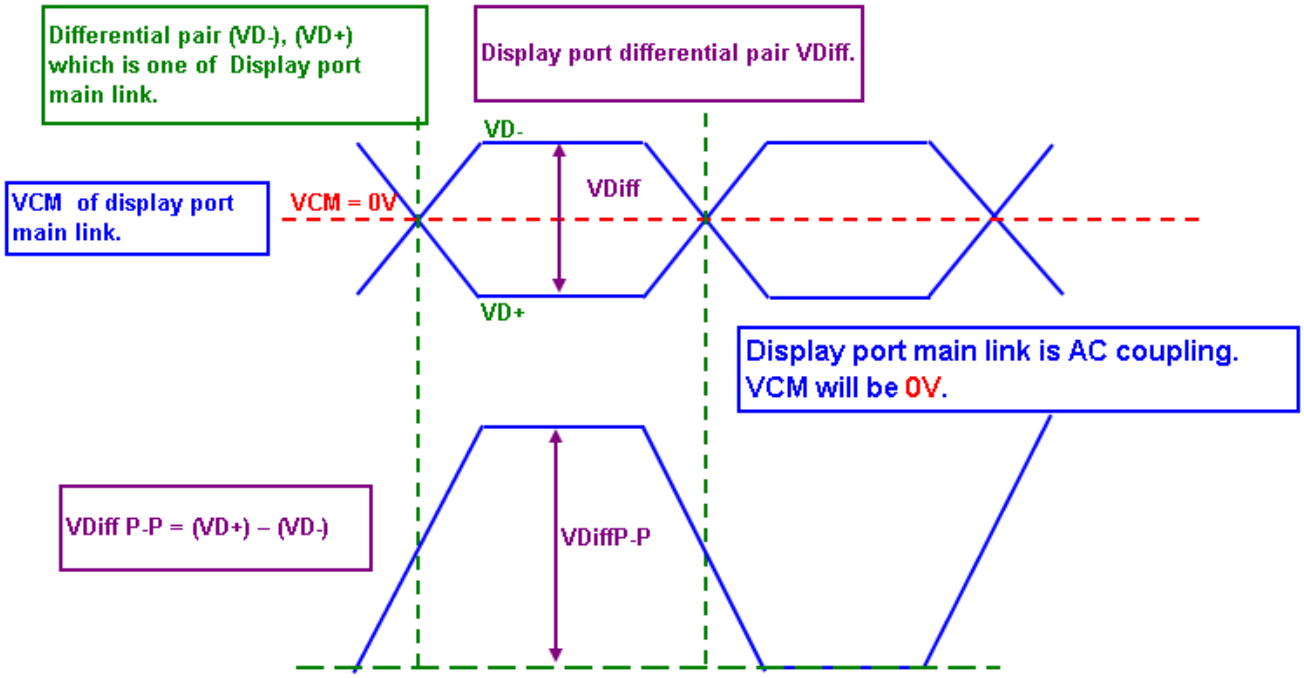
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

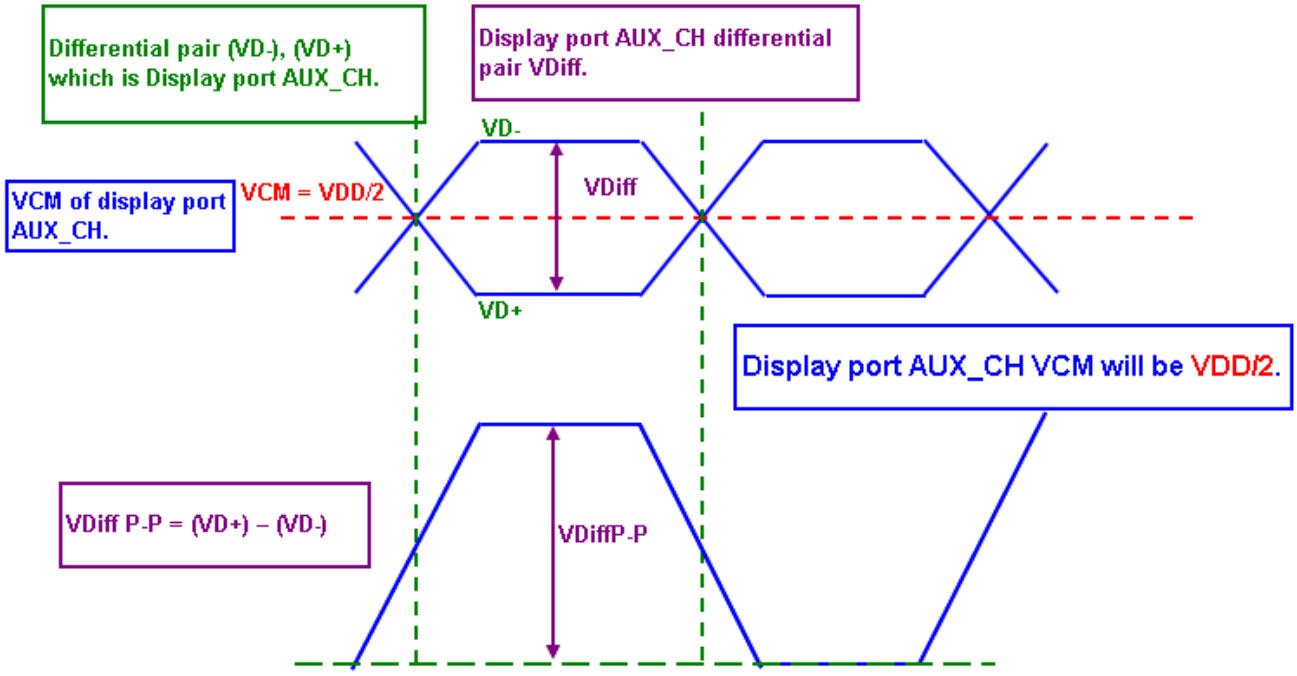
Signal electrical characteristics are as follows;

Display Port main link signal:



Display Port main link					
		Min	Typ	Max	unit
VCM	Differential common mode voltage	0.668	0.68	0.685	V
VDiffP-P level1	Differential peak to peak voltage level1	0.34	0.4	0.46	V
VDiffP-P level2	Differential peak to peak voltage level2	0.51	0.6	0.68	V
VDiffP-P level3	Differential peak to peak voltage level3	0.69	0.8	0.92	V
VDiffP-P level4	Differential peak to peak voltage level4	1.02	1.2	1.38	V

Display Port AUX_CH signal:



Display Port AUX_CH					
		Min	Typ	Max	unit
VCM	Differential common mode voltage	0	VDD/2	2	V
VDiffP-P	Differential peak to peak voltage	0.39		1.38	V

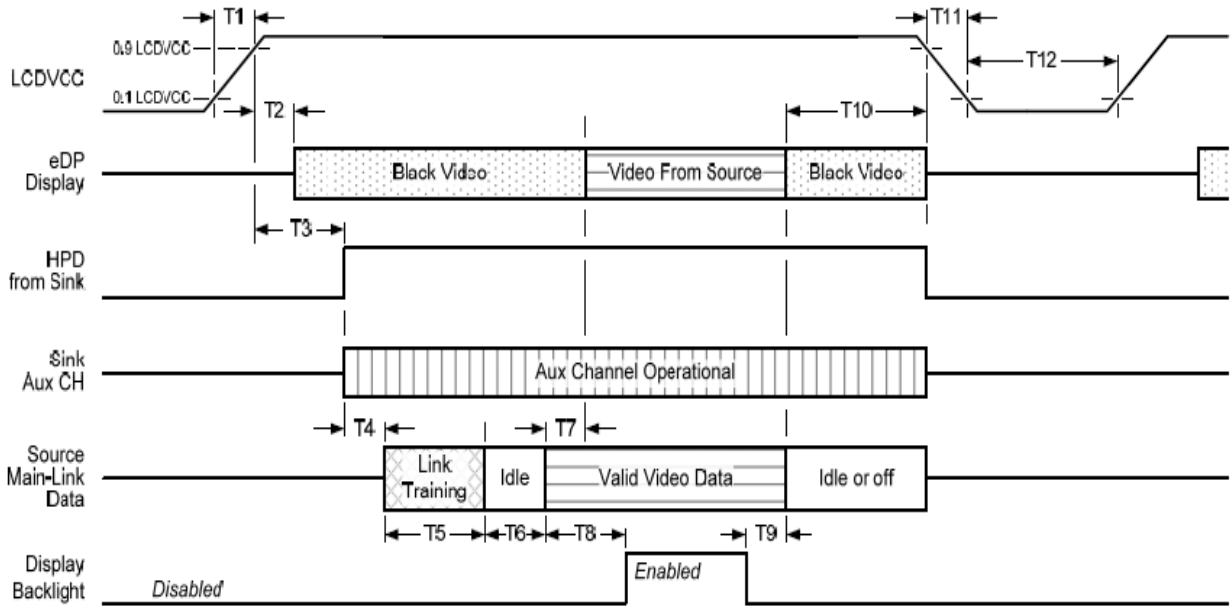
Fallow as VESA display port standard V1.1a.

Display Port V_{HPD} signal:

Display Port V_{HPD}					
		Min	Typ	Max	unit
V_{HPD}	HPD voltage	2.25		3.6	V

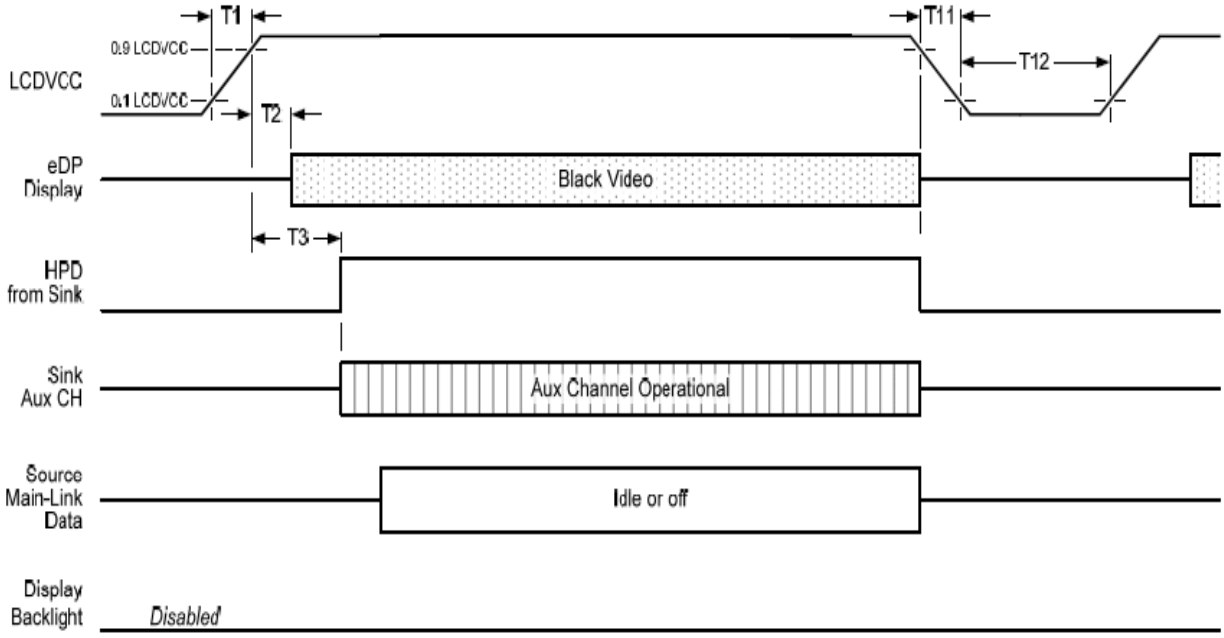
Fallow as VESA display port standard V1.1a.

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

Timing Parameter	Description	Reqd. By	Limits		Notes
			Min	Max	
T1	Power rail rise time, 10% to 90%	Source	0.5ms	10ms	
T2	Delay from LCDVCC to black video generation	Sink	0ms	200ms	Prevents display noise until valid video data is received from the Source (see note 1 below)
T3	Delay from LCDVCC to HPD high	Sink	0ms	200ms	Sink Aux Channel must be operational upon HPD high
T4	Delay from HPD high to link training initialization	Source	-	-	Allows for Source to read Link capability and initialize
T5	Link training duration	Source	-	-	Dependant on Source link training protocol
T6	Link idle	Source	-	-	Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization.
T7	Delay from valid video data from Source to video on display	Sink	0ms	50ms	Max allows Sink validate video data and timing
T8	Delay from valid video data from Source to backlight enable	Source	-	-	Source must assure display video is stable
T9	Delay from backlight disable to end of valid video data	Source	-	-	Source must assure backlight is no longer illuminated (see note 1 below)
T10	Delay from end of valid video data from Source to power off	Source	0ms	500ms	
T11	Power rail fall time, 90% to 10%	Source	-	10ms	
T12	Power off time	Source	500ms	-	

Note 1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)
-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 50ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power-on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

5.2 Backlight Unit

LED Parameter guideline for LED driving selection (Ref. Remark 1)

Parameter	Symbol	Min	Typ	Max	Units	Condition
LED Forward Voltage	V_F	2.95	3.15	3.35	[Volt]	(Ta=25□)
LED Forward Current	I_F		20	30	[mA]	(Ta=25□)
LED Power consumption	P_{LED}		3.78		[Watt]	(Ta=25□) Note 1
LED Life-Time	N/A	12,000	-	-	Hour	(Ta=25□) I_F=20 mA Note 2
Output PWM frequency	FPWM	100	200	20K	Hz	
Duty ratio	--	5	--	100	%	

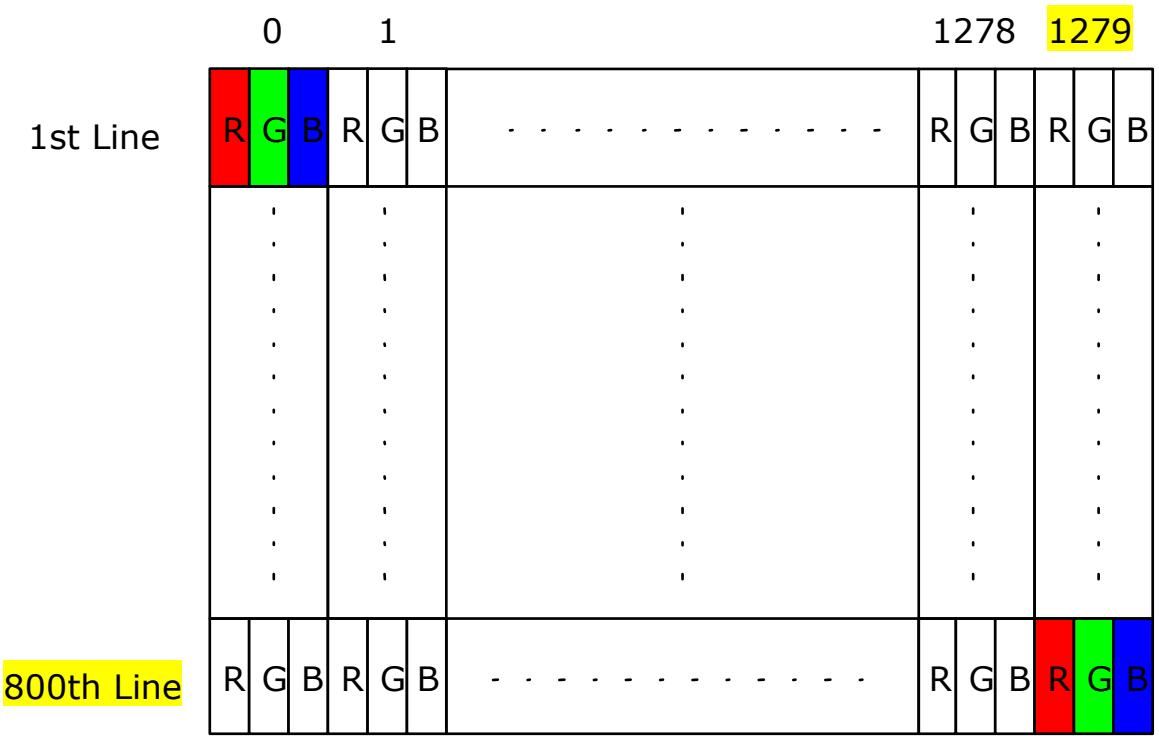
Note 1: Calculator value for reference $I_F \times V_F \times$ 42/ efficiency(85%)=P(typ.)

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

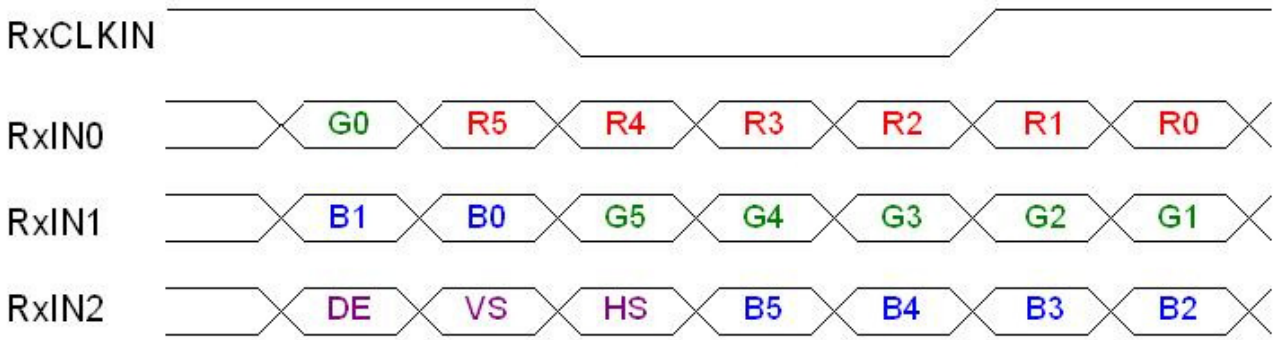
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The typical frequency is 69.3 MHZ. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

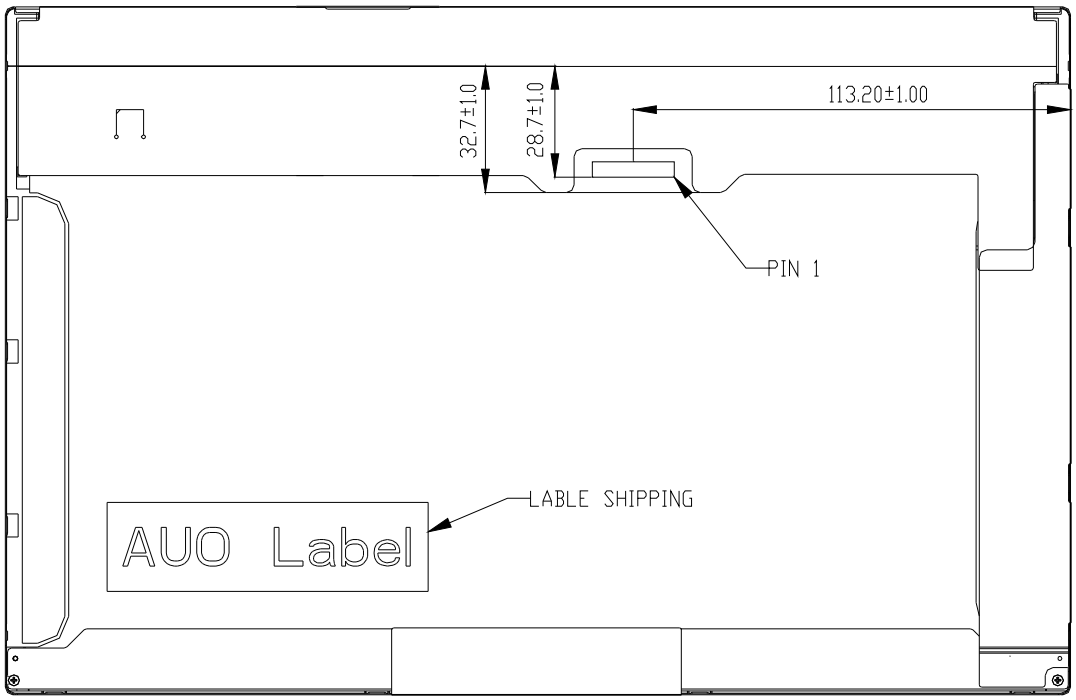
Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Signal Description/Pin Assignment

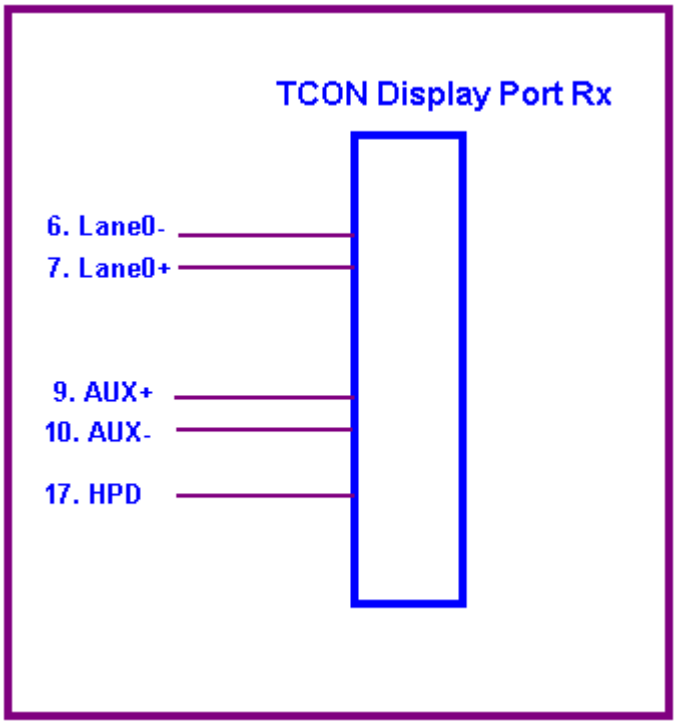
E-DP is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Signal	Description
1	NC	No Connection (Reserved)
2	NC	No Connection (Reserved)
3	NC	No Connection (Reserved)
4	NC	No Connection (Reserved)
5	H_GND	High Speed (Main Link) Ground
6	ML_Lane 0 (n)	Complement Signal-Main Link Lane
7	ML_Lane 0 (p)	True Signal-Main Link Lane
8	H_GND	High Speed (Main Link) Ground
9	AUX_CH(p)	True Signal-Auxiliary channel
10	AUX_CH(n)	Complement Signal-Auxiliary
11	H_GND	High Speed (Main Link) Ground
12	VCC	VCC for Module (3.3V)
13	VCC	VCC for Module (3.3V)
14	BIST	Built-In Self Test (active high)
15	GND	Ground
16	GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL_EN	BL On/Off (On: 2.0~3.3V, Off: 0~0.5V) / NC (100K pull-up) / 5V tolerant
23	BL_PWM	PWM for luminance control (200~1KHz, 3.3V, 10~100%, 0V=off) 5V tolerant
24	NC	No Connection (Reserved)
25	NC	No Connection (Reserved)
26	VBL	BL Power 6V-20V
27	VBL	BL Power 6V-20V
28	VBL	BL Power 6V-20V
29	VBL	BL Power 6V-20V
30	NC	No Connection (Reserved)

Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.
internal circuit of **eDP inputs** are as following.



6.4 Interface Timing

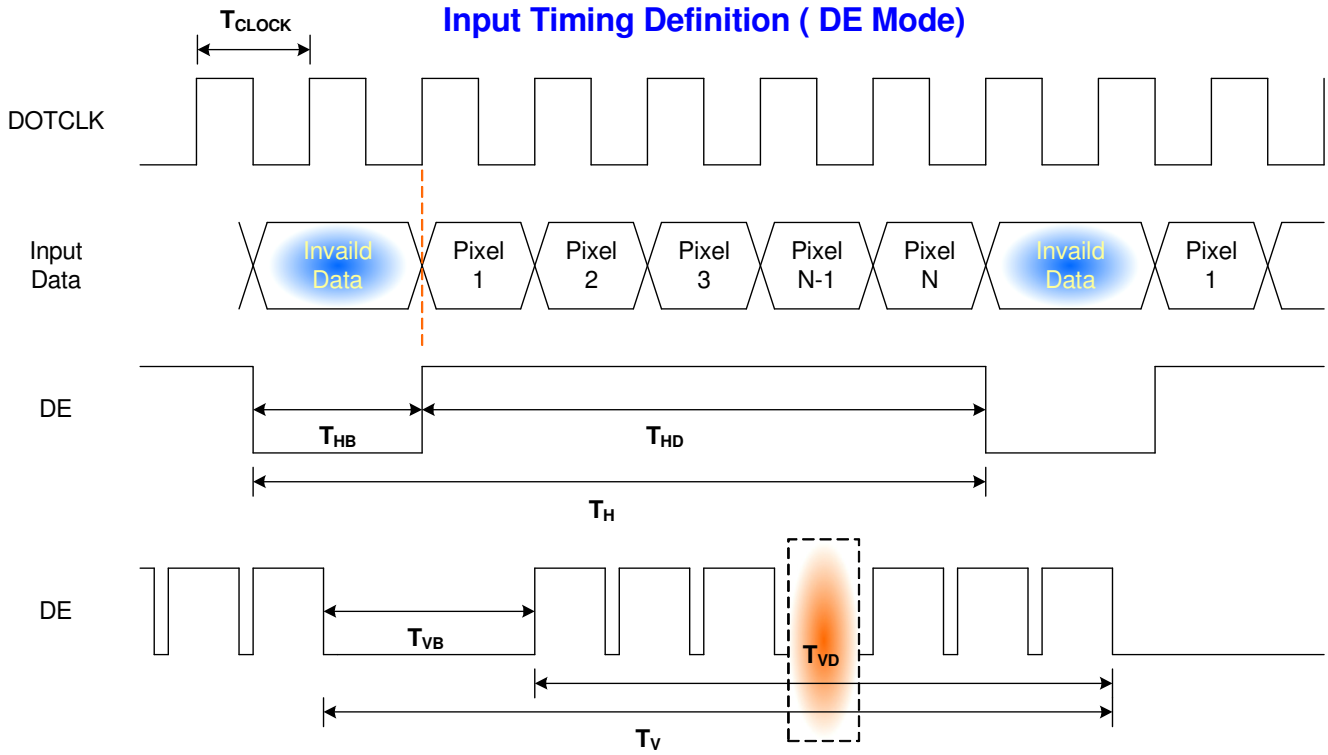
6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T_{Clock}	50-	69.3	80-	MHz
Vertical Section	Period	T_V	803	816	1023	T_{Line}
	Active	T_{VD}	800	800	800	
	Blanking	T_{VB}	3	16	223	
Horizontal Section	Period	T_H	1303	1416	2047	T_{Clock}
	Active	T_{HD}	1280	1280	1280	
	Blanking	T_{HB}	23	136	767	

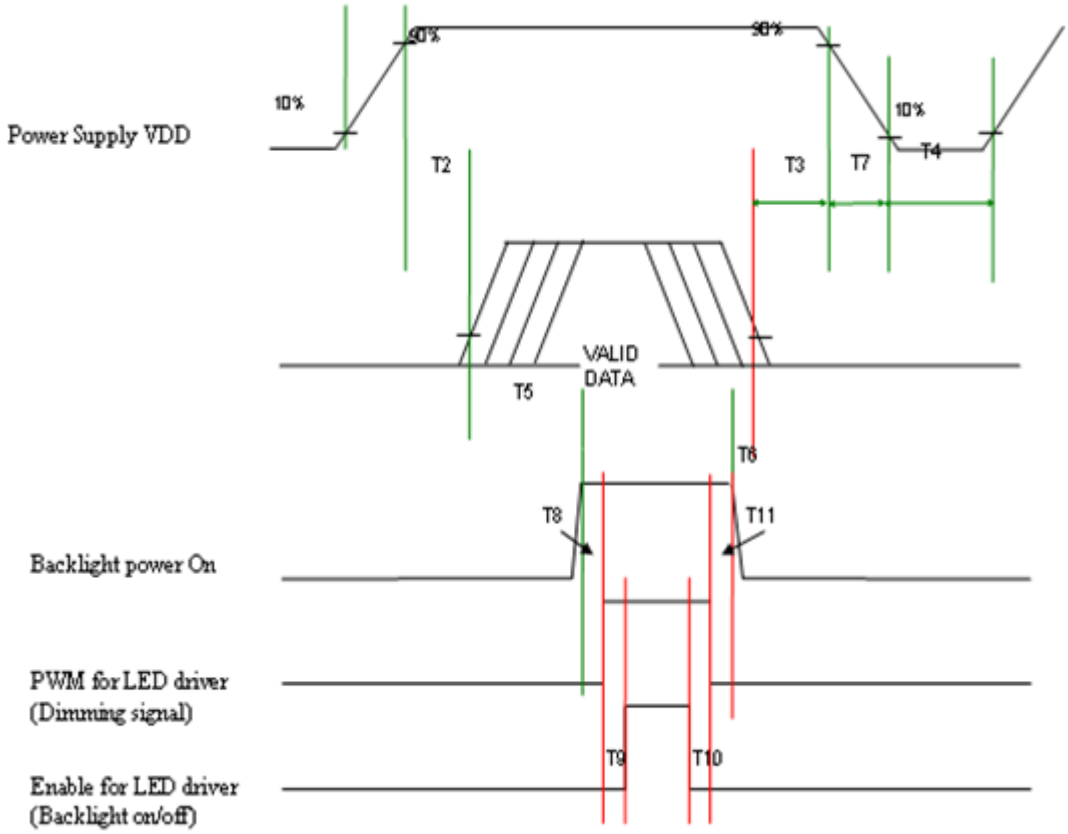
Note : DE mode only

6.4.2 Timing diagram



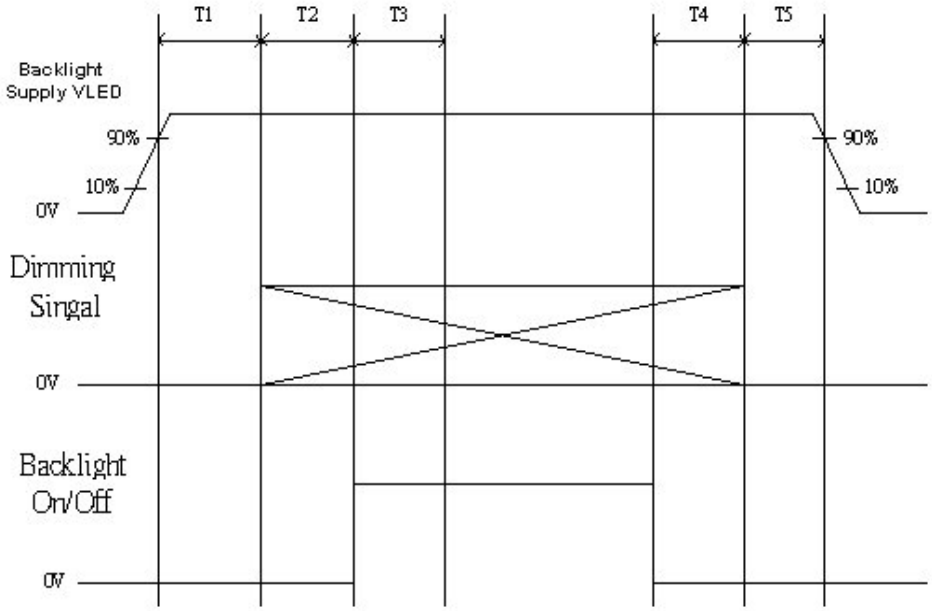
6.5 Power ON /OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	5	-	50	(ms)
T3	0.5	-	50	(ms)
T4	400	-	-	(ms)
T5	300	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)
T8	10	---	---	(ms)
T9	10	---	---	(ms)
T10	0	---	---	(ms)
T11	10	---	---	(ms)

LED on/off sequence is as follows. Interface signals are also shown in the chart.



Symbol	Values			Unit
	Min	Typ	Max	
T1	10	---	---	ms
T2	10	---	---	
T3	50	---	---	
T4	0	---	---	
T5	10	---	---	

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	**For Signal Connector**
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20455-030E-02 or compatible
Mating Housing/Part Number	IPEX 20453-030T-01 or compatible

8. 8. LED Driving Specification

8.1 Connector Description

It is a intergrative interface and comibe into LVDS connector. The type and mating refer to section 7.

8.2 Pin Assignment

Refer to 6.3

9. Vibration and Shock Test

9.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

9.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

10. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40□, 90%RH, 300h	
High Temperature Operation	Ta= 50□, Dry, 300h	
Low Temperature Operation	Ta= 0□, 300h	
High Temperature Storage	Ta= 60□, 300h	
Low Temperature Storage	Ta= -20□, 300h	
Thermal Shock Test	Ta=-20□to 60□, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

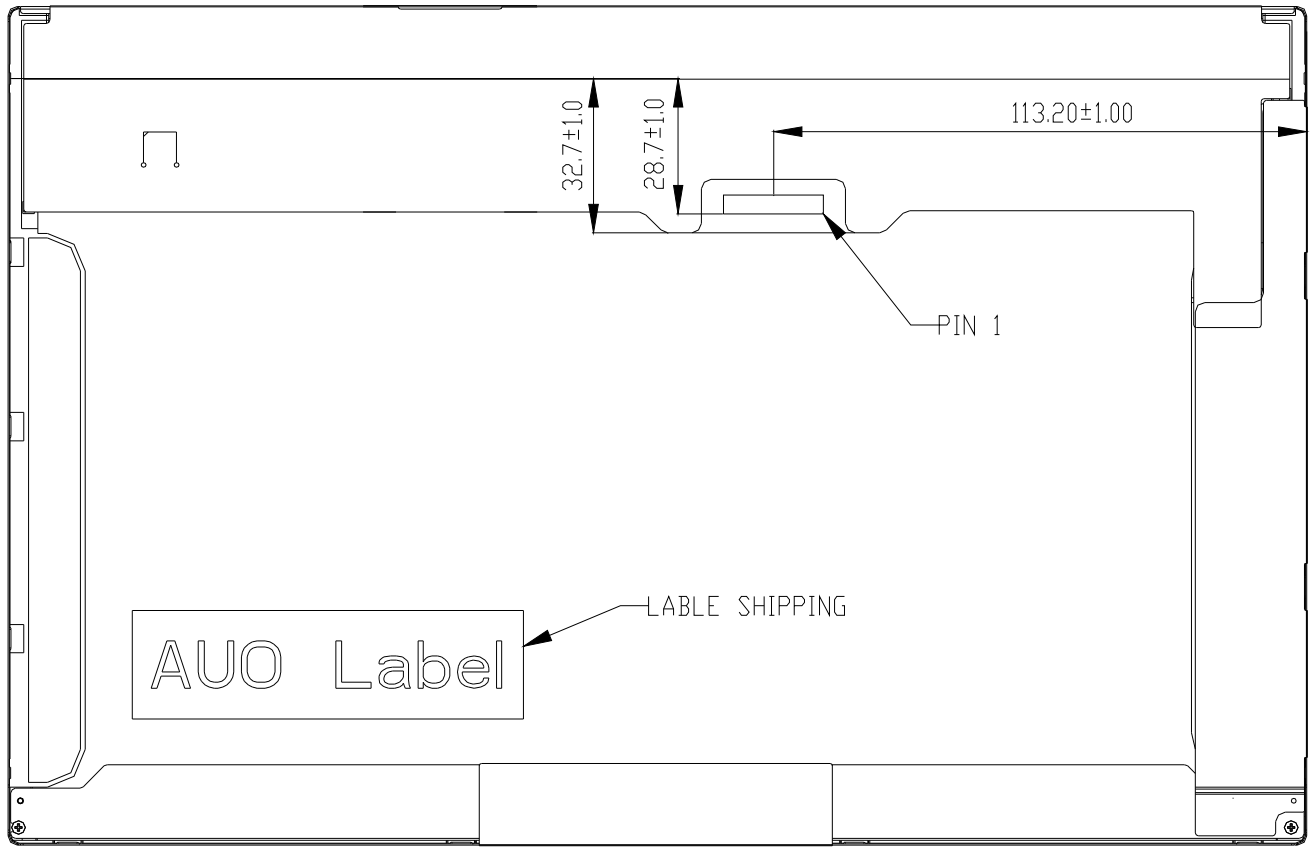
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

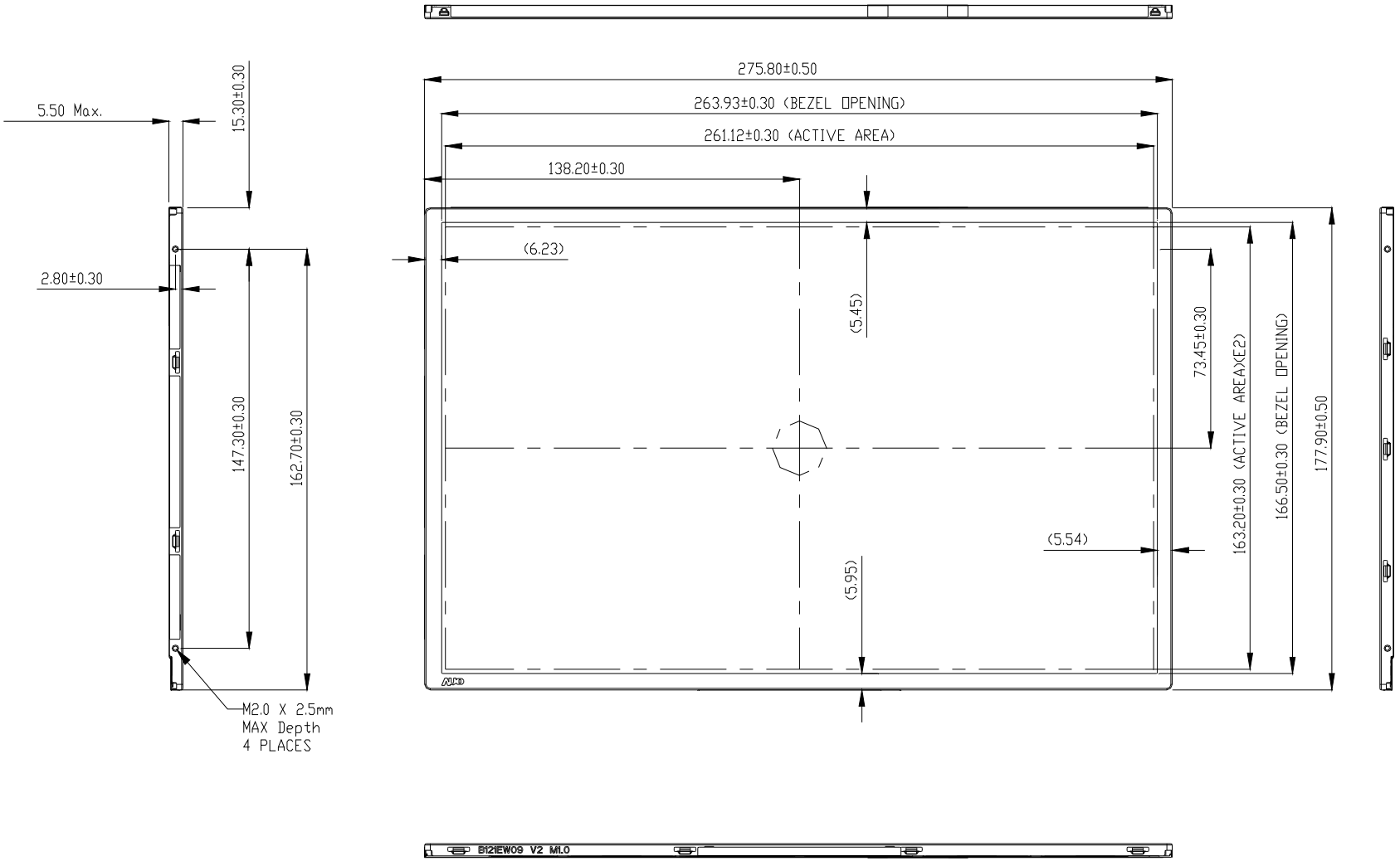
. Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

11. Mechanical Characteristics

11.1 LCM Outline Dimension



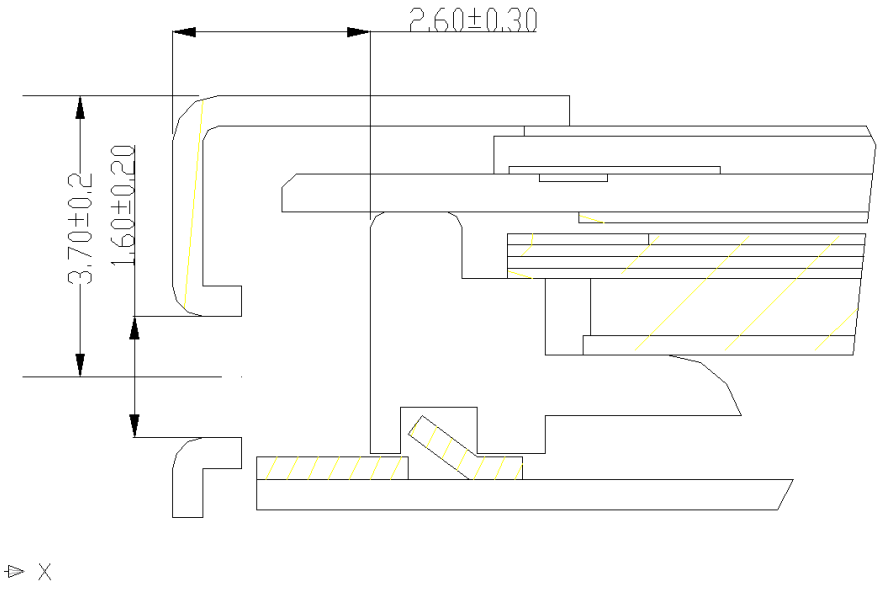

5.50 Max.
15.30±0.30
2.80±0.30
147.30±0.30
162.70±0.30
M2.0 X 2.5mm
MAX Depth
4 PLACES
275.80±0.50
263.93±0.30 (BEZEL OPENING)
261.12±0.30 (ACTIVE AREA)
138.20±0.30
(6.23)
(5.45)
(5.95)
(5.54)
73.45±0.30
163.20±0.30 (ACTIVE AREA)(E2)
166.50±0.30 (BEZEL OPENING)
177.90±0.50
B121EW09 V2 M1.0

SCALE 0.500

11.2 Screw Hole Depth and Center Position

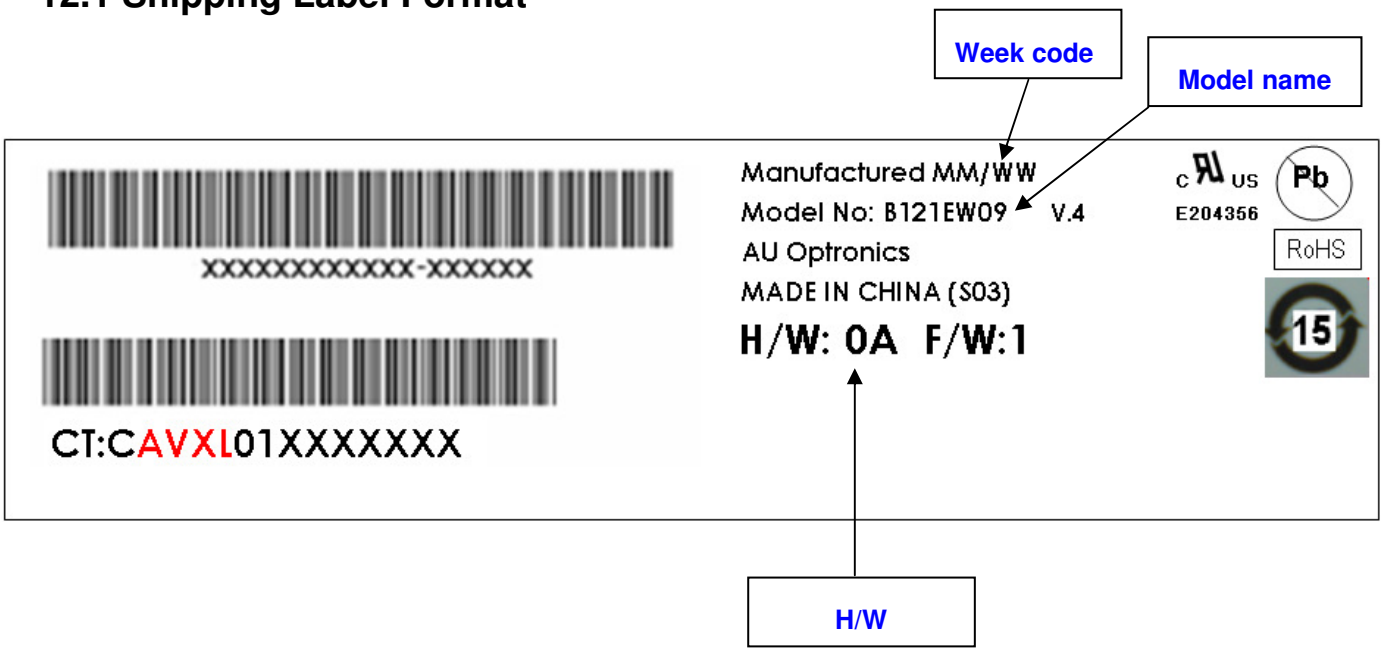
Screw hole minimum depth, from side surface = 2.3 mm (See drawing)

Screw hole center location, from front surface = 3.7 ± 0.2mm (See drawing)
Screw Torque: Maximum 2.5 kgf-cm

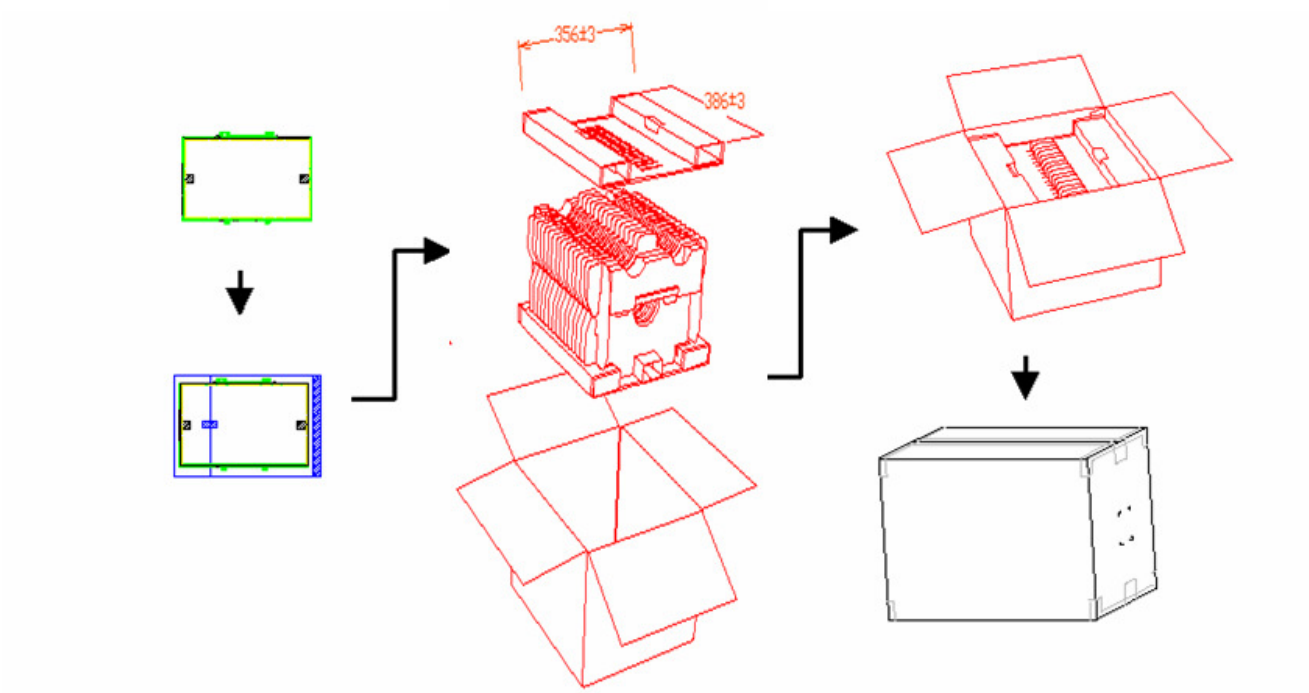


12. Shipping and Package

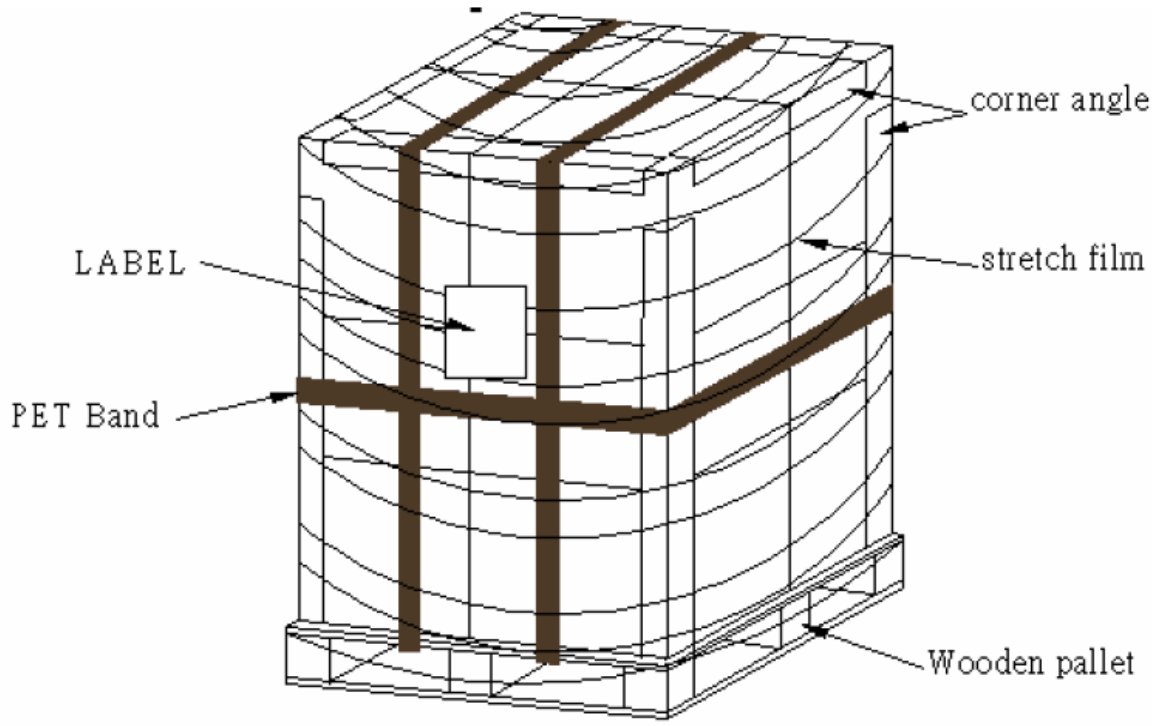
12.1 Shipping Label Format



12.2 Carton package



12.3 Shipping package of palletizing sequence



13. Appendix: EDID description

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	14	00010100	20
0B	hex, LSB first	94	10010100	148
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	00	00000000	0
11	Year of manufacture	13	00010011	19
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	04	00000100	4
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	95	10010101	149
15	**Max H image size** *(rounded to cm)*	1A	00011010	26
16	**Max V image size** *(rounded to cm)*	10	00010000	16
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2
19	Red/green low bits **(Lower 2:2:2:2 bits)**	65	01100101	101
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	85	10000101	133
1B	Red x **(Upper 8 bits)**	8F	10001111	143
1C	Red y/ highER 8 bits	59	01011001	89
1D	Green x	58	01011000	88
1E	Green y	8F	10001111	143
1F	Blue x	26	00100110	38
20	Blue y	1B	00011011	27
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1

27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	12	00010010	18
37	Pixel Clock/10000 USB	1B	00011011	27
38	Horz active **Lower 8bits**	00	00000000	0
39	Horz blanking **Lower 8bits**	8A	10001010	138
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	50	01010000	80
3B	Vertical Active **Lower 8bits**	20	00100000	32
3C	Vertical Blanking **Lower 8bits**	0E	00001110	14
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30	00110000	48
3E	HorzSync. Offset	28	00101000	40
3F	HorzSync.Width	1C	00011100	28
40	VertSync.Offset : VertSync.Width	24	00100100	36
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0
42	Horizontal Image Size **Lower 8bits**	05	00000101	5
43	Vertical Image Size **Lower 8bits**	A3	10100011	163
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0
46	Vertical Border *(zero for internal LCD)*	00	00000000	0
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24
48	Pixel Clock/10,000 (LSB)	0C	00001100	12
49	Pixel Clock/10,000 (MSB)	12	00010010	18
4A	Horizontal Addressable Pixels, lower 8 bits	00	00000000	0
4B	Horizontal Blanking Pixels, lower 8 bits	8A	10001010	138
4C	H Pixels, upper nibble : H Blanking, upper nibble	50	01010000	80
4D	Vertical Addressable Lines, lower 8 bits	20	00100000	32
4E	Vertical Blanking Lines, lower 8 bits	0E	00001110	14
4F	V lines, upper nibble : V blanking, upper nibble	30	00110000	48
50	Horizontal Front Porch, lower 8 bits	28	00101000	40
51	Horizontal Sync Pulse, lower 8 bits	1C	00011100	28

52	V Front Porch, lower nibble : V Sync Pulse, lower nibble	24	00100100	36
53	VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits	00	00000000	0
54	Horizontal Image Size in mm, lower 8 bits	05	00000101	5
55	Vertical Image Size in mm, lower 8 bits	A3	10100011	163
56	H Image Size, upper nibble : V Image Size, upper nibble	10	00010000	16
57	Horizontal Border	00	00000000	0
58	Vertical Border	00	00000000	0
59	Bit Encode Sync Information	18	00011000	24
5A	DC	00	00000000	0
5B	HTOTAL	00	00000000	0
5C	HA	00	00000000	0
5D	HBL	00	00000000	0
5E	HFP	00	00000000	0
5F	HFPe	00	00000000	0
60	HBP	00	00000000	0
61	HB	00	00000000	0
62	HSO	00	00000000	0
63	HS	00	00000000	0
64	VTOTAL	00	00000000	0
65	VA	00	00000000	0
66	VBL	00	00000000	0
67	VFP	00	00000000	0
68	VBP	00	00000000	0
69	VB	00	00000000	0
6A	VSO	00	00000000	0
6B	VS	00	00000000	0
6C	Detail Timing Description #4	00	00000000	0
6D	Flag	00	00000000	0
6E	Reserved	00	00000000	0
6F	For Brightness Table and Power Consumption	02	00000010	2
70	Flag	00	00000000	0
71	PWM % [7:0] @ Step 0	0C	00001100	12
72	PWM % [7:0] @ Step 5	47	01000111	71
73	PWM % [7:0] @ Step 10	F7	11110111	247
74	Nits [7:0] @ Step 0	0A	00001010	10
75	Nits [7:0] @ Step 5	3C	00111100	60
76	Nits [7:0] @ Step 10	64	01100100	100
77	Panel Electronics Power @ 32x32 Chess Pattern =	11	00010001	17
78	Backlight Power @ 60 nits =	12	00010010	18
79	Backlight Power @ Step 10 =	1E	00011110	30
7A	Nits @ 100% PWM Duty =	68	01101000	104
7B	Flag	20	00100000	32

7C	Flag	20	00100000	32
7D	Flag	20	00100000	32
7E	Extension Flag	00	00000000	0
7F	Checksum	80	10000000	128