




# Product Specification

AU OPTRONICS CORPORATION

(✓) Preliminary Specifications

( ) Final Specifications

Module	15.6"HD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B156XTT01.2 (H/W: 1A)
Note (  )	e-TP Display

Customer	Date
_____	_____
Checked & Approved by	Date
_____	_____
Note: This Specification is subject to change without notice.	

Approved by	Date
_____	_____
Prepared by	Date
<u>Alonso JU Hsu</u>	<u>2014/01/13</u>
NBBU Marketing Division AU Optronics corporation	



## Contents

<b>1. Handling Precautions .....</b>	<b>4</b>
<b>2. General Description.....</b>	<b>5</b>
2.1 General Specification .....	5
2.2 Optical Characteristics .....	7
<b>3. Functional Block Diagram .....</b>	<b>12</b>
<b>4. Absolute Maximum Ratings .....</b>	<b>13</b>
4.1 Absolute Ratings of TFT LCD Module .....	13
4.2 Absolute Ratings of Touch Panel.....	13
4.3 Absolute Ratings of Environment .....	13
<b>5. Electrical Characteristics .....</b>	<b>15</b>
5.1 TFT LCD Module .....	15
5.2 Touch Sensor .....	18
5.3 Backlight Unit.....	19
<b>6. Signal Interface Characteristic .....</b>	<b>20</b>
6.1 Pixel Format Image .....	20
6.2 Integration Interface Requirement.....	21
6.3 Interface Timing.....	23
6.4 Power sequence .....	24
<b>7. Panel Reliability Test .....</b>	<b>27</b>
7.1 Vibration Test.....	27
7.2 Shock Test.....	27
7.3 Reliability Test .....	27
<b>8. Mechanical Characteristics .....</b>	<b>28</b>
8.1 LCM Outline Dimension.....	28
<b>9. Shipping and Package.....</b>	<b>30</b>
9.1 Shipping Label Format .....	30
9.2 Carton Package .....	31
9.3 Shipping Package of Palletizing Sequence .....	32
<b>10. Appendix: EDID Description .....</b>	<b>33</b>



# Product Specification

AU OPTRONICS CORPORATION

## Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2013/10/08	All	First Edition for Customer		
0.2 2013/11/08	All		1. Update Outline Dimension, Shipping Label & EDID	
0.3 2014/01/13	P30		Update Label Format	

## 1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electronic breakdown.

## 2. General Description

B156XTT01.2 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x 768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B156XTT01.2 is designed for a display unit of notebook style personal computer and industrial machine.

## 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	394.9			
Active Area	[mm]	344.2 X193.5			
Pixels H x V		1366x3(RGB) x 768			
Pixel Pitch	[mm]	0.252X0.252			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (ILED= TBD mA) (Note: ILED is LED current)	[cd/m <sup>2</sup> ]	200 typ. (5 points average) (Total Solution) 170 min. (5 points average) (Total Solution)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		500 typ.			
Response Time	[ms]	8 typ/16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.7 max. (Include Logic and Blu power)			
Weight	[Grams]	380 max.(Base panel only) 535max			
Physical Size Include bracket (Panel only)	[mm]		Min.	Typ.	Max.
		Length	364.65	364.90	365.15
		Width	224.06	224.56	225.06
Thicknessss		Thicknessss	3.2 (Base panel) 4.2 (Total Solution_Panel Side) 5.2 (Total Solution_PCBA Side)		
Physical Size Include bracket (Total Solution)	[mm]		Min.	Typ.	Max.
		Length	364.65	364.90	365.15
		Width	224.06	224.56	225.06
Electrical Interface		1 Lane eDP			
Glass Thickness	[mm]	0.4			
Surface Treatment		Glare, hardness 3H			
Support Color		262K colors ( RGB 6-bit )			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			



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### 2.1.1 General Touch Specification

Item	Spec	Unit
Type of Touch Sensor	Projective Capacitive (OGS)	
Panel Size	15.6''	
Outline Dimension	357.83 X 205.32 typ	mm
Total Thickness	0.7 typ	mm
Total Weight	140 max	g
TP View Area	345.23 X 194.54 typ	mm
TP Active Area	346.23 X 195.54 typ	mm
Interface	USB and I2C	
Report Rate	Follow win8 – 100Hz	Hz
Multi-Touch Point	10 points	
Input method	Finger	
Touch panel sensor IC	Elan (eKTH3958)	
Channel	72 x 41	
Distance between 2 point	Follow win8 – 13	mm
Surface hardness	7	H
TP F/W version	TBD	
BM ink	PANTONE BLACK C	
Glass	TFT Glass	
TP Power Consumption	Active Mode: 162	mW
	Idle Mode: 108	mW
	Sleep Mode: 1	mW



# Product Specification

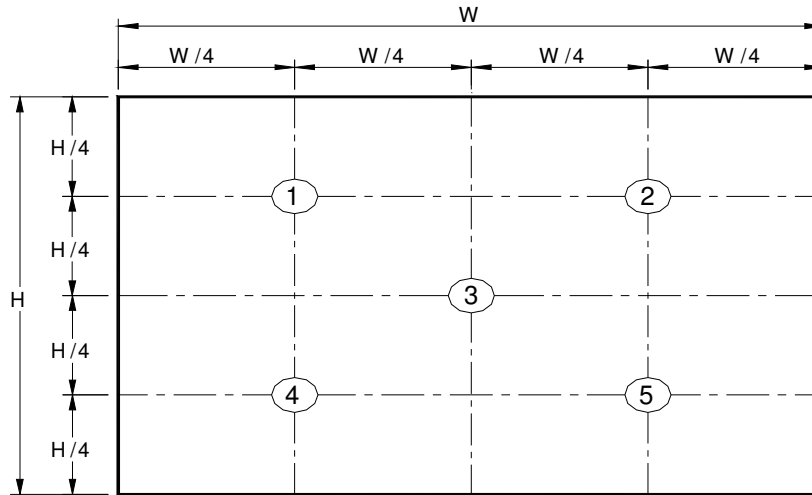
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## 2.2 Optical Characteristics

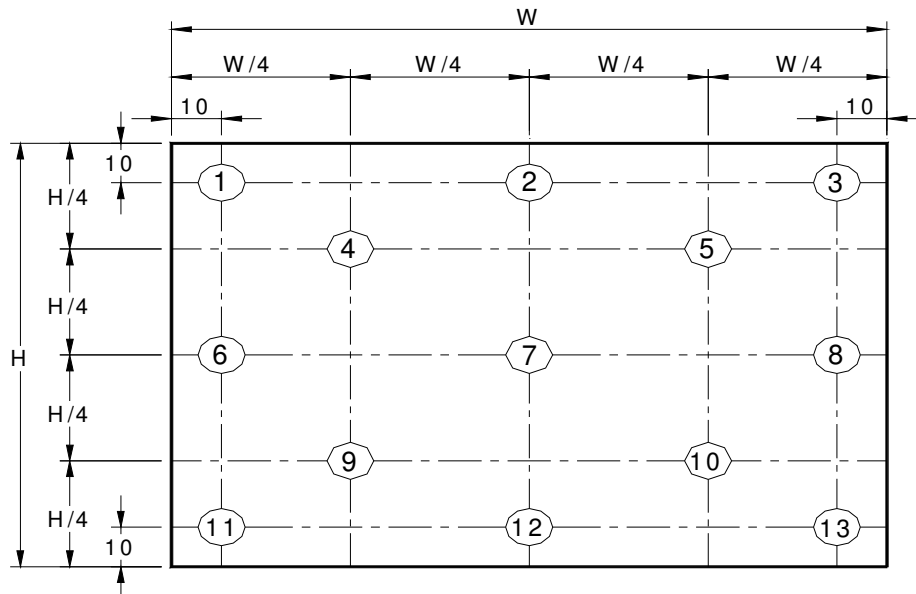
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=20mA			5 points average	170	200	-	cd/m²	1, 4, 5.
Viewing Angle		θ <sub>R</sub> θ <sub>L</sub>	Horizontal (Right) CR = 10 (Left)	40	45	-	degree	4, 9
				40	45	-		
		ψ <sub>H</sub> ψ <sub>L</sub>	Vertical (Upper) CR = 10 (Lower)	10	15	-		
				30	35	-		
Luminance Uniformity		δ <sub>5P</sub>	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ <sub>13P</sub>	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio		CR		400	500	-		4, 6
Cross talk		%				4		4, 7
Response Time		T <sub>RT</sub>	Rising + Falling	-	8	16		
Color / Chromaticity Coordinates	Red	R <sub>x</sub>	CIE 1931	0.550	0.580	0.610		4
		R <sub>y</sub>		0.305	0.335	0.365		
	Green	G <sub>x</sub>		0.300	0.330	0.360		
		G <sub>y</sub>		0.535	0.565	0.595		
	Blue	B <sub>x</sub>		0.125	0.155	0.185		
		B <sub>y</sub>		0.110	0.140	0.170		
	White	W <sub>x</sub>		0.283	0.313	0.343		
		W <sub>y</sub>		0.299	0.329	0.359		
	NTSC			%		-		

**Note 1:** 5 points position (Ref: Active area)



**Note 2:** 13 points position (Ref: Active area)



**Note 3:** The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

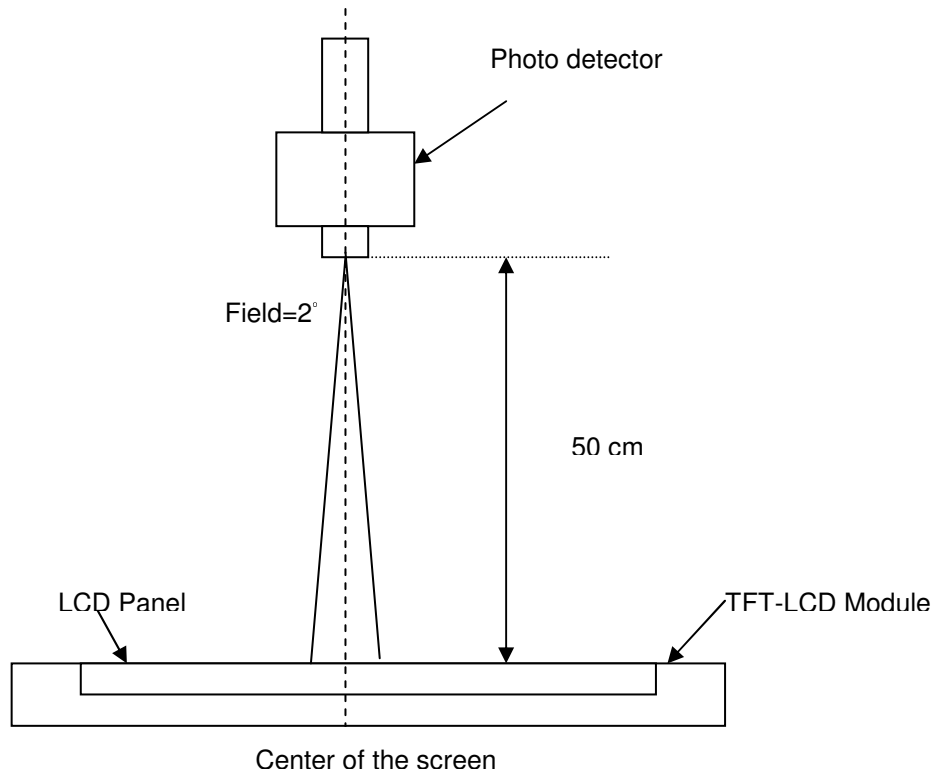
$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

**Note 4:** Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after



lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



**Note 5 :** Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 63 at 5 points ,  $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$  is corresponding to the luminance of the point X at Figure in Note (1).

**Note 6 :** Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

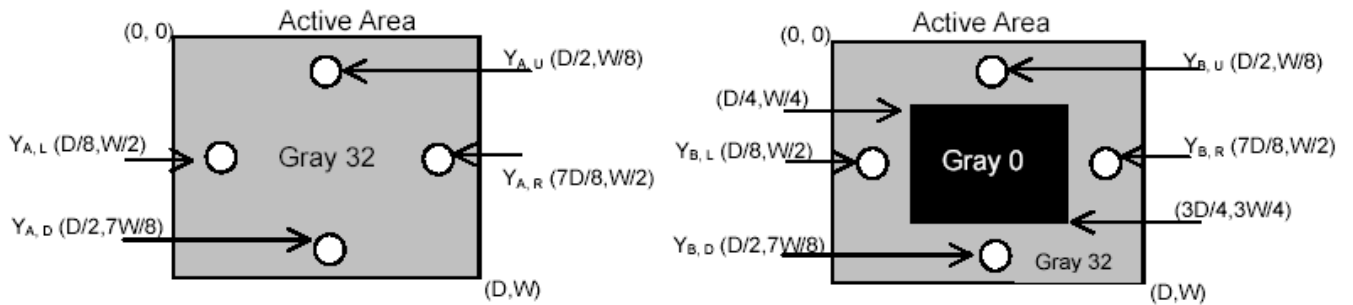
**Note 7 :** Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

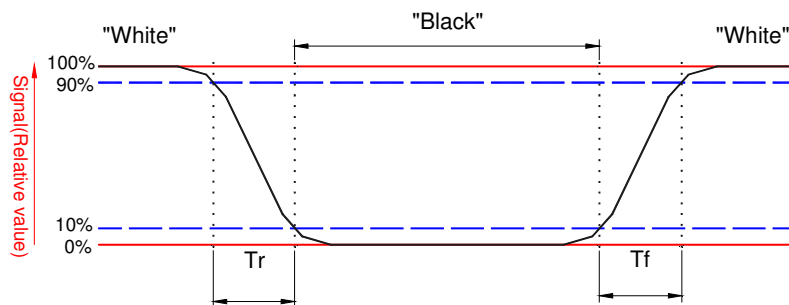
$Y_A$  = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

$Y_B$  = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)



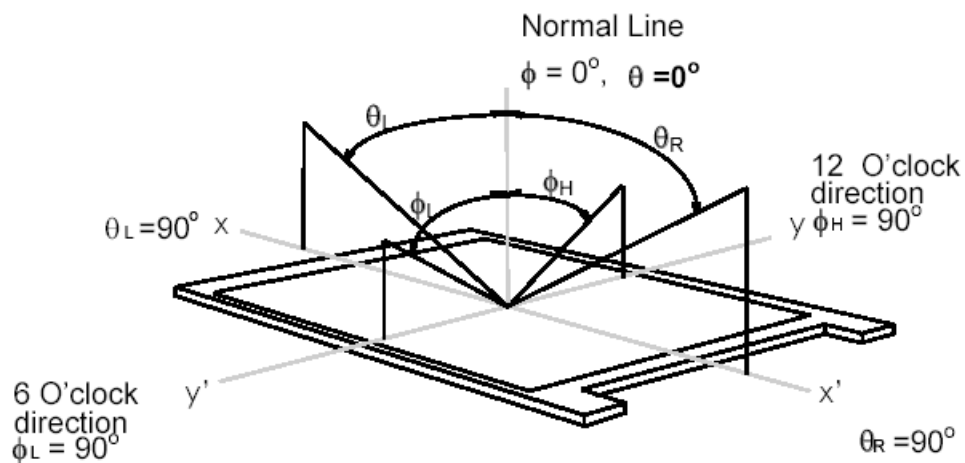
**Note 8:** Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



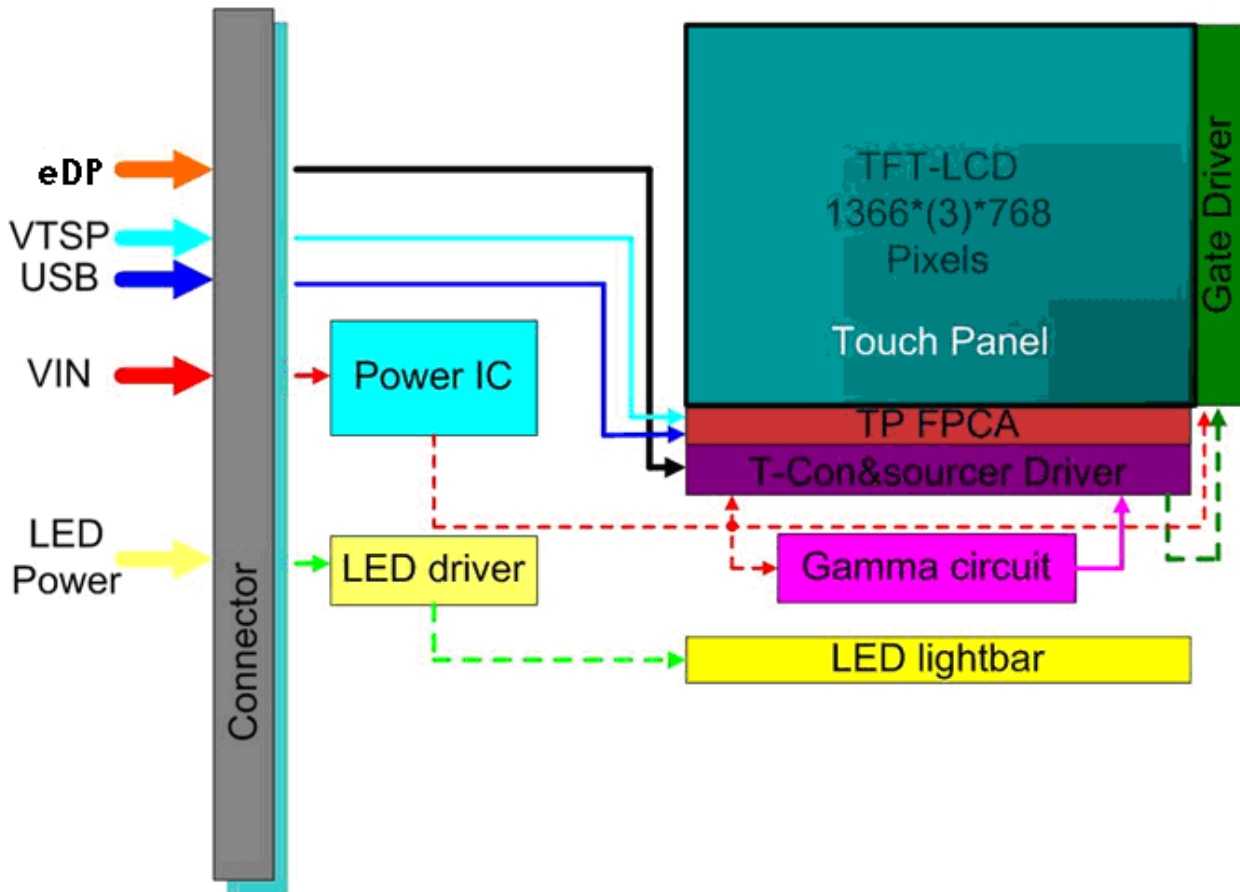
## Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a  $180^\circ$  horizontal and  $180^\circ$  vertical range (off-normal viewing angles). The  $180^\circ$  viewing angle range is broken down as follows;  $90^\circ$  ( $\theta$ ) horizontal left and right and  $90^\circ$  ( $\Phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



## 3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 40 Pin (One CH/connector Module)





## 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

### 4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

### 4.2 Absolute Ratings of Touch Panel

Item	Symbol	Rating	Unit	Conditions
Voltage from VTSP to AGND and DGND	-	+4.0	[Volt]	-
Voltage from any pin to AGND and DGND	-	+4.0	[Volt]	-

### 4.3 Absolute Ratings of Environment

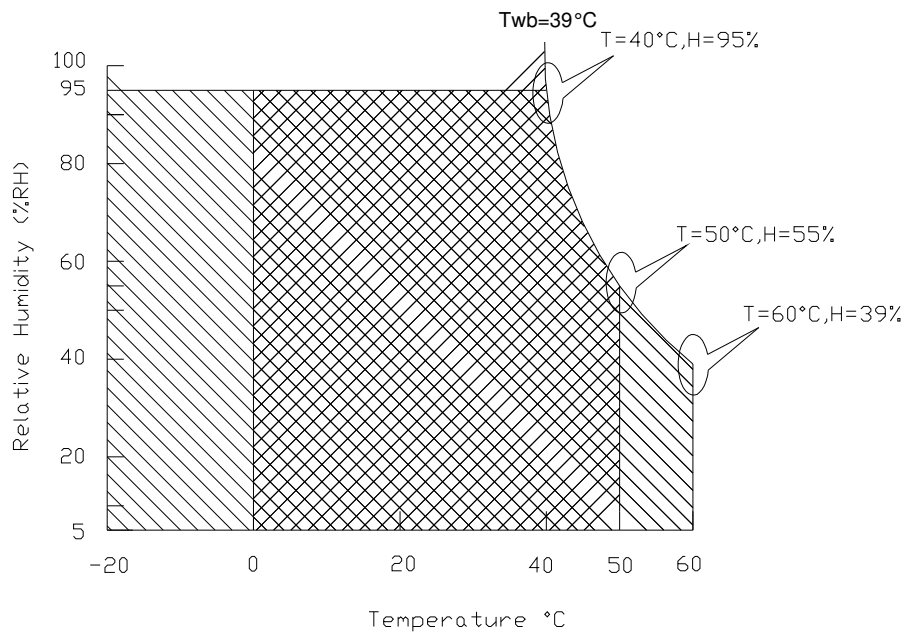
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C )

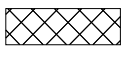
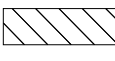
Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

## 5. Electrical Characteristics

### 5.1 TFT LCD Module

#### 5.1.1 Power Specification

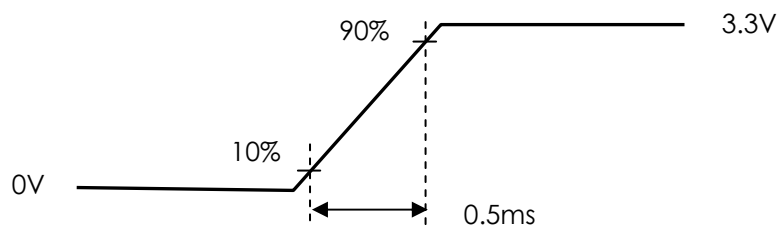
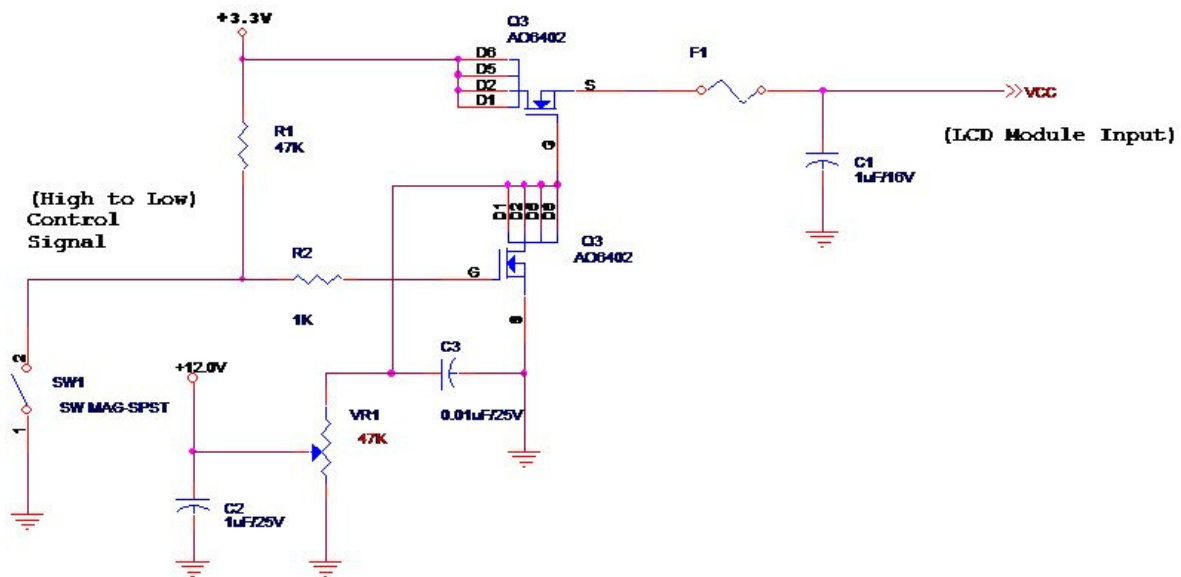
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.0	[Watt]	Note 1
IDD	IDD Current	-	-	166	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ( $P_{max} = V_{3.3} \times I_{black}$ )

Note 2 : Measure Condition



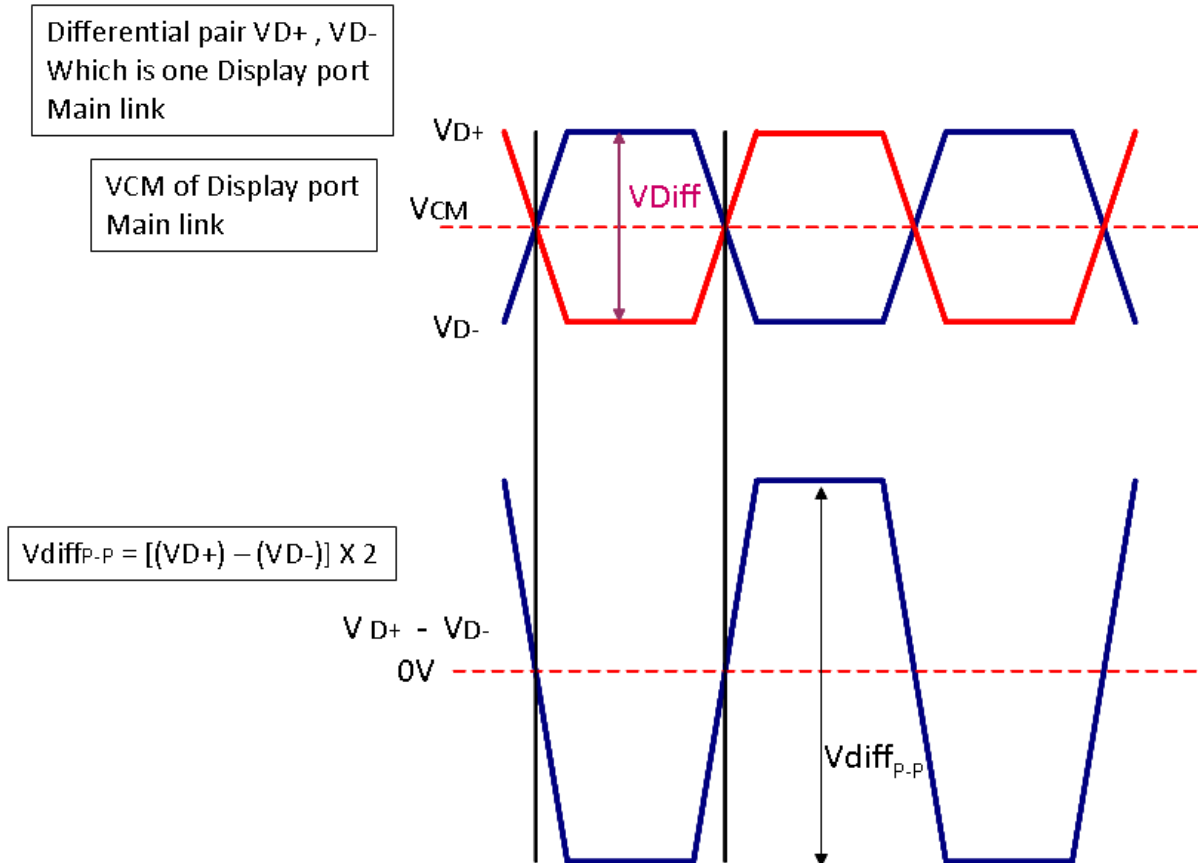
Vin rising time

## 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

### Display Port main link signal:



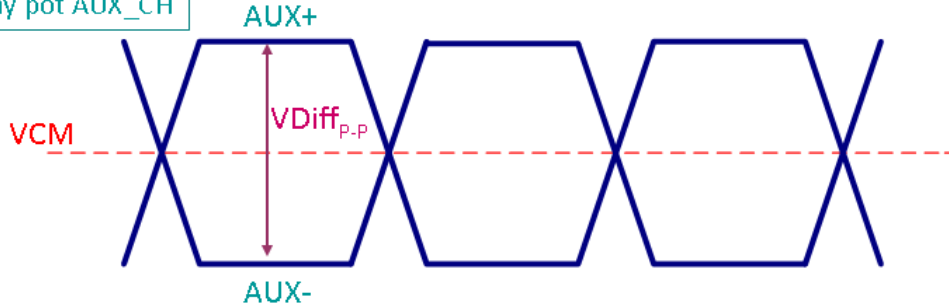
Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$V_{Diff_{P-P}}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Fallow as VESA display port standard V1.1a



## Display Port AUX\_CH signal:

Differential AUX+ , AUX-  
Which is Display port AUX\_CH



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff <sub>P-P</sub>	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Fallow as VESA display port standard V1.1a.

## Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

Fallow as VESA display port standard V1.1a.

## 5.2 Touch Sensor

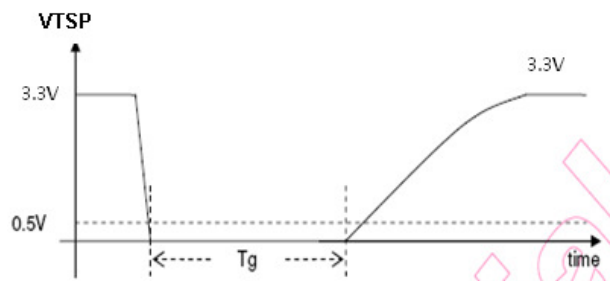
### 5.2.1 Power Specification

Items	Symbol	Specifications			Unit	Notes
		Min.	Typ.	Max.		
Touch Panel Power Supply	VTSP	3.15	3.3	3.6	V	Ripple <100mV
Input voltage	VIH	VTSP×0.7	-	VTSP	V	
	VIL	0	-	VTSP ×0.3	V	
Normal mode Current consumption @ Report rate 100Hz	INORMAL	-	-	45	mA	
Idle mode Current consumption	IIDLE	-	-	30	mA	
Sleep mode Current consumption	ISLEEP	-	60	130	uA	

### 5.2.2 Touch Sensor TP\_EN

TP_EN	TP Function
H	Ok
L	No function
NC	Ok

### 5.2.3 Touch Power off and then Power on Sequence



During power off, the VTSP must be lower than 0.5V for at least 10us ( $T_g > 10\mu s$ ) to make sure the touch controller be correctly reset.



## Product Specification

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### 5.3 Backlight Unit

#### 5.3.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.7	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 If=20 mA

**Note 1:** Calculator value for reference  $P_{LED} = V_F$  (Normal Distribution) \*  $I_F$  (Normal Distribution) / Efficiency

**Note 2:** The LED life-time define as the estimated time to 50% degradation of initial luminous.

#### 5.3.2 Backlight input signal characteristics

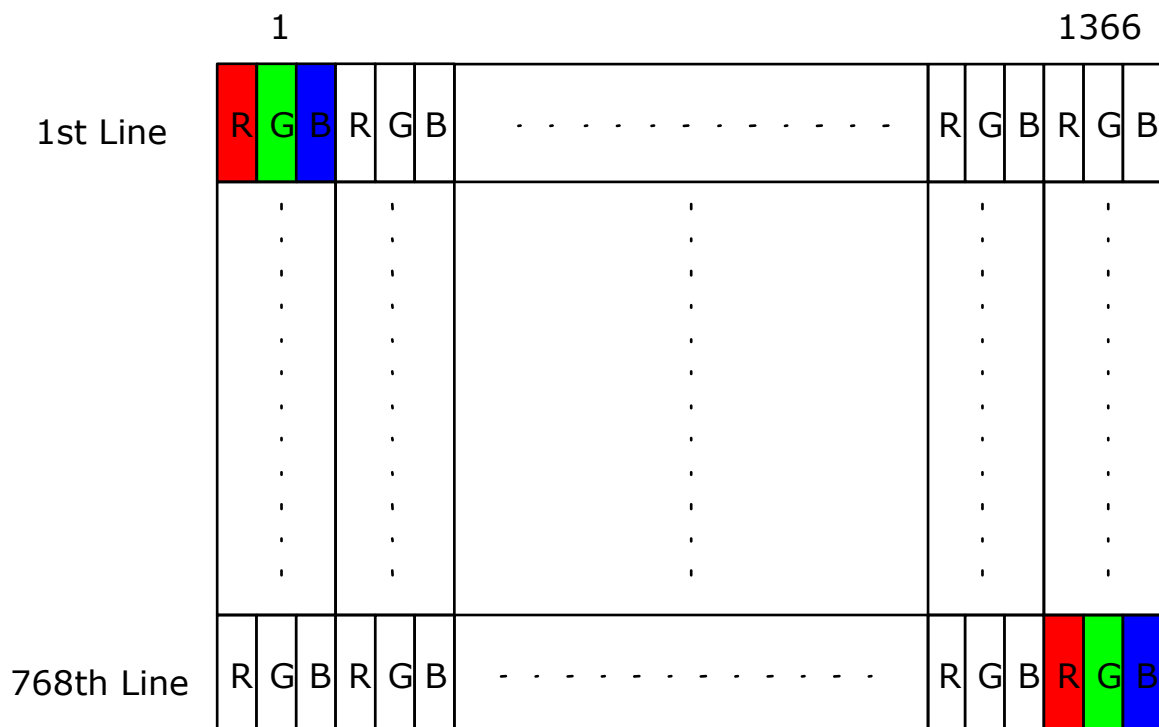
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN *Note 1	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN *Note 1	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

**Note 1 :** Recommend system pull up/down resistor no bigger than 10kohm

## 6. Signal Interface Characteristic

### 6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



## 6.2 Integration Interface Requirement

### 6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	STM or Compatible
Type / Part Number	STM MSAK24025P40 or compatible
Mating Housing/Part Number	IPEX 20453-040T-11 or compatible

### 6.2.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	No Connect (Reserved for DCR)
2	H_GND	High Speed Ground
3	NC	No Connect
4	NC	No Connect
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off



## Product Specification

AU OPTRONICS CORPORATION

23	BL_PWM_DIM	System PWM signal Input
24	NC	No connect (Reverse for AUO TEST only)
25	NC	No connect (Reverse for AUO TEST only)
26	BL_PWR	Backlight power (6V~21V)
27	BL_PWR	Backlight power (6V~21V)
28	BL_PWR	Backlight power (6V~21V)
29	BL_PWR	Backlight power (6V~21V)
30	NC	No Connect (Reserved for CM)
31	TP_D-	USB Data- for Touch
32	TP_D+	USB Data+ for Touch
33	GND	Ground-Shield
34	VTSP	Touch panel power supply (3.3V)
35	VTSP	Touch panel power supply (3.3V)
36	NC/TP_EN	No Connection (Reserve for Touch function enable)
37	TP_CLK	I2C Clock for Touch (NC for USB input)
38	TP_Data	I2C Data for Touch (NC for USB input)
39	INT	Interrupt for Touch (NC for USB input)
40	RST	Reset for Touch (NC for USB input)

Note1 : start from right side

Note2 : Input signals shall be low or High-impedance state when VDD is off.

## 6.3 Interface Timing

### 6.3.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

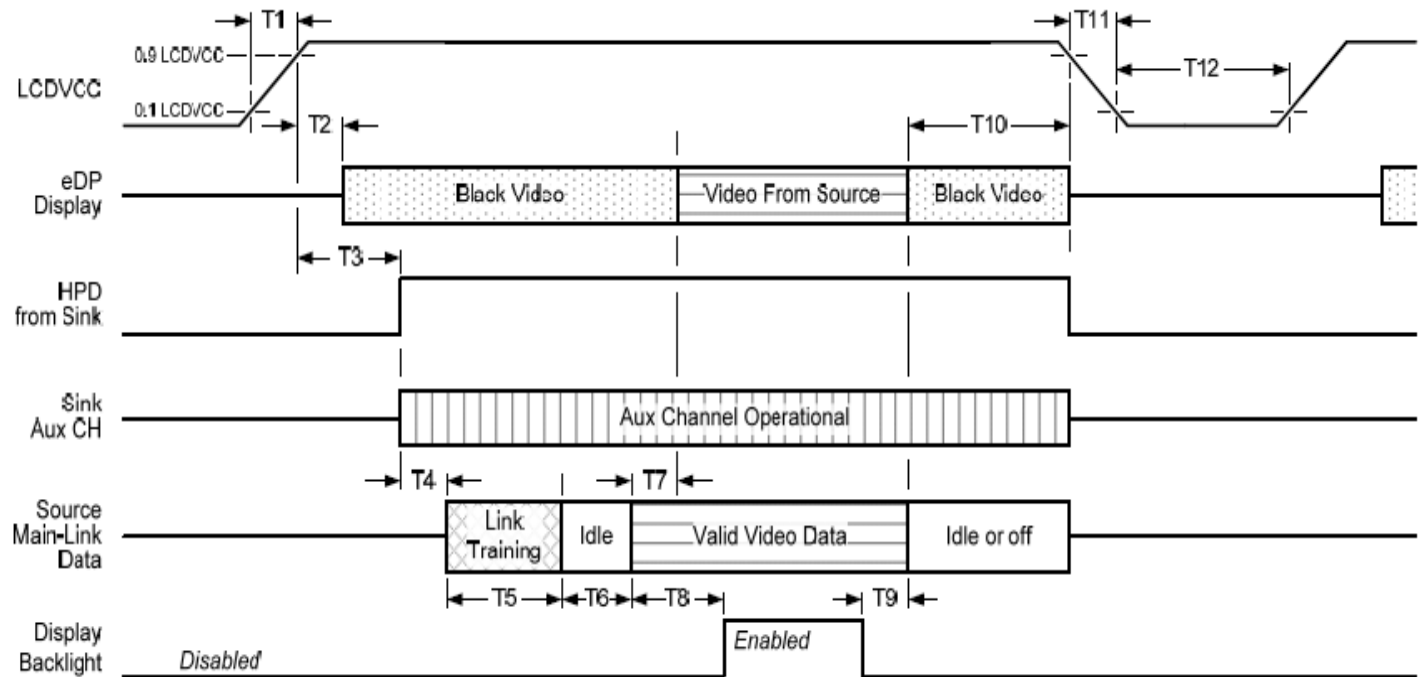
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T <sub>Clock</sub>	66.9	72	80	MHz
Vertical Section	Period	T <sub>V</sub>	788	824	768+A	T <sub>Line</sub>
	Active	T <sub>VD</sub>	768			
	Blanking	T <sub>VB</sub>	20	56	A	
Horizontal Section	Period	T <sub>H</sub>	1416	1456	1366+B	T <sub>Clock</sub>
	Active	T <sub>HD</sub>	1366			
	Blanking	T <sub>HB</sub>	50	90	B	

**Note 1 :** DE mode only

**Note 2 :** The maximum clock frequency = (1366+B)\*(768+A)\*60<80MHz

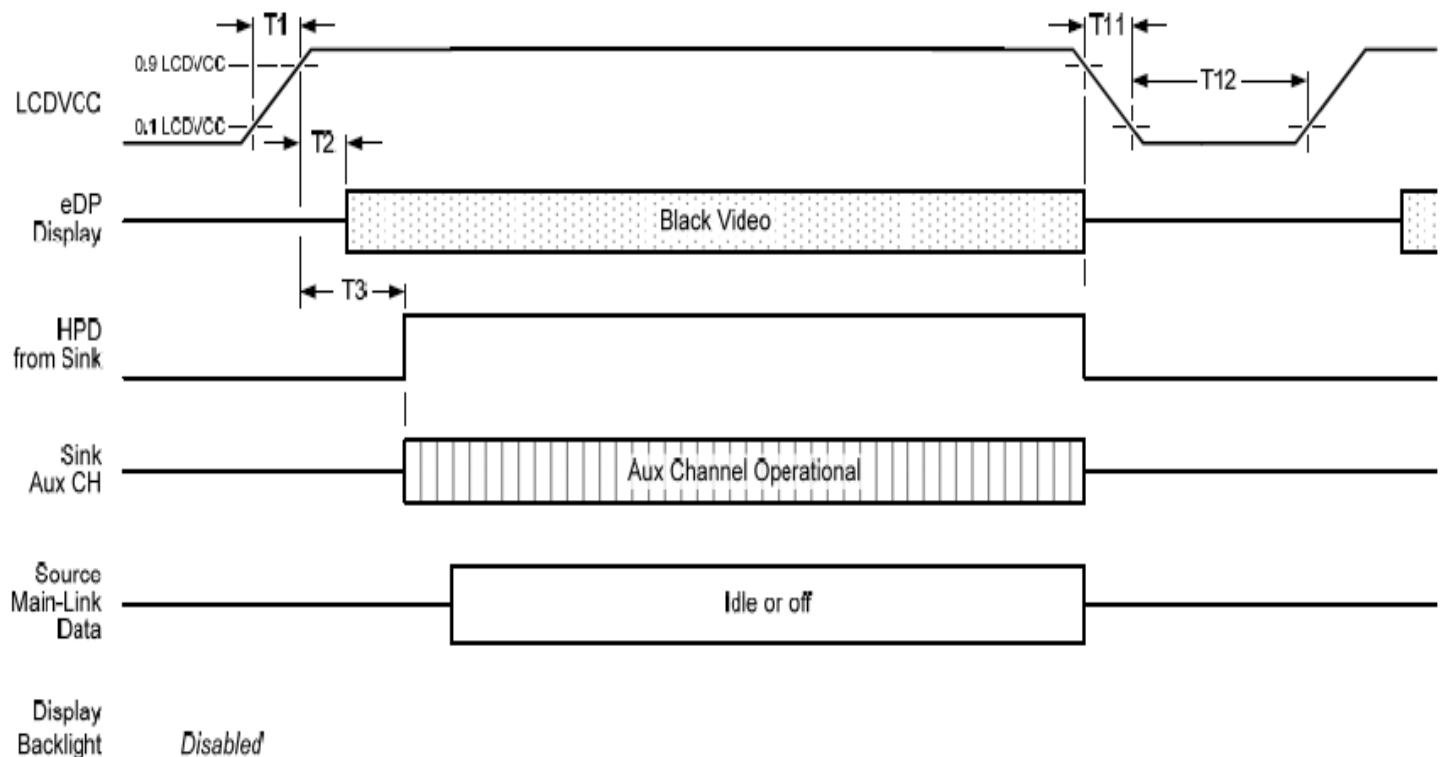
## 6.4 Power sequence

### Display Port panel power sequence:



### Display port interface power up/down sequence, normal system operation

### Display Port AUX\_CH transaction only:



### Display port interface power up/down sequence, AUX\_CH transaction only





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## Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

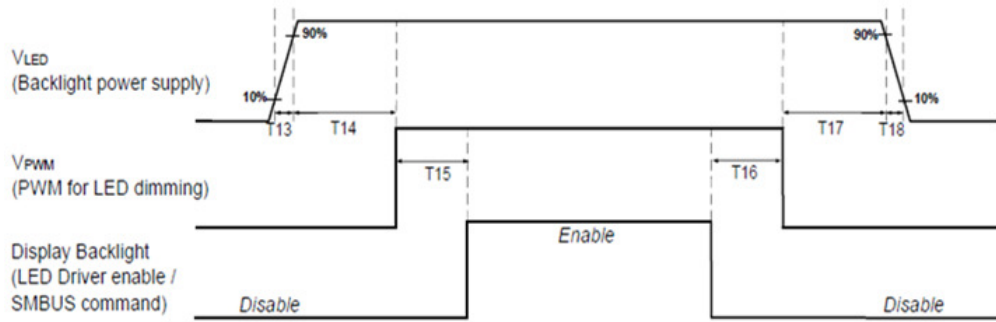
**Note1:** The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

- upon LCDVDD power on (within T2 max)-when the "Novideostream\_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
- when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

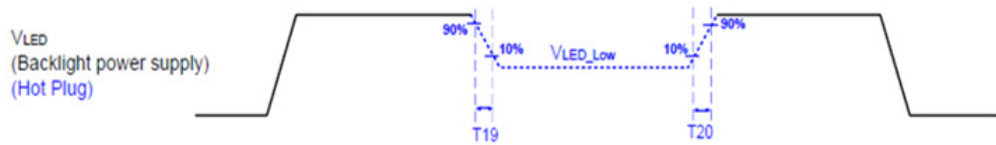
**Note 2:** The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

**Note 3:** The sink must support AUX\_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX\_CH transaction with the time specified within T3 max.

## Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change:  $T19/T20 = 5 \times T_{PWM}^*$

\* $T_{PWM} = 1/PWM \text{ Frequency}$

## 7. Panel Reliability Test

### 7.1 Vibration Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

### 7.2 Shock Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

### 7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃ , 90%RH, 300h	
High Temperature Operation	Ta= 50℃ , Dry, 300h	
Low Temperature Operation	Ta= 0℃ , 300h	
High Temperature Storage	Ta= 60℃ , 35%RH, 300h	
Low Temperature Storage	Ta= -20℃ , 50%RH, 250h	
Thermal Shock Test	Ta=-20℃to 60℃ , Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

**Note1:** According to EN 61000-4-2 , ESD class B: Some performance degradation allowed.

Self-recoverable.

No data lost, No hardware failures.

**Remark:** MTBF (Excluding the LED): 30,000 hours with a confidence level 90%



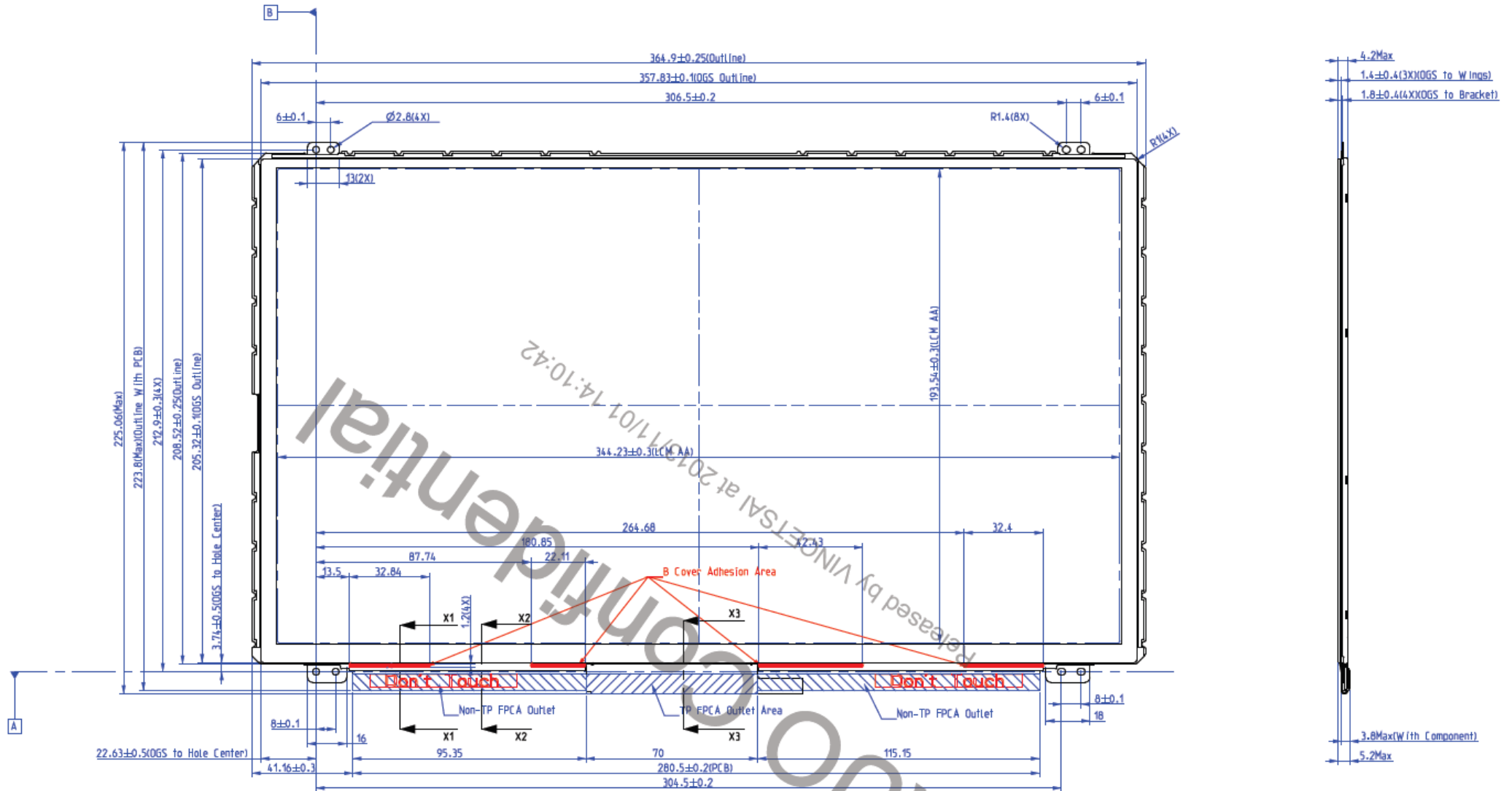
# Product Specification

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## 8. Mechanical Characteristics

### 8.1 LCM Outline Dimension

#### 8.1.1 Standard Front View



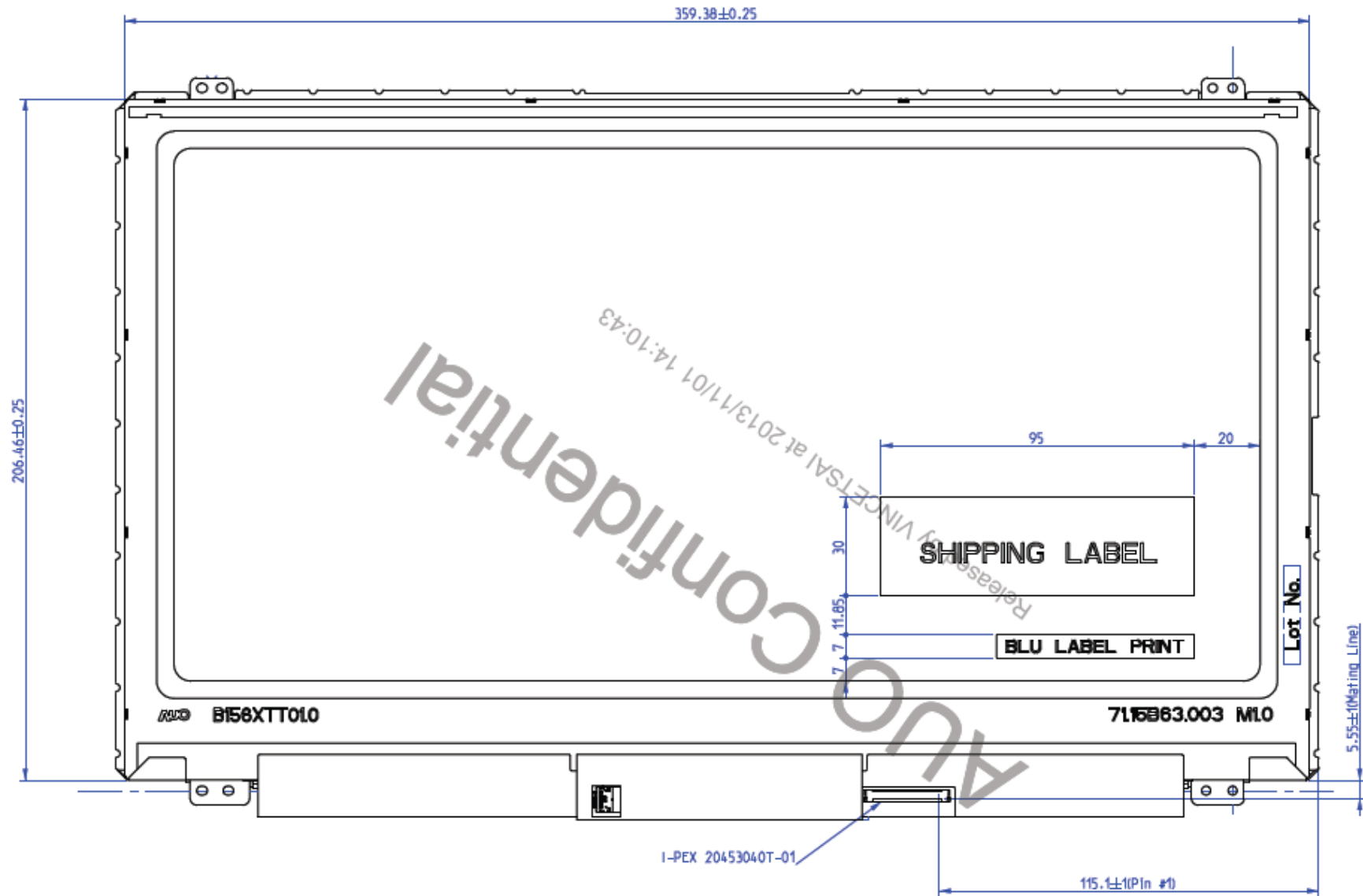
The drawing following 2D standard drawing and remark.



## Product Specification

AU OPTRONICS CORPORATION

### 8.1.2 Standard Rear View





## 9. Shipping and Package

### 9.1 Shipping Label Format

 XXXXXXXXXXXX-XXXXXX	Manufactured MM/WW Model No: B156XTT01.2 AU Optronics MADE IN CHINA (S01) H/W: 1A F/W:1	c  US E204356 
 CT : CECJK 01XXXXXX		 

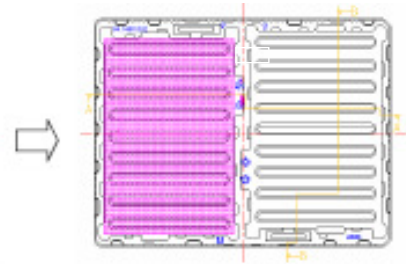
## 9.2 Carton Package



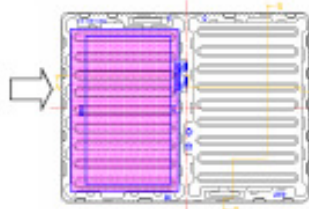
取出白色 PP 瓦楞板



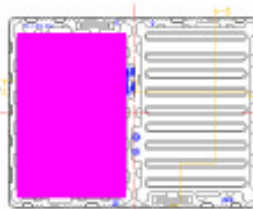
Tray 置放於 PP 瓦楞板上



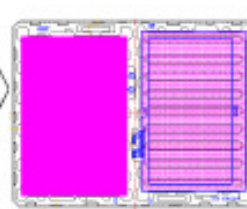
EPE spacer 放於 tray 盤上  
左側穴內



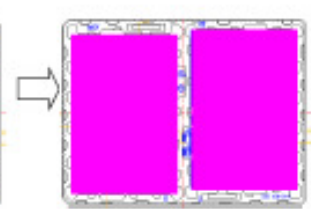
PANEL 放於 spacer 上, PCBA 側  
朝 tray 盤內側放入, sensor 面朝



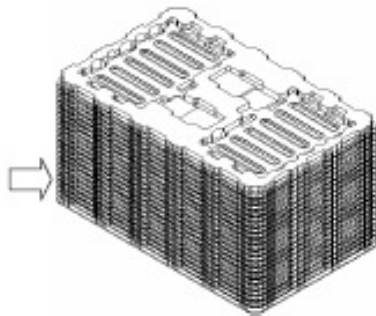
再放入 EPE spacer  
於 SKD 上



EPE spacer 放於 tray 盤上  
右側穴內



先置 SKD 再放入 EPE  
spacer 於 SKD 上



Tray 依上述方式依序堆疊  
(TP 共 16 片, tray 共 17 片,最上面第 17 個  
tray 是空的)



完成堆疊的 tray 放入靜電袋中,  
並使用 tape 封口



EPE cushion 放入紙箱



將包好靜電袋的 tray 整落  
放入紙箱中



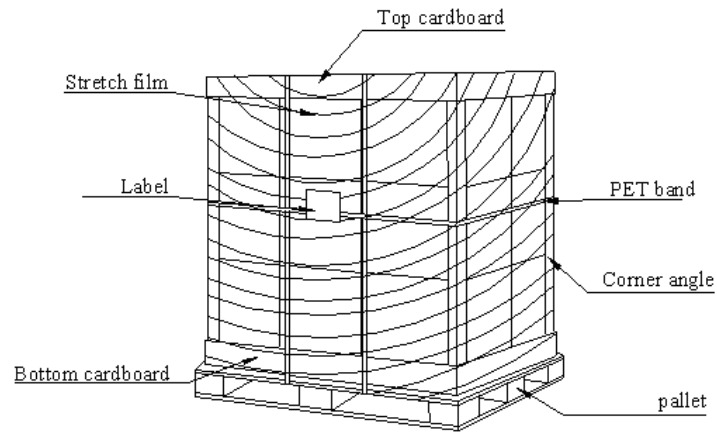
放入 EPE cushion



Tape 封紙箱



## 9.3 Shipping Package of Palletizing Sequence







# Product Specification

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## 10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	0000000 0	0	
01		FF	1111111 1	255	
02		FF	1111111 1	255	
03		FF	1111111 1	255	
04		FF	1111111 1	255	
05		FF	1111111 1	255	
06		FF	1111111 1	255	
07		00	0000000 0	0	
08	EISA Manuf. Code LSB	06	0000011 0	6	
09	Compressed ASCII	AF	1010111 1	175	
0A	Product Code	EC	1110110 0	236	
0B	hex, LSB first	12	0001001 0	18	
0C	32-bit ser #	00	0000000 0	0	Color Engine Setting
0D		00	0000000 0	0	
0E		00	0000000 0	0	
0F		00	0000000 0	0	
10	Week of manufacture	00	0000000 0	0	
11	Year of manufacture	17	0001011 1	23	
12	EDID Structure Ver.	01	0000000 1	1	
13	EDID revision #	04	0000010 0	4	
14	<b>Video input def.</b> (digital I/P, non-TMDS, CRGB)	95	1001010 1	149	
15	<b>Max H image size</b> (rounded to cm)	22	0010001 0	34	
16	<b>Max V image size</b> (rounded to cm)	13	0001001 1	19	
17	<b>Display Gamma</b> $(=(\text{gamma} \times 100) - 100)$	78	0111100 0	120	
18	<b>Feature support</b> (no DPMS, Active OFF, RGB, tmg Blk#1)	02	0000001 0	2	
19	Red/green low bits ( <b>Lower 2:2:2:2 bits</b> )	BB	1011101 1	187	
1A	Blue/white low bits ( <b>Lower 2:2:2:2 bits</b> )	F5	1111010 1	245	
1B	Red x ( <b>Upper 8 bits</b> )	94	1001010 0	148	
1C	Red y/ highER 8 bits	55	0101010 1	85	
1D	Green x	54	0101010 0	84	
1E	Green y	90	1001000 0	144	
1F	Blue x	27	0010011 0	39	



# Product Specification

AU OPTRONICS CORPORATION

			1		
20	Blue y	23	0010001 1	35	
21	White x	50	0101000 0	80	
22	White y	54	0101010 0	84	
23	Established timing 1	00	0000000 0	0	
24	Established timing 2	00	0000000 0	0	
25	Established timing 3	00	0000000 0	0	
26	Standard timing #1	01	0000000 1	1	
27		01	0000000 1	1	
28	Standard timing #2	01	0000000 1	1	
29		01	0000000 1	1	
2A	Standard timing #3	01	0000000 1	1	
2B		01	0000000 1	1	
2C	Standard timing #4	01	0000000 1	1	
2D		01	0000000 1	1	
2E	Standard timing #5	01	0000000 1	1	
2F		01	0000000 1	1	
30	Standard timing #6	01	0000000 1	1	
31		01	0000000 1	1	
32	Standard timing #7	01	0000000 1	1	
33		01	0000000 1	1	
34	Standard timing #8	01	0000000 1	1	
35		01	0000000 1	1	
36	Pixel Clock/10000 LSB	A2	1010001 0	162	
37	Pixel Clock/10000 USB	1C	0001110 0	28	
38	Horz active <b>Lower 8bits</b>	56	0101011 0	86	
39	Horz blanking <b>Lower 8bits</b>	A0	1010000 0	160	
3A	HorzAct:HorzBlnk <b>Upper 4:4 bits</b>	50	0101000 0	80	
3B	Vertical Active <b>Lower 8bits</b>	00	0000000 0	0	
3C	Vertical Blanking <b>Lower 8bits</b>	20	0010000 0	32	
3D	Vert Act : Vertical Blanking <b>(upper 4:4 bit)</b>	30	0011000 0	48	
3E	HorzSync. Offset	28	0010100 0	40	
3F	HorzSync.Width	20	0010000 0	32	
40	VertSync.Offset : VertSync.Width	36	0011011 0	54	
41	Horz&Vert Sync Offset/Width <b>Upper 2bits</b>	00	0000000 0	0	



# Product Specification

AU OPTRONICS CORPORATION

42	Horizontal Image Size <b>Lower 8bits</b>	58	0101100 0	88	
43	Vertical Image Size <b>Lower 8bits</b>	C1	1100000 1	193	
44	Horizontal & Vertical Image Size <b>(upper 4:4 bits)</b>	10	0001000 0	16	
45	Horizontal Border <i>(zero for internal LCD)</i>	00	0000000 0	0	
46	Vertical Border <i>(zero for internal LCD)</i>	00	0000000 0	0	
47	Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i>	18	0001100 0	24	
48	Detailed timing/monitor	00	0000000 0	0	
49	descriptor #2	00	0000000 0	0	
4A		00	0000000 0	0	
4B		0F	0000111 1	15	
4C		00	0000000 0	0	
4D		00	0000000 0	0	
4E		00	0000000 0	0	
4F		00	0000000 0	0	
50		00	0000000 0	0	
51		00	0000000 0	0	
52		00	0000000 0	0	
53		00	0000000 0	0	
54		00	0000000 0	0	
55		00	0000000 0	0	
56		00	0000000 0	0	
57		00	0000000 0	0	
58		00	0000000 0	0	
59		20	0010000 0	32	
5A	Detailed timing/monitor	00	0000000 0	0	
5B	descriptor #3	00	0000000 0	0	
5C		00	0000000 0	0	
5D		FE	1111111 0	254	
5E		00	0000000 0	0	
5F	Manufacture	41	0100000 1	65	A
60	Manufacture	55	0101010 1	85	U
61	Manufacture	4F	0100111 1	79	O
62		0A	0000101 0	10	
63		20	0010000 0	32	
64		20	0010000 0	32	



# Product Specification

AU OPTRONICS CORPORATION

65		20	0010000 0	32	
66		20	0010000 0	32	
67		20	0010000 0	32	
68		20	0010000 0	32	
69		20	0010000 0	32	
6A		20	0010000 0	32	
6B		20	0010000 0	32	
6C	Detailed timing/monitor	00	0000000 0	0	
6D	descriptor #4	00	0000000 0	0	
6E		00	0000000 0	0	
6F		FE	1111111 0	254	
70		00	0000000 0	0	
71	Manufacture P/N	42	0100001 0	66	B
72	Manufacture P/N	31	0011000 1	49	1
73	Manufacture P/N	35	0011010 1	53	5
74	Manufacture P/N	36	0011011 0	54	6
75	Manufacture P/N	58	0101100 0	88	X
76	Manufacture P/N	54	0101010 0	84	T
77	Manufacture P/N	54	0101010 0	84	T
78	Manufacture P/N	30	0011000 0	48	0
79	Manufacture P/N	31	0011000 1	49	1
7A	Manufacture P/N	2E	0010111 0	46	.
7B	Manufacture P/N	32	0011001 0	50	2
7C		20	0010000 0	32	
7D		0A	0000101 0	10	
7E	Extension Flag	00	0000000 0	0	
7F	Checksum	62	0110001 0	98	