AU Optronics Corp.

Doc. version :	7
Total pages :	21
Date :	2003.11.24

Product Specification

1.5″ COLOR TFT-LCD MODULE

MODEL NAME: A015AN02

< >Preliminary Specification

< ◆ > Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0	25/Dec./2001		First draft.
1	10/Apr./2002		FPC length revised
		5	Normal mode: (U/D,SHL): (H,H) → (L,H) Reverse mode: (U/D,SHL): (L,L) → (H,L)
		6	V_{GLAC}: 5.6(typ)→ 5.2(typ)
			V_{GL_H}: -8.1(min). -9.0(typ), -9.9(max) → -8.1(min), -7.1(typ), -6.1(max)
			V_{CAC}: 5.6(typ)→ 5.2(typ)
			I_{GH}: 0.3(typ) mA (V_{GH}=15V)→ 0.13(typ) mA (V_{GH}=17V)
			I_{GL}: -0.6(typ) mA (V_{GH}=-10V)→ -0.19(typ) mA (V_{GL}=-8V)
			I_{CC}: 0.8(typ), 2(max) mA→ 2(typ), 4(max) mA
			I_{DD}: 1.5(typ), 2(max) mA→ 1.15(typ), 2(max) mA
		8	Y: 0.30(min)→0.29(min)
		9	Vertical display start: 15 → 25
		11	Revised the packing form drawing
			Mechical drawing revised
2	09/May/2002		Dc-Dc converter, I/O equivalent circuit
		13	*Revised packing form*
3	31/May/2002	3	Surface treatment: Hard coating(3H)
		7	V_{CAC},V_{GL-AC}: 5.2V→5.6V
		8	Dc-Dc block Output voltage: 13V→13.5V; Vref: 1.25V→1.2V
		12	Add FPC reliability test item
		13	Update outline drawing
		21	Updated application circuit
4	03/Sep/2002	14	Change Package to 420 pcs/Box
5	12/Sep/2002	7	add LED current min and max value
6	*09/Dec/2002*	*7*	Remove LED typical voltage and add LED maximum voltage
11	*24/Nov/2003*	*11*	Revised white chromacity x(0.27~0.35) to(0.26~0.36)

Contents:

A. Physical specification **P3**

B. Electrical specifications **P4**

1. Pin assignment **P4**

a. TFT-LCD panel driving section **P5**

b. Backlight driving section **P5**

2. Equivalent circuit of I/O **P6**

3. Absolute maximum ratings **P6**

4. Electrical characteristics **P6**

a. Typical operating conditions **P6**

b. Current consumption **P7**

c. Backlight driving conditions **P7**

5. AC Timing **P7**

a. Timing conditions **P7**

b. Timing diagram **P8**

6. Dc-Dc converter circuit **P9**

a. Boost converter **P9**

b. Shutdown mode **P10**

c. Oscillator circuit **P10**

C. Optical specifications **P10**

D. Reliability test items **P12**

E. Packing form **P13**

Appendix:

Fig1 DC-DC converter block diagram **P9**
Fig2 DCCK block diagram **P9**
Fig3.PWM control state diagram **P10**
Fig.4 Outline dimension of TFT-LCD module **P14**
Fig.5 Input signal timing relationship **P15**
Fig.6 Input vertical timing **P16**
Fig.7 Horizontal input timing **P17**
Fig.8 Hsync, Vsync, Data, DCLk relationship **P18**

Reference:

Fig.9 Horizontal Input Timing (Wedding CLK Explanation) **P19**
Fig.10 Pre-filtering function timing diagram and block iagram **P20**
Fig.11 Application circuit **P21**

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution(dot)	280(W) ×220(H)	
2	Active area(mm)	29.54(W) ×22.22(H)	
3	Screen size(inch)	1.45(Diagonal)	
4	Dot pitch(mm)	0.1055(W) ×0.101(H)	
5	Color configuration	R. G. B. delta	
6	Overall dimension(mm)	40.5(W) ×34.65(H) ×3.9(D)	Note 1
7	Weight(g)	10 Typ.	
8	Panel Surface treatment	Hard coating (3H)	

Note 1: Refer to Fig. 4

B. Electrical specifications

1.Pin assignment

a. TFT-LCD panel driving section

Pin no	Symbol	I/O	Description	Remark
1	GND	-	Ground for logic circuit	
2	V_{CC}	P	Supply voltage of logic control circuit for scan driver	
3	V_{GL}	P	Negative power for scan driver	
4	V_{GH}	P	Positive power for scan driver	
5	FRP	O	Gate driver input signal that is fram polarity output for Vcom	
6	VCOM	I	Common electrode driving signal	
7	DRV	VO	Power transistor gate signal for the boost converter	
8	FB	VI	Main boost regulator feedback input(FB threshold is 1.2V)	
9	SHL	I	Left/Right scan control input	Note 1
10	STB	I	Stand by mode setting pin.	Note 2
11	V_{CC}	P	Supply voltage for digital circuit	
12	SHDB	I	Shutdown input. Active low.	Note 3
13	AGND	P	Ground pins for analog circuits	
14	VLED	I	LED Anode	
15	GLED	O	LED Cathode	
16	AVDD	P	Power supply for analog circuits	
17	HSYNC	I	Horizontal sync input. Negative polarity	
18	VSYNC	I	Vertical sync input. Negative polarity.	
19	DCLK	I	Clock signal; latch data onto line latches at the rising edge.	
20	D05	I	Data input. :MSB	
21	D04	I	Data input	
22	D03	I	Data input	
23	D02	I	Data input	
24	D01	I	Data input	
25	D00	I	Data input. :LSB	
26	GRB	I	Global reset pin.	Note 4
27	U/D	I	Up/Down scan control input	Note 1

28	GND	-	GND for logic circuit	
29	AVDD1	P	Supply of positive power for level shift circuit.	
30	AGND1	P	Ground for level shift circuit	

I: Input; O: Output. VI: voltage input VO: voltage output P:power

Note 1: Selection of scanning mode

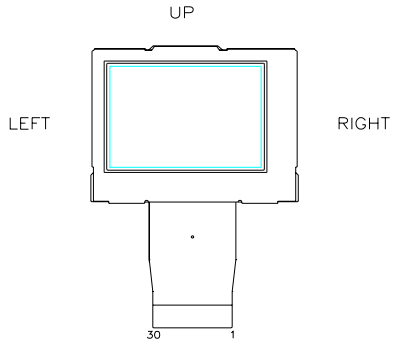
Mode	Setting of scan control input		Scanning direction
	U/D	SHL	Note 5
Normal mode	L	H	From up to down, and from left to right.
Reverse mode	H	L	From down to up, and from right to left.

Note 2: Stand by mode(STB).If STB high, it is normal operation.
If it is low, it is standby function. Normally pulled high.

Note 3:Shutdown input(SHDB).Active low, DC-DC converter is off when SHDB is low, Normally pulled low.

Note 4:Global reset pin. It should be connected to VCC in normal operation. If Connected to GND, the controller is in reset state, normally pulled high.

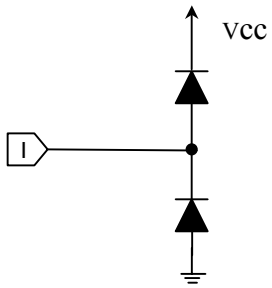
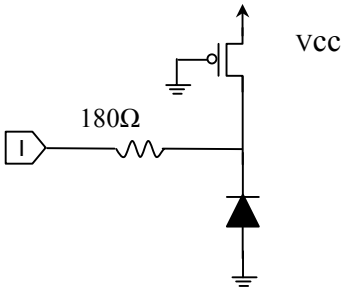
Note 5 : Definition of scanning direction. Refer to figure as below:



b. LED driving section

No.	Symbol	I/O	Description	Remark
Pin14	VLED	I	LED Anode	
Pin 15	GLED	-	LED Cathode	

2. Equivalent circuit of I/O

Pin no & Pin name	Schematics
7.DRV	
8.FB 9 SHL 10.STB 12.SHDB 17.HSYNC 18.VSYNC 19.DCLK 20.D07 21.D06 22.D05 23.D04 24.D03 25.D02 26.GRB 27.U/D	

3. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V_{CC}	GND=0	-0.5	5.	V	
	AV_{DD}	AV_{SS}=0	-0.5	5.5	V	
	V_{GH}	GND=0	-0.3	21	V	
	V_{GL}		-17	0.3	V	
	$V_{GH}-V_{GL}$		-	38	V	
Input signal voltage	VCOM		-2.9	5.2	V	
Operating temperature	Topa		0	60	℃	Ambient temperature
Storage temperature	Tstg		-25	80	℃	Ambient temperature

4. Electrical characteristics

a. Typical operating conditions (GND=AVss=0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
	V_{CC}	2.5	3.3	3.6	V	

		AV_{DD}	3.2	3.3	4.5	V	
		V_{GH}	15.8	17.8	19.5	V	
		$V_{GL\ AC}$	-	5.6	-	Vp-p	AC component of $V_{GL.}$ Note 1
		V_{GL_H}	-8.3	-7.3	-6.3	V	High level of $V_{GL.}$
VCOM		V_{CAC}	-	5.6	-	Vp-p	AC component, Note 2
		V_{CDC}	-0.4	-0.1	0.2	V	DC component, Note 3 Note 4
Output Signal voltage	H Level	V_{OH}	Vcc-0.4				
	L Level	V_{OL}	GND		GND+0.4		
Input Signal voltage	H Level	V_{IH}	$0.7V_{CC}$	-	V_{CC}	V	
	L Level	V_{IL}	GND	-	$0.3V_{CC}$	V	
DRV output voltage		V_{DRV}	0		VCC	V	For DC/DC circuits.
DRV output current		IDRV			10	mA	
Feedback voltage		V_{FB}		1.2	1.25	V	
Output current	H Level	IOH		10		uA	
	L Level	IOL		-10		uA	
Analog stand by		Ist			200	uA	DCLK is stopped
FRP output current	H Level	I_{OHF}			20	mA	For Vcom circuits.
	L Level	I_{OLF}			20	mA	

Note 1: The same phase and amplitude with common electrode driving signal (VCOM).
Note 2: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.
Note 3: V_{CDC} could be adjusted so as to minimize vertical straight line, flicker and maximum contrast on each module.
Note 4: Be sure to apply GND, V_{CC} and V_{GL} (V_{GL} must lower than 0 volt) to the LCD first, and then apply V_{GH}.
Note 5: The applicable pins are SHL,STB,SHDB,HSYNC,VSYNC,DCLK,D05~D00,GRB,U/D

b. Current consumption (GND=AVss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Current for driver	I_{GH}	V_{GH}=17V	-	0.13	0.8	mA	
	I_{GL}	V_{GL_H}=-8V	-	-0.19	-1	mA	
	I_{CC}	V_{CC}=3.3V	-	2	4	mA	
	I_{DD}	AV_{DD}=3.3V	-	1.15	2	mA	

c. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current		**19**	20	**21**	**mA**	
LED voltage	V_L			***8***	***V***	
LED Life Time	L_L	10000			Hr	Note 1,2

Note 1 : Ta. = 25℃, I_L = 20mA

Note 2 : Brightness to be decreased to 50% of the initial value.

5. AC Timing

a. Timing conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK	Frequency	1/Tvc		24.54		MHz	
	High time	Tvch	15			ns	
	Low time	Tvcl	15			ns	
Rising time		t_r	-	-	10	ns	Note 1
Falling time		t_f	-	-	10	ns	Note 1
HSYNC	Period	TH	60	63.56	67	us	Note 2
				1560		DCLK	
	Display period	THd		49.4		us	
	Pulse width	THp	1	25		DCLK	
	HSYNC-Clk timing	THc	15		Tc-15	ns	
Hsync setup time		Tvst	12			ns	
Hsync hold time		Thhd	12			ns	
Horizontal lines per field		t_V	256	262	268	t_H	
VSYNC	Period	TV		16.6		ms	Note 2
				262		t_H	
	Display period	TVd		13.97		ms	
	Pulse width	TVp	1			DCLK	
				3		TH	
Vsync setup time		Tvst	12			ns	
Vsync hold time		Tvhd	12			ns	
DATA D00~D05	DCLK-DATA timing	Tds	10	-	-	ns	
	DATA-CLK timing	Tdh	10	-	-	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	
Data set-up time		Tds	12			ns	
Data hold time		Tdh	12			ns	

Note 1: For all of the logic signals.

Note 2: Display position

A.. Horizontal display position

The display starts from the data of (269DCLK, THe=268DCLK) as shown in Fig 4.

(THe : From Hsync falling edge to 1st displayed data.)

B. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		25		TH	NTSC

b. Timing diagram

Please refer to the attached drawing, from Fig.2 to Fig.5.

6. DC-DC Converter Circuit

A015AN02 contains one high-power step-up DC-DC converter, and backplane drive circuitry for active matrix TFT LCDs. The output voltage of the main boost converter can be set from VCC to 13.5V with external resistors. Also included in A015AN02 are a precision 1.2V reference voltage, fault detection and logic shutdown.

a .Boost Converter

A015AN02 main boost converter uses a boost PWM architecture to produce a positive regulated voltage, Please refer to the below figures to see the block diagram.

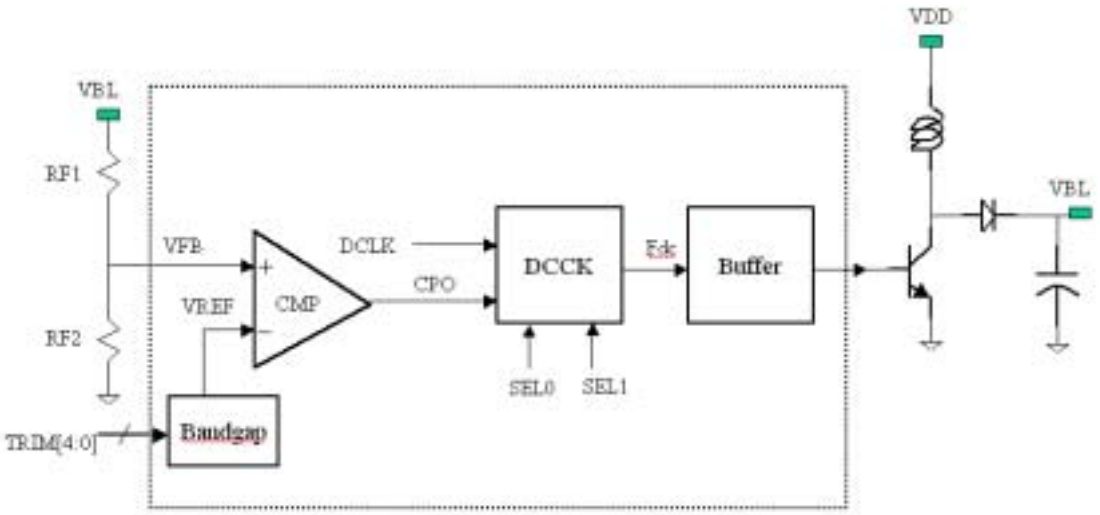


Fig 1 Dc-Dc converter block diagram

In the internal architecture of DC-DC converter. The feedback voltage(VFB) will connect to the tri-angle waveform comparator ,and generates the output signal (CP0) which determines the duty cycle for (Fdc).

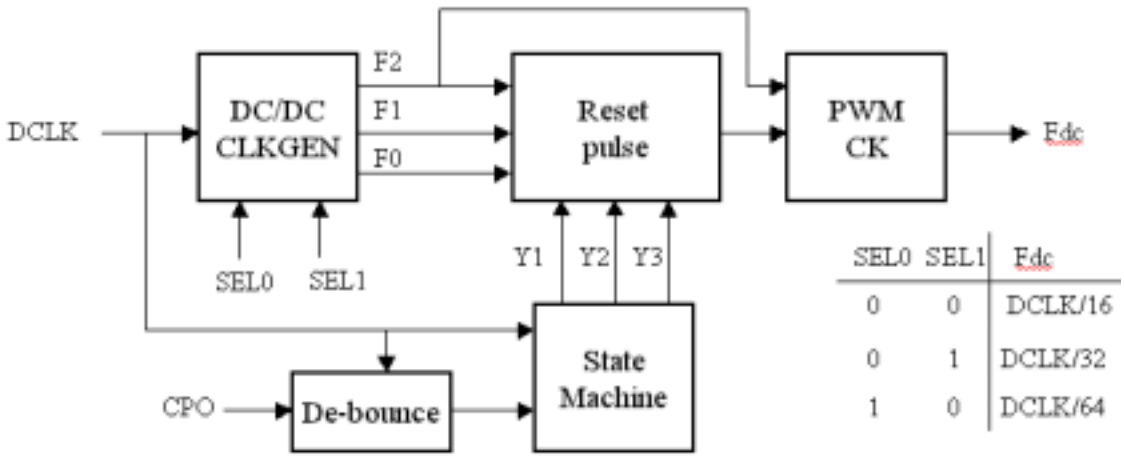


Fig 2 DCCK block diagram

To reduce the noise affect,CP0 will processed by De-bounce circuit. State-machine will generate the duty cycle by CP0 signal. To make sure that VFB can reach default VREF quickly, so State-machine's is designed as a discrete step by step function. please refer to Fig 3. If CP0 is low , Duty cycle will work from 0% to 75%. The maximum duty ratio is 75%.

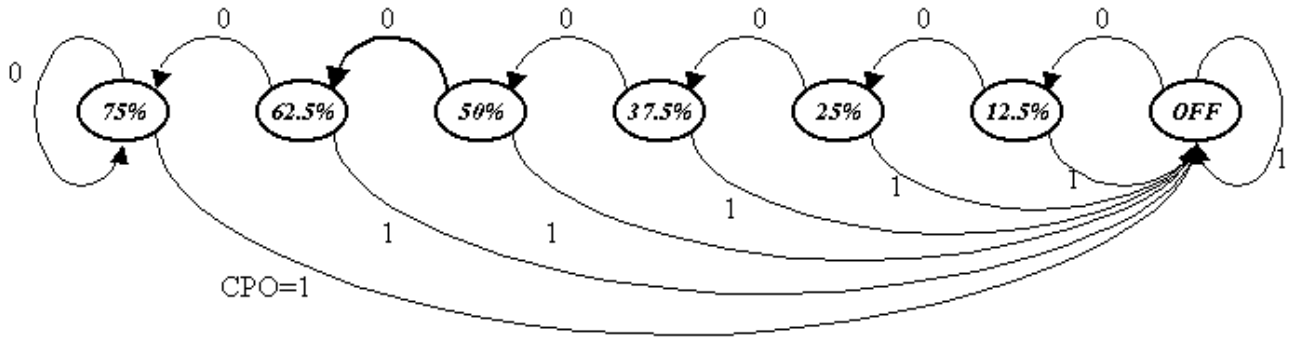


Fig 3 PWM Control state diagram

b.Shutdown Mode

In shutdown mode, a logic-low level on SHDB, pwm controller and the reference are disabled. The supply current drops to maximize battery life and the reference is pulled to ground. Every output voltage will decay. If unused, connect SHDB to VCC.

c.Oscillator Circuit

The boost-converter operating frequency can be set at 1/16,1/32,1/64 times the system clock, DCLK. In A015AN02's model. the DC-DC converter osc frequency is DCLK/64=383.4khz

C. Optical specification (Note 1,Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time Rise Fall	 Tr Tf	 θ =0°	 - -	 25 30	 50 60	 ms ms	Note 4
Contrast ratio	CR	At optimized viewing angle	60	150	-		Note 5,6
Viewing angle Top Bottom Left Right		CR≧10	 10 30 45 45	 - - - -	 - - - -	deg.	Note 7
Brightness	Y_L	θ =0°	*160*	200	-	cd/m^2	Note 8
White chromaticity	X	θ =0°	0.26	0.31	0.36		

	y	θ =0°	0.29	0.35	0.40		

Note 1. Ambient temperature =25℃. And backlight current I_L=20 mA

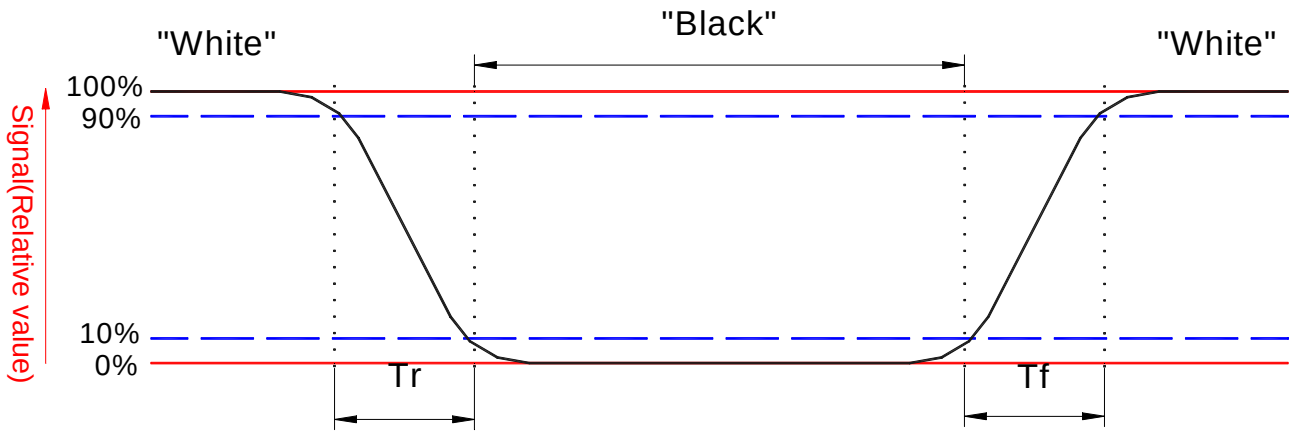
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. White Vi=V_{i50} $\mp$ 1.5V

Black Vi=V_{i50} ± 2.0V

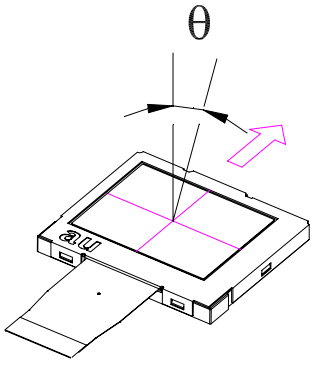
“±” Means that the analog input signal swings in phase with COM signal.

“$\mp$” Means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:



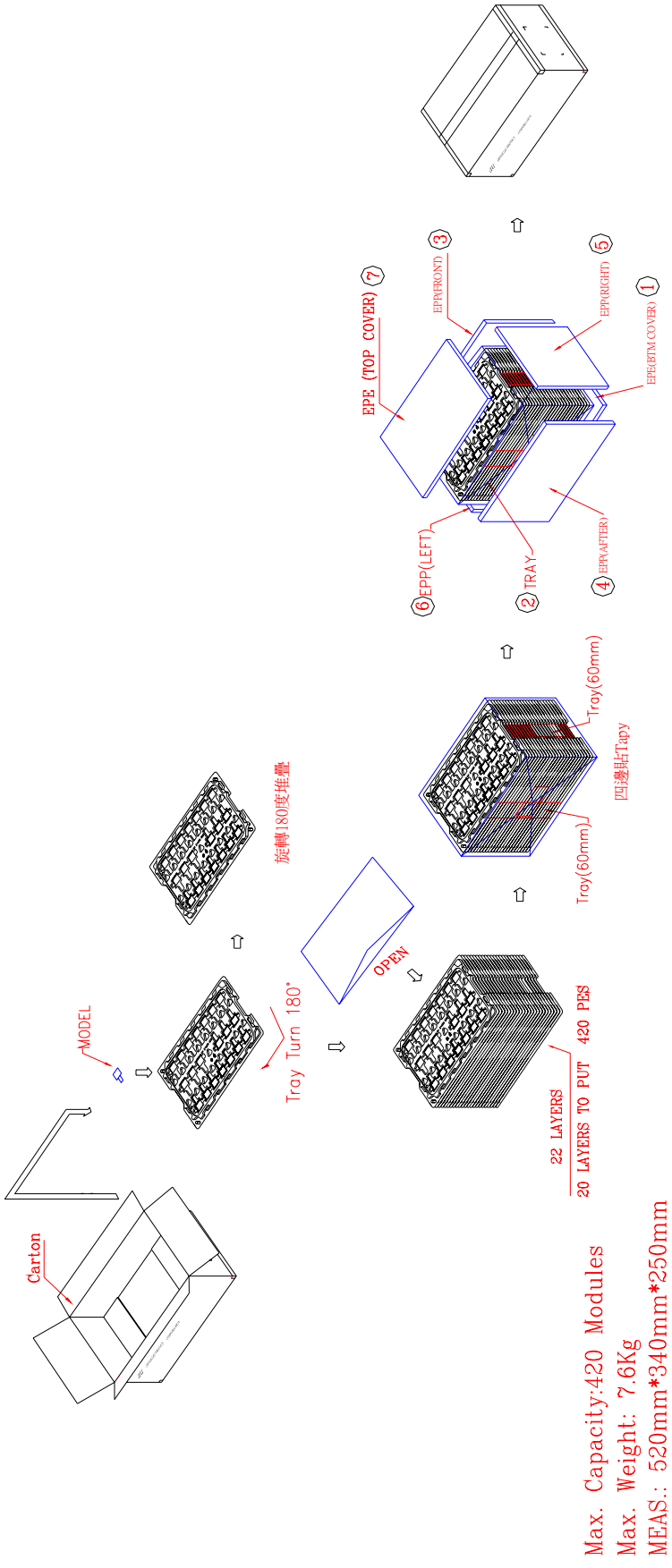
Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

D. Reliability test items:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80℃ 240Hrs	
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	
12	The copper's strength for FPC	The strength is larger 0.7 kg/cm	IPC TM650
13	The film's strength for FPC	The strength is larger 0.35 kg/cm	IPC TM650
14	Flexible ability for FPC	1. curved radius: 2mm 2. curved angle: 270° 3. Pulling force: 500g	MIT folm: Diagram of test set up for folding endurance

Note: Ta: Ambient temperature.

E. Packing form



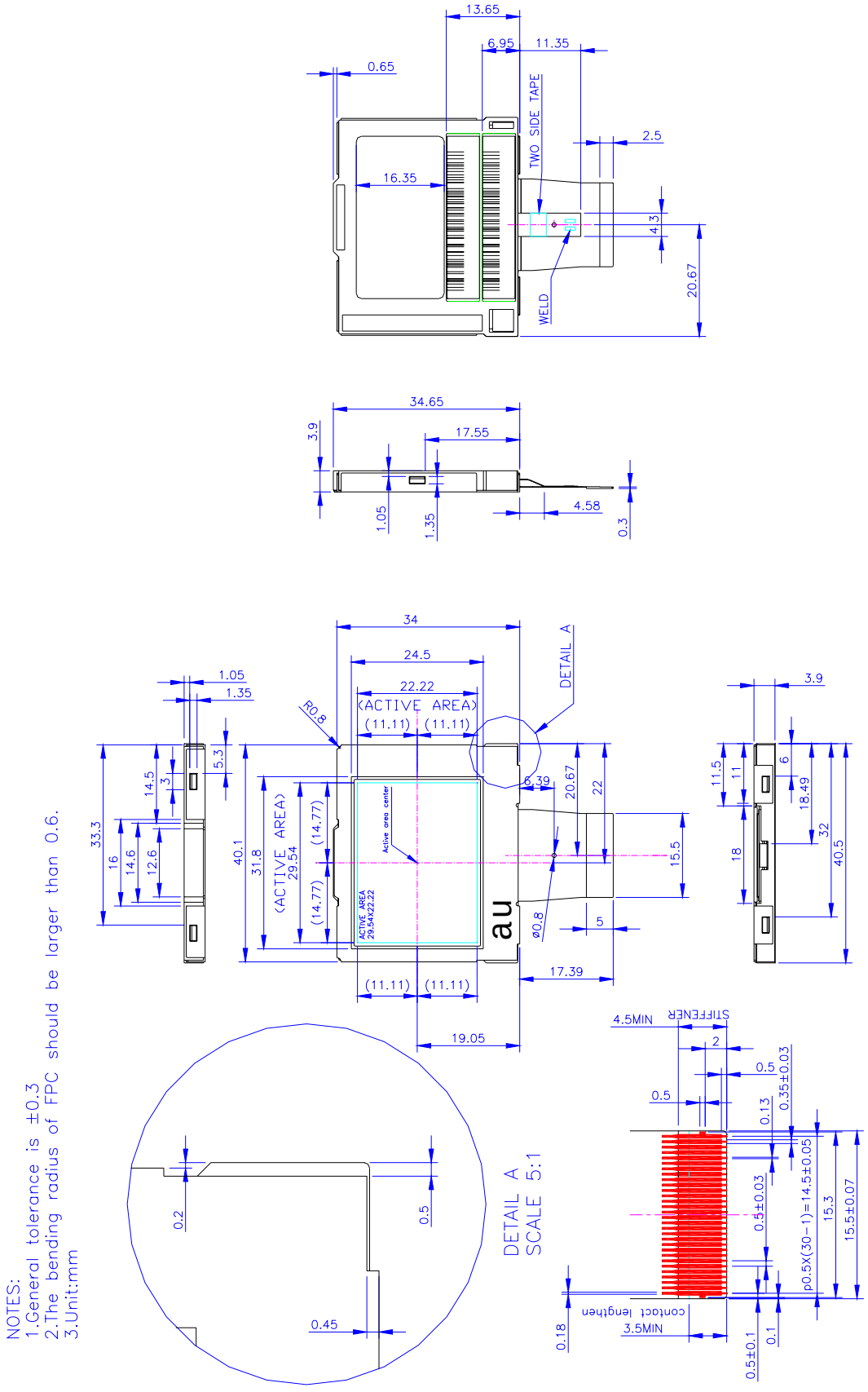


Fig.4 Outline dimension of TFT-LCD module

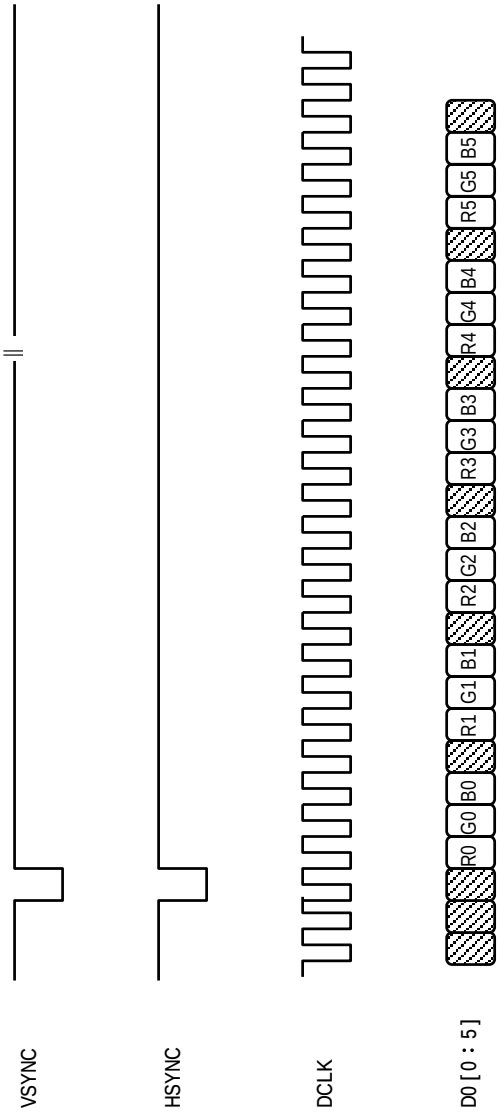


Fig.5 Input signals timing relationship

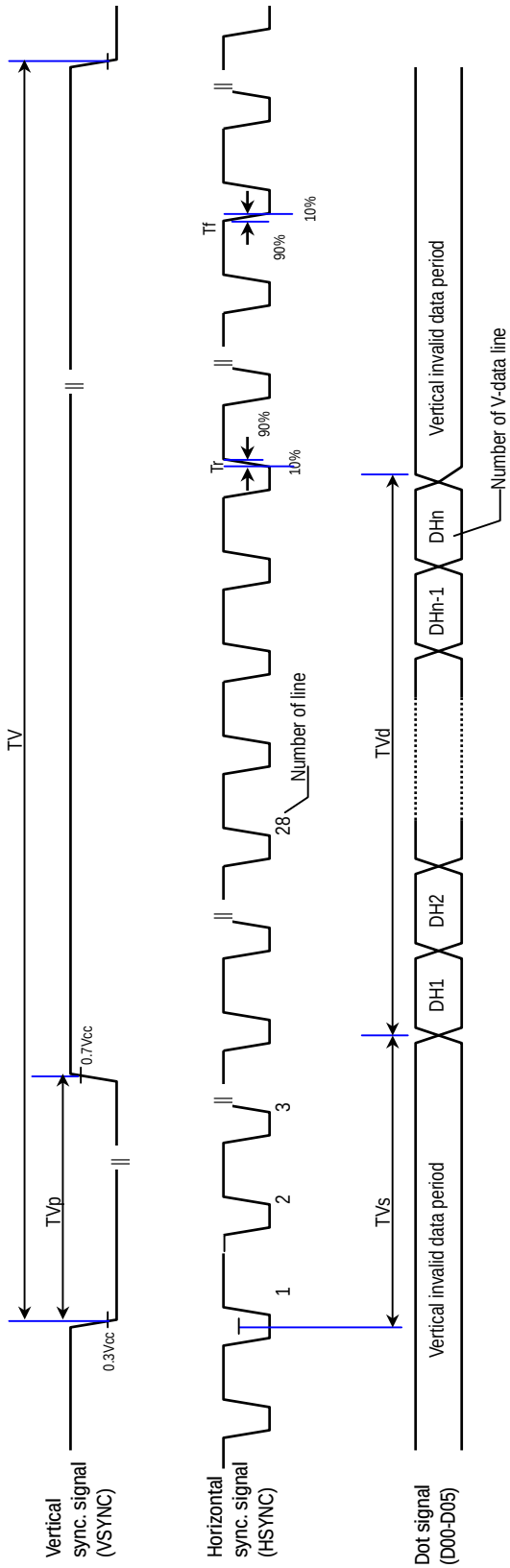


Fig 6 Input Vertical Timing

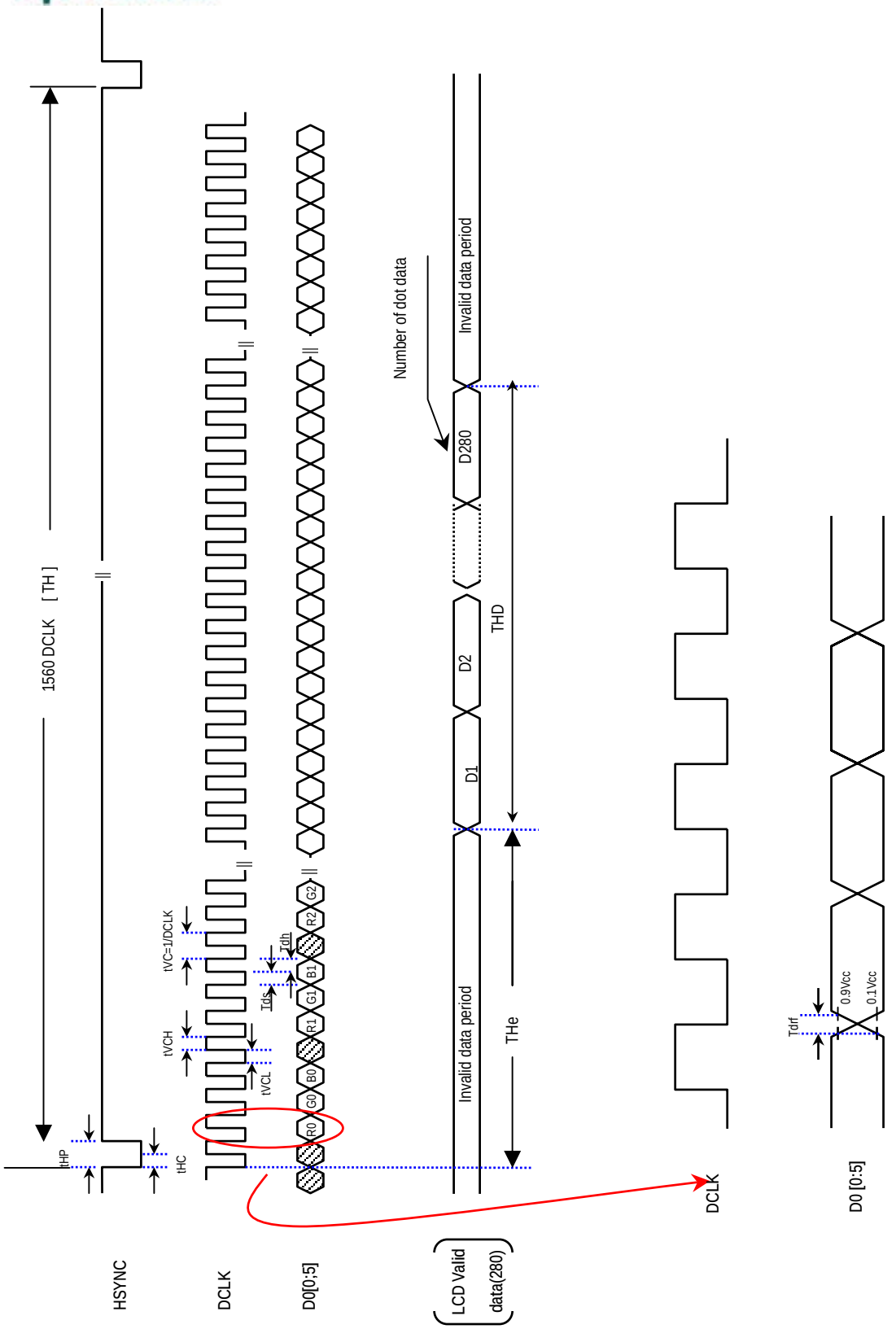


Fig.7 Horizontal Input Timing)

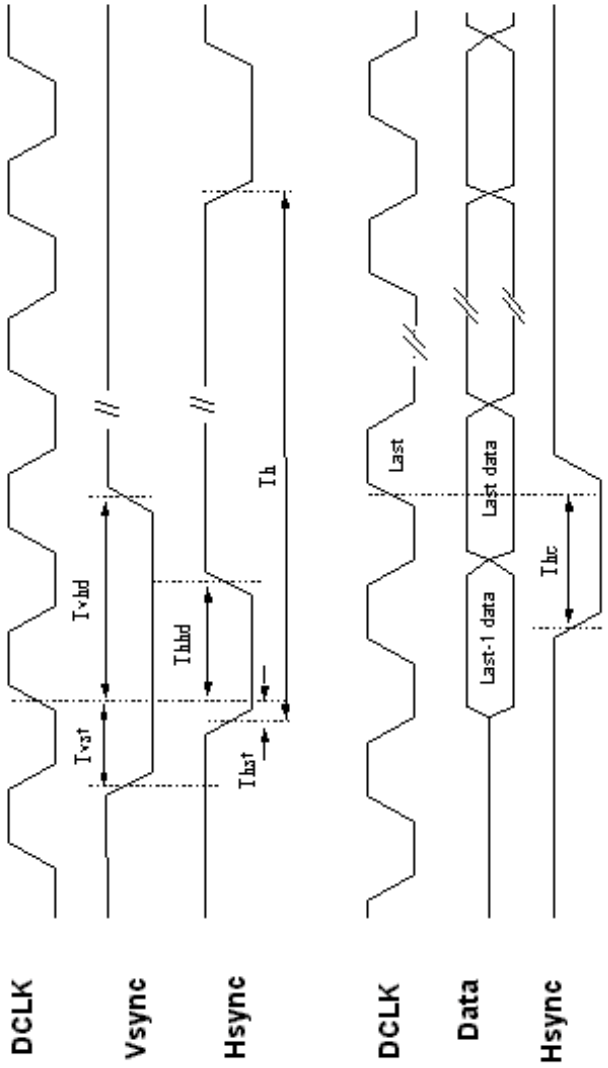


Fig.8 Hsync,Vsync,Data,DCLk relationship

Reference:

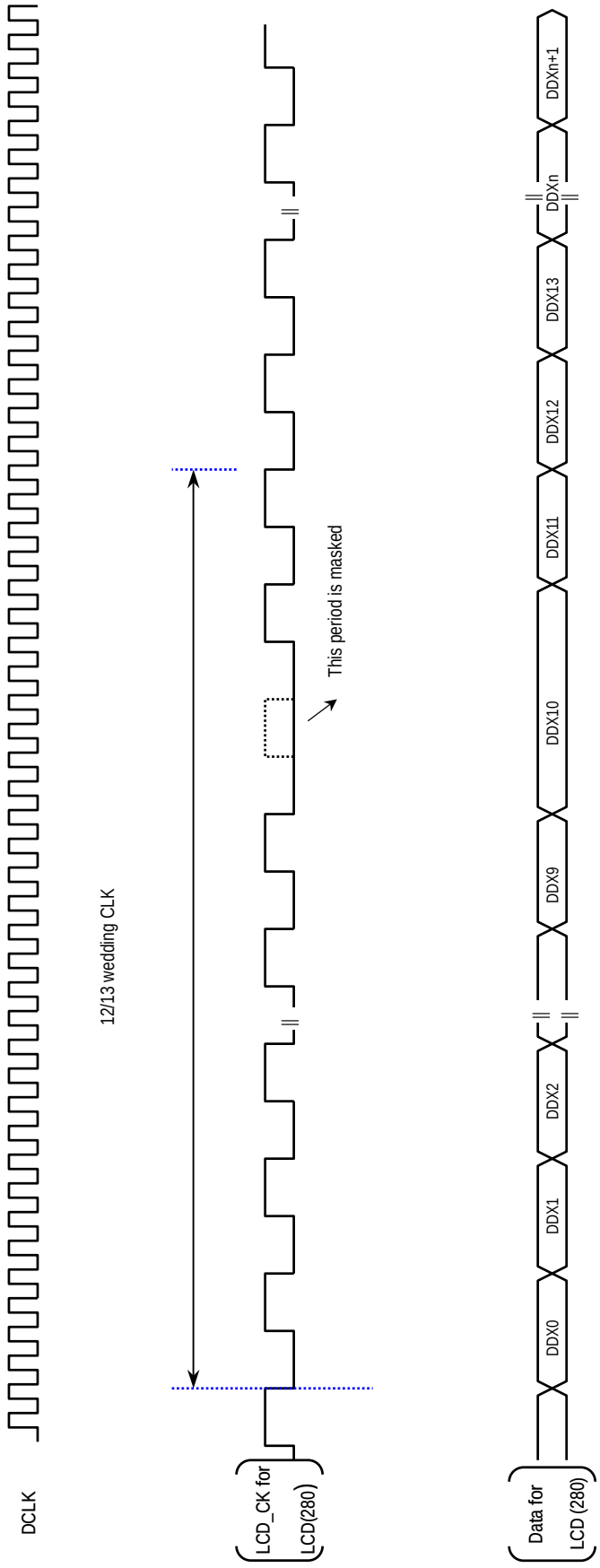


Fig.9 Horizontal Input Timing (Wedding CLK Explanation)

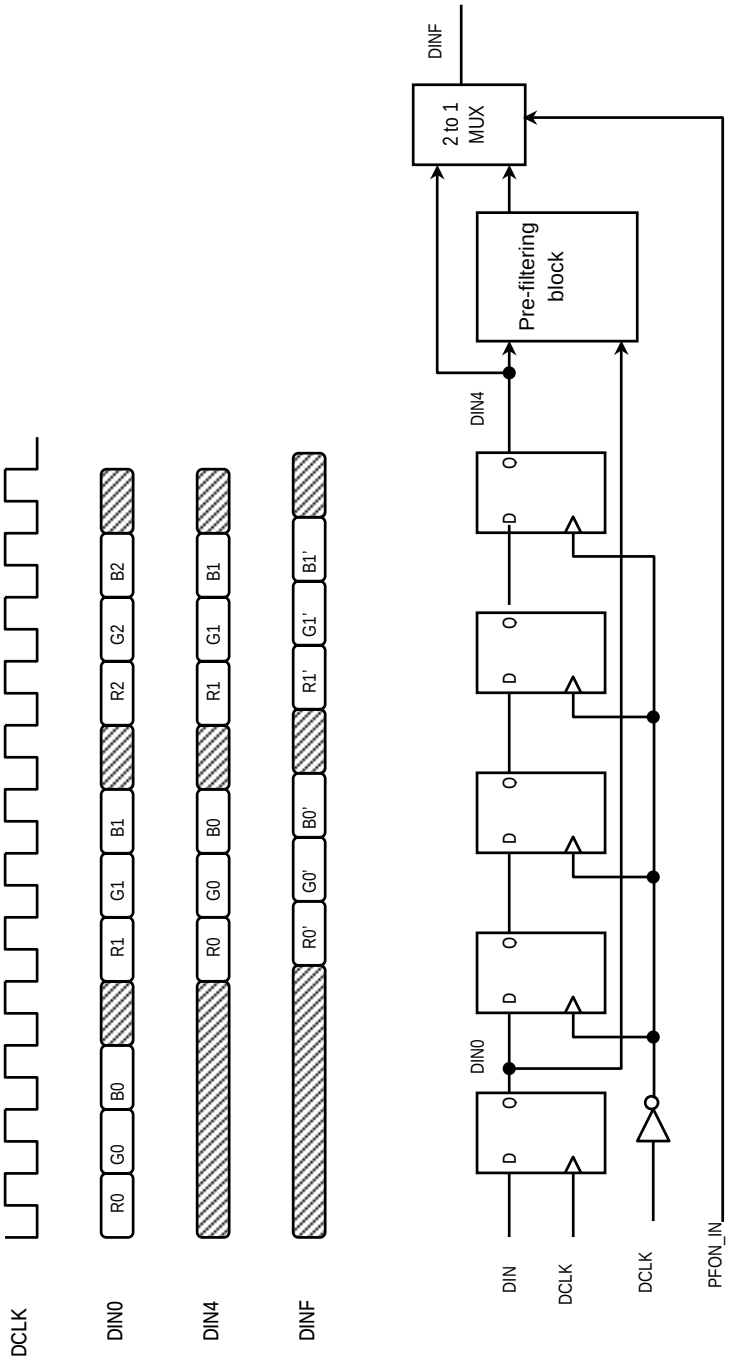


Fig.10 Pre-filtering function timing diagram and block diagram

Application Circuit

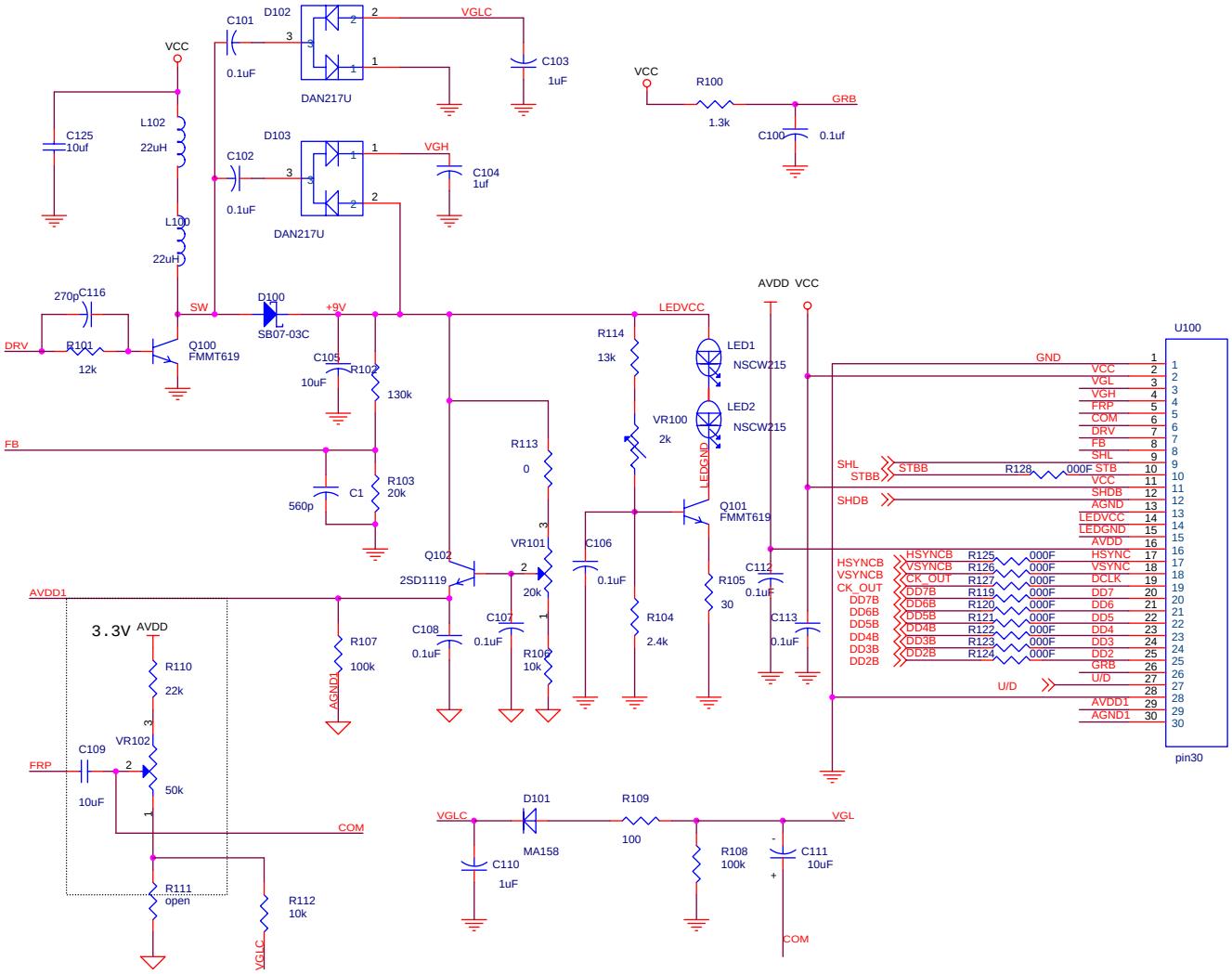


Fig 11 Typical application circuit (for reference)