Doc. Number:

□ Tentative Specification
■ Preliminary Specification
□ Approval Specification

Bozhe technology(HK) Limited

MODEL NO: BZ101IICD1S

Customer:

APPROVED BY **SIGNATURE**

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
1.0	August, 7, 2020	All	Spec Ver.1.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

BZ101IICD1S is a 10.1” (10.1” diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 39 pins MIPI interface.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	10.1 diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	800 x R.G.B. x 1280	pixel	-
Pixel Pitch	0.0564 (H) x 0.1692 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	8bit color depth	color	-
Transmissive Mode	Normally black	-	-
Surface Treatment	HC-Glare	-	-
Luminance, White	350	Cd/m2	
Power Consumption	Total (2.3 W) (Max.) @ cell (0.3 W) (Max.) BL (2.0 W) (Max.)		(1)

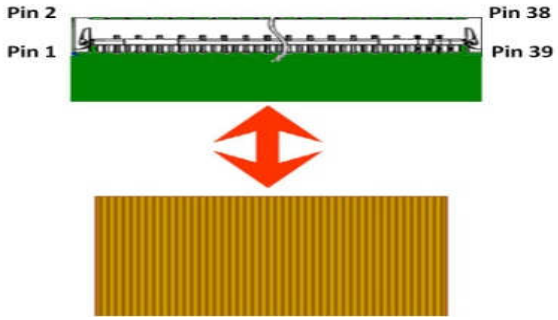
Note (1) The specified power consumption (with converter efficiency) is under the conditions at VDDI = 1.8 V, VCI= 3.3V ,fv = 60 Hz, Brightness = 350nits, I_{F_LED} = (21mA) and Ta = 25 ± 2 ºC, whereas white pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	142.1	142.3	142.5	mm	(1)
	Vertical (V)	228.3	228.5	228.7	mm	
	Thickness (T)	-	2.5(w/o PCBA) (w/ PCBA)	2.65 4.45	mm	
Active Area	Horizontal	135.26	135.36	135.46	mm	
	Vertical	216.48	216.58	216.68	mm	
Weight		-	-	146	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: HIROSE FH26W-39S-0.3SHW(60)

3. ABSOLUTE MAXIMUM RATINGS

3.1 ELECTRICAL ABSOLUTE RATINGS

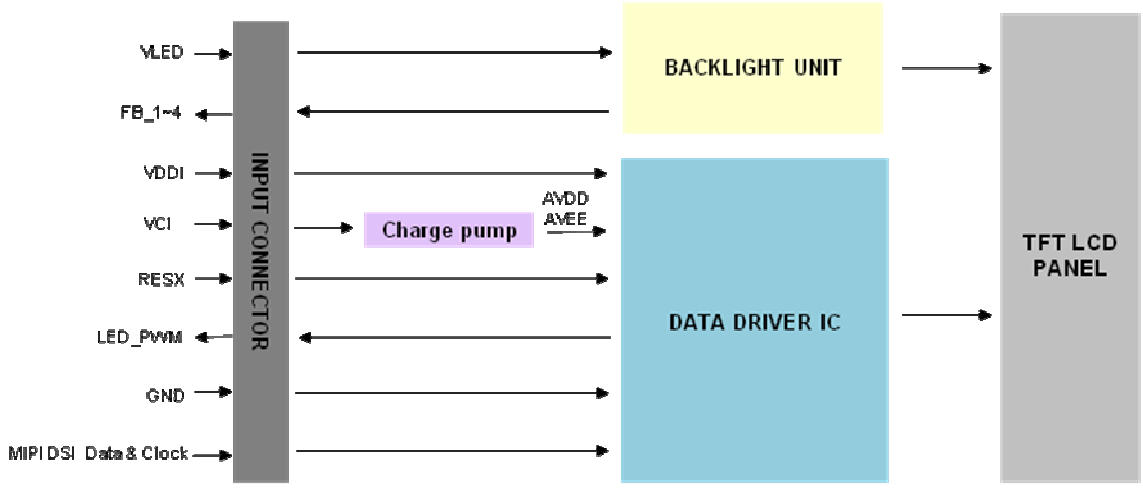
TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VDDI	-0.3	+3.6	V	(1)
	VCI	-0.3	+6.6	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	I/O	Description
1	NC	-	For INX internal use(7.5V for MTP)
2	NC	-	No Connection
3	NC	-	No Connection
4	LED4-	P	Power for LED4 Cathode
5	LED3-	P	Power for LED3 Cathode
6	LED2-	P	Power for LED2 Cathode
7	LED1-	P	Power for LED1 Cathode
8	NC	-	No Connection
9	LED+	P	Power for LED Anode
10	LED+	P	Power for LED Anode
11	LED+	P	Power for LED Anode
12	NC	-	No Connection
13	NC	-	No Connection
14	LEDPWM_OUT	O	Output pin for PWM (Pulse Width Modulation) signal of LED driving
15	ID1	O	Hardware ID Select(Setting “L" ((0 V))
16	RESX	I	This signal will reset the device and must be applied properly to initialize the chip.

17	ID2	O	Hardware ID Select(Setting “H" (3.3 V))
18	TE	O	Vsync signal
19	VCI	P	3.3V for analog circuit blocks
20	VCI	P	3.3V for analog circuit blocks
21	VCI	P	3.3V for analog circuit blocks
22	VDDI	P	1.8V for logic circuit blocks
23	VDDI	P	1.8V for logic circuit blocks
24	GND	P	Ground
25	D3+	I	MIPI differential data3 input (Positive)
26	D3-	I	MIPI differential data3 input (Negative)
27	GND	P	Ground
28	D2+	I	MIPI differential data2 input (Positive)
29	D2-	I	MIPI differential data2 input (Negative)
30	GND	P	Ground
31	CLK+	I	MIPI differential clock input (Positive)
32	CLK-	I	MIPI differential clock input (Negative)
33	GND	P	Ground
34	D1+	I	MIPI differential data1 input (Positive)
35	D1-	I	MIPI differential data1 input (Negative)
36	GND	P	Ground
37	D0+	I	MIPI differential data0 input (Positive)
38	D0-	I	MIPI differential data0 input (Negative)
39	GND	P	Ground

Note (1) The first pixel is odd as shown in the following figure.

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

Parameter	Symbol	Values			Units	Notes
		Min	Typ	Max		
Logic Operating Voltage	VDDI	1.7	1.8	1.9	V	
Analog Positive Voltage	VCI	3.1	3.3	3.5	V	
LED Input Current	I_{LED}	-	21		mA	
“H” Level Input Voltage	V_{IH}	0.7x VDDI	-	VDDI	V	

"L" Level Input Voltage		V_{IL}	0.0	-	0.3x VDDI	V	
"H" Level Output Voltage		V_{OH}	0.8x VDDI	-	VDDI	V	
"L" Level Output Voltage		V_{OL}	0.0	-	0.2x VDDI	V	
Input high level leakage current		I_{IH}	-	-	1	μA	
Input low level leakage current		I_{IL}	-1	-	-	μA	
LCD Operating Current	Normal	I_{VDDI}	-	-	35	mA	(1)
		I_{VCL}	-	-	70		
	Sleep	I_{VDDI}	-	-	60	uA	
		I_{VCL}	-	-	100		

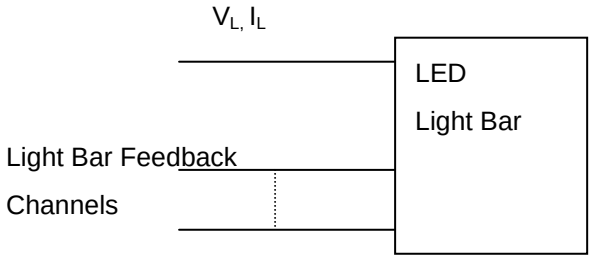
Note (1) The specified power supply current is under the conditions at VCI =3.3 V, VDDI=1.8 V, Ta = 25 ± 2°C, DC current and fv = 60 Hz, whereas a white pattern under 800x1280 60Hz is displayed.

4.3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	19.11	21.56	22.61	V	(1)(2) (Duty100%)
LED Light Bar Power Supply Current	I_L	83.2	84	84.4	mA	
Power Consumption	P_L			2 (L/B)	W	(3)
LED Life Time	L_{BL}	15000			Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :

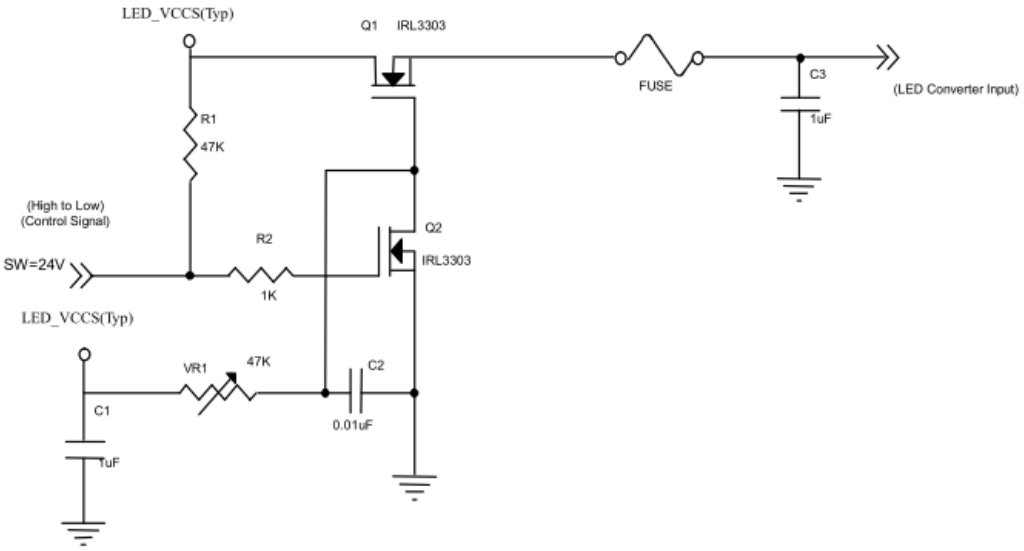


Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

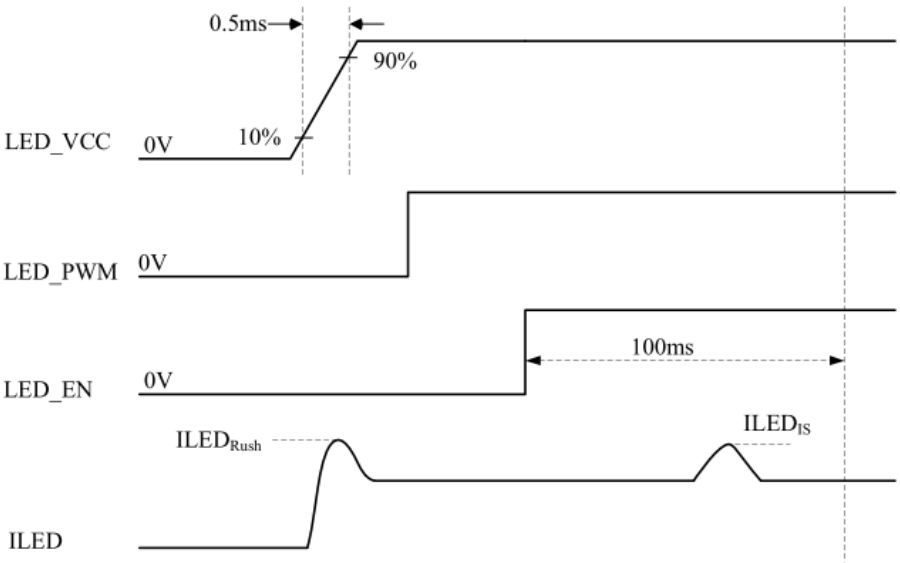
Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 ^{o}C and IL = 20 mA(Per EA) until the brightness becomes ≦ 50% of its original value.

Note (5) ILED RUSH : the maximum current when LED_VCCS is rising, ILED IS : the maximum current of the first 100ms after power-on, Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta =25 ± 2 ºC, Duty = 100%.



VLED rising time is 0.5ms

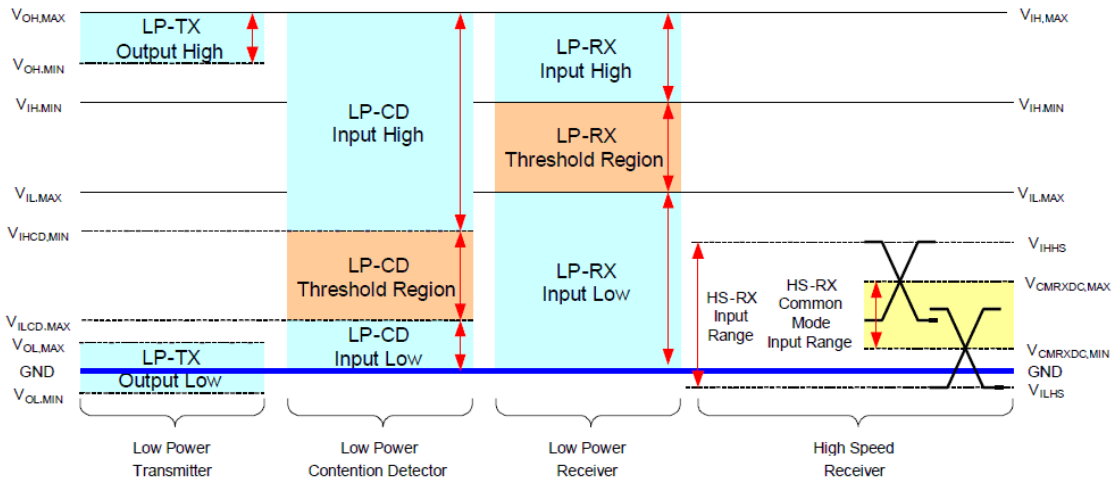


Note (6) If the PWM control duty ratio is less than 10%, that is difficult to control the brightness linearity.

Note (7) If PWM control frequency is less than 1KHz, the “waterfall” phenomenon on the screen may be found. To avoid the issue, it’s a suggestion that PWM control frequency should greater than 1KHz.

Note (8) The specified LED power supply current is under the conditions at “LED_VCCS = Typ.”, Ta = 25 ± 2 ºC, Duty=100%.

4.4 DISPLAY PORT INPUT SIGNAL DC SPECIFICATIONS



4.4.1 DC Electrical Characteristic

- **DC Characteristics for DSI LP Mode**

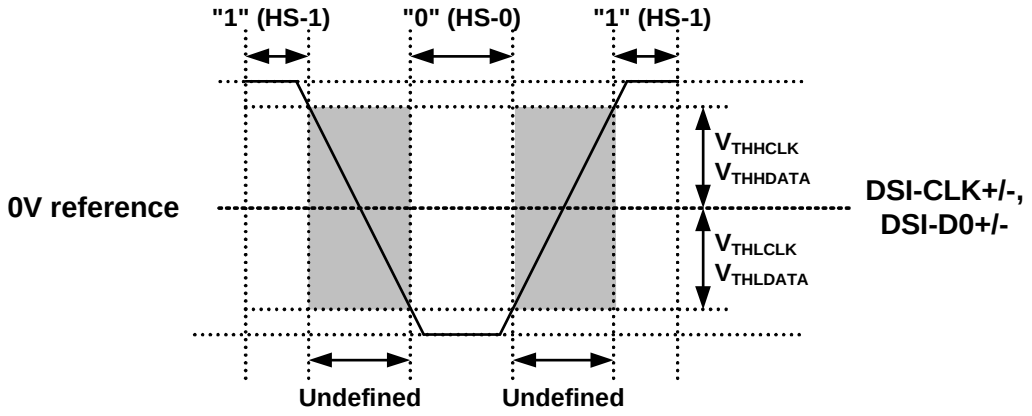
Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

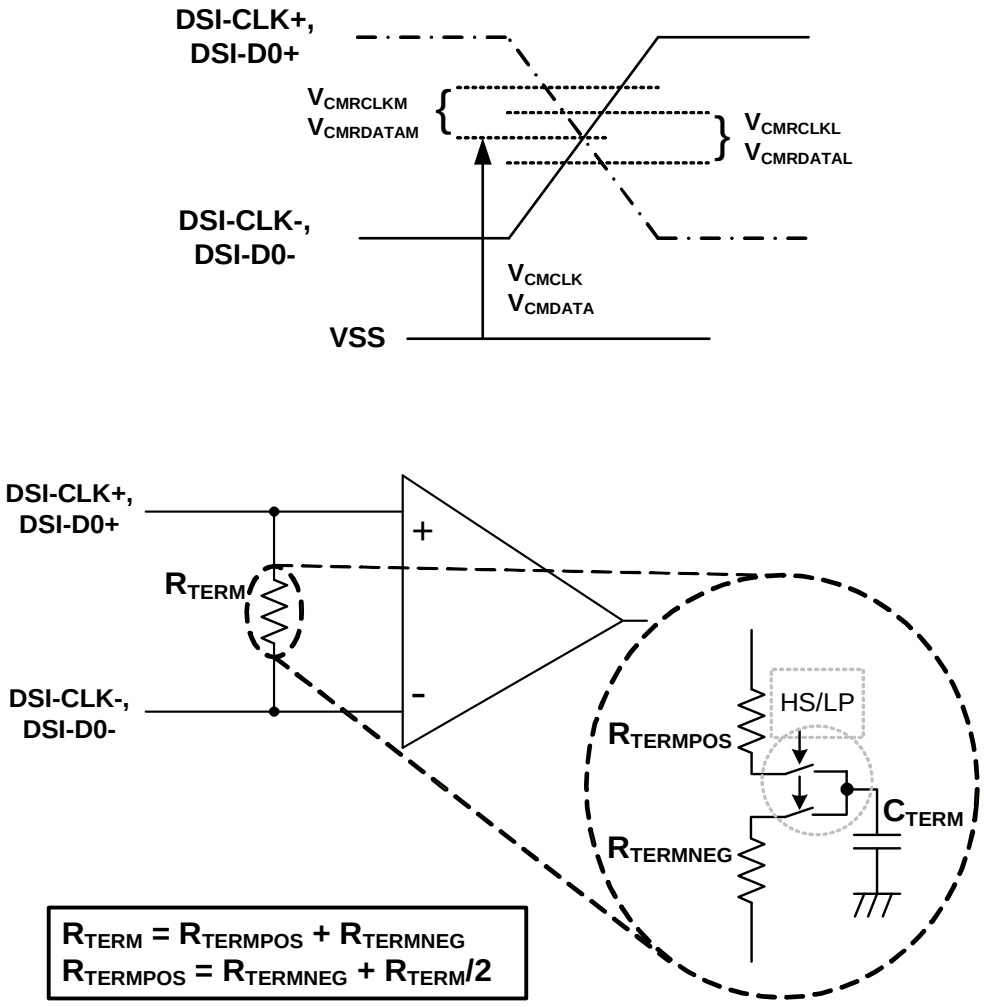
Note 1) VDDI= 1.8 V, VCI = 3.3 V, GND=0V, Ta=-30 to 70 ° C(to +85 ºC no damage)
Note 2) DSI high speed is off.
Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

- **DC Characteristics for DSI HS Mode**

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/-	-	-	60	pF

Note 1) VDDI= 1.8 V, VCI = 3.3 V, GND=0V, Ta=-30 to 70° C
Note 2) Includes 50mV (-50mV to 50mV) ground difference.
Note 3) Without VCMRCLKM450 / VCMRDATAM450 .
Note 4) Without 50mV (-50mV to 50mV) ground difference.
Note 5) Dn=D0, D1, D2 and D3.
Note 6) For higher bit rates, a 14pF capacitor will be needed to meet the common-mode return loss specification.





Differential voltage range, termination resistor and Common mode voltage

4.4.2 AC Electrical Characteristic

- **MIPI DSI Timing Characteristics**

  High Speed Mode

(VDDI= 1.8 V, VCI = 3.3 V, GND=0V, Ta=-30 to 70°C)

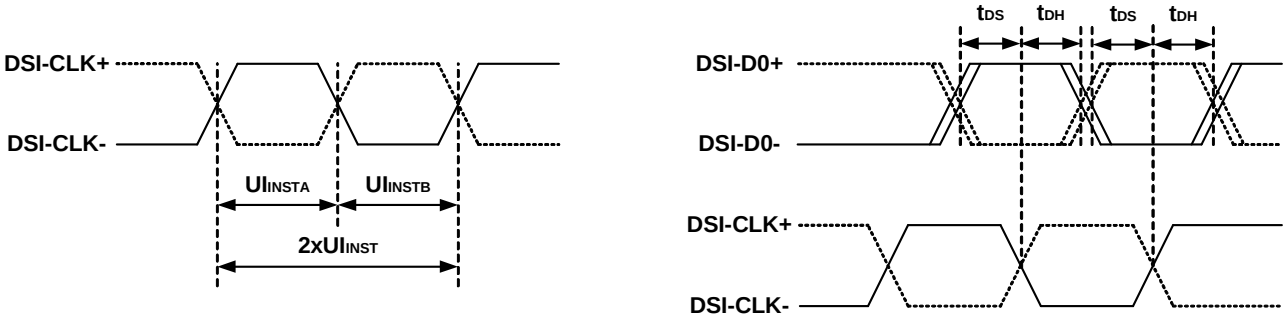
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	Note2	-	25	ns	4 Lane (Note 2)
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs ($UI = UI_{INSTA} = UI_{INSTB}$)	Note2	-	12.5	ns	4 Lane (Note 2)
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15xUI	-	-	ps	

DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3xUI	ps	

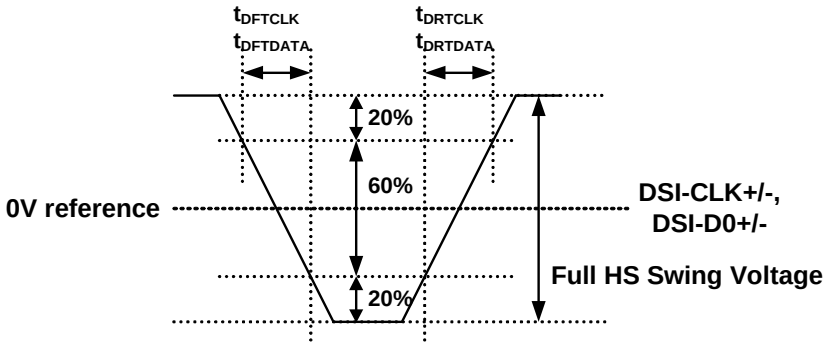
Note 1) UI=UIInsta=UIInstb.

Note 2) Define the minimun vallue, see Table :Limited Clock Channel Speed.

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 001110(0Eh),RGB 565, 16 UI per Pixel	566Mbps	466Mbps	366Mbps
Data Type = 011110(1Eh),RGB 666, 18 UI per Pixel	637Mbps	525Mbps	412Mbps
Data Type = 101110(2Eh),RGB 666 Loosely ,24 UI per Pixel	850Mbps	700Mbps	550Mbps
Data Type = 111110(3Eh),RGB 888 ,24 UI per Pixel	850Mbps	700Mbps	550Mbps



DSI clock channel timing

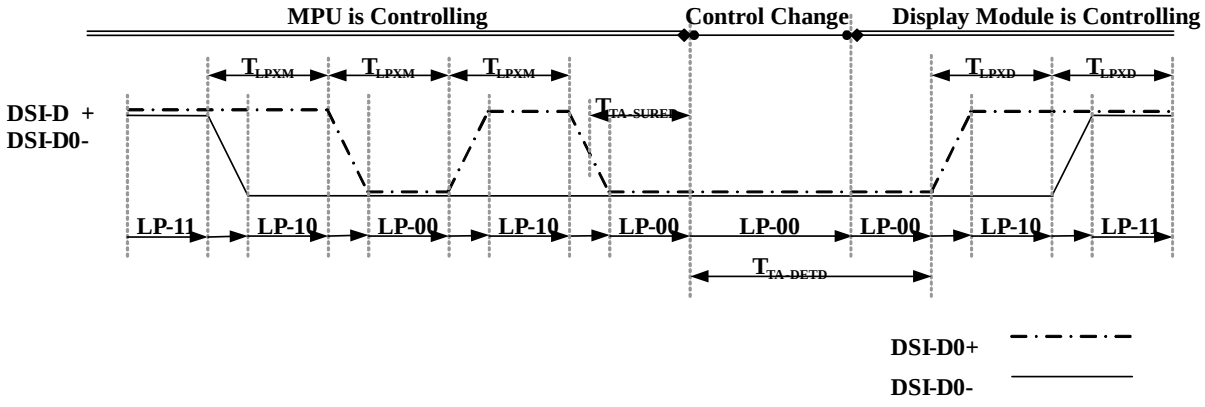


Rising and fall time on clock and data channel

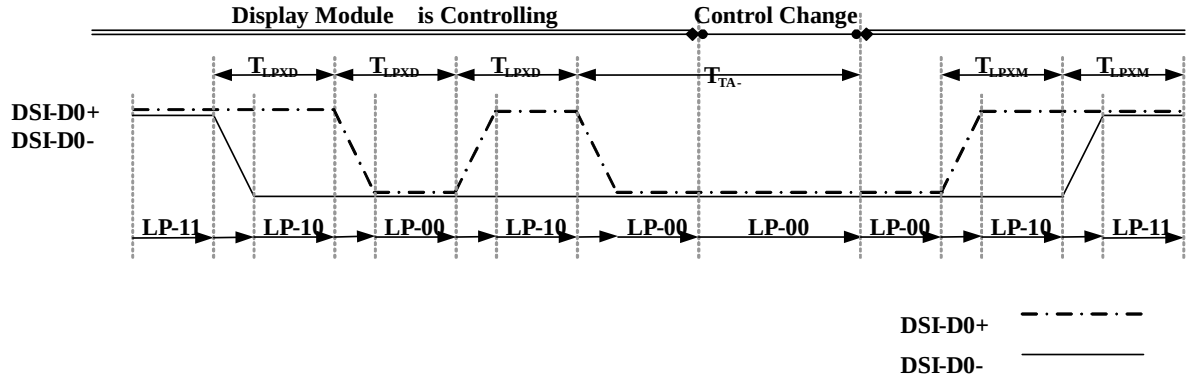
- **Low Power Mode**

(VDDI= 1.8 V, VCI = 3.3 V, GND=0V, Ta=-30 to 70˚C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5xT_{LPXD}$	-	-	ns	Input
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4xT_{LPXD}$	-	-	ns	Output



Bus Turnaround (BAT) from MPU to display module Timing



Bus Turnaround (BAT) from display module to MPU Timing

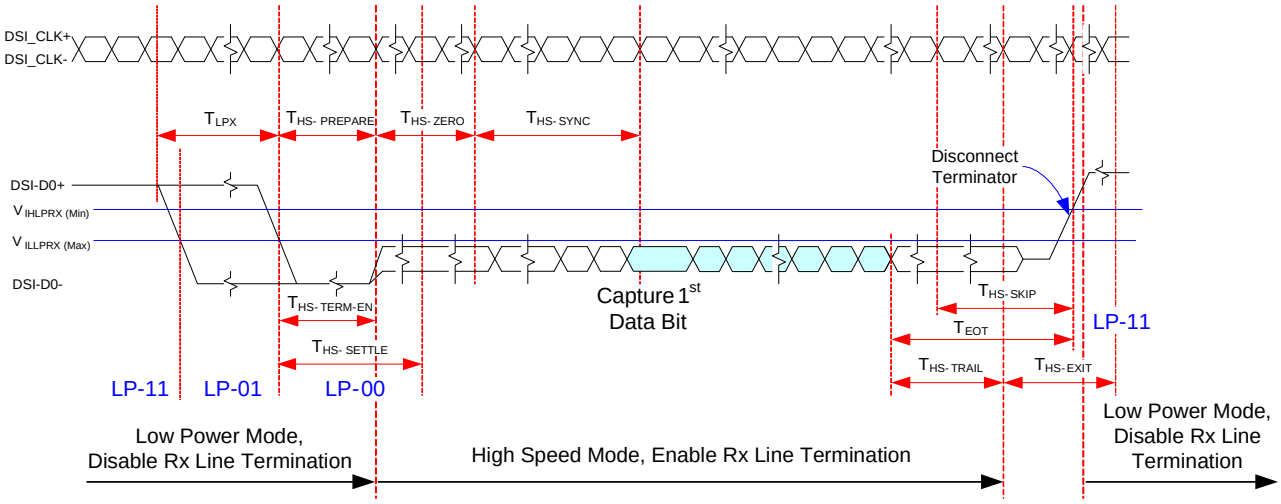
- **DSI Bursts**

(VDDI= 1.8 V, VCI = 3.3 V, GND=0V, Ta=-30 to 70°C)

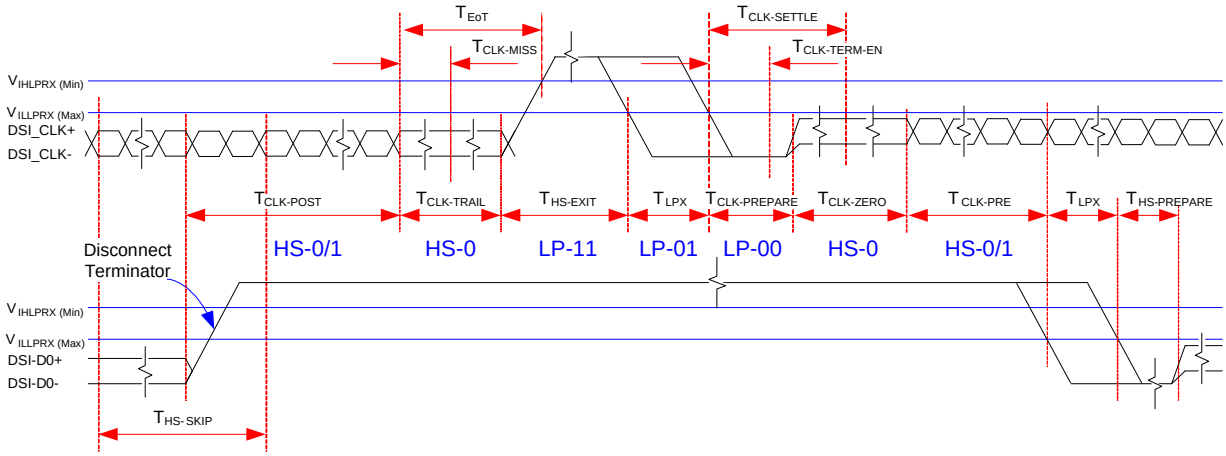
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	T_{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	$T_{HS-TERM-EN}$	Time to enable data receiver line termination measured from when Dn crosses V_{ILMAX}	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	Max(8*UI ,60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	$T_{CLK-POS}$	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$+ $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as THS-EXIT from each other in continuous clock mode. In discontinuous mode, the break is longer which account TCLK-POS , TCLK-TRAIL and THS-EXIT , before activity in clock and data lanes again.

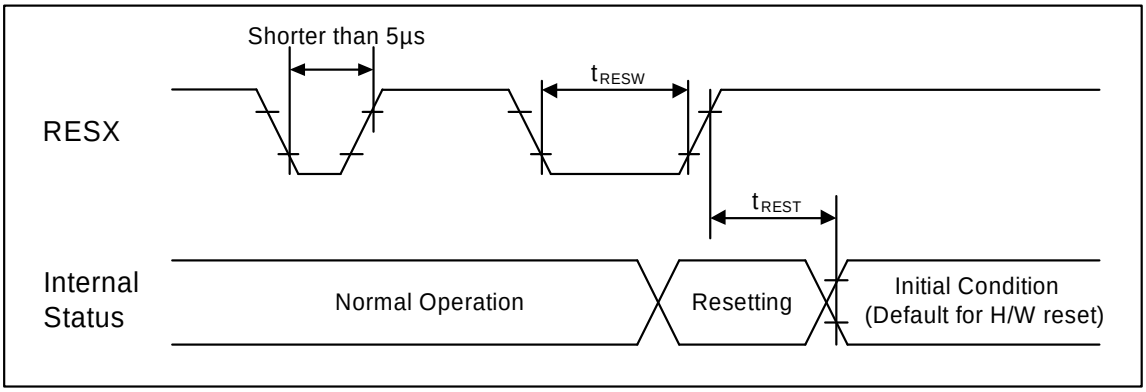


Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

- **Reset Input Timing**



Reset input timing

(VDDI= 1.8 V, VCI = 3.3 V, GND=0V, Ta=-30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit
RESX	t_{RESW}	Reset Pulse duration	10	-	-	µs
	t_{REST}	Reset complete time (Note 2)	-	-	5(note1,5)	ms
			-	-	120(note1,6,7)	ms

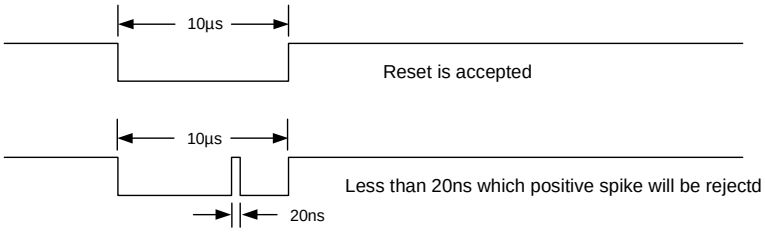
Note 1) The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPR-OM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2) Spike due to an electronstatic discharge on RESX line does not cause irregular system rest according to the Table.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

Note 3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) When Reset applied during Sleep In Mode.

Note 6) When Reset applied during Sleep Out Mode.

Note 7)It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

4.5 MIPI interface (Mobile Industry Processing Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode.

Note: The product only supports Video Mode operation.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

4.5.1 MIPI Lane Configuration

	MCU (Master) Display Module (Slave)
Clock Lane+/-	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane0+/-	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane1+/-	Unidirectional ■ Forward High speed
Data Lane2+/-	Unidirectional ■ Forward High speed
Data Lane3+/-	Unidirectional ■ Forward High speed

The connection between host device and display module is as reference.

Note: Usually, we suggest host can use non-continuous clock mode & non-burst mode with sync events to transmit the video stream to enhance ESD ability.

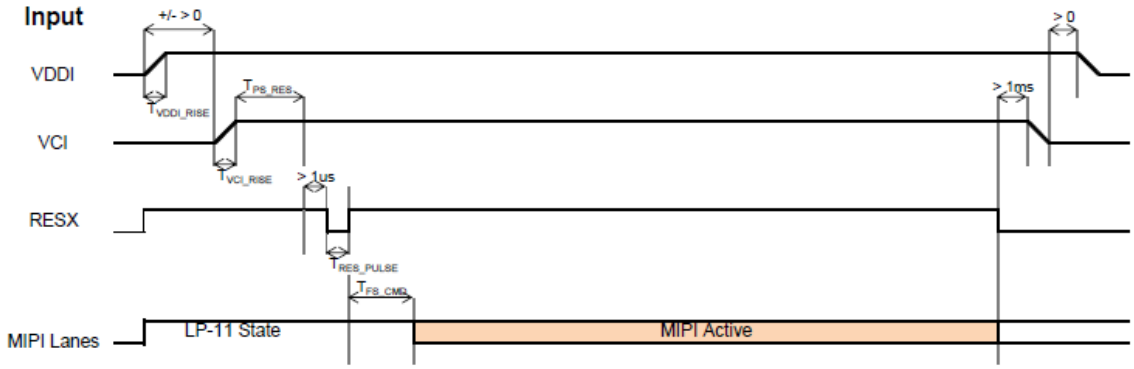
4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram**.**

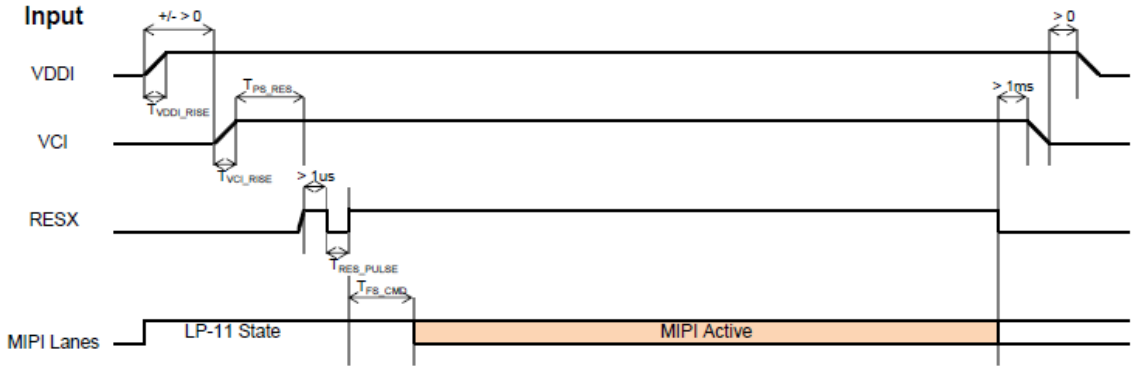
a. Power on Timing Sequence:

VDDI=VCCD=IOVCC=VCCH=1.8V, VCI=VCIP=3.3V

Case A:



Case B:



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

b. Power off Timing Sequence:

VDDI=VCCD=IOVCC=VCCH=1.8V, VCI=VCIP=3.3V

Uncontrolled Power Off

The uncontrolled power off means a situation when a battery is removed without the controlled power off sequence. There will not be any damages for the display module, or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, the ILI9881C will force the display to become blank and will not have any abnormal visible effects within 1 second on the display and remains blank until the Power On Sequence powers it up.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

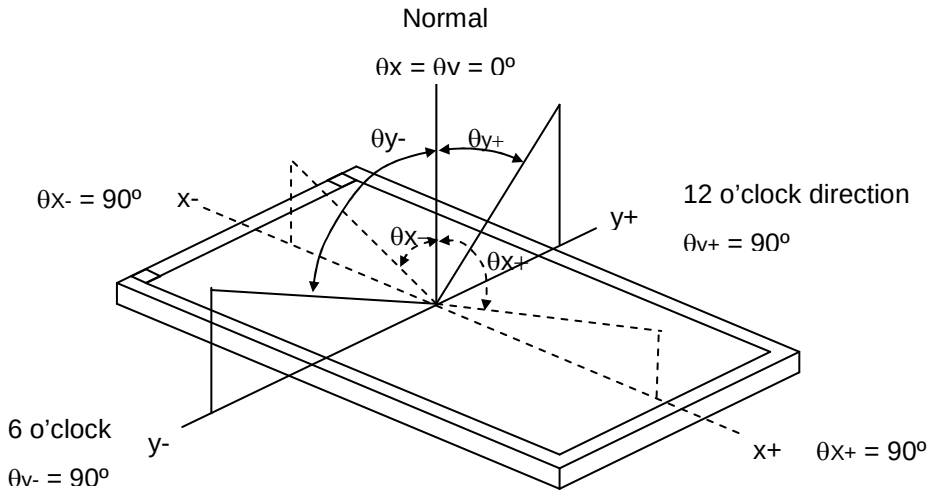
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	84	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	800	1000		-	(2), (5) ,(7)
Response Time		$T_{R+}T_F$			25	30	ms	(3) ,(7)
CP Luminance of White		L_{CP}		300	350		Cd/m^2	(4), (6) ,(7)
Color Chromaticity	Red	Rx		-0.03	0.620	+0.03	-0.03	(1) ,(7)
		Ry			0.356			
	Green	Gx			0.328			
		Gy			0.582			
	Blue	Bx			0.148			
		By			0.062			
	White	Wx			0.295			
		Wy			0.315			
Viewing Angle	Horizontal	θ_x+	CR≥10	80			°	(1),(5) , (7)
		θ_x-		80			°	
	Vertical	θ_Y+		80			°	
		θ_Y-		80			°	
White Variation of 13 Points		δW13p	θx=0°, θY =0°	75	80		75	(5),(6) , (7)

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

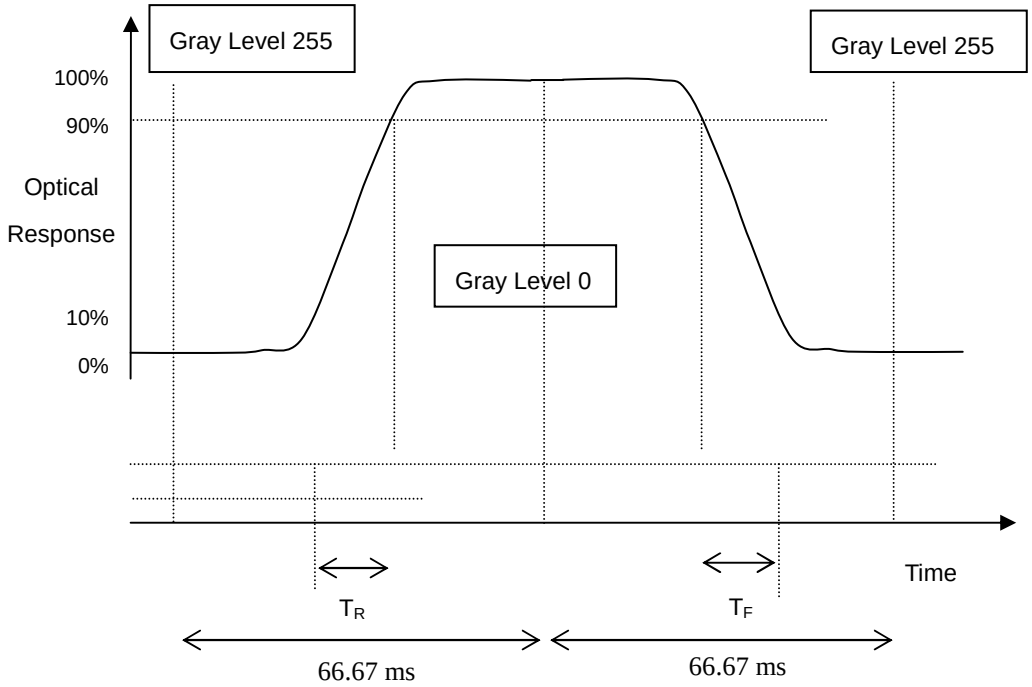
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Center Point Luminance of White (L_{CP}):

Measure the luminance of gray level 255 at center point

L_{CP} = L(1)

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

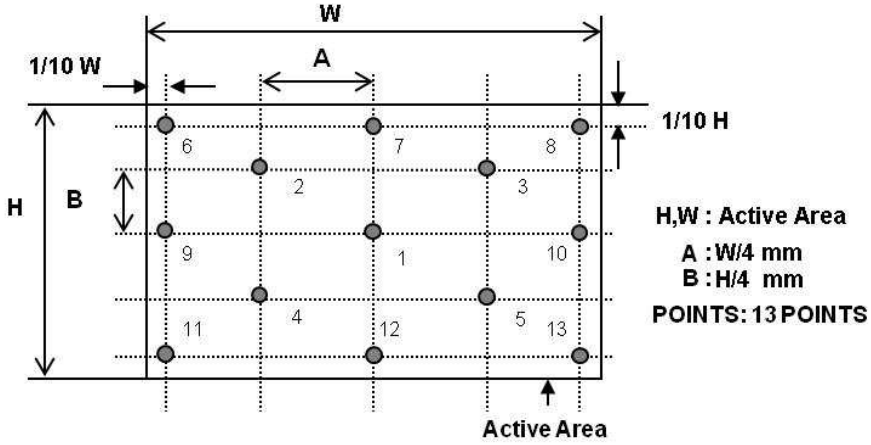
Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 10 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 10 minutes in a windless room.

Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 13 points

δW_{13p} = {Minimum [L (1) ~ L (13)] / Maximum [L (1) ~ L (13)]}*100%



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

ABSOLUTE RATINGS OF ENVIRONMENT

Item	Test Conditions	Remark
High Temperature Storage	T= 60℃,240hours	**(1) (2)**
Low Temperature Storage	T= -20℃,240hours	**(1) (2)**
High Temperature Operation	T = 50℃,240hours	**(1) (2)**
Low Temperature Operation	T = -10℃,240hours	**(1) (2)**
Operate at High Temperature and Humidity	40℃, 90%RH,240hours	**(1) (2)**
Thermal Shock	[(-20℃,30min)→(60℃,30min)],100cycle	**(1) (2)**

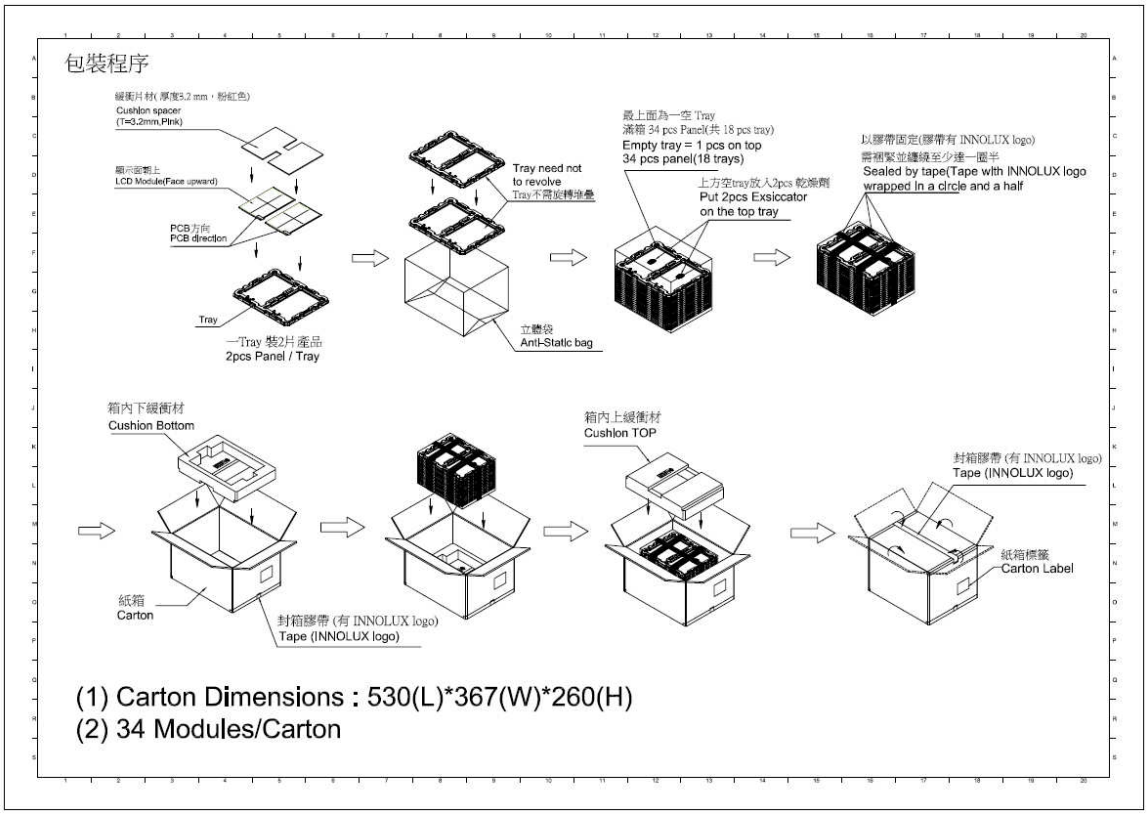
Note:

(1)The test samples have recovery time need more than 2 hours at room temperature before the function check. In the standard conditions , there is no abnormal display function occurred .

(2)After the reliability test , the product only guarantees operational function , but don't guarantee all of the cosmetic specification.

7. Packing Description

The stacked tray per a carton : 18 pcs tray (LCM 34 pcs /1 carton)



NO.	Description	Material
1	LCM	LCM
2	Packing Tray	PET
3	Bag	LDPE
4	Carton Box	Corrugated cardboard

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

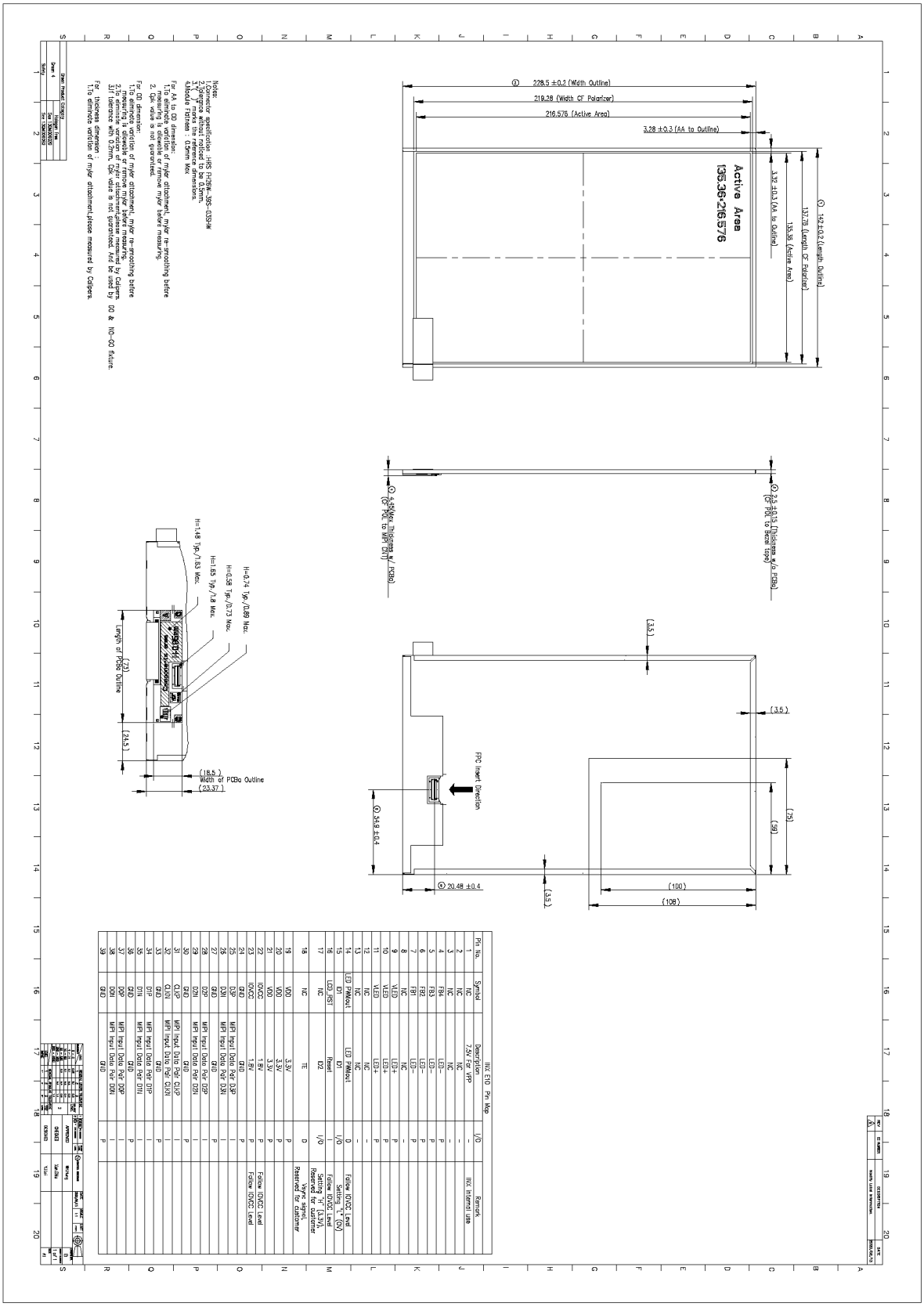
8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

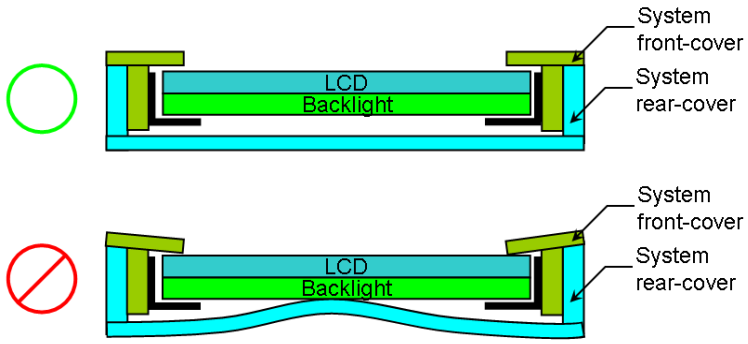
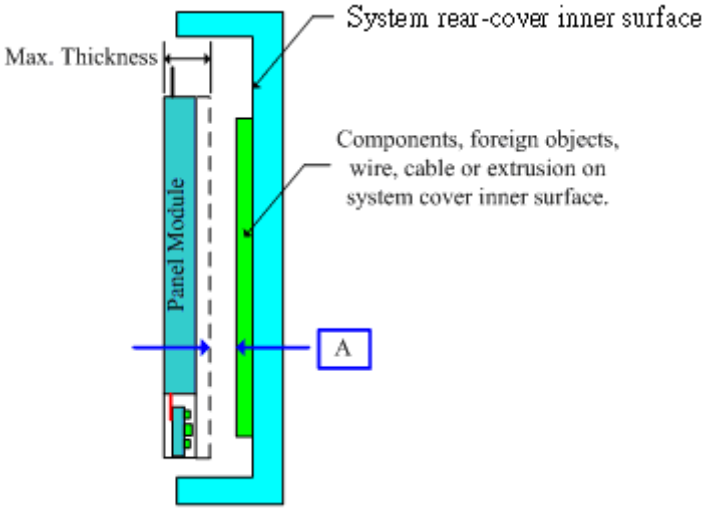
The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit

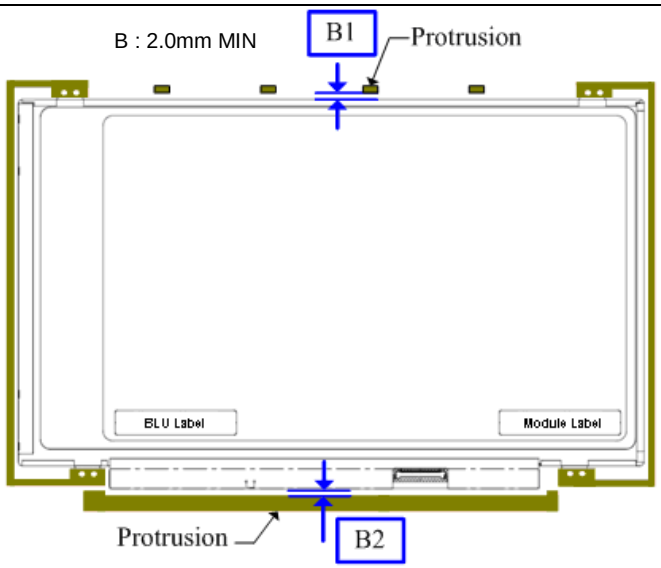
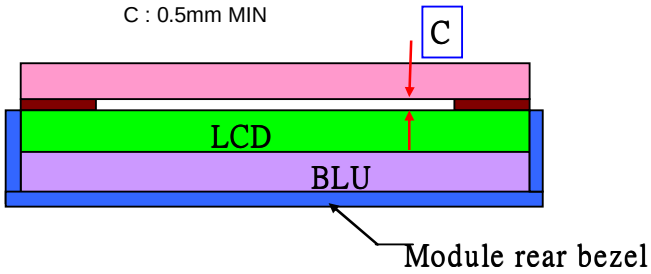
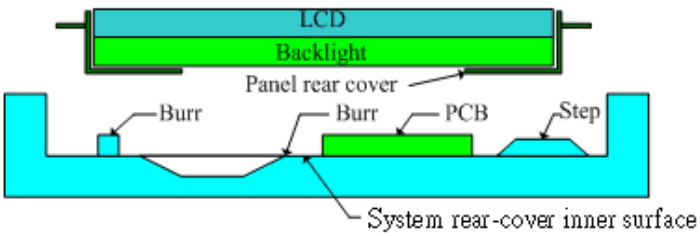
Appendix 1. OUTLINE DRAWING

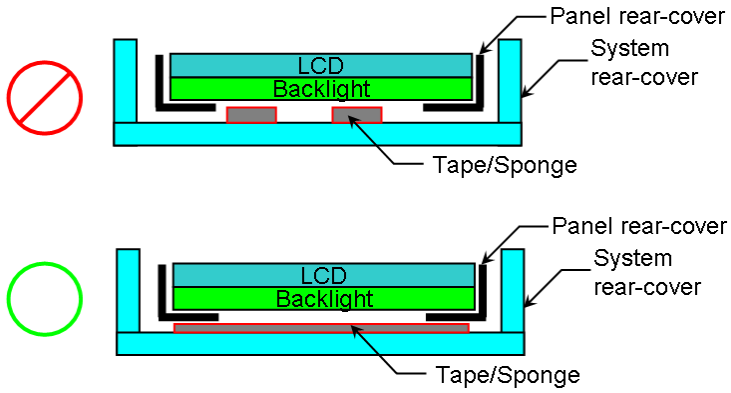
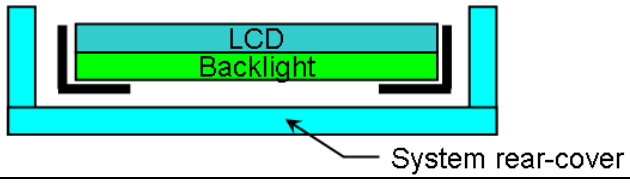
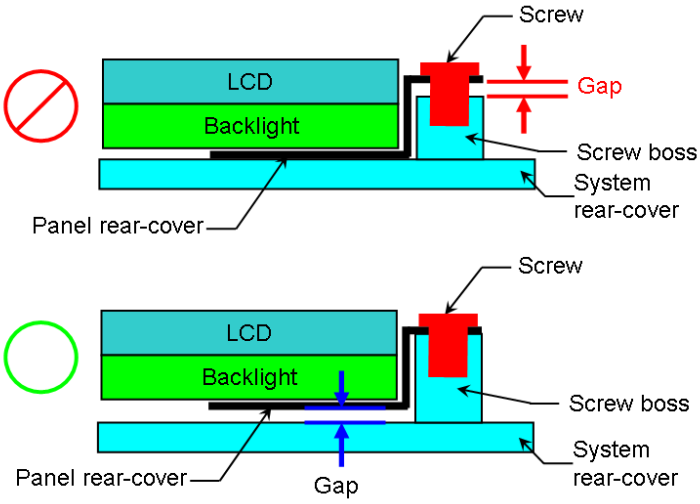


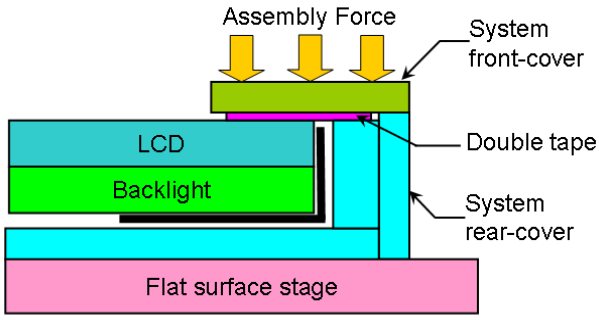
Pin No.	Symbol	IHX E10 Pin Map Description 7.5V For VFP	I/O	Remark
1	NC	NC	–	IHX Internal Use
2	NC	NC	–	
3	NC	NC	–	
4	FB4	LED–	P	
5	FB3	LED–	P	
6	FB2	LED–	P	
7	FB1	LED–	P	
8	NC	NC	–	
9	VLED	LED+	P	
10	VLED	LED+	P	
11	VLED	LED+	P	
12	NC	NC	–	
13	NC	NC	–	
14	LED PWMout	LED PWMout	O	Follow IOVCC Level
15	LED EN	LED EN	I/O	Follow IOVCC Level
16	LED RST	Reset	I/O	Setting "H" (3.3V), Reserved for Customer
17	NC	B02	I/O	Reserved for Customer
18	NC	TE	O	Reserved for Customer
19	VDD	3.3V	P	
20	VDD	3.3V	P	
21	VDD	3.3V	P	
22	IOVCC	1.8V	P	Follow IOVCC Level
23	GND	GND	P	Follow IOVCC Level
24	D3P	MIPI Input Data Pair D3P	I	
25	D3N	MIPI Input Data Pair D3N	I	
26	GND	GND	P	
27	D2P	MIPI Input Data Pair D2P	I	
28	D2N	MIPI Input Data Pair D2N	I	
29	GND	GND	P	
30	D1P	MIPI Input Data Pair D1P	I	
31	D1N	MIPI Input Data Pair D1N	I	
32	GND	GND	P	
33	CLKP	MIPI Input Data Pair CLKP	I	
34	CLKN	MIPI Input Data Pair CLKN	I	
35	GND	GND	P	
36	D0P	MIPI Input Data Pair D0P	I	
37	D0N	MIPI Input Data Pair D0N	I	
38	GND	GND	P	
39	GND	GND	P	

Appendix.2 SYSTEM COVER DESIGN GUIDANCE

1.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.
2.	**Design gap A between panel & any components on system rear-cover**
	
Definition	**Design gap A between panel & any components on system rear-cover**
3	**Design gap B1 & B2 between panel & protrusions**

<table>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>Gap between panel & protrusions is needed to prevent shock test failure. Because protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur.</td></tr>
<tr><td>4</td><td>Design gap C between touch panel & panel surface.</td></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>Air gap design between touch panel & panel surface is needed to prevent pooling, newton ring or glass broken. Compression ration of double side tape may cause pooling issue or newton ring. This phenomenon is obvious during pooling inspection procedure.
To remain sufficient gap between touch panel and panel surface is recommended.</td></tr>
<tr><td>5</td><td>System rear-cover inner surface examination</td></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.</td></tr>
<tr><td>6</td><td>Tape/sponge design on system inner surface</td></tr>
</table>

<table>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.</td></tr>
<tr><td>7</td><td>Material used for system rear-cover</td></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw’s boss positioning for module’s bracket are deformed during open-close test.
Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.</td></tr>
<tr><td>8</td><td>Screw boss height design</td></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>Screw boss height should be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.</td></tr>
<tr><td>9</td><td>Assembly SOP examination for touch panel with double side tape design</td></tr>
</table>

<table>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>To prevent panel crack during touch panel assembly process with double tape design, it is only allowed to give slight pressure with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.</td></tr>
</table>