Doc. version	0.3
Effective date	2007.08.03
Total pages	22
(Not include this cover page)	

Product Specification

2.4″ COLOR TFT-LCD

MODEL NAME: A024QN01 V0

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2007/02/08		First draft
0.1	2007/03/12	15	Modify transmittance from 5.5% to 6.0%
0.2	2007/05/23	18 21-22	Update “G. Suggested FPC Layout Circuit”. Add “I. Recommended Initial Code”.
0.3	2007/08/03	21-23	Update “I. Recommended Initial Code”.

Index

A. General Specification

1. Physical Specifications

NO.	Item	Specification	Remark
1	Display method	Active matrix TFT	
2	Display mode	Transmissive	
3	Display resolution (dot)	240 X RGB (H) X 320(V)	
4	Active area (mm)	36.72 (H) x 48.96 (V)	
5	Screen size (inch)	2.41 inch diagonal	
6	Pixel pitch (mm)	0.153(H) X 0.153(V)	
7	Color configuration	R. G. B. stripe	
8	Display color	262K colors	
9	Surface treatment	Hard Coating	
10	Transmittance	6.0% (Typ.)	
11	Overall dimension (mm)	40.58(H)x 56.96(V)x 1.26(T)	Note 1
12	View Direction	12 o'clock	
13	Weight (g)	TBD	

Key features

- Display moving pictures up to 30 FPS, and support area scrolling and partial display
- MCU interface and RGB interface standardization.

B. Electrical Specifications

1. Input/Output signal interface

<table>
<tr><th>Pin no.</th><th>Symbol</th><th>I/O</th><th>Description</th><th>Connection
When no use</th></tr>
<tr><td>1, 2,
142, 143</td><td>Dummy</td><td>N</td><td>Dummy pin</td><td>N.C.</td></tr>
<tr><td>3 ~ 5,
139 ~
141</td><td>VCOM</td><td>I</td><td>VCOM of LCD panel input.</td><td></td></tr>
<tr><td>6 ~ 13</td><td>VPP1 ~ VPP3</td><td>I</td><td>NVM power input</td><td>Open</td></tr>
<tr><td>14</td><td>TESTO2</td><td>O</td><td>Test pin</td><td>Open</td></tr>
<tr><td>16</td><td>TESTO3</td><td>O</td><td>Test pin</td><td>Open</td></tr>
<tr><td>17, 18</td><td>TEST1, 2</td><td>O</td><td>Test pin</td><td>IOGND</td></tr>
<tr><td>19</td><td>TEST4</td><td>O</td><td>Test pin</td><td>IOVCC</td></tr>
<tr><td>20</td><td>TEST5</td><td>O</td><td>Test pin</td><td>IOGND</td></tr>
<tr><td>21</td><td>Protect</td><td>O</td><td>Test pin</td><td>IOVCC</td></tr>
<tr><td>22 ~ 25</td><td>IM[3..0]</td><td>I</td><td>Select the MCU system interface mode
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MCU I/F</th><th>DB pin used</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Invalid</td><td></td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Invalid</td><td></td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td></td><td>DB[17..10], DB[8..1]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td></td><td>DB[17..10]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td></td><td>SDI, SDO</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>*</td><td>Invalid</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Invalid</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Invalid</td><td></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>i-80, 18bit</td><td>DB[17.. 0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>i-80, 9bit</td><td>DB[17..9]</td></tr>
<tr><td>1</td><td>1</td><td>*</td><td>*</td><td>Invalid</td><td></td></tr>
</table>
When the serial peripheral interface is selected, IM0 pin is used for the device code ID setting.</td><td></td></tr>
<tr><td>26, 28</td><td>TESTO4, 5</td><td>O</td><td>Test pin</td><td>Open</td></tr>
<tr><td>29</td><td>RESET</td><td>I</td><td>Global reset</td><td>IOVCC</td></tr>
<tr><td>30</td><td>VSYNC</td><td>I</td><td>Vertical synchronous signal</td><td>IOVCC</td></tr>
<tr><td>31</td><td>HSYNC</td><td>I</td><td>Horizontal synchronous signal</td><td>IOVCC</td></tr>
</table>

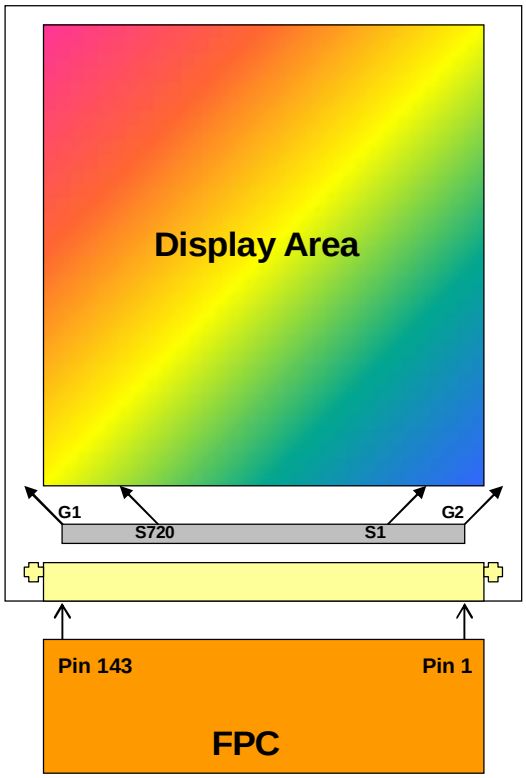
32	DCLK	I	Dot clock	IOVCC
33	ENABLE	I	Data ENEABLE signal for RGB interface operation. Low: Select (access enabled) High: Not select (access inhibited)	IOVCC
34 ~ 43	DB[17.. 8]	I	An 18-bit parallel bi-directional data bus for MCU system interface mode 8-bit I/F: DB[17:10] is used. 9-bit I/F: DB[17:9] is used. 16-bit I/F: DB[17:10] and DB[8:1] is used. 18-bit I/F: DB[17:0] is used. 18-bit parallel bi-directional data bus for RGB interface operation 6-bit RGB I/F: DB[17:12] are used. 16-bit RGB I/F: DB[17:13] and DB[11:1] are used. 18-bit RGB I/F: DB[17:1] are used.	IOVCC
45 ~ 52	DB[7.. 0]	I		
53	SDO	O	Serial data output	Open
54	SDI	I	Serial data input	IOVCC
55	RD	I	A read strobe signal and enables an operation to read out data when the signal is low.	IOVCC
56	WR	I	A write strobe signal and enables an operation to write data when the signal is low.	IOVCC
57	RS	I	A register select signal. Low: select an index or status register High: select a control register	IOVCC
58	CS	I	A chip select signal. Low: the chip is selected and accessible High: the chip is not selected and not accessible	IOVCC
60	TESTO9	O	Test pin	Open
61	FMARK	O	Output a frame head pulse signal. The FMARK signal is used when writing RAM data in synchronization with frame. Leave the pin open when not in use.	Open
62 ~ 69	TS [0..8]	O	Test pin	Open
70	TSC	O	Test pin	IOGND

71, 73, 74	TESTO10, 11, 12	O	Test pin	Open
75	DummyR	N	Dummy pin	N.C.
76 ~ 78	IOGND	G	IO Ground	
79 ~ 81	IOVCC	PI	IO digital power supply	
82 ~ 84	VCI	PI	Analog power input, 2.6~3.3V is recommended.	
85 ~ 87	VDD	C	Charge pumping circuit pin, connect to a capacitor	
88 ~ 90	AGND	G	Analog ground	
91 ~ 95	AGND	G	Analog groun	
96	VGS	C	Charge pumping circuit pin, connect to ground	
97, 98	VCOM	O	VCOM from IC, connect it to pin139 ~ 141 and pin 3 ~ 5	
99, 100	VCOMH	C	Charge pumping circuit pin, connect to a capacitor	
101, 102	VCOML	C	Charge pumping circuit pin, connect to a capacitor	
103	VREG1OUT	C	Charge pumping circuit pin, connect to a capacitor	
104	VCOMR	I	A reference level to generate the VCOMH level either with an externally connected variable resistor or by setting the register of the IC. When using a variable resistor, halt the internal VCOMH adjusting circuit by setting the register and place the resister between VREG1OUT and AGND. When generating the VCOMH level by setting the register, leave this pin open.	Open
105	VCL	C	Charge pumping circuit pin, connect to a capacitor	
106 ~108	AVDD	C	Charge pumping circuit pin, connect to a capacitor	
109 ~ 111	VCI1	C	Charge pumping circuit pin, connect to a capacitor	
112 ~ 115	VCI	PI	Analog power input, 2.6~3.3V is recommended.	
116, 117	C12-	C	Charge pumping circuit pin, connect to a capacitor	

118, 119	C12+	C	Charge pumping circuit pin, connect to a capacitor	
120, 121	C11-	C	Charge pumping circuit pin, connect to a capacitor	
122, 123	C11+	C	Charge pumping circuit pin, connect to a capacitor	
124 ~ 127	VGL	C	Charge pumping circuit pin, connect to a capacitor	
128 ~ 130	VGH	C	Charge pumping circuit pin, connect to a capacitor	
131	C13-	C	Charge pumping circuit pin, connect to a capacitor	
132	C13+	C	Charge pumping circuit pin, connect to a capacitor	
133	C21-	C	Charge pumping circuit pin, connect to a capacitor	
134	C21+	C	Charge pumping circuit pin, connect to a capacitor	
135	C22-	C	Charge pumping circuit pin, connect to a capacitor	
136	C22+	C	Charge pumping circuit pin, connect to a capacitor	
137	C23-	C	Charge pumping circuit pin, connect to a capacitor	
138	C23+	C	Charge pumping circuit pin, connect to a capacitor	
15, 44, 72	IOGNDDUM	O	Output the IOGND voltage level.	
27, 59	IOVCCDUM	O	Output the IOVCC voltage level.	

Note 1: Refer below figure to indicate pin1 and pin143.

Note 2: Customer can refer to H item of page 21 to design FPC.



2. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remark
Input power supply	Vcc	-0.3	4.6	V	Note 1
LCD supply voltage range	VGH-VGL	-0.3	30	V	
LCD input voltage range	Vi	-0.3	Vcc+0.3	V	Note 2
Operating temperature (Ambient)	T_{OPA}	0	60	℃	
Storage temperature (Ambient)	T_{STG}	-25	80	℃	

Note 1: If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop.

Note 2: *DB0 ~DB15*, $\overline{CS}$, $\overline{RS}$, $\overline{WR}$, $\overline{RD}$, $\overline{RESET}$

3. Electrical characteristics

3.1 Typical operating conditions

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Input power supply		Vcc	2.6	2.8	3.3	V	Note 1
Input Signal Voltage	H Level	V_{IH}	0.7 x Vcc	-	Vcc	V	Note 2
	L Level	V_{IL}	0	-	0.3 x Vcc	V	
Output signal voltage	H Level	V_{OH}	0.8 x Vcc	-	Vcc	V	Note 3
	L Level	V_{OL}	0	-	0.2 x Vcc	V	

Note 1: The operations are guaranteed under the recommended operating conditions only. These operations are not guaranteed if a quick voltage change occurs during operation. To prevent noise, a bypass capacitor must be inserted into the line close to power pin.

Note 2: $\overline{CS}$, $\overline{RS}$, *DBN (N=0 ~15)*, $\overline{WR}$, $\overline{RD}$, $\overline{RESET}$,

Note 3: *DBN (N=0 ~15)*

3.2 Power consumption (Note 1)

Mode	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Stand-by	P_S	V_{CC} = 2.8V	-		TBD	mW	Note 2
Partial display	P_P		-	-	TBD	mW	Note 3
Still (65k colors)	P_g		-	-	TBD	mW	Note 4

Note 1: No backlight is driven

Note 2: Display off, black pattern

Note 3: 20 black display lines

Note 4: Full screen with 65K colors (Line inversion)

4. AC Characteristics

4.1 CPU i80 system

VDD = 2.6 to 3.3V, AGND=DGND=0V, Ta = -30 to 70˚C

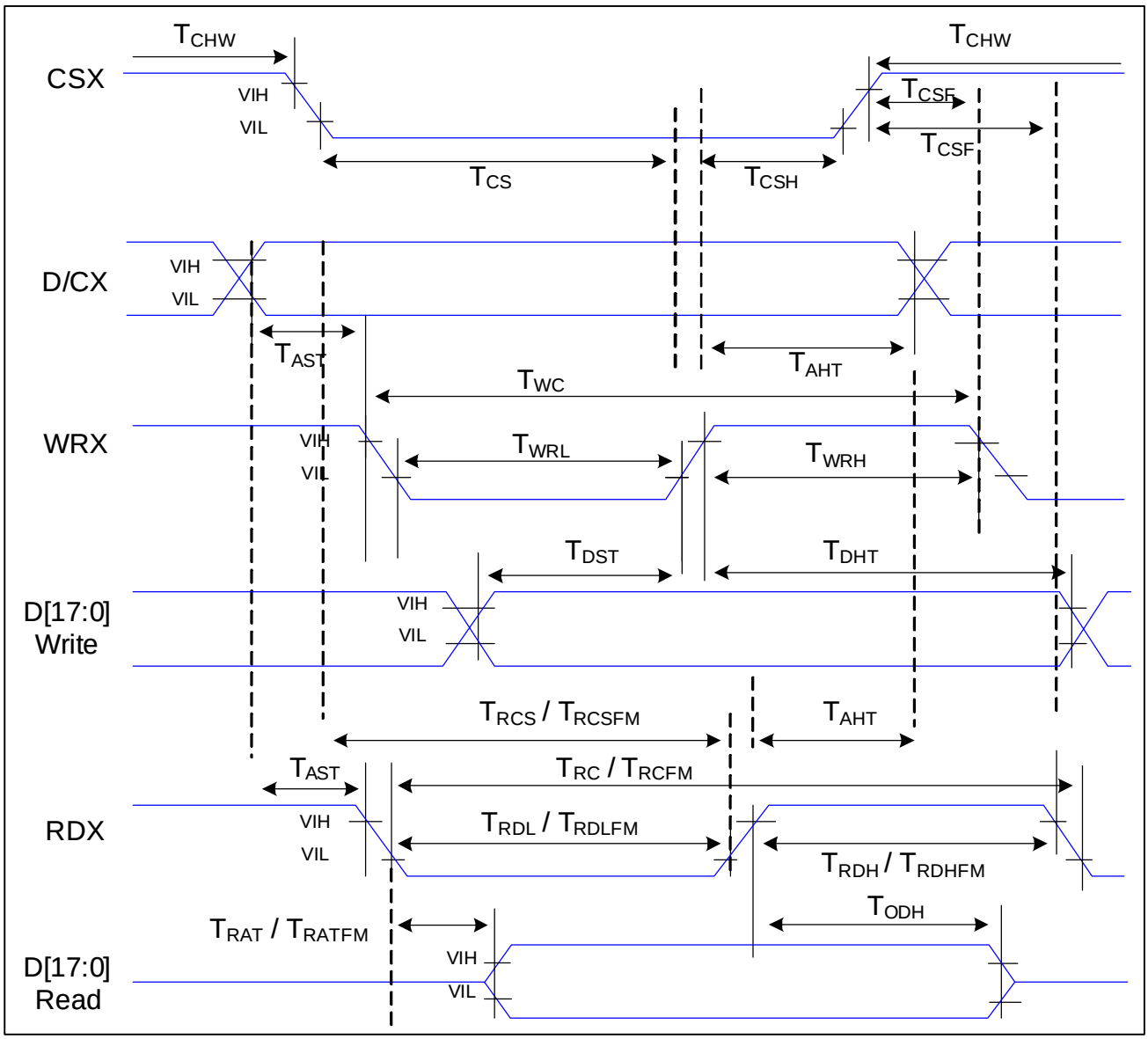


Figure 1: Parallel interface characteristics (8080-series MCU)

Signal	Symbol	Parameter	MIN	MAX	Unit
D/CX	T_{AST}	Address setup time	10		ns
	T_{AHT}	Address hold time (Write/Read)	10		ns
CSX	T_{CHW}	Chip select “H” pulse width	0		ns
	T_{CS}	Chip select setup time (Write)	35		ns
	T_{RCS}	Chip select setup time (Read ID)	45		ns
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns
	T_{CSF}	Chip select wait time (Write/Read)	10		ns
	T_{CSH}	Chip select hold time	10		ns
WRX	T_{WC}	Write cycle	100		ns
	T_{WRH}	Control pulse “H” duration	35		ns
	T_{WRL}	Control pulse “L” duration	35		ns
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns
	T_{RDH}	Control pulse “H” duration (ID)	90		ns
	T_{RDL}	Control pulse “L” duration (ID)	45		ns
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns
	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns
D[17:0]	T_{DST}	Data setup time	10		ns
	T_{DHT}	Data hold time	10		ns
	T_{RAT}	Read access time (ID)		40	ns
	T_{RATFM}	Read access time (FM)		340	ns
	T_{ODH}	Output disable time	20	80	ns

The input signal rise time and fall time for VIH and VIL is specified at 15ns or less.

4.2 CPU i68 system

VDD = 2.6 to 3.3V, AGND=DGND=0V, Ta = -30 to 70˚C

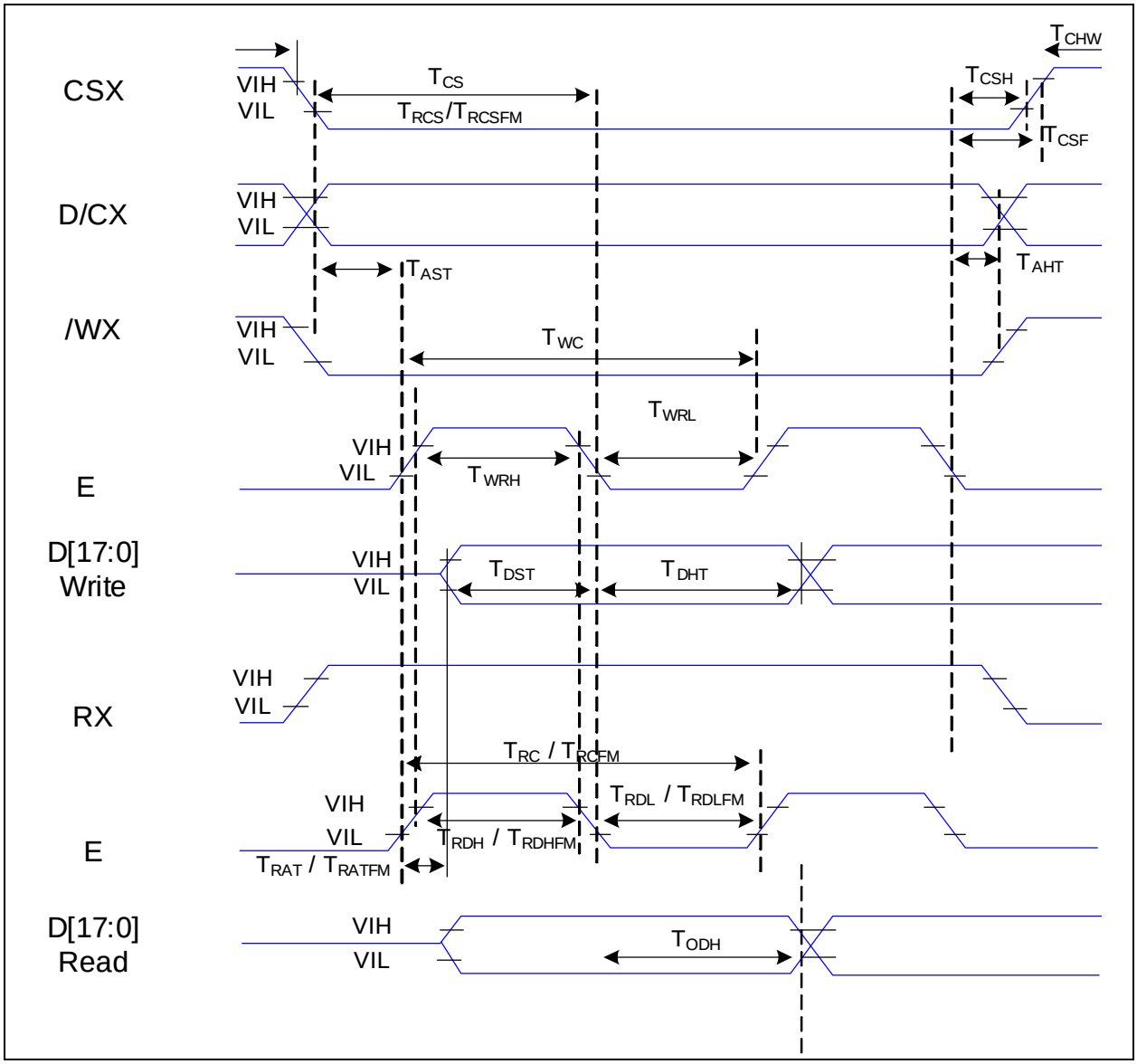


Figure 2: Parallel interface characteristics (6800-series MCU).

Signal	Symbol	Parameter	MIN	MAX	Unit
D/CX	T_{AST}	Address setup time	10		ns
	T_{AHT}	Address hold time (Write/Read)	10		ns
CSX	T_{CHW}	Chip select “H” pulse width	0		ns
	T_{CS}	Chip select setup time (Write)	35		ns
	T_{RCS}	Chip select setup time (Read ID)	45		ns
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns
	T_{CSF}	Chip select wait time (Write/Read)	10		ns
	T_{CSH}	Chip select hold time	10		ns
WRX	T_{WC}	Write cycle	100		ns
	T_{WRH}	Control pulse “H” duration	35		ns
	T_{WRL}	Control pulse “L” duration	35		ns
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns
	T_{RDH}	Control pulse “H” duration (ID)	90		ns
	T_{RDL}	Control pulse “L” duration (ID)	45		ns
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns
	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns
D[17:0]	T_{DST}	Data setup time	10		ns
	T_{DHT}	Data hold time	10		ns
	T_{RAT}	Read access time (ID)		40	ns
	T_{RATFM}	Read access time (FM)		340	ns
	T_{ODH}	Output disable time	20	80	ns

The input signal rise time and fall time for VIH and VIL is specified at 15ns or less.

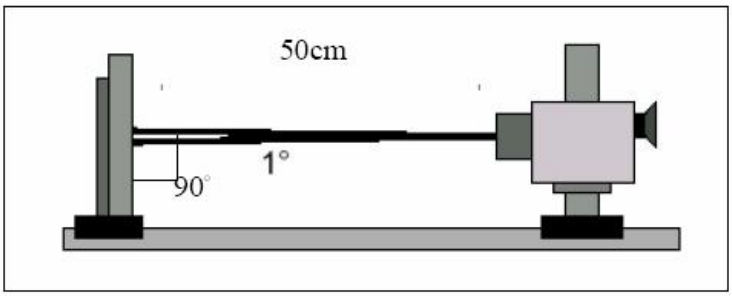
C. Optical Specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise	Tr	θ =0°	-	12	-	ms	Note 4
	Fall	Tf		-	18	-	ms	
Contrast ratio		CR	At optimize viewing angle	250	300	-	-	Note 5
Transmittance		%			6.0		%	
Viewing angle	Top	-	CR≧5	40	60	-	deg.	Note 6
	Bottom			10	20	-		
	Left			30	45	-		
	Right			30	45	-		
Color Tone	White	Wx	θ =0°	0.26	0.31	0.36	-	
		Wy		0.28	0.33	0.38		

Note 1: Ta =25℃±2℃.

Note 2: To be measured in the dark room.

Note 3: To be measured at the center area of panel with a aperture of 1° by Topcon luminance meter BM-5A , after 10 minutes module operation.

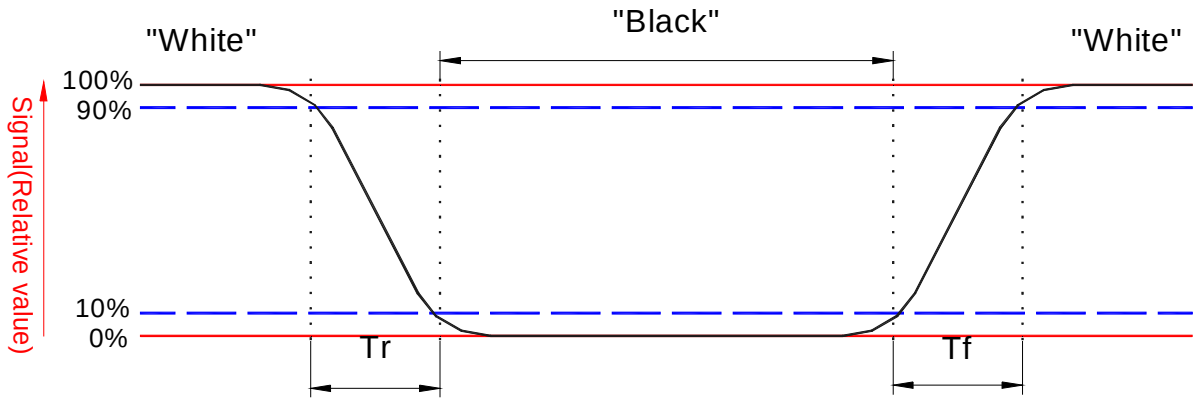


Note 4: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white” (falling time) and from “white” to “black” (rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes.

Refer to figure as below:



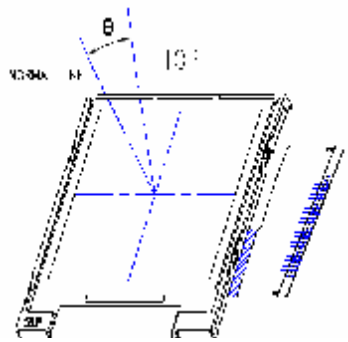
Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. Definition of viewing angle:

Refer to the figure as below.



D. Reliability Test Items:

1. Test Items and Conditions

No.	Test items	Conditions		Remark
1	High temperature storage	Ta= 80℃	168H	
2	Low temperature storage	Ta= -25℃	168H	
3	High temperature operation	Ta= 60℃	168H	
4	Low temperature operation	Ta= 0℃	168H	
5	High temperature and high humidity	Ta= 60℃. 90% RH	168H	Operation
6	Heat shock	-25℃~80℃/50 cycles 2H/cycle		Non-operation
7	Electrostatic discharge	±200V, 200pF(0Ω), once for each terminal		Non-operation
8	Drop (with carton)	Height: 80cm 1 corner, 3 edges, 6 surfaces		

Note 1: Ta: Ambient Temperature.

Note 2: After finishing the test, leave the samples under room temperature and normal humidity for 2 hours, and then this module should work normally.

Note 3: Failure Judgment Criterion:

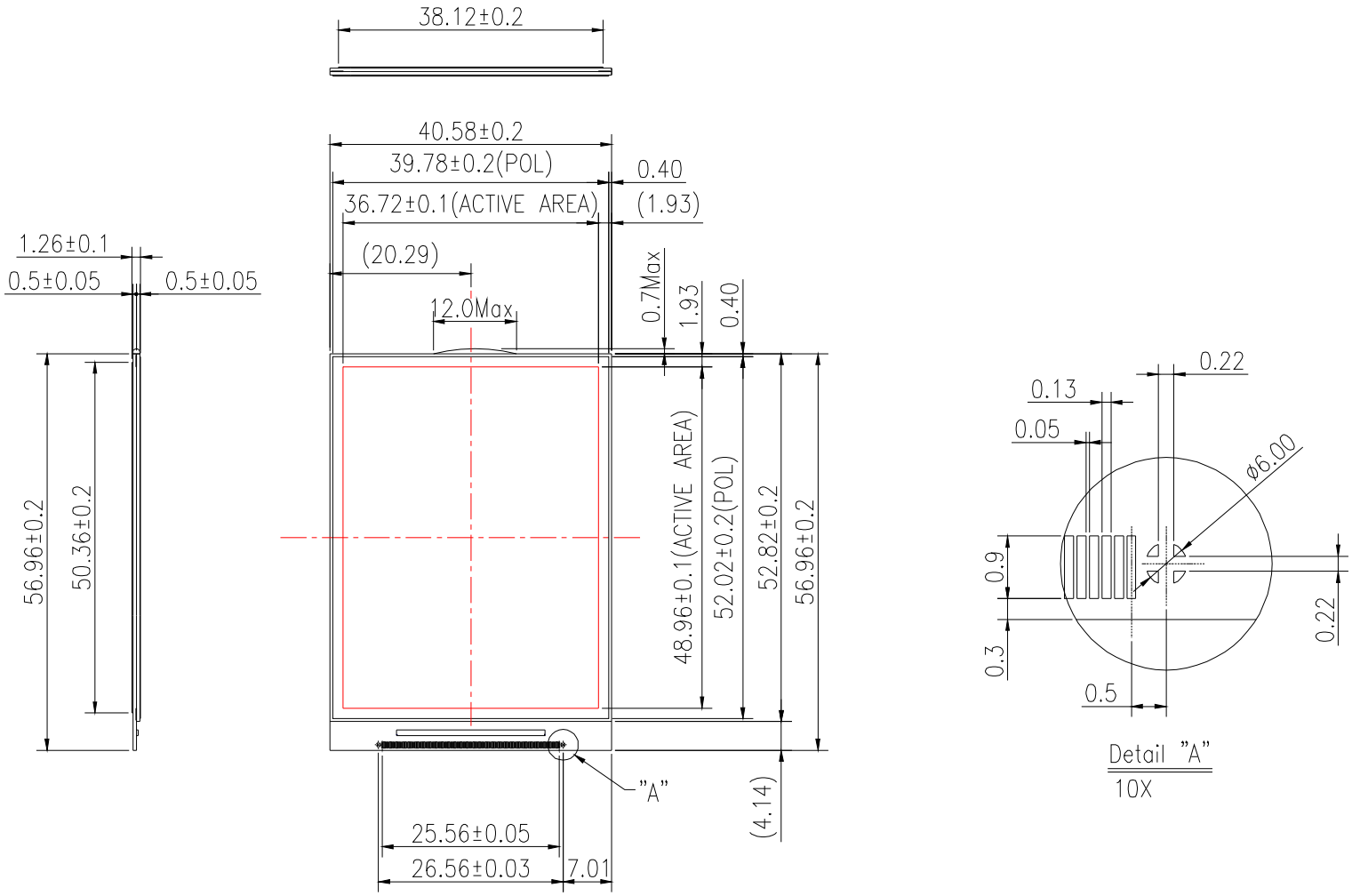
a. Squarely inspect all LCD function before and after reliability test.

b. In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

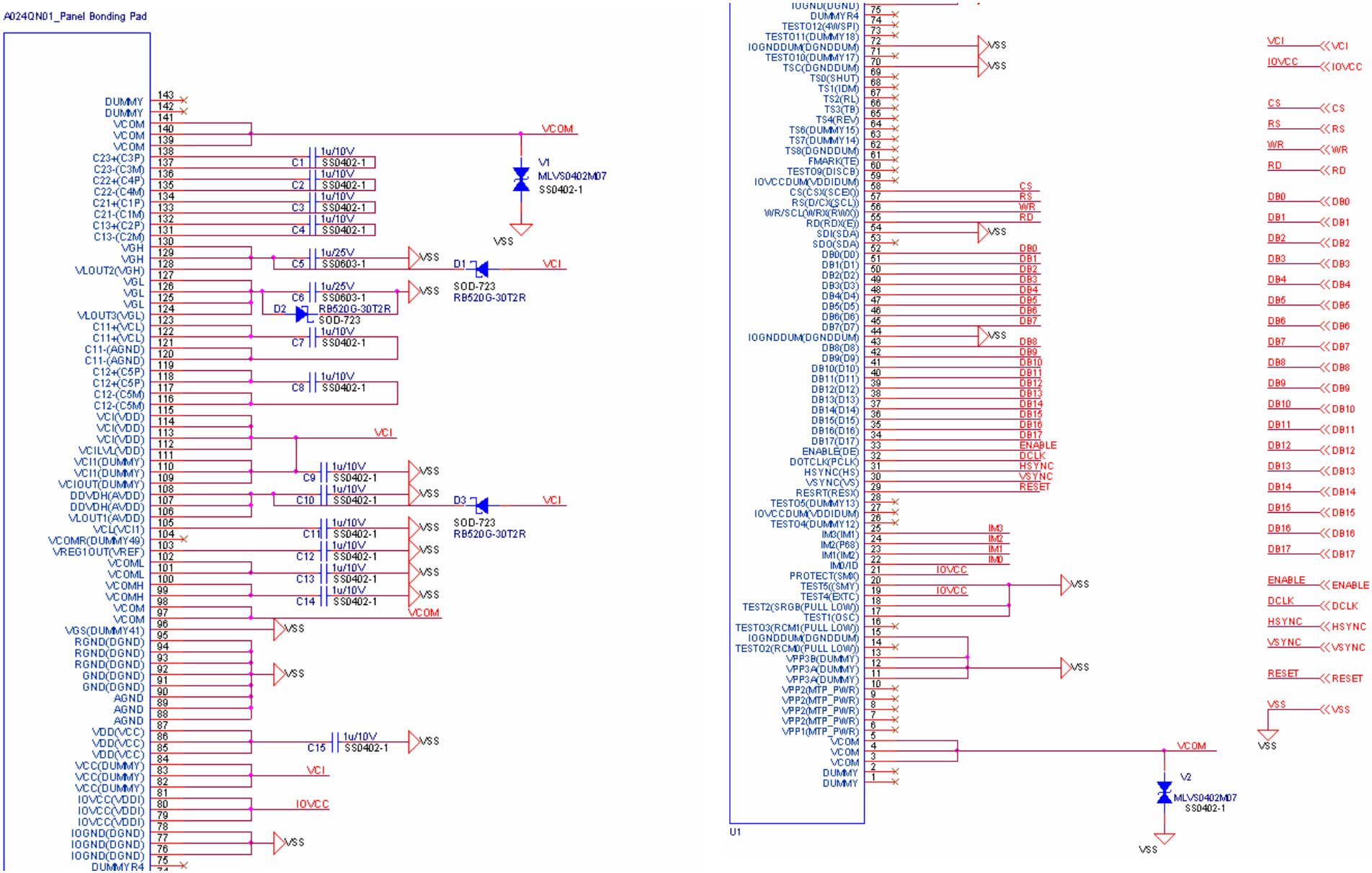
E. Packing Form

TBD

F. Outline Dimensions of TFT LCD Drawing



G. Suggested FPC Layout Circuit



H. Suggested Pin assignment of FPC

Pin no.	Symbol	I/O	Description	Remarks
1	VCI	PI	Analog power input, 2.6~3.3V is recommended.	
2	IOVCC	PI	Digital power input, 1.65~3.3V is recommended.	
3	CS	I	A chip select signal. Low: the chip is selected and accessible High: the chip is not selected and not accessible	
4	RS	I	A register select signal. Low: select an index or status register High: select a control register	
5	WR	I	A write strobe signal and enables an operation to write data when the signal is low.	
6	RD	I	A read strobe signal and enables an operation to read out data when the signal is low.	
7	DB0	I	An 18-bit parallel bi-directional data bus for MCU system interface mode 8-bit I/F: DB[17:10] is used. 9-bit I/F: DB[17:9] is used. 16-bit I/F: DB[17:10] and DB[8:1] is used. 18-bit I/F: DB[17:0] is used. 18-bit parallel bi-directional data bus for RGB interface operation 6-bit RGB I/F: DB[17:12] are used. 16-bit RGB I/F: DB[17:13] and DB[11:1] are used. 18-bit RGB I/F: DB[17:1] are used.	
8	DB1	I		
9	DB2	I		
10	DB3	I		
11	DB4	I		
12	DB5	I		
13	DB6	I		
14	DB7	I		
15	DB8	I		
16	DB9	I		
17	DB10	I		
18	DB11	I		
19	DB12	I		
20	DB13	I		
21	DB14	I		
22	DB15	I		
23	DB16	I		

24	DB17	I		
25	ENABLE	I	Data ENEABLE signal for RGB interface operation. Low: Select (access enabled) High: Not select (access inhibited)	
26	DCLK	I	Dot clock	
27	HSYNC	I	Horizontal synchronous signal	
28	VSYNC	I	Vertical synchronous signal	
29	RESET	I	Global reset	
30	VSS	G	Ground	

Note 1: I: Digital signal input, O: Digital signal output, IO: Digital inout pin, G: GND, PI: Power input.

Note 2: Customer could consider putting LED pad on FPC.

I. Recommended Initial Code

Step	Register Address	Register Value	Remark
1	R00h	0x0000	
2	R01h	0x0100	
3	R02h	0x0701	
4	R03h	0xd030	For 8-bit data bus D15[TRI]=1, 18 bit in 3 times transfer. Set D15[TRI]=0, when using neither 8-bit nor 16-bit.
5	R04h	0x0000	
6	R08h	0x0207	
7	R0Ah	0x0000	
8	R0Ch	0x0000	
9	R0Dh	0x0000	
10	R0Fh	0x0000	
11	R07h	0x0101	
12	R10h	0x15b0	
13	R11h	0x0007	
14	R17h	0x0001	
15	R12h	0x01bb	
16	R13h	0x1c00	
17	R29h	0x0012	
18	R50h	0x0000	
19	R51h	0x00ef	
20	R52h	0x0000	
21	R53h	0x013f	
22	R30h	0x0102	Gamma setting of VSD0
23	R31h	0x0c20	Gamma setting of VSD1
24	R32h	0x0b21	Gamma setting of VSD2
25	R33h	0x250f	Gamma setting of VSD61

26	R34h	0x1d0b	Gamma setting of VSD62
27	R35h	0x0a04	Gamma setting of VSD63
28	R36h	0x1701	Gamma setting of VSD13
29	R37h	0x0617	Gamma setting of VSD50
30	R38h	0x0305	Gamma setting of VSD4
31	R39h	0x0A05	Gamma setting of VSD8
32	R3Ah	0x0f04	Gamma setting of VSD20
33	R3Bh	0x0f00	Gamma setting of VSD27
34	R3Ch	0x000f	Gamma setting of VSD36
35	R3Dh	0x050f	Gamma setting of VSD43
36	R3Eh	0x0204	Gamma setting of VSD55
37	R3Fh	0x0404	Gamma setting of VSD59
38	R90h	0x2700	
39	R92h	0x0000	
40	R93h	0x0103	
41	R95h	0x0110	
42	R97h	0x0000	
43	R98h	0x0000	
44	RF0h	0x5408	
45	RF3h	0x0010	
46	RF4h	0x001f	
47	RF0h	0x0010	
49	R07h	0x0173	
50	R95h	0x0110	
51	R97h	0x0000	
52	R98h	0x0000	
53	RF0h	0x5408	
54	RF3h	0x0005	
55	RF4h	0x001f	

56	RF0h	0x0000	
57	R07h	0x0173	