



TL055VDXP43-00

Coversheet

MODEL NO. : TL055VDXP43-00_

ISSUED DATE: 2015-9-09

VERSION Ver 2.0

> □ Preliminary Specification **■**Final Product Specification

Approved by	Notes

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This technical specification is subjected to change without notice



Global LCD Panel Exchange Center

XIAMEN TIANMA MICRO-ELECTRONICS

TL055VDXP43-00

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Record of Revision

Rev	Issued Date	Description	Editor
1.0	2015-2-5	Preliminary Specification Release	周磊
2.0	2015-2-5	Preliminary Specification Release	周磊





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1. General Specifications

	Feature	Spec
	Size	5.46inch
	Resolution	1080(RGB) x1920
	Interface	MIPI 4 Lane
	Color Depth	16.7M
Display Spec.	Technology Type	LTPS SFT
Diopiny open.	Pixel Pitch (mm)	21um*63um
	Pixel Configuration	R.G.B. Vertical Stripe
	Display Mode	SFT with Normally Black two domain
	Surface Treatment(Up Polarizer)	Clear Type(3H)
	LCM (W x H x D) (mm)	70.44mm*128.66mm*1.34mm
	Active Area(mm)	68.04mm*120.96mm
Mechanical Characteristics	With /Without TSP	Without TSP
Onaracteristics	Weight (g)	TBD
	LED Numbers	12LEDs
Electronic	Driver IC	NT35596

Note 1: Requirements on Environmental Protection: Q/S0002

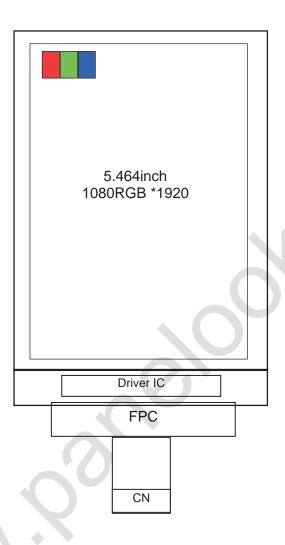
Note 2: LCM weight tolerance: +/- 5%





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2. BLOCK DIAGRAM





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3. INPUT/OUTPUT TERMINALS PIN ASSIGNMENT

3.1 CN1 of FPC

Section	NO.	Symbol	I/O	Power Rail	Description
S	1	GND	Р	GND	System ground
4 RST I IOVCC LCD Reset siganl 5 TE O IOVCC TE signal 6 NC NC 7 GND P GND System ground 8 D3+ I/O MIPI DATA lane 3+ 9 NC NC 10 D3- I/O MIPI DATA lane 3- 11 GND P GND System ground 12 D2+ I/O MIPI DATA lane 3- 13 NC MIPI DATA lane 2- NC 14 D2- I/O MIPI DATA lane 2- 15 GND P GND System ground 16 CLK+ I/O MIPI CLK lane - 17 NC NC 18 CLK- I/O MIPI CLK lane - 19 GND P GND System ground </td <td>2</td> <td>LCM_ID0</td> <td>I</td> <td>GND</td> <td>ID PIN0</td>	2	LCM_ID0	I	GND	ID PIN0
5 TE O IOVCC TE signal 6 NC NC 7 GND P GND System ground 8 D3+ I/O MIPI DATA lane 3+ 9 NC MIPI DATA lane 3- 10 D3- I/O MIPI DATA lane 3- 11 GND P GND System ground 12 D2+ I/O MIPI DATA lane 2- 13 NC NC 14 D2- I/O MIPI DATA lane 2- 15 GND P GND System ground 16 CLK+ I/O MIPI CLK lane 2- 17 NC NC 18 CLK- I/O MIPI CLK lane - 19 GND P GND System ground 20 D1+ I/O	3	LCM_ID1	I	IOVCC	ID PIN1
6 NC NC 7 GND P GND System ground 8 D3+ I/O MIPI DATA lane 3+ 9 NC NC 10 D3- I/O MIPI DATA lane 3- 11 GND P GND System ground 12 D2+ I/O MIPI DATA lane 3- 13 NC NC 14 D2- I/O MIPI DATA lane 3- 15 GND P GND System ground 16 CLK- I/O MIPI DATA lane 2- 15 GND P GND System ground 16 CLK- I/O MIPI CLK lane 2- 17 NC NC NC 18 CLK- I/O MIPI CLK lane - NC 19 GND P	4	RST	I	IOVCC	LCD Reset siganl
7 GND P GND System ground 8 D3+ I/O MIPI DATA lane 3+ 9 NC NC 10 D3- I/O MIPI DATA lane 3- 11 GND P GND System ground 12 D2+ I/O MIPI DATA lane 2- 13 NC NC MIPI DATA lane 2- 14 D2- I/O MIPI DATA lane 2- 15 GND P GND System ground 16 CLK+ I/O MIPI CLK lane 2- 15 GND P GND System ground 16 CLK- I/O MIPI CLK lane 4- 17 NC NC NC 18 CLK- I/O MIPI DATA lane 2- 19 GND P GND System ground 20 D1+ I/O </td <td>5</td> <td>TE</td> <td>0</td> <td>IOVCC</td> <td>TE signal</td>	5	TE	0	IOVCC	TE signal
8 D3+ I/O MIPI DATA lane 3+ 9 NC NC 10 D3- I/O MIPI DATA lane 3- 11 GND P GND System ground 12 D2+ I/O MIPI DATA lane 2+ 13 NC NC 14 D2- I/O MIPI DATA lane 2+ 15 GND P GND System ground 16 CLK+ I/O MIPI CLK lane 2- 17 NC NC 18 CLK- I/O MIPI CLK lane 4- 17 NC NC 18 CLK- I/O MIPI CLK lane 4- 17 NC NC 20 D1+ I/O NC 21 NC NC NC	6	NC			NC
8 D3+ I/O MIPI DATA lane 3+ 9 NC NC 10 D3- I/O MIPI DATA lane 3- 11 GND P GND System ground 12 D2+ I/O MIPI DATA lane 2+ 13 NC NC 14 D2- I/O MIPI DATA lane 2+ 15 GND P GND System ground 16 CLK+ I/O MIPI CLK lane 2- 17 NC NC 18 CLK- I/O MIPI CLK lane 4- 17 NC NC 18 CLK- I/O MIPI CLK lane 4- 17 NC NC 20 D1+ I/O NC 21 NC NC NC	7	GND	Р	GND	System ground
10	8	D3+	I/O		
11	9	NC			NC
12 D2+ I/O MIPI DATA lane 2+ 13 NC NC 14 D2- I/O MIPI DATA lane 2- 15 GND P GND System ground 16 CLK+ I/O MIPI CLK lane + 17 NC NC MIPI CLK lane + 17 NC MIPI CLK lane - NC 18 CLK- I/O MIPI CLK lane - NC 19 GND P GND System ground 20 D1+ I/O NC 21 NC NC NC 22 D1- I/O MIPI DATA lane 1- 23 GND P GND System ground 24 D0+ I/O NC 25 NC NC 26 D0- I/O	10	D3-	I/O		MIPI DATA lane 3-
13 NC NC 14 D2- I/O MIPI DATA lane 2- 15 GND P GND System ground 16 CLK+ I/O MIPI CLK lane + 17 NC NC 18 CLK- I/O MIPI CLK lane - 19 GND P GND System ground 20 D1+ I/O MIPI DATA lane 1+ 21 NC NC 22 D1- I/O MIPI DATA lane 1+ 23 GND P GND System ground 24 D0+ I/O MIPI DATA lane 0- 25 NC NC 26 D0- I/O MIPI DATA lane 0- 27 GND P GND System ground 28 AVDD P ANDD Analog pow	11	GND	Р	GND	System ground
14 D2- I/O MIPI DATA lane 2- 15 GND P GND System ground 16 CLK+ I/O MIPI CLK lane + 17 NC NC 18 CLK- I/O MIPI CLK lane - 19 GND P GND System ground 20 D1+ I/O MIPI DATA lane 1+ 21 NC NC NC 22 D1- I/O MIPI DATA lane 1+ 23 GND P GND System ground 24 D0+ I/O MIPI DATA lane 0+ 25 NC NC NC 26 D0- I/O MIPI DATA lane 0+ 27 GND P GND System ground 28 AVDD P AVDD Analog power supply 30 IOVCC P IOVCC	12	D2+	I/O		MIPI DATA lane 2+
15 GND P GND System ground 16 CLK+ I/O MIPI CLK lane + 17 NC NC 18 CLK- I/O MIPI CLK lane - 19 GND P GND System ground 20 D1+ I/O MIPI DATA lane 1+ 21 NC NC 22 D1- I/O MIPI DATA lane 1+ 23 GND P GND System ground 24 D0+ I/O MIPI DATA lane 1- 25 NC NC 26 D0- I/O MIPI DATA lane 0+ 27 GND P GND System ground 28 AVDD P GND System ground 28 AVDD P AVEE Analog power supply 30 IOVCC P	13	NC			NC
16 CLK+ I/O MIPI CLK lane + 17 NC NC 18 CLK- I/O MIPI CLK lane - 19 GND P GND System ground 20 D1+ I/O MIPI DATA lane 1+ 21 NC NC 22 D1- I/O MIPI DATA lane 1+ 23 GND P GND System ground 24 D0+ I/O MIPI DATA lane 1- 23 GND P GND System ground 24 D0+ I/O MIPI DATA lane 1- 25 NC NC 26 D0- I/O MIPI DATA lane 0- 25 NC NC 26 D0- I/O MIPI DATA lane 0- 25 NC	14	D2-	I/O		MIPI DATA lane 2-
17 NC NC 18 CLK- I/O MIPI CLK lane - 19 GND P GND System ground 20 D1+ I/O MIPI DATA lane 1+ 21 NC NC 22 D1- I/O MIPI DATA lane 1- 23 GND P GND System ground 24 D0+ I/O MIPI DATA lane 0- 25 NC NC 26 D0- I/O MIPI DATA lane 0- 27 GND P GND System ground 28 AVDD P AVDD Analog power supply 29 AVEE P AVEE Analog power supply 30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P <td>15</td> <td>GND</td> <td>Р</td> <td>GND</td> <td>System ground</td>	15	GND	Р	GND	System ground
18 CLK- I/O MIPI CLK lane - 19 GND P GND System ground 20 D1+ I/O MIPI DATA lane 1+ 21 NC NC 22 D1- I/O MIPI DATA lane 1- 23 GND P GND System ground 24 D0+ I/O MIPI DATA lane 0- 25 NC NC 26 D0- I/O MIPI DATA lane 0- 27 GND P GND System ground 28 AVDD P GND System ground 28 AVDD P AVEE Analog power supply 29 AVEE P AVEE Analog power supply 30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+	16	CLK+	I/O		MIPI CLK lane +
19 GND P GND System ground 20 D1+ I/O MIPI DATA lane 1+ 21 NC NC 22 D1- I/O MIPI DATA lane 1- 23 GND P GND System ground 24 D0+ I/O MIPI DATA lane 0- 25 NC NC 26 D0- I/O MIPI DATA lane 0- 27 GND P GND System ground 28 AVDD P GND System ground 28 AVDD P AVEE Analog power supply 29 AVEE P AVEE Analog power supply 30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P LED positive power1 33 LED2+	17	NC			NC
20 D1+ I/O MIPI DATA lane 1+ 21 NC NC 22 D1- I/O MIPI DATA lane 1- 23 GND P GND System ground 24 D0+ I/O MIPI DATA lane 0+ 25 NC NC 26 D0- I/O MIPI DATA lane 0+ 27 GND P GND System ground 28 AVDD P GND System ground 28 AVDD P AVEE Analog power supply 29 AVEE P AVEE Analog power supply 30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P LED positive power1 33 LED2+ P LED negative power2 34 LED	18	CLK-	I/O		MIPI CLK lane -
21 NC NC 22 D1- I/O MIPI DATA lane 1- 23 GND P GND System ground 24 D0+ I/O MIPI DATA lane 0+ 25 NC NC 26 D0- I/O MIPI DATA lane 0- 27 GND P GND System ground 28 AVDD P GND System ground 28 AVDD P AVEE Analog power supply 29 AVEE P AVEE Analog power supply 30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P LED positive power1 33 LED2+ P LED negative power2 34 LED1- P LED negative power2 36 GN	19	GND	Р	GND	System ground
22 D1- I/O MIPI DATA lane 1- 23 GND P GND System ground 24 D0+ I/O MIPI DATA lane 0+ 25 NC NC 26 D0- I/O MIPI DATA lane 0- 27 GND P GND System ground 28 AVDD P GND System ground 28 AVDD P AVEE Analog power supply 29 AVEE P AVEE Analog power supply 30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P LED positive power1 33 LED2+ P LED negative power2 34 LED1- P LED negative power2 35 LED2- P LED driver PWM 36	20	D1+	I/O		MIPI DATA lane 1+
23 GND P GND System ground 24 D0+ I/O MIPI DATA lane 0+ 25 NC NC 26 D0- I/O MIPI DATA lane 0- 27 GND P GND System ground 28 AVDD P AVDD Analog power supply 29 AVEE P AVEE Analog power supply 30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P LED positive power1 33 LED2+ P LED negative power2 34 LED1- P LED negative power2 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC	21	NC			NC
24 D0+ I/O MIPI DATA lane 0+ 25 NC NC 26 D0- I/O MIPI DATA lane 0- 27 GND P GND System ground 28 AVDD P GND Analog power supply 29 AVEE P AVEE Analog power supply 30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P LED positive power1 33 LED2+ P LED negative power2 34 LED1- P LED negative power1 35 LED2- P LED negative power2 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC	22	D1-	I/O		MIPI DATA lane 1-
24 D0+ I/O MIPI DATA lane 0+ 25 NC NC 26 D0- I/O MIPI DATA lane 0- 27 GND P GND System ground 28 AVDD P GND Analog power supply 29 AVEE P AVEE Analog power supply 30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P LED positive power1 33 LED2+ P LED negative power2 34 LED1- P LED negative power1 35 LED2- P LED negative power2 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC	23	GND	Р	GND	System ground
26 D0- I/O MIPI DATA lane 0- 27 GND P GND System ground 28 AVDD P AVDD Analog power supply 29 AVEE P AVEE Analog power supply 30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P LED positive power1 33 LED2+ P LED negative power2 34 LED1- P LED negative power2 35 LED2- P LED negative power2 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC	24	D0+	I/O		
27 GND P GND System ground 28 AVDD P AVDD Analog power supply 29 AVEE P AVEE Analog power supply 30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P LED positive power1 33 LED2+ P LED positive power2 34 LED1- P LED negative power1 35 LED2- P LED negative power2 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC	25	NC			NC
28 AVDD P AVEE Analog power supply 29 AVEE P AVEE Analog power supply 30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P LED positive power1 33 LED2+ P LED negative power2 34 LED1- P LED negative power1 35 LED2- P LED negative power2 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC	26	D0-	I/O		MIPI DATA lane 0-
AVEE P AVEE Analog power supply 30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P LED positive power1 33 LED2+ P LED negative power2 34 LED1- P LED negative power1 35 LED2- P GND System ground 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC	27	GND	Р	GND	System ground
30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P LED positive power1 33 LED2+ P LED positive power2 34 LED1- P LED negative power1 35 LED2- P LED negative power2 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC	28	AVDD	Р	AVDD	Analog power supply
30 IOVCC P IOVCC I/O power supply 31 GND P GND System ground 32 LED1+ P LED positive power1 33 LED2+ P LED positive power2 34 LED1- P LED negative power1 35 LED2- P LED negative power2 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC	29	AVEE	Р	AVEE	Analog power supply
32 LED1+ P LED positive power1 33 LED2+ P LED positive power2 34 LED1- P LED negative power1 35 LED2- P LED negative power2 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC		IOVCC	Р	IOVCC	I/O power supply
32 LED1+ P LED positive power1 33 LED2+ P LED positive power2 34 LED1- P LED negative power1 35 LED2- P LED negative power2 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC	31	GND	Р	GND	System ground
33 LED2+ P LED positive power2 34 LED1- P LED negative power1 35 LED2- P LED negative power2 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC	32	LED1+	Р		
34 LED1- P LED negative power1 35 LED2- P LED negative power2 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC			Р		• • • • • • • • • • • • • • • • • • • •
35 LED2- P LED negative power2 36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC			Р		<u> </u>
36 GND P GND System ground 37 BLU_PWM O LED driver PWM 38 PWR_EN NC					<u> </u>
37 BLU_PWM O LED driver PWM 38 PWR_EN NC			Р	GND	<u> </u>
38 PWR_EN NC			0		
					NC
					

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I/O definition: I----Input O---Output P----Power(Ground) NC---No connection

Table 3.1 input terminal pin assignments

4. DC ELECTRICAL CHARACTERISTICS

4.1 Absolute maximum ratings

LEDK=GND=0V, Ta = 25°C

Item	Symbol	Min	Max	Unit	Remark
Logic Supply Voltage	IOVCC	1.65	3.6	V	
Analog Supply Voltage	AVDD	4.5	6	V	
Analog Supply Voltage	AVEE	-6	-4.5	V	
Operating Temperature	TOPR	-30	+75	$^{\circ}$	
Storage Temperature	TSTG	-40	+85	°C	

Table 4.1 absolute maximum rating

4.2 Recommended Operating Condition

VCC=2.8V,VIO=1.8V,GND=0V, Ta = 25° C

	Item		Symbol	Min.	Тур.	Max.	Unit	Remark	
Logi	ic Supply	Voltage	IOVCC	1.7	1.8	1.9	V	Note 1	
Analo	og Suppl	y Voltage	AVDD	5.3	5.5	5.7	V	Note 1	
Analo	og Suppl	y Voltage	AVEE	-5.7	-5.5	-5.3	V	Note 1	
Inp	out	Low Level	VIL	GND	-	0.3xIOVCC	V	Note 2	
Signal '	Voltage	High Level	VIH	0.7xIOVCC	-	IOVCC	V	Note 2	
	tput	Low Level	VIL	GND	-	0.2xIOVCC	V	Note 2	
Signal '	Voltage	High Level	VIH	0.8xIOVCC	-	IOVCC	V	Note 2	
Note3	The DC/	AC electrical of	characteris	tics of bare die	and wat	er are guarante	ed at +	85℃ .	
	When the measurements are performed with LCD module, Measurement Points are like below.CSX, RDX, WRX, D[23:0], DCX, RESX, SCL, IM[2:0] and Test pins								
		X, RDX, WRX	, D[23:0], [CL, IM[2	: 0] and Test pi		are like	

Table 4.2 LCD module electrical characteristics

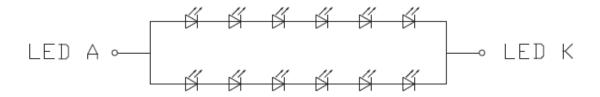


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4.3 Recommended Driving Condition for Backlight



Backlight CIRCUIT DIAGRAM

Figure 4.3 Driving Backlight circuit diagram

	Item	Symbol	Min.	Тур.	Max.	Unit	Remark	
Forw	ard Current	lF	-	20	4	mA	Note 3,4,5	
Forw	ard Voltage	VF	2.8	3.0	3.2	V	Note 3,4,5	
	dight Power	WBL	-	720	768	mW	Note 3,4,5	
Note 3	The figure above	shows the c	onnection	of backlight	LED.			
Note 4	Each LED : IF =2	0 mA, VF = 3	.0V					
Note 5	IF is defined for tw	vo channel L	ED.					
	Optical performan	nce should b	e evaluate	d at Ta=25°	only.			
	If LED is driven by	y high currer	nt, high am	bient temper	rature & hu	midity condit	tion, the life	
	time of LED will be reduced.							
	Operating life mea	ans brightne	ss goes do	own to 50% i	nitial bright	ness. Typica	al operating life	
	time is estimated	data.						

Table 4.3 Driving Condition for Backlight characteristics





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5. AC ELECTRICAL CHARACTERISTICS

5.1 MIPI Interface Characteristics

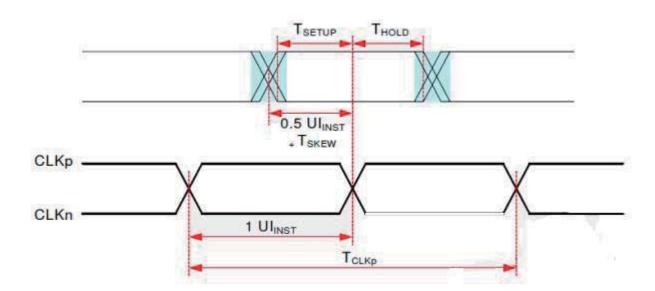


Figure 5.1 MIPI Interface characteristics

	parameter	Symbol	Min.	Тур.	Max.	Units	Remark	
ι	JI instantaneous	UIINST	1	. , , , .	12.5	ns	Note6,7,10	
Data to	Clock Skew [measured at tansmitter]	TSKEW[TX]	-0.15		0.15	UIINST	Note8	
	to Clock Setup Time asured at receiver]	TSETUP[RX]	-0.15			UIINST	Note9	
	to Clock Hold Time asured at receiver]	T HOLD[RX]	-0.15			UIINST	Note9	
20% -	80% rise time and fall	tR / tF	100			Ps		
	time	IK / IF			0.3	UIINST		
Note6	This value corresponds t	o a minimum 80	MHz data	rate				
Note7	The minimum UI shall no data burst.	t be violated for	any single	bit perio	d, i.e.,an	y DDR half	cycle within a	
Note8	Total silicon and package data rate = 1Gbps.	e delay budget o	f 0.3* UIIN	IST wher	D-PHY	is supporti	ng maximum	
Note9	Total setup and hole window for receiver of 0.3* UIINST when D-PHY is supporting maximum data rate = 1Gbps							
Note10	For MIPI speed limitation [1] Per lane bandwidt [2] Total Bit Rate: 2G	h is 850Mbps,	.5Gbps for	6-6-6; 1.	33Gbps	for 5-6-5.		

Table 5.1 MIPI Interface characteristics



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MIPI 24 bits RGB Data Format

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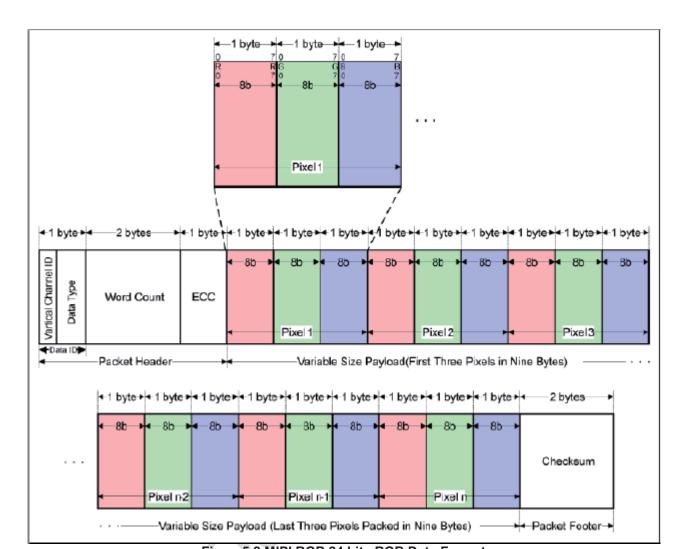


Figure 5.2 MIPI RGB 24 bits RGB Data Format





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5.3 Reset timing

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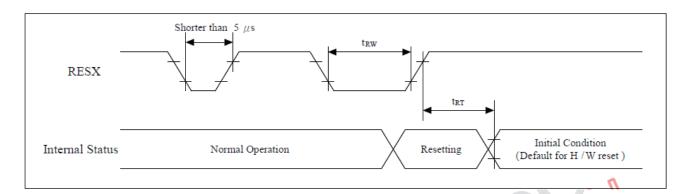


Figure 5.3 Reset Timing

Ta=25°C

Item	Symbol	Min.	Тур.	Max.	Unit	Remark
RESET low pulse width	t _{RW}	10	-	-	us	Note 1
Reset complete time (sleep out mode)	+			10	ms	Note 1
Reset complete time (sleep in mode)	t _{RT}			120	ms	Note 1

Table 5.3 RESET Timing Parameter

Note11:The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 10 ms after a rising edge of RESX.



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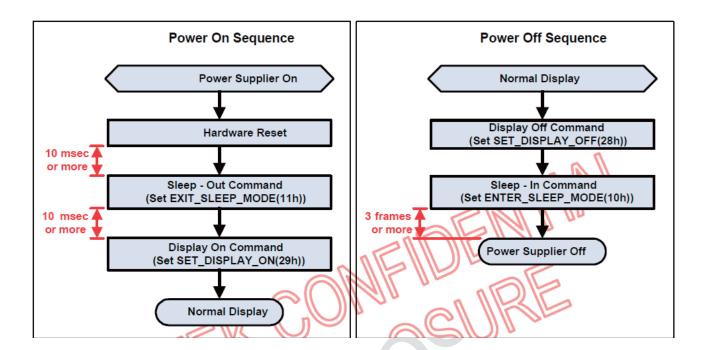


Figure 6.1 Interface power on/off sequence

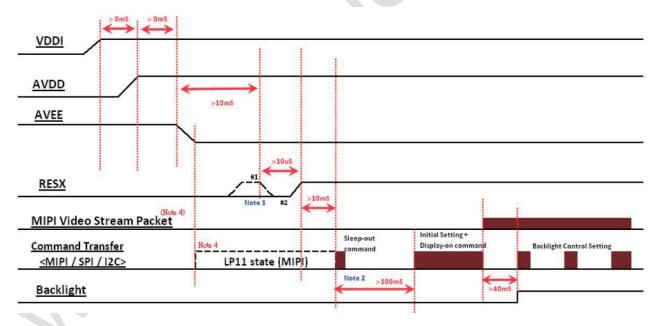


Figure 6. 2 Interface power on/off sequence





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7. Optical Characteristics

7.1 Optical Specification

Ta=25°C

Item	1	Symbol	Condition	Min.	Тур.	Max.	Unit	Remark
\(\tau_{i} \)		θТ		70	80	-		
		θВ	CR≧10	70	80	-	Dograd	Note 2
View Angles		θL	CK=10	70	80	-	Degree	Note 2
		θR		70	80	-		
Contrast Ratio)	CR	θ=0°	800	1000	-		Note1 Note3
		T _{ON}						Note1
Response Tim	ne	T _{OFF}	25℃	-	25	30	ms	Note4
	White	Х		0.275	0.30	0.325		
		у	Backlight is	0.295	0.32	0.345		
	Red	Х		0.61	0.64	0.67		
Chromaticity		у		0.30	0.33	0.36		Note5, Note1
Chilomaticity	Green	Х	on	0.27	0.30	0.33		Note
	Green	У		0.58	0.61	0.64		
	Blue	Х		0.12	0.15	0.18		
	Dide	У		0.03	0.06	0.09		
Uniformity		U		80		-	%	Note1 Note6
NTSC				68	72	-	%	Note 5
Luminance		L		360	450	-	cd/m ²	Note1 Note7

Test Conditions:

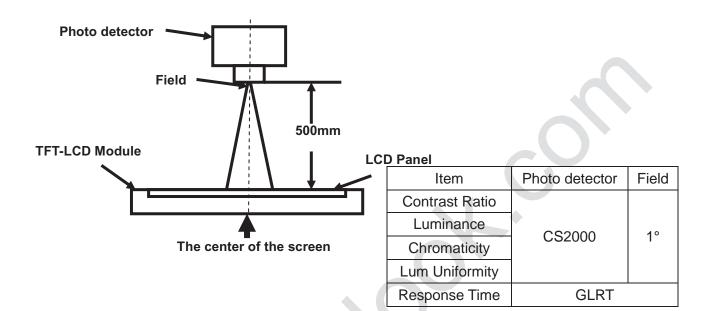
- 1. $V_F = 3.0V$, $1/3*I_F = 20mA$ (Backlight current for each LED), the ambient temperature is 25 °C.
- 2. The test systems refer to Note 1 and Note 2.



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Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system. viewing angle is measured at the center point of the LCD by EZcontrastXL88.

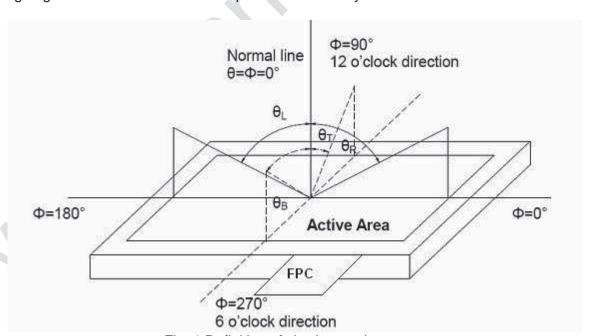


Fig. 1 Definition of viewing angle





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Note 3: Definition of contrast ratio

Luminance measured when LCD is on the "White" state Contrast ratio (CR) = Luminance measured when LCD is on the "Black" state

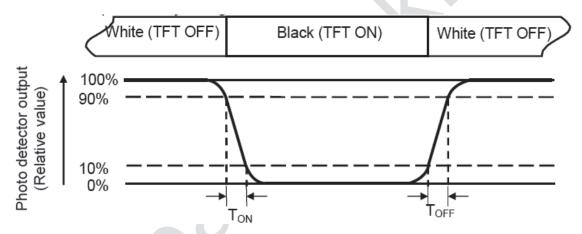
"White state ":The state is that the LCD should be driven by Vwhite.

"Black state": The state is that the LCD should be driven by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.



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Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/Lmax

L----- Active area length W---- Active area width

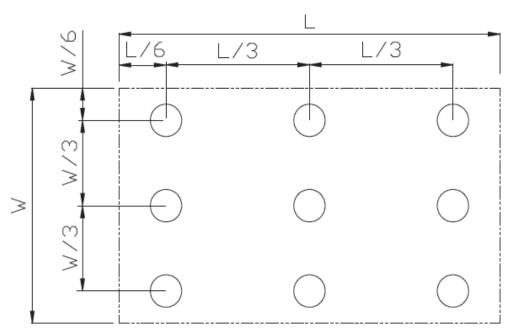


Fig. 2 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.





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8 . Environmental / Reliability Tests

No.	Item	Test Condition	Sample Mumber	Inspection method	Criteria	Remarks	Reference
1	Low Temperature Operation	Ta=-20°C, 48hrs	5				IEC60068-2-1 GB2423.1
2	High Temperature and High Humidity Storage	Ta=+60°C, 90% RH 60 hrs	5	visual and optical inspection after 2hrs in			IEC60068-2-78 GB/T2423.3
3	Thermal Shock storage	-40°C 30 min~+80°C 30 min, Change time:5min, 32Cycles	5	room temperature		start with cold temperature,End with high temperature	IEC60068-2-14 GB2423.22
4	High Temperature Operation	Ts=+70℃, 48hrs	5				IEC60068-2-2 GB2423.2
5	Low Temperature Storage	Ta=-30°C, 24hrs	5				IEC60068-2-1 GB2423.1
6	High Temperature Storage	Ta=+80℃, 24hrs	5		《Reliability Test		IEC60068-2-2 GB2423.2
7	Shock (Non-operation)	60G 6ms, ± X,± Y,± Z 3times, for each direction	2				IEC60068-2-27 GB/T2423.5
8	Electro Static Discharge (Operation)	C=150pF,R=330Ω, 5points/panelContac t: ±4Kv, 5times; Air: ±8Kv, 5times; (Environment: 15°C ~35°C, 30%~60%, 86Kpa~106Kpa)	4	visual inspection after 2hrs in room temperature	Standard»		IEC61000-4-2 GB/T17626.2
9	Vibration (Non-operation)	Frequency range:10~55Hz,Stro ke:1.5mmSweep:10 Hz~55Hz~10Hz 2 hourfor each direction of X.Y.Z.(6 hours for total)(Package condition)	1carton				IEC60068-2-6 GB/T2423
10	Package Drop Test	Height:80 cm 1 corner, 3 edges, 6 surfaces	1carton				IEC60068-2-32 GB/T2423.8

Note1: Ts is the temperature of panel's surface.

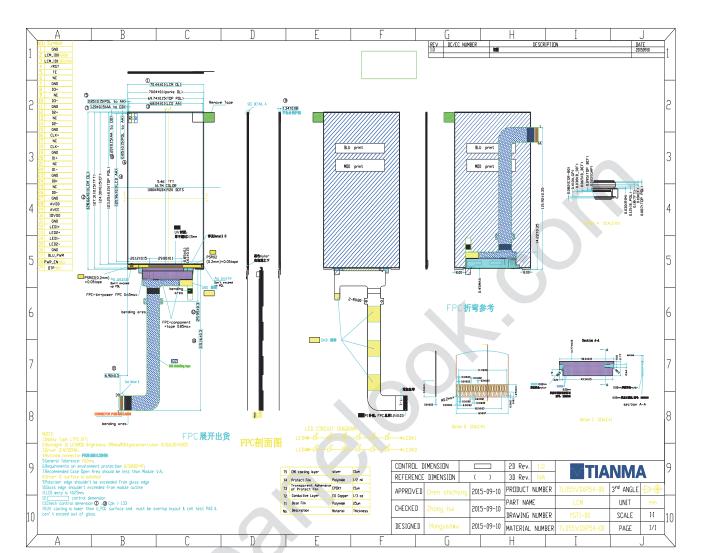
Note2: Ta is the ambient temperature of sample.





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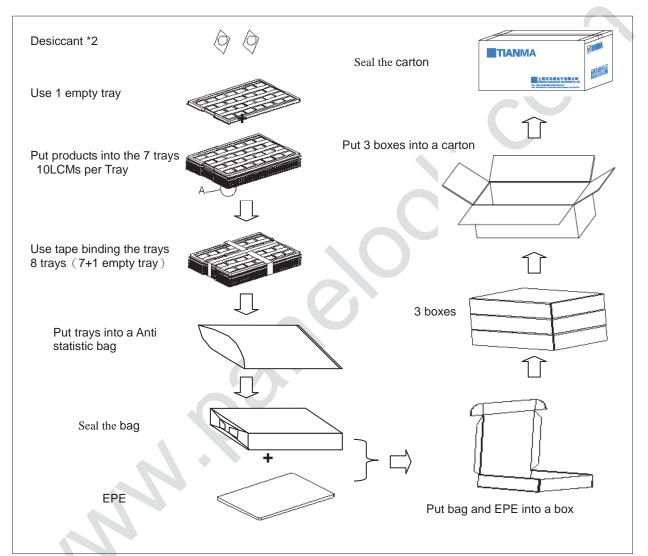
9.Mechanical Drawing



10 . Packing Drawing

No	Item	Model (Material)	Dimensions(mm)	Unit Weight(Kg)	Quantity	Remark
1	LCM module	TL055VDXP43- 0 0	70. 44×128. 66×1. 34	TBD	126	
2	Tray	PET	485×330× 0. 8	TBD	24	
3	EPE	EPE	485×330x5	0.08	3	
4	EPE	EPE	399.5× 248.9 ×1	TBD	21	
5	Anti-statistic bag	PE	450*700*0.08	0. 059	3	

V	XIAMEN TIANMA MICRO-ELECTRONICS			TL055VDXP		
6	вох	CORRUGATED PAPER	520×345×74	0.44	3	
7	Desiccant	DESICCANT	45×35 (2g)	0. 002	6	12g
8	Carton	CORRUGATED PAPER	544×365×250	1.01	1	
9	Total weight			TBD Kg		



11 Precautions for Use of LCD Modules

11.1 Handling Precautions

- 11.1.1The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- 11.1.2If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not

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- to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
- 11.1.3Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- 11.1.4The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- 11.1.5If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:
- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents
 - 11.1.6Do not attempt to disassemble the LCD Module.
 - 11.1.7 If the logic circuit power is off, do not apply the input signals.
 - 11.1.8To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
 - 11.1.8.1 Be sure to ground the body when handling the LCD Modules.
 - 11.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.
 - 11.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
 - 11.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.
- 11.2 Storage precautions
 - 11.2.1When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.
 - 11.2.2The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:
- Temperature : 0° C $\sim 40^{\circ}$ C Relatively humidity: $\leq 80\%$
 - 11.2.3The LCD modules should be stored in the room without acid, alkali and harmful gas.
- 11.3 Transportation Precautions:

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.