

TFT COLOR LCD MODULE
NL10276AC28-02

**36 cm (14.1 inches), 1,024 × 768 pixels, Full-color,
Multi-scan function, Built-in backlight with inverter
Ultra wide viewing angle**

DESCRIPTION

NL10276AC28-02 is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL10276AC28-02 has a built-in backlight with an inverter.

The 36cm (14.1 inches) diagonal display area contains 1,024 × 768 pixels and can display full-color (more than 16 million colors simultaneously). Furthermore, it has also wide viewing angle and multi-scan function. Therefore, NEC calls this modules Super Fine TFT.

FEATURES

- Ultra wide viewing angle
- High luminance and Low reflection
- Analog RGB signals
- Multi-scan function: e.g., XGA, SVGA, VGA, VGA-TEXT, PC-9801, MAC
- Built-in edge-light type backlight (Four lamps into two lamp holders, Inverter)
- Lamp holder replaceable (Part No.: 141LHS-2)

APPLICATIONS

- Engineering workstation(EWS), Desk-top type of PC
- Display terminals for control system
- Monitors for process controller



The information in this document is subject to change without notice.

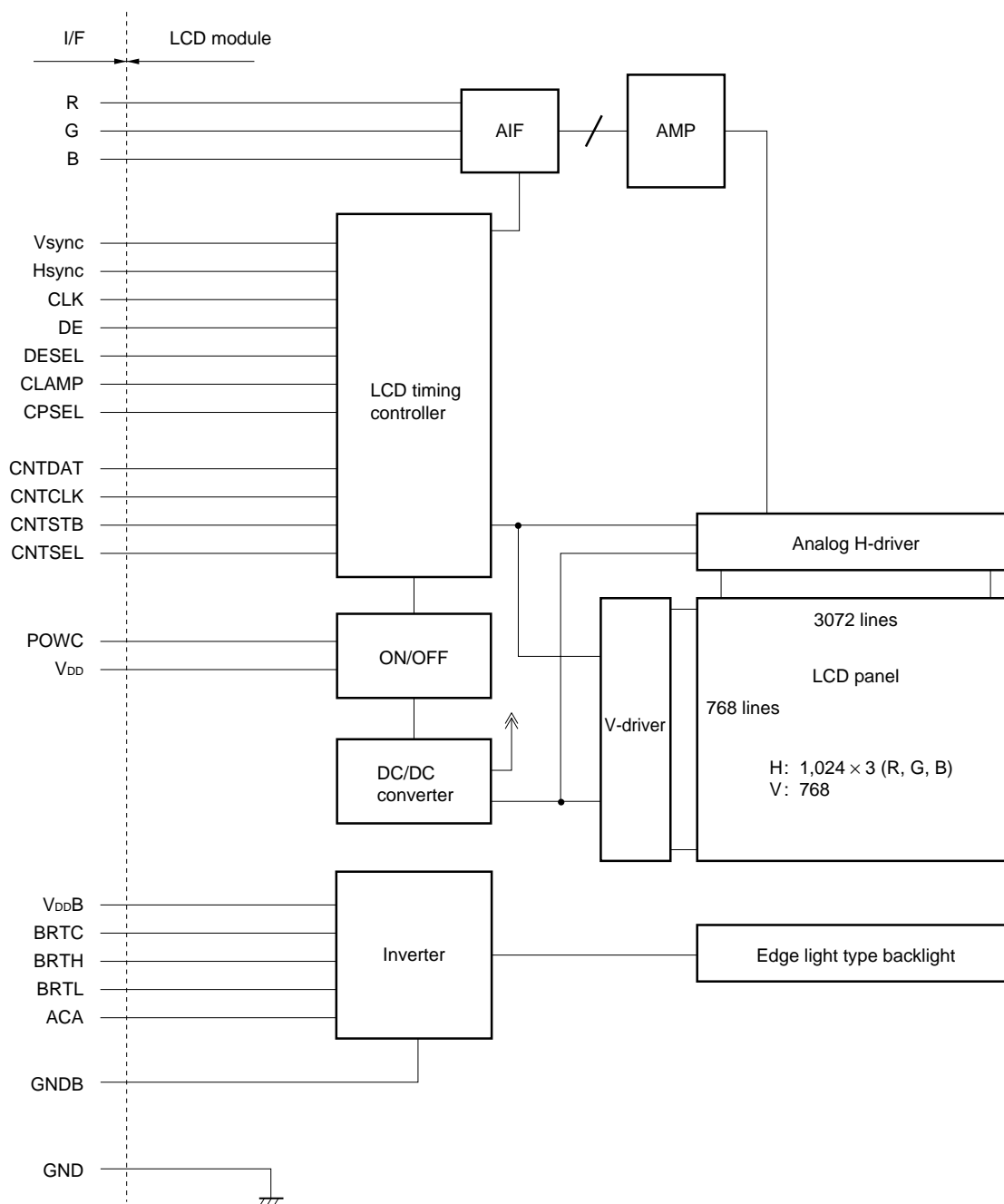
STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT panel structure is created by sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

BLOCK DIAGRAM



Remark Frame is not connected to GND and GNDB.

OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	285.696 (H) × 214.272 (V) mm
Drive system	a-Si TFT active matrix
Display colors	Full-color
Number of pixels	1,024 × 768
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.279 (H) × 0.279 (V) mm
Module size	330.0 (H) × 255.0 (V) × 25.0 (TYP.) (D) mm
Weight	1,495 g (TYP.)
Contrast ratio	150 : 1 (TYP.)
Viewing angle (more than the contrast ratio of 10 : 1)	<ul style="list-style-type: none">• Horizontal : 80° (TYP., left side, right side)• Vertical: 80° (TYP., up side), 70° (TYP., down side)
Designed viewing direction	Optimum grayscale ($\gamma = 2.2$): perpendicular
Color gamut	40% (TYP., center, To NTSC)
Response time	35 ms (TYP.), black to white
Luminance	200 cd/m ² (TYP.)
Signal system	Analog RGB signals, Synchronous signals (Hsync, Vsync), Dot clock (CLK)
Supply voltages	12 V, 12 V (Logic/LCD driving, Backlight)
Backlight	Edge light type: Four cold cathode fluorescent lamps with an inverter
Power consumption	22 W (TYP.)

GENERAL SPECIFICATIONS

Item	Specification	Unit
Module size	330.0 ± 0.5 (H) × 255.0 ± 0.5 (V) × 26.0 (MAX.) (D)	mm
Display area	285.696 (H) × 214.272 (V)	mm
Number of dots	1,024 × 3 (H) × 768 (V)	dot
Number of pixels	1,024 (H) × 768 (V)	pixel
Dot pitch	0.093 (H) × 0.279 (V)	mm
Pixel pitch	0.279 (H) × 0.279 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	—
Display colors	full-color	color
Weight	1,550 (MAX.)	g

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit	Remarks	
Supply voltage	V _{DD} B	−0.3 to +14	V	T _a = 25°C	
	V _{DD}	−0.3 to +14	V		
Logic input voltage	V _{IN1}	−0.3 to +5.5	V	T _a = 25°C V _{DD} = 12 V	
R,G,B input voltage	V _{IN2}	−6.0 to +6.0	V		
CLK input voltage	V _{IN3}	−7.0 to +7.0	V		
BRTL input voltage	V _{IN4}	−0.3 to +1.5	V		
Storage temp.	T _{ST}	−20 to + 60	°C		
Operating temp.	T _{OP}	0 to 50	°C	Module surface Note	
Humidity	—	≤ 95% relative humidity	—	T _a ≤ 40°C	No condensation
	—	≤ 85% relative humidity	—	40°C < T _a ≤ 50°C	
	—	≤ (T _a = 50°C, 85% relative humidity) Absolute humidity	—	T _a > 50°C	

Note Measured at the display area

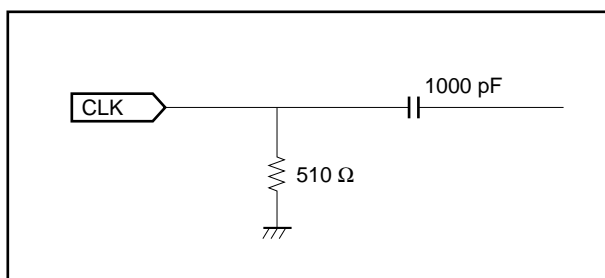
ELECTRICAL CHARACTERISTICS

T_a = 25°C

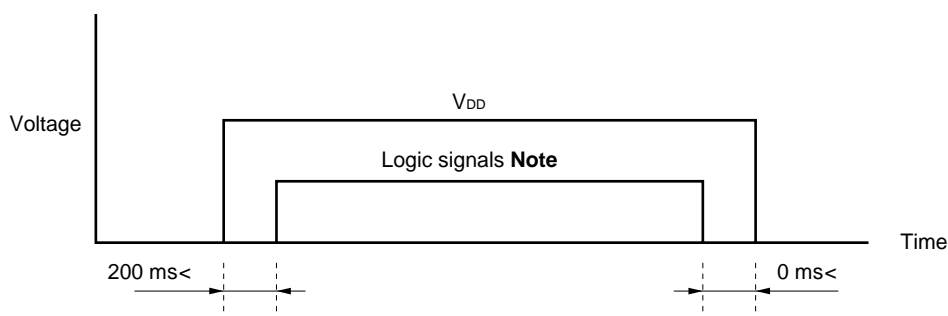
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Supply voltage	V _{DDB}	11.4	12.0	12.6	V	for backlight
	V _{DD}	11.4	12.0	12.6	V	for logic and LCD driving
Logic input Low voltage	V _{IL}	0	–	0.8	V	TTL level
Logic input High voltage	V _{IH}	2.2	–	5.25	V	
CLK input voltage	V _{ICLK}	0.6	–	1.0	V _{p-p}	for CLK
CLK DC input level	V _{IDCLK}	–4.5	–	+4.5	V	
Logic input Low current 1	I _{IL1}	–1,080	–	–	μA	for CNTSEL, CPSEL and POWC
Logic input High current 1	I _{IH1}	–	–	10	μA	
Logic input Low current 2	I _{IL2}	–260	–	–	μA	for BRTC
Logic input High current 2	I _{IH2}	–	–	820	μA	
Logic input Low current 3	I _{IL3}	–500	–	–	μA	for ACA
Logic input High current 3	I _{IH3}	–	–	340	μA	
Logic input Low current 4	I _{IL4}	–10	–	–	μA	for except above terminals
Logic input High current 4	I _{IH4}	–	–	130	μA	
Maximum amplitude (white-black)	V _{IRGB}	0 (black)	–	0.7 (white)	V _{p-p}	RGB input
DC input level (black)	V _{IDCRGB}	–3.5	–	+3.5	V	
Supply current	I _{DDBp}	–	–	4,000	mA	V _{DDB} = 12.0 V
	T _{lDDBp}	–	–	4	ms	
Supply current Note	I _{DD}	–	530	800	mA	V _{DD} = 12.0 V
	I _{DDB}	–	1,300	1,600	mA	V _{DDB} = 12.0 V (MAX. luminance)

Note Checkered flag pattern

CLK input equivalent circuit



SUPPLY VOLTAGE SEQUENCE



Caution Wrong power sequence may damage to the module.

Note Synchronous signal, Control signals

- (1) Logic signals (synchronous signals and control signals) should be "0" voltage (V), when V_{DD} is not input. If higher than 0.3 V is input to signal lines, the internal circuit will be damaged.
- (2) LCD module will shut down the power supply of driving voltage to LCD panel internally, when one of CLK, Hsync, Vsync, DE (at DE mode) is not input more than 90 ms typically. As the display data are unstable in this period, the display is disordered. But the backlight works correctly event this period. So the backlight ON/OFF should be controlled by BRTC signal.
- (3) The ON/OFF (BRTC signal) should be controlled while logic signals are supplied. The backlight power supply (V_{DDB}) is not related to the power supply sequence. However, unstable data will be displayed when the backlight power is turned ON/OFF with no logic signals.
- (4) Keep POWC signal Low more than 200 ms after the power supply (V_{DD}) is input, if POWC signal is controlled.
- (5) Analog RGB input are independent from this power supply sequence.

INTERFACE AND PIN CONNECTION

(1) Interface signals, power supply

CN1

Part No. : MRF03-6R-SMT

Adaptable socket : MRF03-2 × 6P-1.27 (For cable type) or MRF03-6PR-SMT (For board to board type)

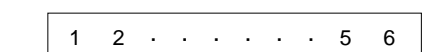
Supplier : HIROSE ELECTRIC CO., LTD. (coaxial type)

Coaxial cable **Note** : UL20537PF75VLAS

Supplier : HITACHI CO., LTD.

Pin No.	Symbol	Pin No.	Symbol
1	B	4	Vsync
2	G	5	Hsync
3	R	6	CLK

Figure from socket view



Note A coaxial cable shield should be connected with GND.

CN2

Part No. : IL-Z-12PL1-SMTY

Adaptable socket : IL-Z-12S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	V _{DD}	7	N.C. Note
2	V _{DD}	8	N.C. Note
3	GND	9	DESEL
4	GND	10	GND
5	POWC	11	GND
6	GND	12	DE

Figure from socket view

12	11	2	1
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Note N.C. (No connection) should be open.

CN3

Part No. : IL-Z-11PL1-SMTY

Adaptable socket : IL-Z-11S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	V _{DD} B	7	ACA
2	V _{DD} B	8	BRTC
3	V _{DD} B	9	BRTH
4	GNDB	10	BRTL
5	GNDB	11	N.C. Note
6	GNDB		

Figure from socket view

11	10	2	1
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Note N.C. (No connection) should be open.

CN4

Part No. : IL-Z-13PL1-SMTY

Adaptable socket : IL-Z-13S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	GND	8	CLAMP
2	CNTSEL	9	GND
3	CNTDAT	10	N.C. Note
4	CNTSTB	11	GND
5	GND	12	N.C. Note
6	CNTCLK	13	GND
7	CPSEL		

Figure from socket view

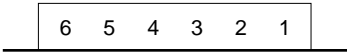
13	12	2	1
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Note N.C. (No connection) should be open.

CN5
Part No. : IL-Z-6PL-SMTY
Adaptable socket : IL-Z-6S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	GNDB	4	BRTC
2	GNDB	5	BRTH
3	ACA	6	BRTL

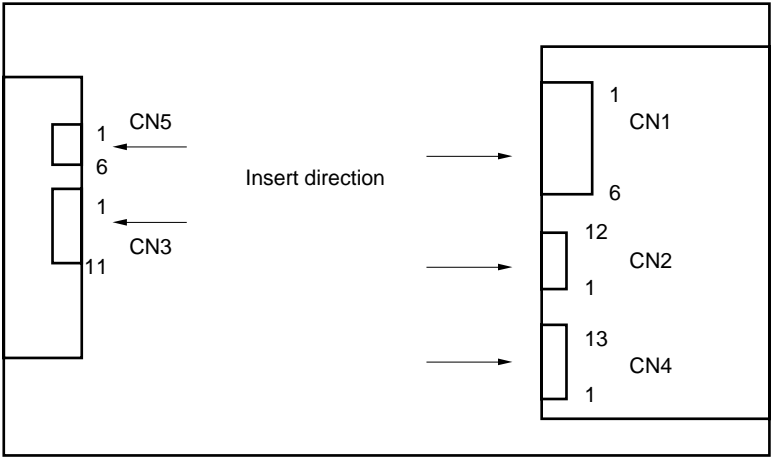
Figure from socket view



Note CN5 should be open in case of CN3 is used.

<Connector location>

Rear view



(2) Pin function

Symbol	I/O	Logic	Description
CLK	Input	Negative	Dot clock input (ECL level). This timing-signal is for display data.
Hsync	Input	Negative	Horizontal synchronous signal input (TTL level)
Vsync	Input	Negative	Vertical synchronous signal input (TTL level)
R	Input	–	Red video signal input (0.7 Vp-p, 75 Ω)
G	Input	–	Green video signal input (0.7 Vp-p, 75 Ω)
B	Input	–	Blue video signal input (0.7 Vp-p, 75 Ω)
POWC	Input	Positive	Power control signal (TTL level) High or open : Logic and LCD power are on. Low : Logic and LCD power are off. When POWC is Low, serial communication data is clear. Please set again Note1 .
DESEL	Input	Positive	DE function select signal (TTL level) High: DE mode, Low or open: Fixed mode
DE	Input	Positive	Data enable signal input (TTL level) 1. Back-porch becomes free, when DESEL is High. 2. Back-porch becomes fix, when DESEL is Low. Then DE should be fixed High or Low.
CNTSEL	Input	–	Display control signal in case of serial communications (TTL level) High or open: Default, Low: External control Serial communications are set up by external control.
CNTDAT	Input	Positive	Display control data (TTL level) Detail of CNTDAT is mentioned in STATUS READ FUNCTIONS .
CNTCLK	Input	Positive	CLK for display control data (TTL level) Detail of CNTDAT is mentioned in STATUS READ FUNCTIONS .
CNTSTB	Input	Positive	Latch pulse for display control data (TTL level) Detail of CNTDAT is mentioned in STATUS READ FUNCTIONS .
CPSEL	Input	–	Clamp signal function select signal High or open: Default, Low: External control
CLAMP	Input	Negative	Clamp timing signal of black level (TTL level) This mode works in CPSEL = Low
ACA	Input	Positive	Luminance control signal (TTL level) High or open : Normal luminance Low : Low luminance (1/2 of normal luminance)
BRTC	Input	Positive	Backlight ON/OFF control signal (TTL level) High or open: Backlight ON, Low: Backlight OFF
BRTH	Input	–	Variable resistor control Note2 or Voltage control Note3
BRTL	Input	–	
V _{DD}	–	–	Power supply for Logic and LCD driving, +12 V (±5 %)
V _{DD} B	–	–	Power supply for backlight, +12 V (±5 %)
GND	–	–	Signal ground for Logic and LCD driving (Connect to a system ground)
GNDB	–	–	Ground for backlight. GNDB is not connected to the frame ground of LCD module.

- Notes 1.** When POWC is “Low” logic input signal should be all “0 V”. If the signal is more than “0.3 V”, inside circuits of the LCD module may be broken.
- 2.** The variable resistor for luminance control should be 10 k Ω type, and zero point of the resistor correspond to the minimum of luminance.



Mating Variable Resistor: 10 k Ω ±5 %, B curve

- 3.** If luminance is controlled by BRTM/BRTL input voltage, at first BRTM is “0 V”, and BRTL input voltage controls brightness. When BRTL input voltage is “1 V” the luminance become maximum, and when BRTL input voltage is “0 V”, the luminance becomes minimum.

STATUS READ FUNCTIONS

This LCD module has following functions by serial data input (See **CNTDAT COMPOSITION**)

- (1) Expansion mode : See **table 1 and EXPANSION FUNCTION**
- (2) Display position control (Vertical) : See **table 2**
- (3) Display position control (Horizontal) : See **table 5**
- (4) CLK delay control : See **table 3**
- (5) CLK fall/rise synchronous change : See **table 4**

Set up the following items to work the above functions

- (A) CLK counts of horizontal period : See **table 6**
- (B) CLK frequency range : See **table 7**

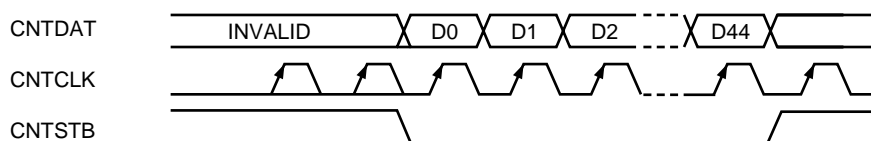
If CNTSEL is Low, the above functions are valid (CNTSEL is High or open, default values are valid.). After serial data are transferred, the data is latched by CNTSTB. Once, the data is latched, the above functions are effective.

Please keep CNTSTB to be Low during transferring data. Input data can be changed during power on, but LCD display may be disturbed. When the serial data are changed, we recommend that the backlight power is off using BRTC function.

SERIAL COMMUNICATION TIMING AND WAVEFORM

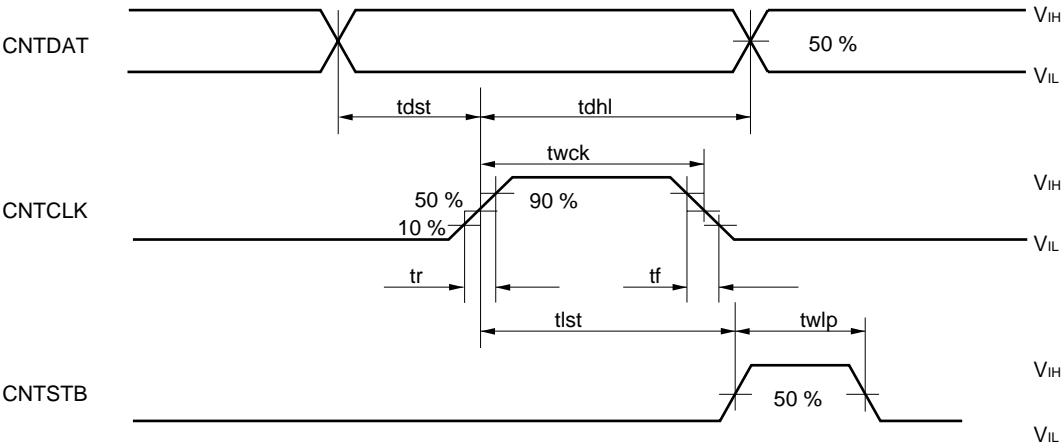
This LCD module can be read the following status data.

Serial Communication Timing



Parameter	Symbol	MIN.	MAX.	Unit	Remark
CLK pulse-width	twck	50	—	ns	CNTCLK
CLK frequency	fclk	—	5	MHz	
DATA set-up-time	tdst	50	—	ns	CNTDAT
DATA hold-time	tdhl	50	—	ns	
Latch pulse-width	twlp	50	—	ns	CNTSTB
Latch set-up time	tlst	50	—	ns	
Rise/fall time	tr, tf	—	50	ns	CNT xxx

Serial Communication Waveform



CNTDATA COMPOSITION

DATA	DATA name	Function	Remark
D0	VEX3	Expansion mode	See table 1.
D1	VEX2	Expansion mode	
D2	VEX1	Expansion mode	
D3	VEX0	Expansion mode	
D4	VD10	Display position control (Vertical) (MSB)	See table 2.
D5	VD9	Display position control (Vertical)	
D6	VD8	Display position control (Vertical)	
D7	VD7	Display position control (Vertical)	
D8	VD6	Display position control (Vertical)	
D9	VD5	Display position control (Vertical)	
D10	VD4	Display position control (Vertical)	
D11	VD3	Display position control (Vertical)	
D12	VD2	Display position control (Vertical)	
D13	VD1	Display position control (Vertical)	
D14	VD0	Display position control (Vertical) (LSB)	
D15	DELAY6	CLK delay control (MSB)	See table 3.
D16	DELAY5	CLK delay control	
D17	DELAY4	CLK delay control	
D18	DELAY3	CLK delay control	
D19	DELAY2	CLK delay control	
D20	DELAY1	CLK delay control	
D21	DELAY0	CLK delay control (LSB)	
D22	CKS	CLK fall/rise synchronous charge	See table 4.
D23	HD8	Display position control (Horizontal) (MSB)	See table 5.
D24	HD7	Display position control (Horizontal)	
D25	HD6	Display position control (Horizontal)	
D26	HD5	Display position control (Horizontal)	
D27	HD4	Display position control (Horizontal)	
D28	HD3	Display position control (Horizontal)	
D29	HD2	Display position control (Horizontal)	
D30	HD1	Display position control (Horizontal)	
D31	HD0	Display position control (Horizontal) (LSB)	
D32	HSE10	CLK counts of horizontal period (MSB)	See table 6.
D33	HSE9	CLK counts of horizontal period	
D34	HSE8	CLK counts of horizontal period	
D35	HSE7	CLK counts of horizontal period	
D36	HSE6	CLK counts of horizontal period	
D37	HSE5	CLK counts of horizontal period	
D38	HSE4	CLK counts of horizontal period	
D39	HSE3	CLK counts of horizontal period	
D40	HSE2	CLK counts of horizontal period	
D41	HSE1	CLK counts of horizontal period	
D42	HSE0	CLK counts of horizontal period (LSB)	
D43	MOD1	CLK frequency range	See table 7.
D44	MOD0	CLK frequency range	

Table 1. Expansion mode (VEX3 to VEX0: 4 bits)

VEX3	VEX2	VEX1	VEX0	Vertical magnification	Display mode	Display image
0	0	0	0	1	XGA	Standard Note
0	0	0	1	1.25	SVGA	See Expansion Function (3) Display Image .
0	0	1	0	1.6	PC98, VGA, VGA text	
0	0	1	1	—	Prohibit	
0	1	0	0	—	Prohibit	
0	1	0	1	—	Prohibit	
0	1	1	0	—	Prohibit	
0	1	1	1	—	Prohibit	
1	0	0	0	—	Prohibit	
1	0	0	1	1.2	832 × 624 (MAC)	
1	0	1	0	—	Prohibit	
1	0	1	1	—	Prohibit	
1	1	0	0	—	Prohibit	
1	1	0	1	—	Prohibit	
1	1	1	0	—	Prohibit	
1	1	1	1	—	Prohibit	

Note When CNTSEL is High or open, display mode is XGA.

Table 2. Display position control (Vertical) (VD10 to VD0: 11 bits)

VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Vertical position [H] Note 1
0	0	0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	0	0	1	Prohibit
0	0	0	0	0	0	0	0	0	1	0	Prohibit
0	0	0	0	0	0	0	0	0	1	1	Prohibit
0	0	0	0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	0	0	1	0	1	5
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047 Note 2

Notes 1. This is horizontal line number for effective VIDEO signal from Vsync-fall.

2. The maximum vertical position is Vsync total.

Remark When CNTSEL is High or open, vertical position is fixed at 35 [H].

Table 3. CLK delay control (DELAY6 to DELAY0: 7 bits)

DELAY [6..0]	Delay Note	Unit	DELAY [6..0]	Delay Note	Unit	DELAY [6..0]	Delay Note	Unit
00H	7.0	ns	2BH	32.8	ns	56H	57.9	ns
01H	7.6	ns	2CH	33.3	ns	57H	58.5	ns
02H	8.2	ns	2DH	33.9	ns	58H	59.2	ns
03H	8.8	ns	2EH	33.4	ns	59H	59.8	ns
04H	9.4	ns	2FH	35.1	ns	5AH	60.4	ns
05H	10.0	ns	30H	35.6	ns	5BH	61.1	ns
06H	10.5	ns	31H	36.1	ns	5CH	61.6	ns
07H	11.2	ns	32H	36.8	ns	5DH	62.2	ns
08H	11.8	ns	33H	37.5	ns	5EH	62.7	ns
09H	12.4	ns	34H	37.9	ns	5FH	63.3	ns
0AH	13.0	ns	35H	38.5	ns	60H	64.0	ns
0BH	13.7	ns	36H	39.1	ns	61H	64.7	ns
0CH	14.2	ns	37H	39.7	ns	62H	65.3	ns
0DH	14.8	ns	38H	40.4	ns	63H	66.0	ns
0EH	15.3	ns	39H	41.0	ns	64H	66.5	ns
0FH	15.9	ns	3AH	41.5	ns	65H	67.1	ns
10H	16.6	ns	3BH	42.1	ns	66H	67.7	ns
11H	17.2	ns	3CH	42.6	ns	67H	68.3	ns
12H	17.8	ns	3DH	43.2	ns	68H	68.9	ns
13H	18.4	ns	3EH	43.8	ns	69H	69.5	ns
14H	18.9	ns	3FH	44.4	ns	6AH	70.1	ns
15H	19.5	ns	40H	45.0	ns	6BH	70.7	ns
16H	20.1	ns	41H	45.6	ns	6CH	71.2	ns
17H	20.7	ns	42H	46.2	ns	6DH	71.9	ns
18H	21.4	ns	43H	46.8	ns	6EH	72.4	ns
19H	22.0	ns	44H	47.3	ns	6FH	73.1	ns
1AH	22.6	ns	45H	47.8	ns	70H	73.6	ns
1BH	23.2	ns	46H	48.4	ns	71H	74.2	ns
1CH	23.8	ns	47H	49.0	ns	72H	74.8	ns
1DH	24.4	ns	48H	49.6	ns	73H	75.4	ns
1EH	24.9	ns	49H	50.2	ns	74H	75.9	ns
1FH	25.6	ns	4AH	50.8	ns	75H	76.5	ns
20H	26.3	ns	4BH	51.4	ns	76H	77.0	ns
21H	26.9	ns	4CH	51.9	ns	77H	77.7	ns
22H	27.4	ns	4DH	52.6	ns	78H	78.3	ns
23H	28.1	ns	4EH	53.1	ns	79H	79.0	ns
24H	28.5	ns	4FH	53.7	ns	7AH	79.6	ns
25H	29.1	ns	50H	54.5	ns	7BH	80.2	ns
26H	29.7	ns	51H	55.0	ns	7CH	80.8	ns
27H	30.3	ns	52H	55.6	ns	7DH	81.4	ns
28H	31.0	ns	53H	56.3	ns	7EH	81.9	ns
29H	31.6	ns	54H	56.8	ns	7FH	82.5	ns
2AH	32.2	ns	55H	57.4	ns			

Note This delay value is typical value at $T_a = 25^\circ\text{C}$. And the value varies by the ambient temperature and the module itself.

Please set up a preferable display position. See the following references.

<1> Variation of CLK delay by temperature drift (for reference). The temperature constant of CLK delay is $0.2\% / ^\circ\text{C}$.

Calculated example:

In case of delay time is 20 ns at $T_a = 25^\circ\text{C}$;

(a) In case T_a rising to 50°C .

Increase of delay time $\rightarrow (50^\circ\text{C} - 25^\circ\text{C}) \times 0.002 \times 20\text{ ns} = +1\text{ ns}$

So, the total delay time is 21 ns at $T_a = 50^\circ\text{C}$.

(b) In case T_a falling to 0°C .

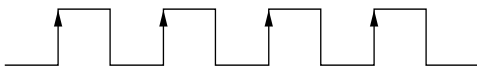
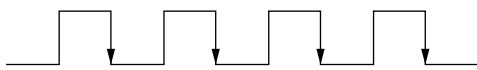
Decrease of delay time $\rightarrow (0^\circ\text{C} - 25^\circ\text{C}) \times 0.002 \times 20\text{ ns} = -1\text{ ns}$

So, the total delay time is 19 ns at $T_a = 0^\circ\text{C}$.

<2> Variation of CLK delay time against each LCD module (for reference).
 -10.5% to $+14.4\%$

	MOD setting			
	0, 0	0, 1	1, 0	1, 1
The upper limit of CLK delay; DELAY [6..0]	Prohibit	59H	6BH	7FH

Table 4. Clock fall/rise synchronous change

CKS	Function
0	DATA is sampled on rising edge of CLK 
1	DATA is sampled on falling edge of CLK 

Remark When CNTSEL is High or open, CKS is "0".

Table 5. Display position control (Horizontal) (HD8 to HD0: 9 bits)

HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal position [CLK] Note
0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	1	Prohibit
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
0	0	1	1	1	1	1	1	1	Prohibit
0	1	0	0	0	0	0	0	0	64
0	1	0	0	0	0	0	0	1	65
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	0	1	509
1	1	1	1	1	1	1	1	0	510
1	1	1	1	1	1	1	1	1	511

Note This is CLK number from Hsync-fall to effecting VIDEO signal.

Remark When CNTSEL is High or open, Horizontal position is set at 296 [CLK].

Table 6. CLK counts of horizontal period (HSE10 to HSE0: 11 bits)

HSE10	HSE 9	HSE 8	HSE 7	HSE 6	HSE 5	HSE 4	HSE 3	HSE 2	HSE 1	HSE 0	CLK count Note
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	0	1	2,045
1	1	1	1	1	1	1	1	1	1	0	2,046
1	1	1	1	1	1	1	1	1	1	1	2,047

Note This is CLK number from Hsync to next Hsync.

- Remarks**
1. When CNTSEL is High or open, CLK count is set at 1344 [CLK].
 2. This CLK count must be equal to CLK count of input signal.

Table 7. CLK frequency select (MOD1 to MOD0: 2 bits)

MOD1	MOD0	CLK frequency [MHz]
0	0	Prohibit
0	1	65 to 79
1	0	50 to 65
1	1	20 to 50

- Remarks**
1. Set up the MOD1 and MOD0 complying with input CLK frequency.
 2. When CNTSEL is High or open, CLK frequency is set 65 to 79 MHz.

EXPANSION FUNCTION

(1) Expansion mode

Expansion mode is a function to expand screen. For example, VGA signal has 640×480 pixels. But, if the display data can be expanded to 1.6 times vertically and horizontally, VGA screen image can be displayed fully on the screen of XGA resolution.

This LCD module has the function of expanding vertical direction as shown in **Table 1**. And expanding horizontal direction is possible by setting input CLK frequency which is equivalent to the magnification. It is necessary to make this CLK outside of this LCD module.

The below image is display example, when DE function is default and HD and VD is set to most suitable frequency. And when DE function is used, HD and VD become default. Adjustment the display to the best position by DE signal.

Please adopt this mode after evaluating display quality, because the appearance of expansion mode is happened to become bad some cases.

The followings show the display magnifications for each mode.

Input display	Number of pixels	Magnification	
		Vertical	Horizontal Note
XGA	1024×768	1	1
SVGA	800×600	1.25	1.25
VGA	640×480	1.6	1.6
VGA text	720×400	1.6	1.4
PC9801	640×400	1.6	1.6
MAC	832×624	1.2	1.2

Note The horizontal magnification multiplies the input clock (CLK).

Input CLK = system CLK \times horizontal magnification

Example In case of XGA and VGA, CLK frequency can be decided as follows.

XGA: (system CLK (65 MHz)) \times 1.0 = 65 MHz

VGA: (system CLK (25.175 MHz)) \times 1.6 = 40.28 MHz

(2) Auto recognition data

Input signal									Module serial data setting		
Mode	System Video CLK [MHz]	Input CLK Calculation formula	Hsync [kHz]	Vsync [Hz]	Horizontal		Vertical		HSE	HD Note2	VD Note2
					Count number [CLK]	DSP Note [CLK]	Count number [H]	DSP Note [H]	Calculation formula		
	(A)	$(A) \times \text{Hor. mag}$			(B)	(C)	—	(D)	$(B) \times \text{Hor. mag.}$	$(C) \times \text{Hor. mag.}$	$= (D)$
XGA (1024 × 768)	65	$(A) \times 1$	48.363	60.004	1,344	296	806	35	$(B) \times 1$	$(C) \times 1$	$= (D)$
	75		56.476	70.069	1,328	280	806	35			
	78.75		60.023	75.029	1,312	272	800	31			
MAC (832 × 624)	57.283	$(A) \times 1.2$	49.725	74.5	1,152	288	667	42	$(B) \times 1.2$	$(C) \times 1.2$	
SVGA (800 × 600)	36	$(A) \times 1.25$	35.156	56.25	1,024	200	625	24	$(B) \times 1.25$	$(C) \times 1.25$	
	40		37.879	60.317	1,056	216	628	27			
	50		48.077	72.188	1,040	184	666	29			
	49.5		46.875	75	1,056	240	666	24			
VGA (640 × 480)	25.175	$(A) \times 1.6$	31.469	59.94	800	144	525	35	$(B) \times 1.6$	$(C) \times 1.6$	
	31.5		37.861	72.809	832	168	520	31			
	31.5		37.5	75	840	184	500	19			
	30.24		35.0	66.667	864	160	525	42			
VGA text (720 × 400)	28.322	$(A) \times 1.4$	31.469	70.087	900	153	449	37	$(B) \times 1.4$	$(C) \times 1.4$	
	35.5		37.927	85.04	936	180	446	45			
PC9801 (640 × 400)	21.053	$(A) \times 1.6$	24.827	56.432	848	144	440	33	$(B) \times 1.6$	$(C) \times 1.6$	443

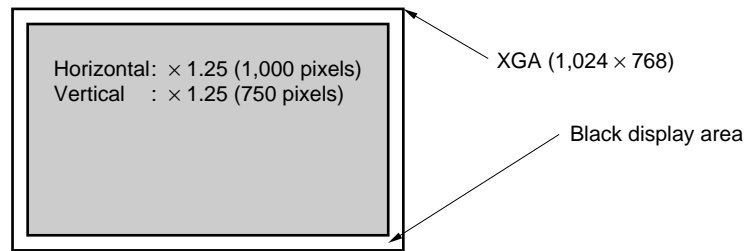
Notes 1. DSP = Display Start Period, DSP is total of “pulse-width” and “back-porch”.

2. HD and VD are approximate value. Set HD and VD in case of adjusting display to the screen center.

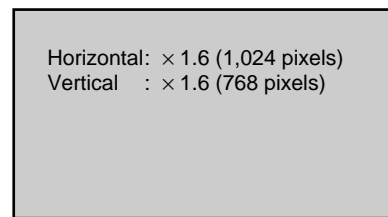
Remark The pulse-width of Hsync, Vsync and back-porch are the same as XGA-mode (Standard mode).

(3) Display Image

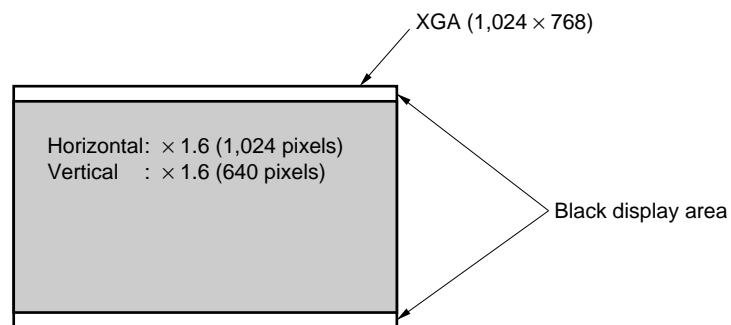
1. SVGA mode (800 × 600)



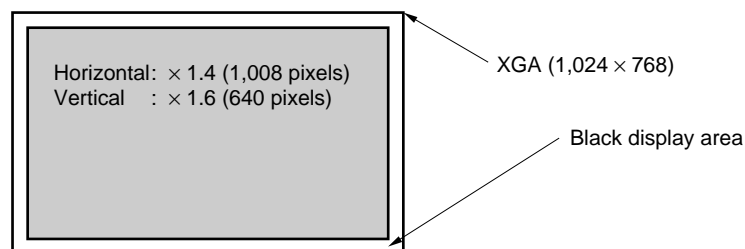
2. VGA mode (640 × 480)



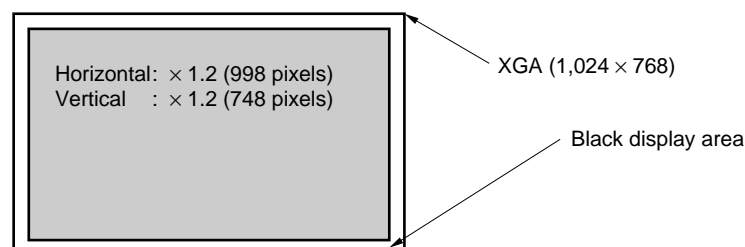
3. PC9801 mode (640 × 400)



4. VGA text mode (720 × 400)



5. 832 × 624 MAC mode (832 × 624)

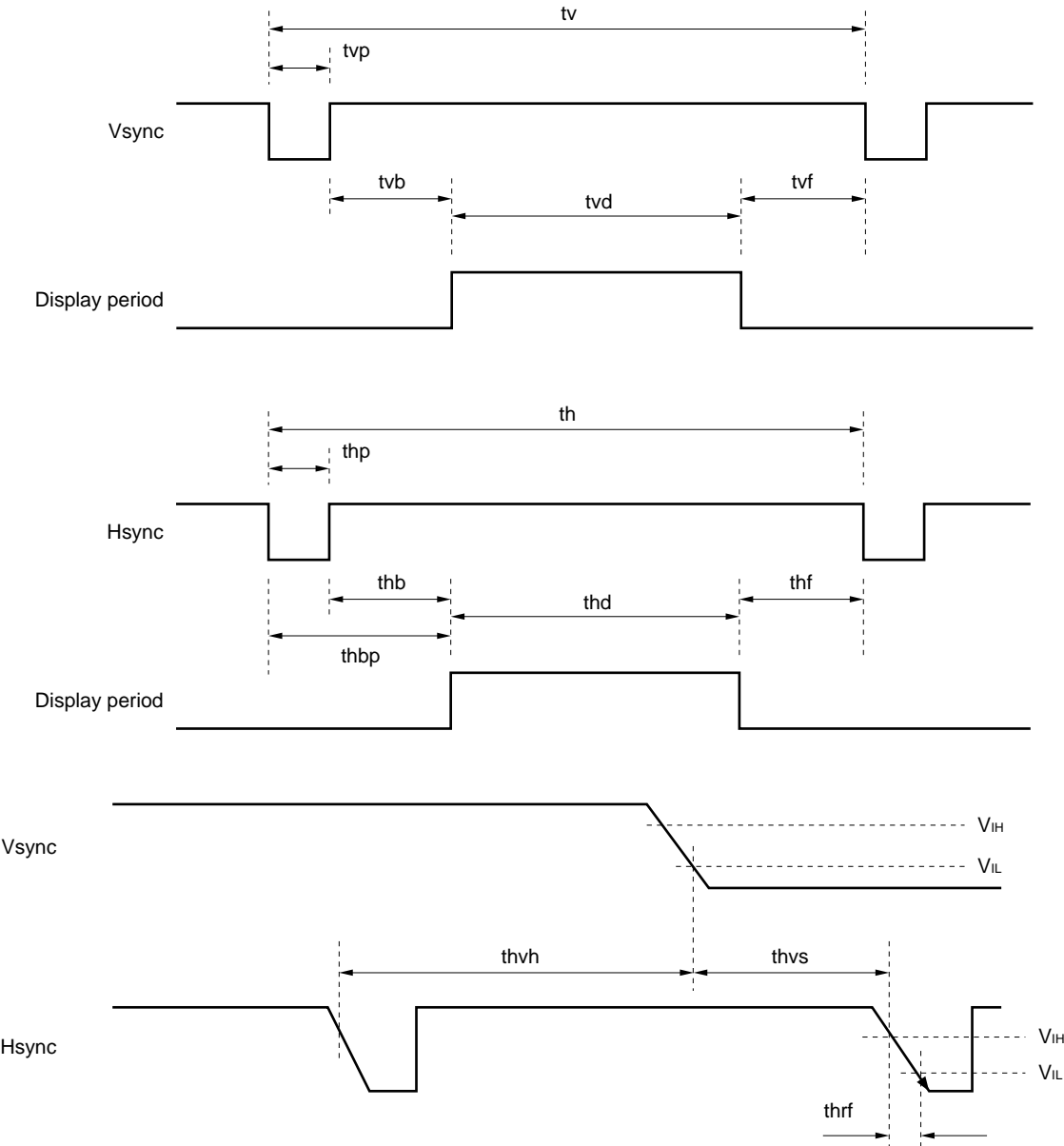


INPUT SIGNAL TIMING

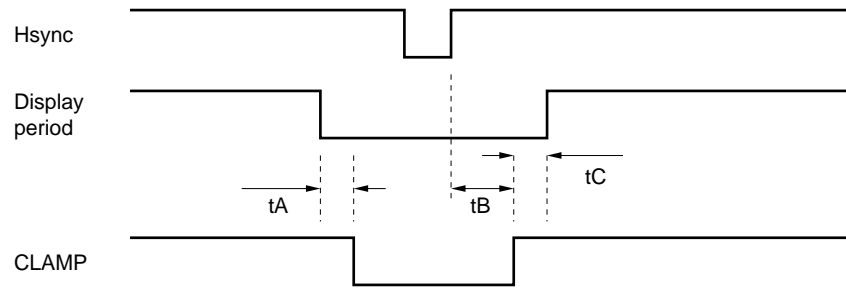
(1) XGA mode (standard)

Name		Symbol	MIN.	TYP.	MAX.	Unit	Remark
CLK	Frequency	1/tc	52.0 –	65.0 15.385	79.0 –	MHz ns	XGA standard
	Rise/Fall	tcrf	–	–	10	ns	
	Pulse-width	tc/tcl	0.4	0.5	0.6	–	
Hsync	Period	th	16.0 –	20.677 1,344	22.7 –	μs CLK	48.363 kHz (TYP.)
	Display	thd	– –	15.754 1,024	– –	μs CLK	
	Front-porch	thf	– 10	0.369 24	– –	μs CLK	
	Pulse-width	thp	– 16	2.092 136	– –	μs CLK	
	Back-porch	thb	1.0 44	2.462 160	– –	μs CLK	Note
	Pulse-width + Back-porch	thbp	1.8	–	–	μs	
	Vsync-Hsync timing	thvh	4	–	–	ns	
		thvs	1	–	–	CLK	
	Rise/Fall	thrf	–	–	10	ns	
Vsync	Period	tv	13.3 –	16.665 806	18.5 –	ms H	60.004 Hz (TYP.)
	Display	tvd	– –	15.880 768	– –	μs H	
	Front-porch	tvf	– 1	62.031 3	– –	μs H	
	Pulse-width	tvp	– 2	124.06 6	– –	μs H	
	Back-porch	tvb	– 5	599.63 29	– –	μs H	
DE	Set-up time	tds	2	–	–	ns	
	Hold time	tdh	4	–	–	ns	
	Rise/Fall	tdrf	–	–	10.0	ns	
Analog R, G, B	–	tda	4	–	–	ns	

Note Minimum values of Back-porch (thb) must be satisfied with both 1.0 μs and 44 CLK.



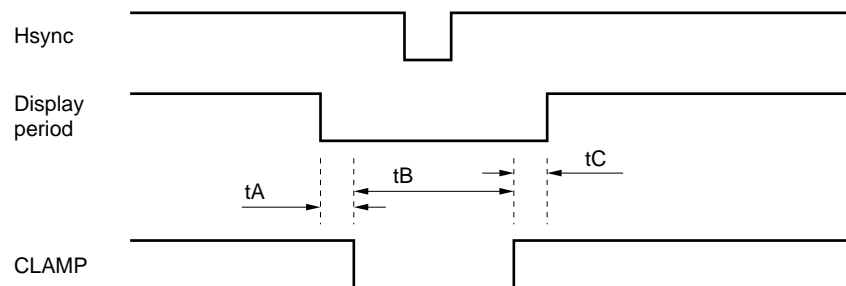
(2) Timing for generating clamp signal internally



MOD1	MOD2	tA [CLK]	tB [CLK]	tC [ns]
0	0	Prohibit		
0	1	44	32	200 minimum
1	0	34	22	
1	1	28	18	

Remark Exclude noises on analog R, G, B signal, because analog R, G, B signals are the black level reference during CLAMP = Low. If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

(3) Timing for inputting clamp signal from outside



Item	Min.	Typ.	Max.	Unit	Remark
tA	0.1	—	—	μs	—
tB	0.3	—	—	μs	—
tC	0.2	—	—	μs	—

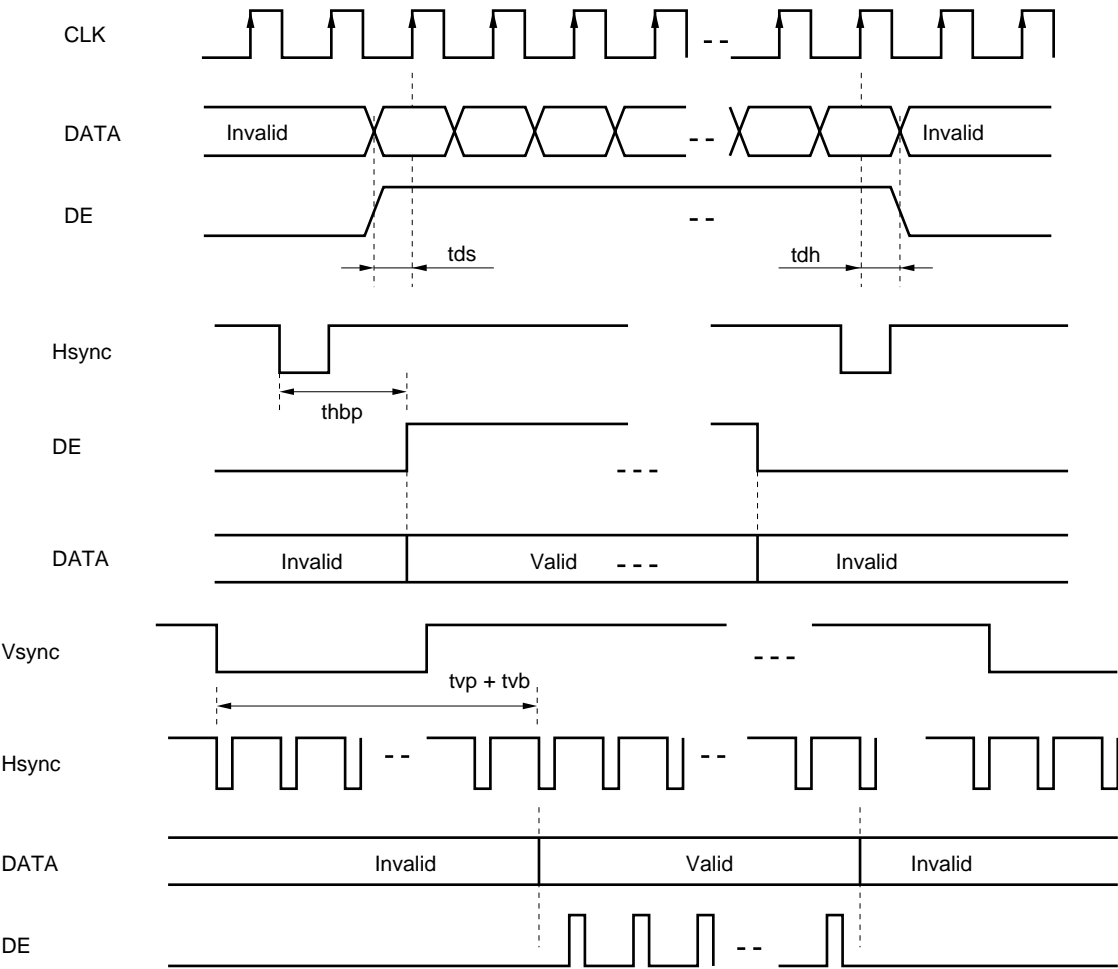
Remark Exclude noises on analog R, G, B signal, because analog R, G, B signals are the black level reference during CLAMP = Low. If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

(1) XGA standard timing

D (0, 0)	D (0, 1)	D (0, 2)	D (0, 1,023)
D (1, 0)	D (1, 1)	D (1, 2)	D (1, 1,023)
D (2, 0)	D (2, 1)	D (2, 2)	D (2, 1,023)
.
.
.
.
D (767, 0)	D (767, 1)	D (767, 2)	D (767, 1,023)



INPUT SIGNAL AND DISPLAY POSITION (DESEL = HIGH)



OPTICAL CHARACTERISTICS

T_a = 25°C, at center ($\theta X = \pm 0^\circ$, $\theta Y = \pm 0^\circ$), V_{DD} = 12 V, V_{DD}B = 12 V

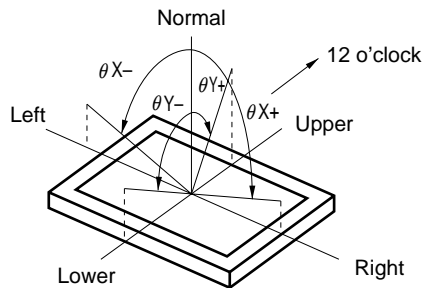
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Luminance		LVMAX	White, at center	150	200	–	cd/m ²	
Contrast ratio		CR	White/Black, at center	100	150	–	–	
Viewing angle range	Horizontal	$\theta X+$	CR > 10, $\theta Y = \pm 0^\circ$, White/Black	70	80	–	deg.	
		$\theta X-$	CR > 10, $\theta Y = \pm 0^\circ$, White/Black	70	80	–	deg.	
	Vertical	$\theta Y+$	CR > 10, $\theta X = \pm 0^\circ$, White/Black	70	80	–	deg.	
		$\theta Y-$	CR > 10, $\theta X = \pm 0^\circ$, White/Black	60	70	–	deg.	
Color gamut		C	at center, to NTSC	35	40	–	%	
Response time		ton	Black to White	–	35	60	ms	
		toff	White to Black	–	40	80		
Luminance uniformity		–	Maximum luminance	–	–	1.30	–	
			Minimum luminance ,white, Refer to Remark 5.					
Luminance control range by BRTH/BRTL		–	Maximum luminance : 100 %	ACA = High	–	30 - 100	–	%
				ACA = Low	–	60 - 100	–	

Remarks 1. The contrast ratio is calculated by using the following formula.

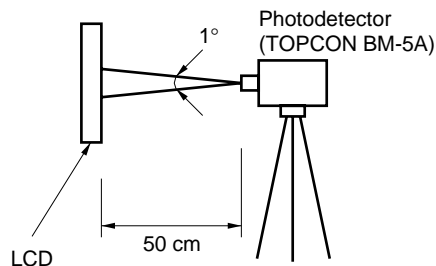
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in white}}{\text{Luminance with all pixels in black}}$$

The Luminance is measured in darkroom.

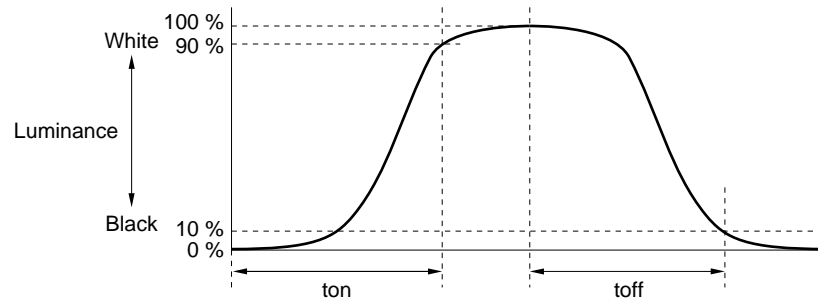
2. Definitions of viewing angle are as follows.



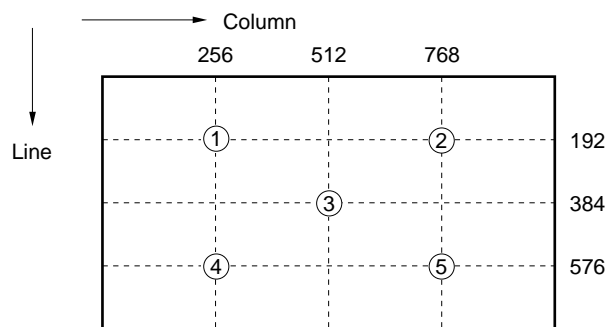
3. The luminance is measured after 20 minutes from the module works, with all pixels in white. Typical value is measured after luminance saturation.



4. Definition of response time is as follows.
 Photo-detector output signal is measured when the luminance changes “white” to “black”.
 Response time is the time between 0 % and 90 % of the photo-detector output amplitude.



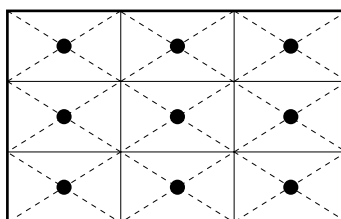
5. The luminance is measured at near the five points shown below.



RELIABILITY TEST


Test item	Test condition
High temperature/humidity operation Note 1	50 ± 2°C, 85% relative humidity 240 hours Display data is black.
Heat cycle Note 1 (operation)	<1> 0°C ± 3°C ... 1 hour 55°C ± 3°C ... 1 hour <2> 50 cycles, 4 hours/cycle <3> Display data is black.
Thermal shock Note 1 (non-operation)	<1> -20°C ± 3°C ... 30 minutes 60°C ± 3°C ... 30 minutes <2> 100 cycles <3> Temperature transition time within 5 minutes
Vibration Notes 1, 2 (non-operation)	<1> 5 - 100 Hz, 2G 1 minute/cycle X, Y, Z direction <2> 50 times each direction
Mechanical shock Notes 1, 2 (non-operation)	<1> 55 G, 11 ms X, Y, Z direction <2> 3 times each direction
ESD Notes 1, 3 (operation)	150 pF, 150 Ω, ±10 kV 9 places on a panel 10 times each place at one-second intervals
Dust Note 1 (operation)	15 kinds of dust (JIS Z 8901) Hourly 15 seconds stir, 8 times repeat



- Notes 1.** Display function is checked by the same condition as LCD module out-going inspection.
2. Physical damage.
3. Discharge points “●” are shown in the figure.




GENERAL CAUTIONS

Next figures and sentence are very important. Please understand these contents as follows.

	CAUTION This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.
---	--

	This figure is a mark that you will get an electric shock when you make a mistake to operate.
	This figure is a mark that you will get hurt when you make a mistake to operate




	Do not touch an inverter, on which is stuck a caution label, while the LCD module is under the operation, because of dangerous high voltage.
---	--

(1) Caution when taking out the module

- a) Pick the pouch only, in taking out module from a carrier box.

(2) Cautions for handling the module

- a) As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges.
- b)  As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- c) As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- d) Do not pull the interface connectors in or out while the LCD module is operating.
- e) Put the module display side down on a horizontal plane.
- f) Handle connectors and cables with care.
- g) When the module is operating, do not lose CLK, Hsync or Vsync signal. If any one of these signals is lost, the LCD panel would be damaged.
- h) The torque to mounting screw should never exceed 0.392 N·m (4 kgf·cm).

(3) Cautions for the atmosphere

- a) Dew drop atmosphere should be avoided.
- b) Do not store and/or operate the LCD module in a high temperature and/or high humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.
- c) This module uses cold cathod fluorescent lamps. Therefore, the life time of lamps becomes short conspicuously at low temperature.
- d) Do not operate the LCD module in a high magnetic field.

(4) Caution for the module characteristics

- a) Do not apply fixed pattern data signal for a long time to the LCD module. It may cause image sticking. Please use screen savers if the display pattern is fixed more than one hour.

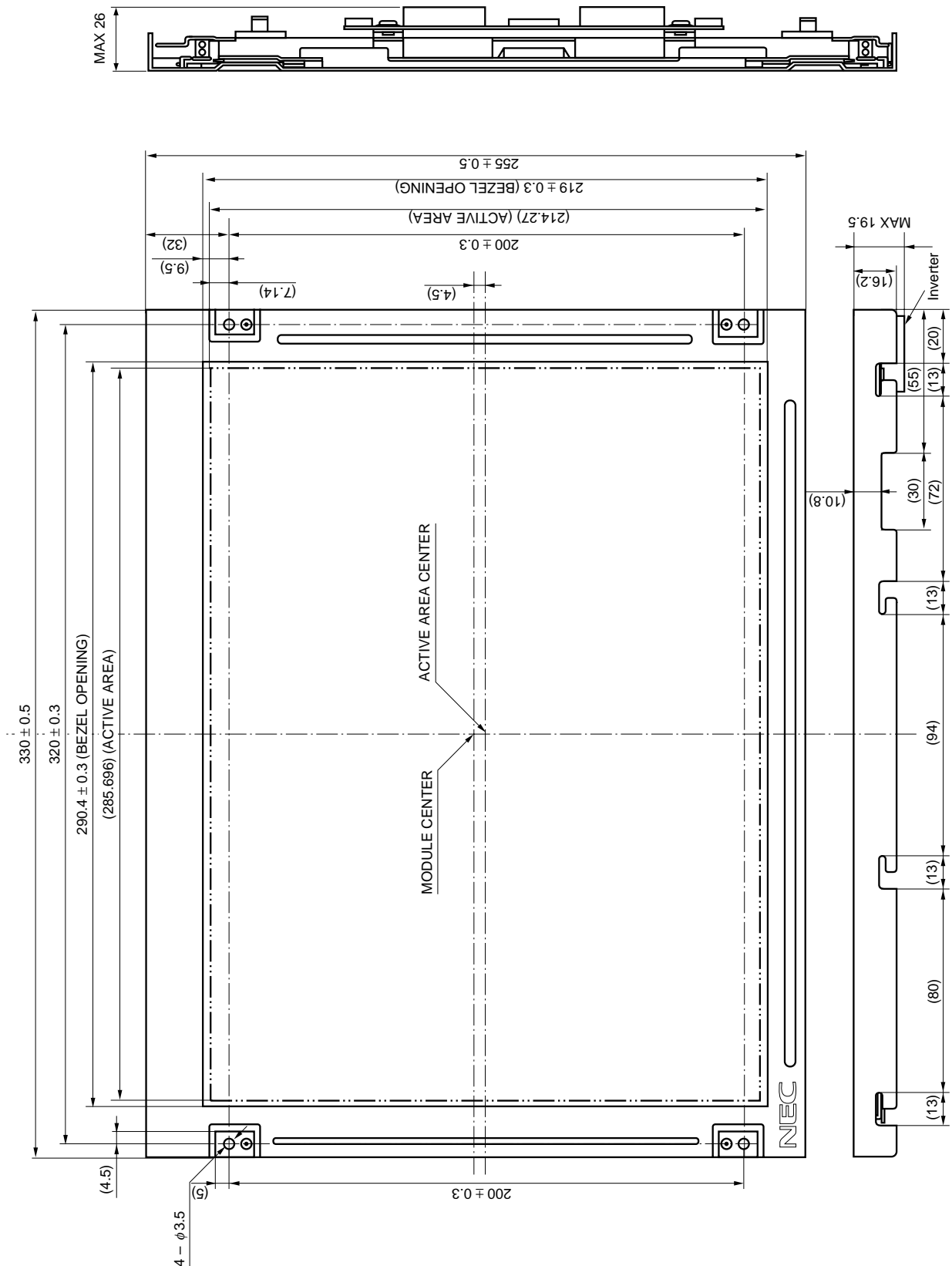
(5) Other cautions

- a) Do not disassemble and/or reassemble LCD module.
- b) Do not readjust variable resistors etc.
- c) When returning the module for repair or etc, please pack the module not to be broken. We recommend to the original shipping packages.

Liquid Crystal Display has the following specific characteristics. There are not defects or malfunctions.

- The display condition of LCD module may be affected by the ambient temperature.
- The LCD module uses cold cathode tube for backlighting. Optical characteristics, like luminance or uniformity, will change during time.
- Uneven brightness and/or small spots may be noticed depending on different display patterns.

OUTLINE DRAWING: Front View (Unit: mm)



Remark The torque to mounting screw should never exceed 0.392 N·m (4 kgf·cm).

[illegible]

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Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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