PRODUCT SPECIFICATION

Doc. Number:

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: N173FGE
SUFFIX: E23

Customer:

APPROVED BY   **SIGNATURE**

<u>**Name / Title**</u>   _____
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
楊竣傑	曹文彬	鍾惠櫻
2013-04-19	2013-04-18	2013-04-11
08:45:15 CST	09:26:32 CST	09:00:23 CST

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PRODUCT SPECIFICATION

REVISION HISTORY

Version	Date	Page	Description
1.0	Sep. 17, 2012	All	Preliminary Spec Ver.1.0 was first issued.
2.0	Feb. 6, 2013	All	Approval Spec Ver.2.0 was first issued.
2.1	Apr.10, 2013	All	Modify logo "INNOLUX"

PRODUCT SPECIFICATION

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N173FGE-E23 is a 17.3" (17.3" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 30 pins eDP interface. This module supports 1600 x 900 HD+ mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 GENERAL SPECIFICATI0NS

| Item	Specification	Unit	Note
Screen Size	17.3" diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1600 x R.G.B. x 900	pixel	-
Pixel Pitch	0.2388 (H) x 0.2388(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Glare	-	-
Luminance, White	220	Cd/m2	
Power Consumption	Total 5.74 W (Max.) @ cell 1.24 W (Max.), BL4.5 W (Max.)		(1)

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	397.6	398.1	398.6	mm	(1)
	Vertical (V)	232.3	232.8	233.3	mm	
	Thickness (T)	-	5.5	5.8	mm	
Bezel Area	Horizontal	386.58	386.88	387.18	mm	
	Vertical	218.02	218.32	218.62	mm	
Active Area	Horizontal	-	382.08	-	mm	
	Vertical	-	214.92	-	mm	
Glass Thickness	CF	0.45	0.5	0.55	mm	
	TFT	0.45	0.5	0.55	mm	
Weight		-	540	555	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE
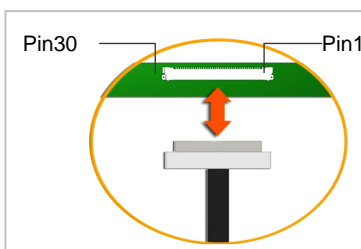
Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-030E-12 or equivalent

User's connector Part No: IPEX-20453-030T-01 or equivalent

3. ABSOLUTE MAXIMUM RATINGS
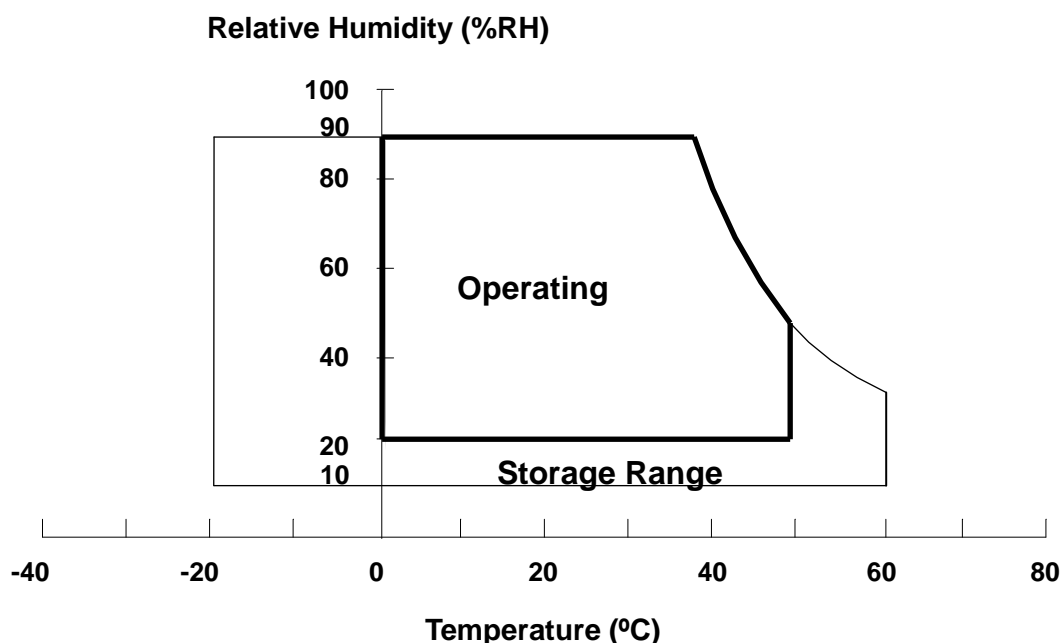
3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1)　　(a) 90 %RH Max. (Ta <= 40 ºC).

　　　　　　(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

　　　　　　(c) No condensation.

Note (2)　　The temperature of panel surface should be 0 ºC min. and 60 ºC max.

Relative Humidity (%RH)

Temperature (ºC)

3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	24	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	5	V	1)
Converter Control Signal Voltage	LED_EN	-0.3	5	V	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS"..

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM
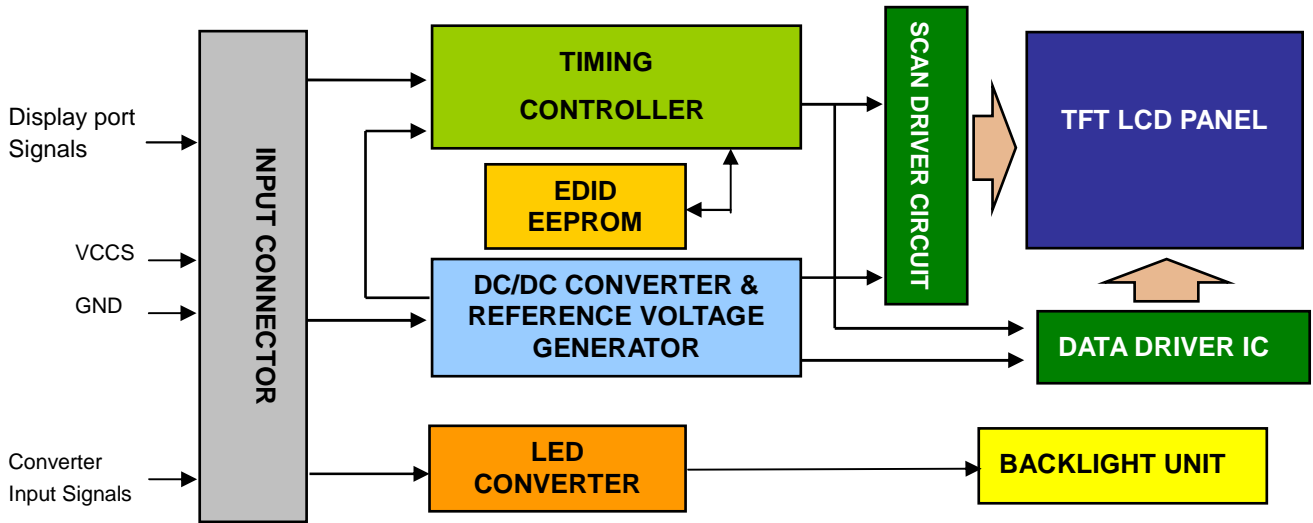

4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for INNOLUX test)	
2	H_GND	High Speed Ground	
3	NC	No Connection (Reserved)	
4	NC	No Connection (Reserved)	
5	H_GND	High Speed Ground	
6	ML0-	Complement Signal-Lane 0	
7	ML0+	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3 V (typical)	
13	VCCS	Power Supply +3.3 V (typical)	
14	NC	No Connection (Reserved for INNOLUX test)	
15	GND	Ground	
16	GND	Ground	
17	HPD	Hot Plug Detect	
18	BL_GND	BL Ground	
19	BL_GND	BL Ground	
20	BL_GND	BL Ground	
21	BL_GND	BL Ground	
22	LED_EN	BL_Enable Signal of LED Converter	
23	LED_PWM	PWM Dimming Control Signal of LED Converter	
24	NC	No Connection (Reserved for INNOLUX test)	
25	NC	No Connection (Reserved for INNOLUX test)	

26	LED_VCCS	BL Power	
27	LED_VCCS	BL Power	
28	LED_VCCS	BL Power	
29	LED_VCCS	BL Power	
30	NC	No Connection (Reserved for INNOLUX test)	

Note (1) The first pixel is odd as shown in the following figure.
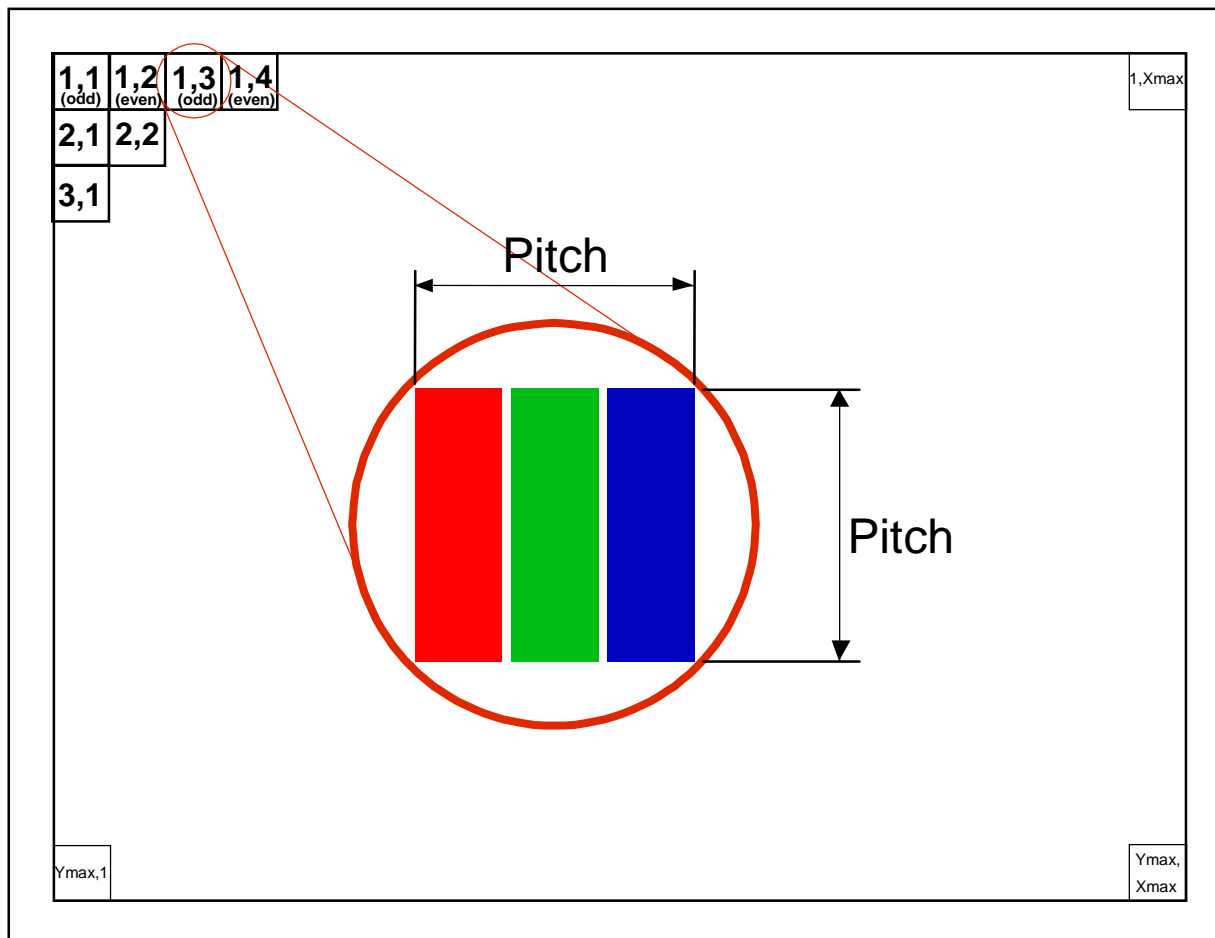
4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)-
HPD	High Level		2.25	-	2.75	V	
	Low Level		0	-	0.4	V	
Ripple Voltage		V_{RP}	-	50	-	mV	(1)-
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	Icc		345	376	mA	(3)a
	Black			440	500	mA	(3)

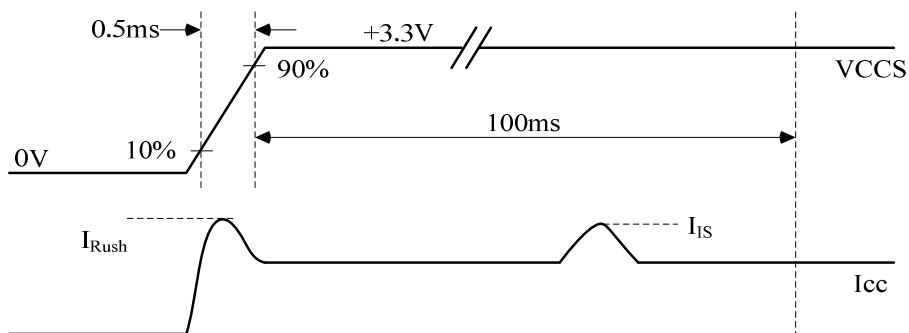Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.
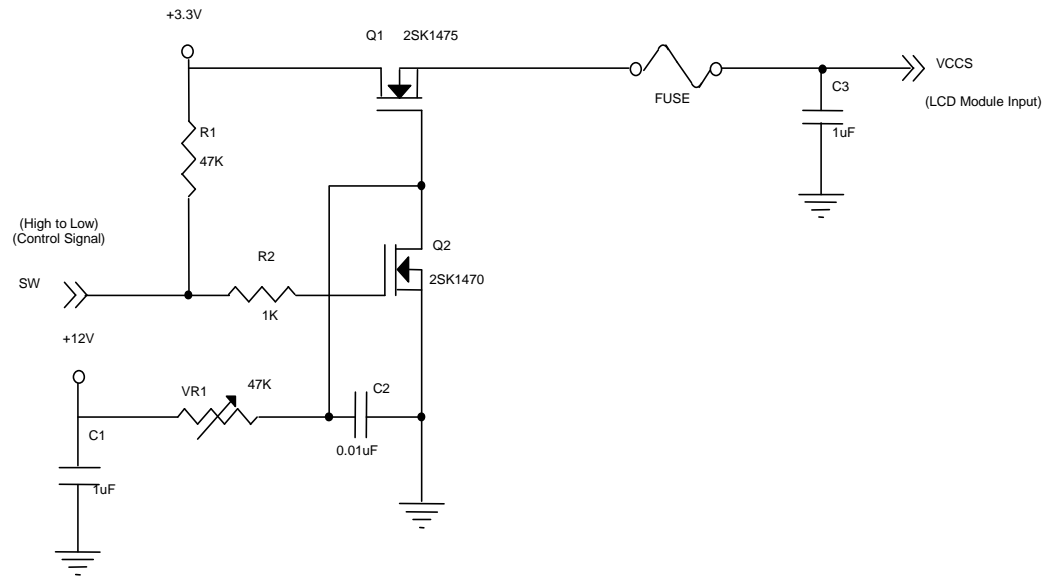
VCCS rising time is 0.5ms

Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC

Current and f_v = 60 Hz, whereas a specified power dissipation check pattern is displayed.

a. Mosaic Pattern
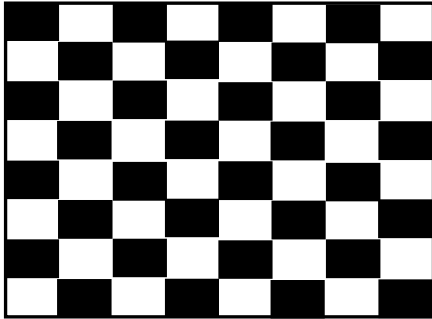
Active Area

4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	6.0	12.0	21.0	V	
Converter Inrush Current		ILED$_{RUSH}$	-	-	1.5	A	(1)
EN Control Level	Backlight On		2.2	-	5.0	V	
	Backlight Off		0	-	0.6	V	
PWM Control Level	PWM High Level		2.2	-	5	V	
	PWM Low Level		0	-	0.6	V	
PWM Control Duty Ratio			5	-	100	%	
PWM Control Permissive Ripple Voltage		VPWM_pp	-	-	100	mV	
PWM Control Frequency		f$_{PWM}$	190	-	2K	Hz	(2)
LED Power Current LED_VCCS =Typ.		ILED	277	340	375	mA	(3)

Note (1) ILED$_{RUSH}$: the maximum current when LED_VCCS is rising,

ILED$_{IS}$: the maximum current of the first 100ms after power-on,
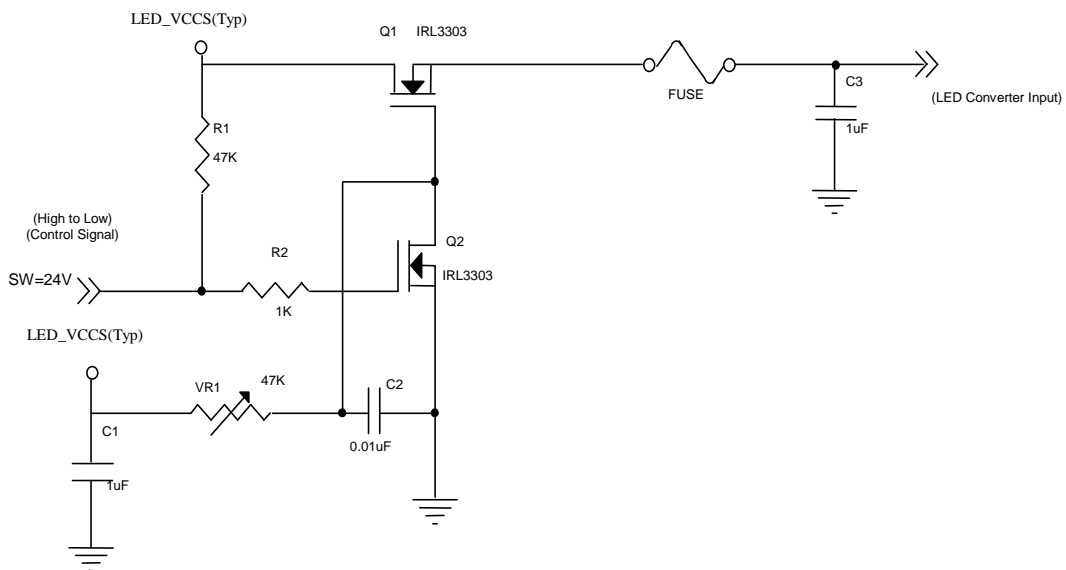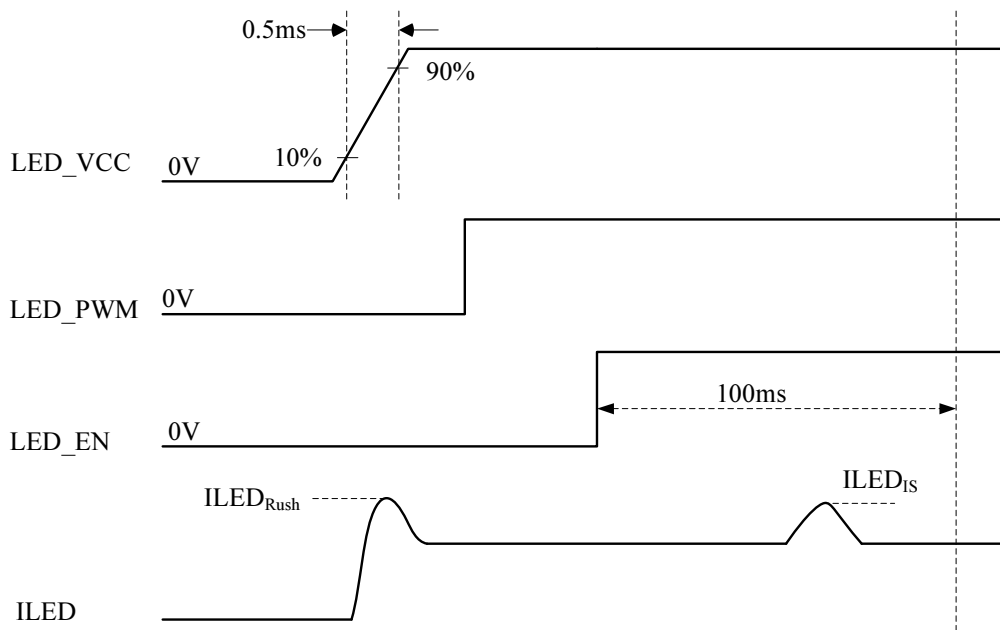
Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f$_{PWM}$ = 200 Hz, Duty=100%.

VLED rising time is 0.5ms

Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

$$N : \text{Integer} \quad (N \geq 3)$$

$$f : \text{Frame rate}$$

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty=100%.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	25.2	27.9	30.6	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L		125		mA	
Power Consumption	P_L		3.4875	3.825	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1)   LED current is measured by utilizing a high frequency current meter as shown below :

V_L, I_L

LED
Light Bar
Parallel: 5
Serial: 9

Light Bar Feedback

Channels
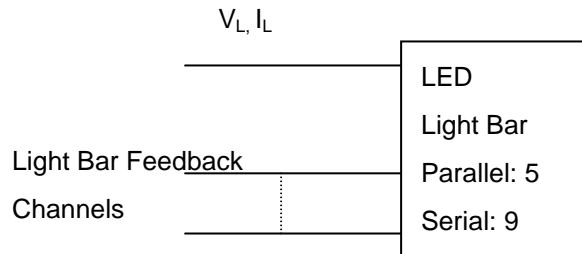
Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 ºC and I_L = 25 mA(Per EA) until the brightness becomes $\leqq$ 50% of its original value.

4.4 DISPLAY PORT SIGNAL TIMING SPECIFICATION

4.4.1 DISPLAY PORT INTERFACE

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(3)
AUX AC Coupling Capacitor	C_{AUX}	75		200	nF	(2)

Note (1) Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.1.

(2) The AUX AC Coupling Capacitor should be placed on Source Devices.

(3)The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1

Single Ended
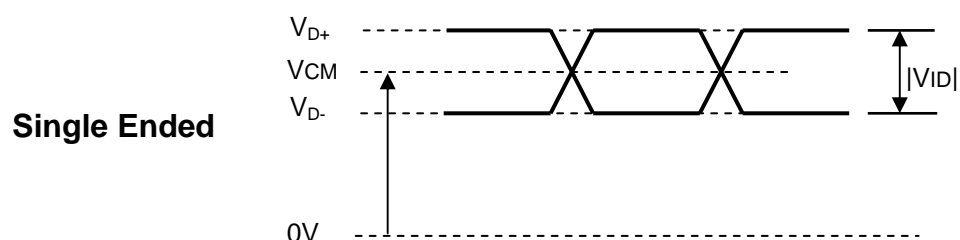
4.4.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input

for the color. The higher the binary input the brighter the color. The table below provides the assignment

of color versus data input.

| Color		Data Signal																		
		Red						Green						Blue						
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Refresh rate 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	53.9	53.9	53.9	MHz	-
DE	Vertical Total Time	TV	925	925	925	TH	-
	Vertical Active Display Period	TVD	900	900	900	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	25	TV-TVD	TH	-
	Horizontal Total Time	TH	1942	1942	1942	Tc	-
	Horizontal Active Display Period	THD	1600	1600	1600	Tc	-
	Horizontal Active Blanking Period	THB	TH-THB	342	TH-THB	Tc	-

INPUT SIGNAL TIMING DIAGRAM
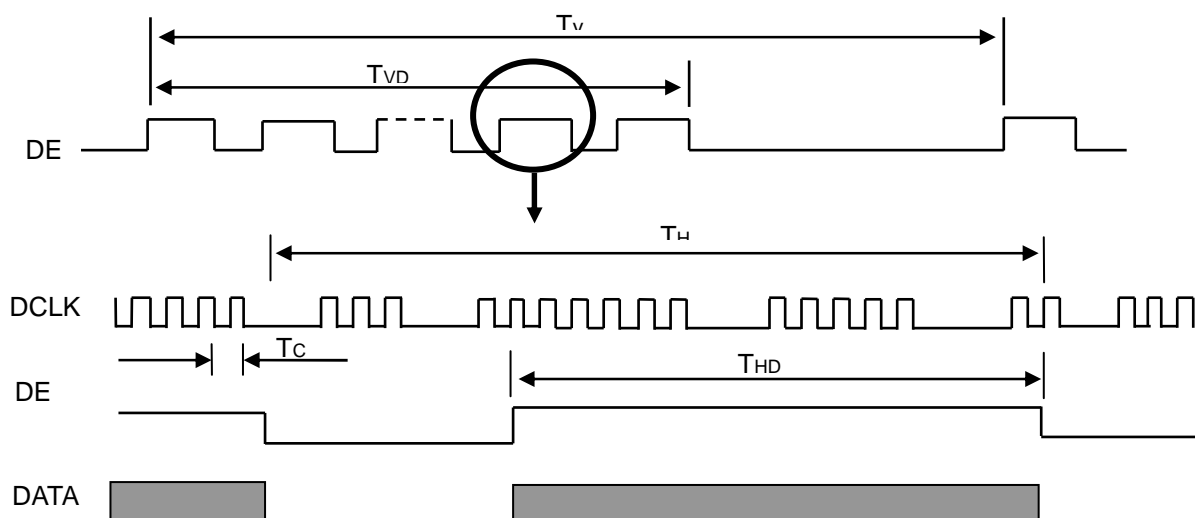
4.6 POWER ON/OFF SEQUENCE
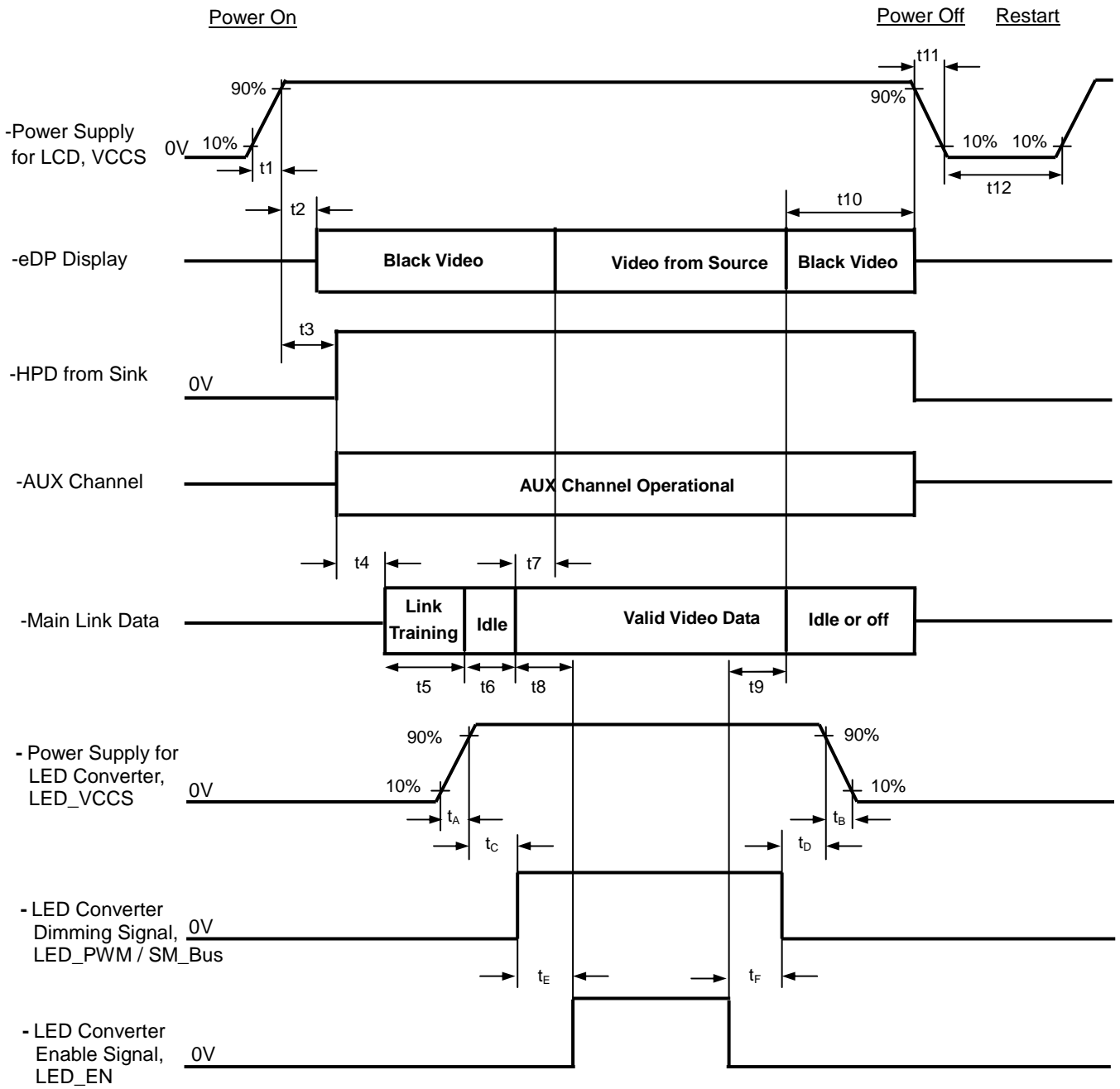
PRODUCT SPECIFICATION

Timing Specifications:

Parameter	Description	Reqd. By	Value Min	Value Max	Unit	Notes
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Prevents display noise until valid video data is received from the Source
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink Aux Channel must be operational upon HPD high
t4	Delay from HPD high to link training initialization	Source	-	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	-	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	-	-	ms	Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max allows Sink validate video data and timing
t8	Delay from valid video data from Source to backlight on	Source	-	-	ms	Source must assure display video is stable
t9	Delay from backlight off to end of valid video data	Source	-	-	ms	Source must assure backlight is no longer illuminated
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	-
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-
t12	VCCS Power off time	Source	500	-	ms	-
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t_B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t_C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t_D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	1	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	1	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) Please avoid floating state of the interface signal during signal invalid period.

Note (3) It is recommended that the backlight power must be turned on after the power supply for LCD and the interface signal is valid.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

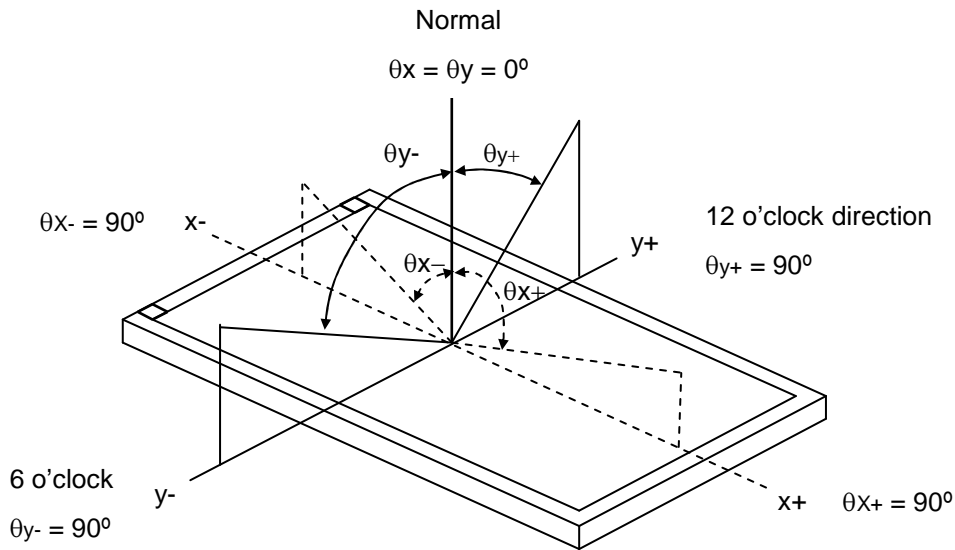| Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	125	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		500	650	-	-	(2),(5),(7)
Response Time		T_R		-	3	8	ms	(3),(7)
		T_F		-	7	12	ms	
Average Luminance of White		L_{AVE}		185	220	-	cd/m^2	(4),(6),(7)
Color Chromaticity	Red	Rx	$\theta_x=0°$, $\theta_Y=0°$ Viewing Normal Angle	Typ − 0.03	0.617	Typ + 0.03	-	(1),(7)
		Ry			0.337		-	
	Green	Gx			0.342		-	
		Gy			0.588		-	
	Blue	Bx			0.156		-	
		By			0.074		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	40	45		Deg.	(1),(5),(7)
		θ_x-		40	45	-		
	Vertical	θ_Y+		15	20	-		
		θ_Y-		40	45	-		
White Variation of 5 Points		δW_{5p}	$\theta_x=0°$, $\theta_Y=0°$	80	90	-	%	(5),(6),(7)

Note (1) Definition of Viewing Angle (θx, θy):

Normal

θx = θy = 0º

θy- θy+

θX- = 90º x-

12 o'clock direction

θy+ = 90º

y+

θx-

θx+

6 o'clock y-

x+ θX+ = 90º

θy- = 90º

Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.
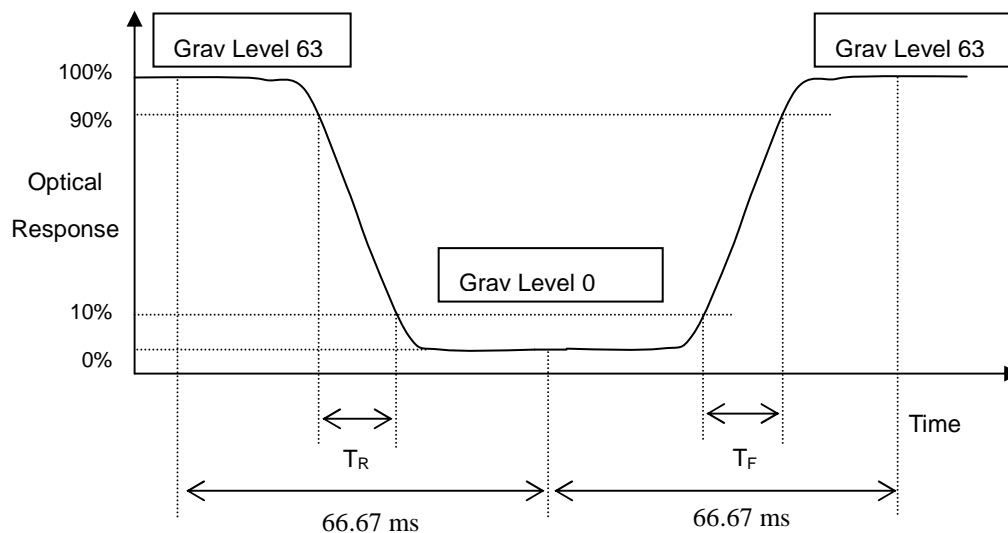
Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):

| Grav Level 63 | | Grav Level 63 |

100%

90%

Optical

Response

Grav Level 0

10%

0%

T_R

T_F

Time

66.67 ms

66.67 ms

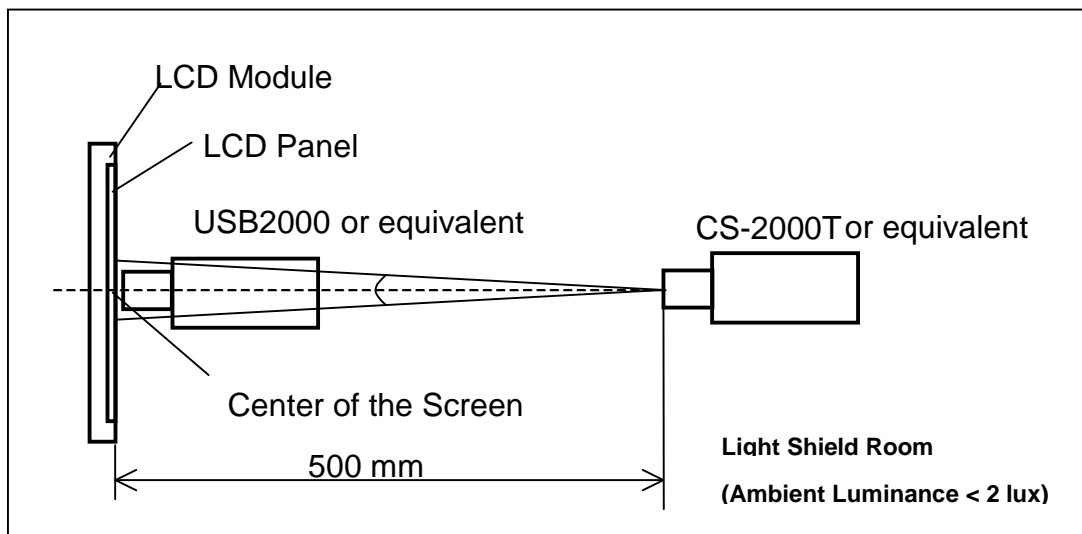Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of White at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.
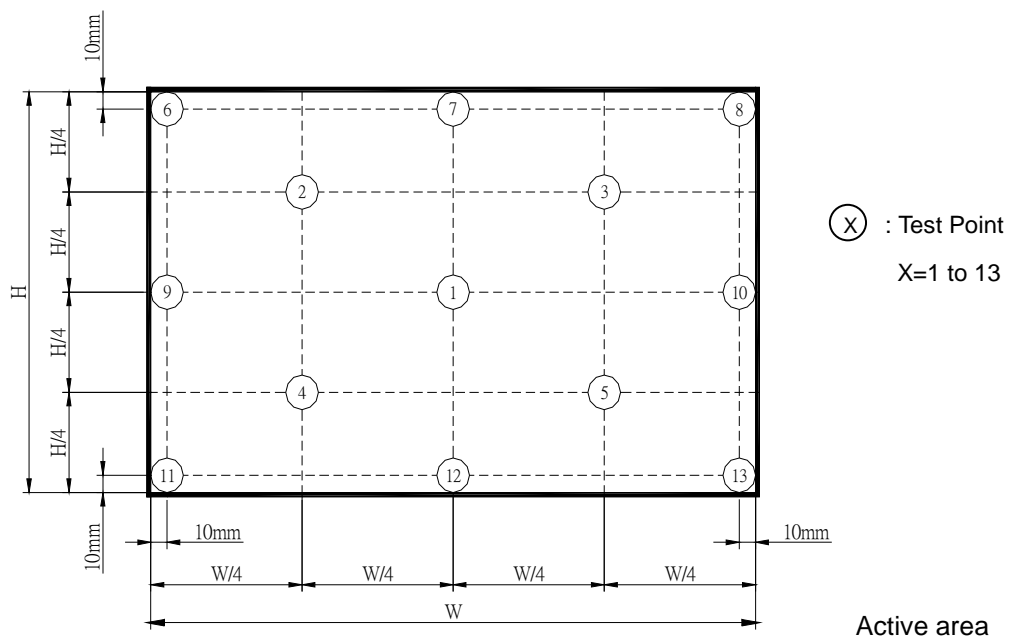

LCD Module

LCD Panel

USB2000 or equivalent

CS-2000T or equivalent

Center of the Screen

500 mm

Light Shield Room

(Ambient Luminance < 2 lux)

Note (6) Definition of White Variation (δW):

Measure the luminance of White at 5 points

δW_{5p} = {Minimum [L (1)~ L (5)] / Maximum [L (1)~ L (5)]}*100%

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of

the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour⟷60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50℃, 80% RH, 240 hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.
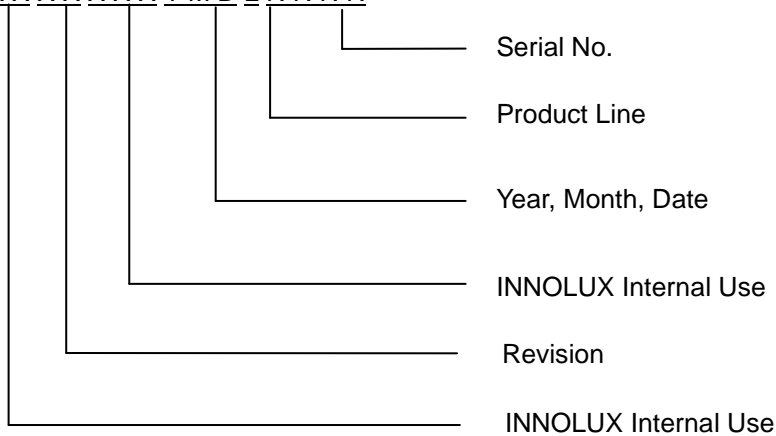
7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N173FGE - E23

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X X Y M D L N N N N

                                                      Serial No.

                                                      Product Line

                                                      Year, Month, Date

                                                      INNOLUX Internal Use

                                                      Revision

                                                      INNOLUX Internal Use

Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

                        Month: 1~9, A~C, for Jan. ~ Dec.

                        Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Production Location: MADE IN XXXX. XXXX stands for production location.

(c) Revision Code: cover all the change

(d) Serial No.: Manufacturing sequence of product
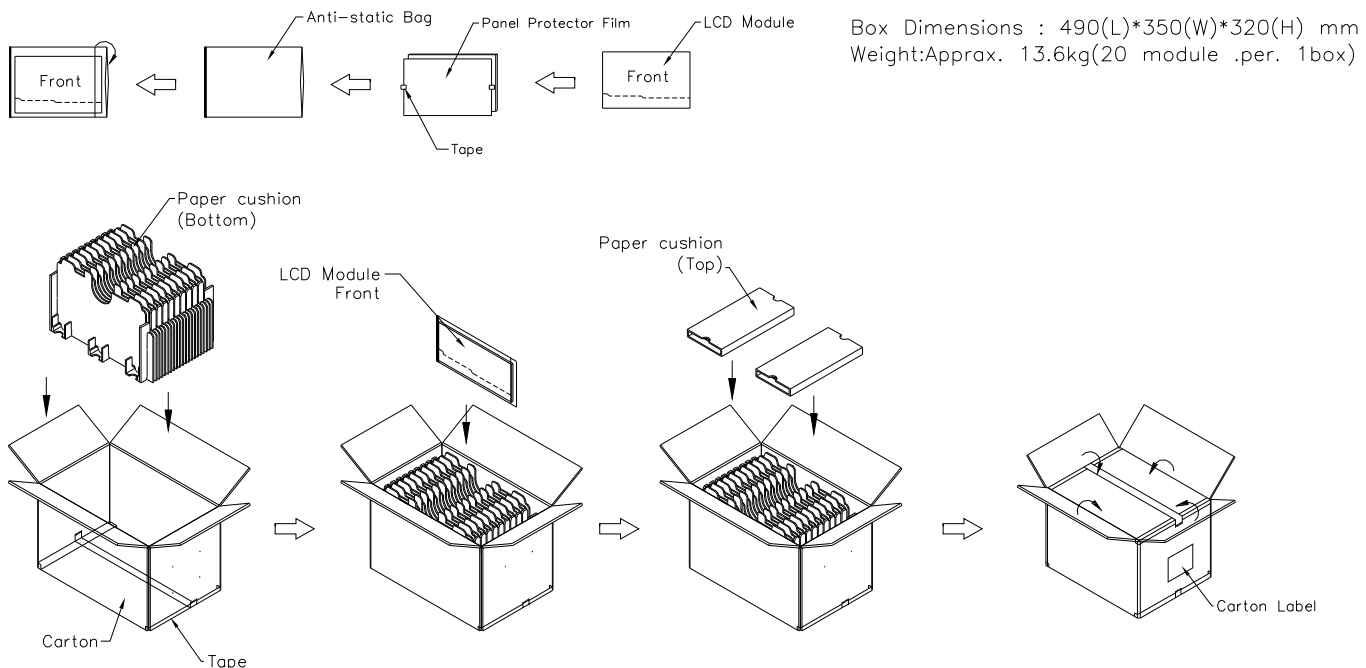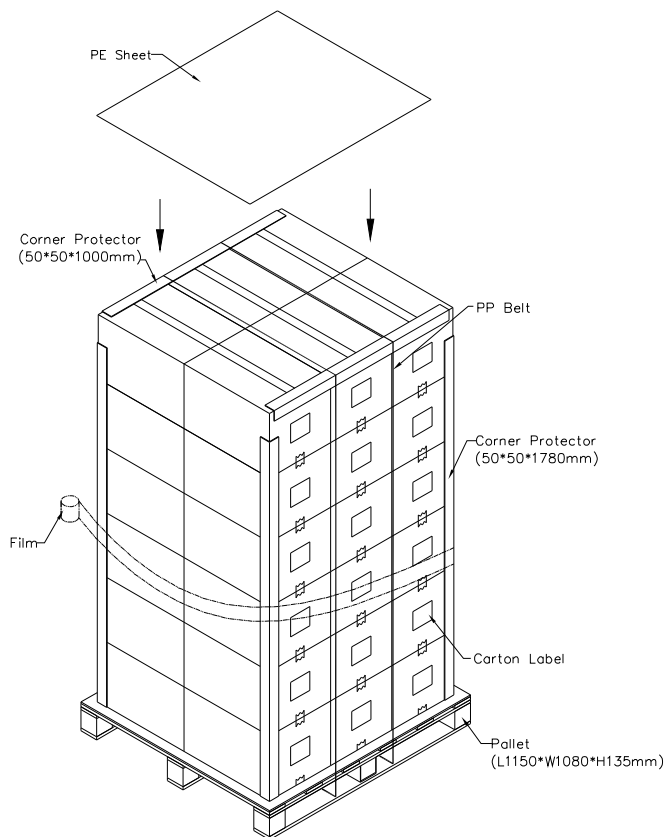
(e) UL Logo: XXXX is UL factory ID

7.2 CARTON

Box Dimensions : 490(L)*350(W)*320(H) mm
Weight:Approx. 13.6kg(20 module .per. 1box)

Figure. 7-2 Packing method

7.3 PALLET
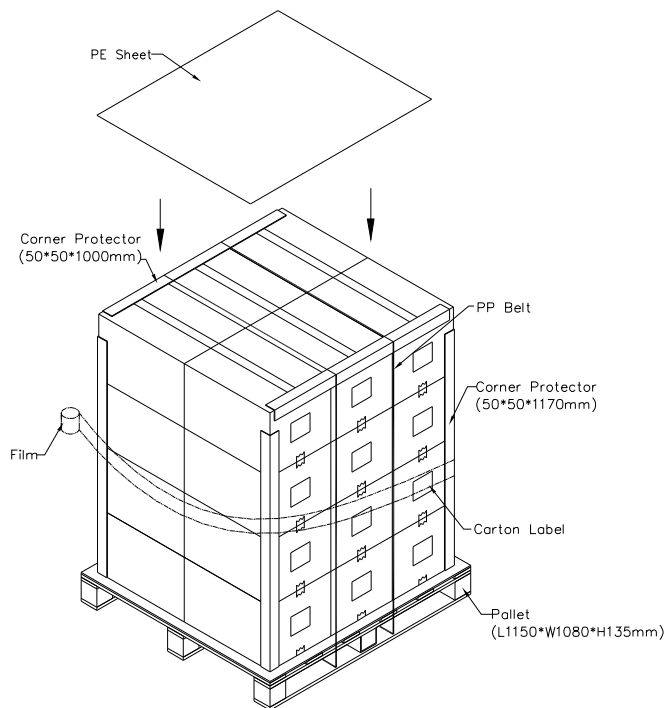
Figure. 7-3 Packing method

7.4 PALLET UN-PACKAGING METHOD

remove paper cushion(top)

take Module out

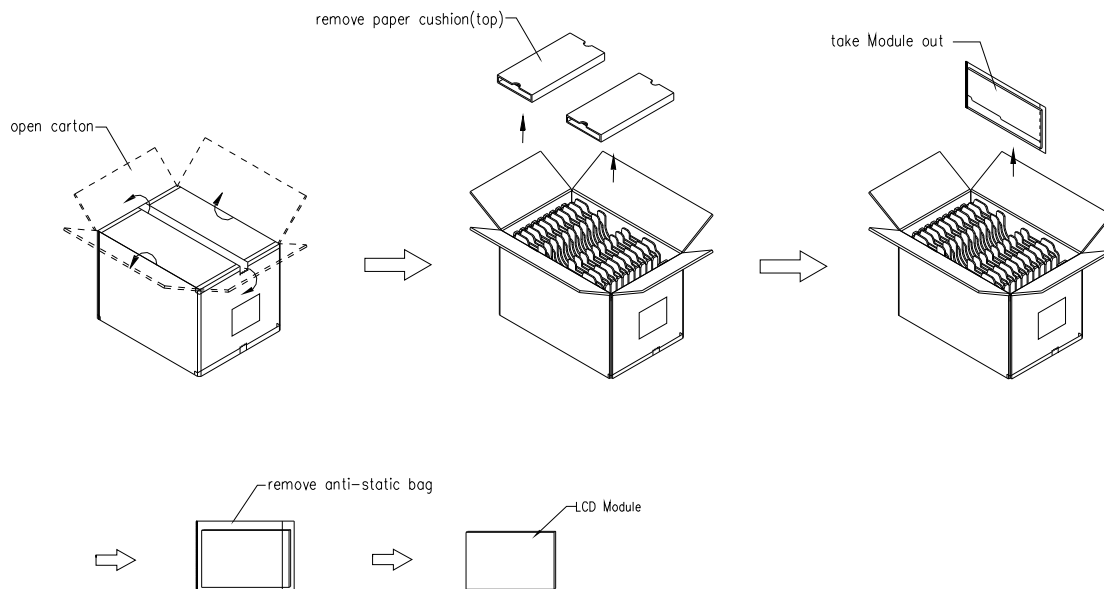open carton

remove anti-static bag

LCD Module

Figure. **7.4** un-packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while

assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the

VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMN")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AE	10101110
10	0A	ID product code (N173FGE-E23)	0D	00001101
11	0B	ID product code (hex LSB first; N173FGE-E23)	AE	10101110
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture ("43")	2B	00101011
17	11	Year of manufacture ("2012")	16	00010110
18	12	EDID structure version # ("1")	01	00000001
19	13	EDID revision # ("4")	04	00000100
20	14	Video I/P definition("digital")	95	10010101
21	15	Max H image size ("39cm")	27	00100111
22	16	Max V image size ("22"cm")	16	00010110
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support (Active off, RGB Color)	02	00000010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	1A	00011010
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	05	00000101
27	1B	Rx=0.617	9E	10011110
28	1C	Ry=0.337	56	01010110
29	1D	Gx=0.342	57	01010111
30	1E	Gy=0.588	96	10010110
31	1F	Bx=0.156	28	00101000
32	20	By=0.074	13	00010011
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("107.8"MHz, According to VESA CVT Rev1.4)	1C	00011100
55	37	# 1 Pixel clock (hex LSB first)	2A	00101010
56	38	# 1 H active ("1600")	40	01000000
57	39	# 1 H blank ("342")	56	01010110
58	3A	# 1 H active : H blank ("1600 : 342")	61	01100001
59	3B	# 1 V active ("900")	84	10000100
60	3C	# 1 V blank ("25")	19	00011001
61	3D	# 1 V active : V blank ("900 : 25")	30	00110000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 5")	35	00110101
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48 : 32 : 3 : 5")	00	00000000
66	42	# 1 H image size ("388 mm")	84	10000100
67	43	# 1 V image size ("219 mm")	DB	11011011
68	44	# 1 H image size : V image size ("388 : 219")	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74	4A	# 2 Reserved	00	00000000
75	4B	# 2 FE (hex) defines ASCII string (Model Name "N173FGE-E23", ASCII)	FE	11111110
76	4C	# 2 Flag	00	00000000
77	4D	# 2 1st character of name ("N")	4E	01001110
78	4E	# 2 2nd character of name ("1")	31	00110001
79	4F	# 2 3rd character of name ("7")	37	00110111
80	50	# 2 4th character of name ("3")	33	00110011
81	51	# 2 5th character of name ("F")	46	01000110
82	52	# 2 6th character of name ("G")	47	01000111
83	53	# 2 7th character of name ("E")	45	01000101
84	54	# 2 8th character of name ("-")	2D	00101101
85	55	# 2 9th character of name ("E")	45	01000101

86	56	# 2 10th character of name ("2")	32	00110010
87	57	# 2 11th character of name ("3")	33	00110011
88	58	# 2 New line character indicates end of ASCII string	0A	00001010
89	59	# 2 Padding with "Blank" character	20	00100000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Vendor "CMN", ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 1st character of string ("C")	43	01000011
96	60	# 3 2nd character of string ("M")	4D	01001101
97	61	# 3 3rd character of string ("N")	4E	01001110
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with "Blank" character	20	00100000
100	64	# 3 Padding with "Blank" character	20	00100000
101	65	# 3 Padding with "Blank" character	20	00100000
102	66	# 3 Padding with "Blank" character	20	00100000
103	67	# 3 Padding with "Blank" character	20	00100000
104	68	# 3 Padding with "Blank" character	20	00100000
105	69	# 3 Padding with "Blank" character	20	00100000
106	6A	# 3 Padding with "Blank" character	20	00100000
107	6B	# 3 Padding with "Blank" character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 FE (hex) defines ASCII string (Model Name "N173FGE-E23", ASCII)	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 1st character of name ("N")	4E	01001110
114	72	# 4 2nd character of name ("1")	31	00110001
115	73	# 4 3rd character of name ("7")	37	00110111
116	74	# 4 4th character of name ("3")	33	00110011
117	75	# 4 5th character of name ("F")	46	01000110
118	76	# 4 6th character of name ("G")	47	01000111
119	77	# 4 7th character of name ("E")	45	01000101
120	78	# 4 8th character of name ("-")	2D	00101101
121	79	# 4 9th character of name ("E")	45	01000101
122	7A	# 4 10th character of name ("2")	32	00110010
123	7B	# 4 11th character of name ("3")	33	00110011
124	7C	# 4 New line character indicates end of ASCII string	0A	00001010
125	7D	# 4 Padding with "Blank" character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	7F	01111111

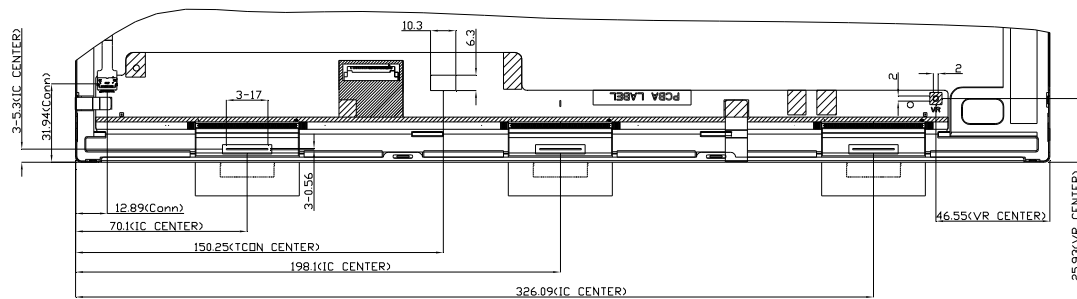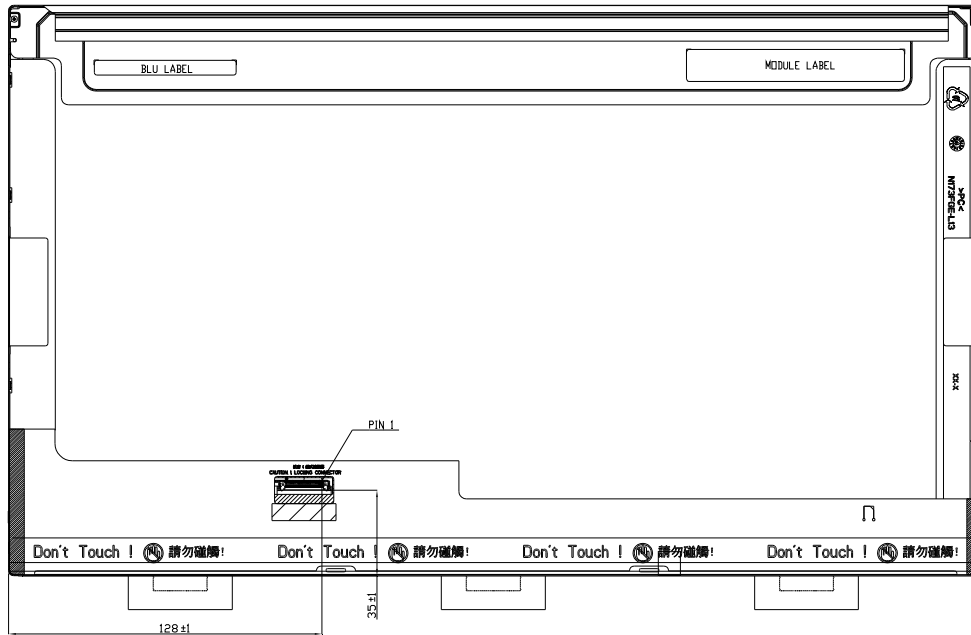**Appendix. OUTLINE DRAWING**
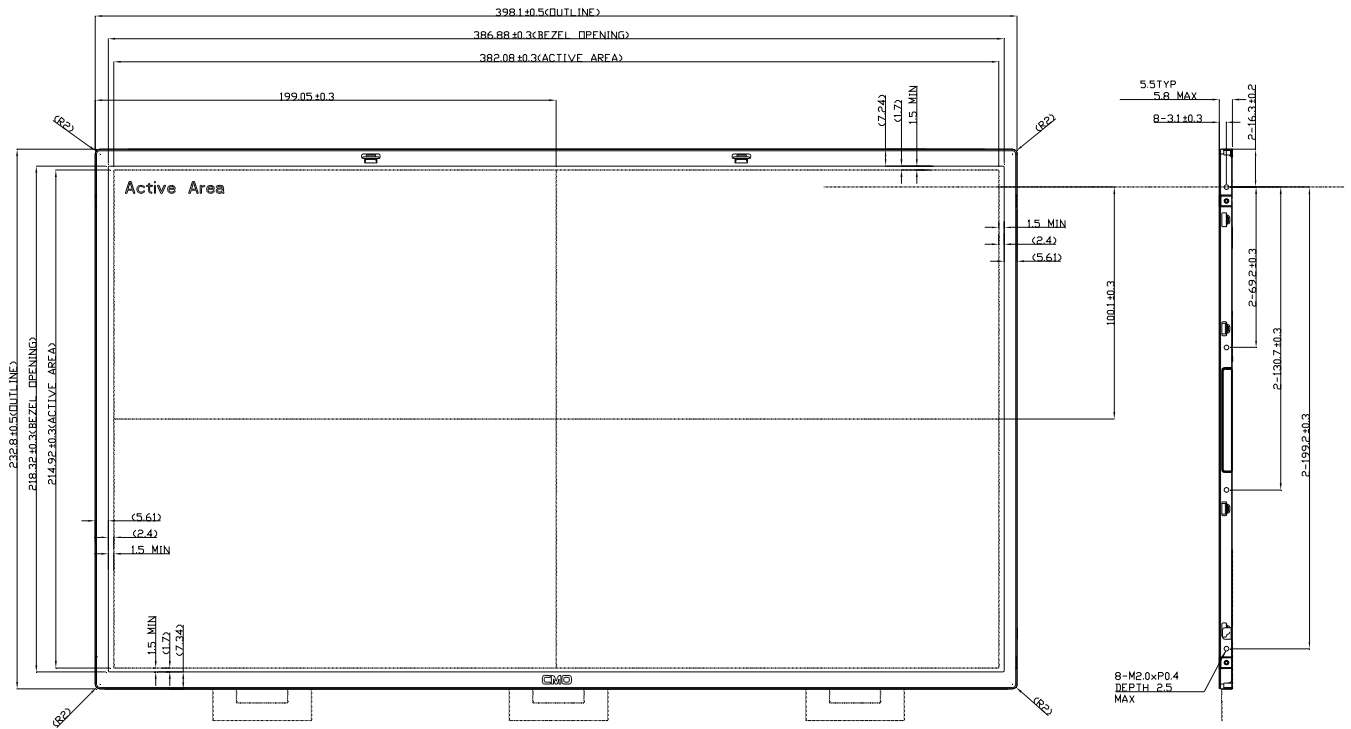
NOTES :
1. MAX SCREW LENGTH : 2.5mm.
2. MAX SCREW TORQUE : 2.0 kgf-cm.
3. LCD MODULE INPUT CONNECTOR : I-PEX 20455-030E-12
4. GAP BETWEEN BEZEL AND PANEL : 0.5mm MAX.
5. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT,
      NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN,
WAN OR
      FOREIGN OBJECTS OVER COF DRIVER IC, T-CON AND VR LOCATIONS.
6. EDP CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
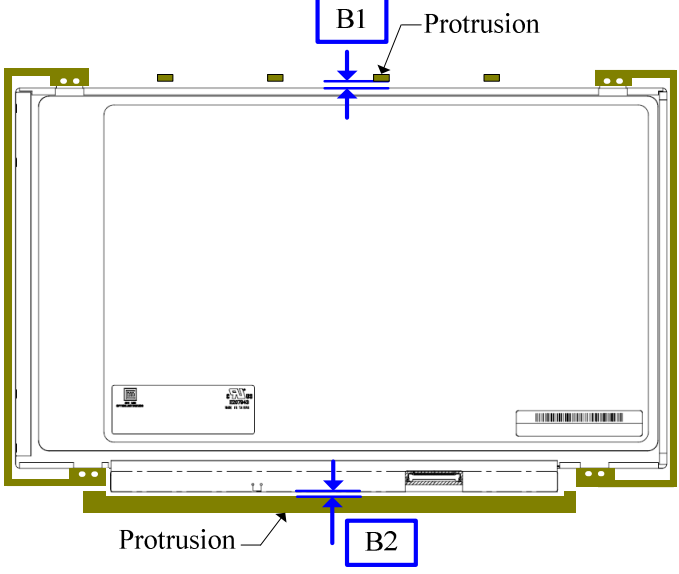7. FLATNESS SPEC 0.5mm MAX.
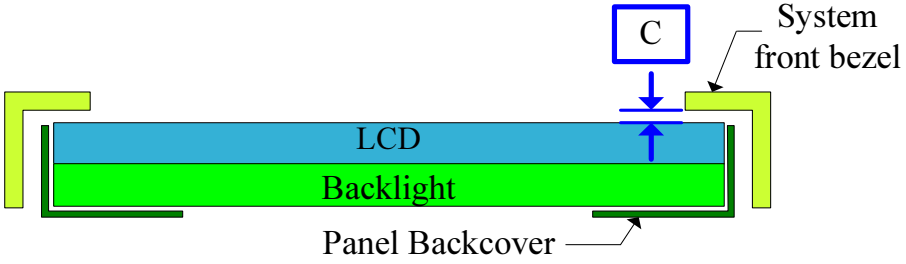8. "( )" MARKS THE REFERENCE DIMENSIONS.

BLU LABEL

MODULE LABEL

LT3E35CN

XX.X

PIN 1

Don't Touch ! 請勿碰觸! Don't Touch ! 請勿碰觸! Don't Touch ! 請勿碰觸! Don't Touch ! 請勿碰觸!

128±1

35±1

10.3

6.3

3-5.3(IC CENTER)

31.94(Conn)

3-17

PCBA LABEL

2

2

3-0.56

12.89(Conn)
70.1(IC CENTER)
150.25(TCON CENTER)
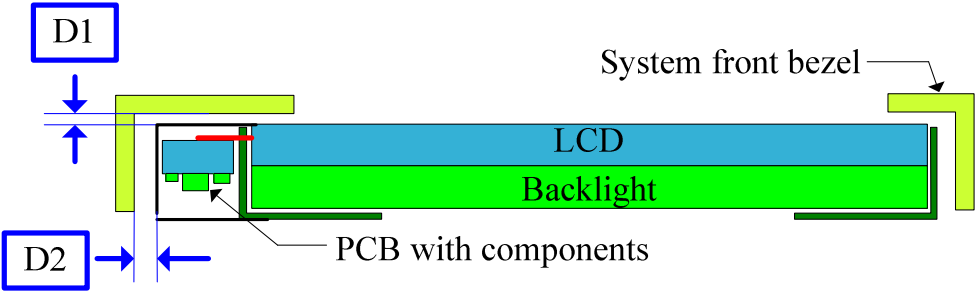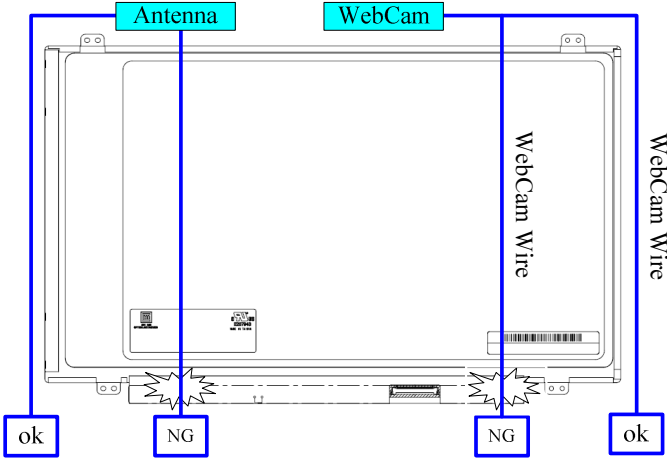198.1(IC CENTER)
326.09(IC CENTER)

46.55(VR CENTER)

25.93(VR CENTER)
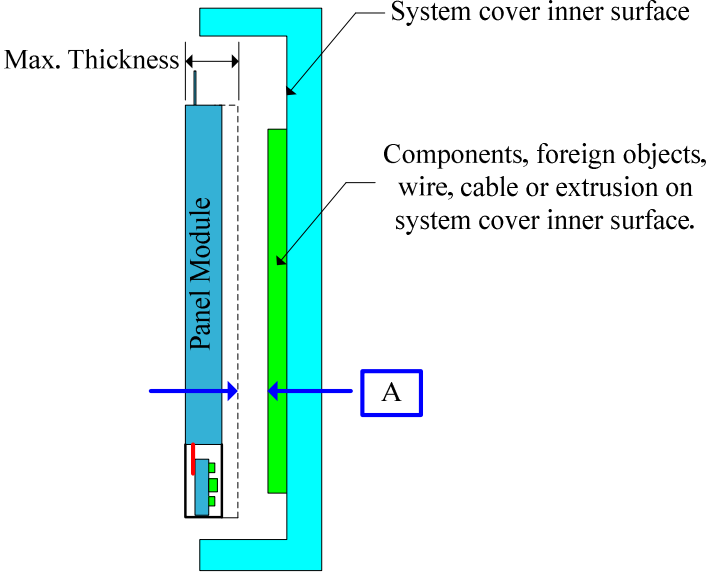
DRIVER IC, COF, TCON, AND VR
LOCATIONS
SEE NOTES FOR EXPLANATION

Appendix. SYSTEM COVER DESIGN NOTICE

1.	Design gap A between panel & any components on system cover

System cover inner surface

Max. Thickness

Panel Module

Components, foreign objects, wire, cable or extrusion on system cover inner surface.

A

Definition	a). Sufficient gap between panel & system is a must for preventing from backpack or pogo test fail. b). Zero gap from panel's maximum thickness boundary to any components, foreign objects, wire, cable or extrusion on system cover inner surface is forbidden.

2	Design gap B1 & B2 between panel & protrusions

B1 Protrusion

Protrusion B2

Definition	2.0mm min. gap is recommended between panel & protrusions for preventing from shock related failures.

3	Design gap C between system front bezel & panel surface.

Definition	a). Sufficient gap between system front bezel & panel surface is a must for preventing from pooling or glass broken. b). Zero gap or interference is forbidden.
4	**Design gap D1 & D2 between system front bezel & PCB Assembly.**

Definition	a). Sufficient gap between system front bezel & PCB assembly is a must for preventing from abnormal display after backpack test, hinge test, twist test or pogo test. b). Zero gap or interference is forbidden.
5	**Interference examination of antenna cable and WebCam wire**

Definition	a). Antenna cable or WebCam wire overlap with panel outline is forbidden for preventing from abnormal display & white spot after backpack test, hinge test, twist test or pogo test. b). Antenna cable or WebCam wire bypass panel outline is recommended.
6	**System inner surface examination**

PRODUCT SPECIFICATION
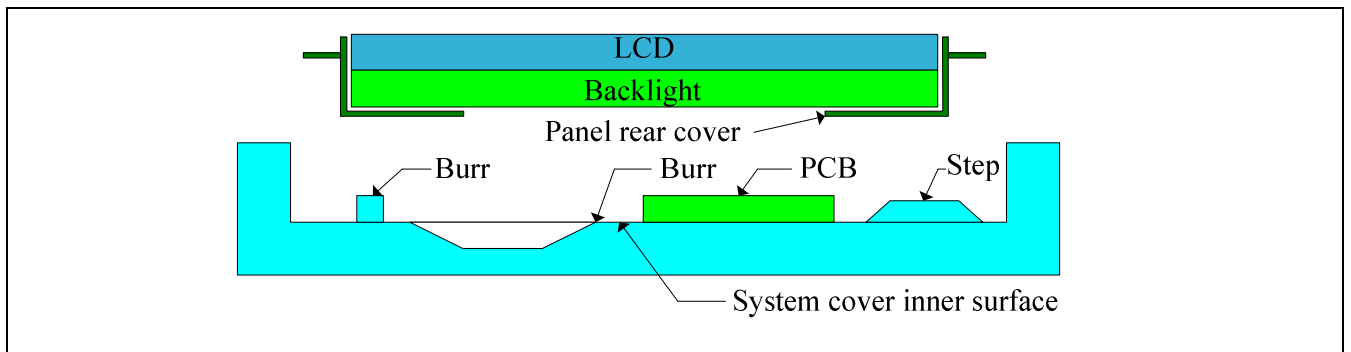
Definition	a). Burr at logo edge, step, protrusion or PCB board will easily cause white spot or glass broken. b). Keeping flat surface underneath backlight is recommended.