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(V) Final Specification

Module 27" Color TFT-LCD			
Model Name M270QAN02.1			
Suffix Name	Q0		
Document version	D07		

Document						
APPROVED BY		Date: May. 11, 2017				
PREPARED BY		Date: May. 11, 2017				

CUSTOMER APPROVED AND FEEDBACK					
CUSTOMER					
APPROVED BY		Date :			

Note: This Specification is subject to change without notice.



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			Record of Revision
Document Version	Date (Y/M/D)	Page	Description
D01	2016/09/23		First Version
D02	2016/10/12	15	Modify $\triangle Vs$ Max. value from 5.4V to 3.6 V
5 02	2010/10/12	22	Modify Connector Pin Assignment Pin 9,10,11 to NC pin.
D03	2016/12/05	5	Modify Panel Weight
200	2010/12/00	6	Modify Color Coordinates
D04	2016/12/23	6	Modify Vertical Viewing Angle
		6	Modify Response Time
D05	2016/12/29	12	Modify Recommended Operating Condition
D06 2017/05/05		6-9	Modify Description of Note
		11	Remove Note 4-3
D07	2017/05/11	30-31	Modify Panel Drawing

1. Handling Precautions

- 1. Since front polarizer is easily damaged, pay attention not to scratch it.
- 2. Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3. Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4. When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5. Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6. Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7. Do not open or modify the Module Assembly.
- 8. Do not press the reflector sheet at the back of the module to any directions.
- 9. In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lightbar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.
- 10. At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11. After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12. Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13. Please avoid touching COF Position while you are doing mechanical design.
- 14. When storing modules as spares for a long time, the following precaution is necessary:
 - a. Store them in a dark place. Do not expose the module to sunlight or fluorescent light.
 - b. Keep the temperature between 5° C and 35° C at normal humidity.

2. General Description



This specification applies to the 27 inch wide color a-Si TFT-LCD Module M270QAN02.1-A000 The display supports the UHD - 3840(H) x 2160(V) screen format and 1.07B colors (RGB 8bits + Hi-FRC). The linput interface is 8-lanes eDP and this module doesn't contain an driver board for backlight.

Display Characteristics

The following items are characteristics summary on the table under 25°C condition:

ITEMS	Unit	SPECIFICATIONS		
Screen Diagonal	mm	684(26.93")		
Active Area mm		596.16 (H) x 335.34 (V)		
Pixels H x V		3840x3(RGB) x 2160		
Pixel Pitch	um	155.25(per one triad) ×155.25		
Pixel Arrangement		R.G.B. Vertical Stripe		
Display Mode		AHVA Mode (Advanced Hyper-Viewing Angle), Normally Black		
White Luminance (Center)	cd/m ²	300 cd/m ² (Typ.)		
Contrast Ratio		1000(Typ.)		
Optical Response Time	msec	12ms (Typ., Gray to Gray)		
Power Consumption (VDD line + LED line)	Watt	Total=27.5 W(Typ) LCD module: PDD (Typ)=10.8 @ white pattern 60 HZ 12V Backlight unit: PBLU (Typ)=16.7@ IS=80 mA		
Color Gamut	%	sRGB 100% (typ)		
Weight	Grams	2380(Typ.)		
Outline Dimension	mm	608.8(H)x354.91(V)x14.58(D)		
Electrical Interface		8-lanes eDP, 10 bits RGB data input (RGB 8bits + Hi-FRC)		
Support Color		1.07B colors		
Surface Treatment		Anti-Glare, 3H		
Temperature Range Operating Storage (Shipping)	°C °C	0 to +50 -20 to +60		
RoHS Compliance		RoHS Compliance		
TCO Compliance		TCO 7.0 Compliance		



Optical Characteristics

The optical characteristics are measured under stable conditions at 25° C:

Test Condition:

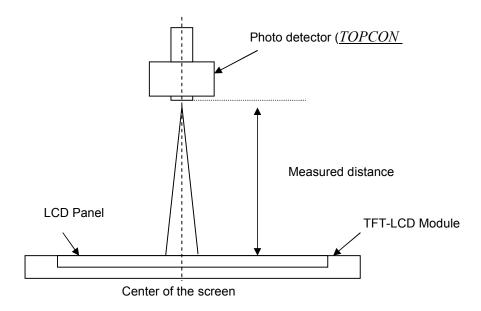
- 1. Equiment setuo: Please refer to Note 2-1
- 2.Panel Lighting:30 Minutes
- 3.DD=12.0V, Fv=60Hz, Is=80mA, Ta=25°C

Symbol	Description		Min.	Тур.	Max.	Unit	Remark
Lw	White Luminance (Cente	er of screen)	240	300	-	[cd/m ²]	Note 2-1
Luni	Luminance Uniformity	(9 points)	75	80	-	[%]	Note 2-2
CR	Contrast Ratio (Center of screen)		600	1000	-	-	Note 2-3
θR	Horizontal Viewing Angle	Right	75	89	-		
θL	(CR=10)	Left	75	89	-		
ΦR	Vertical Viewing Angle	Up	75	89	-		
ФL	(CR=10)	Down	75	89	-	[degree]	
θR	Horizontal Viewing Angle	Right	75	89	-	[degree]	Note 2-4
θL	(CR=5)	Left	75	89	-		
ФR	Vertical Viewing Angle	Up	75	89	-		
ФL	(CR=5)	Down	75	89	-		
Твтв	Response Time	Gray to Gray	-	12	-	[msec]	Note 2-5
Rx		Red x	0.625	0.655	0.685		Note 2-6
Ry		Red y	0.301	0.331	0.361		
Gx		Green x	0.264	0.294	0.324		
Gy	Color Coordinates	Green y	0.589	0.619	0.649		
Bx	(CIE 1931)	Blue x	0.117	0.147	0.177	_	Note 2-0
Ву		Blue y	0.022	0.052	0.082		
Wx		White x	0.283	0.313	0.343		
Wy		White y	0.299	0.329	0.359		
СТ	Crosstalk	-	-	1.5	[%]	Note 2-7	
FdB	Flicker (Center of s	-	-	-20	[dB]	Note 2-8	

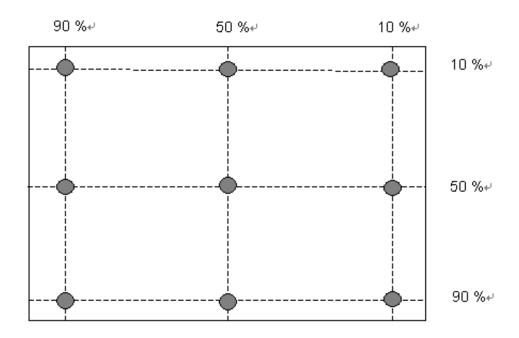


Note 2-1: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring (at surface 35°C). In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 2-2: Luminance uniformity of these 9 points is defined as below and measured by TOPCON SR-3



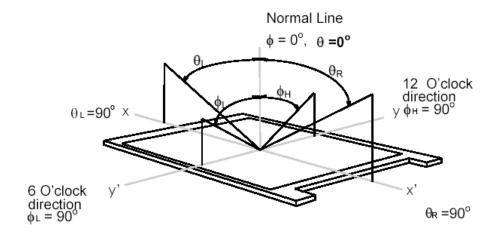
Uniformity = $\frac{\text{Minimum Luminance in 9 points (1-9)}}{\text{Maximum Luminance in 9 Points (1-9)}}$



Note2-3: Contrast ratio is measured by TOPCON SR-3

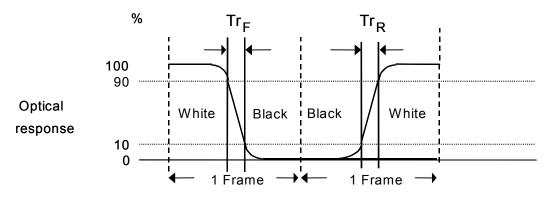
Note 2-4: Definition of viewing angle measured by TOPCON SR-3

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



Note 2-5: Definition of Response time measured by Westar TRD-100

The output signals of photo detector are measured when the input signals are changed from "Black" to



"White" (rising time, T_R), and from "White" to "Black" (falling time, T_F), respectively. The response time is interval between the 10% and 90% of optical response.(*Black & White color definition: Please refer section 3.4.3*)

Note 2-6: Color chromaticity and coordinates (CIE) is measured by TOPCON SR-3

Note 2-7 Crosstalk is defined as below and measured by TOPCON SR-3

Crosstalk measurement

Definition:

 $CT = Max. (CT_H, CT_V);$

Where

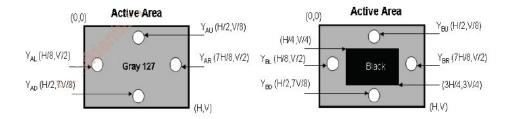
a. Maximum Horizontal Crosstalk:

$$CT_H = Max. (|Y_{BL} - Y_{AL}|/Y_{AL} \times 100 \%, |Y_{BR} - Y_{AR}|/Y_{AR} \times 100 \%);$$

Maximum Vertical Crosstalk:

$$CT_V = Max. (|Y_{BU} - Y_{AU}|/Y_{AU} \times 100 \%, |Y_{BD} - Y_{AD}|/Y_{AD} \times 100 \%);$$

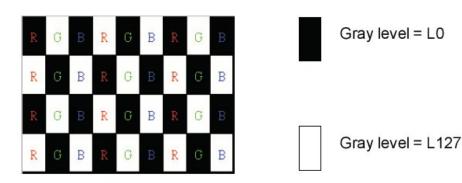
b. Y_{AU} , Y_{AD} , Y_{AL} , Y_{AR} = Luminance of measured location without Black pattern Y_{BU} , Y_{BD} , Y_{BL} , Y_{BR} = Luminance of measured location with Black pattern



Note 2-8: Test Patern: Subchecker Pattern measured by TOPCON SR-3

Flicker measurement

a. Test pattem: It is listed as following.



R: Red, G: Green, B:Blue

b. Measured position: Center of screen & perpendicular to the screen

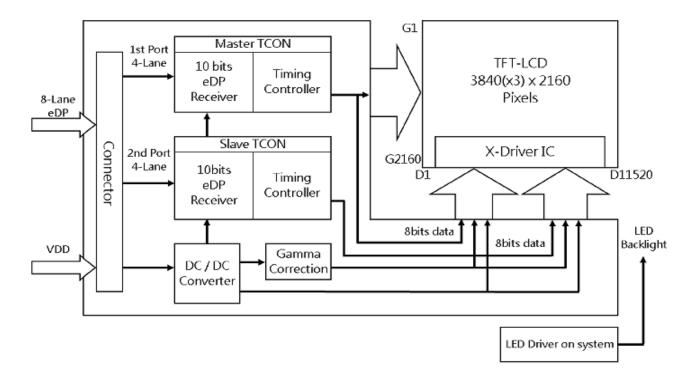


3. Functional Block Diagram

3.TFT-LCD

3-1. Block Diagram

The following shows the block diagram of the 27.0 inch Color TFT-LCD Module.



4. Absolute Maximum Ratings

Backlight Unit

	Symbol	Min	Тур	Max	Unit	Conditions
LED Current	ILED	-	80	120	[mA]	Note 4-1,4-2

Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	
Center Glass Surface temperature (Operation)	TGS	0	+65	[°C]	
Operation Humidity	НОР	5	90	[%RH]	
Storage Temperature	TST	-20	+60	[°C]	
Storage Humidity	HST	5	90	[%RH]	

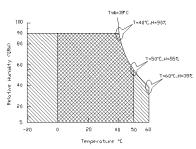
Note 4-1: With in Ta (25 ℃)

Note 4-2: Permanent damage to the device may occur if exceeding maximum values

. 1. 90% RH Max (Ta ≤39°C)

2. Max wet-bulb temperature at 39°C or less (1'a ≤ 39 °C)

3. No condensation



Operating Range



Storage Range



5. Electrical characteristics-TFT LCD Module

Power Specification – TFT-LCD

Input power specifications are as following:

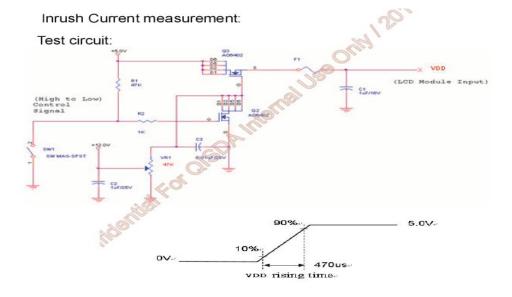
5.1 Absolute Maximum Rating

Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14	[Volt]	Ta=25°C

5.2 Recommended Operating Condition

Symbol	Description	Min	Тур	Max	Unit	Remark
VDD	Power Supply Input Voltage	10.8	12	13.2	[Volt]	
IDD	Power Supply Input Current (RMS)	1	0.9	1.08	[A]	VDD= 12.0V, White Pattern, Fv= 60Hz
PDD	VDD Power Consumption	1	10.8	12.96	[Watt]	VDD= 12.0V, White Pattern, Fv= 60Hz
IRush	Inrush Current	-	-	3.0	[A]	Note 5-1
VDDrp	Allowable LCD Ripple Voltage	1	-	VDD*5%	[mV]	VDD= 12.0V, White Pattern, Fv= 60Hz

Note 5-1: Measurement conditions:



The duration of VDD rising time: 470us.



5.3 LCD Pixel Format

Following figure shows the relationship between the input signals and LCD pixel format.

	1st Lane0 ↓	1st Lane1 ↓	1st Lane2 ↓	1st Lane3 ↓		2nd LaneO	↓	↓	↓	2040
					 1920	1921	1922	1923	1924	 3840
1	R G B	R G B	R G B	R G B	 R G B	R G B	R G B	R G B	R G B	 R G B
+										
2160	R G B	R G B	R G B	R G B	 R G B	R G B	R G B	R G B	R G B	 R G B

5.4 eDP Data Format

1st Lane0	1st Lane1	1st Lane?	1st Lane3		
R1-9:2	R2-9:2	R3-9:2	R4-9:2		
R1-1:0IG1-9:4	R2-1:0/G2-9:4	R3-1:0IG3-9:4	R4-1:0/G4-9:4		
G1-3:0IB1-9:6	G2-3:0IB2-9:6	G3-3:0IB3-9:6	G4-3:0IB4-9:6		
B1-5:0IR5-9:8	B2-5:0IR6-9:8	B3-5:0IR7-9:8	B4-5:0IR8-9:8		
RS-7:0	R6-7:0	R7-7:0	R8-7:0		
GS-9:2	G6-9:2	G7-9:2	G8-9:2		
GS-1:0IBS-9:4	G6-1:0IB6-9:4	G7-1:0IB7-9:4	G8-1:0IB8-9:4		
B5-3:0IR9-9:6	B6-3:0IR10-9:6	B7-3:0IR11-9:6	B8-3:0IR12-9:6		
R9-5:0109-9:8	R10-5:00G10-9:8	R11-5:0IG11-9:8	R12-5:0(G12-9:8		
G9-7:C	G10-7:0	G11-7:0	G12-7:0		
B9-9:2	B10-9:2	B11-9:2	B12-9:2		
B9-1:0R13-9:4	B10-1:0IR14-9:4	B11-1:0IR15-9:4	B12-1:0IR16-9:4		
R13-3:01G13-9:6	R14-3:00G14-9:6	R15-3:0IG15-9:6	R16-3:0/G16-9:6		
G13-5:01B13-9:8	G14-5:0IB14-9:8	G15-5:0(B15-9:8	G16-5:0IB16-9:8		
B13-7:0	B14-7:0	B15-7:0	B16-7:0		
	. .				

2nd Lane0	2nd Lanel	2nd Lane2	2nd Lane3
R1921-9:2	R1922-9:2	R1923-9:2	R1924-9:2
R1921-1:0/G1921-9:4	R1922-1:0/G1922-9:4	R1923-1:01G1923-9:4	R1924-1:0lG1924-9:4
G1921-3:0IB1921-9:6	G1922-3:01B1922-9:6	G1923-3:0IB1923-9:6	G1924-3:0IB1924-9:6
B1921-5:0IR1925-9:8	B1922-5:0IR1926-9:8	B1923-5:0IR1927-9:8	B1924-5:0IR1928-9:8
R1925-7:0	R1926-7:0	R1927-7:0	R1928-7:0
G1925-9:2	G1926-9:2	G1927-9:2	G1928-9:2
G1925-1:0IB1925-9:4	G1926-1:0IB1926-9:4	G1927-1:0IB1927-9:4	G1928-1:0IB1928-9:4
B1925-3:0IR1929-9:6	B1926-3:0IR1930-9:6	B1927-3:0IR1931-9:6	B1928-3:0IR1932-9:6
R1929-5:01G1929-9:8	R1930-5:0(G1930-9:8	R1931-5:0IG1931-9:8	R1932-5:0IG1932-9:8
G1929-7:0	G1930-7:0	G1931-7:0	G1932-7:0
B1929-9:2	B1930-9:2	B1931-9:2	B1932-9:2
B1929-1:0IR1933-9:4	B1930-1:0IR1934-9:4	B1931-1:0IR1935-9:4	B1932-1:0IR1936-9:4
R1933-3:0IG1933-9:6	R1934-3:00G1934-9:6	R1935-3:0IG1935-9:6	R1936-3:0IG1936-9:6
G1933-5:0IB1933-9:8	G1934-5:0IB1934-9:8	G1935-5:0IB1935-9:8	G1936-5:0IB1936-9:8
B1933-7:0	B1934-7:0	B1935-7:0	B1936-7:0

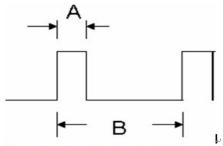


Power Specification - LED Back light

5.5 Absolute Maximum Rating

Parameter damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
lo	LED String Current	0	150	[mA]	100% duty ratio
Is	LED String Current	O	300	[mA]	Duty ratio 10% Pulse time=10ms



Duty ratio= (A / B) X 100%; (A: Pulse time, B: Period)

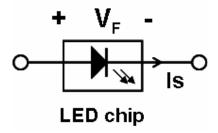
5.5.1 Parameter guideline for LED driving is under stable conditions at 25° C (Room Temperature):

Symbol	Parameter	Min.	Тур.	Max.	Unit	Note
IR _{LED}	LED Operation Current		80	88	[mA]	
V _{LB}	Light Bar Operation Voltage (for reference)	46.8	52.2	57.6	[Volt] Note 7-1 Note 7-5	0 11 11
ΔVs	Maximum Vs Voltage Deviation of light bar			3.6	[Volt] Note 7-2	Operating with fixed driving current
P _{BLU}	BLU Power consumption (for reference)		16.7	18.43	[Watt] Note 7-3	
LT _{LED}	LED life Time (Typical)			-	[Hour] Note 7-4	

Note 7-1: Vs (Typ.) = VF (Typ.) X LED No. (one string);

- a. V_F : LED chip forward voltage, V_F (Min.)=2.6V, V_F (Typ.)=2.9V, V_F (Max.)=3.2V
- b. The same euqation to calculate Vs(Min.) & Vs (Max.) for respective V_F (Min.) & V_F (Max.);





Note 7-2: ΔVs (Max.) = ΔVF X LED No. (one string);

of LED string voltage (Vs) at least.

- a. ΔVF: LED chip forward voltage deviation; (0.2 V, each Bin of LED VF)
- **Note 7-3:** P_{BLU} (Typ.) = Vs (Typ.) X Is (Typ.) X 4; (4 is total String No. of LED Light bar) P_{BLU} (Max.) = Vs (Max.) X Is (Typ.) X 4;
- Note 7-4: Definition of life time:
 - a. Brightness of LED becomes to 50% of its original value
 - b. Test condition: Is = 80mA and 25°C (Room Temperature)
- Note 7-5: Recommendation for LED driver power design:

 Due to there are electrical property deviation in LED & monitor set system component after long time operation. AUO strongly recommend the design value of LED driver board OVP (over voltage protection) should be 10% higher than max. value
- **Note 7-6:** AUO strongly recommend "Analog Dimming" method for backlight brightness control for Wavy Noise Free. Otherwise, recommend that Dimming Control Signal (PWM Signal) should be synchronized with Frame Frequency.



6. Signal Characteristic

3.4.3 Color versus Input Data

The following table is for color versus input data (10bit). The higher the gray level, the brighter the color.

															Col	or In	out [)ata														
Color	Gary Level						data 9, LSE	a 3:R0))					ı		REEI B:G9						0			(MS	B:B9			ı			Remark
		R9	R8	R7	R6	R5	R4	R3	R2	R1	RO	G9	G8	G7	G6	G5	G4	G3	G2	G1	GO	В9	В8	В7	В6	B5	В4	ВЗ	В2	В1	ВО	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
L511		0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	
	LO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
Red	:	14	81	:	:	:	:	:	13	:	:	:	:	ः	:	:	33	:	٠	183	:	:	:	:	:	:	:	y:	:	:	:	
	L1023	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	LO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	o	Black
Green		123	21	:	:	is:	,31	1	8	83	3	10	11.	::	1	10	72	.:	8	\$5	::	:	:0	:::	:	:	:	83	,di	:	10	
	L1023	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
	LO	0	٥	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
Blue	:	100	1	:	:		1	;	1	ः		:	:	:	:	i	ं	:	:	1	1	:	:	4	:	:	:	9	3	1	8	
	L1023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	

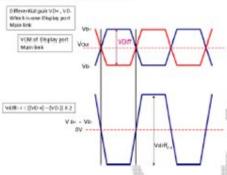


6.2 eDP Specification (Follow as VESA Displayport Standard Version 1.1)

eDP Specification

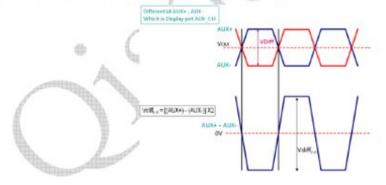
a. DisplayPort main link signal:

	DisplayPort main link				
		Min	Тур	Max	unit
VCM	RX input DC Common Mode Voltage	0	-	2.0	V
VDiff _{P-P}	Peak-to-peak Voltage at a receiving Device	150	-		mV



b. DisplayPort AUX_CH signal:

	DisplayPort AUX_CH				
A 25	A (%	Min	Тур	Max	unit
VCM	AUX DC Common Mode Voltage	0	-	2.0	٧
VDiff _{P-P}	AUX Peak-to-peak voltage at a receiving device	0.27		1.36	٧



c. DisplayPort VHPD signal:

	DisplayPo	ort VHPD			
		Min	Тур	Max	unit
VHPD	HPD Voltage	2.25	<u></u>	3.6	٧

6.3 Input timing is shown as the following table

The input timing is shown as the following table.

Symbol	Description	on	Min.	Тур.	Max.	Unit	Remark
Tv		Period	2180	2200	4500	Th	
Tdisp (v)		Active	2160	2160	2160	Th	
Tblk (v)	Vertical Section	Blanking	20	40	2340	Th	
Fv		Frequency	29	60	65	Hz	Note 3-6 Note 3-7
Th		Period	2000	2100	3520	Tclk	The same of the sa
Tdisp (h)	Horizontal Section	Active	1920	1920	1920	Tclk)
Tblk (h)	Horizontal Section	Blanking	80	180	1600	Tclk	(0)
Fh		Frequency	40	132	151	kHz	Note 3-4
Tclk	Pixel Clock	Period	3.330	3.608	12.500	ns	1/Fclk
Fclk	Pixel Olock	Frequency	80	277	300.3	MHz	Note 3-5
	Link Rate per Lane		Apr.	2.7	60	Gbps	3 1

Note 3-4: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = Fclk (Min.) / Th (Min.)

Fh (Typ.) = Fclk (Typ.) / Th (Typ.) Fh (Max.)= Fclk (Max.) / Th (Min.)

Note 3-5: The equation is listed as following. Please don't exceed the above recommended value.

1st Lane N & 2nd Lane N skew < 200ns

Fclk (Typ.) = Fv (Typ.) x Th (Typ.) x Tv (Typ.)

Fclk (Min.) ≤ Fv x Th x Tv ≤ Fclk (Max.)

Note 3-6: The equation is listed as following. Please don't exceed the above recommended value.

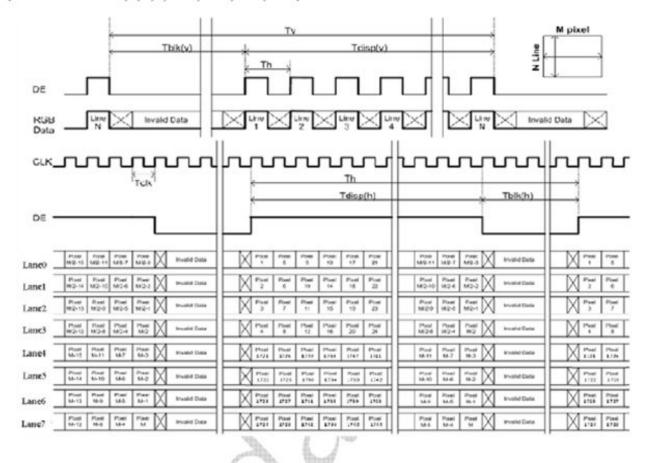
Fv =Fclk(Typ.) / (Tv x Th)

Note 3-7: The optimal Vertical Frequency is 50~65 Hz for best picture quality.



Timing diagram

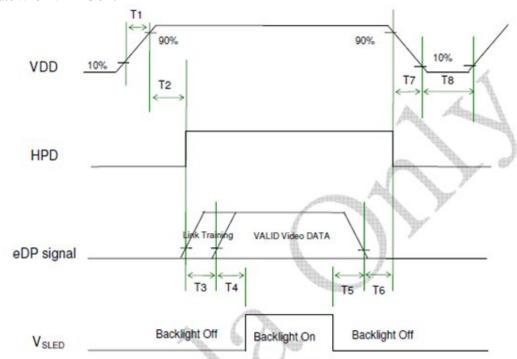
(Lane0-7 eDP data:1, 2, 3, 4, 1921, 1922, 1923, 1924)





6.4 Power ON/OFF Sequence

VDD power,eDP signal and backlight on/off sequence are as following. eDP signals from any system shall be Hi-Z state when VDD is off.



Power Sequence Timing

Cumbal	1	Value			Remark
Symbol	Min.	Typ.	Max.	Unit	
T1	0.5	9 -	10	[ms]	
T2	0	-	200	[ms]	
T3	0	-	-	[ms]	Note 3-8
T4	500	-	-	[ms]	
T ₅	100	-	-	[ms]	
T6	0		50	[ms]	Note 3-9 Note 3-10
T7	0	-	200	[ms]	Note 3-10 Note 3-11
T8	1000		-	[ms]	

Note 3-8: During T3 period, eDP link training time by customer's system.

Note 3-9: Recommend setting T6 = 0ms to avoid electronic noise when VDD is off.

Note 3-10: During T6 and T7 period , please keep the level of input eDP signals with Hi-Z state.

Note 3-11: Voltage of VDD must decay smoothly after power-off.(customer system decide this value)



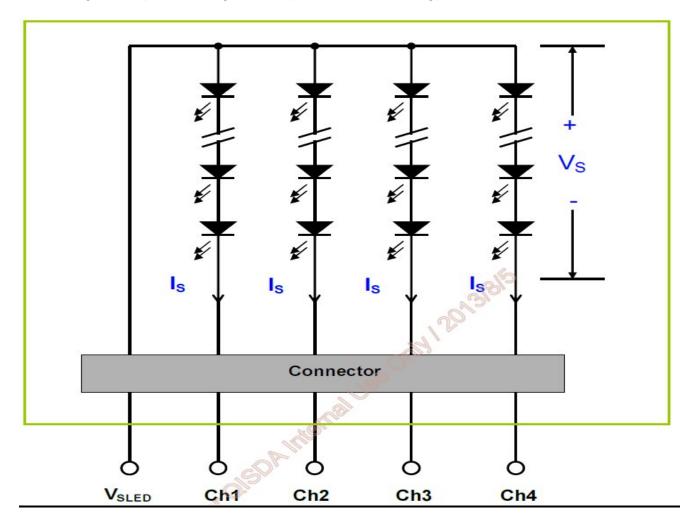
7. Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

TFT LCD Module

7.1 Block Diagram

The following shows the block diagram of the 27 inch Backlight Unit. And it includes 72pcs LED in the LED light bar 2pcs. (4 strings and 18 pcs LED of one string).



TFT-LCD	Manufacturer	P-TWO	JAE
Connector	Part Number	187059-5122	FI-RTE51SZ-HF
Mating	Manufacturer	JAE or o	ompatible
Connector	Part Number	FI-RI	E51CL 4

7.2.1 Connector Pin Assignment

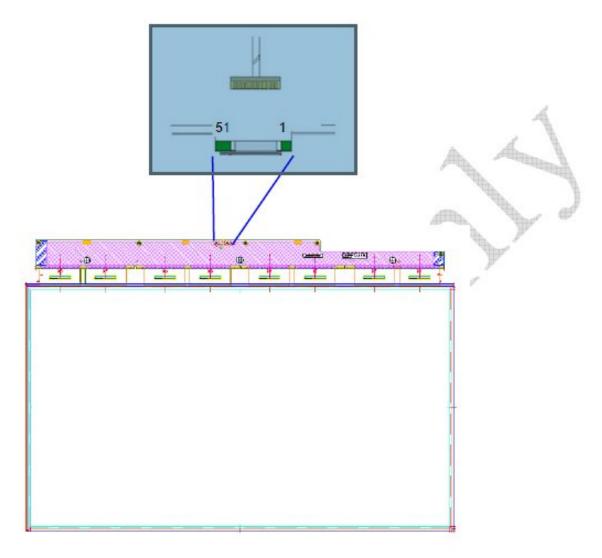
PIN#	Symbol	Description	Remark
1	VDD	Power +12V	23
2	VDD	Power +12V	V
3	VDD	Power +12V	
4	VDD	Power +12V	
5	VDD	Power +12V	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	NC	No connection (for AUO test only. Do not connect)	
10	NC	No connection (for AUO test only. Do not connect)	
11	NC	No connection (for AUO test only. Do not connect)	
12	NC	No connection (for AUO test only. Do not connect)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	NC	No connection (for AUO test only. Do not connect)	
16	NC	No connection (for AUO test only. Do not connect)	
17	GND	Ground	
18	1st Lane3_N	Negative eDP differential data input	
19	1st Lane3_P	Positive eDP differential data input	
20	GND	Ground	



1st Lane2_P Positive eDP differential data input GND Ground 1st Lane1_N Negative eDP differential data input forum 1st Lane1_P Positive eDP differential data input GND Ground Tst Lane0_N Negative eDP differential data input St Lane0_P Positive eDP differential data input SND Ground Tst Lane0_P Positive eDP differential data input GND Ground 1st AUX_CH_P Positive AUX Channel differential data input Tst AUX_CH_N Negative AUX Channel differential data input GND Ground NC No connection (for AUO test only. Do not connect) AGND Ground SOUND Ground COND COND COND COND COND COND COND COND			
GND Ground 24 1st Lane1_N Negative eDP differential data input 25 1st Lane1_P Positive eDP differential data input 26 GND Ground 27 1st Lane0_N Negative eDP differential data input 28 1st Lane0_P Positive eDP differential data input 29 GND Ground 30 1st AUX_CH_P Positive AUX Channel differential data input 31 1st AUX_CH_N Negative AUX Channel differential data input 32 GND Ground 33 NC No connection (for AUO test only. Do not connect) 34 GND Ground 35 2nd Lane3_N Negative eDP differential data input 36 2nd Lane3_P Positive eDP differential data input 37 GND Ground 38 2nd Lane2_N Negative eDP differential data input 39 2nd Lane2_P Positive eDP differential data input 40 GND Ground 41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	21	1st Lane2_N	Negative eDP differential data input
24 1st Lane1_N Negative eDP differential data input 25 1st Lane1_P Positive eDP differential data input 26 GND Ground 27 1st Lane0_N Negative eDP differential data input 28 1st Lane0_P Positive eDP differential data input 29 GND Ground 30 1st AUX_CH_P Positive AUX Channel differential data input 31 1st AUX_CH_N Negative AUX Channel differential data input 32 GND Ground 33 NC No connection (for AUO test only. Do not connect) 34 GND Ground 35 2nd Lane3_N Negative eDP differential data input 36 2nd Lane3_P Positive eDP differential data input 37 GND Ground 38 2nd Lane2_N Negative eDP differential data input 39 2nd Lane2_P Positive eDP differential data input 40 GND Ground 41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	22	1st Lane2_P	Positive eDP differential data input
25	23	GND	Ground
26 GND Ground 27 1st Lane0_N Negative eDP differential data input 28 1st Lane0_P Positive eDP differential data input 29 GND Ground 30 1st AUX_CH_P Positive AUX Channel differential data input 31 1st AUX_CH_N Negative AUX Channel differential data input 32 GND Ground 33 NC No connection (for AUO test only. Do not connect) 34 GND Ground 35 2nd Lane3_N Negative eDP differential data input 36 2nd Lane3_P Positive eDP differential data input 37 GND Ground 38 2nd Lane2_N Negative eDP differential data input 39 2nd Lane2_P Positive eDP differential data input 40 GND Ground 41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	24	1st Lane1_N	Negative eDP differential data input
1st Lane0_N Negative eDP differential data input Rond Ground St AUX_CH_P Positive AUX Channel differential data input St AUX_CH_N Negative AUX Channel differential data input Rond Ground St AUX_CH_N Negative AUX Channel differential data input Rond Ground Rond Rond Ground Rond Rond Rond Rond Rond Rond Rond Rond	25	1st Lane1_P	Positive eDP differential data input
28 1st Lane0_P Positive eDP differential data input 29 GND Ground 30 1st AUX_CH_P Positive AUX Channel differential data input 31 1st AUX_CH_N Negative AUX Channel differential data input 32 GND Ground 33 NC No connection (for AUO test only. Do not connect) 34 GND Ground 35 2nd Lane3_N Negative eDP differential data input 36 2nd Lane3_P Positive eDP differential data input 37 GND Ground 38 2nd Lane2_N Negative eDP differential data input 39 2nd Lane2_P Positive eDP differential data input 40 GND Ground 41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	26	GND	Ground
GND Ground 1st AUX_CH_P Positive AUX Channel differential data input 1st AUX_CH_N Negative AUX Channel differential data input GND Ground No connection (for AUO test only. Do not connect) A GND Ground Conductor of Aux Channel differential data input Conductor of Conductor of Aux Channel differential data input Conductor of Conductor of Conductor of Conductor of Conductor of Conductor o	27	1st Lane0_N	Negative eDP differential data input
1st AUX_CH_P Positive AUX Channel differential data input 1st AUX_CH_N Negative AUX Channel differential data input 3c GND Ground 3n NC No connection (for AUO test only. Do not connect) 3n GND Ground 3n Degative eDP differential data input 3n Cend Lane3_N Negative eDP differential data input 3n Cend Lane3_P Positive eDP differential data input 4n Cend Lane3_P Positive AUX Channel differential data input 4n Cend AUX_CH_P Positive AUX Channel differential data input	28	1st Lane0_P	Positive eDP differential data input
31	29	GND	Ground
32 GND Ground 33 NC No connection (for AUO test only. Do not connect) 34 GND Ground 35 2nd Lane3_N Negative eDP differential data input 36 2nd Lane3_P Positive eDP differential data input 37 GND Ground 38 2nd Lane2_N Negative eDP differential data input 39 2nd Lane2_P Positive eDP differential data input 40 GND Ground 41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	30	1st AUX_CH_P	Positive AUX Channel differential data input
33 NC No connection (for AUO test only. Do not connect) 34 GND Ground 35 2nd Lane3_N Negative eDP differential data input 36 2nd Lane3_P Positive eDP differential data input 37 GND Ground 38 2nd Lane2_N Negative eDP differential data input 39 2nd Lane2_P Positive eDP differential data input 40 GND Ground 41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	31	1st AUX_CH_N	Negative AUX Channel differential data input
34 GND Ground 35 2nd Lane3_N Negative eDP differential data input 36 2nd Lane3_P Positive eDP differential data input 37 GND Ground 38 2nd Lane2_N Negative eDP differential data input 39 2nd Lane2_P Positive eDP differential data input 40 GND Ground 41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	32	GND	Ground
35 2nd Lane3_N Negative eDP differential data input 36 2nd Lane3_P Positive eDP differential data input 37 GND Ground 38 2nd Lane2_N Negative eDP differential data input 39 2nd Lane2_P Positive eDP differential data input 40 GND Ground 41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	33	NC	No connection (for AUO test only. Do not connect)
36 2nd Lane3_P Positive eDP differential data input 37 GND Ground 38 2nd Lane2_N Negative eDP differential data input 39 2nd Lane2_P Positive eDP differential data input 40 GND Ground 41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	34	GND	Ground
GND Ground 38 2nd Lane2_N Negative eDP differential data input 39 2nd Lane2_P Positive eDP differential data input 40 GND Ground 41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	35	2nd Lane3_N	Negative eDP differential data input
2nd Lane2_N Negative eDP differential data input 2nd Lane2_P Positive eDP differential data input 40 GND Ground 41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	36	2nd Lane3_P	Positive eDP differential data input
39 2nd Lane2_P Positive eDP differential data input 40 GND Ground 41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	37	GND	Ground
40 GND Ground 41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	38	2nd Lane2_N	Negative eDP differential data input
41 2nd Lane1_N Negative eDP differential data input 42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	39	2nd Lane2_P	Positive eDP differential data input
42 2nd Lane1_P Positive eDP differential data input 43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	40	GND	Ground
43 GND Ground 44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	41	2nd Lane1_N	Negative eDP differential data input
44 2nd Lane0_N Negative eDP differential data input 45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	42	2nd Lane1_P	Positive eDP differential data input
45 2nd Lane0_P Positive eDP differential data input 46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	43	GND	Ground
46 GND Ground 47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	44	2nd Lane0_N	Negative eDP differential data input
47 2nd AUX_CH_P Positive AUX Channel differential data input 48 2nd AUX_CH_N Negative AUX Channel differential data input	45	2nd Lane0_P	Positive eDP differential data input
48 2nd AUX_CH_N Negative AUX Channel differential data input	46	GND	Ground
	47	2nd AUX_CH_P	Positive AUX Channel differential data input
49 GND Ground	48	2nd AUX_CH_N	Negative AUX Channel differential data input
TO CITE CITED IN	49	GND	Ground



50	HPD	Hot plug detection	
51	GND	Ground	



Note: input signals of port 1 to port 4 clocks shall be the same timing



7.3 LED Connector Type

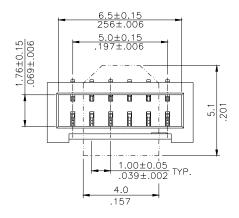
This connector is mounted on LED light-bar.

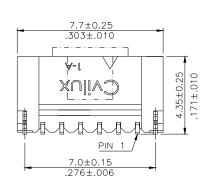
Connector Name / Designation	Light Bar Connector
Manufacturer	CVILUX
Type Part Number	CI1406M1VL0-NH

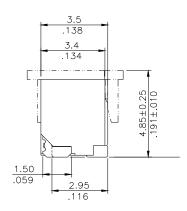
7.3.1 LED Connector Pin Assignment

Pin#	Symbol	Description	Remark
1	Ch1	LED Current Feedback Terminal (Channel 1)	
2	Ch2	LED Current Feedback Terminal (Channel 2)	
3	V _{SLED}	LED Power Supply Voltage Input Terminal	
4	V _{SLED}	LED Power Supply Voltage Input Terminal	A 1
5	Ch3	LED Current Feedback Terminal (Channel 3)	January .
6	Ch4	LED Current Feedback Terminal (Channel 4)	()

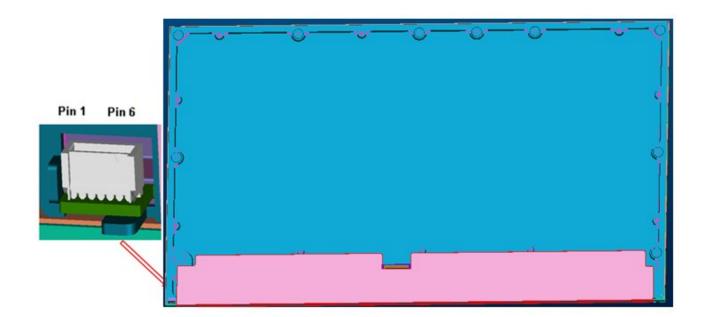
7.3.2 Backlight Connector dimension:













8. Reliability Test

Environment test conditions are listed as following Monitor test condition.

Items	Required Condition	Note	
Temperature Humidity Bias (THB)	Ta= 50°C, 80%RH, 300 hours		
High Temperature Operation (HTO)	Ta= 50°C, 50%RH, 300 hours		
Low Temperature Operation (LTO)	Ta= 0°C, 300 hours		
High Temperature Storage (HTS)	Ta= 60°C, 300 hours		
Low Temperature Storage (LTS)	Ta= -20°C, 300 hours	<	
Vibration Test (Non-operation)	Acceleration: 1.5 Grms Wave: Random Frequency: 10 - 200 Hz Duration: 30 Minutes each Axis (X, Y, Z)		
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)		
Drop Test	Height: 46 cm, package test		
Thermal Shock Test (TST)	-20°C/30min, 60°C/30min, 100 cycles	Note 1	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles		
ECD (Electro Ctatic Discharge)	Contact Discharge: ± 15KV, 150pF(330Ω) 1sec, 15 points, 25 times/ point		
ESD (Electro Static Discharge)	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 15 points, 25 times/ point	Note 2	
Altitude Test	Operation: 18,000 ft Non-Operation: 40,000 ft		

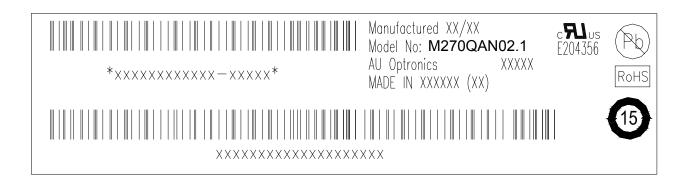
Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: EN61000-4-2, ESD class B: Certain performance degradation allowed:

- No data lost
- Self-recoverable
- No hardware failures



9. Shipping label



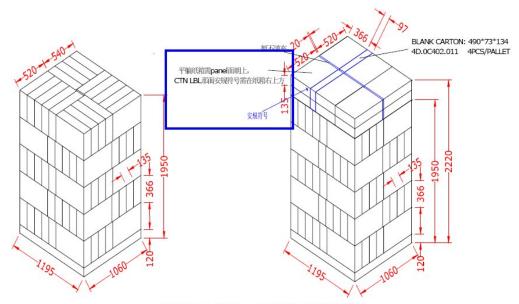
- *Note 9-1:* For Pb Free products, AUO will add for identification.
- *Note 9-2:* For RoHS compatible products, AUO will add RoHS for identification.
- *Note 9-3:* For China RoHS compatible products, AUO will add 65 for identification.
- *Note 9-4:* The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.



10. Packing Precautions

TFT-LCD Module (or monitor) should be stand or be placed face up in traffic or storage conditions; please do not keep TFT-LCD Module face down (polarizer side down).

Monitor maker should add the notice above in packing description; See the configuration example as below:



栈板尺寸参照: 1199*1061*120

18*5+12=102 PCS

