Coversheet

MODEL NO. : G1548FH101GF-001

ISSUED DATE: 2016-11-15

VERSION : A0

■**Preliminary Specification**

□**Final Product Specification**

Customer :_____

Approved by	Notes

GVO Confirmed :

Prepared by	Checked by	Approved by

This technical specification is subjected to change without notice.

Table of Contents

Record of Revision

Rev	Issue Date	Description	Editor
A0	2016.11.15	Draft	Zhao Tianyu

1 General Specifications

Feature		Spec	Remark
Display Spec	Screen Size (inch)	5.48	
	Display Mode	AMOLED	
	Resolution(dot)	1080(W)×1920(H)	
	Active Area(mm)	68.256(W)×121.344 (H)	
	Pixel Pitch (um)	94.8 (W)×63.2(H)	
	Technology Type	LTPS	
	Color Depth	16.7M	
	Interface	MIPI 4LANE	
	Surface Treatment	Hard Coating	
Mechanical Characteristics	With TP/Without TP	With TP(on Cell)	
	Module Outline Dimension(W x H x D) (mm)	73.56 (W)x148.86(H)x1.92(D)	Including Cover lens
	Weight (g)	TBD	
Electronic	Driver IC(Type)	RM67198	
	Touch IC(Type)	GT1151	

Note 1: Requirements on Environmental Protection: RoHS.

2 Input/output Terminals

2.1 Main FPC Pin Assignment

FPC connector: AXE340124, B-TO-B Connector.

Main board recommended connector: AXE440124 B-TO-B Connector.

No	Symbol	I/O	Description
1	VPP	P	Power supply for MTP Programming or Erase. If it is not used please open it.
2	D3N	I	MIPI data lane
3	NC		NC
4	D3P	I	MIPI data lane
5	ELON2	O	DC/DC Power IC S-Wire CTRL Pin
6	GND	GND	Ground
7	VDDP_EN	O	DC/DC Power Enable Pin
8	D0N	I/O	MIPI data lane
9	PCD	O	Panel Crack Detection Pin
10	D0P	I/O	MIPI data lane
11	TE	I	Sync Signal for preventing Tearing Effect
12	GND	GND	Ground
13	ERR_FG	O	MIPI Error Pin
14	CKN	I	MIPI clock lane
15	RESX	I	Display reset. Active low.
16	CKP	I	MIPI clock lane
17	VDDIO	P	Power supply for display logic circuits
18	GND	GND	Ground
19	TSP_1.8V	P	Power supply for display logic circuits
20	D1N	I	MIPI data lane
21	VLIN_6.5V	P	External Power Input for AVDD
22	D1P	I	MIPI data lane
23	VCI	P	Power supply for display analog circuits
24	GND	GND	Ground
25	TSP_SDA	I/O	SDA pin for TP

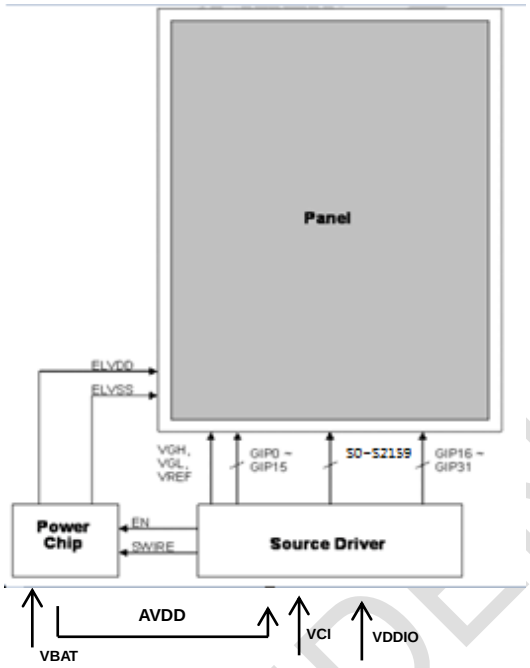
26	D2N	I	MIPI data lane
27	TSP_SCL	I	SCL pin for TP
28	D2P	I	MIPI data lane
29	TSP_ATTN	I	INT pin for TP
30	GND	GND	Ground
31	TSP_ 3.3V	P	Analog Power for TP
32	TSP_RESET	I	Reset Pin for TP, Active low.
33	TSP_1.8V	P	Power supply for TP logic circuits
34	NC		NC
35	ELVDD	P	Positive power supply for EL
36	ELVSS	P	Negative power supply for EL
37	ELVDD	P	Positive power supply for EL
38	ELVSS	P	Negative power supply for EL
39	ELVDD	P	Positive power supply for EL
40	ELVSS	P	Negative power supply for EL

Note: I=Input; O=Output; P=Power; I/O=Input / Output

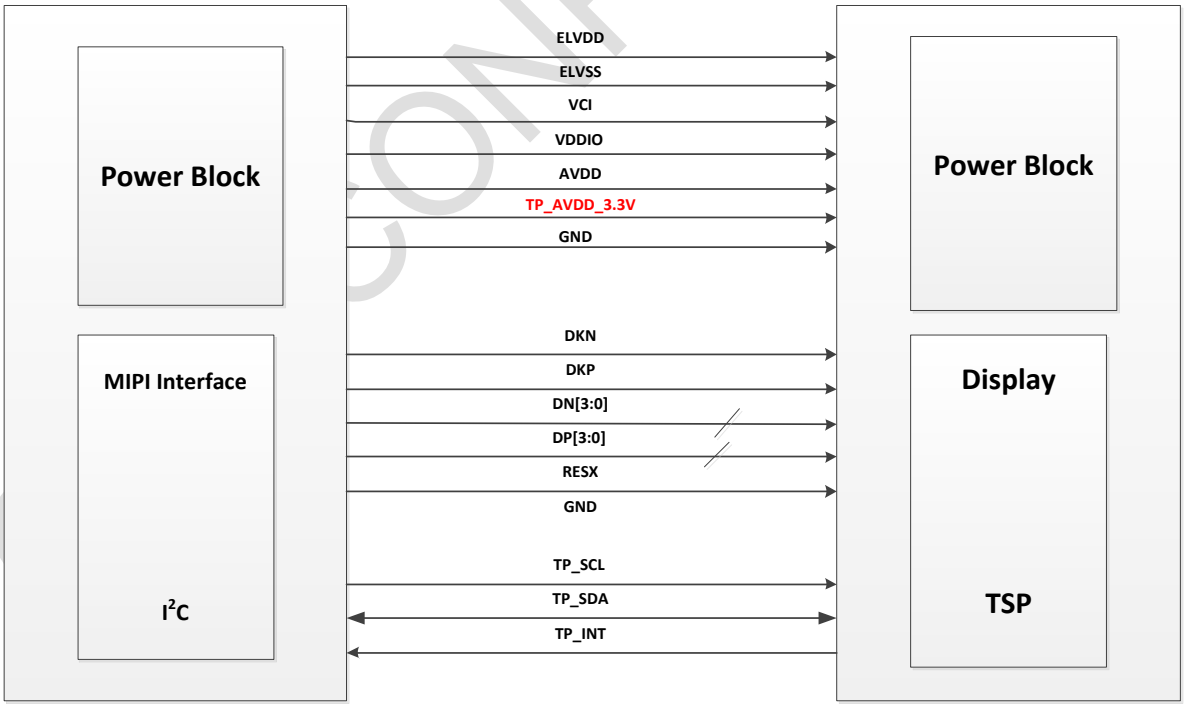
2.2 TP FPC Pin Assignment-On-cell TP Input / Output Signal Interface

No	Symbol	I/O	Description
1	TSP_DVDD_1.8V	Power	Power supply for display logic circuits
2	TSP_RESET	I	Reset Pin for TP, Active low
3	TSP_AVDD_3.3V	Power	Analog Power for TP
4	TSP_SDA	I/O	SDA pin for TP
5	TSP_SCL	I/O	SCL pin for TP
6	TSP_ATTN	I/O	INT pin for TP
7	GND	GND	Ground

2.3 Circuit block diagram (Display)



2.4 MCU and Display Module Interface Conflagration



3 Absolute Maximum Ratings

3.1 Driving AMOLED Panel

Maximum Ratings (Voltage Referenced to VSS) Vss=0V, Ta=25℃

Item	Symbol	MIN	MAX	Unit
Analog Power supply	VCI	-0.3	+5.0	V
Logic Power supply	VDDIO	-0.3	+4.0	V
Positive Power Input	ELVDD	-	+5.0	V
Negative Power Input	ELVSS	-5.0	-	V

Note: Functional operation should satisfy the limits in the Electrical Characteristics tables or Pin Description section. If the module exceeds the absolute maximum ratings, permanent damage may occur. Besides, if the module is operated with the absolute maximum ratings for a long time, the reliability may also drop.

4 Electrical Characteristics

4.1 Driving AMOLED Panel

Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit
Logic Power supply		VDDIO	1.65	1.80	3.30	V
Analog Power supply		VCI	2.65	2.80	3.60	V
ELVDD Supply Voltage		ELVDD	4.55	4.60	4.65	V
ELVSS Supply Voltage		ELVSS	-1	TBD	-5	V
Input Signal Voltage	High Level	VIH	0.80*VDDIO	-	VDDIO	V
	Low Level	VIL	0.00	-	0.20*VDDIO	V
Output Signal Voltage	High Level	VOH	0.80*VDDIO	-	VDDIO	V
	Low Level	VOL	0.00	-	0.20*VDDIO	V

Note1: The input digital voltage is the I/O reference voltage.

Note2: VDDIO usually ranges from 1.65V to 1.95 V. If VDDIO is changed, the remaining voltage needs to be changed to the same voltage as VDDIO.

4.2 Current Consumption

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Panel Power		P_{NL}	ELVDD=4.6V	-	TBD	TBD	mW	Note1
		I_{NL}	ELVSS=TBD	-	191.80	TBD	mA	Note2
IC	Normal	I_{VCI}	VCI=2.8V		1.5	TBD	mA	-
		I_{IOVCC}	VDDIO=1.8V		42	TBD	mA	-
	Stand-by	I_{VCI}	VCI=2.8V		1	TBD	uA	-
		I_{IOVCC}	VDDIO=1.8V		1	TBD	uA	-

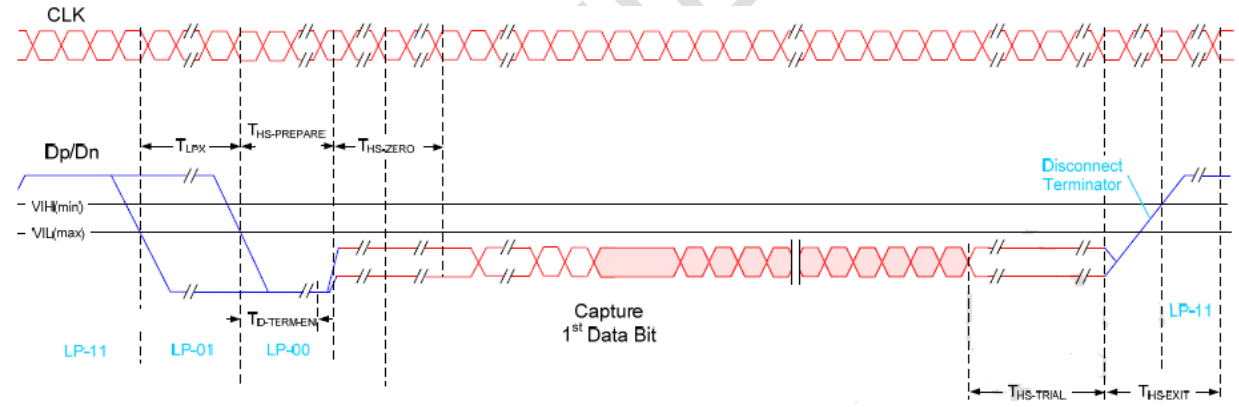
Note1: Based on L255 (350nit) full white pattern.

Note2: Video Mode 60Hz.

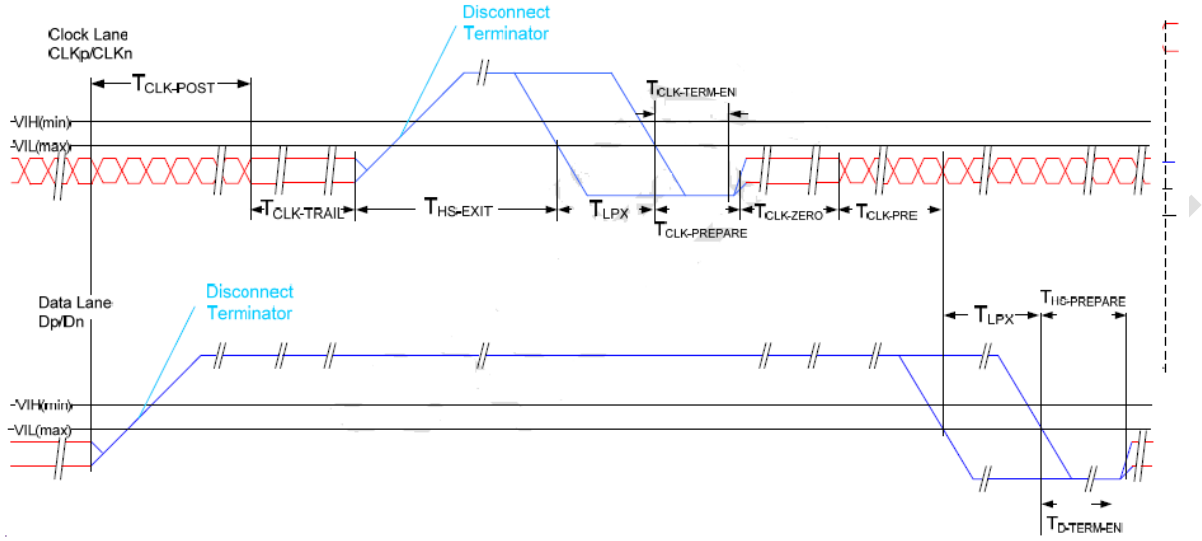
5 AC Characteristics

5.1 MIPI Interface Characteristics

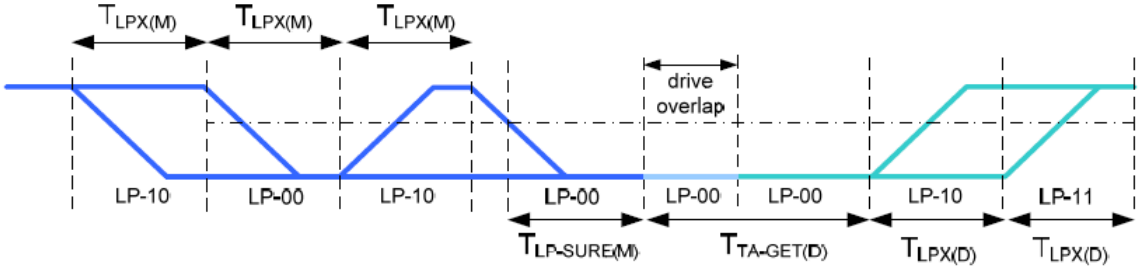
HS Data Transmission Burst



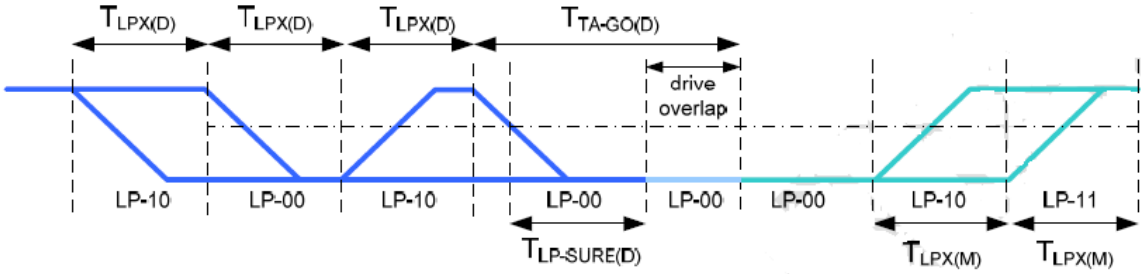
HS clock transmission



Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



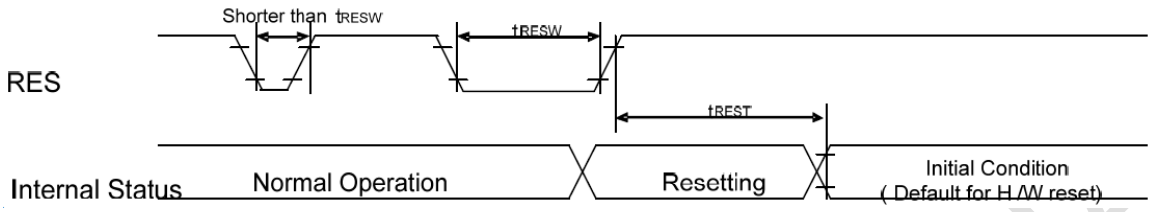
Timing Parameters：

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	**300**			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	**$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.**	**145ns + 10*UI**			**ns**
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		**150**	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		**150**	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

5.2 Display RESET Timing Characteristics

Reset input timing:



VDDIO=1.65 to 3.3V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

Timing Parameters

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

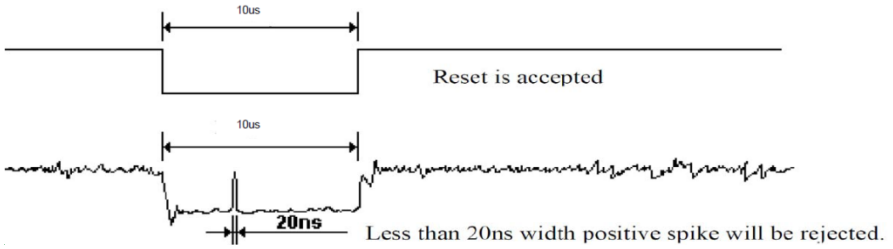
Note1.Spike caused by an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blank (The display is entering blanking sequence, whose maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains blank in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:

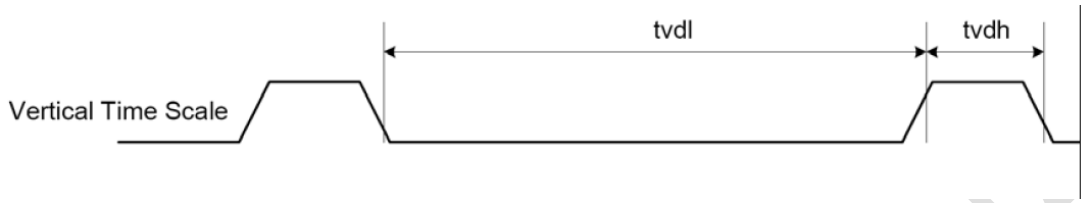


Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out

command cannot be sent for 120msec.

5.3 TE Timing Characteristics

Mode1, The Tearing Effect Output line consists of V-Blanking information only.

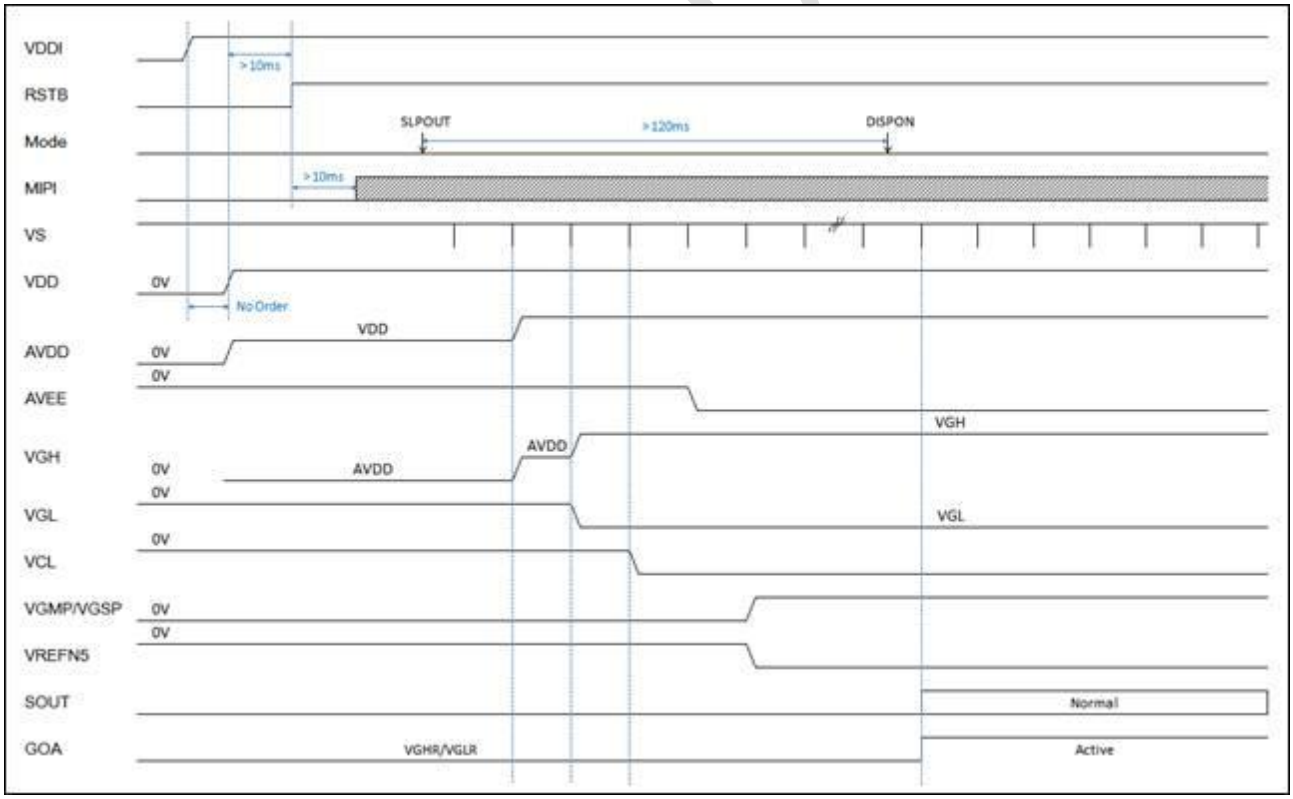


Tvdh = The LCD display is not updated from the frame memory.
Tvdl = The LCD display is updated from the frame memory.

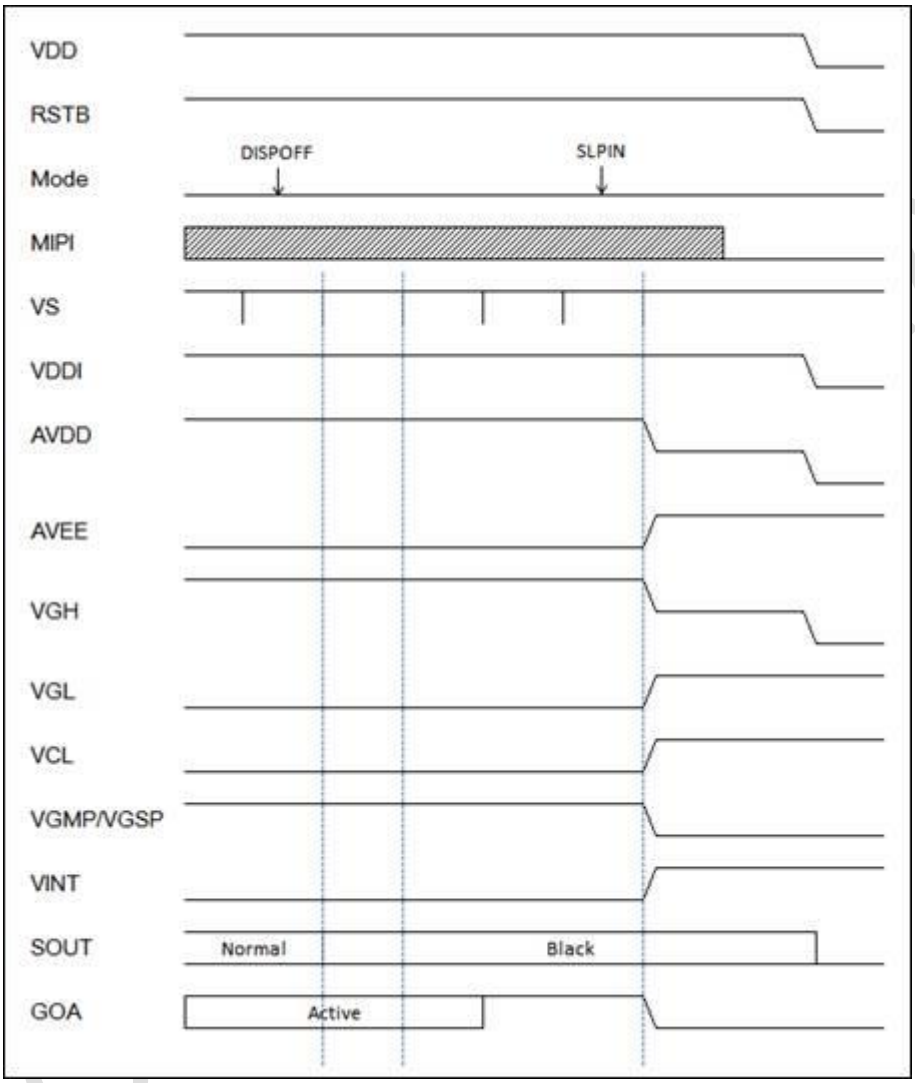
6 Recommended Operating Sequence

6.1 Display Power on / off Sequence

6.1.1 Power On Sequence



6.1.2 Power Off Sequence



6.2 Display Initial code

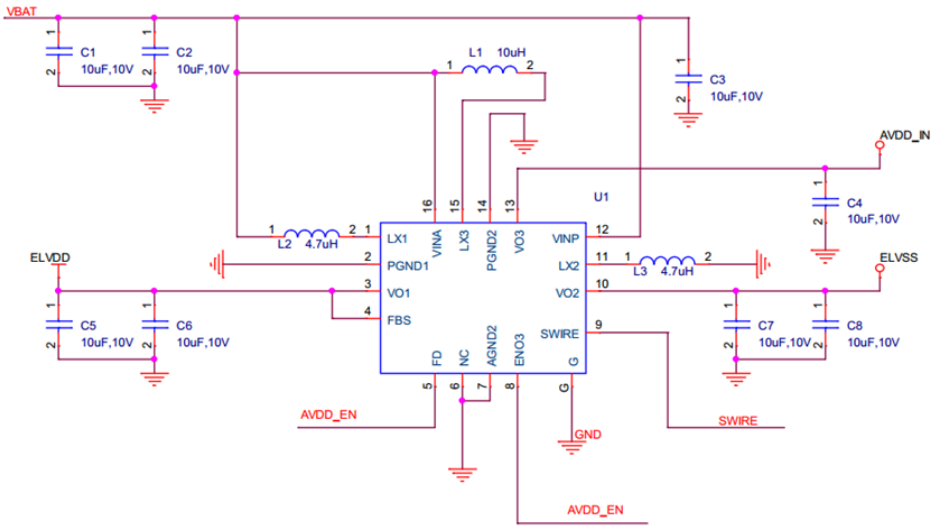
TBD

6.3 Brightness control

Inst/Para	R/W	Address		Date Type	Description
		MIPI	Other		
BRTCTRL	W	51h	5100h	Hex	Value form 0~255(FF)

7 Application Circuit

Concerning ELVDD&ELVSS & AVDD power supply schematic, the Triple DC/DC converter TPS65651/ RT4722 is recommended. The application schematics and external components are as below.



Description	Part Reference	Manufacturer	Manufacturer PN
10uF, 10V, ±20%, X5R, 0402	C1, C2, C3, C4, C5, C6, C7, C8	Murata	GRM155R61A106ME44D
		Samsung	CL05A106MP5NUNC
Power Inductor, 10uH, 20%, LS2520	L1	成育科技	ACDNR252010UP-100MT
		科明电子	KMPHS252010-100M
Power Inductor, 4.7uH, 20%, LS2520	L2, L3	成育科技	ACDNR252010T-4R7MT
		科明电子	KMPHS252010-4R7M
QFN16(3.0X3.0)	U1	TI	TPS65651
		RICHTEK	RT4722

8 Optical Characteristics Optical Specification

Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angle	θT	CR≥10	75	85		Degree	Note 2 Test Equipment：CS2000A
	θB		75	85			
	θL		75	85			
	θR		75	85			
Contrast Ratio	CR	θ=0°	10000				Note1 Note3 Test Equipment：CS2000A
Response Time	T_{ON}	25℃			1	ms	Note1

		T_{OFF}						Note4 Test Equipment： Admesy MSE
Chromaticity	White	x		(0.280)	(0.300)	(0.320)		Test Equipment： CS2000A Note: Chromaticity can be modified according to customer demand
		y		(0.300)	(0.320)	(0.340)		
	Red	x		(0.620)	(0.660)	(0.700)		
		y		(0.290)	(0.330)	(0.370)		
	Green	x		(0.200)	(0.250)	(0.300)		
		y		(0.660)	(0.710)	(0.760)		
	Blue	x		(0.110)	(0.140)	(0.170)		
		y		(0.030)	(0.060	(0.090)		
Uniformity		U		75			%	Note1 Note6 luminance of center point is 350±35nits Test Equipment： CS2000A
NTSC				85	100		%	Note5
Luminance		L		280	350	420	Cd/m^2	Note1 Note7 Test Equipment： CS2000A
Cross-talk						1.5	%	Note8 L≤350nits Test Equipment： CS2000A
Gamma				2.0	2.2	2.4		Gamma=2.2±0.2（L≤350nits）; Gamma Self-adjustment (L＞350nits) Test Equipment： CS2000A
Flicker				-	-	-	db	Note9 Customer RFQ did not mentioned the item
Color Temperature				-	-	-	K	Test Equipment：

							CS2000A Customer RFQ did not mentioned the item
Color shift		-	-	-	-	JNCD	Note10 Customer RFQ did not mentioned the item
Gray-scale transition	Delta Tc	Gray-scale ⩾64	-	-	-	K	Test Equipment：CS2000A Customer RFQ did not mentioned the item
	Delta u'v'	Gray-scale ⩾64	-	-	-	-	Test Equipment：CS2000A
Color Uniformity			-	-	-		Full White Customer RFQ did not mentioned the item

Test Conditions:

the ambient temperature is 25℃.

1. The test systems refer to Note1 and Note2.

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the AMOLED screen. All input terminals AMOLED panel must be ground when measuring the center area of the panel.

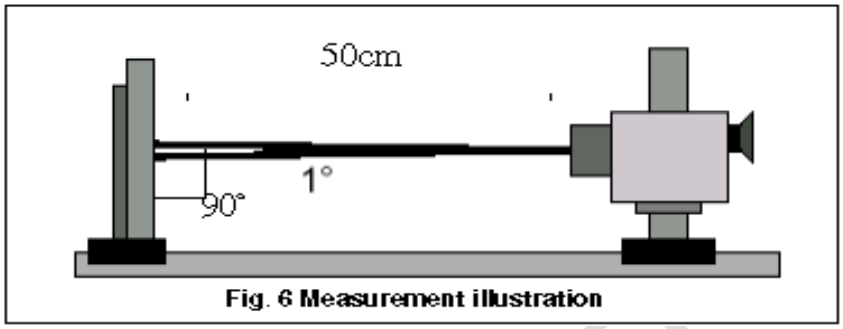


Fig. 6 Measurement illustration

Note 2: Definition of viewing angle range and measurement system.

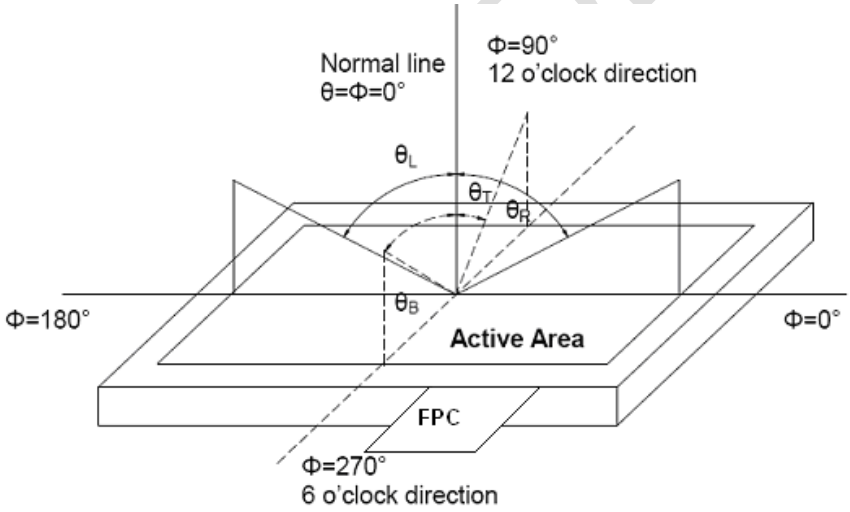


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$\text{Contrast ratio(CR)} = \frac{\text{Luminance measured when LCD is on the "white" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

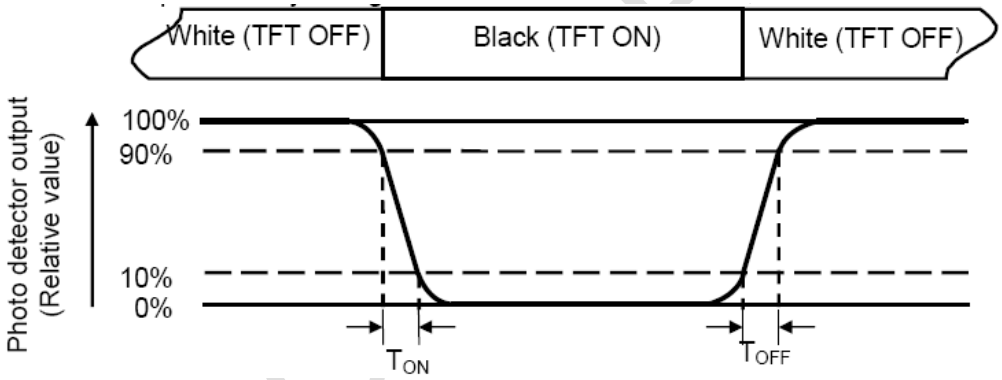
“White state “: A state where the AMOLED should be driven by Vwhite.

“Black state”: A state where the AMOLED should be driven by Vblack.

Note 4: Definition of response time

The response time is defined as the AMOLED optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time betwe

g from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changing from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates are measured at the center point of AMOLED.

Note 6: Definition of luminance uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax

L-------Active area length W----- Active area width

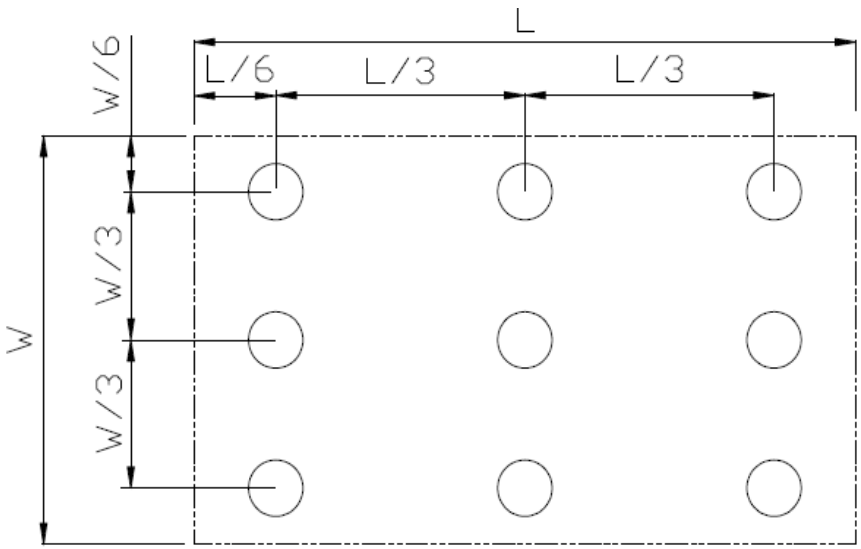


Fig. 2 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

Note 7: Definition of luminance:

Measure the luminance of white state at the center point.

Note 8: Cross Talk

A. Measure luminance at the position, P0.

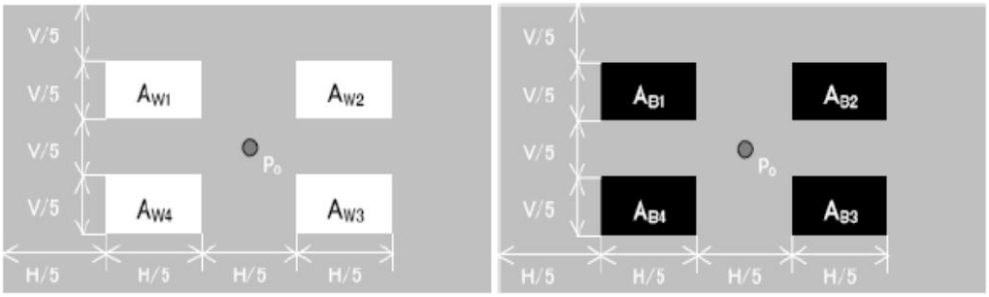
B. Calculate cross talk as below equation.

$$L_{W\_OFF} = \frac{L_{W1} + L_{W2} + L_{W3} + L_{W4}}{4}$$

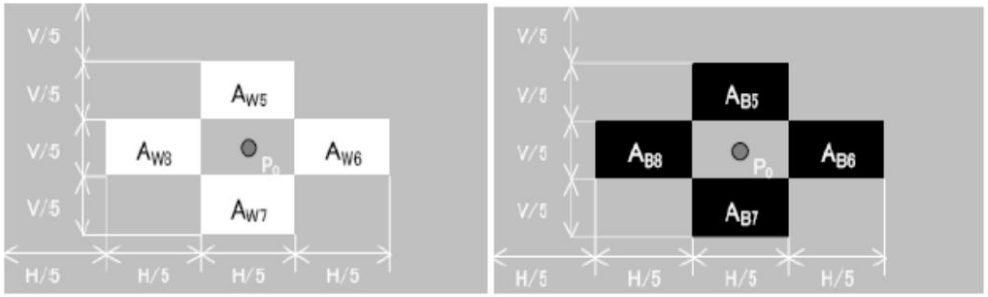
$$L_{B\_OFF} = \frac{L_{B1} + L_{B2} + L_{B3} + L_{B4}}{4}$$

$$\text{crosstalk} = \frac{|L_{Wi\_ON} - L_{W\_OFF}|}{L_{W\_OFF}} \times 100\% \qquad (i = 5 \text{ to } 8)$$

$$\text{crosstalk} = \frac{|L_{Bi\_ON} - L_{B\_OFF}|}{L_{B\_OFF}} \times 100\% \qquad (i = 5 \text{ to } 8)$$



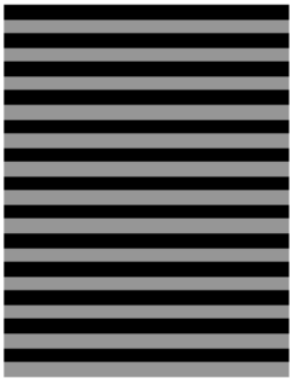
(a) L_{W_OFF}, L_{B_OFF} measuring pattern



(b) L_{W_ON}, L_{B_ON} measuring pattern

Note 9 : Flicker

Suggested Instrument s: **Konica Minolta CA-310** or **Klein Instruments K-8**



Odd row : **L0** Black
Even row : **L186** gray level

Flicker Test Pattern

The flicker level is defined by Fast Fourier Transformation (FTT) as follows:

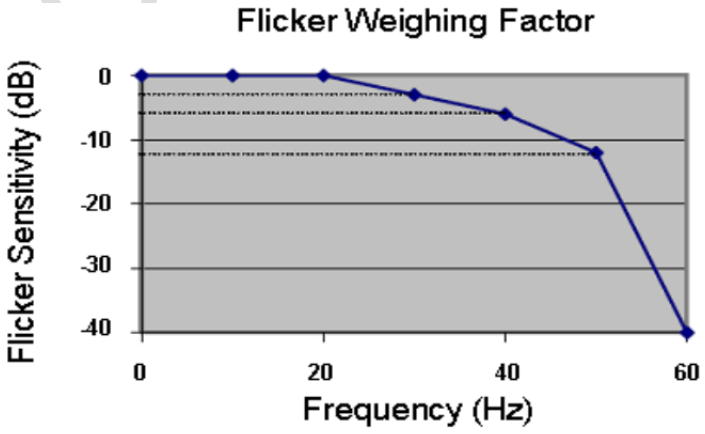
$$Flic\ker = 20\log_{10}\left(2\frac{f_{FFTC}(n)}{f_{FFTC}(0)}\right) + FS(Hz) \quad \text{(dB)}$$

$f_{FFTC}(n)$ is the n-th FFT coefficient.

$f_{FFTC}(0)$ is the 0-th FFT coefficient that is DC component.

FS(Hz) is the flicker sensitivity as a function of frequency.

The peak flicker level shall be reported based on the calculation using above formula in which FS(Hz) is determined by the flicker weighing factor shown below.



Note10: Color Shift JNCD

- For JNCD measure:
- Test pattern: Full White
- On the condition θ=0 F=0°, we can get the color coordinate (u1', v1') and on 30° we can get another color coordinate (u2', v2')
- Delta = Square Root((u2'-u1')^2 + (v2'-v1')^2)
- JNCD stands for "Just Noticeable Color Difference"
- For the (u', v') color space JNCD=0.0040.
- 2JNCD means Delta u'v'<0.0080
- This Requirement is from our customer and we have test some of our phone display and the result is OK.

9 Environmental / Reliability Test

No	Test Item	Condition	Remark
1	High Temperature Operation	+60℃, 120hrs	IEC60068-2-2,GB2423.2
2	Low Temperature Operation	-20℃, 120hrs	IEC60068-2-1 GB2423.1
3	High Temperature Storage	+70℃, 120hrs	IEC60068-2-2 GB2423.2
4	Low Temperature Storage	-30℃, 120hrs	IEC60068-2-1 GB2423.1
5	High Temperature & High Humidity Operation	60℃, 90% RH,120hrs	IEC60068-2-78 GB/T2423.3
6	Thermal Shock (Non-operation)	-40(℃)/30(min) ~+85 (℃)/30(min), Change time:10min, 30Cycles	Start with cold temperature, End with high temperature, IEC60068-2-14,GB2423.22
7	High Temperature & High Humidity Storage	60℃, 90% RH,120hrs	IEC60068-2-78 GB/T2423.3
8	ESD	Air:+/-8KV,Contact:+/-4KV	IEC61000-4-2 GB/T17626.2

10 Quality Level

10.1 AMOLED Module of Characteristic Inspection

The environmental condition and visual inspection shall be conducted as below:

(1) Ambient temperature: 20~25℃

(2) Humidity: 55 ± 10%RH

(3) Ambient light intensity of visual inspection: 1000 ~ 1200 lux

(4) Ambient light intensity of function inspection: 100~150lux

(5) Viewing Distance: 30 ± 5cm

(6) Viewing angle (tolerance): the front side 45° (Z) ±15°

(7) Inspection time: 10 ±2 sec

10.2 Sampling Procedures for each item acceptance table

Defect type	Sampling Procedures	AQL
Major defect	GB/T2828.1-2003 Inspection level Ⅱ normal inspection single sample inspection	0.25
Minor defect	GB/T2828.1-2003 Inspection level Ⅱ normal inspection single sample inspection	0.65

Major defect:

Any defect may result in functional failure, or reduce the usability of product for its purpose, such as electrical failure, deformation and so on.

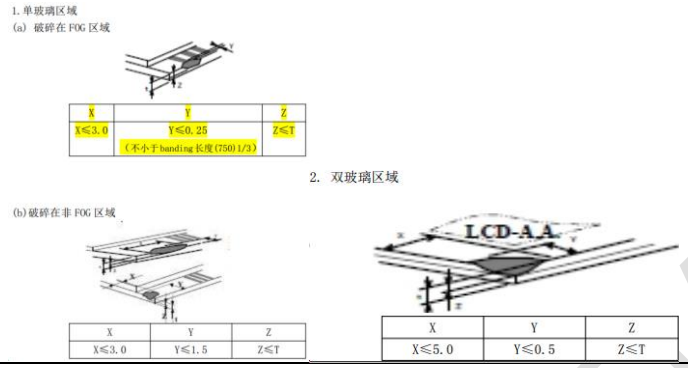
Minor defect

A defect does not reduce the usability of product for its intended purpose, such as dot defect and so on.

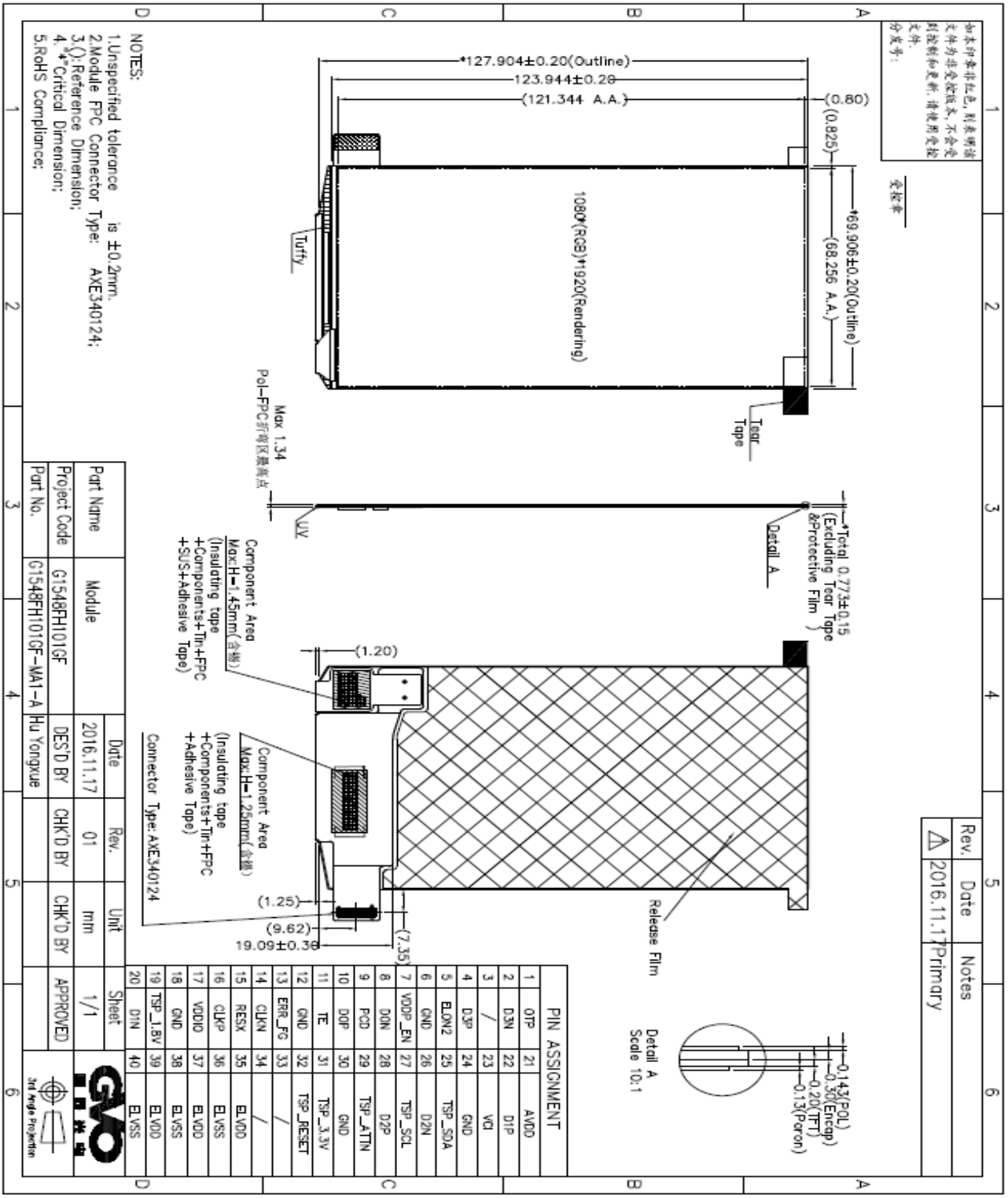
The criteria on major and/or minor judgment will be according with the classification of defects.

10.3 Inspection Item

No.	Item	Criterion of Defect			Defect type
1	Bright Dot	D≤0.1		Ignore	
		0.1＜D≤0.2		N≤2 ,DS≥10mm	
		0.2＜D		Not allowed	
2	Dark Dot	(Pixel level)	Single	Ignore	Minor
			Two connected dot	N≤4, DS≥10mm	
			Three connected dot	Not allowed	
		D≤0.1		Ignore	
		0.1＜D≤0.2		N≤2,DS≥10mm	
3	Dot Defect (Concave dot/Black dot/ Bubble)	D≤0.10		Ignore(N≤3, DS≤10mm)	Minor
		0.10mm＜D≤0.15mm		≤2 (DS≥10mm)	
4	Linear Defect(Fiber/ flocks)	W≤0.03mm		Ignore	Minor
		0.03mm＜D≤0.05mm, L≤1.0mm		≤2 (DS≥10mm)	
		Other		Not allowed	
5	Panel Scratch	W≤0.03mm		Ignore	Minor
		0.03mm＜D≤0.05mm, L≤5.0mm		≤2 (DS≥10mm)	
		Other		Not allowed	
6	NO Display	Not allowed			Major
7	Display unevenly	Not allowed			Major
8	Flashing Screen	Not allowed			Major
9	Missed line	Not allowed			Major
10	Mura	Limit sample			Major
11	Newton's Ring	Limit sample			Major

12	Edge/Side breakage	Not allowed in AA and VA 	Major
13	FPCA	The component can not reverse polarity	Minor
		No wrong insertion	
		FPC should not have serious crease which destroy the line, prick and spots damage. Scratch is not allowed if Cu layer is exposed.	
		The gold fingers should not be oxidized, scraped, folded, impressed, broken, spotted or dissymmetry.	
		Make sure FPC is not scalded, with its location holes not having deficiency or obviously shift.	
		The component of FPC should be the same as BOM list.	
		No remaining soldering Sn	
		No visual particle on the pad line	

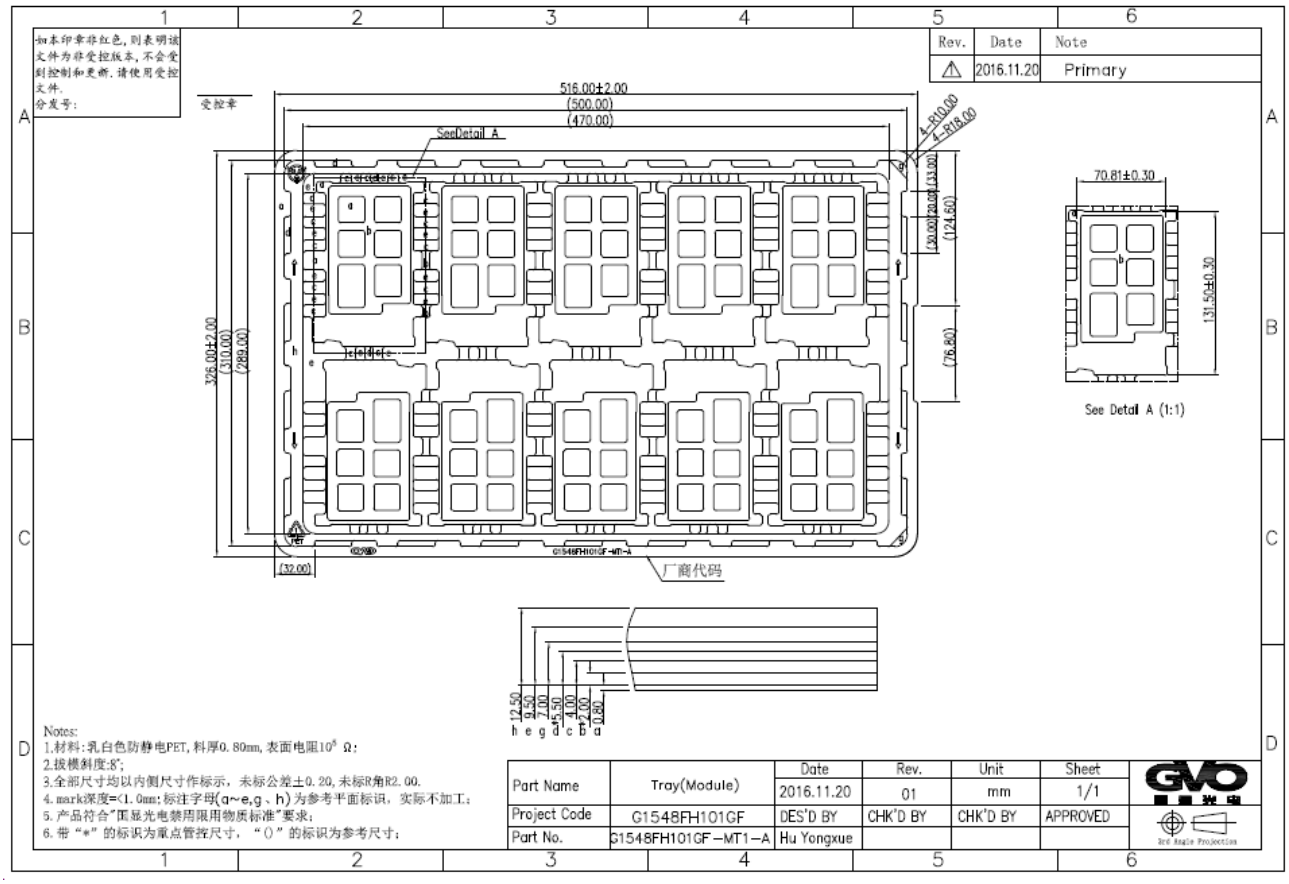
11 Mechanical Drawing



PIN	ASSIGNMENT	PIN	ASSIGNMENT
1	OTP	21	AVDD
2	D3N	22	D1P
3	/	23	VCI
4	D3P	24	GND
5	ELON2	25	TSP_SDA
6	GND	26	D2N
7	VDDP_EN	27	TSP_SCL
8	D0N	28	D2P
9	PCD	29	TSP_ATTN
10	D0P	30	GND
11	TE	31	TSP_3.3V
12	GND	32	TSP_RESET
13	ERR_FG	33	/
14	CLKN	34	/
15	RESX	35	ELVDD
16	CLKP	36	ELVSS
17	VDDIO	37	ELVDD
18	GND	38	ELVSS
19	TSP_1.8V	39	ELVDD
20	D1N	40	ELVSS

Packing Drawing

Packing Condition	Contents
Packing Type	TRAY + Carton packing type
TRAY material model	tray (10^5~$10^9\Omega$)
Tray packing type	See the picture 1
Number of panels per tray	10 pieces
Number of Tray per carton	21units ((20 units + 1 empty)PET tray)
Number of panels per carton	200 pieces



Picture 1

12 Precautions for Use of AMOLED Modules

12.1 Handling Precautions:

12.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from height.

12.1.2 Do not press down the screen or the adjoining areas too hard because the color tone may be shifted.

12.1.3 The polarizer covering the display surface of the AMOLED module is soft and easily scratched. Handle this polarizer carefully.

12.1.4 If the display surface is contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is still not completely clear, moisten the cloth with ethyl alcohol.

12.1.5 Solvents may damage the polarizer. Do not use water, ketone or aromatic solvents except ethyl alcohol.
Do not attempt to disassemble the AMOLED Module.

12.1.6 If the logic circuit power is off, do not apply the input signals.

12.1.7 To prevent destruction from static electricity, be careful to maintain an optimum working environment.

12.1.8 Be sure to make yourself in contact with the ground when handling with the AMOLED Modules.

12.1.9 Tools required for assembly, such as soldering irons, must be properly ground.

12.1.10 To reduce the generation of static electricity, do not conduct assembly or other work under dry conditions.

12.1.11 To protect the display surface, the AMOLED Module is coated with a film. Be careful when peeling off this protective film, because static electricity may generate.

12.2 Storage Precautions:

12.2.1 When storing the AMOLED modules, be sure that they are not directly exposed to the sunlight or the light of fluorescent lamps.

12.2.2 The AMOLED modules should be stored under the storage temperature range. If the AMOLED modules will be stored for a long time, the recommended condition is:
Temperature: 0℃~40℃ Relatively humidity: ≤80%

12.2.3 The AMOLED modules should be stored in the room without acid, alkali or harmful gas.

12.3 Transportation Precautions:

12.3.1 The AMOLED modules should not be suffered from falling and violent shocking during transportation. Besides, excessive press, water, damp and sunshine, should be avoided.