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NV156FHM-N4G V3.0 Product Specification Rev.P2

BUYER	
SUPPLIER	HEFEI BOE Optoelectronics Technology CO., LTD
FG-Code	NV156FHM-N4G V3.0

ITEM BUYER SIGNATURE DATE	ITEM SUPPLIER SIGNATURE DATE
	Prepared
	Reviewed
	Approved

HEFEI BOE OPTOELECTRONICS TECHNOLOGY

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REV.	ECN No.	DESCRIPTION	OF CHANGES		DATE		PREPARED		
Р0		Initial R	elease		2017-12-2	1	SHAOLINFEI		
P1		Update EDID	0&PACKING		2018-1-2	5	SHAOLINFE		
P2		Change MDL label size to 48*12mm			2018-03-0)1	SHAOLINFE		

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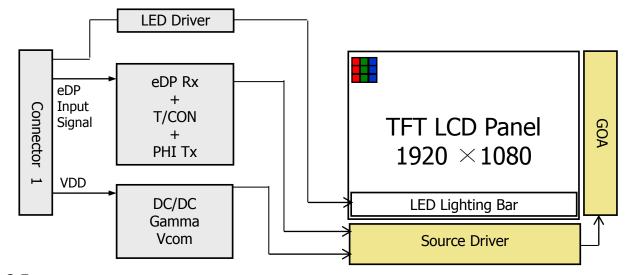
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1.0 GENERAL DESCRIPTION

1.1 Introduction

NV156FHM-N4G V3.0 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 15.6 inch diagonally measured active area with FHD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical Stripe and this module can display 16.7M colors. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED Driver for back-light driving is built in this model. All input signals are eDP interface compatible.



1.2 Features

- Support G-SYNC with Direct Driver
- Frame rate support range: 72Hz~144Hz;
- 4 lane Edp1.4 Interface with 5.4Gbps Link Rates
- Thin and light weight
- 8-bit color depth, display 16.7M colors
- Single LED Lighting Bar. (Bottom side/Horizontal Direction)
- Data enable signal mode
- Side Mounting Frame
- Green Product (RoHS & Halogen free product)
- On board LED Driving circuit
- Low driving voltage and low power consumption
- On board EDID chip

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1.3 Application

• Note Book

1.4 General Specification
The followings are general specifications at the NV156FHM-N4G V3.0

<Table 1. LCD Module Specifications>

Parameter	Specification	Unit	Remarks
Active Area	344.16(H)*193.59(V)	Mm	
Number Of Pixels	1920(H)×1080(V)	Pixels	
Pixel Pitch	0.17925(H)×RGB×0.17925(V)	mm	
Pixel Arrangement	Pixels RGB stripe arrangement		
Display Mode	Normally Black		
Display Colors	16.7M(8bits)	Colors	
Display Mode	Normally Black		
Surface Treatment	上POL:高精细AG25;下POL:APF		
Contrast Ratio	1200:1(typ.)		
Viewing Angle(CR>10)	89/89/89/89(typ.)	deg.	
Response Time	Tr+Tf=9 typ/12max.; GTG avg=3.8typ/5max	Ms	
Color Gamut	72%		
Brightness	300(typ)	cd/m2	
Brightness Uniformity	80% min for 5 points 60% min for 13 points		
Power Consumption	LCD: 2.4(Max.)(144Hz, Mosaic) BLU: 3.7W(Max.)	Watt	
Outline Dimension(LCM)	350.66(typ)*215.25(typ)*2.6(max)	mm	
Weight	280(max.)	gram	

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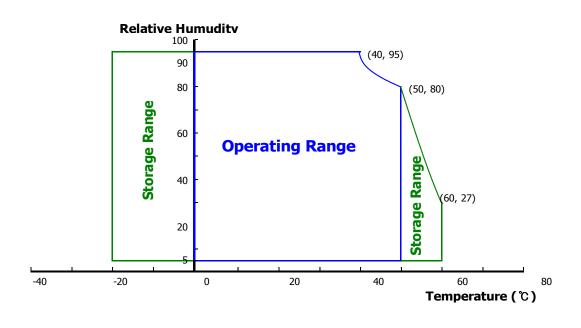
2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

 $Ta = 25 + / - 2^{\circ}C$

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
Logic Supply Voltage	V _{IN}	V _{ss} -0.3	V _{DD} +0.3	V	Note 1
Operating Temperature	T _{OP}	0	+50	°C	Note 2
Storage Temperature	T _{ST}	-20	+60	°C	Note 2

- Notes: 1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.
 - 2. Temperature and relative humidity range are shown in the figure below. 95 % RH Max. (40 °C ≥ Ta) Maximum wet - bulb temperature at 39 °C or less .(Ta > 40 °C) No condensation.



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3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3. Electrical specifications >

[Ta =25±2 ℃]

Parameter		Min.	Тур.	Max.	Unit	Remarks	
Power Supply Voltage	V _{DD}	3.0	3.3	3.6	V	Note 1	
Permissible Input Ripple V oltage	V _{RF}	ı	-	100	mV	At V _{DD} = 3.3V	
Power Supply Current	I _{DD}	-	727	1121	mA	Note 1	
LX Current Limit	I _{LX}		2		Α		
Positive-going Input Thres hold Voltage	V _{IT+}	-	-	100	mV	V = 1.2V typ	
Negative-going Input Thr eshold Voltage	V _{IT-}	-100	-	-	mV	V _{cm} = 1.2V typ.	
Differential Input Voltage	V _{ID}	200	-	600	mV		
	P _D	-	2.4	3.7	W	Note 1	
Power Consumption	P_{BL}	-		3.7	W	Note 2	
	P _{total}	-	6.1	7.4	W		

Notes : 1. The supply voltage is measured and specified at the interface connector of LCM . The current draw and power consumption specified is for 3.3V at $25^{\circ}C$.

a) Typ : Mosaic pattern b) Max : RGB pattern

2. Calculated value for reference (VLED × ILED)

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3.2 Back-Light Unit

< Table 4. LED Driving guideline specifications >

[Ta =25±2 ℃]

P	arameter		Min.	Тур.	Max.	Unit	Remarks
LED Forward Vo	oltage	V _F	-	1	2.9	٧	
LED Forward Cu	urrent	I _F	-	22.5	-	mA	
LED Power Con	sumption	P _{LED}	-	-	3.7	W	Note 1
LED Life-Time		N/A	15,000	-	-	Hour	I _F = 20.0mA
Power supply voltage for LED Driver		V _{LED}	5	12	21	٧	
EN Control	Backlight on		2.5	ı	5.0	V	
Level	Backlight off		0	ı	0.6	٧	
PWM Control	PWM High Level		2.0	ı	5.0	V	
Level	PWM Low Level		0	1	0.6	٧	
PWM Control Frequency		F _{PWM}	200	ı	10,000	Hz	
Duty Ratio		_	1	_	100	%	

Notes : 1. Power supply voltage12V for LED Driver, Driver efficiency 87%, Calculator Value for reference IF \times VF \times 30 / 0.87 = PLED

2. The LED Life-time define as the estimated time to 50% degradation of initial luminous.

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3.3 Pin assignment for LED Bar Connector : MSK24022P10 (STM)

< Table5. Pin assignment for LED Bar >

Pin No	Symbol	Description	Remarks
1	VLED	LED Anode Power Supply	
2	VLED	LED Anode Power Supply	
3	VLED	LED Anode Power Supply	
4	NC	NC	
5	FB1	LED Cathode Power Supply	
6	FB2	LED Cathode Power Supply	
7	FB3	LED Cathode Power Supply	
8	FB4	LED Cathode Power Supply	
9	FB5	LED Cathode Power Supply	
10	FB6	LED Cathode Power Supply	

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4.0 OPTICAL SPECIFICATIONS

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance \leq 1lux and temperature = $25\pm2^{\circ}\text{C}$) with the equipment of Luminance meter system (Gonio meter system and TOPCON BM-5) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta\emptyset$ =0 (=03) as the 3 o' clock direction (the "right"), $\theta\emptyset$ =90 (=012) as the 12 O' clock direction ("upward"), $\theta\emptyset$ =180 (=09) as the 9 O' clock direction ("left") and $\theta\emptyset$ =27 0(=06) as the 6 O' clock direction ("bottom"). While scanning θ and/or \emptyset , the center of the measuring spot on the Display surface shall stay fixed.

4.2 Optical Specifications

< Table 6. Optical Table >

Parame	eter	Symbol	Condition	Min.	Тур.	Max.	Unit	Remark	
	Horizontal	Θ_3		80	89	-	Deg.		
Viewing Angle	Honzoniai	Θ_9	CR > 10	80	89	-	Deg.	Note 1	
range	Vertical	Θ ₁₂	CR > 10	80	89	-	Deg.	Note	
	Vertical	Θ_6		80	89	-	Deg.		
Luminance Co	ntrast ratio	CR	Θ = 0°	900	1200	-	-	Note 2	
Luminance of White	Center Point	Y _w	Θ = 0°	255	300	-	cd/m ²	Note 3	
White	5 Points	ΔΥ5		80%	-	-	-		
Luminance uniformity	13 Points	ΔΥ13	1225 20 11111	60%	-	-	-	Note 4	
White Chromaticity		X _w	Θ = 0°	-0.03	0.313	+0.03	-	Note 5	
write Cillo	Пансну	y_{w}	0 = 0	-0.03	0.329	+0.03	-	NOIE 3	
	Red	X _R			0.642		-		
	ixeu	y _R			0.339		-	-	
Reproduction	Green	X _G	Θ = 0°	-0.025	0.316	+0.025	-	_	
of color	Oleen	y _G	0-0	-0.023	0.606	+0.025	-	-	
	Blue	X _B			0.153		-		
	Blue y _B		0.050		-				
Gamı	ut	-	Θ = 0°	67	72	-	%	NTSC	
Response (Rising + F		T _{RT}	Ta= 25° C Θ = 0°	-	9	12	ms	Note 6	
Cross T	alk	СТ	Θ = 0°	-	-	2.0	%	Note 7	

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Notes:

- 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o' clock direction and the vertical or 6, 12 o' clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).
- 2. Contrast measurements shall be made at viewing angle of Θ = 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

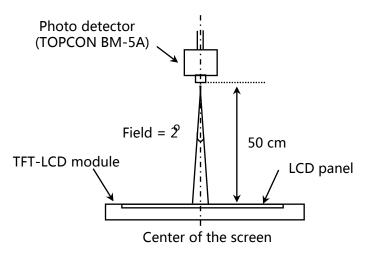
- 3. Center Luminance of white pattern on the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display.
- 4. The White luminance uniformity on LCD surface is then expressed as : ΔY = Minimum Luminance of 5(or 13) points / Maximum Luminance of 5(or 13) points. (see FIGURE 2 and FIGURE 3).
- 5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
- 6. The electro-optical response time measurements shall be made as FIGURE 4 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.
- 7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark.

 (See FIGURE 5).

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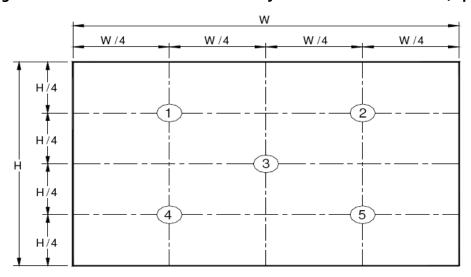
4.3 Optical measurements

Figure 1. Measurement Set Up



Optical characteristics measurement setup

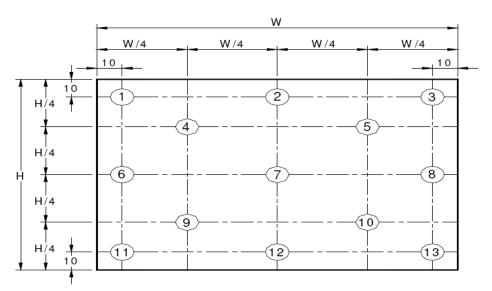
Figure 2. White Luminance and Uniformity Measurement Locations (5 points)



Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display.

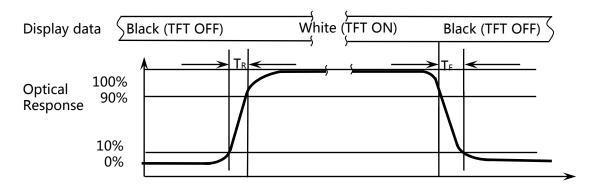
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Figure 3. Uniformity Measurement Locations (13 points)



The White luminance uniformity on LCD surface is then expressed as : $\Delta Y5$ = Minimum Luminance of five points / Maximum Luminance of five points (see FIGURE 2) , $\Delta Y13$ = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see FIGURE 3).

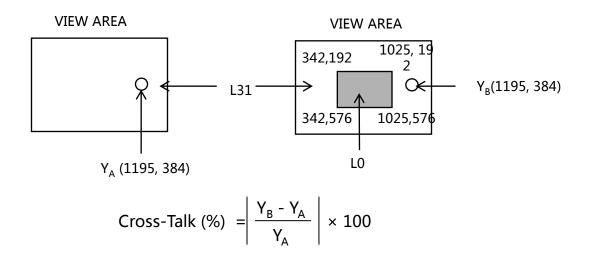
Response Time Testing



The electro-optical response time measurements shall be made as shown in FIGURE 4 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr and 90% to 10% is Tf.

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Figure 5. Cross Modulation Test Description



Where:

 Y_A = Initial luminance of measured area (cd/m²)

 Y_B = Subsequent luminance of measured area (cd/m²)

The location measured will be exactly the same in both patterns

Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark (Refer to FIGURE 5).

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5.0 INTERFACE CONNECTION.

5.1 Electrical Interface Connection

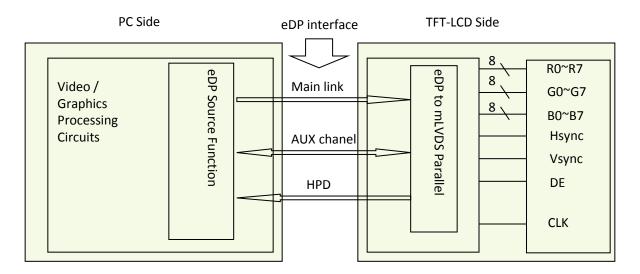
The electronics interface connector is STM. The mating connector part number is STM MSAK24025P40. The connector interface pin assignments are listed in Table 7.

<Table 7. Pin Assignments for the Interface Connector>

Terminal Symbol Description	<tab< th=""><th>ole 7. Pin Assignments for the 1</th><th>Interface Connector></th></tab<>	ole 7. Pin Assignments for the 1	Interface Connector>
1	Terminal	Symbol	Functions
Connect to GND Connect to GND	PIN No.	Symbol	Description
3	1	NC	NC
4 Lane3_P 5 H_GND 6 Lane2_N 7 Lane2_P 8 H_GND 9 Lane1_1N 10 Lane1_1P 11 H_GND 12 Lane1_0N 13 Lane1_0P 14 H_GND 15 AUX_CH_P 16 AUX_CH_N 17 H_GND 18 LCD_VCC 19 LCD_VCC 20 LCD_VCC 21 LCD_VCC 22 LCD_Self_Test(BIST) BIST (IN Port) 23 LCD_GND 24 LCD_GND 25 LCD_GND (Connect to GND in Module) 26 LCD_GND (Connect to GND in Module) 27 HPD HPD (OUT Port 2.5V/3.3V) 28 BL_GND BLU GND 29 BL_GND (Connect to GND in Module)	2	H_GND	
5 H_GND 6 Lane2_N 7 Lane2_P 8 H_GND 9 Lane1_1N 10 Lane1_1P 11 H_GND 12 Lane1_0N 13 Lane1_0P 14 H_GND 15 AUX_CH_P 16 AUX_CH_N 17 H_GND 18 LCD_VCC 19 LCD_VCC 20 LCD_VCC 21 LCD_VCC 22 LCD_Self_Test(BIST) BIST (IN Port) 23 LCD_GND 24 LCD_GND 25 LCD_GND (Connect to GND in Module) 26 LCD_GND HPD HPD (OUT Port 2.5V/3.3V) 28 BL_GND BLU GND 29 BL_GND BLU GND Connect to GND in Module) Connect to GND in Module)	3	Lane3_N	
6 Lane2_N 7 Lane2_P 8 H_GND 9 Lane1_1N 10 Lane1_P 11 H_GND 12 Lane1_0N 13 Lane1_0P 14 H_GND 15 AUX_CH_P 16 AUX_CH_N 17 H_GND 18 LCD_VCC 19 LCD_VCC 20 LCD_VCC 21 LCD_VCC 22 LCD_Self_Test(BIST) BIST (IN Port) 23 LCD_GND 24 LCD_GND 25 LCD_GND 26 LCD_GND 27 HPD HPD (OUT Port 2.5V/3.3V) 28 BL_GND 29 BL_GND BL_GND (Connect to GND in Module)	4	Lane3_P	
7 Lane2_P 8 H_GND 9 Lane1_1N 10 Lane1_1P 11 H_GND 12 Lane1_0N 13 Lane1_0P 14 H_GND 15 AUX_CH_P 16 AUX_CH_N 17 H_GND 18 LCD_VCC 19 LCD_VCC 20 LCD_VCC 21 LCD_VCC 22 LCD_Self_Test(BIST) BIST (IN Port) 23 LCD_GND 24 LCD_GND 25 LCD_GND 26 LCD_GND 27 HPD 4PD HPD (OUT Port 2.5V/3.3V) 28 BL_GND 30 BL_GND (Connect to GND in Module)	5	H_GND	
8 H_GND 9 Lane1_1N 10 Lane1_1P 11 H_GND 12 Lane1_0N 13 Lane1_0P 14 H_GND 15 AUX_CH_P 16 AUX_CH_N 17 H_GND 18 LCD_VCC 19 LCD_VCC 20 LCD_VCC 21 LCD_VCC 22 LCD_Self_Test(BIST) BIST (IN Port) 23 LCD_GND LOB_GND Logic GND 24 LCD_GND Logic GND 25 LCD_GND (Connect to GND in Module) 26 LCD_GND HPD HPD (OUT Port 2.5V/3.3V) 28 BL_GND BLU GND 29 BL_GND (Connect to GND in Module)	6	Lane2_N	
Section	7	Lane2_P	
Section	8	H_GND	-DD I
11	9	Lane1_1N	eDP lane
11	10	Lane1_1P	Up to 5.40
13	11	H_GND	υρ το 5.4G
13	12	Lane1_0N	
15	13		
16 AUX_CH_N 17 H_GND 18 LCD_VCC 19 LCD_VCC 20 LCD_VCC 21 LCD_VCC 22 LCD_Self_Test(BIST) BIST (IN Port) 23 LCD_GND 24 LCD_GND Logic GND 25 LCD_GND (Connect to GND in Module) 26 LCD_GND HPD (OUT Port 2.5V/3.3V) 28 BL_GND BLU GND 29 BL_GND BLU GND 30 BL_GND (Connect to GND in Module)	14	H_GND	
17 H_GND 18 LCD_VCC 19 LCD_VCC 20 LCD_VCC 21 LCD_VCC 22 LCD_Self_Test(BIST) BIST (IN Port) 23 LCD_GND 24 LCD_GND Logic GND 25 LCD_GND (Connect to GND in Module) 26 LCD_GND HPD HPD (OUT Port 2.5V/3.3V) 28 BL_GND BLU GND 30 BL_GND (Connect to GND in Module)	15	AUX_CH_P	
18 LCD_VCC LCD_Logic Power 19 LCD_VCC LCD Logic Power 20 LCD_VCC (3.3±0.3V) 21 LCD_VCC BIST (IN Port) 22 LCD_Self_Test(BIST) BIST (IN Port) 23 LCD_GND Logic GND 24 LCD_GND Logic GND 25 LCD_GND (Connect to GND in Module) 26 LCD_GND HPD (OUT Port 2.5V/3.3V) 28 BL_GND BLU GND 29 BL_GND BLU GND 30 BL_GND (Connect to GND in Module)	16	AUX_CH_N	
19 LCD_VCC LCD Logic Power 20 LCD_VCC (3.3±0.3V) 21 LCD_VCC BIST (IN Port) 22 LCD_Self_Test(BIST) BIST (IN Port) 23 LCD_GND Logic GND 24 LCD_GND (Connect to GND in Module) 25 LCD_GND (Connect to GND in Module) 27 HPD HPD (OUT Port 2.5V/3.3V) 28 BL_GND BLU GND 30 BL_GND (Connect to GND in Module)	17	H_GND	
20 LCD_VCC (3.3±0.3V) 21 LCD_VCC BIST (IN Port) 22 LCD_Self_Test(BIST) BIST (IN Port) 23 LCD_GND Logic GND 24 LCD_GND (Connect to GND in Module) 25 LCD_GND (HPD 27 HPD HPD (OUT Port 2.5V/3.3V) 28 BL_GND BLU GND 30 BL_GND (Connect to GND in Module)	18	LCD_VCC	
20 LCD_VCC (3.3±0.3V) 21 LCD_VCC 22 LCD_Self_Test(BIST) BIST (IN Port) 23 LCD_GND 24 LCD_GND Logic GND 25 LCD_GND (Connect to GND in Module) 26 LCD_GND HPD (OUT Port 2.5V/3.3V) 28 BL_GND BLU GND 30 BL_GND (Connect to GND in Module)	19	LCD_VCC	LCD Logic Power
22 LCD_Self_Test(BIST) BIST (IN Port) 23 LCD_GND Logic GND 24 LCD_GND (Connect to GND in Module) 25 LCD_GND (HPD (OUT Port 2.5V/3.3V) 27 HPD HPD (OUT Port 2.5V/3.3V) 28 BL_GND BLU GND 29 BL_GND BLU GND 30 BL_GND (Connect to GND in Module)	20	LCD_VCC	
23 LCD_GND 24 LCD_GND 25 LCD_GND 26 LCD_GND 27 HPD 4 HPD (OUT Port 2.5V/3.3V) 28 BL_GND 29 BL_GND 30 BL_GND (Connect to GND in Module)	21	LCD_VCC	
24 LCD_GND Logic GND 25 LCD_GND (Connect to GND in Module) 26 LCD_GND 27 HPD HPD (OUT Port 2.5V/3.3V) 28 BL_GND 29 BL_GND BLU GND 30 BL_GND (Connect to GND in Module)	22	LCD_Self_Test(BIST)	BIST (IN Port)
25 LCD_GND (Connect to GND in Module) 26 LCD_GND 27 HPD HPD (OUT Port 2.5V/3.3V) 28 BL_GND 29 BL_GND BLU GND 30 BL_GND (Connect to GND in Module)	23	LCD_GND	
26 LCD_GND 27 HPD HPD (OUT Port 2.5V/3.3V) 28 BL_GND 29 BL_GND BLU GND 30 BL_GND (Connect to GND in Module)	24	LCD_GND	Logic GND
27 HPD HPD (OUT Port 2.5V/3.3V) 28 BL_GND 29 BL_GND BLU GND 30 BL_GND (Connect to GND in Module)	25	LCD_GND	(Connect to GND in Module)
28 BL_GND 29 BL_GND BLU GND 30 BL_GND (Connect to GND in Module)	26	LCD_GND	
28 BL_GND 29 BL_GND 30 BL_GND (Connect to GND in Module)	27	HPD	HPD (OUT Port 2.5V/3.3V)
30 BL_GND (Connect to GND in Module)	28	BL_GND	
	29	BL_GND	
	30		(Connect to GND in Module)
31 BL_GND	31	BL_GND	
32 BL_ENABLE IN Port	32		
33 BL_PWM IN Port		BL_PWM	
34 H_sync H_sync (OUT Port)	34	H_sync	H_sync (OUT Port)
NC NC	35		NC
36 BL_PWR			
37 BL_PWR BLU Power	37	BL_PWR	BLU Power
38 BL_PWR (5~21V)	38	BL_PWR	(5~21V)
39 BL_PWR	39	BL_PWR	
40 Color Engine NC	40	Color Engine	NC

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5.2. eDP Interface



Note. Transmitter: Novatek NT71870. Transmitter is not contained in Module.

5.3.eDP Input signal

Lane 0	Lane 1
R0-7:0	R1-7:0
G0-7:0	G1-7:0
B0-7:0	B1-7:0
R2-7:0	R3-7:0
G2-7:0	G3-7:0
B2-7:0	B3-7:0
R4-7:0	R5-7:0
G4-7:0	G5-7:0
B4-7:0	B5-7:0

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6.0 SIGNAL TIMING SPECIFICATION

6.1 Timing Parameters

	Item	Symbols	Min	Тур	Max	Unit
Frequency		1/Tc	171.03	342.05		MHz
Clock	High Time	Tch	-	4/7Tc	ı	Tc
	Low Time	Tcl	-	3/7Tc	ı	Tc
			-	2284	ı	lines
Fra	me Period	Tv	72	144	144	Hz
			13.9	6.9	6.9	ms
Vert	Vertical Display Period		-	1080	ı	lines
One line Scanning Period Horizontal Display Period		Th	-	2080	-	clocks
		Thd	-	1920	-	clocks

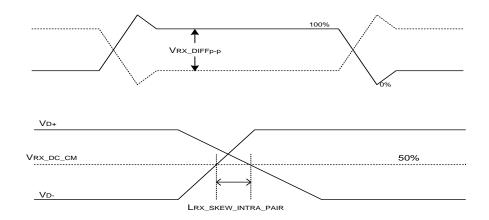
Note*: This Module can support low frame refresh rate 60Hz

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6.2 eDP Rx Interface Timing ParameterThe specification of the eDP Rx interface timing parameter is shown in Table 8.

<Table 9. eDP Rx Interface Timing Specification>

Item	Symbol	Min	Тур	Max	Unit	Remark
Spread spectrum clock	SSC		0.5		%	
Differential peak-to-peak input voltage at package pins	VRX-DIFFp-p	70	-	-	mV	
Rx input DC common mode voltage	VRX_DC_CM	-	GND	-	V	
Differential termination resistance	RRX-DIFF	80	100	120	Ω	
Single-ended termination resistance	Rrx-se	40	-	60	Ω	
Rx short circuit current limit	IRX_SHORT	-	_	50	mA	
Intra-pair skew at Rx package p ins (HBR) RX intra-pair skew tolerance at HBR	LRX_SKEW_ INTRA_PAIR	-	-	150	ps	



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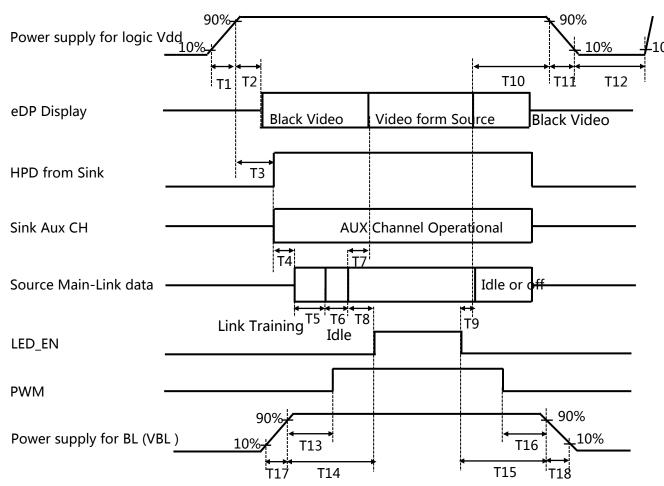
7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

		Colors &									Data	sig	nal													
		Gray scale	R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	В0	В1	B2	В3	В4	B5	В6	В7
		Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Basic		Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
colors		Light Blue	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Purple	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
		White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Δ	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray scale	of	Δ				,	1								1							•	†			
Red		∇				,	l								↓							,	<u> </u>			
		Brighter	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		∇	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Δ	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Darker	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray scale	of	Δ				,	1								1							•	1			
Green		∇				,	ļ								↓								<u> </u>			
		Brighter	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
		∇	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
		Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
		Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Δ	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
		Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Gray scale	of	Δ				,	Ì								1							,	Î.			
Blue		∇				,	l .								↓								<u> </u>			
		Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1_	1_
	ļ	∇	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
		Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
_		Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray		Δ	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
scale		Darker	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
of		Δ				,	1								1							•	Î.			
White		∇				,	<u> </u>								↓								<u> </u>			
&		Brighter	1	0	1	1	1	1	1	1	1		1	1	1	1	1	1	1	0	1	1	1	1	1	1
Black		∇	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1_	1	0	1	1	1	1	1	1	1
		White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off se quence shall be as shown in below



- $0.5 \text{ms} \leq \text{T1} \leq 10 \text{ ms}$
- 0ms ≤ T2 ≤ 200 ms
- 0ms ≤ T3 ≤ 200 ms
- 0ms ≤ T13
- 0ms ≤ T14
- 0ms ≤ T17
- 80ms ≤ T8

- 0ms ≤ T7 ≤ 50ms
- 0ms ≤ T10 ≤ 500 ms
- $\bullet \quad 0.5 ms \qquad \leq \ T11 \ \leq \ 10 \ ms$
- 500ms ≤ T12
- 0ms ≤ T15
- 0ms ≤ T16
- 0ms ≤ T18

Notes:

- 1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
- 2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

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9.0 Connector Description

Physical interface is described as for the connector on LCM. These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

Connector Name /Description	For Signal Connector					
Manufacturer	STM					
Type/ Part Number	MSAK24025P40					
Mating housing/ Part Number	I-PEX 20454-030T					

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10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

FIGURE 6 shows mechanical outlines for the model NV156FHM-N4G v3.0. Other parameters are shown in Table 9.

<Table 10. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	344.16(H) × 193.59(V)	mm
Number of pixels	1920(H) × 1080(V)	
Pixel pitch	0.17925(H) × 0.17925(V)	mm
Pixel arrangement	RGB Vertical stripe	
Display colors	16.7M	
Display mode	HADS	
Dimensional outline	350.66(TYP)*215.25(TYP)*2.6(MAX)	mm
Weight	280Max	gram
Posk Light	Connector :MSK24022P10D	
Back Light	6P*8S	

10.2 Mounting

See FIGURE 6.

10.3 Glare and Polarizer Hardness.

The surface of the LCD has a glare coating to maximize readability and hard coating to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

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11.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

<Table 11. Reliability test>

		-
No	Test Items	Conditions
1	High temperature storage test	Ta = 70 °C, 240 hrs
2	Low temperature storage test	Ta = -30 °C, 240 hrs
3	High temperature/High humidity Storage	Ta = 60 °C, 90%RH, 240 hrs
4	High temperature operation test	Ta = 60 °C, 240 hrs
5	Low temperature operation test	Ta = -10 °C, 240 hrs
6	Thermal Shock Storage	Ta = -30 °C ↔ 70 °C (0.5 hr), 27 cycle
7	Package Drop test	Height: 60cm, 1 corner, 3 edges, 6 surfaces: 1 time for each direction
8	Shock test	220G, 2ms, Half sine
^	(non-operating)	$\pm X, \pm Y, \pm Z$
9	Package Vibration test	Frequency range: 10-55Hz, stroke:1.5mm, swep time: 1 minute, test period: 2 hours for each direction of X, Y, Z
10	Electro-static discharge test	Power OFF: Air discharged +/- 15kV Criteria C Contact discharged +/- 8kV Criteria C Power ON: Air discharged +/- 10kV Criteria B Contact discharged +/- 6kV Criteria B

12.0 HANDLING & CAUTIONS

- (1) Cautions when taking out the module
 - Pick the pouch only, when taking out module from a shipping package.
- (2) Cautions for handling the module
 - As the electrostatic discharges may break the LCD module, handle the LCD module with
 - care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
 - As the LCD panel and back light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
 - As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

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(4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics

- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions

- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken.

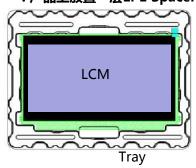
We recommend to use the original shipping packages.

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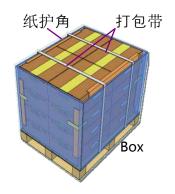
13.0 PACKING INFORMATION(产品形态:)

Packing procedure:

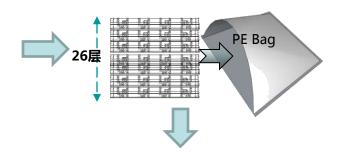
- -. 将 1pcs MDL 平放入Tray, CF 侧向上放置;
- -. 产品上放置一层EPE Spacer



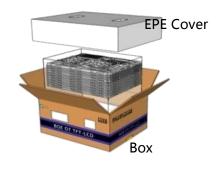
- -. 每个Pallet上放3层Box 1层4箱,共计12ea Box
- -. Pallet外进行缠膜包装
- -. 容量: 300pcs/Pallet



- -. 将26pcs PET Tray 平放入PE Bag 顶部1pcs 空Tray
- -. Tray 不旋转码放



- .将PET Tray堆码后平放入Inner Box 上下放置EPE Cover
- -. 容量: 25pcs/Inner Box



13.1 Packing Note(产品形态:LCM)

- Box Dimension: 500mm(W) x 400mm(D) x 300mm(H)
- Package Quantity in one Box: 25pcs

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13.2 Box label (产品形态: LCM)

DDUDITION COULD

• Label Size:115mm*80mm

Contents

1. FG-CODE: NV156FHM-N4G V3.0

2. Box 包装数量

3. Box ID, 编码规则如下

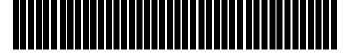
4. Box Packing 日期

5. 客户料号: 5D10R00685

BOE BOE Technology Group Co., Ltd.

MODEL: NV156FHM-N4G V3.0 ① QTY: 25 ②

SERIAL NO: XXXXXXXXXXXXXXX ③ DATE: 20XX . XX ④



XXXXX-XXXXXXXX (5)

XXXX

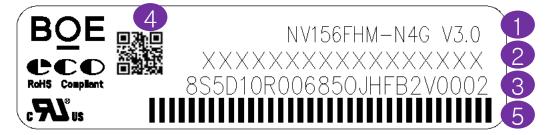


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14.0 Product Label



标签贴付于产品背面左下角 标签尺寸: 48mm × 12mm 物料编号: 44-9231007

PRODUCT GROUP

- 1. FG-CODE: NV156FHM-N4G V3.0
- 2. MDL ID
- 3. PPID
- 4. PPID对应二维码
- 5. MDL ID对应条形码

MDL ID 编码规则

序 列 号	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
代码	Х	Χ	Р	3	1	2	7	Х	Х	Х	Х	0	0	1	Е	П	J
描述	GBN	代码	等级	В3	年	份	月	F	G Cod	e后四位	Ĭ.			序列	引号		

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15.0 APPENDIX

Mechanical DrawingDrawing Attachment: Front

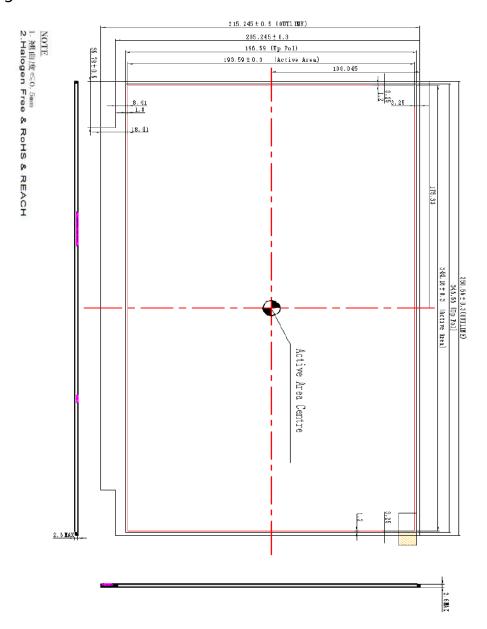
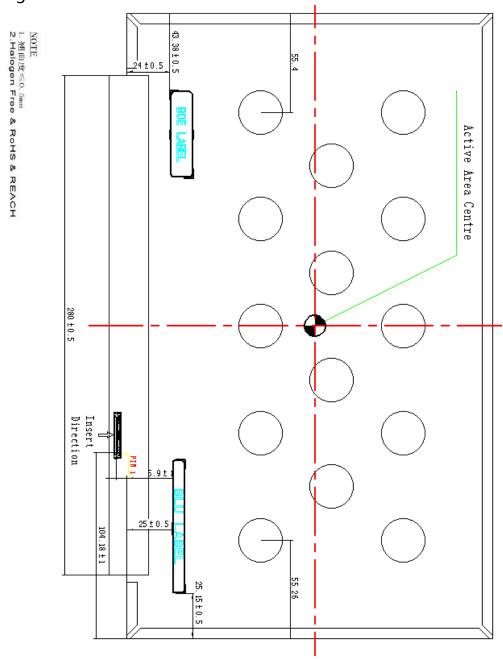


Figure 3. MDL OUTLINE

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Mechanical DrawingDrawing Attachment: Back



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16.0 EDID Table

Address (HEX)	Function	Hex	Dec	Input values.	Notes
00		00	0	0	
01]	FF	255	255	
02		FF	255	255	
03	114	FF	255	255	EDID Handau
04	Header	FF	255	255	EDID Header
05		FF	255	255	
06		FF	255	255	
07		00	0	0	
08	ID Manufacturer Na	09	9	DOE	ID 005
09	me	E5	229	BOE	ID = BOE
0A	TD D 1 C	AF	175	1067	ID 1067
0B	ID Product Code	07	7	1967	ID = 1967
0C		00	0	0	
0D	22.1.	00	0	0	
0E	32-bit serial No.	00	0	0	
0F		00	0	0	
10	Week of manufactur e	01	1	1	
11	Year of Manufacture	1C	28	2018	Manufactured in 2017
12	EDID Structure Ver.	01	1	1	EDID Ver 1.0
13	EDID revision #	04	4	4	EDID Rev. 0.4
14	Video input definitio n	A5	165	-	
15	Max H image size	22	34	34	34.416 cm (Approx)
16	Max V image size	13	19	19	19.359 cm (Approx)
17	Display Gamma	78	120	2.2	Gamma curve = 2.2
18	Feature support	02	2	-	RGB display, Preferred Timming mode
19	Red/Green low bits	4C	76	-	Red / Green Low Bits
1A	Blue/White low bits	30	48	-	Blue / White Low Bits
1B	Red x high bits	A4	164	0.642	Red (x) = 10100100 (0.642)
1C	Red y high bits	54	84	0.329	Red $(y) = 01010100 (0.329)$
1D	Green x high bits	51	81	0.316	Green $(x) = 01010001 (0.316)$
1E	Green y high bits	9B	155	0.606	Green $(y) = 10011011 (0.606)$
1F	Blue x high bits	27	39	0.153	Blue (x) = $00100111 (0.153)$
20	BLue y high bits	0C	12	0.050	Blue (y) = 00001100 (0.050)
21	White x high bits	50	80	0.313	White $(x) = 01010000 (0.313)$
22	White y high bits	54	84	0.329	White $(y) = 01010100 (0.329)$
23	Established timing 1	00	0	-	(,,
24	Established timing 2	00	0	_	

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25	Established timing 2	00	0		
26	Established timing 3	00		-	
27	Standard timing #1		1		Not Used
28		01	1		
29	Standard timing #2	01	1		Not Used
		01	1		
2A	Standard timing #3	01	1		Not Used
2B		01 1			
2C	Standard timing #4	01	1		Not Used
2D		01	1		
2E	Standard timing #5	01	1		Not Used
2F		01	1		
30	Standard timing #6	01	1		Not Used
31	_	01	1		
32	Standard timing #7	01	1		Not Used
33	-	01	1		
34	Standard timing #8	01	1		Not Used
35	_	01	1		
36		9D	157	342.1	342.052MHz Main clock
37	-	85	133		
38	-	80	128	1920	Hor Active = 1920
39	-	A0	160	160	Hor Blanking = 160
3A	-	70	112	-	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B	-	38	56	1080	Ver Active = 1080
3C		3E	62	62	Ver Blanking = 62
3D		40	64	-	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E	Detailed timing/mo	6C	108	108	Hor Sync Offset = 108
3F	nitor descriptor #1	30	48	48	H Sync Pulse Width = 48
40		AA	170	10	V sync Offset = 10 line
41		00	0	10	V Sync Pulse width: 10 line
42		58	88	344	Horizontal Image Size = 344.16 mm (Low 8 bits)
43		C1	193	194	Vertical Image Size = 193.59 mm (Low 8 bits)
44		10	16	-	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0	0	Hor Border (pixels)
46		00	0	0	Vertical Border (Lines)
47		1A	26	-	Refer to right table

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		CDEC TITLE		

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SPEC. NUMBERSPEC. TITLEPAGENV156FHM-N4G V3.0 Product Specification32 OF 33

16.0 EDID Table

	1		1	1	
48		CE	206	171	171.026MHz Main clock
49		42	66	1,1	TO TIOZOT IT Z TIGHT GOCK
4A		80	128	1920	Hor Active = 1920
4B		A0	160	160	Hor Blanking = 160
4C		70	112	-	4 bits of Hor. Active + 4 bits of Hor. Blanking
4D		38	56	1080	Ver Active = 1080
4E		3E	62	62	Ver Blanking = 62
4F		40	64	-	4 bits of Ver. Active + 4 bits of Ver. Blanking
50	Detailed timing/mo	6C	108	108	Hor Sync Offset = 108
51	nitor	30	48	48	H Sync Pulse Width = 48
52	descriptor #2	AA	170	10	V sync Offset = 10 line
53	1	00	0	10	V Sync Pulse width: 10 line
54]	58	88	344	Horizontal Image Size = 344.16 mm (Low 8 bits)
55	1	C1	193	194	Vertical Image Size = 193.59 mm (Low 8 bits)
56		10	16	-	4 bits of Hor Image Size + 4 bits of Ver Image Size
57	1	00	0	0	Hor Border (pixels)
58	1	00	0	0	Vertical Border (Lines)
59]	1A	26	-	
5A		00	0		
5B	1	00	0		
5C	1	00	0		ASCII Data Sting Tag
5D	1	FE	254		
5E	1	00	0		
5F	1	42	66	В	
60	1	4F	79	0	
61	1	45	69	Е	
62	Detailed timing/mo	20	32		
63	nitor	48	72	Н	
64	descriptor #3	46	70	F	
65		0A	10		Manufacture name : BOEHF
66		20	32		
67		20	32		
68		20	32		
69	1	20	32		
6A	† †	20	32		
6B	†	20	32		

				-	
TFT- LCD PI	RODUCT	P2	2018-03-01	D⊻L	
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	NV156FHM-N4G V3.0 Product				OF 33

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16.0 EDID Table

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6C		00	0		
6D		00	0		
6E		00	0		Product Name Tag (ASCII)
6F		FE	254		
70		00	0		
71		4E	78	N	
72		56	86	V	
73		31	49	1	
74	Detailed timing/mon itor	35	53	5	
75	descriptor #4	36	54	6	
76	descriptor #4	46	70	F	Model name: NV156FHM-N4B
77		48	72	Н	Model Halle . NV150FHM-N4B
78		4D	77	М	
79		2D	45	-	
7A		4E	78	N	
7B		34	52	4	
7C		47	71	G	
7D		0A	10		
7E	Extension flag	00	0	1	0:1个EDID;N-1:N个EDID
7F	Checksum	70	112	-	