SPECIFICATION
FOR
APPROVAL

(●) **Preliminary Specification**
( ) **Final Specification**

Title	14.1” WXGA+ TFT LCD

BUYER	General
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LP141WP2
Suffix	TLA1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE
K. J. Kwon / S.Manager	
REVIEWED BY	
G. J. Han / Manager	
PREPARED BY	
K. Y. Kwon / Engineer	

Product Engineering Dept.
LG Display Co., Ltd

Contents

RECORD OF REVISIONS

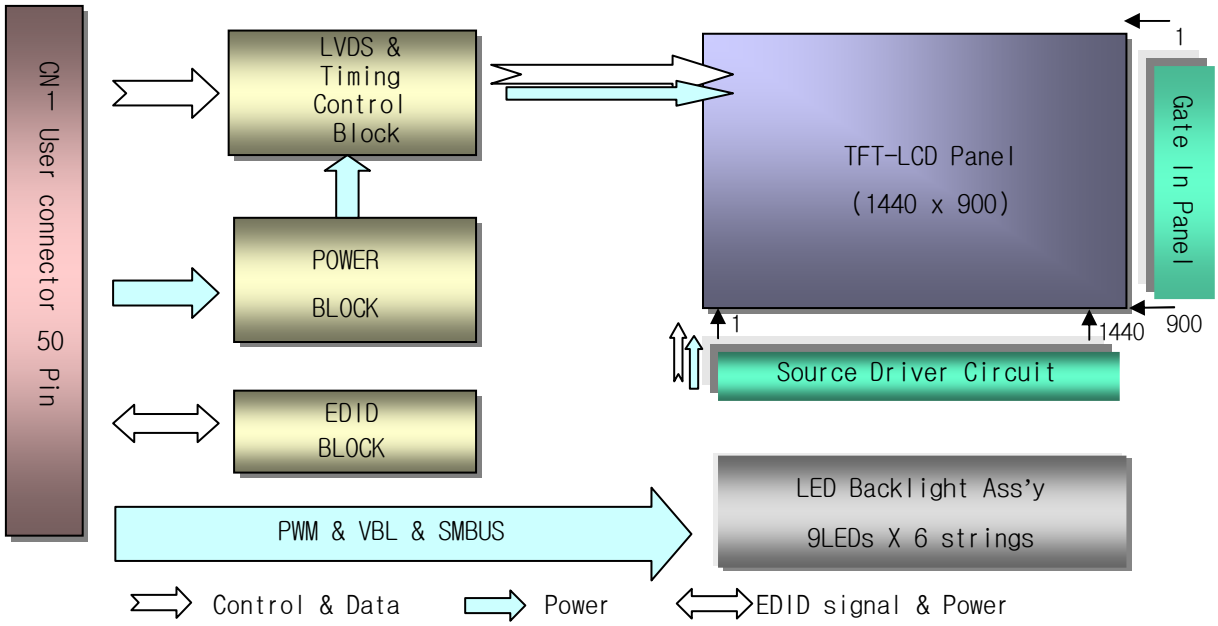
Revision No	Revision Date	Page	Description	EDID ver
0.0	22. Apr. 2008	-	First Draft (Preliminary Specification)	0.0

1. General Description

The LP141WP2 is a Color Active Matrix Liquid Crystal Display with an integral LED backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally white mode. This TFT-LCD has 14.1 inches diagonally measured active display area with WXGA+ resolution(1440 horizontal by 900 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors.

The LP141WP2 has been designed to apply the interface method that enables low power, high speed, low EMI.

The LP141WP2 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP141WP2 characteristics provide an excellent flat display for office automation products such as Notebook PC.



General Features

Active Screen Size	14.1 inches diagonal
Outline Dimension	320.0 (H) × 207.0 (V) × 5.5(D, max.) mm
Pixel Pitch	0.2106 mm × 0.2106 mm
Pixel Format	1440 horiz. by 900 vert. Pixels RGB strip arrangement
Color Depth	6-bit, 262,144 colors
Luminance, White	300 cd/m^2(Typ., @I_{LED}=19mA) , 5 points Average
Power Consumption	Total 5.45Watt @ LCM circuit 1.55W(Typ.), B/L 3.3 W (Typ.), LED Driver 0.6W(Typ.)
Weight	375g(Max.)
Display Operating Mode	Transmissive mode, normally white
Surface Treatment	Hard coating(3H) Anti Glare treatment of the front polarizer
RoHS Comply	Yes

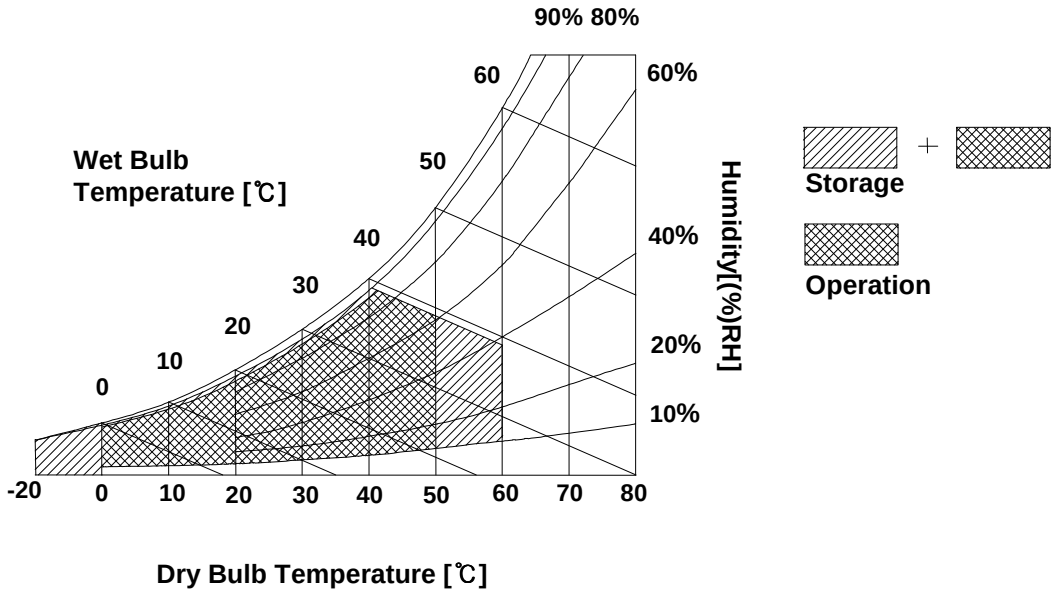
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	Vdc	at 25 ± 5°C
Operating Temperature	TOP	0	50	°C	1
Storage Temperature	HST	-20	60	°C	1
Operating Ambient Humidity	HOP	10	90	%RH	1
Storage Humidity	HST	10	90	%RH	1

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.



3. Electrical Specifications

3-1. Electrical Characteristics

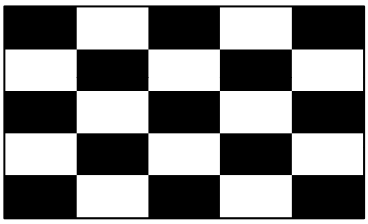
The LP141WP2 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input which powers the LED BL.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
MODULE :						
Power Supply Input Voltage	VCC	3.0	3.3	3.6	V_{DC}	
Power Supply Input Current	I_{CC}	400	470	540	mA	1
Power Consumption	Pc	-	1.55	1.78	Watt	1
Differential Impedance	Zm	90	100	110	Ohm	2
LED Backlight :						
Operating Voltage	V_{LED}	-	28.8	30.6	V	3
Operating Current per string	I_{LED}	-	19	-	mA	4
Power Consumption	P_{BL}	-	3.3	3.5	Watt	5
Life Time		10,000	-	-	Hrs	6

Note)

1. The specified current and power consumption are under the Vcc = 3.3V , 25℃, fv = 60Hz condition whereas Mosaic pattern is displayed and fv is the frame frequency.

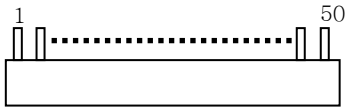


2. This impedance value is needed to proper display and measured form LVDS Tx to the mating connector.
3. The variance of the voltage is ± 10%.
4. The typical operating current is for the typical surface luminance (L_{WH}) in optical characteristics. I_{LED} is the current of each LEDs' string, LED backlight has 6 strings on it.
5. The LED power consumption shown above does not include power of external LED driver circuit for typical current condition.
6. The life time is determined as the time at which brightness of LED is 50% compare to that of initial value at the typical LED current.

3-2. Interface Connections

This LCD employs two interface connections, a 50 pin connector is used for the module electronics interface and the other connector is used for the internal backlight system.
The electronics interface connector is a model FI-VHP50S manufactured by JAE.

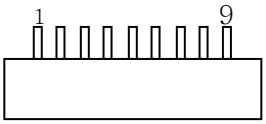
Table 3. MODULE CONNECTOR PIN CONFIGURATION (CN1)

Pin	Symbol	Description	Notes
1	Test Loop	Test Loop (only to pin 30)	1, Interface chips 1.1 LCD : SW, ST2_BS (LCD Controller) including LVDS Receiver 1.2 System : * Pin to Pin compatible with LVDS 2.Connector 2.1 LCD :JAE FI-VHP50 or equivalent (1.0 mm thickness, lock-in type, pin 1 starts from left on the front) 2.2 Mating:JAE FI-VHP50 series or equivalent (micro-coax type) 2.3 Connector pin arrangement LCD rear view  [LCD Module Rear View]
2	VEEDID	EDID 3.3V power	
3	VSS	Ground	
4	CLK EEDID	EDID clock	
5	DATA EEDID	EDID data	
6	VSS	Ground	
7	Odd_Rin0-	Negative LVDS differential data input	
8	Odd_Rin0+	Positive LVDS differential data input	
9	VSS1	Ground	
10	Odd_Rin1-	Negative LVDS differential data input	
11	Odd_Rin1+	Positive LVDS differential data input	
12	VSS2	Ground	
13	Odd_Rin2-	Negative LVDS differential data input	
14	Odd_Rin2+	Positive LVDS differential data input	
15	VSS3	Ground	
16	Odd_ClkIN-	Negative LVDS differential clock input	
17	Odd_ClkIN+	Positive LVDS differential clock input	
18	VSS4	Ground	
19	Even_Rin0-	Negative LVDS differential data input	
20	Even_Rin0+	Positive LVDS differential data input	
21	VSS5	Ground	
22	Even_Rin1-	Negative LVDS differential data input	
23	Even_Rin1+	Positive LVDS differential data input	
24	VSS6	Ground	
25	Even_Rin2-	Negative LVDS differential data input	
26	Even_Rin2+	Positive LVDS differential data input	
27	VSS7	Ground	
28	Even_ClkIN-	Negative LVDS differential clock input	
29	Even_ClkIN+	Positive LVDS differential clock input	
30	Test Loop	Test Loop (only to pin 1)	

1	CONNTST	Connector test (only to pin 20)	
2	VDD	Logic power 3.3V	
3	VDD	Logic power 3.3V	
4	TEST(BIST_EN)	Panel Self Test	
5	+5V_ALW	No connection	
6	VSS	Ground	
7	VSS	Ground	
8	PWM_BL	PWM brightness control	
9	VBL-	LED power return	
10	VBL-	LED power return	
11	VBL-	LED power return	
12	VBL-	LED power return	
13	NC	No connect	
14	VBL+	7V ~ 20V LED power	
15	VBL+	7V ~ 20V LED power	
16	VBL+	7V ~ 20V LED power	
17	VBL+	7V ~ 20V LED power	
18	SMB_DATA	SMBus Data	
19	SMB_CLK	SMBus Clk	
20	CONNTST	Connector test(only to pin 1)	

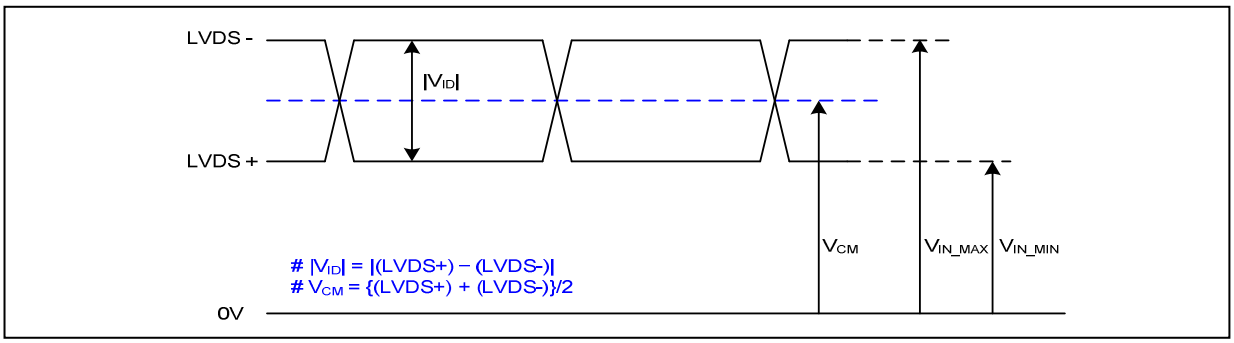
The LED backlight connector is a model TF12-9S-0.5H, manufactured by Hirose.

Table 4. BACKLIGHT CONNECTOR PIN CONFIGURATION (CN2)

Pin	Symbol	Description	Notes
1	Vdc(1,2,3,4,5,6)	LED Anode(Positive)	
2	Vdc(1,2,3,4,5,6)	LED Anode(Positive)	
3	NC	No Connection	
4	Vdc1	LED Cathode (Negative)	
5	Vdc2	LED Cathode (Negative)	
6	Vdc3	LED Cathode (Negative)	
7	Vdc4	LED Cathode (Negative)	
8	Vdc5	LED Cathode (Negative)	
9	Vdc6	LED Cathode (Negative)	

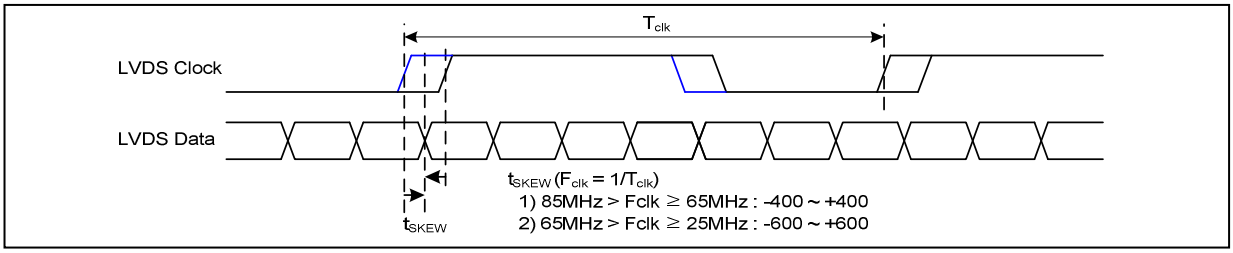
3-3. LVDS Signal Timing Specifications

3-3-1. DC Specification

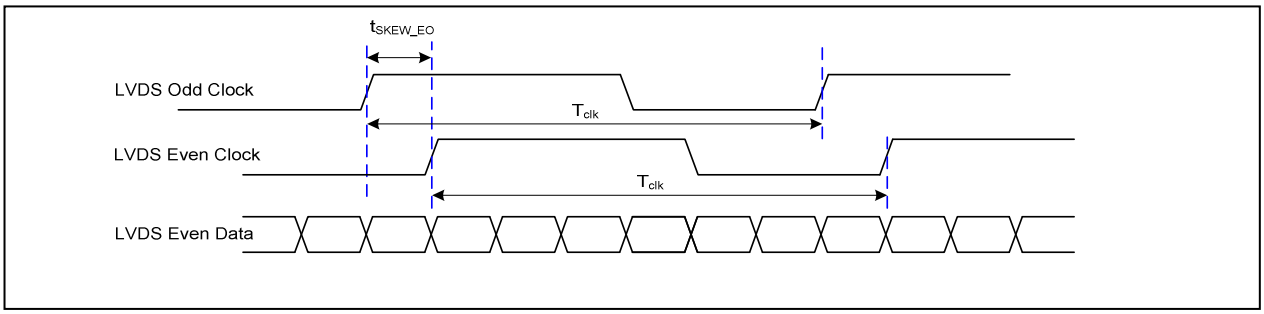


Description	Symbol	Min	Max	Unit	Notes
LVDS Differential Voltage	$\|V_{ID}\|$	100	600	mV	-
LVDS Common mode Voltage	V_{CM}	0.6	1.8	V	-
LVDS Input Voltage Range	V_{IN}	0.3	2.1	V	-

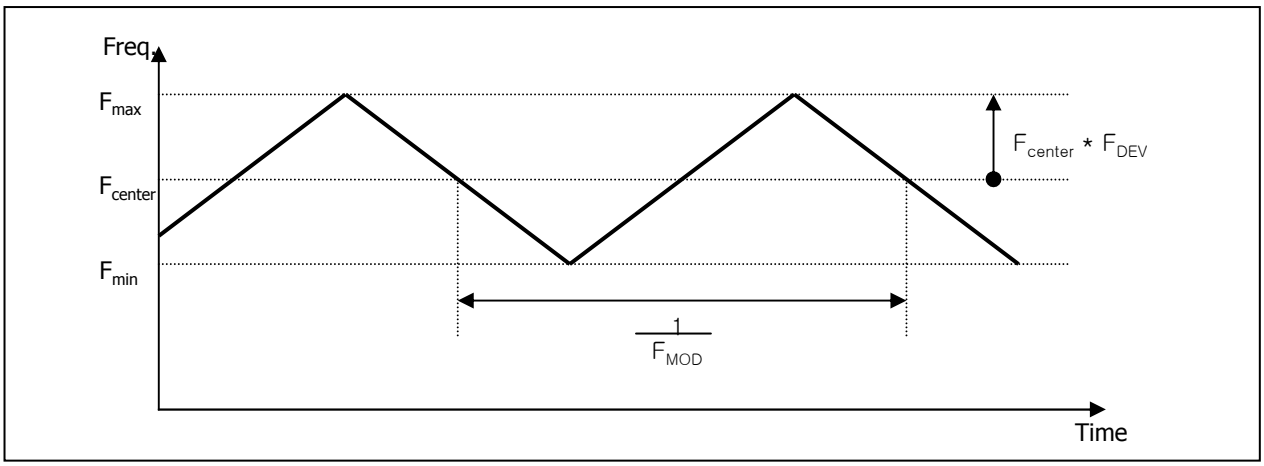
3-3-2. AC Specification



Description	Symbol	Min	Max	Unit	Notes
LVDS Clock to Data Skew Margin	t_{SKEW}	- 400	+ 400	ps	85MHz > Fclk ≥ 65MHz
	t_{SKEW}	- 600	+ 600	ps	65MHz > Fclk ≥ 25MHz
LVDS Clock to Clock Skew Margin (Even to Odd)	t_{SKEW_EO}	- 1/7	+ 1/7	T_{clk}	-
Maximum deviation of input clock frequency during SSC	F_{DEV}	-	± 3	%	-
Maximum modulation frequency of input clock during SSC	F_{MOD}	-	200	KHz	-



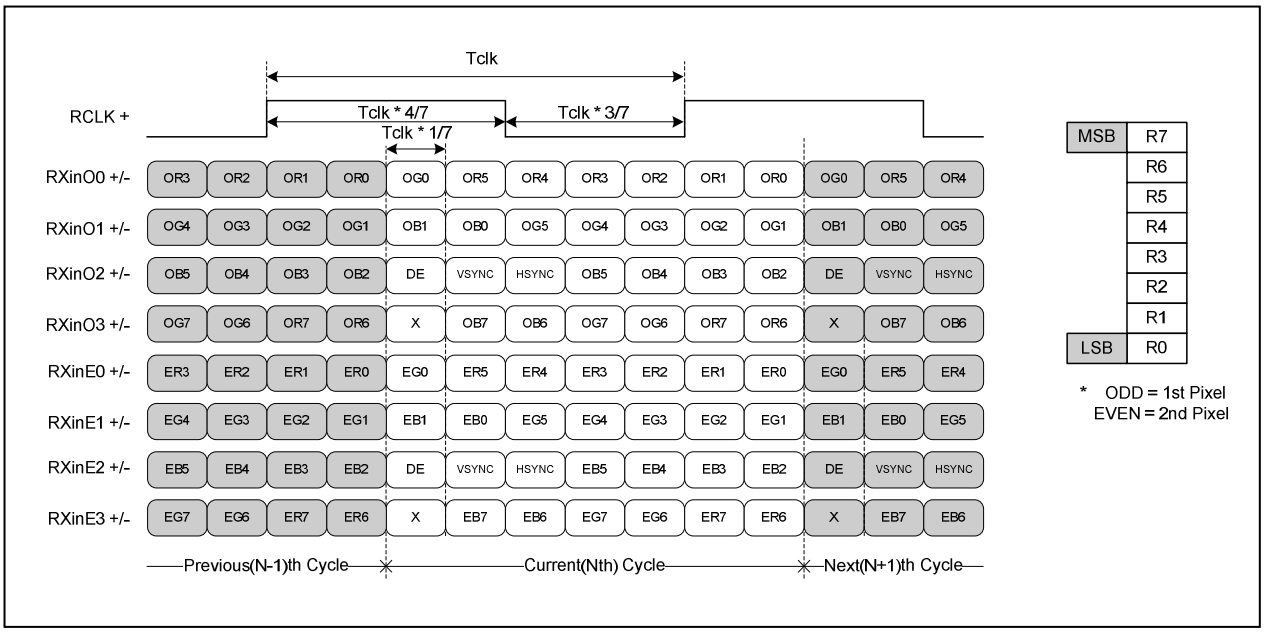
< Clock skew margin between channel >



< Spread Spectrum >

3-3-3. Data Format

- LVDS 2 Port



< LVDS Data Format >

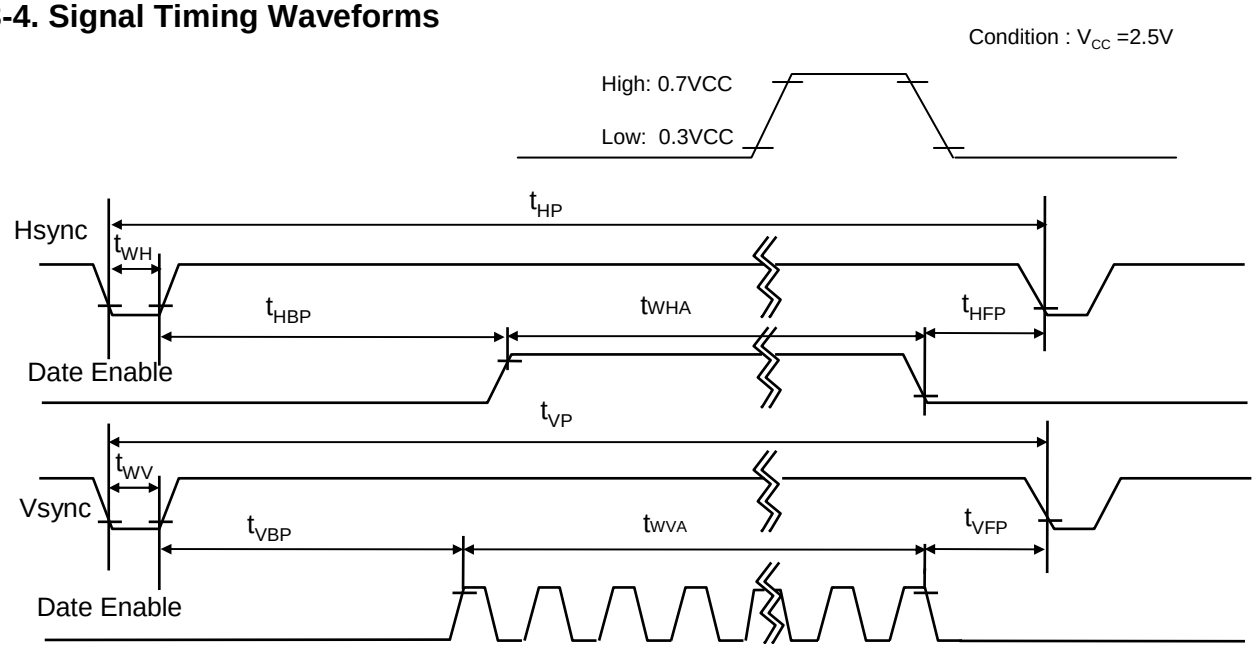
3-3-4. Signal Timing Specifications

This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of LVDS Tx/Rx for its proper operation.

Table 5. TIMING TABLE

ITEM	Symbol		Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	f_{CLK}	-	50.8	-	MHz	
Hsync	Active	tw_{HA}	896	912	928	tCLK	
	Period	t_{HP}	16	16	16		
	Width-Active	t_{WH}	720	720	720		
Vsync	Active	tw_{VA}	920	926	939	tHP	
	Period	t_{VP}	3	6	10		
	Width-Active	t_{WV}	900	900	900		
Data Enable	Horizontal back porch	t_{HBP}	144	152	160	tCLK	
	Horizontal front porch	t_{HFP}	20	24	28		
	Vertical back porch	t_{VBP}	12	17	23	tHP	
	Vertical front porch	t_{VFP}	2	3	6		

3-4. Signal Timing Waveforms



3-5. Color Input Data Reference

The brightness of each primary color (red,green and blue) is based on the 6-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 6. COLOR DATA REFERENCE

Color		Input Color Data																	
		RED						GREEN						BLUE					
		MSB					LSB	MSB					LSB	MSB					LSB
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	...			...						...						...			
	RED (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	...			...						...						...			
	GREEN (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	BLUE (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	...			...						...						...			
	BLUE (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

3-6. Power Sequence

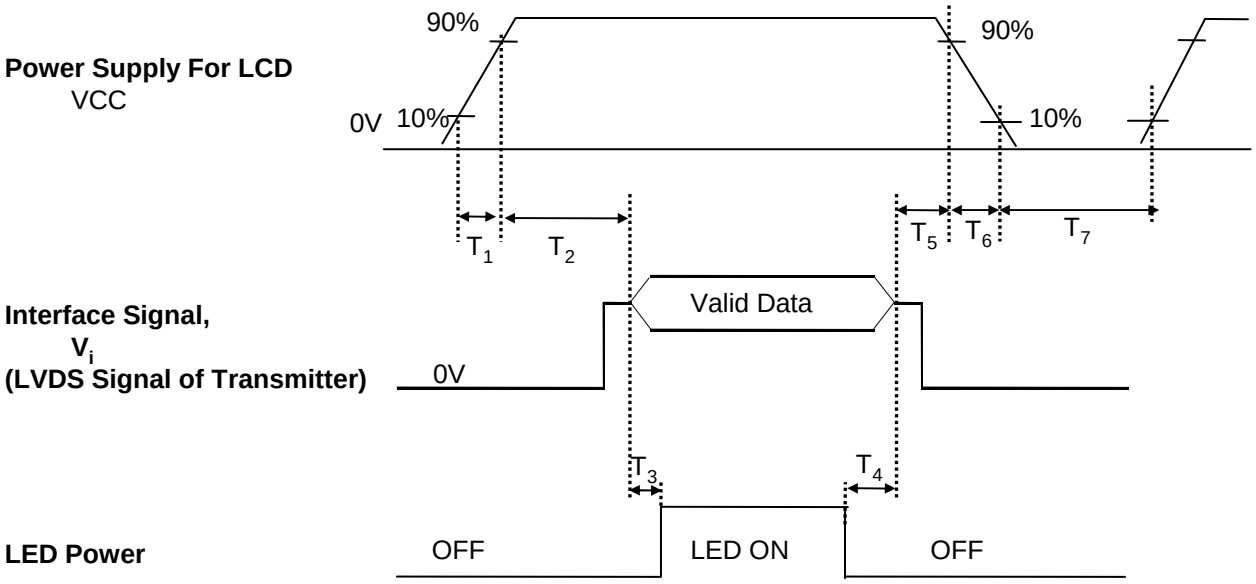


Table 7. POWER SEQUENCE TABLE

Parameter	Value			Units
	Min.	Typ.	Max.	
T_1	0	-	10	(ms)
T_2	0	-	50	(ms)
T_3	200	-	-	(ms)
T_4	200	-	-	(ms)
T_5	0	-	50	(ms)
T_6	0	-	10	(ms)
T_7	400	-	-	(ms)

Note)
1. Valid Data is Data to meet “3-3. LVDS Signal Timing Specifications”
2. Please avoid floating state of interface signal at invalid period.
3. When the interface signal is invalid, be sure to pull down the power supply for LCD VCC to 0V.
4. Lamp power must be turn on after power supply for LCD and interface signal are valid.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 20 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0°.
FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

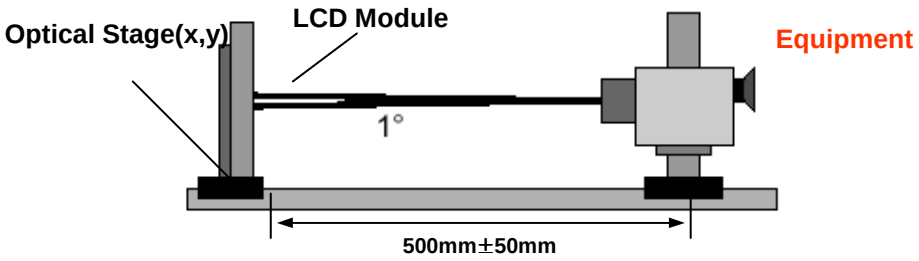


Table 8. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz, f_{CLK}= 102MHz, I_{LED} = 19mA

Parameter	Symbol	Values			Units	Notes
		Min	Typ	Max		
Contrast Ratio	CR	300	-	-		1
Surface Luminance, white	L_{WH}	250	300	-	cd/m^2	2
Luminance Variation(13points)	δ_{WHITE}		1.4	1.6		3
Response Time	Tr_R+ Tr_D		16	25	ms	4
Color Coordinates						
RED	RX	0.547	0.577	0.607		
	RY	0.319	0.349	0.379		
GREEN	GX	0.299	0.329	0.359		
	GY	0.520	0.550	0.580		
BLUE	BX	0.132	0.162	0.192		
	BY	0.103	0.133	0.163		
WHITE	WX	0.283	0.313	0.343		+/- 0.030
	WY	0.299	0.329	0.359		+/- 0.030
Viewing Angle						5
x axis, right(Φ=0°)	Θr	40	45	-	degree	
x axis, left (Φ=180°)	Θl	40	45	-	degree	
y axis, up (Φ=90°)	Θu	10	15	-	degree	
y axis, down (Φ=270°)	Θd	30	35	-	degree	
Gray Scale				-		6

Notes)

1. Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the 5point (1~5)average across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 2.
   When I_{LED}= 19mA, L_{WH}=300cd/m^2(Typ.)

3. Luminance variation is measured for 13 point For more information see FIG 2.
   δ WHITE = Maximum(LN1,LN2, ….. LN13) ÷ Minimum(LN1,LN2, ….. LN13)

4. Response time is the time required for the display to transition from white to black (rise time, Tr_R) and from black to white(Decay Time, Tr_D). For additional information see FIG 3.

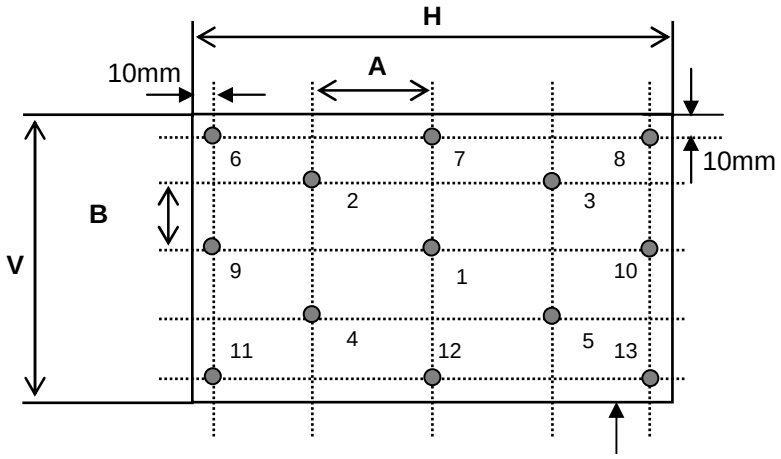
5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

6. Gray scale specification * f_V=60Hz

Gray Level	Luminance [%] (Typ)
L0	0.33
L7	1.47
L15	4.5
L23	10.7
L31	19.9
L39	33.0
L47	50.8
L55	73.0
L63	100

FIG. 2 Luminance

<Measuring point for Average Luminance & measuring point for Luminance variation>



H,V : ACTIVE AREA
A : H/4 mm
B : V/4 mm
POINTS: 13 POINTS

FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.

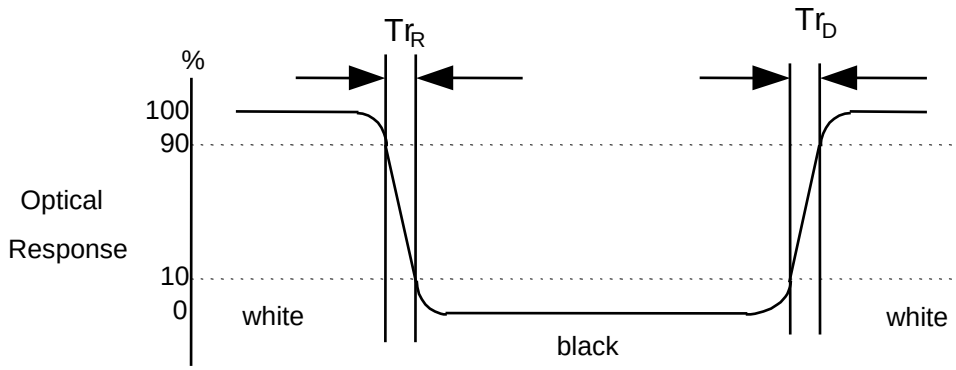
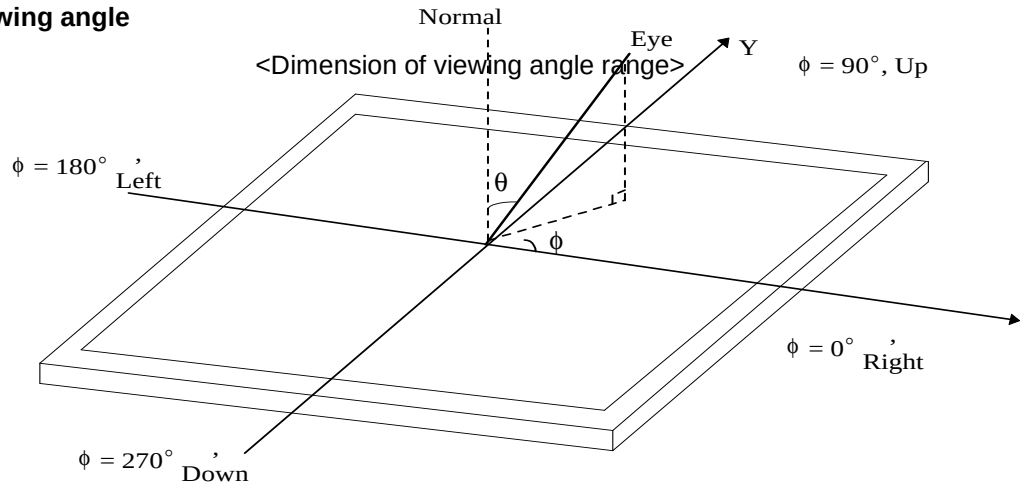


FIG. 4 Viewing angle

<Dimension of viewing angle range>



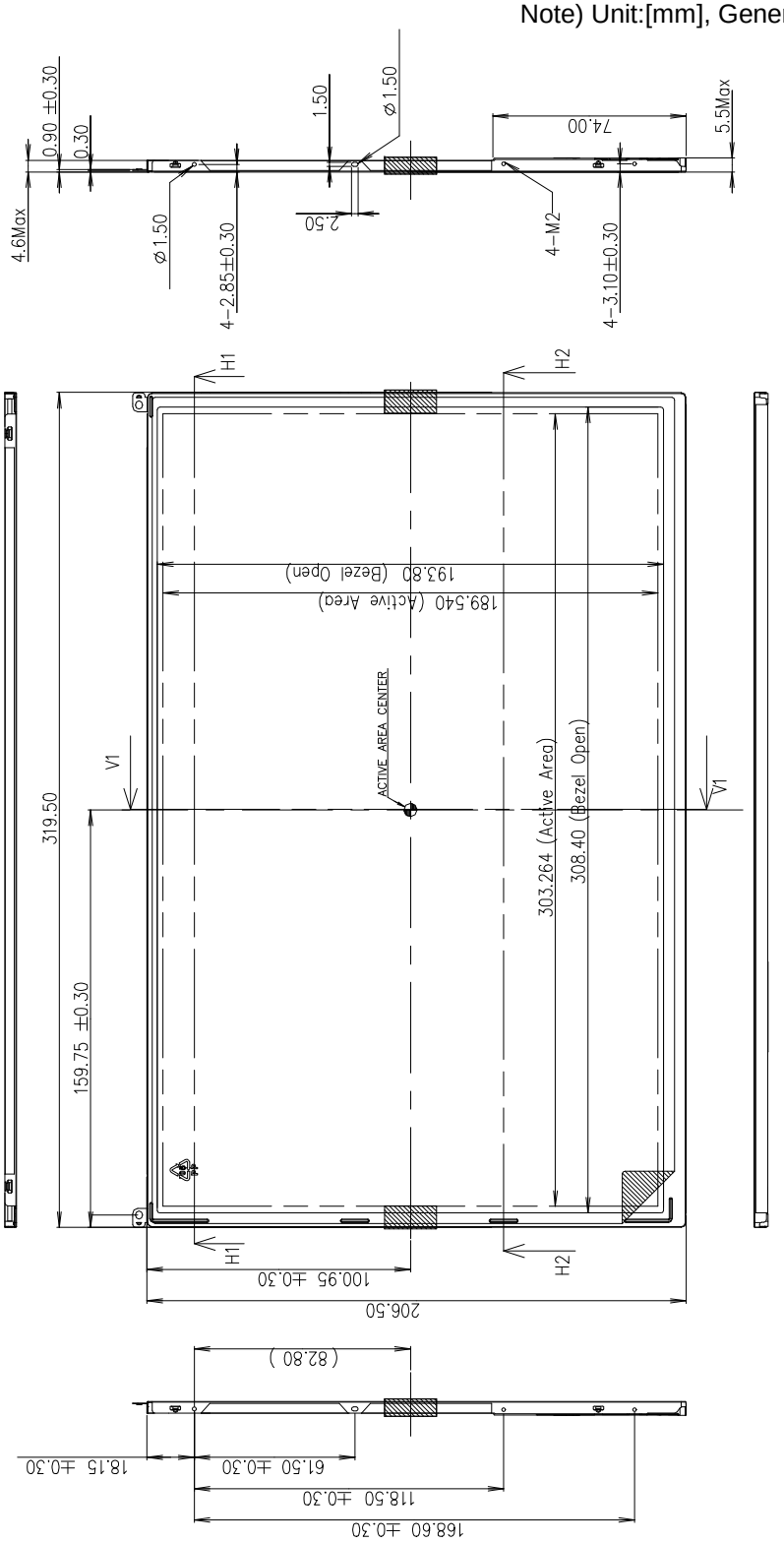
5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LP141WP2.
In addition the figures in the next page are detailed mechanical drawing of the LCD.

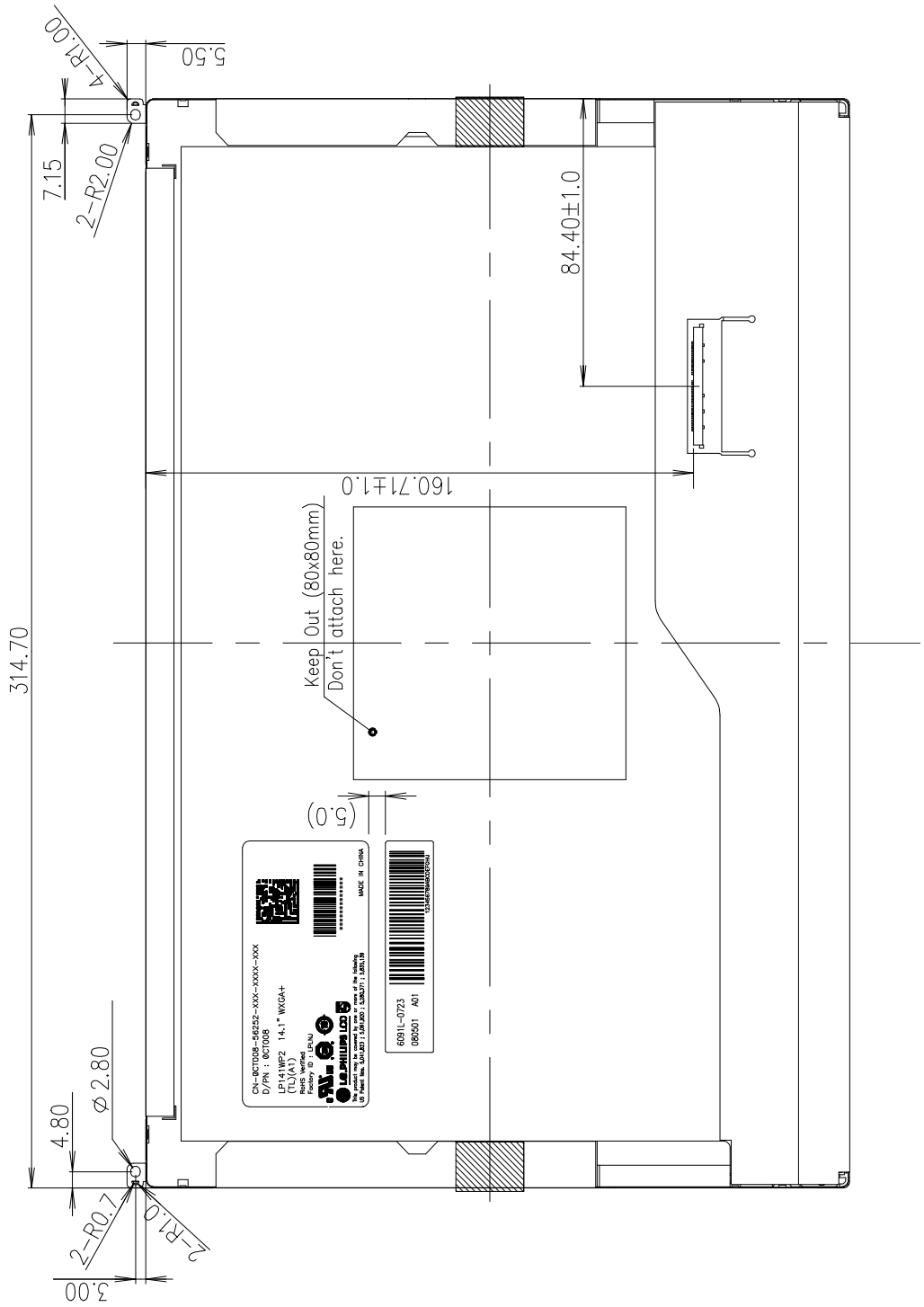
Outline Dimension	Horizontal	319.5 ± 0.50mm
	Vertical	206.5 ± 0.50mm
	Depth	5.5mm(Max.)
Bezel Area	Horizontal	308.4mm
	Vertical	193.8mm
Active Display Area	Horizontal	303.264mm
	Vertical	189.54 mm
Weight	375g (Max.)	
Surface Treatment	Hard coating(3H) Anti Glare treatment of the front polarizer	

<FRONT VIEW>

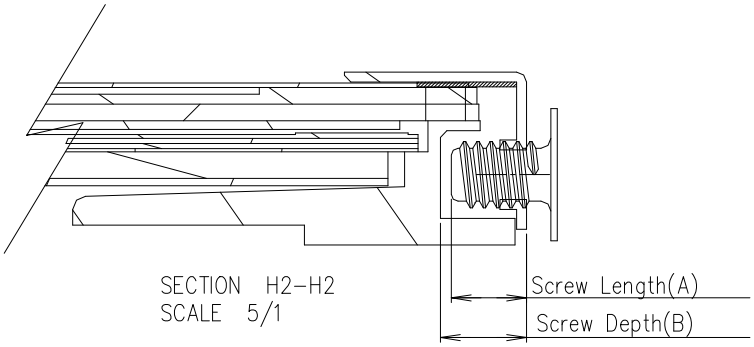
Note) Unit:[mm], General tolerance: ± 0.5mm



<REAR VIEW>


4-R1.00
5.50
7.15
2-R2.00
84.40±1.0
160.7±1.0
Keep Out (80x80mm)
Don't attach here.
314.70
(5.0)
4.80
Ø 2.80
2-R0.7
2-R1.0
3.00

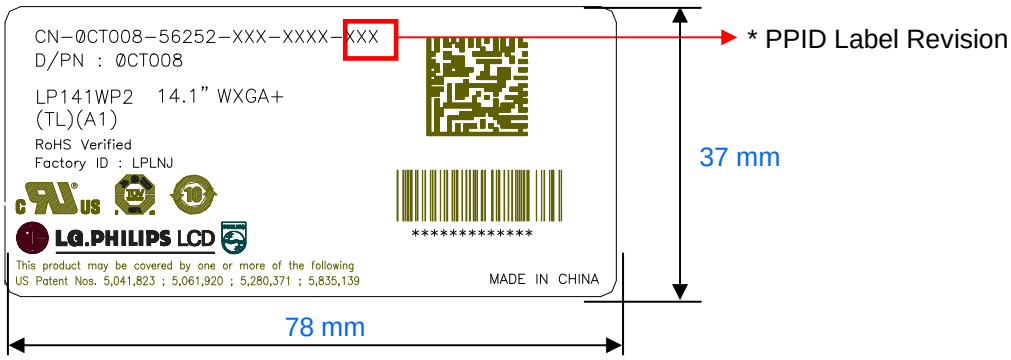
[DETAIL DESCRIPTION OF SIDE MOUNTING SCREW]



* Mounting Screw Length (A)
  = 2.0(Min) / 2.5(Max)
* Mounting Screw Hole Depth (B)
  = 2.5(Min)
* Torque : 2.5 kgf.cm(Max)
  (Measurement gauge : torque meter)

Notes : 1. Screw plated through the method of non-electrolytic nickel plating is preferred to reduce possibility that results in vertical and/or horizontal line defect due to the conductive particles from screw surface.

[DETAIL INFORMATION OF PPID LABEL AND REVISION CODE]

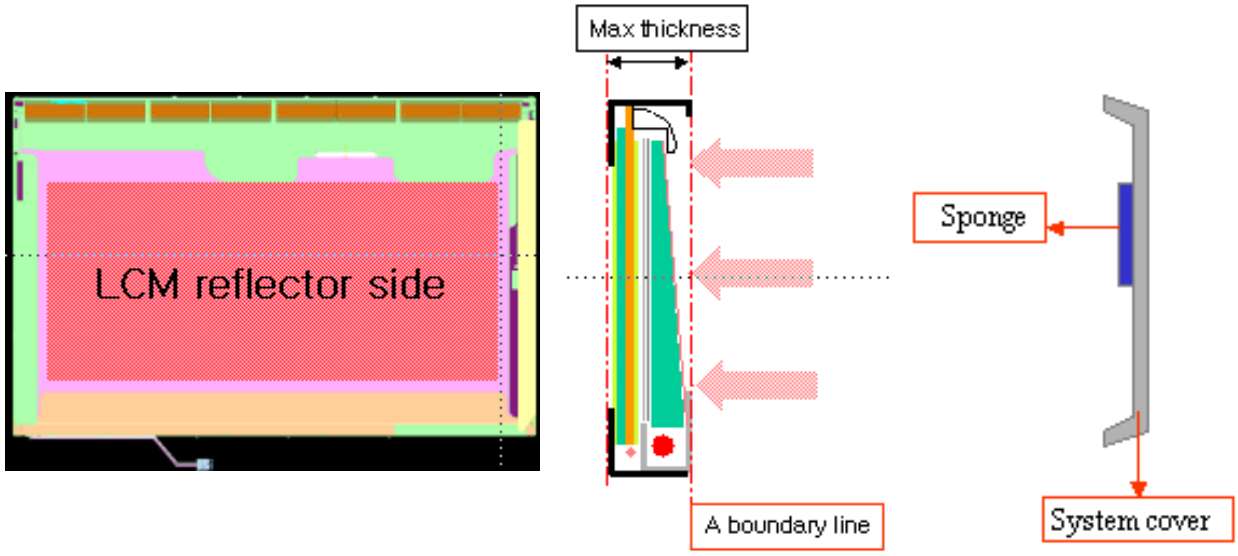


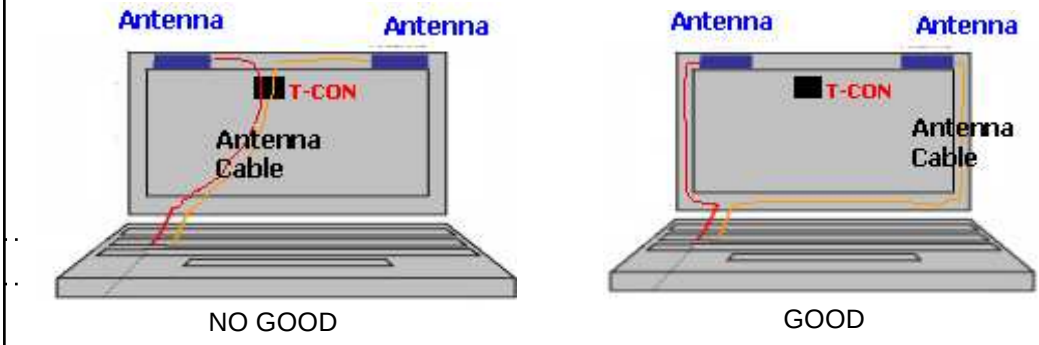
* PPID Label Revision :
  It is subject to change with Dell event. Please refer to the below table for detail.

Classification	No Change	1st Revision	2nd Revision	…	9th Revision	…
SST(WS)	X00	X01	X02	…	A09	…
PT(ES)	X10	X11	X12	…	A19	…
ST(CS)	X20	X21	X22	…	A29	…
XB(MP)	A00	A01	A02	…	A09	…

LPL Proposal for system cover design.(Appendix)

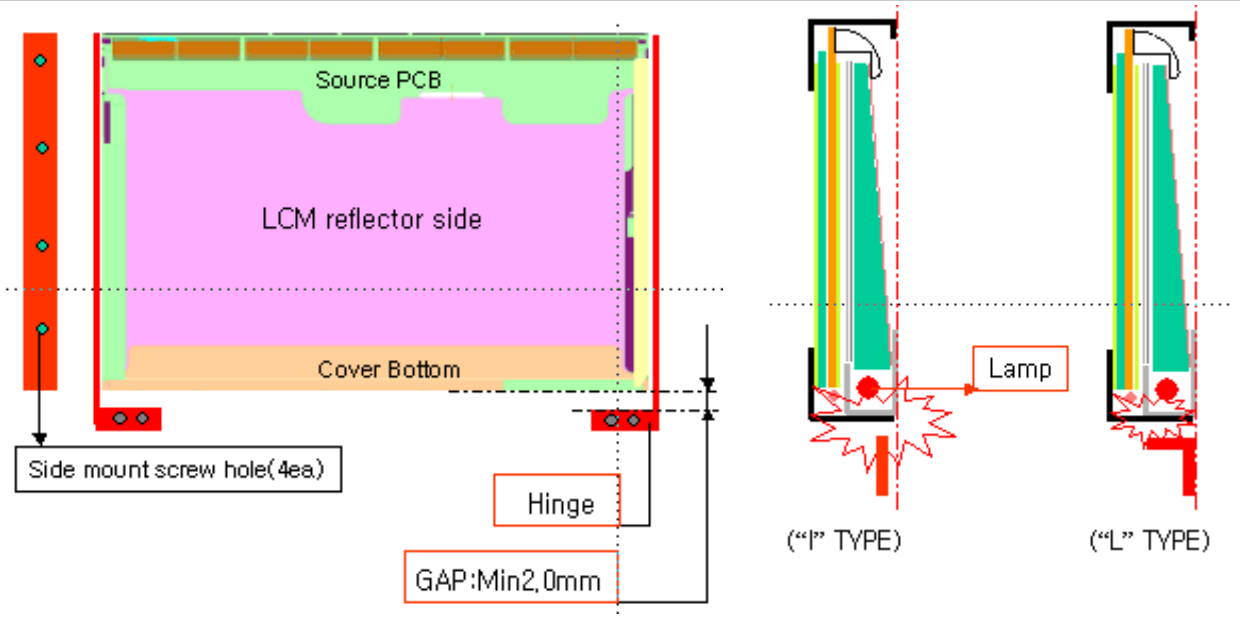
1	Gap check for securing the enough gap between LCM and System cover.	



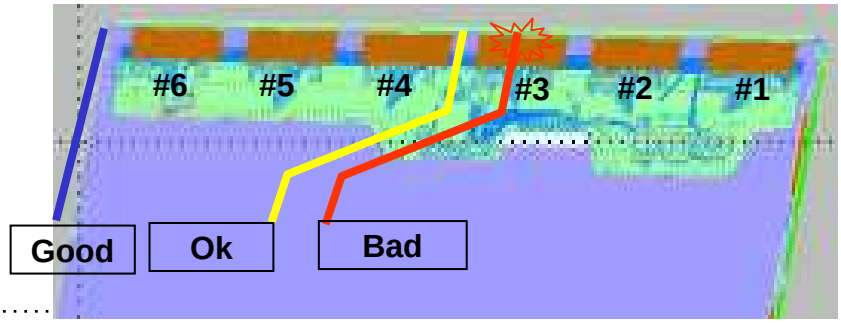
Define	1.Rear side of LCM is sensitive against external stress,and previous check about interference is highly needed. 2.In case there is something from system cover comes into the boundary above,mechanical interference may cause the FOS defects. (Eg:Ripple,White spot..)
2	Check if antenna cable is sufficiently apart from T-CON of LCD Module.
Define	
	1.If system antenna is overlapped with T-CON,it might be cause the noise.

LPL Proposal for system cover design.

3	Gap check for securing the enough gap between LCM and System hinge.	



Define	1.At least 2.0mm of gap needs to be secured to prevent the shock related defects. 2."L" type of hinge is recommended than "I" type under shock test.
4	Checking the path of the System wire.

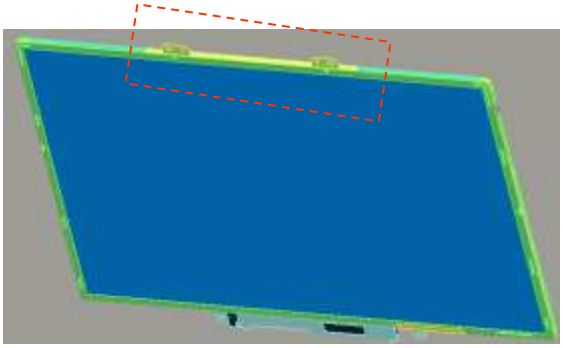


Define	1.COF area needs to be handled with care. 2.GOOD ➔Wire path design to system side. OK➔ Wire path is located between COFs. BAD➔Wire path overlapped with COF area.

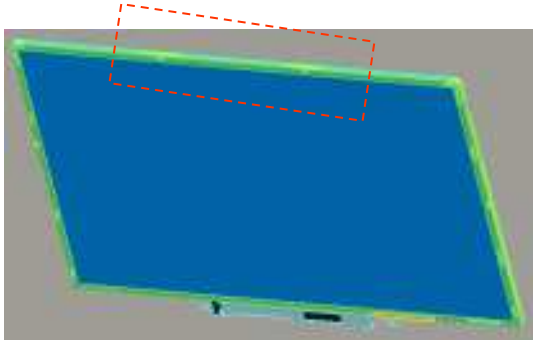
LPL Proposal for system cover design.

5	Using a bracket on the top of LCM is not recommended.	

bracket

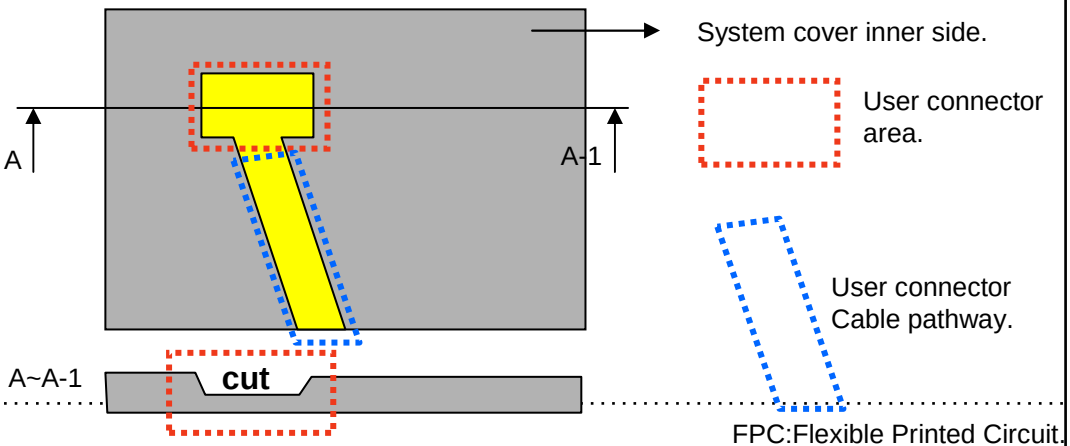


With bracket



Without bracket

Define	1.Condition without bracket is good for mechanical noise,and can minimize the light leakage from deformation of bracket. 2.The results shows that there is no difference between the condition with or without bracket.
6	Securing additional gap on CNT area..



Define	1.CNT area is specially sensitive against external stress,and additional gap by cutting on system cover will be helpful on removing the Ripple. 2.Using a thinner CNT will be better. (eg: FPC type)

6. Reliability

Environment test condition

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Vibration test (non-operating)	Sine wave, 5 ~ 150Hz, 1.5G, 0.37oct/min 3 axis, 30min/axis
6	Shock test (non-operating)	- No functional or cosmetic defects following a shock to all 6 sides delivering at least 180 G in a half sine pulse no longer than 2 ms to the display module - No functional defects following a shock delivering at least 200 g in a half sine pulse no longer than 2 ms to each of 6 sides. Each of the 6 sides will be shock tested with one each display, for a total of 6 displays
7	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr

{ Result Evaluation Criteria }
There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

7. International Standards

7-1. Safety

a) UL 1950 Third Edition, Underwriters Laboratories, Inc. Jan. 28, 1995.
Standard for Safety of Information Technology Equipment Including Electrical Business Equipment.
b) CAN/CSA C22.2 No. 950-95 Third Edition, Canadian Standards Association, Jan. 28, 1995.
Standard for Safety of Information Technology Equipment Including Electrical Business Equipment.
c) EN 60950 : 1992+A1: 1993+A2: 1993+A3: 1995+A1: 1997+A11: 1997
IEC 950 : 1991+A1: 1992+A2: 1993+A3: 1995+A1: 1996
European Committee for Electrotechnical Standardization(CENELEC)
EUROPEAN STANDARD for Safety of Information Technology Equipment Including Electrical Business Equipment.

7-2. EMC

a) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHZ to 40GHz. “American National Standards Institute(ANSI), 1992
b) C.I.S.P.R “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.“ International Special Committee on Radio Interference.
c) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.“ European Committee for Electrotechnical Standardization.(CENELEC), 1998

8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box : 30 pcs

b) Box Size : 490mm X 393mm X 287mm

9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1. MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

9-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=± 200mV(Over and under shoot voltage)

(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
(3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Header	0	**00**	Header	**00**	00000000
	1	**01**	Header	**FF**	11111111
	2	**02**	Header	**FF**	11111111
	3	**03**	Header	**FF**	11111111
	4	**04**	Header	**FF**	11111111
	5	**05**	Header	**FF**	11111111
	6	**06**	Header	**FF**	11111111
	7	**07**	Header	**00**	00000000
Vendor / Product	8	**08**	EISA manufacture code (3 Character ID) LPL	**32**	00110010
	9	**09**	EISA manufacture code (Compressed ASCII)	**0C**	00001100
	10	**0A**	Panel Supplier Reserved - Product Code 0140h	**40**	01000000
	11	**0B**	(Hex. LSB first)	**01**	00000001
	12	**0C**	LCD Module Serial No - Preferred but Optional ("0" If not used)	**00**	00000000
	13	**0D**	LCD Module Serial No - Preferred but Optional ("0" If not used)	**00**	00000000
	14	**0E**	LCD Module Serial No - Preferred but Optional ("0" If not used)	**00**	00000000
	15	**0F**	LCD Module Serial No - Preferred but Optional ("0" If not used)	**00**	00000000
	16	**10**	Week of Manufacture : 00 weeks	**00**	00000000
	17	**11**	Year of Manufacture 2008 year	**12**	00010010
	18	**12**	EDID structure version # = 1	**01**	00000001
	19	**13**	EDID revision # = 3	**03**	00000011
Display	20	**14**	Video input Definition = Digital signal, 6 bit _ Dell only	**90**	10010000
	21	**15**	Max H image size (Rounded cm) = 30 cm	**1E**	00011110
	22	**16**	Max V image size (Rounded cm) = 19 cm	**13**	00010011
	23	**17**	Display gamma = (gamma*100)-100 = Example:(2.2*100)-100=120 = 2.2 Gamma	**78**	01111000
	24	**18**	Feature Support (no_DPMS, no_Active Off/Very Low Power, RGB color display, Timing BLK 1,no_GTF)	**0A**	00001010
Vendor / Product	25	**19**	Red/Green Low Bits (RxRy/GxGy)	**D7**	11010111
	26	**1A**	Blue/White Low Bits (BxBy/WxWy)	**85**	10000101
	27	**1B**	Red X Rx = 0.577	**93**	10010011
	28	**1C**	Red Y Ry =0.349	**59**	01011001
	29	**1D**	Green X Gx = 0.329	**54**	01010100
	30	**1E**	Green Y Gy =0.55	**8C**	10001100
	31	**1F**	Blue X Bx = 0.162	**29**	00101001
	32	**20**	Blue Y By = 0.133	**22**	00100010
	33	**21**	White X Wx =0.313	**50**	01010000
	34	**22**	White Y Wy =0.329	**54**	01010100
Established	35	**23**	Established timing 1 (00h if nt used)	**00**	00000000
	36	**24**	Established timing 2 (00h if nt used)	**00**	00000000
	37	**25**	Manufacturer's timings (00h if nt used)	**00**	00000000
Standard Timing ID	38	**26**	Standard timing ID1 (01h if not used)	**01**	00000001
	39	**27**	Standard timing ID1 (01h if not used)	**01**	00000001
	40	**28**	Standard timing ID2 (01h if not used)	**01**	00000001
	41	**29**	Standard timing ID2 (01h if not used)	**01**	00000001
	42	**2A**	Standard timing ID3 (01h if not used)	**01**	00000001
	43	**2B**	Standard timing ID3 (01h if not used)	**01**	00000001
	44	**2C**	Standard timing ID4 (01h if not used)	**01**	00000001
	45	**2D**	Standard timing ID4 (01h if not used)	**01**	00000001
	46	**2E**	Standard timing ID5 (01h if not used)	**01**	00000001
	47	**2F**	Standard timing ID5 (01h if not used)	**01**	00000001
	48	**30**	Standard timing ID6 (01h if not used)	**01**	00000001
	49	**31**	Standard timing ID6 (01h if not used)	**01**	00000001
	50	**32**	Standard timing ID7 (01h if not used)	**01**	00000001
	51	**33**	Standard timing ID7 (01h if not used)	**01**	00000001
	52	**34**	Standard timing ID8 (01h if not used)	**01**	00000001
	53	**35**	Standard timing ID8 (01h if not used)	**01**	00000001

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Timing Descriptor #1	54	**36**	Pixel Clock/10,000 (LSB) 101.6 MHz @ 60.15Hz	**B0**	10110000
	55	**37**	Pixel Clock/10,000 (MSB)	**27**	00100111
	56	**38**	Horizontal Active (lower 8 bits) 1440 Pixels	**A0**	10100000
	57	**39**	Horizontal Blanking(Thp-HA) (lower 8 bits) 384 Pixels	**80**	10000000
	58	**3A**	Horizontal Active / Horizontal Blanking(Thp-HA) (upper 4:4bits)	**51**	01010001
	59	**3B**	Vertical Avtive 900 Lines	**84**	10000100
	60	**3C**	Vertical Blanking (Tvp-HA) (DE Blanking typ.for DE only panels) 26 Lines	**1A**	00011010
	61	**3D**	Vertical Active : Vertical Blanking (Tvp-HA) (upper 4:4bits)	**30**	00110000
	62	**3E**	Horizontal Sync. Offset (Thfp) 48 Pixels	**30**	00110000
	63	**3F**	Horizontal Sync Pulse Width (HSPW) 32 Pixels	**20**	00100000
	64	**40**	Vertical Sync Offset(Tvfp) : Sync Width (VSPW) 3 Lines : 6 Lines	**36**	00110110
	65	**41**	Horizontal Vertical Sync Offset/Width (upper 2bits)	**00**	00000000
	66	**42**	Horizontal Image Size (mm) 304 mm	**30**	00110000
	67	**43**	Vertical Image Size (mm) 190 mm	**BE**	10111110
	68	**44**	Horizontal Image Size / Vertical Image Size	**10**	00010000
	69	**45**	Horizontal Border = 0 (Zero for Notebook LCD)	**00**	00000000
	70	**46**	Vertical Border = 0 (Zero for Notebook LCD)	**00**	00000000
	71	**47**	Non-Interlace, Normal display, no stereo, Digital Separate (Vsync_NEG, Hsync_POS)	**1A**	00011010
Timing Descriptor #2	72	**48**	Pixel Clock/10,000 (LSB) 67.86 MHz @ 40.18Hz	**82**	10000010
	73	**49**	Pixel Clock/10,000 (MSB)	**1A**	00011010
	74	**4A**	Horizontal Active (lower 8 bits) 1440 Pixels	**A0**	10100000
	75	**4B**	Horizontal Blanking(Thp-HA) (lower 8 bits) 384 Pixels	**80**	10000000
	76	**4C**	Horizontal Active / Horizontal Blanking(Thp-HA) (upper 4:4bits)	**51**	01010001
	77	**4D**	Vertical Avtive 900 Lines	**84**	10000100
	78	**4E**	Vertical Blanking (Tvp-HA) (DE Blanking typ.for DE only panels) 26 Lines	**1A**	00011010
	79	**4F**	Vertical Active : Vertical Blanking (Tvp-HA) (upper 4:4bits)	**30**	00110000
	80	**50**	Horizontal Sync. Offset (Thfp) 48 Pixels	**30**	00110000
	81	**51**	Horizontal Sync Pulse Width (HSPW) 32 Pixels	**20**	00100000
	82	**52**	Vertical Sync Offset(Tvfp) : Sync Width (VSPW) 3 Lines : 6 Lines	**36**	00110110
	83	**53**	Horizontal Vertical Sync Offset/Width (upper 2bits)	**00**	00000000
	84	**54**	Horizontal Image Size (mm) 304 mm	**30**	00110000
	85	**55**	Vertical Image Size (mm) 190 mm	**BE**	10111110
	86	**56**	Horizontal Image Size / Vertical Image Size	**10**	00010000
	87	**57**	Horizontal Border = 0 (Zero for Notebook LCD)	**00**	00000000
	88	**58**	Vertical Border = 0 (Zero for Notebook LCD)	**00**	00000000
	89	**59**	Non-Interlace, Normal display, no stereo, Digital Separate (Vsync_NEG, Hsync_POS)	**1A**	00011010
Timing Descriptor #3	90	**5A**	Flag	**00**	00000000
	91	**5B**	Flag	**00**	00000000
	92	**5C**	Flag	**00**	00000000
	93	**5D**	Data Type Tag : Alphanumeric Data String (ASCII String)	**FE**	11111110
	94	**5E**	Flag	**00**	00000000
	95	**5F**	Dell P/N 1st Character = C	**43**	01000011
	96	**60**	Dell P/N 2nd Character = T	**54**	01010100
	97	**61**	Dell P/N 3rd Character = 0	**30**	00110000
	98	**62**	Dell P/N 4th Character = 0	**30**	00110000
	99	**63**	Dell P/N 5th Character = 8	**38**	00111000
	100	**64**	EDID Revision Build Name = ST (CS) , Revision # = X20	**14**	00010100
	101	**65**	Manufacturer P/N = 1	**31**	00110001
	102	**66**	Manufacturer P/N = 4	**34**	00110100
	103	**67**	Manufacturer P/N = 1	**31**	00110001
	104	**68**	Manufacturer P/N = W	**57**	01010111
	105	**69**	Manufacturer P/N = P	**50**	01010000
	106	**6A**	Manufacturer P/N = 2	**32**	00110010
	107	**6B**	Manufacturer P/N(If<13 char--> 0Ah, then terminate with ASCⅡ code 0Ah,set remaining char = 20h)	**0A**	00001010

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Timing Descriptor #4	108	**6C**	Flag	**00**	00000000
	109	**6D**	Flag	**00**	00000000
	110	**6E**	Flag	**00**	00000000
	111	**6F**	Data Type Tag : Descriptor Defined by manufacturer	**00**	00000000
	112	**70**	Flag	**00**	00000000
	113	**71**	SMBUS Value(Step #1) = 0 nits	**00**	00000000
	114	**72**	SMBUS Value(Step #2) = 0 nits	**00**	00000000
	115	**73**	SMBUS Value(Step #3) = 0 nits	**00**	00000000
	116	**74**	SMBUS Value(Step #4) = 0 nits	**00**	00000000
	117	**75**	SMBUS Value(Step #5) = 0 nits	**00**	00000000
	118	**76**	SMBUS Value(Step #6) = 0 nits	**00**	00000000
	119	**77**	SMBUS Value(Step #7) = 0 nits	**00**	00000000
	120	**78**	SMBUS Value(Step #8) = 0 nits (Typically = FFh, Max nits)	**00**	00000000
	121	**79**	Dual channel LVDS, No RTC support	**02**	00000010
	122	**7A**	BIST support	**01**	00000001
	123	**7B**	(If<13 char--> 0Ah, then terminate with ASCⅡ code 0Ah,set remaining char = 20h)	**0A**	00001010
	124	**7C**	(If<13 char--> 0Ah, then terminate with ASCⅡ code 0Ah,set remaining char = 20h)	**20**	00100000
	125	**7D**	(If<13 char--> 0Ah, then terminate with ASCⅡ code 0Ah,set remaining char = 20h)	**20**	00100000
Checksum	126	**7E**	Extension flag (# of optional 128 panel ID extension block to follow, Typ = 0)	**00**	00000000
	127	**7F**	Check Sum (The 1-byte sum of all 128 bytes in this panel ID block shall = 0)	**D3**	11010011