(V) Preliminary Specifications
( ) Final Specifications

Module	**14.0”(13.97”) HD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	B140XTN03.3 (H/W:0A)
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
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Note: This Specification is subject to change without notice.		**NBBU Marketing Division AU Optronics corporation**	

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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2012/07/27	All	First Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B140XTN03.3 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B140XTN03.3 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	354.95			
Active Area	[mm]	309.399x173.952			
Pixels H x V		1366x3(RGB) x 768			
Pixel Pitch	[mm]	0.2265 x 0.2265			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance	[cd/m^2]	200 typ. (5 points average) 170 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		400 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.3 max. (Include Logic and Blu power)			
Weight	[Grams]	320 max.			
Physical Size **Include bracket**	[mm]		Min.	Typ.	Max.
		Length	319.9	320.4	320.9
		Width	204.6	205.1	205.6
		Thickness	-	-	3.6
Electrical Interface		1 Lane eDP			
Glass Thickness	[mm]	0.5			
Surface Treatment		AG, Hardness 3H,			
Support Color		262K colors (RGB 6-bit)			

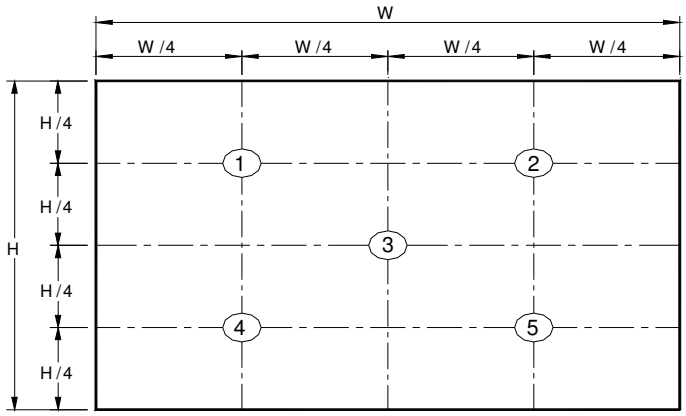
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

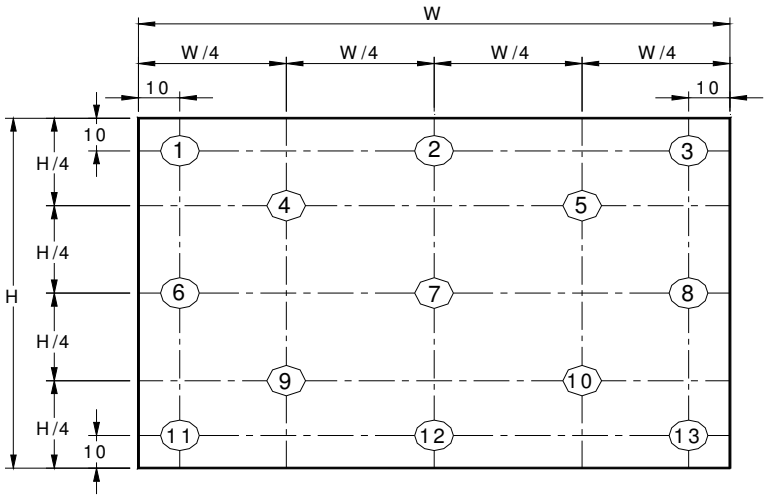
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=22mA			5 points average	170	200	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	40 40	45 45	- -	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	10 30	15 35	- -		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio		CR		300	400	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_{RT}	Rising + Falling	-	8	16	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.558	0.588	0.618	-	4
		Ry		0.315	0.345	0.375		
	Green	Gx		0.297	0.327	0.357		
		Gy		0.512	0.542	0.572		
	Blue	Bx		0.121	0.151	0.181		
		By		0.113	0.143	0.173		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		42	45	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

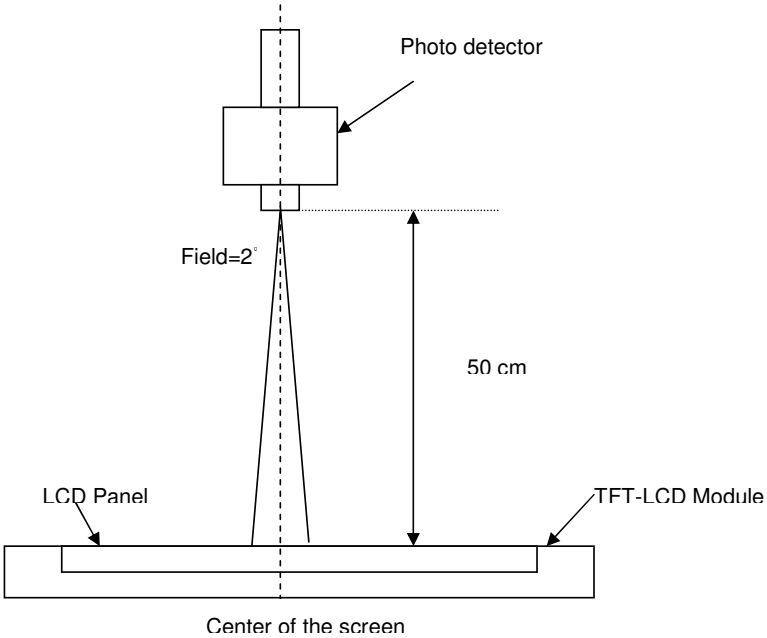
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points, Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

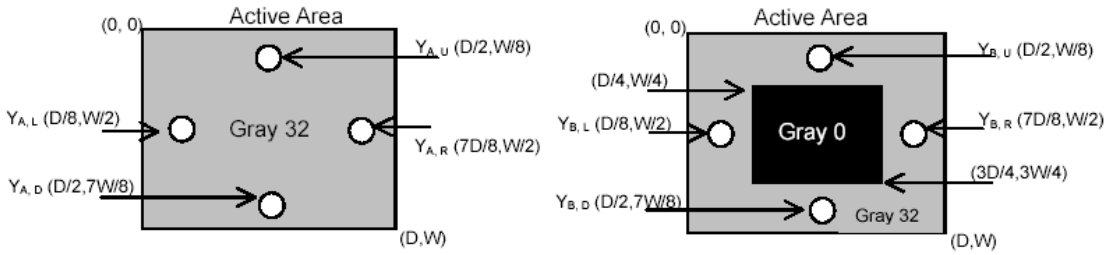
Note 7 : Definition of Cross Talk (CT)

$CT = |Y_B - Y_A| / Y_A \times 100\ (\%)$

Where

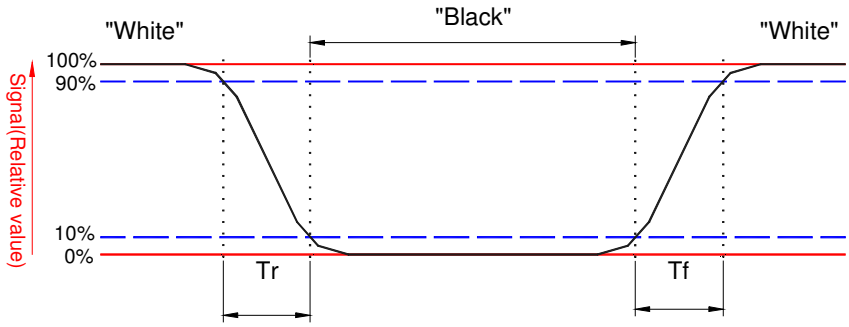
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



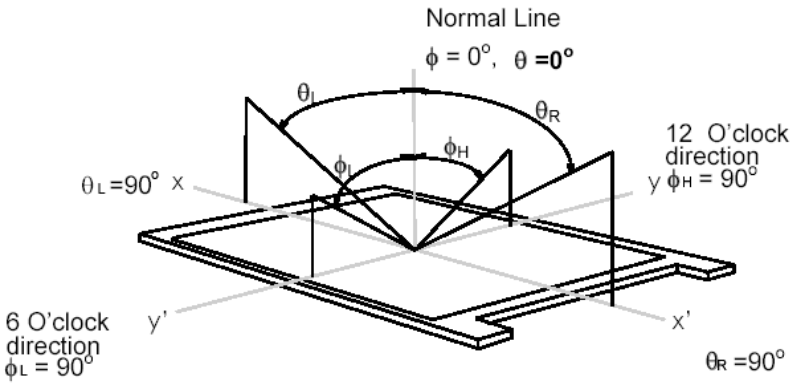
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



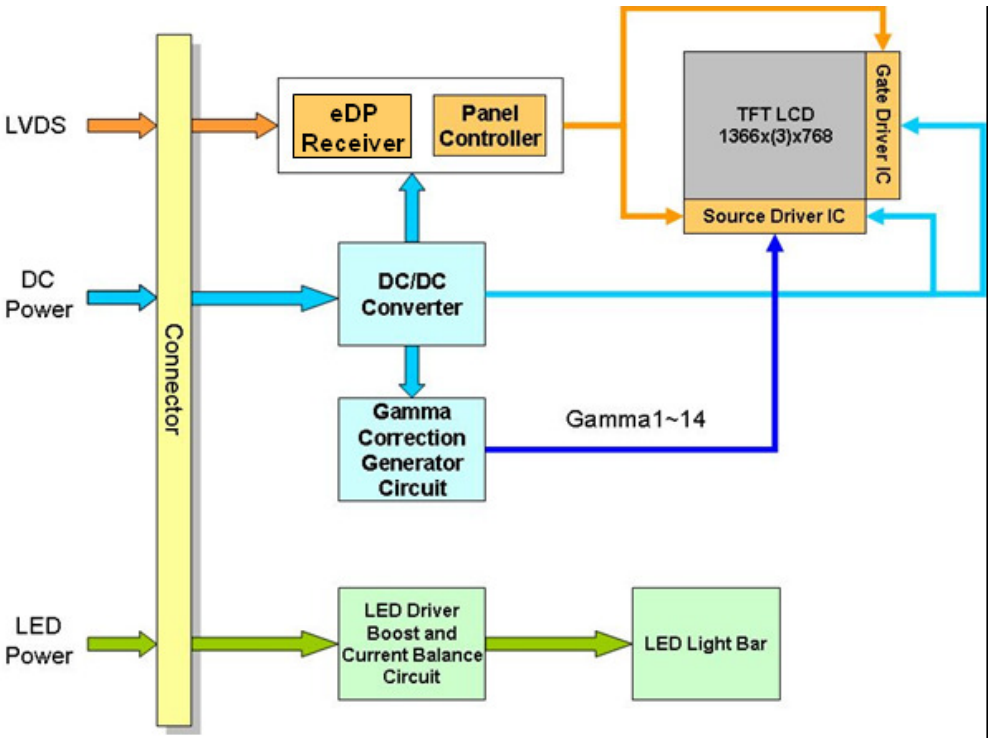
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 30 Pin



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

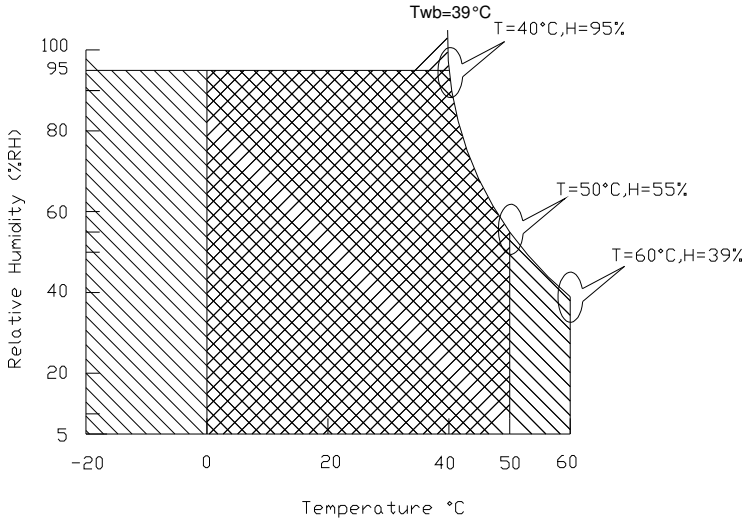
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

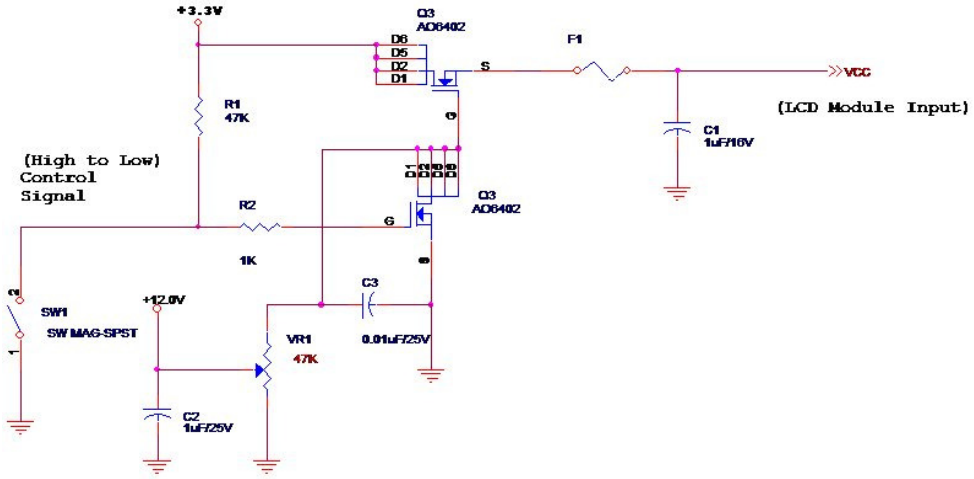
The power specification are measured under 25℃ and frame frenquency under 60Hz

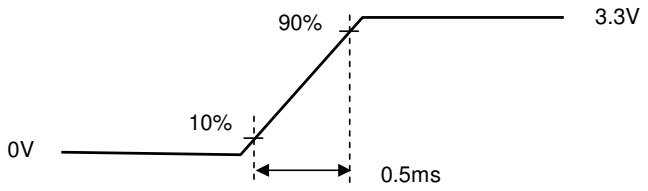
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.9	[Watt]	Note 1
IDD	IDD Current	-	-	250	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Typical Measurement Condition : Mosaic Pattern

Note 2：Measure Condition





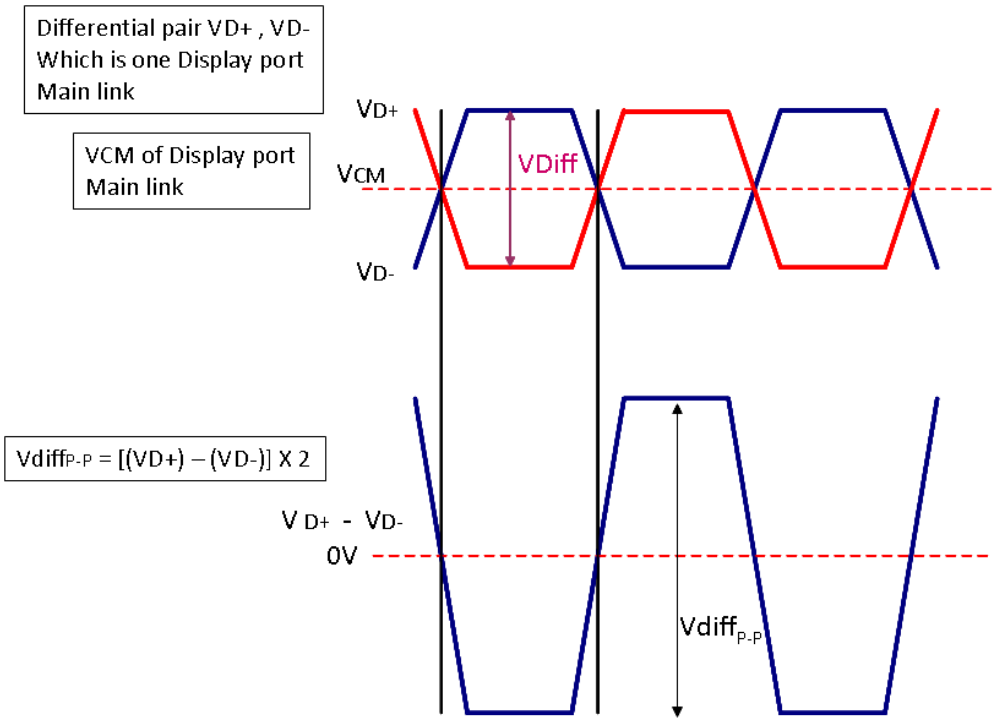
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

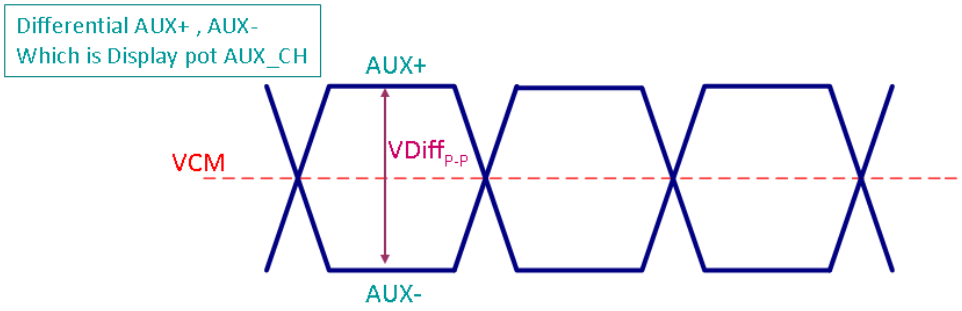
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		mV
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Fallow as VESA display port standard V1.1a

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		mV
VDiff$_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	400	600	800	mV

Fallow as VESA display port standard V1.1a.

Display Port V_{HPD} signal:

Display port V_{HPD}					
		Min	Typ	Max	unit
V_{HPD}	HPD Voltage	0	2.5	2.5	V

Fallow as VESA display port standard V1.1a.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.4	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	12,000	-	-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

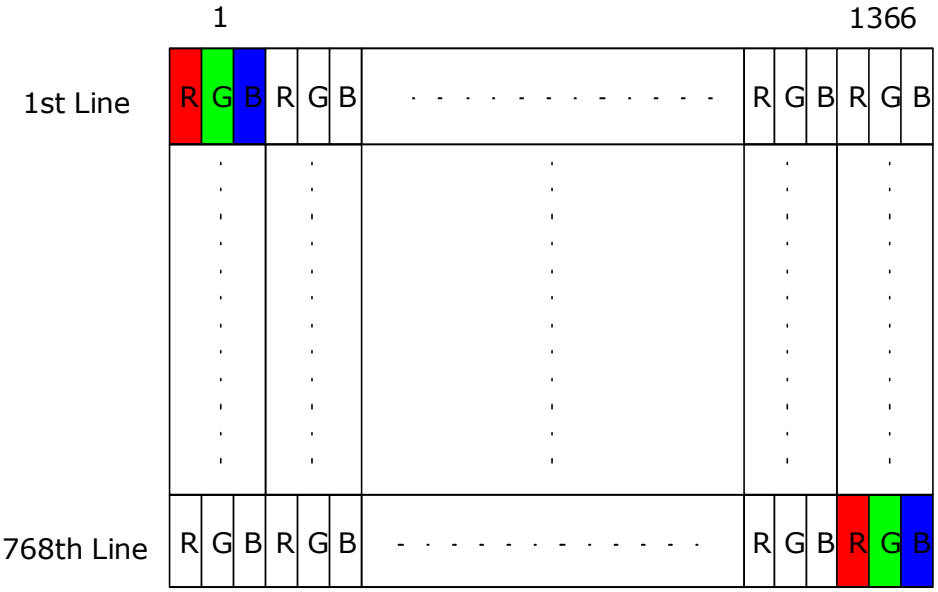
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.0	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	100	600	1K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

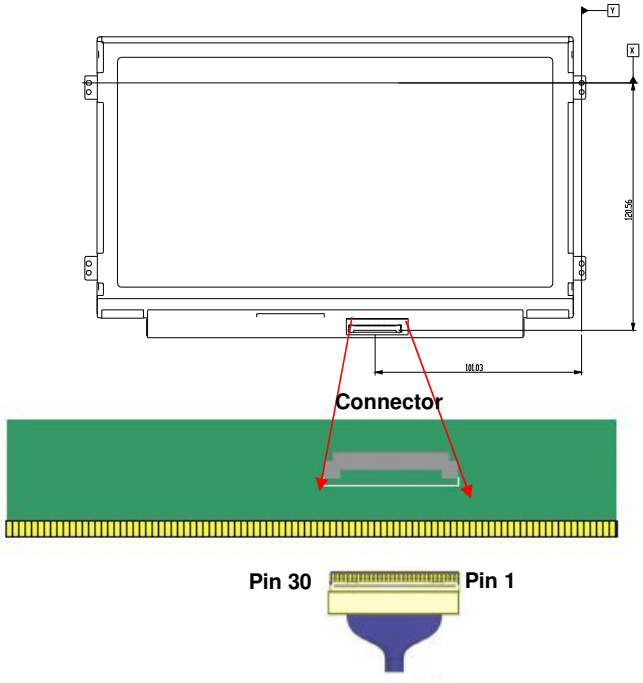
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX
Type / Part Number	IPEX 20455-030E-12
Mating Housing/Part Number	IPEX 20453-030T-1

6.2.2 Pin Assignment (1 Lane)

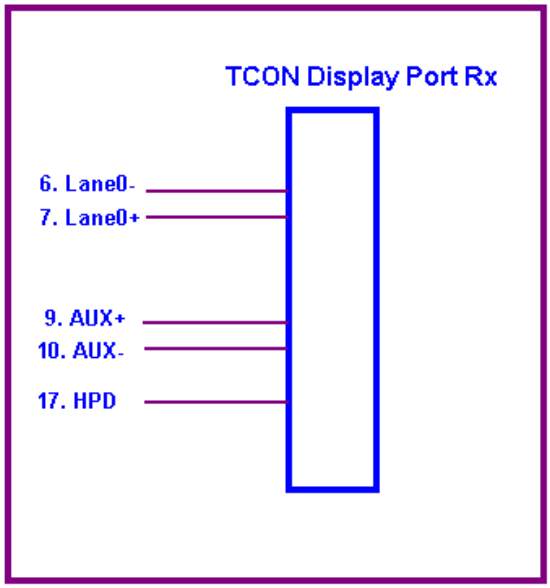
eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	DCR_EN	DCR_EN
2	H_GND	High Speed Ground
3	Lane1_N	NC
4	Lane1_P	NC
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	BIST	LCD Panel Self Test Enable
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	HPD	HPD signale pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL PWM DIM	System PWM signal Input
24	NC	Reverse for AUO TEST only
25	NC	Reverse for AUO TEST only
26	BL_PWR	Backlight power (6V~21V)
27	BL_PWR	Backlight power (6V~21V)
28	BL_PWR	Backlight power (6V~21V)
29	BL_PWR	Backlight power (6V~21V)
30	CM-EN	NC



Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



6.3 Interface Timing

6.3.1 Timing Characteristics

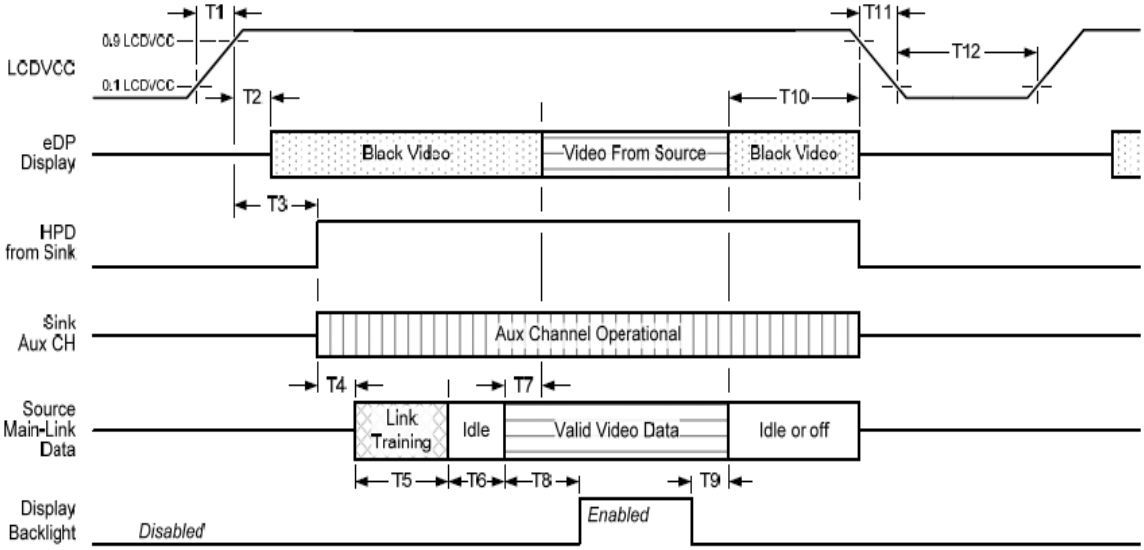
Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		$1/T_{Clock}$	66.9	76.6	80	MHz
Vertical Section	Period	T_V	788	798	768+A	T_{Line}
	Active	T_{VD}	768			
	Blanking	T_{VB}	20	30	A	
Horizontal Section	Period	T_H	1416	1598	1366+B	T_{Clock}
	Active	T_{HD}	1366			
	Blanking	T_{HB}	50	232	B	

Note 1 : The above is as optimized setting
Note 2 : The maximum clock frequency = (1366+B)*(768+A)*60<80MHz

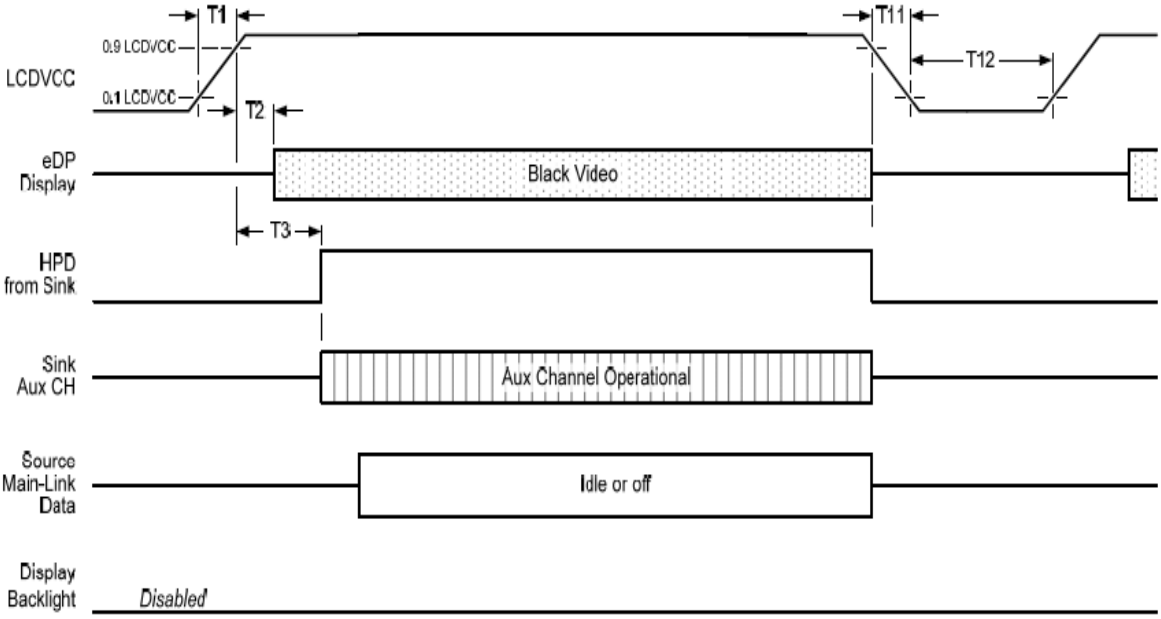
6.4 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

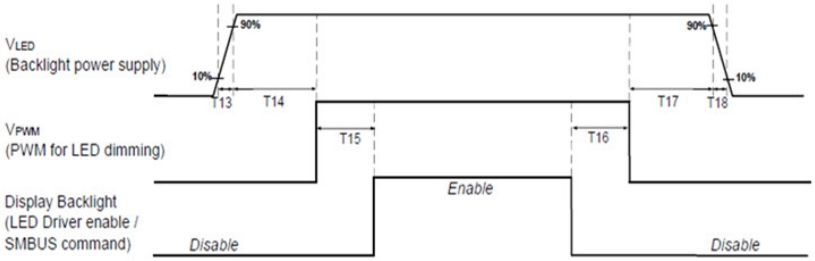
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

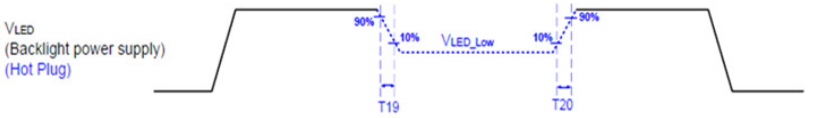
Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	**Ta= 40℃, 90%RH, 300h**	
High Temperature Operation	**Ta= 50℃, Dry, 300h**	
Low Temperature Operation	**Ta= 0℃, 300h**	
High Temperature Storage	**Ta= 60℃, 35%RH, 300h**	
Low Temperature Storage	**Ta= -20℃, 50%RH, 250h**	
Thermal Shock Test	**Ta=-20℃to 60℃, Duration at 30 min, 100 cycles**	
ESD	**Contact : ±8 KV** **Air : ±15 KV**	Note 1

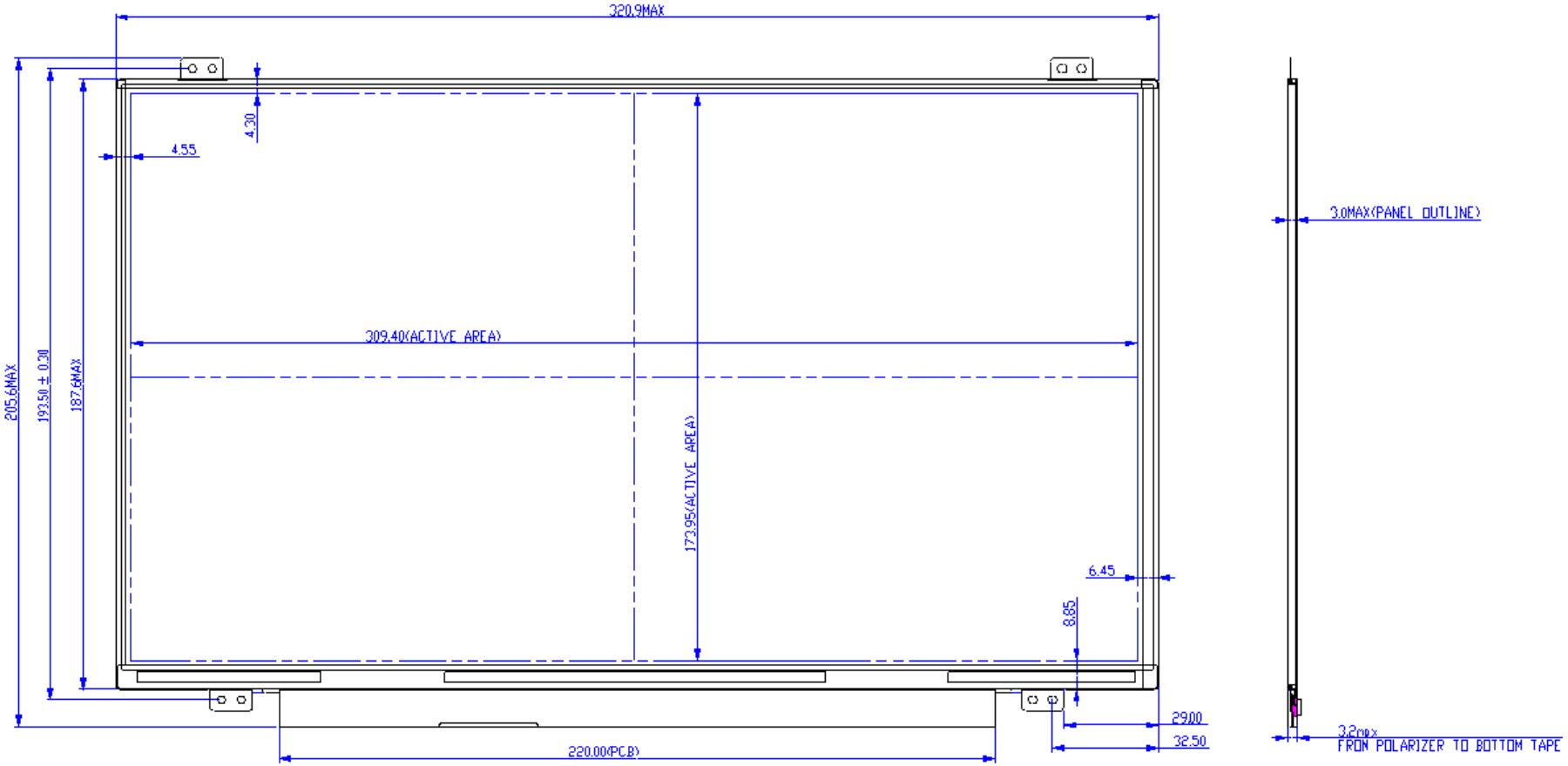
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

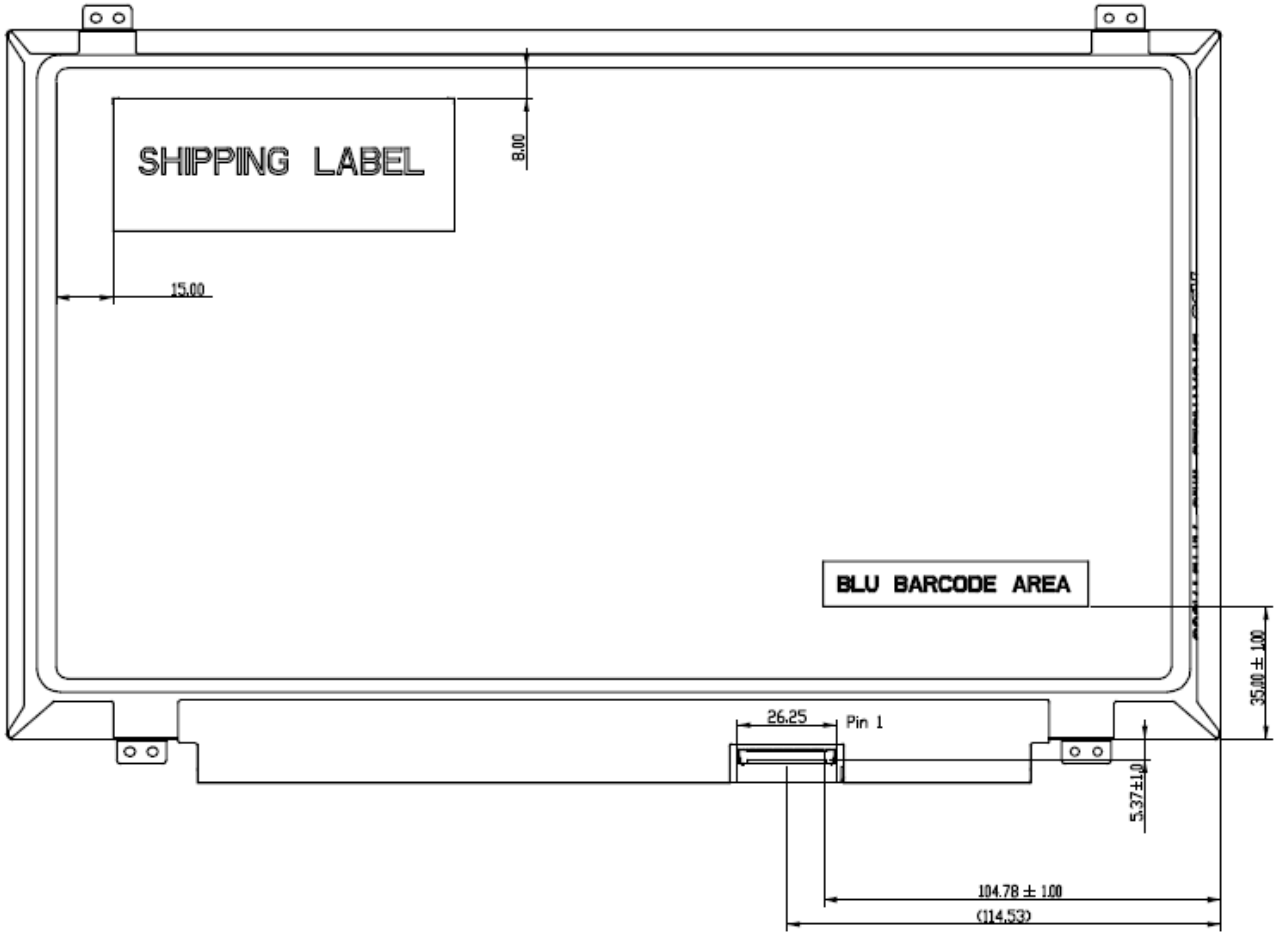
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension

註解 [L1]:
1.Get RD drawing and paste as PDF format only.
2.Should Follow VESA format

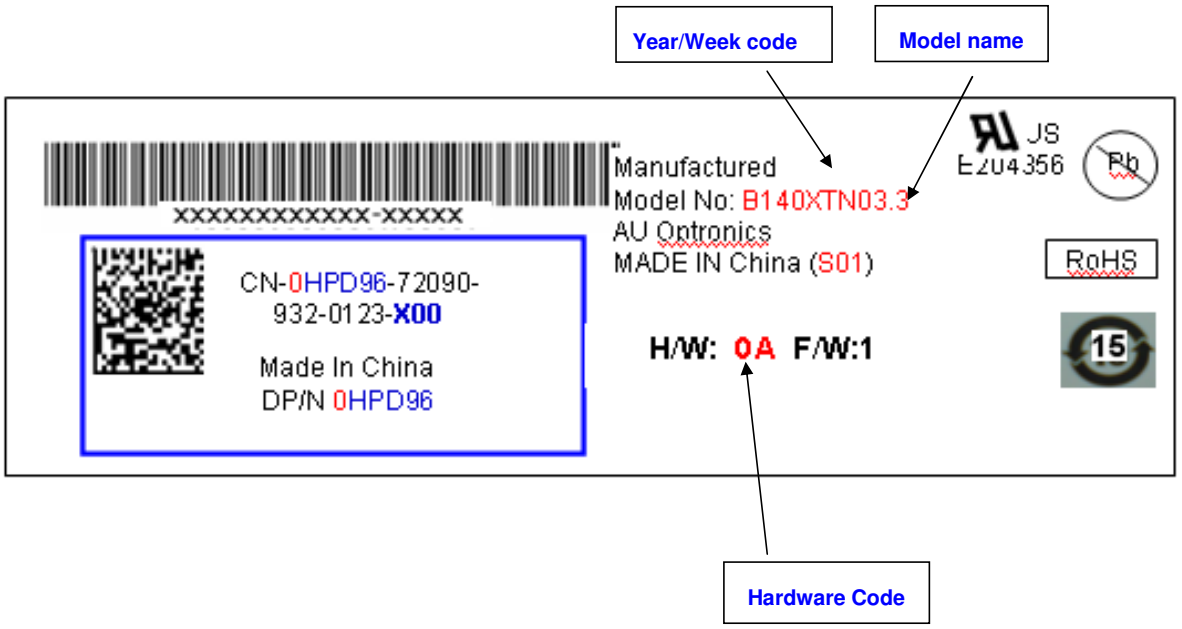




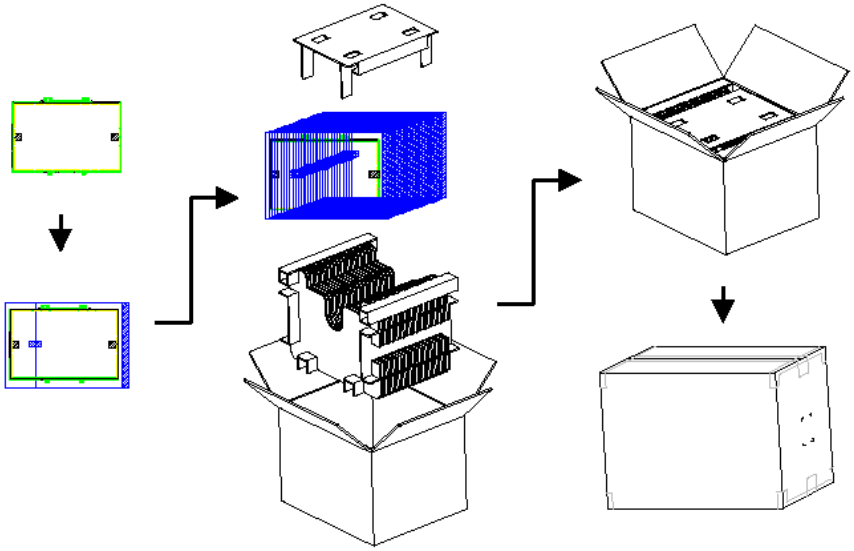
Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

9. Shipping and Package

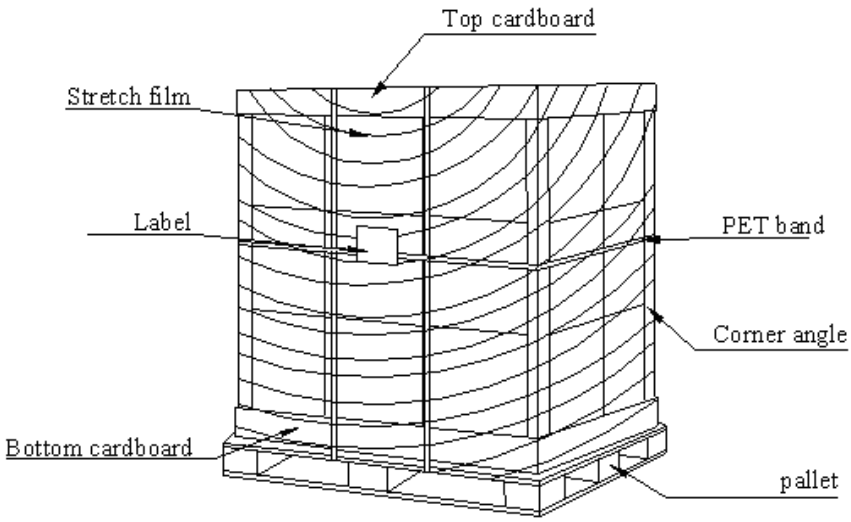
9.1 Shipping Label Format



9.2 Carton Package



9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

Address HEX	FUNCTION	Value (hex)	Value (binary)	Value (DEC)	Note
00	Header	00	00000000	0	
01	Header	FF	11111111	255	
02	Header	FF	11111111	255	
03	Header	FF	11111111	255	
04	Header	FF	11111111	255	
05	Header	FF	11111111	255	
06	Header	FF	11111111	255	
07	Header	00	00000000	0	
08	EISA manufacture code = 3 Character ID	06	00000110	6	
09	EISA manufacture code (Compressed ASCII)	AF	10101111	175	
0A	Panel Supplier Reserved – Product Code	3C	00111100	60	
0B	Panel Supplier Reserved – Product Code	33	00110011	51	
0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0	
0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0	
0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0	
0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	16	00010110	22	
12	EDID structure version # = 1	01	00000001	1	
13	EDID revision # = 4	04	00000100	4	
14	Video I/P definition	95	10010101	149	
15	Max H image size = ?? cm (Rounded to cm)	1F	00011111	31	
16	Max V image size = ?? cm (Rounded to cm)	11	00010001	17	
17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78	01111000	120	
18	Feature support	02	00000010	2	
19	Red/Green Low bit (RxRy/GxGy)	AF	10101111	175	
1A	Blue/White Low bit (BxBy/WxWy)	E5	11100101	229	
1B	Red X Rx = 0.???	96	10010110	150	
1C	Red Y Ry = 0.???	58	01011000	88	
1D	Green X Rx = 0.???	53	01010011	83	
1E	Green Y Ry = 0.???	8A	10001010	138	

1F	Blue X Rx = 0.???	26	00100110	38	
20	Blue Y Ry = 0.???	24	00100100	36	
21	White X Rx = 0.???	50	01010000	80	
22	White Y Ry = 0.???	54	01010100	84	
23	Established timings 1 (00h if not used)	00	00000000	0	
24	Established timings 2 (00h if not used)	00	00000000	0	
25	Manufacturer's timings (00h if not used)	00	00000000	0	
26	Standard timing ID1 (01h if not used)	01	00000001	1	
27	Standard timing ID1 (01h if not used)	01	00000001	1	
28	Standard timing ID2 (01h if not used)	01	00000001	1	
29	Standard timing ID2 (01h if not used)	01	00000001	1	
2A	Standard timing ID3 (01h if not used)	01	00000001	1	
2B	Standard timing ID3 (01h if not used)	01	00000001	1	
2C	Standard timing ID4 (01h if not used)	01	00000001	1	
2D	Standard timing ID4 (01h if not used)	01	00000001	1	
2E	Standard timing ID5 (01h if not used)	01	00000001	1	
2F	Standard timing ID5 (01h if not used)	01	00000001	1	
30	Standard timing ID6 (01h if not used)	01	00000001	1	
31	Standard timing ID6 (01h if not used)	01	00000001	1	
32	Standard timing ID7 (01h if not used)	01	00000001	1	
33	Standard timing ID7 (01h if not used)	01	00000001	1	
34	Standard timing ID8 (01h if not used)	01	00000001	1	
35	Standard timing ID8 (01h if not used)	01	00000001	1	
36	Pixel Clock/10,000 (LSB)	EC	11101100	236	
37	Pixel Clock/10,000 (MSB)	1D	00011101	29	
38	Horizontal Active = ???? pixels (lower 8 bits)	56	01010110	86	
39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	E8	11101000	232	
3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000	80	
3B	Vertical Active = ??? lines	00	00000000	0	
3C	Vertical Blanking (Tvbp) = ?? lines (DE Blanking typ. for DE only panels)	1E	00011110	30	
3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48	
3E	Horizontal Sync, Offset (Thfp) = ?? pixels	26	00100110	38	

3F	Horizontal Sync, Pulse Width = ??? pixels	16	00010110	22	
40	Vertical Sync, Offset (Tvfp) = ? lines Sync Width = ? lines	36	00110110	54	
41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0	
42	Horizontal Image Size = ??? mm	35	00110101	53	
43	Vertical image Size = ??? mm	AD	10101101	173	
44	Horizontal Image Size / Vertical image size	10	00010000	16	
45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0	
46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0	
47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The int	1A	00011010	26	
48	Pixel Clock/10,000 (LSB)	F3	11110011	243	
49	Pixel Clock/10,000 (MSB)	13	00010011	19	
4A	Horizontal Active = xxxx pixels (lower 8 bits)	56	01010110	86	
4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	E8	11101000	232	
4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000	80	
4D	Vertical Active = xxxx lines	00	00000000	0	
4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	1E	00011110	30	
4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48	
50	Horizontal Sync, Offset (Thfp) = xxxx pixels	26	00100110	38	
51	Horizontal Sync, Pulse Width = xxxx pixels	16	00010110	22	
52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	36	00110110	54	
53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0	
54	Horizontal Image Size =xxx mm	35	00110101	53	
55	Vertical image Size = xxx mm	AD	10101101	173	
56	Horizontal Image Size / Vertical image size	10	00010000	16	
57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0	

58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0	
59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The int	1A	00011010	26	
5A	Flag	00	00000000	0	
5B	Flag	00	00000000	0	
5C	Flag	00	00000000	0	
5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254	
5E	Flag	00	00000000	0	
5F	Dell P/N 1st Character	48	01001000	72	
60	Dell P/N 2nd Character	50	01010000	80	
61	Dell P/N 3rd Character	44	01000100	68	
62	Dell P/N 4th Character	39	00111001	57	
63	Dell P/N 5th Character	36	00110110	54	
64	**EDID Revision** **Bit[6:0] See charts below** **Bit[7] 0: X-rev, 1: A-rev**	00	00000000	0	
65	Manufacturer P/N	42	01000010	66	
66	Manufacturer P/N	31	00110001	49	
67	Manufacturer P/N	34	00110100	52	
68	Manufacturer P/N	30	00110000	48	
69	Manufacturer P/N	58	01011000	88	
6A	Manufacturer P/N	54	01010100	84	
6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	4E	01001110	78	
6C	Flag	00	00000000	0	
6D	Flag	00	00000000	0	
6E	Flag	00	00000000	0	
6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00	00000000	0	
70	Flag	00	00000000	0	
71	Color Management	01	00000001	1	
72	Panel Structure	41	01000001	65	
73	Frame Rate	21	00100001	33	
74	Light Controller Interface and Luminance	94	10010100	148	

75	Outdoor Features	00	00000000	0	
76	Multi-Media Features	11	00010001	17	
77	Multi-Media Features	00	00000000	0	
78	Special Features #1	00	00000000	0	
79	Special Features #2	09	00001001	9	
7A	Special Features #3	01	00000001	1	
7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10	
7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32	
7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32	
7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0	
7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	F2	11110010	242	