■ Preliminary Specification

Module	24" WUXGA Color TFT-LCD
Model Name	G240UAN01.0

Customer	Date
Approved by	
Note: This content of s to change	pecification is subject

Checked & Approved by	Date			
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Product Specification

G240UAN01.0

AU OPTRONICS CORPORATION

Record of Revision

Version & Date	Page	Old Description	New Description
V0		First Edition for Customer	
V1	p.5,13,14	power consumption	power consumption
VI	p.17	Pin#1 signal name:RxOIN0-	Pin#1 signal name:VSS

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1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of LED light bar edge. Instead, press at the far ends of LED light bar edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Avoid stressing front bezel position when doing mechanical design.

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2. General Description

G240UAN01.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT-LCD panel, a driver circuit, and a backlight system. The screen format is intended to support the WUXGA (1920(H) x 1200(V)) screen and 1.07B colors. All input signals are 2-channel LVDS interface compatible.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 $^{\circ}\text{C}$ condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	611.32 (24.07")
Active Area	[mm]	518.4 (H) x 324.0 (V)
Pixels H x V		1920(x3) x 1200
Pixel Pitch	[mm]	0.270 (per one triad) x 0.270
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		AHVA mode, Normally Black
White Luminance	[cd/m ²]	900 (center, Typ) @ 60mA
Contrast Ratio		1000 : 1 (Typ)
Optical ResponseTime	[msec]	14 (Typ., on/off)
Power Supply Input Voltage (VDD)	[Volt]	+12 V
Power Consumption	[Watt]	TBC (sim: LED 40.33(W) + LCD 4.8(W) (typ))
Weight	[Grams]	2500 (Typ)
Physical Size (H x V x D)	[mm]	546.4 (H) x 352.0 (V) x 18.1 (D) (Typ)
Electrical Interface		Dual channel LVDS
Surface Treatment		Anti-Glare treatment
Support Color		1.07B colors
Temperature Range Operating Storage (Non-Operating)	[°C]	0 to +40 -20 to +50
RoHS Compliance		RoHS Compliance

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2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature):

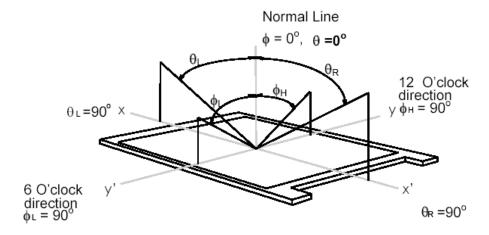
Item	Unit	Condi	Min.	Тур.	Max.	Note	
Viewing Angle	[dograp]	Horizontal CR = 10	(Right) (Left)	75 75	89 89	ı	1
	[degree]	Vertical CR = 10	(Up) (Down)	70 70	89 89	-	1
Luminance Uniformity	[%]	9 Points		80	85	-	2, 3
Optical Response Time	[msec]	Rising + Fall	ing	-	14	25	4, 6
		Red x			(0.654)		
		Red y			(0.335)		
		Green x			(0.313)		
Color / Chromaticity		Green y			(0.643)		4
Coordinates (CIE)		Blue x			(0.156)		4
		Blue y			(0.057)		
		White x		0.283	0.313	0.343	
		White y		0.299	0.329	0.359	
White Luminance (At LED= 60mA)	[cd/m ²]			720	900	-	4
Contrast Ratio				700	1000	-	4

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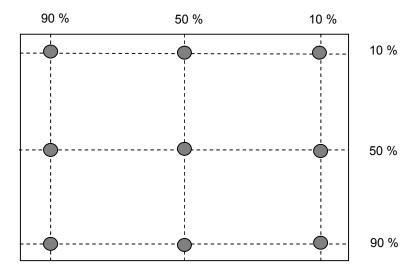


Note 1: Definition of viewing angle, measured by ELDIM (EZContrast 88)

Viewing angle is the measurement of contrast ratio \geq 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



Note 2: 9 points position



Note 3: The luminance uniformity of 9 points is defined by dividing the maximum luminance values by the minimum test point luminance. And measured by TOPCON SR-3

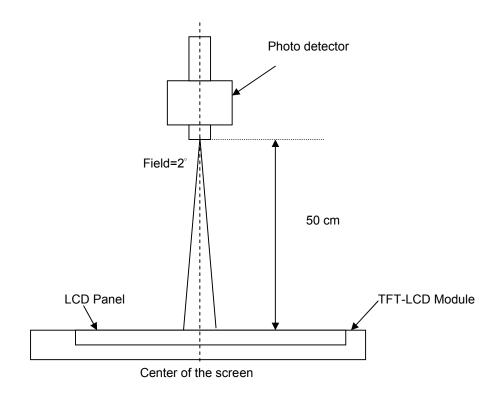
$$\delta_{\text{W9}} = \frac{\text{Minimum Luminance of 9 points}}{\text{Maximum Luminance of 9 points}}$$

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Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.

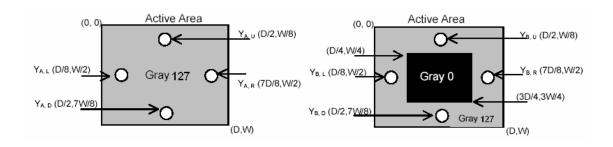


Note 5: Definition of Cross Talk (CT) and measured by TOPCON SR-3 CT = | YB - YA | / YA \times 100 (%)

Where

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

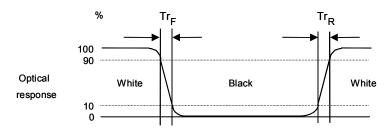
YB = Luminance of measured location with gray level 0 pattern (cd/m2)



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Note 6: Definition of response time, measured by WESTAR TRD-100A

The output signals of photo detector are measured when the input signals are changed from "Full Black" to "Full White" (rising time), and from "Full White" to "Full Black" (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.

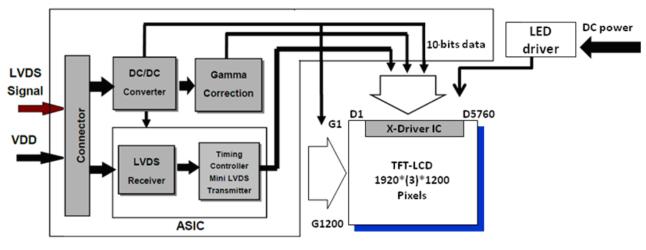


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3. Functional Block Diagram

The following diagram shows the functional block of the 24 inches Color TFT-LCD Module:



Control Board

I/F PCB Interface:

FI-RE51S-HF-R1500

Mating Type:

FI-RE51HL

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4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min.	Max.	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+16.5	[Volt]	Note 1, 2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min.	Max.	Unit	Conditions
LED Power Current	lled	-	1.7	[A] rms	Note 1, 2

4.3 Absolute Ratings of Environment

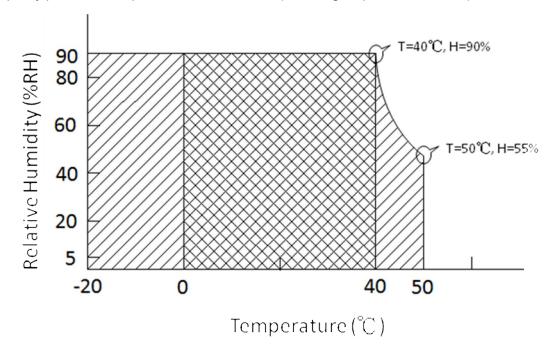
Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+40	[°C]	
Operation Humidity	HOP	5	90	[%RH]	Note 3
Storage Temperature	TST	-20	+50	[°C]	Note 5
Storage Humidity	HST	5	90	[%RH]	

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Note 1: With in Ta= 25°C

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



operating range: ⋈XX storage range: ∠✓✓ + ⋈XX

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5. Electrical characteristics

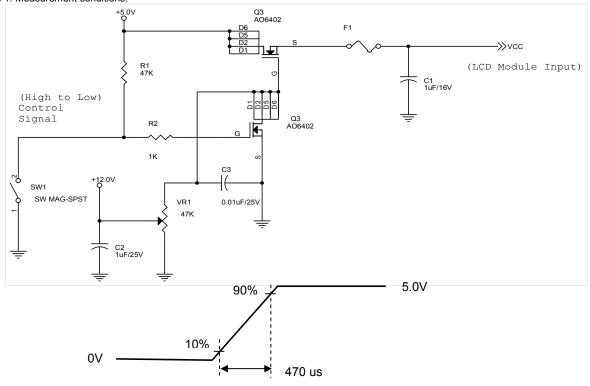
5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows:

Symble	Parameter	Min.	Тур.	Max.	Unit	Condition
VCC	Logic/LCD Drive Voltage	10.8	12.0	13.2	[Volt]	±10%
ICC	Input Current	ı	0.4	0.6	[A]	Vin=12V, White Pattern, at 60Hz
IRush	Inrush Current	1	2.7	3.4	[A]	Note 1
PCC	VCC Power	-	4.8	7.2	[Watt]	Vin=12V, White Pattern, at 60Hz
VCCrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	300	[mV] p-p	With panel loading





VDD rising time

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5.2 Backlight Unit

Following characteristics are measured under a stable condition at 25 °C (Room Temperature):

Symbol	Parameter	Min.	Тур.	Max.	Unit	Remark
VDD	Input Voltage	23.5	24.0	24.5	[Volt]	
I _{VDD}	Input Current		1.68	2.02	[A]	100% PWM Duty
P_{VDD}	Power Consumption		40.33	41.16	[Watt]	100% PWM Duty
Irush LED	Inrush Current	ı	-	6	[A]	at rising time=470us
	Dimming Frequency	0.1	0.2	20	[kHz]	
F _{PWM}	Swing Voltage	3	3.3	5	V	
	Dimming Duty Cycle	10	-	100	%	
I _F	LED Forward Current		60		mA	Ta = 25°C
		1	-	1	Volt	
V\ _F	LED Forward Voltage	ı	38.4	40.8	Volt	$I_F = 60 \text{ mA}, \text{ Ta} = 25^{\circ}\text{C}$
		-	-	-		
P. co	LED Power		16.13	17.14	Watt	I _F =60 mA, Ta = 25°C
PLED	Consumption	-	10.13	17.14	vvall	LBx2: 16.13x2=32.26(typ)
LED Lifetime		50,000			Hrs	I _F =60 mA, Ta= 25°C

Note 1: Ta means ambient temperature of TFT-LCD module.

Note 2: VDD, P_{VDD} , P_{VDD} , Irush LED are defined for LED B/L.(100% duty of PWM dimming)

Note 3: I_F , V_F are defined for one channel LED. There are seven LED channels in one light bar. P_{LED} is defined for one light bar. For G240UAN01.0, there are two light bars in back light unit.

Note 4: If G240UAN01.0 module is driven by high current or at high ambient temperature & humidity condition. The operating life will be reduced.

Note 5: LED life means brightness goes down to 50% initial brightness.

Note 6: Only one kind types for adjusting brightness: PWM.

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6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

	1	2		1919	1920
1st Line	R G B	R G B		R G B	R G B
				-	
		(-)		-	*
		-	· 8	-	
		:	:	:	
				:	:
		-		•	
1200 Line	R G B	R G B	*****	R G B	R G B

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6.2 The Input Data Format

Data Mapping of JEIDA Format

RXCLKP	
RXCLKN	
RXIN10 P/N	X1R4 X1G4 X1R9 X1R8 X1R7 X1R6 X1R5 X1R4 X1G4
RXIN11 P/N	X 1G5 X 1B5 X 1B4 X 1G9 X 1G8 X 1G7 X 1G6 X 1G5 X 1B5
RXIN12 P/N	X 186 DE X 189 X 187 X 186 DE
RXIN13 P/N	X 1R2 X 1B3 X 1B2 X 1G3 X 1G2 X 1R3 X 1R2
RXIN14 P/N	X 180 X 181 X 180 X 1G1 X 1G0 X 1R1 X 1R0
RXIN20 P/N	X 2R4
RXIN21 P/N	2G5 2B5 2B4 2G9 2G8 2G7 2G6 2G5 2B5
RXIN22 P/N	2B6
RXIN23 P/N	X 2R2 X 2B3 X 2B2 X 2G3 X 2G2 X 2R3 X 2R2
RXIN24 P/N	X2R0 X2B1 X2B0 X2G1 X2G0 X2R1 X2R0

10 BIT COLOR BIT ORDER		
MSB	R9	
	R8	
	R7	
	R6	
	R5	
	R4	
	R3	
	R2	
	R1	
LSB	R0	

Note1: Normally DE mode only. VS and HS on EVEN channel are not used.

Note2: Please follow VESA.

Note3: 10-bit in

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6.3 Signal Description

The module using a pair of LVDS receiver SN75LVDS82(Texas Instruments) or compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS83(negative edge sampling) or compatible. The first LVDS port(RxOxxx) transmits odd pixels while the second LVDS port(RxExxx) transmits even pixels.

PIN # SIGNAL NAME	while th	ne second LVDS po	ort(RxExxx) transmits even pixels.
2 NC Do not connect (for AUO test) 3 NC Do not connect (for AUO test) 4 NC Do not connect (for AUO test) 5 NC Do not connect (for AUO test) 6 NC Do not connect (for AUO test) 7 VSS Power Ground 8 VSS Power Ground 9 NC Do not connect (for AUO test) 10 VSS Power Ground 11 VSS Power Ground 12 RXOINO- Negative LVDS differential data input (Odd data) 13 RXOINO+ Positive LVDS differential data input (Odd data) 14 RXOIN1- Negative LVDS differential data input (Odd data) 15 RXOIN1+ Positive LVDS differential data input (Odd data) 16 RXOIN2- Negative LVDS differential data input (Odd data) 17 RXOIN2+ Positive LVDS differential data input (Odd data) 18 VSS Power Ground 19 RXOCLKIN- Negative LVDS differential data input (Odd data) 20 RXOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RXOIN3- Negative LVDS differential data input (Odd data) 23 RXOIN3- Negative LVDS differential data input (Odd data) 24 RXOIN4- Positive LVDS differential data input (Odd data) 25 RXOIN4- Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RXEIN0- Negative LVDS differential data input (Even data) 29 RXEIN0+ Positive LVDS differential data input (Even data)	PIN#	SIGNAL NAME	DESCRIPTION
3 NC Do not connect (for AUO test) 4 NC Do not connect (for AUO test) 5 NC Do not connect (for AUO test) 6 NC Do not connect (for AUO test) 7 VSS Power Ground 8 VSS Power Ground 9 NC Do not connect (for AUO test) 10 VSS Power Ground 11 VSS Power Ground 12 RxOINO- Negative LVDS differential data input (Odd data) 13 RxOINO+ Positive LVDS differential data input (Odd data) 14 RxOIN1- Negative LVDS differential data input (Odd data) 15 RxOIN1+ Positive LVDS differential data input (Odd data) 16 RxOIN2- Negative LVDS differential data input (Odd data) 17 RxOIN2+ Positive LVDS differential data input (Odd data) 18 VSS Power Ground 19 RxOCLKIN- Negative LVDS differential data input (Odd data) 20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential clock input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	1	VSS	Power Ground
4 NC Do not connect (for AUO test) 5 NC Do not connect (for AUO test) 6 NC Do not connect (for AUO test) 7 VSS Power Ground 8 VSS Power Ground 9 NC Do not connect (for AUO test) 10 VSS Power Ground 11 VSS Power Ground 11 VSS Power Ground 12 RxOINO- Negative LVDS differential data input (Odd data) 13 RxOINO+ Positive LVDS differential data input (Odd data) 14 RxOIN1- Negative LVDS differential data input (Odd data) 15 RxOIN1+ Positive LVDS differential data input (Odd data) 16 RxOIN2- Negative LVDS differential data input (Odd data) 17 RxOIN2+ Positive LVDS differential data input (Odd data) 18 VSS Power Ground 19 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4- Negative LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	2	NC	Do not connect (for AUO test)
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8 VSS Power Ground 9 NC Do not connect (for AUO test) 10 VSS Power Ground 11 VSS Power Ground 11 VSS Power Ground 12 RxOIN0- Negative LVDS differential data input (Odd data) 13 RxOIN0+ Positive LVDS differential data input (Odd data) 14 RxOIN1- Negative LVDS differential data input (Odd data) 15 RxOIN1+ Positive LVDS differential data input (Odd data) 16 RxOIN2- Negative LVDS differential data input (Odd data) 17 RxOIN2+ Positive LVDS differential data input (Odd data) 18 VSS Power Ground 19 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0- Positive LVDS differential data input (Even data)	6	NC	Do not connect (for AUO test)
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10 VSS Power Ground 11 VSS Power Ground 12 RxOIN0- Negative LVDS differential data input (Odd data) 13 RxOIN0+ Positive LVDS differential data input (Odd data) 14 RxOIN1- Negative LVDS differential data input (Odd data) 15 RxOIN1+ Positive LVDS differential data input (Odd data) 16 RxOIN2- Negative LVDS differential data input (Odd data) 17 RxOIN2+ Positive LVDS differential data input (Odd data) 18 VSS Power Ground 19 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	8	VSS	Power Ground
11 VSS Power Ground 12 RxOIN0- Negative LVDS differential data input (Odd data) 13 RxOIN0+ Positive LVDS differential data input (Odd data) 14 RxOIN1- Negative LVDS differential data input (Odd data) 15 RxOIN1+ Positive LVDS differential data input (Odd data) 16 RxOIN2- Negative LVDS differential data input (Odd data) 17 RxOIN2+ Positive LVDS differential data input (Odd data) 18 VSS Power Ground 19 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data)	9	NC	Do not connect (for AUO test)
12 RxOIN0- Negative LVDS differential data input (Odd data) 13 RxOIN0+ Positive LVDS differential data input (Odd data) 14 RxOIN1- Negative LVDS differential data input (Odd data) 15 RxOIN1+ Positive LVDS differential data input (Odd data) 16 RxOIN2- Negative LVDS differential data input (Odd data) 17 RxOIN2+ Positive LVDS differential data input (Odd data) 18 VSS Power Ground 19 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data)	10	VSS	Power Ground
13 RxOIN0+ Positive LVDS differential data input (Odd data) 14 RxOIN1- Negative LVDS differential data input (Odd data) 15 RxOIN1+ Positive LVDS differential data input (Odd data) 16 RxOIN2- Negative LVDS differential data input (Odd data) 17 RxOIN2+ Positive LVDS differential data input (Odd data) 18 VSS Power Ground 19 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data)	11	VSS	Power Ground
14 RxOIN1- Negative LVDS differential data input (Odd data) 15 RxOIN2- Negative LVDS differential data input (Odd data) 16 RxOIN2- Negative LVDS differential data input (Odd data) 17 RxOIN2+ Positive LVDS differential data input (Odd data) 18 VSS Power Ground 19 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	12	RxOIN0-	Negative LVDS differential data input (Odd data)
15 RxOIN1+ Positive LVDS differential data input (Odd data) 16 RxOIN2- Negative LVDS differential data input (Odd data) 17 RxOIN2+ Positive LVDS differential data input (Odd data) 18 VSS Power Ground 19 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	13	RxOIN0+	Positive LVDS differential data input (Odd data)
16 RxOIN2- Negative LVDS differential data input (Odd data) 17 RxOIN2+ Positive LVDS differential data input (Odd data) 18 VSS Power Ground 19 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	14	RxOIN1-	Negative LVDS differential data input (Odd data)
17 RxOIN2+ Positive LVDS differential data input (Odd data) 18 VSS Power Ground 19 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	15	RxOIN1+	Positive LVDS differential data input (Odd data)
18 VSS Power Ground 19 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	16	RxOIN2-	Negative LVDS differential data input (Odd data)
19 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	17	RxOIN2+	Positive LVDS differential data input (Odd data)
20 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	18	VSS	Power Ground
21 VSS Power Ground 22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	19	RxOCLKIN-	Negative LVDS differential clock input (Odd clock)
22 RxOIN3- Negative LVDS differential data input (Odd data) 23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	20	RxOCLKIN+	Positive LVDS differential clock input (Odd clock)
23 RxOIN3+ Positive LVDS differential data input (Odd data) 24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	21	VSS	Power Ground
24 RxOIN4- Negative LVDS differential data input (Odd data) 25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	22	RxOIN3-	Negative LVDS differential data input (Odd data)
25 RxOIN4+ Positive LVDS differential data input (Odd data) 26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	23	RxOIN3+	Positive LVDS differential data input (Odd data)
26 VSS Power Ground 27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	24	RxOIN4-	Negative LVDS differential data input (Odd data)
27 VSS Power Ground 28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	25	RxOIN4+	Positive LVDS differential data input (Odd data)
28 RxEIN0- Negative LVDS differential data input (Even data) 29 RxEIN0+ Positive LVDS differential data input (Even data)	26	VSS	Power Ground
29 RxEIN0+ Positive LVDS differential data input (Even data)	27	VSS	Power Ground
	28	RxEIN0-	Negative LVDS differential data input (Even data)
	29	RxEIN0+	Positive LVDS differential data input (Even data)
30 RXEIN1- Negative LVDS differential data input (Even data)	30	RxEIN1-	Negative LVDS differential data input (Even data)

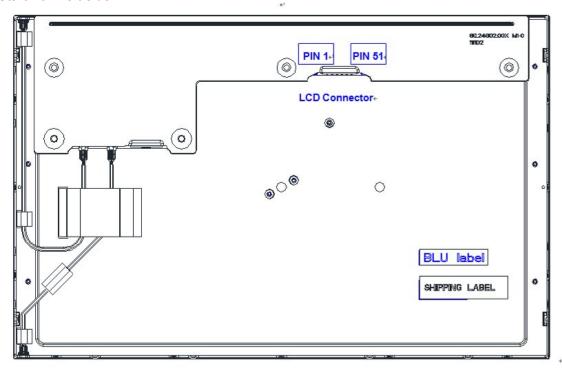
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PIN#	SIGNAL NAME	DESCRIPTION
31	RxEIN1+	Positive LVDS differential data input (Even data)
32	RxEIN2-	Negative LVDS differential data input (Even data)
33	RxEIN2+	Positive LVDS differential data input (Even data)
34	VSS	Power Ground
35	RxECLKIN-	Negative LVDS differential clock input (Even clock)
36	RxECLKIN+	Positive LVDS differential clock input (Even clock)
37	VSS	Power Ground
38	RxEIN3-	Negative LVDS differential data input (Even data)
39	RxEIN3+	Positive LVDS differential data input (Even data)
40	RxEIN4-	Negative LVDS differential data input (Even data)
41	RxEIN4+	Positive LVDS differential data input (Even data)
42	VSS	Power Ground
43	VSS	Power Ground
44	VSS	Power Ground
45	VSS	Power Ground
46	NC	Do not connect (for AUO test)
47	NC	Do not connect (for AUO test)
48	VCC	+12.0V Power Supply
49	VCC	+12.0V Power Supply
50	VCC	+12.0V Power Supply
51	VCC	+12.0V Power Supply

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Note1: Start from left side



Note2: Input signals of odd and even clock shall be the same timing.

Note3: Please follow VESA.

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6.4 Interface Timing

6.4.1 Timing Characteristics

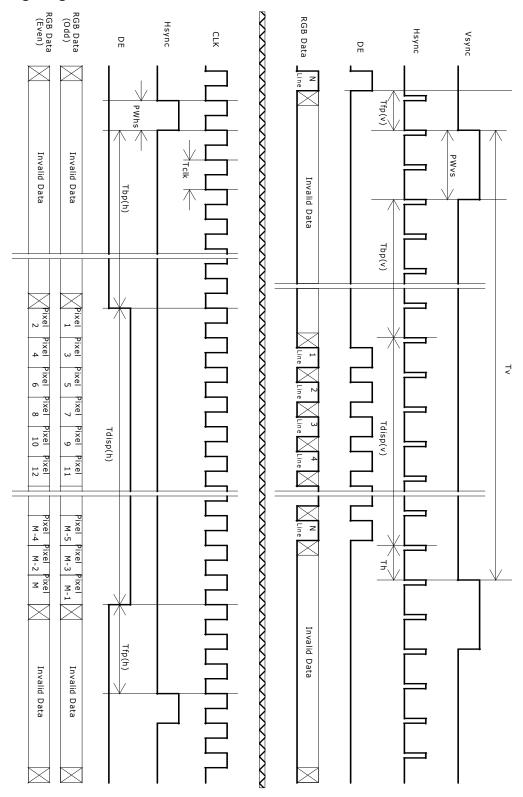
Signal	Item	Symbol	Min	Тур	Max	Unit
	Period	Tv	1214	1235	1734	Th
Vertical	Active	Tdisp(v)	1200	1200	1200	Th
Section	Blanking	Tbp(v)+Tfp(v)+PWvs	14	35	534	Th
	Period	Th	1000	1040	1428	Tclk
Horizontal	Active	Tdisp(h)	960	960	960	Tclk
Section	Blanking	Tbp(h)+Tfp(h)+PWhs	40	80	468	Tclk
	Period	Tclk	11.8	13	16.8	ns
Clock	Frequency	Freq.	59.5	77	85	MHz
Frame Rate	Frequency	1/Tv	49	60	66	Hz

Note: DE mode only

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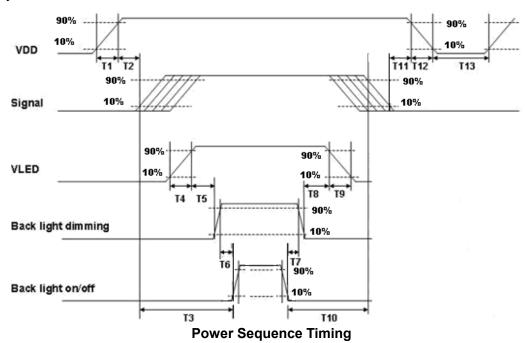
6.4.2 Timing Diagram





6.5 Power ON/OFF Sequence

VDD power and LED on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



	Power Sequence Timing			
Davamatav	Value			11-24-
Parameter	Min.	Тур.	Max.	Units
T1	0.5	-	10	
T2	30	40	50	
Т3	200	-		
T4	0.5	-	10	
Т5	10	-	-	
Т6	10	-	-	
Т7	0	-	-	ms
Т8	10	-	-	
Т9	-	-	10	
T10	110	-	-	
T11	0	16	50	
T12	0		10	
T13	1000	-	-	

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7. Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

7.1.1 Connector

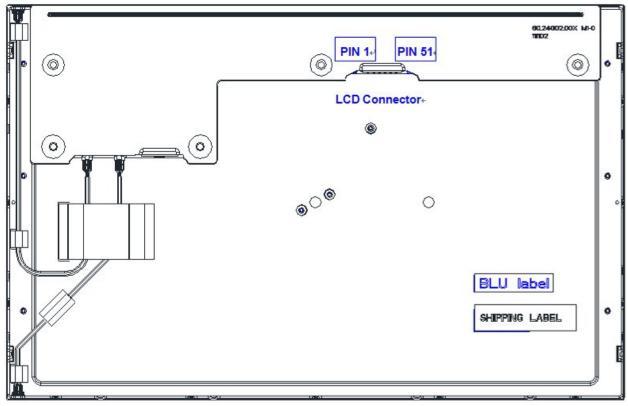
LCD	manufacturer	JAE
	part number	FI-RE51S-HF-R1500
Mating	manufacturer	JAE
waing	part number	FI-RE51HL

7.1.2 Pin Assignment

PIN#	Symbol	PIN#	Symbol
1	GND	27	GND
2	NC	28	RE0N
3	NC	29	RE0P
4	NC	30	RE1N
5	NC	31	RE1P
6	NC	32	RE2N
7	GND	33	RE2P
8	GND	34	GND
9	NC	35	RECLKN
10	GND	36	RECLKP
11	GND	37	GND
12	RO0N	38	RE3N
13	RO0P	39	RE3P
14	RO1N	40	RE4N
15	RO1P	41	RE4P
16	RO2N	42	GND
17	RO2P	43	GND
18	GND	44	GND
19	ROCLKN	45	GND

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20	ROCLKP	46	NC
21	GND	47	NC
22	RO3N	48	VDD
23	RO3P	49	VDD
24	RO4N	50	VDD
25	RO4P	51	VDD
26	GND		



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7.2 Backlight Unit

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

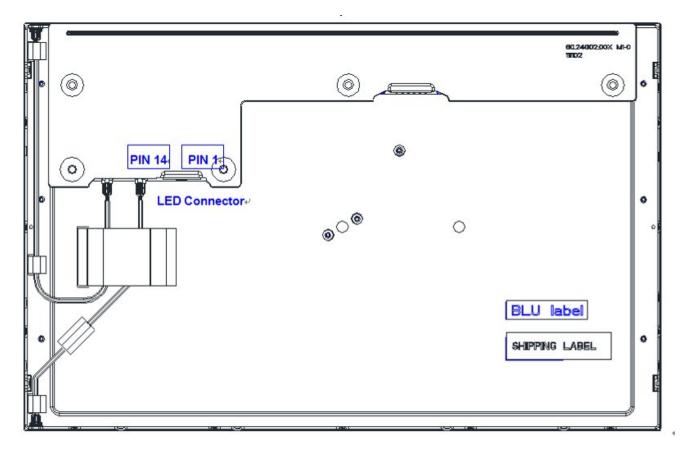
Daaldialat	manufacturer	JST
Backlight	part number	S14B-PH-SM6-K-TB(HF)
N 4 = 1" = =	manufacturer	JST
Mating	part number	PHR-14

7.2.1 Signal for LED connector

Pin#	Symbol	Pin Description
1	VDD	Power +24V
2	VDD	Power +24V
3	VDD	Power +24V
4	VDD	Power +24V
5	VDD	Power +24V
6	GND	GND
7	GND	GND
8	GND	GND
9	GND	GND
10	GND	GND
11	NC	Do not connect
12	EN	Enable(0V:disable, 2.5~5V:Enable)
13	Dimming	PWM; duty 10%~ 100%
14	NC	Do not connect

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8. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 40°C, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 40°C, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0°C, 300hours	
High Temperature Storage (HTS)	Ta= 50°C, 300hours	
Low Temperature Storage (LTS)	Ta= -20°C, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 G Wave: Random Frequency: 10 - 200 - 10 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20 °C /30min, 50/ °C 30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electrostatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 9 points, 25 times/ point.	2
	Air Discharge: \pm 15KV, 150pF(330 Ω) 1sec 9 points, 25 times/ point.	
Altitude Test	Operation:10,000 ft Non-Operation:30,000 ft	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20°C to 50°C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2, ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

Note 3:

- Water condensation is not allowed for each test items.
- Each test is done by new TFT-LCD module. Don't use the same TFT-LCD module repeatedly for reliability test.
- The reliability test is performed only to examine the TFT-LCD module capability.
- To inspect TFT-LCD module after reliability test, please store it at room temperature and room humidity for 24 hours at least in advance.
- No function failure occurs.

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9. Shipping Label and Packaging

9.1 Shipping Label

The label is on the panel as shown below:



Manufactured XX/XX Madel No: **G240UAN01.0** AU Optronics XXXX MADE IN XXXXXX (XX)







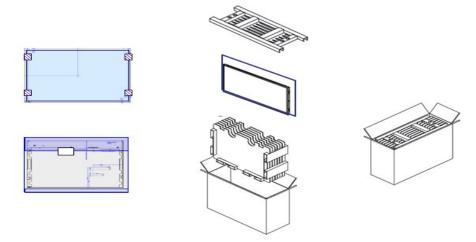
Note 1: For Pb Free products, AUO will add for identification.

Note 2: For RoHS compatible products, AUO will add RoHS for identification.

Note 3: For China RoHS compatible products, AUO will add for identification.

Note 4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

9.2 Packaging



Max capacity: 6 PCS TFT-LCD module per carton

Max weight: 17.3 kg per carton

Outside dimension of carton: 630mm(L)* 245mm(W)*450mm(H)

Pallet size: 1060 mm * 760 mm * 132mm

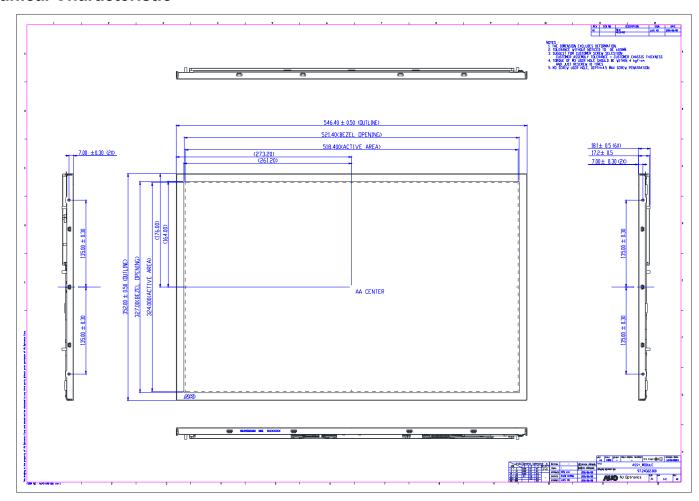
Box stacked

Module by air Max: (1 *4) *3 layers, one pallet put 12 boxes, total 72pcs module

Module by $sea_Max : (1*4)*3$ layers + (1*4)*1 layers , two pallet put 16 boxes , total 96pcs module Module by $sea_HQ_Max : (1*4)*3$ layers+(1*4)*1 layers, two pallet put 16 boxes, total 96pcs module

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10. Mechanical Characteristic

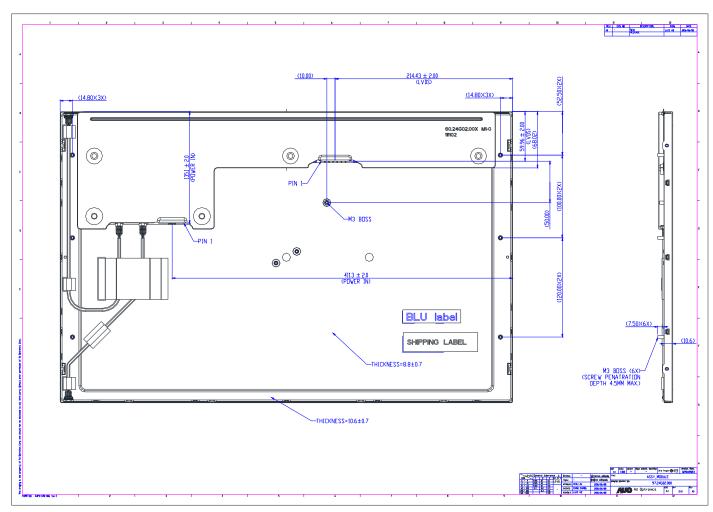


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