(V) Preliminary Specifications
( ) Final Specifications

Module	**10.1”(10.01”) WXGA 16:10 Color TFT-LCD**
Model Name	**B101EAN01.0 (H/W: 0A) LCM**
Note ( )	

Customer	**Date**	**Approved by**	**Date**
		YW Lee	August 28, 2013
Checked & Approved by	**Date**	**Prepared by**	
		Bing Ho	August 28th, 2013

Note: This Specification is subject to change without notice.

MPBU Marketing Division
AU Optronics corporation

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 8/28/2013			1st version	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Disconnecting power supply before handling LCD , it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors. It can prevent electrostatic breakdown.

2. General Description

This specification applies to the 10.1 inch-wide Color a-Si TFT-LCD Module B101EAN01.0. The display supports the 16:10 WXGA, 1280(H) x800(V) screen and 16.7M colors (RGB 6-bits data driver with FRC). All input signals are LVDS interface compatible and this module doesn't contain an inverter board for backlight.

2.1 Display Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	10.07			
Active Area	[mm]	216.96(H) x 135.6(V)			
Pixels H x V		1280 x 3(RGB) x 800			
Pixel Pitch	[mm]	0.1695 X 0.1695			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		AHVA, Normally Black			
White Luminance (I_{LED}=17.2mA) **(Note: ILED is LED current)**	[cd/m2]	450 typ. (Center Point)			
Luminance Uniformity		TYP. 90% / MIN.80% 9 points measure (W/R/G/B/Gray)			
Contrast Ratio		TYP. 900:1 / Min 700:1			
Response Time	[ms]	Typ. 30 (White to black)			
Nominal Input Voltage VDD	[Volt]	3.3V typ			
Power Consumption	[Watt]	Logic: 0.79 W@ full white pattern BLU: 2.064W max. , w/o effi. * 40ea x 17.2mA x 3.0V			
Weight	[Grams]	145g Max			
Physical Size **Include bracket**	[mm]		Min	Typ	Max
		Length	228.01	228.21	228.41
		Width	148.66	148.86	149.06
		Thicknes	-	2.39	2.59
Electrical Interface		1 channel LVDS			
Glass Thickness	[mm]	0.25/0.25 (w/o PF)			
Surface Treatment (panel only)		HCLR			
Support Color		16.7M colors (RGB 6-bit +FRC)			

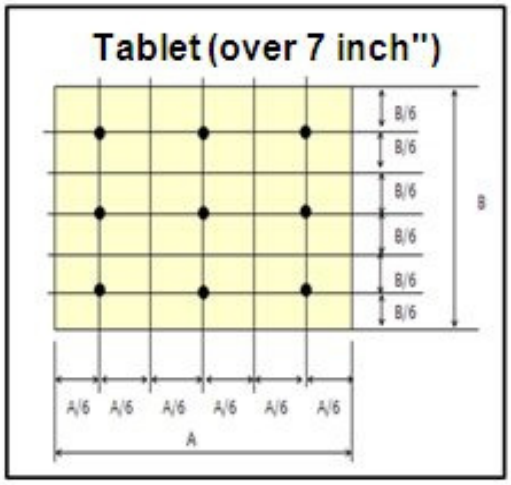
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=17.2mA			Center point	360	450	-	cd/m^2	1, 3.
Viewing Angle		θ_R	Horizontal (Right)		80	-	degree	4, 9
		θ_L	CR = 10 (Left)		80	-		
		ϕ_H	Vertical (Upper)		80	-		
		ϕ_L	CR = 10 (Lower)		80	-		
Brightness Uniformity		%	9 Points	80	90			1, 3, 4
Contrast Ratio		CR		700	900	-		4, 6
Flicker		%	CA-310 (Flicker pattern < 10 FLK)		10			4, 7
Response Time		T_{RT}	White to black	-	30		msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.598	0.601	0.604		4
		Ry		0.347	0.35	0.353		
	Green	Gx		0.329	0.332	0.335		
		Gy		0.585	0.588	0.591		
	Blue	Bx		0.146	0.149	0.152		
		By		0.126	0.129	0.132		
	White	CCT		6500	7000	7700		
		uv		0.0025	0.01	0.0175		
NTSC		%		45	50	-		

Note 1: 9 points position (Ref: Active area)

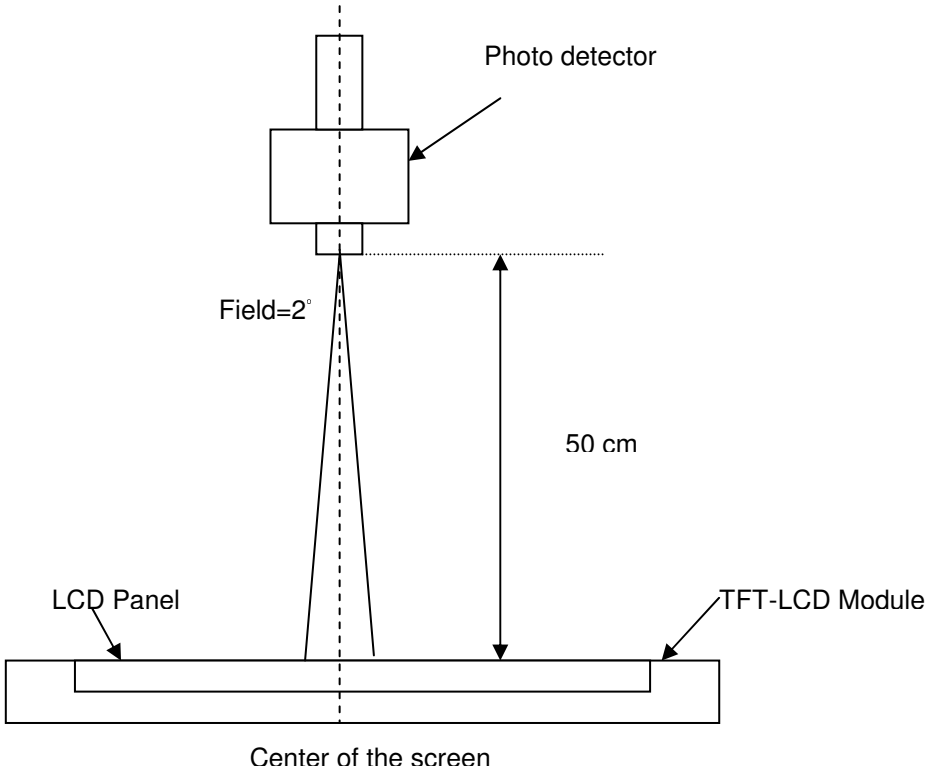


Note 2: The luminance uniformity of 9 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of nine points}}{\text{Minimum Brightness of nine points}}$$

Note 3: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 4： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

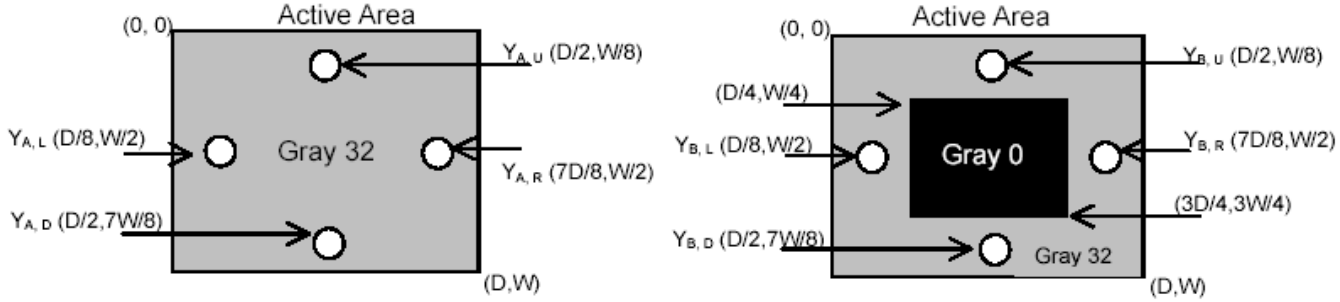
Note 5： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$

Where

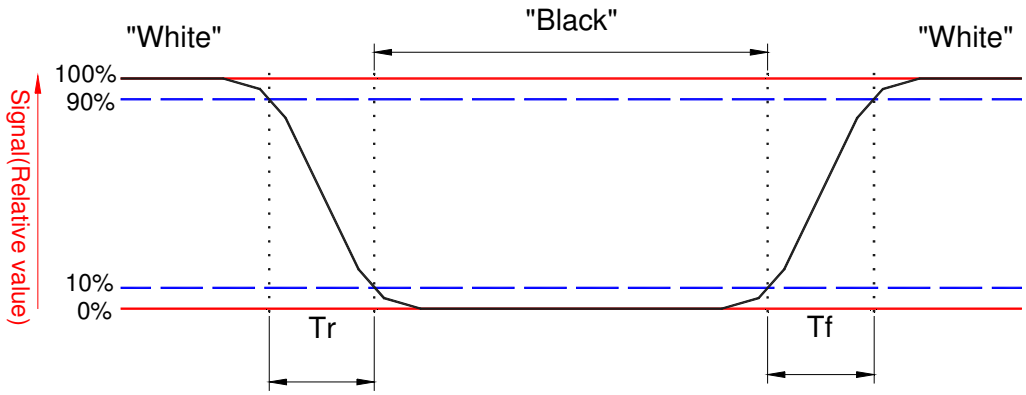
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



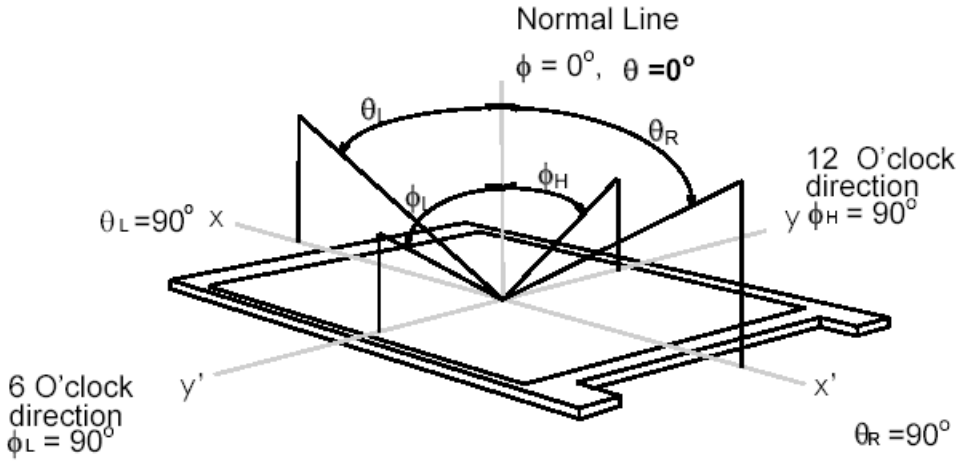
Note 6 Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



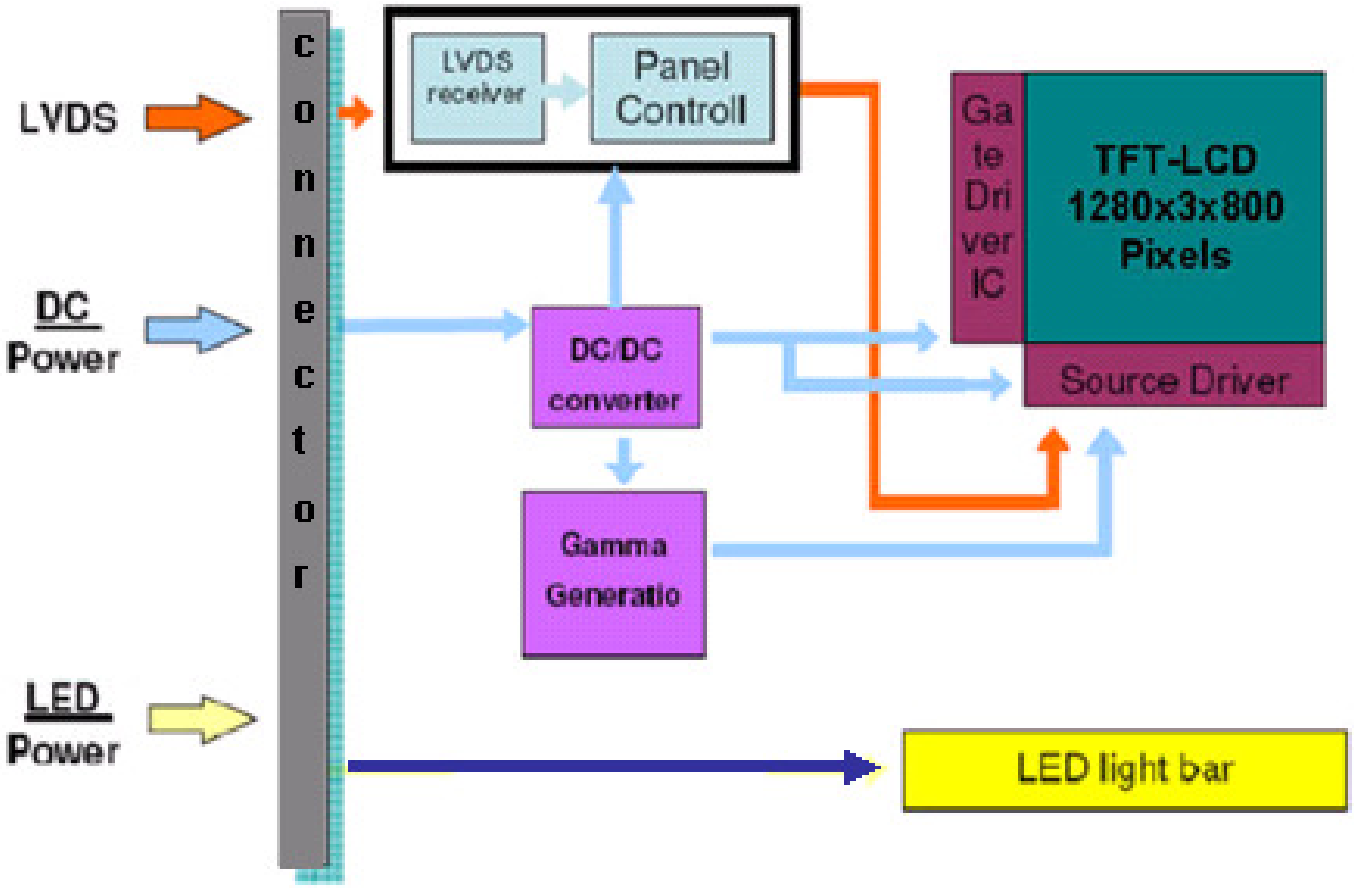
Note 7. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 45 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

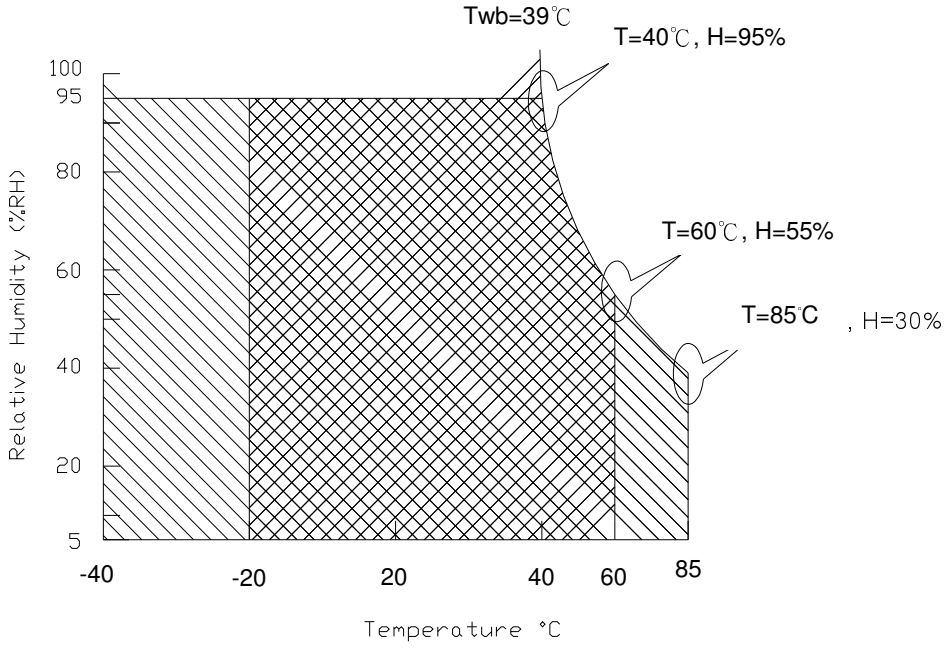
4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	-20	+60	[°C]	Note 3
Operation Humidity	HOP	0	95	[%RH]	Note 3
Storage Temperature	TST	-40	+85	[°C]	Note 3
Storage Humidity	HST	0	85	[%RH]	Note 3

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range

Storage Range

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

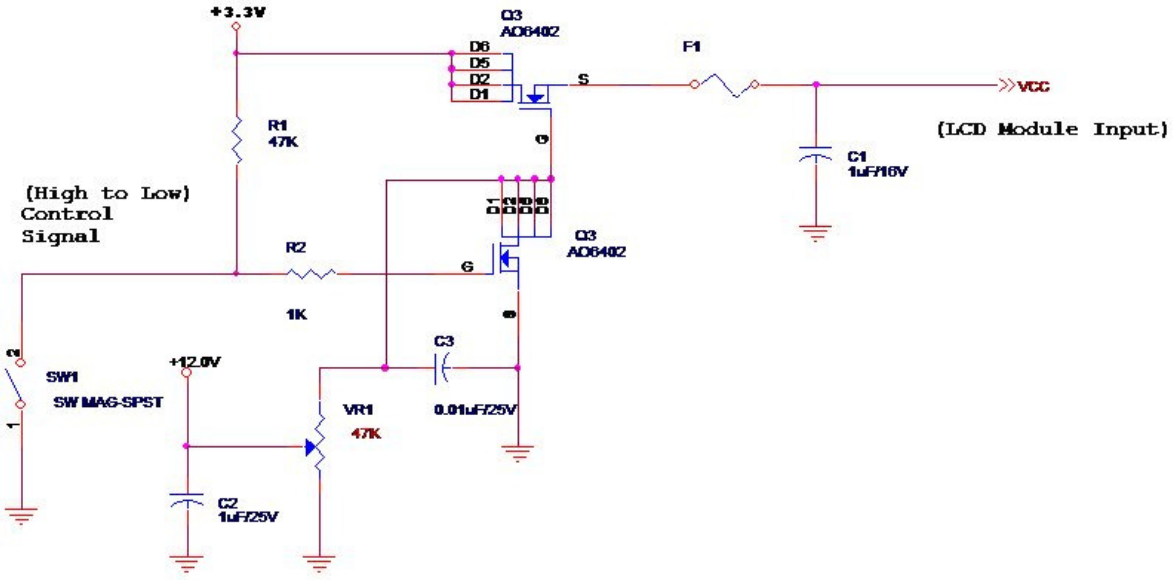
Input power specifications are as follows;

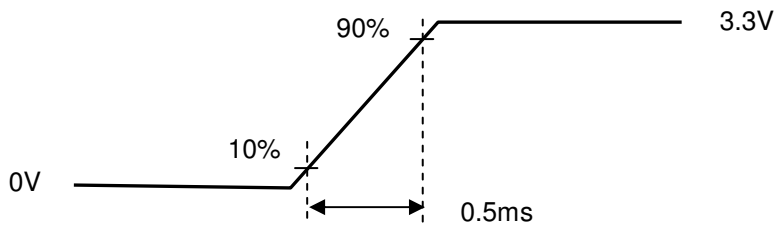
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.79	[Watt]	Note 1
IDD	IDD Current	-	-	240	[mA]	Note 1
IRush	Inrush Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{white}$)

Note 2 : Measure Condition





Vin rising time

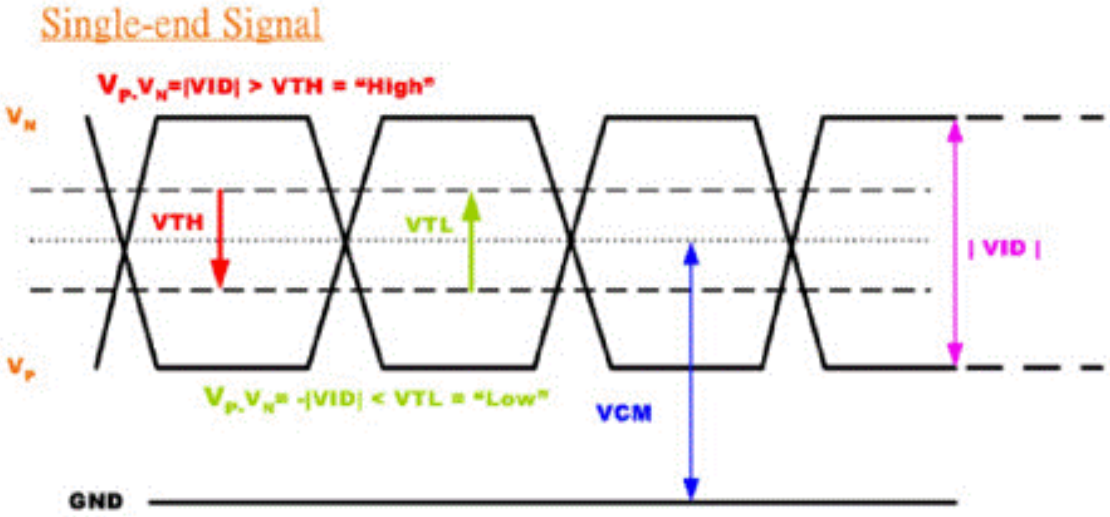
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{TH}	Differential Input High Threshold (Vcm=+1.2V)	---	100	[mV]
V_{TL}	Differential Input Low Threshold (Vcm=+1.2V)	-100	----	[mV]
$\|V_{ID}\|$	Differential Input Voltage	100	600	[mV]
V_{CM}	Differential Input Common Mode Voltage	1.125	1.375	[V]

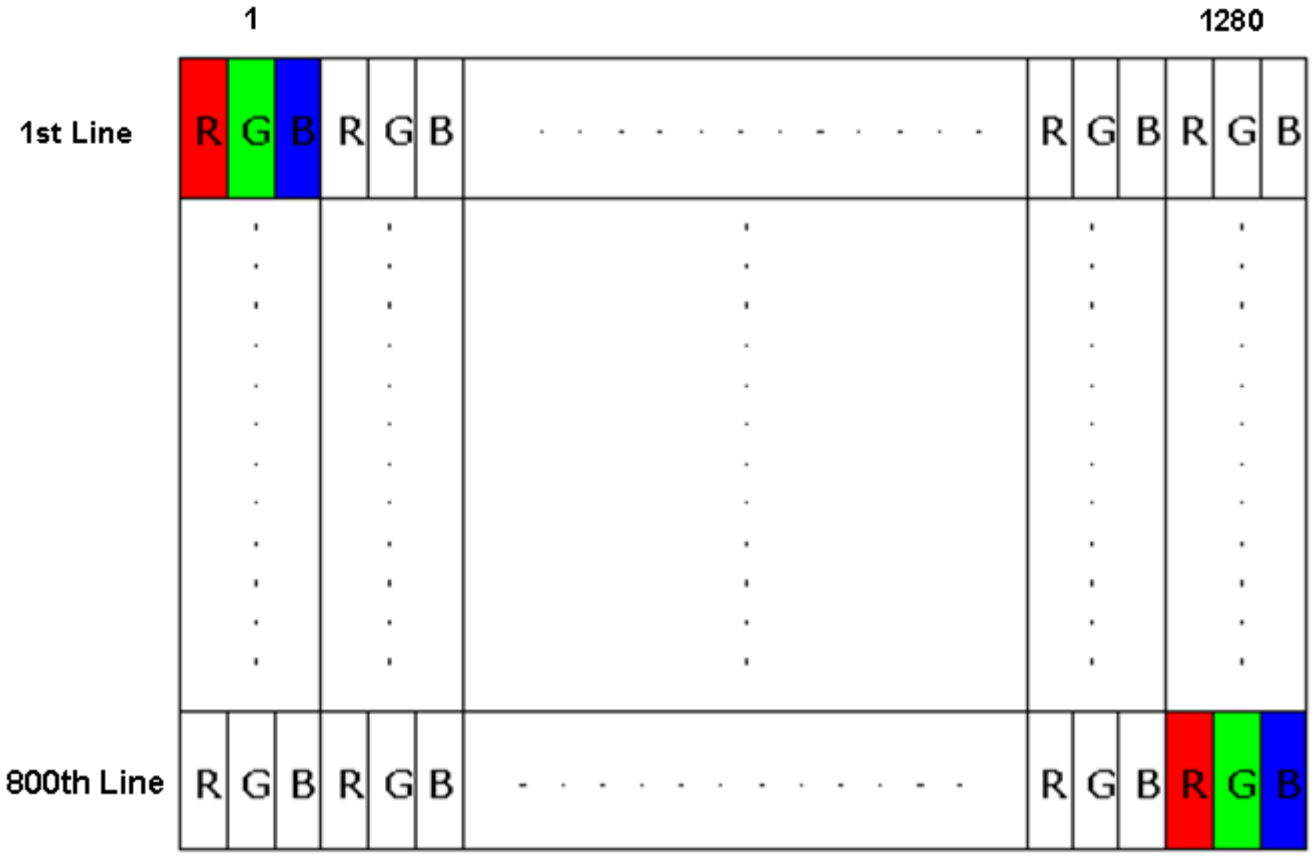
Note: LVDS Signal Waveform



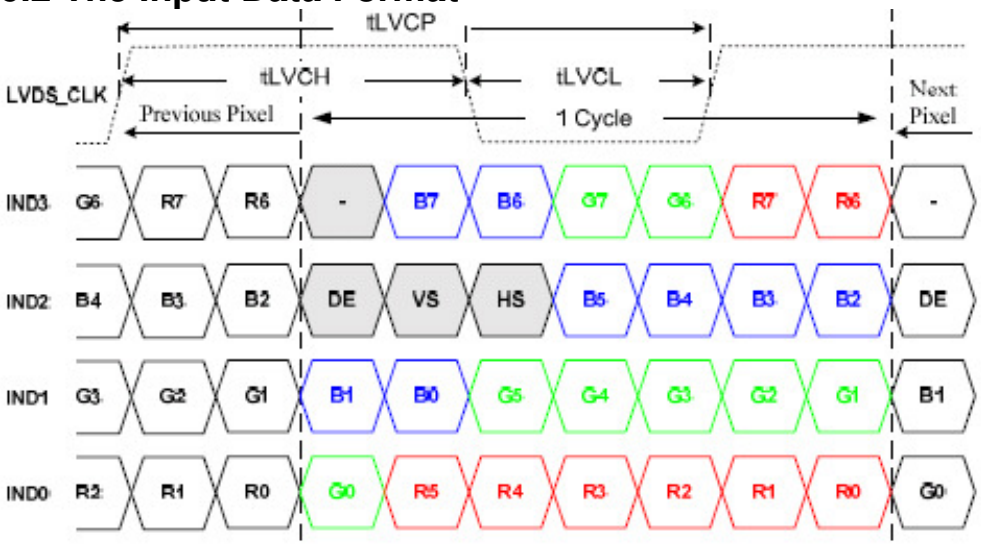
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Signal Name	Description	
R7 R6 R5 R4 R3 R2 R1 R0	Red Data 7 (MSB) Red Data 6 Red Data 5 Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 8 bits pixel data.
G7 G6 G5 G4 G3 G2 G1 G0	Green Data 7 (MSB) Green Data 6 Green Data 5 Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 8 bits pixel data.
B7 B6 B5 B4 B3 B2 B1 B0	Blue Data 7 (MSB) Blue Data 6 Blue Data 5 Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 8 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 LVDS Connector Description

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	DDK
Type / Part Number	FF12-45A-R12BN-D3

6.3.2 LVDS Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

	Signal Name	Description
1	VSS	Ground
2	ID	ID pin
3	NC	No connection
4	VDD	Logic power 3.3V
5	VDD	Logic power 3.3V
6	VDD	Logic power 3.3V
7	VDD	Logic power 3.3V
8	VDD	Logic power 3.3V
9	WPN	No connection
10	SCL	No connection
11	SDA	No connection
12	VSS	Ground
13	VSS	Ground
14	VSS	Ground
15	RXin3N	-LVDS differential data (3N)
16	RXin3P	+LVDS differential data (3P)
17	VSS	Ground
18	LVDS_RX_N	-LVDS differential clock input
19	LVDS_RX_P	+LVDS differential clock input
20	VSS	Ground
21	RXin2N	-LVDS differential data (2N)
22	RXin2P	+LVDS differential data (2P)
23	VSS	Ground
24	RXin1N	-LVDS differential data (1N)
25	RXin1P	+LVDS differential data (1P)
26	VSS	Ground
27	RXin0N	-LVDS differential data (0N)
28	RXin0P	+LVDS differential data (0P)
29	VSS	Ground
30	VSS	Ground
31	NC	No connection

32	FB1	LED FB1
33	FB2	LED FB2
34	FB3	LED FB3
35	FB4	LED FB4
36	NC	No connection
37	NC	No connection
38	NC	No connection
39	VLED1	LED Power Supply Voltage
40	VLED2	LED Power Supply Voltage
41	VLED3	LED Power Supply Voltage
42	VLED4	LED Power Supply Voltage
43	VLED5	LED Power Supply Voltage
44	NC	No connection
45	VSS	Ground

6.3.3 LED Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	**For Signal Connector**
Manufacturer	Hirose
Type / Part Number	TF13-9S-0.4SH-001

6.3.4 LED Pin Assignment

	Signal Name	**Description**
1	VLED+	LED positive voltage
2	VLED+	LED positive voltage
3	VLED+	LED positive voltage
4	-	NC
5	-	NC
6	VLED-	LED FB1
7	VLED-	LED FB2
8	VLED-	LED FB3
9	VLED-	LED FB1

6.4 LVDS Interface Timing

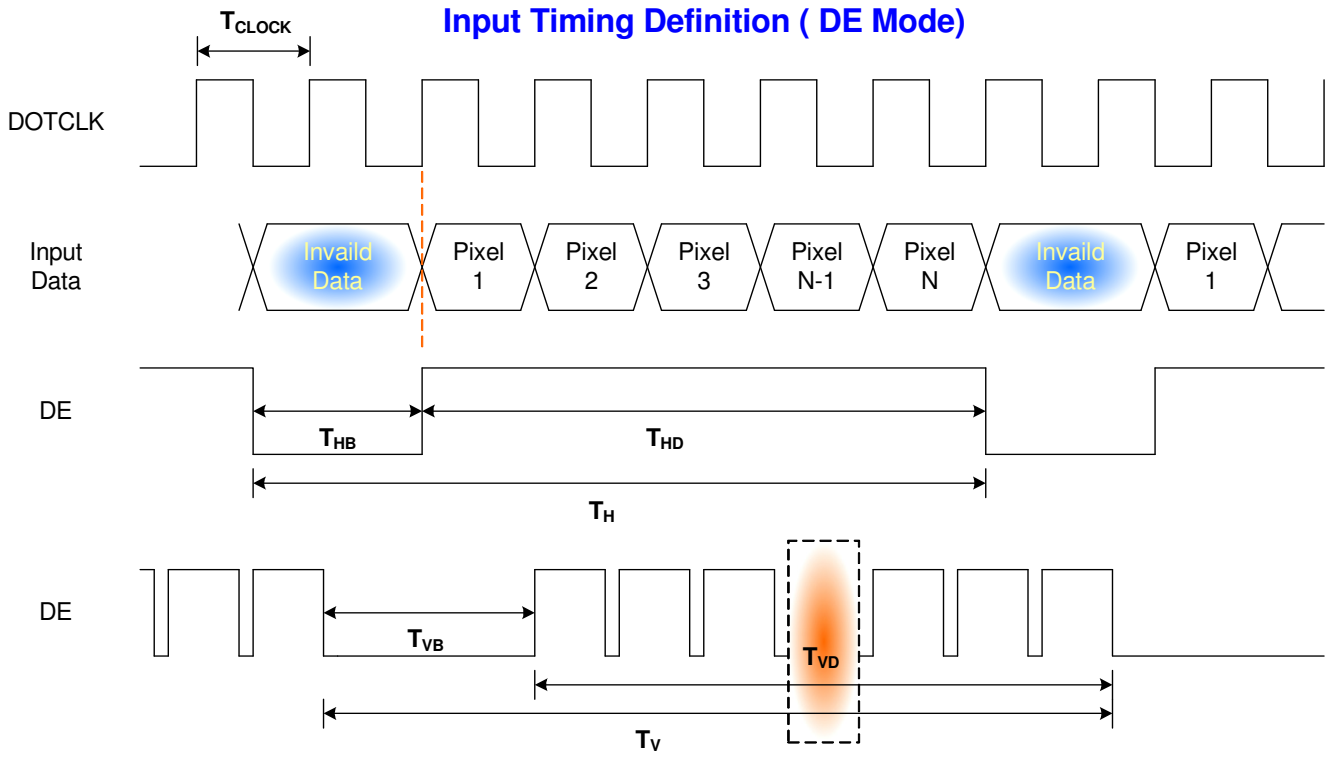
6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T_{Clock}	64	68.93	80	MHz
Vertical Section	Period	T_V	808	816	1023	T_{Line}
	Active	T_{VD}	800			
	Blanking	T_{VB}	8	16	223	
Horizontal Section	Period	T_H	1310	1408	2047	T_{Clock}
	Active	T_{HD}	1280			
	Blanking	T_{HB}	30	128	767	

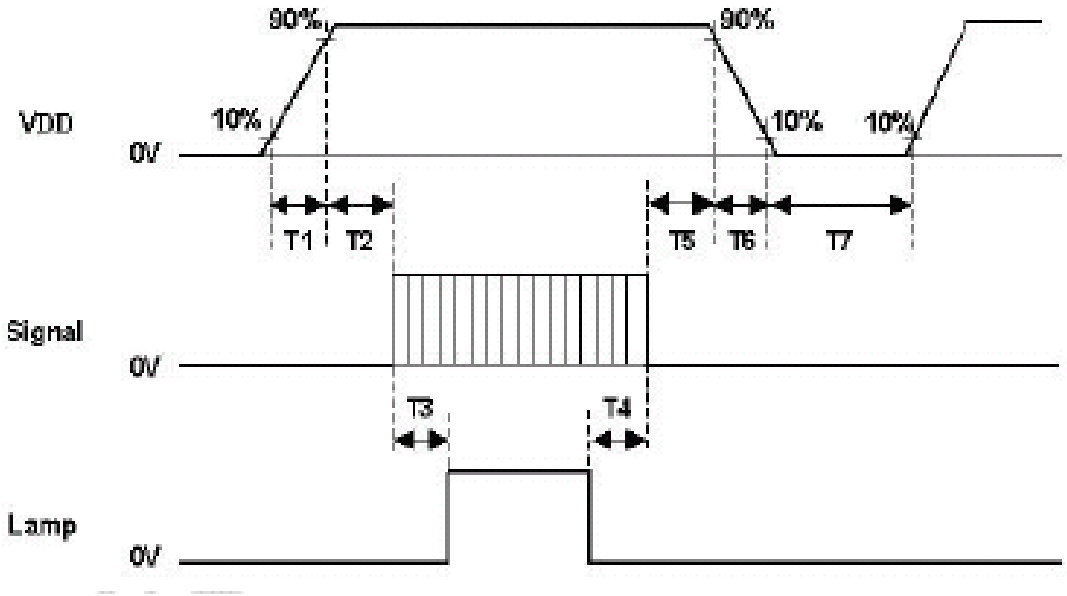
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Power Sequence Timing			
Parameter	Value		Units
	Min.	Max.	
T1	**0.5**	**10**	**ms**
T2	**30**	**50**	
T3	**200**	**-**	
T4	**200**	**-**	
T5	**0**	**50**	
T6	**0**	**10**	
T7	**500**	**-**	

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

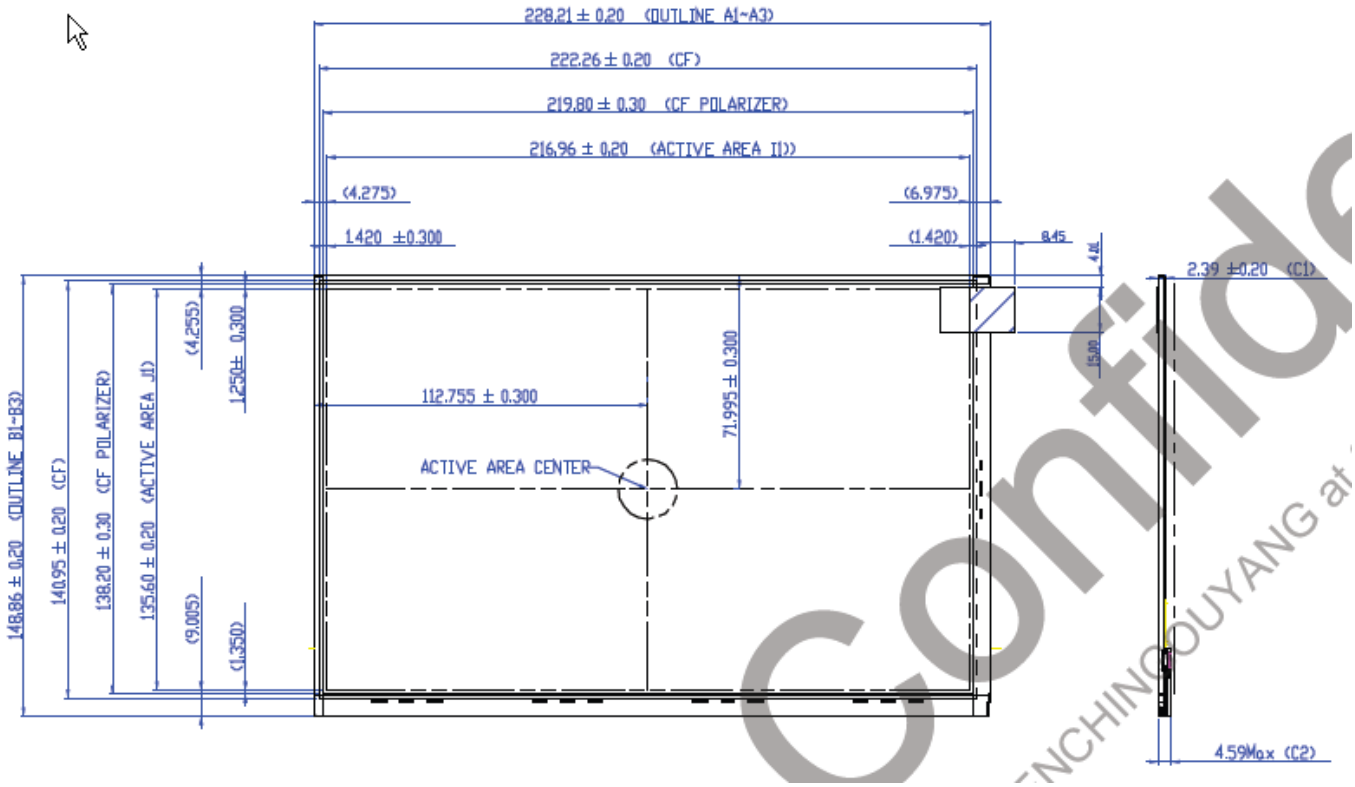
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 240h	
High Temperature Operation	Ta= 50℃, Dry, 240h	
Low Temperature Operation	Ta= 0℃, 240h	
High Temperature Storage	Ta= 60℃, 240h	
Low Temperature Storage	Ta= -20℃, 240h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

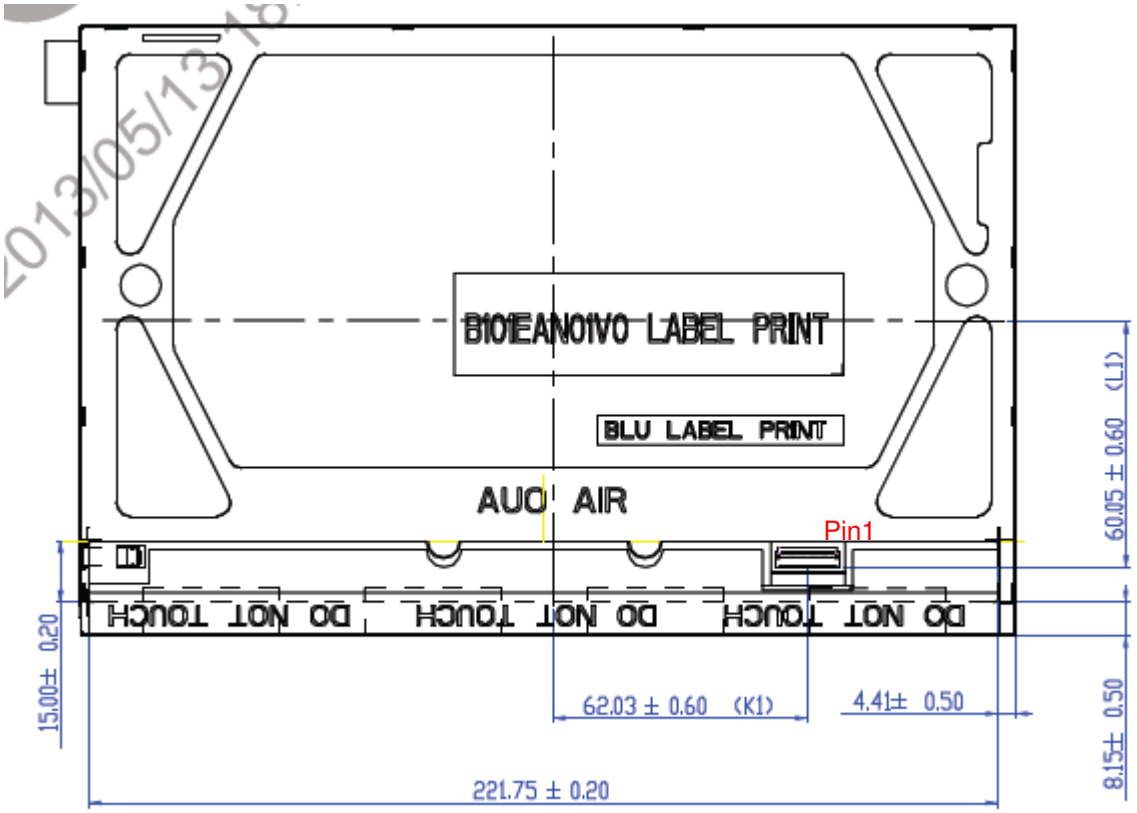
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 Standard Front View



8.2 Standard Rear View



9. Shipping and Package

9.1 Shipping Label Format

YY/WW : year/week code, B101EAN01.0 : Model name

9.2 Carton Label Format

9.3 hipping Package of Palletizing Sequence

TBD