(٧)	Preliminary Specification
())	Final Specification

Module	24.0" WUXGA Color TFT-LCD
Model Name	M240UW01 V0

Customer Date	Prepared by Date
Approved by	Approved by
Note: This Specification is subject to change without notice.	Desktop Display Business Group / AU Optronics corporation

document version 0.3 1/26



Contents

1.0 Handling Precautions	
2.0 General Description	5
2.1 Display Characteristics	5
2.2 Optical Characteristics	6
3.0 Functional Block Diagram	10
4.0 Absolute Maximum Ratings	
4.1 TFT LCD Module	11
4.2 Backlight Unit	11
4.3 Absolute Ratings of Environment	11
5.0 Electrical characteristics	12
5.1 TFT LCD Module	12
5.1.1 Power Specification	12
5.1.2 Signal Electrical Characteristics	13
6.0 Signal Characteristic	
6.1 Pixel Format Image	15
6.2 The input data format	15
6.3 Signal Description	16
6.4 Timing Characteristics	17
6.5 Timing diagram	18
6.6 Power ON/OFF Sequence	19
7.0 Connector & Pin Assignment	20
7.1 TFT LCD Module	20
7.1.1 Pin Assignment	20
7.2 Backlight Unit	21
7.2.1 Signal for Lamp connector	21
8.0 Reliability Test	
9.0 Shipping Label	23
•	24



AU OPTRONICS CORPORATION

Record of Revision

Vers	Version and Date Page		Old description	New Description	Remark	
0.1	2005/12/15	All	First Edition for Customer	-		
0.2	2006/3/10	5,6	Response Time TBD (Typ., GTG)	Response Time 8ms (Typ., GTG)		
		11	4.3 Absolute Ratings of Environment T=40°C,H=95%	4.3 Absolute Ratings of Environment T=40°C, H=90 %	Modified	
		17	6.4 Timing Characteristics Max. Frame Rate: Vsync= TBD Min. Frame Rate: Vsync= TBD	6.4 Timing Characteristics Max. Frame Rate: Vsync= 47Hz Min. Frame Rate: Vsync= 65Hz		
0.3	2006/5/2	5,6,7	$\label{eq:response} \begin{aligned} & \text{Response Time 12ms(Typ., on/off);} \\ & \text{Raising 7ms and Falling 5ms;} \\ & \text{Response Time 8ms (AVG., GTG);} \\ & & \text{Level A - Level B} \geq 16 \\ & \\ & \frac{\text{Level A - Level B}}{\text{Response Time}} & \frac{\text{Unit}}{\text{Imsec}} & \frac{\text{Conditions}}{\text{Raising Time}} & \frac{\text{Min.}}{\text{7}} & \frac{\text{Typ.}}{\text{Max.}} \\ & \frac{\text{Item}}{\text{Imsec}} & \frac{\text{Unit}}{\text{Raising Time}} & - & 5 \\ & \frac{\text{Imsec}}{\text{Imsec}} & \frac{\text{Raising Finhe}}{\text{Raising + Falling}} & - & 12 \\ & \frac{\text{Imsec}}{\text{Imsec}} & \frac{\text{Gray to Gray}}{\text{Gray to Gray}} & - & 8 \\ & - & \\ \end{aligned}$	Response Time 16 ms(Typ., on/off); Raising 10 ms and Falling 6 ms; Response Time 6ms (AVG., GTG); Level A - Level B \geq 32; Max. 10 ms 2.2 Optical Characteristics	Modified	
		12	LCD Inrush Curent TBD	LCD Inrush Curent 5 A		
		14	CCFL Frequency: Min 48KHz; Max 58KHz	CCFL Frequency: Min 40 KHz; Max 60 KHz	Modified	

document version 0.3 3/26



1.0 Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL reflector edge. Instead, press at the far ends of the CCFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit (IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

document version 0.3 4/26



AU OPTRONICS CORPORATION

2.0 General Description

This specification applies to the 24.0 inch Color a-Si TFT-LCD Module M240UW01.

The display supports the WUXGA (1920(H) x 1200(V)) screen format and 16.7M colors (RGB 8-bits data).

All input signals are 2 channel LVDS interface compatible.

This module doesn't contain an inverter board for backlight.

2.1 Display Characteristics

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	611.32(24")
Active Area	[mm]	518.4 (H) x 324 (V)
Pixels H x V		1920(x3) x 1200
Pixel Pitch	[mm]	0.270 (per one triad) x 0.270
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally Black
White Luminance (Center)	[cd/m ²]	$500 \text{ cd/m}^2 $
Contrast Ratio		1000 : 1 (Typ.)
Optical Response Time	[msec]	16ms(Typ., on/off); 6ms(AVG., GTG)
Nominal Input Voltage VDD	[Volt]	+5.0 V
Power Consumption	[Watt]	74 W (Typ.) (without inverter)
(VDD line + CCFL line)		
Weight	[Grams]	3250 (Max)
Physical Size	[mm]	546.4(W) x 352(H) x 35.8(D) (Typ.)
Electrical Interface		Even/Odd R/G/B data, clock LVDS
Support Color		16.7M colors (RGB 8-bit data)
Surface Treatment		Anti-Glare, 3H
Temperature Range		
Operating	[°C]	0 to +50
Storage (Shipping)	[°C]	-20 to +60
RoHS Compliance		RoHS Compliance

document version 0.3 5/26



AU OPTRONICS CORPORATION

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C:

Item	Unit	Conditions	Min.	Тур.	Max.	Note
Viewing Angle	[degree]	Horizontal (Right) CR = 10 (Left)	75 75	89 89	-	
	[degree] [degree]	Vertical (Up) CR = 10 (Down)	75 75	89 89	-	
Contrast ratio		Normal Direction	700	1000	-	
Response Time	[msec]	Raising Time	-	10	-	Note 1
	[msec]	Falling Time	-	6	-	Note 1
	[msec]	Raising + Falling	-	16	20	Note 1
	[msec]	Gray to Gray	-	6	10	Note 2
Color / Chromaticity Coordinates (CIE)		Red x	0.623	0.653	0.683	
Coordinates (CIL)		Red y	0.307	0.337	0.367	
		Green x	0.265	0.295	0.325	
		Green y	0.577	0.607	0.637	
		Blue x	0.114	0.144	0.174	
		Blue y	0.045	0.075	0.105	
Color Coordinates (CIE) White		White x	0.283	0.313	0.343	
Color Coordinates (CIL) Write		White y	0.299	0.329	0.359	
Central Luminance (I _L =6mA)	[cd/m ²]		400	500	-	
Luminance Uniformity	[%]		75	80		Note 3
Crosstalk (in60Hz)	[%]				1.5	Note 4
Flicker	dB				-20	Note 5

Equipment Pattern Generator, Power Supply, Digital Voltmeter, Luminance meter (PR 880, BM-5A,

BM 7, CS-1000, & EZContrast*)

Aperture
Test Point
Environment

1° with 100cm VD or 2° with 50cm viewing distance Center (VESA point 9) < 1 lux

PR-880 / BM5A / BM7

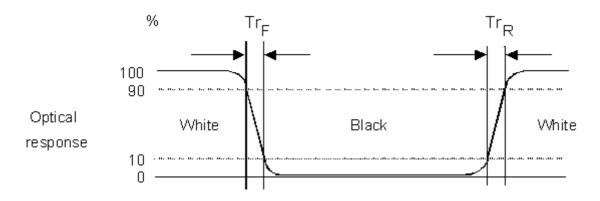
document version 0.3 6/26



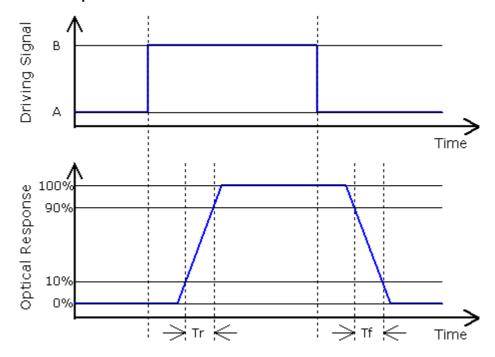
*' EZ Contrast is different measurement tool with very close viewing distance.

Note 1: Definition of Response time

The output signals of photodetector are measured when the input signals are changed from "Black" to "White" (rising time), and from "White" to "Black "(falling time), respectively. The response time is interval between the 10% and 90% of amplitudes.



Note 2: Over-Drive and Response time:



Algorithm:

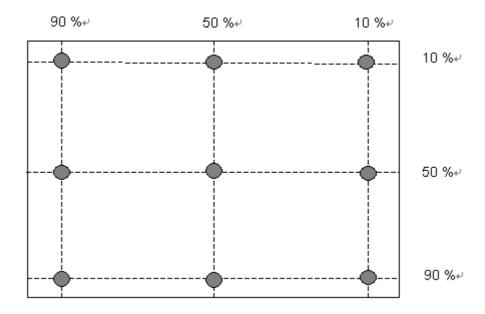
Level A - Level B \geq 32 then the average of Grey-to-Grey response time is 6 ms. (F= 60 Hz).

Tr (rising time; from "Black" to "White") + Tf (Falling time; from "White" to "Black") = 16 ms(typ).

document version 0.3 7/26



Note 3: Luminance uniformity of these 9 points is defined as below



Uniformity = $\frac{\text{Minimum Luminance in 9 points (1-9)}}{\text{Maximum Luminance in 9 Points (1-9)}}$

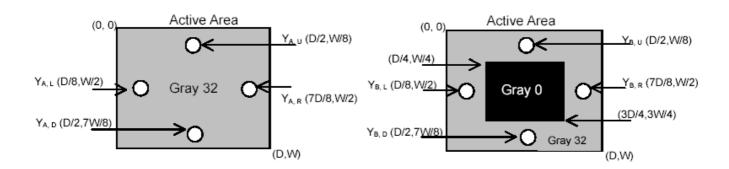
Note 4: Crosstalk is defined as below:

$$CT = | YB - YA | / YA \times 100 (\%)$$

Where

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

YB = Luminance of measured location with gray level 0 pattern (cd/m2)



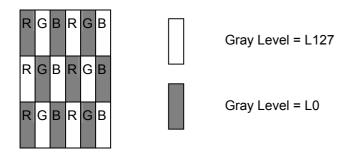
document version 0.3 8/26



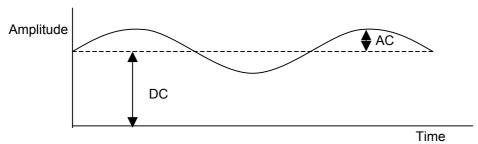
M240UW01 V0

AU OPTRONICS CORPORATION

Note 5: Test Paterm: Subchecker Pattern



Method: Record dBV & DC value with (WESTAR)TRD-100

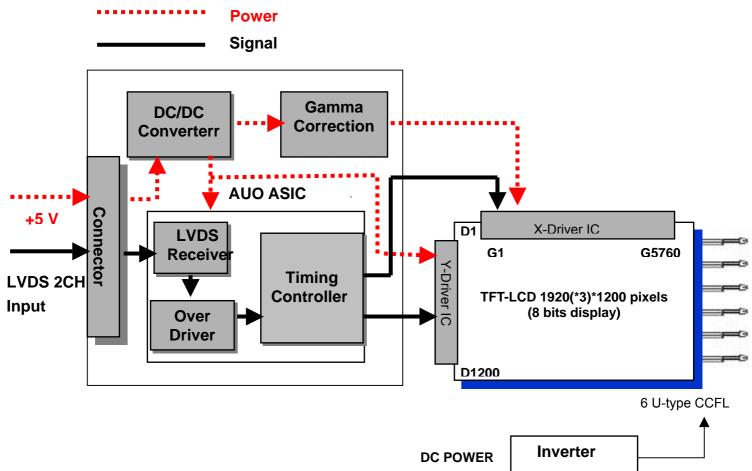


Flicker (dB) = $20 \log \frac{AC \text{ Level(at 30 Hz)}}{DC \text{ Level}}$

document version 0.3 9/26

3.0 Functional Block Diagram

The following diagram shows the functional block of the 24.0 inch Color TFT-LCD Module:



I/F PCB Interface:

JAE FI-XB30SSL-HF15 or compatible

Mating Type:

FI-X30HL-T (Locked Type)

FI-X30S-H (Unlocked Type)

document version 0.3 10/26

4.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	VIN	4.5	5.5	[Volt]	Note 1,2

4.2 Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICFL	2.0	8.0	[mA] rms	Note 1,2

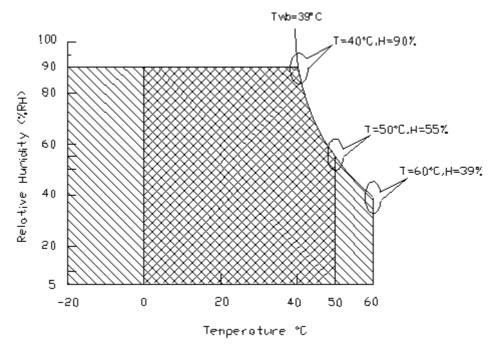
4.3 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	
Operation Humidity	HOP	5	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	90	[%RH]	

Note 1: With in Ta = 25°C

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality perfermance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range



Storage Range



document version 0.3



5.0 Electrical characteristics

5.1 TFT LCD Module

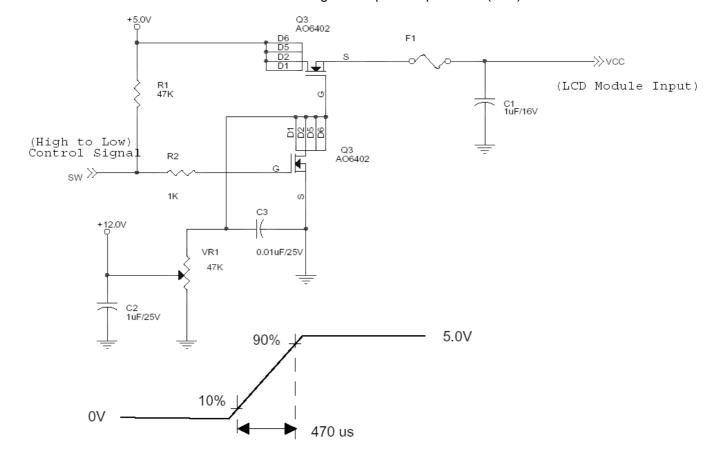
5.1.1 Power Specification

Input power specifications are as follows;

Symbol	Parameter	Min	Тур	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	4.5	5.0	5.5	[Volt]	±10%
IDD	VDD current	-	1.8	2.2	[A]	VDD=5V , All White Pattern, at frame rate 60Hz
Irush	LCD Inrush Current	-	-	5	[A]	Note
PDD	VDD Power	-	9	11	[Watt]	VDD=5V , All White Pattern, at 60Hz

Note: Measurement conditions:

The duration of rush current is about 2ms and rising time of power input is 1ms(min.).



Vin rising time

document version 0.3



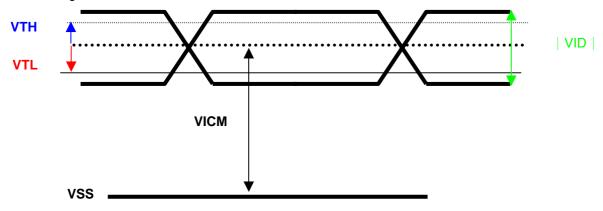
AU OPTRONICS CORPORATION

5.1.2 Signal Electrical Characteristics Input signals shall be low or Hi-Z state when Vin is off It is recommended to refer the specifications of SN75LVDS82DGG (Texas Instruments) in detail.

Each signal characteristics are as follows;

Symbol	Parameter	Min	Тур	Max	Units	Condition
VTH	Differential Input High		+50	+100	[mV]	VICM = 1.2V
VIII	Threshold	ı				Note
\	Differential Input Low	400	-50	-	[mV]	VICM = 1.2V
VTL	Threshold	-100				Note
VID	Input Differential Voltage	100	-	600	[mV]	Note
) // CN /	Differential Input Common	.4.0	.4.0	.4.5	D. /1	VTH-VTL = 200MV
VICM	Mode Voltage	+1.0	+1.2	+1.5	[V]	Note

Note: LVDS Signal Waveform



document version 0.3 13/26



5.2 Backlight Unit

Parameter guideline for CCFL Inverter is under stable conditions at 25°C (Room Temperature):

Parameter	Min.	Тур.	Max.	Unit	Condition	
CCFL Operation Current(IRCFL)	2.0	6.0	8.0	[mA] rms	Note 2	
CCFL Frequency(FCFL)	40	53	60	[KHz]	Note 3,4	
CCFL Ignition Voltage(ViCFL, Ta= 0°C)	2850	-	-	[Volt] rms	Note 5	
CCFL Ignition Voltage(ViCF, Ta= 25°C)	2280	-	-	[Volt] rms		
CCFL Operation Voltage (VCFL)	-	1800 (@ 6mA)	-	[Volt] rms	Note 6	
CCFL Power Consumption(PCFL)	-	64.8	-	[Watt]	Note 6	
CCFL Life Time(LTCFL)	40,000	50,000	-	[Hour]	Note 7	

Note 1: Typ. are AUO recommended design points.

- *1 All of characteristics listed are measured under the condition using the AUO test inverter.
- *2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
- *3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CCFL is damaged.
- *4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
- *5 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.
- Note 2: CCFL standard current is measured at 25±2°C.
- Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.
- Note 4: The frequency range will not affect to lamp life and reliability characteristics.
- Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 2850 voltage. Lamp units need 2850 voltage minimum for ignition.
- Note 6: The variance of CCFL power consumption is $\pm 10\%$. Calculator value for reference (IRCFL × VCFL × 6 = PCFL)
- Note 7: Definition of life: brightness becomes 50% or less than the minimum luminance value of CCFL. The typical life time of CCFL is on the condition at 6 mA lamp current.

document version 0.3 14/26



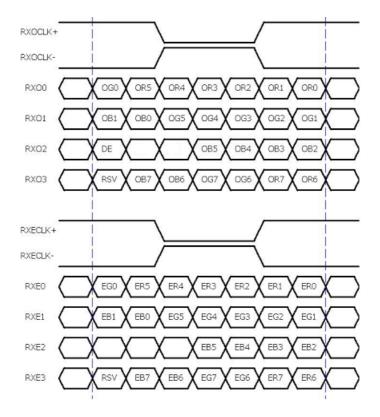
6.0 Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

		1		2			1	91	9	19	920	С
1st Line	R	G B	R	G	В		R	G	В	R	G	В
		-		-		- -		-			-	
		- -		-		• •		-			-	
		-		-		- -		-			-	
		-										
		•				•					•	
		•										
1200 Line	R	G B	R	G	В		R	G	В	R	G	В

6.2 The input data format



Note 1: R/G/B data 7:MSB, R/G/B data 0:LSB

O = "First Pixel Data" E = "Second Pixel Data"

document version 0.3 15/26



AU OPTRONICS CORPORATION

6.3 Signal Description

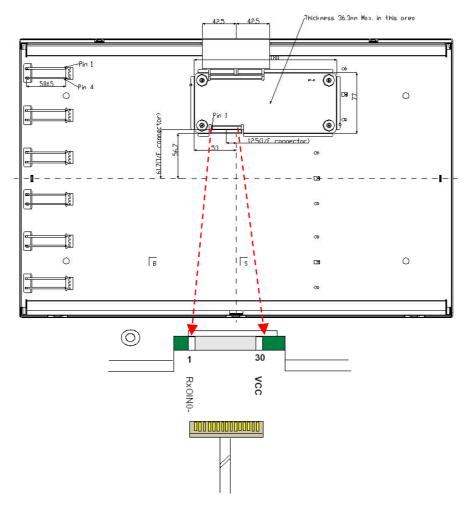
The module using one LVDS receiver SN75LVDS82(Texas Instruments) or compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS83(negative edge sampling) or compatible. The first LVDS port(RxOxxx) transmits odd pixels while the second LVDS port(RxExxx) transmits even pixels.

PIN#	SIGNAL NAME	DESCRIPTION
1	RxOIN0-	Negative LVDS differential data input (Odd data)
2	RxOIN0+	Positive LVDS differential data input (Odd data)
3	RxOIN1-	Negative LVDS differential data input (Odd data)
4	RxOIN1+	Positive LVDS differential data input (Odd data)
5	RxOIN2-	Negative LVDS differential data input (Odd data, DSPTMG)
6	RxOIN2+	Positive LVDS differential data input (Odd data, DSPTMG)
7	GND	Power Ground
8	RxOCLK-	Negative LVDS differential clock input (Odd clock)
9	RxOCLK+	Positive LVDS differential clock input (Odd clock)
10	RxOIN3-	Negative LVDS differential data input (Odd data)
11	RxOIN3+	Positive LVDS differential data input (Odd data)
12	RxEIN0-	Negative LVDS differential data input (Even data)
13	RxEIN0+	Positive LVDS differential data input (Even data)
14	GND	Power Ground
15	RxEIN1-	Positive LVDS differential data input (Even data)
16	RxEIN1+	Negative LVDS differential data input (Even data)
17	GND	Power Ground
18	RxEIN2-	Negative LVDS differential data input (Even data)
19	RxEIN2+	Positive LVDS differential data input (Even data)
20	RxECLK-	Negative LVDS differential clock input (Even clock)
21	RxECLK+	Positive LVDS differential clock input (Even clock)
22	RxEIN3-	Negative LVDS differential data input (Even data)
23	RxEIN3+	Positive LVDS differential data input (Even data)
24	GND	Power Ground
25	NC	No connection
26	NC	No connection
27	VDD	Power +5V
28	VDD	Power +5V
29	VDD	Power +5V
30	VDD	Power +5V

Note1: Start from left side

document version 0.3





Note2: Input signals of odd and even clock shall be the same timing.

6.4 Timing Characteristics

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS82DGG (Texas Instruments) or equivalent.

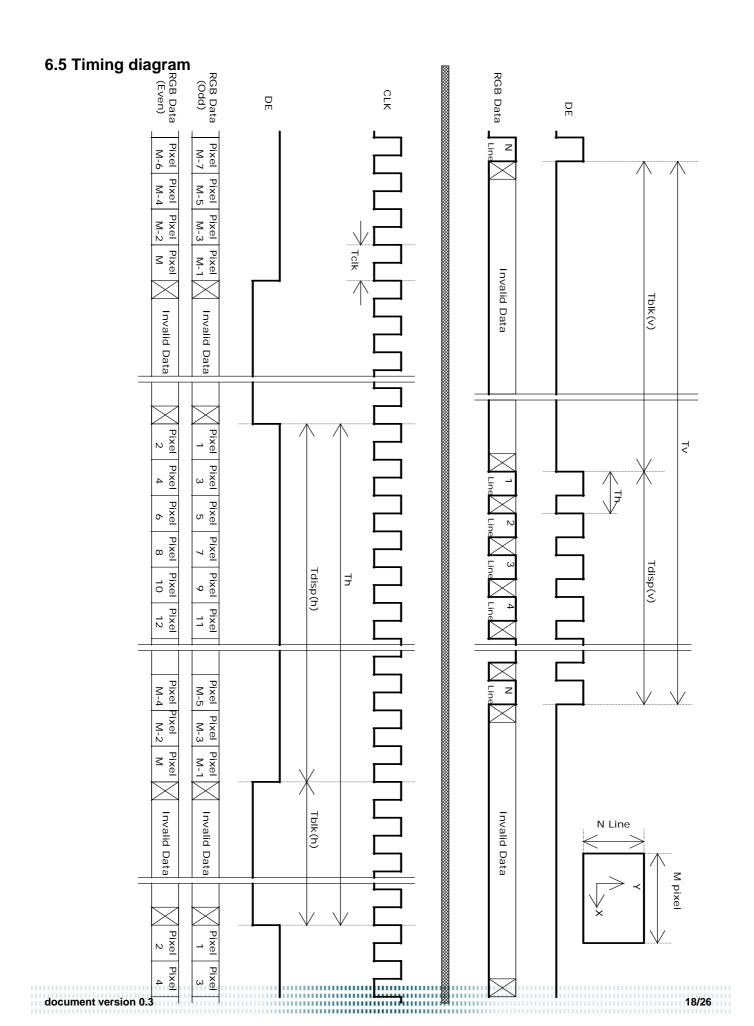
Note: Typical value refer to VESA STANDARD

Signal	Item	Symbol	Min	Тур	Max	Unit
	Period	Tv	1211	1212	2048	Th
Vertical	Active	Tdisp(v)	1200	1200	1200	Th
Section	Blanking	Tblk(v)	11	12	-	Th
	Period	Th	1040	1072	2048	Tclk
Horizontal Section	Active	Tdisp(h)	960	960	960	Tclk
	Blanking	Tblk(h)	80	112	-	Tclk
	Period	Tclk	11.76	-	-	ns
Clock	Frequency	Freq	-	-	85	MHz
Frame Rate	Frequency	Vsync	47	60	65	Hz

Note: DE mode only

document version 0.3 17/26



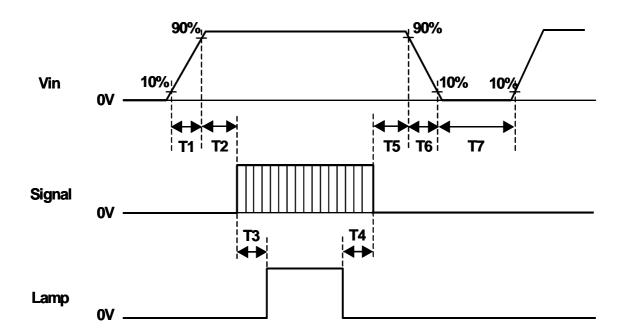




AU OPTRONICS CORPORATION

6.6 Power ON/OFF Sequence

Vin power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when Vin is off.



Symbol		Unit		
Symbol	Min	Тур	Max	Offic
T1	0.3	-	10	[ms]
T2	0.5	40	50	[ms]
Т3	300	1	-	[ms]
T4	300	1	-	[ms]
T5	0.5	16	50	[ms]
T6	0.5	-	60	[ms]
T7	1000	-	-	[ms]

document version 0.3 19/26



AU OPTRONICS CORPORATION

7.0 Connector & Pin Assignment

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	Interface Connector / Interface card		
Manufacturer	JAE or compatible		
Type Part Number	FI-XB30SSL-HF15		
Moting Housing Port Number	FI-X30HL-T (Locked Type)		
Mating Housing Part Number	FI-X30S-H (Unlocked Type)		

7.1.1 Pin Assignment

Pin#	Signal Name	Pin#	Signal Name
1	RxOIN0-	2	RxOIN0+
3	RxOIN1-	4	RxOIN1+
5	RxOIN2-	6	RxOIN2+
7	GND	8	RxOCLKIN-
9	RxOCLKIN+	10	RxOIN3-
11	RxOIN3+	12	RxEIN0-
13	RxEIN0+	14	GND
15	RxEIN1-	16	RxEIN1+
17	GND	18	RxEIN2-
19	RxEIN2+	20	RxECLKIN-
21	RxECLKIN+	22	RxEIN3-
23	RxEIN3+	24	GND
25	NV	26	NC
27	VDD	28	VDD
29	VDD	30	VDD

document version 0.3 20/26



AU OPTRONICS CORPORATION

7.2 Backlight Unit

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	Lamp Connector / Backlight lamp
Manufacturer	JST
Type Part Number	BHR-04VS-1
Mating Type Part Number	SM02(12)B-BH

7.2.1 Signal for Lamp connector

Connector	Pin No.	Input	Color	Function
CN1	1	Hot	Pink	High Voltage
	4	Hot	White	High Voltage
CN2	1	Hot	Pink	High Voltage
	4	Hot	White	High Voltage
CN3	1	Hot	Pink	High Voltage
	4	Hot	White	High Voltage
CN4	1	Hot	Pink	High Voltage
	4	Hot	White	High Voltage
CN5	1	Hot	Pink	High Voltage
	4	Hot	White	High Voltage
CN6	1	Hot	Pink	High Voltage
	4	Hot	White	High Voltage

document version 0.3 21/26



AU OPTRONICS CORPORATION

8.0 Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50°C, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0°C, 300hours	
High Temperature Storage (HTS)	Ta= 60°C, 300hours	
Low Temperature Storage (LTS)	Ta= -20°ℂ, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 G Wave: Random Frequency: 10 - 200 - 10 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20°C/30min, 60°C/30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: \pm 8KV, 150pF(330 Ω) 1sec, 8 points, 25 times/ point.	2
ESD (ElectroStatic Discharge)	Air Discharge: \pm 15KV, 150pF(330 Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:10,000 ft Non-Operation:30,000 ft	

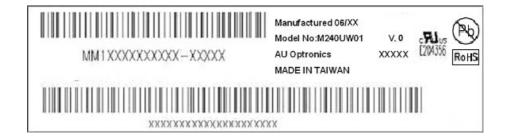
- Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.
- Note 2: According to EN61000-4-2, ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

document version 0.3 22/26



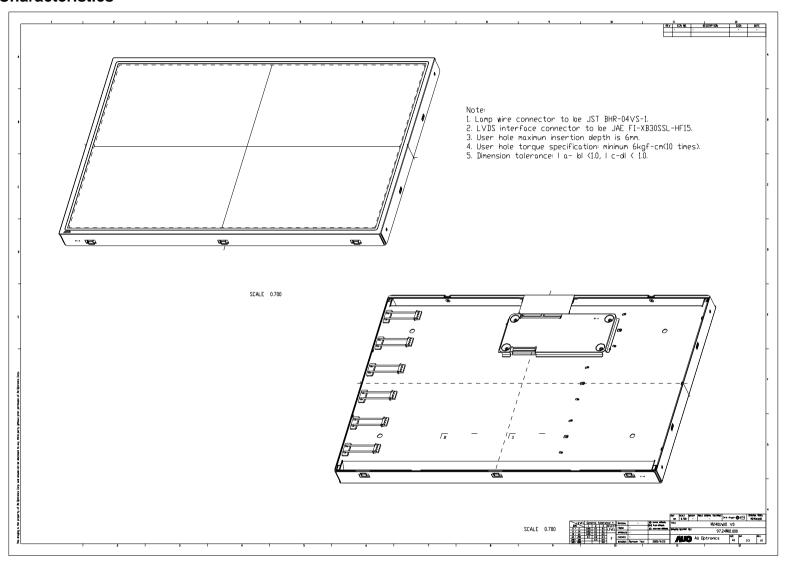
9.0 Shipping Label

The label is on the panel as shown below:

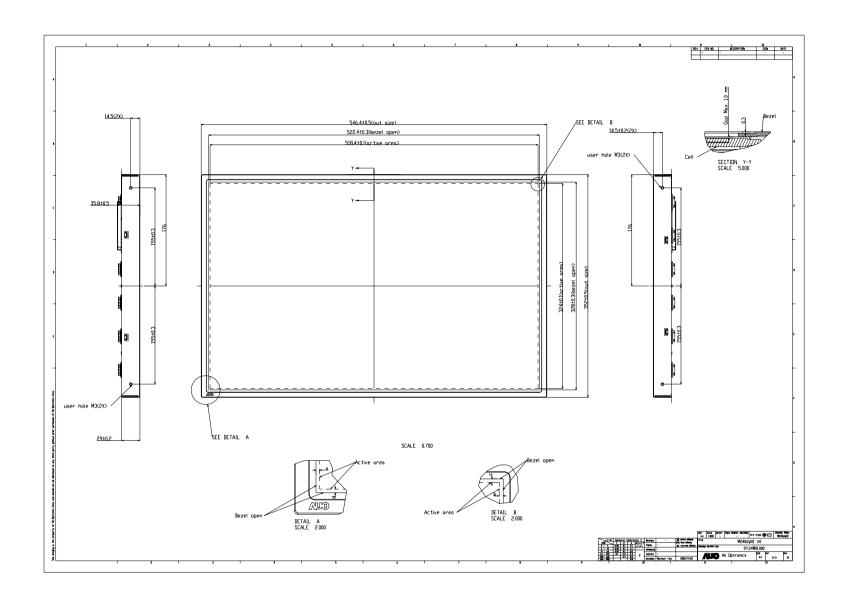


document version 0.3 23/26

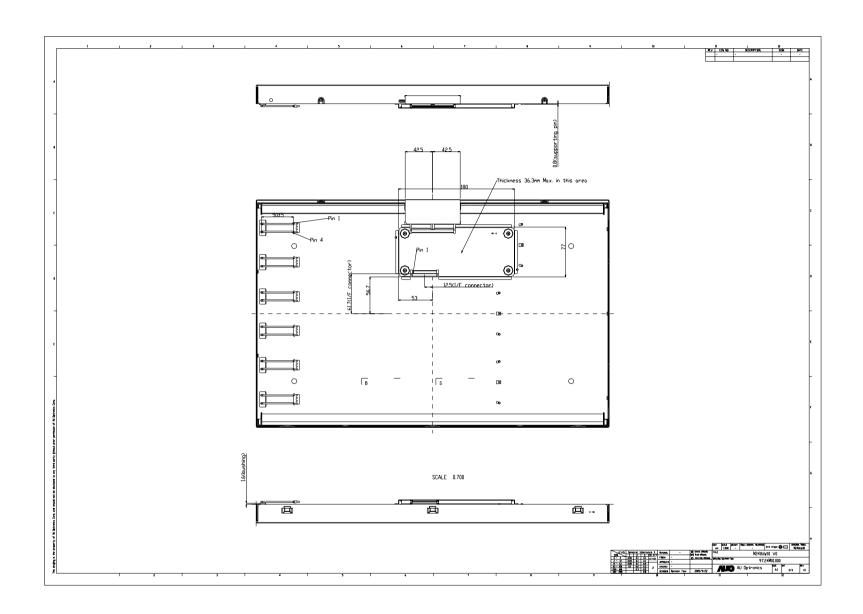
10.0 Mechanical Characteristics



Ver0.3 24/26



Ver0.3 25/26



Ver0.3 26/26