(V) Preliminary Specifications
( ) Final Specifications

Module	**10.1”(10.1”) WUXGA 16:10 Color TFT-LCD with LED Backlight design**
Model Name	**B101UAN01.A (H/W:1A)**
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
		YW Lee	04/01/2014
Checked & Approved by	**Date**	**Prepared by**	**Date**
		Maggie Yeh	05/09/2014
Note: This Specification is subject to change without notice.		**MPBU Marketing Division AU Optronics corporation**	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2014/05/09	All	First Edition		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B101UAN01.A is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 WUXGA, 1,920(H) x1,200(V) screen and 16.7M colors (RGB 6bits + Hi-FRC) with LED backlight driving circuit. All input signals are eDP interface compatible.

B101UAN01.A is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	256.42
Active Area	[mm]	216.81 X 135.50 typ
Pixels H x V		1,920x3(RGB) x 1,200
Pixel Pitch	[mm]	0.11292x 0.11292
Pixel Format		R.G.B. Vertical Stripe
Display Mode		AHVA, Normally Black
White Luminance Note: ILED is LED current)	[cd/m^2]	400 nits (typ), 340 nits (min)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		800 typ, 600 min
Response Time	[ms]	25 typ / 35 Max
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption (Column Inversion)	[Watt]	3.6W max. (with LED driver)
Weight	[Grams]	171g max

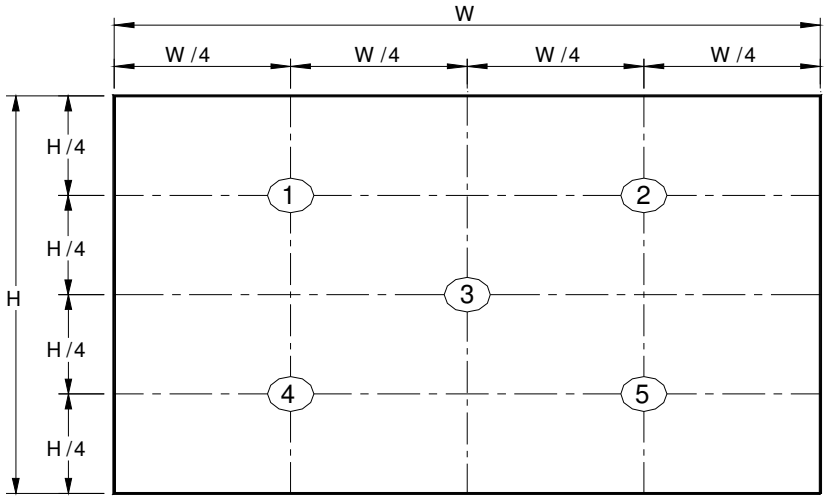
Physical Size	[mm]		Min.	Typ.	Max.
		Length	228.10	228.60	229.10
		Width	147.67	148.17	148.67
		Thickness	-	-	2.50 (Panel Side) 4.70 (PCBA Side)
Electrical Interface		40 pin eDP with LED driver			
Glass Thickness	[mm]	0.25			
Surface Treatment		Glare			
Support Color		16.7M colors (6 bits + Hi-FRC)			
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

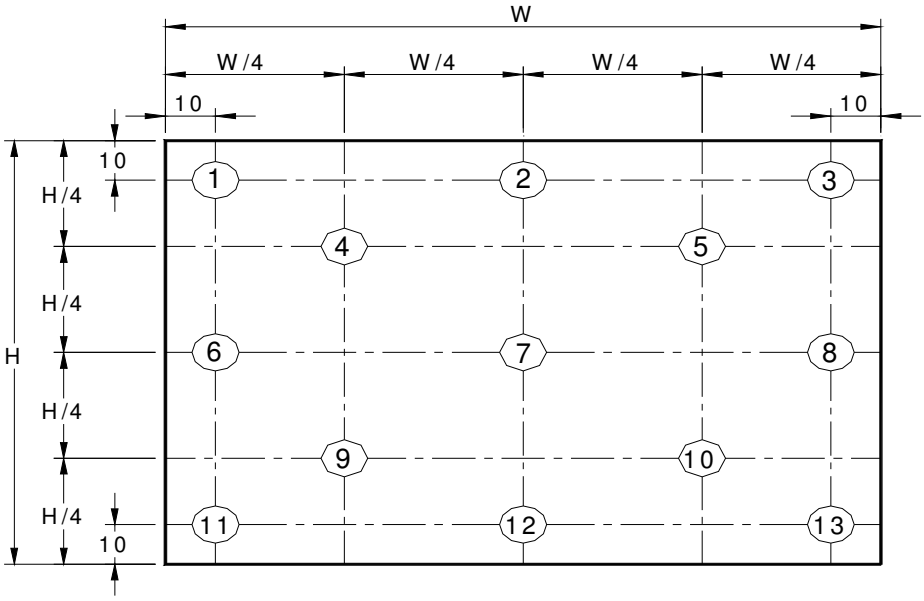
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=20mA (Base Panel Only)			5 points average	340	400	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10	80	85	-	degree	4, 9
		θ_L	(Left)	80	85	-		
		ψ_H	Vertical (Upper) CR = 10	80	85	-		
		ψ_L	(Lower)	80	85	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.5		2, 3, 4
Contrast Ratio		CR		600	800	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_r	Rising	-	15	20	msec	4, 8
		T_f	Falling	-	10	15		
		T_{RT}	Rising + Falling	-	25	35		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.567	0.597	0.627		4
		Ry		0.316	0.346	0.376		
	Green	Gx		0.292	0.322	0.352		
		Gy		0.550	0.580	0.610		
	Blue	Bx		0.120	0.150	0.180		
		By		0.096	0.126	0.156		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	50	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

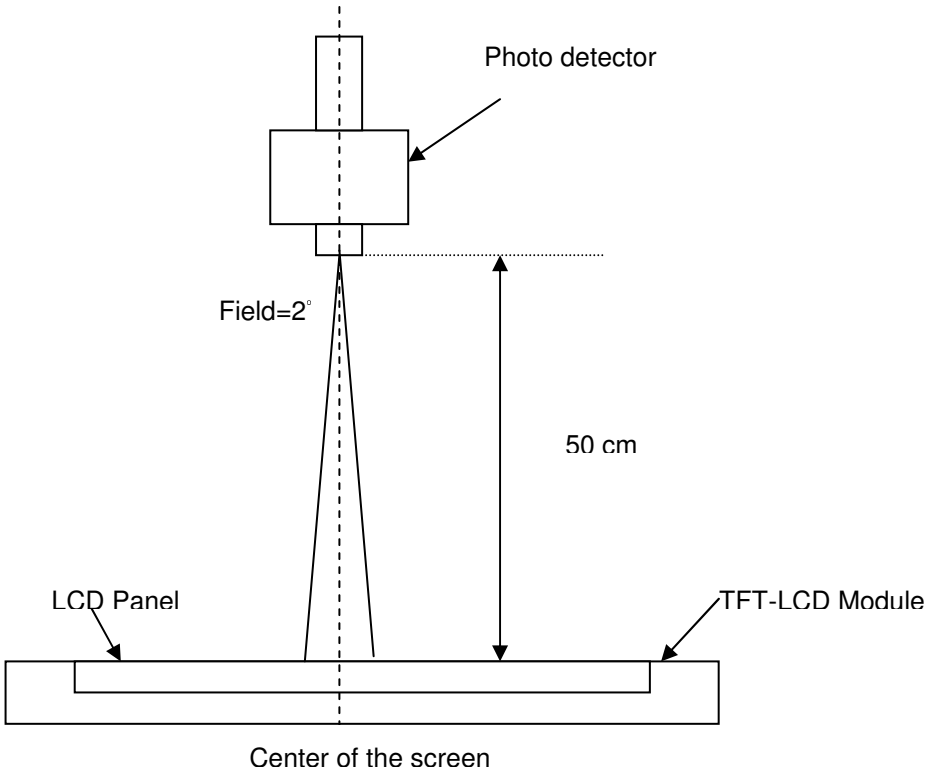
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

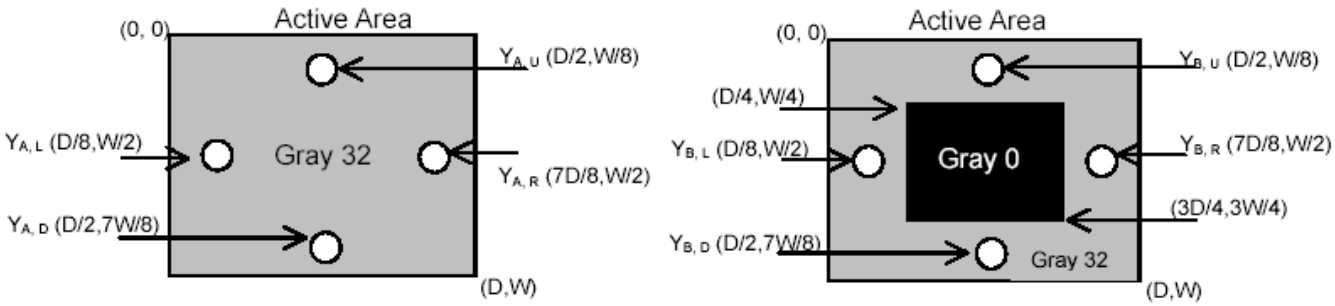
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where

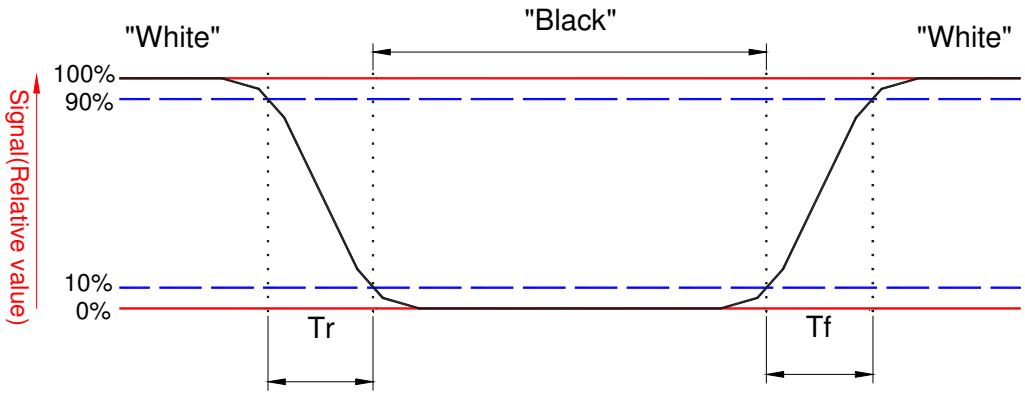
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



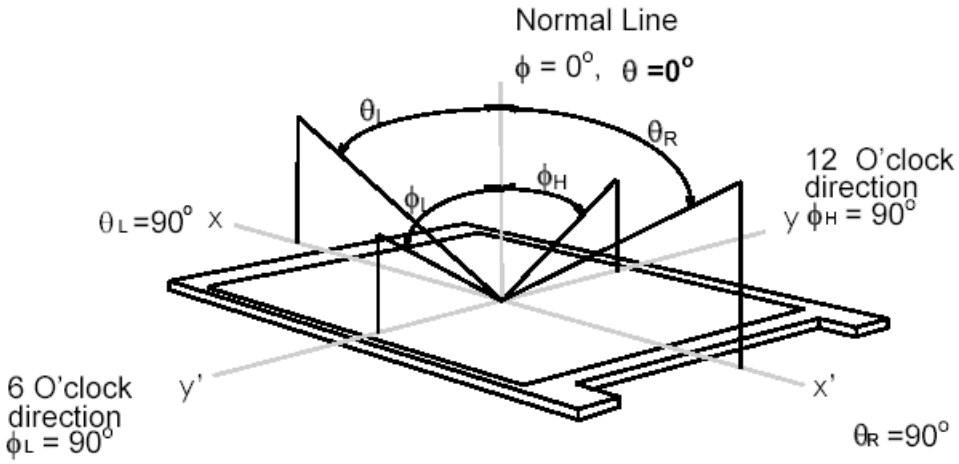
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



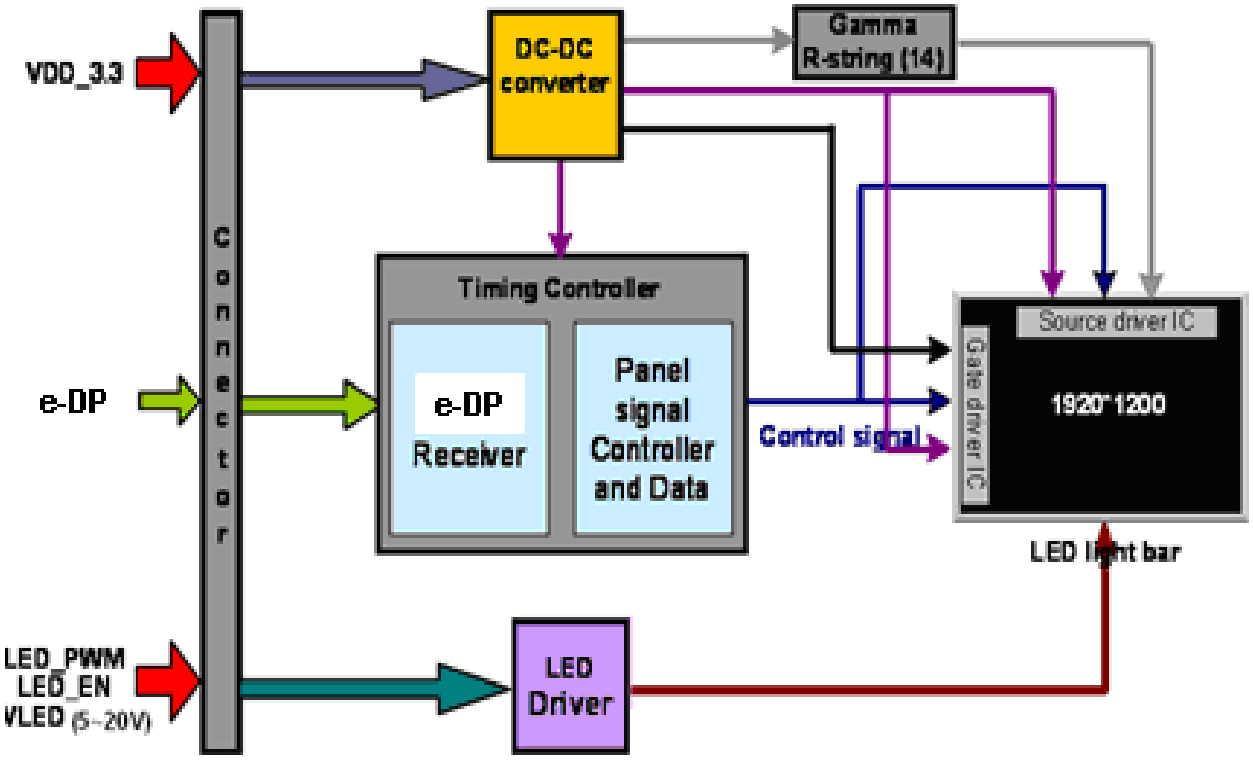
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 40 Pin two channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	-0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

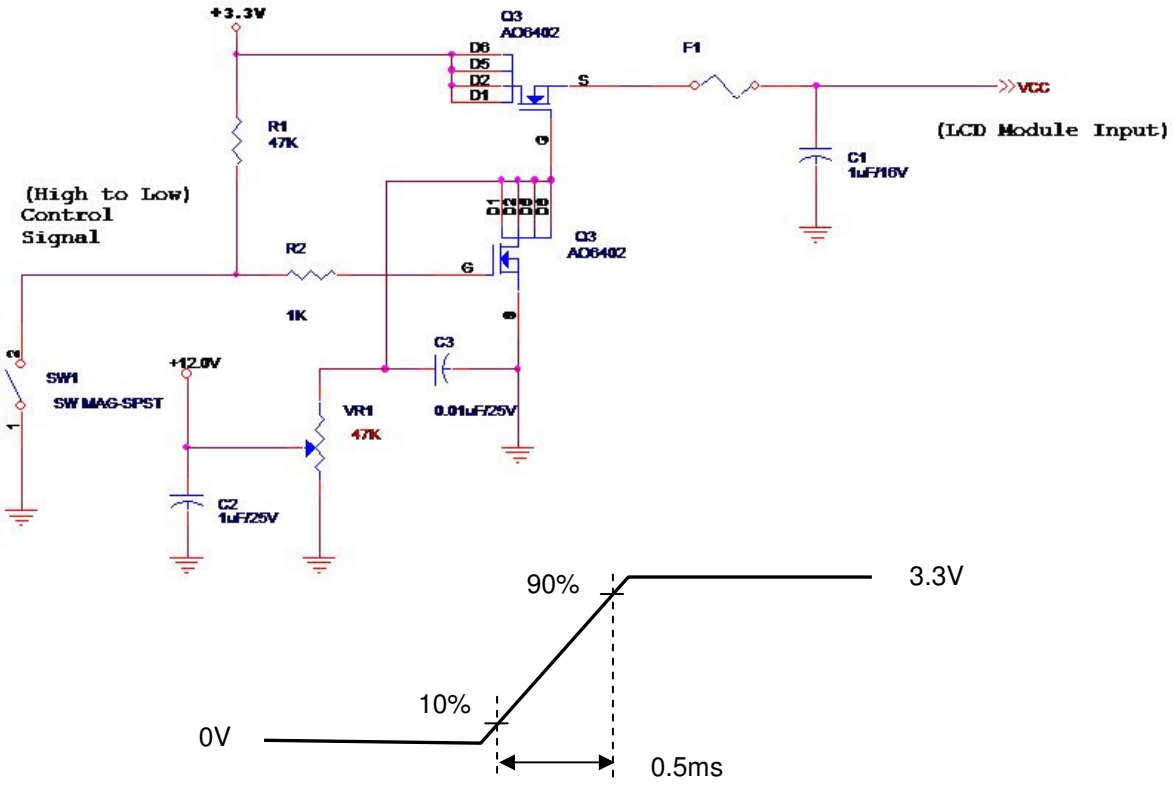
Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.15	[Watt]	Note 1
IDD	IDD Current	-	318	350	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{white}$)

Note 2 : Measure Condition



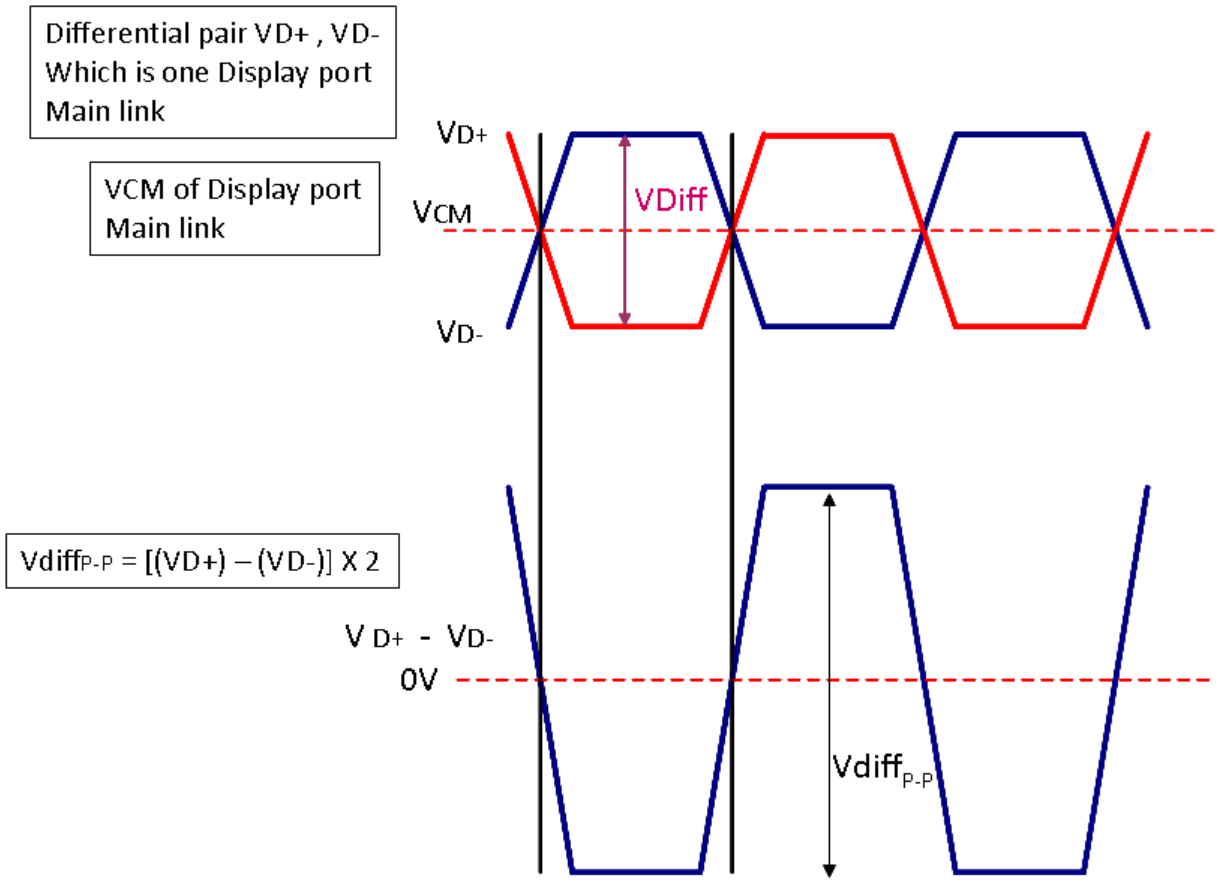
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

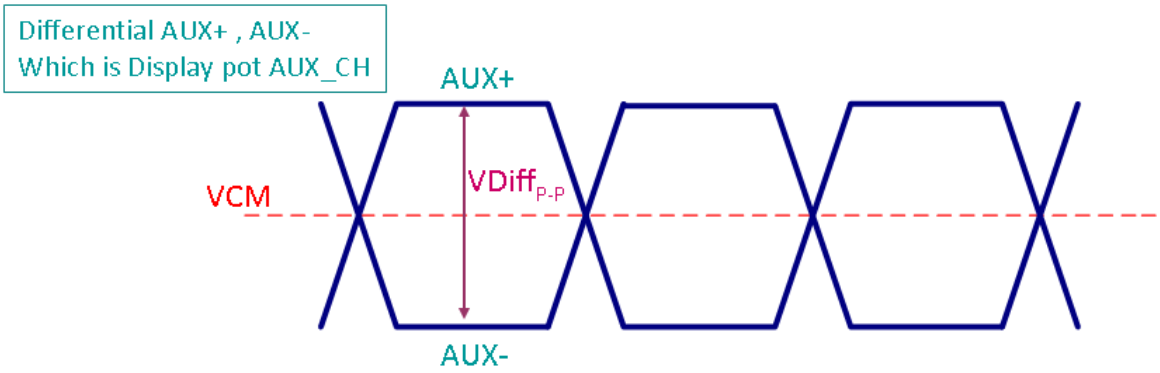
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Follow as VESA display port standard V1.3

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

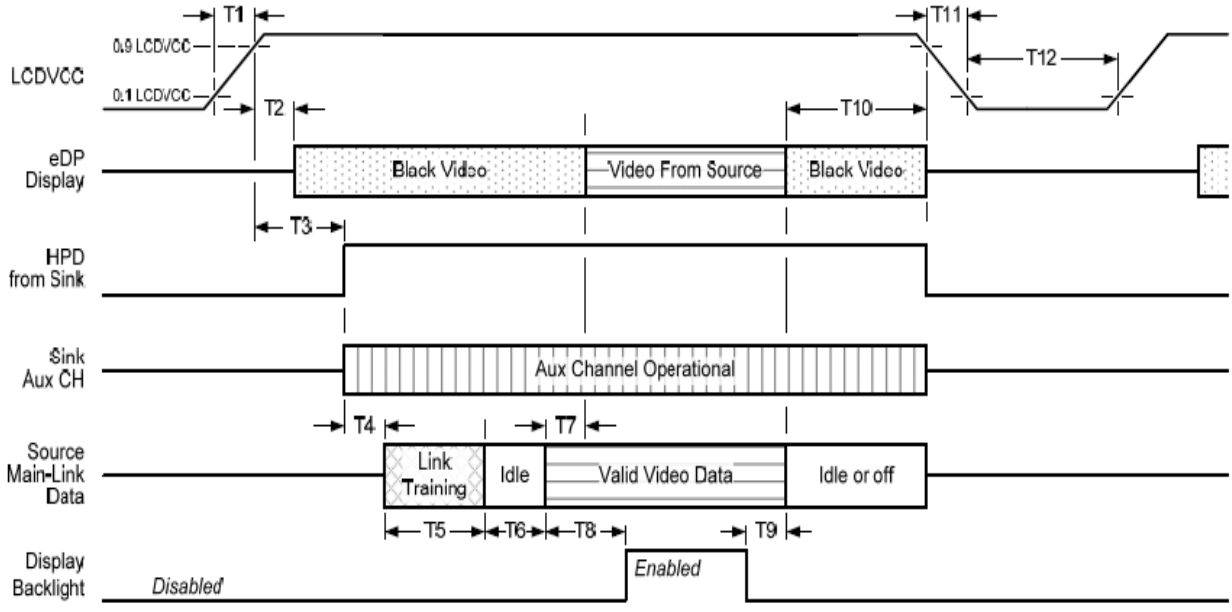
Follow as VESA display port standard V1.3.

Display Port V_{HPD} signal:

Display port V_{HPD}					
		Min	Typ	Max	unit
V_{HPD}	HPD Voltage	2.25		3.6	V

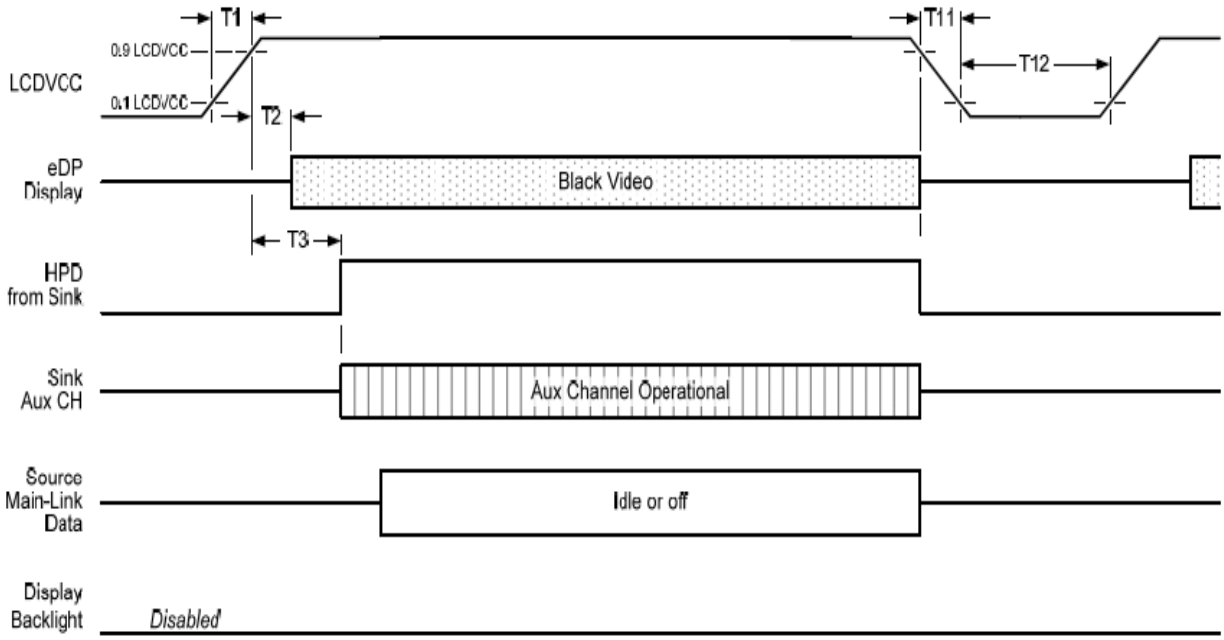
Follow as VESA display port standard V1.3

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

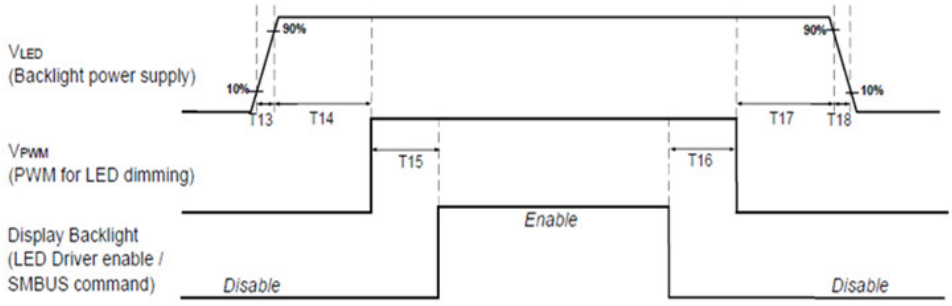
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

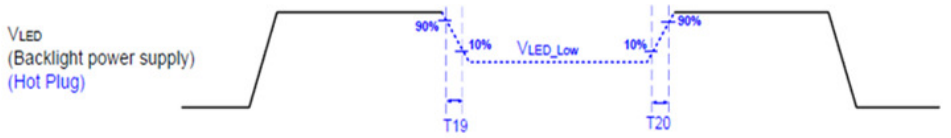
Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.45	[Watt]	(Ta=25℃), Note 1
LED Life-Time	N/A	15,000		-	Hour	(Ta=25℃), Note 2 I_F=20.5 mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency and depends on system LED driver design.

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

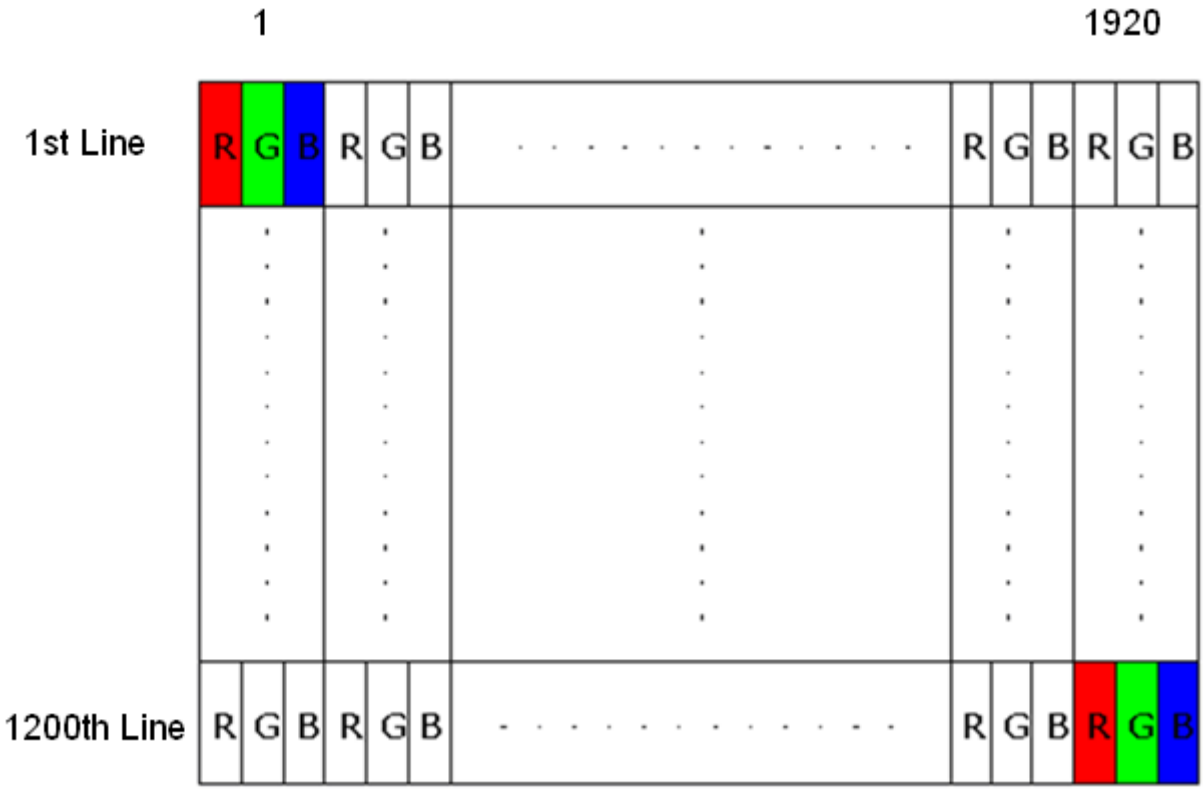
5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED (Note 1)	5		20	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	200		20K	Hz	
PWM Duty Ratio	Duty	5		100	%	

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

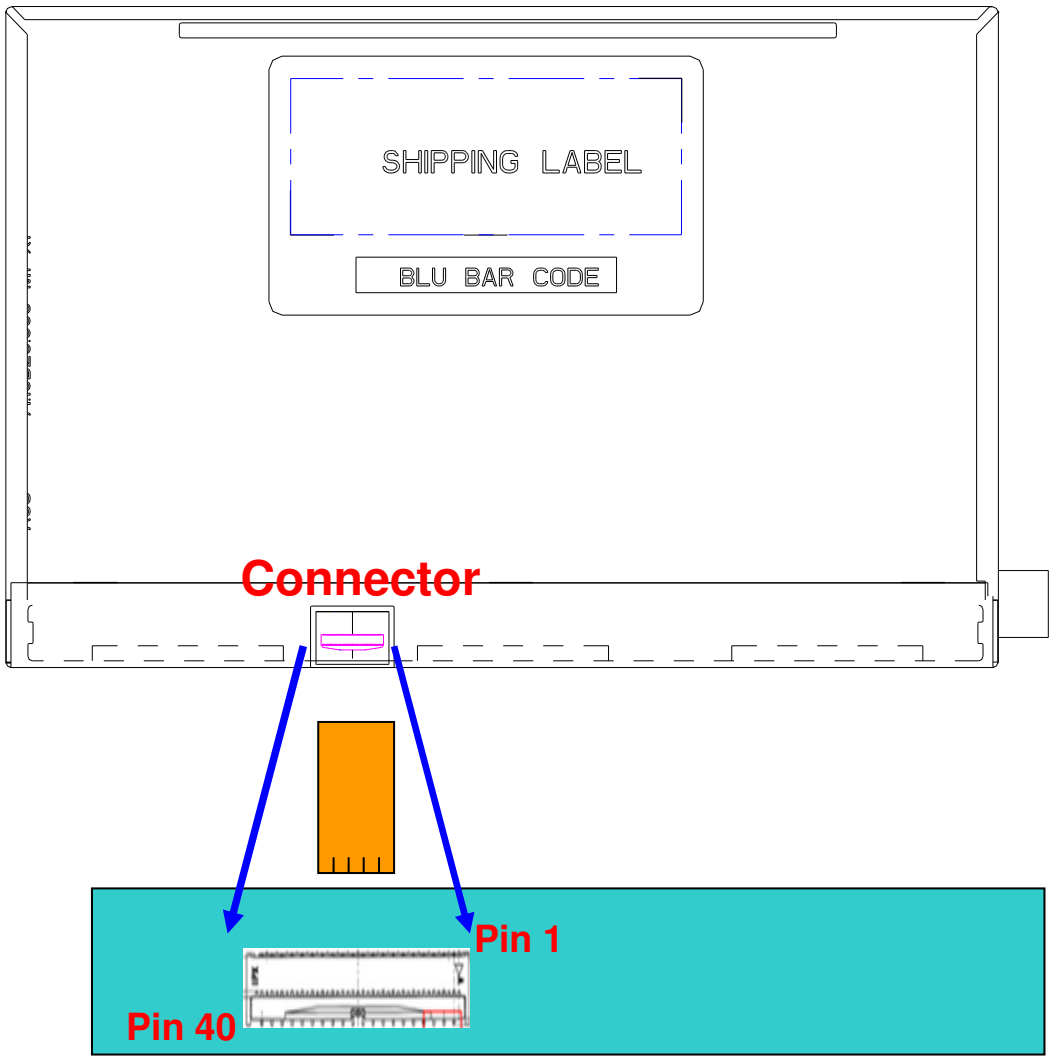
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	I_PEX or Compatible
Type / Part Number	20584-040E-01 or compatible
Mating Housing/Part Number	N/A

6.2.2 Pin Assignment

eDP is a differential signal technology for LCD interface and high speed data transfer device.

No.	Pin name	Description
1	H_GND	High Speed Ground
2	Lane1_N	Complement Signal Link Lane 1
3	Lane1_P	True Signal Link Lane 1
4	H_GND	High Speed Ground
5	Lane0_N	Complement Signal Link Lane 0
6	Lane0_P	True Signal Link Lane 0
7	H_GND	High Speed Ground
8	AUX_CH_P	True signal Auxiliary Channel
9	AUX_CH_N	Complement Signal Auxiliary Channel
10	H_GND	High Speed Ground
11	NC	No Connection
12	NC	No Connection
13	LCD_VCC	LCD logic and driver power
14	LCD_VCC	LCD logic and driver power
15	LCD_VCC	LCD logic and driver power
16	LCD_VCC	LCD logic and driver power
17	LCD_Self_Test or NC	LCD Panel Self-Test Enable (optional)
18	NC	No Connection
19	NC	No Connection
20	LCD_GND	LCD logic and driver ground
21	LCD_GND	LCD logic and driver ground
22	HPD	HPD signal pin
23	BL_GND	Backlight ground
24	BL_GND	Backlight ground
25	BL_GND	Backlight ground
26	BL_GND	Backlight ground
27	NC	No Connection
28	NC	No Connection
29	BL_ENABLE or NC	Backlight On/Off (optional)
30	BL_PWM_DIM or NC	System PWM singal input for dimming (optional)
31	NC	No Connection
32	NC	No Connection
33	NC-RESERVED	Reserved for LCD manufacturer's use
34	NC-RESERVED	Reserved for LCD manufacturer's use
35	NC	No Connection
36	NC	No Connection
37	BL_PWR	Backlight power
38	BL_PWR	Backlight power
39	BL_PWR	Backlight power
40	BL_PWR	Backlight power


SHIPPING LABEL
BLU BAR CODE
Connector
Pin 1
Pin 40

6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1200 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	--	60	---	Hz
Clock frequency		$1/T_{Clock}$		TBD		MHz
Vertical Section	Period	T_V	1087	TBD	1200	T_{Line}
	Active	T_{VD}	1200			
	Blanking	T_{VB}	4	TBD	2000	
Horizontal Section	Period	T_H	2040	TBD	2500	T_{Clock}
	Active	T_{HD}	1920			
	Blanking	T_{HB}	80	TBD	400	

Note1 : DE mode only

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta=0℃, 300h	
High Temperature Storage	Ta= 60℃, 300h	
Low Temperature Storage	Ta= -20℃, 300h	
Thermal Shock Test	Ta=-20℃(30min) ~60℃(30min), 100cycles condition.	
ESD	Contact : ±8 KV Air : ±15 KV	**Note 1**

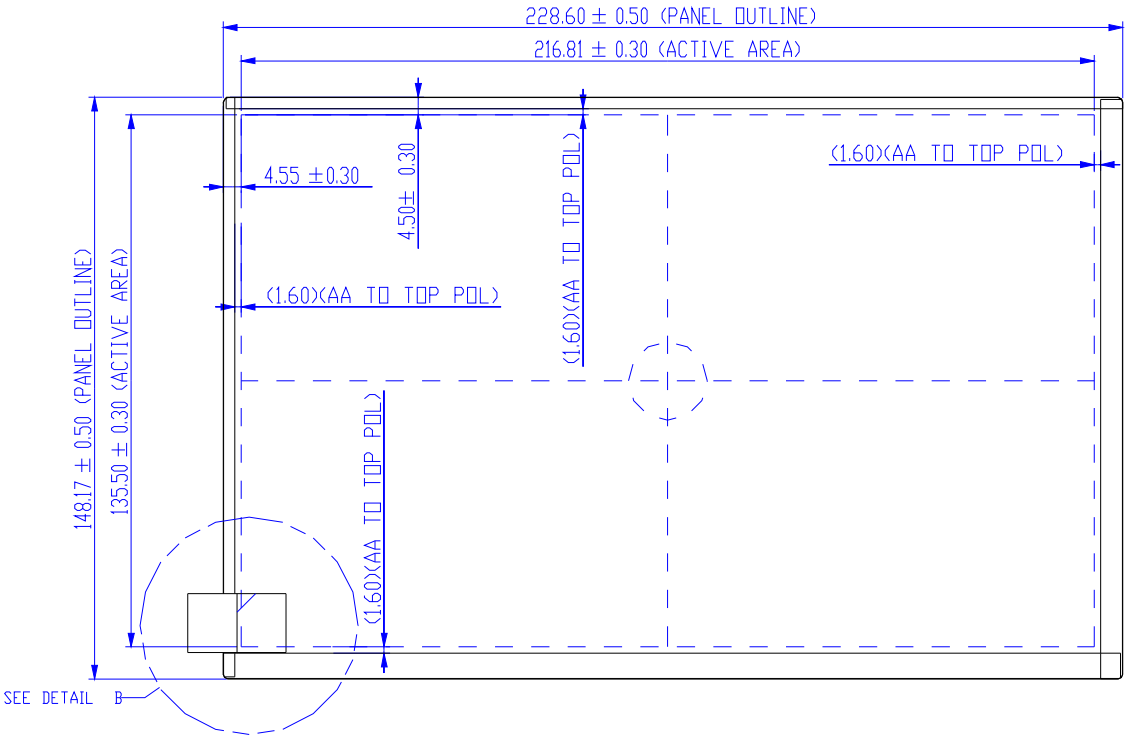
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

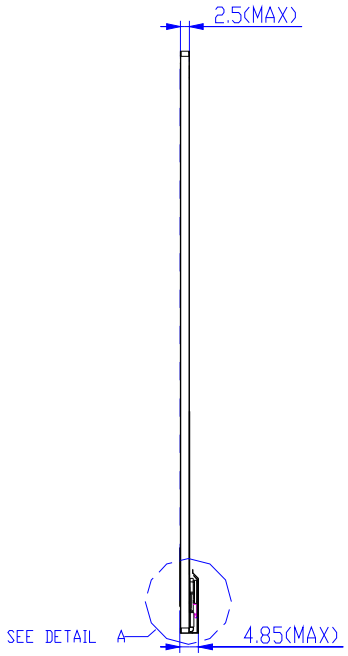
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

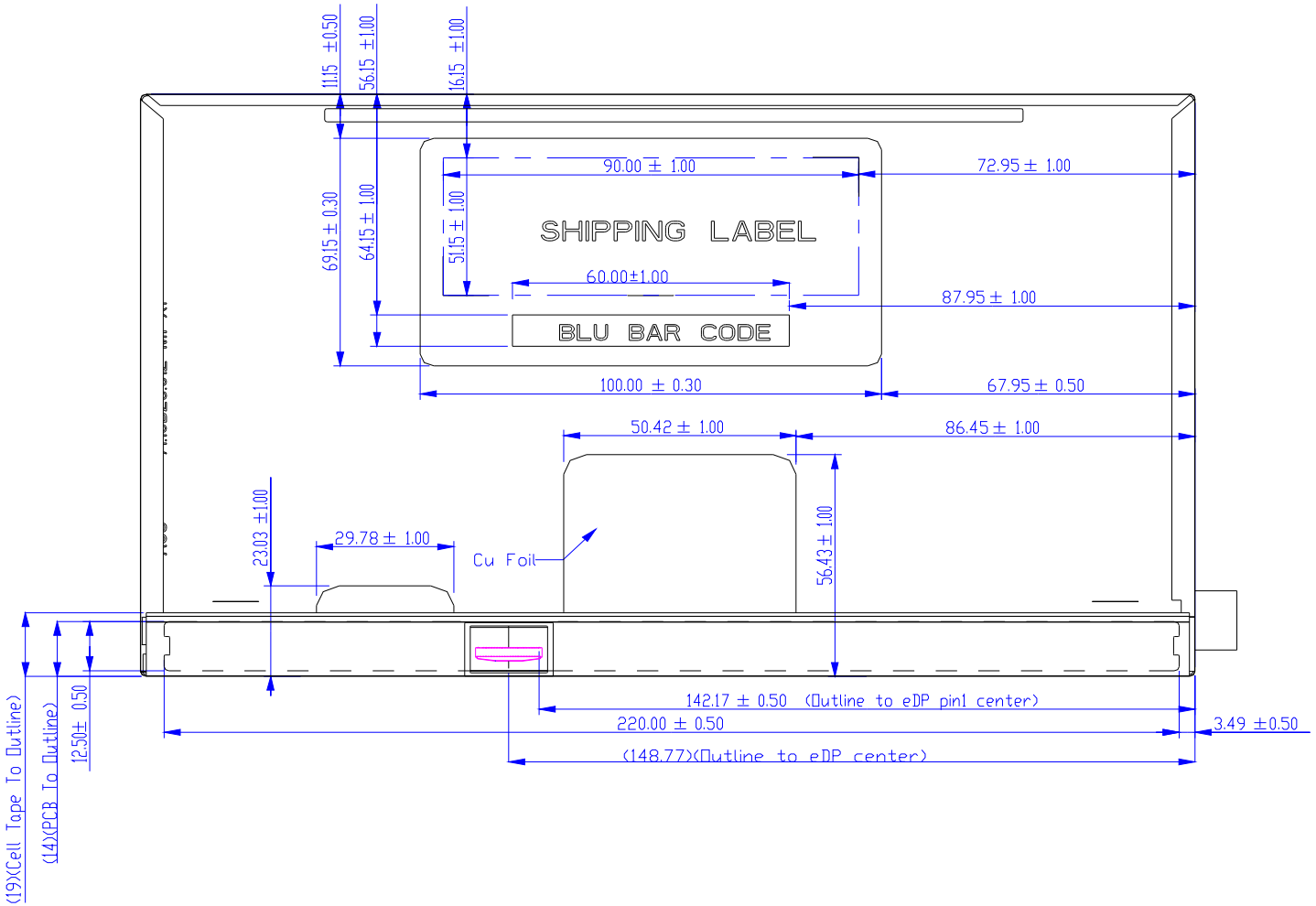
8.1 LCM Outline Dimension

8.1.1 Front View



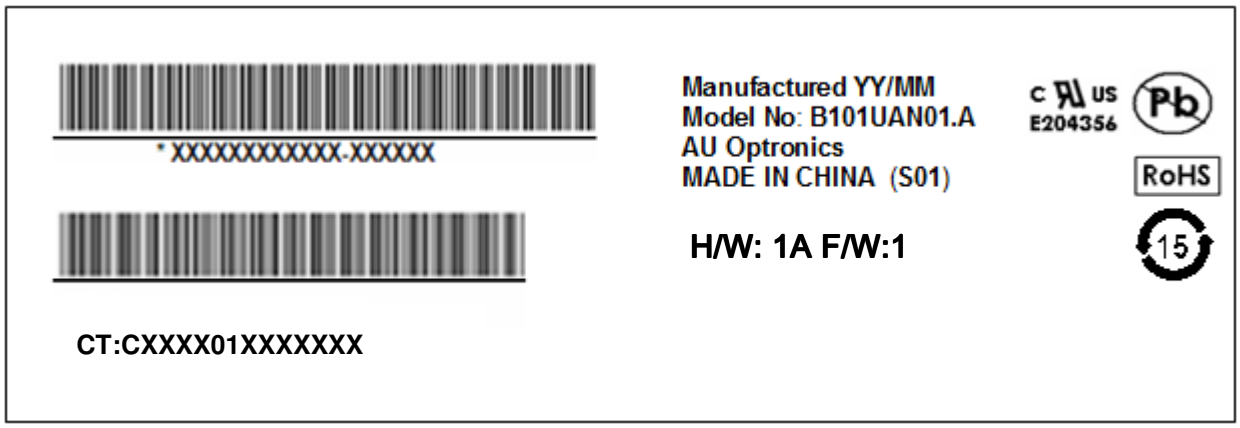


8.1.2 Rear View

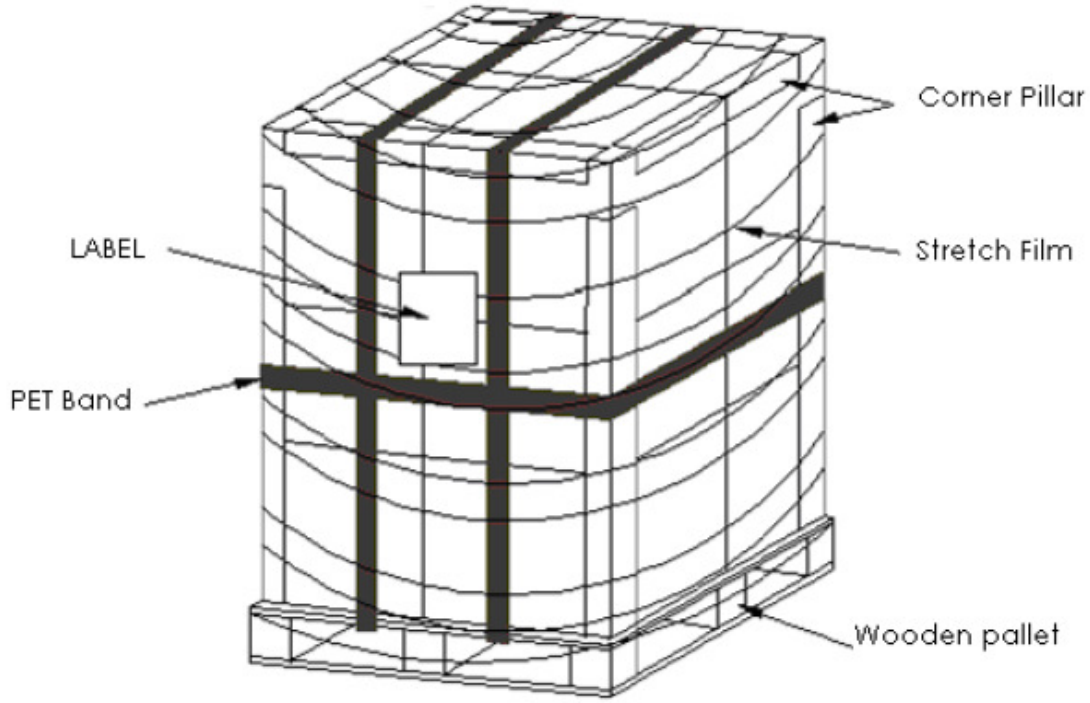


9. Shipping and Package

9.1 Shipping Label Format



9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	D8	11011000	216
0B	hex, LSB first	1A	00011010	26
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	00	00000000	0
11	Year of manufacture	17	00010111	23
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	04	00000100	4
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	A5	10100101	165
15	**Max H image size** *(rounded to cm)*	16	00010110	22
16	**Max V image size** *(rounded to cm)*	0E	00001110	14
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2
19	Red/green low bits **(Lower 2:2:2:2 bits)**	98	10011000	152
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	25	00100101	37
1B	Red x **(Upper 8 bits)**	99	10011001	153
1C	Red y/ highER 8 bits	58	01011000	88
1D	Green x	54	01010100	84
1E	Green y	8E	10001110	142
1F	Blue x	27	00100111	39
20	Blue y	1E	00011110	30
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1

2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	8E	10001110	142
37	Pixel Clock/10000 USB	3A	00111010	58
38	Horz active **Lower 8bits**	80	10000000	128
39	Horz blanking **Lower 8bits**	90	10010000	144
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	70	01110000	112
3B	Vertical Active **Lower 8bits**	B0	10110000	176
3C	Vertical Blanking **Lower 8bits**	0A	00001010	10
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40	01000000	64
3E	HorzSync. Offset	2C	00101100	44
3F	HorzSync.Width	20	00100000	32
40	VertSync.Offset : VertSync.Width	35	00110101	53
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0
42	Horizontal Image Size **Lower 8bits**	D8	11011000	216
43	Vertical Image Size **Lower 8bits**	88	10001000	136
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	00	00000000	0
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0
46	Vertical Border *(zero for internal LCD)*	00	00000000	0
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24
48	Pixel Clock/10,000 (LSB)	09	00001001	9
49	Pixel Clock/10,000 (MSB)	27	00100111	39
4A	Horizontal Addressable Pixels, lower 8 bits	80	10000000	128
4B	Horizontal Blanking Pixels, lower 8 bits	90	10010000	144
4C	H Pixels, upper nibble : H Blanking, upper nibble	70	01110000	112
4D	Vertical Addressable Lines, lower 8 bits	B0	10110000	176
4E	Vertical Blanking Lines, lower 8 bits	0A	00001010	10
4F	V lines, upper nibble : V blanking, upper nibble	40	01000000	64
50	Horizontal Front Porch, lower 8 bits	2C	00101100	44
51	Horizontal Sync Pulse, lower 8 bits	20	00100000	32
52	V Front Porch, lower nibble : V Sync Pulse, lower nibble	35	00110101	53
53	VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits	00	00000000	0
54	Horizontal Image Size in mm, lower 8 bits	D8	11011000	216
55	Vertical Image Size in mm, lower 8 bits	88	10001000	136
56	H Image Size, upper nibble : V Image Size, upper nibble	00	00000000	0
57	Horizontal Border	00	00000000	0
58	Vertical Border	00	00000000	0
59	Bit Encode Sync Information	18	00011000	24
5A	DC	00	00000000	0
5B	HTOTAL	00	00000000	0
5C	HA	00	00000000	0
5D	HBL	00	00000000	0

5E	HFP	00	00000000	0
5F	HFPe	00	00000000	0
60	HBP	00	00000000	0
61	HB	00	00000000	0
62	HSO	00	00000000	0
63	HS	00	00000000	0
64	VTOTAL	00	00000000	0
65	VA	00	00000000	0
66	VBL	00	00000000	0
67	VFP	00	00000000	0
68	VBP	00	00000000	0
69	VB	00	00000000	0
6A	VSO	00	00000000	0
6B	VS	00	00000000	0
6C	Detail Timing Description #4	00	00000000	0
6D	Flag	00	00000000	0
6E	Reserved	00	00000000	0
6F	For Brightness Table and Power Consumption	02	00000010	2
70	Flag	00	00000000	0
71	PWM % [7:0] @ Step 0	01	00000001	1
72	PWM % [7:0] @ Step 5	26	00100110	38
73	PWM % [7:0] @ Step 10	FF	11111111	255
74	Nits [7:0] @ Step 0	01	00000001	1
75	Nits [7:0] @ Step 5	3C	00111100	60
76	Nits [7:0] @ Step 10	C8	11001000	200
77	Panel Electronics Power @ 32x32 Chess Pattern =	16	00010110	22
78	Backlight Power @ 60 nits =	08	00001000	8
79	Backlight Power @ Step 10 =	1E	00011110	30
7A	Nits @ 100% PWM Duty =	C8	11001000	200
7B	Flag	20	00100000	32
7C	Flag	20	00100000	32
7D	Flag	20	00100000	32
7E	Extension Flag	00	00000000	0
7F	Checksum	08	00001000	8