Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications
(✓) Final Specifications

Module	**15.6" (15.6) UHD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	B156ZAN03.1 (H/W:0A)
Note (💡)	*LED Backlight with driving circuit design*

Customer	**Date**
____________	____________
Checked & Approved by	**Date**
____________	____________

Note: This Specification is subject to change without notice.

Approved by	**Date**
Buffy Chen	_2017/07/26_
Prepared by	**Date**
Eric DC Liu	*2017/07/26*

NBBU Marketing Division
AU Optronics corporation

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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2017/05/26	All	First Edition for Customer		
1.0 2017/07/26	All		Final Edition for Customer	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electronic breakdown.

2. General Description

B156ZAN03.1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 UHD, 3840(H) x2160(V) screen and 16.7M colors (RGB 8-bits data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B156ZAN03.1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

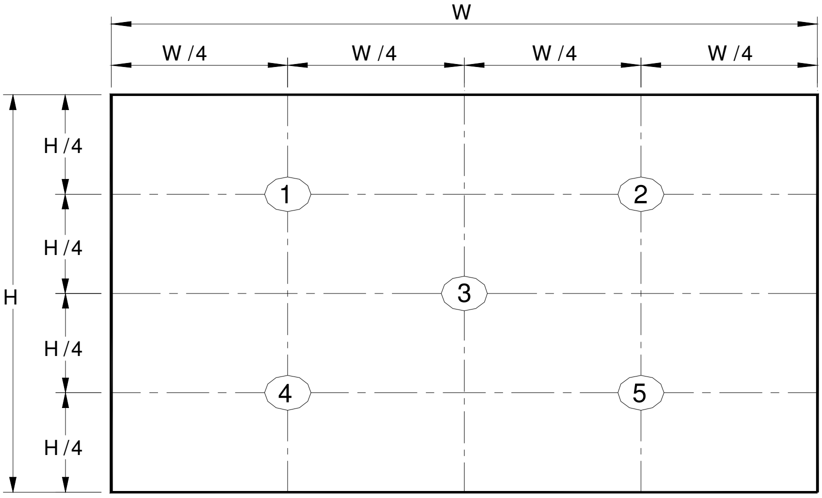
Items	**Unit**	**Specifications**			
Screen Diagonal	[mm]	15.6			
Active Area	[mm]	344.2176x193.6224			
Pixels H x V		3840 x 3(RGB) x 2160			
Pixel Pitch	[mm]	0.08964 x 0.08964			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (ILED= 20 mA) **(Note: ILED is LED current)**	[cd/m^2]	400 typ. (5 points average) 340 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		1200:1 typ			
Response Time	[ms]	30 Typ,			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	7.7W			
Weight	[Grams]	320 max.			
Physical Size **Include bracket**	[mm]		Min.	Typ.	Max.
		Length	347.92	348.22	348.52
		Width	214.71	215.21	215.71
Thicknessss		Thicknessss	2.6 max		
Electrical Interface		4 Lane eDP1.4a (5.4G)			
Glass Thickness	[mm]	0.3			
Surface Treatment		Anti-Glare			
Support Color		16.7M colors (RGB 8-bit)			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

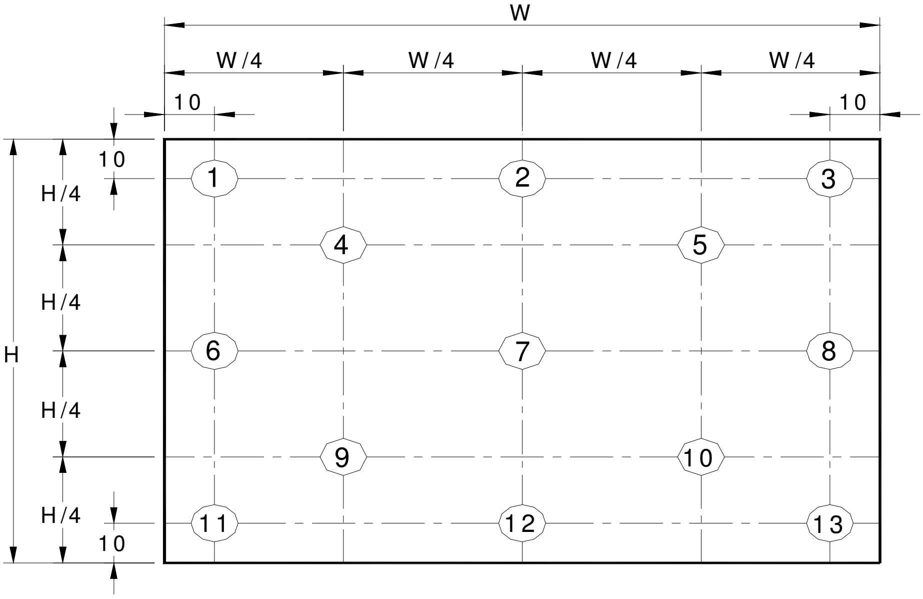
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=20 mA			5 points average	340	400	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right)	80	85	-	degree	4, 9
		θ_L	CR = 10 (Left)	80	85	-		
		ψ_H	Vertical (Upper)	80	85	-		
		ψ_L	CR = 10 (Lower)	80	85	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio		CR		800	1200	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_{RT}	Rising + Falling	-	30	35		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.621	0.651	0.681		4
		Ry		0.298	0.328	0.358		
	Green	Gx		0.176	0.206	0.236		
		Gy		0.683	0.713	0.743		
	Blue	Bx		0.116	0.146	0.176		
		By		0.028	0.058	0.088		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
Adobe		%		-	100	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



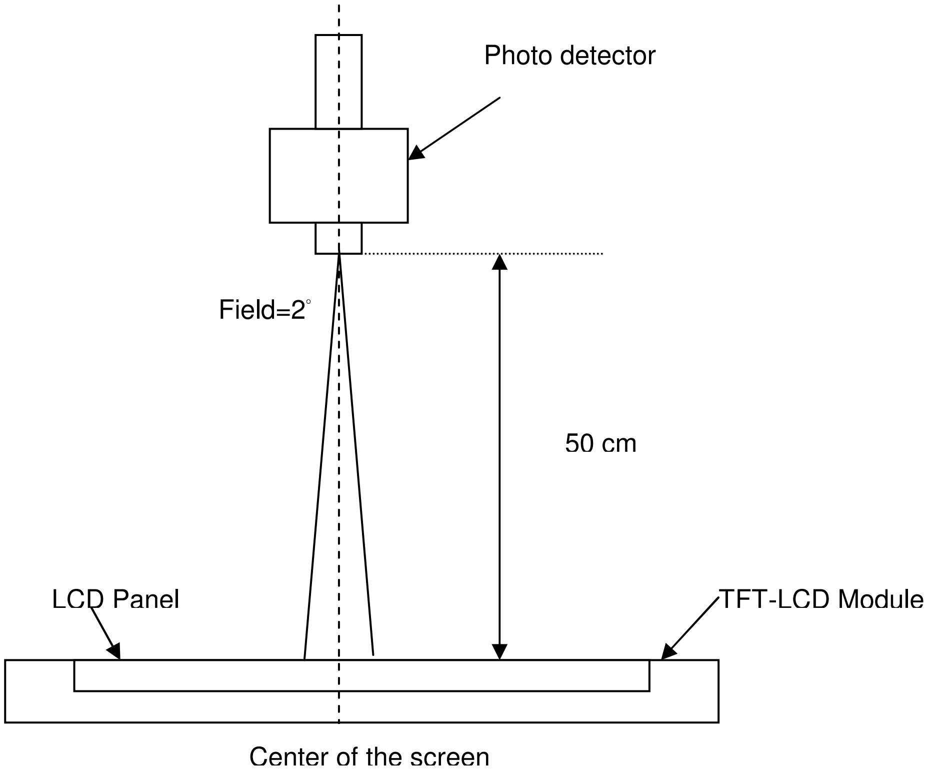
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

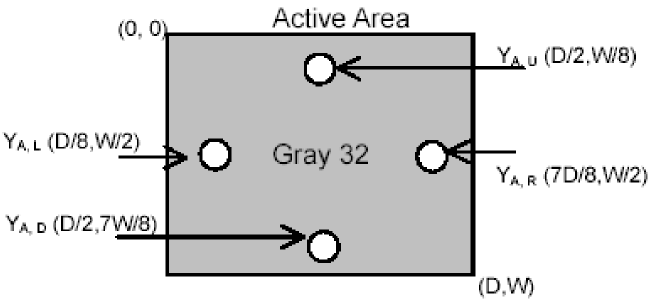
Note 7： Definition of Cross Talk (CT)

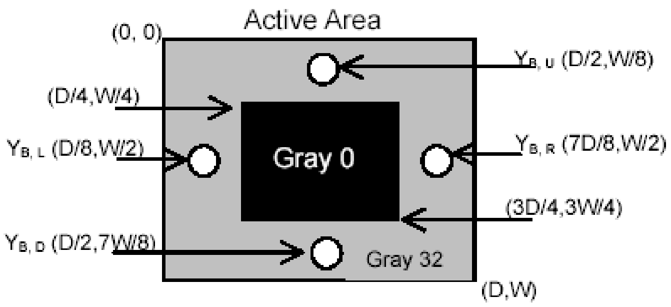
CT = | YB – YA | / YA × 100 (%)

Where

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

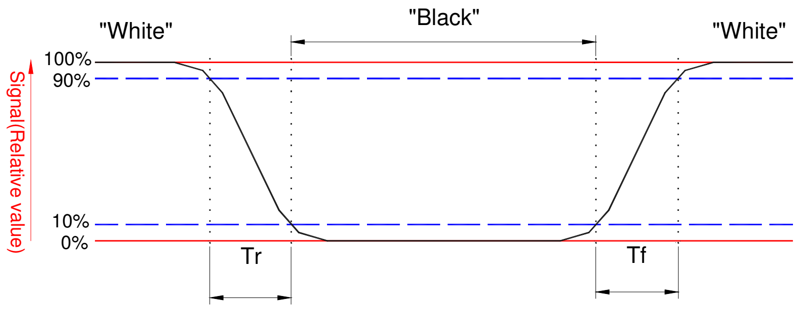
YB = Luminance of measured location with gray level 0 pattern (cd/m2)


Active Area
(0, 0)
YA, U (D/2,W/8)
YA, L (D/8,W/2)
Gray 32
YA, R (7D/8,W/2)
YA, D (D/2,7W/8)
(D,W)


Active Area
(0, 0)
YB, U (D/2,W/8)
(D/4,W/4)
YB, L (D/8,W/2)
Gray 0
YB, R (7D/8,W/2)
(3D/4,3W/4)
YB, D (D/2,7W/8)
Gray 32
(D,W)

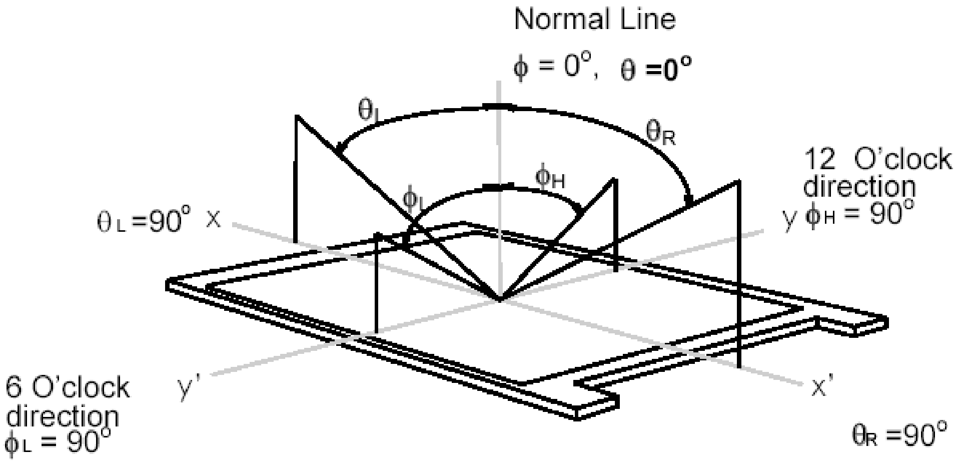
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



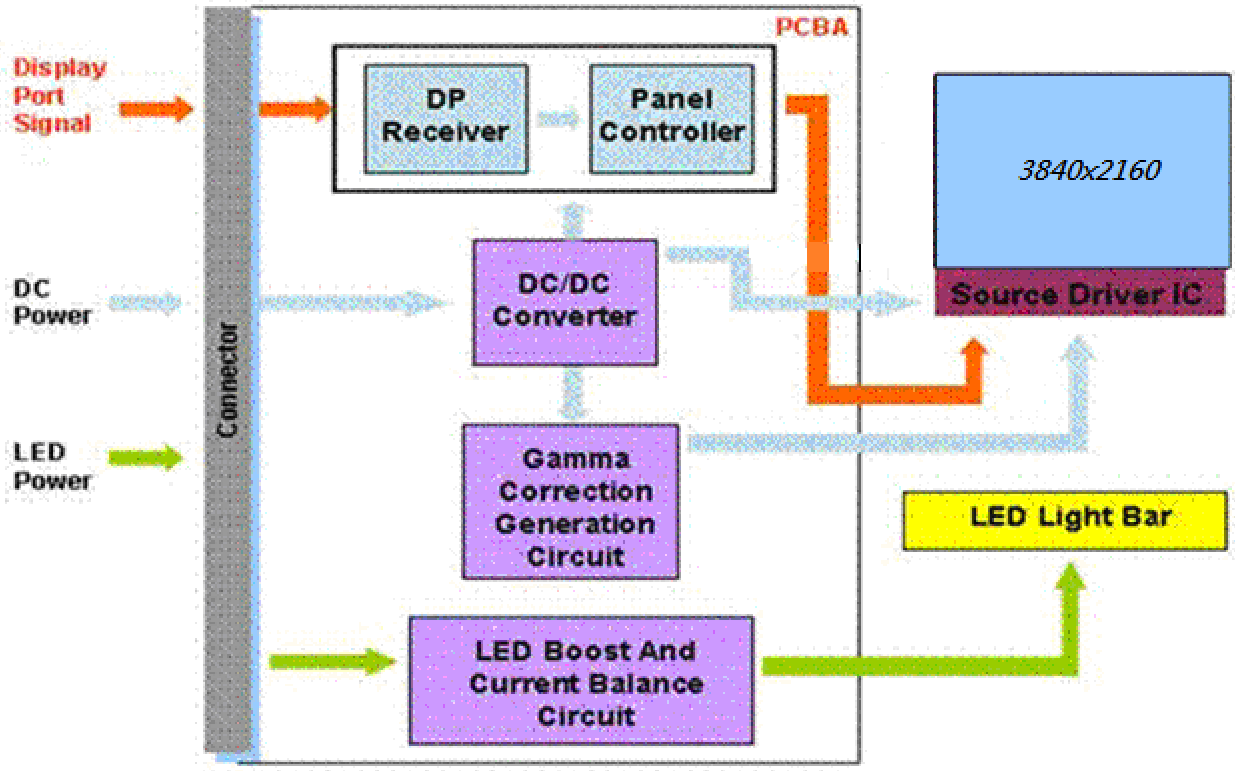
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.


Normal Line
$\phi = 0^\circ$, $\theta = 0^\circ$
θ_L
θ_R
ϕ_H
ϕ_L
12 O'clock direction
y $\phi_H = 90^\circ$
$\theta_L = 90^\circ$ x
6 O'clock direction
$\phi_L = 90^\circ$
y'
x'
$\theta_R = 90^\circ$

3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 40 Pin (One CH/connector Module)


Display Port Signal
DC Power
LED Power
Connector
PCBA
DP Receiver
Panel Controller
DC/DC Converter
Gamma Correction Generation Circuit
LED Boost And Current Balance Circuit
3840x2160
Source Driver IC
LED Light Bar

4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

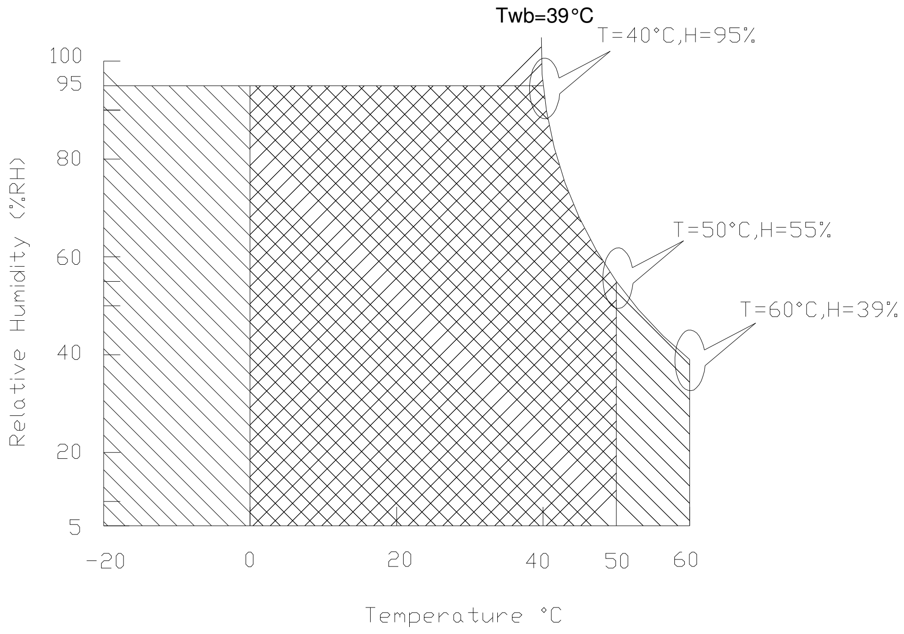
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range ▩   Storage Range ▩ + ▧

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

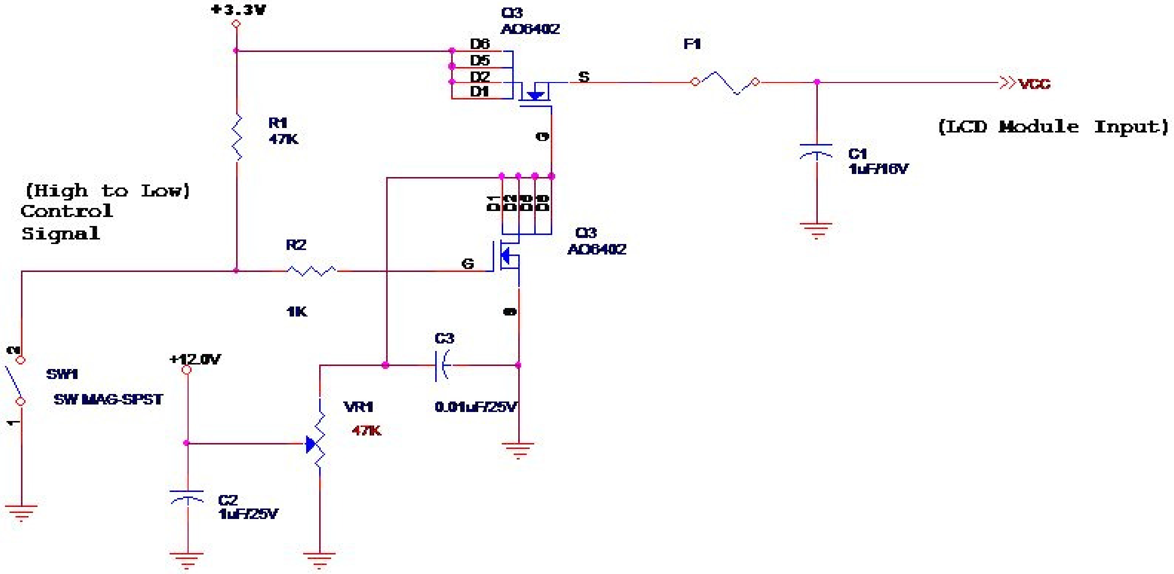
Input power specifications are as follows;

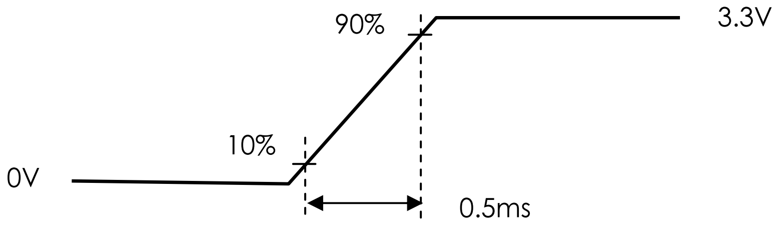
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.9	[Watt]	Note 1
IDD	IDD Current	-	-	633	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Mosaic pattern (PDD (max) = VDD(min) x IDD(max))

Note 2：Measure Condition


+3.3V
Q3
AO6402
D6
D5
D2
D1
S
F1
VCC
(LCD Module Input)
R1
47K
C1
1uF/16V
(High to Low)
Control
Signal
R2
1K
G
Q3
AO6402
C3
0.01uF/25V
SW1
SW MAG-SPST
+12.0V
VR1
47K
C2
1uF/25V

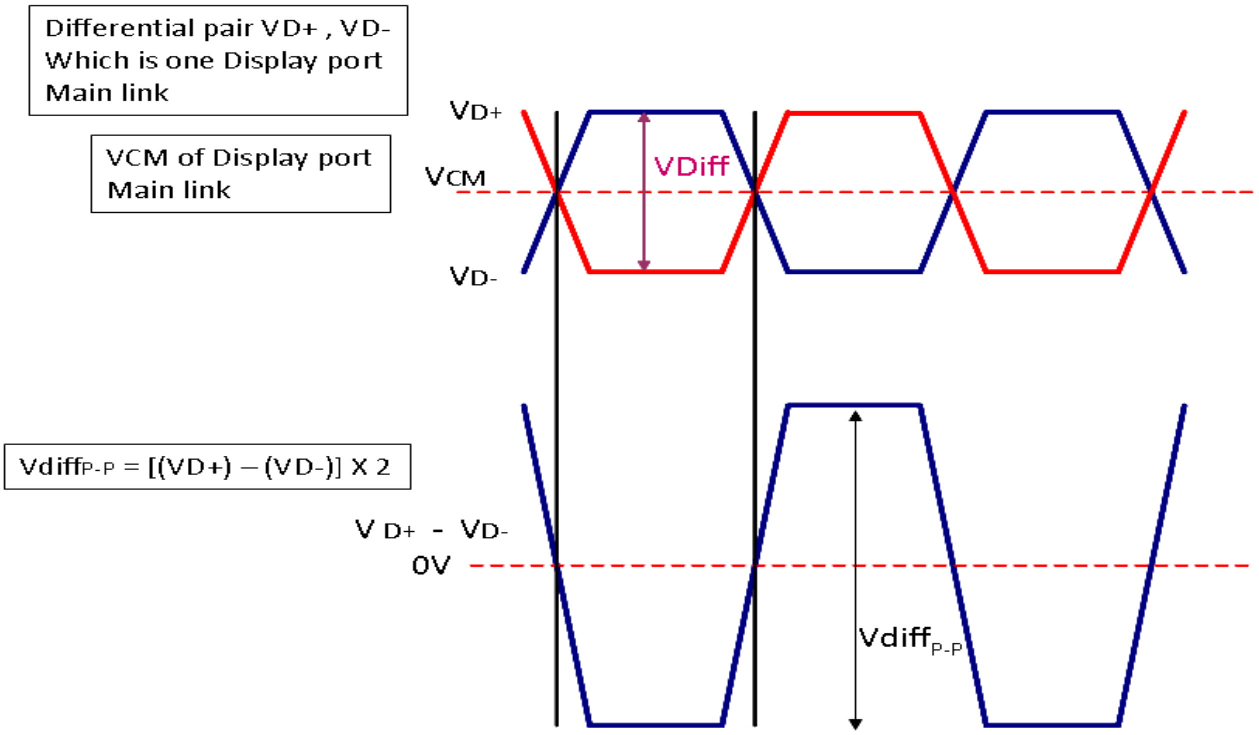


Vin rising time

5.1.2 Signal Electrical Characteristics

Signal electrical characteristics are as follows;

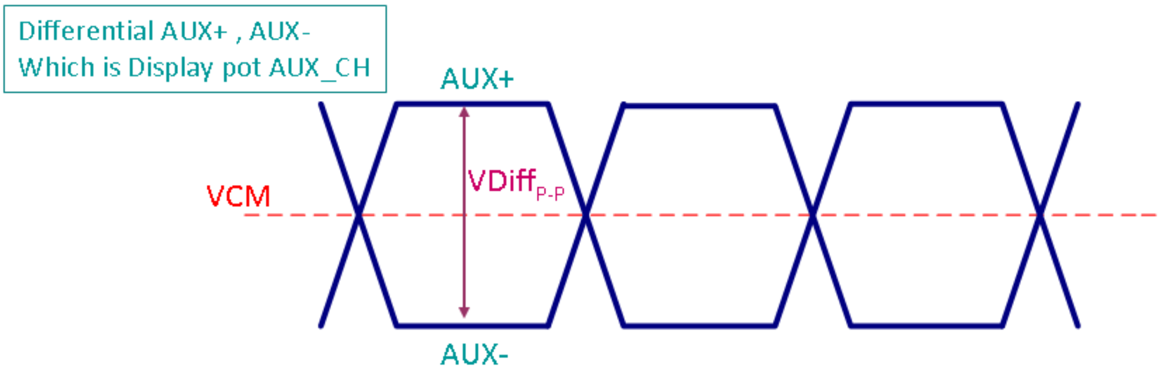
Display Port main link signal:


Differential pair VD+ , VD- Which is one Display port Main link
VCM of Display port Main link
VD+
VCM
VD-
VDiff
Vdiff$_{P-P}$ = [(VD+) – (VD-)] X 2
V D+ - VD-
0V
Vdiff$_{P-P}$

Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff$_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Follow as VESA display port standard V1.1a

Display Port AUX_CH signal:


Differential AUX+ , AUX- Which is Display pot AUX_CH
AUX+
VCM
VDiff$_{P-P}$
AUX-

Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Follow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	-	3.6	V

Follow as VESA display port standard V1.1a.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	5.8	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=20mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

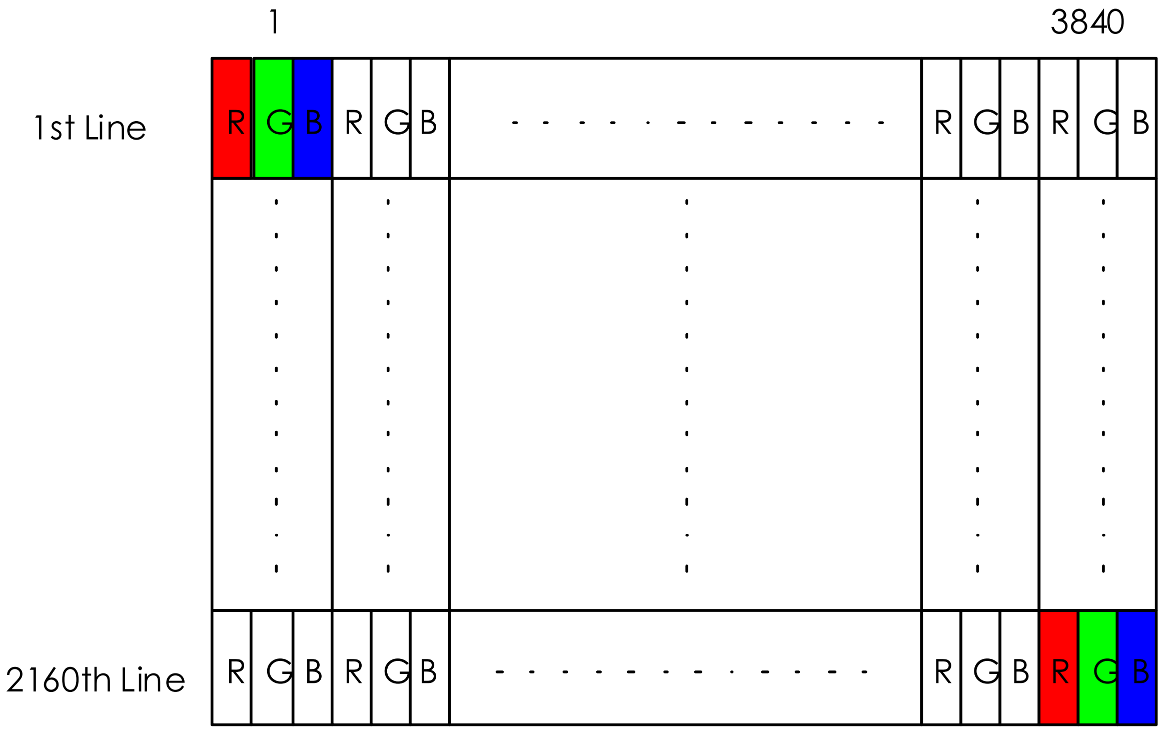
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	9.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN *Note 1	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN *Note 1	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.


1
3840
1st Line
2160th Line
R
G
B

6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	I-PEX or compatible
Type / Part Number	IPEX 20455-040E-12R or compatible
Mating Housing/Part Number	I-PEX 20453-040T-01 or compatible

6.2.2 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	No Connect (Reserved)
2	H_GND	High Speed Ground
3	Lane3_N	Comp Signal Lane3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Comp Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Comp Signal Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Comp Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Ch.
16	AUX_CH_N	Comp Signal Auxiliary Ch.
17	H_GND	High Speed Ground
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	LCD_Self_Test or NC	LCD Panel Self Test Enable (Optional)
23	LCD GND	LCD logic and driver ground
24	LCD GND	LCD logic and driver ground

25	LCD GND	LCD logic and driver ground
26	LCD GND	LCD logic and driver ground
27	HPD	HPD signale pin
28	BL_GND	Backlight_ground
29	BL_GND	Backlight_ground
30	BL_GND	Backlight_ground
31	BL_GND	Backlight_ground
32	BL_Enable	Backlight On / Off
33	BL PWM DIM	System PWM signal Input
34	NC	NC
35	NC	No connect (Reverse for AUO TEST only)
36	BL_PWR	Backlight power (9V~21V)
37	BL_PWR	Backlight power (9V~21V)
38	BL_PWR	Backlight power (9V~21V)
39	BL_PWR	Backlight power (9V~21V)
40	NC	No Connect

Note1：start from right side
Note2：Input signals shall be low or High-impedance state when VDD is off.

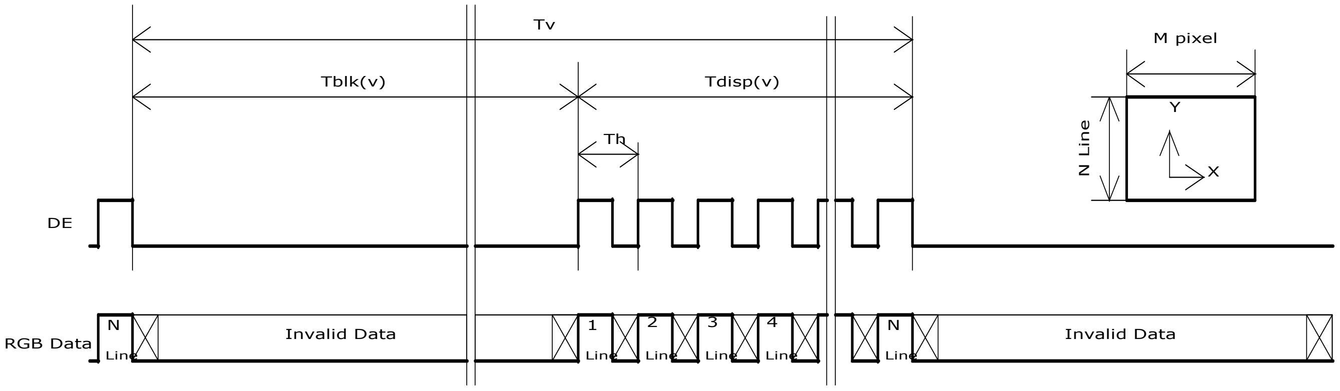
6.3 Interface Timing

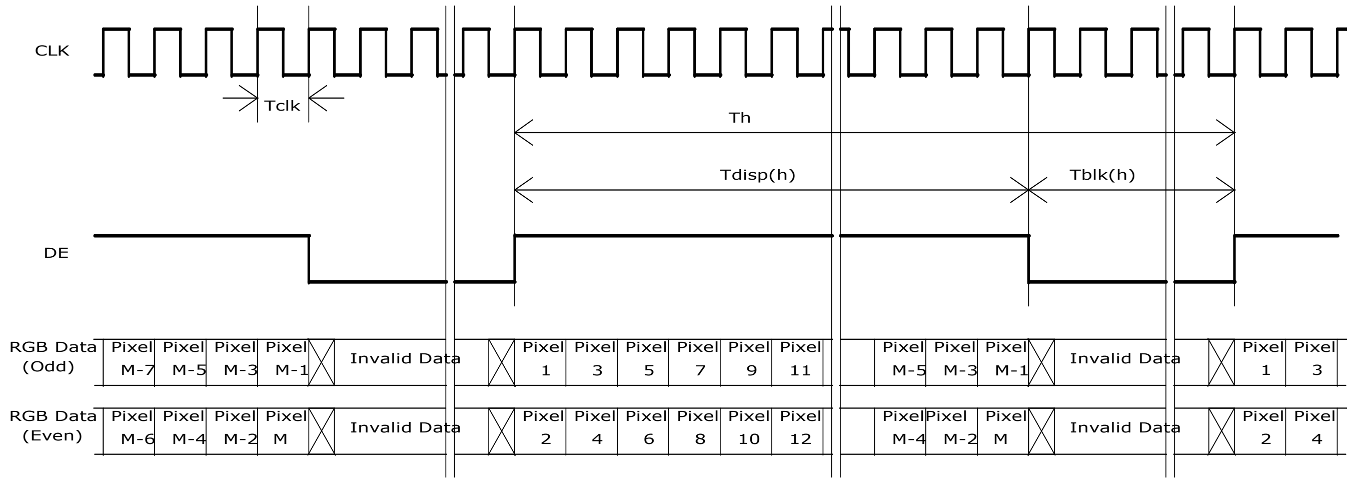
Basically, interface timings should match the 3840x2160 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T_{Clock}	-	533.5	-	MHz
Vertical Section	Period	T_V	-	2222	-	T_{Line}
	Active	T_{VD}		2160		
	Blanking	T_{VB}	-	62	-	
Horizontal Section	Period	T_H	-	4000	-	T_{Clock}
	Active	T_{HD}		3840		
	Blanking	T_{HB}	-	160	-	

Note : 1. DE mode only

6.3.2 Timing diagram

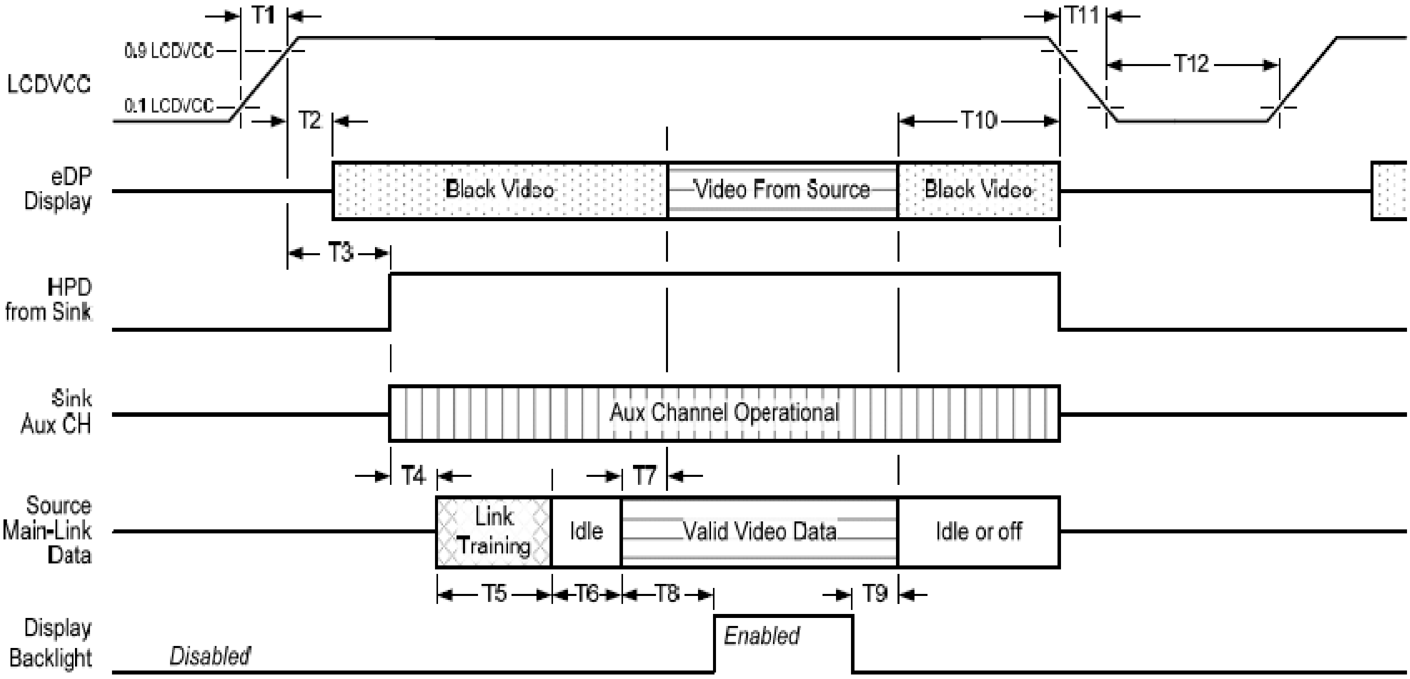

Tv
Tblk(v)
Tdisp(v)
Th
M pixel
N Line
Y
X
DE
RGB Data
N Line
Invalid Data
1 Line
2 Line
3 Line
4 Line
N Line
Invalid Data


CLK
Tclk
Th
Tdisp(h)
Tblk(h)
DE
RGB Data (Odd)
Pixel M-7
Pixel M-5
Pixel M-3
Pixel M-1
Invalid Data
Pixel 1
Pixel 3
Pixel 5
Pixel 7
Pixel 9
Pixel 11
Pixel M-5
Pixel M-3
Pixel M-1
Invalid Data
Pixel 1
Pixel 3
RGB Data (Even)
Pixel M-6
Pixel M-4
Pixel M-2
Pixel M
Invalid Data
Pixel 2
Pixel 4
Pixel 6
Pixel 8
Pixel 10
Pixel 12
Pixel M-4
Pixel M-2
Pixel M
Invalid Data
Pixel 2
Pixel 4

6.4 Power ON/OFF Sequence

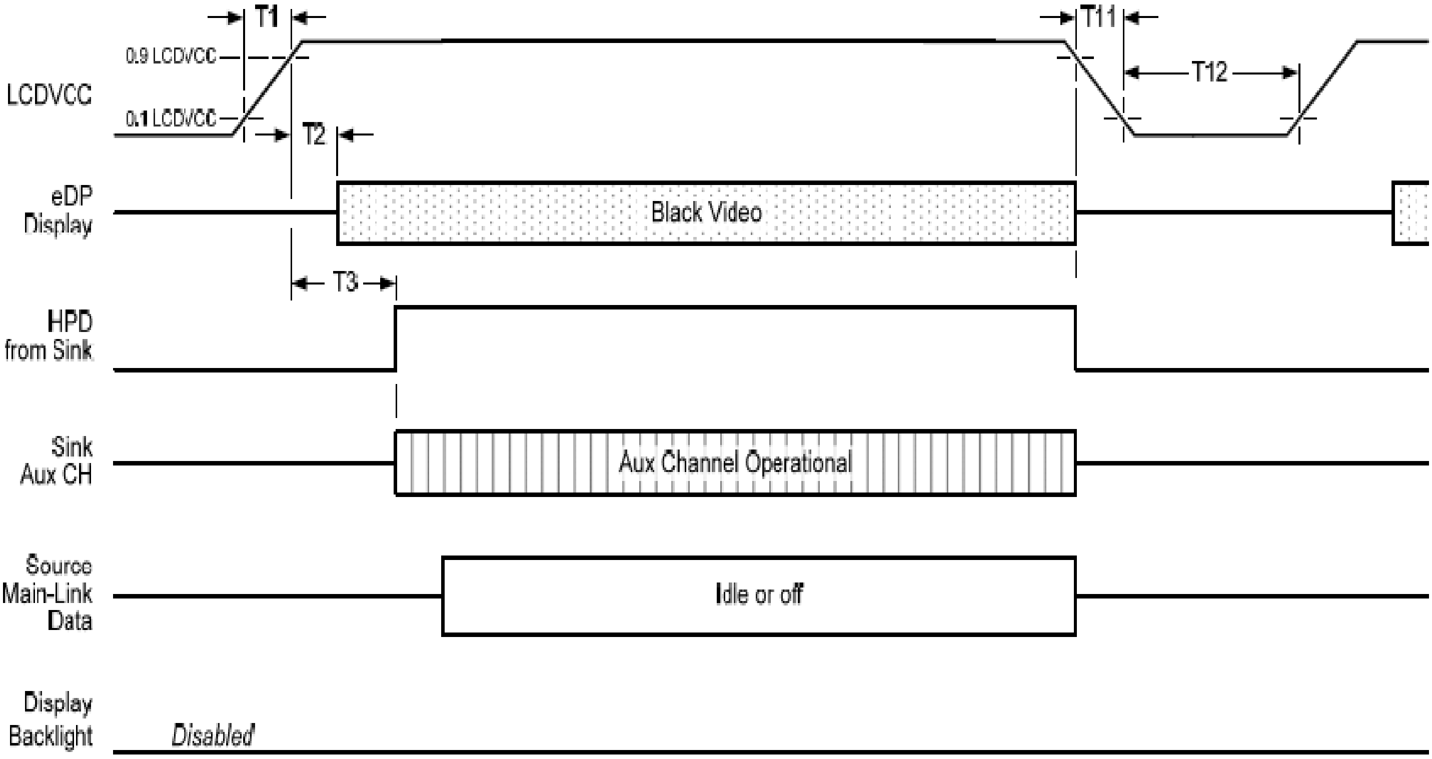
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port panel power sequence:


T1
T11
T12
0.9 LCDVCC
0.1 LCDVCC
LCDVCC
T2
T10
eDP Display
Black Video
Video From Source
Black Video
T3
HPD from Sink
Sink Aux CH
Aux Channel Operational
T4
T7
Source Main-Link Data
Link Training
Idle
Valid Video Data
Idle or off
T5
T6
T8
T9
Display Backlight
Disabled
Enabled

Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:


T1
T11
T12
0.9 LCDVCC
0.1 LCDVCC
LCDVCC
T2
eDP Display
Black Video
T3
HPD from Sink
Sink Aux CH
Aux Channel Operational
Source Main-Link Data
Idle or off
Display Backlight
Disabled

Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

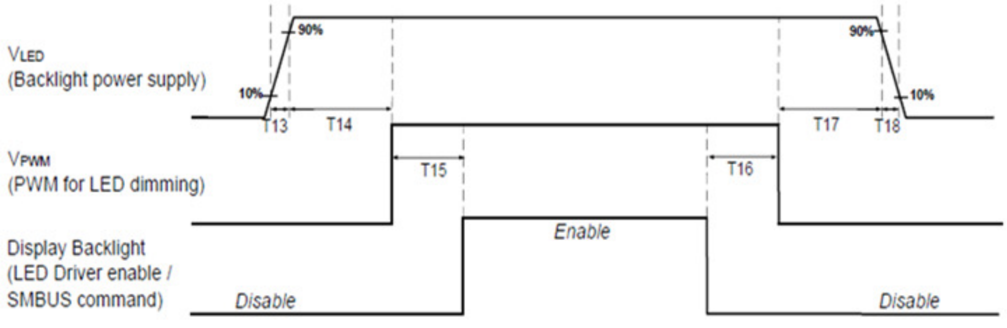
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).

-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

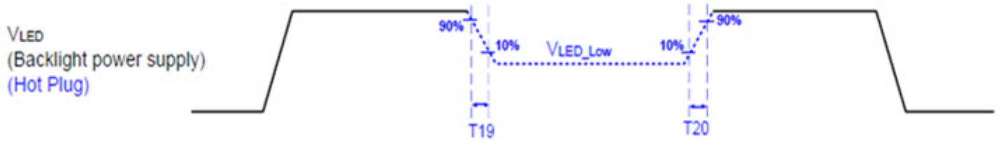
Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:


VLED
(Backlight power supply)
90%
10%
90%
10%
T13
T14
T17
T18
VPWM
(PWM for LED dimming)
T15
T16
Display Backlight
(LED Driver enable /
SMBUS command)
Disable
Enable
Disable

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.


VLED
(Backlight power supply)
(Hot Plug)
90%
10%
VLED_Low
10%
90%
T19
T20

	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = $5xT_{PWM}$*

*T_{PWM}= 1/PWM Frequency

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

● Test method:	Non-Operation
● Acceleration:	1.5 G
● Frequency:	10 - 500Hz Random
● Sweep:	30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

● Test method:	Non-Operation
● Acceleration:	220 G , Half sine wave
● Active time:	2 ms
● Pulse:	X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta=0℃, 300h	
High Temperature Storage	Ta= 60℃, 300h	
Low Temperature Storage	Ta= -20℃, 250h	
Thermal Shock Test	Ta=-20℃(30min) ~60℃(30min), 100cycles condition.	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

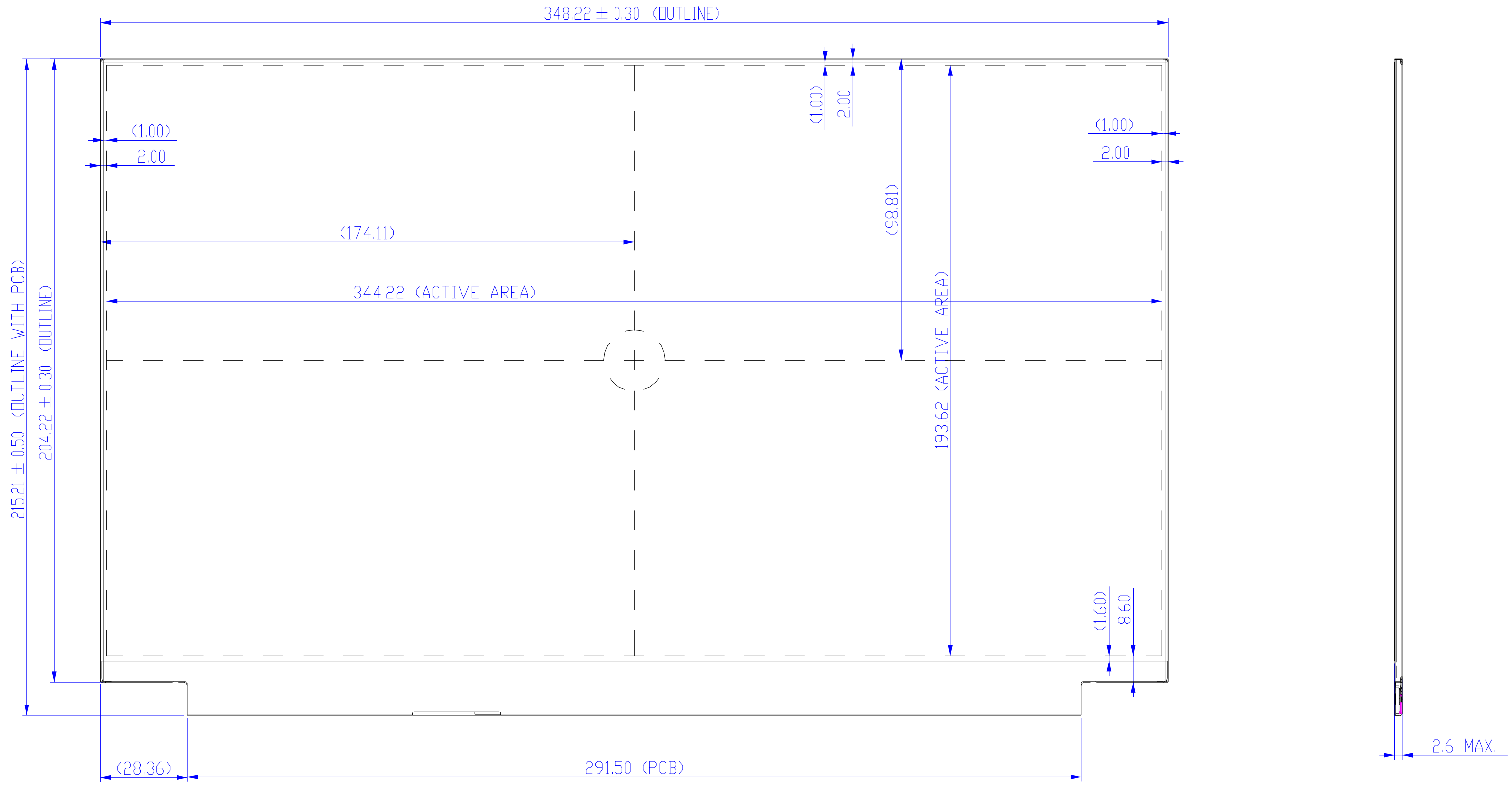
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

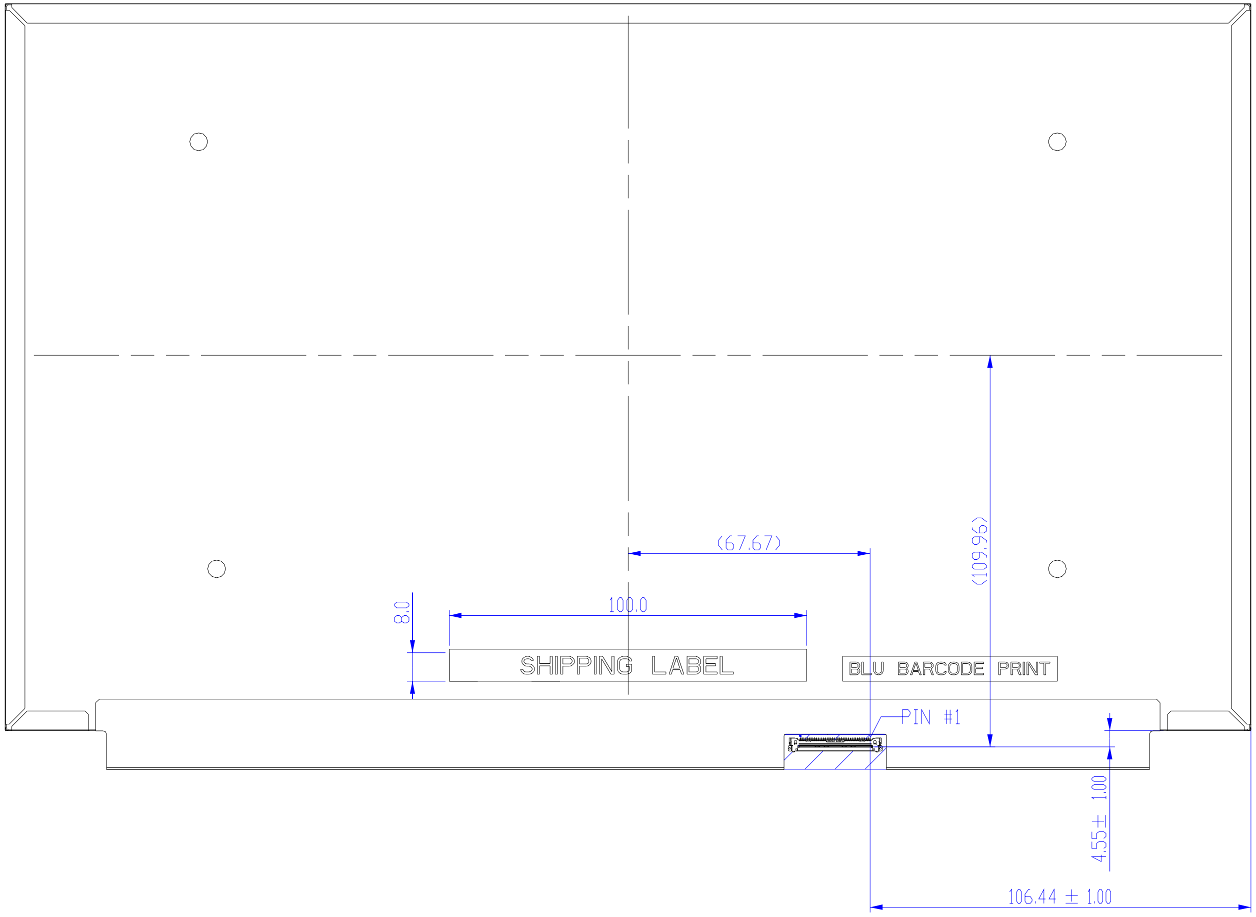
8. Mechanical Characteristics

8.1 LCM Outline Dimension

8.1.1 Standard Front View

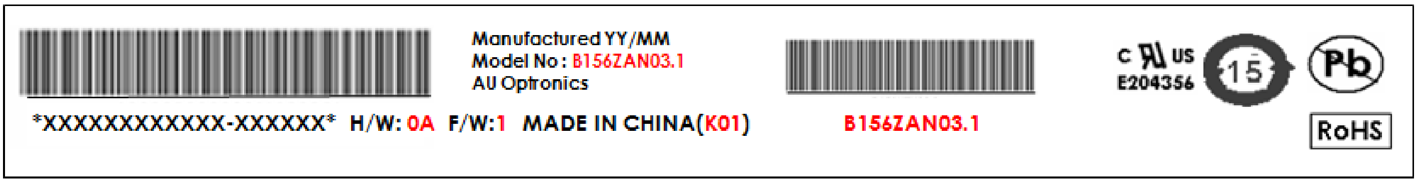

348.22 ± 0.30 (OUTLINE)
(1.00)
2.00
(1.00)
2.00
(1.00)
2.00
(174.11)
344.22 (ACTIVE AREA)
(98.81)
193.62 (ACTIVE AREA)
215.21 ± 0.50 (OUTLINE WITH PCB)
204.22 ± 0.30 (OUTLINE)
(1.60)
8.60
(28.36)
291.50 (PCB)
2.6 MAX.

8.1.2 Standard Rear View


(67.67)
(109.96)
100.0
8.0
SHIPPING LABEL
BLU BARCODE PRINT
PIN #1
4.55± 1.00
106.44 ± 1.00

9. Shipping and Package

9.1 Shipping Label Format



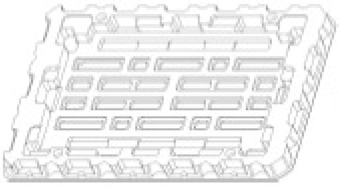
Manufactured YY/MM
Model No : B156ZAN03.1
AU Optronics

XXXXXXXXXXXX-XXXXXX H/W: 0A F/W:1 MADE IN CHINA(K01)

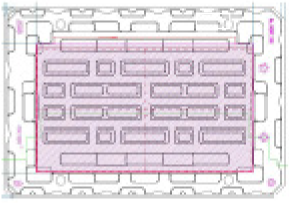
B156ZAN03.1

9.2 Carton Package

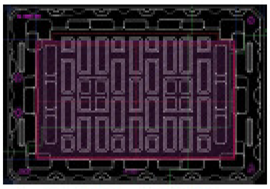
1、取出 PP 瓦楞



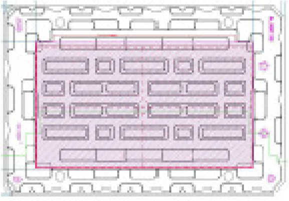
2、Tray 置放於 PP 瓦楞板上



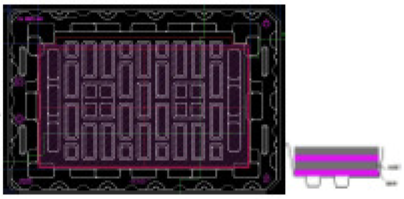
3、第一层 EPE spacer 放於 tray 盤上



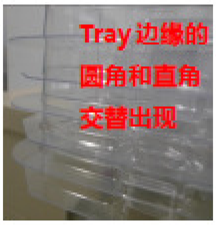
4、第一层 Panel 放於 Spacer 上, CF 面朝上



5、第二层 EPE spacer 放於 第一层 Panel 上

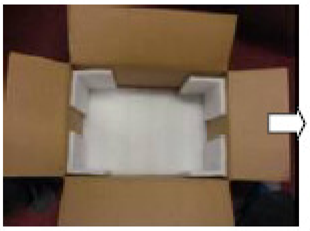


6、第二层 Panel 放於 Spacer 上, CF 面朝上



7、Tray 旋转堆叠
(Panel 共 26 片,最上面第 14 個 tray 是空的)

8、完成堆叠的 tray 放入靜電袋中, 並使用 tape 封口



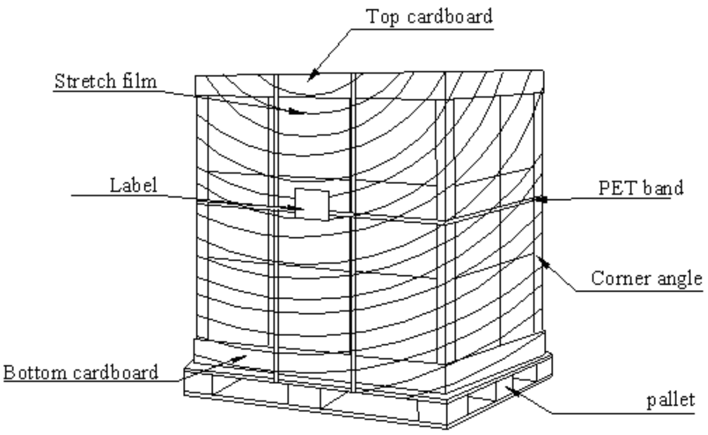
9、EPE cushion 放入紙箱

10、將包好靜電袋的 tray 整落 放入紙箱中

11、放入 EPE cushion

12、Tape 封紙箱

9.3 Shipping Package of Palletizing Sequence


Top cardboard
Stretch film
Label
PET band
Corner angle
Bottom cardboard
pallet

10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		**HEX**	**BIN**	**DEC**	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	EB	11101011	235	
0B	hex, LSB first	31	00110001	49	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	10	00010000	16	
11	Year of manufacture	1B	00011011	27	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	A5	10100101	165	
15	**Max H image size** *(rounded to cm)*	22	00100010	34	
16	**Max V image size** *(rounded to cm)*	13	00010011	19	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	CE	11001110	206	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	B5	10110101	181	
1B	Red x **(Upper 8 bits)**	A6	10100110	166	
1C	Red y/ highER 8 bits	54	01010100	84	
1D	Green x	34	00110100	52	
1E	Green y	B6	10110110	182	
1F	Blue x	25	00100101	37	
20	Blue y	0E	00001110	14	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	

29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	52	01010010	82	
37	Pixel Clock/10000 USB	D0	11010000	208	
38	Horz active **Lower 8bits**	00	00000000	0	
39	Horz blanking **Lower 8bits**	A0	10100000	160	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	F0	11110000	240	
3B	Vertical Active **Lower 8bits**	70	01110000	112	
3C	Vertical Blanking **Lower 8bits**	3E	00111110	62	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	80	10000000	128	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	35	00110101	53	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	58	01011000	88	
43	Vertical Image Size **Lower 8bits**	C1	11000001	193	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		00	00000000	0	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	

57		00	00000000	0	
58		00	00000000	0	
59		18	00011000	24	
5A	Detailed timing/monitor descriptor #3	00	00000000	0	
5B		00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor descriptor #4	00	00000000	0	
6D		00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	35	00110101	53	5
74	Manufacture P/N	36	00110110	54	6
75	Manufacture P/N	5A	01011010	90	Z
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	4E	01001110	78	N
78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	33	00110011	51	3
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	31	00110001	49	1
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	E7	11100111	231	