Version	1.9
Total pages	27
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Product Specification

Color TFT-LCD module

MODEL NAME: A080SN01 V0
(97.08A07.000)

(◆) Preliminary Specification
(..…) Final Specification

Record of Revision

| Version	Revise Date	Page	Content
0.0	14/Mar/2007		First draft.
0.1	16/Mar/2007	6	Revise min. operation and storage temperature
		7	Add min and max LED lightbar voltage
		16	Add brightness condition, V=12V
0.2	28/Mar/2007	20~22	Add suggested application circuit
		23~24	Revise outline drawing - FPC length: from 30.3mm to 45mm - Suggested FPC connector: XF2M-6015-1AH
0.3	14/May/2007	6	Update min. & max. VCOM value
		16	Update white chromaticity
		23-24	Update outline drawing
0.4	25/May/2007	6	Update AV_{DD} , V_{GH} , V_{GL} , VCOM value
		12	Update register description
		15	Update recommended power on register setting
		21	Updata suggested application circuit
		24	Revise outline drawing - Update FPC connector: XF2M-6015-1AH
0.5	1/Jun/2007	7	Update the figure of LED series/parallel connection
0.6	13/Jul/2007	4	Modify pin#35 & #37 of FPC
		6	Remove DC/DC converter section
		6	Add power consumption
		21~23	Update suggested application circuit
0.7	24/Jul/2007	12	Modify serial register table(default value): R4/D8: 1
0.8	21/Aug/2007	8	Modify DCLK frequency of Horizontal timing
		12	Update serial register table(default value): R0/D3: 0
		23	Modify application circuit: VCOM => VCOMin
0.9	27/Aug/2007	25	Update outline drawing – Back side
1.0	13/Dec/2007	16~17	Add VGH, VGL Power on/off sequence
1.1	24/Jan/2008	25	Update outline drawing – Front side

1.2	2008/04/15	27	Add Suggestion- System block
1.3	2008/05/06	3	Add Total Power Consumption
		6	Update Electrical characteristics
1.4	2008/07/08	7	Remove LED lightbar voltage min value
		15	Add note on Recommended Power On Register Setting
1.5	2008/07/29	15	Update note on Recommended Power On Register
1.6	2008/11/06	18	Update Viewing angle
		25	Update Drawing FPC connector
		26	Update bar code label size to 83*9mm
1.7	2008/11/12	18	Update Response time
1.8	2009/01/07	12	Update Serial register table
		13	Delete R1 setting
1.9	2009/01/20	5	Update Pin35,37
		12	Update Serial Register table
		15	Delete notes

Contents:

Appendix:

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution (dot)	800RGB(W)x600(H)	
2	Active area (mm)	162(W)x121.5(H)	
3	Dot pitch (mm)	0.2025(W)x0.2025(H)	
4	Color configuration	R. G. B. stripe	Note 1
5	Overall dimension (mm)	183(W)x141(H)x6.3(D)	Note 2
6	Weight (g)	235 ±10	
7	Surface treatment	Anti-Glare	
8	Backlight unit	24 pcs of LED	
9	Total Power Consumption (Watt)	2.3 W Max (Include Logic and BLU power)	

Note 1: Below figure shows the dot stripe arrangement.
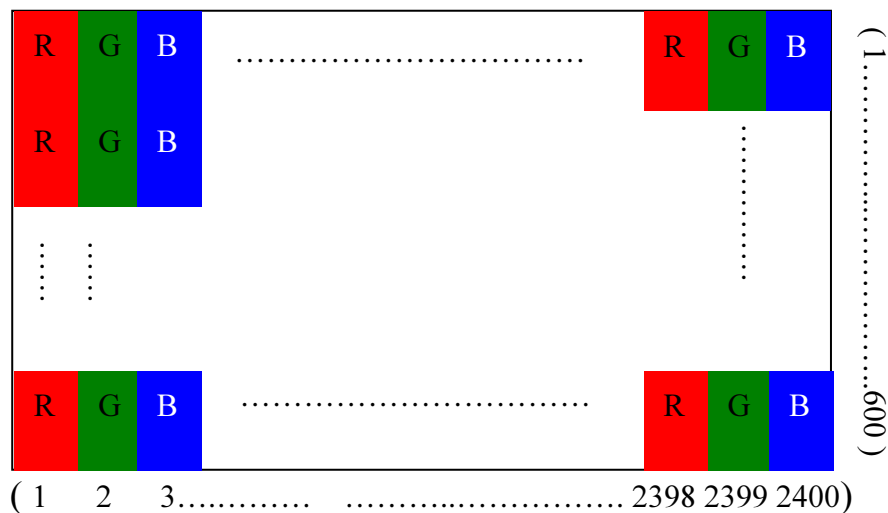
Note 2: Refer to Fig. 1

B. Electrical specifications

1.Pin assignment

a. TFT-LCD panel driving section

Pin no	Symbol	I/O	Description	Remark
1	AGND	P	Analog Ground	
2	AVDD	P	Analog Power	
3	VCC	P	Digital Power	
4	R0	I	Data input (LSB)	
5	R1	I	Data input	
6	R2	I	Data input	
7	R3	I	Data input	
8	R4	I	Data input	
9	R5	I	Data input	
10	R6	I	Data input	
11	R7	I	Data input (MSB)	
12	G0	I	Data input (LSB)	
13	G1	I	Data input	
14	G2	I	Data input	
15	G3	I	Data input	
16	G4	I	Data input	
17	G5	I	Data input	
18	G6	I	Data input	
19	G7	I	Data input (MSB)	
20	B0	I	Data input (LSB)	
21	B1	I	Data input	
22	B2	I	Data input	
23	B3	I	Data input	
24	B4	I	Data input	
25	B5	I	Data input	
26	B6	I	Data input	
27	B7	I	Data input (MSB)	
28	DCLK	I	Clock input	
29	DE	I	Data enable signal	
30	HSYNC	I	Horizontal sync input. Negative polarity	
31	VSYNC	I	Vertical sync input. Negative polarity	
32	SCL	I	Serial communication clock input	
33	SDA	I	Serial communication data input	

34	CSB	I	Serial communication chip select	
35	NC	-	For test, do not connect (Please leave it open)	
36	VCC	P	Digital Power	
37	NC	-	For test, do not connect (Please leave it open)	
38	GND	P	Digital ground	
39	AGND	P	Analog ground	
40	AVDD	P	Analog Power	
41	VCOMin	I	For external VCOM DC input (Optional)	
42	DITH	I	Dithering setting DITH = "L" 6bit resolution(last 2 bits of input data turncated) DITH = "H" 8bit resolution(Default setting)	
43	NC	-	Not connect	
44	VCOM	O	connect a capacitor	
45	V10	P	Gamma correction voltage reference	
46	V9	P	Gamma correction voltage reference	
47	V8	P	Gamma correction voltage reference	
48	V7	P	Gamma correction voltage reference	
49	V6	P	Gamma correction voltage reference	
50	V5	P	Gamma correction voltage reference	
51	V4	P	Gamma correction voltage reference	
52	V3	P	Gamma correction voltage reference	
53	V2	P	Gamma correction voltage reference	
54	V1	P	Gamma correction voltage reference	
55	NC	-	Not connect	
56	VGH	P	Positive power for TFT	
57	VCC	P	Digital Power	
58	VGL	P	Negative power for TFT	
59	GND	P	Digital Ground	
60	CAP	C	Connected to a capacitor	

I: Input; P: Power; G: Ground; C: Capacitor

b. Backlight driving section (Refer to Figure 1)

No.	Symbol	I/O	Description	Remark
1	HI	I	Power supply for backlight unit (High voltage)	--
2	GND	-	Ground for backlight unit	--

2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V_{CC}	GND=0	-0.5	5	V	
	AV_{DD}	AGND=0	-0.5	15	V	
	V_{GH}	GND=0	-0.3	42	V	
	V_{GL}		-20	0.3	V	
	$V_{GH}-V_{GL}$		-	40	V	
Input signal voltage	V_I		-0.3	V_{CC}+0.3	V	Note 1
	VCOM		0	6.5	V	
Operating temperature	Topa		-10	60	℃	
Storage temperature	Tstg		-20	70	℃	

Note 1: HS , VS , DE , Digital Data

3. Electrical characteristics

a. Typical operating conditions (GND=AVss=0V, Note 2)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		V_{CC}	2.7	3.3	3.6	V	
		I_{VCC}	-	11	14	mA	Black Pattern@V_{CC}=3.3
		AV_{DD}	11	11.68	12	V	
		I_{AVDD}	-	16	20	mA	Black Pattern
		V_{GH}	7	15	VEE+40	V	
		I_{VGH}	-	0.16	0.2	mA	Black Pattern
		V_{GL}	-20	-6.75	-5	V	
		I_{VGL}	-	0.16	0.2	mA	Black Pattern
Power Consumption		P	-	230	260	mW	Black Pattern
VCOM		V_{CDC}	3.9	4.1	4.3	V	DC component
Input signal voltage	H Level	V_{IH}	0.7 V_{CC}	-	V_{CC}	V	Note 1
	L Level	V_{IL}	0	-	0.3 V_{CC}	V	
Input level of V1~V7		Vx	VCOMDC	-	AVDD-0.5		Positive gamma correction voltage
Input level of V8~V14		Vx	0.5	-	VCOMDC		Negative gamma correction voltage

Note 1: HS , VS , DE, Digital Data

b. Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED lightbar voltage	V_L	-	12	12	V	Note 1, 2
LED Lightbar current	I_L	-	160		mA	Note 1, 2
LED Lightbar life time		10,000	-	-	Hr	Note 1, 2, 3, 4

Note 1: LED backlight is LED lightbar type(24 pcs of LED).

Note 2: Definition of "LED Lifetime": brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25℃ and LED lightbar voltage = 12V
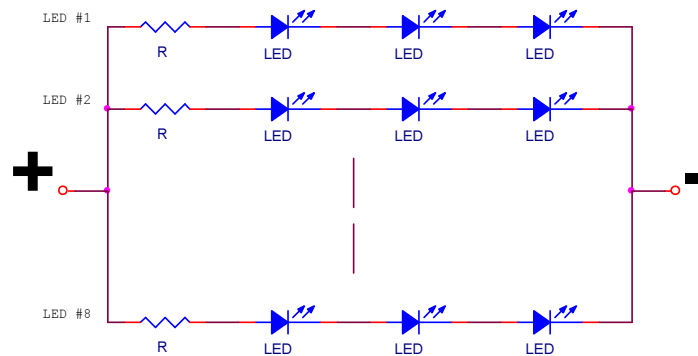
Note 3: The value is only for reference.

Note 4: If it operates with LED lightbar voltage more than 12V, it maybe decreases LED lifetime.

4. AC Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Clock High time	T_{WCL}	8	-	-	ns	
Clock Low time	T_{WCH}	8	-	-	ns	
Hsync setup time	T_{HSU}	5	-	-	ns	
Hsync hold time	T_{HHD}	10	-	-	ns	
Vsync setup time	T_{VSU}	0	-	-	ns	
Vsync hold time	T_{VHD}	2	-	-	ns	
Data setup time	T_{DSU}	5	-	-	ns	
Data hold time	T_{DHD}	10	-	-	ns	
Data enable set-up time	T_{ESU}	4	-	-	ns	
Data enable hold time	T_{EHD}	2	-	-	ns	
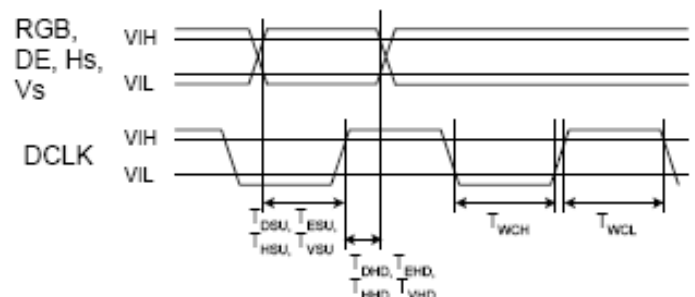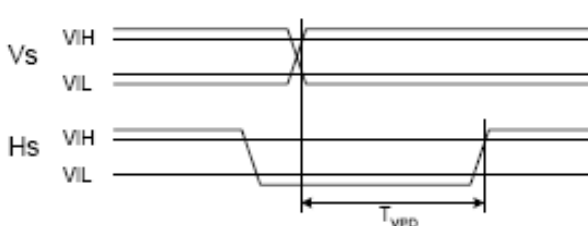
Input timing details

5. RGB Parallel Input Timing

a. Horizontal timing

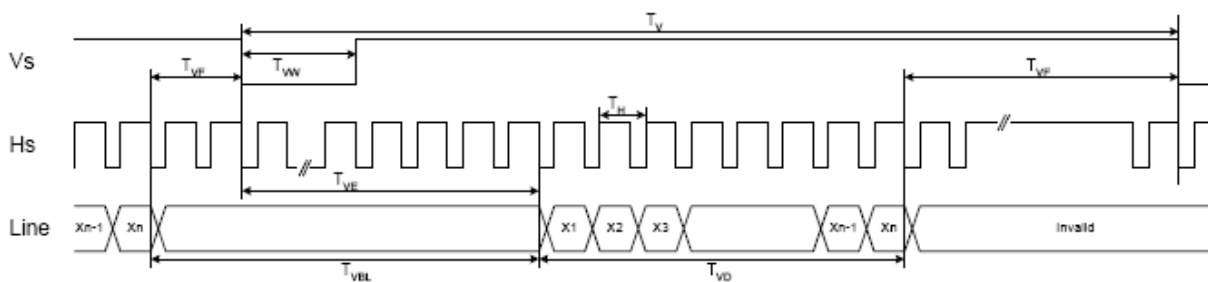| Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency	F_{DCLK}	25	40	45	MHz	
DCLK period	T_{DCLK}	22	25	40	ns	
Hsync period (= T_{HD} + T_{HBL})	T_H	986	1056	1183	DCLK	
Active Area	T_{HD}	-	800	-	DCLK	
Horizontal blanking (= T_{HF} + T_{HE})	T_{HBL}	186	256	383	DCLK	
Hsync front porch	T_{HF}	-	40	-	DCLK	
Delay from Hsync to 1st data input (= T_{HW} + T_{HB})	T_{HE}	88	216	343	DCLK	Function of HDL[7..0] settings
Hsync pulse width	T_{HW}	1	128	136	DCLK	
Hsync back porch	T_{HB}	10	88	342	DCLK	
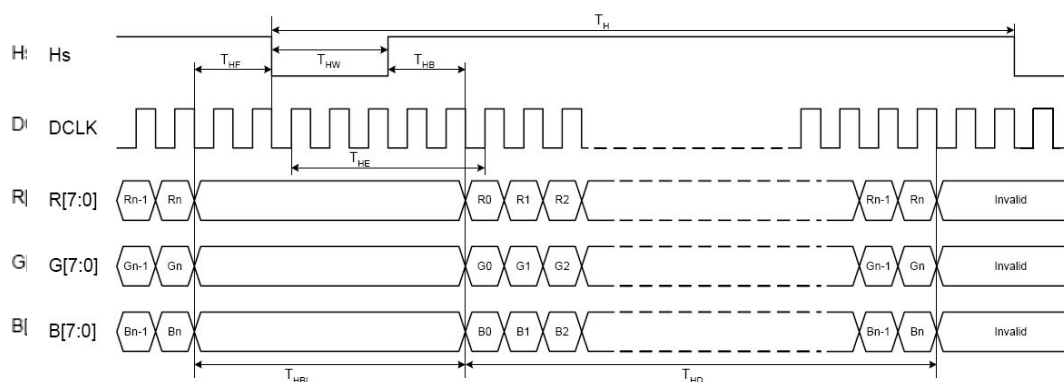
Horizontal input timing (HV mode)
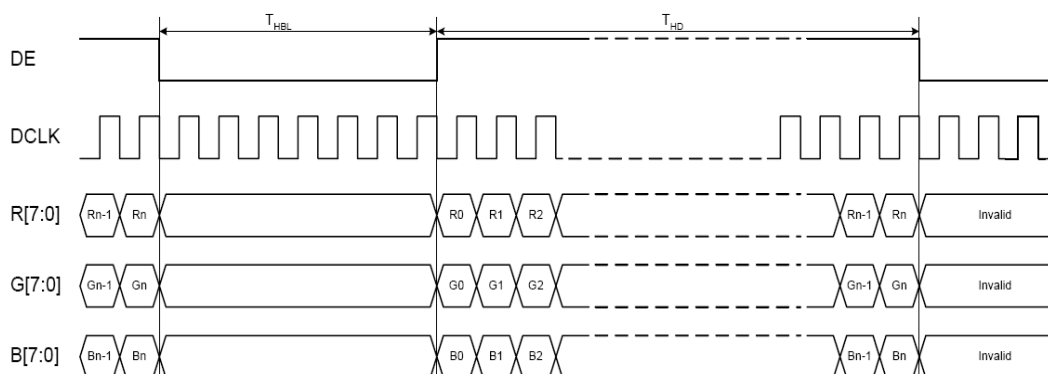
Horizontal input timing (DE mode)

b. Vertical timing

| Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Vsync period (= $T_{VD} + T_{VBL}$)	T_V	620	628	635	Th	
Active lines	T_{VD}	-	600	-		
Vertical blanking (= $T_{VF} + T_{VE}$)	T_{VBL}	20	28	35	Th	
Vsync front porch	T_{VF}	-	1	-	Th	
GD start pulse delay	T_{VE}	19	27	34	HS	Function of VDL[3..0] settings
Vsync pulse width	T_{VW}	1	3	16	Th	
Hsync/Vsync phase shift	T_{VPD}	2	320	-	DCLK	

Vertical timing (HV mode)
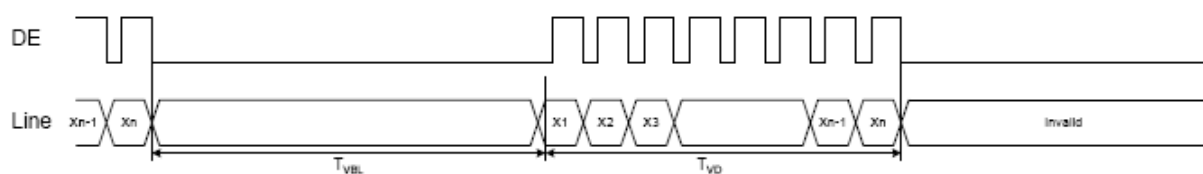
Vertical timing (DE mode)

6. Serial control interface

| Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Serial data setup time	T_{IST}	120	-	-	ns	
Serial data hold time	T_{IHD}	120	-	-	ns	
CSB setup time	T_{CST}	120	-	-	ns	
CSB hold time	T_{CHD}	120	-	-	ns	
Serial clock high/low	T_{SSW}	120	-	-	ns	
Serial clock	T_{SCK}	320	-	-	ns	
Delay from CSB to VSYNC	T_{CV}	1	-	-	us	
Chip select distinguish	T_{CD}	1	-	-	us	
Serial data output delay	T_{ID}	-	-	60	ns	CL=20pF
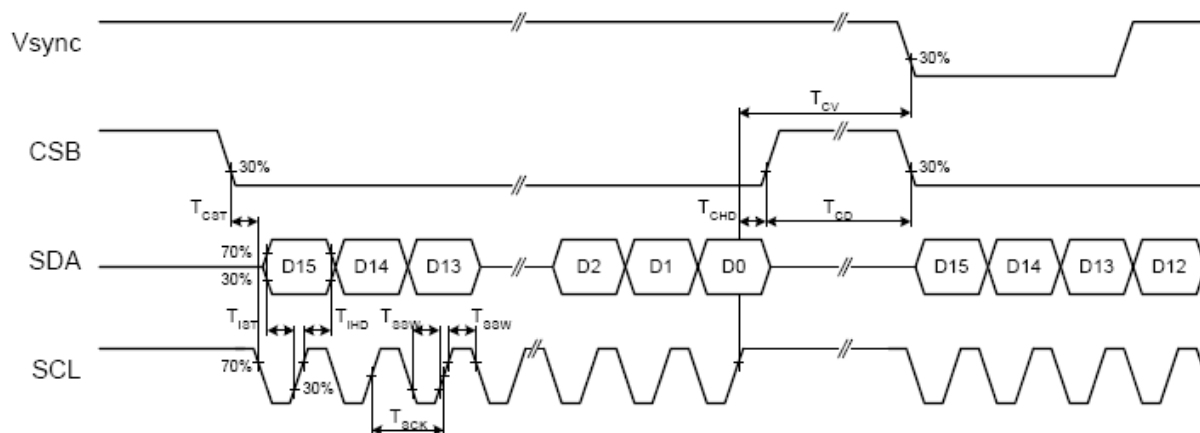
AC serial interface write mode timings
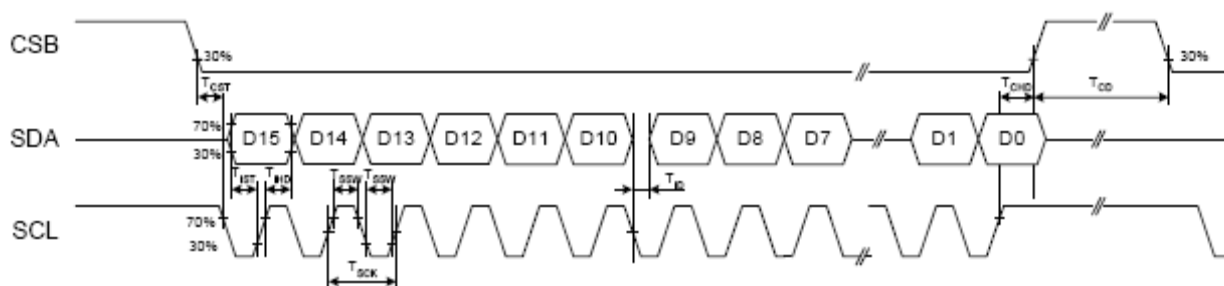
AC serial interface read mode timings

7. Register Bank

There is a total of 6 registers each containing several parameters. For a detailed description of the parameters refer to register table. The serial register has read/write function. D[15:12] are the register address, D[11] defines the read or write mode and D[10:0] are the data.
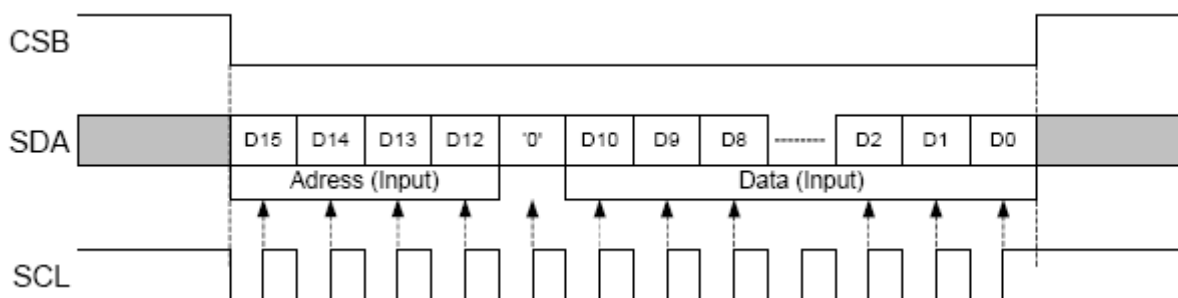
Serial Interface Write sequence
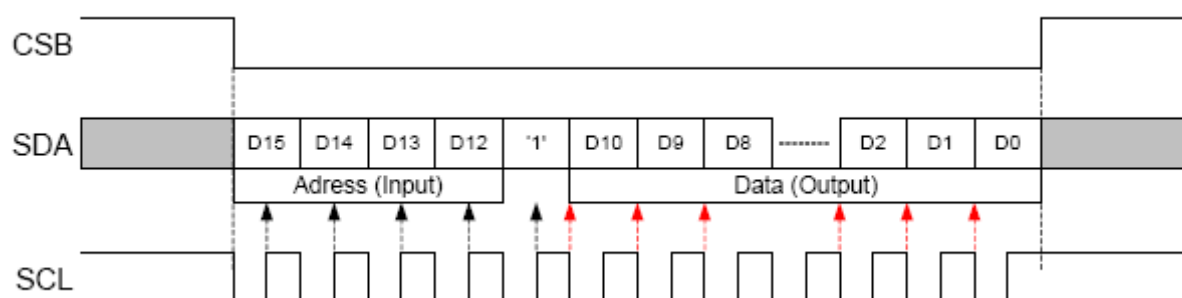
Serial Interface Read sequence

1. At power-on, the default values specified for each parameter are taken.

2. If less than 16-bit data are read during the CS low time period, the data is cancelled.

   a. The write operation is cancelled.

   b. The read operation is interrupt.

3. If more than 16-bit data are read during the CS low time period, the last 16 bits are kept.

   a. Address & R/W are always defined form CSB falling edge.

   b. The write operation load last 11 bit data before CSB rising edge.

   c. The read operation is "D0" is output to SDA until CSB rising edge.

4. All items are set at the falling edge of the vertical sync, except R0[1:0].

5. When GRB is activated through the serial interface, all registers are cleared, except the GRB value.

6. Register R/W setting: D11 = "L" → write mode; D11 = "H" → read mode.

7. The register setting values are valid when VCC already goes to high and after VSYNC starts.

8. It is suggested that VSYNC, HSYNC, DCLK always exists in the same time. But if HSYNC, DCLK stops, only VSYNC operating, the register setting is still valid.

9. If the chip goes to standby mode, the register value will still keep. MCU can wake up the chip only by changing standby mode value from low to high.

10. The register setting values are rewritten by the influence of static electricity, a noise, etc. to unsuitable value, incorrect operating may occur. It is suggested that the SPI interface will setup as frequently as possible.

8. Serial Register table(Default Value)

Reg	ADDRESS				R/W	DATA										
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	(01)		(01)		(1)	U/D (0)	SHL (1)	(1)	(0)	GRB (1)	STB (1)
R1	0	0	0	1	0	×	(0)	(1)	(01)		(2Fh)					
R2	0	0	1	0	0	×	×	×	HDL (80h)							
R3	0	0	1	1	0	×	×	(0)	(0)	(0)	(0)	(0)	VDL (1000)			
R4	0	1	0	0	0	×	×	(0)	(0)	(0)	(0)	(1)	(1111)			
R6	0	1	1	0	0	×	(0)	EnGB12 (1)	EnGB11 (1)	EnGB10 (1)	(0)	(0)	EnGB5 (1)	EnGB4 (1)	EnGB3 (1)	(0)

X: Reserved. Please set to "0".

9. Register Description

a. R0 setting

Address	Bit	Description		Default
0000	[10..0]	Bits 10-9	AUO Internal Use	01
		Bits7-8	AUO Internal Use	01
		Bit6 (DITH)	Dithering function.	1
		Bit5 (U/D)	Vertical shift direction selection.	0
		Bit4 (SHL)	Horizontal shift direction selection.	1
		Bit3 (SHDB1)	AVDD DC-DC converter shutdown setting.	1
		Bit2	AUO Internal Use	0
		Bit1 (GRB)	Global reset.	1
		Bit0 (STB)	Standby mode setting.	1

Bit6	DITH function
0	DITH off.
1	DITH on. **(default)**

Bit5	U/D function
0	Scan down; First line= Gn -> Gn-1 -> … -> G2 -> Last line=G0. **(default)**
1	Scan up; First line= G0 -> G2 -> … -> Gn-1 -> Last line=Gn

Bit4	SHL function
0	Shift left; First data= Y600 -> Y599 -> … -> Y2 -> Last data=Y1.
1	Shift right; First data= Y1 -> Y2 -> … -> Y599 -> Last data=Y600. **(default)**

Bit3	SHDB1 function
0	AVDD DC-DC converter is off.
1	AVDD DC-DC converter is on. **(default)**

Bit1	GRB function
0	The controller is reset. Reset all registers to default value.
1	Normal operation. **(default)**

Bit0	STB function
0	T-CON, source driver and DC-DCs converters are off. All outputs are set to GND.
1	Normal operation. **(default)**

b. R2 setting

Address	Bit	Description		Default
0010	[7..0]	Bit7-0(HDL)	Horizontal start pulse adjustment function	80H

Bit7-0	HDL function
00h	$T_{HE} = T_{HEtyp}$ - 128 CLK period.
80h	$T_{HE} = T_{HEtyp}$. **(default)**
FFh	$T_{HE} = T_{HEtyp}$ + 127 CLK period.

c. R3 setting

Address	Bit	Description		Default
0011	[8..0]	Bit8	AUO Internal Use	0
		Bit7	AUO Internal Use	0
		Bit6	AUO Internal Use	0
		Bit5	AUO Internal Use	0
		Bit4	AUO Internal Use	0
		Bit3-0(VDL)	Vertical start pulse adjustment function	1000

Bit3-0	VDL function
0000	$T_{VE} = T_{VEtyp} - 8$ Hs period.
0001	$T_{VE} = T_{VEtyp} - 7$ Hs period.
0010	$T_{VE} = T_{VEtyp} - 6$ Hs period.
0011	$T_{VE} = T_{VEtyp} - 5$ Hs period.
0100	$T_{VE} = T_{VEtyp} - 4$ Hs period.
0101	$T_{VE} = T_{VEtyp} - 3$ Hs period.
0110	$T_{VE} = T_{VEtyp} - 2$ Hs period.
0111	$T_{VE} = T_{VEtyp} - 1$ Hs period.
1000	$T_{VE} = T_{VEtyp}$. (default)
1001	$T_{VE} = T_{VEtyp} - 1$ Hs period.

1010	$T_{VE} = T_{VEtyp} - 2$ Hs period.
1011	$T_{VE} = T_{VEtyp} - 3$ Hs period.
1100	$T_{VE} = T_{VEtyp} - 4$ Hs period.
1101	$T_{VE} = T_{VEtyp} - 5$ Hs period.
1110	$T_{VE} = T_{VEtyp} - 6$ Hs period.
1111	$T_{VE} = T_{VEtyp} - 7$ Hs period.

d. R6 setting

Address	Bit	Description		Default
0110	[9..0]	Bits9	AUO Internal Use	0
		Bits8(EnGB12)	Gamma buffer Enable for V9	1
		Bits7(EnGB11)	Gamma buffer Enable for V8	1
		Bits6(EnGB10)	Gamma buffer Enable for V7	1
		Bits5	AUO Internal Use	0
		Bits4	AUO Internal Use	0
		Bits3(EnGB5)	Gamma buffer Enable for V4	1
		Bits2(EnGB4)	Gamma buffer Enable for V3	1
		Bits1(EnGB3)	Gamma buffer Enable for V2	1
		Bits0	AUO Internal Use	0

Bitx	EnGBx function
0	Gamma buffer for VX is disabled (High Z).
1	Gamma buffer is enabled. VX must be connected externally.

Recommended Power On Register Setting

Reg No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	ADDRESS				R/W	DATA										
R0	0	0	0	0	0	10		01		1	0	1	0	0	1	1
R1	0	0	0	1	0	0	01		01		2Fh					
R2	0	0	1	0	0	0	0	0	80h							
R3	0	0	1	1	0	0	0	0	0	0	0	0	1000			
R4	0	1	0	0	0	0	0	1	1	00		1	1111			
R6	0	1	1	0	0	0	0	1	1	1	0	0	1	1	1	0

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10. Power Sequence
Sequence for power on/off and Signal on/off

a. Power on sequence
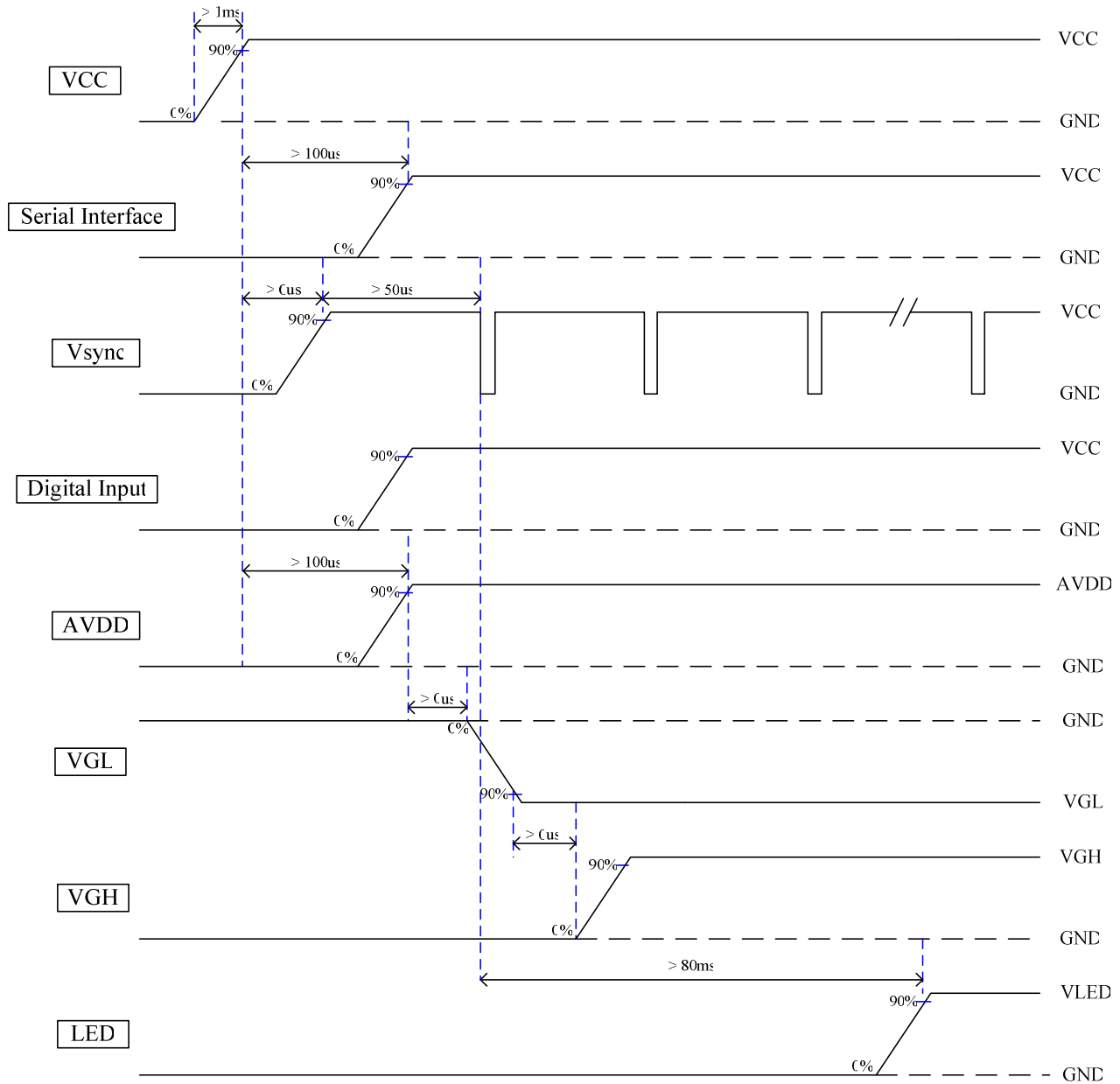
b. Power off sequence

友達光電
AU Optronics
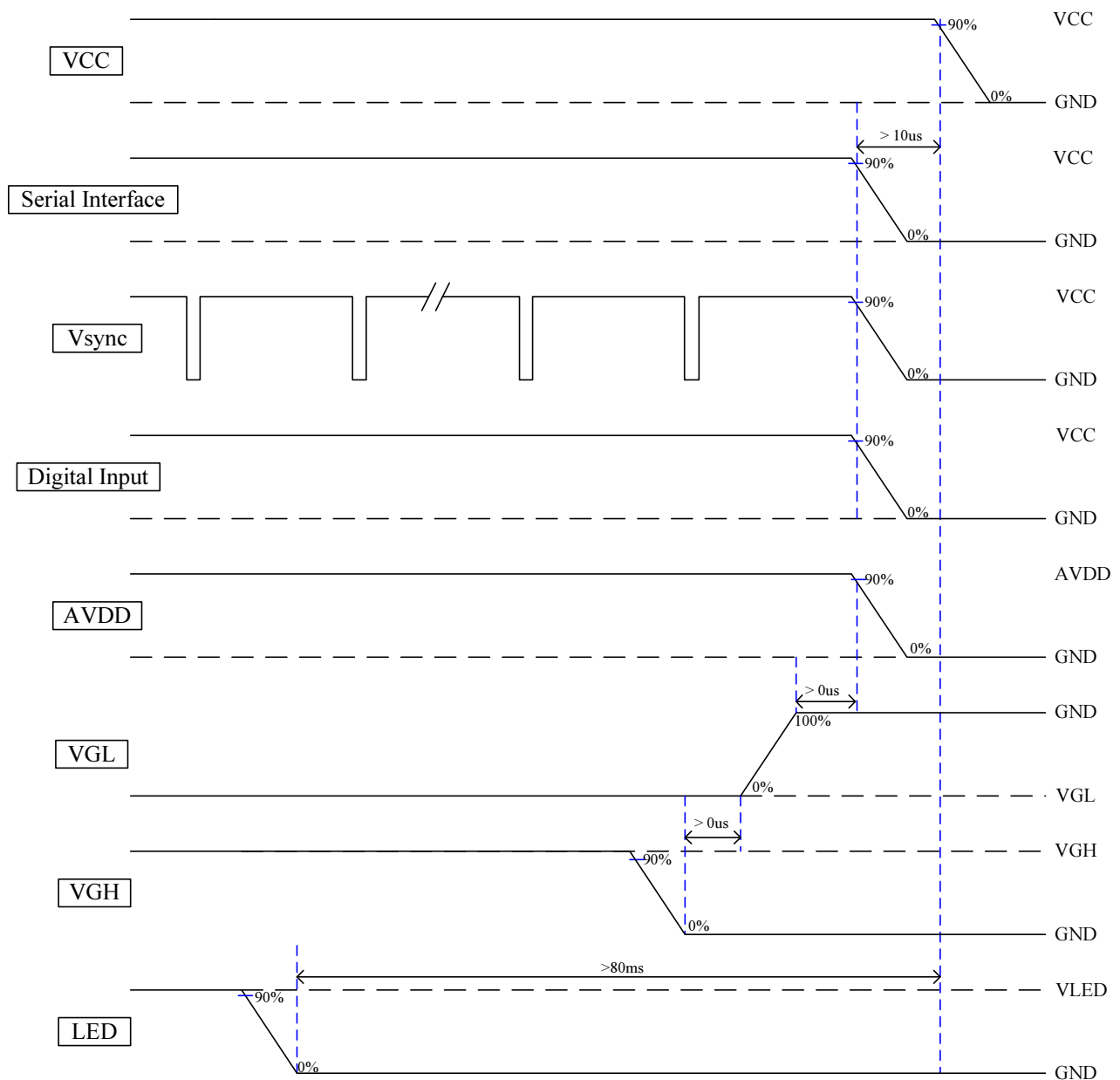
C. Optical specification (Note 1, Note 2)

| Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise Fall	Tr Tf	$\theta = 0°$	- -	4 16	8 32	ms ms	Note 3,5
Contrast ratio		CR	At optimized Viewing angle	300	400	-		Note 4, 5
Viewing angle	Top Bottom Left Right		$CR \geqq 10$	40 55 60 60	50 65 70 70	- - - -	deg.	Note 5, 6
Brightness		Y_L	$V_L = 12V$	150	200	-	cd/m^2	Note 7
White chromaticity		X	$\theta = 0°$	0.26	0.31	0.36		Note 7
		Y	$\theta = 0°$	0.28	0.33	0.38		

Note 1 : To be measured in the dark room. Ambient temperature =25℃, and LED lightbar voltage V_L = 12V.

Note 2 : To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-5A, after 15 minutes operation.

Note 3. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.
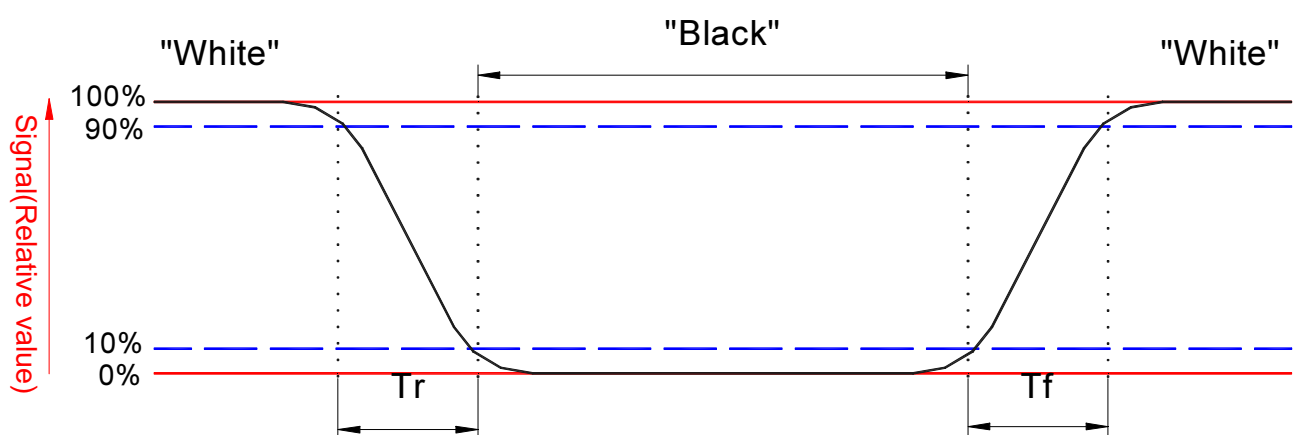
Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 5. White Vi=V_{i50} $+$ 1.5V

　　　　Black Vi=V_{i50} $\pm$ 2.0V

"$\pm$" means that the analog input signal swings in phase with V_{COM} signal.

"$\overline{+}$" means that the analog input signal swings out of phase with V_{COM} signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6. Definition of viewing angle, Refer to figure as below.
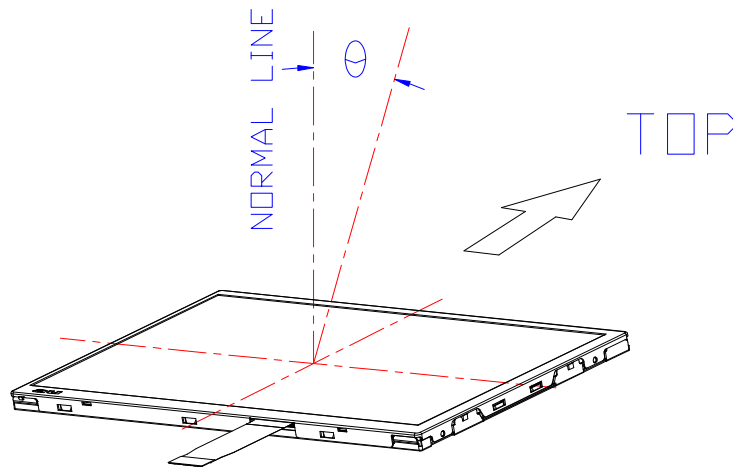
Note 7. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

D. Reliability test conditions (Note 2):

| No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70℃ 240Hrs	
2	Low temperature storage	Ta= -20℃ 240Hrs	
3	High temperature operation	Tp= 60℃ 240Hrs	
4	Low temperature operation	Ta= -10℃ 240Hrs	
5	High temperature and high humidity	Tp= 50℃, 80% RH 240Hrs	Operation
6	Heat shock	-10℃~60℃/ 100 cycles 1Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10 ~ 55 ~ 10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	JIS C7021, A-10 Condition A
9	Mechanical shock	100G, 6ms, ±X,±Y,±Z 3 times for each direction	JIS C7021, A-7 Condition C
10	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	JIS Z0202

Note1: Ta: Ambient Temperature.

Note2: Tp: Panel Surface Temperature

Note3: In the standard conditions, there is not display function NG issue occurred. All the cosmetic

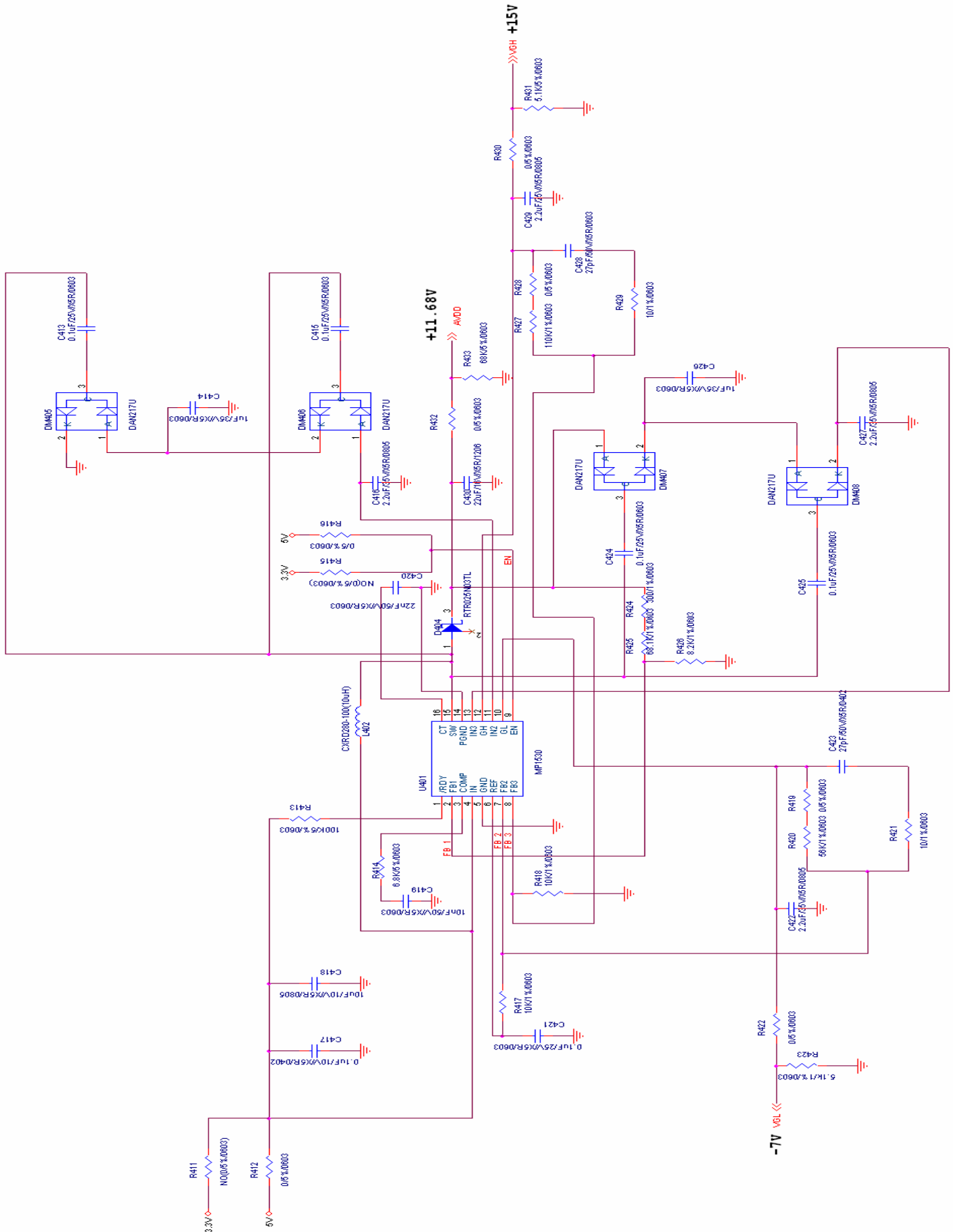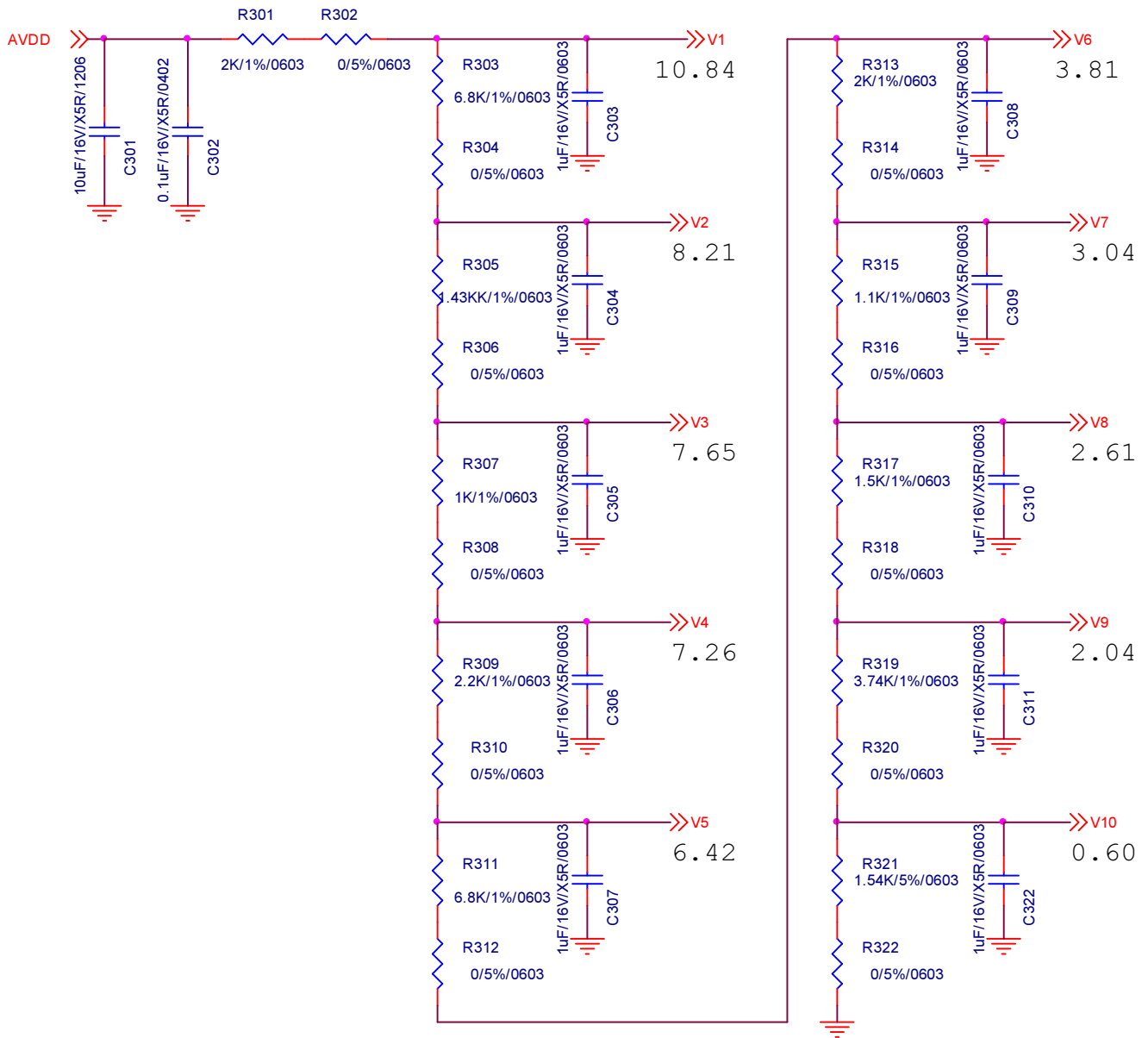specification is judged before the reliability stress.

E. Packing form

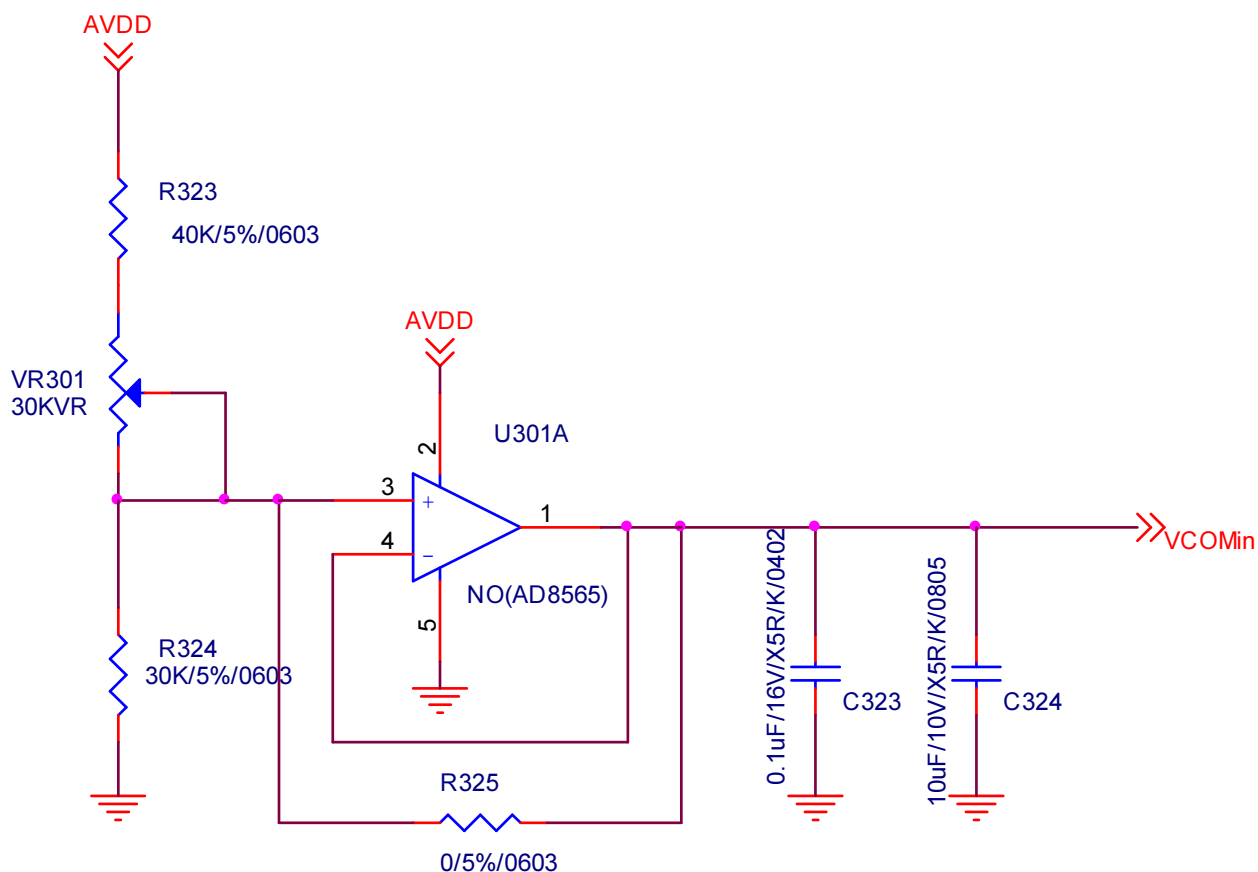| No.	Part Name	Part No.
1	A/S BAG A080FW01	79.08A02.001
2	S291 TAPE	84.01A04.001
3	TAPE 18MM(W) L133x1	80.13B01.011
4	CUSHION PACKAGING	83.08A07.001
5	CARTON AB ORG 520*340*250	81.01A09.003
6	CARTON BLANK LABEL	82.17B02.001
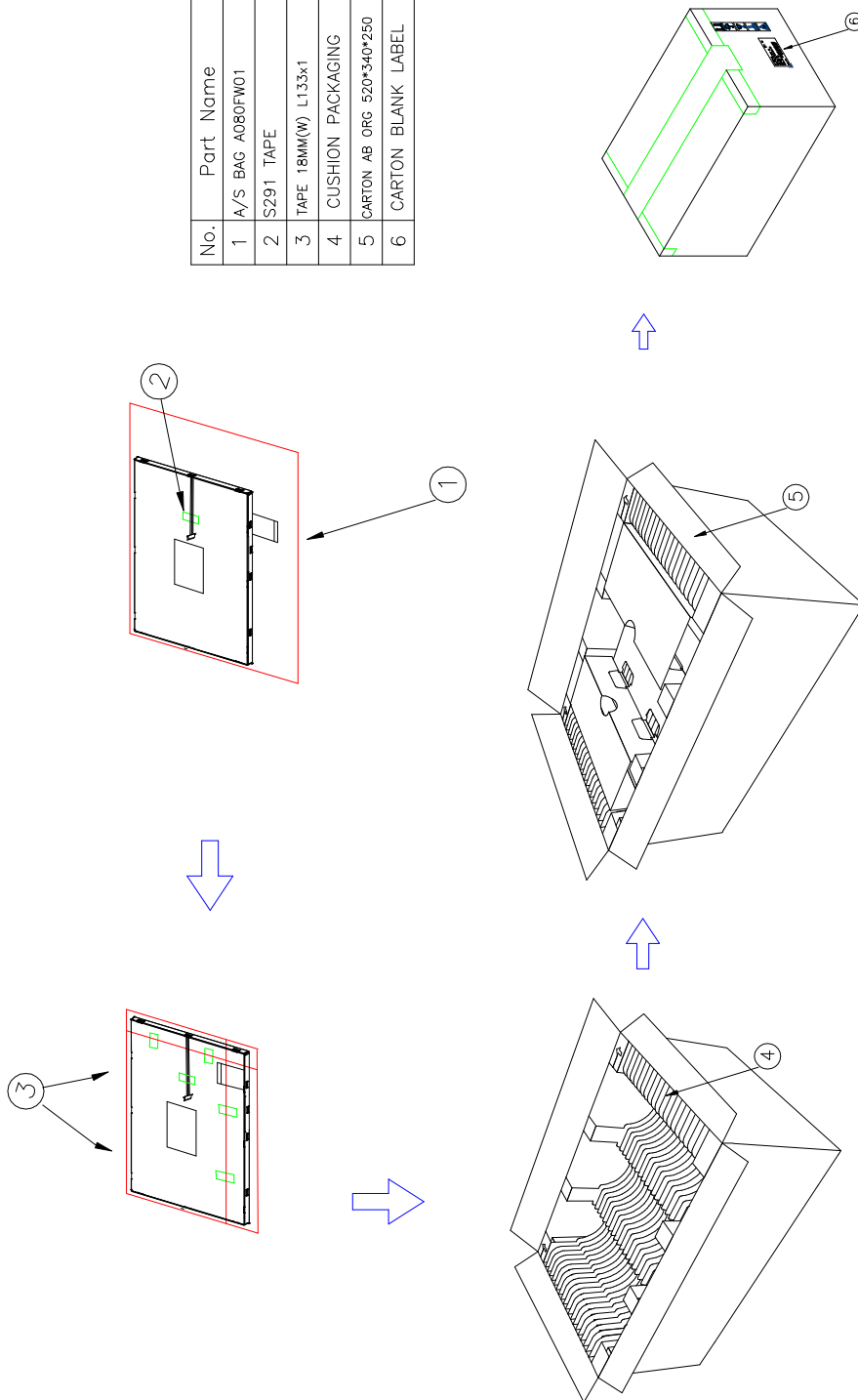
Max. capacity: 30 modules
Max. Weight : 7kg
Carton outline : 520 x 340 x 250 mm

F. Suggested application circuit

AVDD

R301 2K/1%/0603   R302 0/5%/0603

C301 10uF/16V/X5R/1206
C302 0.1uF/16V/X5R/0402

R303 6.8K/1%/0603
R304 0/5%/0603
C303 1uF/16V/X5R/0603
V1 10.84

R305 1.43KK/1%/0603
R306 0/5%/0603
C304 1uF/16V/X5R/0603
V2 8.21

R307 1K/1%/0603
R308 0/5%/0603
C305 1uF/16V/X5R/0603
V3 7.65

R309 2.2K/1%/0603
R310 0/5%/0603
C306 1uF/16V/X5R/0603
V4 7.26

R311 6.8K/1%/0603
R312 0/5%/0603
C307 1uF/16V/X5R/0603
V5 6.42

R313 2K/1%/0603
R314 0/5%/0603
C308 1uF/16V/X5R/0603
V6 3.81

R315 1.1K/1%/0603
R316 0/5%/0603
C309 1uF/16V/X5R/0603
V7 3.04

R317 1.5K/1%/0603
R318 0/5%/0603
C310 1uF/16V/X5R/0603
V8 2.61

R319 3.74K/1%/0603
R320 0/5%/0603
C311 1uF/16V/X5R/0603
V9 2.04

R321 1.54K/5%/0603
R322 0/5%/0603
C322 1uF/16V/X5R/0603
V10 0.60

NOTES:
1.GENERAL TOLERANCE:±0.3mm
2.LCD LIGHTBAR CONNECTOR: MOLEX 51021-0200
3.FPC CONNECTOR:XT2M-6015-1AH BY omz
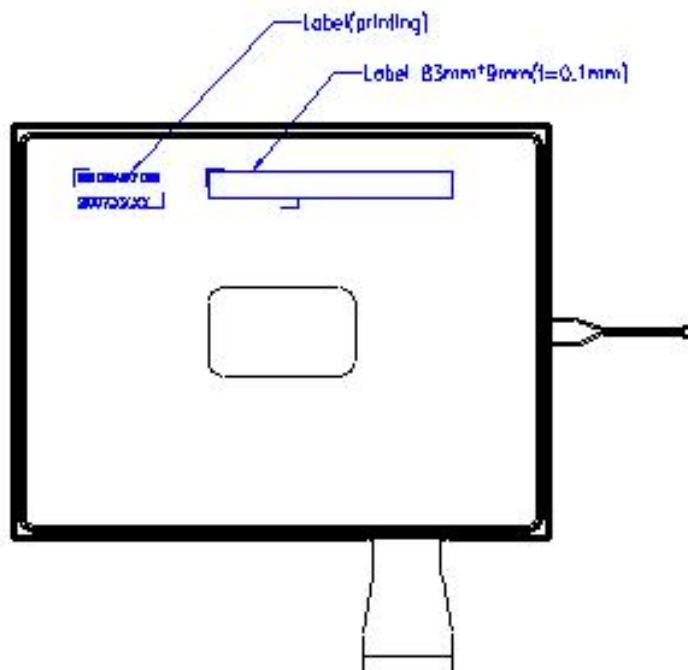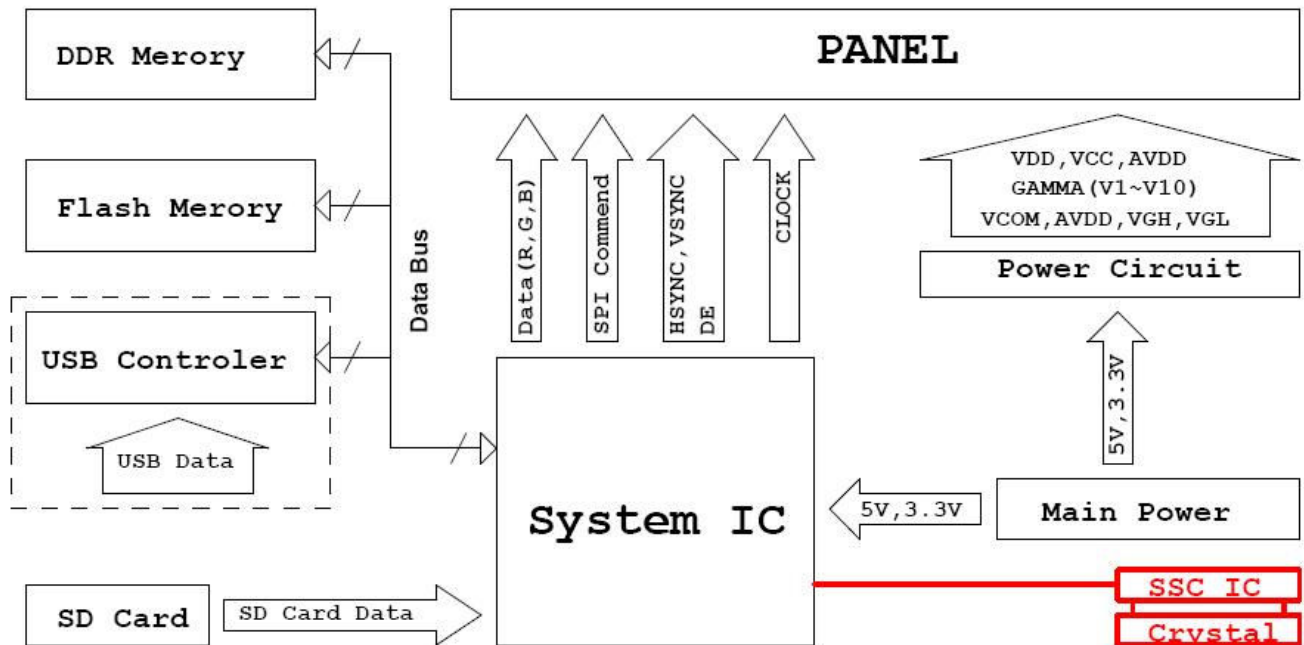4.THE BENDING RADIUS OF FPC SHOULD BE LARGER THAN 0.6mm.

Fig.1-(a) Outline dimension of TFT-LCD module (Front side)

Fig.1-(b) Outline dimension of TFT-LCD module (Back side)

G. Suggestion- System block

According to there are some risks of EMI issue.
Please refer to this function block before design.
If add SSC (Spread Spectrum Clocking) IC on the clock of system may cause
USB abnormal work. Please add USB controller to control USB data.