

NLT Technologies, Ltd.

TFT MONOCHROME LCD MODULE

NL204153AM21-18A

54cm (21.3 Type)

QXGA

LVDS interface (4 ports)

DATA SHEET

DOD-PP-2134 (3rd edition)



**This DATA SHEET is updated document from
DOD-PP-1620(2).**

**All information is subject to change without notice.
Please confirm the sales representative before
starting to design your system.**

INTRODUCTION



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The **Standard**: Applications as any failure, malfunction or error of the products are free from any damage to death, human bodily injury or other property (Products Safety Issue) and not related the safety of the public (Social Issues), like general electric devices.

Examples: Office equipment, audio and visual equipment, communication equipment, test and measurement equipment, personal electronic equipment, home electronic appliances, car navigation system (with no vehicle control functions), seat entertainment monitor for vehicles and airplanes, fish finder (except marine radar integrated type), PDA, etc.

The **Special**: Applications as any failure, malfunction or error of the products might directly cause any damage to death, human bodily injury or other property (Products Safety Issue) and the safety of the public (Social Issues) and required high level reliability by conventional wisdom.

Examples: Vehicle/train/ship control system, traffic signals system, traffic information control system, air traffic control system, surgery/operation equipment monitor, disaster/crime prevention system, etc.

The **Specific**: Applications as any failure, malfunction or error of the products might severe cause any damage to death, human bodily injury or other property (Products Safety Issue) and the safety of the public (Social Issues) and developed, designed and manufactured in accordance with the standards or quality assurance program designated by the customer who requires extremely high level reliability and quality.

Examples: Aerospace system (except seat entertainment monitor), nuclear control system, life support system, etc.

The quality grade of this product is the "**Standard**" unless otherwise specified in this document.

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1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Monochrome LCD module NL204153AM21-18A is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a monochrome-filter glass substrate.

Grayscale data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Monochrome images are created by regulating the amount of transmitted light through the TFT array.

1.2 APPLICATION

- Monochrome monitor system

1.3 FEATURES

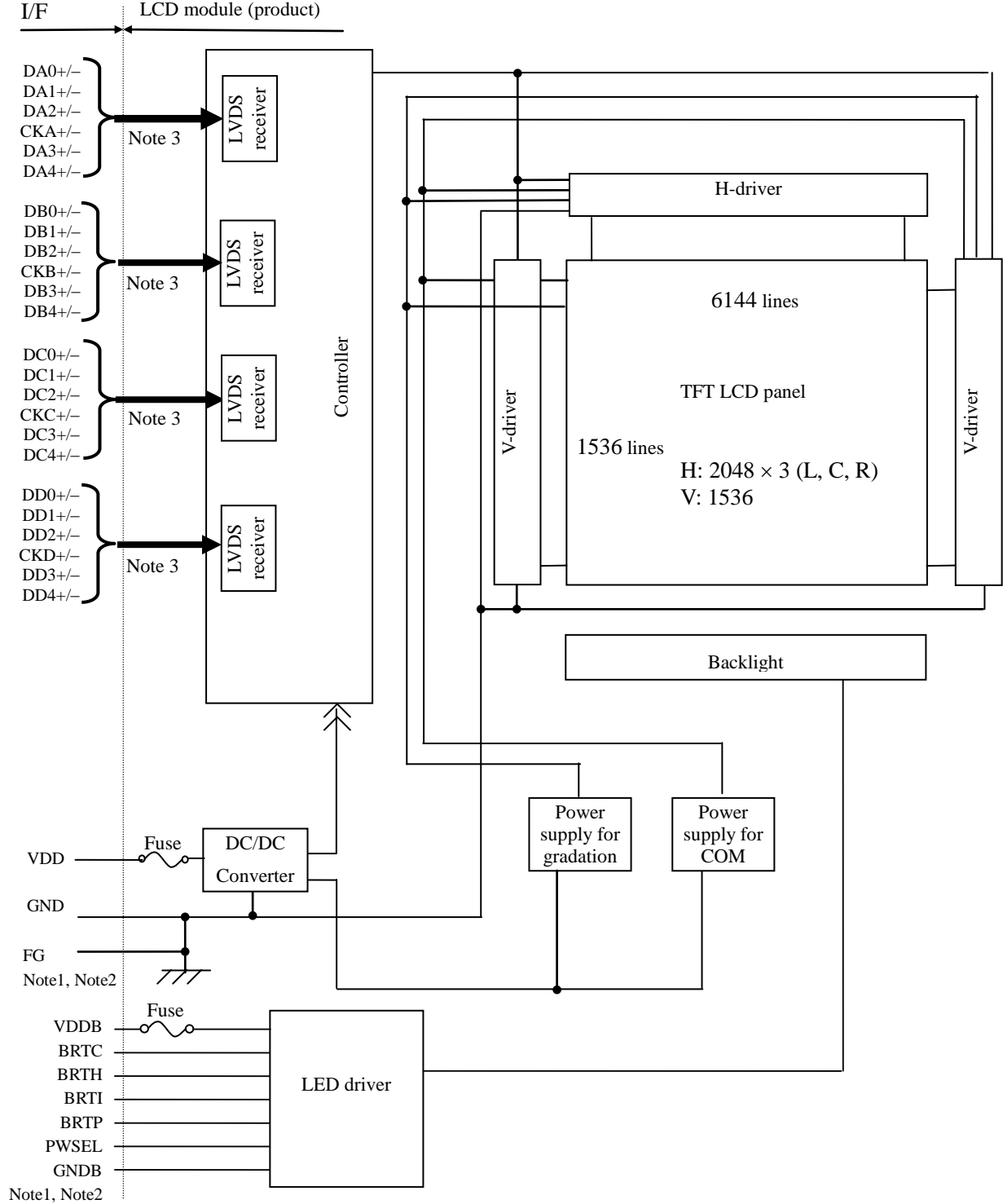
- Ultra-wide viewing angle (Super Fine TFT (SFT))
- High luminance
- High contrast
- Low reflection
- 1,024 gray scales per 1 sub-pixel (10-bit)
- LVDS interface
- Small foot print
- Long life LED backlight
- Built in LED driver
- Compliant with the European RoHS directive (2011/65/EU)
- Acquisition product for UL60950-1/CSA C22.2 No.60950-1-03 (File number: E170632)

2. GENERAL SPECIFICATIONS

Display area	433.152 (H) × 324.864 (V) mm
Diagonal size of display	54cm (21.3 inches)
Drive system	a-Si TFT active matrix
Display grayscale	1,024 gray scales per 1 sub-pixel (10-bit) (3,072 gray scales per 1 pixel)
Pixel	2,048 (H) × 1,536 (V) pixels (1 pixel consists of 3 sub-pixels (LCR).)
Pixel arrangement	LCR vertical stripe
Sub-pixel pitch	0.0705 (H) × 0.2115 (V) mm
Pixel pitch	0.2115 (H) × 0.2115 (V) mm
Module size	457.0 (W) × 350.0 (H) × 21.5 (D) mm (typ.)
Weight	2,700 g (typ.)
Contrast ratio	1,400:1 (typ.)
Viewing angle	At the contrast ratio $\geq 10:1$ <ul style="list-style-type: none"> • Horizontal: Right side 88° (typ.), Left side 88° (typ.) • Vertical: Up side 88° (typ.), Down side 88° (typ.)
Designed viewing direction	Viewing angle with optimum grayscale ($\gamma \approx \text{DICOM}$): Normal axis (perpendicular) Note1
Polarizer surface	Antiglare
Polarizer pencil-hardness	2H (min.) [by JIS K5600]
Response time	$T_{on} + T_{off}$ (10% \longleftrightarrow 90%) 40ms (typ.)
Luminance	At the maximum luminance control 1,700cd/m ² (typ.)
Signal system	4 ports LVDS interface (THC63LVD104S×2pcs, THine Electronics, Inc. or equivalent) [LCR 10-bit signals, Data enable signal (DE), Dot clock (CK)]
Power supply voltage	LCD panel signal processing board: 12.0V LED driver: 12.0V
Backlight	LED backlight built in LED driver
Power consumption	At checkered flag pattern, the maximum luminance control 37.0W (typ.)

Note1: When the product luminance is 450cd/m², the gamma characteristic is designed to $\gamma \approx \text{DICOM}$.

3. BLOCK DIAGRAM



Note1: Relations between GND (Signal ground), FG (Frame ground) and GNDB (LED driver board ground) in the LCD module are as follows.

GND - FG	Connected
GND - GNDB	Not connected
FG - GNDB	Not connected

Note2: GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that these grounds to be connected together in customer equipment.

Note3: Each pair of the LVDS signal lines has 100Ω terminating resistance.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	457.0 ±0.5 (W) × 350.0 ±0.5 (H) × 21.5 (typ., D) 23.0 (max. D) Note1, Note2	mm
Display area	433.152 (H) × 324.864 (V) Note2	mm
Weight	2,700 (typ.), 2,980 (max.)	g

Note1: Excluding warpage of the cover for LED driver board.

Note2: See "8. OUTLINE DRAWINGS".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board		VDD	-0.3 to +14.0	V	-
	LED driver		VDDDB	-0.3 to +15.0	V	
Input voltage for signals	LCD panel signal processing board Note1		Vi	-0.3 to +2.8	V	VDD= 12.0V
	LED driver	BRTI signal	VBI	-0.3 to +1.5	V	VDDDB= 12.0V
		BRTP signal	VBP	-0.3 to +5.5	V	
		BRTC signal	VBC	-0.3 to +5.5	V	
		PWSEL signal	VBS	-0.3 to +5.5	V	
Storage temperature Note6		Tst	-20 to +60	°C	-	
Operating temperature		Front surface	TopF	0 to +60	°C	Note2
		Rear surface	TopR	0 to + 60	°C	Note3
Relative humidity Note4			RH	≤ 95	%	Ta ≤ 40°C
				≤ 85	%	40°C < Ta ≤ 50°C
				≤ 70	%	50°C < Ta ≤ 55°C
Absolute humidity Note4			AH	≤ 73 Note5	g/m ³	Ta > 55°C
Operating altitude			-	≤ 5,100	m	0°C ≤ Ta ≤ 55°C
Storage altitude			-	≤ 13,600	m	-20°C ≤ Ta ≤ 60°C

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

Note2: Measured at LCD panel surface (including self-heat)

Note3: Measured at LCD module's rear shield surface (including self-heat)

Note4: No condensation

Note5: Water amount at T_a = 55°C and RH = 70%

Note6: The image quality may cause degradation in case of rapid change humidity and temperature.

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta= 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	10.8	12.0	13.2	V	-
Power supply current		IDD	-	590 Note1	980 Note2	mA	at VDD= 12.0V
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input threshold voltage	High	VTH	-	-	+100	mV	at VCM= 1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	Note4
Terminating resistance		RT	-	100	-	Ω	-

Note1: Checkered flag pattern (by EIAJ ED-2522)

Note2: Pattern for maximum current

Note3: Common mode voltage for LVDS driver

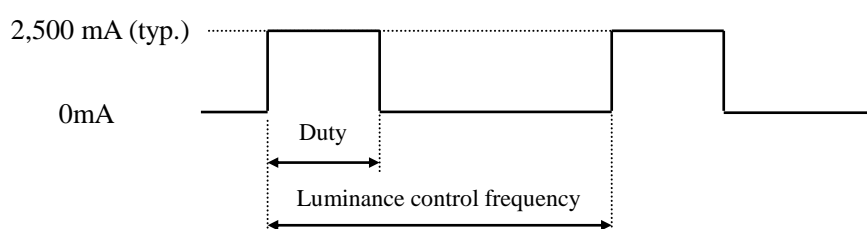
Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

4.3.2 LED driver

(Ta= 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDDB	11.4	12.0	12.6	V	-
Power supply current		IDDB	-	2,500	3,300	mA	VDDB= 12.0V, At the maximum luminance control
Input voltage for signals	BRTI signal		VBI	0	-	1.0	V
	BRTP signal	High	VBPH	2.0	-	5.25	V
		Low	VBPL	0	-	0.8	V
	BRTC signal	High	VBCH	2.0	-	5.25	V
		Low	VBCL	0	-	0.8	V
	PWSEL signal	High	VBSH	2.0	-	5.25	V
		Low	VBSL	0	-	0.8	V
							-
Input current for signals	BRTI signal		IBI	-200	-	-100	μA
	BRTP signal	High	IBPH	-	-	1,000	μA
		Low	IBPL	-600	-	-	μA
	BRTC signal	High	IBCH	-	-	300	μA
		Low	IBCL	-300	-	-	μA
	PWSEL signal	High	IPSH	-	-	1,000	μA
		Low	IPSL	-600	-	-	μA

4.3.3 Current wave for LED driver



Duty: At the maximum luminance control 100% to at the minimum luminance control 1%.
Luminance control frequency: 270Hz (typ.)

Note1: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "**4.6.2 Detail of BRTP timing**".

Note2: The power supply lines (VDDB and GNDB) have large ripple voltage during luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on.



4.3.4 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

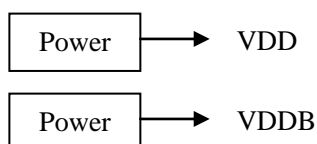
Power supply voltage		Ripple voltage (Measure at input terminal of power supply)	Note1	Unit
VDD	12.0V	≤ 100		mVp-p
VDDB	12.0V	≤ 200		mVp-p

Note1: The permissible ripple voltage includes spike noise.

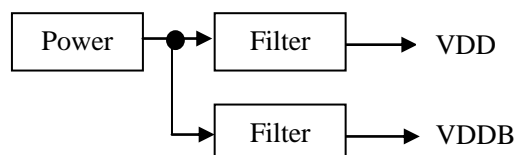


Example of the power supply connection

a) Separate the power supply



b) Put in the filter



4.3.5 Fuse

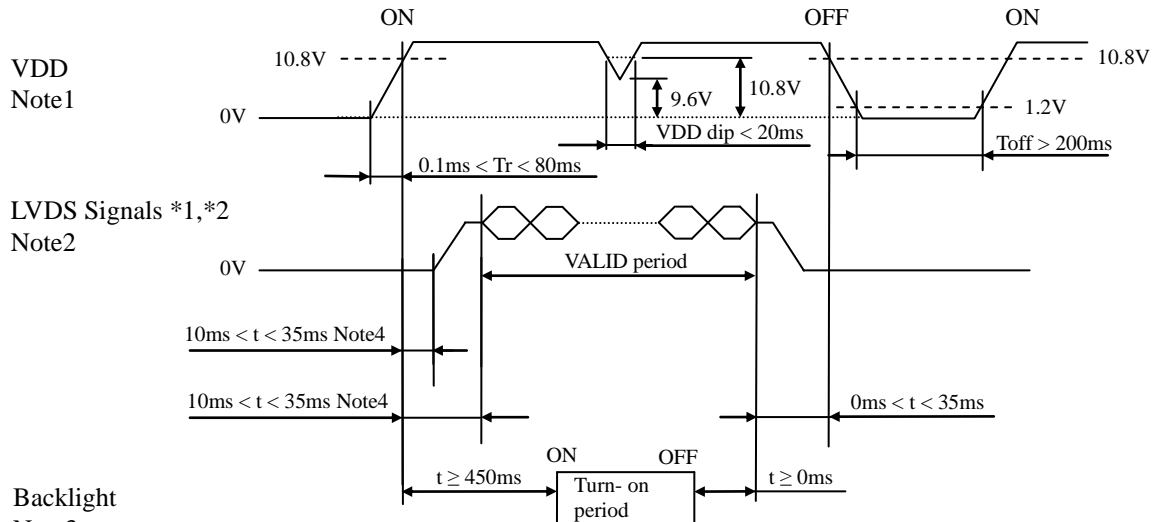
Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16202AB	KAMAYA ELECTRIC Co., Ltd.	2.0 A	4.0A, 5 seconds maximum	Note1
			32 V		
VDDB	CCF1N10	KOA Corporation	10 A	20 A, 1 seconds maximum	
			60 V		

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.



4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board



*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

*2: LVDS signals should be measured at the terminal of $100\ \Omega$ resistance.

Note1: If there is a voltage variation (voltage drop) at the rising edge of VDD below 10.8V, there is a possibility that a product does not work due to a protection circuit.

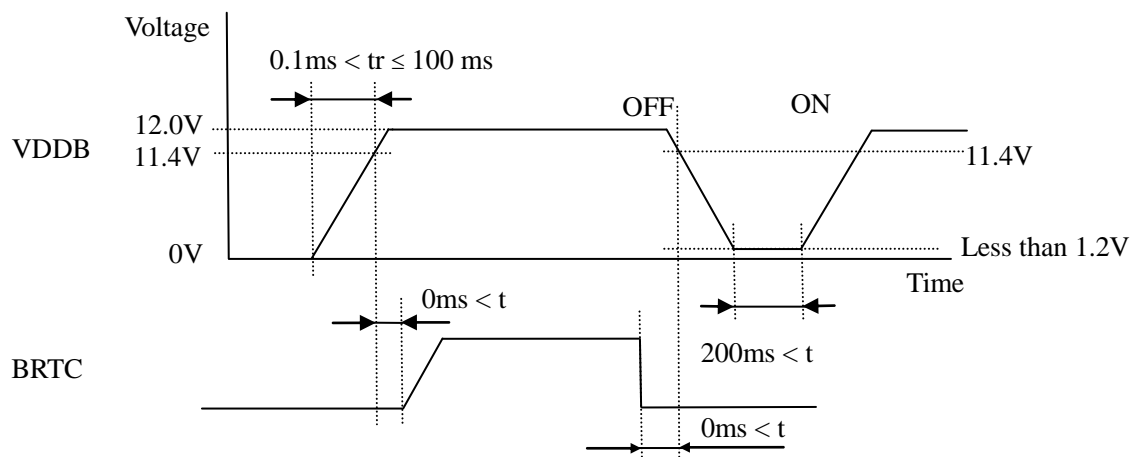
Note2: LVDS signals must be set to Low or High-impedance, except the VALID period (See above sequence diagram), in order to avoid the circuitry damage.

If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. If a customer stops the display and function signals, VDD also must be shut down.

Note3: The backlight should be turned on within the turn-on period, in order to avoid unstable data display.

Note4: After turning VDD on, terminal voltages on LVDS input terminals (*1) will rise. This is caused by initial operation of the product.

4.4.2 LED driver



Note1: If t_r is more than 100 ms, the backlight will be turned off by a protection circuit for LED driver board.

Note2: When VDDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-RE51S-HF (Japan Aviation Electronics Industry Limited (JAE))

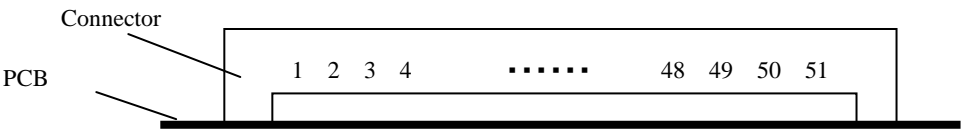
Adaptable plug: FI-RE51HL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	
3	GND	Ground	
4	DA0-	Pixel data A0	LVDS differential data input Note2
5	DA0+		
6	GND	Ground	Note1
7	DA1-	Pixel data A1	LVDS differential data input Note2
8	DA1+		
9	GND	Ground	Note1
10	DA2-	Pixel data A2	LVDS differential data input Note2
11	DA2+		
12	GND	Ground	Note1
13	CKA-	Pixel clock A	LVDS differential data input Note2
14	CKA+		
15	GND	Ground	Note1
16	DA3-	Pixel data A3	LVDS differential data input Note2
17	DA3+		
18	GND	Ground	Note1
19	DA4-	Pixel data A4	LVDS differential data input Note2
20	DA4+		
21	GND	Ground	Note1
22	DB0-	Pixel data B0	LVDS differential data input Note2
23	DB0+		
24	GND	Ground	Note1
25	DB1-	Pixel data B1	LVDS differential data input Note2
26	DB1+		
27	GND	Ground	Note1
28	DB2-	Pixel data B2	LVDS differential data input Note2
29	DB2+		
30	GND	Ground	Note1
31	CKB-	Pixel clock B	LVDS differential data input Note2
32	CKB+		
33	GND	Ground	Note1
34	DB3-	Pixel data B3	LVDS differential data input Note2
35	DB3+		
36	GND	Ground	Note1
37	DB4-	Pixel data B4	LVDS differential data input Note2
38	DB4+		
39	GND	Ground	Note1

Continued

40	GND	Ground	Note1
41	RSVD	-	Keep this pin Open.
42	RSVD	-	Keep this pin Open.
43	RSVD	-	Keep this pin Open.
44	RSVD	-	Keep this pin Open.
45	GND	Ground	Note1
46	GND	Ground	Note1
47	GND	Ground	Note1
48	RSVD	-	Keep this pin Open.
49	RSVD	-	Keep this pin Open.
50	RSVD	-	Keep this pin Open.
51	GND	Ground	Note1

CN1: Insert surface side



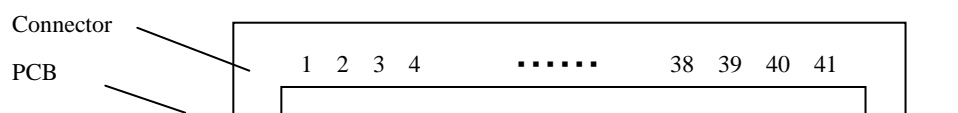
- Note1: All GND terminals should be used without any non-connected lines.
- Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN2 socket (LCD module side): FI-RE41S-HF (Japan Aviation Electronics Industry Limited (JAE))

Adaptable plug: FI-RE41HL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	
3	GND	Ground	
4	DC0-	Pixel data C0	LVDS differential data input Note2
5	DC0+		
6	GND	Ground	Note1
7	DC1-	Pixel data C1	LVDS differential data input Note2
8	DC1+		
9	GND	Ground	Note1
10	DC2-	Pixel data C2	LVDS differential data input Note2
11	DC2+		
12	GND	Ground	Note1
13	CKC-	Pixel clock C	LVDS differential data input Note2
14	CKC+		
15	GND	Ground	Note1
16	DC3-	Pixel data C3	LVDS differential data input Note2
17	DC3+		
18	GND	Ground	Note1
19	DC4-	Pixel data C4	LVDS differential data input Note2
20	DC4+		
21	GND	Ground	Note1
22	DD0-	Pixel data D0	LVDS differential data input Note2
23	DD0+		
24	GND	Ground	Note1
25	DD1-	Pixel data D1	LVDS differential data input Note2
26	DD1+		
27	GND	Ground	Note1
28	DD2-	Pixel data D2	LVDS differential data input Note2
29	DD2+		
30	GND	Ground	Note1
31	CKD-	Pixel clock D	LVDS differential data input Note2
32	CKD+		
33	GND	Ground	Note1
34	DD3-	Pixel data D3	LVDS differential data input Note2
35	DD3+		
36	GND	Ground	Note1
37	DD4-	Pixel data D4	LVDS differential data input Note2
38	DD4+		
39	GND	Ground	Note1
40	GND	Ground	Note1
41	GND	Ground	Note1

CN2: Insert surface side



Note1: All GND terminals should be used without any non-connected lines.

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

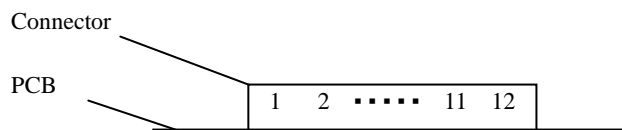
CN3 socket (LCD module side): 53261-1271 (MOLEX Inc.)



Adaptable plug: 51021-1200 (MOLEX Inc.)

Pin No.	Symbol	Function	Description
1	GND	Signal ground	Note1
2	GND		
3	GND		
4	GND		
5	GND		
6	GND		
7	VDD	Power supply	Note1
8	VDD		
9	VDD		
10	VDD		
11	VDD		
12	VDD		

CN3: Insert surface side



Note1: All VDD and GND terminals should be used without any non-connected lines.

4.5.2 LED driver

CN201 socket (LCD module side): DF3Z-10P-2H (2*) (HIROSE ELECTRIC Co.,Ltd.)

Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co.,Ltd.)

Pin No.	Symbol	Function	Description
1	GNDB	LED driver ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

Note1: All VDDB and GNDB terminals should be used without any non-connected lines.

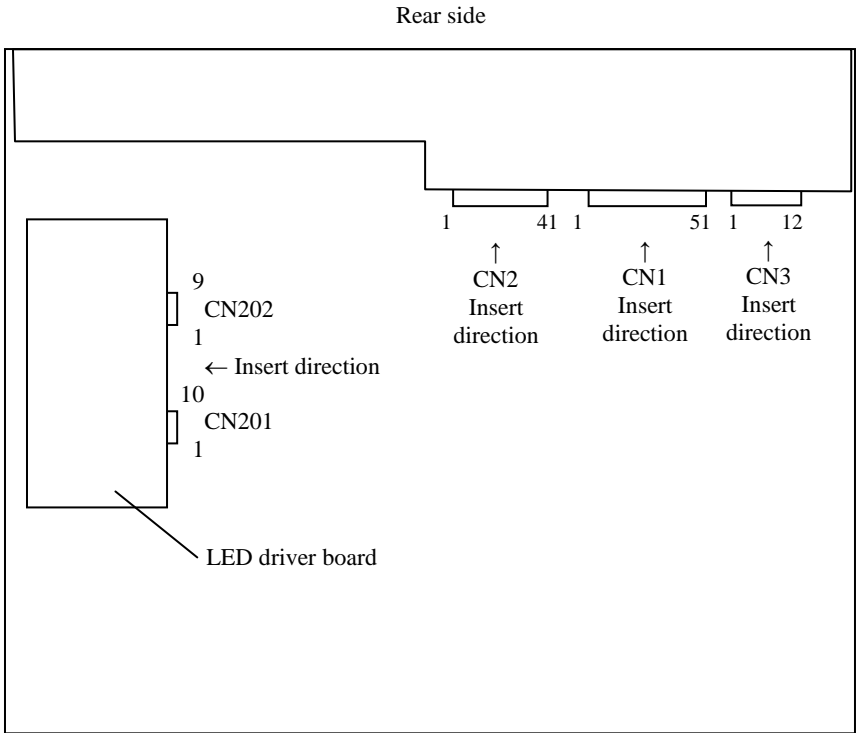
CN202 socket (LCD module side): 53261-0971 (MOLEX Inc.)
Adaptable plug: 51021-0900 (MOLEX Inc.)



Pin No.	Symbol	Function	Description
1	PWSEL	Selection of luminance control signal method	Note2, Note3
2	GNDB	LED driver ground	Note1
3	BRTP	BRTP signal	Note2
4	BRTI	Luminance control terminal	
5	BRTH		
6	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
7	N. C.	-	Keep this pin Open.
8	GNDB	LED driver ground	Note1
9	GNDB		

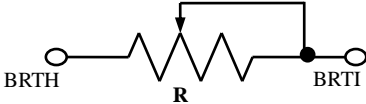
Note1: All GNDB terminals should be used without any non-connected lines.
Note2: See "4.6 LUMINANCE CONTROL".
Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5.3 Positions of socket



4.6 LUMINANCE CONTROL

4.6.1 Luminance control methods

Method	Adjustment and luminance ratio	PWSEL terminal	BRTP terminal						
<div>Variable resistor control</div> <div>Note1</div>	<div><div>• Adjustment</div><p>The variable resistor (R) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance. The resistor (R) must be connected between BRTH-BRTI terminals.</p><div></div><div>• Luminance ratio Note3</div><table><tr><th>Resistance</th><th>Luminance ratio</th></tr><tr><td>0Ω</td><td>0% (Min. Luminance)</td></tr><tr><td>10 kΩ</td><td>100% (Max. Luminance)</td></tr></table></div>	Resistance	Luminance ratio	0Ω	0% (Min. Luminance)	10 kΩ	100% (Max. Luminance)	High or Open	Open
Resistance	Luminance ratio								
0Ω	0% (Min. Luminance)								
10 kΩ	100% (Max. Luminance)								
<div>Voltage control</div> <div>Note1</div>	<div><div>• Adjustment</div><p>Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance. Luminance is the maximum when BRTI terminal is Open.</p><div>• Luminance ratio Note3</div><table><tr><th>BRTI Voltage (VBI)</th><th>Luminance ratio</th></tr><tr><td>0V</td><td>0% (Min. Luminance)</td></tr><tr><td>1.0V</td><td>100% (Max. Luminance)</td></tr></table></div>	BRTI Voltage (VBI)	Luminance ratio	0V	0% (Min. Luminance)	1.0V	100% (Max. Luminance)		
BRTI Voltage (VBI)	Luminance ratio								
0V	0% (Min. Luminance)								
1.0V	100% (Max. Luminance)								
<div>Pulse width modulation</div> <div>Note1 Note2 Note4</div>	<div><div>• Adjustment</div><p>Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal.</p><div>• Luminance ratio Note3</div><table><tr><th>Duty ratio</th><th>Luminance ratio</th></tr><tr><td>0.01</td><td>1% (Min. Luminance) (At frequency: 325 Hz)</td></tr><tr><td>1.0</td><td>100% (Max. Luminance)</td></tr></table></div>	Duty ratio	Luminance ratio	0.01	1% (Min. Luminance) (At frequency: 325 Hz)	1.0	100% (Max. Luminance)	Low	BRTP signal
Duty ratio	Luminance ratio								
0.01	1% (Min. Luminance) (At frequency: 325 Hz)								
1.0	100% (Max. Luminance)								

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.

Use PWM method, if interference noises appear on the display image!

Note2: The LED driver board will stop working, if the Low period of BRTP signal is more than 50ms while BRTP signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The LED driver board will start to work when power is supplied again.

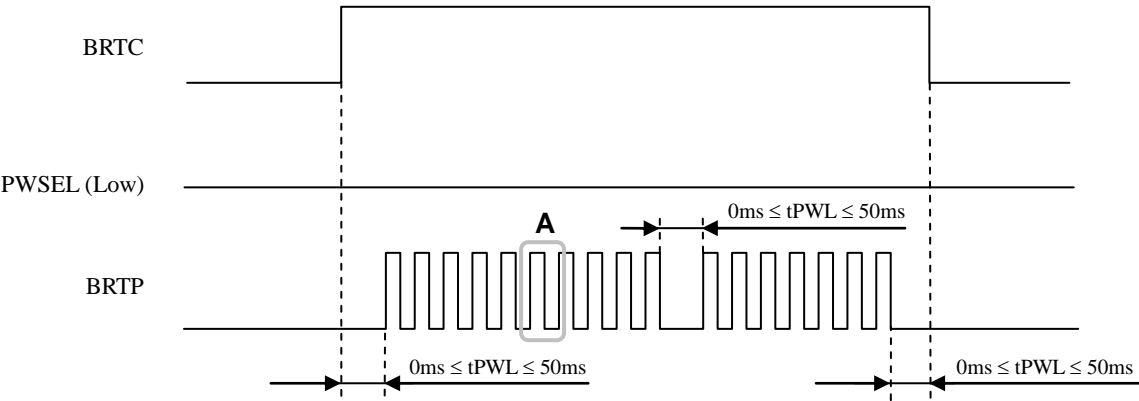
Note3: These data are the target values.

Note4: See "4.6.2 Detail of BRTP timing".

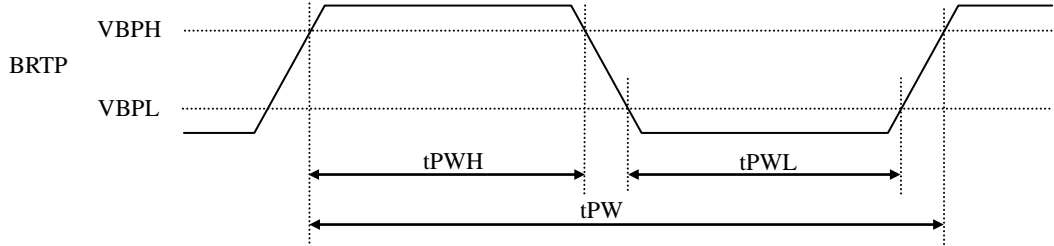
4.6.2 Detail of B RTP timing

(1) Timing diagrams

• Outline chart



• Detail of A part



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
PWM frequency	f_{PWM}	185	-	1k	Hz	Note1,2,3
PWM duty ratio	DR_{PWM}	1	-	100	%	Note4,5
PWM pulse width	tPWH	30	-	-	μs	Note1,4,5

Note1: Definition of parameters is as follows.

$$f_{\text{PWM}} = \frac{1}{t_{\text{PW}}}, \quad \text{DR}_{\text{PWM}} = \frac{t_{\text{PWH}}}{t_{\text{PW}}}$$

Note2: A recommended f_{PWM} value is as follows.

$$f_{\text{PWM}} = \frac{2n-1}{4} \times f_v$$

(n= integer, f_v = frame frequency of LCD module)

Note3: Depending on the frequency used, some noise may appear on the screen, please conduct a thorough evaluation.

Note4: While the BRTC signal is high, do not set the tPWH (PWM pulse width) is less than 30 μs . It may cause abnormal working of the backlight. In this case, turn the backlight off and then on again by BRTC signal.

Note5: Regardless of the PWM frequency, both PWM duty ratio and PWM pulse width must be always more than the minimum values.

4.7 METHOD OF CONNECTION FOR LVDS TRANSMITTER

	Bit mapping	Transmitter Pin Assign		Output Connector		CN1	
		Single type LVDS Tx	Dual type LVDS Tx Thine THC63LVD1023B			Pin No.	Signal Name
odd Pixel data A	LA4	TA0	R14	ATA-	→	-	-
	LA5	TA1	R15			4	DA0-
	LA6	TA2	R16			5	DA0+
	LA7	TA3	R17			-	-
	LA8	TA4	R18			7	DA1-
	LA9	TA5	R19			8	DA1+
	CA4	TA6	G14	ATB-	→	-	-
	CA5	TB0	G15			10	DA2-
	CA6	TB1	G16			11	DA2+
	CA7	TB2	G17			-	-
	CA8	TB3	G18			16	DA3-
	CA9	TB4	G19			17	DA3+
	RA4	TB5	B14	ATC-	→	-	-
	RA5	TB6	B15			19	DA4-
	RA6	TC0	B16			20	DA4+
	RA7	TC1	B17			-	-
	RA8	TC2	B18			13	CKA-
	RA9	TC3	B19			14	CKA+
	Hsync	TC4	Hsync	ATD-	→	-	-
	Vsync	TC5	Vsync			22	DB0-
	DE	TC6	DE			23	DB0+
	LA2	TD0	R12			-	-
	LA3	TD1	R13			25	DB1-
	CA2	TD2	G12			26	DB1+
	CA3	TD3	G13	ATE-	→	-	-
	RA2	TD4	B12			28	DB2-
	RA3	TD5	B13			29	DB2+
	N.C.	TD6	-			-	-
	LA0	TE0	R10			34	DB3-
	LA1	TE1	R11			35	DB3+
	CA0	TE2	G10	ATE+	→	-	-
	CA1	TE3	G11			37	DB4-
	RA0	TE4	B10			38	DB4+
	RA1	TE5	B11			-	-
	N.C.	TE6	-			31	CKB-
	CLK	CLK	CLK	ATCLK- ATCLK+	→	32	CKB+
even Pixel data B	LB4	TA0	R14	BTA-	→	-	-
	LB5	TA1	R15			22	DB0-
	LB6	TA2	R16			23	DB0+
	LB7	TA3	R17			-	-
	LB8	TA4	R18			25	DB1-
	LB9	TA5	R19			26	DB1+
	CB4	TA6	G14	BTB-	→	-	-
	CB5	TB0	G15			28	DB2-
	CB6	TB1	G16			29	DB2+
	CB7	TB2	G17			-	-
	CB8	TB3	G18			34	DB3-
	CB9	TB4	G19			35	DB3+
	RB4	TB5	B14	BTC-	→	-	-
	RB5	TB6	B15			37	DB4-
	RB6	TC0	B16			38	DB4+
	RB7	TC1	B17			-	-
	RB8	TC2	B18			31	CKB-
	RB9	TC3	B19			32	CKB+
	Hsync	TC4	Hsync	BTD-	→	-	-
	Vsync	TC5	Vsync			22	DB0-
	DE	TC6	DE			23	DB0+
	LB2	TD0	R12			-	-
	LB3	TD1	R13			25	DB1-
	CB2	TD2	G12			26	DB1+
	CB3	TD3	G13	BTE-	→	-	-
	RB2	TD4	B12			28	DB2-
	RB3	TD5	B13			29	DB2+
	N.C.	TD6	-			-	-
	LB0	TE0	R10			34	DB3-
	LB1	TE1	R11			35	DB3+
	CB0	TE2	G10	BTE+	→	-	-
	CB1	TE3	G11			37	DB4-
	RB0	TE4	B10			38	DB4+
	RB1	TE5	B11			-	-
	N.C.	TE6	-			31	CKB-
	CLK	CLK	CLK	BTCLK- BTCLK+	→	32	CKB+

	Bit mapping	Transmitter Pin Assign		Output Connector		CN2	
		Single type LVDS Tx	Dual type LVDS Tx Thine THC63LVD1023B			Pin No.	Signal Name
odd Pixel data C	LC4	TA0	R14	CTA-	→	-	-
	LC5	TA1	R15			4	DC0-
	LC6	TA2	R16			5	DC0+
	LC7	TA3	R17			-	-
	LC8	TA4	R18			7	DC1-
	LC9	TA5	R19			8	DC1+
	CC4	TA6	G14	CTB-	→	-	-
	CC5	TB0	G15			10	DC2-
	CC6	TB1	G16			11	DC2+
	CC7	TB2	G17			-	-
	CC8	TB3	G18			16	DC3-
	CC9	TB4	G19			17	DC3+
	RC4	TB5	B14	CTC-	→	-	-
	RC5	TB6	B15			19	DC4-
	RC6	TC0	B16			20	DC4+
	RC7	TC1	B17			-	-
	RC8	TC2	B18			13	CKC-
	RC9	TC3	B19			14	CKC+
	Hsync	TC4	Hsync	CTD-	→	-	-
	Vsync	TC5	Vsync			22	DD0-
	DE	TC6	DE			23	DD0+
	LC2	TD0	R12			-	-
	LC3	TD1	R13			25	DD1-
	CC2	TD2	G12			26	DD1+
	CC3	TD3	G13	CTE-	→	-	-
	RC2	TD4	B12			28	DD2-
	RC3	TD5	B13			29	DD2+
	N.C.	TD6	-			-	-
	LC0	TE0	R10			34	DD3-
	LC1	TE1	R11			35	DD3+
	CC0	TE2	G10	CTE+	→	-	-
	CC1	TE3	G11			37	DD4-
	RC0	TE4	B10			38	DD4+
	RC1	TE5	B11			-	-
	N.C.	TE6	-			31	CKD-
	CLK	CLK	CLK	CTCLK-CTCLK+	→	32	CKD+
even Pixel data D	LD4	TA0	R14	DTA-	→	-	-
	LD5	TA1	R15			22	DD0-
	LD6	TA2	R16			23	DD0+
	LD7	TA3	R17			-	-
	LD8	TA4	R18			25	DD1-
	LD9	TA5	R19			26	DD1+
	CD4	TA6	G14	DTB-	→	-	-
	CD5	TB0	G15			28	DD2-
	CD6	TB1	G16			29	DD2+
	CD7	TB2	G17			-	-
	CD8	TB3	G18			34	DD3-
	CD9	TB4	G19			35	DD3+
	RD4	TB5	B14	DTC-	→	-	-
	RD5	TB6	B15			37	DD4-
	RD6	TC0	B16			38	DD4+
	RD7	TC1	B17			-	-
	RD8	TC2	B18			31	CKD-
	RD9	TC3	B19			32	CKD+
	Hsync	TC4	Hsync	DTD-	→	-	-
	Vsync	TC5	Vsync			22	DD0-
	DE	TC6	DE			23	DD0+
	LD2	TD0	R12			-	-
	LD3	TD1	R13			25	DD1-
	CD2	TD2	G12			26	DD1+
	CD3	TD3	G13	DTE-	→	-	-
	RD2	TD4	B12			28	DD2-
	RD3	TD5	B13			29	DD2+
	N.C.	TD6	-			-	-
	LD0	TE0	R10			34	DD3-
	LD1	TE1	R11			35	DD3+
	CD0	TE2	G10	DTE+	→	-	-
	CD1	TE3	G11			37	DD4-
	RD0	TE4	B10			38	DD4+
	RD1	TE5	B11			-	-
	N.C.	TE6	-			31	CKD-
	CLK	CLK	CLK	DTCLK-DTCLK+	→	32	CKD+

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

4.8 DISPLAY GRAYSCALE AND INPUT DATA SIGNALS

This product can display 1,024 gray scales in each LCR sub-pixel and 3,072 gray scales per 1 pixel. Also the relation between display gray scale and input data signals is as follows.

Display gray scale		Data signal (0: Low level, 1: High level)																															
		LA9 LA8 LA7 LA6 LA5 LA4 LA3 LA2 LA1 LA0										CA9 CA8 CA7 CA6 CA5 CA4 CA3 CA2 CA1 CA0										RA9 RA8 RA7 RA6 RA5 RA4 RA3 RA2 RA1 RA0											
		LB9 LB8 LB7 LB6 LB5 LB4 LB3 LB2 LB1 LB0										CB9 CB8 CB7 CB6 CB5 CB4 CB3 CB2 CB1 CB0										RB9 RB8 RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0											
		LC9 LC8 LC7 LC6 LC5 LC4 LC3 LC2 LC1 LC0										CC9 CC8 CC7 CC6 CC5 CC4 CC3 CC2 CC1 CC0										RD9 RC8 RC7 RC6 RC5 RC4 RC3 RC2 RC1 RC0											
		LD9 LD8 LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0										CD9 CD8CD7 CD6 CD5 CD4 CD3 CD2 CD1 CD0										RD9 RD8 RD7 RD6 RD5 RD4 RD3 RD2 RD1 RD0											
Left sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	dark	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	bright	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
White	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Center sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	
	bright	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
White	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Right sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1
White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	

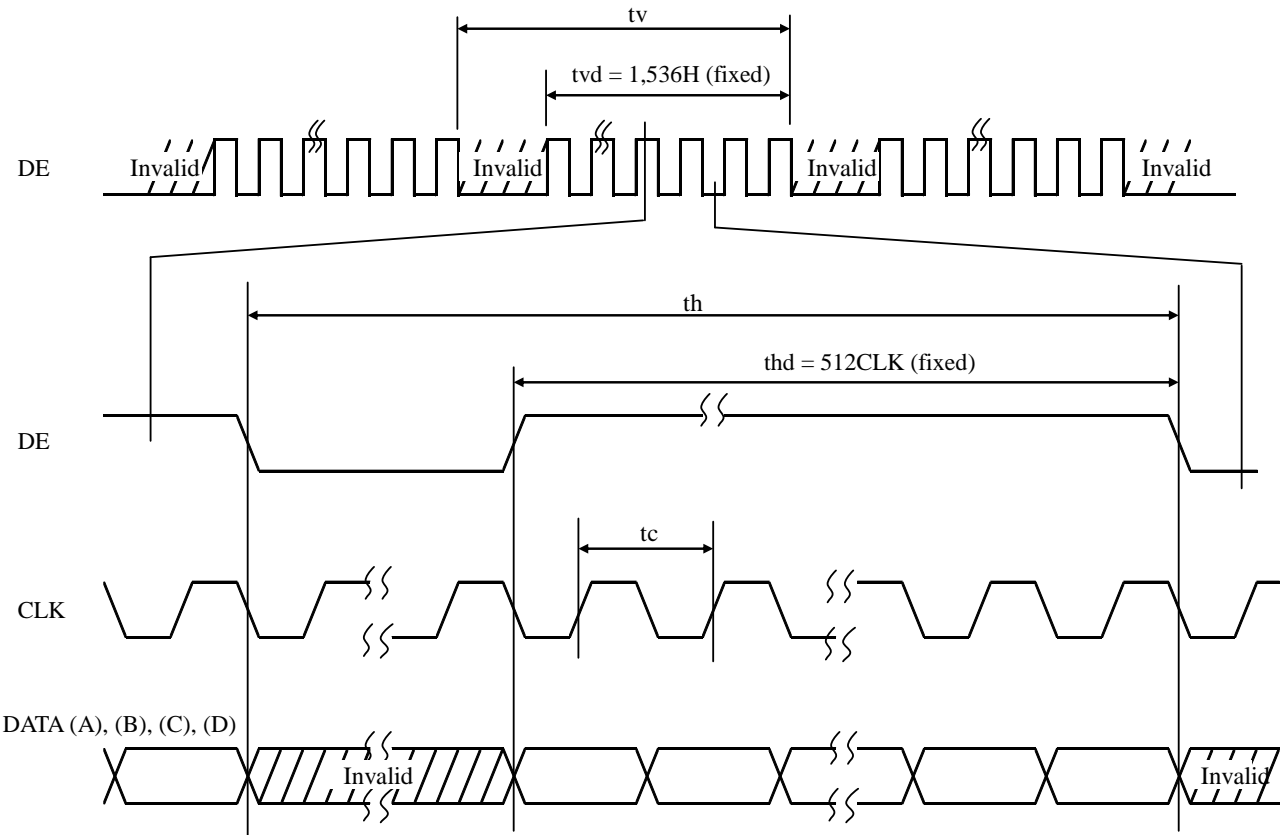
4.9 INPUT SIGNAL TIMINGS

4.9.1 Timing characteristics

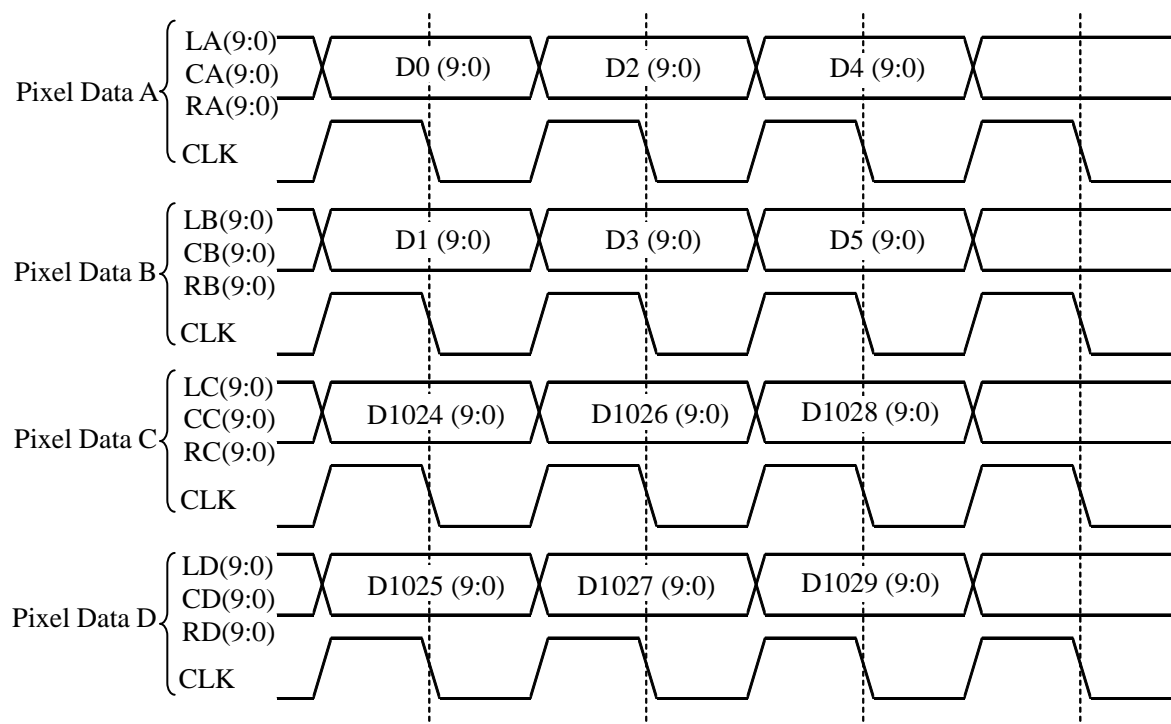
Parameter			Symbol	min.	typ.	max.	Unit	Remarks	
CLK	Frequency		1/ tc	60.0	65.0	66.0	MHz	-	
	Duty ratio		-	See the data sheet of LVDS transmitter.			-	-	
	Rise time, Fall time		-				ns	-	
DE	Horizontal	Cycle	th	10.34	10.34	10.77	μs	96,72kHz(typ.) Note1	
				640	672	700	CLK		
		Display period	thd	512			CLK	-	
	Vertical	Cycle	tv	15.47	16.667	17.9	ms	60.0Hz(typ.)	
				1547	1612	1628	H		
		Display period	tvd	1536			H	-	
	CLK-DE	Setup time	-	See the data sheet of LVDS transmitter.			ns	-	
		Hold time	-				ns	-	
	Rise time, Fall time			-				ns	-

Note1: The sum of jitter and skew of horizontal period should be within ±1 CLK.

4.9.2 Input signal timing chart

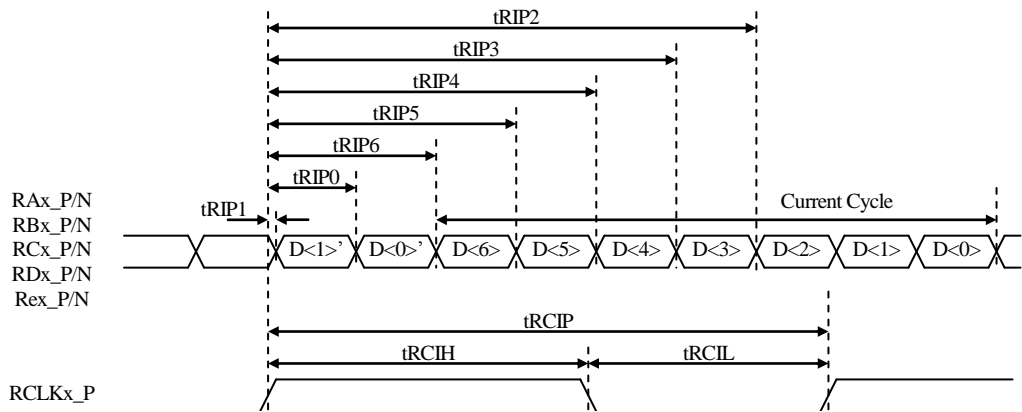


4.10 LVDS DATA TRANSMISSION METHOD



4.11 LVDS Rx AC SPEC

Symbol	Parameter	min.	typ.	max.	Units
t_{RCIP}	RCLKx_P Period	11.76	-	40.0	ns
t_{RCH}	RCLKx_P High pulse width	-	$\frac{4}{7} t_{RCIP}$	-	ns
t_{RCIL}	RCLKx_P Low pulse width	-	$\frac{3}{7} t_{RCIP}$	-	ns
t_{RMG}	Receiver Data Input Margin fCLKIN= 60MHz	-0.65	-	0.65	ns
	fCLKIN= 65MHz				
	fCLKIN= 66MHz				
t_{RIP1}	Input Data Position0	$- t_{RMG} $	0.0	$+ t_{RMG} $	ns
t_{RIP0}	Input Data Position1	$\frac{t_{RCIP}}{7} - t_{RMG} $	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7} + t_{RMG} $	ns
t_{RIP6}	Input Data Position2	$2\frac{t_{RCIP}}{7} - t_{RMG} $	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7} + t_{RMG} $	ns
t_{RIP5}	Input Data Position3	$3\frac{t_{RCIP}}{7} - t_{RMG} $	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7} + t_{RMG} $	ns
t_{RIP4}	Input Data Position4	$4\frac{t_{RCIP}}{7} - t_{RMG} $	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7} + t_{RMG} $	ns
t_{RIP3}	Input Data Position5	$5\frac{t_{RCIP}}{7} - t_{RMG} $	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7} + t_{RMG} $	ns
t_{RIP2}	Input Data Position6	$6\frac{t_{RCIP}}{7} - t_{RMG} $	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7} + t_{RMG} $	ns



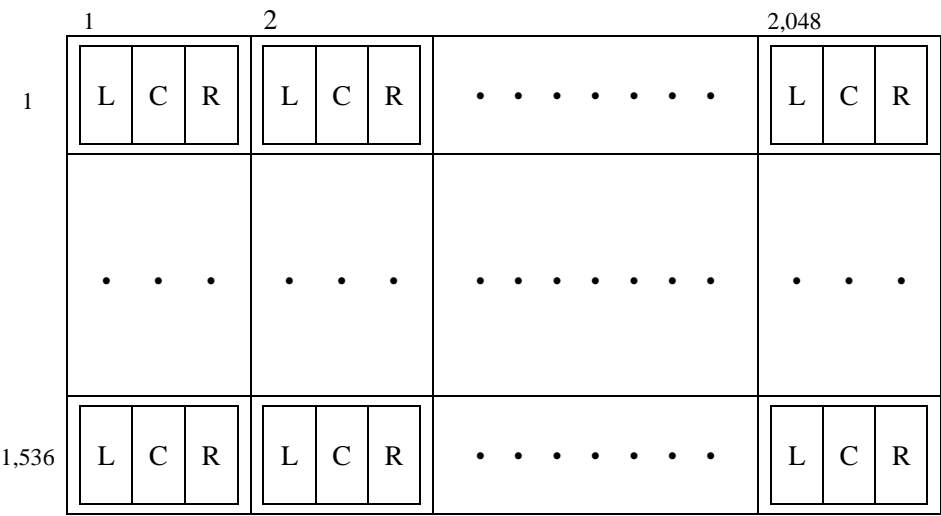
4.12 DISPLAY POSITIONS

Odd pixel: LA= Left data
 CA= Center data
 RA= Right data

Even pixel: LB= Left data
 CB= Center data
 RB= Right data

D (1, 1)			D (2, 1)			D (1025, 1)			D (1026, 1)		
LA	CA	RA	LB	CB	RB	LC	CC	RC	LD	CD	RD
1, 1	2, 1	...	1023, 1	1024, 1	1025, 1	1026, 1	...	2047, 1	2048, 1		
1, 2	2, 2	...	1023, 2	1024, 2	1025, 2	1026, 2	...	2047, 2	2048, 2		
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
1, 1535	2, 1535	...	1023, 1535	1024, 1535	1025, 1535	1026, 1535	...	2047, 1535	2048, 1535		
1, 1536	2, 1536	...	1023, 1536	1024, 1536	1025, 1536	1026, 1536	...	2047, 1536	2048, 1536		

4.13 PIXEL ARRANGNMENT



4.14 OPTICS

4.14.1 Optical characteristics

(Note1, Note2)

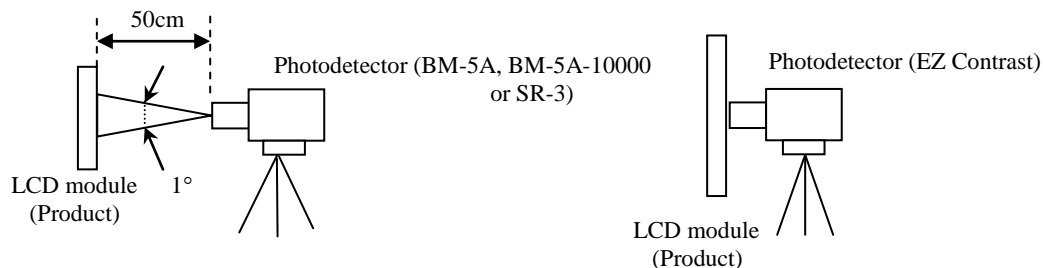
Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance		White at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	L	1,250	1,700	-	cd/m ²	BM-5A or SR-3	Note3
Contrast ratio		White/Black at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	CR	1,000	1,400	-	-	BM-5A or SR-3	Note3 Note5
Luminance uniformity		White θR= 0°, θL= 0°, θU= 0°, θD= 0°	LU	80	-	-	%	BM-5A or SR-3	Note4 Note6
Chromaticity	White	x coordinate	Wx	0.269	0.299	0.329		SR-3	Note3 Note7
		y coordinate	Wy	0.285	0.315	0.345	-		
Response time		Black to White	Ton	-	20	30	ms	BM-5A -10000	Note3 Note8
		White to Black	Toff	-	20	30	ms		
Viewing angle	Right	θU= 0°, θD= 0°, CR≥ 10	θR	70	88	-	°	BM-5A or EZ Contrast	Note3 Note9
	Left	θU= 0°, θD= 0°, CR≥ 10	θL	70	88	-	°		
	Up	θR= 0°, θL= 0°, CR≥ 10	θU	70	88	-	°		
	Down	θR= 0°, θL= 0°, CR≥ 10	θD	70	88	-	°		

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta= 25°C, VDD= 12.0V, VDDb= 12.0V, PWM: Duty 100%, Display mode: QXGA,
Horizontal cycle= 1/96.72 kHz, Vertical cycle= 1/60.0 Hz

Optical characteristics are measured at luminance saturation 20minutes after the product works in the dark room. Also measurement methods are as follows.



Note3: Product surface temperature TopF = 29°C (at the maximum luminance control)

Note4: Product surface temperature TopF = 27°C (at the product luminance 450cd/m²)

LU is measured under the condition of temperature differences in the display area are less than 10°C

Note5: See "4.14.2 Definition of contrast ratio".

Note6: See "4.14.3 Definition of luminance uniformity".

Note7: These coordinates are found on CIE 1931 chromaticity diagram.

Note8: See "4.14.4 Definition of response times".

Note9: See "4.14.5 Definition of viewing angles".

4.14.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

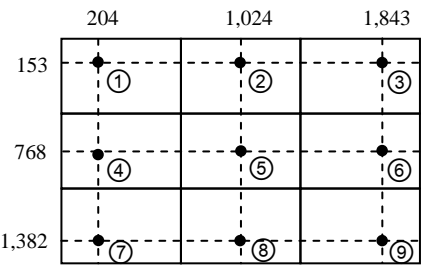
Contrast ratio (CR) = $\frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$

4.14.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

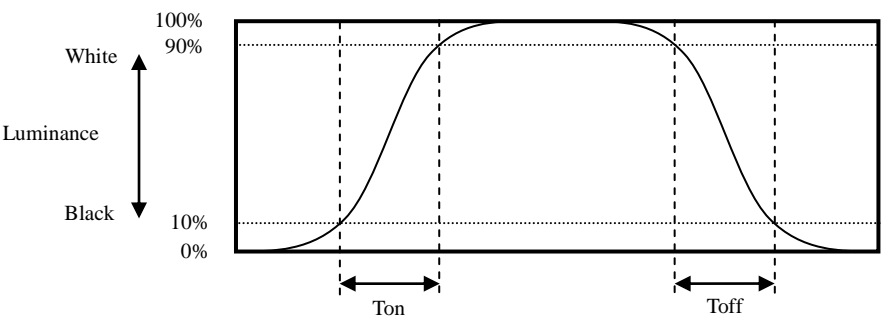
Luminance uniformity (LU) = $\frac{\text{Minimum luminance from ① to ⑨}}{\text{Maximum luminance from ① to ⑨}}$

The luminance is measured at near the 9 points shown below.

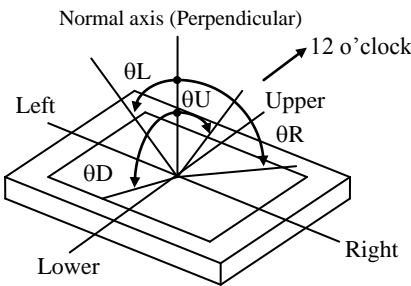


4.14.4 Definition of response times

Response time is measured at the time when the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time when the luminance changes from 10% up to 90%. Also Toff is the time when the luminance changes from 90% down to 10% (See the following diagram.).



4.14.5 Definition of viewing angles



5. ESTIMATED LUMINANCE LIFETIME

The luminance lifetime is the time from initial luminance to half-luminance.

This lifetime is the estimated value, and is not guarantee value.

Condition		Estimated luminance lifetime (Life time expectancy) Note1, Note2, Note3	Unit
LED elementary substance	25°C (Ambient temperature of the product) Continuous operation, PWM duty ratio: 100%	70,000	h
	60°C (Surface temperature at screen) Continuous operation, PWM duty ratio: 100%	60,000	

Note1: Life time expectancy is mean time to half-luminance.

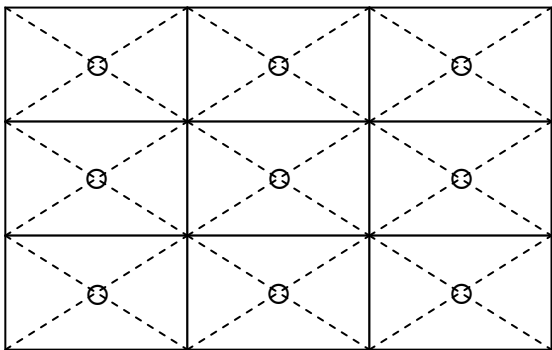
Note2: Estimated luminance lifetime is not the value for LCD module but the value for LED elementary substance.

Note3: By ambient temperature, the lifetime changes particularly. Especially, in case the product works under high temperature environment, the lifetime becomes short.

6. RELIABILITY TESTS

Test item		Condition	Judgment	Note1
High temperature and humidity (Operation)		① 60 ± 2°C, RH= 60%, 240hours ② Display data is white. Note2	No display malfunctions	
Heat cycle (Operation)		① 0 ± 3°C...1hour 60 ± 3°C...1hour ② 50cycles, 4hours/cycle ③ Display data is white. Note2		
Thermal shock (Non operation)		① -20 ± 3°C...30minutes 60 ± 3°C...30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.		
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s ² ② 1 minute/cycle ③ X, Y, Z directions ④ 10 times each directions	No display malfunctions No physical damages	☆
Mechanical shock (Non operation)		① 294m/s ² , 11ms ② ±X, ±Y, ±Z directions ③ 3 times each directions		
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface ③ 10 times each places at 1 sec interval Note3	No display malfunctions	
Low pressure	Non-operation	① 15kPa (Equivalent to altitude 13,600m) ② -20°C±3°C...24 hours ③ +60°C±3°C...24 hours	No display malfunctions	☆
	Operation	① 53.3kPa (Equivalent to altitude 5,100m) ② 0°C±3°C...24 hours ③ +55°C±3°C ...24 hours Note2		

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.
Note2: Luminance: 450cd/m² at luminance control.
Note3: See the following figure for discharge points



7. PRECAUTIONS

7.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "7.2 CAUTIONS" and "7.3 ATTENTIONS"!**



This sign has the meaning that a customer will be injured or the product will sustain damage if the customer practices wrong operations.



This sign has the meaning that a customer will be injured if the customer practices wrong operations.

7.2 CAUTIONS



*** Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: Equal to or no greater than 294m/s^2 and equal to or no greater than 11ms, Pressure: Equal to or no greater than 19.6N ($\phi 16\text{mm}$ jig))**

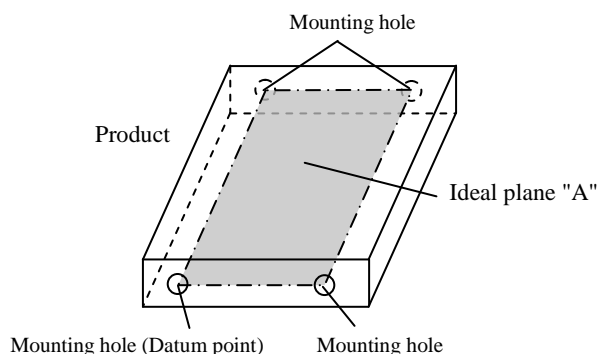
7.3 ATTENTIONS



7.3.1 Handling of the product

- ① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
- ② Do not hook or pull cables such as lamp cable, and so on, in order to avoid any damage.
- ③ When the product is put on the table temporarily, display surface must be placed downward.
- ④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
- ⑤ The torque for product mounting screws must never exceed $0.735\text{N}\cdot\text{m}$. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be $\leq 5.0\text{mm}$.

- ⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.
- Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within ± 0.3 mm.



- ⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, wipe it with a soft dry cloth.
- ⑧ Do not push or pull the interface connectors while the product is working.
- ⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
- ⑩ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal by any chance, please wash it away with soap and water.

7.3.2 Environment

- ① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
- ② In order to prevent dew condensation occurred by temperature difference, the product packing box must be opened after enough time being left under the environment of an unpacking room. Evaluate the storage time sufficiently because dew condensation is affected by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with the original packing state after a customer receives the package)
- ③ Do not operate in high magnetic field. If not, circuit boards may be broken.
- ④ This product is not designed as radiation hardened.

7.3.3 Characteristics

The following items are neither defects nor failures.

- ① Response time, luminance and color may be changed by ambient temperature.
- ② Display mura, flickering, vertical streams or tiny spots may be observed depending on display patterns.
- ③ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
- ④ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
- ⑤ Optical characteristics may be changed depending on input signal timings.

7.3.4 Others

- ① All GND, GNDB, VDD and VDDDB terminals should be used without any non-connected lines.
- ② Do not disassemble a product or adjust variable resistors.
- ③ Pack the product with the original shipping package, in order to avoid any damages during transportation, when returning the product to NLT for repairing and so on.
- ④ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.
- ⑤ The information of China RoHS directive six hazardous substances or elements in this product is as follows.

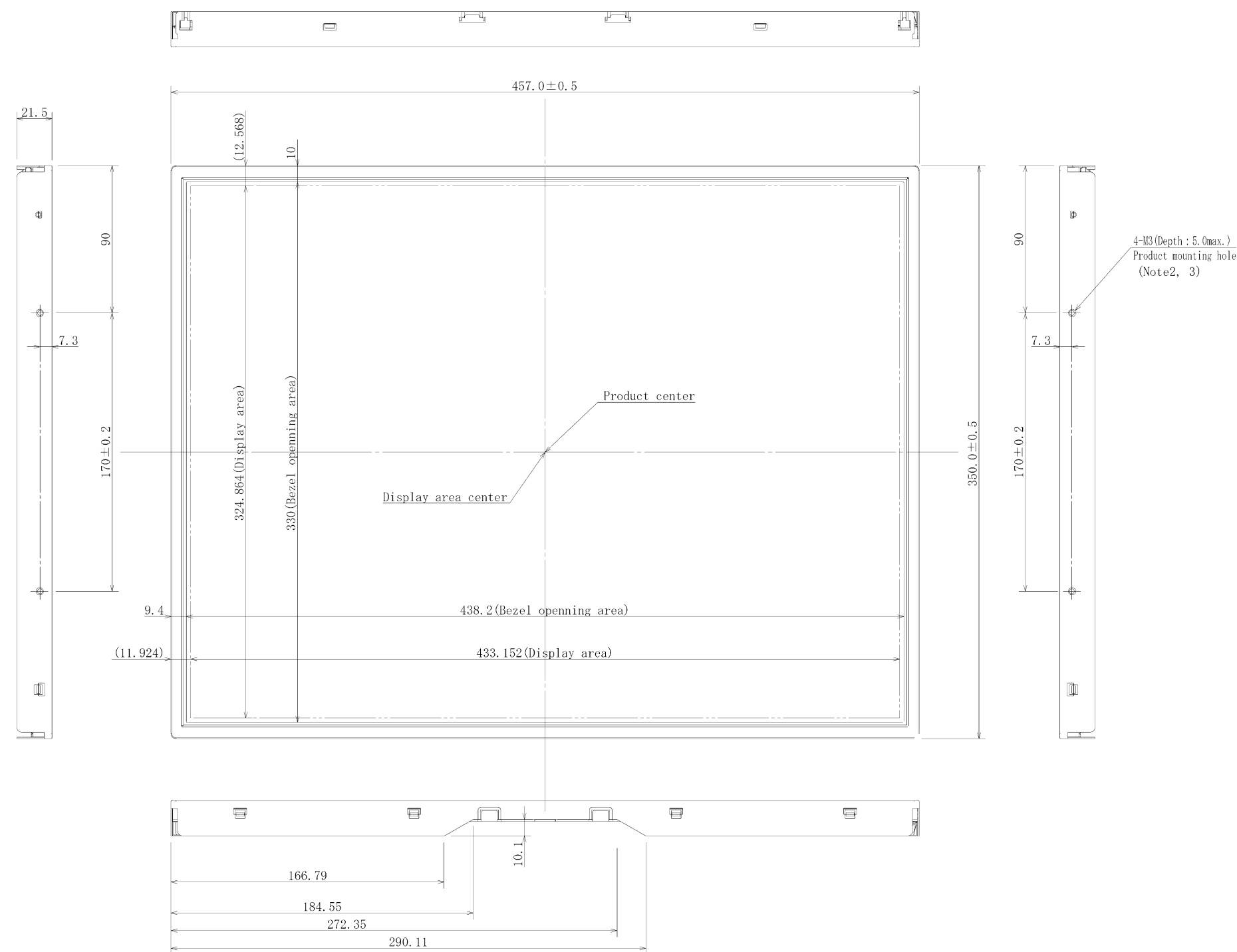
China RoHS directive six l hazardous substances or elements					
Lead (Pb)	Merc ury (Hg)	Cadmium (Cd)	Hexavalen t Chromium (Cr VI)	Polybrominated Biphenys (PBB)	Polybrominated Biphenyl Ethers (PBDE)
×	○	○	○	○	○

Note1: ○: This indicates that the poisonous or harmful material in all the homogeneous materials for this part is equal or below the limitation level of SJ/T11363-2006 standard regulation.

×: This indicates that the poisonous or harmful material in all the homogeneous materials for this part is above the limitation level of SJ/T11363-2006 standard regulation.

8. OUTLINE DRAWINGS

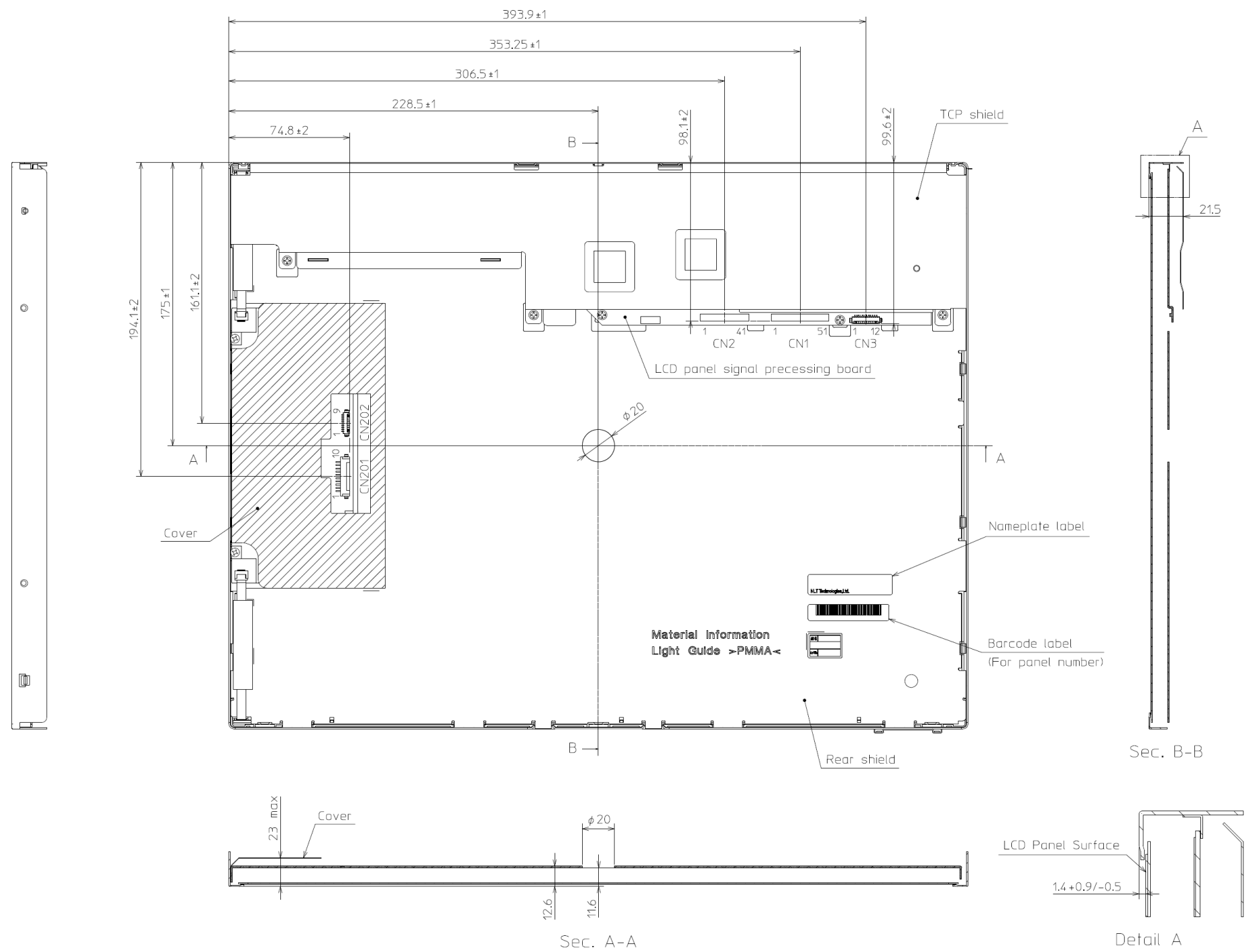
8.1 FRONT VIEW



- Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The length of product mounting screws from surface of plate must be ≤ 5.0mm.
Note4: The values in parentheses are for reference.

Unit: mm

8.2 REAR VIEW



- Note1: Not shown tolerances of the dimensions are ± 0.5 mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The length of product mounting screws from surface of plate must be ≤ 5.0 mm.
Note4: The values in parentheses are for reference.

Unit: mm