SPECIFICATION
FOR
APPROVAL

( ) **Preliminary Specification**
(●) **Final Specification**

Title	17.1” WXGA+ TFT LCD

BUYER	Dell
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LP171WPA
Suffix	TLA1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

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Product Engineering Dept.
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RECORD OF REVISIONS

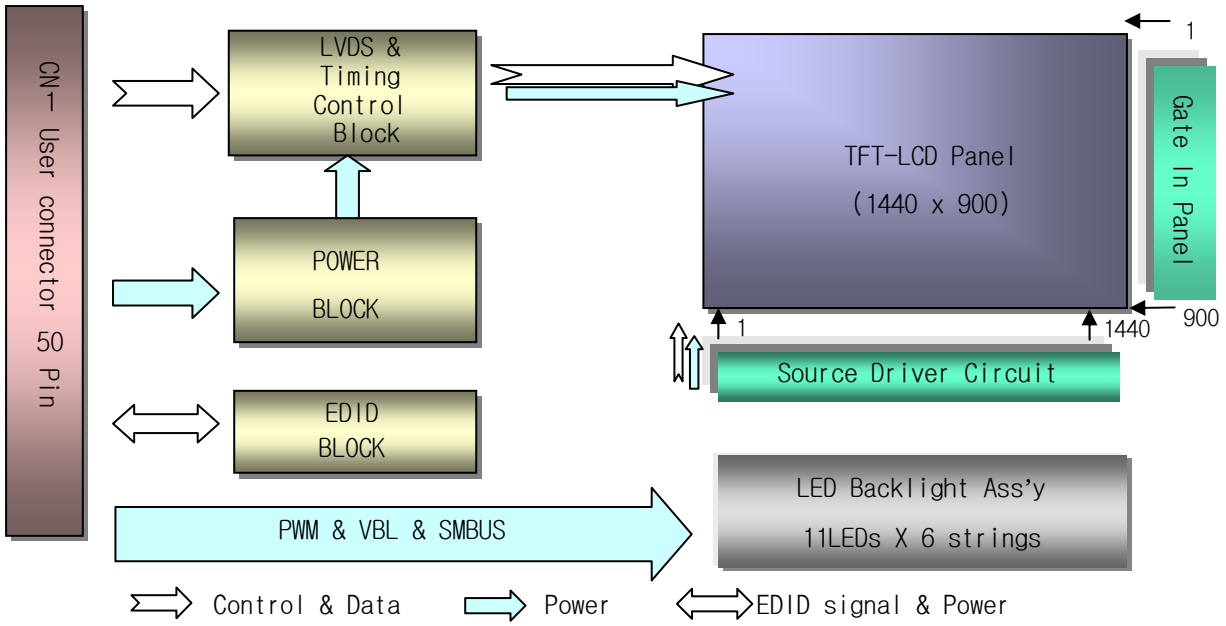
Revision No	Revision Date	Page	Description	EDID ver
0.0	Jun.12.2008	-	First Draft (Preliminary Specification)	0.1
0.1	Jun.30.2008	18	Change Mechanical Characteristics - Connector location update @ rear view	0.1
0.2	Jul.02.2008	28-30	Update EDID Data for Post-RTS samples	0.2

1. General Description

The LP171WPA is a Color Active Matrix Liquid Crystal Display with an integral LED backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally white mode. This TFT-LCD has 17.1 inches diagonally measured active display area with WXGA+ resolution(1440 horizontal by 900 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors.

The LP171WPA has been designed to apply the interface method that enables low power, high speed, low EMI.

The LP171WPA is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP171WPA characteristics provide an excellent flat display for office automation products such as Notebook PC.



General Features

Active Screen Size	17.1 inches diagonal
Outline Dimension	382.20 (H) × 247.0 (V) × 7.0(D, max.) mm
Pixel Pitch	0.255 mm × 0.255 mm
Pixel Format	1440 horiz. by 900 vert. Pixels RGB strip arrangement
Color Depth	6-bit, 262,144 colors
Luminance, White	270 cd/m^2(Min., @I_{LED}=19mA) , 5 points Min
Power Consumption	Total 5.41Watt @LCM circuit 1.40W(Typ.), LED 4.01 W (Typ.)
Weight	610g(Max.)
Display Operating Mode	Transmissive mode, normally white
Surface Treatment	Hard coating(3H), Glare treatment of the front polarizer
RoHS Comply	Yes

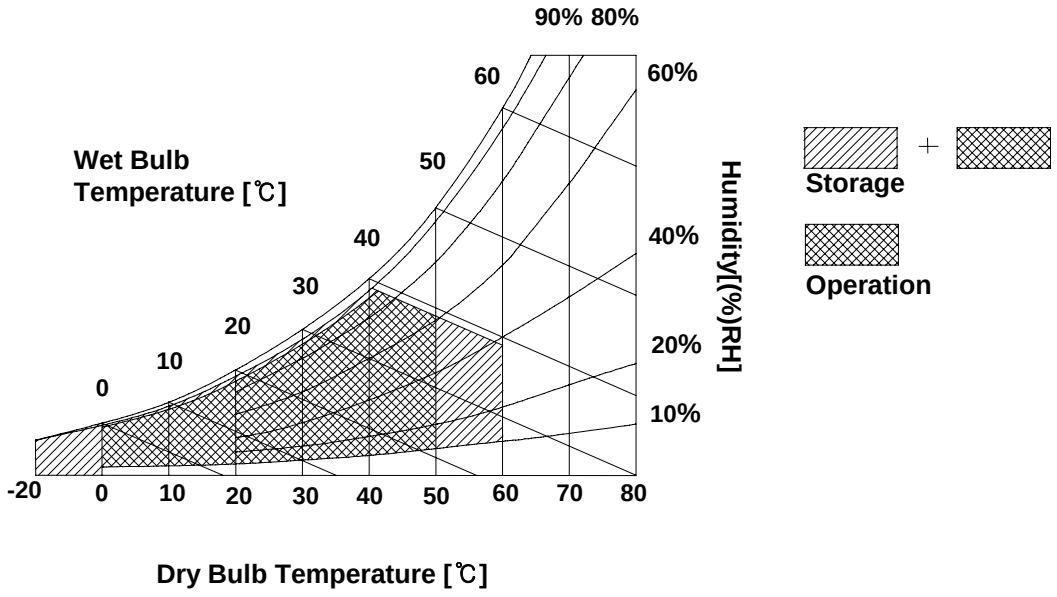
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	Vdc	at 25 ± 5°C
Operating Temperature	TOP	0	50	°C	1
Storage Temperature	HST	-20	60	°C	1
Operating Ambient Humidity	HOP	10	90	%RH	1
Storage Humidity	HST	10	90	%RH	1

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.



3. Electrical Specifications

3-1. Electrical Characteristics

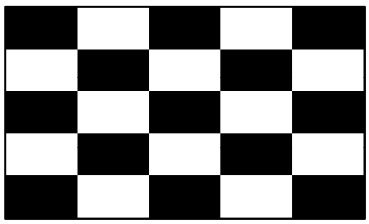
The LP171WPA requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input which powers the LED BL.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
MODULE :						
Power Supply Input Voltage	VCC	3.0	3.3	3.6	V_{DC}	
Power Supply Input Current (Window desktop pattern)	I_{CC}	360	425	490	mA	1
Power Consumption (Window desktop pattern)	Pc	-	1.40	1.6	Watt	1
Differential Impedance	Zm	90	100	110	Ohm	2
LED Backlight :						
Operating Voltage	V_{LED}	-	35.2	36.3	V	3
Operating Current per string	I_{LED}	-	19	-	mA	4
Power Consumption (dimming 100%)	P_{BL}	-	4.01	4.14	Watt	-
LED Driver power consumption	P_{Driver}	-	1.15	-	Watt	-
Life Time		10,000	-	-	Hrs	5
BL Input Voltage	BL_VCC	7.5	12	21	V	
PWM input signal :			5.0		V	
Input Frequency (for operating)	-	100	-	500	Hz	6
Input Frequency (for reliability)	-	217	222	227	Hz	
on threshold	-	2.1	-	-	V	
off threshold	-	-	-	0.8	V	
Duty Cycle	-	12.5	-	100	%	7, 8

Note)

1. The specified current and power consumption are under the Vcc = 3.3V , 25℃, fv = 60Hz condition whereas Window desktop pattern is displayed and fv is the frame frequency.

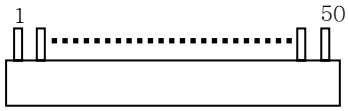


2. This impedance value is needed to proper display and measured form LVDS Tx to the mating connector.
3. The variance of the voltage is ± 10%.
4. The typical operating current is for the typical surface luminance (L_{WH}) in optical characteristics. I_{LED} is the current of each LEDs' string, LED backlight has 6 strings on it.
5. The life time is determined as the time at which brightness of LED is 50% compare to that of initial value at the typical LED current.
6. LED Driver operating Frequency
7. There may be a flickering Under 6% dimming.
8. There is no reliability issue.(under 12.5% duty cycle)

3-2. Interface Connections

This LCD employs two interface connections, a 50 pin connector is used for the module electronics interface and the other connector is used for the internal backlight system.
The electronics interface connector is a model FI-VHP50S manufactured by JAE.

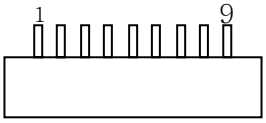
Table 3. MODULE CONNECTOR PIN CONFIGURATION (CN1)

Pin	Symbol	Description	Notes
1	VSS	Ground (Buyer's Test loop to pin 30)	1, Interface chips 1.1 LCD : SW, ST2_BS (LCD Controller) including LVDS Receiver 1.2 System : * Pin to Pin compatible with LVDS 2.Connector 2.1 LCD :JAE FI-VHP50 or equivalent (1.0 mm thickness, lock-in type, pin 1 starts from left on the front) 2.2 Mating:JAE FI-VHP50 series or equivalent (micro-coax type) 2.3 Connector pin arrangement LCD rear view  [LCD Module Rear View]
2	VEEDID	EDID 3.3V power	
3	VSS	Ground	
4	CLK EEDID	EDID clock	
5	DATA EEDID	EDID data	
6	VSS	Ground	
7	Odd_Rin0-	Negative LVDS differential data input	
8	Odd_Rin0+	Positive LVDS differential data input	
9	VSS	Ground	
10	Odd_Rin1-	Negative LVDS differential data input	
11	Odd_Rin1+	Positive LVDS differential data input	
12	VSS	Ground	
13	Odd_Rin2-	Negative LVDS differential data input	
14	Odd_Rin2+	Positive LVDS differential data input	
15	VSS	Ground	
16	Odd_ClkIN-	Negative LVDS differential clock input	
17	Odd_ClkIN+	Positive LVDS differential clock input	
18	VSS	Ground	
19	Even_Rin0-	Negative LVDS differential data input	
20	Even_Rin0+	Positive LVDS differential data input	
21	VSS	Ground	
22	Even_Rin1-	Negative LVDS differential data input	
23	Even_Rin1+	Positive LVDS differential data input	
24	VSS	Ground	
25	Even_Rin2-	Negative LVDS differential data input	
26	Even_Rin2+	Positive LVDS differential data input	
27	VSS	Ground	
28	Even_ClkIN-	Negative LVDS differential clock input	
29	Even_ClkIN+	Positive LVDS differential clock input	
30	VSS	Ground (Buyer's Test loop to pin 1)	

31	VSS	Ground (Buyer's Test loop to 50pin)	
32	VDD	Logic power 3.3V	
33	VDD	Logic power 3.3V	
34	BIST_EN	Panel Self Test	
35	+5V_ALW	No connection	
36	VSS	Ground	
37	VSS	Ground	
38	PWM_BL	PWM brightness control	
39	VSS	Ground (VBL-)	
40	VSS	Ground (VBL-)	
41	VSS	Ground (VBL-)	
42	VSS	Ground (VBL-)	
43	NC	No connect	
44	VBL+	7.5V ~ 21V LED power	
45	VBL+	7.5V ~ 21V LED power	
46	VBL+	7.5V ~ 21V LED power	
47	VBL+	7.5V ~ 21V LED power	
48	SMB_DATA	SMBus Data	
49	SMB_CLK	SMBus Clk	
50	VSS	Ground (Buyer's Test loop to 31pin)	

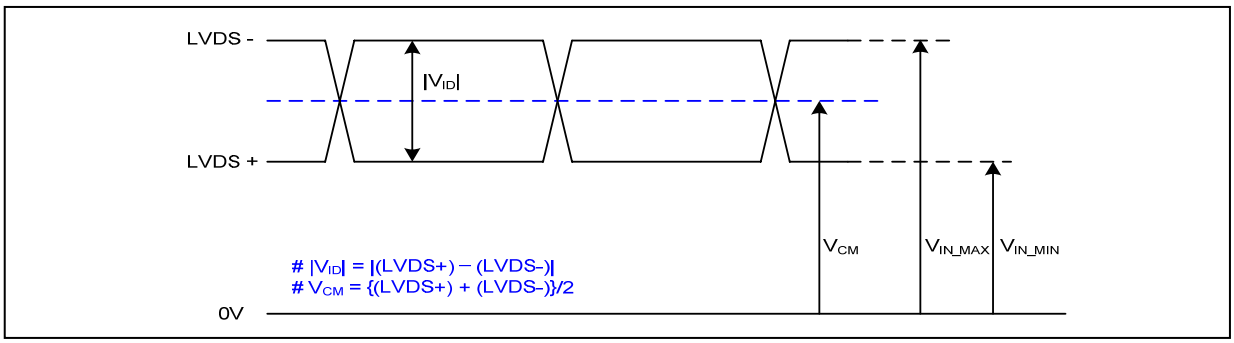
The LED backlight connector is a model TF12-9S-0.5H, manufactured by Hirose.

Table 4. BACKLIGHT CONNECTOR PIN CONFIGURATION (CN2)

Pin	Symbol	Description	Notes
1	Vdc(1,2,3,4,5,6)	LED Anode(Positive)	
2	Vdc(1,2,3,4,5,6)	LED Anode(Positive)	
3	NC	No Connection	
4	Vdc1	LED Cathode (Negative)	
5	Vdc2	LED Cathode (Negative)	
6	Vdc3	LED Cathode (Negative)	
7	Vdc4	LED Cathode (Negative)	
8	Vdc5	LED Cathode (Negative)	
9	Vdc6	LED Cathode (Negative)	

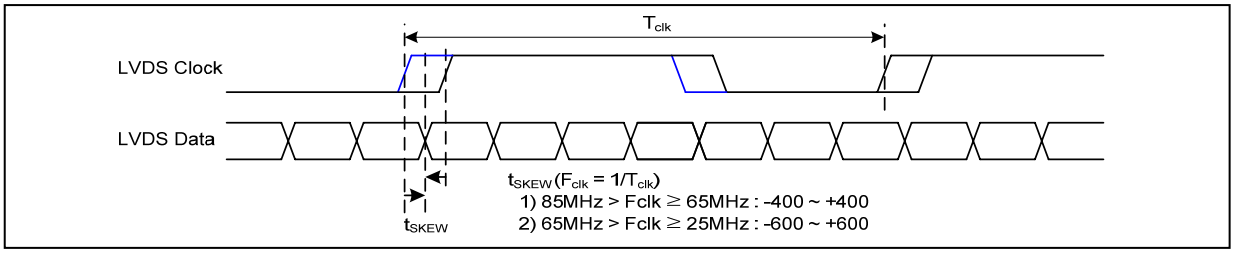
3-3. LVDS Signal Timing Specifications

3-3-1. DC Specification

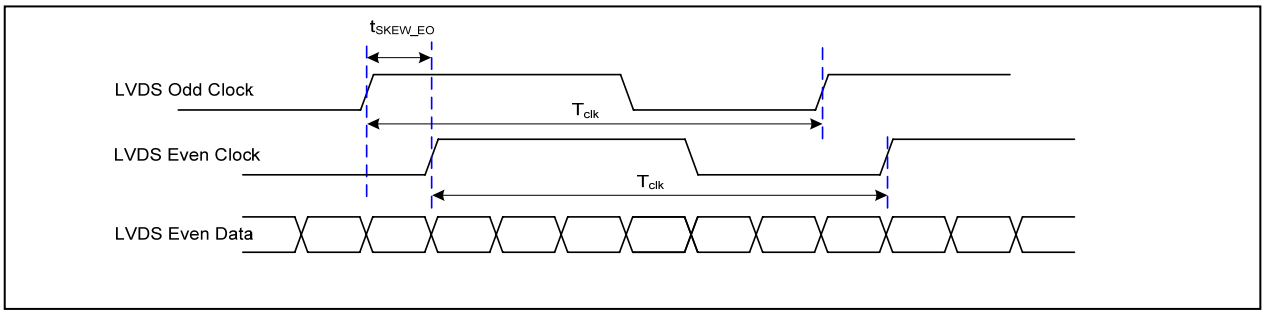


Description	Symbol	Min	Max	Unit	Notes
LVDS Differential Voltage	$\|V_{ID}\|$	200	600	mV	-
LVDS Common mode Voltage	V_{CM}	0.6	1.8	V	-
LVDS Input Voltage Range	V_{IN}	0.3	2.1	V	-

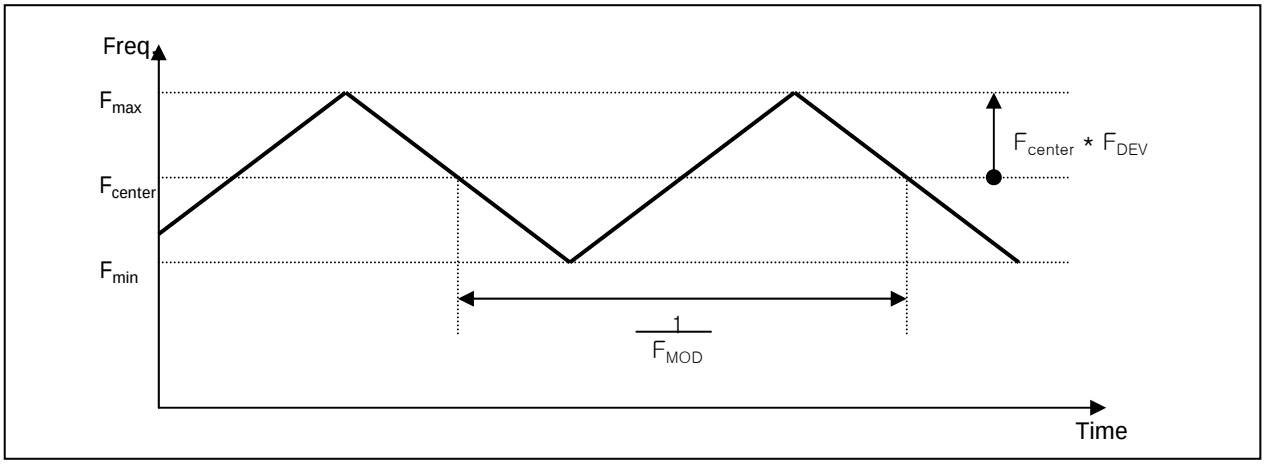
3-3-2. AC Specification



Description	Symbol	Min	Max	Unit	Notes
LVDS Clock to Data Skew Margin	t_{SKEW}	- 400	+ 400	ps	85MHz > Fclk ≥ 65MHz
	t_{SKEW}	- 600	+ 600	ps	65MHz > Fclk ≥ 25MHz
LVDS Clock to Clock Skew Margin (Even to Odd)	t_{SKEW_EO}	- 1/7	+ 1/7	T_{clk}	-
Maximum deviation of input clock frequency during SSC	F_{DEV}	-	± 3	%	-
Maximum modulation frequency of input clock during SSC	F_{MOD}	-	200	KHz	-



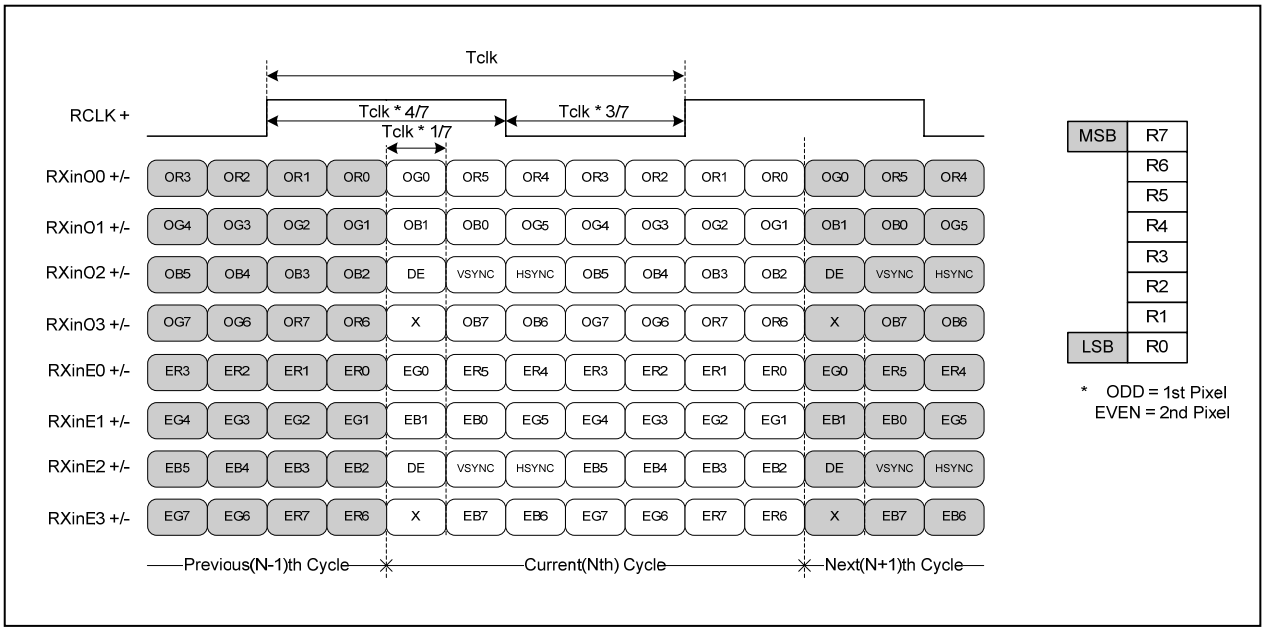
< Clock skew margin between channel >



< Spread Spectrum >

3-3-3. Data Format

- LVDS 2 Port



< LVDS Data Format >

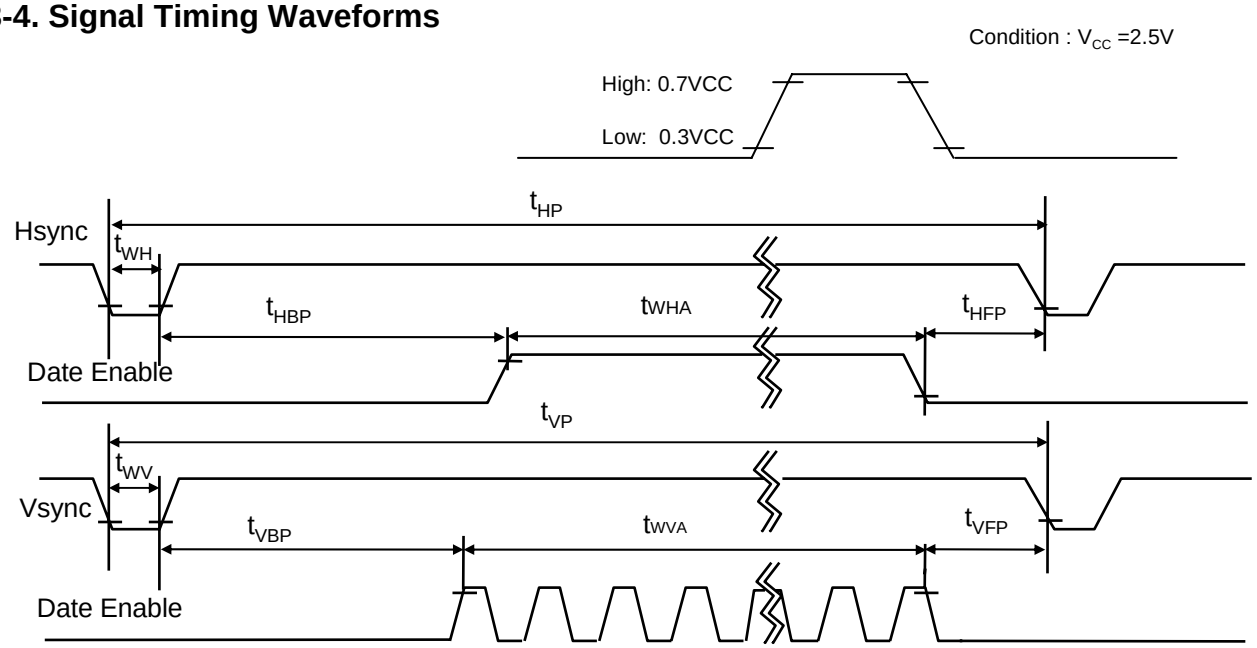
3-3-4. Signal Timing Specifications

This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of LVDS Tx/Rx for its proper operation.

Table 5. TIMING TABLE

ITEM	Symbol		Min	Typ	Max	Unit	Note
DCLK	Frequency	f_{CLK}	-	54.75	-	MHz	2port
Hsync	Period	tw_{HA}	952	1000	1048	tCLK	2port
	Width	t_{HP}	32	40	48		
	Active	t_{WH}	720	720	720		
Vsync	Period	tw_{VA}	907	912	926	tHP	
	Width	t_{VP}	2	3	5		
	Active	t_{WV}	900	900	900		
Data Enable	Horizontal back porch	t_{HBP}	176	200	224	tCLK	2port
	Horizontal front porch	t_{HFP}	24	40	56		
	Vertical back porch	t_{VBP}	4	7	15	tHP	
	Vertical front porch	t_{VFP}	1	2	6		

3-4. Signal Timing Waveforms



3-5. Color Input Data Reference

The brightness of each primary color (red,green and blue) is based on the 6-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 6. COLOR DATA REFERENCE

Color		Input Color Data																	
		RED						GREEN						BLUE					
		MSB					LSB	MSB					LSB	MSB					LSB
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	…			…						…						…			
	RED (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	...			...						...						...			
	GREEN (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	BLUE (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	…			…						…						…			
	BLUE (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

3-6. Power Sequence

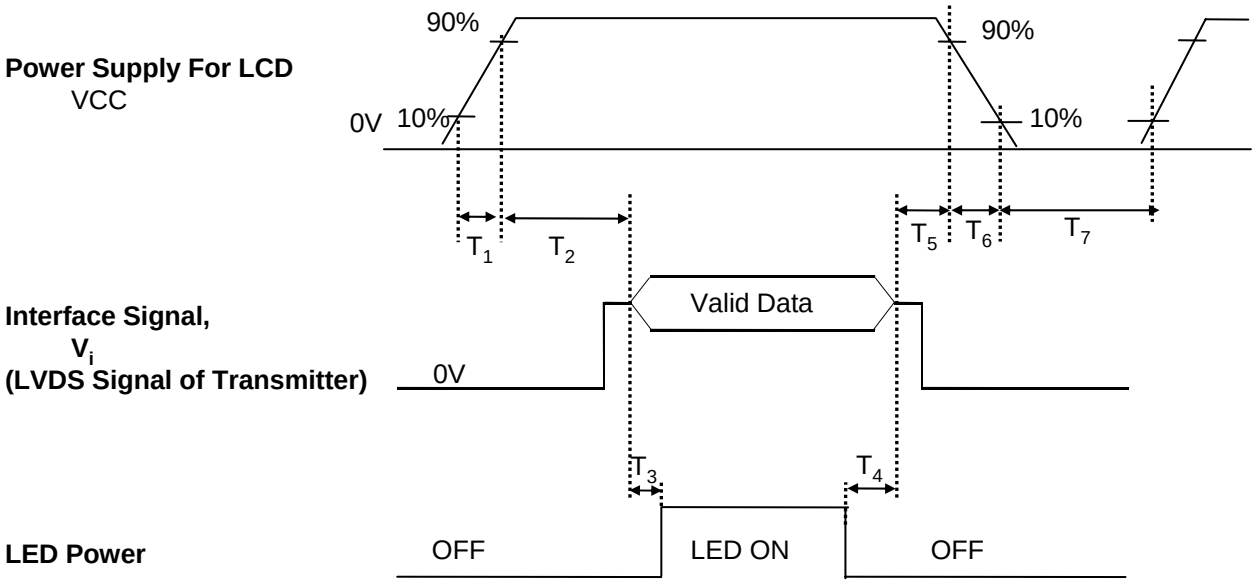


Table 7. POWER SEQUENCE TABLE

Parameter	Value			Units
	Min.	Typ.	Max.	
T_1	0	-	10	(ms)
T_2	0	-	50	(ms)
T_3	200	-	-	(ms)
T_4	200	-	-	(ms)
T_5	0	-	50	(ms)
T_6	0	-	10	(ms)
T_7	400	-	-	(ms)

Note)
1. Valid Data is Data to meet “3-3. LVDS Signal Timing Specifications”
2. Please avoid floating state of interface signal at invalid period.
3. When the interface signal is invalid, be sure to pull down the power supply for LCD VCC to 0V.
4. Lamp power must be turn on after power supply for LCD and interface signal are valid.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 20 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0°.
FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

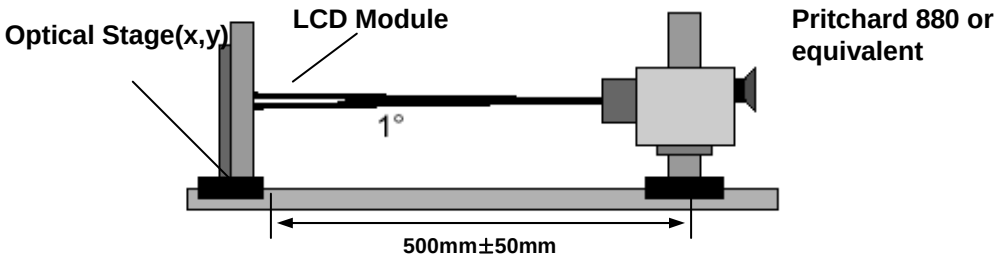


Table 8. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz, f_{CLK}= 102MHz, I_{LED} = 19mA

Parameter	Symbol	Values			Units	Notes
		Min	Typ	Max		
Contrast Ratio	CR	400	600	-		1
Surface Luminance, white	L_{WH}	270	-	-	cd/m^2	2
Luminance Variation(13points)	δ_{WHITE}		1.4	1.6		3
Response Time	Tr_R+ Tr_D		16	25	ms	4
Color Coordinates						
RED	RX	0.561	0.591	0.621		
	RY	0.318	0.348	0.378		
GREEN	GX	0.309	0.339	0.369		
	GY	0.520	0.550	0.580		
BLUE	BX	0.126	0.156	0.186		
	BY	0.096	0.126	0.156		
WHITE	WX	0.283	0.313	0.343		+/- 0.030
	WY	0.299	0.329	0.359		+/- 0.030
Viewing Angle						5
x axis, right(Φ=0°)	Θr	55	60	-	degree	
x axis, left (Φ=180°)	Θl	55	60	-	degree	
y axis, up (Φ=90°)	Θu	45	50	-	degree	
y axis, down (Φ=270°)	Θd	45	50	-	degree	
Gray Scale				-		6

Notes)

1. Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the 5point (1~5)average across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 2.
When I_{LED}= 19mA, L_{WH}=300cd/m^2(Typ.)

3. Luminance variation is measured for 13 point For more information see FIG 2.
δ WHITE = Maximum(LN1,LN2, ….. LN13) ÷ Minimum(LN1,LN2, ….. LN13)

4. Response time is the time required for the display to transition from white to black (rise time, Tr_R) and from black to white(Decay Time, Tr_D). For additional information see FIG 3.

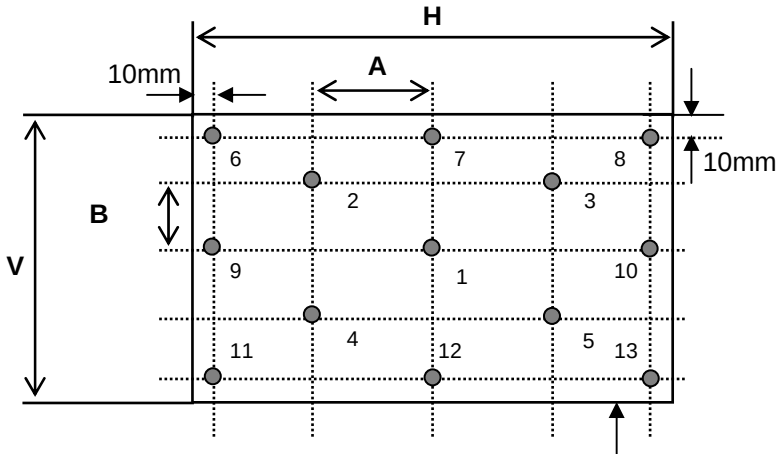
5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

6. Gray scale specification * f_V=60Hz

Gray Level	Luminance [%] (Typ)
L0	0.10
L7	1.58
L15	6.10
L23	12.8
L31	21.6
L39	35.4
L47	54.0
L55	76.0
L63	100

FIG. 2 Luminance

<Measuring point for Average Luminance & measuring point for Luminance variation>



H,V : ACTIVE AREA
A : H/4 mm
B : V/4 mm
POINTS: 13 POINTS

FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.

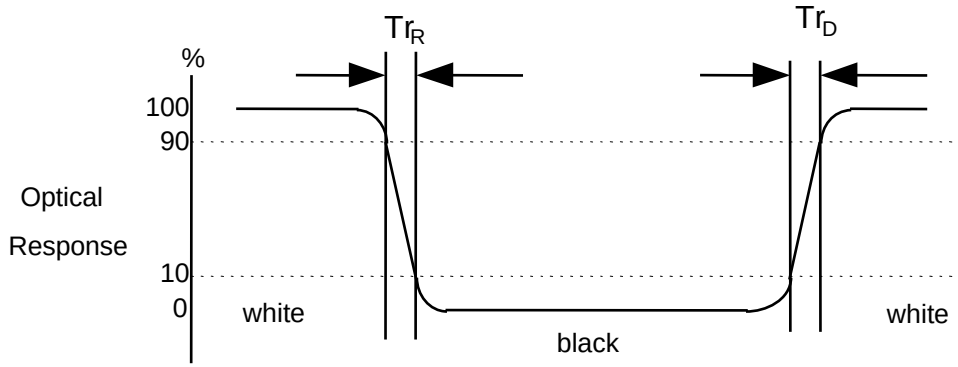
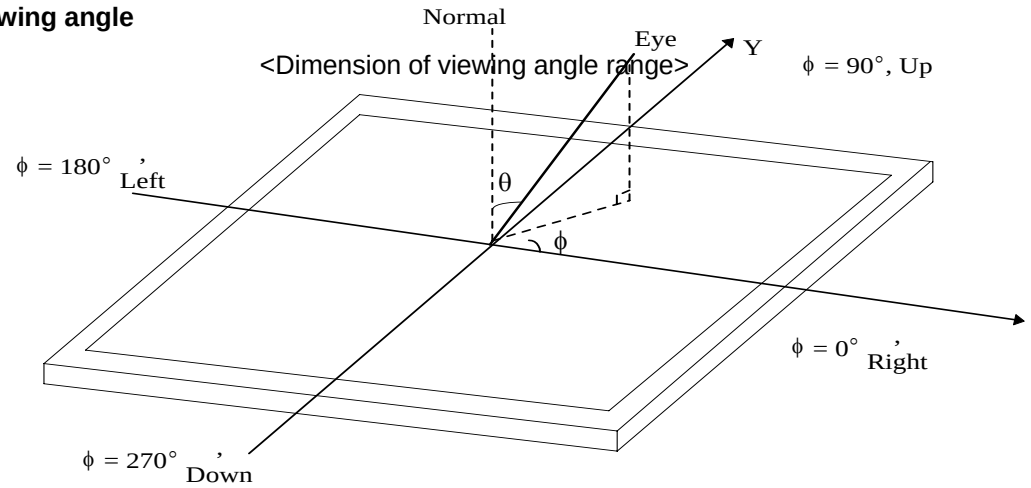


FIG. 4 Viewing angle

<Dimension of viewing angle range>



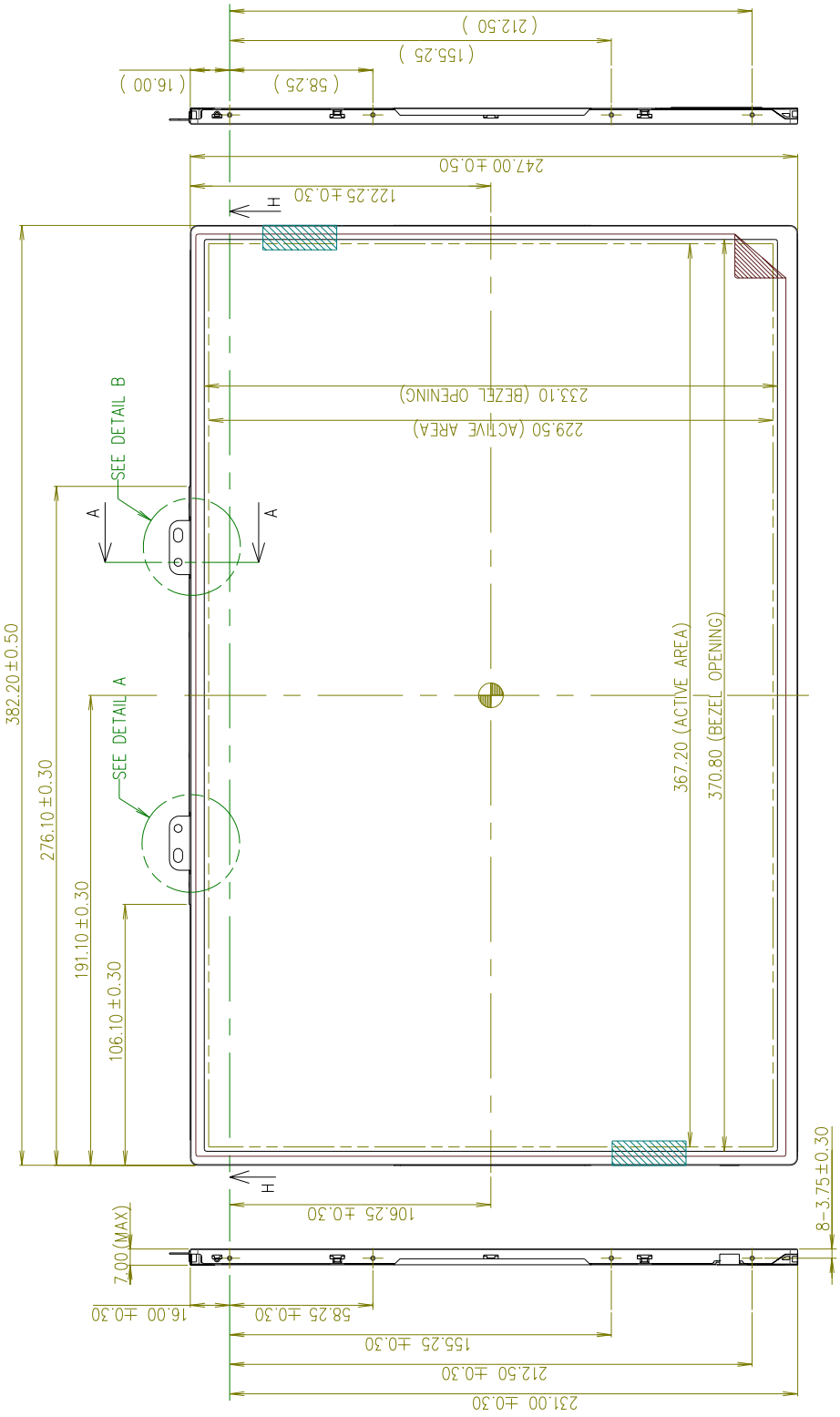
5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LP171WPA.
In addition the figures in the next page are detailed mechanical drawing of the LCD.

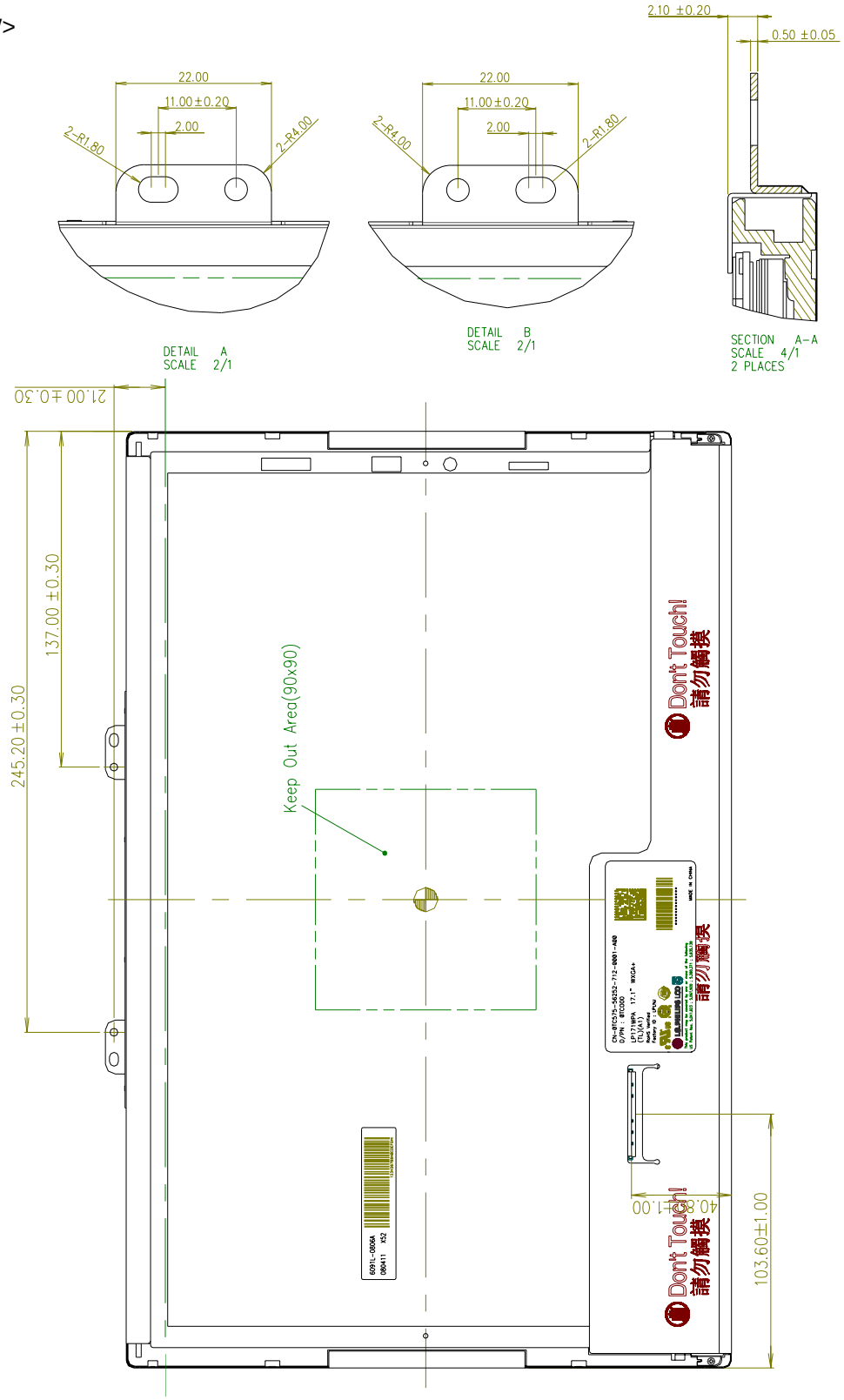
Outline Dimension	Horizontal	382.2 ± 0.50 mm
	Vertical	247.0 ± 0.50 mm
	Depth	7.0 mm (Max.)
Bezel Area	Horizontal	370.8 ± 0.50 mm
	Vertical	233.1 ± 0.50 mm
Active Display Area	Horizontal	367.2 mm
	Vertical	229.5 mm
Weight	610g (Max.)	
Surface Treatment	Hard coating(3H), Glare treatment of the front polarizer	

<FRONT VIEW>

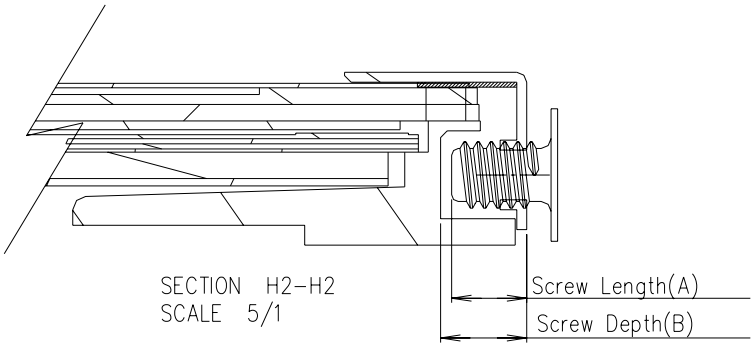
Note) Unit:[mm], General tolerance: ± 0.5mm



<REAR VIEW>


22.00
11.00±0.20
2.00
2-R1.80
2-R4.00
DETAIL A
SCALE 2/1
22.00
11.00±0.20
2.00
2-R4.00
2-R1.80
DETAIL B
SCALE 2/1
2.10 ±0.20
0.50 ±0.05
SECTION A-A
SCALE 4/1
2 PLACES
21.00±0.30
137.00 ±0.30
245.20±0.30
Keep Out Area(90x90)
Don't Touch!
請勿觸摸
40.80±1.00
103.60±1.00

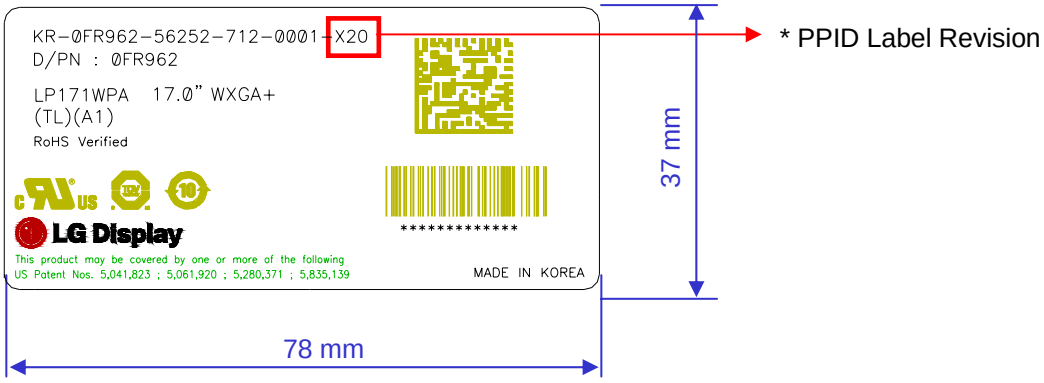
[DETAIL DESCRIPTION OF SIDE MOUNTING SCREW]



* Mounting Screw Length (A)
  = 2.0(Min) / 2.5(Max)
* Mounting Screw Hole Depth (B)
  = 2.5(Min)
* Torque : 2.5 kgf.cm(Max)
  (Measurement gauge : torque meter)

Notes : 1. Screw plated through the method of non-electrolytic nickel plating is preferred to reduce possibility that results in vertical and/or horizontal line defect due to the conductive particles from screw surface.

[DETAIL INFORMATION OF PPID LABEL AND REVISION CODE]

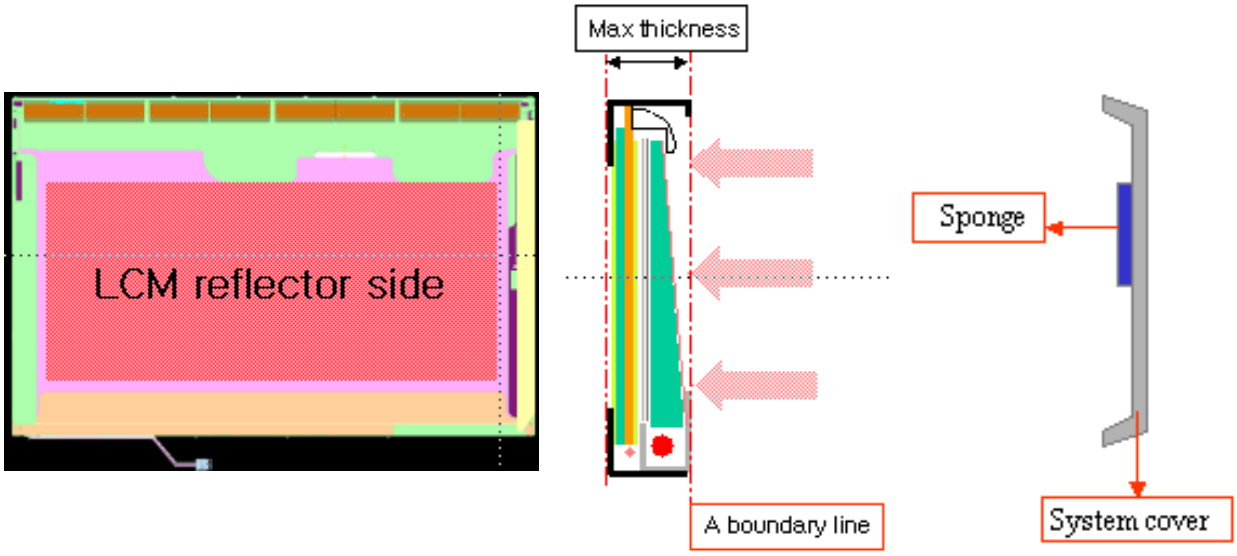


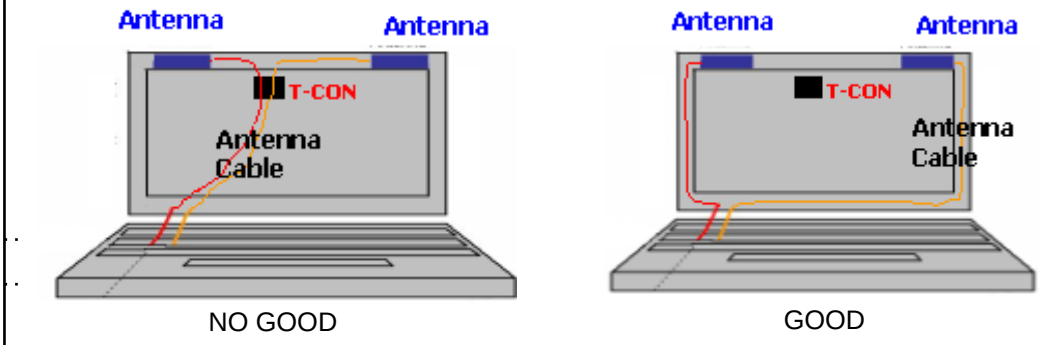
* PPID Label Revision :
It is subject to change with Dell event. Please refer to the below table for detail.

Classification	No Change	1st Revision	2nd Revision	…	9th Revision	…
SST(WS)	X00	X01	X02	…	A09	…
PT(ES)	X10	X11	X12	…	A19	…
ST(CS)	X20	X21	X22	…	A29	…
XB(MP)	A00	A01	A02	…	A09	…

LPL Proposal for system cover design.(Appendix)

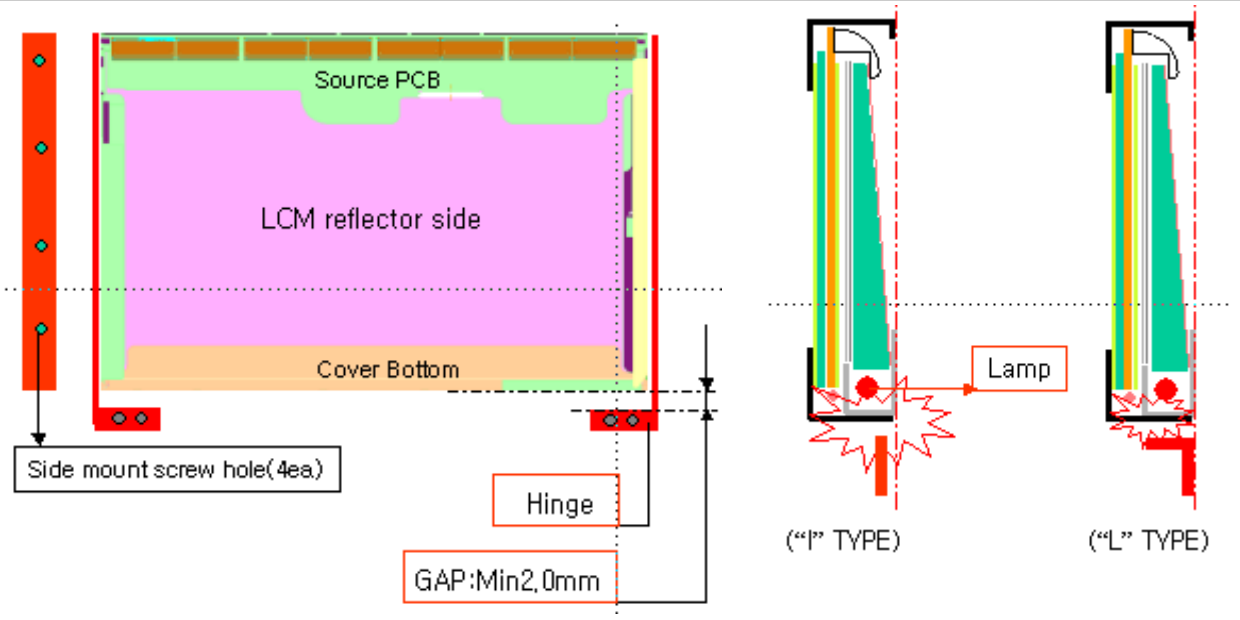
1	Gap check for securing the enough gap between LCM and System cover.	



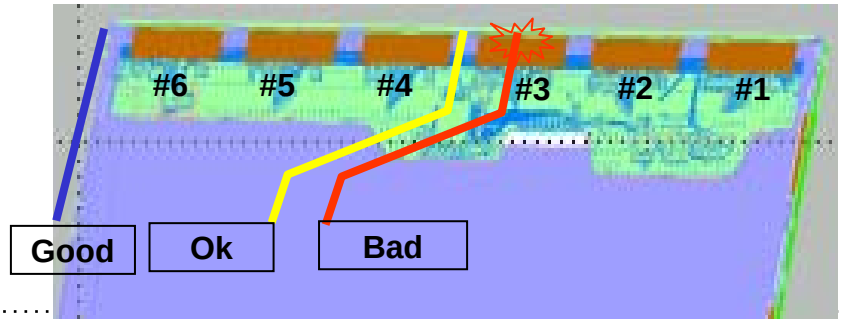
Define	1.Rear side of LCM is sensitive against external stress,and previous check about interference is highly needed. 2.In case there is something from system cover comes into the boundary above,mechanical interference may cause the FOS defects. (Eg:Ripple,White spot..)
2	Check if antenna cable is sufficiently apart from T-CON of LCD Module.
Define	
	1.If system antenna is overlapped with T-CON,it might be cause the noise.

LPL Proposal for system cover design.

3	Gap check for securing the enough gap between LCM and System hinge.	



Define	1.At least 2.0mm of gap needs to be secured to prevent the shock related defects. 2."L" type of hinge is recommended than "I" type under shock test.
4	Checking the path of the System wire.

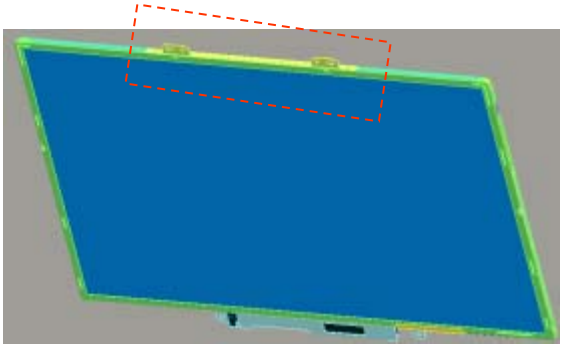


Define	1.COF area needs to be handled with care. 2.GOOD ➔Wire path design to system side. OK➔ Wire path is located between COFs. BAD➔Wire path overlapped with COF area.

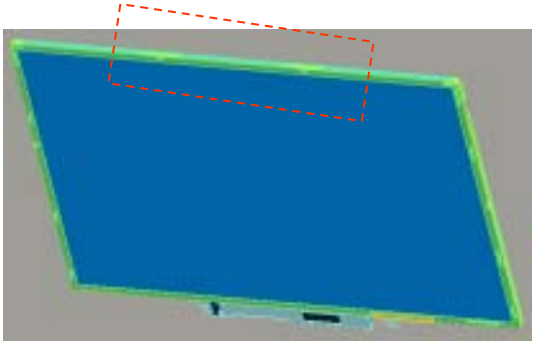
LPL Proposal for system cover design.

5	Using a bracket on the top of LCM is not recommended.	

bracket

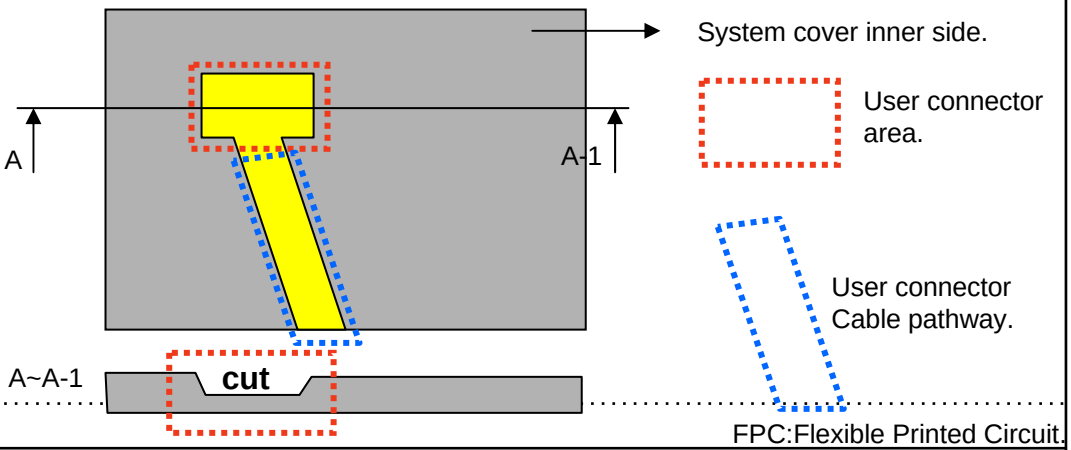


With bracket



Without bracket

Define	1.Condition without bracket is good for mechanical noise,and can minimize the light leakage from deformation of bracket. 2.The results shows that there is no difference between the condition with or without bracket.
6	Securing additional gap on CNT area..



Define	1.CNT area is specially sensitive against external stress,and additional gap by cutting on system cover will be helpful on removing the Ripple. 2.Using a thinner CNT will be better. (eg: FPC type)

6. Reliability

Environment test condition

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Vibration test (non-operating)	Sine wave, 5 ~ 150Hz, 1.5G, 0.37oct/min 3 axis, 30min/axis
6	Shock test (non-operating)	- No functional or cosmetic defects following a shock to all 6 sides delivering at least 180 G in a half sine pulse no longer than 2 ms to the display module - No functional defects following a shock delivering at least 200 g in a half sine pulse no longer than 2 ms to each of 6 sides. Each of the 6 sides will be shock tested with one each display, for a total of 6 displays
7	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr

{ Result Evaluation Criteria }
There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

7. International Standards

7-1. Safety

a) UL 60950-1:2003, First Edition, Underwriters Laboratories, Inc.,
Standard for Safety of Information Technology Equipment.
b) CAN/CSA C22.2, No. 60950-1-03 1st Ed. April 1, 2003, Canadian Standards Association,
Standard for Safety of Information Technology Equipment.
c) EN 60950-1:2001, First Edition,
European Committee for Electrotechnical Standardization(CENELEC)
European Standard for Safety of Information Technology Equipment.

7-2. EMC

a) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHZ to 40GHz. “American National Standards Institute(ANSI), 1992
b) CISPR22 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.“ International Special Committee on Radio Interference.
c) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.“ European Committee for Electrotechnical Standardization.(CENELEC), 1998
(Including A1: 2000)