INNOLUX 群創光電

PRODUCT SPECIFICATION

Doc. Number:

□ Tentative Specification
■ Preliminary Specification
□ Approval Specification

MODEL NO.: N080JCE
SUFFIX: G41

Customer:

APPROVED BY **SIGNATURE**

Name / Title

Note :
Only for reference

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
HENRY.CHIEN	LYNN.LIAO	CHINGKUO.CHIANG

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REVISION HISTORY

Version	Date	Page	Description
0.0	Jan, 14, 2014	All	Spec Ver.0.0 was first issued.
1.0	Jun, 30, 2014	All	Spec Ver.1.0 was first issued.
2.0	Jan,12,2015	P30	Add NT51021 Register setting appendix.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N080JCE-G41 is a 8” (8” diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 39 pins MIPI interface. This module supports 1200 x 1920 WUXGA mode.

1.2 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	8” diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1200 x R.G.B. x 1920	pixel	-
Pixel Pitch	0.0299 (H) x 0.0897 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216 (8bit color depth)	color	-
Transmissive Mode	Normally black	-	-
Surface Treatment	Hard coating (3H), Glare	-	-
Luminance, White(**center**)	400	Cd/m2	
Power Consumption	Total 1.82 W (Max.) (panel 0.4 W (Max.), BL 1.42W (Max.))		(1)

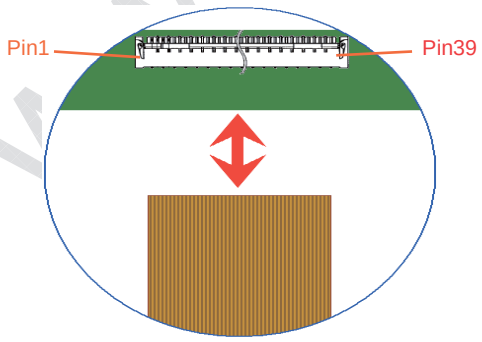
Note (1) The specified power consumption (with converter efficiency) is under the conditions at **VDD= 3.3V, fv = 60 Hz, Brightness(center)= 400nits, I_{F_LED} = 21mA** and Ta = 25 ± 2 ºC, whereas **white** pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	114.1	114.6	115.1	mm	Module Size
	Vertical (V)	183.6	184.1	184.6	mm	
	Thickness (T)			2.3 (w/o PCBA) 3.95(w/ PCBA)	mm	
CF Polarizer	Horizontal	110.24	110.44	110.64	mm	CF Polarizer
	Vertical	175.424	175.624	175.824	mm	
Active Area	Horizontal	107.59	107.64	107.69	mm	Active Area
	Vertical	172.174	172.224	172.274	mm	
Weight		-	-	80	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: **Hirose FH26-39S-0.3SHW**

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

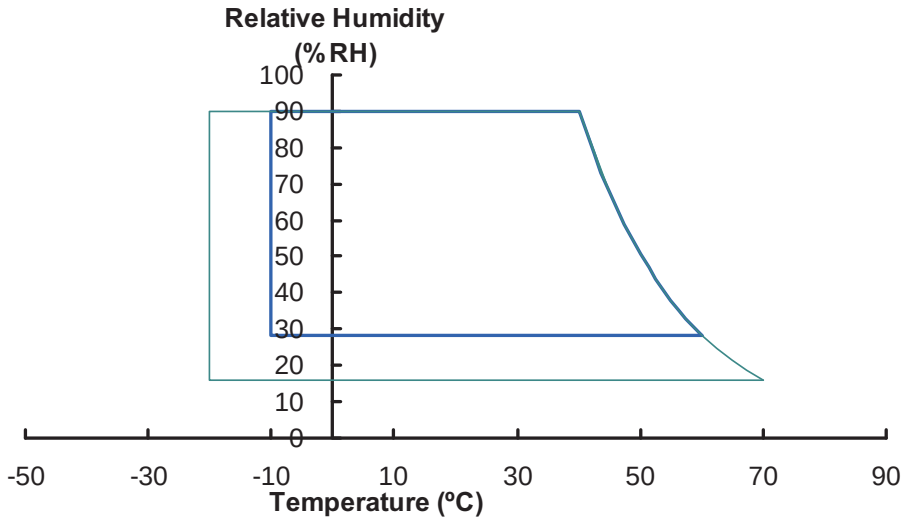
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+70	ºC	(1)
Operating Ambient Temperature	T_{OP}	-10	+60	ºC	(1), (2)

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be -10 ºC min. and 70 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

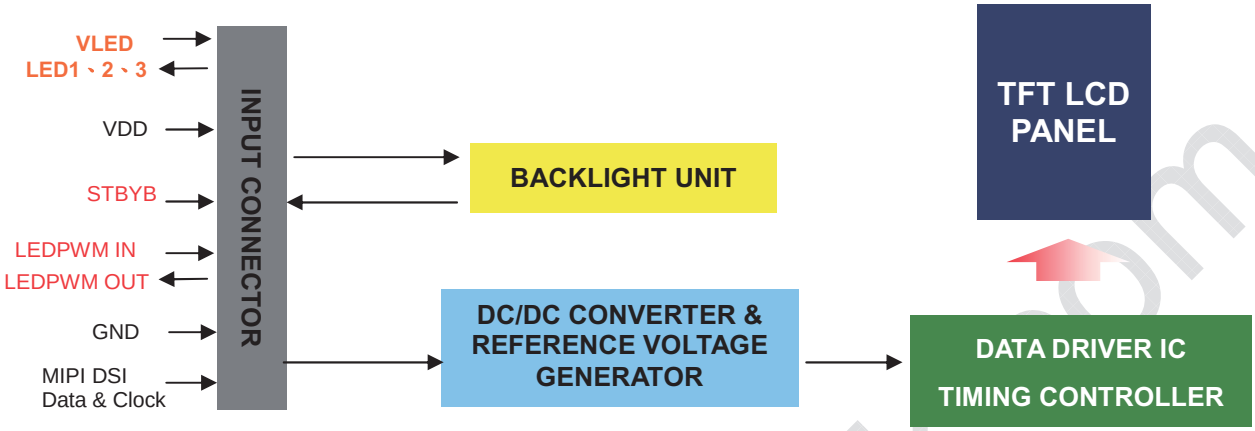
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	**VDD**	**+2.7**	**+3.6**	**V**	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

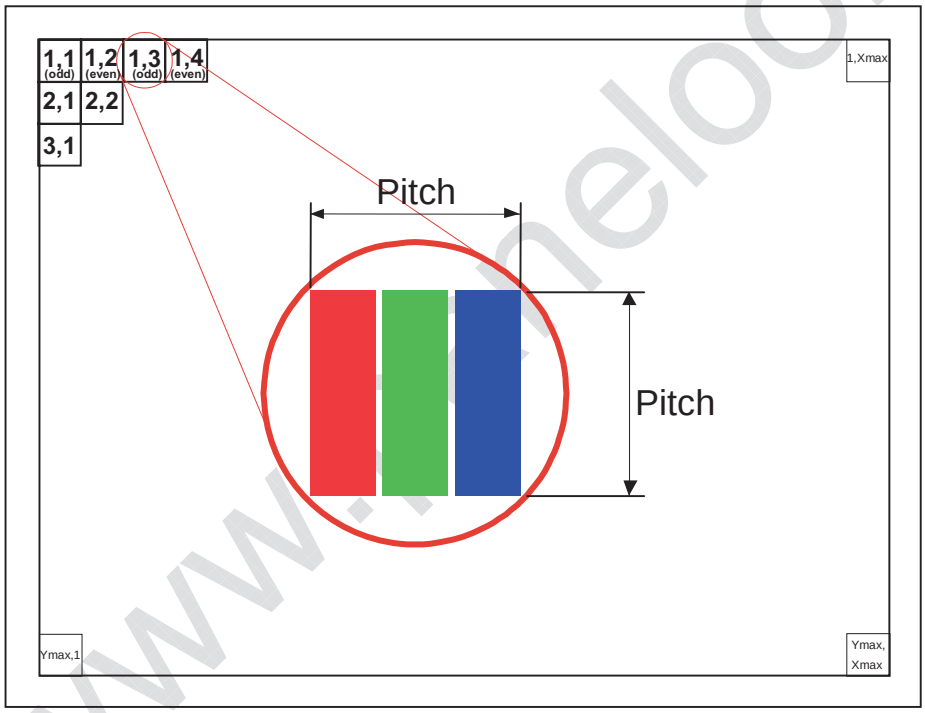
PIN ASSIGNMENT

Pin	Symbol	I/O	Description	Remark
1	VDD	P	3.3V input	3.0V~3.6V
2	VDD	P	3.3V input	3.0V~3.6V
3	VDD	P	3.3V input	3.0V~3.6V
4	VDD	P	3.3V input	3.0V~3.6V
5	NC(BIST)		Normal Operation/BIST pattern select.	1.4V~1.6V
6	NC(MTP)		No connection, please keep it floating	7.4V~7.6V
7	LED_PWM_IN	I	ALS sensor PWM signal input.	3.0V~3.6V
8	LED_PWM_OUT	O	PWM control signal for LED driver (CABC)	3.0V~3.6V
9	NC(SCL)	O	No connection	
10	NC(SDA)	O	No connection	
11	GND	P	Ground	
12	D0+	I	MIPI differential data0 input (Positive)	
13	D0-	I	MIPI differential data0 input (Negative)	
14	GND	P	Ground	
15	D1+	I	MIPI differential data1 input (Positive)	
16	D1-	I	MIPI differential data1 input (Negative)	
17	GND	P	Ground	
18	CLK+	I	MIPI differential clock input (Positive)	
19	CLK-	I	MIPI differential clock input (Negative)	
20	GND	P	Ground	
21	D2+	I	MIPI differential data2 input (Positive)	
22	D2-	I	MIPI differential data2 input (Negative)	
23	GND	P	Ground	
24	D3+	I	MIPI differential data3 input (Positive)	

25	D3-	I	MIPI differential data3 input (Negative)	
26	GND	P	Ground	
27	GND	P	Ground	
28	ID		3.3V	
29	STBYB	I	3.3V	3.0V~3.6V
30	LED1	P	Cathode for light bar	
31	LED2	P	Cathode for light bar	
32	LED3	P	Cathode for light bar	
33	NC		NC	
34	NC		NC	
35	NC		NC	
36	NC(WPN)		No connection, please keep it floating	
37	NC			
38	VLED	P	Anode for light bar	22.4V
39	VLED	P	Anode for light bar	22.4V

Note (1) The first pixel is odd as shown in the following figure.

Note (2) Normal operation/BIST pattern selection. (Control by MIPI LP Command)



4.3 ELECTRICAL CHARACTERISTICS

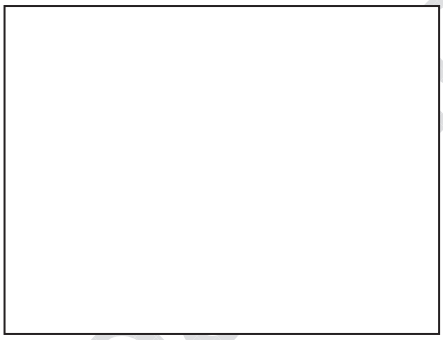
4.3.1 LCD ELETRONICS SPECIFICATION

Item		Symbol	Values			Unit	Remark
			Min.	Typ.	Max.		
Power supply voltage		VDD	3.0	3.3	3.6	V	
VDD High level input voltage		V_{IH1}	0.7 VDD	-	VDD	V	Applicable Pin： STBYB、LED_PWM_IN
VDD Low level input voltage		V_{IL1}	0	-	0.3 VDD	V	
Power Supply Current	White	Ivdd		116	120	mA	Note (2)

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) The specified power supply current is under the conditions at VDD = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

b. White Pattern



Active Area

4.3.2 LED CONVERTER SPECIFICATION

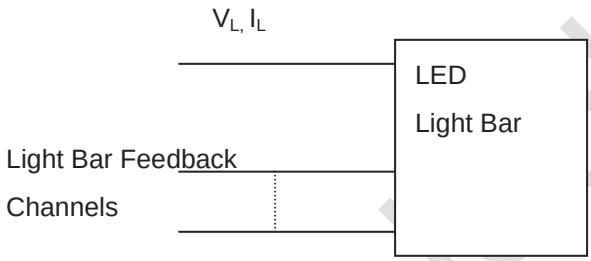
N/A

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L			22.4	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	-	63	-	mA	
Power Consumption	P_L	-		1.42	W	(3)
LED Life Time	L_{BL}	15,000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and I_L = 21 mA(Per EA) until the brightness becomes ≦ 50% of its original value.

4.3.4 SIGNAL TIMING SPECIFICATIONS

Signal	Item	Symbol	Min.	Typ.	Max.	Unit
DCLK	Frequency	1/Tc	-	159.4	-	MHz
DE	Vertical Total Time	TV	1981	1981	1982	TH
	Vertical Active Display Period	TVD	-	1920	-	TH
	Vertical Front Porch Period	TVFP	35	35	36	TH
	Vsync pulse width	TVPW	1	1	1	TH
	Vertical Back Porch Period	TVBP		25		TH
	Horizontal Total Time	TH	1275	1341	1342	Tc
	Horizontal Active Display Period	THD	-	1200	-	Tc
	Horizontal Front Porch Period	THFP	42	80	81	Tc
	Horizontal pulse width	THPW	1	1	1	Tc
	Horizontal Back Porch Period	THBP	32	60	60	Tc
	MIPI Data frequency	FDATA	955	999	1000	MHz

Note: DCLK = TV x TH x frame rate, and frame rate = 60Hz.

4.4 MIPI Interface DC/AC Characteristic

4.4.1 MIPI Interface DC characteristic

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
MIPI digital operation current	I_{VCCIF}	VCC=VCC_IF=1.6V, Data Rate=500Mbps,	-		24	mA
MIPI digital stand-by current	$I_{VCCIFST}$	VCC_IF input current. All input signal are stopped.	-	200	-	uA
MIPI Characteristics for High Speed Receiver						
Single-endedl input low voltage	V_{ILHS}		-40	-	-	mV
Single-endedl input high voltage	V_{IHHS}		-	-	460	mV
Common-mode voltage	V_{CMRXDC}		155	-	330	mV
Differential input impedance	Z_{ID}		80	100	125	ohm
Differential input high threshold	V_{IDTH}			-	70	mV
Differential input low threshold	V_{IDTL}		70	-	-	mV
MIPI Characteristics for Low Power Mode						
Pad signal voltage range	V_I		-50	-	1350	mV
Ground shift	V_{GNDSH}		-50	-	50	mV
Output low level	V_{OL}		-150		150	mV
Output high level	V_{OH}		1.1	1.2	1.3	V

Note 1) VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85℃

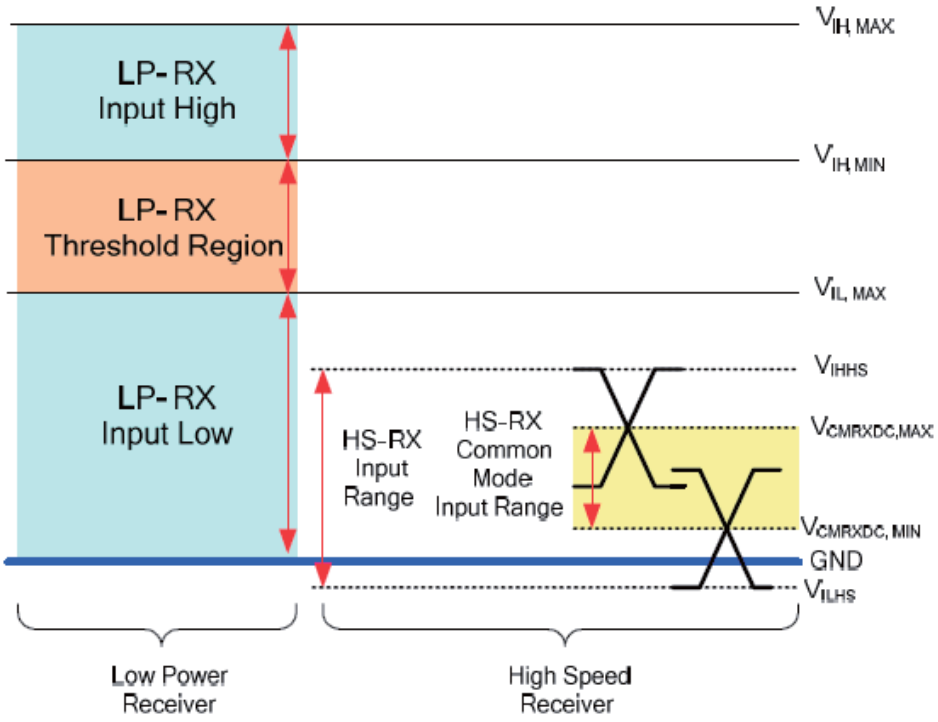


Figure :MIPI DC Diagram

4.4.2 MIPI AC Characteristic

4.4.2.1 LP Transmission

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85℃)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
15%-85% rise time and fall time	T_{RLP} / T_{FLP}	-	-	25	ns
Pulse width of the LP exclusive-OR clock	$T_{LP-PULSE-TX}$	-50	-	-	ns
Period of the LP exclusive-OR clock	$T_{LP-PER-TX}$	100			ns

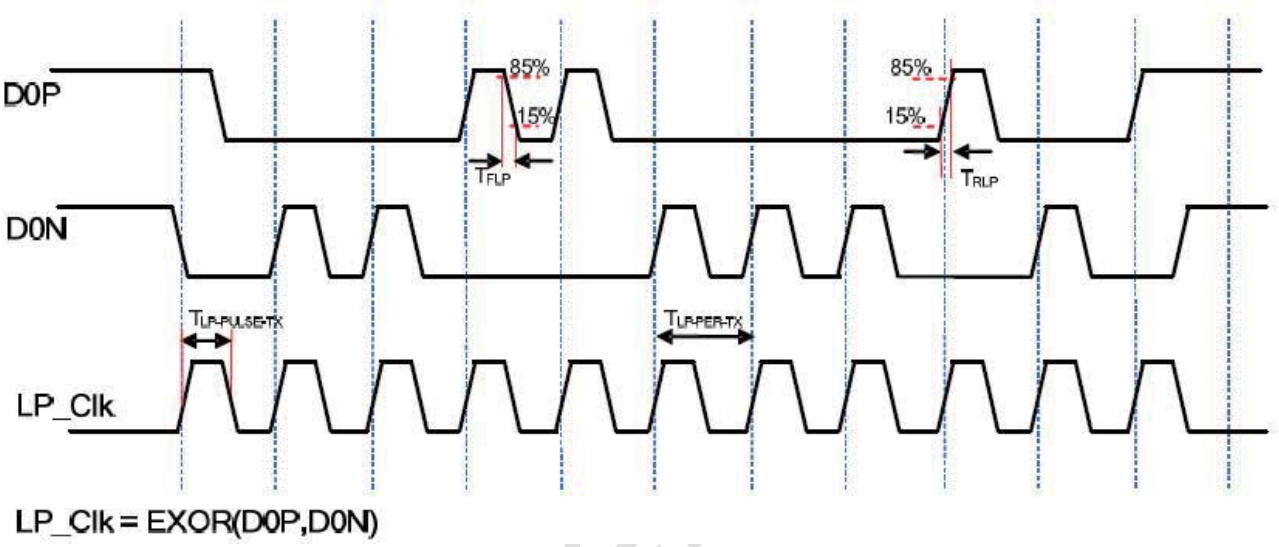


Figure :LP Transmitter Timing Definitions

4.4.3 High Speed Transmission

4.4.3.1 Data-Clock Timing Specifications

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85℃)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
UI instantaneous	UI_{INST}	1.0	-	12.5	ns
Data to Clock Setup Time	T_{SETUP}	0.25	-	-	UI_{INST}
Data to Clock Hold Time	T_{HOLD}	0.25	-	-	UI_{INST}

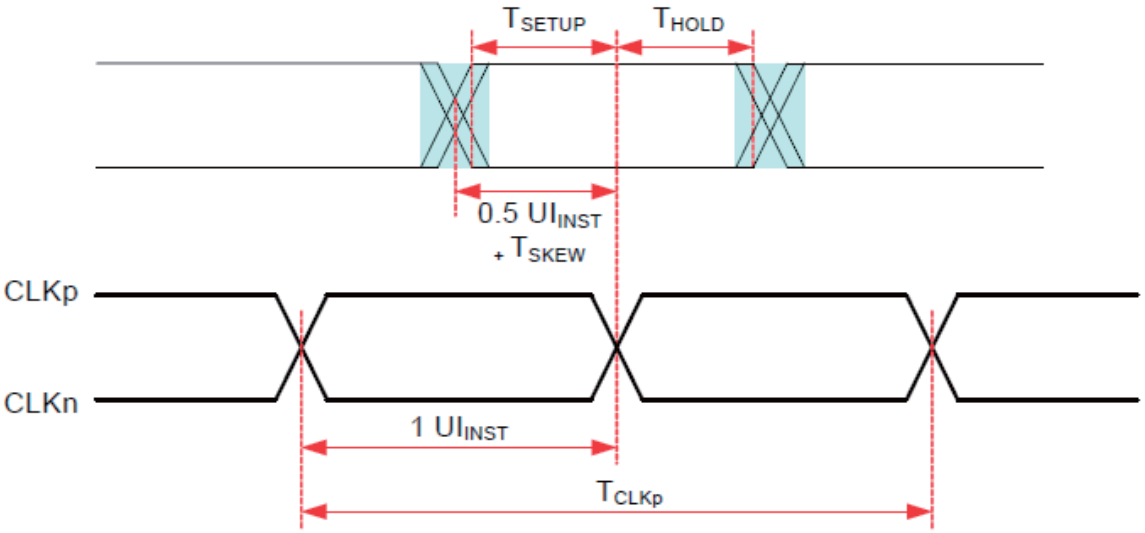


Figure : Data to Clock Timing Definitions

4.4.3.2 High-Speed Data Transmission in Bursts

4.4.3.2.1 High-Speed Data Transmission Operation Timing Parameters

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85℃)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state	T_{EOT}	-	-	105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$	-	-	35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI	-	-	ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
Length of any Low-Power state period	T_{LPX}	50	-	-	ns
Sync sequence period	$T_{HS-SYNC}$	-	8UI	-	ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI	-	-	ns

Note:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. UI means Unit Interval, equal to one half HS clock period on the Clock Lane.
3. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

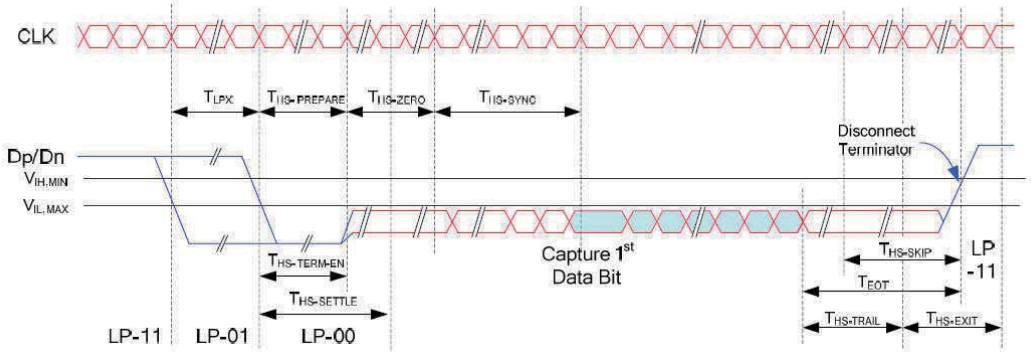


Figure : High-Speed Data Transmission in Bursts

4.4.3.3 High-Speed Clock Transmission

4.4.3.3.1 Switching the Clock Lane Operation Timing Parameters

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85℃)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$	-	-	60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38	-	95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns

Note:

The DSI host processor shall support continuous clock on the Clock Lane for NT chip that require it, so the host processor needs to keep the HS serial clock running.

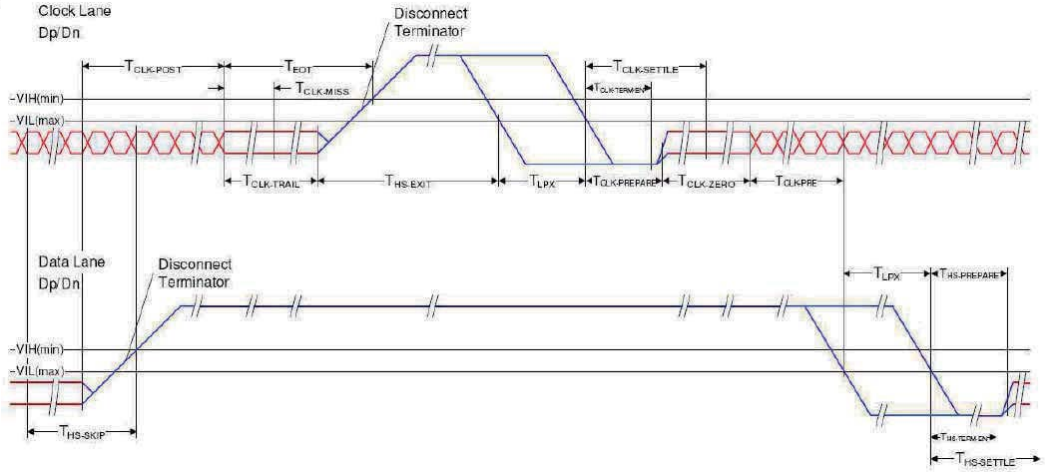
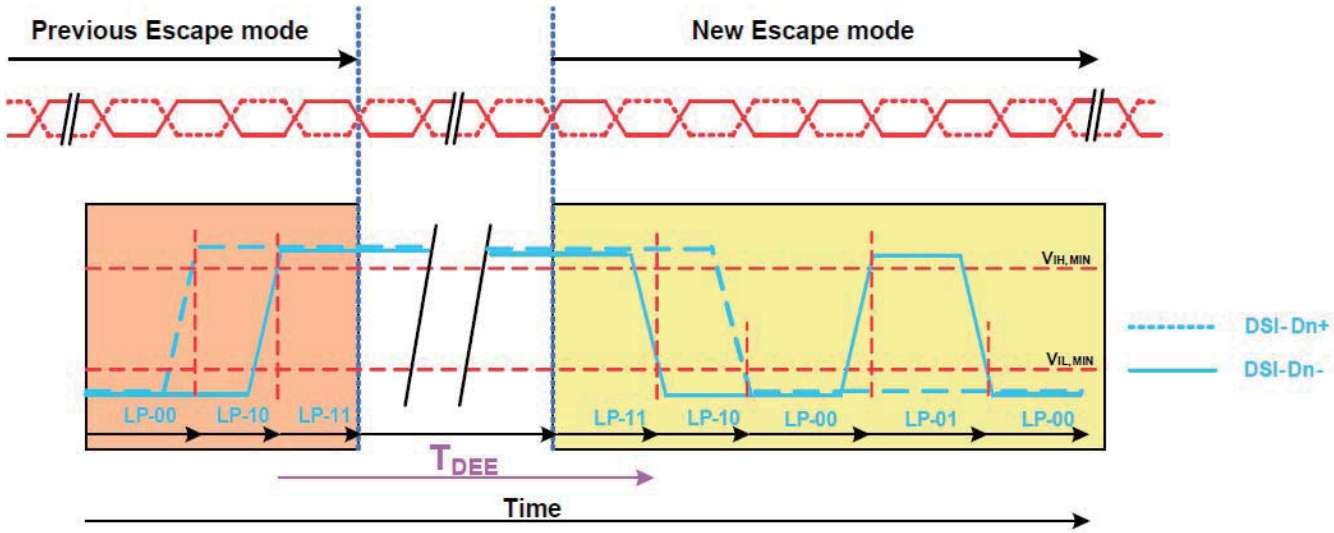


Figure :Switching the Clock Lane between Clock Transmission and Low-Power Mode

4.4.3.4 LP11 timing request between data transformation

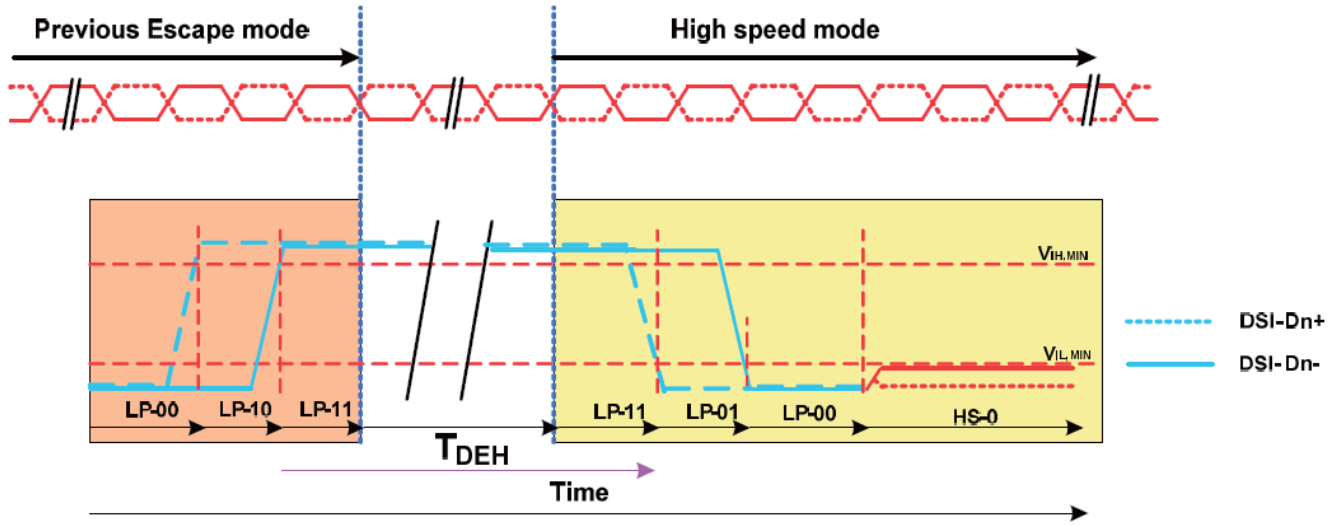
When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Low power mode. If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode. The LP-11 minimum timing is required for RX chip in the following 9 conditions, include of LP - LP, LP - HS, HS - LP, and HS – HS. This rule is suitable for short or long packet between TX and RX data transmission.

(1) Timing between LP - LP command



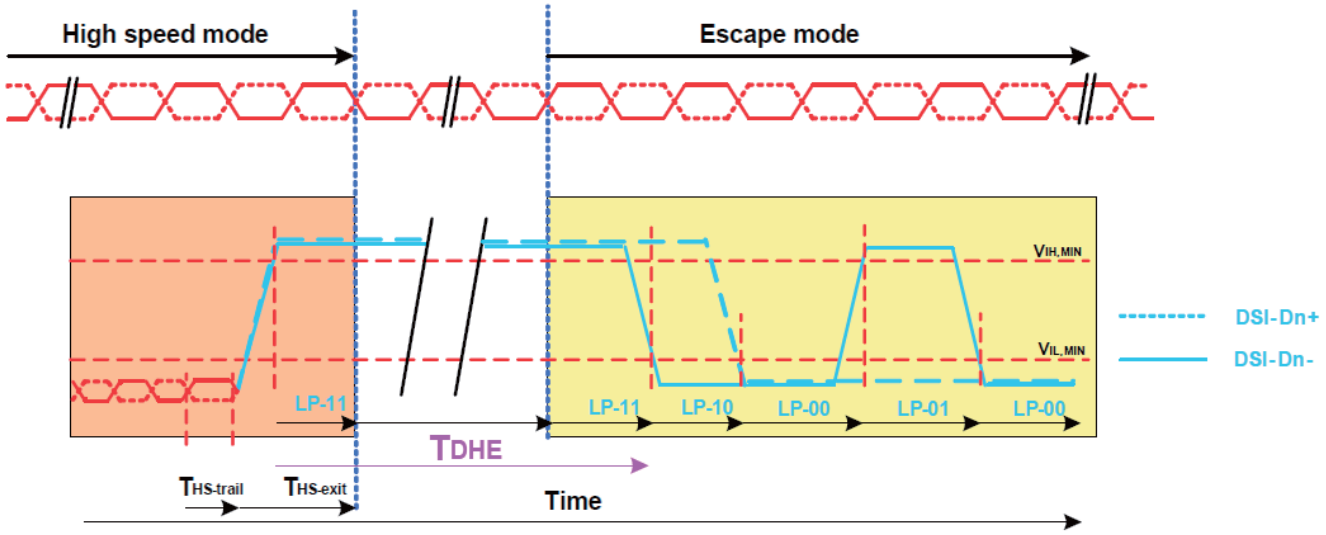
Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the new Escape Mode Entry	T_{DEE}	150	-	-	ns

(2)Timing between LP - HS command



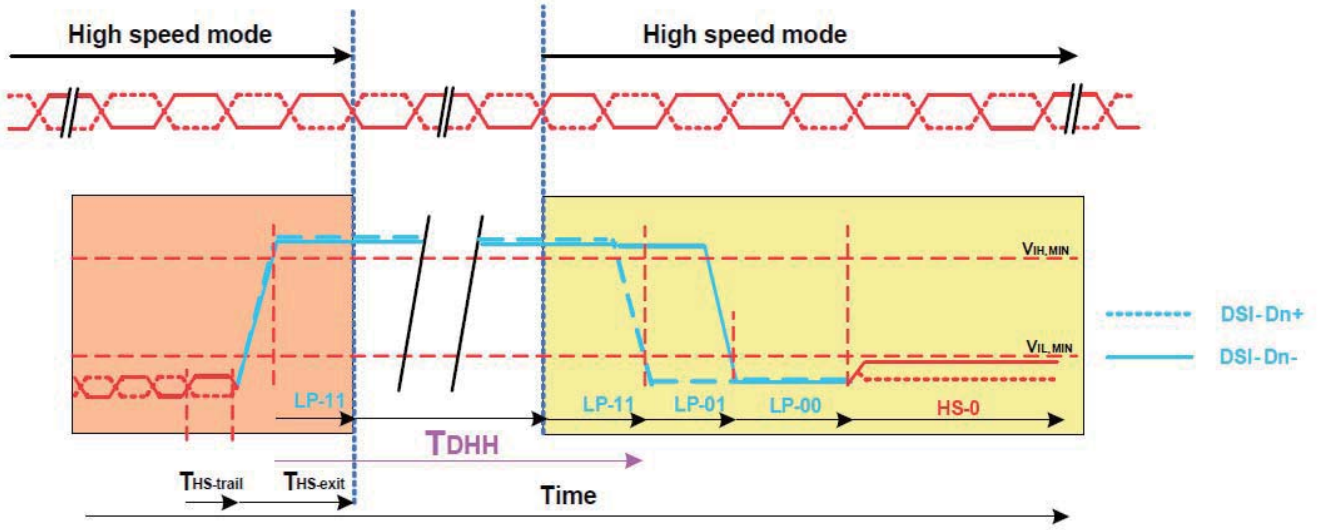
Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the Entering High Speed Mode	T_{DEH}	Max(150,32UI)	-	-	ns

(3)Timing between HS - LP command



Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the Escape Mode Entry	T_{DHE}	Max(150,32UI)	-	-	ns

(4)Timing between HS - HS command



Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the Entering High Speed Mode	T_{DHH}	Max(150,32UI)	-	-	ns

4.5 MIPI interface (Mobile Industry Processing Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards. DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers. Systems using Command Mode write to, and read from the registers.The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Note: The NT51021 IC only supports Video Mode operation.

4.5.1 MIPI Lane Configuration

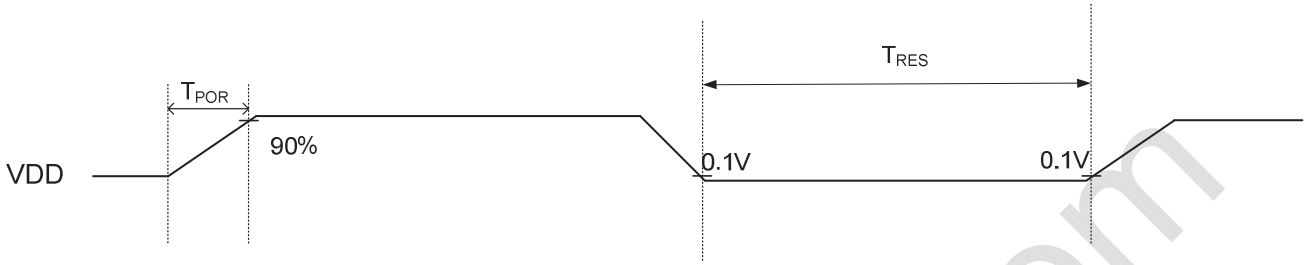
	MCU (Master) Display Module (Slave)
Clock Lane+/-	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane0+/-	Unidirectional Lane ■ Forward High-Speed ■ Forward Escape Mode ■ Forward LPDT
Data Lane1+/-	Unidirectional ■ Forward High speed
Data Lane2+/-	Unidirectional ■ Forward High speed
Data Lane3+/-	Unidirectional ■ Forward High speed

The connection between host device and display module is as reference.

4.6 Input AC Characteristic

a. VDD AC characteristic:

VDD= 3..3V, GND=AGND= 0V, TA= -20 to +85℃)



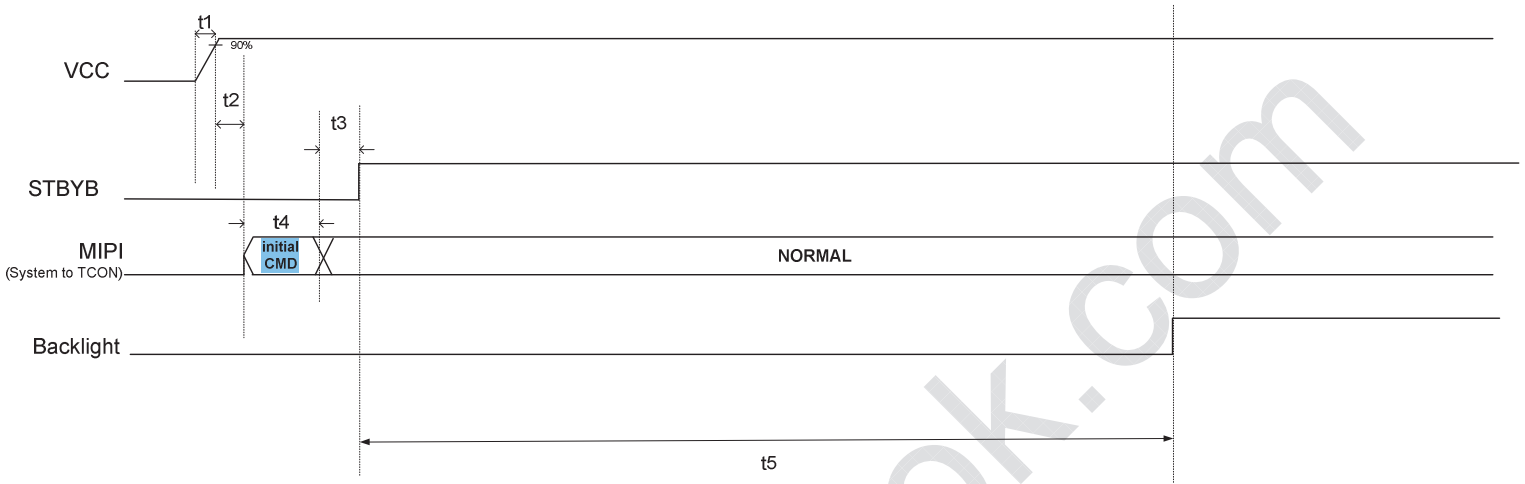
Parameter Symbol	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD power source slew time	T_{POR}	-	-	20	ms	From 0V to 90% VDD
VDD resettle time	T_{RES}	1	-	-	s	

4.7 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.

a. Power on Timing Sequence:

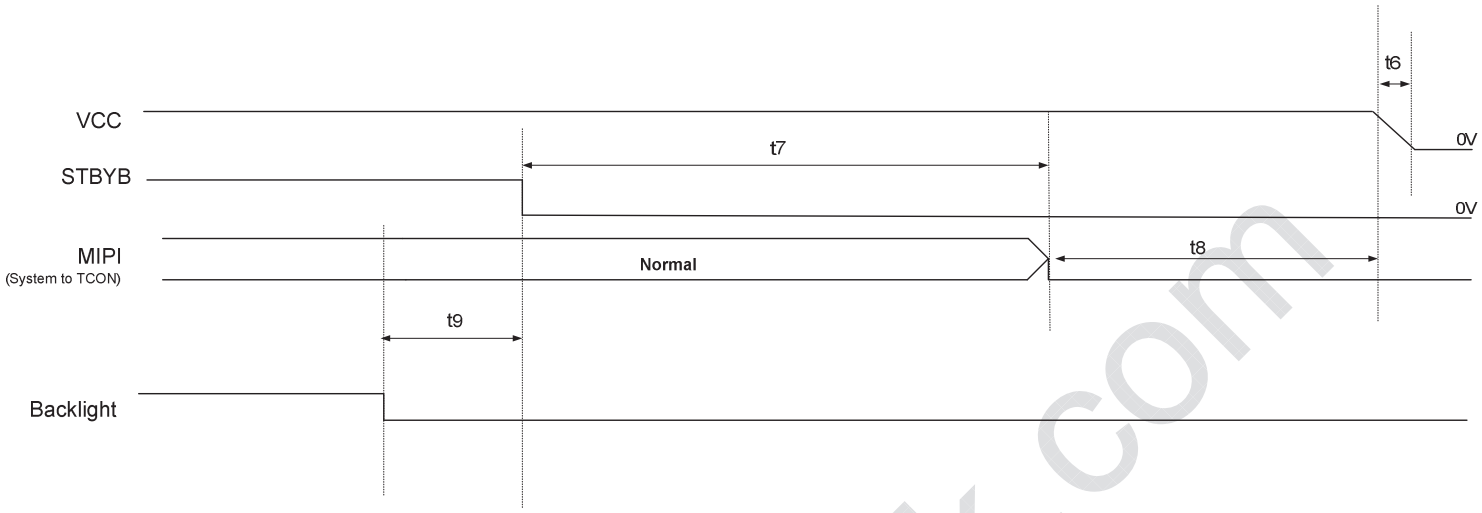
VDD=3.0 to 3.6V



Symbol	Value			Unit	Remark Min.
	Min.	Typ.	Max.		
t1	-	-	2	t1	-
t2	300	-	-	t2	
t3	10	-	-	t3	
t4	0	-	-	t4	
t5	100	-	-	t5	

b. Power off Timing Sequence:

VDD=3.0 to 3.6V



Symbol	Value			Unit	Remark Min.
	Min.	Typ.	Max.		
t6	0	-	-	t6	
t7	100	-	-	t7	
t8	0	-	-	t8	
t9	20	-	-	t9	

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

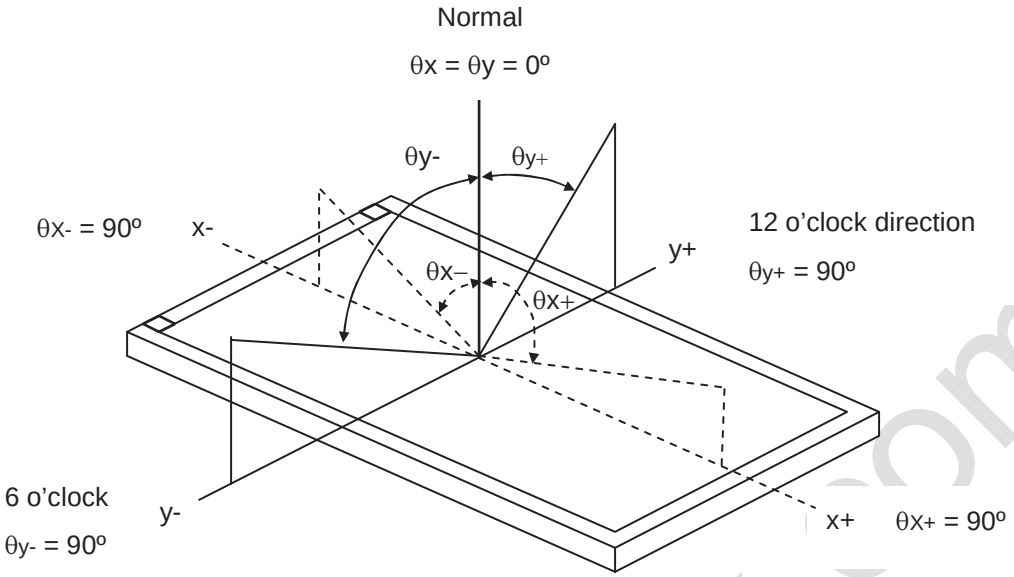
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VDD	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	63	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° CS-2000 R=G=B=255 Gray scale	700	900	-	-	(2),(5),(7)
Response Time		$T_{R+}T_F$		-	25	30	ms ms	(3),(7)
CP Luminance of White		L_{CP}		340	400	-	Cd/m^2	(4),(6),(7)
	White	Wx		Typ – 0.03	0.300	Typ + 0.03	-	(4),(6),(7)
		Wy			0.320		-	
	Red	Rx			0.613			
		Ry			0.350			
	Green	Gx			0.325			
		Gy			0.605			
	Blue	Bx			0.152			
		By			0.071			
Viewing Angle	Horizontal	x- + x+	CR > 10	170	178	-	Deg.	(1),(5),(7)
	Vertical	y- + y+		170	178	-		
White Variation of 5 Points		δW_{5p}	θ_x=0°, θ_Y =0°	80			%	(5),(6),(7)
White Variation of 13 Points		δW_{13p}		67				
Color Gamut				55	60		%	(5),(6),(7)

Note (1) Definition of Viewing Angle (θx, θy)



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

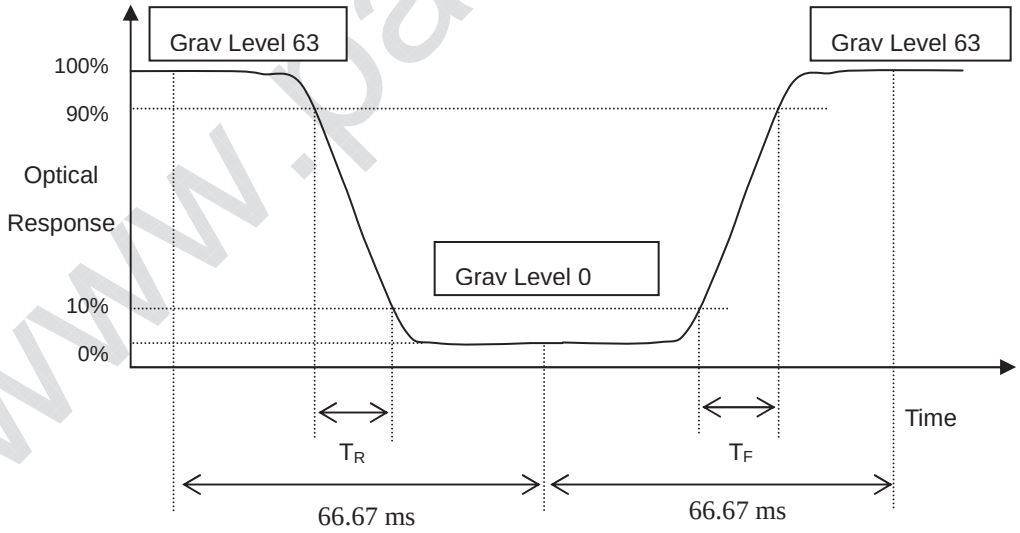
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Center Point Luminance of White (L_{CP}):

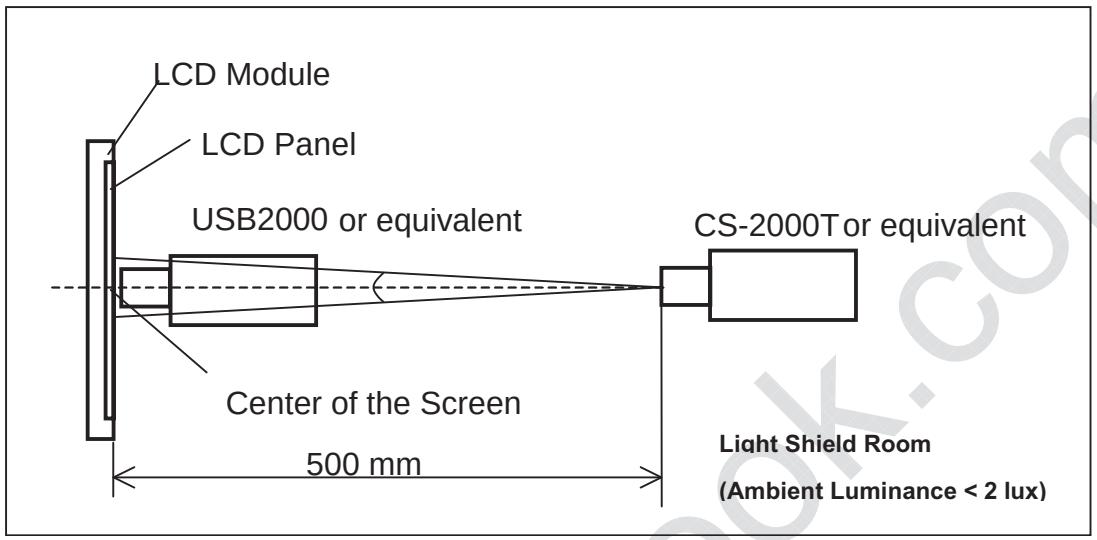
Measure the luminance of gray level 63 at center point

L_{CP} = L(5)

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

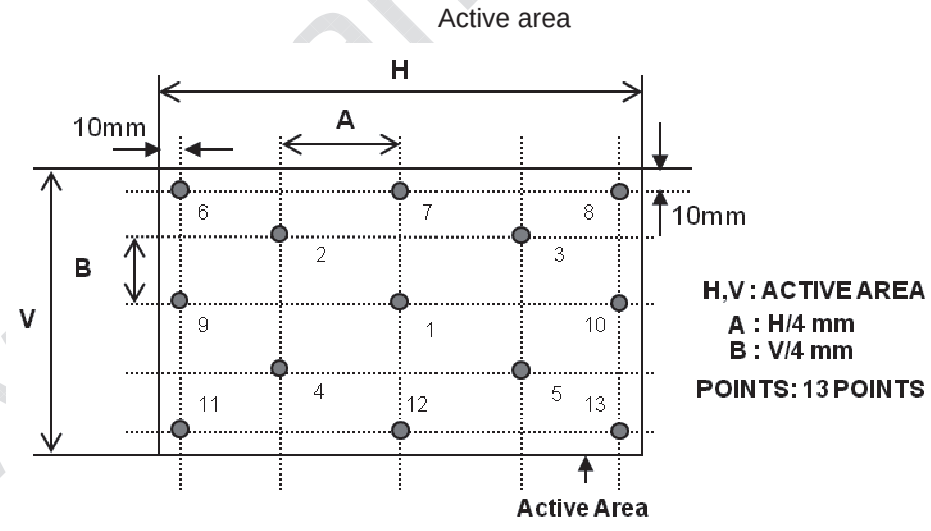
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 13 points

δW_{9p} = {Minimum [L (1) ~ L (13)] / Maximum [L (1) ~ L (13)]}*100%



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	70ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→70℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	60ºC, 240 hours	
Low Temperature Operation Test	-10ºC, 240 hours	
High Temperature & High Humidity Operation Test	60ºC, RH 90%, 240hours	
ESD Test (Operation)	Condition 1 : Contact Discharge, ± 4KV (Module level) Condition 2 : Air Discharge, ± 8KV (Module level)	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

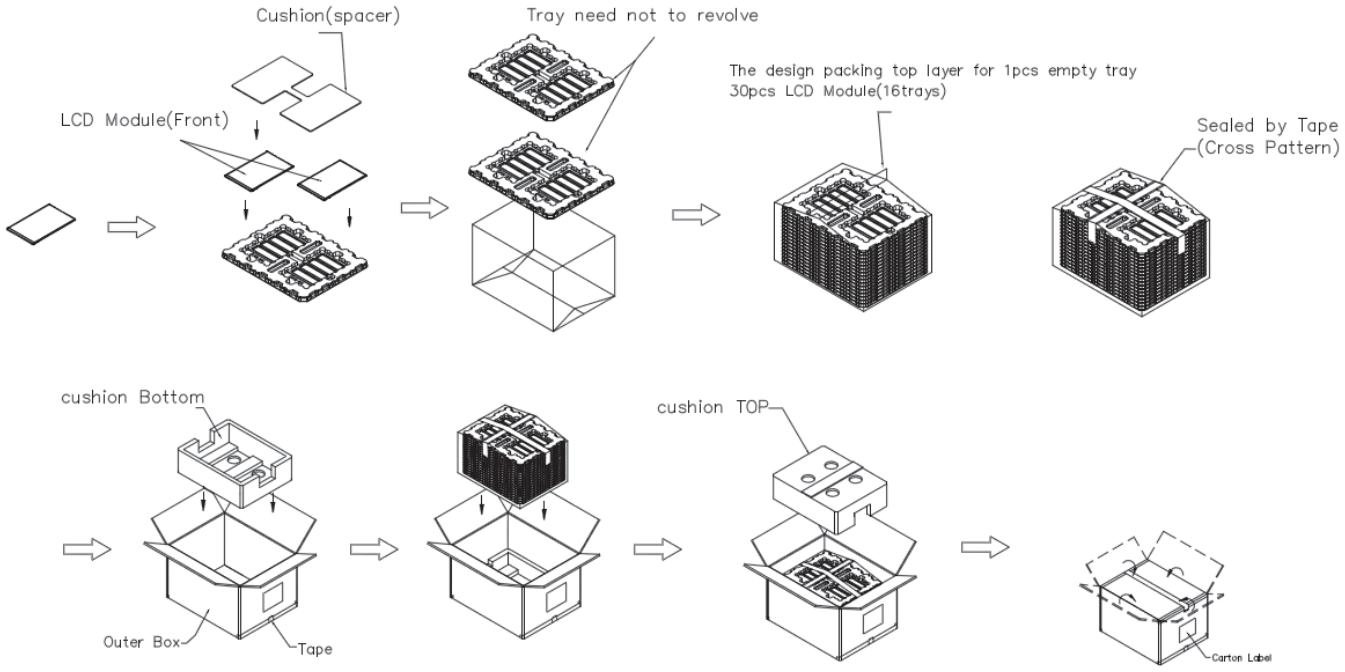
Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. Package

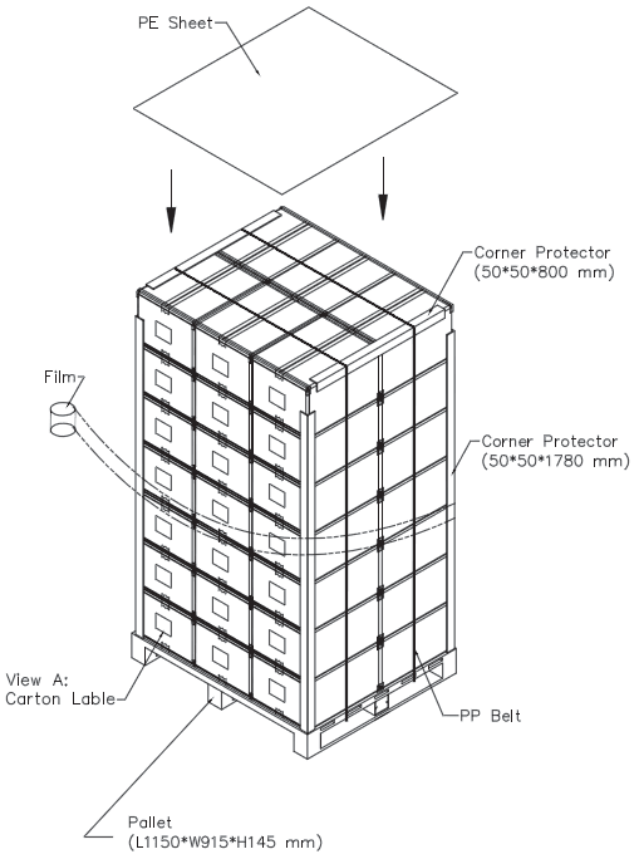
7.1. Packing Description



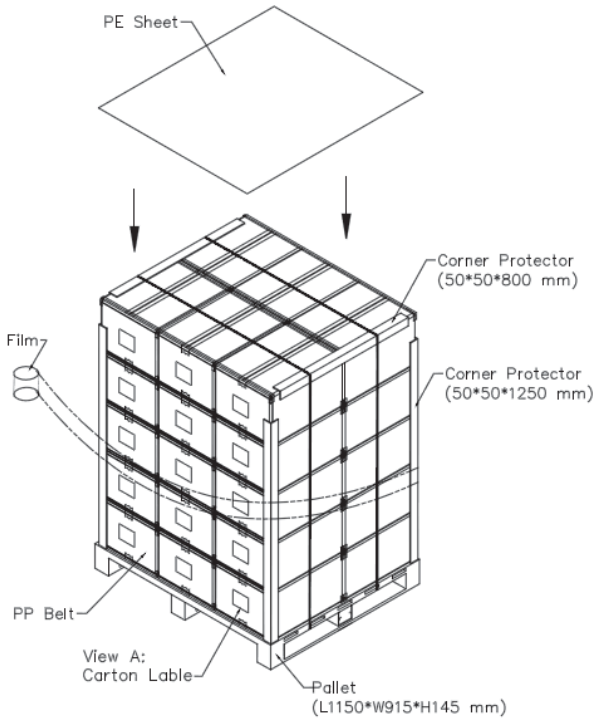
(1) Box Dimensions : 435(L)*350(W)*275(H)
(2) 30 Modules/Carton

7.2. Description of Pallet

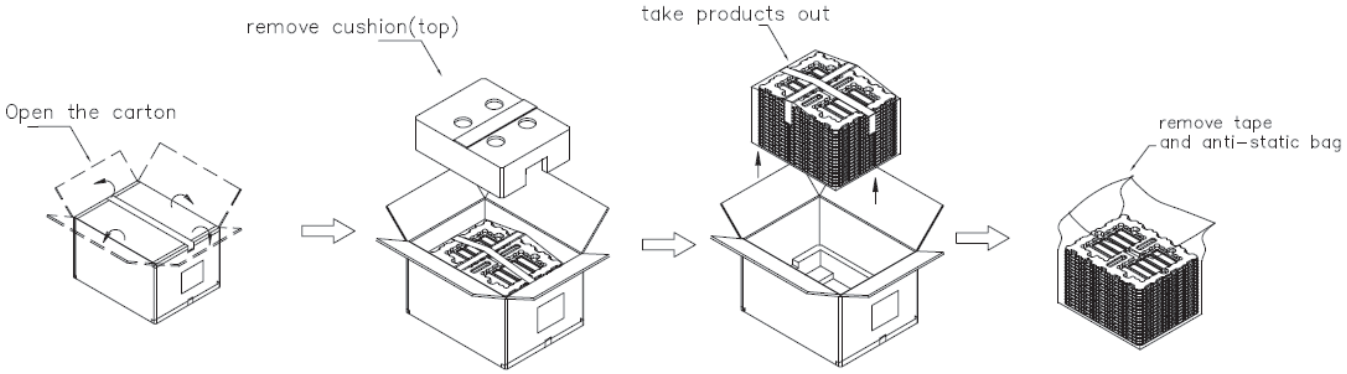
Sea & Land Transportation

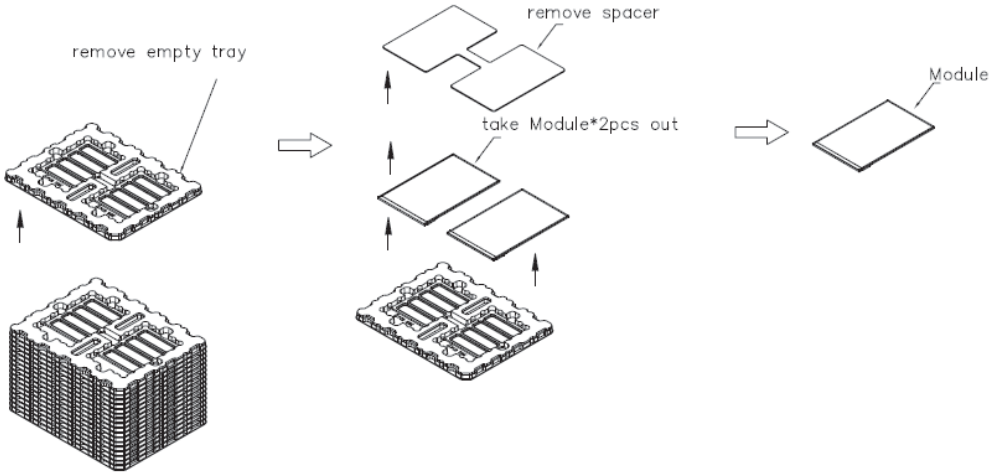


Air Transportation

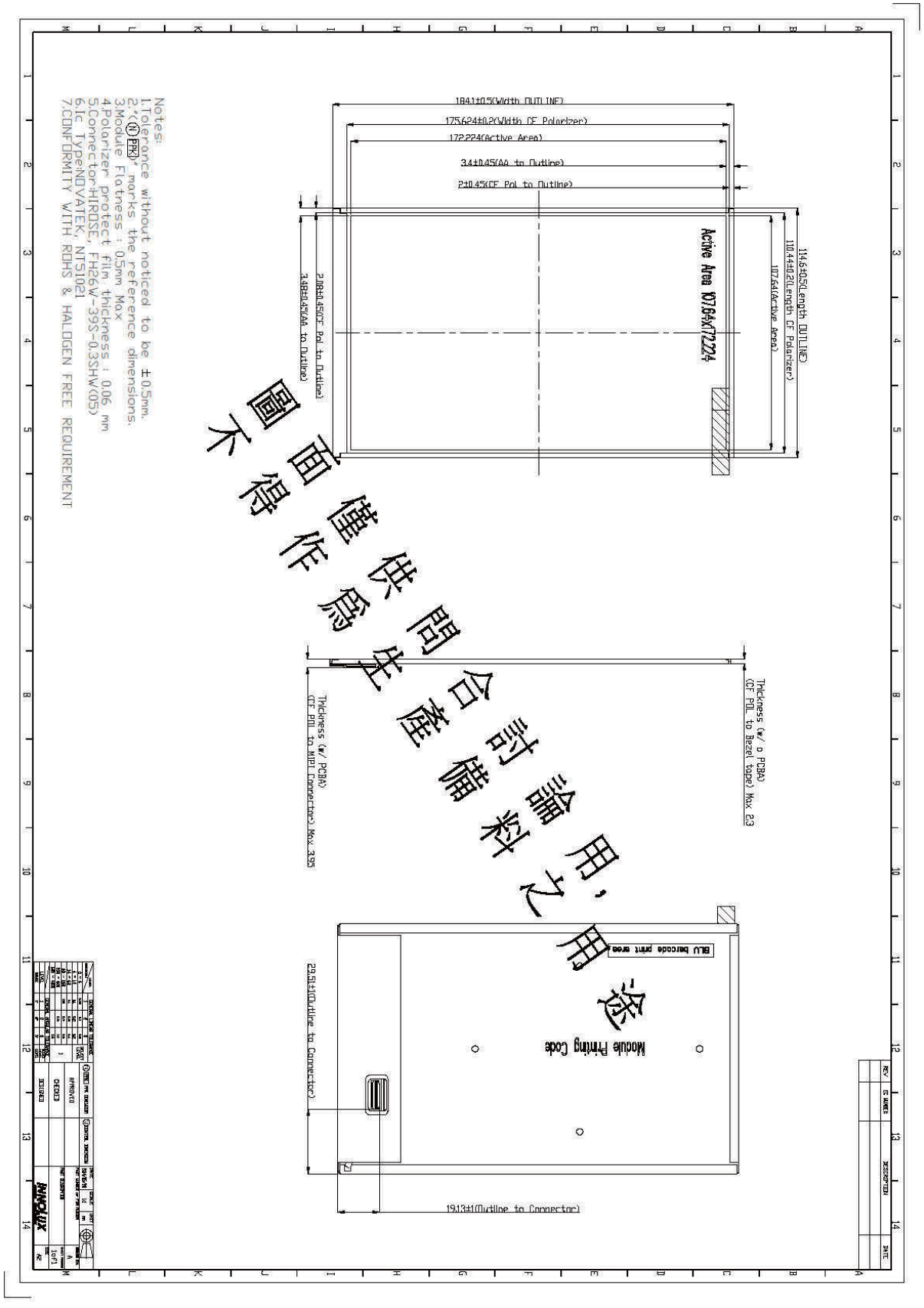


7.3. Un-Packing Description





Appendix. OUTLINE DRAWING (Label position will be updated as requirement)



Appendix. NT51021 Register setting (Used by MIPI LP-command)

REGW 0x83, 0xAA
REGW 0x84, 0x11
REGW 0xA9, 0x4B

Note: Please provide the final set to Innolux for checking MIPI signal integrity. After confirming, the optimized MIPI code would be provided.