




Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications

() Final Specifications

Module	13.3" WXGA Color TFT-LCD
Model Name	B133EW04 V3
Note ()	<i>LED Backlight without driving circuit design</i>

Customer

Date

Checked &
Approved by

Date

Note: This Specification is subject to change without notice.

Approved by

Date

Howard Lee

11/30/2008

Prepared by

Date

Johnson Kuo

11/30/2008

**NBBU Marketing Division /
AU Optronics corporation**



Contents

1. Handling Precautions	4
2. General Description	5
2.1 General Specification	5
2.2 Optical Characteristics	6
3. Functional Block Diagram	8
4. Absolute Maximum Ratings.....	9
4.1 Absolute Ratings of TFT LCD Module	9
4.2 Absolute Ratings of Backlight Unit.....	9
4.3 Absolute Ratings of Environment	9
5. Electrical characteristics	10
5.1 TFT LCD Module.....	10
5.2 Backlight Unit	12
6. Signal Characteristic	13
6.1 Pixel Format Image	13
6.2 The input data format	14
6.3 Signal Description/Pin Assignment.....	15
6.4 Interface Timing	16
7. Connector Description.....	19
7.1 TFT LCD Module.....	19
8. Dynamic Test	20
8.1 Vibration Test	20
8.2 Shock Test Spec:.....	20
9. Reliability.....	21
10. Mechanical Characteristics.....	22
10.1 LCM Outline Dimension.....	22
11. Shipping and Package	26
11.1 Shipping Label Format	26
11.2 Carton package	27
11.3 Shipping package of palletizing sequence	27
12. Appendix: EDID description	29



Product Specification

AU OPTRONICS CORPORATION

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2008/08/29	All	First Edition for Customer		



1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lamp Reflector edge. Instead, press at the far ends of the LED lamp Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



Product Specification

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2. General Description

B133EW04 V3 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver) without backlight inverter. All input signals are LVDS interface compatible.

B133EW04 V3 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	337.8 (13.3W")			
Active Area	[mm]	286.08 (H) X 178.8 (V)			
Pixels H x V		1280x3(RGB) x 800			
Pixel Pitch	[mm]	0.2235 x 0.2235			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance Note: ILED is lamp current	[cd/m ²]	275 typ @ 95% duty cycle 248 min @ 95% duty cycle			
Luminance Uniformity	%	50 max. (160 points)			
Contrast Ratio		500 typ, 400min			
Response Time	[ms]	16 typ, 25 max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.3 W @ Black (typical)			
Weight	[Grams]	300(typical), 310 (max.)			
Physical Size	[mm]		L	W	T
		Max			3.6
		Typical	297.15	203.15	-
		Min			-
Electrical Interface		one channel LVDS			
Surface Treatment		Glare, Hardness 3H,			



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Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -25 to +65
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance	[cd/m ²]	160 points average	248	275	-	1,2,3
Viewing Angle	[degree] [degree]	Right/left	40/40	50/50	- -	1,2,3
	[degree] [degree]	Up Down	15 30	25 35	- -	
Luminance Uniformity	%	160 point	50	-		1,2
CR: Contrast Ratio			400	500	-	1,2,3
Cross talk	%	Optical			2.0	1,2,3
Response Time	[msec]	Rising + Falling	-	16	25	1,2,3
Chromaticity of color Coordinates (CIE 1931) NTSC	%	Red x	0.575	0.595	0.615	
		Red y	0.325	0.345	0.365	
		Green x	0.300	0.320	0.340	
		Green y	0.535	0.555	0.575	
		Blue x	0.135	0.155	0.175	
		Blue y	0.125	0.145	0.165	
		White x	0.297	0.313	0.329	
		White y	0.313	0.329	0.345	
		CIE 1931	-	45	-	



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Note 1: The testing conditions are specified in 2.3

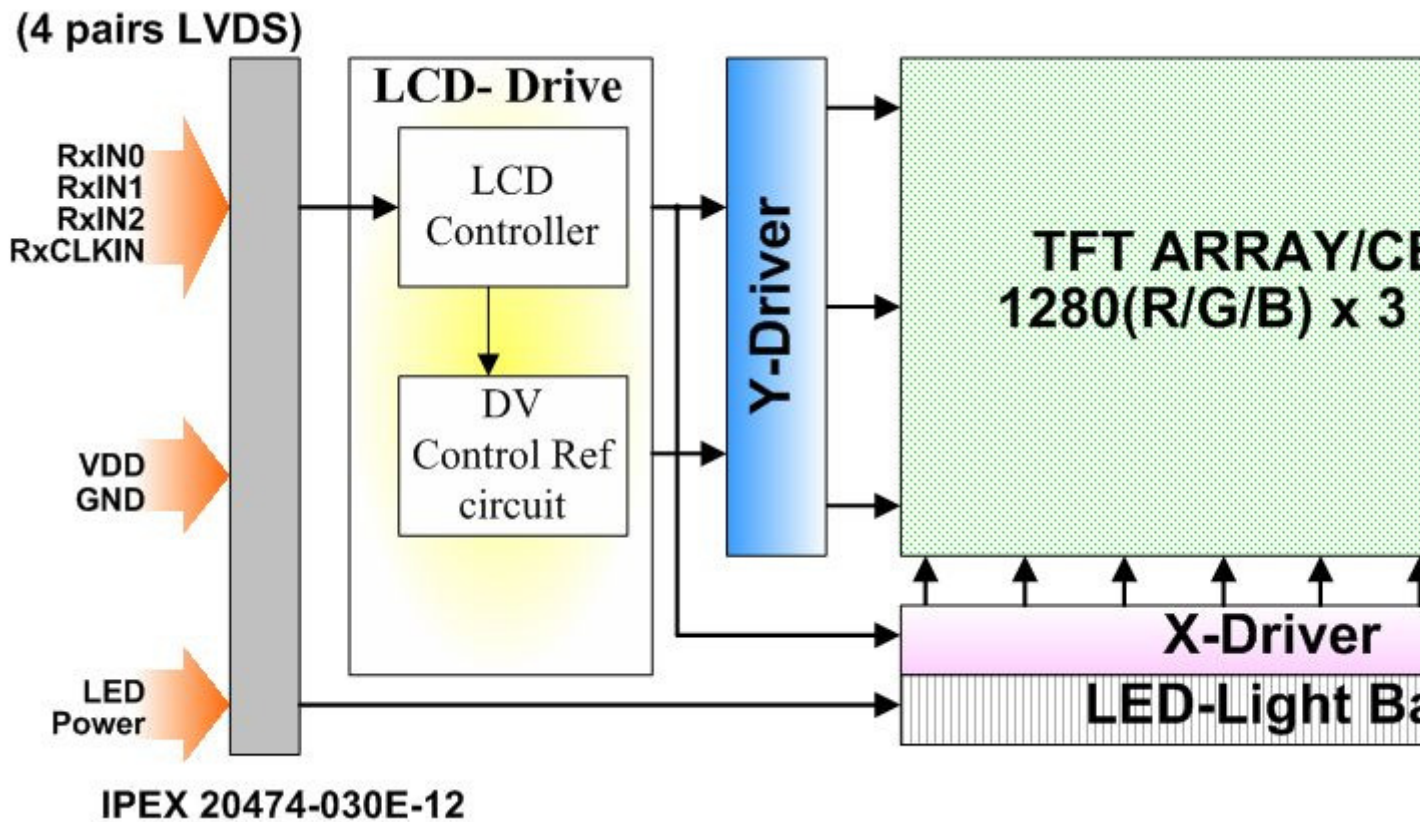
Note 2: The definitions of optical characteristics are shown in 2.4

Note 3: Measured at center point. Equivalent performance over the entire panel required

Note 4: Both center point and average of 160 points

3. Functional Block Diagram

The following diagram shows the functional block of the 13.3 inches wide Color TFT/LCD Module:



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V _{in}	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
LED Current	I _{LED}	-	35	[mA] rms	Note 1,2

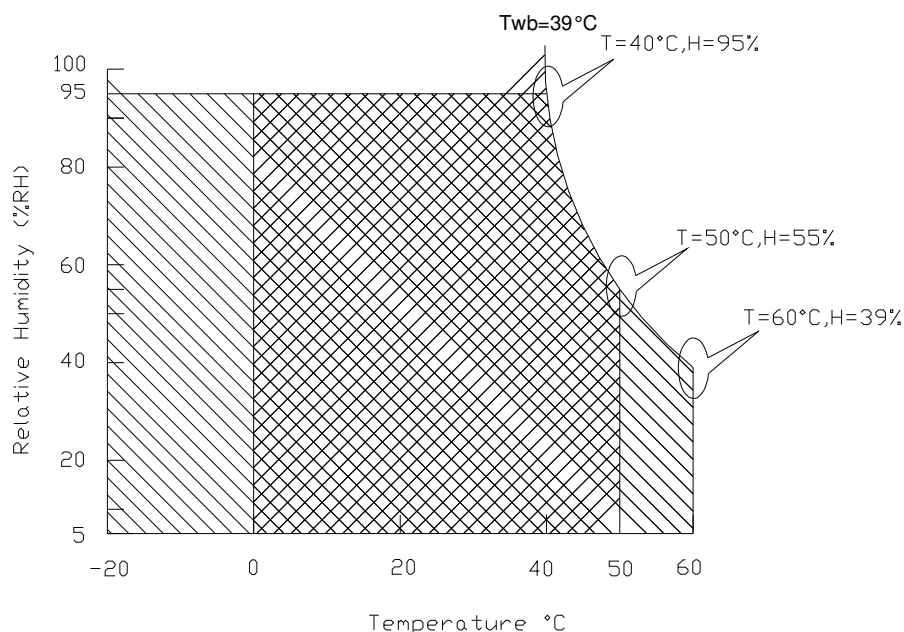
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	T _{OP}	0	+50	[°C]	Note 3
Operation Humidity	H _{OP}	5	95	[%RH]	Note 3
Storage Temperature	T _{ST}	-20	+60	[°C]	Note 3
Storage Humidity	H _{ST}	5	95	[%RH]	Note 3

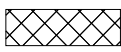
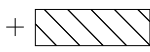
Note 1: At T_a (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

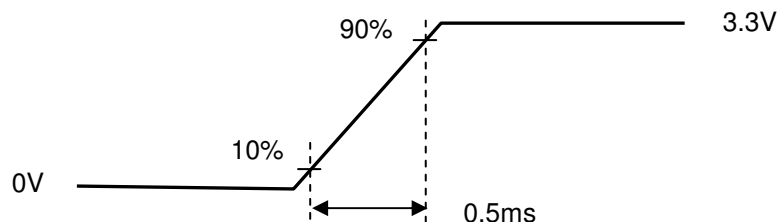
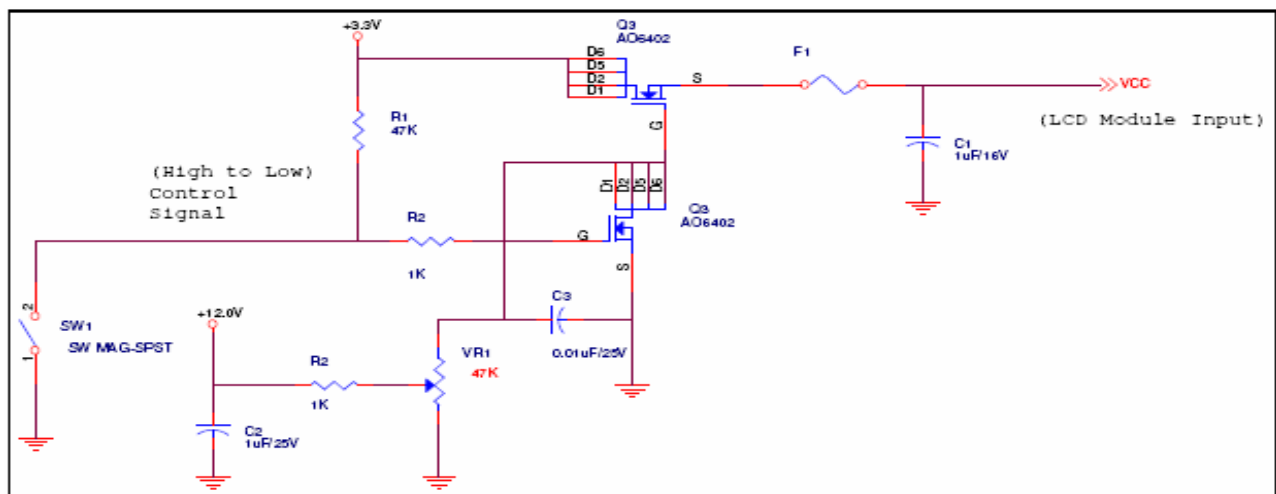
Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-		0.9	[Watt]	Note 1/2
IDD	IDD Current	-	220	250	[mA]	Note 1/2
IRush	Inrush Current	-	0.7	1.5	[A]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Typical Measurement Condition: Mosaic Pattern

Note 3 : Measure Condition



Vin rising time

5.1.2 Signal Electrical Characteristics

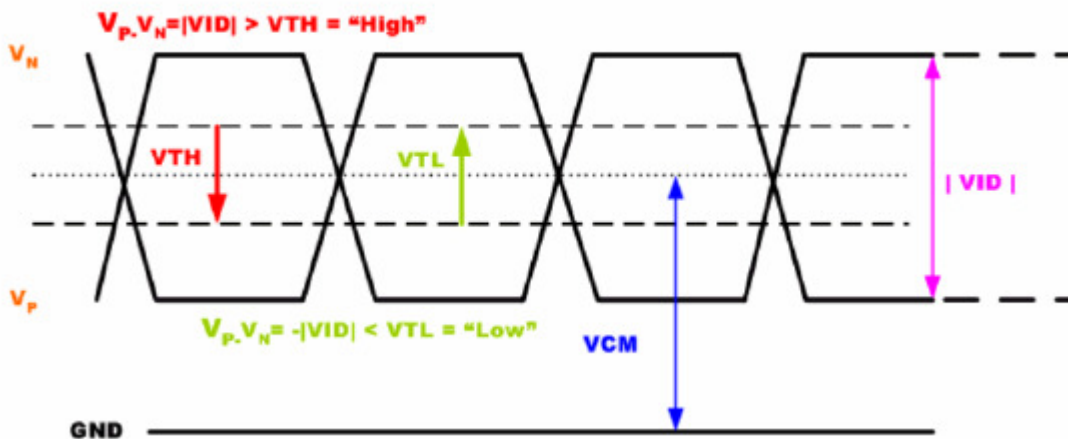
Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)	-	+100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
Vcm	Differential Input Common Mode Voltage	0.8	2.0	[V]

Note: LVDS Signal Waveform

Single-end Signal



5.2 Backlight Unit

Parameter guideline for LED

LED Parameter guideline for LED driving selection (Ref. Remark 1)

Parameter	Symbol	Min	Typ	Max	Units	Condition
LED Forward Voltage	VF	2.8	3.0	3.2	[Volt]	(Ta=25°C)
LED Forward Current	IF		20	30	[mA]	(Ta=25°C)
LED Power consumption	P _{LED}		4		[Watt]	(Ta=25°C) Note 1
LED Life-Time\	N/A	10,000	-	-	Hour	(Ta=25°C) IF=20 mA Note 2
Output PWM frequency	F _{PWM}	100	200	20K	Hz	
Duty ratio @20kHz	--	5	--	100	%	

Note 1: Calculator value for reference $IF \times VF = P$

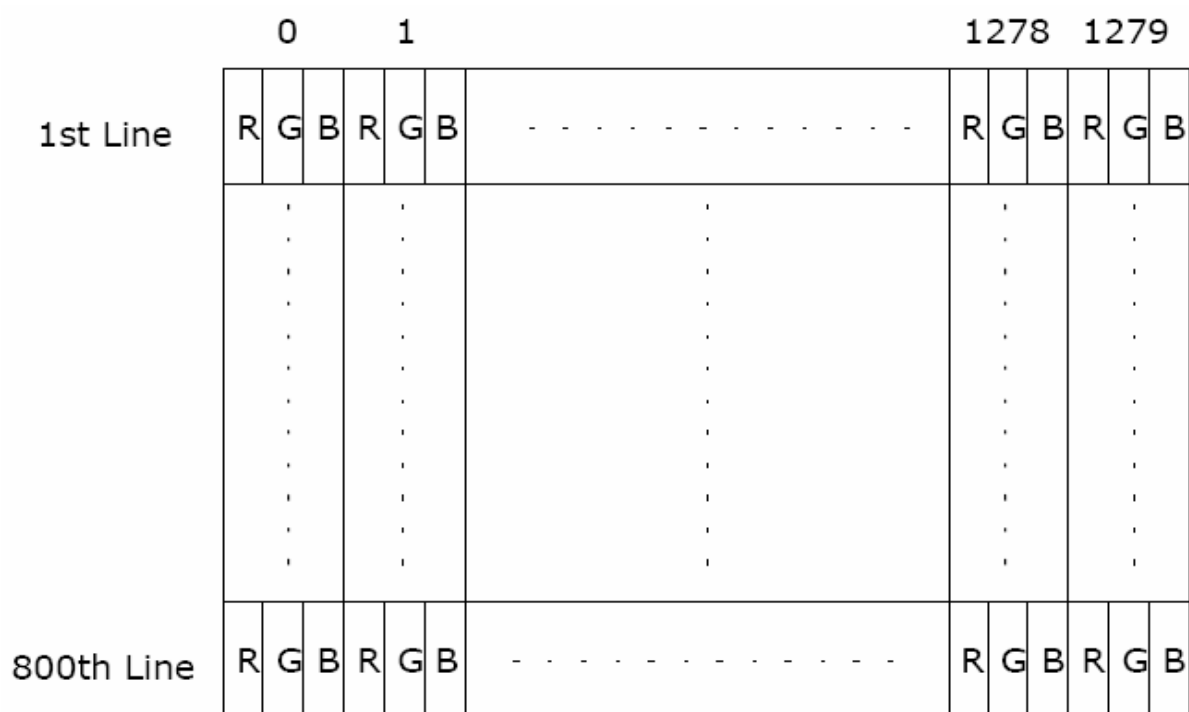
Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous

Note 3: Totally using 54 Led bins

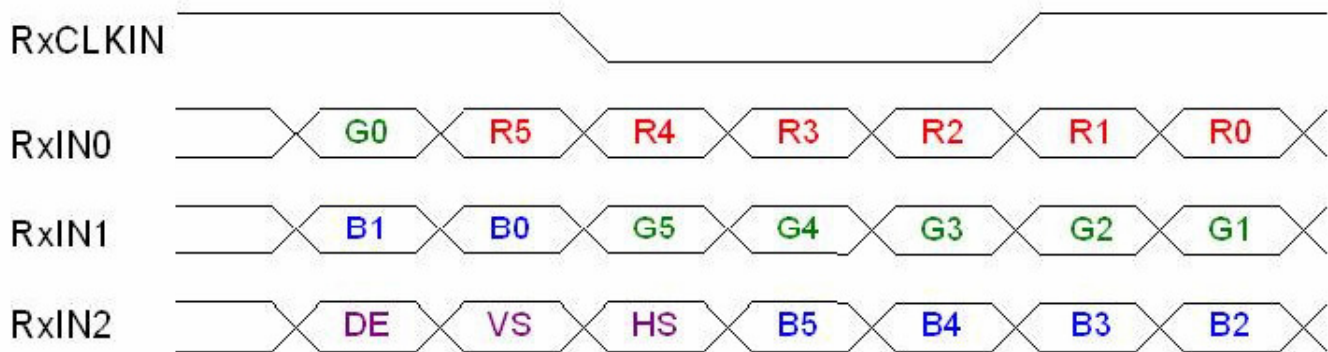
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
	Red-pixel Data	
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
	Green-pixel Data	
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
	Blue-pixel Data	
RxCLKIN	Data Clock	The typical frequency is 68.9 MHZ.. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Signal	Description
1	GND	Ground
2	Vcc	Power Supply (+3.3V)
3	Vanalog	Power Supply (+3.3V)
4	VEDID	DDC Power +3.3V
5	Vsync	Vsync
6	ClkEDID	DDC Clock
7	DATAEDID	DDC Data
8	Rin0-	Differential Data Input
9	Rin0+	Differential Data Input
10	GND	Ground
11	Rin1-	Differential Data Input
12	Rin1+	Differential Data Input
13	GND	Ground
14	Rin2-	Differential Data Input
15	Rin2+	Differential Data Input
16	GND	Ground
17	Clkin-	Differential Clock Input
18	Clkin+	Differential Clock Input
19	GND	Ground
20	NC	NC
21	Vdc	LED Anode (~31V)
22	Vdc	LED Anode (~31V)
23	NC	NC
24	Vdc1	LED Cathode (Ground)
25	Vdc2	LED Cathode (Ground)
26	Vdc3	LED Cathode (Ground)
27	Vdc4	LED Cathode (Ground)
28	Vdc5	LED Cathode (Ground)
29	Vdc6	LED Cathode (Ground)
30	AGING	AGING

6.4 Interface Timing

6.4.1 Timing Characteristics

Basically, interface timings should match the [1280x800 /60Hz](#) manufacturing guide line timing.

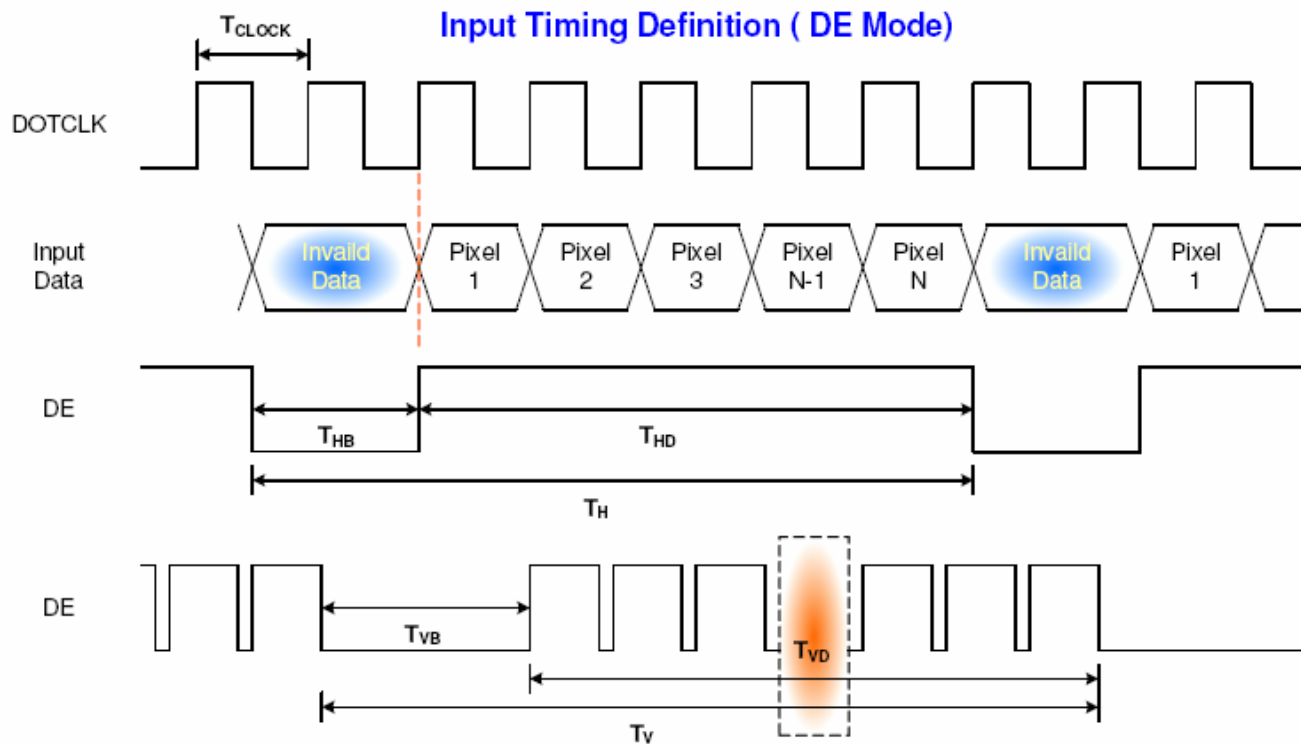
Signal	Parameter	Symbol	Min	Typ	Max	Unit	Note
D _{CLK}	Clock Period	T _C		13.79		ns	1
	Clock Frequency	f _C		72.50		MHz	1/T _C
	Duty Ratio (% High)	K _{dr}	40	50	60	%	T _{Ch} /T _C
	Rise Time	T _{R CLK}	-	4.42	-	ns	
	Fall Time	T _{F CLK}	-	4.42	-	ns	
DE (Data Enable Only) (DTMG) Data	DE Setup Time	T _{se}	4	-	-	ns	2 f _V =59.94 Hz, 3
	Data Setup Time	T _{sd}	4	-	-	ns	
	Data Hold Time	T _{hd}	2	-	-	ns	
	Horizontal Period	T _H		1440		T _C	
	Horizontal Blank Period	T _{ha}		160		T _C	
	Vertical Period	T _V		823		T _H	
	Vertical Blank Period	T _{wvb}		23		T _H	
H _{sync}	H _{sync} Back Porch	H _{bp}		80		T _C	Display Period
	H _{sync} Pulse Width	T _{WH}		32		T _C	
	H _{sync} Front Porch	H _{fp}		48		T _C	
	Horizontal Active Period	T _{HD}	1280	1280	1280	T _C	
V _{sync}	V _{sync} Back Porch	V _{bp}		14		T _H	Display Period
	V _{sync} Pulse Width	T _{WV}		6		T _H	
	V _{sync} Front Porch	V _{fp}		3		T _H	
	Vertical Active Period	T _{VD}	800	800	800	T _H	

Note: (1) When the WXGA+ controller sets DE Mode, and H_{sync} and V_{sync} are required. The duration of DE (DTMG) signal must be longer than 1 clock period (T_C) at every horizontal sync period;

(2) Horizontal Period = One Line Scanning Time;

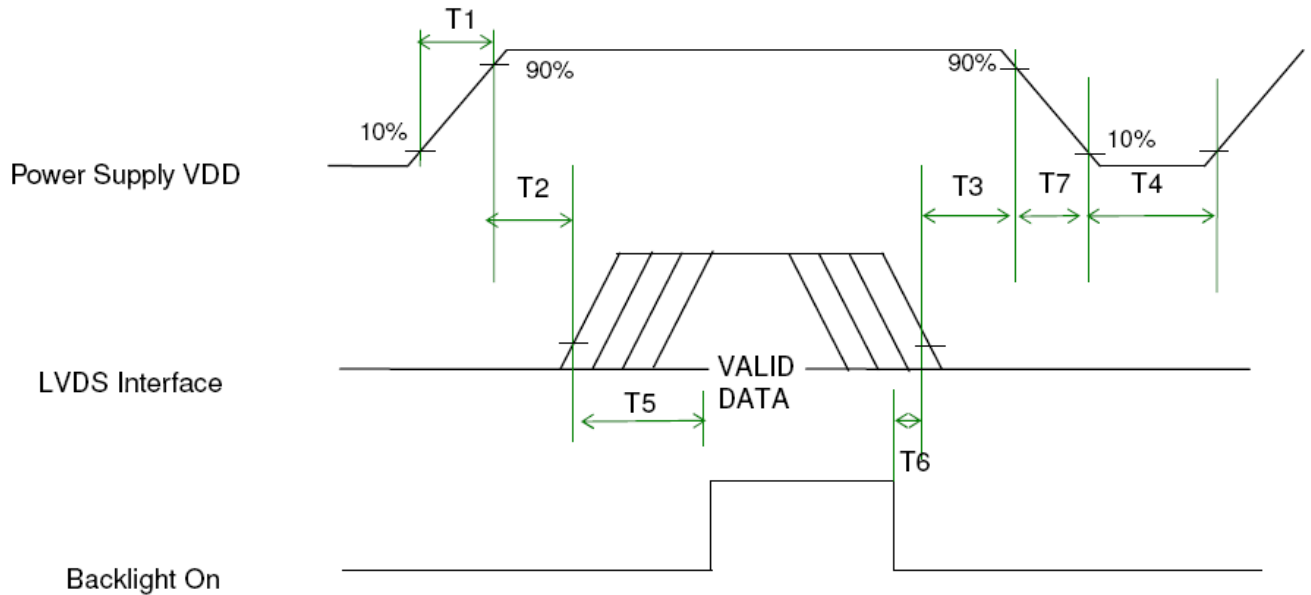
(3) The vertical period T_V is related to the frame frequency f_V, i.e., 60 Hz.

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)



7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	I-PEX
Type / Part Number	I-PEX 20474-030E-12
Mating Housing/Part Number	I-PEX 20472-030T-10



8. Dynamic Test

8.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 3.0 G
- Frequency: 5 - 150Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 200 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 50°C, 90%RH, 240h	
High Temperature Operation	Ta= 50°C, RH, 300h	
Low Temperature Operation	Ta= 0°C, RH, 300h	
High Temperature Storage	Ta= 65°C, RH, 500h	
Low Temperature Storage	Ta= -25°C, RH, 500h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

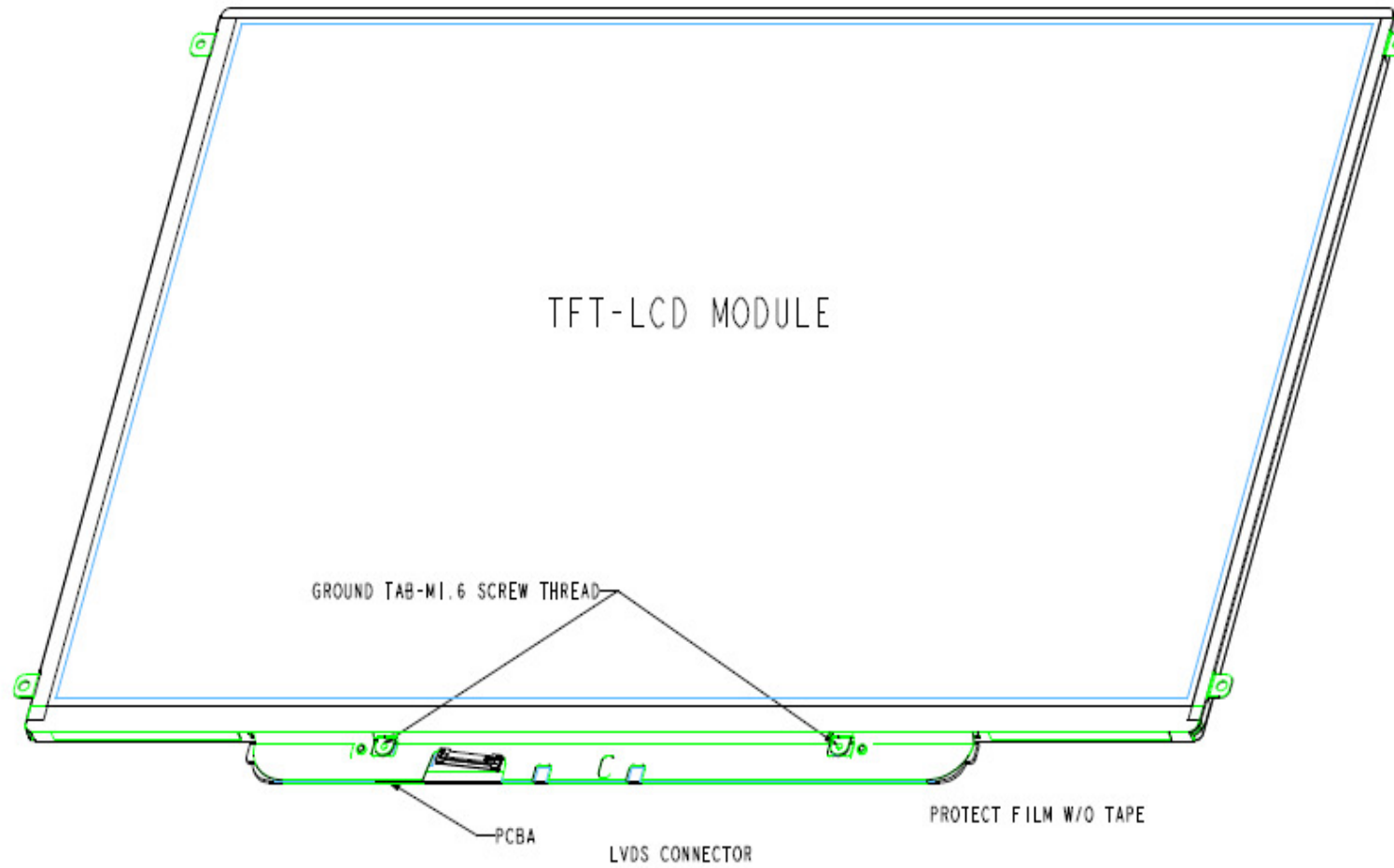
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

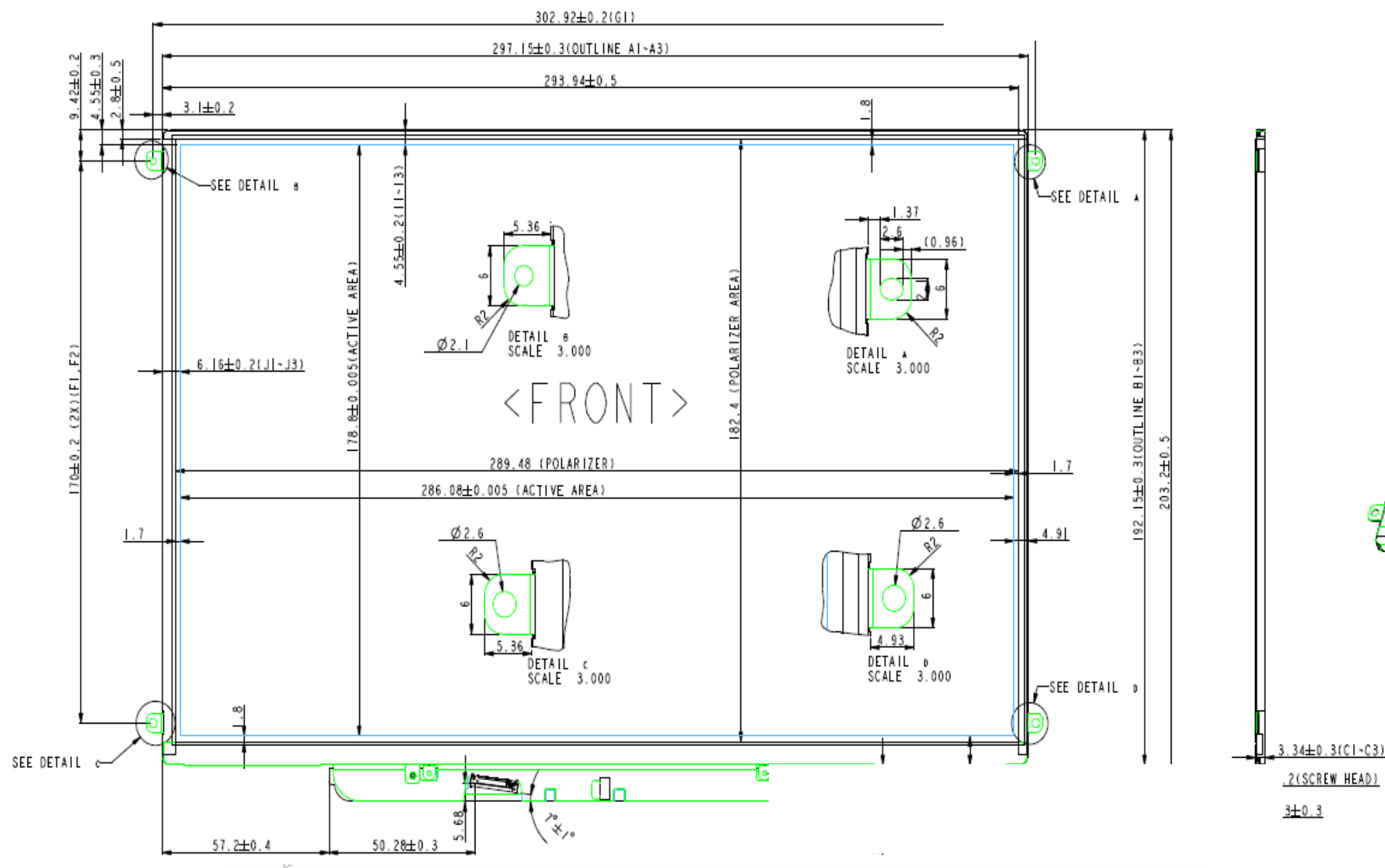
. Self-recoverable. No hardware failures.

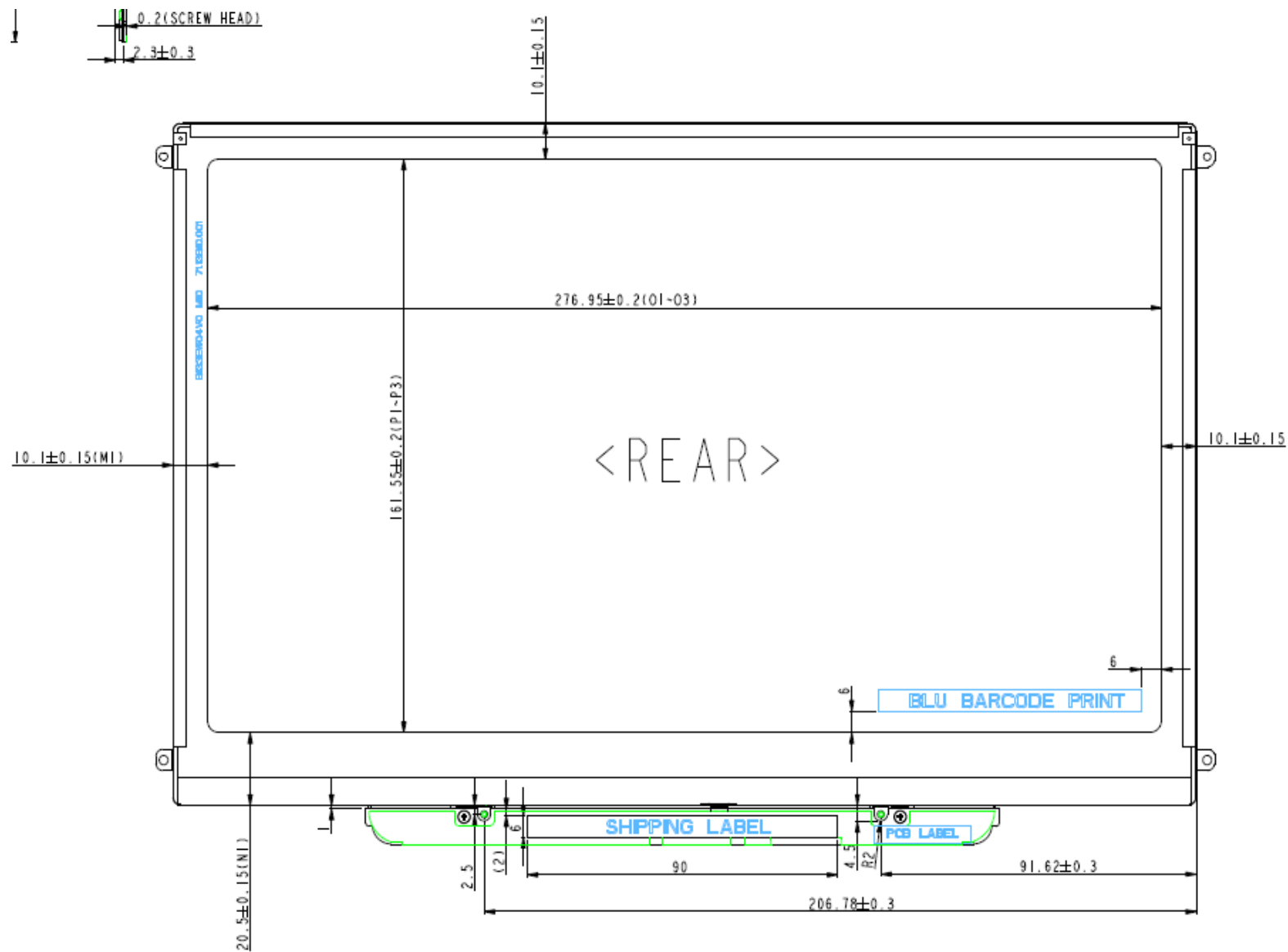
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

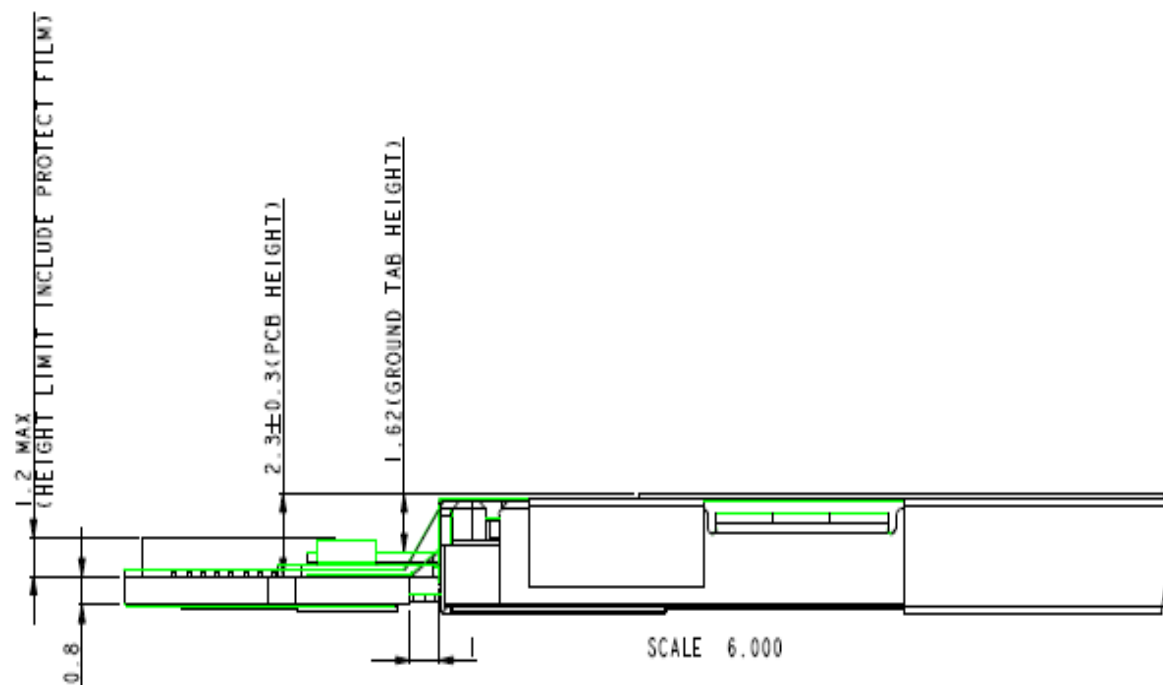
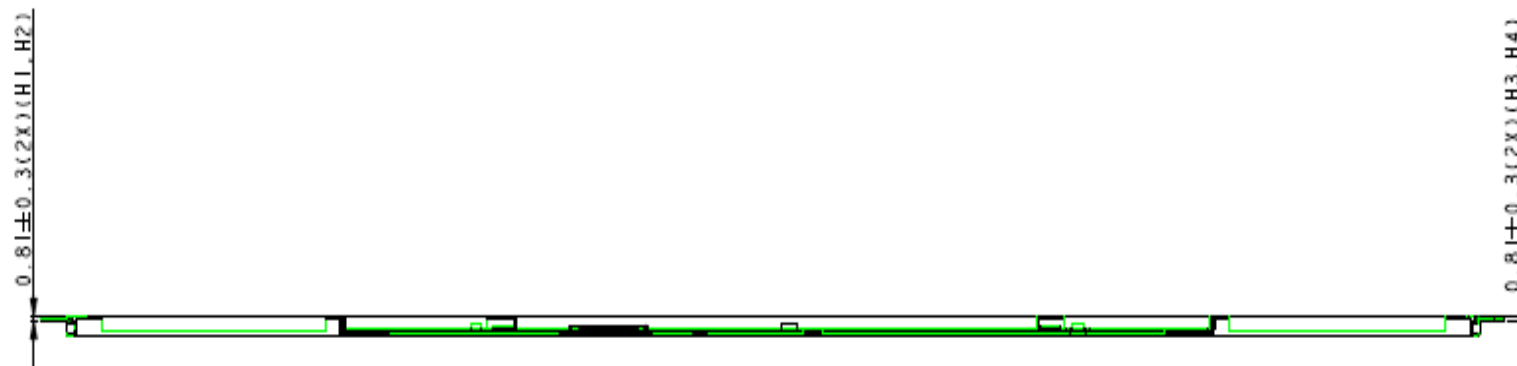
10. Mechanical Characteristics

10.1 LCM Outline Dimension









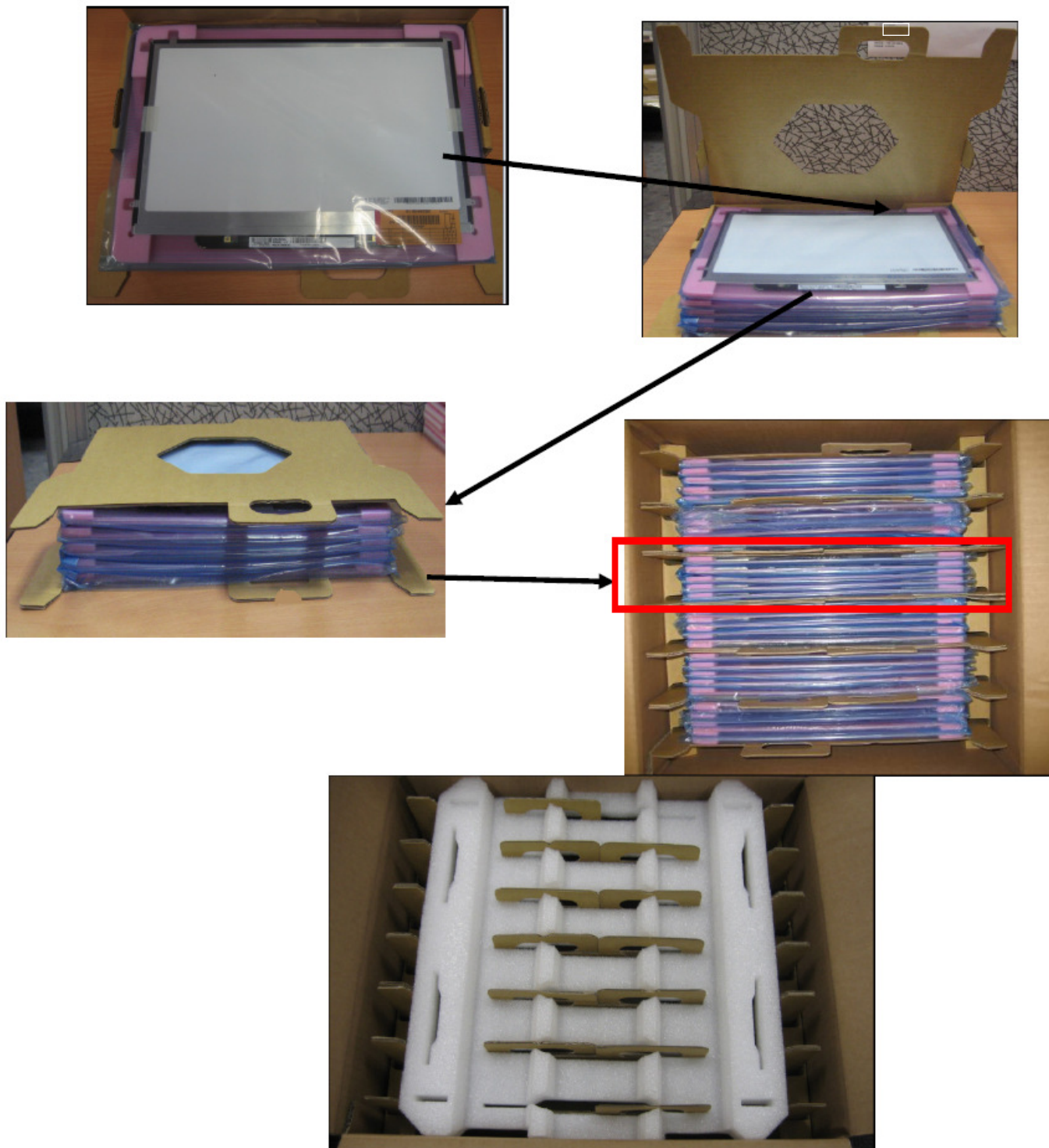
11. Shipping and Package
11.1 Shipping Label Format

11.1 Shipping Label Format

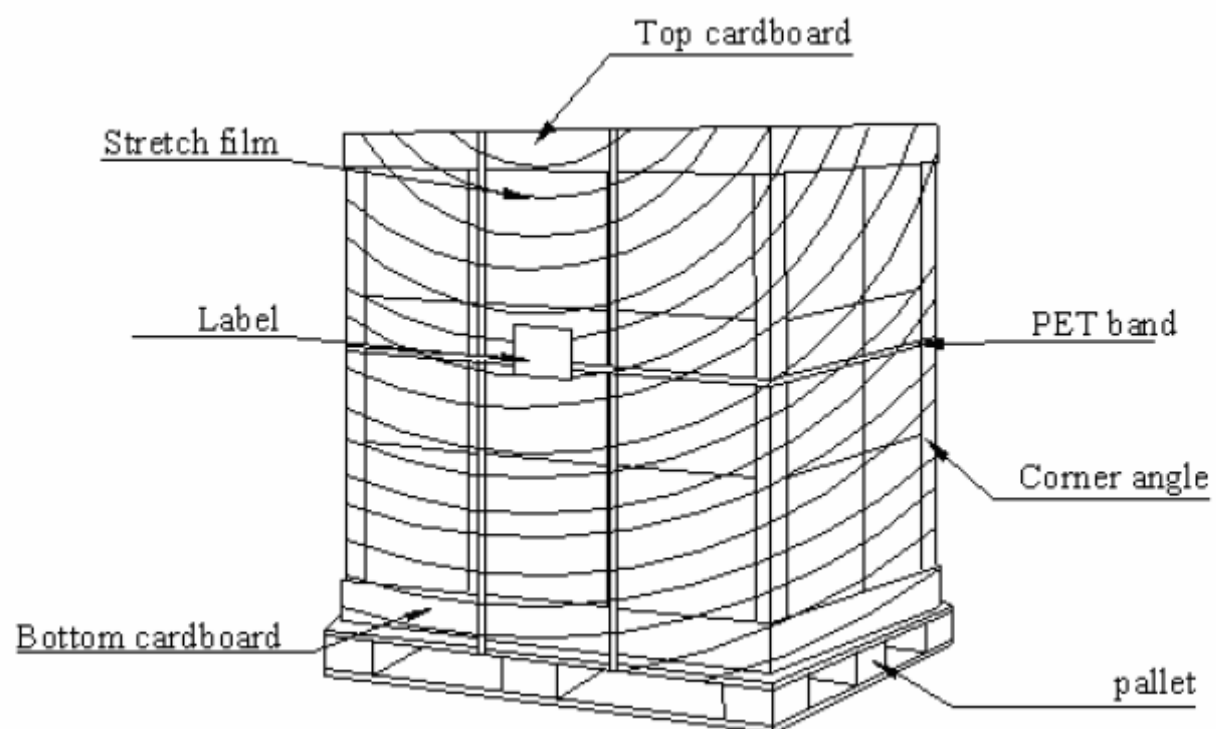


11.2 Carton package

The outside dimension of carton is 435 (L)mm x 377 (W)mm x 335 (H)mm



11.3 Shipping package of palletizing sequence



12. Appendix: EDID description

B133EW04 V0

Address	FUNCTION	B133EW04	Value	Value	Note
HEX	Header	HEX	BIN	DEC	
00		00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07	EISA Manuf. Code LSB Compressed ASCII Product Code hex, LSB first 32-bit ser # Week of manufacture Year of manufacture EDID Structure Ver. EDID revision # Video input definition Max H image size Max V image size Display Gamma Feature support	00	00000000	0	
08		06	00000110	6	
09		10	00010000	16	
0A		8C	10001100	140	
0B		9C	10011100	156	
0C		01	00000001	1	
0D		01	00000001	1	
0E		01	00000001	1	
0F		01	00000001	1	
10		05	00000101	5	
11		12	00010010	18	
12		01	00000001	1	
13		03	00000011	3	
14		80	10000000	128	
15		1D	00011101	29	
16		12	00010010	18	
17		78	01111000	120	
18		0A	00001010	10	
19	Red/green low bits	50	01010000	80	
1A	Blue/white low bits	85	10000101	133	
1B	Red x/ high bits	98	10011000	152	
1C	Red y	58	01011000	88	
1D	Green x	52	01010010	82	
1E	Green y	8E	10001110	142	
1F	Blue x	26	00100110	38	
20	Blue y	25	00100101	37	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Manufacturer's Timing	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	

28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10,000 (LSB)	52	01010010	82
37	Pixel Clock/10,000 (MSB)	1C	00011100	28
38	Horiz. Active pixels(Lower 8 bits)	00	00000000	0
39	Horiz.Blanking (Lower 8 bits)	A0	10100000	143
3A	Horiz. Active pixels:Horiz. Blanking (Upper4:4 bits)	50	01010000	80
3B		20	00100000	32
3C		17	00010111	46
3D	Vert. Active pixels:Vert. Blanking (Upper4:4 bits)	30	00110000	48
3E		30	00110000	48
3F		20	00100000	32
40	Vert. Sync. Offset=xx lines, Sync Width=xx lines	36	00110110	54
41	Horz. Ver. Sync/Width (upper 2 bits)	00	00000000	0
42	Hori. Image size (Lower 8 bits)	1E	00011110	30
43	Vert. Image size (Lower 8 bits)	B3	10110011	179
44	Hori. Image size : Vert. Image size (Upper 4 bits)	10	00010000	16
45		00	00000000	0
46		00	00000000	0
47		18	00011000	24
48	Detailed timing/monitor	00	00000000	0
49	descriptor #2	00	00000000	0
4A		00	00000000	0
4B		01	00000001	1
4C	Version	00	00000000	0
4D	Apple edid signature	06	00000110	6
4E	Apple edid signature	10	00010000	16
4F	Link Type (LVDS Link,MSB justified)	20	00100000	32
50	Pixel and link component format (6-bit panel interface)	00	00000000	0
51	Panel features (No inverter)	00	00000000	0

52	Detailed timing/monitor descriptor #3	00	00000000	0	ASCII Data String: B133EW04 V0
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		0A	00001010	10	
59		20	00100000	32	
5A		00	00000000	0	
5B		00	00000000	0	
5C		00	00000000	0	B 1 3 3 E W 0 4 V 3
5D		FE	11111110	254	
5E		00	00000000	0	
5F		42	01000010	66	
60		31	00110001	49	
61		33	00110011	51	
62		33	00110011	51	
63		45	01000101	69	
64		57	01010111	87	
65		30	00110000	48	
66	Detailed timing/monitor descriptor #4	34	00110100	52	Monitor Name: Color LCD
67		20	00100000	32	
68		56	01010110	86	
69		33	00110011	51	
6A		0A	00001010	10	
6B		20	00100000	32	
6C		00	00000000	0	
6D		00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	C o l o r L C D
71		43	01000011	67	
72		6F	01101111	111	
73		6C	01101100	108	
74		6F	01101111	111	
75		72	01110010	114	
76		20	00100000	32	
77		4C	01001100	76	
78		43	01000011	67	
79		44	01000100	68	
7A		0A	00001010	10	
7B		20	00100000	32	
7C		20	00100000	32	
7D		20	00100000	32	

7E	Extension Flag	00	00000000	0	
7F	Checksum	09	00001001	9	