CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A035VL01 V2**
CUSTOMER APPROVED	**Title :** **Name :**

- ☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.____)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver.____)**
- ☐ **CUSTOMER REMARK :**

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Product Specification
3.5" COLOR TFT-LCD MODULE

Model Name：	A035VL01 V2/ 04
Planned Lifetime:	From **2010/July** To **2011/Dec**
Phase-out Control:	From **2011/Nov** To **2011/Dec**
EOL Schedule:	**2011/Dec**

< □ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2010/07/06	-	First Draft

Contents

A. General Information

NO.	Item	Specification	Remark
1	Display resolution（dot）	800RGB(W) x 480(H)	
2	Active area（mm）	75.60 x 45.36	
3	Screen size（inch）	3.471 (Diagonal)	
4	Dot pitch（um）	31.5 X 94.5	
5	Color configuration	R, G, B stripe	
6	Overall dimension（mm）	86.1 x 51.66 x 2.42	Note 1
7	Weight（g）	23.5±10%	
8	Panel surface treatment	Glare type	

Note 1: Refer to F. Outline Dimension

B. Electrical Specifications

1. Pin Assignment For LCD

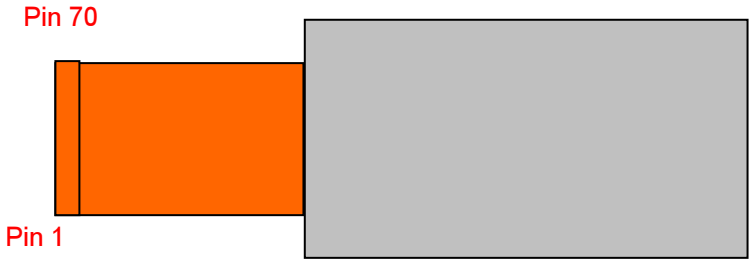
Pin no	Symbol	I/O	Description	Remark
1	VLED+	P	Backlight LED anode	
2	VLED-	P	Backlight LED cathode	
3	DR7	I	Red data Input (MSB)	
4	DR6	I	Red data input	
5	DR5	I	Red data input	
6	DR4	I	Red data input	
7	DR3	I	Red data input	
8	DR2	I	Red data input	
9	DR1	I	Red data input	
10	DR0	I	Red data input (LSB)	
11	DG7	I	Green data Input (MSB)	
12	DG6	I	Green data input	
13	DG5	I	Green data input	
14	DG4	I	Green data input	
15	DG3	I	Green data input	
16	DG2	I	Green data input	
17	DG1	I	Green data input	
18	DG0	I	Green data input (LSB)	
19	DB7	I	Blue data Input (MSB)	
20	DB6	I	Blue data input	
21	DB5	I	Blue data input	
22	DB4	I	Blue data input	
23	DB3	I	Blue data input	
24	DB2	I	Blue data input	
25	DB1	I	Blue data input	
26	DB0	I	Blue data input (LSB)	
27	SDA	I/O	Data input/output of SPI	
28	CS	I	Chip select (Low active) of SPI	
29	SCL	I	Clock input of SPI	
30	GND	P	Ground for digital circuit	
31	DCLK	I	Data clock Input	Note
32	GND	P	Ground for digital circuit	
33	DEN	I	Data enable Input (High active)	
34	HSYNC	I	Horizontal sync input	

35	VSYNC	I	Vertical sync input	
36	RESET	I	H/W reset pin. (Low active)	
37	VDDIO	P	Digital interface supply voltage of digital	
38	VCC	C	Intermediate voltage for charge pump	
39	VREF	C	Intermediate voltage for charge pump	
40	NGVDD	C	Intermediate voltage for charge pump	
41	GVDD	C	Intermediate voltage for charge pump	
42	VDD	P	Analog power supply voltage	
43	VCI1	C	Intermediate voltage for charge pump	
44	C11P	C	Pins to connect capacitance for power circuitry	
45	C11N	C	Pins to connect capacitance for power circuitry	
46	C12P	C	Pins to connect capacitance for power circuitry	
47	C12N	C	Pins to connect capacitance for power circuitry	
48	VDDA	C	Intermediate voltage for charge pump	
49	C41P	C	Pins to connect capacitance for power circuitry	
50	C41N	C	Pins to connect capacitance for power circuitry	
51	C42P	C	Pins to connect capacitance for power circuitry	
52	C42N	C	Pins to connect capacitance for power circuitry	
53	NVDDA	C	Intermediate voltage for charge pump	
54	C31N	C	Pins to connect capacitance for power circuitry	
55	C31P	C	Pins to connect capacitance for power circuitry	
56	C32N	C	Pins to connect capacitance for power circuitry	
57	C32P	C	Pins to connect capacitance for power circuitry	
58	VCL	C	Intermediate voltage for charge pump	
59	C21N	C	Pins to connect capacitance for power circuitry	
60	C21P	C	Pins to connect capacitance for power circuitry	
61	C22N	C	Pins to connect capacitance for power circuitry	
62	C22P	C	Pins to connect capacitance for power circuitry	
63	VGL	C	Pins to connect capacitance for power circuitry	
64	VGH	C	Pins to connect capacitance for power circuitry	
65	VCOMDC	C	Pins to connect capacitance for power circuitry	
66	VDD_TP	P	Voltage input pin for touch panel	
67	INT	O	Touched Interrupt Indicator	
68	SDA_TP	I	Data input pin of SPI mode for touch panel	
69	SCL_TP	I	Clock input pin of SPI mode for touch panel	
70	GND_TP	P	Ground of touch panel	

I：Input, O：Output, C：Capacitor, P：Power, D：Dummy

Note: DCLK signal can not be stopped when panel is operating or display off mode.

Definition of scanning direction, Refer to figure as below：



2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Supply Voltage	VDD	GND=0V	-0.3	4.2	V	
	VDDIO	GND=0V	-0.3	3.6	V	
Input Signal Voltage	CS,SDA,SCL,Vsync, Hsync,DCLK,D0~D7	GND=0V	-0.3	VDDIO+ 0.3	V	

3. Electrical characteristics

3.1 Recommended operating conditions (GND=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.1	3.3	3.5	V	
		VDDIO	1.65	3.3	3.6	V	
Input Signal voltage	H Level	V_{IH}	0.7* VDDIO	-	VDDIO	V	
	L Level	V_{IL}	GND	-	0.3* VDDIO	V	

3.2 Electrical characteristics (GND=0V)

Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
I_{VDD}	V_{VDD}=3.3V	-	17.5	25	mA	Note
I_{VDDTP}	V_{VDDTP}=3.3V	-	3.5	5	mA	Note
I_{VDDIO}	V_{VDDIO}=3.3V		2.2	3	mA	Note
I_{VDDIO}	V_{VDDIO}=2.0V		2.2	3	mA	Note
I_{VDDIO}	V_{VDDIO}=1.8V		2.0	3	mA	Note

Note 1: Test Condition: 8colorbar+Grayscale pattern, Frame rate: 60Hz, other registers are default setting.

3.3 Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.[Note1]	Unit	Remark
Backlight Current			25	27.5	mA	**Note2**
Backlight voltage	V_L	15	16.5	17.5	V	

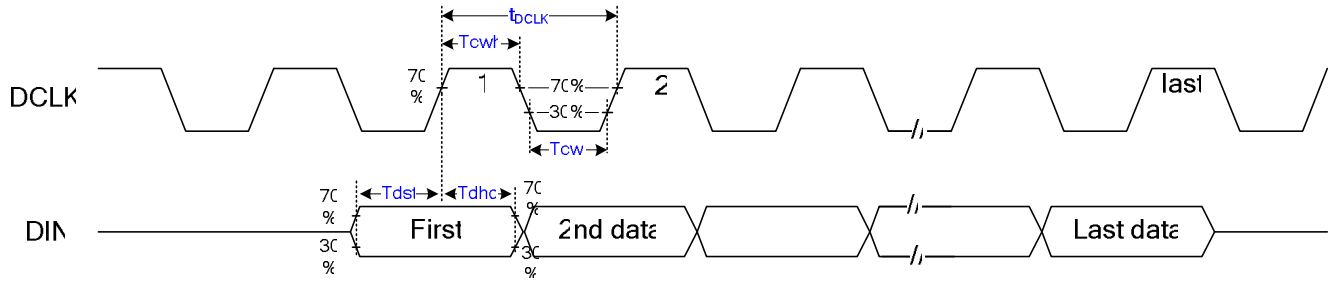
Note1: To consider LED driver and feedback resistor tolerance.
Note2: If using LCD internal LED driver controller the maximum setting should be typical value. Constant current design only. Ta=25℃

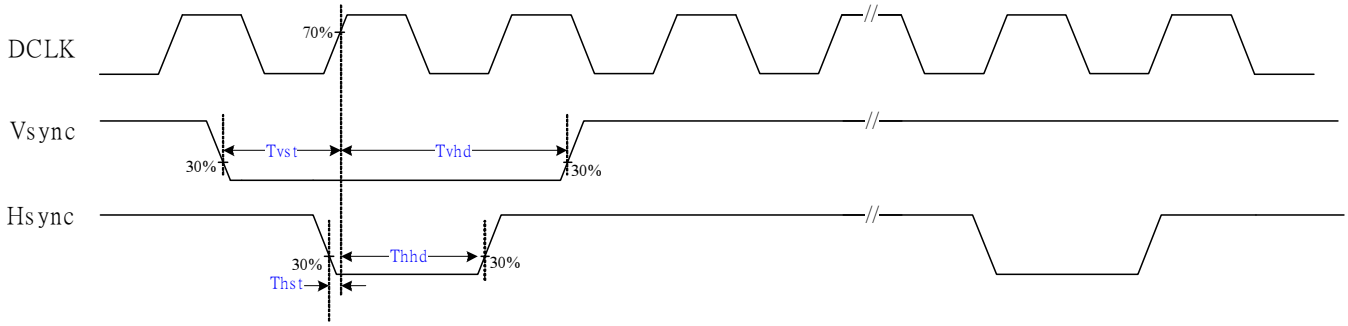
4. Input timing AC characteristic

(VDD=3.0 ~3.6V, AGND=GND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK duty cycle	Tcw	40	50	60	%	
VSYNC setup time	Tvst	15	-	-	ns	
VSYNC hold time	Tvhd	15	-	-	ns	

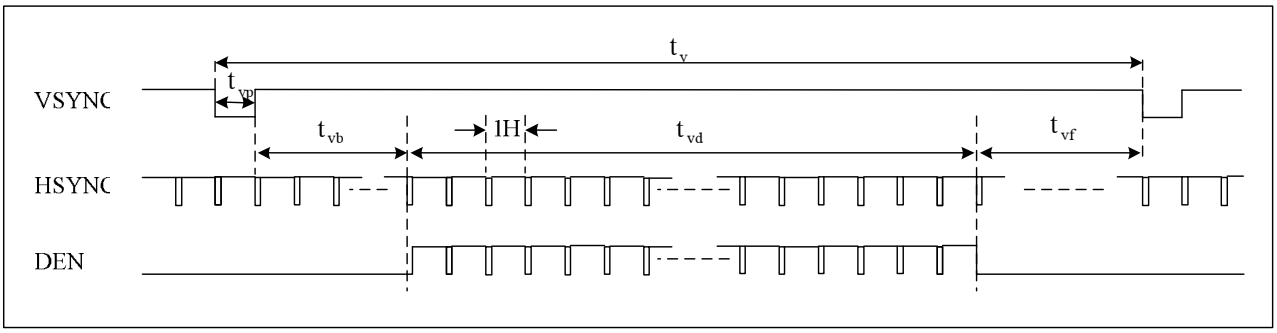
HSYNC setup time	Thst	15	-	-	ns	
HSYNC hold time	Thhd	15	-	-	ns	
Data setup time	Tdst	15	-	-	ns	
Data hold time	Tdhd	15	-	-	ns	



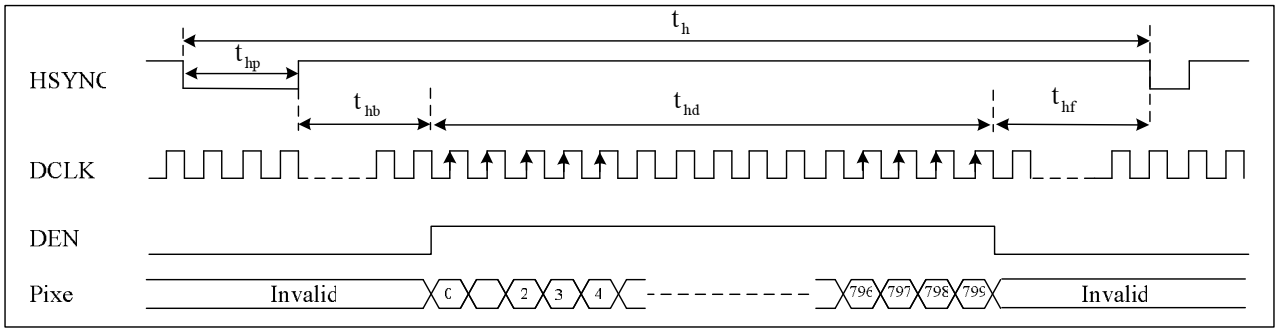


5. Input timing format

5.1 Vertical timing



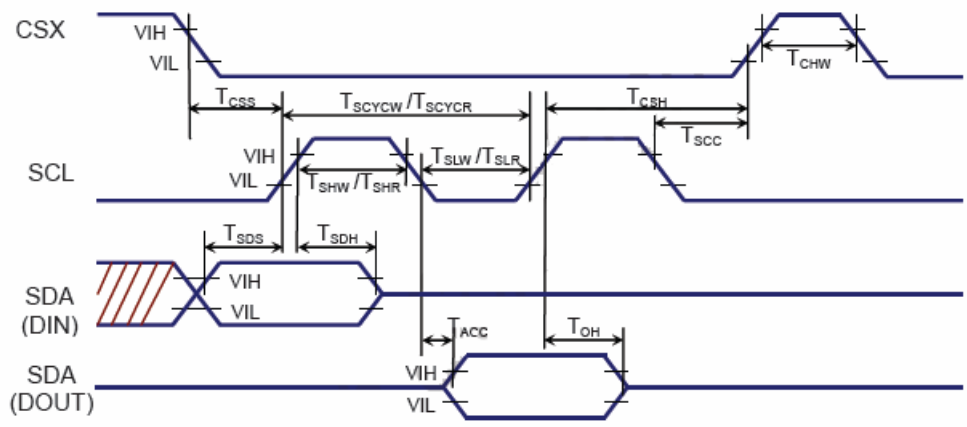
5.2 Horizontal timing



5.3 Timing parameters

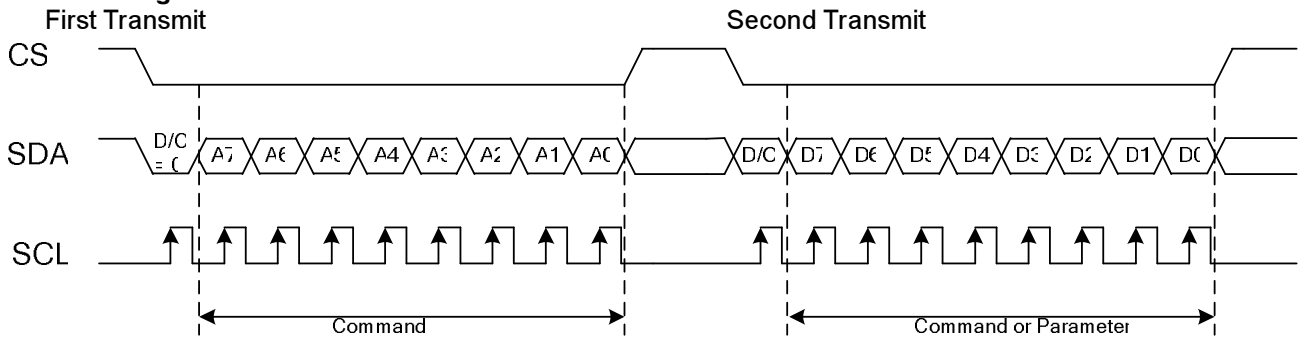
PARAMETER	Symbol	Min	Typ	Max	Unit
Clock cycle	$1/t_{CLK}$	20	27	30	MHz
Hsync cycle	$1/t_{fh}$	24.2	29.3	31.3	KHz
Vsync cycle	$1/t_{fv}$	50	60	65	Hz
Horizontal Signal					
Horizontal cycle	t_h	824	920	956	CLK
Horizontal display period	t_{hd}	-	800	-	CLK
Horizontal front porch	t_{hf}	2	50	52	CLK
Horizontal pulse width	t_{hp}	2	20	52	CLK
Horizontal back porch	t_{hb}	2	50	52	CLK
Vertical Signal					
Vertical cycle	t_v	486	488	492	H
Vertical display period	t_{vd}	-	480	-	H
Vertical front porch	t_{vf}	2	3	4	H
Vertical pulse width	t_{vp}	2	2	4	H
Vertical back porch	t_{vb}	2	3	4	H

6. Serial control interface AC characteristic



Item	Symbol	Min	Typical	Max	Unit
CS input setup Time	T_{CSS}	60	-	-	ns
CS input hold Time	T_{SCC}	60	-	-	ns
CS pulse high width	T_{CHW}	40	-	-	ns
Serial data input setup Time	T_{SDS}	10	-	-	ns
Serial data input hold Time	T_{SDH}	10	-	-	ns
Serial data output disable Time	T_{OH}	15	-	-	ns
Serial clock cycle(Write)	T_{SCYCW}	66	-	-	ns
SCL pulse low width(Write)	T_{SLW}	20	-	-	ns
SCL pulse high width(Write)	T_{SHW}	20	-	-	ns
Serial clock cycle(Read)	T_{SCYCR}	150	-	-	ns
SCL pulse low width(Read)	T_{SLR}	60	-	-	ns
SCL pulse high width(Read)	T_{SHR}	60	-	-	ns

6.1 Timing chart



6.2 Register table

Register	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Function
01h	0	0	0	0	0	0	0	0	1	Software reset
10h	0	0	0	0	1	0	0	0	0	Sleep in & booster off
11h	0	0	0	0	1	0	0	0	1	Sleep out & booster on
28h	0	0	0	1	0	1	0	0	0	Display off
29h	0	0	0	1	0	1	0	0	1	Display on
36h	0	0	0	1	1	0	1	1	0	Scan Direction
B1h	0	1	0	1	1	0	0	0	1	HV/DE mode selection

C5h	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**VCOM setting**
C6h	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**0**	**GVDD/GVSS setting**
C7h	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**1**	**NGVDD/NGVSS setting**
E0h	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**Positive polarity gamma setting**
E1h	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**Negative polarity gamma setting**

Register	**01h (Software reset)**
Description	**When the software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs ar set to VSS(display off).** **Note: The frame memory contents are not affected by this command.**
Restriction	**It will be necessary to wait 10 msec before sending new command following software reset.**

Register	**10h (Sleep in)**
Description	**This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC conveter is stopped, internal display oscillator is stopped, and panel scanning is stopped.** **Note: The memory keeps its contents.**
Restriction	**It will be necessary to wait 5 msec before sending next command, this is to allow time for the supply voltage and clock circuits to stabilize.**

Register	**11h (Sleep out)**
Description	**This command turns off sleep mode.** **In this mode the DC/DC conveter is enabled, internal display oscillator is started, and panel scanning is started.**
Restriction	**It will be necessary to wait 120 msec before sending next command, this is to allow time for the supply voltage and clock circuits to stabilize.**

Register	**28h (Display off)**
Description	**This command is used to enter into DISPLAY OFF mode.** **In this mode, the output from Frame memory is disabled and blank page inserted.**
Restriction	**-**

Register	**29h (Display on)**
Description	**This command is used to recover from DISPLAY OFF mode.** **Output from Frame memory is enabled.**
Restriction	**-**

36H	**Scan Direction**									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	1	1	0	1	1	0	36
1st Parameter	1	MY	MX	0	0	0	0	0	0	00h

Description	Set the scan direction of LCD. MY = '0': Scan direction is from top to bottom, MY = '1': Scan direction is from bottom to top. MX = '0': Scan direction is from left to right, MX = '1': Scan direction is from right to left.
Default	Default value is {0000 0000}

B1H	**HV/DE Mode Setting**									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	0	0	1	B1
1st Parameter	1	0	0	0	0	0	1	HV/DE	0	04h
2nd Parameter	1	HBlanking								00h

3rd Parameter	1	VBlanking	00h

Description

HV/DE: HV/DE mode setting.

HV/DE	Description
0	DE mode is selected. DE signal is needs input externally. HBlanking and VBlanking parameters are ineffective.
1	HV mode is selected. DE signal doesn't need input. Blanking settings are controlled by HBlanking/VBlanking parameters.

HBlanking[7:0]: horizontal blanking setting. HBlanking should be set as value of t_{hp} add t_{hb}.
Ex: t_{hp} = 20(decimal), t_{hb} = 50(decimal).
HBlanking = 20 + 50 = 70(decimal) = "0100 0110"(binary)

VBlanking[7:0]: vertical blanking setting. VBlanking should be set as value of t_{vp} add t_{vb}.
Ex: t_{vp} = 2 (decimal), t_{vb} = 3(decimal).
VBlanking = 2 + 3 = 5(decimal) = "0000 0101"(binary)

C5H	VCOMDC(VCOM Setting)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	1	0	1	C5
1st Parameter	1	NVM2	VCOMD CGND	-	-	-	-	-	-	00h
2nd Parameter	1	COMDC7	COMDC6	COMDC5	COMDC4	COMDC3	COMDC2	COMDC1	COMDC0	

NOTE: "-" Don't care

Description	NVM2=0, VCOMDC setting is from NVM, NVM2=1, VCOMDC setting is from register
Restriction	
Register Availability	
Default	Default value is {0101 1101}
Flow Chart	-

COMDC[7:0]	VCOMDC(V)	COMDC[7:0]	VCOMDC(V)	COMDC[7:0]	VCOMDC(V)	COMDC[7:0]	VCOMDC(V)
FFh	1.905	BFh	0.945	7Fh	0.000	3Fh	-0.960
FEh	1.890	BEh	0.930	7Eh	-0.015	3Eh	-0.975
FDh	1.875	BDh	0.915	7Dh	-0.030	3Dh	-0.990
FCh	1.860	BCh	0.900	7Ch	-0.045	3Ch	-1.005
FBh	1.845	BBh	0.885	7Bh	-0.060	3Bh	-1.020
FAh	1.830	BAh	0.870	7Ah	-0.075	3Ah	-1.035
F9h	1.815	B9h	0.855	79h	-0.090	39h	-1.050
F8h	1.800	B8h	0.840	78h	-0.105	38h	-1.065
F7h	1.785	B7h	0.825	77h	-0.120	37h	-1.080
F6h	1.770	B6h	0.810	76h	-0.135	36h	-1.095
F5h	1.755	B5h	0.795	75h	-0.150	35h	-1.110
F4h	1.740	B4h	0.780	74h	-0.165	34h	-1.125
F3h	1.725	B3h	0.765	73h	-0.180	33h	-1.140
F2h	1.710	B2h	0.750	72h	-0.195	32h	-1.155
F1h	1.695	B1h	0.735	71h	-0.210	31h	-1.170

F0h	1.680	B0h	0.720	70h	-0.225	30h	-1.185
EFh	1.665	AFh	0.705	6Fh	-0.240	2Fh	-1.200
EEh	1.650	AEh	0.690	6Eh	-0.255	2Eh	-1.215
EDh	1.635	ADh	0.675	6Dh	-0.270	2Dh	-1.230
ECh	1.620	ACh	0.660	6Ch	-0.285	2Ch	-1.245
EBh	1.605	ABh	0.645	6Bh	-0.300	2Bh	-1.260
EAh	1.590	AAh	0.630	6Ah	-0.315	2Ah	-1.275
E9h	1.575	A9h	0.615	69h	-0.330	29h	-1.290
E8h	1.560	A8h	0.600	68h	-0.345	28h	-1.305
E7h	1.545	A7h	0.585	67h	-0.360	27h	-1.320
E6h	1.530	A6h	0.570	66h	-0.375	26h	-1.335
E5h	1.515	A5h	0.555	65h	-0.390	25h	-1.350
E4h	1.500	A4h	0.540	64h	-0.405	24h	-1.365
E3h	1.485	A3h	0.525	63h	-0.420	23h	-1.380
E2h	1.470	A2h	0.510	62h	-0.435	22h	-1.395
E1h	1.455	A1h	0.495	61h	-0.450	21h	-1.410
E0h	1.440	A0h	0.480	60h	-0.465	20h	-1.425
DFh	1.425	9Fh	0.465	5Fh	-0.480	1Fh	-1.440
DEh	1.410	9Eh	0.450	5Eh	-0.495	1Eh	-1.455
DDh	1.395	9Dh	0.435	5Dh	-0.510	1Dh	-1.470
DCh	1.380	9Ch	0.420	5Ch	-0.525	1Ch	-1.485
DBh	1.365	9Bh	0.405	5Bh	-0.540	1Bh	-1.500
DAh	1.350	9Ah	0.390	5Ah	-0.555	1Ah	-1.515
D9h	1.335	99h	0.375	59h	-0.570	19h	-1.530
D8h	1.320	98h	0.360	58h	-0.585	18h	-1.545
D7h	1.305	97h	0.345	57h	-0.600	17h	-1.560
D6h	1.290	96h	0.330	56h	-0.615	16h	-1.575
D5h	1.275	95h	0.315	55h	-0.630	15h	-1.590
D4h	1.260	94h	0.300	54h	-0.645	14h	-1.605
D3h	1.245	93h	0.285	53h	-0.660	13h	-1.620
D2h	1.230	92h	0.270	52h	-0.675	12h	-1.635
D1h	1.215	91h	0.255	51h	-0.690	11h	-1.650
D0h	1.200	90h	0.240	50h	-0.705	10h	-1.665
CFh	1.185	8Fh	0.225	4Fh	-0.720	0Fh	-1.680
CEh	1.170	8Eh	0.210	4Eh	-0.735	0Eh	-1.695
CDh	1.155	8Dh	0.195	4Dh	-0.750	0Dh	-1.710
CCh	1.140	8Ch	0.180	4Ch	-0.765	0Ch	-1.725
CBh	1.125	8Bh	0.165	4Bh	-0.780	0Bh	-1.740
CAh	1.110	8Ah	0.150	4Ah	-0.795	0Ah	-1.755
C9h	1.095	89h	0.135	49h	-0.810	09h	-1.770
C8h	1.080	88h	0.120	48h	-0.825	08h	-1.785
C7h	1.065	87h	0.105	47h	-0.840	07h	-1.800
C6h	1.050	86h	0.090	46h	-0.855	06h	-1.815
C5h	1.035	85h	0.075	45h	-0.870	05h	-1.830
C4h	1.020	84h	0.060	44h	-0.885	04h	-1.845
C3h	1.005	83h	0.045	43h	-0.900	03h	-1.860
C2h	0.990	82h	0.030	42h	-0.915	02h	-1.875
C1h	0.975	81h	0.015	41h	-0.930	01h	-1.890
C0h	0.960	80h	0.000	40h	-0.945	00h	-1.905

C6H	GVDD/GVSS(GVDD/GVSS Setting)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	1	1	0	C6
1st Parameter	1	GVDD7	GVDD6	GVDD5	GVDD4	GVDD3	GVDD2	GVDD1	GVDD0	
2nd Parameter	1	NVM4	-	GVSS5	GVSS4	GVSS3	GVSS2	GVSS1	GVSS0	

NOTE: "-" Don't care

Description	NVM4=0, GVDD setting is from NVM, NVM4=1, GVDD setting is from register
Restriction	
Register Availability	
Default	GVDD default value is {1010 1011} ; GVSS default value is {0000 0100}
Flow Chart	-

- GVDD voltage setting

GVDD[7:0]	GVDD(V)	GVDD[7:0]	GVDD(V)	GVDD[7:0]	GVDD(V)	GVDD[7:0]	GVDD(V)
FFh	6	BFh	5.04	7Fh	4.08	3Fh	3.12
FEh	5.985	BEh	5.025	7Eh	4.065	3Eh	3.105
FDh	5.97	BDh	5.01	7Dh	4.05	3Dh	3.09
FCh	5.955	BCh	4.995	7Ch	4.035	3Ch	3.075
FBh	5.94	BBh	4.98	7Bh	4.02	3Bh	3.06
FAh	5.925	BAh	4.965	7Ah	4.005	3Ah	3.045
F9h	5.91	B9h	4.95	79h	3.99	39h	3.03
F8h	5.895	B8h	4.935	78h	3.975	38h	3.015
F7h	5.88	B7h	4.92	77h	3.96	37h	3
F6h	5.865	B6h	4.905	76h	3.945	36h	2.985
F5h	5.85	B5h	4.89	75h	3.93	35h	2.97
F4h	5.835	B4h	4.875	74h	3.915	34h	2.955
F3h	5.82	B3h	4.86	73h	3.9	33h	2.94
F2h	5.805	B2h	4.845	72h	3.885	32h	2.925
F1h	5.79	B1h	4.83	71h	3.87	31h	2.91
F0h	5.775	B0h	4.815	70h	3.855	30h	2.895
EFh	5.76	AFh	4.8	6Fh	3.84	2Fh	2.88
EEh	5.745	AEh	4.785	6Eh	3.825	2Eh	2.865
EDh	5.73	ADh	4.77	6Dh	3.81	2Dh	2.85
ECh	5.715	ACh	4.755	6Ch	3.795	2Ch	2.835
EBh	5.7	ABh	4.74	6Bh	3.78	2Bh	2.82
EAh	5.685	AAh	4.725	6Ah	3.765	2Ah	2.805
E9h	5.67	A9h	4.71	69h	3.75	29h	2.79
E8h	5.655	A8h	4.695	68h	3.735	28h	2.775
E7h	5.64	A7h	4.68	67h	3.72	27h	2.76
E6h	5.625	A6h	4.665	66h	3.705	26h	2.745
E5h	5.61	A5h	4.65	65h	3.69	25h	2.73
E4h	5.595	A4h	4.635	64h	3.675	24h	2.715
E3h	5.58	A3h	4.62	63h	3.66	23h	2.7
E2h	5.565	A2h	4.605	62h	3.645	22h	2.685
E1h	5.55	A1h	4.59	61h	3.63	21h	2.67
E0h	5.535	A0h	4.575	60h	3.615	20h	2.655
DFh	5.52	9Fh	4.560	5Fh	3.600	1Fh	2.655
DEh	5.505	9Eh	4.545	5Eh	3.585	1Eh	2.655
DDh	5.49	9Dh	4.530	5Dh	3.570	1Dh	2.655
DCh	5.475	9Ch	4.515	5Ch	3.555	1Ch	2.655

DBh	5.46	9Bh	4.500	5Bh	3.540	1Bh	2.655
DAh	5.445	9Ah	4.485	5Ah	3.525	1Ah	2.655
D9h	5.43	99h	4.470	59h	3.510	19h	2.655
D8h	5.415	98h	4.455	58h	3.495	18h	2.655
D7h	5.4	97h	4.440	57h	3.480	17h	2.655
D6h	5.385	96h	4.425	56h	3.465	16h	2.655
D5h	5.37	95h	4.410	55h	3.450	15h	2.655
D4h	5.355	94h	4.395	54h	3.435	14h	2.655
D3h	5.34	93h	4.380	53h	3.420	13h	2.655
D2h	5.325	92h	4.365	52h	3.405	12h	2.655
D1h	5.31	91h	4.350	51h	3.390	11h	2.655
D0h	5.295	90h	4.335	50h	3.375	10h	2.655
CFh	5.28	8Fh	4.320	4Fh	3.360	0Fh	2.655
CEh	5.265	8Eh	4.305	4Eh	3.345	0Eh	2.655
CDh	5.25	8Dh	4.290	4Dh	3.330	0Dh	2.655
CCh	5.235	8Ch	4.275	4Ch	3.315	0Ch	2.655
CBh	5.22	8Bh	4.260	4Bh	3.300	0Bh	2.655
CAh	5.205	8Ah	4.245	4Ah	3.285	0Ah	2.655
C9h	5.19	89h	4.230	49h	3.270	09h	2.655
C8h	5.175	88h	4.215	48h	3.255	08h	2.655
C7h	5.16	87h	4.200	47h	3.240	07h	2.655
C6h	5.145	86h	4.185	46h	3.225	06h	2.655
C5h	5.13	85h	4.170	45h	3.210	05h	2.655
C4h	5.115	84h	4.155	44h	3.195	04h	2.655
C3h	5.1	83h	4.140	43h	3.180	03h	2.655
C2h	5.085	82h	4.125	42h	3.165	02h	2.655
C1h	5.07	81h	4.110	41h	3.150	01h	2.655
C0h	5.055	80h	4.095	40h	3.135	00h	2.655

- GVSS voltage setting

GVSS[5:0]	GVSS (V)	GVSS[5:0]	GVSS (V)
3Fh	1.05	1Fh	0.57
3Eh	1.035	1Eh	0.555
3Dh	1.02	1Dh	0.54
3Ch	1.005	1Ch	0.525
3Bh	0.99	1Bh	0.51
3Ah	0.975	1Ah	0.495
39h	0.96	19h	0.48
38h	0.945	18h	0.465
37h	0.93	17h	0.45
36h	0.915	16h	0.435
35h	0.9	15h	0.42
34h	0.885	14h	0.405
33h	0.87	13h	0.39
32h	0.855	12h	0.375
31h	0.84	11h	0.36
30h	0.825	10h	0.345
2Fh	0.81	0Fh	0.33
2Eh	0.795	0Eh	0.315
2Dh	0.78	0Dh	0.3
2Ch	0.765	0Ch	0.285
2Bh	0.75	0Bh	0.27
2Ah	0.735	0Ah	0.255
29h	0.72	09h	0.24

28h	0.705	08h	0.225
27h	0.69	07h	0.21
26h	0.675	06h	0.195
25h	0.66	05h	0.18
24h	0.645	04h	0.165
23h	0.63	03h	0.15
22h	0.615	02h	0.135
21h	0.6	01h	0.12
20h	0.585	00h	0.105

C7H	NGVDD/NGVSS(NGVDD/NGVSS Setting)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	1	1	1	C7
1st Parameter	1	NGVDD7	NGVDD6	NGVDD5	NGVDD4	NGVDD3	NGVDD2	NGVDD1	NGVDD0	
2nd Parameter	1	NVM5	-	NGVSS5	NGVSS4	NGVSS3	NGVSS2	NGVSS1	NGVSS0	

NOTE: "-" Don't care

Description	NVM5=0, NGVDD setting is from NVM, NVM5=1, NGVDD setting is from register
Restriction	
Register Availability	
Default	NGVDD default value is {1010 1011} ; NGVSS default value is {0000 0100}
Flow Chart	-

- NGVDD voltage setting

NGVDD[7:0]	NGVDD(V)	NGVDD[7:0]	NGVDD(V)	NGVDD[7:0]	NGVDD(V)	NGVDD[7:0]	NGVDD(V)
FFh	-6	BFh	-5.04	7Fh	-4.08	3Fh	-3.12
FEh	-5.985	BEh	-5.025	7Eh	-4.065	3Eh	-3.105
FDh	-5.97	BDh	-5.01	7Dh	-4.05	3Dh	-3.09
FCh	-5.955	BCh	-4.995	7Ch	-4.035	3Ch	-3.075
FBh	-5.94	BBh	-4.98	7Bh	-4.02	3Bh	-3.06
FAh	-5.925	BAh	-4.965	7Ah	-4.005	3Ah	-3.045
F9h	-5.91	B9h	-4.95	79h	-3.99	39h	-3.03
F8h	-5.895	B8h	-4.935	78h	-3.975	38h	-3.015
F7h	-5.88	B7h	-4.92	77h	-3.96	37h	-3
F6h	-5.865	B6h	-4.905	76h	-3.945	36h	-2.985
F5h	-5.85	B5h	-4.89	75h	-3.93	35h	-2.97
F4h	-5.835	B4h	-4.875	74h	-3.915	34h	-2.955
F3h	-5.82	B3h	-4.86	73h	-3.9	33h	-2.94
F2h	-5.805	B2h	-4.845	72h	-3.885	32h	-2.925
F1h	-5.79	B1h	-4.83	71h	-3.87	31h	-2.91
F0h	-5.775	B0h	-4.815	70h	-3.855	30h	-2.895
EFh	-5.76	AFh	-4.8	6Fh	-3.84	2Fh	-2.88
EEh	-5.745	AEh	-4.785	6Eh	-3.825	2Eh	-2.865
EDh	-5.73	ADh	-4.77	6Dh	-3.81	2Dh	-2.85
ECh	-5.715	ACh	-4.755	6Ch	-3.795	2Ch	-2.835
EBh	-5.7	ABh	-4.74	6Bh	-3.78	2Bh	-2.82
EAh	-5.685	AAh	-4.725	6Ah	-3.765	2Ah	-2.805
E9h	-5.67	A9h	-4.71	69h	-3.75	29h	-2.79
E8h	-5.655	A8h	-4.695	68h	-3.735	28h	-2.775
E7h	-5.64	A7h	-4.68	67h	-3.72	27h	-2.76
E6h	-5.625	A6h	-4.665	66h	-3.705	26h	-2.745

E5h	-5.61	A5h	-4.65	65h	-3.69	25h	-2.73
E4h	-5.595	A4h	-4.635	64h	-3.675	24h	-2.715
E3h	-5.58	A3h	-4.62	63h	-3.66	23h	-2.7
E2h	-5.565	A2h	-4.605	62h	-3.645	22h	-2.685
E1h	-5.55	A1h	-4.59	61h	-3.63	21h	-2.67
E0h	-5.535	A0h	-4.575	60h	-3.615	20h	-2.655
DFh	-5.52	9Fh	-4.56	5Fh	-3.6	1Fh	-2.655
DEh	-5.505	9Eh	-4.545	5Eh	-3.585	1Eh	-2.655
DDh	-5.49	9Dh	-4.53	5Dh	-3.57	1Dh	-2.655
DCh	-5.475	9Ch	-4.515	5Ch	-3.555	1Ch	-2.655
DBh	-5.46	9Bh	-4.5	5Bh	-3.54	1Bh	-2.655
DAh	-5.445	9Ah	-4.485	5Ah	-3.525	1Ah	-2.655
D9h	-5.43	99h	-4.47	59h	-3.51	19h	-2.655
D8h	-5.415	98h	-4.455	58h	-3.495	18h	-2.655
D7h	-5.4	97h	-4.44	57h	-3.48	17h	-2.655
D6h	-5.385	96h	-4.425	56h	-3.465	16h	-2.655
D5h	-5.37	95h	-4.41	55h	-3.45	15h	-2.655
D4h	-5.355	94h	-4.395	54h	-3.435	14h	-2.655
D3h	-5.34	93h	-4.38	53h	-3.42	13h	-2.655
D2h	-5.325	92h	-4.365	52h	-3.405	12h	-2.655
D1h	-5.31	91h	-4.35	51h	-3.39	11h	-2.655
D0h	-5.295	90h	-4.335	50h	-3.375	10h	-2.655
CFh	-5.28	8Fh	-4.32	4Fh	-3.36	0Fh	-2.655
CEh	-5.265	8Eh	-4.305	4Eh	-3.345	0Eh	-2.655
CDh	-5.25	8Dh	-4.29	4Dh	-3.33	0Dh	-2.655
CCh	-5.235	8Ch	-4.275	4Ch	-3.315	0Ch	-2.655
CBh	-5.22	8Bh	-4.26	4Bh	-3.3	0Bh	-2.655
CAh	-5.205	8Ah	-4.245	4Ah	-3.285	0Ah	-2.655
C9h	-5.19	89h	-4.23	49h	-3.27	09h	-2.655
C8h	-5.175	88h	-4.215	48h	-3.255	08h	-2.655
C7h	-5.16	87h	-4.2	47h	-3.24	07h	-2.655
C6h	-5.145	86h	-4.185	46h	-3.225	06h	-2.655
C5h	-5.13	85h	-4.17	45h	-3.21	05h	-2.655
C4h	-5.115	84h	-4.155	44h	-3.195	04h	-2.655
C3h	-5.1	83h	-4.14	43h	-3.18	03h	-2.655
C2h	-5.085	82h	-4.125	42h	-3.165	02h	-2.655
C1h	-5.07	81h	-4.11	41h	-3.15	01h	-2.655
C0h	-5.055	80h	-4.095	40h	-3.135	00h	-2.655

- NGVSS voltage setting

NGVSS[5:0]	NGVSS (V)	NGVSS[5:0]	NGVSS (V)
3Fh	-1.050	1Fh	-0.570
3Eh	-1.035	1Eh	-0.555
3Dh	-1.020	1Dh	-0.540
3Ch	-1.005	1Ch	-0.525
3Bh	-0.990	1Bh	-0.510
3Ah	-0.975	1Ah	-0.495
39h	-0.960	19h	-0.480
38h	-0.945	18h	-0.465
37h	-0.930	17h	-0.450
36h	-0.915	16h	-0.435
35h	-0.900	15h	-0.42
34h	-0.885	14h	-0.405
33h	-0.870	13h	-0.39

32h	-0.855	12h	-0.375
31h	-0.840	11h	-0.36
30h	-0.825	10h	-0.345
2Fh	-0.810	0Fh	-0.33
2Eh	-0.795	0Eh	-0.315
2Dh	-0.780	0Dh	-0.3
2Ch	-0.765	0Ch	-0.285
2Bh	-0.750	0Bh	-0.27
2Ah	-0.735	0Ah	-0.255
29h	-0.720	09h	-0.24
28h	-0.705	08h	-0.225
27h	-0.690	07h	-0.21
26h	-0.675	06h	-0.195
25h	-0.660	05h	-0.18
24h	-0.645	04h	-0.165
23h	-0.630	03h	-0.15
22h	-0.615	02h	-0.135
21h	-0.600	01h	-0.12
20h	-0.585	00h	-0.105

E0H	GMCTRP1(Gamma Correction Characteristics Setting (Positive polarity))									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	1	0	0	0	0	0	E0
1st Parameter	1			GP1R5	GP1R4	GP1R3	GP1R2	GP1R1	GP1R0	
2nd Parameter	1			GP2R5	GP2R4	GP2R3	GP2R2	GP2R1	GP2R0	
3rd Parameter	1			GP3R5	GP3R4	GP3R3	GP3R2	GP3R1	GP3R0	
4th Parameter	1			-	GP4R4	GP4R3	GP4R2	GP4R1	GP4R0	
5th Parameter	1			-	GP5R4	GP5R3	GP5R2	GP5R1	GP5R0	
6th Parameter	1			-	GP6R4	GP6R3	GP6R2	GP6R1	GP6R0	
7th Parameter	1			-	-	GP7R3	GP7R2	GP7R1	GP7R0	
8th Parameter	1			-	-	GP8R3	GP8R2	GP8R1	GP8R0	
9th Parameter	1			-	-	GP9R3	GP9R2	GP9R1	GP9R0	
10th Parameter	1			-	-	GP10R3	GP10R2	GP10R1	GP10R0	
11th Parameter	1			-	GP11R4	GP11R3	GP11R2	GP11R1	GP11R0	
12th Parameter	1			-	GP12R4	GP12R3	GP12R2	GP12R1	GP12R0	
13th Parameter	1			-	GP13R4	GP13R3	GP13R2	GP13R1	GP13R0	
14th Parameter	1			GP14R5	GP14R4	GP14R3	GP14R2	GP14R1	GP14R0	
15th Parameter	1			GP15R5	GP15R4	GP15R3	GP15R2	GP15R1	GP15R0	
16th Parameter	1			GP16R5	GP16R4	GP16R3	GP16R2	GP16R1	GP16R0	

NOTE: "-" Don't care

Description	Gamma adjustment for positive polarity setting. GP1R : For Positive polarity Gamma Level 0 GP2R : For Positive polarity Gamma Level 4 GP3R : For Positive polarity Gamma Level 8 GP4R : For Positive polarity Gamma Level 16 GP5R : For Positive polarity Gamma Level 32 GP6R : For Positive polarity Gamma Level 52 GP7R : For Positive polarity Gamma Level 80 GP8R : For Positive polarity Gamma Level 108 GP9R : For Positive polarity Gamma Level 147 GP10R : For Positive polarity Gamma Level 175 GP11R : For Positive polarity Gamma Level 203 GP12R : For Positive polarity Gamma Level 223 GP13R : For Positive polarity Gamma Level 239 GP14R : For Positive polarity Gamma Level 247 GP15R : For Positive polarity Gamma Level 251 GP16R : For Positive polarity Gamma Level 255
Restriction	
Register Availability	
Default	
Flow Chart	-

E1H	GMCTRN1(Gamma Correction Characteristics Setting (Negative polarity))									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	1	0	0	0	0	1	E1
1st Parameter	1			GN1R5	GN1R4	GN1R3	GN1R2	GN1R1	GN1R0	
2nd Parameter	1			GN2R5	GN2R4	GN2R3	GN2R2	GN2R1	GN2R0	
3rd Parameter	1			GN3R5	GN3R4	GN3R3	GN3R2	GN3R1	GN3R0	
4th Parameter	1			-	GN4R4	GN4R3	GN4R2	GN4R1	GN4R0	
5th Parameter	1			-	GN5R4	GN5R3	GN5R2	GN5R1	GN5R0	
6th Parameter	1			-	GN6R4	GN6R3	GN6R2	GN6R1	GN6R0	
7th Parameter	1			-	-	GN7R3	GN7R2	GN7R1	GN7R0	
8th Parameter	1			-	-	GN8R3	GN8R2	GN8R1	GN8R0	
9th Parameter	1			-	-	GN9R3	GN9R2	GN9R1	GN9R0	
10th Parameter	1			-	-	GN10R3	GN10R2	GN10R1	GN10R0	
11th Parameter	1			-	GN11R4	GN11R3	GN11R2	GN11R1	GN11R0	
12th Parameter	1			-	GN12R4	GN12R3	GN12R2	GN12R1	GN12R0	
13th Parameter	1			-	GN13R4	GN13R3	GN13R2	GN13R1	GN13R0	
14th Parameter	1			GN14R5	GN14R4	GN14R3	GN14R2	GN14R1	GN14R0	
15th Parameter	1			GN15R5	GN15R4	GN15R3	GN15R2	GN15R1	GN15R0	
16th Parameter	1			GN16R5	GN16R4	GN16R3	GN16R2	GN16R1	GN16R0	

NOTE: "-" Don't care

Description	Gamma adjustment for negative porlarity setting. GN1R : For Negative polarity Gamma Level 0 GN2R : For Negative polarity Gamma Level 4 GN3R : For Negative polarity Gamma Level 8 GN4R : For Negative polarity Gamma Level 16 GN5R : For Negative polarity Gamma Level 32 GN6R : For Negative polarity Gamma Level 52 GN7R : For Negative polarity Gamma Level 80 GN8R : For Negative polarity Gamma Level 108 GN9R : For Negative polarity Gamma Level 147 GN10R : For Negative polarity Gamma Level 175 GN11R : For Negative polarity Gamma Level 203 GN12R : For Negative polarity Gamma Level 223 GN13R : For Negative polarity Gamma Level 239 GN14R : For Negative polarity Gamma Level 247 GN15R : For Negative polarity Gamma Level 251 GN16R : For Negative polarity Gamma Level 255
Restriction	
Register Availability	
Default	
Flow Chart	-

C. Touch Panel Command and Register Map

1. I2C Protocol Definition

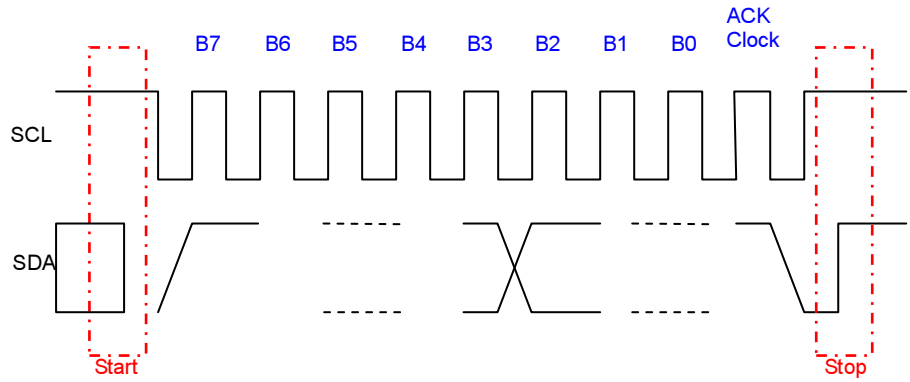


Figure 1. Standard I^2C Transaction Unit

The sensor controller supports standard I^2C protocol with SCL up to 400KHz. The device address is 0x58. The chip also provides both single and sequential access. Figure 2 shows the write operation using single or sequential mode. Figure 3 also depicts the standard I2C transaction for single for sequential read mechanism.

Write Operation

Single	Start	Device Address (W)	A	Mem Addr	A	Data[0]	A	Stop						
Sequential	Start	Device Address (W)	A	Mem Addr	A	Data[0]	A	Data[1]	A	……	A	Data[n]	A	Stop

Figure 2. Write Operation with Single/Multiple Access

Read Operation

Single	Start	Device Address (W)	A	Mem Addr	A	Start	Device Address (R)	A	Data[0]	NA	Stop			
Sequential	Start	Device Address (W)	A	Mem Addr	A	Start	Device Address (R)	A	Data[0]	A	……	A	Data[n]	NA	Stop

Figure 3. Read Operation with Single/Multiple Access

2. I2C Data Map

2.1 Register Data Map

Addr.	Description	R/W	B7	B6	B5	B4	B3	B2	B1	B0
0	NumMailboxes	R	0	0	0	0	0	0	0	1
1	SlaveID	R/W	Busy	0	0	0	0	0	0	0
2	reserved		0	0	0	0	0	0	0	0
3	X1 (MSB)	R	0	0	0	0	0	0	X1[9]	X1[8]
4	X1 (LSB)	R	X1[7]	X1[6]	X1[5]	X1[4]	X1[3]	X1[2]	X1[1]	X1[0]
5	Y1 (MSB)	R	0	0	0	0	0	0	Y1[9]	Y1[8]
6	Y1 (LSB)	R	Y1[7]	Y1[6]	Y1[5]	Y1[4]	Y1[3]	Y1[2]	Y1[1]	Y1[0]
7	X2 (MSB)	R	0	0	0	0	0	0	X2[9]	X2[8]
8	X2 (LSB)	R	X2[7]	X2[6]	X2[5]	X2[4]	X2[3]	X2[2]	X2[1]	X2[0]
9	Y2 (MSB)	R	0	0	0	0	0	0	Y2[9]	Y2[8]
10	Y2 (LSB)	R	Y2[7]	Y2[6]	Y2[5]	Y2[4]	Y2[3]	Y2[2]	Y2[1]	Y2[0]
11	TouchNumber	R	0	0	0	0	0	0	TouchNumer[1:0]	
12	Gesture	R	Gesture[7:0]							
13	reserved		0	0	0	0	0	0	0	0
14	reserved		0	0	0	0	0	0	0	0
15	reserved		0	0	0	0	0	0	0	0
16	reserved		0	0	0	0	0	0	0	0
17	X[0]	R	ADC_0[7]	ADC_0[6]	ADC_0[5]	ADC_0[4]	ADC_0[3]	ADC_0[2]	ADC_0[1]	ADC_0[0]
18	X[1]	R	ADC_1[7]	ADC_1[6]	ADC_1[5]	ADC_1[4]	ADC_1[3]	ADC_1[2]	ADC_1[1]	ADC_1[0]
19	X[2]	R	ADC_2[7]	ADC_2[6]	ADC_2[5]	ADC_2[4]	ADC_2[3]	ADC_2[2]	ADC_2[1]	ADC_2[0]
20	X[3]	R	ADC_3[7]	ADC_3[6]	ADC_3[5]	ADC_3[4]	ADC_3[3]	ADC_3[2]	ADC_3[1]	ADC_3[0]
21	X[4]	R	ADC_4[7]	ADC_4[6]	ADC_4[5]	ADC_4[4]	ADC_4[3]	ADC_4[2]	ADC_4[1]	ADC_4[0]
22	X[5]	R	ADC_5[7]	ADC_5[6]	ADC_5[5]	ADC_5[4]	ADC_5[3]	ADC_5[2]	ADC_5[1]	ADC_5[0]
23	X[6]	R	ADC_6[7]	ADC_6[6]	ADC_6[5]	ADC_6[4]	ADC_6[3]	ADC_6[2]	ADC_6[1]	ADC_6[0]
24	X[7]	R	ADC_7[7]	ADC_7[6]	ADC_7[5]	ADC_7[4]	ADC_7[3]	ADC_7[2]	ADC_7[1]	ADC_7[0]
25	X[8]	R	ADC_8[7]	ADC_8[6]	ADC_8[5]	ADC_8[4]	ADC_8[3]	ADC_8[2]	ADC_8[1]	ADC_8[0]
26	X[9]	R	ADC_9[7]	ADC_9[6]	ADC_9[5]	ADC_9[4]	ADC_9[3]	ADC_9[2]	ADC_9[1]	ADC_9[0]
27	X[10]	R	ADC_10[7]	ADC_10[6]	ADC_10[5]	ADC_10[4]	ADC_10[3]	ADC_10[2]	ADC_10[1]	ADC_10[0]
28	X[11]	R	ADC_11[7]	ADC_11[6]	ADC_11[5]	ADC_11[4]	ADC_11[3]	ADC_11[2]	ADC_11[1]	ADC_11[0]
29	X[12]	R	ADC_12[7]	ADC_12[6]	ADC_12[5]	ADC_12[4]	ADC_12[3]	ADC_12[2]	ADC_12[1]	ADC_12[0]
30	X[13]	R	ADC_13[7]	ADC_13[6]	ADC_13[5]	ADC_13[4]	ADC_13[3]	ADC_13[2]	ADC_13[1]	ADC_13[0]
31	Y[0]	R	ADC_14[7]	ADC_14[6]	ADC_14[5]	ADC_14[4]	ADC_14[3]	ADC_14[2]	ADC_14[1]	ADC_14[0]
32	Y[1]	R	ADC_15[7]	ADC_15[6]	ADC_15[5]	ADC_15[4]	ADC_15[3]	ADC_15[2]	ADC_15[1]	ADC_15[0]
33	Y[2]	R	ADC_16[7]	ADC_16[6]	ADC_16[5]	ADC_16[4]	ADC_16[3]	ADC_16[2]	ADC_16[1]	ADC_16[0]
34	Y[3]	R	ADC_17[7]	ADC_17[6]	ADC_17[5]	ADC_17[4]	ADC_17[3]	ADC_17[2]	ADC_17[1]	ADC_17[0]
35	Y[4]	R	ADC_18[7]	ADC_18[6]	ADC_18[5]	ADC_18[4]	ADC_18[3]	ADC_18[2]	ADC_18[1]	ADC_18[0]
36	Y[5]	R	ADC_19[7]	ADC_19[6]	ADC_19[5]	ADC_19[4]	ADC_19[3]	ADC_19[2]	ADC_19[1]	ADC_19[0]
37	Y[6]	R	ADC_20[7]	ADC_20[6]	ADC_20[5]	ADC_20[4]	ADC_20[3]	ADC_20[2]	ADC_20[1]	ADC_20[0]
38	Y[7]	R	ADC_21[7]	ADC_21[6]	ADC_21[5]	ADC_21[4]	ADC_21[3]	ADC_21[2]	ADC_21[1]	ADC_21[0]
39	INT_SETTING	R/W	0	0	0	0	0	0	INT_MODE[1]	INT_MODE[0]
40	INT_WIDTH	R/W	INT_WIDTH[7:0]							

2.2 Default Setting

39	INT_SETTING	R/W	0	0	0	0	1	1	0	0
40	INT_WIDTH	R/W	0	0	0	0	1	0	1	0

3. Raw Data Register Map

17	X[0]	R	ADC_0[7]	ADC_0[6]	ADC_0[5]	ADC_0[4]	ADC_0[3]	ADC_0[2]	ADC_0[1]	ADC_0[0]
18	X[1]	R	ADC_1[7]	ADC_1[6]	ADC_1[5]	ADC_1[4]	ADC_1[3]	ADC_1[2]	ADC_1[1]	ADC_1[0]
19	X[2]	R	ADC_2[7]	ADC_2[6]	ADC_2[5]	ADC_2[4]	ADC_2[3]	ADC_2[2]	ADC_2[1]	ADC_2[0]
20	X[3]	R	ADC_3[7]	ADC_3[6]	ADC_3[5]	ADC_3[4]	ADC_3[3]	ADC_3[2]	ADC_3[1]	ADC_3[0]
21	X[4]	R	ADC_4[7]	ADC_4[6]	ADC_4[5]	ADC_4[4]	ADC_4[3]	ADC_4[2]	ADC_4[1]	ADC_4[0]
22	X[5]	R	ADC_5[7]	ADC_5[6]	ADC_5[5]	ADC_5[4]	ADC_5[3]	ADC_5[2]	ADC_5[1]	ADC_5[0]
23	X[6]	R	ADC_6[7]	ADC_6[6]	ADC_6[5]	ADC_6[4]	ADC_6[3]	ADC_6[2]	ADC_6[1]	ADC_6[0]
24	X[7]	R	ADC_7[7]	ADC_7[6]	ADC_7[5]	ADC_7[4]	ADC_7[3]	ADC_7[2]	ADC_7[1]	ADC_7[0]
25	X[8]	R	ADC_8[7]	ADC_8[6]	ADC_8[5]	ADC_8[4]	ADC_8[3]	ADC_8[2]	ADC_8[1]	ADC_8[0]
26	X[9]	R	ADC_9[7]	ADC_9[6]	ADC_9[5]	ADC_9[4]	ADC_9[3]	ADC_9[2]	ADC_9[1]	ADC_9[0]
27	X[10]	R	ADC_10[7]	ADC_10[6]	ADC_10[5]	ADC_10[4]	ADC_10[3]	ADC_10[2]	ADC_10[1]	ADC_10[0]
28	X[11]	R	ADC_11[7]	ADC_11[6]	ADC_11[5]	ADC_11[4]	ADC_11[3]	ADC_11[2]	ADC_11[1]	ADC_11[0]
29	X[12]	R	ADC_12[7]	ADC_12[6]	ADC_12[5]	ADC_12[4]	ADC_12[3]	ADC_12[2]	ADC_12[1]	ADC_12[0]
30	X[13]	R	ADC_13[7]	ADC_13[6]	ADC_13[5]	ADC_13[4]	ADC_13[3]	ADC_13[2]	ADC_13[1]	ADC_13[0]
31	Y[0]	R	ADC_14[7]	ADC_14[6]	ADC_14[5]	ADC_14[4]	ADC_14[3]	ADC_14[2]	ADC_14[1]	ADC_14[0]
32	Y[1]	R	ADC_15[7]	ADC_15[6]	ADC_15[5]	ADC_15[4]	ADC_15[3]	ADC_15[2]	ADC_15[1]	ADC_15[0]
33	Y[2]	R	ADC_16[7]	ADC_16[6]	ADC_16[5]	ADC_16[4]	ADC_16[3]	ADC_16[2]	ADC_16[1]	ADC_16[0]
34	Y[3]	R	ADC_17[7]	ADC_17[6]	ADC_17[5]	ADC_17[4]	ADC_17[3]	ADC_17[2]	ADC_17[1]	ADC_17[0]
35	Y[4]	R	ADC_18[7]	ADC_18[6]	ADC_18[5]	ADC_18[4]	ADC_18[3]	ADC_18[2]	ADC_18[1]	ADC_18[0]
36	Y[5]	R	ADC_19[7]	ADC_19[6]	ADC_19[5]	ADC_19[4]	ADC_19[3]	ADC_19[2]	ADC_19[1]	ADC_19[0]
37	Y[6]	R	ADC_20[7]	ADC_20[6]	ADC_20[5]	ADC_20[4]	ADC_20[3]	ADC_20[2]	ADC_20[1]	ADC_20[0]
38	Y[7]	R	ADC_21[7]	ADC_21[6]	ADC_21[5]	ADC_21[4]	ADC_21[3]	ADC_21[2]	ADC_21[1]	ADC_21[0]

Note: Chip provides 10-bit ADC capability at least. While the unused ADC bit should be reserved as '0'

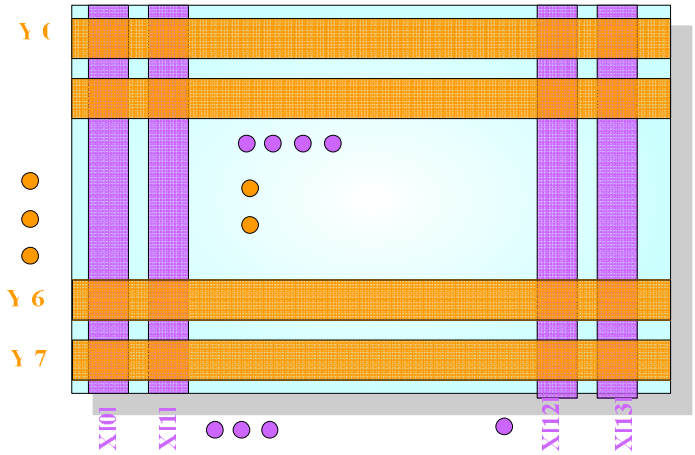


Figure 4. Reference of channel location diagram

4. Coordinate Register Map

3	X1 (MSB)	R	0	0	0	0	0	0	X1[9]	X1[8]
4	X1 (LSB)	R	X1[7]	X1[6]	X1[5]	X1[4]	X1[3]	X1[2]	X1[1]	X1[0]
5	Y1 (MSB)	R	0	0	0	0	0	0	Y1[9]	Y1[8]
6	Y1 (LSB)	R	Y1[7]	Y1[6]	Y1[5]	Y1[4]	Y1[3]	Y1[2]	Y1[1]	Y1[0]
7	X2 (MSB)	R	0	0	0	0	0	0	X2[9]	X2[8]
8	X2 (LSB)	R	X2[7]	X2[6]	X2[5]	X2[4]	X2[3]	X2[2]	X2[1]	X2[0]
9	Y2 (MSB)	R	0	0	0	0	0	0	Y2[9]	Y2[8]
10	Y2 (LSB)	R	Y2[7]	Y2[6]	Y2[5]	Y2[4]	Y2[3]	Y2[2]	Y2[1]	Y2[0]

Note: (1) (X1, Y1) means left-up touched point
(X2, Y2) means right-down touched point

(2) The coordinate of X1 = X1(LSB) + X1(MSB)*256, X2 = X2(LSB) + X2(MSB)*256, Y1 = Y1(LSB) + Y1(MSB)*256, Y2 = Y2(LSB) + Y2(MSB)*256

(3) If panel resolution is smaller than 256, user doesn't need reading address 68 ~ 71

(4)

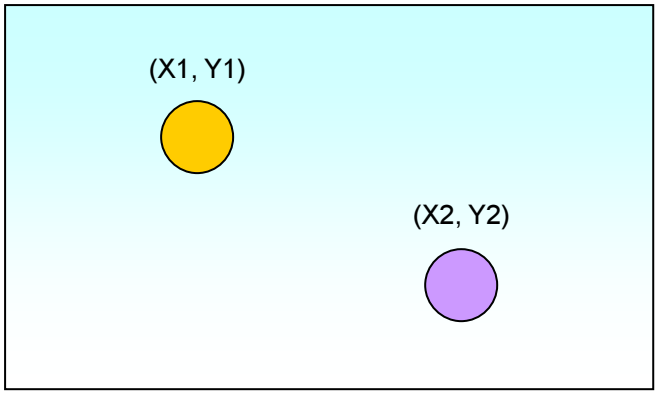


Figure 5. Reference of touched point diagram

If touched point of (X1,Y1)、(X2, Y2) is (14,50) and (280,160), the coordinate register map will be recorded as following:

3	X1 (MSB)	R	0	0	0	0	0	0	0	0
4	X1 (LSB)	R	0	0	0	0	1	1	1	0
5	Y1 (MSB)	R	0	0	0	0	0	0	0	0
6	Y1 (LSB)	R	0	0	1	1	0	0	1	0
7	X2 (MSB)	R	0	0	0	0	0	0	0	1
8	X2 (LSB)	R	0	0	0	1	1	0	0	0
9	Y2 (MSB)	R	0	0	0	0	0	0	0	0
10	Y2 (LSB)	R	1	0	1	0	0	0	0	0

5. Interrupt Operation Mode

This chip should support both polling and interrupt way to get the coordinate and raw data by I2C interface. The figure below depicts the interruption operation.

6.1 Interrupt Mode Setting

39	INT_SETTING	R/W	0	0	0	0	0	0	INT_MODE[1]	INT_MODE[0]
40	INT_WIDTH	R/W	INT_WIDTH[7:0]							

Note: (1) EN_INT
0: Disable interrupt mechanism 1: Enable interrupt mechanism
(2) INT_POL
0: The interrupt is low-active 1: the interrupt is high-active
(3) INT_ MODE[1:0]
00: INT assert periodically 01: INT assert only when coordinate difference
10: Touch Indicate 11: Reserved (INT disabled)

6.2 Sensing Periodical Mode **(INT_MODE[1:0] = [0,0]).**
For sensing periodical mode, the INT_MODE[1:0] should be [0,0].
The data must be ready (including coordinate and raw data) before signal 'INT' rising.

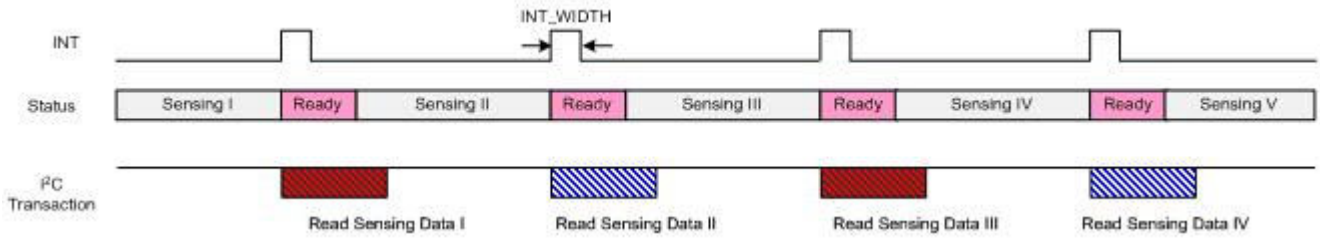


Figure 7: Interruption with INT_R auto-reset

6.3 Coordinate Compare Mode **(INT_MODE[1:0] = [0,1]).**
The INT signal will be asserted while coordinate changes under comparison mode (INT_MODE[1:0] = [0,1]).

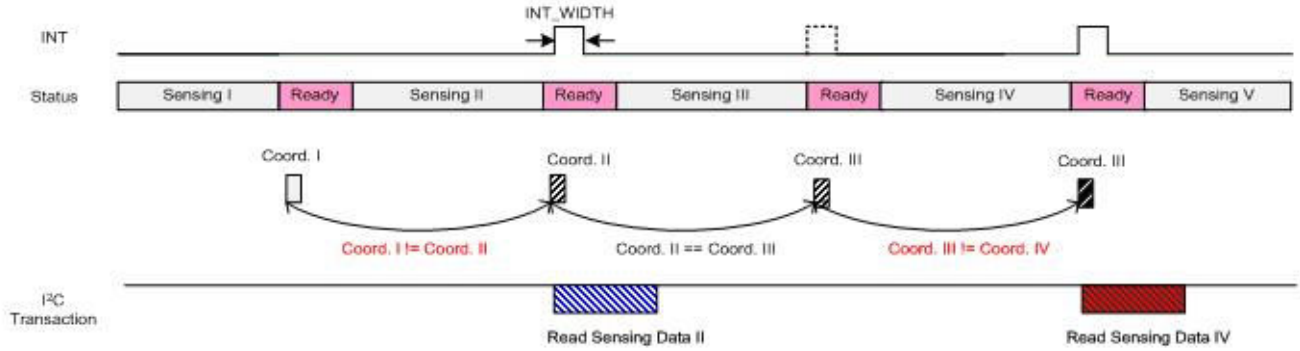


Figure 8: Interruption Flag under Coordinate Compare Mode

6.4 Touch Indicate Mode **(INT_MODE[1:0] = [1,0]).**

The interrupt will assert when the touch is valid. The interrupt should keep high until the touch is released.

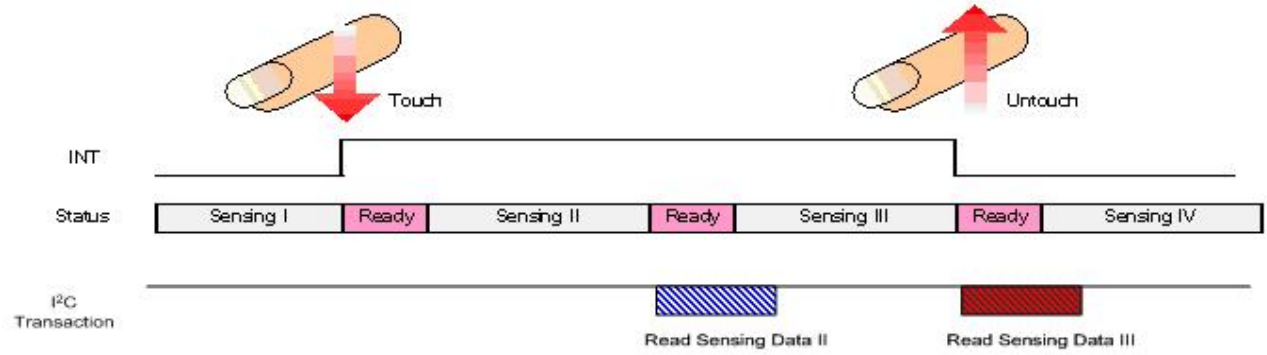
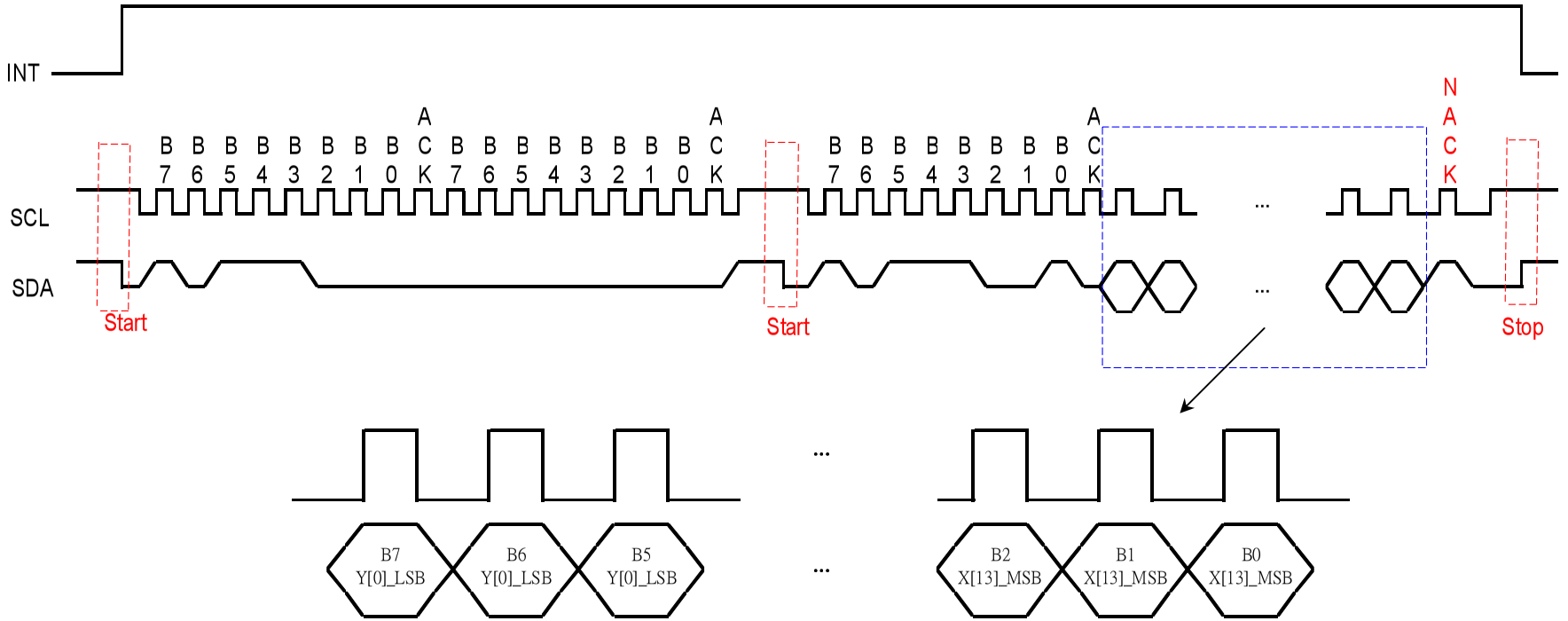


Figure 9: Touch Indicate Mode

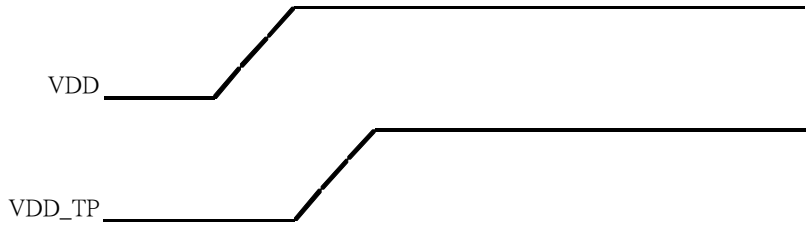
Combination interrupt with I2C sequential read raw data operation for as following (for INT_MODE[1:0] = [1,0])



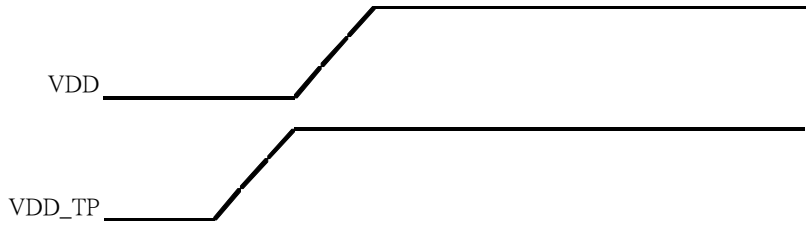
7. Power on/off Sequence (both have two cases)

- Power on Sequence

Case1:

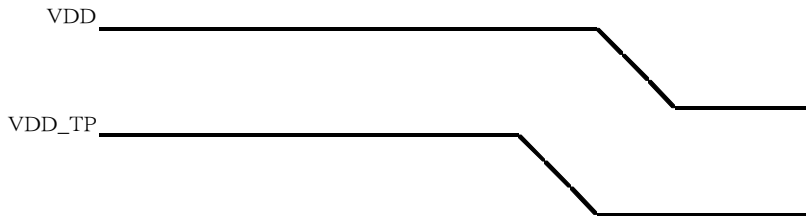


Case2:

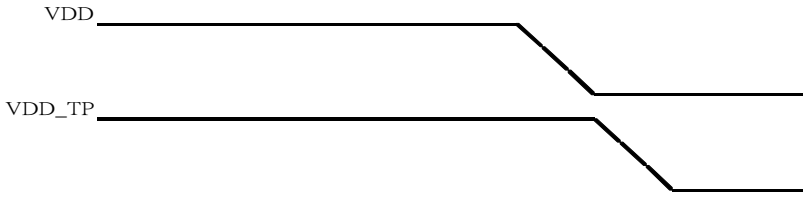


- Power off Sequences

Case1:



Case2:



D. Optical Specification (Note1, Note 2 and Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall	 Tr Tf	θ=0°	 -- --	 15 30	 30 50	 ms ms	Note 4
Contrast ratio	CR	At optimized viewing angle	600	800	--		Note 5,6
Viewing Angle Top Bottom Left Right	Φ_T Φ_B Φ_L Φ_R	CR□10	70 70 70 70	80 80 80 80	-- -- -- --	deg.	Note 7
Brightness	Y_L	θ=0°	250	315	--	cd/m^2	Note 8
Chromaticity White	X	θ=0°	0.26	0.31	0.36		
	Y	θ=0°	0.28	0.33	0.38		
Uniformity	ΔY_L	%	70	75	--	%	Note 9

Note 1. Ambient temperature =25℃.

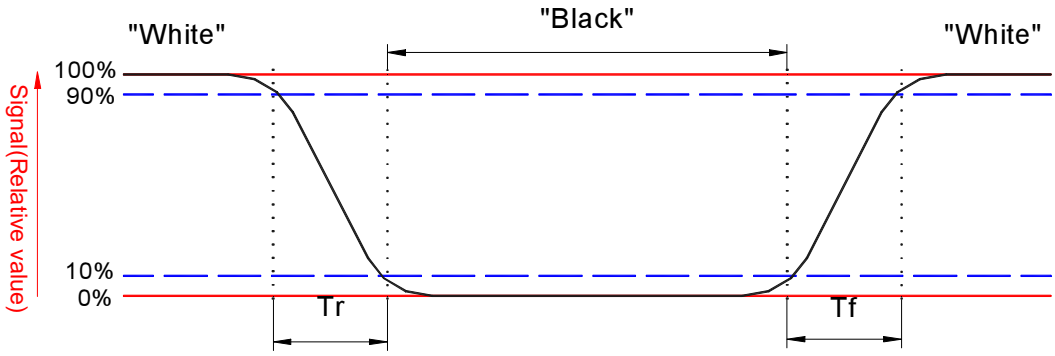
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-5A, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White $Vi=V_{i50} \mp 1.5V$

Black $Vi=V_{i50} \pm 2.0V$

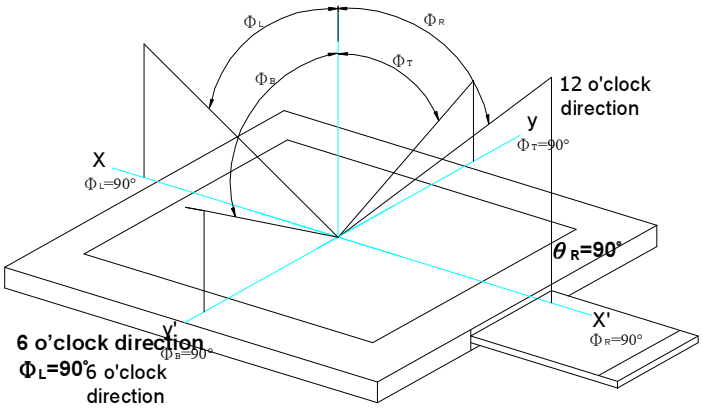
"±" Means that the analog input signal swings in phase with COM signal.

"$\mp$" Means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

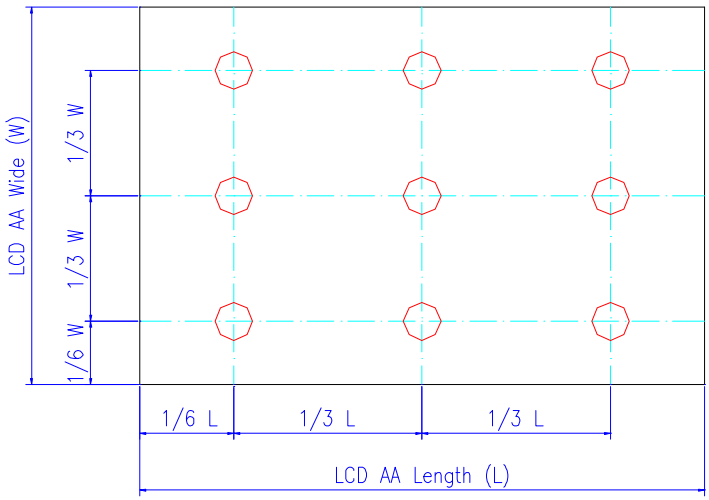
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle, ϕ, Refer to figure as below.



Note 8. Measured at the center area of the panel in gray level 255

Note 9. Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

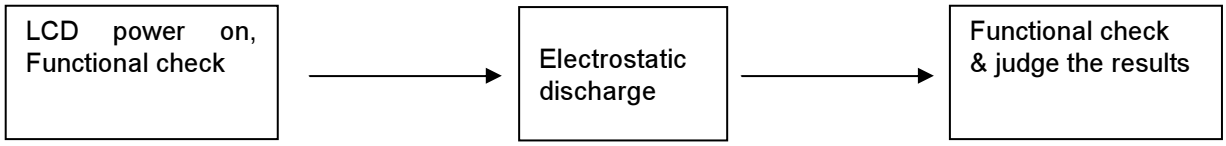
E. Reliability Test Items

No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70□ 240Hrs	
2	Low Temperature Storage	Ta= -25□ 240Hrs	
3	High Ttemperature Operation	Tp= 60□ 240Hrs	
4	Low Temperature Operation	Ta= -10□ 240Hrs	Note 2
5	High Temperature & High Humidity	Tp= 60□. 90% RH 240Hrs	Operation
6	Heat Shock	-25□~80□, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	Note 3,4
8	Vibration (With Carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
9	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1. Ta: Ambient temperature. No. 1~No.5 test condition are in the laboratory environment after 2 hours of recovery time.

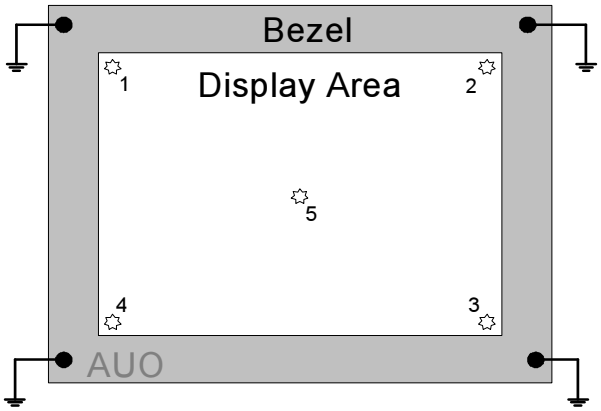
Note.2. Judged by the on/off testing results of AUO's standard w/o functional fail.

Note 3. ESD Testing Flow as the below,



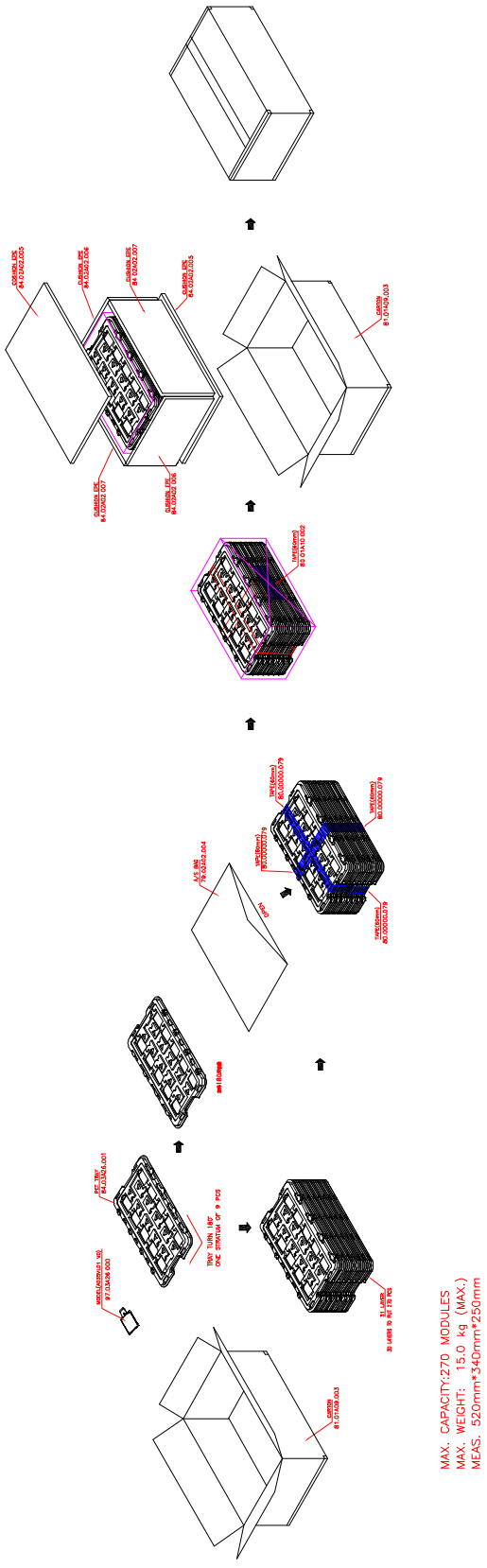
Note 4. ESD testing method.

1. Ambient: 24~26□, 56~65%RH
2. Instruments:NoisekenESS-2000,
3. Operation System: "CX40FL-B"
4. Test Mode: Operating mode, test pattern: colorbar+8Gray scale
5. Test Method:
   a. Contact Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
   b. Air Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
6. Test point:

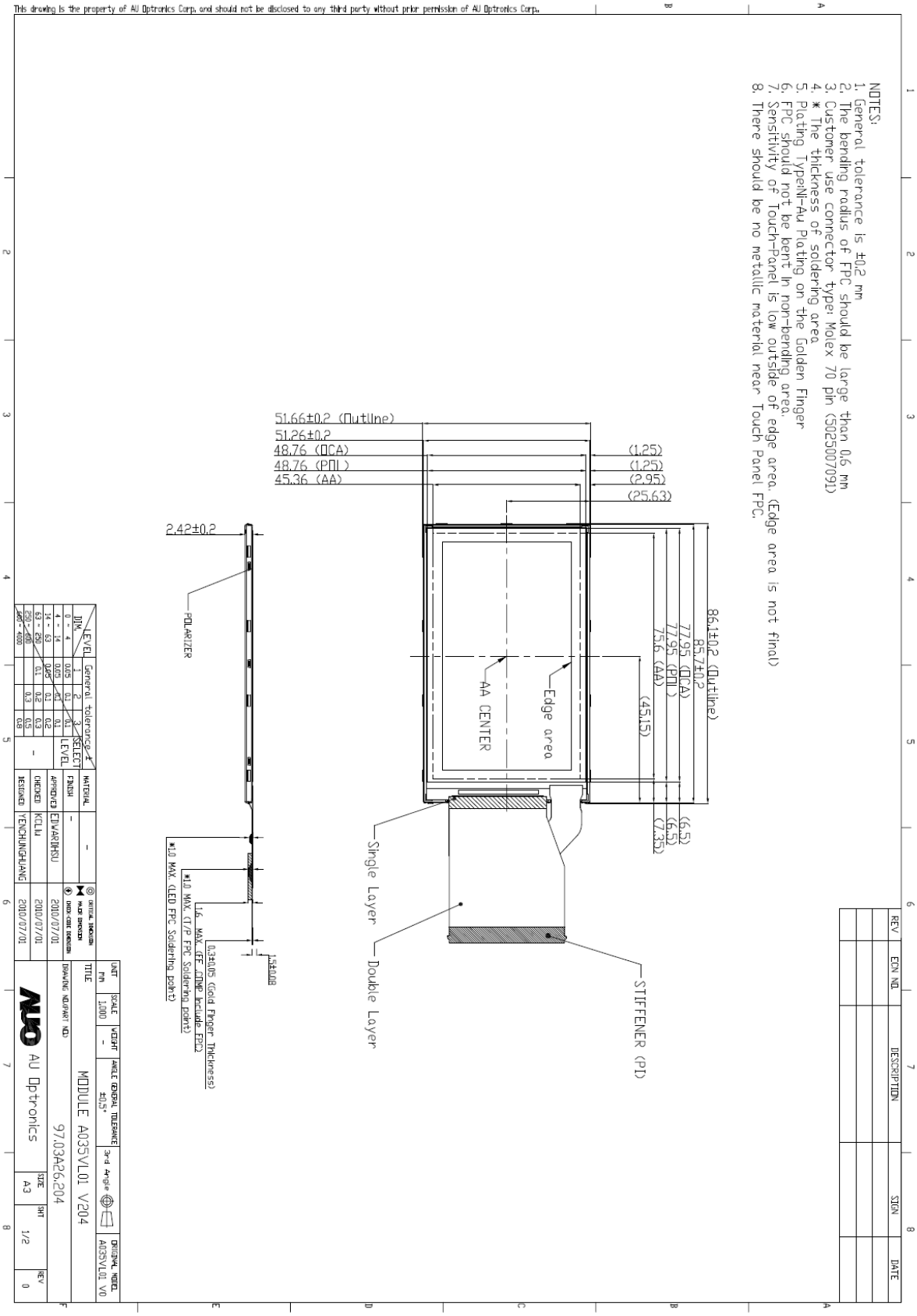


7. The metal casing is connected to power supply ground (0V) at four corners.

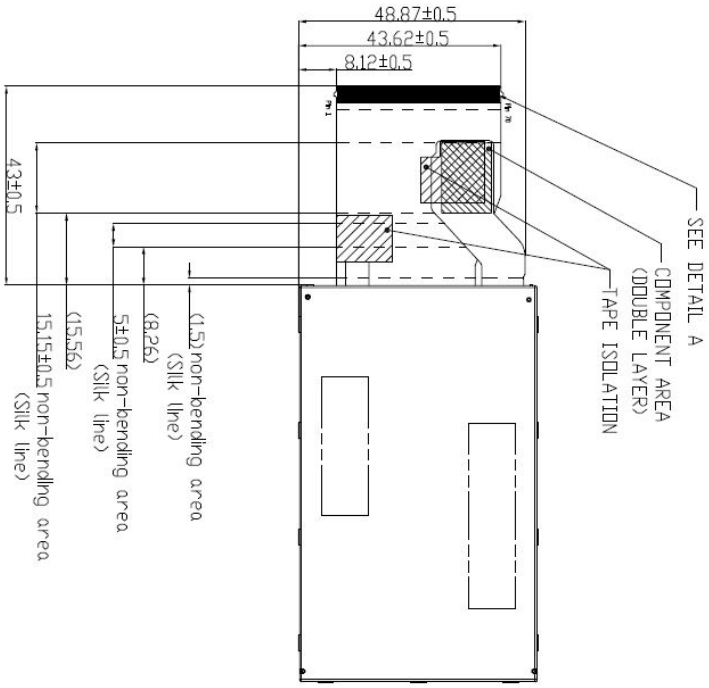
Packing Form

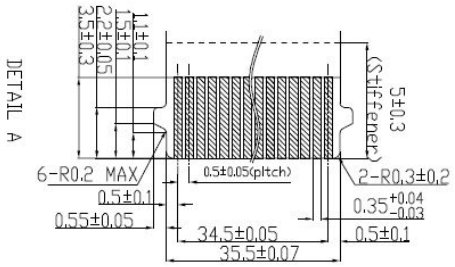


F. Outline dimension



NOTES:
1. General tolerance is ±0.2 mm
2. The bending radius of FPC should be large than 0.6 mm
3. Customer use connector type: Molex 70 pin (502500791)
4. * The thickness of soldering area
5. Plating Type:Ni-Au Plating on the Golden Finger
6. FPC should not be bent in non-bending area.
7. Sensitivity of Touch-Panel is low outside of edge area. (Edge area is not final)
8. There should be no metallic material near Touch Panel FPC.





LEVEL	General tolerance
DIM.	SELECT LEVEL
0.5 ~ 4	1 0.05
4 ~ 63	2 0.1
63 ~ 250	3 0.3
250 ~ 400	
400 ~ 1000	

MATERIAL	-	CRITICAL DIMENSION	
FINISH	-	MAJOR DIMENSION	
APPROVED	EDWARDHSU	MECH-CODE DIMENSION	2010/07/01
CHECKED	KCLiu		2010/07/01
DESIGNED	YENCHUNGHUANG		2010/07/01

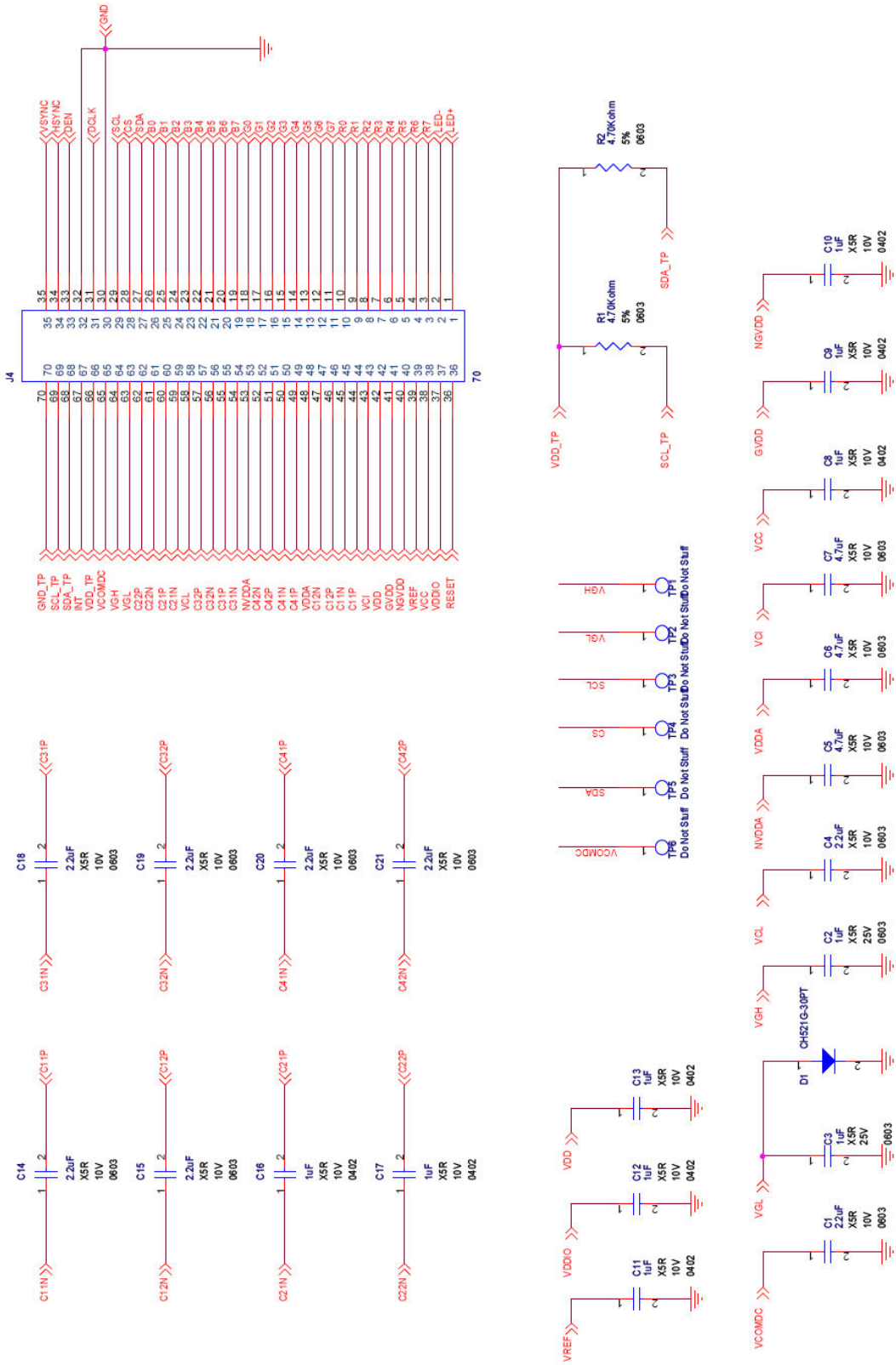
UNIT	mm	TITLE	MODULE A035VL01 V204
SCALE	1.000	DRAWING NO(PART NO)	97.03A26.204
WEIGHT	-		
ANGLE (GENERAL TOLERANCE ±0.5°)			
3rd Angle			
SIZE	A3	SHT	2/2
REV	0	ORIGINAL MODEL	A035VL01 V0

AU Optronics

REV.	ECN NO.	DESCRIPTION	SIGN	DATE

G. Application note

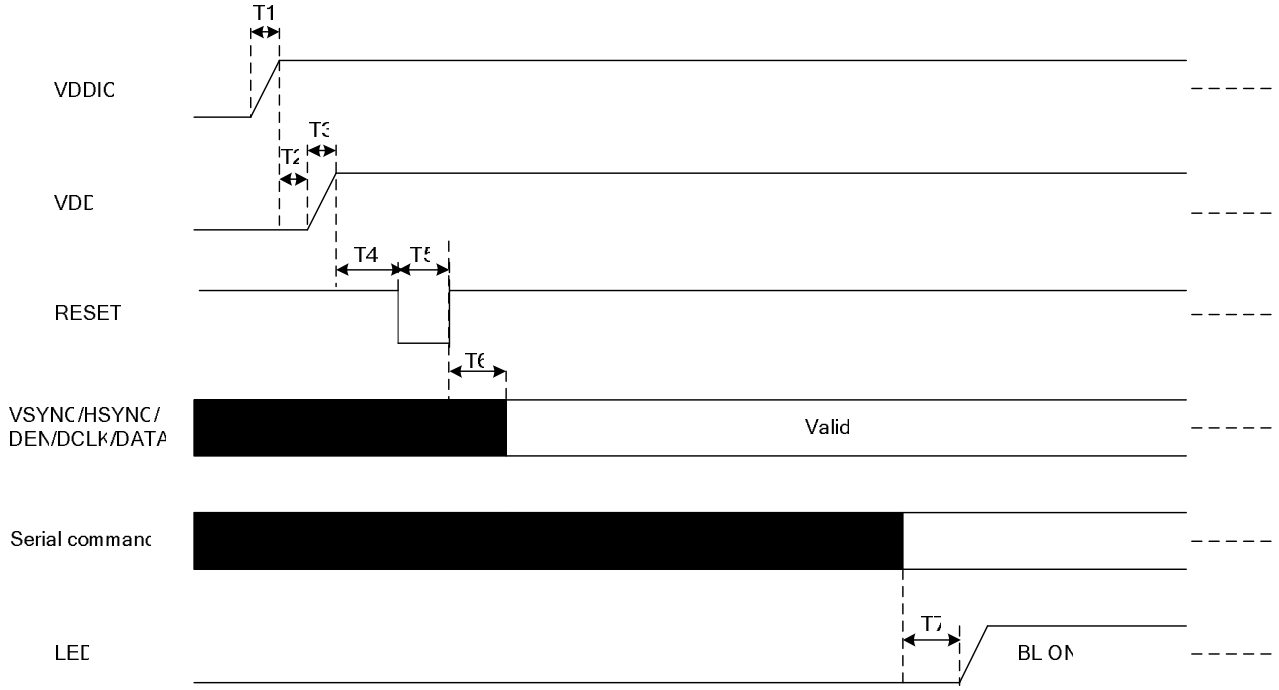
1. Application circuit



2. Power on/off sequence

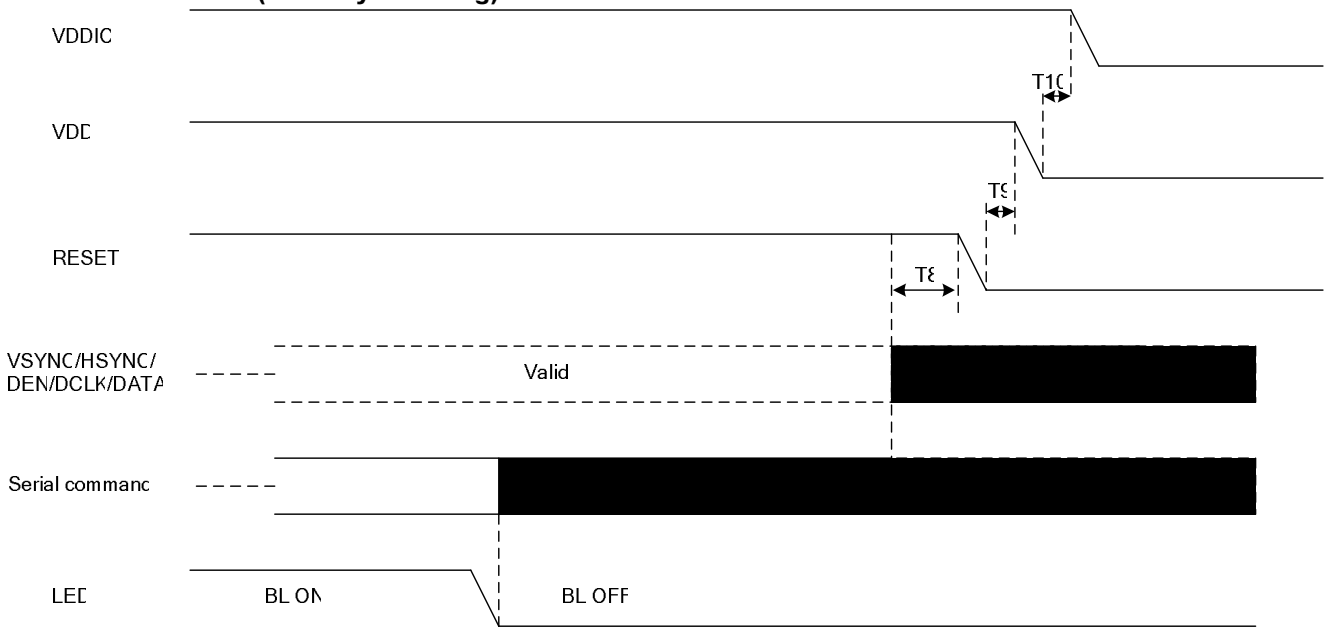
The register setting of standby mode disabling / enabling is used to control the build-in power on / off sequence.

2.1 Power on (Standby Disabling)



Note: 0us<T1<500us; 100us>T2≧0us; 0us <T3<500us; T4≧5ms; T5≧50us; T6≧120ms; T7≧120ms

2.2 Power off (Standby Enabling)



Note: T8≧70ms ;T9≧1ms; T10≧1ms

3. Recommended power on/off serial command settings

3.1 Recommended power on register setting (Just for reference,)

Number	Command(Binary)		Number	Command(Binary)	
1	000010001	Sleep out	32	100010001	Positive gamma setting
WAIT 120ms			33	100001101	
2	000000001	SW reset	34	100001110	
WAIT 120ms			35	100000000	
3	011000001	VGH/VGL Setting	36	100000100	
4	110101000		37	100001000	
5	110110001		38	100010011	
6	101000101		39	100010100	
7	100000100		40	100101111	
8	011000101	VCOMDC	41	100101001	
9	110000000		42	100100100	
10	101101100		43	011100001	Negative gamma setting
11	011000110	GVDD/GVSS	44	100000000	
12	110111101		45	100000100	
13	110000100		46	100001000	
14	011000111	NGVDD/NGVSS	47	100001011	
15	110111101		48	100001100	
16	110000100		49	100010001	
17	010111101	Disable Pre-Charge	50	100001101	
18	100000010		51	100001110	
19	000010001	Sleep out	52	100000000	
WAIT 120ms			53	100000100	
20	011110010	Gamma setting follow 26h, E0h, E1h	54	100001000	
21	100000000		55	100010011	
22	100000000		56	100010100	
23	110000010		57	100101111	
24	000100110	Enable gamma setting	58	100101001	
25	100001000		59	100100100	
26	011100000	Positive gamma setting	60	000100110	Enable gamma setting
27	100000000		61	100001000	
28	100000100		62	011111101	Enable 2-dot function
29	100001000		63	100000000	
30	100001011		64	100001000	
31	100001100		65	000101001	Display on

3.2 Recommended power off register setting

Number	Command(Binary)
1	000010000