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Date :	Feb. 9, 2003

Product Specifications

2.0″ COLOR LTPS TFT-LCD MODULE

MODEL NAME: A020BL01

<◆>Preliminary Specifications

< > Final Specifications

Note: The content of the specifications is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.4a	Feb. 9, 2004		Draft.

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A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution(dot)	640(W) × 240(H)	
2	Active area(mm)	40.64(W) × 30.48(H)	
3	Screen size(inch)	2.0 (Diagonal)	
4	Dot pitch(mm)	0.0635(W) × 0.127(H)	
5	Color configuration	R. G. B. delta	
6	Overall dimension(mm)	48.5(W) × 39.8(H) × 3.3(D)	Note 1
7	Weight(g)	20 g	
8	Panel Surface treatment	Hard coating (3H)	

Note 1: Refer to Fig. 7

B. Electrical specifications

1.Pin assignment

a. TFT-LCD panel driving section

Pin no	Symbol	I/O	Description	Remark
1	CS	I	Serial command enable signal	Note 1
2	SDA	I	Serial command data input	Note 1
3	SCL	I	Serial command clock input	Note 1
4	HSYNC	I	Horizontal sync input	
5	VSYNC	I	Vertical sync input	
6	DCLK	I	Input data clock	
7	D7	I	Data input; MSB	
8	D6	I	Data input	
9	D5	I	Data input	
10	D4	I	Data input	
11	D3	I	Data input	
12	D2	I	Data input	
13	D1	I	Data input	
14	D0	I	Data input; LSB	
15	DRV	O	VLED boost transistor driving signal	
16	VLED	P	LED power: anode	
17	FB	I / P	LED power: cathode	
18	AVDD	C	Power setting capacitor	
19	AGND	P	Ground for analog circuit	
20	GND	P	Ground for digital circuit	
21	VCC	P	Power supply for integrated LCD driver IC	
22	V1	C	Power setting capacitor	
23	V2	C	Power setting capacitor	
24	V3	C	Power setting capacitor	
25	V4	C	Power setting capacitor	
26	V5	C	Power setting capacitor	

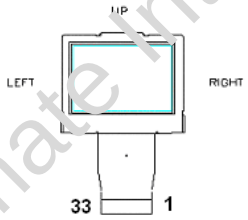
27	V6	C	Power setting capacitor	
28	V7	C	Power setting capacitor	
29	V8	C	Power setting capacitor	
30	FRP	O	VCOM driving signal	Note 2
31	VGL	C	Power setting capacitor	
32	VGH	C	Power setting capacitor	
33	VCOM	I	Common voltage	

I: Input; O: Output; P: Power; C: Capacitor.

Note 1: 3-wire serial control interface is operational after VCC power on reset, but execution of programmed commands is synchronized at front edge of next VSYNC pulse.

Note 2: FRP is the output of Vcom driver. It is the same phase and amplitude with common electrode driving signal (Vcom). The Vcom amplitude and DC level setting can be adjusted through serial control. External Vcom DC adjustment is also achievable. Please refer to the application note for details.

Note 3: For pin sequence arrangement and scan direction, please refer to the figure as below:



b. Backlight driving section

No.	Symbol	I/O	Description	Remark
Pin 16	VLED	I	LED Anode	
Pin 17	FB	-	LED Cathode	

2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V_{CC}	GND=0	-0.5	5	V	
Operating temperature	Topa		0	60	℃	Ambient temperature
Storage temperature	Tstg		-25	80	℃	Ambient temperature

3. Electrical Specifications

a. Recommended operating conditions (GND=AGND=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		V_{CC}	2.7	3.3	3.6	V	Note 1
Input Signal voltage	H Level	V_{IH}	2.4	-	V_{CC}	V	
	L Level	V_{IL}	GND	-	0.8	V	

Note 1: A build-in power on reset circuit for V_{CC} is provided within the integrated LCD driver IC. The LCD module is in power save mode in default, and a standby releasing is required after V_{CC} power on through serial control. Please refer to the register STB setting for detail.

b. Electrical Characteristics (GND=AGND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for V_{CC}	I_{CC}	V_{CC}=3.3V	-	TBD		mA	Note 1
	$I_{CC(STANDBY)}$	V_{CC}=3.3V	-	TBD		mA	
DC-DC voltage	V_{GH}	V_{CC}=3.3V		8.5		V	Note 2
	V_{GL}	V_{CC}=3.3V		-6.5		V	Note 2
VCOM voltage	V_{CAC}		5.0	5.6	6.4	Vp-p	AC component, Note 3
	V_{CDC}		0		1.75	V	DC component, Note 4
DRV output voltage	V_{DRV}		0		VCC	V	
DRV output current	IDRV				TBD	mA	
Feedback voltage	V_{FB}		0.57	0.6	0.63	V	

Note 1: Total power consumption: mW (typ.); mW (max.)

Note 2: V_{GH} and V_{GL} are output voltages of integrated LCD driver IC.

Note 3: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.

Note 4: V_{CDC} could be adjusted so as to minimize flicker and maximum contrast on each module.

c. Recommended Capacitance Values of External Capacitor

The recommended capacitance values of the external capacitor are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

Pin name	Recommended value of capacitors (µF)	Withstanding voltage (V)
AVDD	1 to 4.7	10 or more
VGH	1 to 4.7	10 or more
VGL	1 to 4.7	10 or more
V1(+), V2(-)	1 to 4.7	10 or more
V3(-), V4(+)	1 to 4.7	10 or more
V5(+), V6(-)	1 to 4.7	10 or more
V7(-), V8(+)	1 to 4.7	10 or more

d. Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current		19.5	20	20.5	mA	
LED voltage	V_L		10.8	12	V	
LED Life Time	L_L	10000			Hr	Note 1,2

Note 1 : Ta. = 25℃, I_L = 20mA
Note 2 : Brightness to be decreased to 50% of the initial value.

4. AC Timing

a. UPS051 timing specifications (refer to Fig. 1, Fig. 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	11.29(*)	12.95	13.59	MHz	
HSYNC	Period	t_H	768	823	864	DCLK	Note 1
	Display period	t_{hdisp}	640			DCLK	
	Blanking	t_{hblk}	25	30	121	DCLK	
	Front porch	t_{hfp}	103	153	—	DCLK	
	Pulse width	t_{hsw}	1	1	t_{hblk} -1	DCLK	
VSYNC	Period	t_V	245	262.5	265	t_H	Note 2
	Display period	t_{vdisp}	240			t_H	
	Blanking	t_{vblk}	3	21	31	t_H	
	Pulse width	t_{vsw}	1 DCLK	1 DCLK	t_{vblk} – 1DCLK		
Data set-up time		t_{ds}	12			ns	
Data hold time		t_{dh}	12			ns	
Vsync-to-Hsync set-up time		t_{vhs}	1			DCLK	

(*) when t_V =245 t_H

Note 1: UPS051 Horizontal blanking time (t_{hblk}) is adjustable by setting register HBLK; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: UPS051 Vertical blanking time (t_{vblk}) is adjustable by setting register VBLK. UPS051 accepts odd-field-only or even-field-only vertical input format.

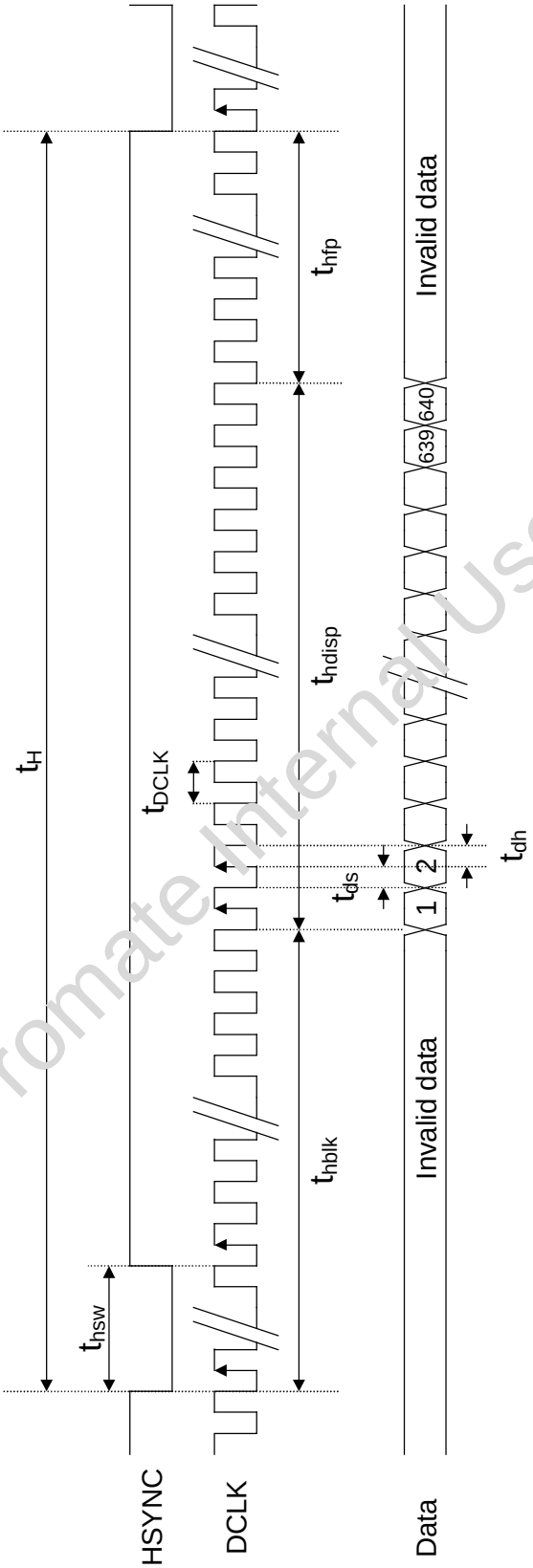


Fig.1 UPS051 Input Horizontal Signal

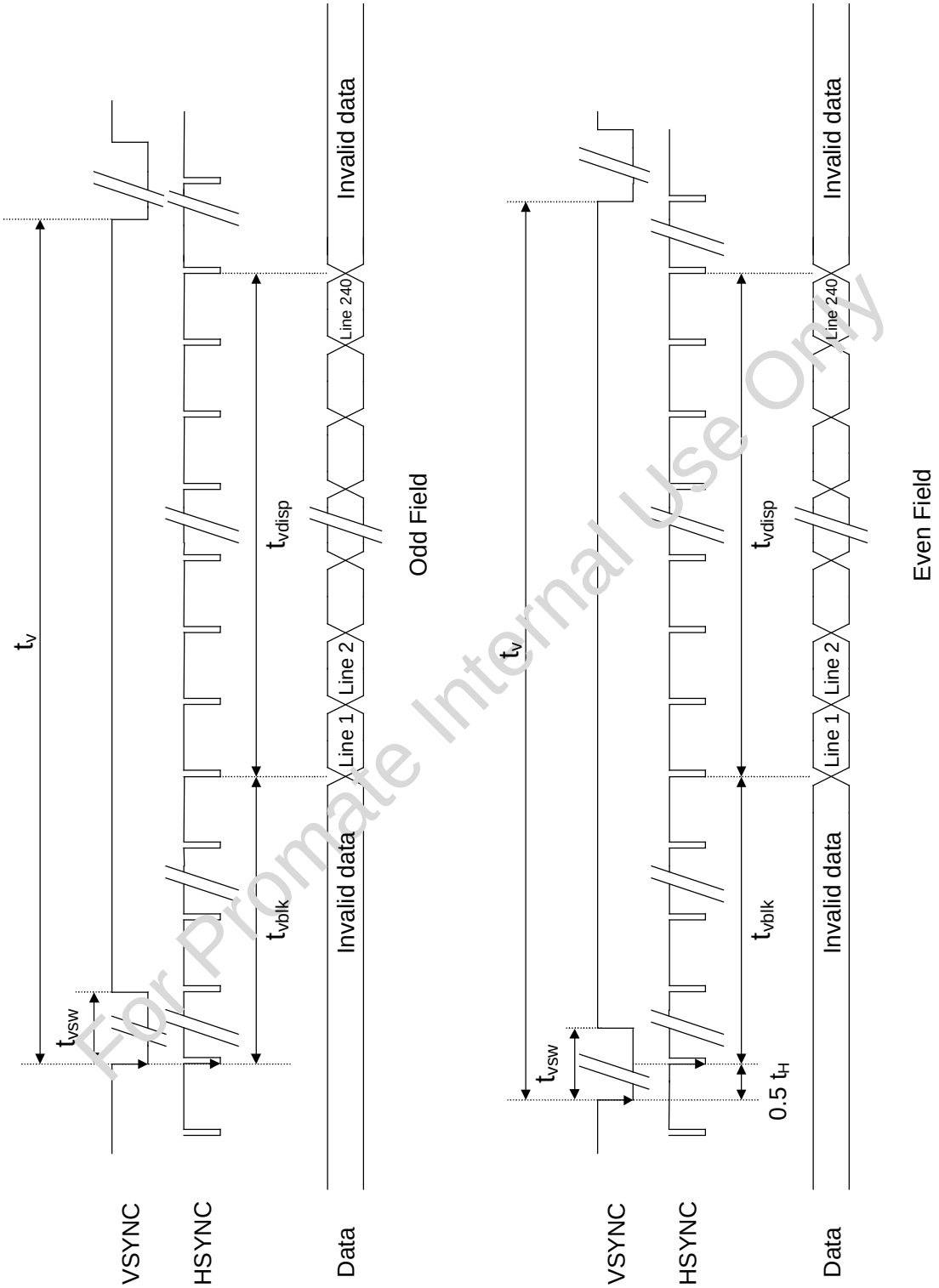


Fig.2 UPS051 Input Vertical Signal

b - 1. UPS052 (320 mode/NTSC/24.545MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	24	24.545	27	MHz	
HSYNC	Period	t_H	1540	1560	1660	DCLK	
	Display period	t_{hdisp}	1280			DCLK	
	Blanking	t_{hblk}	241			DCLK	
	Pulse width	t_{hsw}	1	1	96	DCLK	
VSYNC	Period	t_V	262	262.5	265	t_H	
	Display period	t_{vdisp}	240			t_H	
	Blanking	t_{vblk}	21			t_H	
	Pulse width	t_{vsw}	1 DCLK	1 DCLK	6 t_H		

b - 2. UPS052 (320 mode/PAL/24.375MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	24	24.375	27	MHz	
HSYNC	Period	t_H	1540	1560	1660	DCLK	
	Display period	t_{hdisp}	1280			DCLK	
	Blanking	t_{hblk}	241			DCLK	
	Pulse width	t_{hsw}	1	1	96	DCLK	
VSYNC	Period	t_V	312	312.5	315	t_H	
	Display period	t_{vdisp}	288			t_H	
	Blanking	t_{vbp}	24			t_H	
	Pulse width	t_{vsw}	1 DCLK	1 DCLK	6 t_H		

c - 1. UPS052 (352 mode/NTSC/27MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$		27		MHz	
HSYNC	Period	t_H		1716		DCLK	
	Display period	t_{hdisp}	1408			DCLK	
	Blanking	t_{hblk}	241			DCLK	
	Pulse width	t_{hsw}	1	1	96	DCLK	
VSYNC	Period	t_V	262	262.5	265	t_H	
	Display period	t_{vdisp}	240			t_H	
	Blanking	t_{vblk}	21			t_H	
	Pulse width	t_{vsw}	1 DCLK	1 DCLK	6 t_H		

c - 2. UPS052 (352 mode/PAL/27MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$		27		MHz	
HSYNC	Period	t_H		1728		DCLK	
	Display period	t_{hdisp}		1408		DCLK	
	Blanking	t_{hblk}		241		DCLK	
	Pulse width	t_{hsw}	1	1	96	DCLK	
VSYNC	Period	t_V	312	312.5	315	t_H	
	Display period	t_{vdisp}		288		t_H	
	Blanking	t_{vbp}		24		t_H	
	Pulse width	t_{vsw}	1 DCLK	1 DCLK	6 t_H		

d - 1. UPS052 (360 mode/NTSC/27MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$		27		MHz	
HSYNC	Period	t_H		1716		DCLK	
	Display period	t_{hdisp}		1440		DCLK	
	Blanking	t_{hblk}		241		DCLK	
	Pulse width	t_{hsw}	1	1	96	DCLK	
VSYNC	Period	t_V	262	262.5	265	t_H	
	Display period	t_{vdisp}		240		t_H	
	Blanking	t_{vblk}		21		t_H	
	Pulse width	t_{vsw}	1 DCLK	1 DCLK	6 t_H		

d - 2. UPS052 (360 mode/PAL/27MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$		27		MHz	
HSYNC	Period	t_H		1728		DCLK	
	Display period	t_{hdisp}		1440		DCLK	
	Blanking	t_{hblk}		241		DCLK	
	Pulse width	t_{hsw}	1	1	96	DCLK	
VSYNC	Period	t_V	312	312.5	315	t_H	
	Display period	t_{vdisp}		288		t_H	
	Blanking	t_{vbp}		24		t_H	
	Pulse width	t_{vsw}	1 DCLK	1 DCLK	6 t_H		

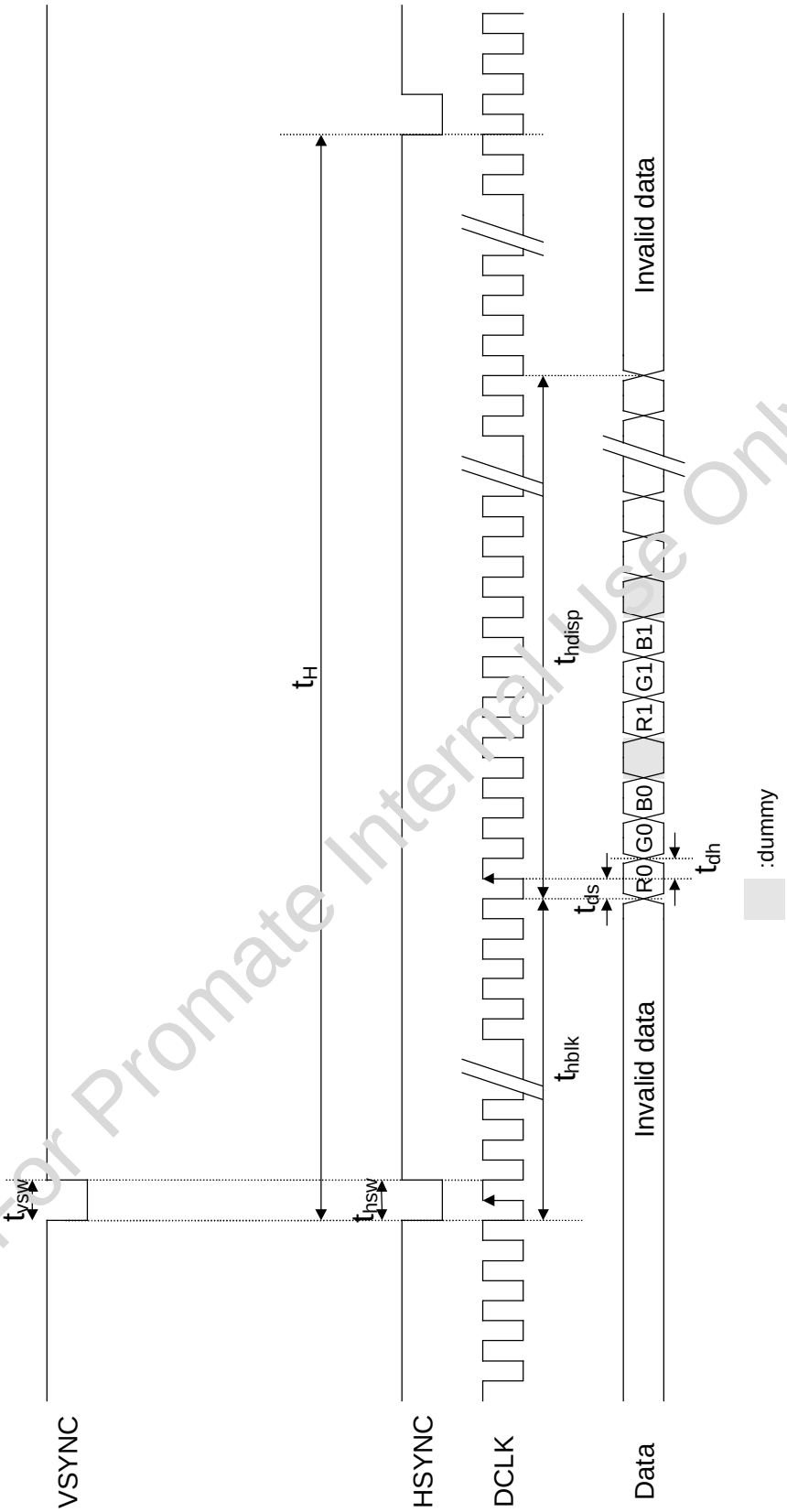


Fig. 3 UPS052 Input Horizontal Signal

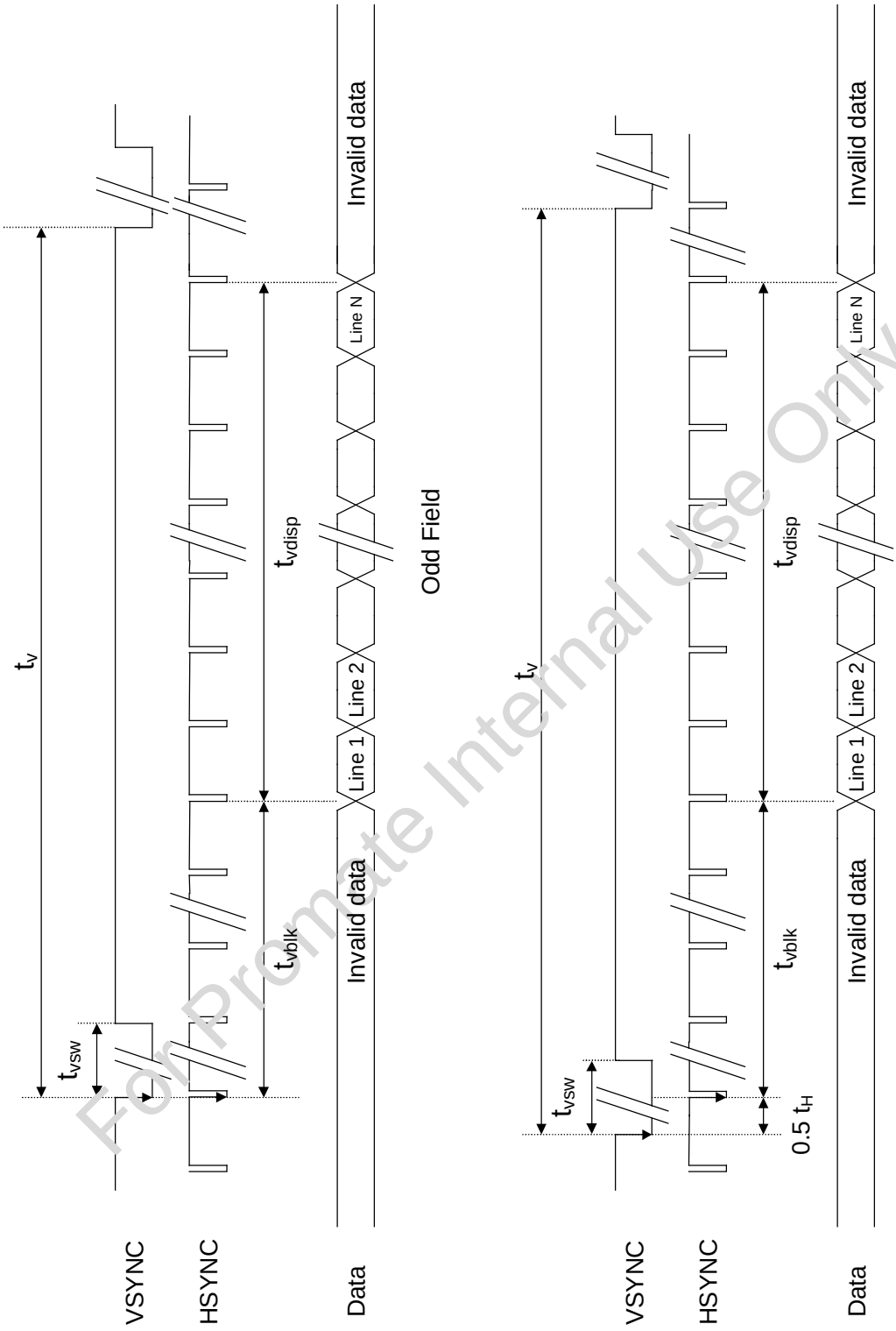


Fig.4 UPS052 Input Vertical Signal

5. Serial Control Interface

a. Input timing specifications (refer to Fig. 5)

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Serial load input setup time	t_{s0}	150			ns	
Serial load input hold time	t_{h0}	150			ns	
Serial data input setup time	t_{s1}	150			ns	
Serial data input hold time	t_{h1}	150			ns	
SCL pulse width	t_{w1L}	210			ns	
	t_{w1H}	210			ns	
CS pulse width	t_{s0}	1			µs	

b. Serial setting map

No	Test				Register Address				Register Data (Default setting)							
	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
R0	0	×	×	×	0	0	0	0	×	×	×	×	×	VCOM_AC (011)		
R1	0	×	×	×	0	0	0	1	×	FLK (0)	VCOM_DC (20h)					
R2	0	×	×	×	0	0	1	0	×	×	×	×	CONTRAST (0100)			
R3	0	×	×	×	0	0	1	1	BRIGHT (40h)							
R4	0	×	×	×	0	1	0	0	×	×	SEL (00)		NTSC/PAL (10)		VDIR (1)	HDIR (1)
R5	0	×	×	×	0	1	0	1	×	GRB (1)	PWMM (1)	PWM_DUTY (10)		SHDB2 (1)	SHDB1 (1)	STB (0)
R6	0	×	×	×	0	1	1	0	×	×	×	VBLK (15h)				
R7	0	×	×	×	0	1	1	1	HBLK (1Eh)							
R8	0	×	×	×	1	0	0	0	×	×	×	×	×	PSL (000)		
R9	0	×	×	×	1	0	0	1	×	×	×	×	×	CP1_FREQ (001)		
R10	0	×	×	×	1	0	1	0	×	×	CP3_FREQ (001)			CP2_FREQ (001)		
R11	0	×	×	×	1	0	1	1	×	×	×	×	×	OP (000)		

× : Dummy bit

c. Description of Serial Control Operations

- Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL
- Command loading operation starts from the falling edge of CS and is completed at the next rising edge
- The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid. Please refer to Fig. 6.
- If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
- If 16 bits or more of SCL are input while CS is low, the first 16 bits of transferred data before

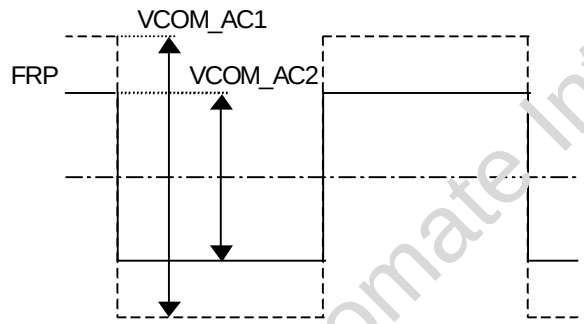
the rising edge of CS pulse are valid data.

- Serial block operates with the SCL clock and serial data can be accepted in the power save mode

d. Description of serial control data

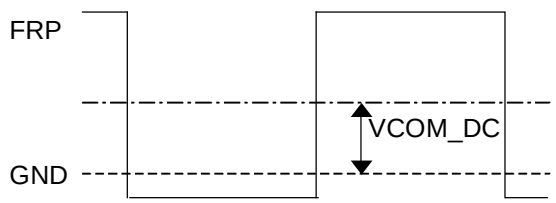
(1) VCOM_AC: Common voltage AC level selection; 3 bit setting, 0.2V / LSB (deviation ±4%)

(MSB – LSB)	VCOM AC LEVEL	UNIT
000	5.0	V
001	5.2	
010	5.4	
011	5.6 (Default)	
100	5.8	
101	6.0	
110	6.2	
111	6.4	



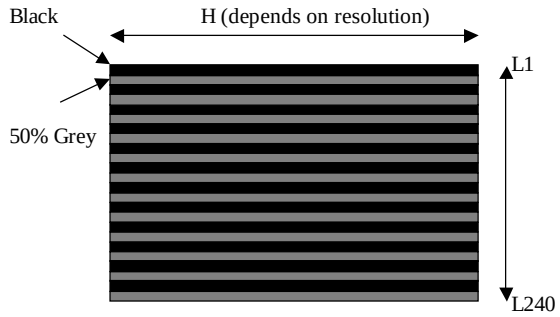
(2) VCOM_DC : Common voltage DC level selection; 6 bit setting, 27.8mV / LSB

(MSB – LSB)	VCOM AC LEVEL	UNIT
00h	1.75	V
20h	0.86(Default)	
3Fh	0	



(3) FLK : flicker pattern output

FLK	Function
0	Normal operation (Default)
1	Flicker patttern output



(4) CONTRAST : RGB contrast level setting; 4-bit setting

(MSB-LSB)	Function
0000	Low contrast
0100	Center (Default)
1111	High contrast

(5) BRIGHTNESS : RGB bright level setting; 8-bit setting

(MSB-LSB)	Function
00h	Dark
40h	Center (Default)
FFh	Bright

(6) HDIR : Horizontal scan direction setting

HDIR	Function
0	Right-to-left scan
1	Left-to-right scan (Default)

(7) VDIR : Vertical scan direction setting

VDIR	Function
0	Down-to-up scan
1	Up-to-down scan (Default)

(8) NTSC/PAL : NTSC or PAL mode selection (for UPS052 input timing)

(MSB-LSB)	Function
00	PAL mode
01	NTSC mode
10	Auto-detection mode (Default)
11	

(9) SEL : Input data timing format selection; please refer to AC timing section for detail specifications.

(MSB-LSB)	Input Timing Format
00	UPS051 (Default)
01	UPS052: 320x240
10	UPS052: 352x240
11	UPS052: 360x240

(10) STB : Standby (power saving) mode setting

STB	Function
0	Standby mode (Default)
1	Normal operation

(11) SHDB1: Shut-down of the power boost converter for LED backlight unit

SHDB1	Function
0	The LED power converter is off
1	The LED power converter is controlled by build-in on/off sequence (Default)

(12) SHDB2: Shut-down for VGH/VGL charge pump

SHDB2	Function
0	The VGH/VGL charge pump is off
1	The VGH/VGL charge pump is controlled by build-in on/off sequence (Default)

(13) PWM_DUTY: PWM duty cycle selection for LED backlight power converter (valid when PWMM = 0)

(MSB-LSB)	PWM duty cycle
00	50%
01	60%
10	65% (Default)
11	70%

(14) PWMM: PWM mode selection

PWMM	Function
0	Mode 0: fixed duty cycle
1	Mode 1: increasing duty cycle (Default)

(15) GRB: Register reset setting

GRB	Function
0	Reset all registers to default values
1	Normal operation (Default)

(16) VBLK: Vertical blanking setting for UPS051; 5-bit setting, 1 line/LSB

(MSB-LSB)	V-blanking t_{vblk}	UNIT
00h	0	line
15h	21 (Default)	
1Fh	31	

(17) HBLK: Horizontal blanking setting for UPS051; 8-bit setting, 1 DCLK/LSB

(MSB-LSB)	H-blanking t_{hblk}	UNIT
00h	0	DCLK
1Eh	30 (Default)	
FFh	255	

(18) PSL : Panel resolution selection

(MSB-LSB)	Function
0XX	Controlled by driver IC input pins : PSL0, PSL1 (Default)
100	502 * 240 (dots)
101	640 * 240 (dots)
110	720 * 240 (dots)
111	960 * 240 (dots)

Note : “X“ is “0” or “1”

(19) CP1_FREQ : Charge pump 1 frequency setting for driver IC analog power AVDD

(MSB-LSB)	Charge Pump Frequency	UNIT
000	10	KHz
001	20 (Default)	
010	40	
011	60	
100	80	
101	120	
110	160	
111	200	

(20) CP2_FREQ : Charge pump 2 frequency setting for LCD positive power VGH

(MSB-LSB)	Charge Pump Frequency	UNIT
000	10	KHz
001	20 (Default)	
010	40	
011	60	
100	80	
101	120	
110	160	
111	200	

(21) CP3_FREQ : Charge pump 3 frequency setting for LCD negative power VGL

(MSB-LSB)	Charge Pump Frequency	UNIT
000	10	KHz
001	20 (Default)	
010	40	
011	60	
100	80	
101	120	
110	160	
111	200	

(22) OP : DAC output driving capability selection

(MSB-LSB)	Function
0XX	Controlled by driver IC input pins : OP0, OP1 (Default)
100	-25%
101	Normal
110	+25%
111	+50%

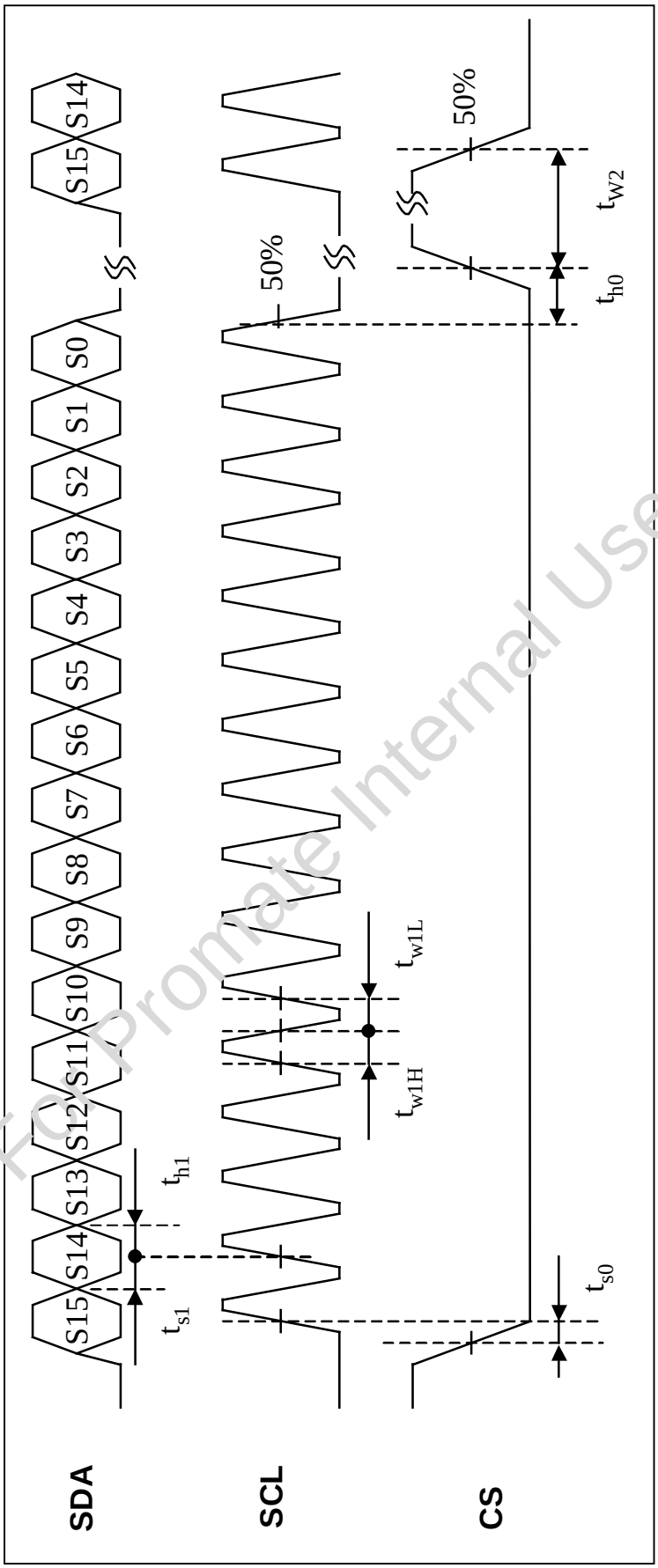


Fig. 5 Serial Control Timing

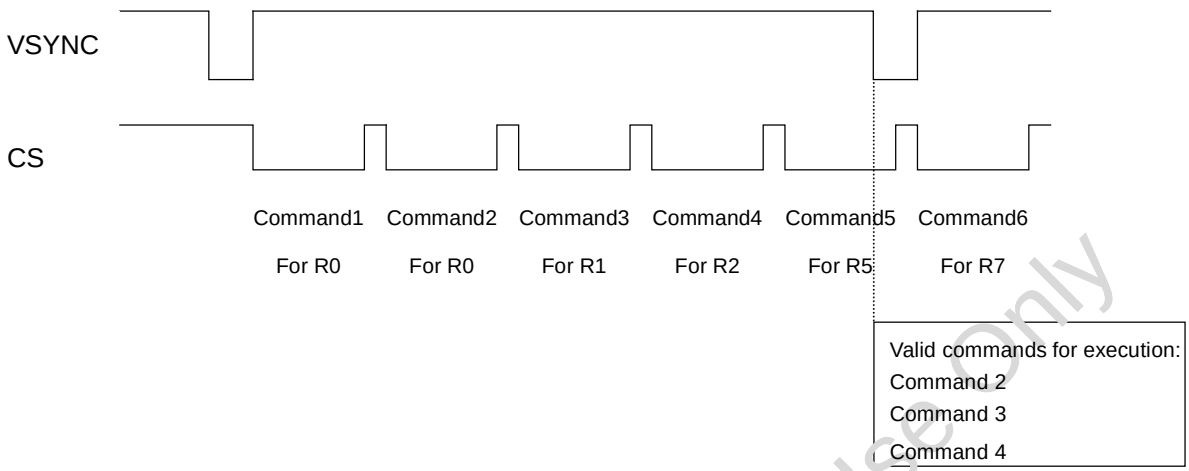


Fig. 6 Example of Serial Command Operation

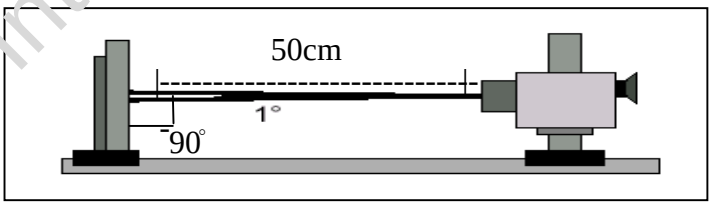
C. Optical specifications (Note 1,Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time Rise Fall	 Tr Tf	θ =0°	 - -	 15 20	 25 30	 ms ms	Note 4
Contrast ratio	CR	At optimized viewing angle	120	200	-		Note 5,6
Viewing angle Top Bottom Left Right		CR≧10	 10 30 40 40	 - - - -	 - - - -	 deg.	Note 7
Brightness	Y_L	θ =0°	200	240	-	nits	Note 8
White chromaticity	X	θ =0°	0.27	0.31	0.35		
	y	θ =0°	0.29	0.35	0.40		
Backlight Luminance Uniformity			60			%	

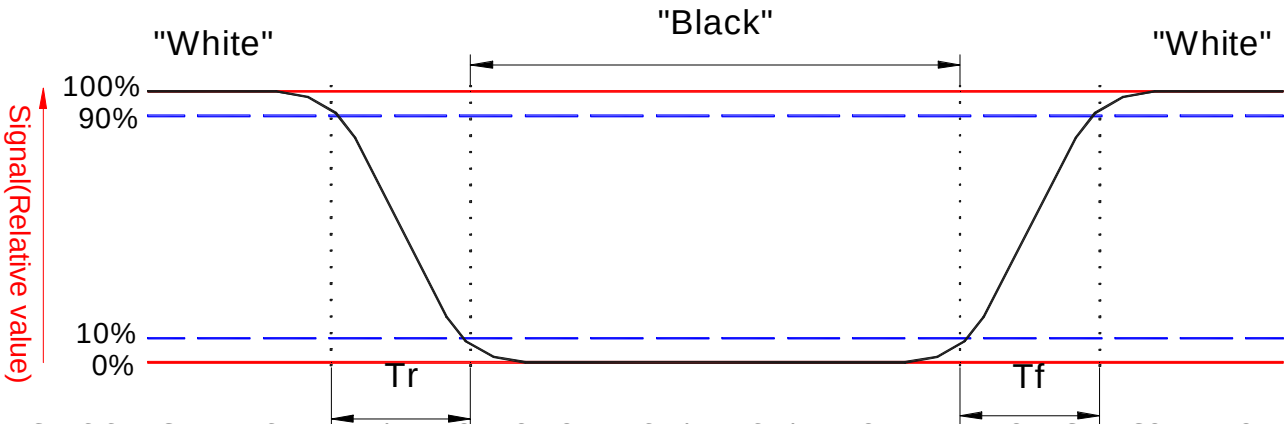
Note 1. Ambient temperature =25℃. And backlight current I_L=20 mA

Note 2. To be measured in the dark room.

Note 3. To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation, distance: 450±50mm.



Note 4. Definition of response time: The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.
The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. White Vi=$V_{i50} \pm$ 1.5V

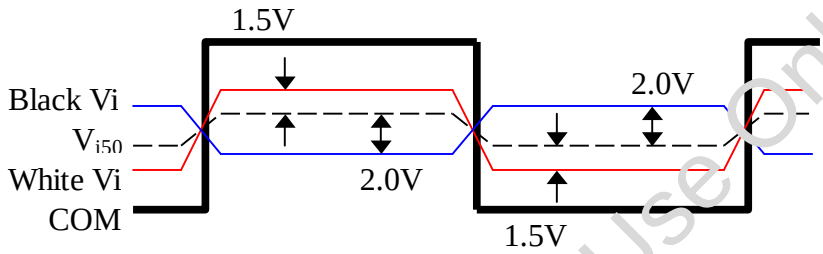
Black Vi=$V_{i50} \mp$ 2.0V

“$\pm$” Means that the analog input signal swings in phase with COM signal.

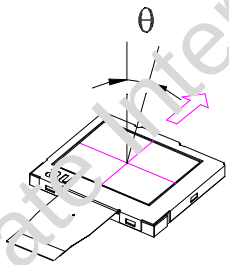
“$\mp$” Means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.



Note 7. Definition of viewing angle:



Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

D. Reliability test items:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80℃ 240Hrs	
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note: Ta: Ambient temperature.

E. Outline dimension

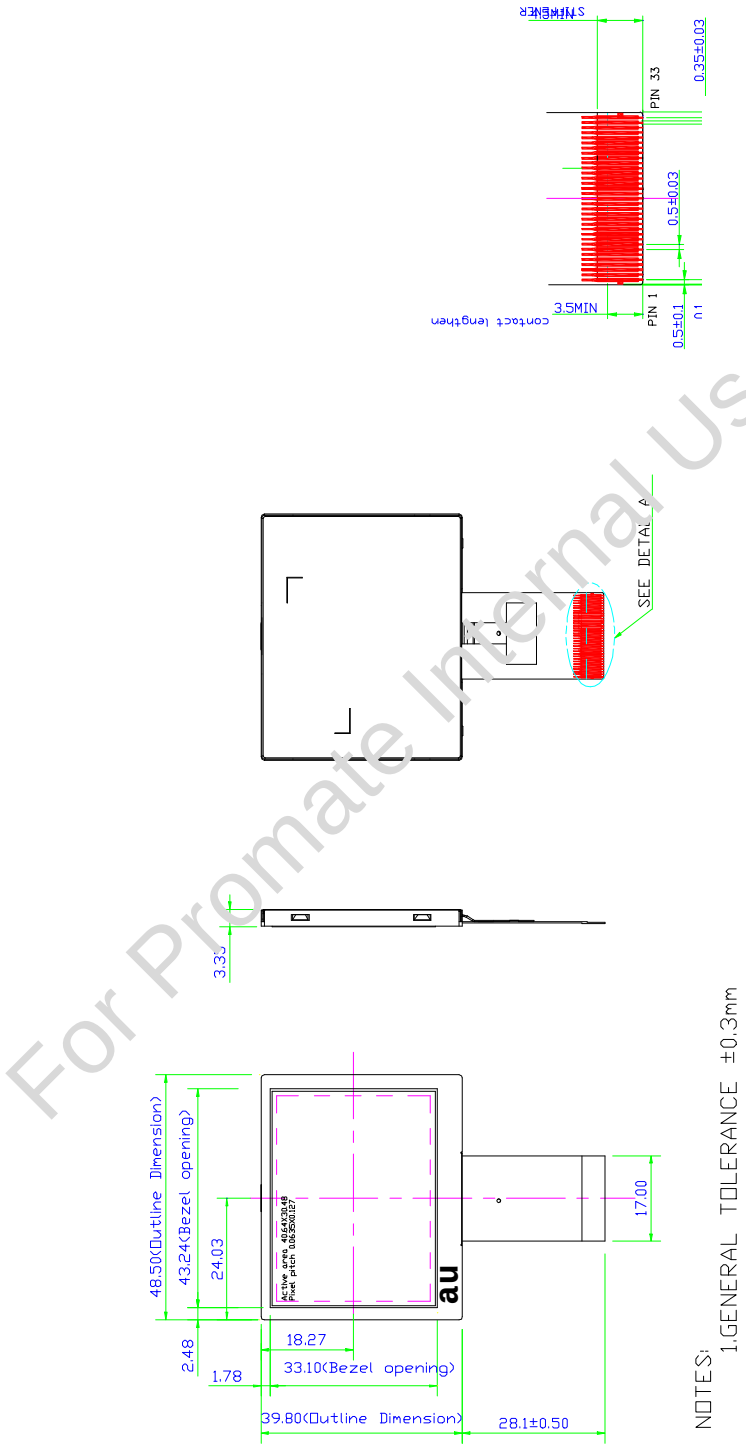
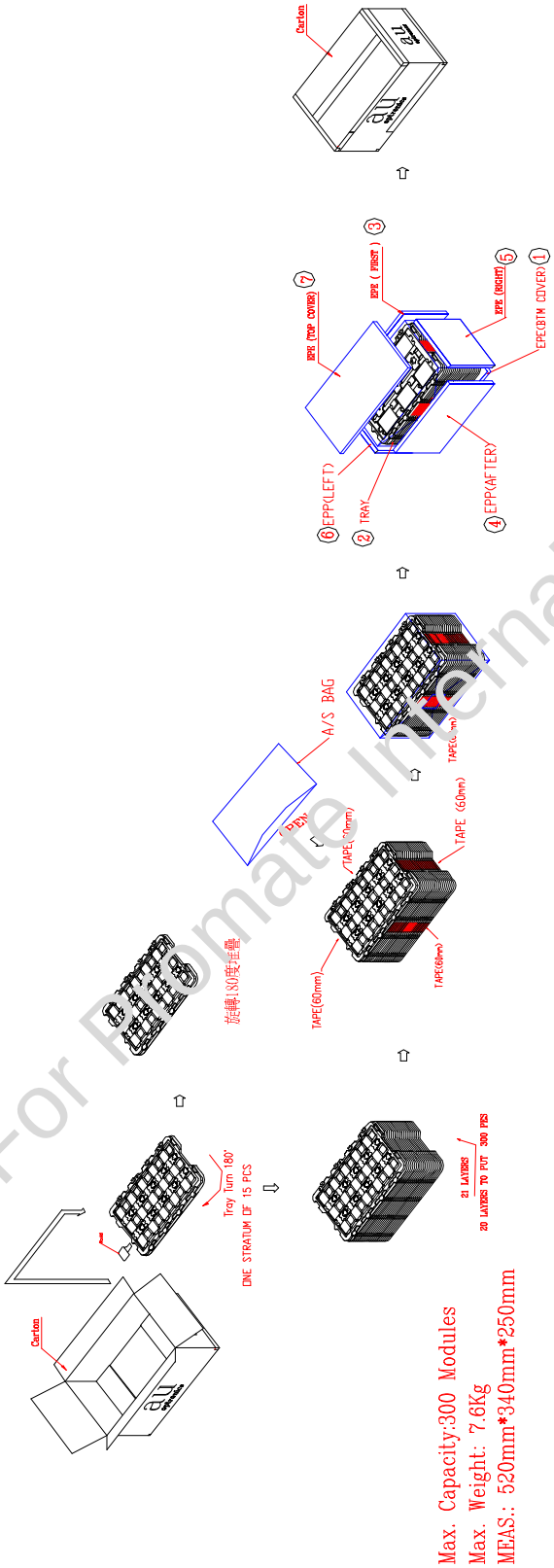


Fig.7 Outline dimension of TFT-LCD module

F. Packing form



G. Application Notes

This LTPS TFT LCD module is designed for digital still camera application. A COG type LCD driver IC is integrated within this module, makes it much easier to design and cost-effective. The main features of integrated driver are:

- Accepting digital serial R, G, B 8-bit signal, fewer adjustment, fewer design effort, and lower power consumption compared to other analog LTPS solution.
- Integrated timing controller for UPS051 and UPS052 input timing formats. For UPS052 input timing, the input signal is always the same for different panel resolution.
- Integrated LED power converter controller, DC-DC charge pump, and Vcom driver. A design requires less peripheral components and reduces the total system cost.

1. Input Data Timing

Two kinds of input timing format are supported: UPS051 and UPS052. In UPS051 input format, the conversion of image data to display dots is controled by the user. In UPS052 input format, the mapping of incoming data to display dots is take cared by built in scaling function of driver IC.

For UPS051 timing, the module accpet one dot video data at the rising edge of DCLK, and display them one dot by one dot. Therefore the input data timing is different according to different panel resolutions and scan directions. Refer to the AC Timing of UPS051 part, you can use the typ. value for a typical case, or you can use the min. value to lower down the power consumption and EMI.

Because of delta color filter arrangement, the RGB data sequence for even and odd lines are different based on scan direction. For the definition of even and odd lines, see Fig. 8.

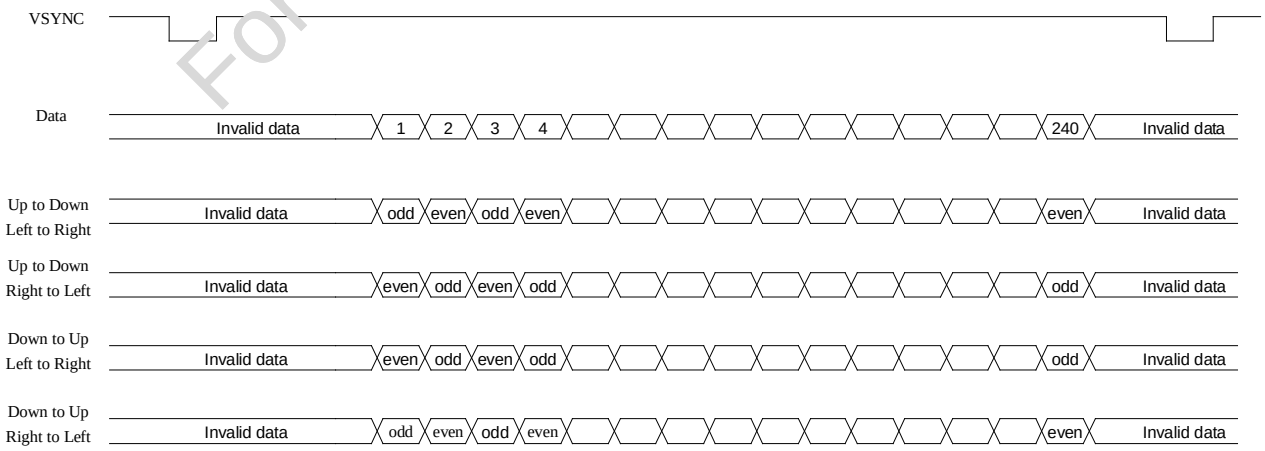


Fig 8. UPS051 even and odd lines definition

For the RGB sequence, see Fig. 9.

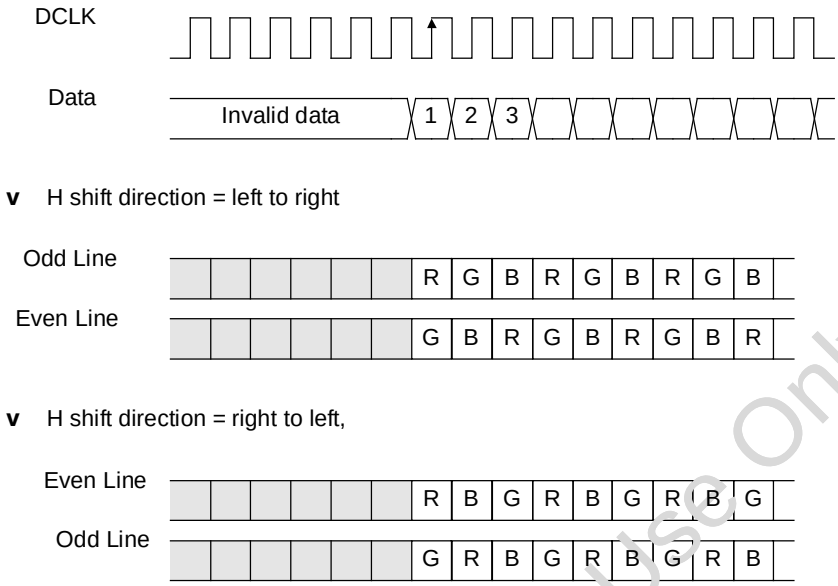


Fig. 9 UPS051 Input RGB sequence

For the color filter arrangement, see Fig. 10.

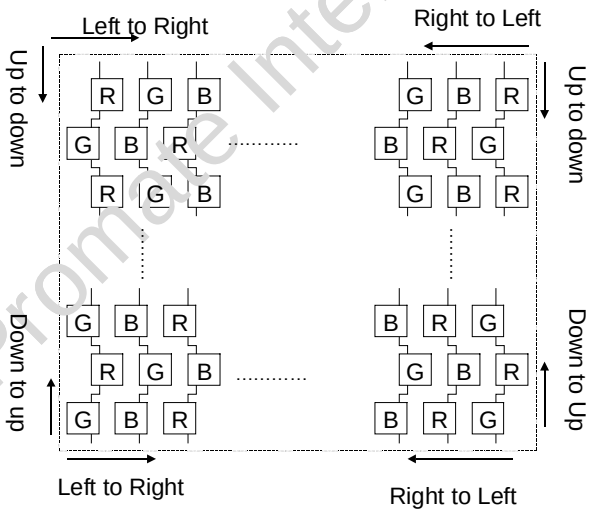


Fig. 10 Color filter arrangement

For UPS052 timing, there are three input RGB data modes to choose from: 320xRGB, 352xRGB, and 360xRGB. Input data is processed and mapped to display dots by integrated driver IC according to panel resolution and scan direction settings. UPS052 input format saves the effort of data scaling for users and keeps a consistent interface for different display resolutions, in the cost of higher input data rate and less image processing elasticity. An additional NTSC/PAL auto-detection function is provided for UPS052 input format. When the function is active, the HSYNC and VSYNC inputs are monitored. If there are more than

288 HSYNC in a VSYNC period, it is detected as the PAL mode (288 active lines). On the other hand, if there are less than 288 HSYNC in a VSYNC period, it is asserted as the NTSC mode (240 active lines). Please refer to the serial control setting for more details.

For vertical input timing, both UPS051 and UPS052 accept odd / even field switching or single field only input. For detail timing spec., please refer to Fig 2 and Fig 4.

2. Typical Application Circuit

The integrated driver IC provides build-in LED booster controller, DC-DC charge pump, and Vcom driver. See Fig. 11 for the application circuit.

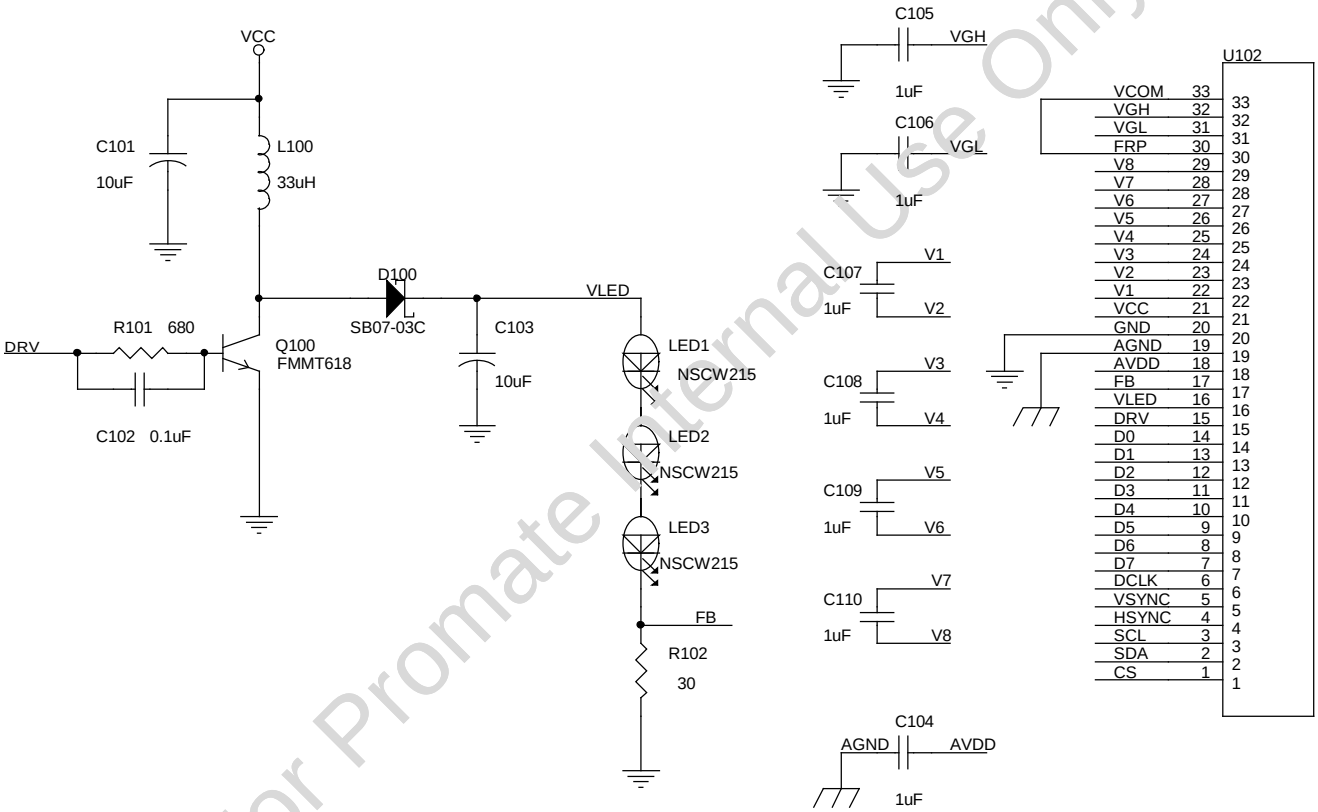


Fig.11 Typical Application Circuit

A single 3.3V power supply (VCC) is required to provide driver IC power and generate all necessary voltages for LCD related circuits.

According to Fig. 11, the L100, Q100, D100,and C103 together form the LED boost converter. The converter with 0.6V feedback (FB) and R102 provide a constant 20mA current for LED backlight unit. The boost converter switching signal DRV is generated base on divided frequency of DCLK. Therefore the DCLK input is required for LED driver operation, and the absent of DCLK signal during normal operation will set the driver IC into standby mode. A low ESR capacitor for C103 is recommended in order to reduce voltage ripple of

VLED. The build-in LED boost controller is default active, and it is able to be turned off by setting the register SHDB1 to low.

The positive (VGH) and negtive (VGL) power supplies for LCD are generated through build-in DC-DC charge pump circuit, an elegant design with only seven passive power-setting capacitors are required.

The build-in VCOM driver provides programmable amplitude and DC-level adjustments through serial control interface to optimize image contrast and minimize flicker. Optional external VCOM DC-level adjustment is achievable through FRP output pin and VCOM input pin, please refer to Fig. 12.

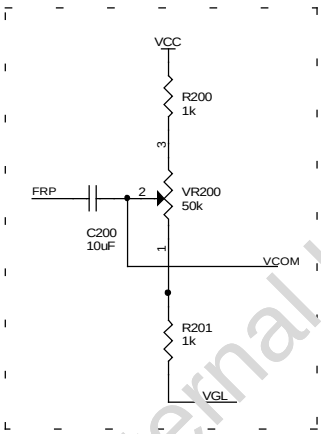


Fig.12 VCOM-DC External Adjustment Circuit

3. Power ON/OFF Sequence

After VCC power on reset, VSYNC/HSYNC/DCLK/DATA can be input, and serial control interface is also operational. The LCD driver is in default standby mode after VCC power-on, and setting register STB to high to disable the standby mode is required for normal operation. When the standby mode is disabled, a build-in power on sequence is started. The driver IC analog power AVDD is turned on first, and then the LCD positive and negative power supplies VGH/VGL are pumped, and followed by the LED power VLED. Please refer to Fig.13 for the detail timing of power on/off sequence.

Since the LCD driver supports different panel resolutions, settings of output resolution and DAC driving capability are essential for proper LCD operation. The setting of output resolution is through register “PSL” and setting of DAC driving capability is register “OP”. For 2-inch 640x240 LCD: PSL[2:0] = 101, OP[2:0] = 101. It is recommended to program essential serial commands first before releasing the LCD module from default standby mode.

The DCLK signal is required for normal operation. When DCLK < 140KHz during normal operation, the driver will be operated in standby mode, and LED power converter will be turned off. A standby disabling is required after the DCLK signal is recovered.

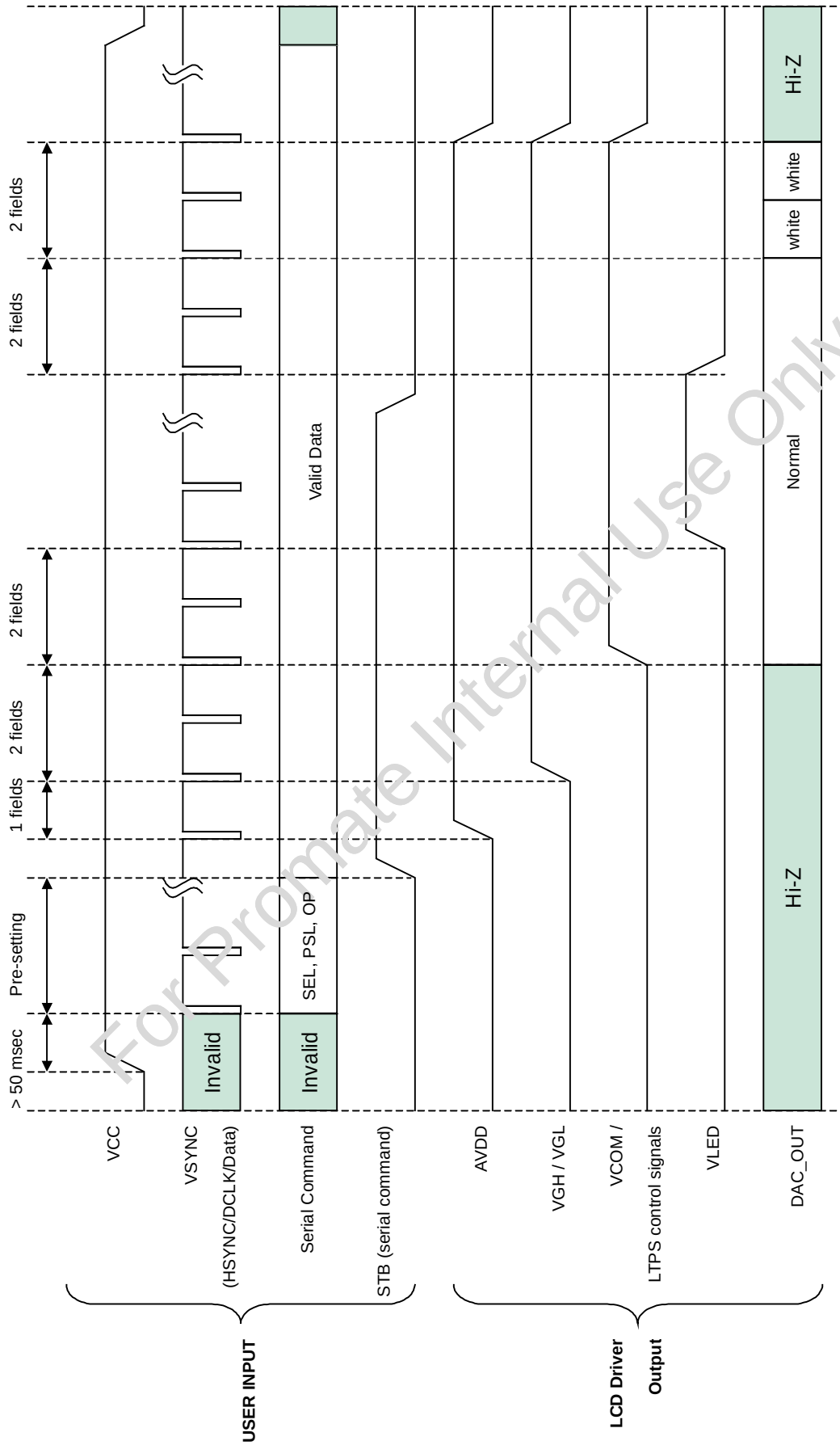


Fig.13 Power ON / OFF Sequence