(V) Preliminary Specification

( ) Final Specification

Module	32.0" Color TFT-LCD
Model Name	M320DAN02.2

Customer	Date

Approved by

Approved by	Date
CH Lin	Aug. 13, 2019

Prepared by	Date
Alan Wu	Aug. 13, 2019

Note: This Specification is subject to change without notice.

AU Optronics corporation

Contents

Record of Revision

Version	Date	Page	Old description	New Description	
0.0	2019/7/19	All	First preliminary version release.	-	

1 Handling Precautions

1) Since polarizer is easily damaged, do not touch or press the surface of polorizer with hand.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.

7) Do not open or modify the Module Assembly.

8) Do not press the reflector sheet at the back of the module to any directions.

9) In case a TFT-LCD Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lightbar edge. Otherwise the TFT-LCD Module may be damaged.

10) Insert or pull out the interface connector, be sure not to rotate nor tilt it of the TFT-LCD Module.

11) Do not twist nor bend the TFT -LCD Module even momentary. It should be taken into consideration that no bending/twisting forces are applied to the TFT-LCD Module from outside. Otherwise the TFT-LCD Module may be damaged.

12) Please avoid touching COF position while you are doing mechanical design.

13) When storing modules as spares for a long time, the following precaution is necessary: Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.

14) Do not apply the same pattern for a long time, it will enhance relevant defect.

15) When this reverse-type model(PCBA on bottom side) is used as forward-type model(PCBA on top side) , AUO can not guarantee any defects of LCM .

2 General Description

This specification applies to the 32.0 inch wide Color a-Si TFT-LCD Module M320DAN02.2. The display supports the QHD – 2,560(H) x 1,440(V) screen format and 1.07B colors (RGB 8bits + Hi-FRC). The input interface is 4-lanes eDP and this module doesn't contain an driver board for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	812.9 (32.0")
Active Area	[mm]	708.48 (H) x 398.52 (V)
Pixels H x V	-	2,560 (x3) x 1,440
Pixel Pitch	[um]	276.75 (per one triad) × 276.75
Pixel Arrangement	-	R.G.B. Vertical Stripe
Display Mode	-	AHVA Mode (Advances Hyper-Viewing Angle),Normally Black
White Luminance (Center of screen)	[cd/m2]	TBD
HDR White Luminance (Center of screen)	[cd/m2]	440 (Typ.)
HDR PEAK White Luminance (Center of screen)		600 (Min.)
Contrast Ratio	-	1,000 : 1 (Typ.)
Response Time	[msec]	5 (Typ., Gray to Gray)
Power Consumption (LCD Module + BLU)	[Watt]	45.36W (Typ.) LCD module : PDD(Typ.)=TBD@white pattern,60Hz,12V Backlight unit : PBLU (Typ.) =36.5W @Is=50mA
HDR PEAK Power Consumption (LCD Module + BLU)	[Watt]	64.46 (Typ.) LCD module : PDD(Typ.)=TBD@white pattern,60Hz,12V Backlight unit : PBLU (Typ.) =71.7W @Is=95mA
Weight	[Grams]	3,900 (Typ.) / 4,095 (Max.)
Outline Dimension	[mm]	721.68 (H) x 417.9 (V) × 16.57 (D) (Typ.)
Electrical Interface	-	4-lanes eDP

Support Color	-	1.07B colors (RGB 8bits + Hi-FRC)
Surface Treatment	-	Anti-Glare, 3H, Haze 25%

Temperature Range
   Operating
   Storage (Shipping)
	[℃]
	[℃]
		0 to +50
		-20 to +60

RoHS Compliance	-	RoHS Compliance
TCO Compliance	-	NA

2.2 Absolute Maximum Rating of Environment

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	*Note 2-1*
TGS	Glass surface temperature (operation)	0	+68	[°C]	*Note 2-1* *Function judged only*
HOP	Operation Humidity	5	90	[%RH]	*Note 2-1*
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-1: Temperature and relative humidity range are shown as the below figure.

    1. 90% RH Max (Ta ≦39℃)

    2. Max wet-bulb temperature at 39℃ or less. (Ta ≦39℃)

    3. No condensation
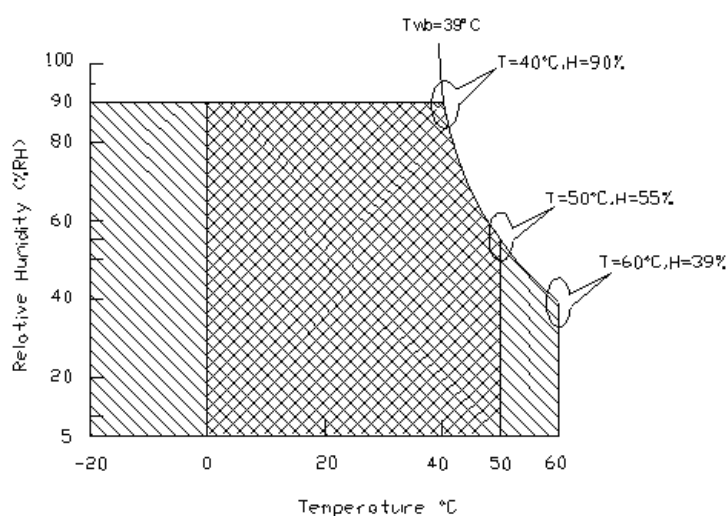
Operating Range   Storage Range

2.3 Optical Characteristics

The optical characteristics are measured on the following test condition.

Test Condition:

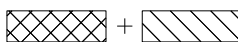1. Equipment setup: Please refer to *Note 2-2*.

2. Panel Lighting time: 30 minutes

3. VDD=12.0V, Fv=60Hz, Ta=25℃

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
L_W	White Luminance (Center of screen)		TBD	TBD	-	[cd/m2]	*Note 2-3* *By SR-3*
L_{WH}	HDR White Luminance (Center of screen)		350	440	-	[cd/m2]	*Note 2-4* *By SR-3*
L_{WP}	HDR PEAK White Luminance (Center of screen)		600	-	-	[cd/m2]	*Note 2-5* *By SR-3*
L_{uni}	Luminance Uniformity (9 points)		75	80	-	[%]	*Note 2-6* *By SR-3*
CR	Contrast Ratio (Center of screen)		600	1000	-	-	*Note 2-7* *By SR-3*
θ_R	Horizontal Viewing Angle (CR=5)	Right	75	89	-	[degree]	*Note 2-8* *By SR-3*
θ_L		Left	75	89	-		
Φ_H	Vertical Viewing Angle (CR=5)	Up	75	89	-		
Φ_L		Down	75	89	-		
T_{GTG}	Response Time	Gray to Gray	-	5	-		*Note 2-9* *By TRD-100*
R_x	Color Coordinates (CIE 1931)	Red x	TBD	TBD	TBD	-	*By SR-3*
R_y		Red y	TBD	TBD	TBD		
G_x		Green x	TBD	TBD	TBD		
G_y		Green y	TBD	TBD	TBD		
B_x		Blue x	TBD	TBD	TBD		
B_y		Blue y	TBD	TBD	TBD		
W_x		White x	0.283	0.313	0.343		
W_y		White y	0.299	0.329	0.359		
Ru'	Color Coordinates (CIE 1976)	Red u'	-	TBD	-	-	*By SR-3*
Rv'		Red v'	-	TBD	-		
Gu'		Green u'	-	TBD	-		

Gv'		Green v'	-	TBD	-			
Bu'		Blue u'	-	TBD	-			
Bv'		Blue v'	-	TBD	-			
Wu'		White u'	-	0.198	-			
Wv'		White v'	-	0.468	-			
DCIP3 coverage ratio (CIE1976)				95		[%]	*By SR-3*

Note 2-2: Equipment setup :
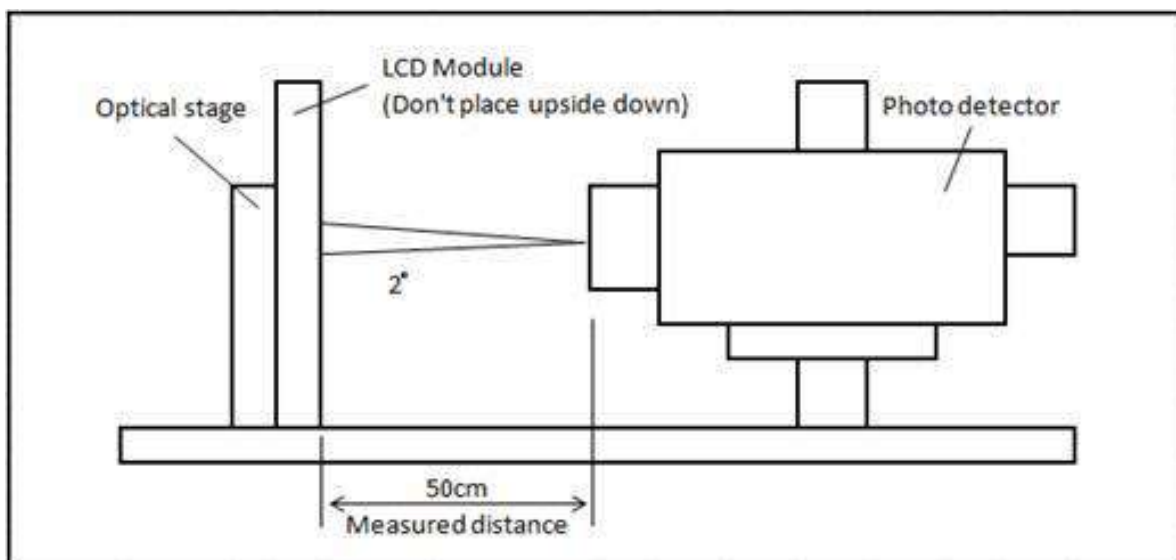
Note 2-3: LED current condition I_S=TBD mA.

Note 2-4: HDR LED current condition I_{SH}=50mA.

Note 2-5: HDR PEAK LED current condition I_{SP}=95mA.

Note 2-6: Luminance Uniformity Measurement

Definition:

$$Luminance\ Uniformity = \frac{Minimum\ Luminance\ of\ 9\ Points\,(P1 \sim P9)}{Maximum\ Luminance\ of\ 9\ Points\,(P1 \sim P9)}$$

a. Test pattern: White Pattern
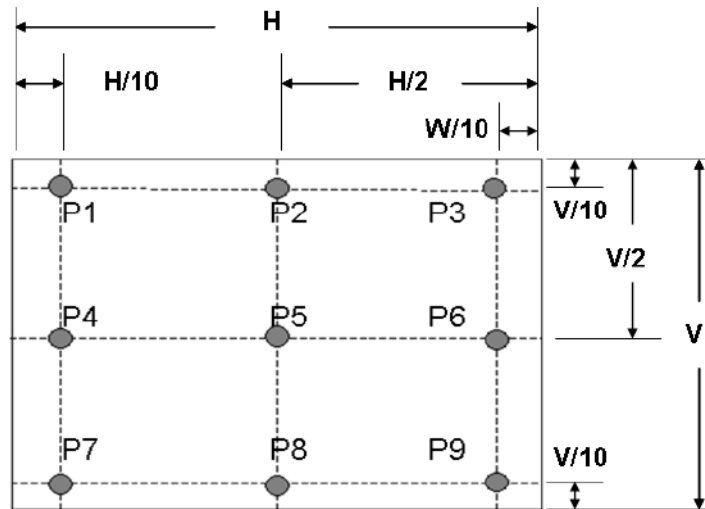
Note 2-7: Contrast Ratio Measurement

Definition:

$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

a. Measured position: Center of screen (P5) & perpendicular to the screen (θ=Φ=0°)

Note 2-8: Viewing angle measurement

Definition:

a. Horizontal view angle: Divide to left & right (θ_L & θ_R)

   Vertical view angle: Divide to up & down (Φ_H & Φ_L)

Note 2-9: Response time measurement

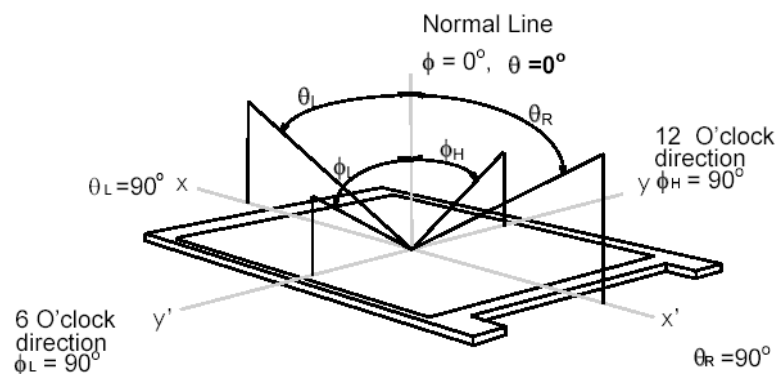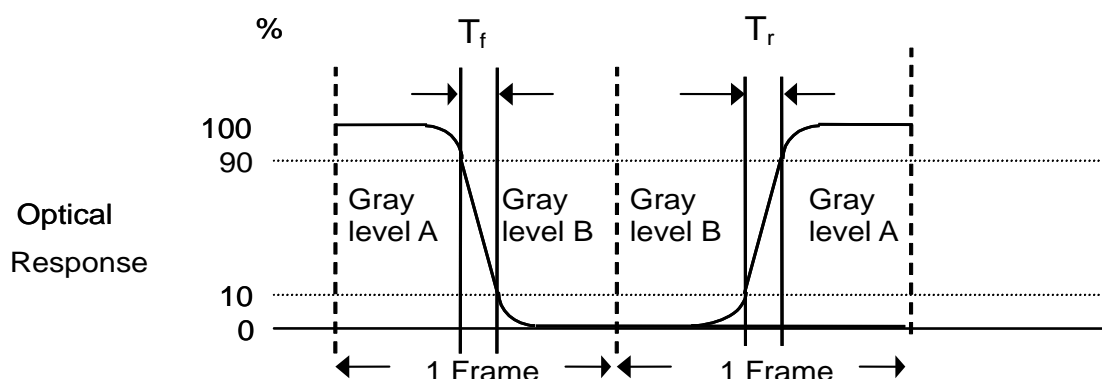The output signals of photo detector are measured when the input signals are changed from "Gray level A" to "Gray level B" (falling time, TF), and from "Gray level B" to "Gray level A" (rising time, TR), respectively. The response time is interval between the 10% and 90% of optical response.

The gray to gray response time is defined as the following table.

The gray to gray response time is defined as the following table.

Gray Level to Gray Level		Target gray level				
		L0	L63	L127	L191	L255
Start gray level	L0					
	L63					
	L127					
	L191					
	L255					

■ T_{GTG_typ} is the total average time at rising time and falling time of gray to gray.

Note 2-10 : Evaluation test and mass production inspection shall be applied with LED current I_S White Luminance condition if there is not specified condition.

2.4 Mechanical Characteristics

Symbol	Description	Min.	Max.	Unit	Remark
P_{bc}	Backside Compression	2.5	-	[Kgf]	*Note 2-11*

Note 2-11: 1. Test condition:

    (1)   Ambient illumination: 10~15lux

    (2)   Test patter: Gray (L128)

    (3)   Distance of judgment: 30cm from surface of LCD panel

    (4)   Viewing angle of judgment: Front

    (5)   Test jig: Push-pull Gauge & Flat Head (Φ2)

2. Test Method:

The point is at a distance from right-downside 25mm x 25mm defined as the Start Point of Measure Points, and the point is at a distance 25mm from left-side & around 10mm from PCB defined as the End Point.

Align 50mm x 50mm block from Start Point on the Bezel Back, and the corners of each block are Measure Points.

If the distance from the last block to each side of the End Point $\geqq$ 25mm, add other blocks to make sure that most area of Bezel Back can be measured.

    a.   Test pattern: It is listed as following.
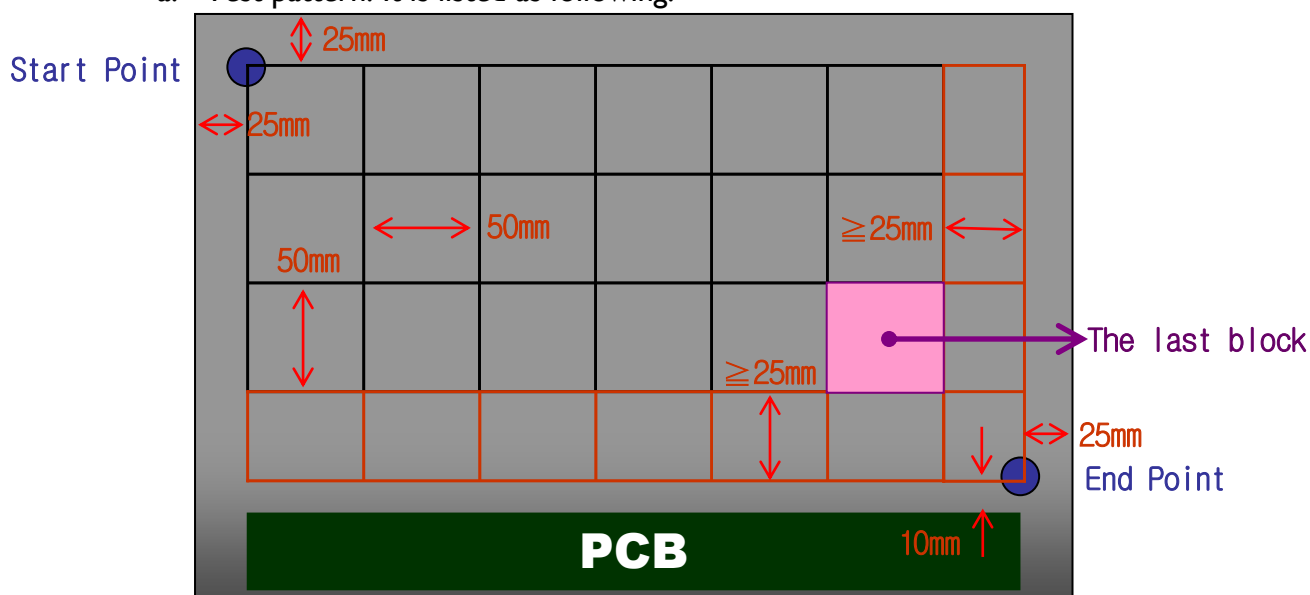
3 TFT-LCD Module

3.1 Block Diagram

The following shows the block diagram of the 32.0 inch Color TFT-LCD Module.

3.2 Interface Connection

3.2.1 Connector Type

TFT-LCD Connector	Manufacturer	JAE	P-TWO	STARCONN (CHIEF LAND)
	Part Number	FI-RTE51SZ-HF	187059-5122	115E51-0000RA-M3-R
Mating Connector	Manufacturer	JAE or Compatible		
	Part Number	FI-RE51CL (Locked Type)		

3.2.2 Connector Pin Assignment

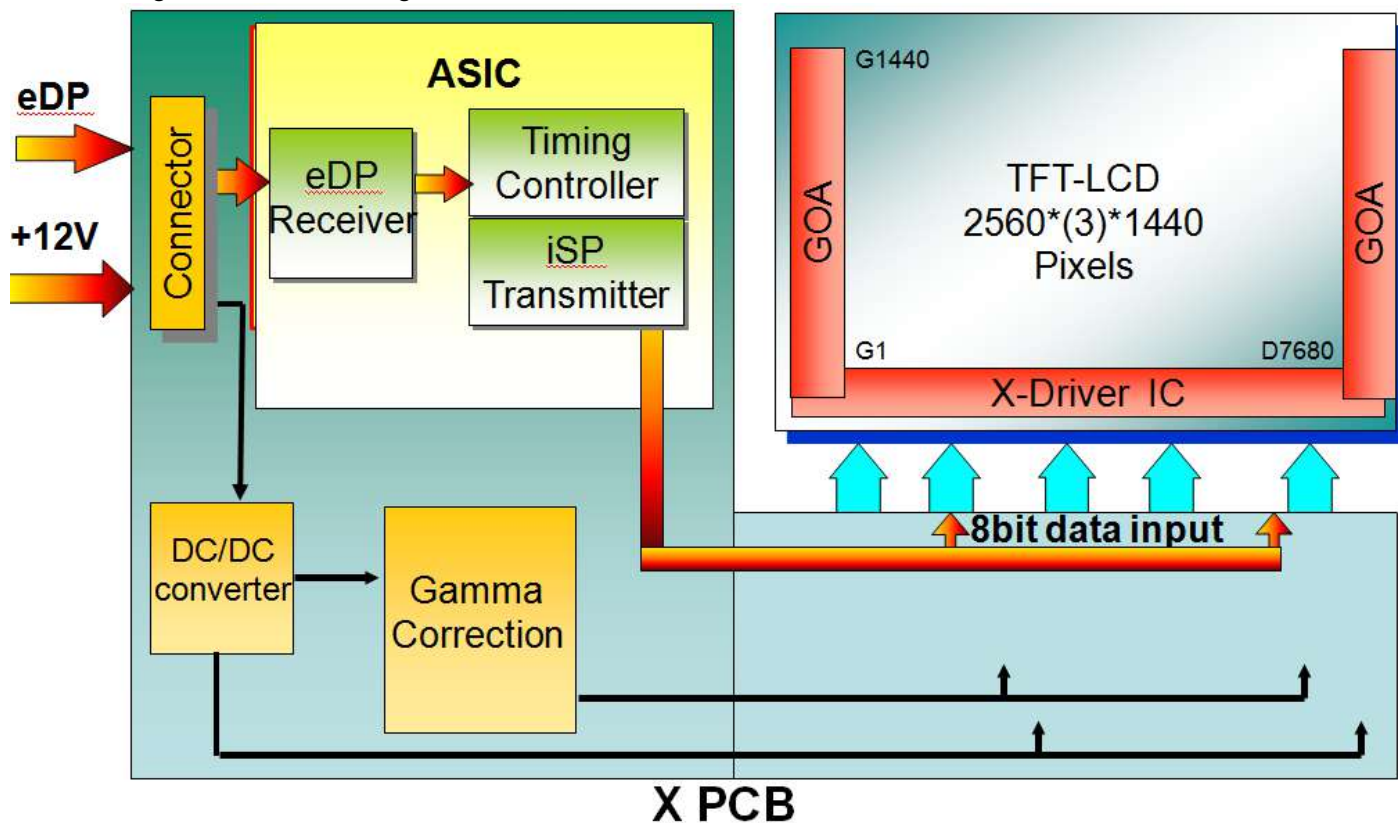| PIN #	Symbol	Description	Remark
1	VDD	Power +12V	
2	VDD	Power +12V	
3	VDD	Power +12V	
4	VDD	Power +12V	
5	VDD	Power +12V	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	NC	No connection (for AUO test only. Do not connect)	
10	NC	No connection (for AUO test only. Do not connect)	
11	NC	No connection (for AUO test only. Do not connect)	
12	NC	No connection (for AUO test only. Do not connect)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	IMS	Interlace Mode Selection (I)	
16	IMS_POL	Interlace Mode Selection Polarity (O)	
17		Ground	
18	1st Lane3_N	Negative eDP differential data input	
19	1st Lane3_P	Positive eDP differential data input	
20	GND	Ground	
	1st Lane2_N	Negative eDP differential data input	
22	1st Lane2_P	Positive eDP differential data input	
23	GND	Ground	
24	1st Lane1_N	Negative eDP differential data input	
25	1st Lane1_P	Positive eDP differential data input	
26	GND	Ground	

27	1st Lane0_N	Negative eDP differential data input	
28	1st Lane0_P	Positive eDP differential data input	
29	GND	Ground	
30	1st AUX_CH_P	Positive AUX Channel differential data input	
31	1st AUX_CH_N	Negative AUX Channel differential data input	
32	GND	Ground	
33	NC	No connection (for AUO test only. Do not connect)	
34	GND	Ground	
35	NC	No connection (for AUO test only. Do not connect)	
36	NC	No connection (for AUO test only. Do not connect)	
37	GND	Ground	
38	NC	No connection (for AUO test only. Do	
39	NC	No connection (for AUO test only. Do not connect)	
40	GND	Ground	
41	NC	No connection (for AUO test only. Do not connect)	
42	NC	No connection (for AUO test only. Do not connect)	
43	GND	Ground	
44	NC	No connection (for AUO test only. Do not connect)	
45	NC	No connection (for AUO test only. Do not connect)	
46	GND	Ground	
47	NC	No connection (for AUO test only. Do not connect)	
48	NC	No connection (for AUO test only. Do not connect)	
49	GND	Ground	
50	HPD	Hot plug detection	
51	GND	Ground	

3.3 Electrical Characteristics

3.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14	[Volt]	Ta=25℃

3.3.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power supply Input voltage	10.8	12.0	13.2	[Volt]	
IDD	Power supply Input Current (RMS)	-	TBD	TBD	[A]	VDD= 12V, Black Pattern, Fv=165Hz
PDD	VDD Power Consumption	-	TBD	TBD	[Watt]	VDD= 12V, Black Pattern, Fv=165Hz
IRush	Inrush Current	-	-	3.0	[A]	*Note 3-2*
VDDrp	Allowable VDD Ripple Voltage	-	-	1200	[mVolt]	VDD= 12.0V, Black Pattern, Fv=165Hz

Note 3-1: Inrush Current measurement:

Test circuit:

The duration of VDD rising time: 470us.

3.4 Signal Characteristics

3.4.1 LCD Pixel Format

Following figure shows the relationship between the input signals and LCD pixel format.


```
1stLane0 :  1, 5  ...................→ 2557 pixel  ➔ 4N+1, N=0 ~ 639 (1,5.. 2557pixe)
1stLane1 :  2, 6  ...................→ 2558 pixel  ➔ 4N+2, N=0 ~ 639 (2,6.. 2558pixe)
1stLane2 :  3, 7  ...................→ 2559 pixel  ➔ 4N+3, N=0 ~ 639 (3,7.. 2559pixe)
1stLane3 :  4, 8  ...................→ 2560 pixel  ➔ 4N+4, N=0 ~ 639 (4,8.. 2560pixe)
```

3.4.2 eDP Data Format

1st Lane0	1st Lane1	1st Lane2	1st Lane3
R1-7:0	R2-7:0	R3-7:0	R4-7:0
G1-7:0	G2-7:0	G3-7:0	G4-7:0
B1-7:0	B2-7:0	B3-7:0	B4-7:0
R5-7:0	R6-7:0	R7-7:0	R8-7:0
G5-7:0	G6-7:0	G7-7:0	G8-7:0
B5-7:0	B6-7:0	B7-7:0	B8-7:0
R9-7:0	R10-7:0	R11-7:0	R12-7:0
G9-7:0	G10-7:0	G11-7:0	G12-7:0
B9-7:0	B10-7:0	B11-7:0	B12-7:0
.	.	.	.
.	.	.	.
.	.	.	.

3.4.3 Color versus Input Data

The following table is for color versus input data (8bit). The higher the gray level, the brighter the color.

| Color	Gray Level	RED data (MSB:R7, LSB:R0)								GREEN data (MSB:G7, LSB:G0)								BLUE data (MSB:B7, LSB:B0)								Remark
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

3.4.4 eDP Specification (Follow as VESA DisplayPort Standard Version 1.2)

a. DisplayPort main link signal:

DisplayPort main link		Min	Typ	Max	unit
Frequency	Main link Frequency	-	2.7	-	Gbps
UI	Unit Interval	-	370	-	ps
VCM	RX input DC Common Mode Voltage	-	0	-	[Volt]
VDiff$_{P-P}$	Peak-to-peak Voltage at a receiving Device	150	-	-	[mVolt]
Down_Spread_Freq	Link clock down spread frequency	30	-	33	KHz
Down_Spread_Amplitude	Link clock down spread amplitude	-	-	0.5	%

Point	Time (UI)	Voltage (V)
1	0.245	0
2	0.5	75mV
3	0.755	0
4	0.5	-75mV

Figure 5.55.3 Downstream Device EYE Mask at Receiver Connector for HBR

Figure 5.55.1 Downstream Device EYE Mask at Receiver Connector Pins

Freq(bps)

< Spread Spectrum>
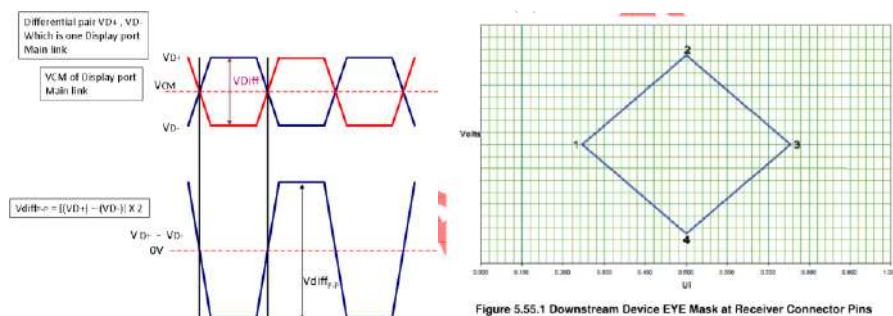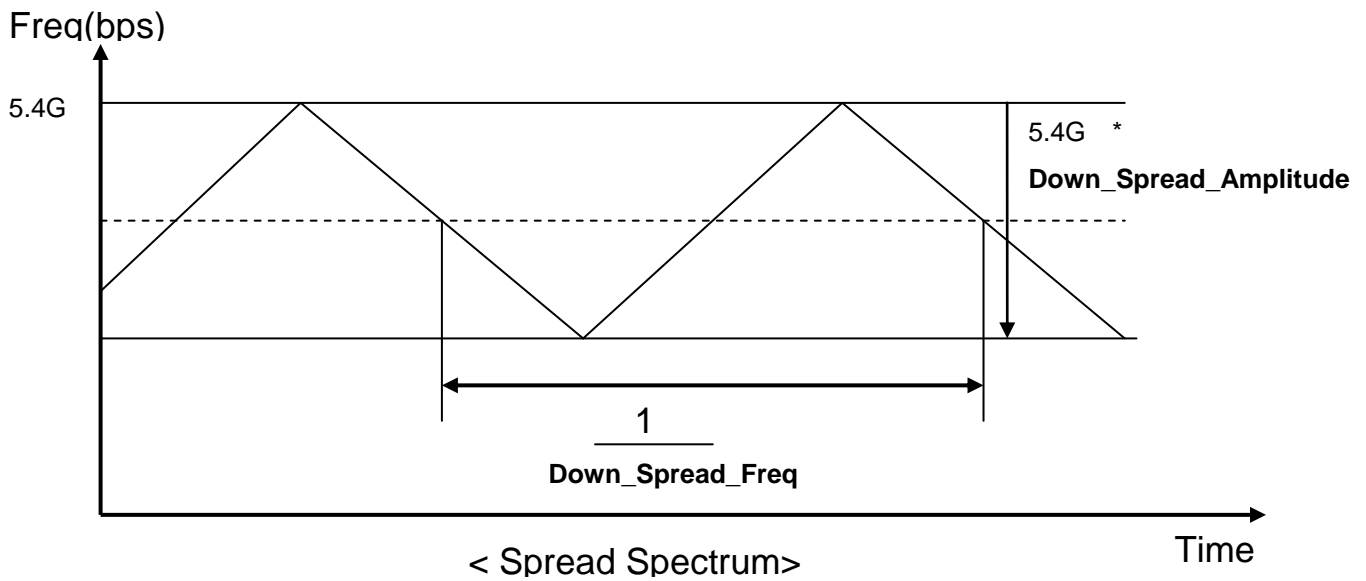
b. DisplayPort AUX_CH signal:

	DisplayPort AUX_CH				
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage	0	-	2.0	[Volt]
VDiff$_{P-P}$	AUX Peak-to-peak voltage at a receiving device	0.27	-	1.36	[Volt]
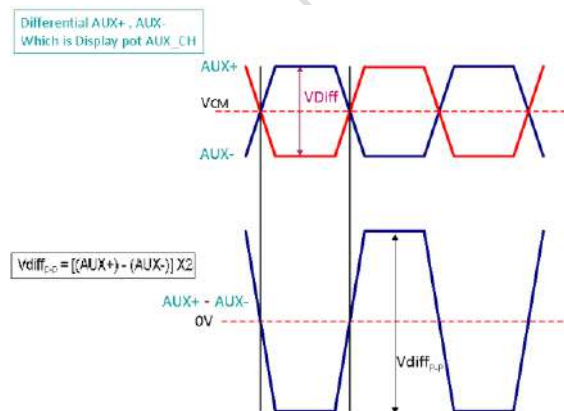
c. DisplayPort VHPD signal:

	Display Port VHPD				
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	-	3.6	[Volt]

d. Intra-Pair skew

LRX-SKEW-INTRA_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTRA_PAIR	Lane Intra-pair Skew Tolerance	-	-	50	[ps]

e. Inter-Pair Skew

LRX-SKEW-INTER_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTER_PAIR	Lane-to-Lane Skew at RX package pins	-	-	5200	[ps]

3.4.5 Input Timing Specification

The input timing is shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	1460	1464	8080	Th	
Tdisp (v)		Active	1440	1440	1440	Th	
Tblk (v)		Blanking	20	24	6640	Th	
Fv		Frequency	30	120	165	Hz	*Note 3-5* *Note 3-6*
Th	Horizontal Section	Period	2640	2720	2860	Tclk	
Tdisp (h)		Active	2560	2560	2560	Tclk	
Tblk (h)		Blanking	80	160	300	Tclk	
Fh		Frequency	90.9	175.7	242.4	kHz	*Note 3-3*
Tclk	Pixel Clock	Period	1.56	2.09	4.17	ns	1/Fclk
Fclk			240	477.85	639.9	MHz	*Note 3-4*
Link Rate per Lane				5.4		Gbps	

Note 3-3: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = $Fclk$ (Min.) / Th (Min.)
Fh (Typ.) = $Fclk$ (Typ.) / Th (Typ.)
Fh (Max.)= $Fclk$ (Max.) / Th (Min.)

Note 3-4: The equation is listed as following. Please don't exceed the above recommended value.

1st Lane N & 2nd Lane N skew < 200ns
$Fclk$ (Typ.) = Fv (Typ.) x Th (Typ.) x Tv (Typ.)
$Fclk$ (Min.)$\leq Fv$ x Th x $Tv \leq Fclk$ (Max.)

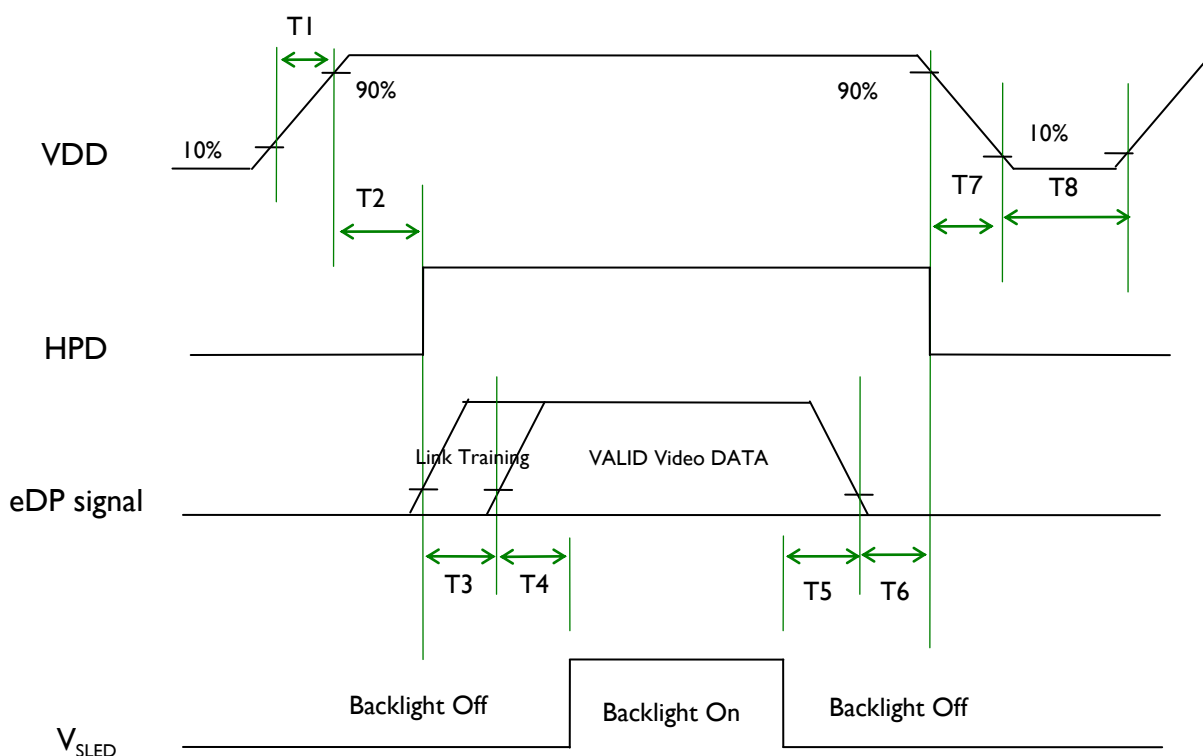***Note 3-5:*** The equation is listed as following. Please don't exceed the above recommended value.

Fv =$Fclk$(Typ.) / (Tv x Th)

Note 3-6: The optimal Vertical Frequency is 50~65 Hz for best picture quality.

3.5 Power ON/OFF Sequence

VDD power,eDP signal and backlight on/off sequence are as following. eDP signals from any system tshall be Hi-Z state when VDD is off.

Power Sequence Timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	200	[ms]	
T3	0	-	-	[ms]	Note 3-7
T4	500	-	-	[ms]	
T5	100	-	-	[ms]	
T6	0	-	50	[ms]	Note 3-8 Note 3-9
T7	0	-	200	[ms]	Note 3-9 Note 3-10
T8	1000	-	-	[ms]	

Note 3-7: During T3 period , eDP link training time by customer's system.

Note 3-8: Recommend setting T6 = 0ms to avoid electronic noise when VDD is off.

Note 3-9: During T6 & T7 period , please keep the level of input eDP signals with Hi-Z state.

Note 3-10: Voltage of VDD must decay smoothly after power-off.(customer system decide this value)

4 Backlight Unit

4.1 Block Diagram

The following shows the block diagram of the 32.0 inch Backlight Unit. And it includes 2 pcs LED light bar in Backlight Unit. Each LED light bar includes 64pcs LED package. (= 8 strings; 8 pcs LED for each string).
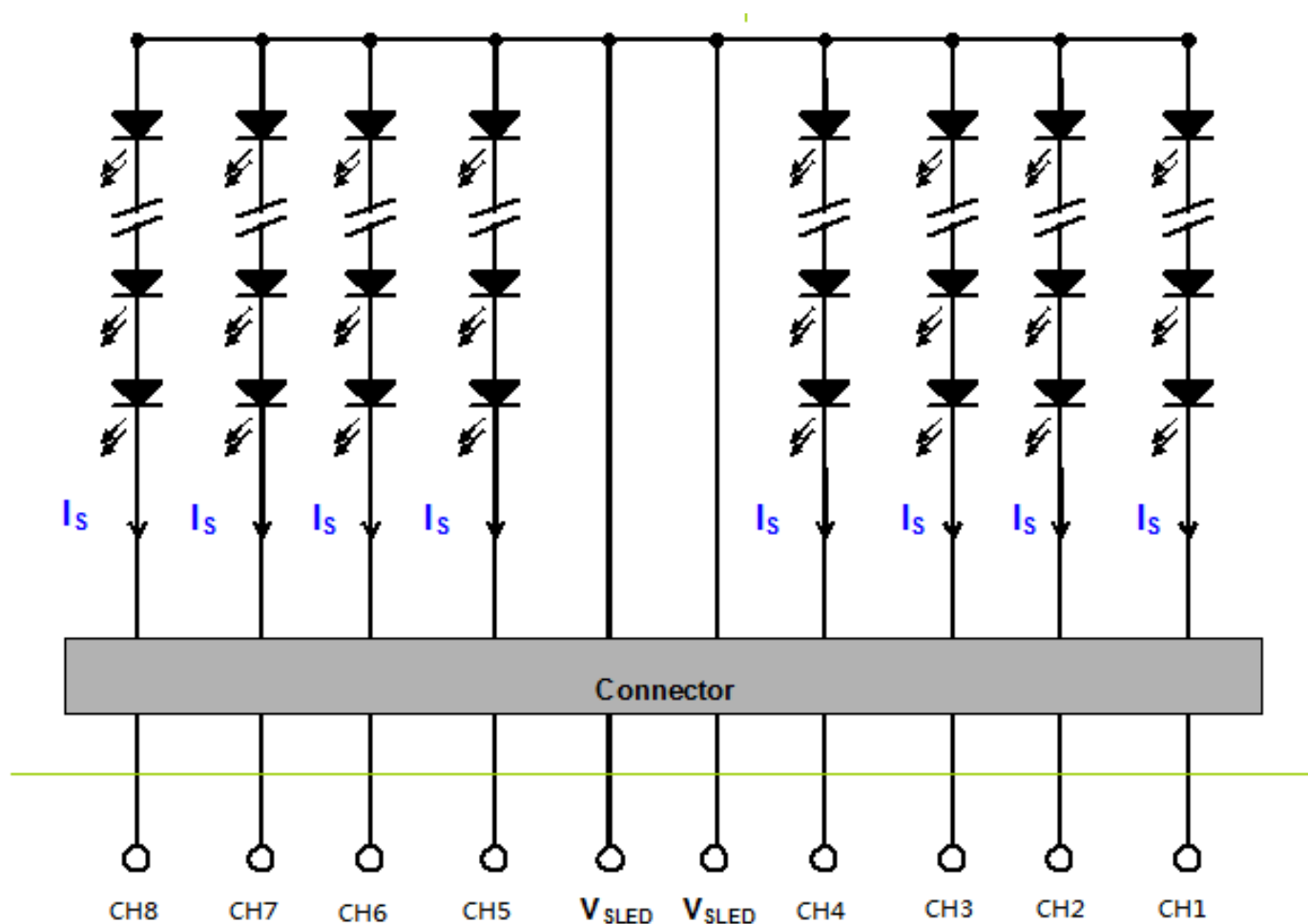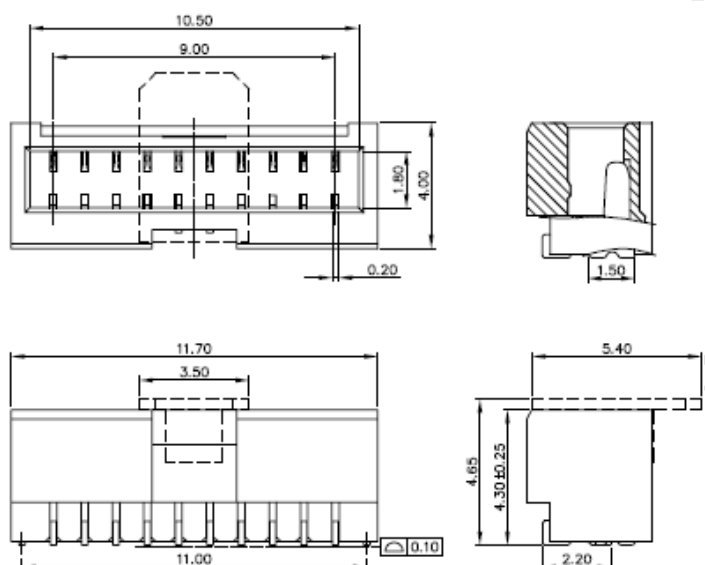
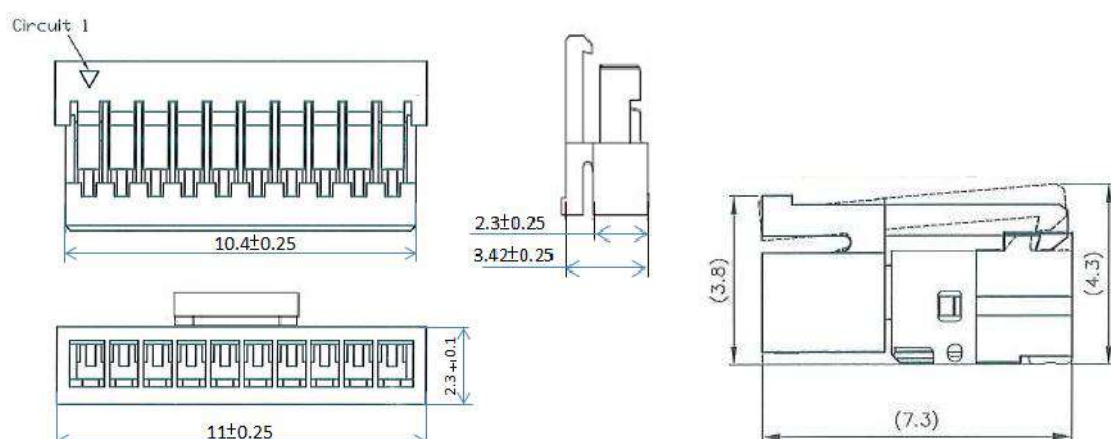## 4.2 Interface Connection

4.2.1 Connector Type

Backlight Connector	Manufacturer	ENTERY
	Part Number	3709K-F10C-04L
Mating Connector	Manufacturer	ENTERY
	Part Number	H112K-D10N-31B (Locking type) H112K-D10N-30B (Non-Locking type)

Backlight Connector dimension:

$$H \times V \times D = 11.7 \times 4.00 \times 4.65, Pitch = 1.0 (unit = mm)$$

Mating Connector dimension:

4.2.2 Connector Pin Assignment

Pin#	Symbol	Description	Remark
1	Ch1	LED Current Feedback Terminal (Channel 1)	
2	Ch2	LED Current Feedback Terminal (Channel 2)	
3	Ch3	LED Current Feedback Terminal (Channel 3)	
4	Ch4	LED Current Feedback Terminal (Channel 4)	
5	V_{SLED}	LED Power Supply Voltage Input Terminal	
6	V_{SLED}	LED Power Supply Voltage Input Terminal	
7	Ch5	LED Current Feedback Terminal (Channel 5)	
8	Ch6	LED Current Feedback Terminal (Channel 6)	
9	Ch7	LED Current Feedback Terminal (Channel 7)	
10	Ch8	LED Current Feedback Terminal (Channel 8)	
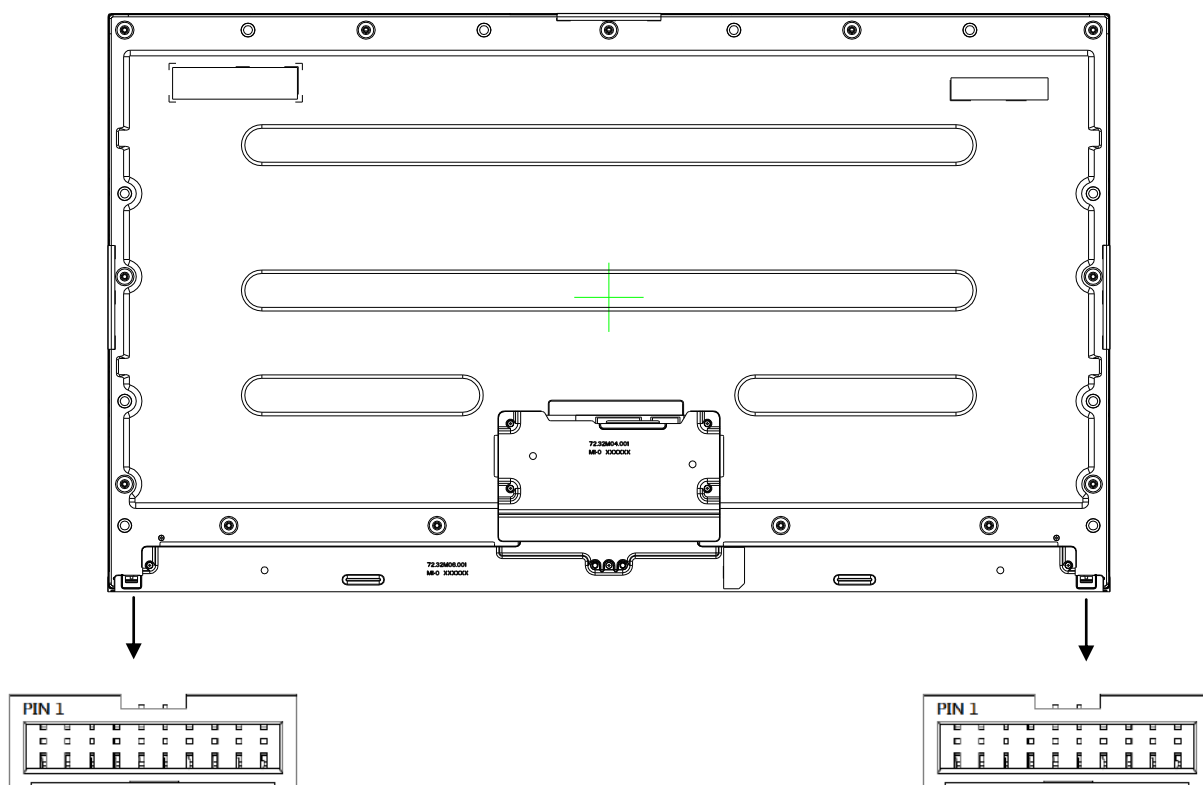
4.3 Electrical Characteristics

4.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

(Ta=25℃)

Symbol	Description	Min	Max	Unit	Remark
Is	LED String Current	0	180	[mA]	100% duty ratio

4.3.2 Recommended Operating Condition

Symbol	Description	Min.	Typ.	Max.	Unit	Remark
I_S	LED String Current	-	50	55	[mA]	100% duty ratio of LED chip; *Note 4-7*
I_{SP}	HDR PEAK LED String Current	-	95	105	[mA]	100% duty ratio of LED chip; *Note 4-7*
V_S	LED String Voltage	43.2	45.6	48.8	[Volt]	I_S=50mA @ 100% duty ratio; *Note 4-1, Note 4-5*
V_{SP}	HDR PEAK LED String Voltage	44	47.2	50.4	[Volt]	I_{SP}=95mA @ 100% duty ratio; *Note 4-1, Note 4-5*
ΔV_S	Maximum Vs Voltage Deviation of light bar	-	-	1.6	[Volt]	100% duty ratio of LED chip; *Note 4-2*
P_{BLU}	LED Light Bar Power Consumption	34.6	36.5	39.0	[Watt]	I_S=50mA; *Note 4-3*
P_{BLUP}	Power Consumption	66.9	71.7	76.6	[Watt]	I_{SP}=95mA; *Note 4-3*
LT_{LED}	LED Life Time	30000			[Hour]	*Note 4-4*
OVP	Over Voltage Protection in system board	110% Vsmax	-	-	[Volt]	*Note 4-5*

Note 4-1: Vs (Typ.) = V_F (Typ.) X LED No. (one string);

  a. V_F: LED chip forward voltage, V_F(Min.)=5.4V, V_F(Typ.)=5.7V, V_F(Max.)=6.1V;

  b. The same euqation to calculate V_S(Min.) & V_S(Max.) for respective V_F(Min.) & V_F(Max.);

  c. V_{FP}: LED chip forward voltage, V_{FP}(Min.)=5.5V, V_{FP}(Typ.)=5.9V, V_{FP}(Max.)=6.3V;

  d. The same euqation to calculate V_{SP}(Min.) & V_{SP}(Max.) for respective V_{FP}(Min.) & V_{FP}(Max.);

LED chip

Note 4-2: ΔVs (Max.) = ΔV_F X LED No. (one string);
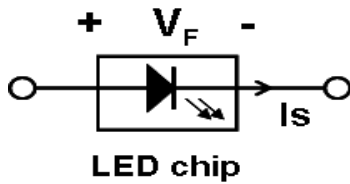
  a. ΔV_F: LED chip forward voltage deviation (0.2V , each Bin of LED V_F)

Note 4-3: P_{BLU} (Typ.) = Vs (Typ.) X Is (Typ.) X 16 (16 is total String No. of BLU)

  P_{BLU} (Max.) = Vs (Max.) X Is (Typ.) X 16

  a. The same euqation to calculate P_{BLUP}(Typ.) & P_{BLUP}(Max.) for respective P_{BLU}(Typ.) & P_{BLU}(Max.);

Note 4-4: Definition of life time:

  a. Brightness of LED becomes to 50% of its original value

  b. Test condition: Is = 50mA and 25℃ (Room Temperature)

Note 4-5: Recommendation for LED driver power design:

Due to there are electrical property deviation in LED & monitor set system component after long time operation. AUO strongly recommend the design value of LED driver board OVP (over voltage protection) should be 10% higher than max. value of LED string voltage (Vs) at least.

Note 4-6: AUO strongly recommend "Analog Dimming" method for backlight brightness control for Wavy Noise Free. Otherwise, recommend that Dimming Control Signal (PWM Signal) should be synchronized with Frame Frequency

Note 4-7 Ensure that the LED light bar is not subjected either forward or reverse voltage while monitor set is on standby mode or not in use.

5 Reliability Test

AUO reliability test items are listed as following table. (*Bare Panel only*)

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50℃, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0℃, 300hours	
High Temperature Storage (HTS)	Ta= 60℃, 300hours	
Low Temperature Storage (LTS)	Ta= -20℃, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 Grms Wave: Random Frequency: 10 - 200 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	*Note 5-1*
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 15KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	*Note 5-2*
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:18,000 ft Non-Operation:40,000 ft	

Note 5-1: a. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test.

b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 5-2: EN61000-4-2, ESD class B: Certain performance degradation allowed

No data lost

Self-recoverable

No hardware failures.

ESD discharged points should avoid display area and periphery front bezel of

display area. Suggest points were 4 side parallel edge of display area surface.

Metal front bezel must cover half area of BM (black matrix), and metal front

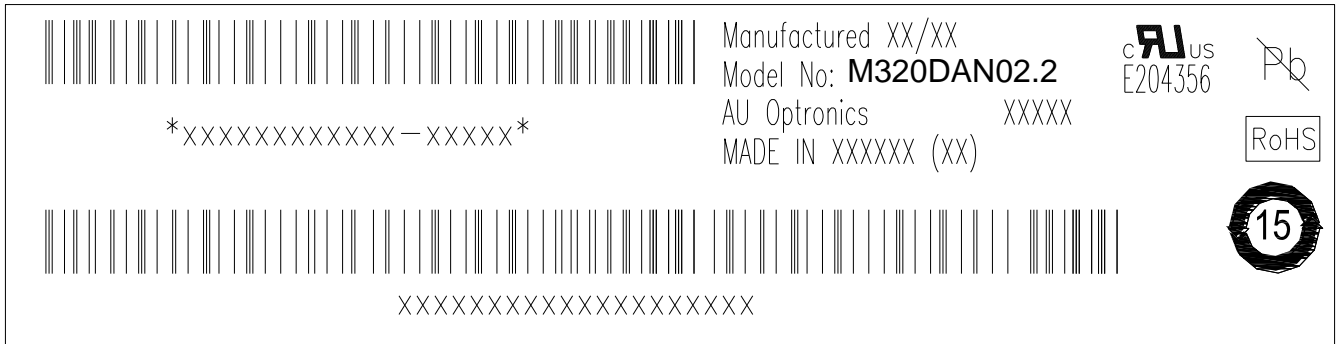bezel must connect with metal back bezel to protect source IC of panel by ESD damaged.

Note 5-3: Result Evaluation Criteria:

TFT-LCD panels test should take place after gradually cooling enough at room temperature. In the normal application, there should be no particular problems that may affect the display function.

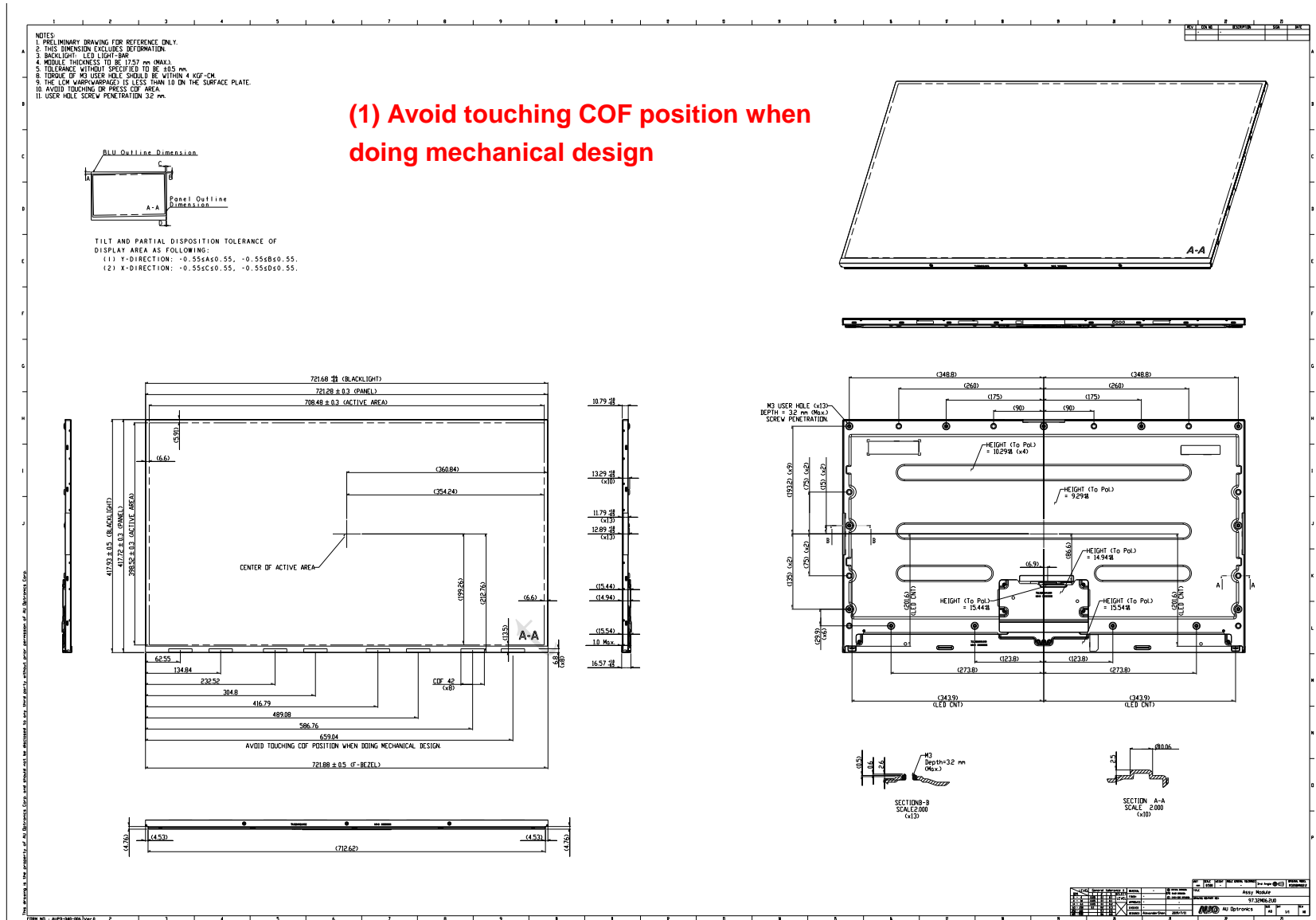## 6 Shipping Label

The label is on the panel as shown below:

```
Manufactured XX/XX
Model No: M320DAN02.2
AU Optronics          XXXXX
MADE IN XXXXXX (XX)
```

××××××××××××－×××××

××××××××××××××××××××

E204356

Pb

RoHS

15

Note 6-1: For Pb Free products, AUO will add for identification.

Note 6-2: For RoHS compatible products, AUO will add for identification.

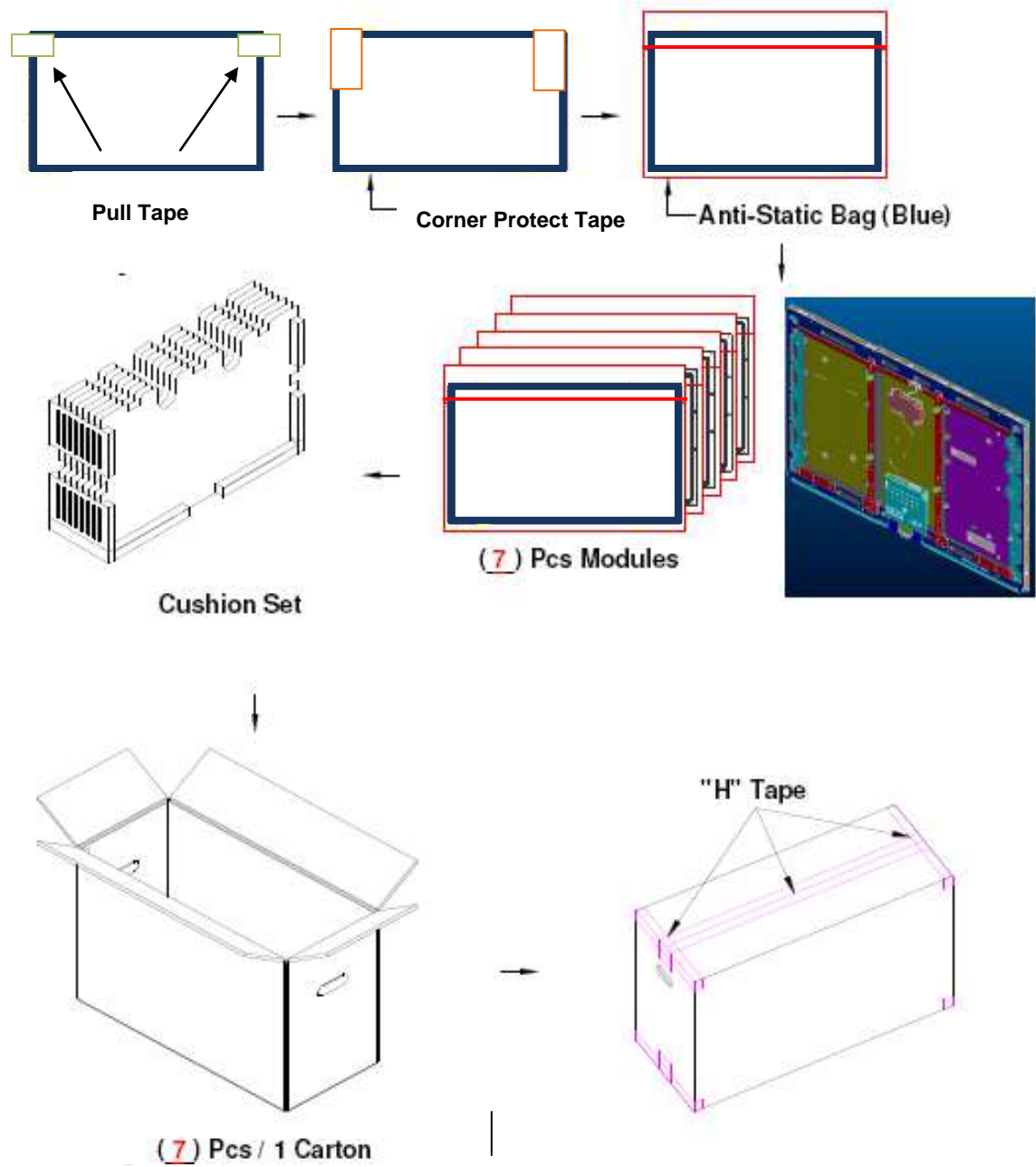*Note 6-3:* For China RoHS compatible products, AUO will add for identification.

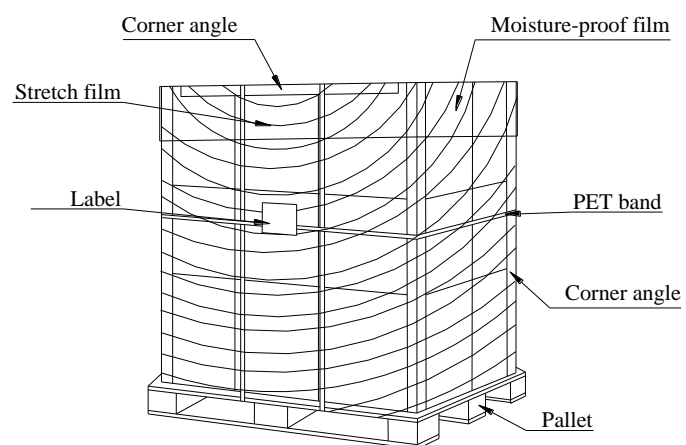*Note 6-4:* The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

7 Mechanical Characteristics

(1) Avoid touching COF position when doing mechanical design

8 Packing Specification

8.1 Packing Flow

Pull Tape → **Corner Protect Tape** → Anti-Static Bag (Blue)

Cushion Set ← (7) Pcs Modules

(7) Pcs / 1 Carton → "H" Tape

Corner angle

Moisture-proof film

Stretch film

Label

PET band

Corner angle

Pallet

8.2 Pallet and shipment information

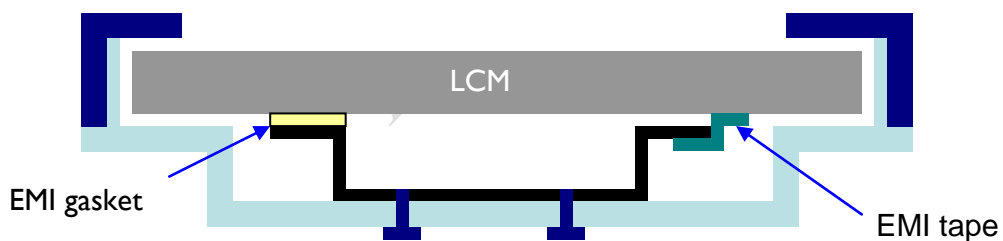| Item	Specification			Remark
	Q'ty	Dimension	Weight(kg)	
Panel	1	721.68(H)mm x 417.9(V)mm x 16.57(D)mm	3.90	
Cushion	1	-	6.88	
Box	1	805(L)mm x 280(W)mm x 512(H)mm		without Panel
Packing Box	7 pcs/Box	805(L)mm x 280(W)mm x 512(H)mm	34.18	with panel & cushion & Box
Pallet	1	1150(L)mm x 840(W)mm x 132	13.8	
Pallet after Packing	8 boxes/pallet	1150(L)mm x 840(W)mm x 1156(H)mm	287.24	

9 Design Guide for System

9.1 AHVA design guide

### 9.1.1 The gap between LCM and system rear bracket should be bigger than 0.5mm.

### 9.1.2 The system bracket should be fixed on back cover firmly.

Front cover

LCM

Back cover

Gap>0.5mm

Bracket

Bracket and back cover, fixed by screws or
strong mechanical structures.
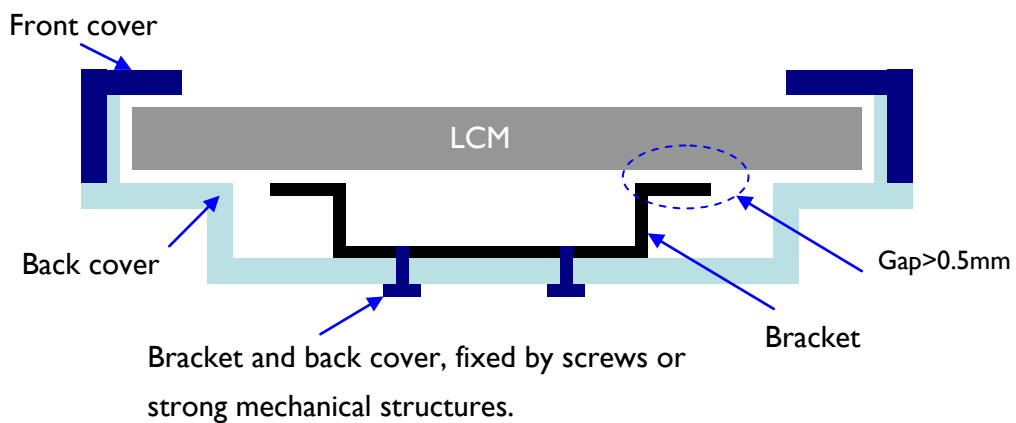
9.1.3 The EMI gasket should be uniform and not push panel strongly.

LCM

EMI gasket

EMI tape

9.1.4 For stable assembly, the system bracket should use 4 screws to fix system and panel by dual sides.
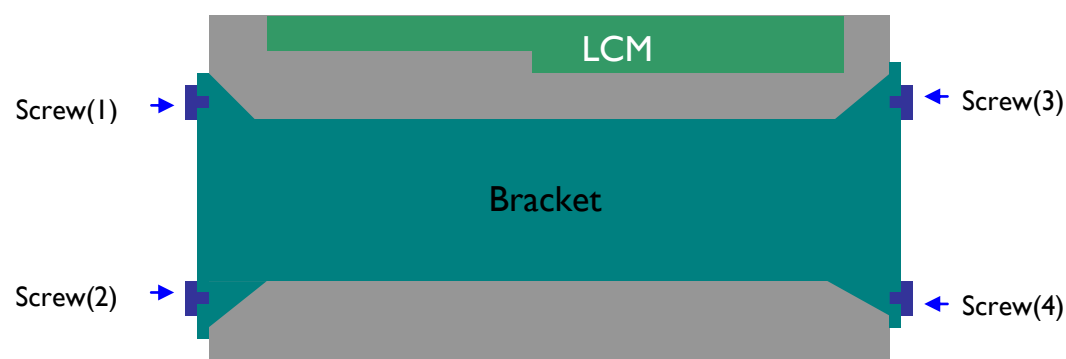
9.1.5 The system bracket and panel should be in parallel with having no gap after inserting screws.
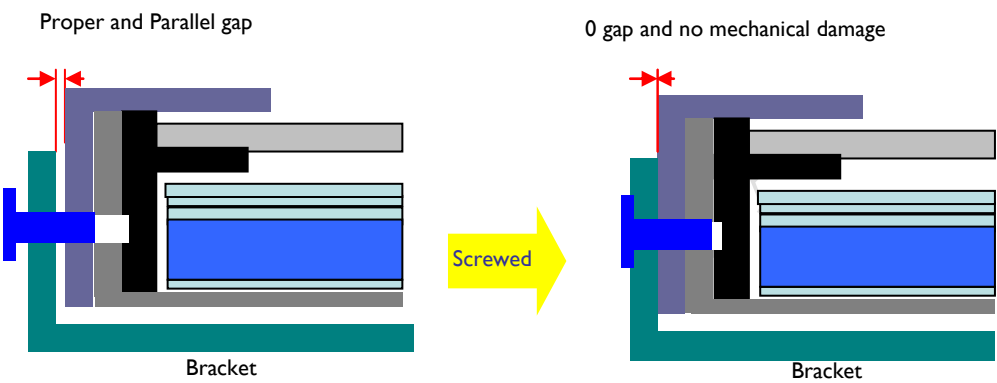
9.1.6 Avoid scratching LCM, the rib on system front-cover should not exceed the bottom edge of LCM's front-bezel.