( ) Preliminary Specifications
(V) Final Specifications

Module	**14.0" HD Color TFT-LCD with LED Backlight design**
Model Name	B140XW01 V1
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**
Checked & Approved by	**Date**
Note: This Specification is subject to change without notice.	

Approved by	**Date**
~~Bonnie Chen~~	~~08/06/2009~~
Prepared by	
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Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2008/04/30	All	First Edition for Customer		
0.2 2008/05/16	15/24/25	ConnectorType & Pin Assignment	20455-040E-12 & Pin Assignment Backlight Unit Parameter	
0.3	32		Add China RoHS 15	
0.4	22;32		6.4.1 Timing Characteristics; Shipping Label remove PM code	
0.5	6;32-34	Modify White Luminance item	200 typ/170 min.;32-34 Update Carton and Shipping package of palletizing sequence	
0.6	13		Add LED Driving Input Voltage	
0.7	35	Modify :Appendix: EDID description	16:9 EDID Format	
0.8	35	Modify :Appendix: EDID description		
0.9	32	Modify Label	GP Mark	
1.0	18 32	Add second source H/W code 6.3 Integration Interface and Pin Assignment	Modify Label H/W code VLED LED Power Supply 7V-20V	
1.1	18	Modify LVDS pin1, pin34 description.	Pin1, pin34 for N.C.	
1.2	6 23	Modify chromaticity data. Modify luminance data 170min, 200typ Note: “The duty of LED dimming signal should be more than 20% in T2 and “T3	 187min, 220 typ. Delete LED duty ratio note.	
1.3	34~37	Old EDID code.	New EDID code.	
1.4	1	Premilinary spec	Final spec.	
1.5 08/06/2009	13 18	Modified 5.1.1 note3 figure.(+5.0v) Pin-assingment description update: pin 36 LEDEN (+3.0V input) pin38~40(7V~20V)	Modified 5.1.1 note3 figure.(+3.3v) Pin-assingment description update: pin 36 LEDEN (+3.3V input) pin38~40(7V~21V)	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breakdown.

2. General Description

B140XW01 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the HD (1366(H) x 768(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B140XW01 V1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	354.95 (14.0W")			
Active Area	[mm]	309.40 X 173.95			
Pixels H x V		1366x3(RGB) x 768			
Pixel Pitch	[mm]	0.2265X0.2265			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance **(I_{LED}=20mA)** **(Note: ILED is LED current)**	[cd/m^2]	220 typ. (5 points average)			
~~Luminance Uniformity~~		~~187 min. (5 points average)~~ 1.25 max. (5 points)			
~~Contrast Ratio~~		~~400 typ~~			
~~Response Time~~	~~[ms]~~	~~8 typ / 12 Max~~			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.8 max. (Include Logic and Blu power)			
~~Weight~~	~~[Grams]~~	~~350 max.~~			
Physical Size **without inverter, bracket.**	[mm]		~~Min.~~	~~Typ.~~	~~Max.~~
		~~Length~~		~~323.5~~	~~324~~
		~~Width~~		~~192~~	~~192.5~~
		~~Thickness~~			~~5.2~~
Electrical Interface		1 channel LVDS			
Surface Treatment		Anti-Glare.			
Support Color		262K colors (RGB 6-bit)			

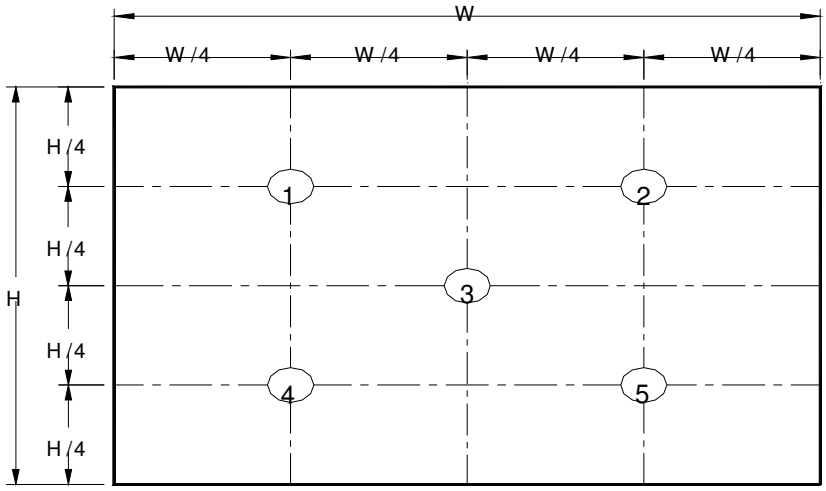
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

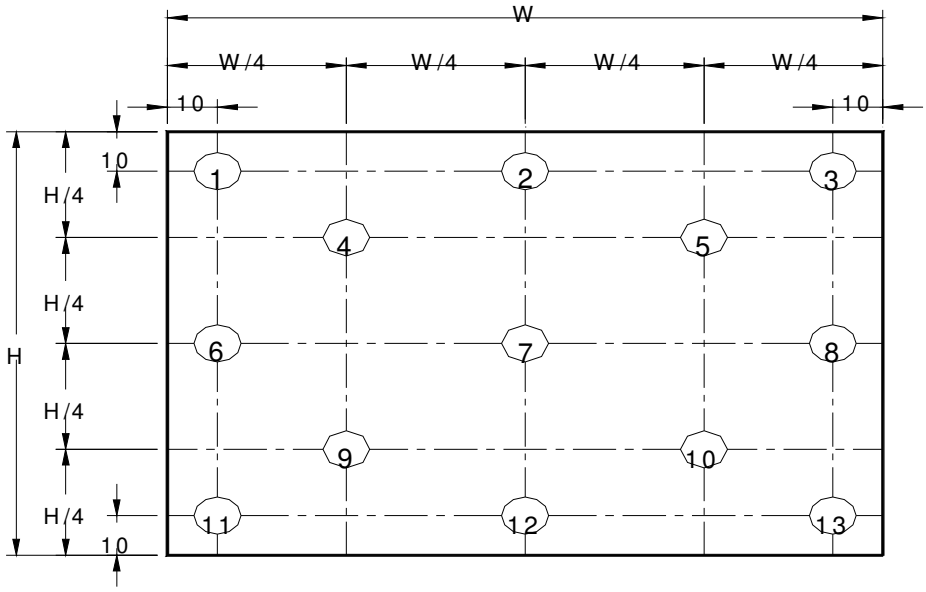
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=20mA			5 points average	187	220	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	40 40	45 45	- -	degree	4, 9
		Ψ_H Ψ_L	Vertical (Upper) CR = 10 (Lower)	10 30	15 35	- -		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.50		2, 3, 4
Contrast Ratio		CR		300	400	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_r	Rising	-	-	-	msec	4, 8
		T_f	Falling	-	-	-		
		T_{RT}	Rising + Falling	-	8	12		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.590	0.620	0.650		4
		Ry		0.310	0.340	0.370		
	Green	Gx		0.300	0.330	0.360		
		Gy		0.540	0.570	0.600		
	Blue	Bx		0.120	0.150	0.180		
		By		0.030	0.060	0.090		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	60	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

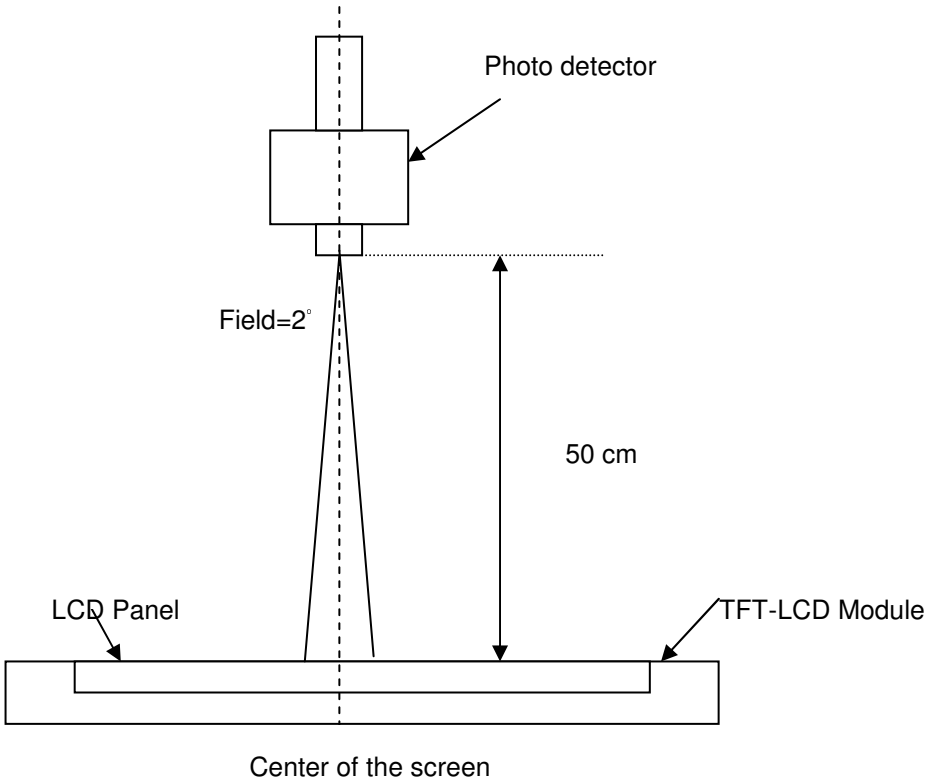
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

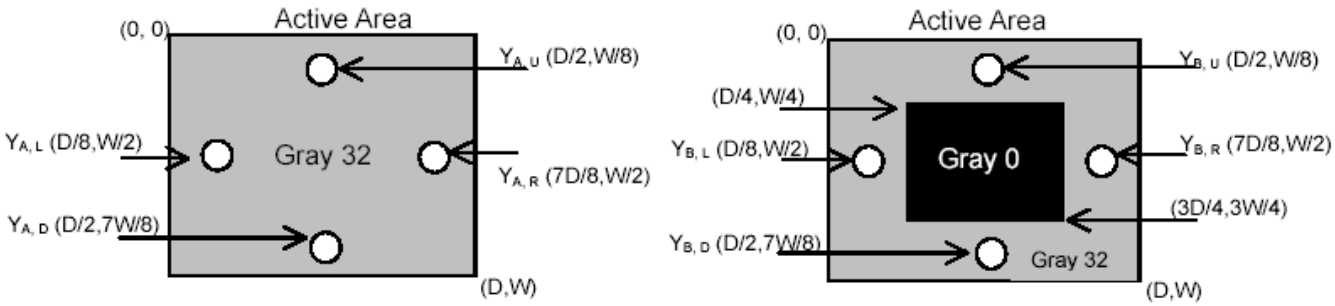
Note 7 : Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

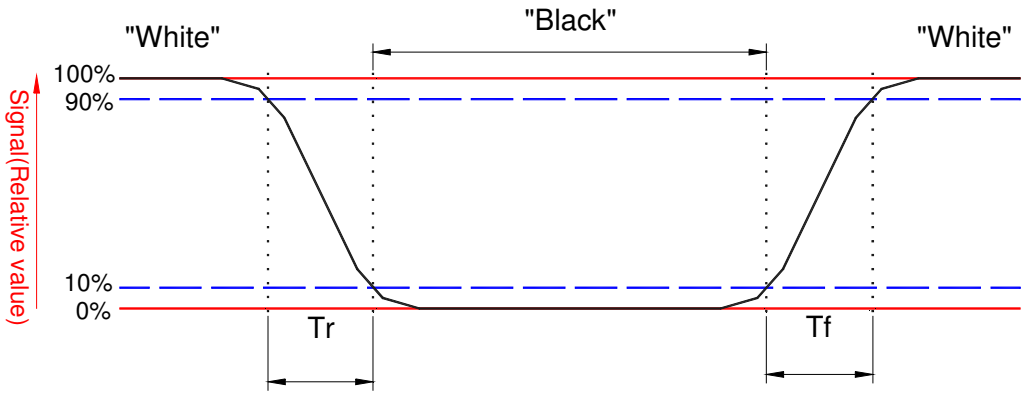
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



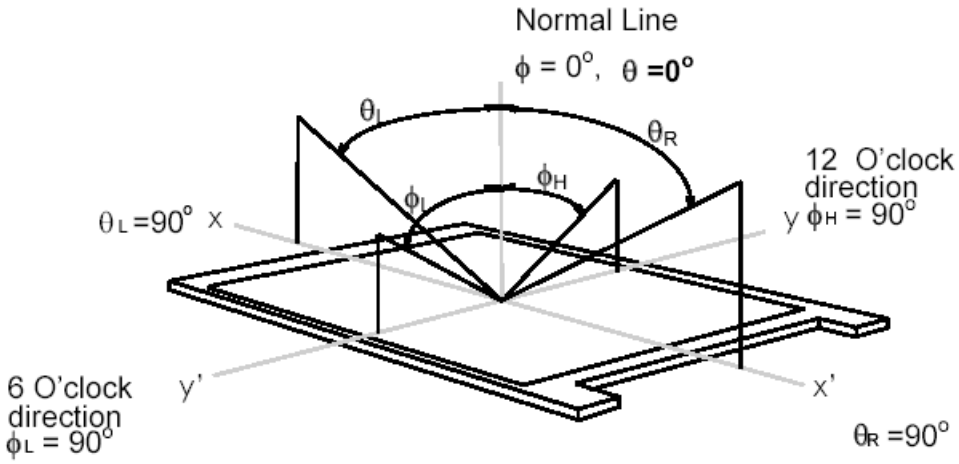
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



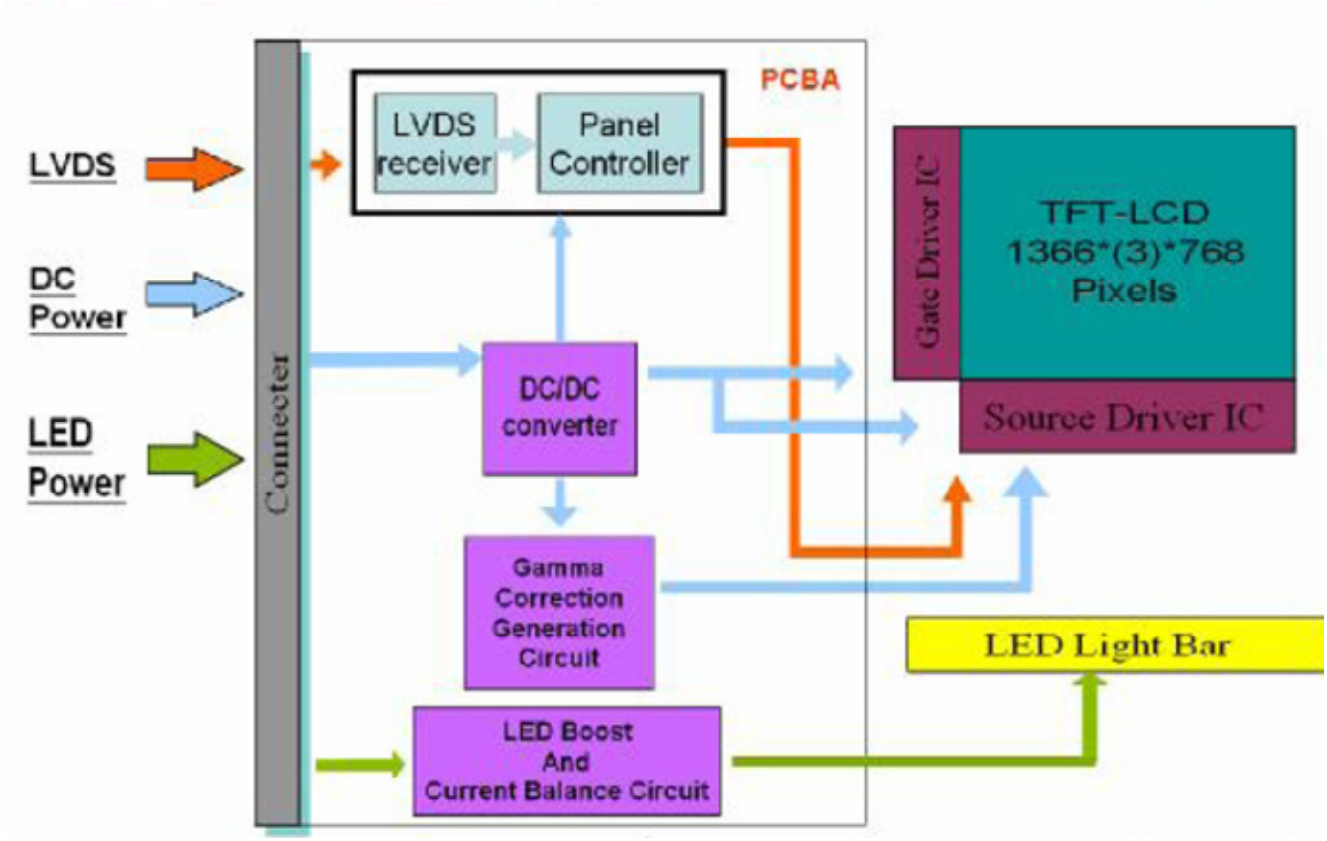
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 40 Pin (One CH/connector Module)



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

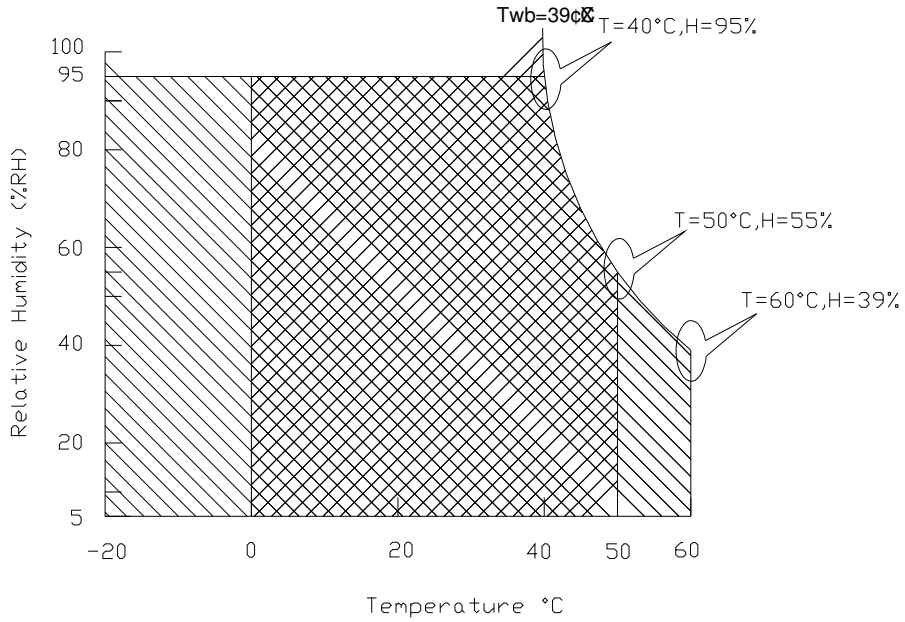
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	10	90	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	10	90	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range

Storage Range

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

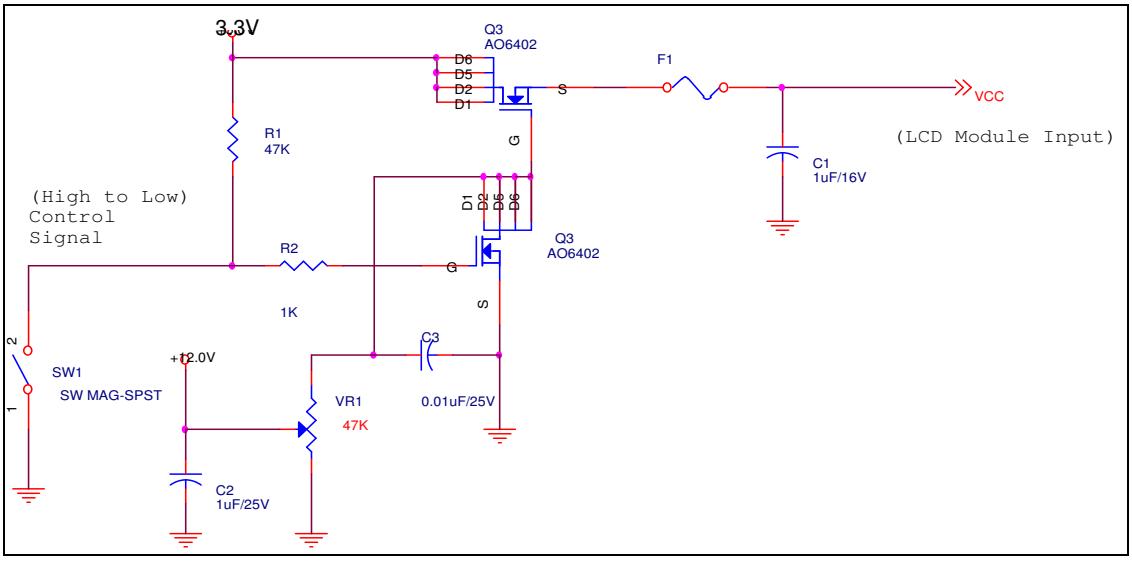
The power specification are measured under 25℃ and frame frenquency under 60Hz

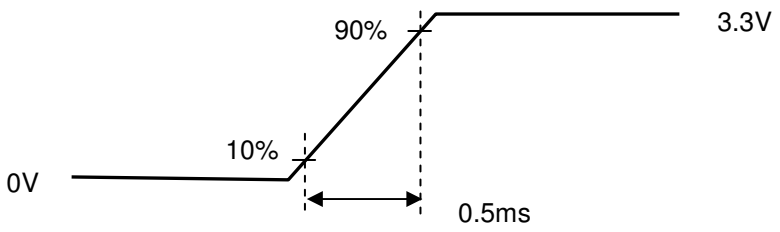
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	1.1	1.2	[Watt]	Note 1/2
IDD	IDD Current	-	333	364	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Typical Measurement Condition: Mosaic Pattern

Note 3 : Measure Condition





Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

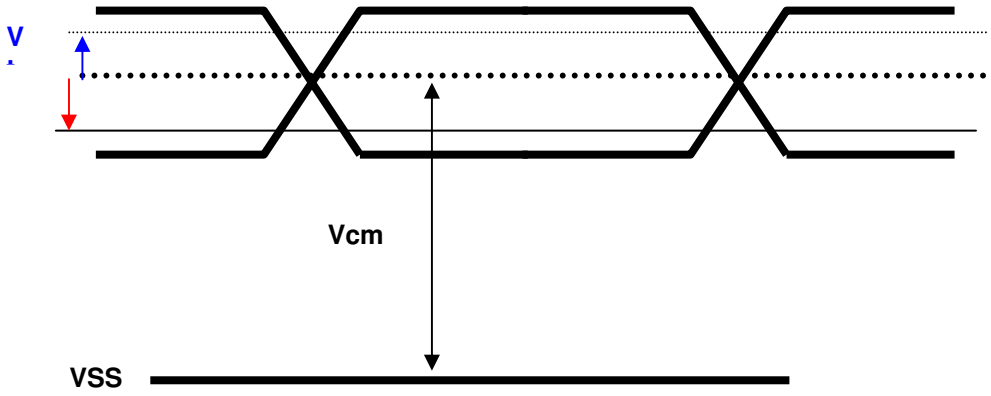
It is recommended to refer the specifications of THC63LVDF84A (Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Typ	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)	-		100 *note1	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100 *note1		-	[mV]
Vcm	Differential Input Common Mode Voltage	0.05	1.2	1.9	[V]

Note: LVDS Signal Waveform

*note1 R_{xVCM}=1.2V



5.2 Backlight Unit

LED Parameter guideline for LED driving selection (Ref. Remark 1)

Parameter	Symbol	Min	Typ	Max	Units	Condition
LED Forward Voltage	V_F	2.95	3.2	3.4	[Volt]	(Ta=25℃)
LED Forward Current	I_F		20	20.6	[mA]	(Ta=25℃)
LED Power consumption	P_{LED}		3.07	3.36	[Watt]	(Ta=25℃) Note 1
LED Driving Input Voltage	V_{LED}	7	12	21	[Volt]	
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25℃) I_F=20 mA Note 2
Output PWM frequency	F_{PWM}	100	200	20K	Hz	
Duty ratio	--	5	--	100	%	

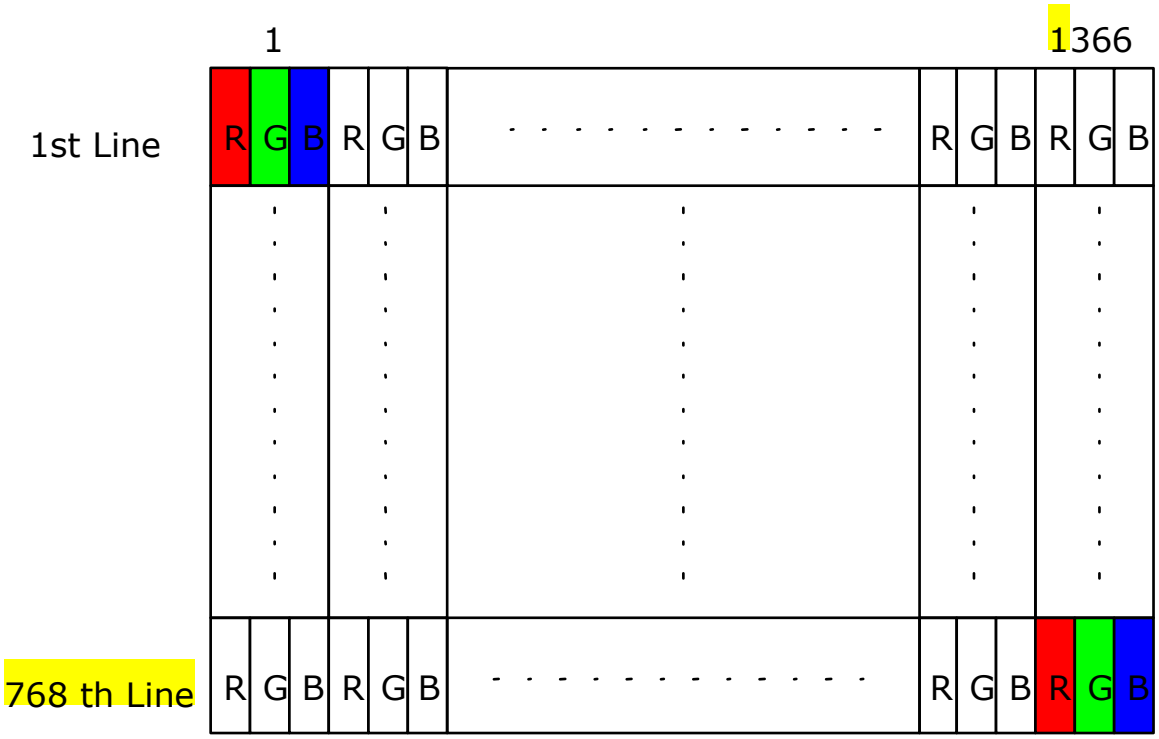
Note 1: Calculator value for reference $I_F \times V_F = P$

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

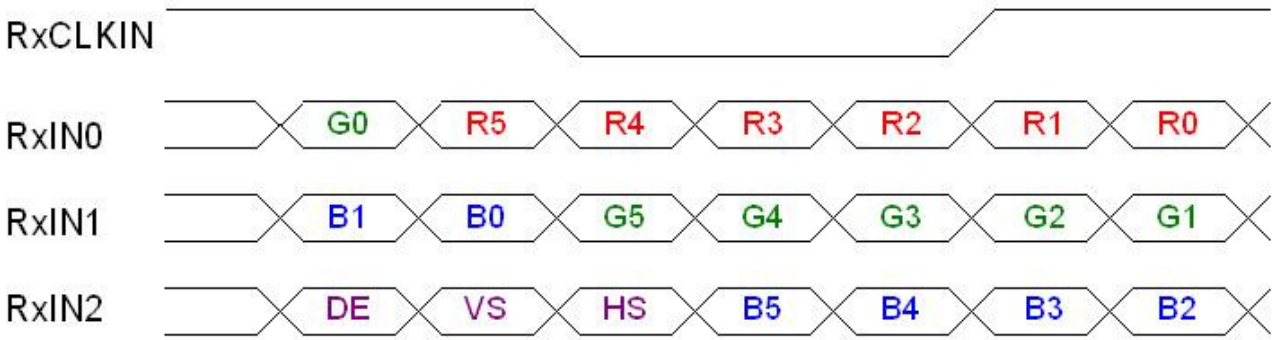
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



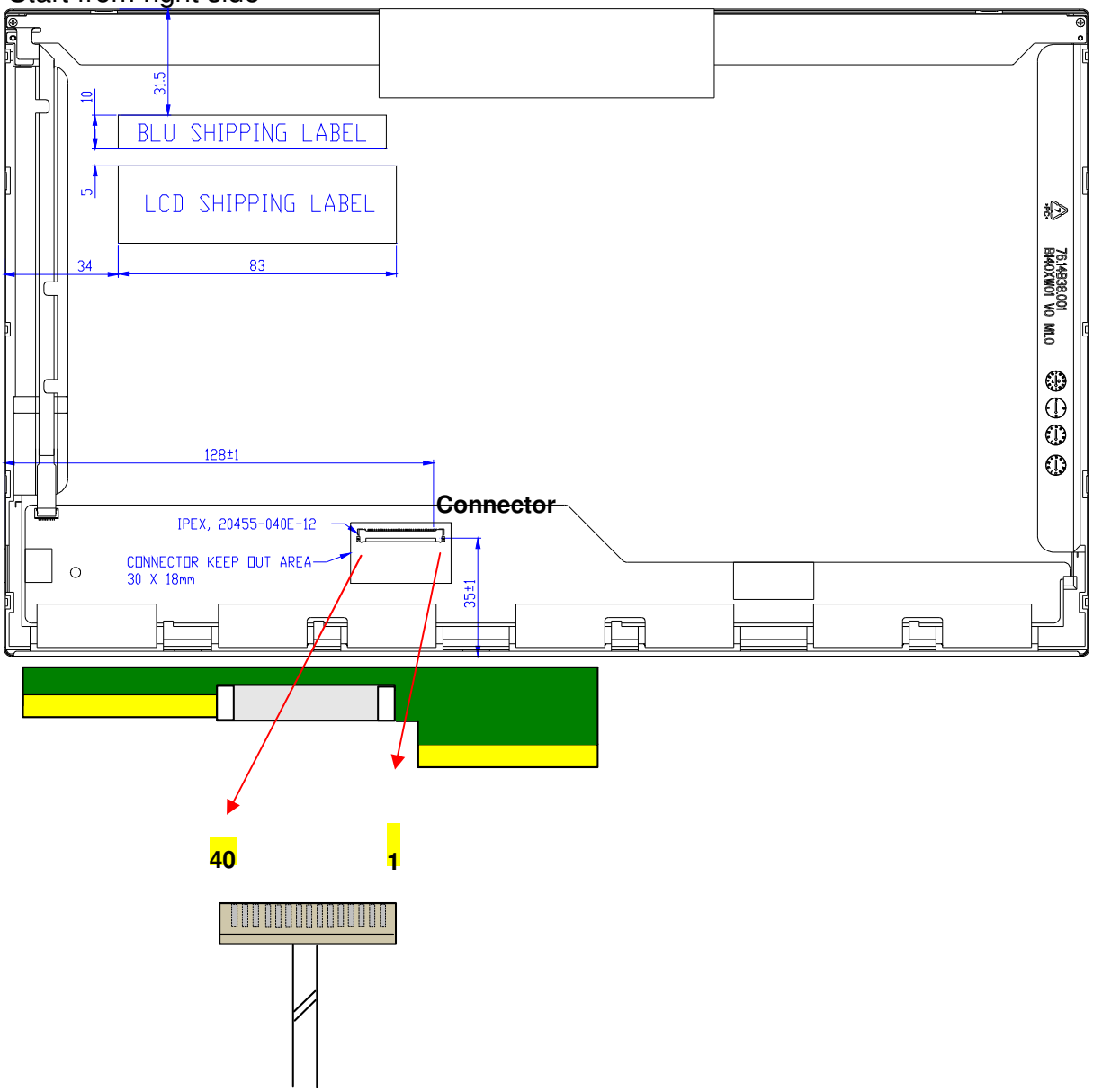
Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface and Pin Assignment

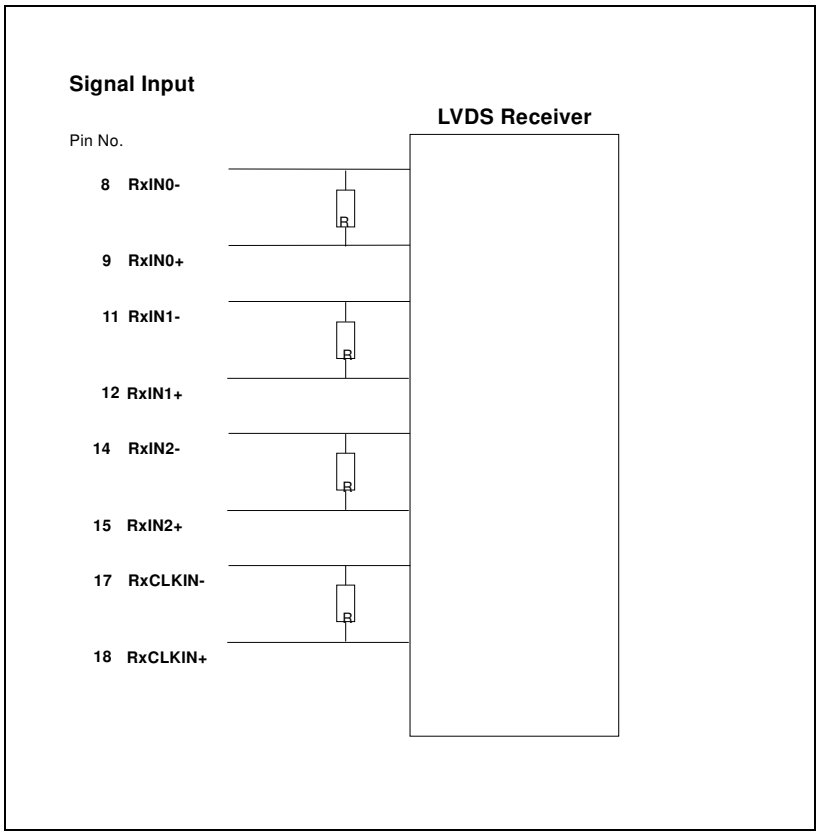
Pin	Signal	Description
1	NC	No Connection (Reserve)
2	VDD	PowerSupply,3.3V(typical)
3	VDD	PowerSupply,3.3V(typical)
4	VEEDID	DDC 3.3Vpower
5	TEST	PanelSelfTest-BIST
6	ClkEEDID	DDCClock
7	DATAEEDID	DDCData
8	Rin0-	-LVDS differential data input(R0-R5,G0)(oddpixels)
9	Rin0+	+LVDSdifferential data input(R0-R5,G0)(oddpixels)
10	VSS	Ground–Shield
11	Rin1-	-LVDSdifferential data input(G1-G5,B0-B1)(oddpixels)
12	Rin1+	+LVDSdifferential data input(G1-G5,B0-B1)(oddpixels)
13	VSS	Ground–Shield
14	Rin2-	-LVDSdifferential data input(B2-B5,HS,VS,DE)(oddpixels)
15	Rin2+	+LVDSdifferential data input(B2-B5,HS,VS,DE)(oddpixels)
16	VSS	Ground–Shield
17	ClkIN-	-LVDSdifferential clock input(oddpixels)
18	ClkIN+	+LVDSdifferential clock input(oddpixels)
19	VSS	Ground–Shield
20	NC	No Connection (Reserve)
21	NC	No Connection (Reserve)
22	GND	Ground–Shield
23	NC	No Connection (Reserve)
24	NC	No Connection (Reserve)
25	GND	Ground–Shield
26	NC	No Connection (Reserve)
27	NC	No Connection (Reserve)
28	GND	Ground–Shield
29	NC	No Connection (Reserve)
30	NC	No Connection (Reserve)
31	VSSLED	LED Ground
32	VSSLED	LED Ground
33	VSSLED	LED Ground
34	NC	No Connection (Reserve)
35	PWM	System PWM Signal Input
36	LED_EN	LED enable pin(+3.3V Input)
37	NC	No Connection (Reserve)
38	VLED	LED Power Supply 7V-21V
39	VLED	LED Power Supply 7V-21V
40	VLED	LED Power Supply 7V-21V

Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.

internal circuit of LVDS inputs are as following.
The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

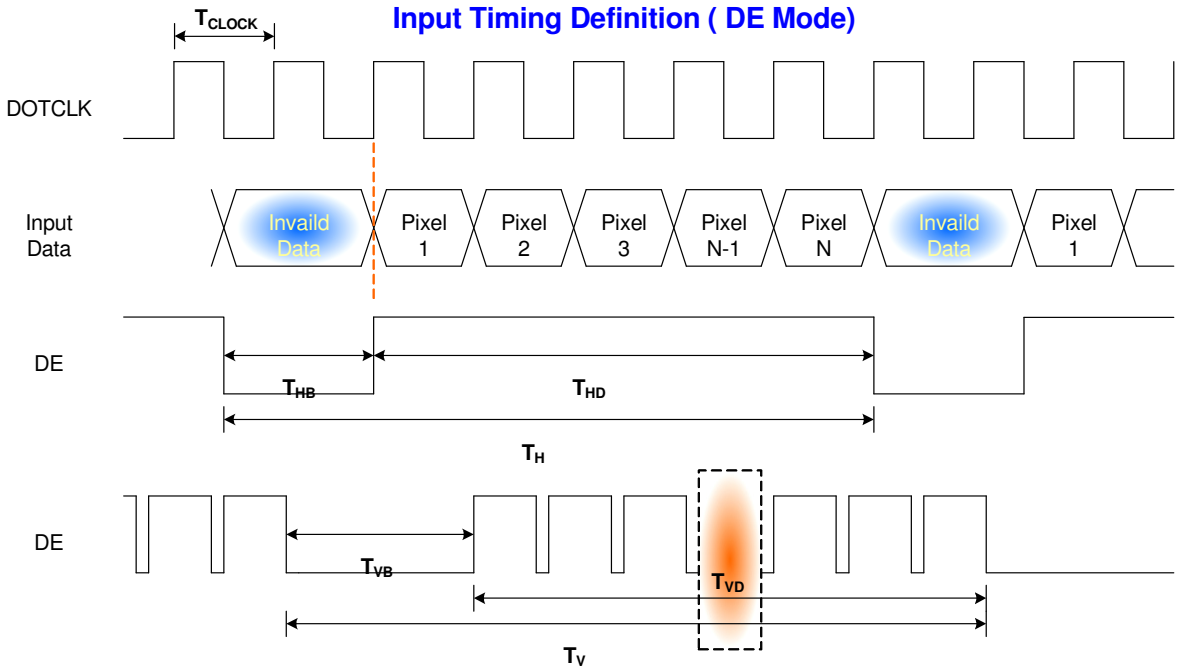
6.4.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		$1/T_{Clock}$	65	72	85	MHz
Vertical Section	Period	T_V	776	808	1023	T_{Line}
	Active	T_{VD}	768			
	Blanking	T_{VB}	8	40	255	
Horizontal Section	Period	T_H	1396	1606	2047	T_{Clock}
	Active	T_{HD}	1366			
	Blanking	T_{HB}	30	240	681	

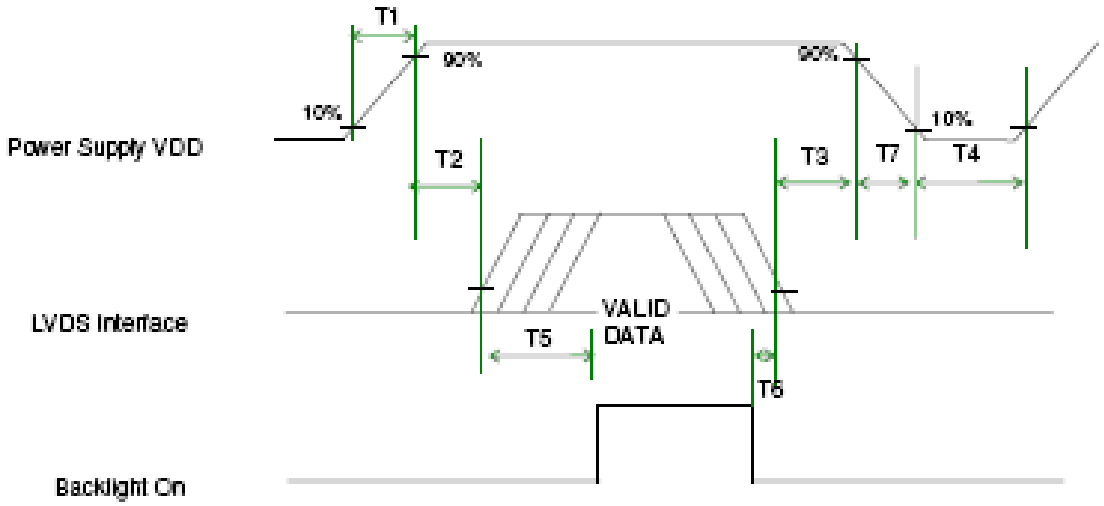
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

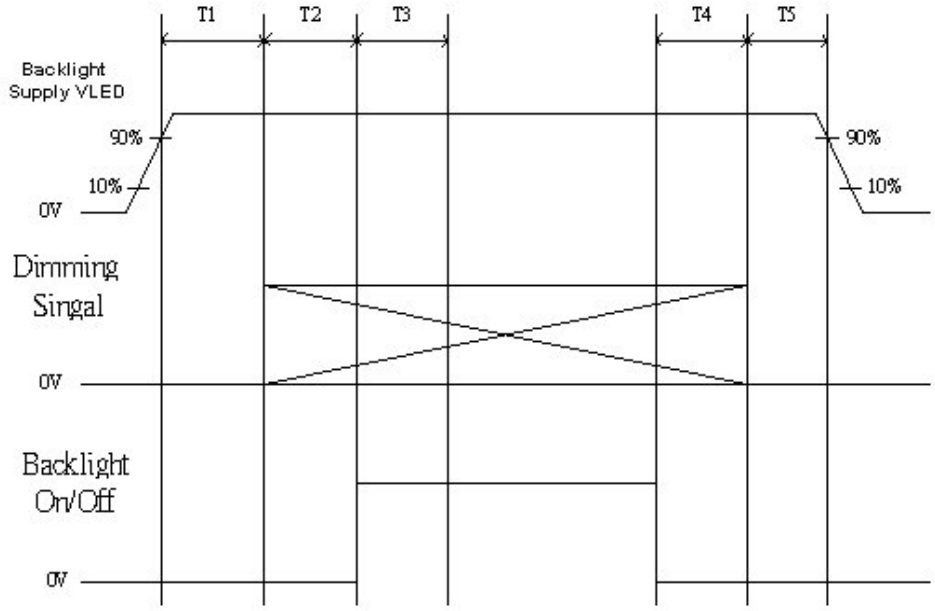
VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	50	
T3	0	-	50	
T4	400	-	-	
T5	200	-	-	
T6	200	-	-	
T7	0	-	10	

LED on/off sequence is as follows. Interface signals are also shown in the chart.



Symbol	Values			Unit
	Min	Typ	Max	
T1	10	---	---	ms
T2	10	---	---	
T3	50	---	---	
T4	0	---	---	
T5	10	---	---	

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	**IPEX**
Type / Part Number	**IPEX 20455-040E-12**
Mating Housing/Part Number	**IPEX 20453-040T-11**

8. LED Driving Specification

8.1 Connector Description

It is a intergrative interface and comibe into LVDS connector. The type and mating refer to section 7.

8.2 Pin Assignment

Ref. to 6.3

9. Vibration and Shock Test

9.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

9.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

10. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 300h	
Low Temperature Storage	Ta= -20℃, 250h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

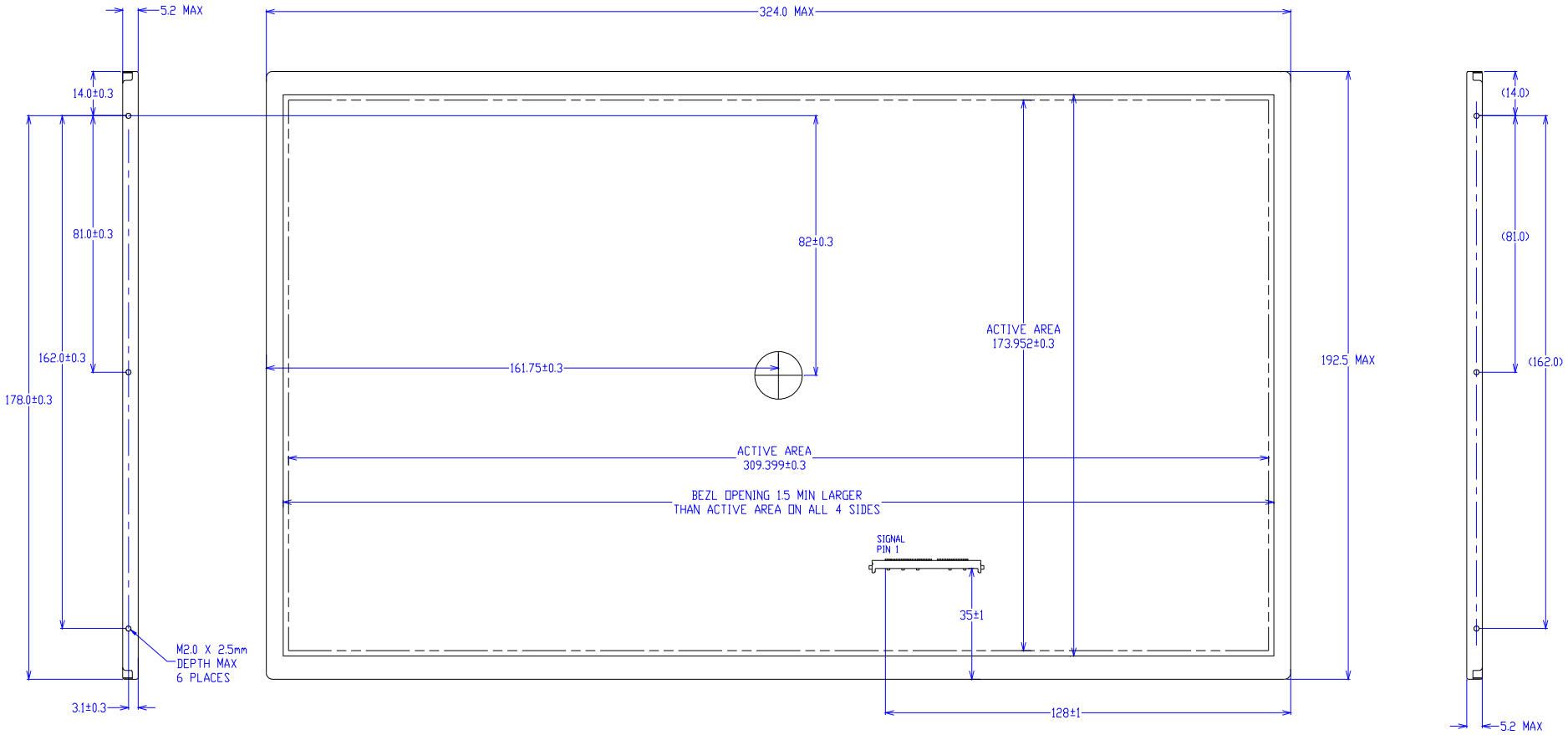
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

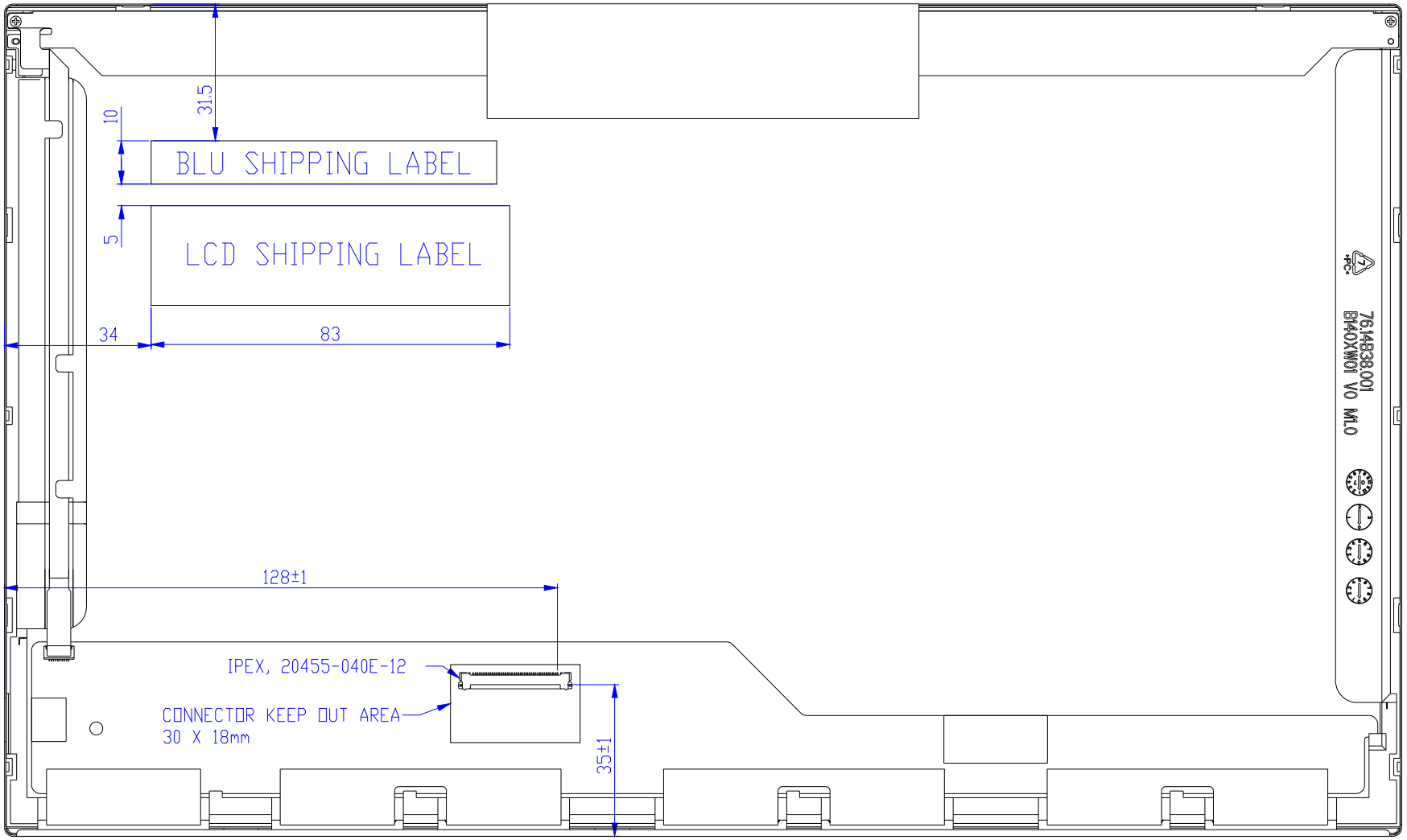
. Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

11. Mechanical Characteristics

11.1 LCM Outline Dimension



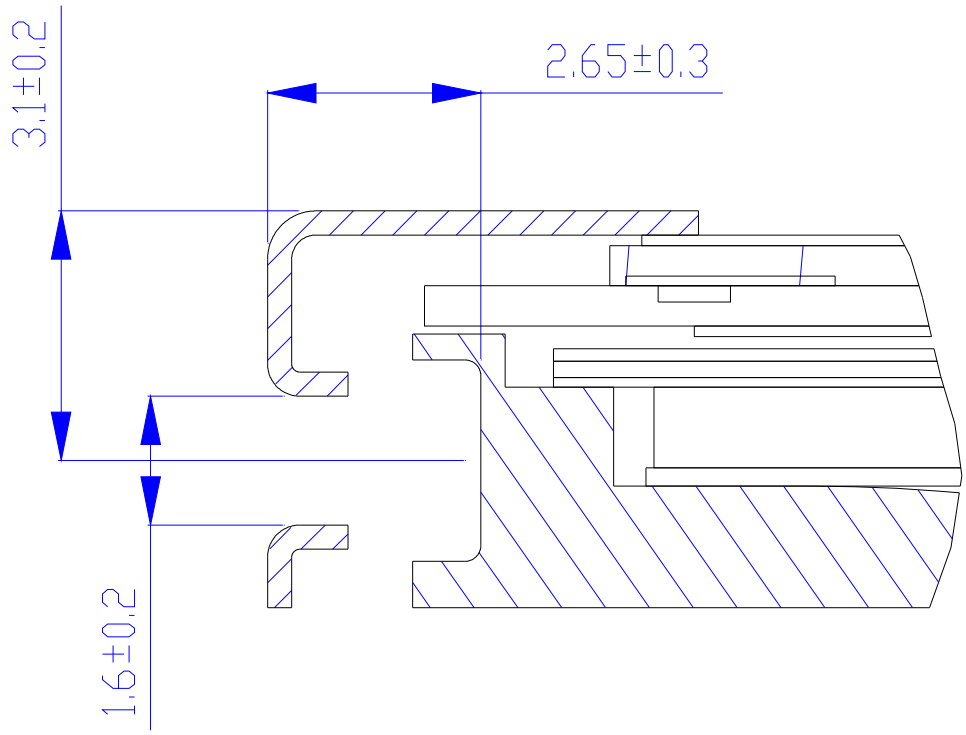


Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

11.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface = 2.35 mm (See drawing)

Screw hole center location, from front surface = 3.1 ± 0.2mm (See drawing)
Screw Torque: Maximum 2.5 kgf-cm



12. Shipping and Package

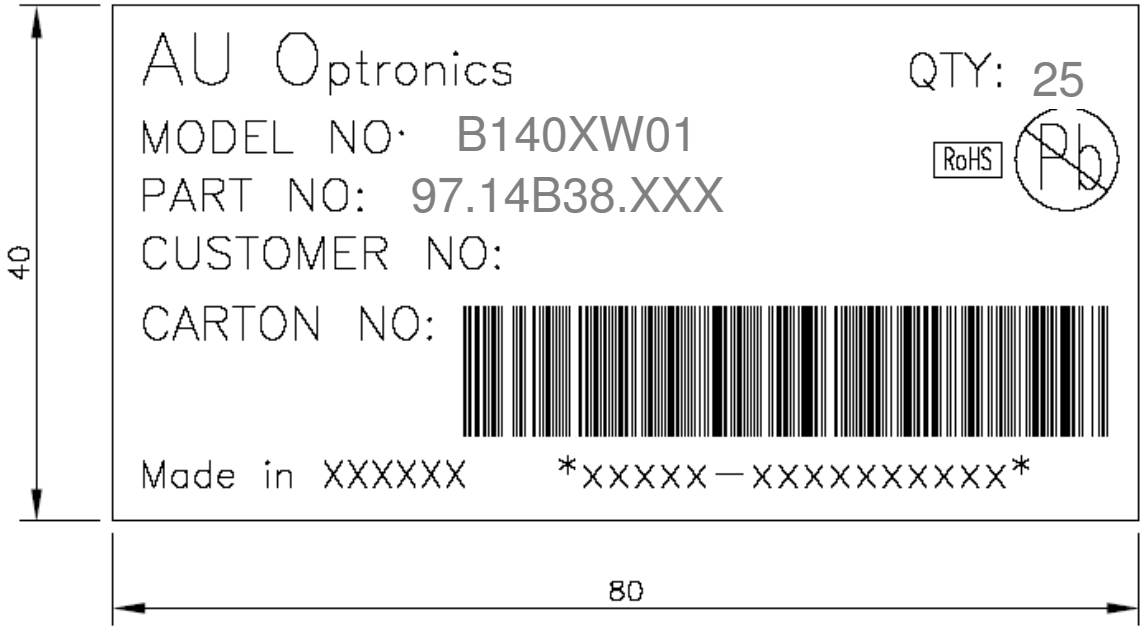
12.1 Shipping Label Format

Size :90 mm(length) ×35mm(width)

H/W	Source IC	Gate IC
0A	NOVATEK	NOVATEK

12.2 Carton package

Carton Label: 80mm * 40mm



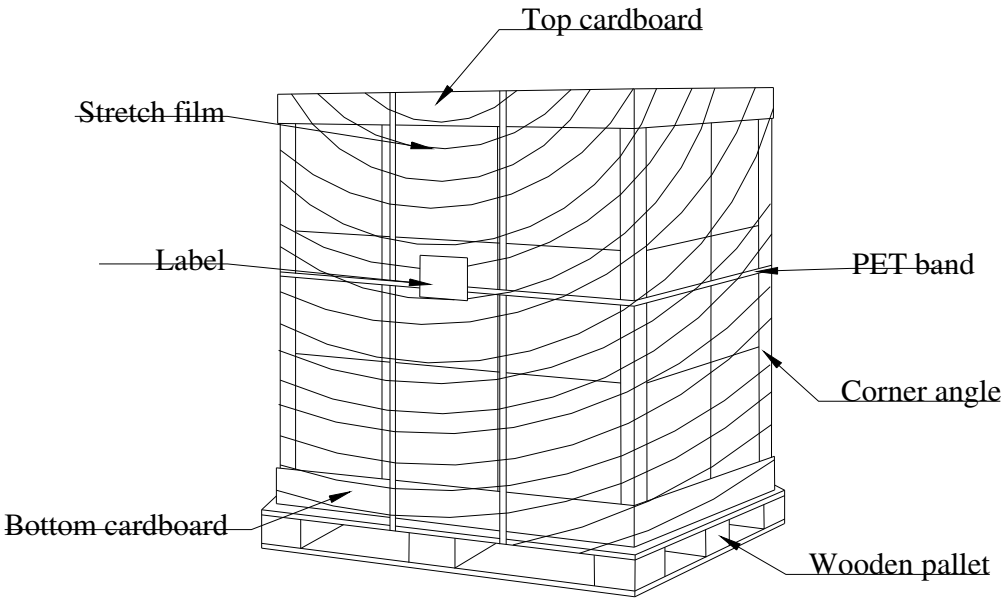
The outside dimension of carton is 454(L)mm* 376(W)mm* 302(H)mm, carton and cushion weight are 2200g

12.3 Shipping package of palletizing sequence

The outside dimension of Pallet is 114(L)mm* 83(W)mm* 13.8(H)mm

By air : 6 *4 layers, one pallet put 24 boxes, total 600 pcs module.

By sea : 6 *6 layers, one pallet put 36 boxes, total 900 pcs module.



13. Appendix: EDID description

B140XW01 V1 EDID Code

Address HEX	FUNCTION	Value HEX	Value BIN	Value DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	30	00110000	48
09	Compressed ASCII	AE	10101110	174
0A	Product Code	A0	10100000	160
0B	hex, LSB first	40	01000000	64
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	01	00000001	1
11	Year of manufacture	12	00010010	18
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	03	00000011	3
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	80	10000000	128
15	**Max H image size** *(rounded to cm)*	1F	00011111	31
16	**Max V image size** *(rounded to cm)*	11	00010001	17
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	EA	11101010	234
19	Red/green low bits **(Lower 2:2:2:2 bits)**	45	01000101	69
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	25	00100101	37
1B	Red x **(Upper 8 bits)**	9C	10011100	156
1C	Red y/ highER 8 bits	5B	01011011	91
1D	Green x	55	01010101	85
1E	Green y	9C	10011100	156
1F	Blue x	27	00100111	39
20	Blue y	19	00011001	25
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0

24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	20	00100000	32
37	Pixel Clock/10000 USB	1C	00011100	28
38	Horz active **Lower 8bits**	56	01010110	86
39	Horz blanking **Lower 8bits**	80	10000000	128
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	50	01010000	80
3B	Vertical Active **Lower 8bits**	00	00000000	0
3C	Vertical Blanking **Lower 8bits**	23	00100011	35
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30	00110000	48
3E	HorzSync. Offset	30	00110000	48
3F	HorzSync.Width	20	00100000	32
40	VertSync.Offset : VertSync.Width	36	00110110	54
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0
42	Horizontal Image Size **Lower 8bits**	35	00110101	53
43	Vertical Image Size **Lower 8bits**	AE	10101101	173
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0
46	Vertical Border *(zero for internal LCD)*	00	00000000	0
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24
48	Detailed timing/monitor	70	01110000	112
49	descriptor #2	17	00010111	23
4A		56	01010110	86

4B		80	10000000	128
4C		50	01010000	80
4D		00	00000000	0
4E		23	00100011	35
4F		30	00110000	48
50		30	00110000	48
51		20	00100000	32
52		36	00110110	54
53		00	00000000	0
54		35	00110101	53
55		AE	10101110	174
56		10	00010000	16
57		00	00000000	0
58		00	00000000	0
59		18	00011000	24
5A	Detailed timing/monitor	00	00000000	0
5B	descriptor #3	00	00000000	0
5C		00	00000000	0
5D		0F	00001111	15
5E		00	00000000	0
5F	Manufacture	8C	10001100	140
60	Manufacture	09	00001001	9
61	Manufacture	32	01100010	50
62		8C	10001100	140
63		09	00001001	9
64		28	00101000	40
65		16	00010110	22
66		09	00001001	9
67		00	00000000	0
68		06	00000110	6
69		AF	10101111	175
6A		56	01010110	86
6B		31	00110001	49
6C	Detailed timing/monitor	00	00000000	0
6D	descriptor #4	00	00000000	0
6E		00	00000000	0
6F		FE	11111110	254
70		00	00000000	0
71	Manufacture P/N	42	01000010	66

72	Manufacture P/N	31	00110001	49
73	Manufacture P/N	34	00110100	52
74	Manufacture P/N	30	00110000	48
75	Manufacture P/N	58	01011000	88
76	Manufacture P/N	57	01010111	87
77	Manufacture P/N	30	00110000	48
78	Manufacture P/N	31	00110001	49
79	Manufacture P/N	20	00100000	32
7A	Manufacture P/N	56	01010110	86
7B	Manufacture P/N	31	00110001	489
7C		20	00100000	32
7D		0A	00001010	10
7E	Extension Flag	00	00000000	0
7F	Checksum	5E	01011110	94