Version	7.0
Total pages	21
Date	2007.12.12

Product Specification

Color TFT-LCD module

MODEL NAME: A085FW01 V5

(.....) Preliminary Specification

(◆) Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	25/Sep/2006		First draft.
1.0	17/May/2007	6	Update lamp starting voltage
2.0	11/Jul/2007	8	Add a note for power on/off sequence
3.0	17/Jul/2007	12	Update packing form
4.0	26/Jul/2007		Change to final version on the cover page
5.0	30/Jul/2007	5	Update Absolute maximum ratings - Operating temperature & storage temperature
6.0	25/Oct/2007	6	Update backlight driving conditions – lamp voltage & current
7.0	17/Dec/2007	7	Modify Vcc value to Typ.3.3V/Max3.6V.(for 3.3V system) Modify Vcc value to Typ. 5V/Max5.25V.(for 5V system)

Contents:

A. Physical specification **P3**

B. Electrical specifications **P4**

1. Pin assignment **P4**

a. TFT-LCD panel driving section **P4**

b. Backlight driving section **P5**

2. Absolute maximum ratings **P5**

3. Electrical characteristics **P6**

a. Typical operating conditions **P6**

b. Current consumption **P6**

c. Backlight driving conditions **P6**

4. AC Timing **P7**

a. Timing conditions **P7**

b. Timing diagram **P7**

5. Power Sequence **P8**

C. Optical specifications **P9**

D. Reliability test items **P11**

E. Packing form **P12**

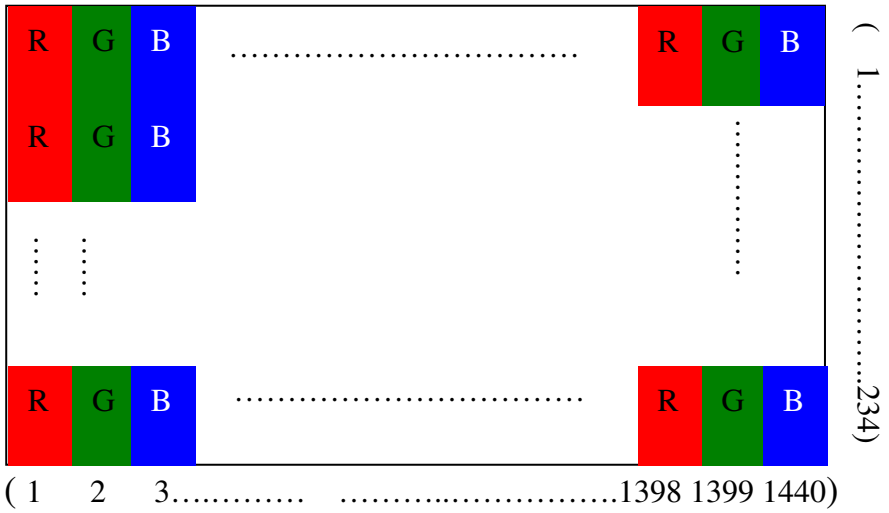
Appendix:

Fig.1-(a) Outline dimension of TFT-LCD module(Front side). **P13**
Fig.1-(b) Outline dimension of TFT-LCD module(Back side). **P14**
Fig.2 Sampling clock timing. **P15**
Fig.3 Horizontal display timing range. **P16**
Fig.4-(a) Horizontal timing. **P17**
Fig.4-(b) Detail horizontal timing. **P18**
Fig.5 Vertical shift clock timing. **P19**
Fig.6-(a) Vertical timing (From up to down). **P20**
Fig.6-(b) Vertical timing (From down to up) **P21**

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution(dot)	480RGB(W)×234(H)	
2	Active area(mm)	187.2(W)×105.3(H)	
3	Dot pitch(mm)	0.130(W)×0.450(H)	
4	Color configuration	R. G. B. stripe	Note 1
5	Overall dimension(mm)	199.0(W)×119.0(H)×5.8(D)	Note 2
6	Weight(g)	232 ±10	
7	Surface treatment	Anti-Glare	
8	Backlight unit	CCFL	

Note 1: Below figure shows the dot stripe arrangement.



Note 2: Refer to Fig. 1

B. Electrical specifications

1.Pin assignment

a. TFT-LCD panel driving section

Pin no	Symbol	I/O	Description	Remark
1	GND	-	Ground for logic circuit	
2	V_{CC}	I	Supply voltage of logic control circuit for scan driver	
3	V_{GL}	I	Negative power for scan driver	
4	V_{GH}	I	Positive power for scan driver	
5	STVD	I/O	Vertical start pulse	Note 1
6	STVU	I/O	Vertical start pulse	Note 1
7	CKV	I	Shift clock input for scan driver	
8	U/D	I	UP/DOWN scan control input	Note 1,2
9	OEV	I	Output enable input for scan driver	
10	VCOM	I	Common electrode driving signal	
11	VCOM	I	Common electrode driving signal	
12	L/R	I	LEFT/RIGHT scan control input	Note 1,2
13	MOD	I	Sequential sampling and simultaneous sampling setting	Note 3
14	OEH	I	Output enable input for data driver	
15	STHL	I/O	Start pulse for horizontal scan line	Note 1
16	STHR	I/O	Start pulse for horizontal scan line	Note 1
17	CPH3	I	Sampling and shifting clock pulse for data driver	
18	CPH2	I	Sampling and shifting clock pulse for data driver	
19	CPH1	I	Sampling and shifting clock pulse for data driver	
20	V_{CC}	I	Supply voltage of logic control circuit for data driver	
21	GND	-	Ground for logic circuit	
22	VR	I	Alternated video signal input(Red)	
23	VG	I	Alternated video signal input(Green)	
24	VB	I	Alternated video signal input(Blue)	
25	AV_{DD}	I	Supply voltage for analog circuit	
26	AV_{SS}	-	Ground for analog circuit	

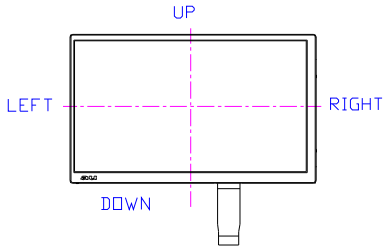
Note 1: Selection of scanning mode (please refer to the following table)

Setting of scan control input		IN/OUT state for start pulse				Scanning direction
U/D	L/R	STVD	STVU	STHR	STHL	
GND	V_{CC}	OUT	IN	OUT	IN	From up to down, and from left to right.
V_{CC}	GND	IN	OUT	IN	OUT	From down to up, and from right to left.
GND	GND	OUT	IN	IN	OUT	From up to down, and from right to left.
V_{CC}	V_{CC}	IN	OUT	OUT	IN	From down to up, and from left to right.

IN: Input; OUT: Output.

Note 2: Definition of scanning direction.

Refer to figure as below:



Note 3: MOD = H: Simultaneous sampling.

MOD = L: Sequential sampling.

Please set CPH2 and CPH3 to GND when MOD = H.

b. Backlight driving section (Refer to Figure 1)

No.	Symbol	I/O	Description	Remark
1	HI	I	Power supply for backlight unit (High voltage)	--
2	GND	-	Ground for backlight unit	--

2. Absolute maximum ratings(Note 3)

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V_{CC}	GND=0	-0.3	7	V	
	AV_{DD}	AV_{SS}=0	-0.3	7	V	
	V_{GH}	GND=0	-0.3	18	V	
	V_{GL}		-15	0.3	V	
	$V_{GH}-V_{GL}$		-	33	V	
Input signal voltage	V_i		-0.3	AV_{DD}+0.3	V	Note 1
	V_I		-0.3	V_{CC}+0.3	V	Note 2
	VCOM		-2.9	5.2	V	
Operating temperature	Topa	--	-10	60	℃	Ambient Temperature
Storage temperature	Tstg	--	-20	70	℃	Ambient Temperature

Note 1: VR, VG, VB.

Note 2: STHL, STHR, OEH, L/R, CPH1~CPH3, STVD, STVU, OEV, CKV, U/D.

Note 3: Functional operation should be restricted under normal ambient temperature.

3. Electrical characteristics

a. Typical operating conditions (GND=AVss=0V, Note 3)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		V_{CC}	3	**3.3**	**3.6**	V	For 3.3V interface. Note 4
		V_{CC}	4.5	**5**	**5.25**	V	For 5V interface. Note 5
		AV_{DD}	4.5	5	5.5	V	
		V_{GH}	14.3	15	15.7	V	
		V_{GL}	-10.5	-10	-9.5	V	
Video signal amplitude (VR,VG,VB)		V_{iA}	0.4	-	AV_{DD}-0.4	V	Note 1
		V_{iAC}	-	3	-	V	AC component
		V_{iDC}	-	AV_{DD}/2	-	V	DC component
VCOM		V_{CAC}	5.3	5.6	5.9	Vp-p	AC component
		V_{CDC}	1.6	1.9	2.2	V	DC component
Input signal voltage	H Level	V_{IH}	0.8 V_{CC}	-	V_{CC}	V	Note 2
	L Level	V_{IL}	0	-	0.2 V_{CC}	V	

Note 1: Refer to Fig.4- (a).
Note 2: STHL, STHR, OEH, L/R, CPH1~CPH3, STVD, STVU, OEV, CKV, U/D.
Note 3: Be sure to apply GND, V_{CC} and V_{GL} to the LCD first, and then apply V_{GH}.
Note 4: STH,OEH,L/R CPH1~CHP3,STV,CKV,OEV,U/D,Vih>0.8/Vcc=0.8*3.6=2.88V
Note 5: STH,OEH,L/R CPH1~CHP3,STV,CKV,OEV,U/D,Vih>0.8/Vcc=0.8*5.25=4.2V

b. Current consumption (GND=AVss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Current for driver	I_{GH}	V_{GH}=15V	-	0.20	0.5	mA	
	I_{GL}	V_{GL}=-10V	-	0.20	0.5	mA	
	I_{CC}	V_{CC}=5V	-	3.0	6.0	mA	
	I_{DD}	AV_{DD}=5V	-	15.0	30	mA	

c. Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	632 (8.0mA)	677 (6.5mA)	757 (4.0mA)	Vrms	Note 1
Lamp current	I_L	4.0	6.5	8.0	mArms	Note 1
Frequency	F_L	-	60	80	kHz	Note 4
Lamp starting voltage	V_S	-	-	1,180	Vrms	Note 1,5
		-	-	1,540	Vrms	Note 2,5
		-	-	1,780	Vrms	Note 3,5,7
Lamp life time		15,000	-	-	Hr	Note 6

Note 1: Ta = 25℃ and at normal environment
Note 2: Ta = 0℃ and at normal environment.
Note 3: Ta = -25℃.(Product does not guarantee dark discharge start up)
Note 4: The lamp frequency should be selected as different as possible from display horizontal synchronous signal to avoid interference.
Note 5: For starting the backlight unit, the output voltage of DC/AC's transformer should be larger than the

maximum lamp starting voltage. Vs value is measured from connector of product. The value is for reference.

Note 6: The" Lamp life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃, I_L=6.5mA.

Note 7: The value is only for reference.

4. AC Timing

a. Timing conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
High and low level pulse width	t_{CPH}	99	103	107	ns	CPH1~CPH3
CPH pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3
CPH pulse delay	t_{C12} t_{C23} t_{C31}	30	t_{CPH}/3	t_{CPH}/2	ns	CPH1~CPH3
STH setup time	t_{SUH}	20	-	-	ns	STHR, STHL
STH hold time	t_{HDH}	20	-	-	Ns	STHR, STHL
STH pulse width	t_{STH}	-	1	-	t_{CPH}	STHR, STHL
STH period	t_H	61.5	63.5	65.5	μs	STHR, STHL
OEH pulse width	t_{OEH}	-	1.22	-	μs	OEH
Sample and hold disable time	t_{DIS1}	-	8.28	-	μs	
OEV pulse width	t_{OEV}	-	5.40	-	μs	OEV
CKV pulse width	t_{CKV}	-	4.18	-	μs	CKV
Clean enable time	t_{DIS2}	-	3.74	-	μs	
Horizontal display start	t_{SH}	-	0	-	T_{CPH}/3	
Horizontal display timing range	t_{DH}	-	1440	-	T_{CPH}/3	
STV setup time	t_{SUV}	400	-	-	ns	STVU, STVD
STV hold time	t_{HDV}	400	-	-	ns	STVU, STVD
STV pulse width	t_{STV}	-	-	1	t_H	STVU, STVD
Horizontal lines per field	t_V	256	262	268	t_H	Note 2
Vertical display start	t_{SV}		3	-	t_H	
Vertical display timing range	t_{DV}		234	-	t_H	
VCOM rising time	t_{rCOM}		-	5	μs	
VCOM falling time	t_{fCOM}		-	5	μs	
VCOM delay time	t_{DCOM}		-	3	μs	
RGB delay time	t_{DRGB}		-	1	μs	

Note 1: For all of the logic signals.

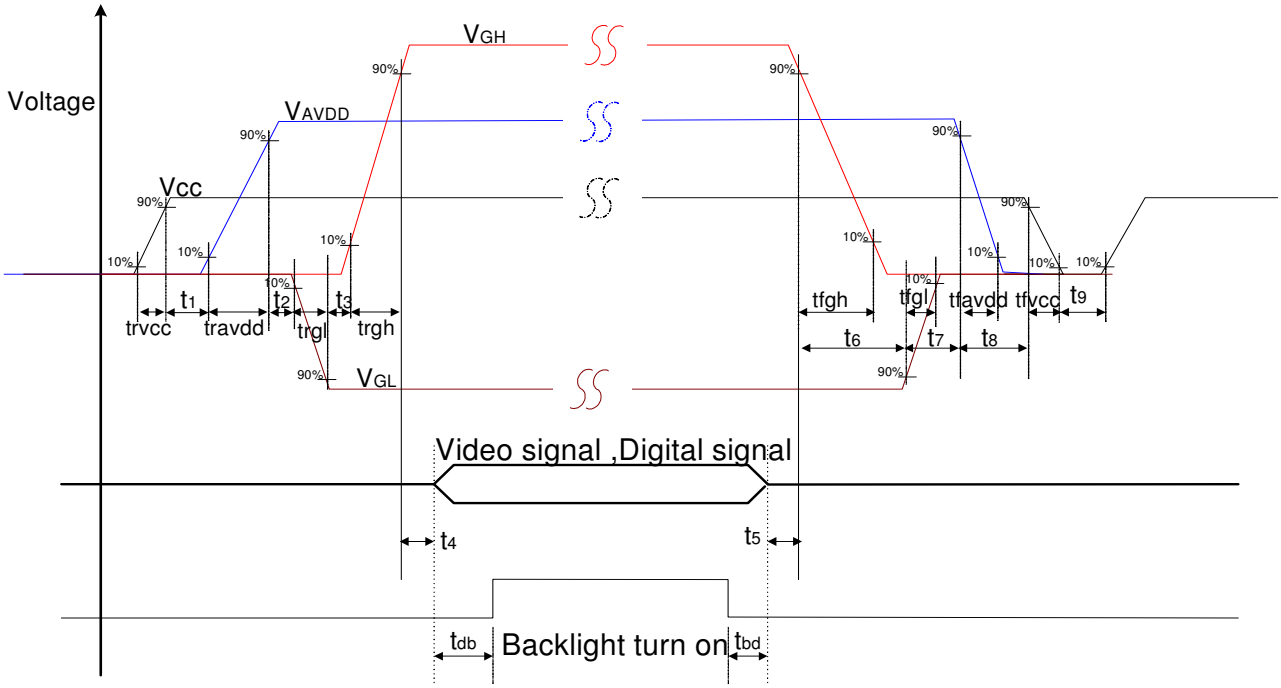
Note 2: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b. Timing diagram

Please refer to the attached drawing, from Fig.2 to Fig.6.

5. Power Sequence

Sequence for power on/off and Signal on/off



trvcc□15ms(From 10%VCC to 90%VCC ,when VCC is low to high)

travdd□15ms(From 10%VAVDD to 90%VAVDD ,when VAVDD is low to high)

trgh□15ms(From 10%VGH to 90%VGH ,when VGH is low to high)

trgl□15ms(From 10%VGL to 90%VGL ,when VGL is low to high)

tfvcc□20ms(From 90%VCC to 10%VCC ,when VCC is high to low)

tfavdd□20ms(From 90%VAVDD to 10%VAVDD ,when VAVDD is high to low)

tfgh□20ms(From 90%VGH to 10%VGH ,when VGH is high to low)

tfgl□20ms(From 90%VGL to 10%VGL ,when VGL is high to low)

0□t1□10ms(From 90%Vcc to 10% VAVDD , when VCC is low to high)

0□t2□10ms(From 90%VAVDD to 10% VGL , when VCC is low to high)

0□t3□10ms(From 90%VGL to 10% VGH , when VCC is low to high)

0□t4□10ms(From 90%VGH to video signal start ,when VGH is low to high)

0□t5□10ms(From video signal end to 90%VGH ,when VGH is low to high)

t6□10ms(From 10%VGH to 90% VGL ,when VCC is high to low)

t7□10ms(From 10%VGL to 90% VAVDD , when VCC is high to low)

t8□10ms(From 10%VAVDD to 90% VCC , when VCC is high to low)

t9□0.4s(From 10%VCC is H → L to 10%VCC is L → H)

0□tdb□10ms(From video signal start to backlight on)

0□tbd□10ms(From backlight off to video signal end)

Note: Please follow above power off sequence or turn off all power simultaneously.

C. Optical specification (Note 1, Note 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise Fall	Tr Tf	θ =0°	- -	12 18	24 36	ms ms	Note 3,5
Contrast ratio		CR	At optimized Viewing angle	200	300	-		Note 4, 5
Viewing angle	Top Bottom Left Right		CR≧10	40 55 55 55	50 65 65 65	- - - -	deg.	Note 5, 6
Brightness		Y_L	I_L=6.5mA, 25℃	210	250	-	cd/m^2	Note 7
White chromaticity		X	θ =0°	0.27	0.32	0.37		Note 7
		Y	θ =0°	0.29	0.34	0.39		

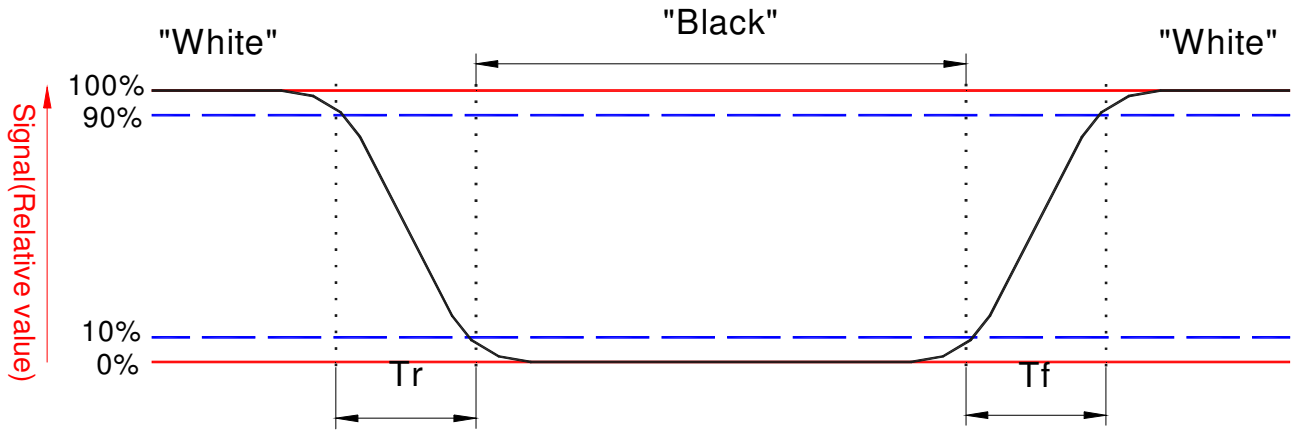
Note 1 : To be measured in the dark room. Ambient temperature =25℃, and lamp current I_L = 6.5 mArms. DC/AC inverter driving frequency: 60 kHz.

Note 2 :To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-5, after 15 minutes operation.

Note 3. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 5. White $Vi=V_{i50} + 1.5V$

Black $Vi=V_{i50} \pm 2.0V$

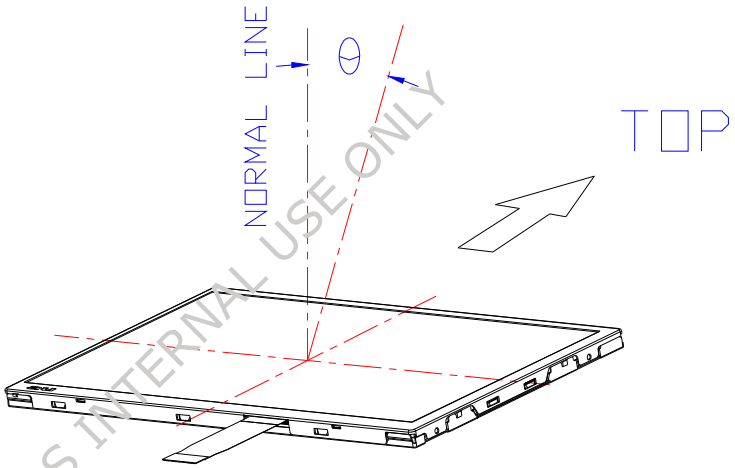
"±" means that the analog input signal swings in phase with V_{COM} signal.

"$\overline{+}$" means that the analog input signal swings out of phase with V_{COM} signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6. Definition of viewing angle, Refer to figure as below.



Note 7. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

D. Reliability test conditions (Note 2):

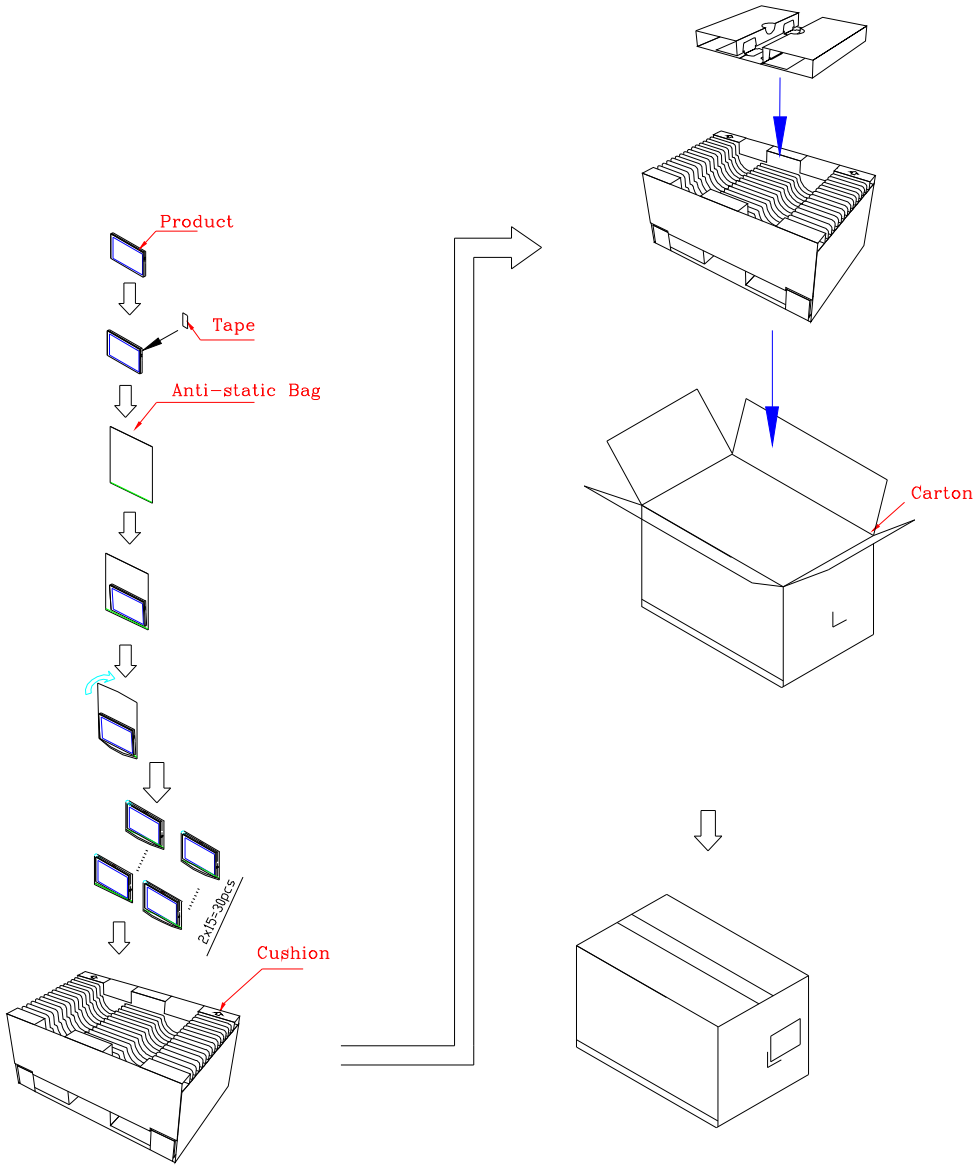
No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70℃ 200Hrs	
2	Low temperature storage	Ta= -20℃ 200Hrs	
3	High temperature operation	Tp= 60℃ 200Hrs	
4	Low temperature operation	Ta= -10℃ 200Hrs	
5	High temperature and high humidity	Tp= 50℃, 80% RH 200Hrs	Operation
6	Heat shock	-30℃~70℃/ 50 cycles 1Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10 ~ 55 ~ 10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	JIS C7021, A-10 Condition A
9	Mechanical shock	100G, 6ms, ±X,±Y,±Z 3 times for each direction	JIS C7021, A-7 Condition C
10	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	JIS Z0202

Note1: Ta: Ambient Temperature.

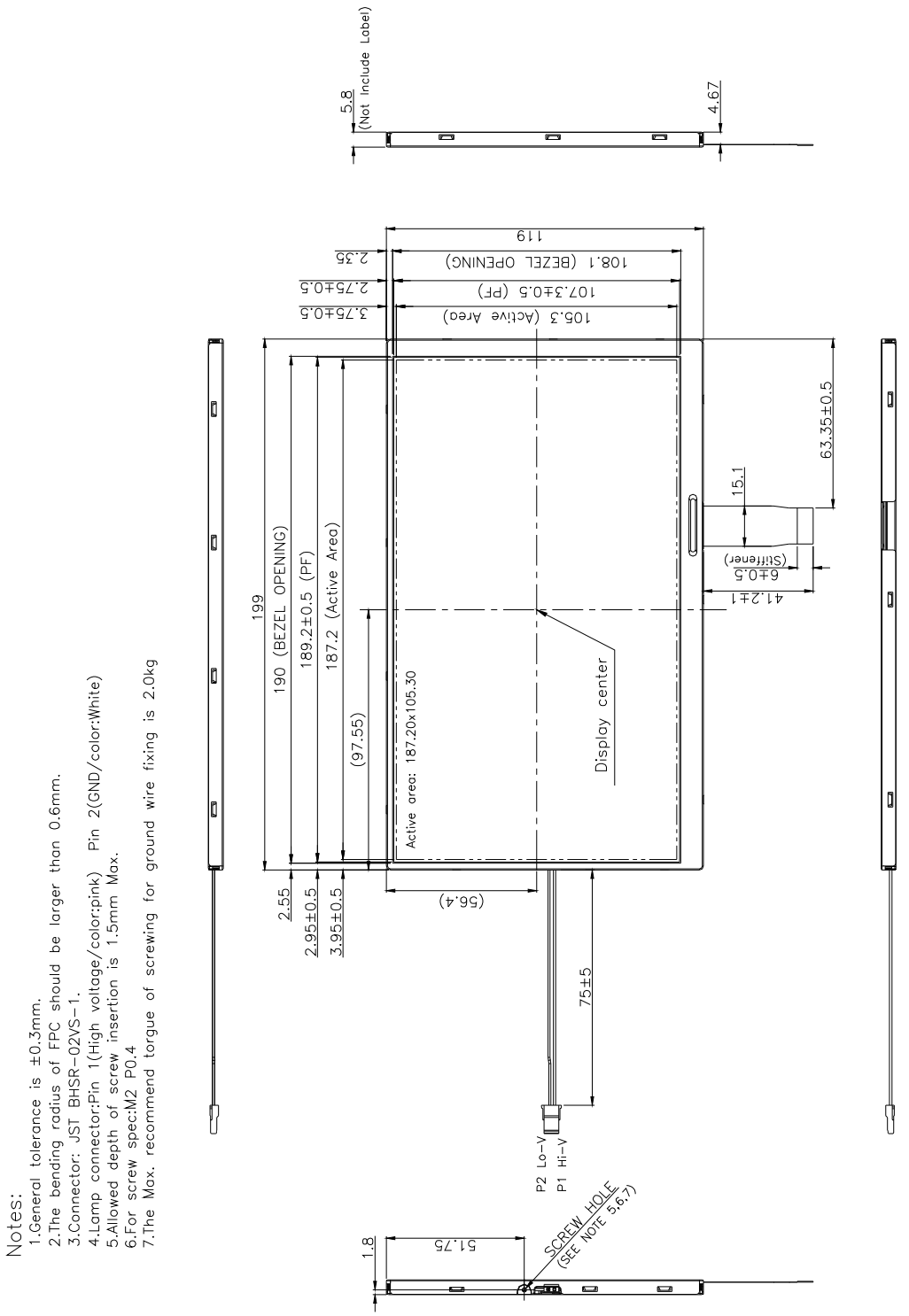
Note2: Tp: Panel Surface Temperature

Note3: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

E. Packing form



MAX. CAPACITY:30 MODULES
MAX. WEIGHT:15 KG
CARTON OUTLINE: 520mm*340mm*250mm
CARTON STACK UP 5 LAYERS



Notes:
1.General tolerance is ±0.3mm.
2.The bending radius of FPC should be larger than 0.6mm.
3.Connector: JST BHSR-02VS-1.
4.Lamp connector:Pin 1(High voltage/color:pink) Pin 2(GND/color:White)
5.Allowed depth of screw insertion is 1.5mm Max.
6.For screw spec:M2 P0.4
7.The Max. recommend torque of screwing for ground wire fixing is 2.0kg

Fig.1-(a) Outline dimension of TFT-LCD module (Front side)

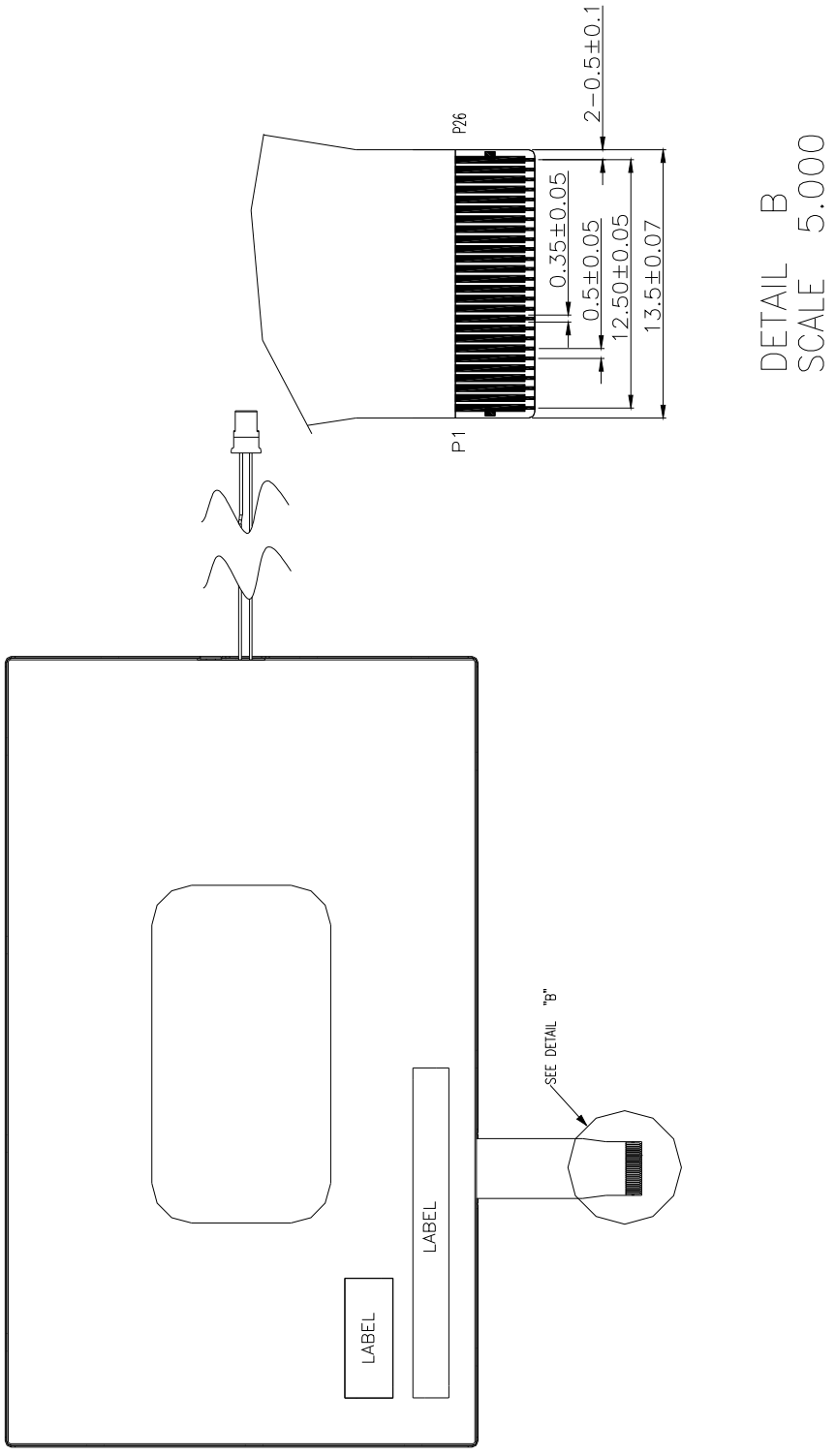


Fig.1-(b) Outline dimension of TFT-LCD module (Back side)

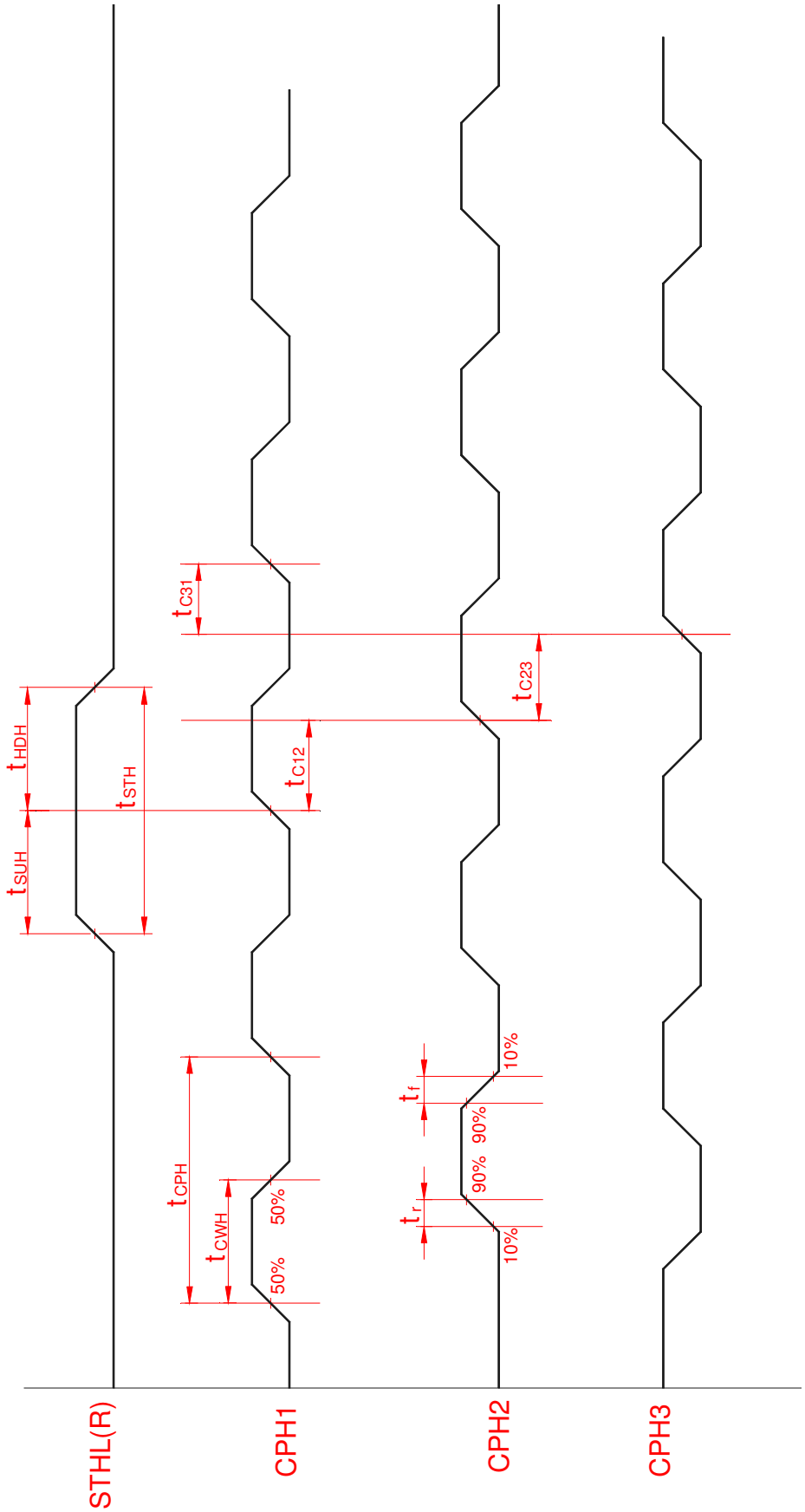


Fig.2 Sampling clock timing

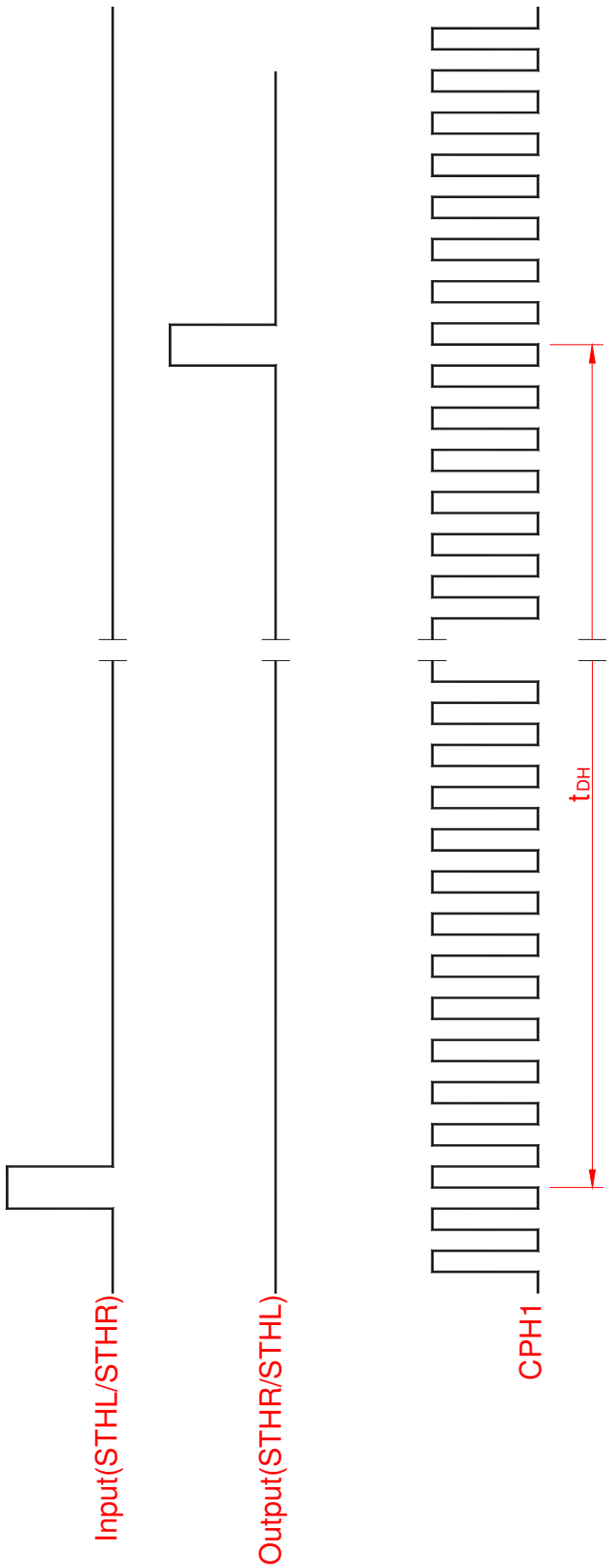


Fig.3 Horizontal display timing range

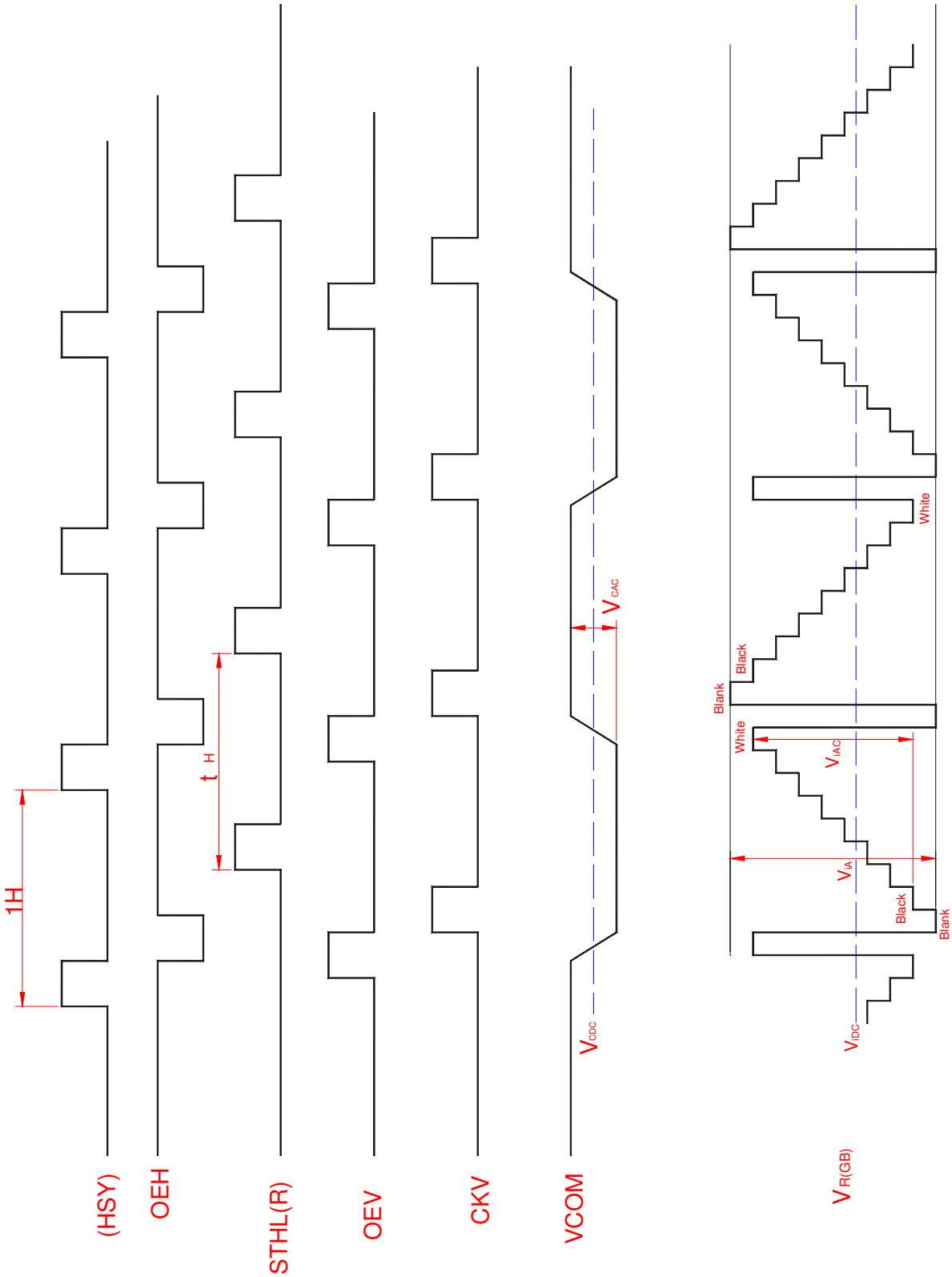
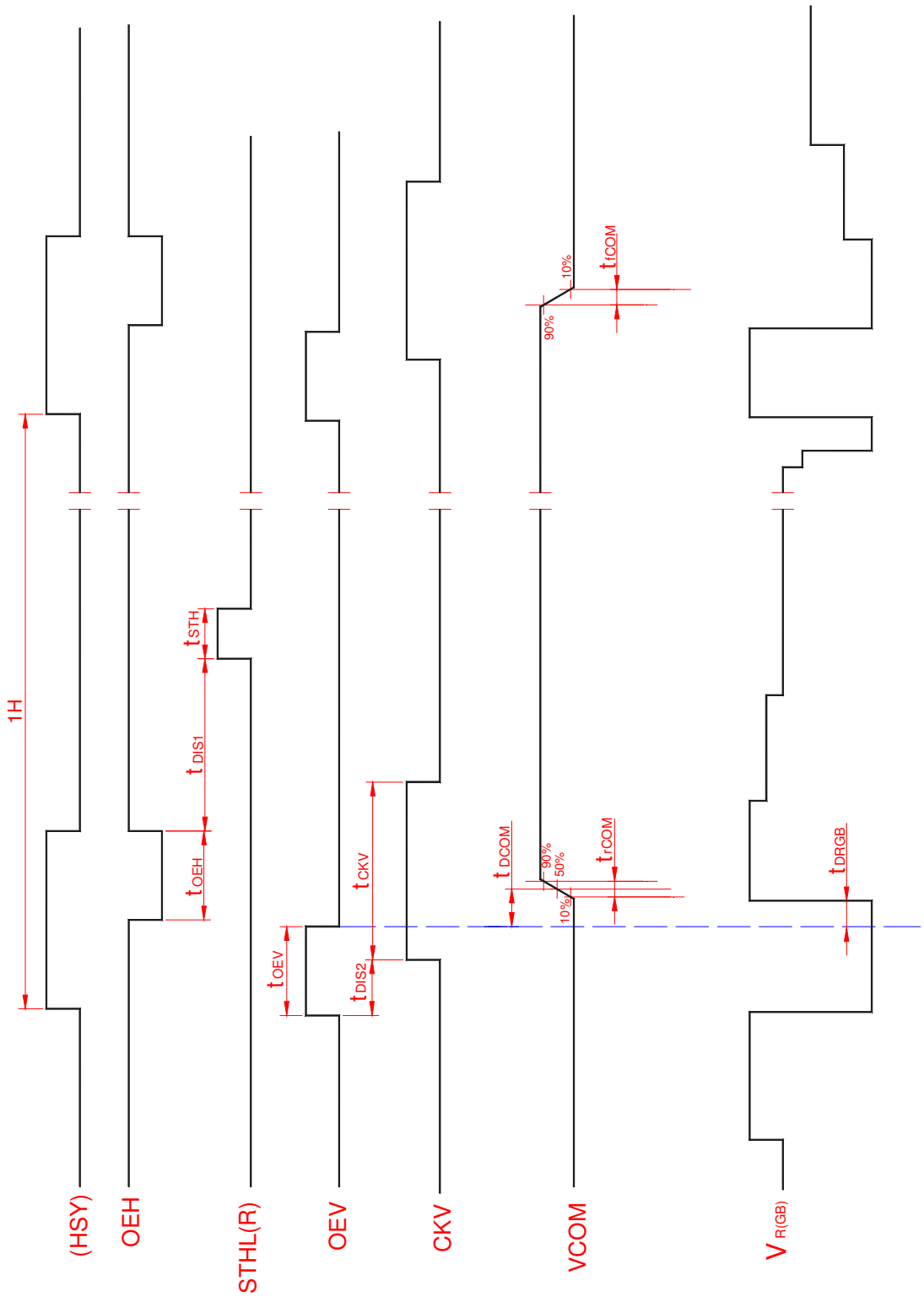


Fig.4-(a) Horizontal timing



Note: The falling edge of OEV should be synchronized with the falling edge of OEH

Fig.4-(b) Detail horizontal timing

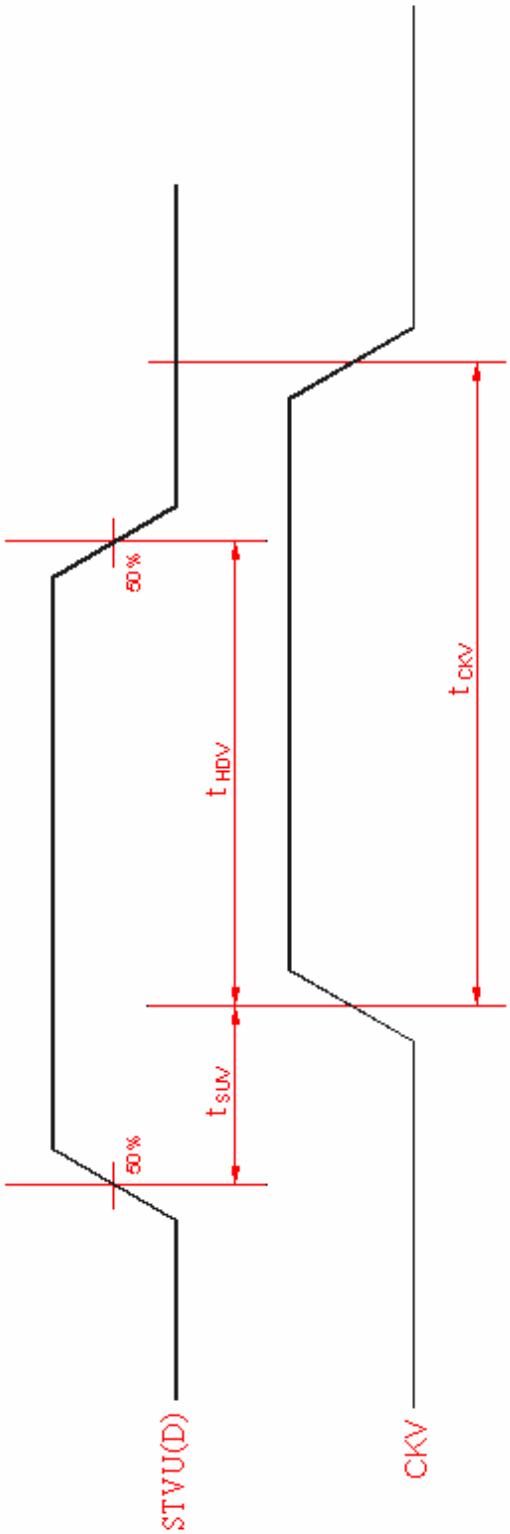


Fig.5 Vertical shift clock timing

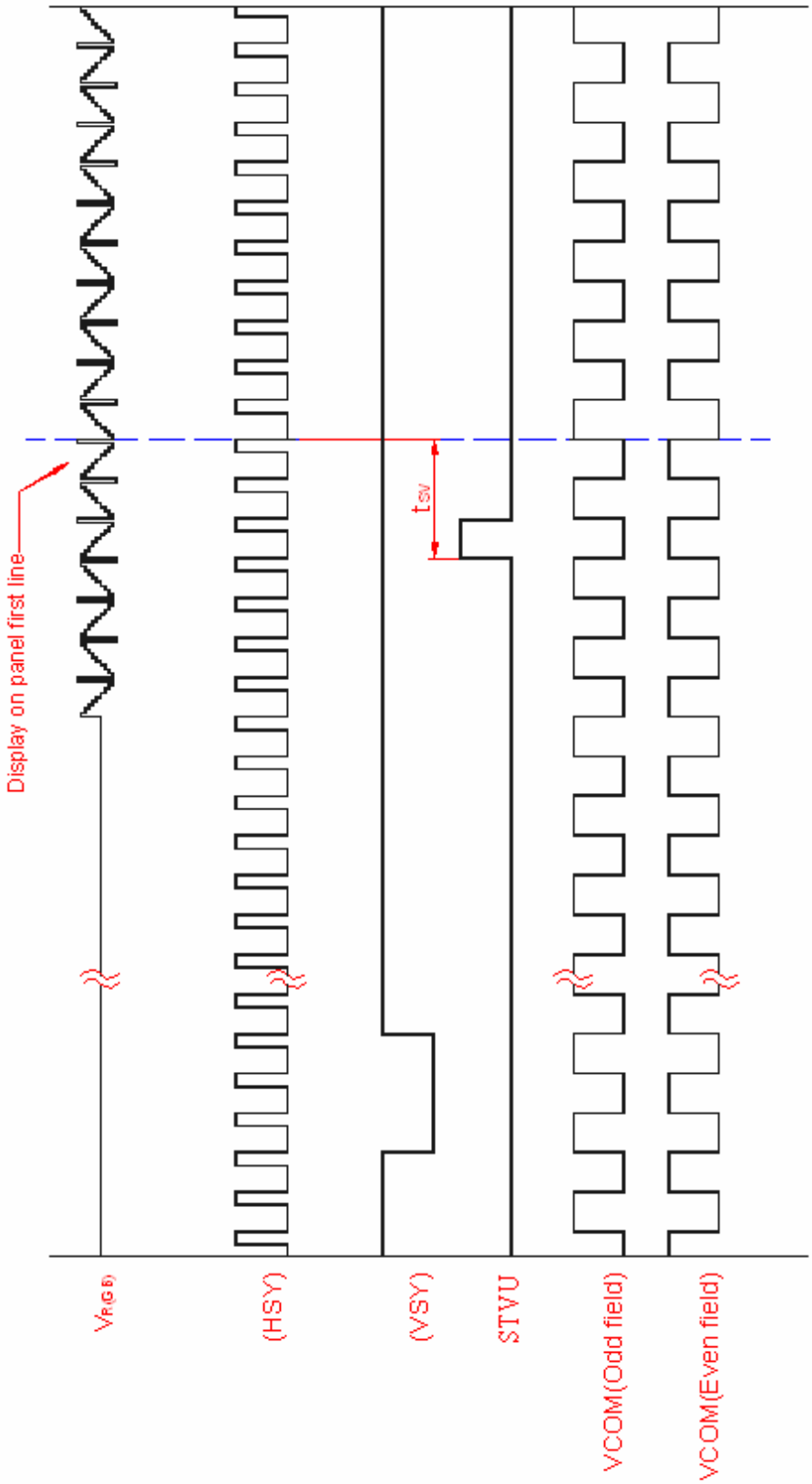


Fig.6-(a) Vertical timing (From up to down)

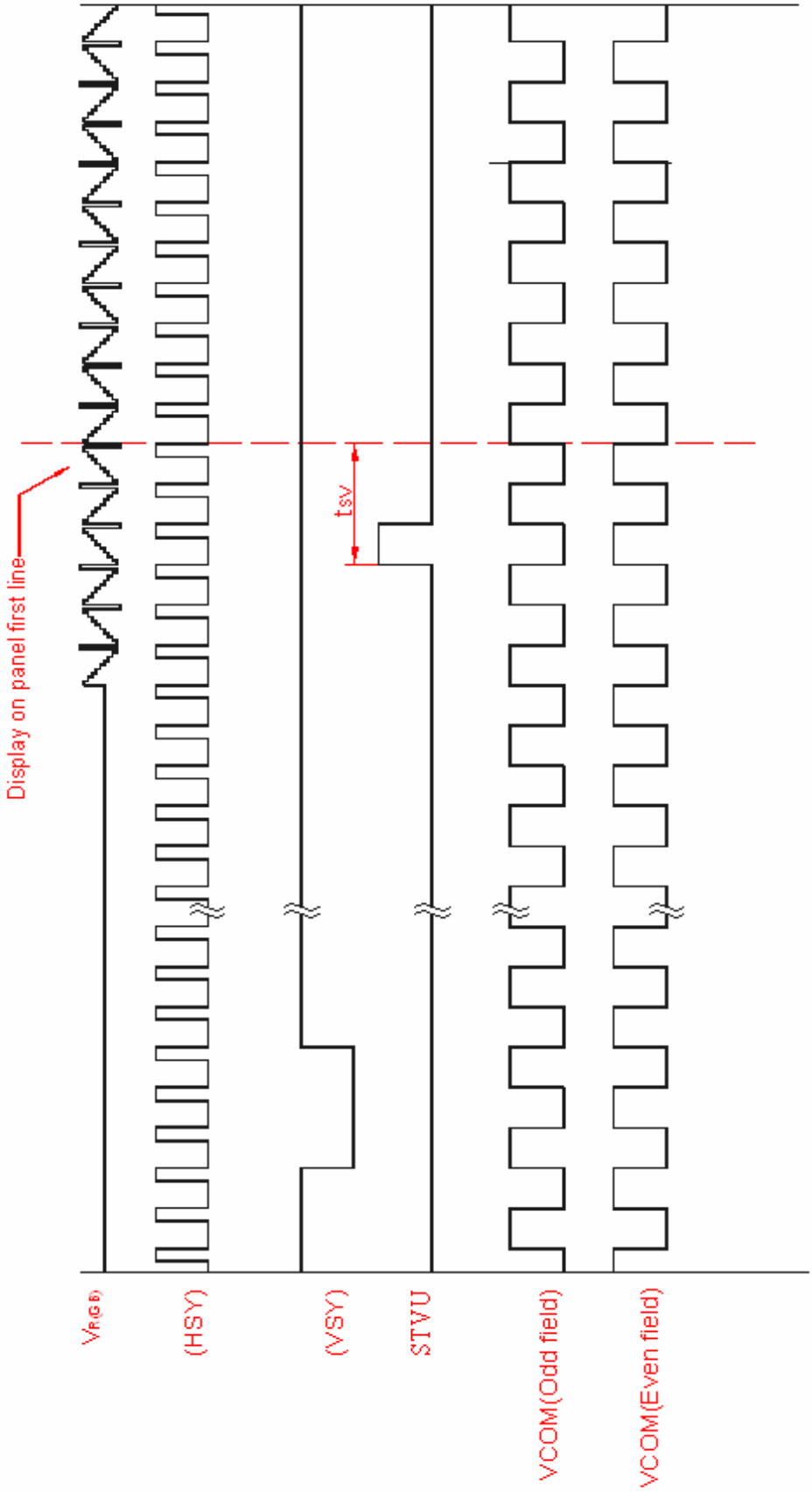


Fig.6-(b) Horizontal timing (From down to up)