Support by:
GLYN
a partner of KOE

KOE
JDI Group

TENTATIVE

Kaohsiung Opto-Electronics Inc.

FOR MESSRS : _____

DATE : Aug. 9th ,2013

TECHNICAL DATA

TX13D201VM0AAA

Contents

PROPOSED BY:

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2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY

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3. GENERAL DATA

(1)	Part Name	TX13D201VM0AAA
(2)	Module Dimensions	67.2 (W) mm × 122.2 (H) mm × 1.37 (t) mm (Excluding I/F-FPC and electronic components)
(3)	Active Area Dimensions	64.8 (W) mm × 115.2 (H) mm (5.2")
(4)	Pixel Pitch	0.060 (W) mm × 0.060 (H) mm (423ppi)
(5)	Resolution	1080 × 3 (R,G,B) (W) × 1920 (H) dots (FHD)
(6)	Color Pixel Arrangement	RGB Vertical Stripe
(7)	Display Mode	Transmissive Type, Normally Black Mode, In-Plane Switching Mode
(8)	Number of Colors	16,777,216 Colors
(9)	Viewing Direction	-
(10)	Backlight	Light Emitting Diode (LED), 12 LEDs are 2 parallel, 6 series connection Backlight current : 20mA / LED (typ)
(11)	Weight	(17)g (typ)
(12)	Power Supply Voltage	VSP = +5.5+/-0.1 V, VSN = -5.4+/-0.1 V
(13)	Interface I/O power supply Note (1)	IOVCC = 1.8+/-0.1 V The same voltage as "H" level of a customer's interface signal must be supplied to IOVCC.
(14)	LCD Driver IC	R63417 (Source and Power IC : Renesas SP Drivers Inc.)
(15)	Interface	MIPI-DSI Command mode & Video mode (4-Lane)
(16)	Methode of Inversion	Column Inversion
(17)	Surface Treatment	Hard coat (Hardness:3H)

Note (1) IOVCC is the reference voltage for adjusting the I/O signal level of R63417.
IOVCC voltage must be determined according to a customer's system.

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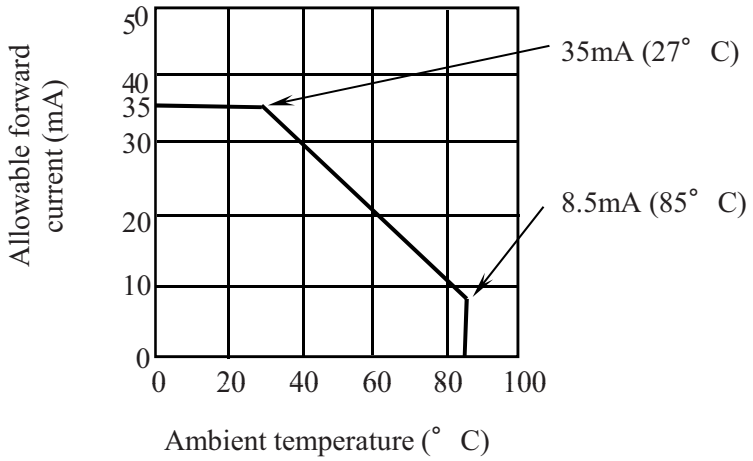
4. ABSOLUTE MAXIMUM RATINGS

4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS OF LCD Ta=25°C

Item	Symbol	Min	Max	Unit	Note
Power Supply for I/O Interface	IOVCC	-0.3	4.6	V	(1)
Power Supply Voltage for LCD	VSP	-0.3	6.5	V	(1)
Power Supply Voltage for LCD	VSN	-6.5	0.3	V	(1)
Input Voltage	Vt	-0.3	IOVCC+0.3	V	(2)
LED Reverse Voltage	V_R	-	5	V	
LED Forward Current	I_{LED}	-	Note (3)	mA	per LED

Notes (1) Keep all Voltages no lower than GND.
(2) Applies to the RESET.
(3) Ambient Temperatures vs. Allow able Forward Current.



4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

Item	Operating		Storage		Remarks
	Min	Max	Min	Max	
Ambient Temperature	-20°C	70°C	-30°C	80°C	Note (2)
Humidity	Note (1)		Note (1)		No condensation
Corrosive Gas	Not Acceptable		Not Acceptable		

Notes (1) Ta ≤ 40°C 85%RH max.
Ta > 40°C Absolute humidity must be lower than the humidity of 85%RH at 40°C.
(2) Background color slightly changes depending on ambient temperature and viewing angle.

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5. ELECTRICAL CHARACTERISTICS

LCD Module Ta=25°C

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Power Supply Voltage for I/O Interface	IOVCC	- -	1.7	1.8	1.9	V	-
Power Supply Voltage for LCD	VSP	- -	5.4	5.5	5.6	V	-
Power Supply Voltage for LCD	VSN	-	-5.5	-5.4	-5.3	V	-
Input Voltage for Logic Circuits	VIH	"H" level	0.70×IOVCC	-	IOVCC	V	(1),(2)
	VIL	"L" level	0	-	0.30×IOVCC		
Output Voltage for Logic Circuits	VOH1	"H" level	0.80×IOVCC	-	-	V	(1),(3)
	VOL1	"L" level	-	-	0.20×IOVCC		
Power Supply Current	Iiovcc	All White	-	10	15	mA	(4)
		Deep standby	-	1	15	µA	(5)
	Ivsp	All White	-	13	20	mA	(4)
		Deep standby	-	1	15	µA	(5)
	Ivsn	All White	-	11	17	mA	(4)
		Deep standby	-	1	15	µA	(5)
LED Forward Voltage	VLED	-	2.6	-	3.3	V	(6),(7)
LED Forward Current	ILED	-	-	20	'-	mA	(6),(7)
LED Reverse Current	IR	-	-	-	50	µA	(7)
Frame Frequency	fFLM	-	-	60	-	Hz	(8)

Notes (1) IOVCC = 1.7V to 1.9V
(2) Input : RESET
(3) Output : VSYNC, PWM
(4) IOVCC=1.8V, VSP=5.5V, VSN=-5.4V, fFLM=60Hz, Column inversion mode, MIPI Command mode.
(5) IOVCC=1.8V, VSP=5.5V, VSN=-5.4V, Deep standby mode.
(6) Each value is the characteristics of one LED.
(7) The operating current of LED should be determined within the maximum rating of the temperature environmental condition.
(8) The value is a frame frequency when the data of Item (9.7.2) is set to the register. When changing setting data, please contact us.

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6. OPTICAL CHARACTERISTICS

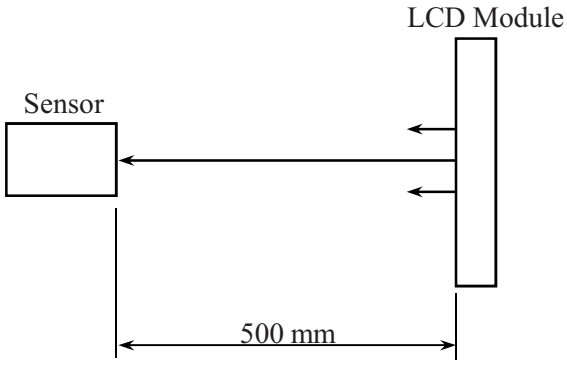
LCD (BACKLIGHT ON)

Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Brightness		B	φ=0°, θ=0°	400	500	-	cd/m^2	(1),(2)
Brightness Uniformity		-	φ=0°, θ=0°	80	-	-	%	(2),(3),(5)
Viewing Angle		φ1+φ2	θ=0°, CR≥10	-	170	-	deg	(4),(6),(7)
			θ=90°, CR≥10	-	170	-		
Contrast Ratio		CR	φ=0°, θ=0°	700	1000	-	-	(6)
Response Time		tr+tf	φ=0°, θ=0°	-	18	40	ms	(8)
Color Tone (Primary Color)	Red	x	φ=0°, θ=0°	0.615	0.640	0.665	-	(9)
		y		0.305	0.330	0.355		
	Green	x		0.275	0.290	0.315		
		y		0.565	0.590	0.615		
	Blue	x		0.125	0.150	0.175		
		y		0.035	0.060	0.085		
	White	x		0.276	0.3013	0.326	-	
		y		0.293	0.3182	0.343		
NTSC Ratio		-	φ=0°, θ=0°	65	70	-	%	-
Color Gamut (CIE 1931)		sRGB	φ=0°, θ=0°	90	100	-	%	-
Cross Talk		C/T	φ=0°, θ=0°	-	3	5	%	(10)
Flecker		F/K	φ=0°, θ=0°	-	-	20	%	(10)

Measurement Conditions

Measurement environment : Dark room
Ambient temperature : Ta=25°C
Sequence : Refer to Item 9.7.2
Power supply voltage : IOVCC=1.8V, VSP=5.5V, VSN=-5.4V
Backlight current : I_{BL}=20mA (I_{LED}=20mA)

Notes (1) Definition of Brightness "B"



Sensor : KONICA MINOLTA CS-1000 or equivalent
Measurement point : Center of LCD's active area

(2) Display image for measurement : All White

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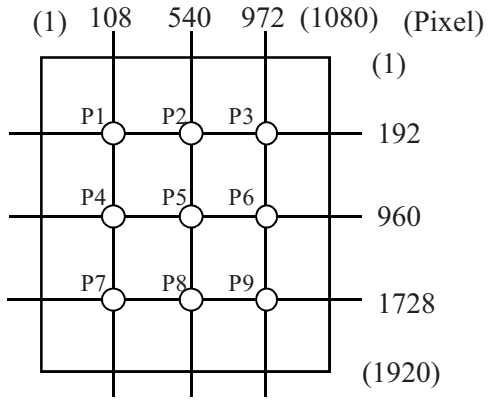
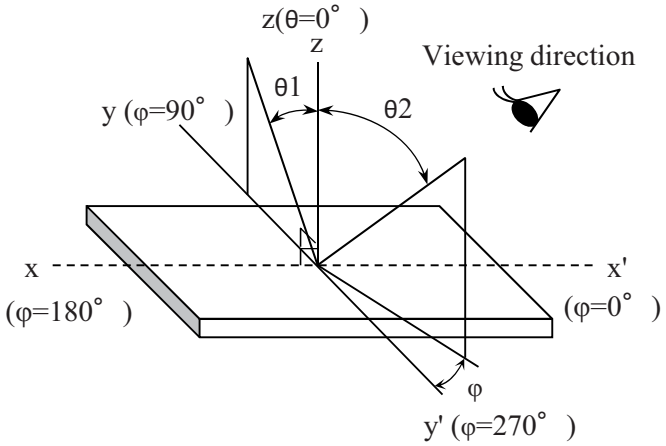
Notes (3) Measurement point



(4) Definition of θ and φ



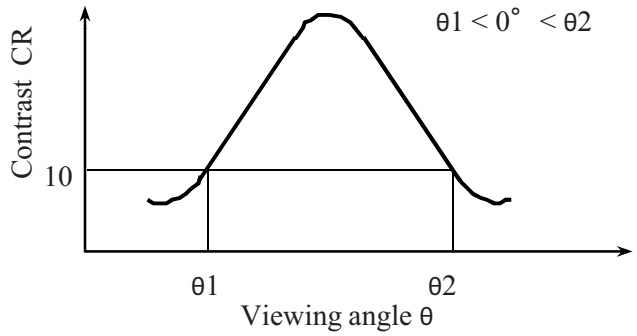
(5) Definition of brightness uniformity

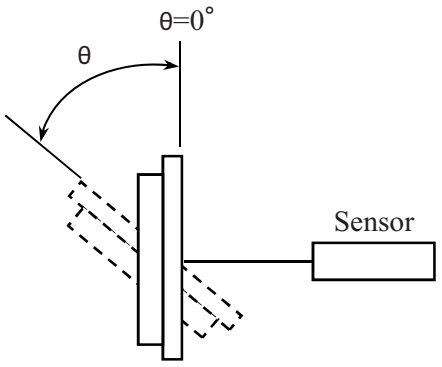
$$\text{Brightness uniformity} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100\ (\%)$$

(6) Definition of Contrast "CR"

$$CR = \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$

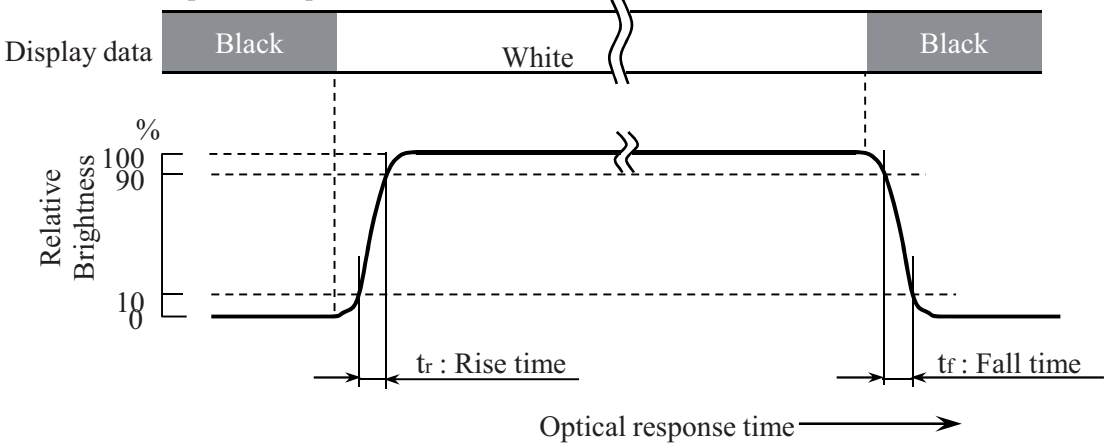
(7) Definition of Viewing Angle θ1and θ2





Sensor : TOPCON's BM-5A or equivalent

(8) Definition of Optical Response Time



(9) It is not the guaranteed value for lot acceptance. If the tolerance between +/-0.025 and +/-0.03 is found, both parties will have a discussion to solve it.

(10) If a nonconformance is found, both parties will have a discussion to solve it.

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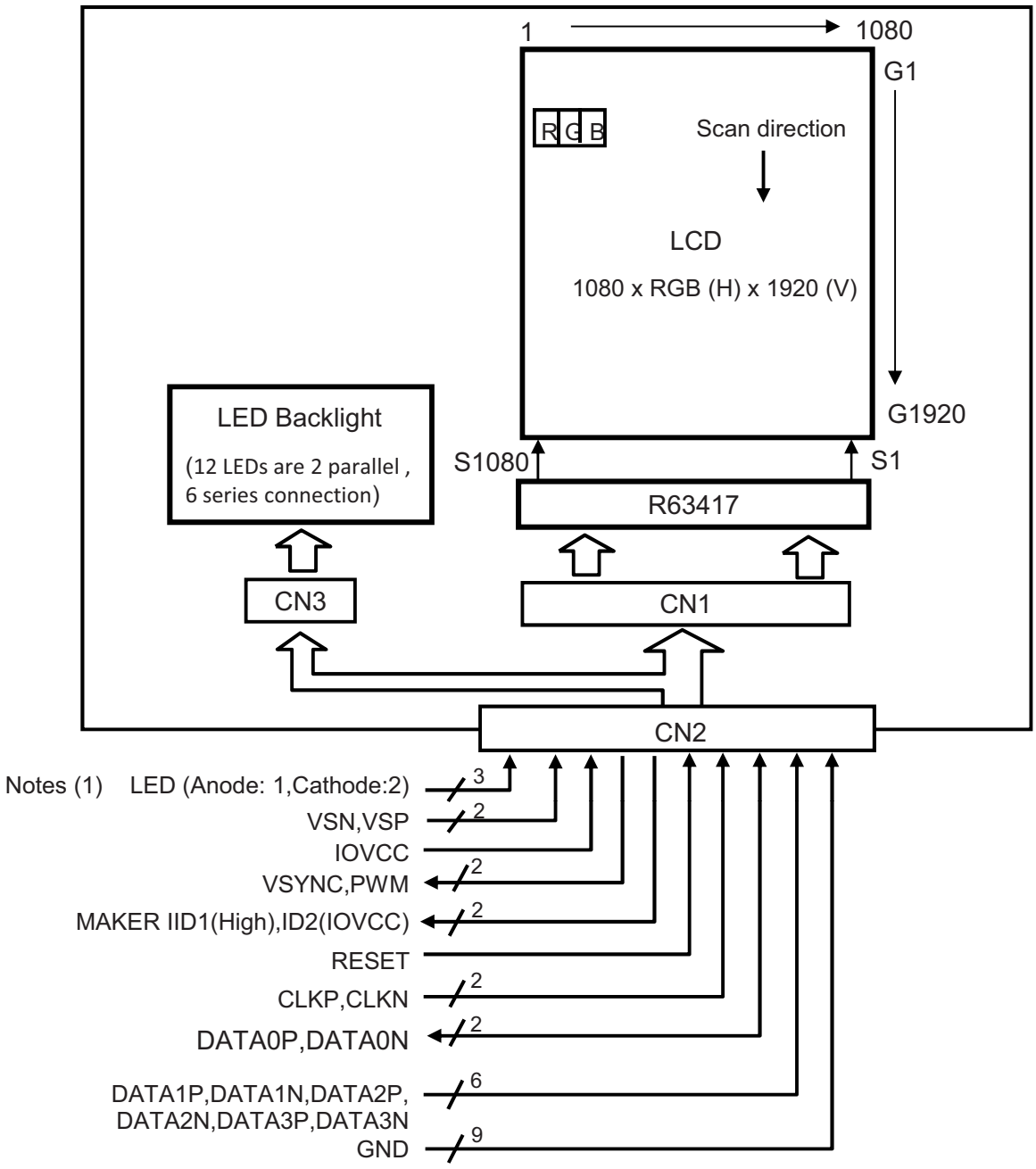
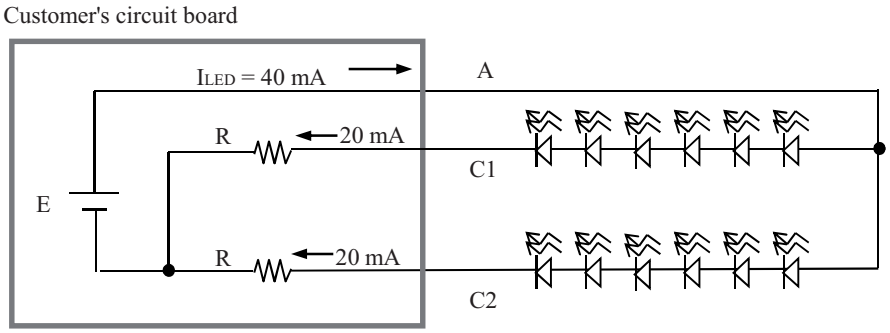
7. BLOCK DIAGRAM



Notes (1) Please connect the resistor (R=200 ohm) for current control between LED (cathode) and GND in the customer's system.

(2)



R : Resistance for limiting current (R > 100 ohm)

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8. INTERFACE

8.1 INTERNAL PIN CONNECTION

Pin No.	Signal	I/O	Function	Driver's Signal name
1	GND	-	Ground	-
2	LED_C1	-	GND for LED	-
3	LED_C2	-	GND for LED	-
4	ID1(IOVCC)	O	Maker ID(IOVCC:IOVCC level)	IOVCC
5	IOVCC	-	Power Supply for I/O Interface and Logic circuit (1.8V)	IOVCC
6	PWM	O	PWM output pin of Active Back Light control processing	LEDPWM
7	VSYNC	O	VSYNC Output pin	VSOUT
8	RESET	I	Reset Input pin	RESX
9	GND	-	Ground	-
10	DATA1P	I	MIPI DSI data-1 signal line(+)	DATA1P
11	DATA1N	I	MIPI DSI data-1 signal line(-)	DATA1N
12	GND	-	Ground	-
13	DATA0P	I/O	MIPI DSI data-0 signal line(+)	DATA0P
14	DATA0N	I/O	MIPI DSI data-0 signal line(-)	DATA0N
15	ID2(GND)	-	Ground	-
16	GND	-	Ground	-
17	DATA3N	I	MIPI DSI data-3 signal line(-)	DATA3N
18	DATA3P	I	MIPI DSI data-3 signal line(+)	DATA3P
19	GND	-	Ground	-
20	CLKN	I	MIPI DSI Clock signal line(-)	CLKN
21	CLKP	I	MIPI DSI Clock signal line(+)	CLKP
22	GND	-	Ground	-
23	DATA2N	I	MIPI DSI data-2 signal line(-)	DATA2N
24	DATA2P	I	MIPI DSI data-2 signal line(+)	DATA2P
25	GND	-	Ground	-
26	VSN	I	Power supply to analog circuit	VSN
27	VSP	I	Power supply to analog circuit	VSP
28	GND	-	Ground	-
29	LED_AN	-	Power Supply for LED	-
30	GND	-	Ground	-

LCM Connector : BM10B(0.8)-30DP-0.4V(51)…Header (HIROSE) ,
Suitable Connector : BM10NB(0.8)-30DS0.4V(51)…Receptacle (Hirose)

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8.2 Timing CHARACTERISTICS

(1)MIPI DSI Characteristics

Item		Symbol	Unit	Condition	Min	Typ	Max	Note
HS-RX	Differential input high threshold	VIDTH	mV	IOVCC=1.65~3.30V	-	-	70	3)
	Differential input low threshold	VIDTL	mV	IOVCC=1.65~3.30V	-70	-	-	3)
	Single-ended input low voltage	VILHS	mV	IOVCC=1.65~3.30V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVCC=1.65~3.30V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVCC=1.65~3.30V	70	-	330	1)
	Differential input impedance	ZID	Ω	IOVCC=1.65~3.30V	-	100	-	2)
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVCC=1.65~3.30V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVCC=1.65~3.30V	880	-	1350	
	I/O leakage current	ILEAK	uA	Vin=-50mV - 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	IOVCC=1.65~3.30V	-50	-	50	
	Thevenin output high level	VOH	V	IOVCC=1.65~3.30V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVDD=1.80V	110	-	-	2)
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVCC=1.65~3.30V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVCC=1.65~3.30V	450	-	-	

Notes (1) VCMRX(DC) = (VP + VDN) / 2

(2) Excluding COG resistance (contact resistance and ITO wiring resistance).The values are tentative.

(3) Minimum 110mV/-110mV HS differential swing is required for display data transfer.

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MIPI DSI HS-RX Clock and Data-Clock Specifications

Item	Symbol	Unit	Condition	Min	Typ	Max	Note
DISCLK Frequency	fDSICLK	MHz	IOVCC=1.65~3.30V	100	-	500	4)
DSICLK Cycle time	tCLKP	ns	IOVCC=1.65~3.30V	1		10	
DSI Data Transfer Rate	tDSIR	Mbps	IOVCC=1.65~3.30V	200		1000	4)
Data to Clock Setup Time	tSETUP	UI	IOVCC=1.65~3.30V	0.15	-	-	
		ns	IOVCC=1.65~3.30V	0.15	-	-	5)
Clock to Data Hold Time	tHOLD	UI	IOVCC=1.65~3.30V	0.15	-	-	
		ns	IOVCC=1.65~3.30V	0.15	-	-	5)

Notes (4) When fDSICLK < 125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.

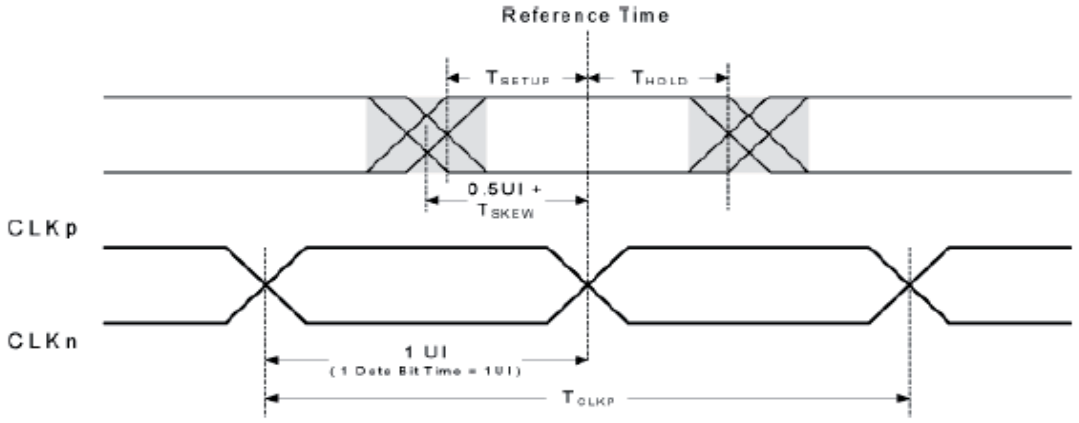
(5) Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.

MIPI DSI LP-RX/TX Clock and Data-Clock Specifications

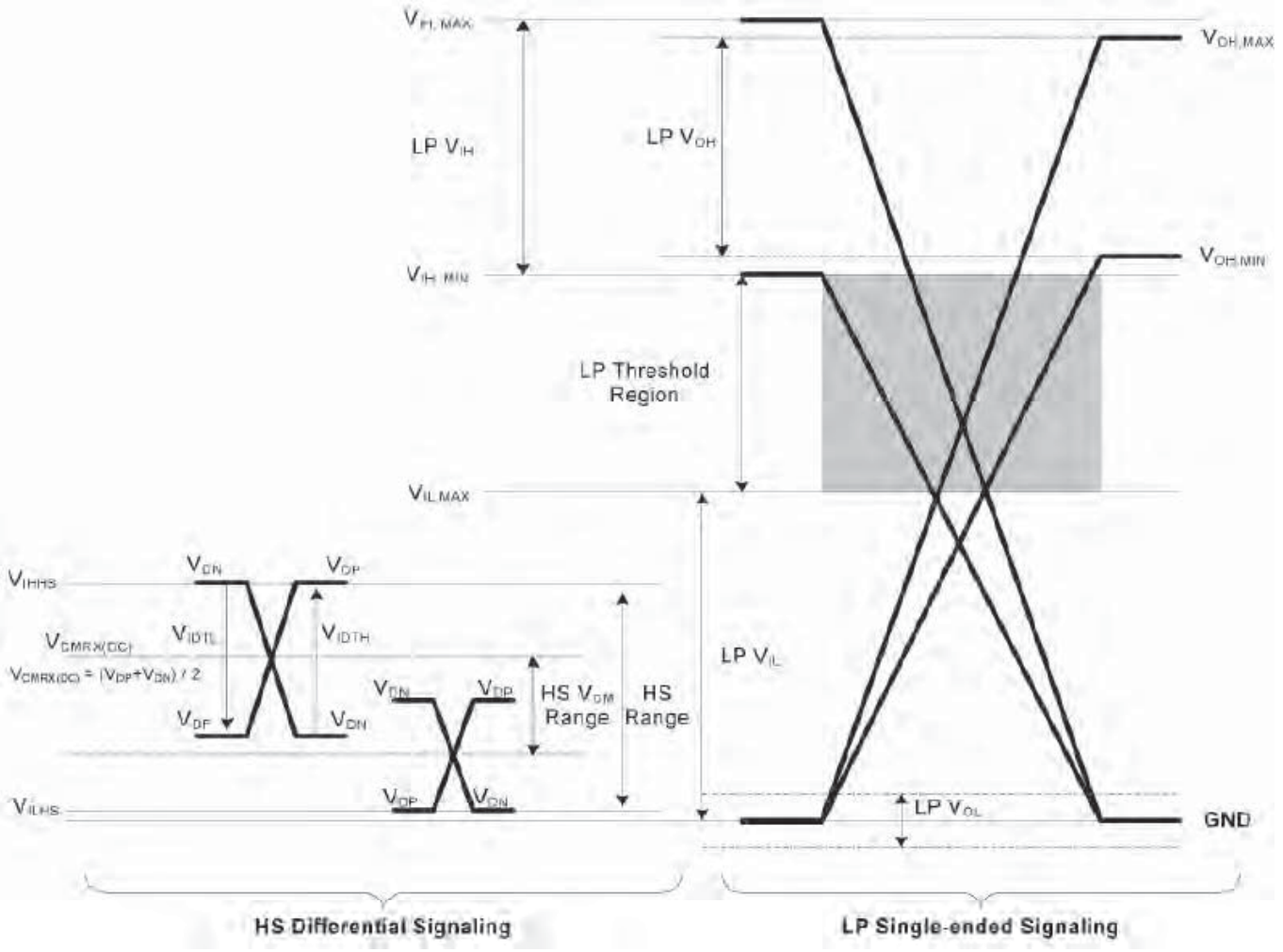
Item	Symbol	Unit	Condition	Min	Typ	Max	Note
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	ns	IOVCC=1.65~3.30V	40ns +4*UI	-	85ns +6*UI	
$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	$T_{HS-PREPARE} + T_{HS-ZERO}$	ns	IOVCC=1.65~3.30V	145ns +10*UI	-	-	
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	ns	IOVCC=1.65~3.30V	max (n*8UI, 60ns + n*4*UI)	-	-	1), 2)
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	ns	IOVCC=1.65~3.30V	100	-	-	
Time to drive LP-00 after Tumaround Request	T_{TA-GO}		IOVCC=1.65~3.30V	$4*T_{LPTX}$			
Time-out before new TX side starts driving	$T_{TA-SURE}$		IOVCC=1.65~3.30V	$1*T_{LPTX}$	-	$2*T_{LPTX}$	
Time to drive LP-00 by new TX	T_{TA-GET}		IOVCC=1.65~3.30V	$5*T_{LPTX}$			
Length of any Low-Power state period	T_{LPX}	ns	IOVCC=1.65~3.30V	50	-	-	
Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	Ratio T_{LPX}		IOVCC=1.65~3.30V	2/3	-	3/2	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	UI	IOVCC=1.65~3.30V	60ns +52UI	-	-	3)
$T_{CLK-PREPARE}$ + Time for lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	ns	IOVCC=1.65~3.30V	300	-	-	

Item	Symbol	Unit	Condition	Min	Typ	Max	Note
Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	UI	IOVCC=1.65~3.30V	8	-	-	
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns	IOVCC=1.65~3.30V	38	-	95	
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns	IOVCC=1.65~3.30V	60	-	-	
Time from start of THS-TRAIL period to start of LP-11 state	T_{EOT}		IOVCC=1.65~3.30V	-	-	105ns + n*12*UI	2)
Length of Low-Power TX period in case of using DSI clock	T_{LPTX1}	UI	IOVCC=1.65~3.30V	-	48	-	4)
Length of Low-Power TX period in case of using internal OSC clock	T_{LPTX2}	ns	IOVCC=1.65~3.30V	-	1/(fosc/2)	-	

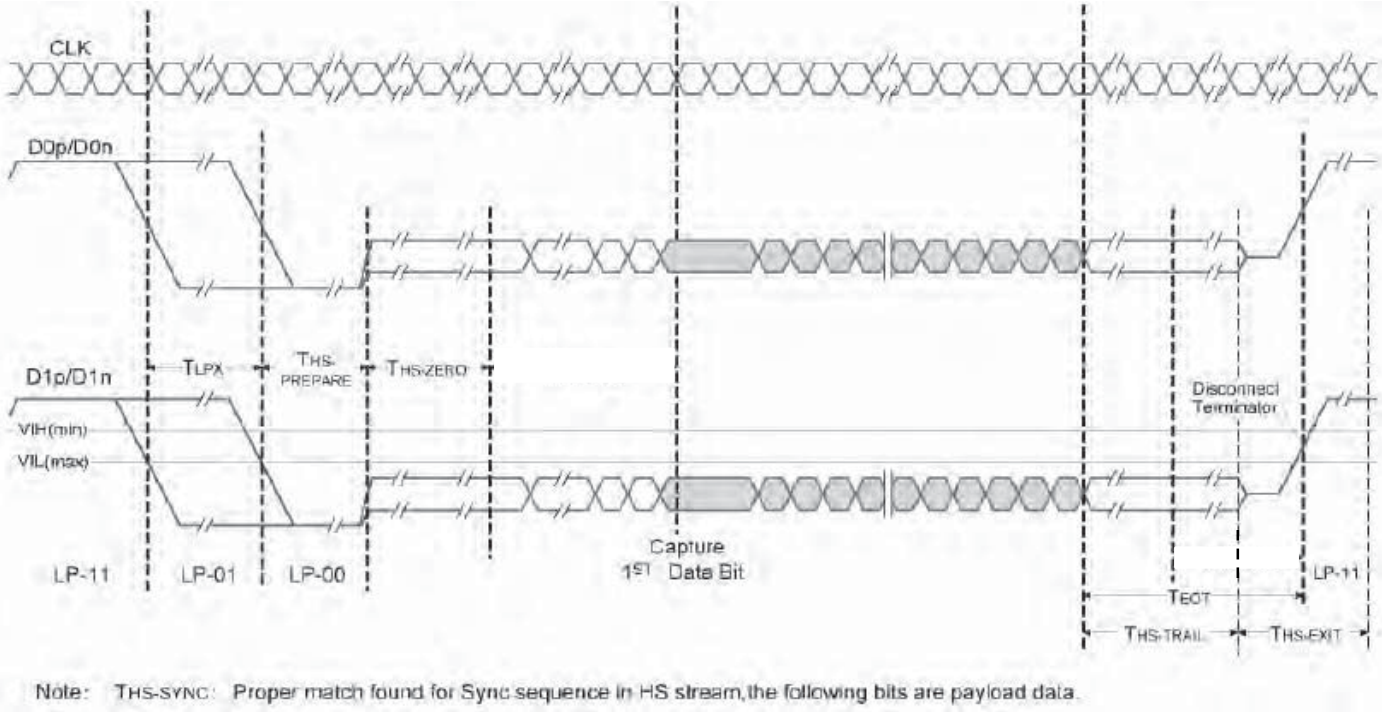
Notes (1) If a > b then max(a,b) = a, otherwise max(a,b) = b
(2) Where n = 1 for Forward-direction HS mode.
(3) The R63417 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and the R63417 can work without the remained process if tCLK-POST is more than256 UI.
(4) The R63417 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disabled.



Data to Clock Timing Definitions

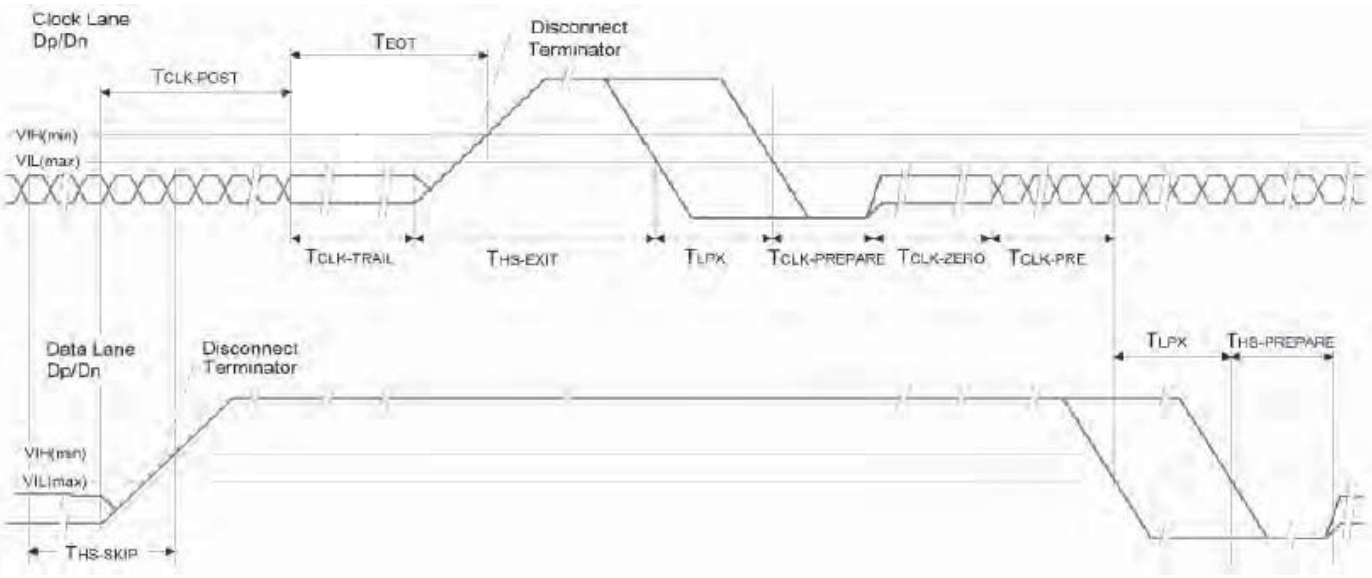


DSI LP Mode

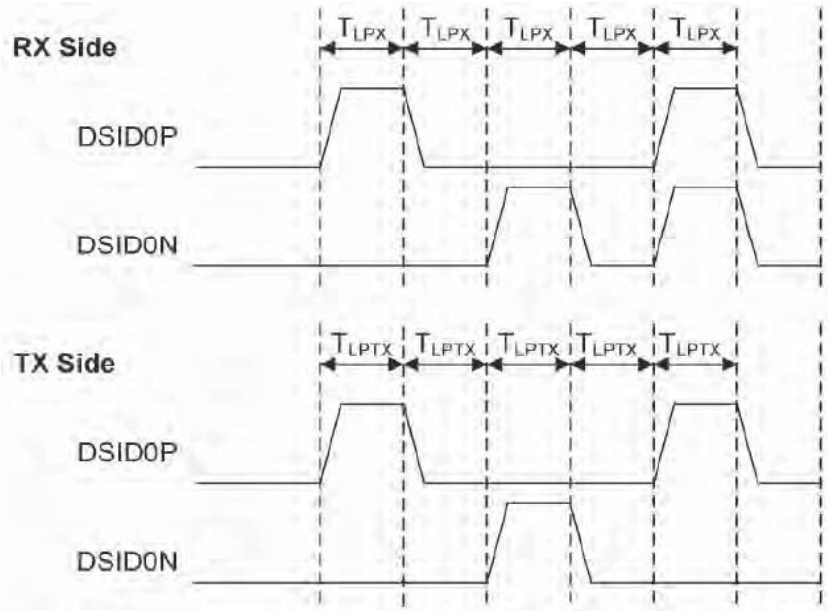


Note: THS-SYNC: Proper match found for Sync sequence in HS stream, the following bits are payload data.

HS Data Transmission in Bursts



Switching the clock lane between clock Transmission and LP mode



DSI LP Mode

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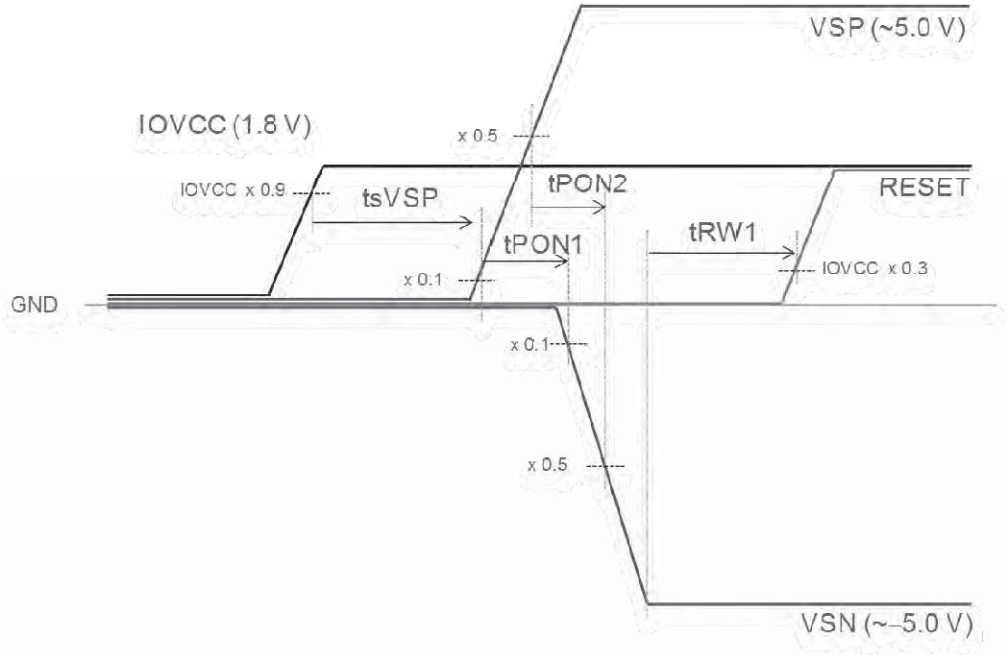
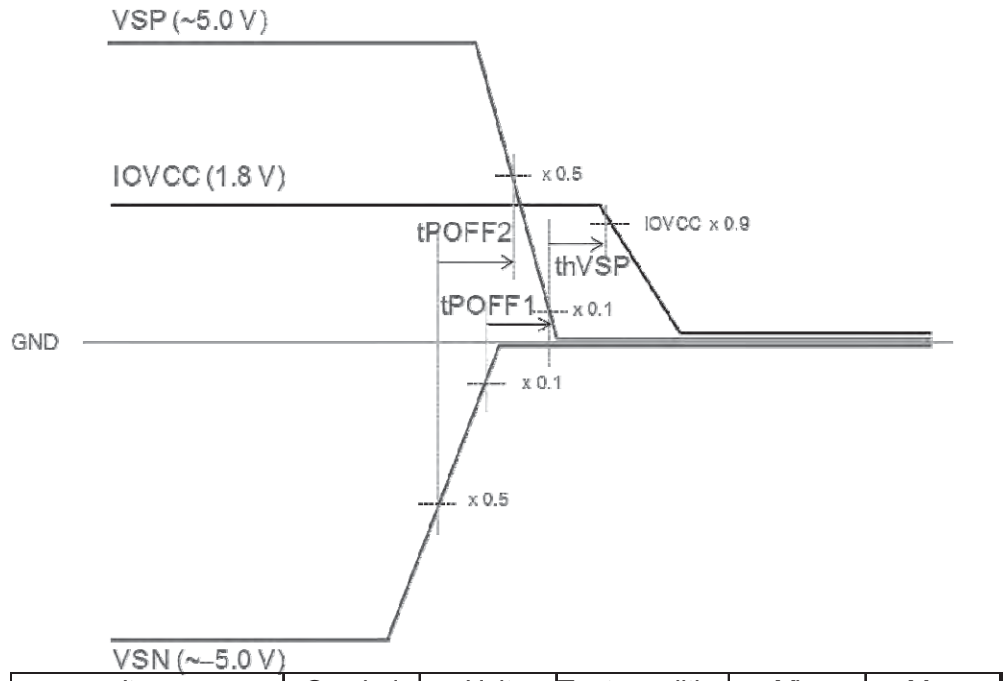
8.3 POWER SEQUENCE

8.3.1 POWER ON SEQUENCE



Item	Symbol	Unit	Test condition	Min.	Max.
VSP ON timing	tsVSP	ms	Power On	1	–
VSN ON timing1	tPON1	ms	Power On	0	–
VSN ON timing2	tPON2	ms	Power On	0	–
Reset Low level width	tRW1	ms	Power On	1	–
Reset time	tRT	ms	–	3	–

8.3.2 POWER OFF SEQUENCE

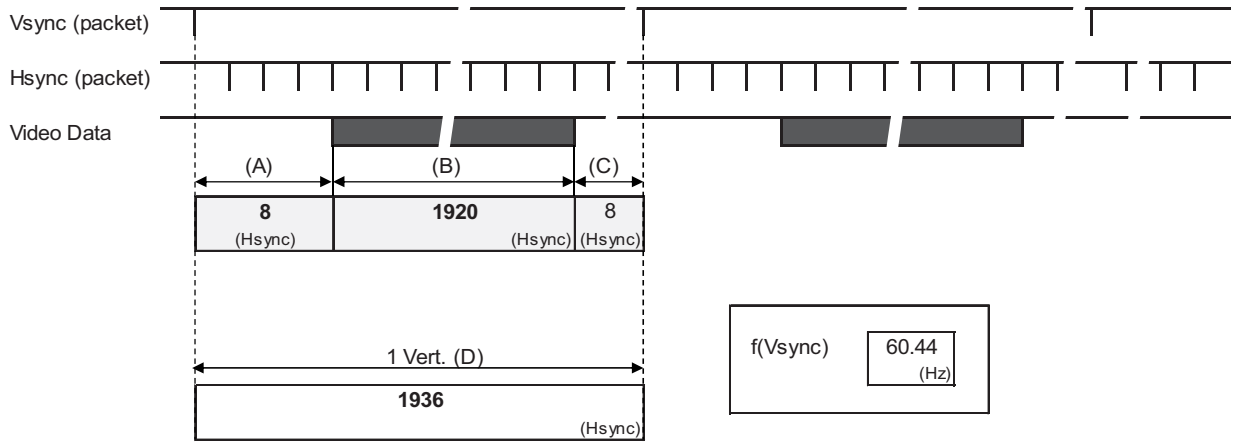


Item	Symbol	Unit	Test condition	Min.	Max.
VSP OFF timing	thVSP	ms	Power Off	0	–
VSN OFF timing1	tPOFF1	ms	Power Off	0	–
VSN OFF timing2	tPOFF2	ms	Power Off	0	–

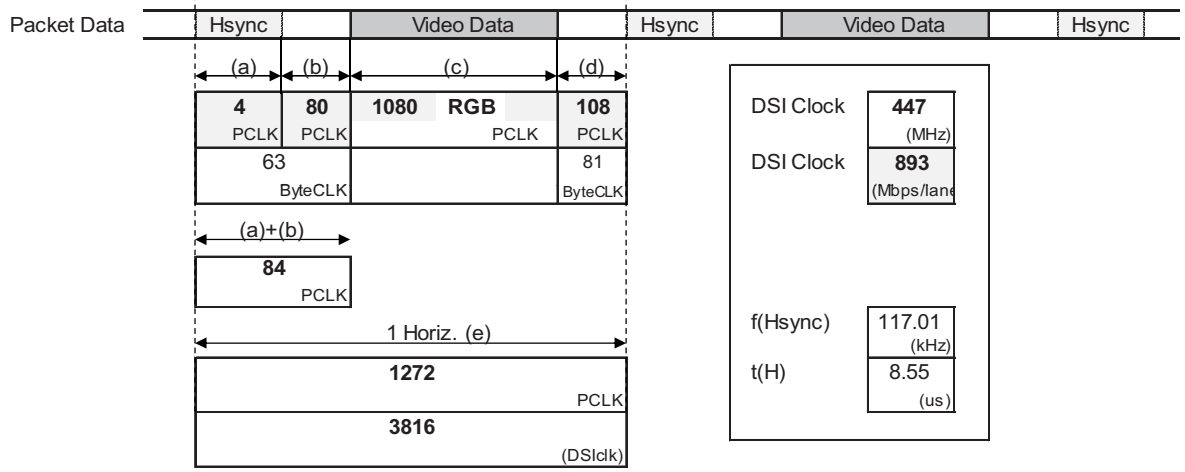
8.4 Video Mode Interface Timing (DPI style)

4 lane

Vertical Timing



Horizontal Timing



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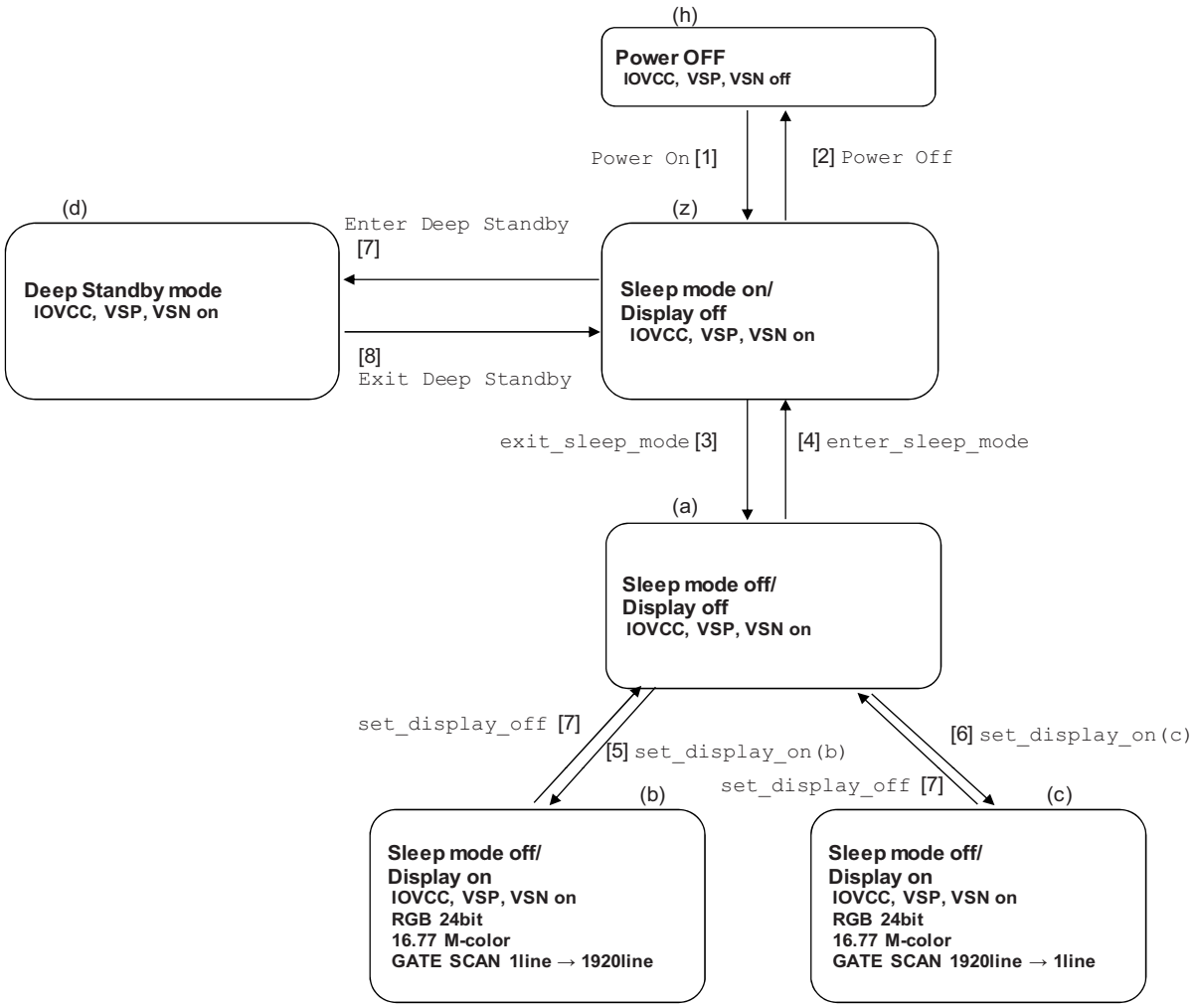
8.5 REGISTER SETTING

8.5.1 STATE TRANSITION DIAGRAM OF OPERATION MODE



8.5.2 SEQUENCE

[1] Power On Note 1) State (h) → (z)

Order	Instruction	Data		previous	Remarks
1		RESX = "L"			
2	Power On	IOVCC On			
6		wait	1ms(min.)		
7		VSP On			
8		VSN On			
		wait	1ms(min.)		
	Power On Reset	RESX = "H"			
		wait	3ms(min.)		Loading NVM

[2] Power off State (z) → (h)

Order	Instruction	Data	previous	Remarks
1	Power Off	VSN Off		
		VSP Off		
		IOVCC Off		

[3] exit_sleep_mode State (z) → (a)

Order	Instruction	Data		previous	Remarks
1	set_column_address	DI	0x39		
2		WC	0x05		
3		WC	0x00		
4		ECC			
5		CMD	0x2A		
6		P1	0x00		
7		P2	0x00		
8		P3	0x04		
9		P4	0x37		
10		CRC			
11		CRC			
12	set_page_address	DI	0x39		
13		WC	0x05		
14		WC	0x00		
15		ECC			
16		CMD	0x2B		
17		P1	0x00		
18		P2	0x00		
19		P3	0x07		
20		P4	0x7F		
21		CRC			
22		CRC			
23	exit_sleep_mode	DI	0x05		
24		CMD	0x11		
25		dummy	0x00		
26		ECC			
27		wait	6frame (min.)		

[3] Note for 11h command (exit_sleep_mode).
(1) Do NOT input any command during ON sequence.

[4] enter_sleep_mode State (a) → (z)

Order	Instruction	Data	previous	Remarks
1	enter_sleep_mode	DI	0x05	
2		CMD	0x10	
3		dummy	0x00	
4		ECC		
5		wait	3frame(min.)	

[3] Note for 11h command (exit_sleep_mode).
(1) Do NOT input any command during ON sequence.

[5] set_display_on — State (a) → (b)

Order	Instruction		Data	previous	Remarks
1	set_address_mode	DI	0x15		
2		CMD	0x36		
3		P1	0x00		B7=1,B6=1,B4=1,B4=0,B0=0
4		ECC			
5		wait	1 frame(min)		
6	set_pixel_format	DI	0x15		
7		CMD	0x3A		
8		P1	0x77		D[6:4]=0x07,D[2:0]=0x07
9		ECC			
10	set_display_on	DI	0x05		
11		CMD	0x29		
12		dummy	0x00		
13		ECC			
14		wait	-		

[6] set_display_on — State (a) → (c)

Order	Instruction		Data	previous	Remarks
1	set_address_mode	DI	0x15		
2		CMD	0x36		
3		P1	0xD0	0x01	B7=1,B6=1,B4=1,B0=0
4		ECC			
5		wait	1 frame(min)		
6	set_pixel_format	DI	0x15		
7		CMD	0x3A		
8		P1	0x77		D[6:4]=0x07,D[2:0]=0x07
9		ECC			
10	set_display_on	DI	0x05		
11		CMD	0x29		
12		dummy	0x00		
13		ECC			
14		wait	-		

[7] set_display_off — State (b) → (a)

Order	Instruction		Data	previous	Remarks
1	set_display_off	DI	0x05		
2		CMD	0x28		
3		dummy	0x00		
4		ECC			
5		wait	1frame(min.)		

[8] Enter Deep Standby — State (z) → (d)

Order	Instruction		Data	previous	Remarks
1	Manufacturer Command Access Protect	DI	0x23		
2		CMD	0xB0		
3		P1	0x04		MCAP=3'h4
4		ECC			
5	Low Power Mode Control	DI	0x23		
6		CMD	0xB1		
7		P1	0x01		DSTB=1
8		ECC			
9		wait	1ms(min.)		

[8] Note for Enter Deep Standby.

Do NOT release deep standby within 1 ms after entering deep standby.
If releasing within 1 ms, VDD may restart from middle voltage, it may cause unstable state of LCD driver.

[9] Exit Deep Standby		State (d) → (z)			
Order	Instruction		Data	previous	Remarks
1	RESET	RESX = "L"			
2		wait	10us(min)		
3		RESX = "H"			
4		wait	3ms(min.)		

Note) (a), (b), (d), (h), (i) and (z) in this sheet mean LCD module state which are explained in "State Transition Diagram".
Note) After sending command "0_x29 (set_display_on)", image which are sent as a data is started to be displayed from next frame.
Note) After sending command "0_x28 (set_display_off)", image will be stopped from next frame.

[10] Command mode to Video mode change sequence during Display			
Normal Display MODE (Command mode)			
1	Data Type	0x23	MCAP
2	Command	0xB0	
3	P1	0x04	
4	Data Type	0x29	Interface setting Video mode (Video Trough mode)
5	Command	0xB3	
6	P1	0x1C	
7	P2	0x00	
8	P3	0x00	
9	P4	0x00	
10	P5	0x00	
11	P6	0x00	
12	Data Type	0x23	MCAP
13	Command	0xB0	
14	P1	0x03	
Video mode signal Start			
Normal Display MODE (Video mode)			

[11] Video mode to Command mode change sequence during Display			
Normal Display MODE (Video mode)			
1	Data Type	0x23	MCAP
2	Command	0xB0	
3	P1	0x04	
4	Data Type	0x29	Interface setting Command mode
5	Command	0xB3	
6	P1	0x0C	
7	P2	0x00	
8	P3	0x00	
9	P4	0x00	
10	P5	0x00	
11	P6	0x00	
12	Data Type	0x23	MCAP
13	Command	0xB0	
14	P1	0x03	
Normal Display MODE (Video mode) more than 2 frame period			
Video mode signal Stop			
Normal Display MODE (Command mode)			

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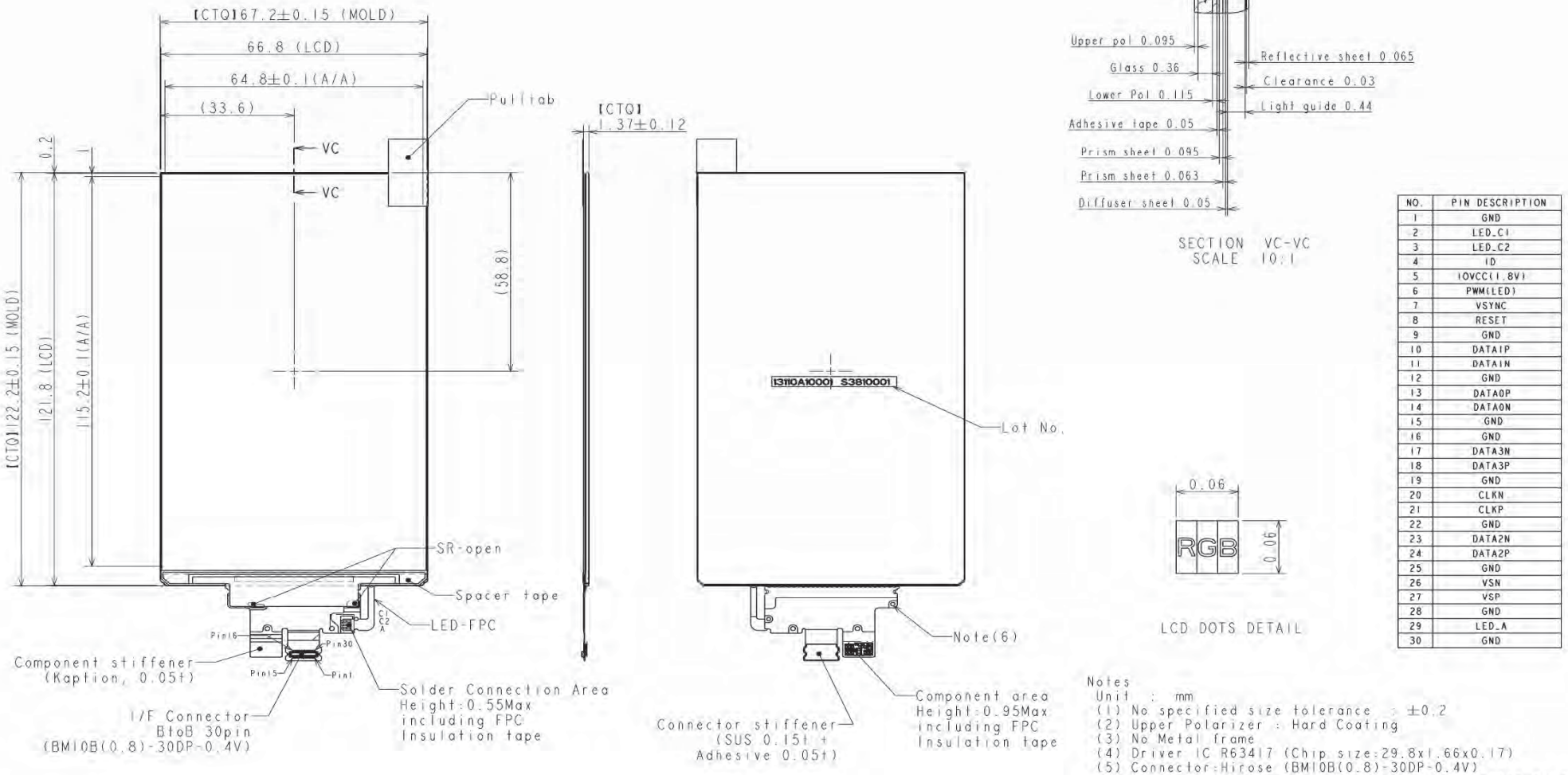
9. OUTLINE DIMENSIONAL



NO.	PIN DESCRIPTION
1	GND
2	LED_C1
3	LED_C2
4	ID
5	IOVCC(1.8V)
6	PWM(LED)
7	VSYNC
8	RESET
9	GND
10	DATA1P
11	DATA1N
12	GND
13	DATA0P
14	DATA0N
15	GND
16	GND
17	DATA3N
18	DATA3P
19	GND
20	CLKN
21	CLKP
22	GND
23	DATA2N
24	DATA2P
25	GND
26	VSN
27	VSP
28	GND
29	LED_A
30	GND

Notes
Unit : mm
(1) No specified size tolerance : ±0.2
(2) Upper Polarizer : Hard Coating
(3) No Metal frame
(4) Driver IC R63417 (Chip size:29.8x1.66x0.17)
(5) Connector:Hirose (BM10B(0.8)-30DP-0.4V)
(6) Please avoid providing any conductive matter at areas where noted "Note(6)". There are exposed electric conductors due to electrolytic plating.