MODEL NO.: N144NGE
SUFFIX: E41

Customer: Toshiba

APPROVED BY	SIGNATURE

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
楊竣傑	王茂春	吳振嘉
2012-06-19	2012-06-18	2012-06-15
13:52:22 CST	17:32:05 CST	15:06:31 CST

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
3.0	Mar.30, 2012	All	Spec Ver.3.0 was first issued.
3.1	APR.16.2012	17	T3:Power ON/OFF Sequence
		18	T3:Delay from VDD to AUX channel
3.2	May. 16.2012	25~26	7.2 CARTON/ 7.3 PALLET
		28~30	APPENDIX. EDID DATA STRUCTURE
		32	Rear view
3.3	June.13. 2012	24	7.1 MODULE LABEL
		25	7.2 CARTON
		26	7.3 PALLET

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N144NGE-E41 is a 14.4" (14.4" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 30 pins eDP interface. This module supports 1792 x 768 resolution and can display 16,777,216 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	14.4" diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1792 x R.G.B. x 768	pixel	-
Pixel Pitch	0.1875 (V) x 0.1875 (H)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16777216 (8 bit)	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Glare	-	-
Luminance, White	300	cd/m^2	
Power Consumption	Total 4.5W (Max.) @ cell 1.4 W (Max.), BL 3.1 W (Max.)	-	(1)

Note (1) The specified power consumption (with converter efficiency) is under the conditions at V_{DD} = 3.3 V, fv = 60 Hz, I_{LED} = 21mA, V_{LED} = Typ., Duty=100% and Ta = 25 ± 2 °C, whereas black pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	352.5	353	353.5	mm	(1)
	Vertical (V)	180.3	180.8	181.3	mm	
	Thickness (T)	-	-	3.3	mm	
Bezel Area	Horizontal	352.5	353	353.5	mm	
	Vertical	161.8	162.3	162.8	mm	
Active Area	Horizontal	-	336	-	mm	
	Vertical	-	144	-	mm	
Weight		-	270	285	g	

Note (1) Please refer to Appendix Outline Drawing for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE
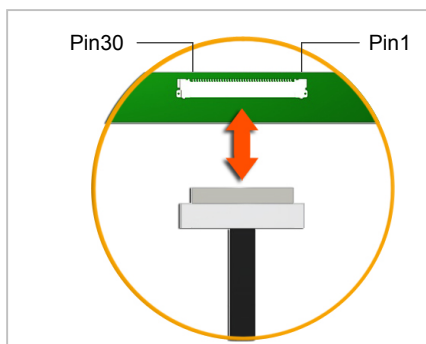
Please refer to Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-030E-12 or equivalent

User's connector Part No: IPEX-20453-030T-01 or equivalent

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1)   (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Relative Humidity (%RH)
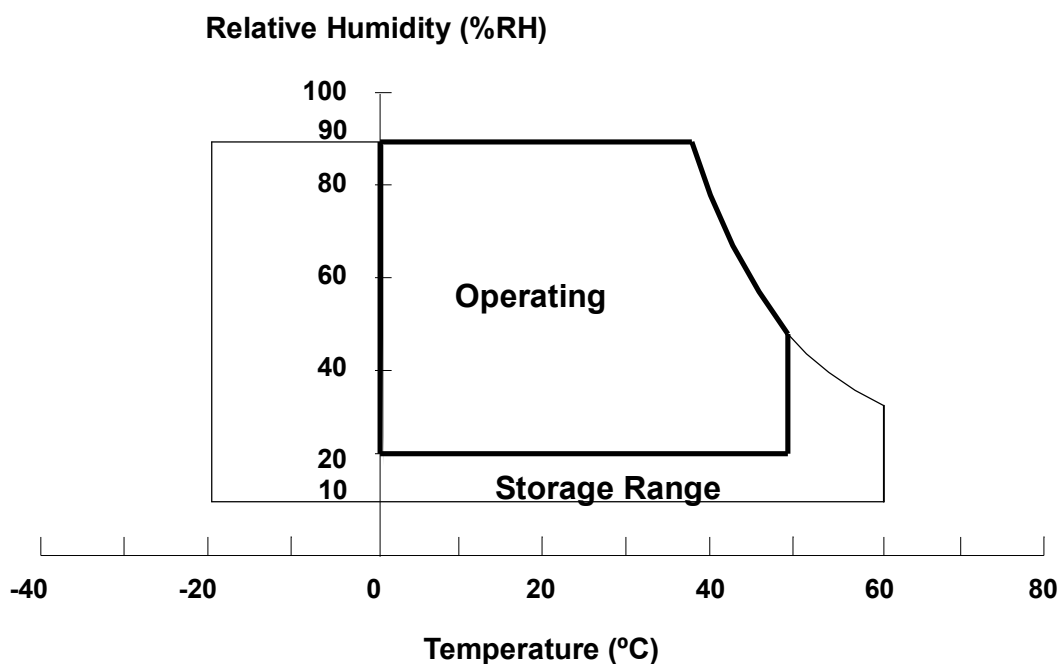
Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.

3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{DD}	-0.3	4	V	(1)
Logic Input Voltage	V_{IN}	-0.3	4	V	
Converter Input Voltage	V_{LED}	-0.3	(22)	V	(1)
Converter Control Signal Voltage	BL_PWM_DIM	-0.3	(6)	V	(1)
Converter Control Signal Voltage	BL_ENABLE	-0.3	(6)	V	(1)

Note (1) Stress beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM

```
INPUT CONNECTOR

EDID EEPROM          GAMMA GENERATOR

TIMING ONTROLLER     DATA DRIVER IC
eDP Input

STEP-UP DC/DC        SCAN DRIVER IC
& STEP-DOWN DC/DC
GENERATOR            TFT LCD
                     PANEL
                     1792 X 768

LED CONVERTER        LED LIGHT BAR ASS'Y
```

→ Control & Data   → signal & Power   → Power   → Control
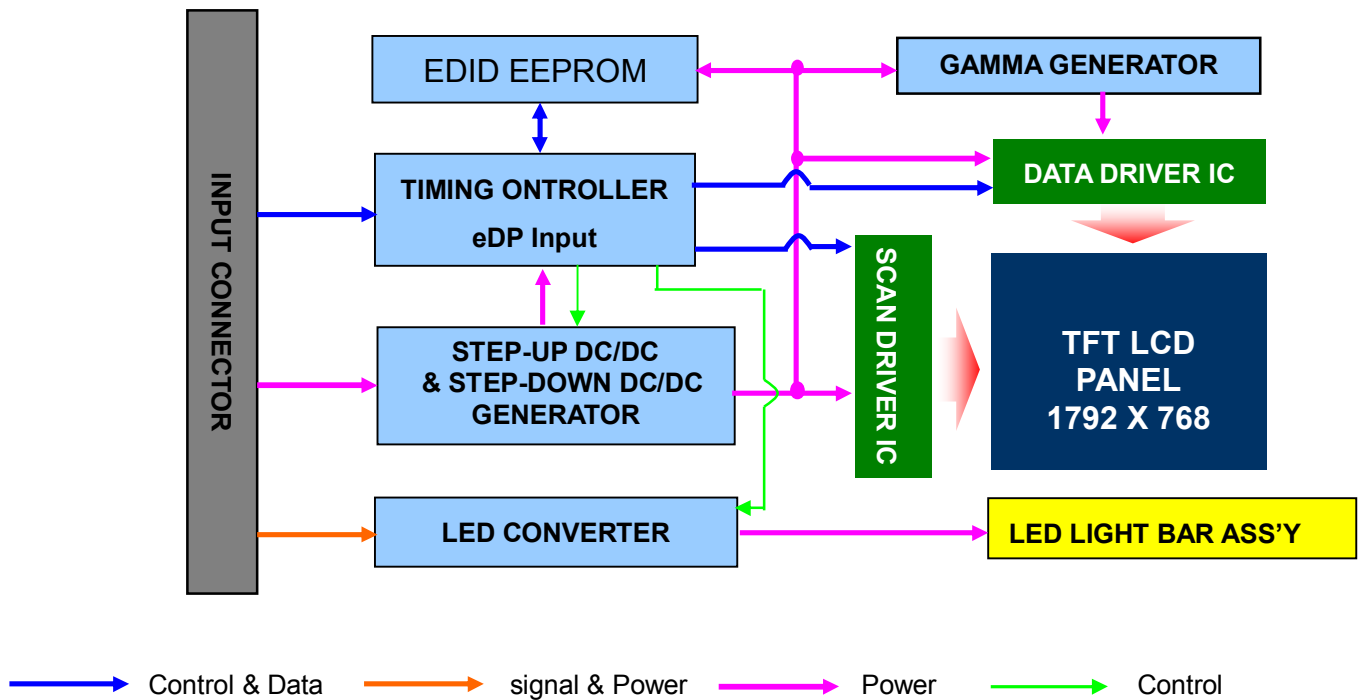
4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection	
2	H_GND	High Speed Ground	
3	Lane1_N	Complement Signal Link Lane 1	
4	Lane1_P	True Signal Link Lane 1	
5	H_GND	High Speed Ground	
6	Lane0_N	Complement Signal Link Lane 0	
7	Lane0_P	True Signal Link Lane 0	
8	H_GND	High Speed Ground	
9	AUX_CH_P	True Signal Auxiliary Channel	
10	AUX_CH_N	Complement Signal Auxiliary Channel	
11	H_GND	High Speed Ground	
12	LCD_V_{DD}	LCD logic and driver power	
13	LCD_V_{DD}	LCD logic and driver power	
14	NC - RESERVED	Reserved for LCD manufacturer's use	
15	LCD_GND	LCD logic and driver ground	
16	LCD_GND	LCD logic and driver ground	
17	HPD	HPD signal pin	
18	BL_GND	Backlight ground	
19	BL_GND	Backlight ground	
20	BL_GND	Backlight ground	
21	BL_GND	Backlight ground	
22	BL_ENABLE	Backlight On/Off	
23	BL_PWM_DIM	System PWM signal input for dimming	
24	NC - RESERVED	Reserved for LCD manufacturer's use	
25	NC - RESERVED	Reserved for LCD manufacturer's use	
26	BL_V_{LED}	Backlight power	
27	BL_V_{LED}	Backlight power	
28	BL_V_{LED}	Backlight power	
29	BL_V_{LED}	Backlight power	
30	NC	NO Connection	

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRICAL SPECIFICATIONS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Logic/LCD Drive Voltage	V_{DD}	3.0	3.3	3.6	V	
I_{DD} Current	I_{DD}	--	394	424	mA	(1)
I_{DD} Power	P_{DD}	--	1.3	1.4	Watt	(1)
Inrush Current	I_{RUSH}	--	--	1.5	A	(2)
Allowable Logic/LCD Drive Ripple Voltage	V_{DD} Ripple	--	--	100	mV$_{p-p}$	

Note (1) The ambient temperature is Ta = 25 ± 2 ℃.

Note (2) I_{RUSH}: the maximum current when V_{DD} is rising

Measurement Conditions: Shown as the following figure. Test pattern: black.
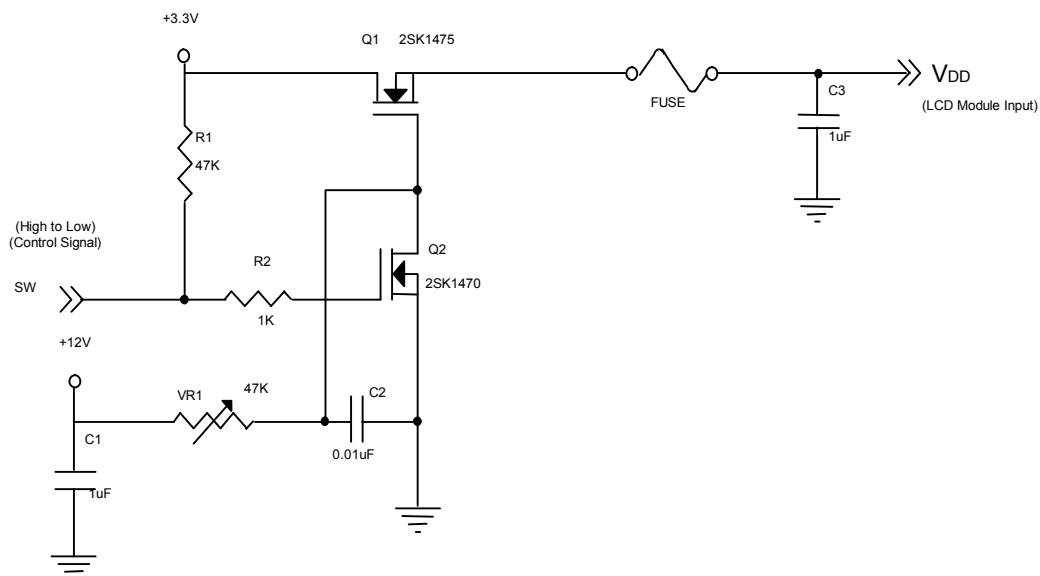
V_{DD} rising time is 470us

4.3.2 LED CONVERTER SPECIFICATIONS
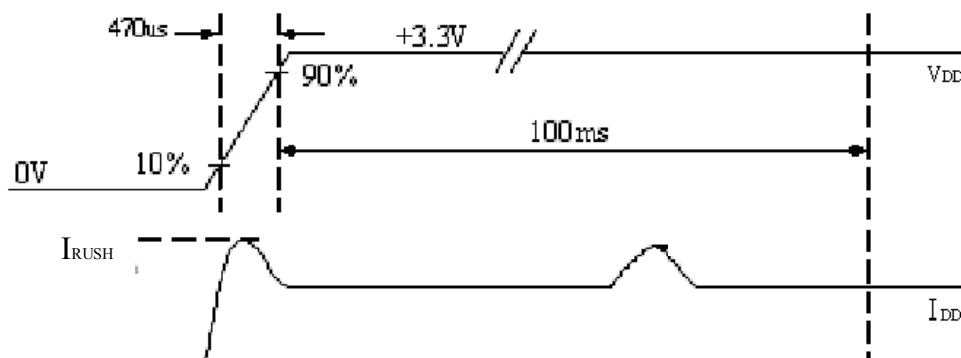
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input Power Supply Voltage		V_{LED}	(6.0)	(12.0)	(19.5)	V	
Converter Inrush Current		$I_{LED RUSH}$	-	-	(2)	A	(1)
EN Control Level	Backlight On		(2.3)	-	(3.6)	V	
	Backlight Off		0	-	(0.8)	V	
PWM Control Level	PWM High Level		(2.3)	-	(3.6)	V	
	PWM Low Level		0	-	(0.15)	V	
PWM Control Duty Ratio			10	-	100	%	
			5	-	100	%	(2)
PWM Control Permissive Ripple Voltage		V_{PWM_p-p}	-	-	100	mV	
PWM Control Frequency		f_{PWM}	200	-	10K	Hz	(3)
LED Power Current	V_{LED} =Typ.	I_{LED}	154	255	517	mA	(4)

Note (1) $I_{LED RUSH}$: the maximum current when V_{LED} is rising,

Measurement Conditions: Shown as the following figure. V_{LED} = Typ, Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty=100%.

V$_{LED}$ rising time is 0.5ms
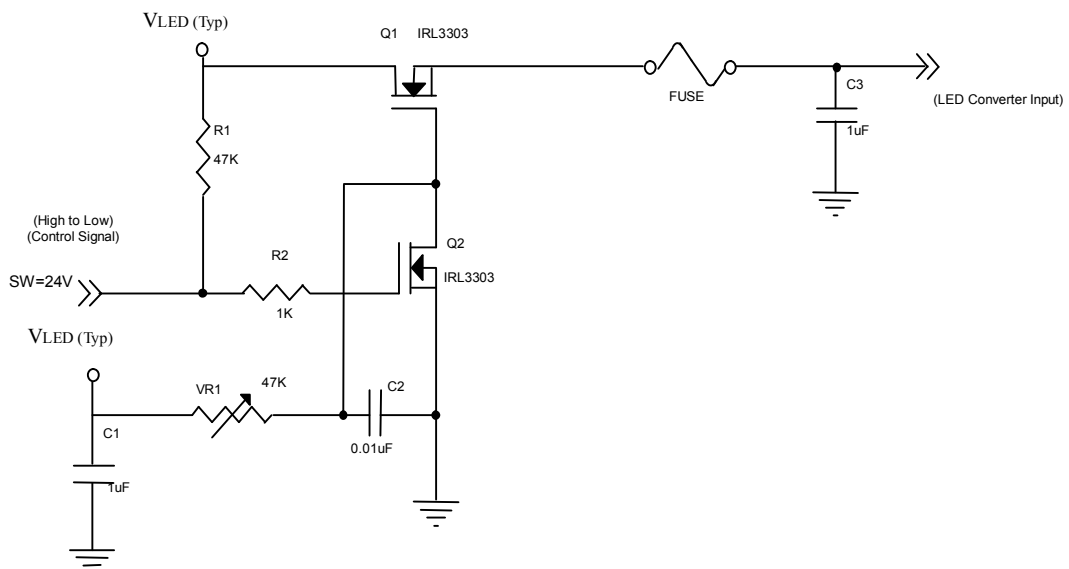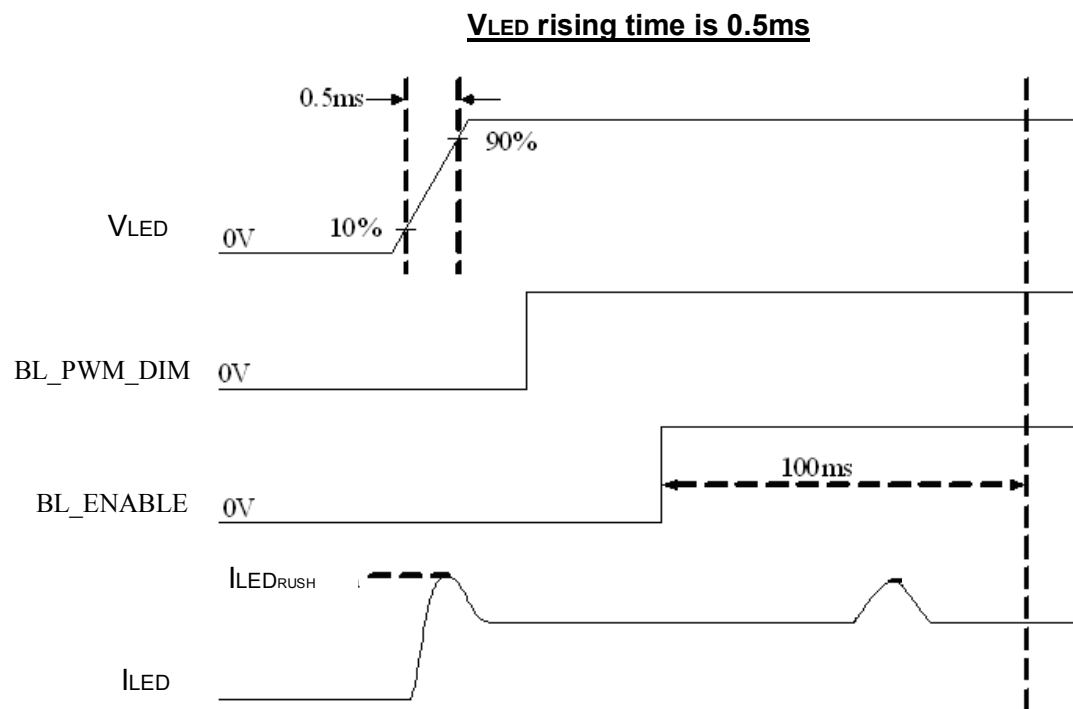
Note (2) If the BL_PWM_DIM control duty ratio is less than 5%, there is some possibility that acoustic noise or backlight flash can be found. And it is also difficult to control the brightness linearity.

Note (3) If BL_PWM_DIM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

BL_PWM_DIM control frequency f$_{PWM}$ should be in the range

$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

$$N : \text{Integer} \ (N \geq 3)$$

$$f : \text{Frame rate}$$

Note (4) The specified LED power supply current is under the conditions at "V$_{LED}$ = Typ.", Ta = 25 ± 2 ºC, Duty=100%.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ℃

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	--	20.3	21	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	--	126	--	mA	
Power Consumption	P_L	--	2.56	2.65	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high current meter as shown below :

$V_{L,} I_L$

LED

Light Bar

Light Bar Feedback

Channels
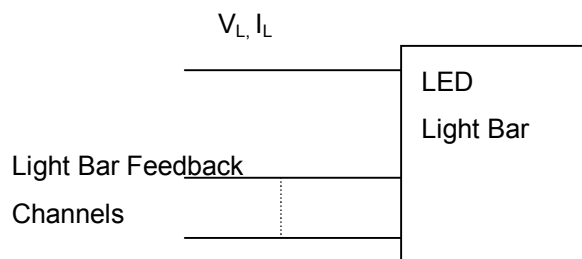
Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter

with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The Life Time of LED is defined as the time when it continues to operate under the conditions at Ta

= 25 ±2 ^{o}C and I_L = 21 mA(Per EA) until the brightness becomes $\leq$ 50% of its original value.

4.4 eDP INPUT SIGNAL TIMING SPECIFICATIONS

4.4.1 eDP DC SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
MainLink Input Signal Peak-to-peak Voltage	$|VDIFF_{P-P}|_{(MainLink)}$	120	-	-	mV	High bit rate
		40	-	-	mV	Reduced bit rate
AUX Differential Input Voltage	$|V_{ID}|_{(AUX)}$	160	-	680	mV	
Differential Signal Common Mode Voltage	VCM	0	-	2	V	
AUX AC Coupling Capacitor	C_{AUX}	75	-	200	nF	
Lane Intra-pair Skew	$V_{RX-SKEW-INTRA\_PAIR}$	-	-	100	ps	High bit rate
		-	-	300		Reduced bit rate

Note (1) Display port interface related AC coupled signals are following VESA Display Port Standard V1.2
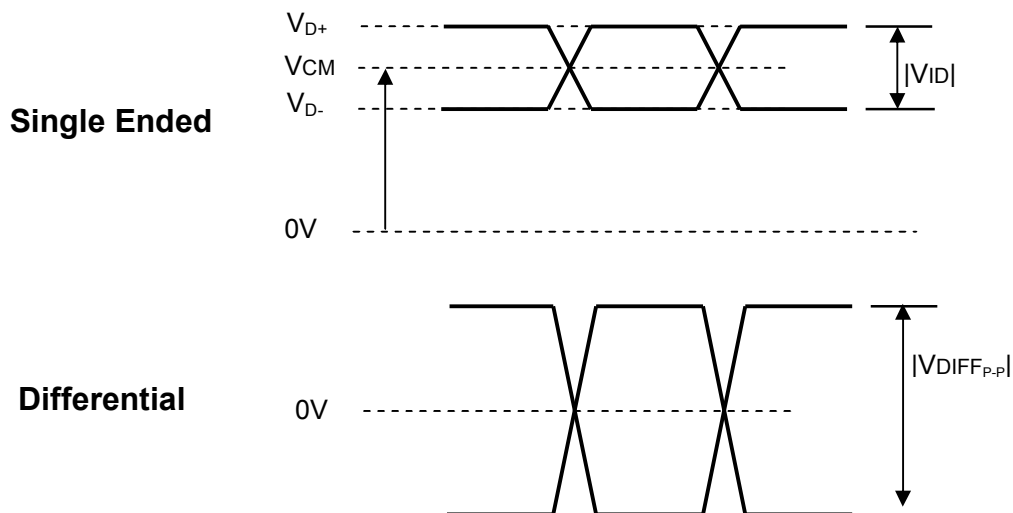
4.4.2 eDP INTERFACE:

Compliant to DP spec v1.1a & eDP spec v1.1

Lane 0   **Lane 1**
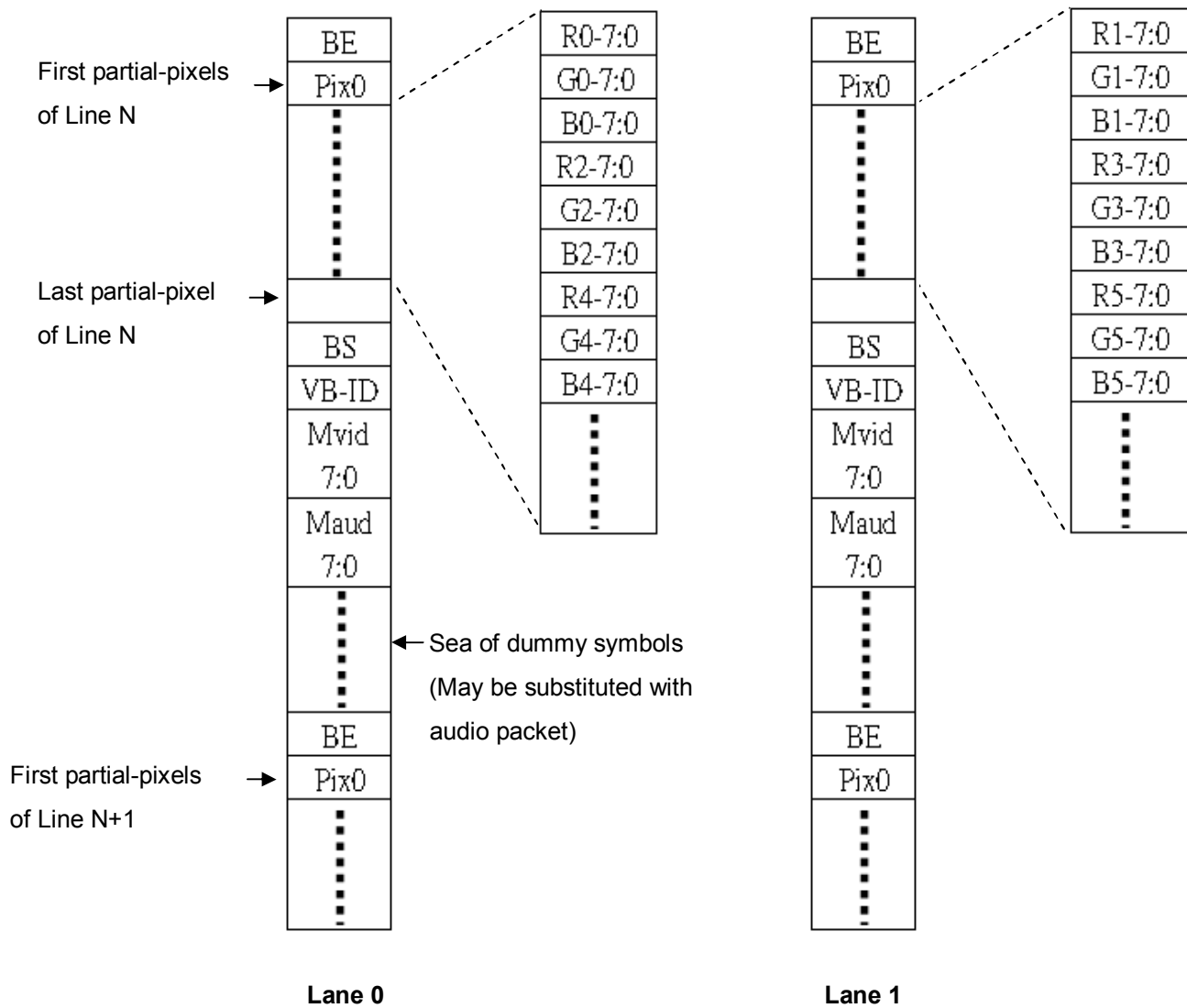
4.4.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input is the brighter the color will be. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

| Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	88	100	110	MHz	-
DE	Vertical Total Time	TV	778	--	872	Lines	-
	Vertical Active Display Period	TVD	--	768	--	Lines	-
	Horizontal Total Time	TH	1890	2078	2100	Clocks	-
	Horizontal Active Display Period	THD	--	1792	--	Clocks	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.
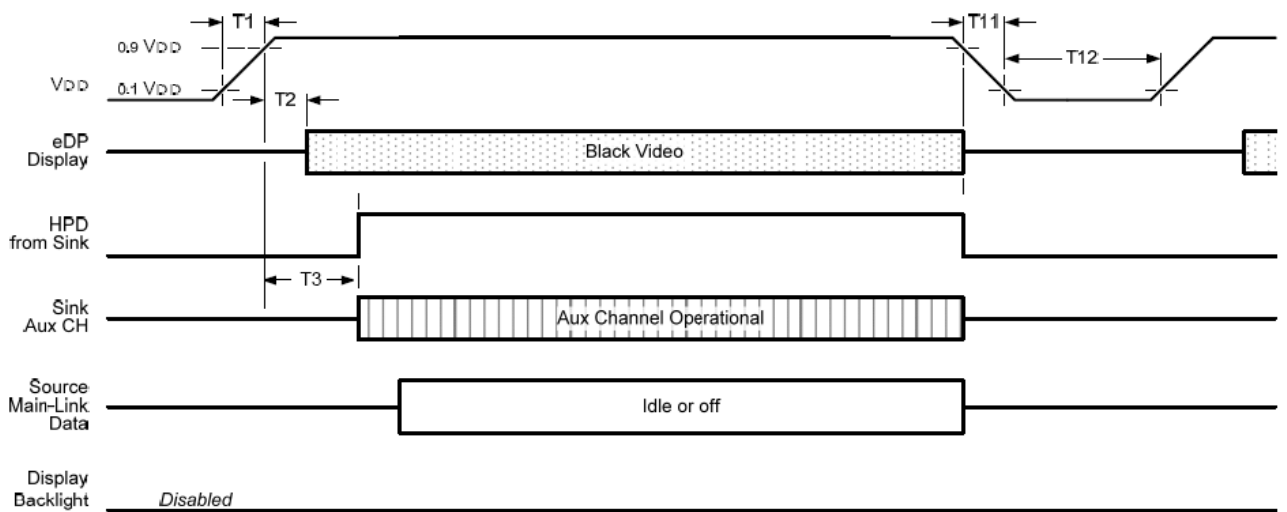
INPUT SIGNAL TIMING DIAGRAM
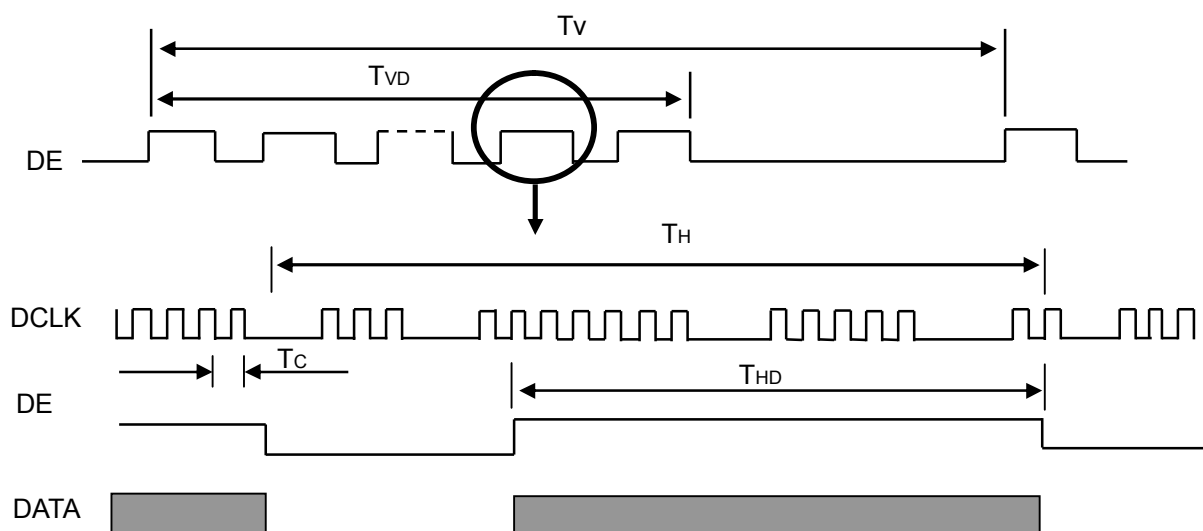
4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.
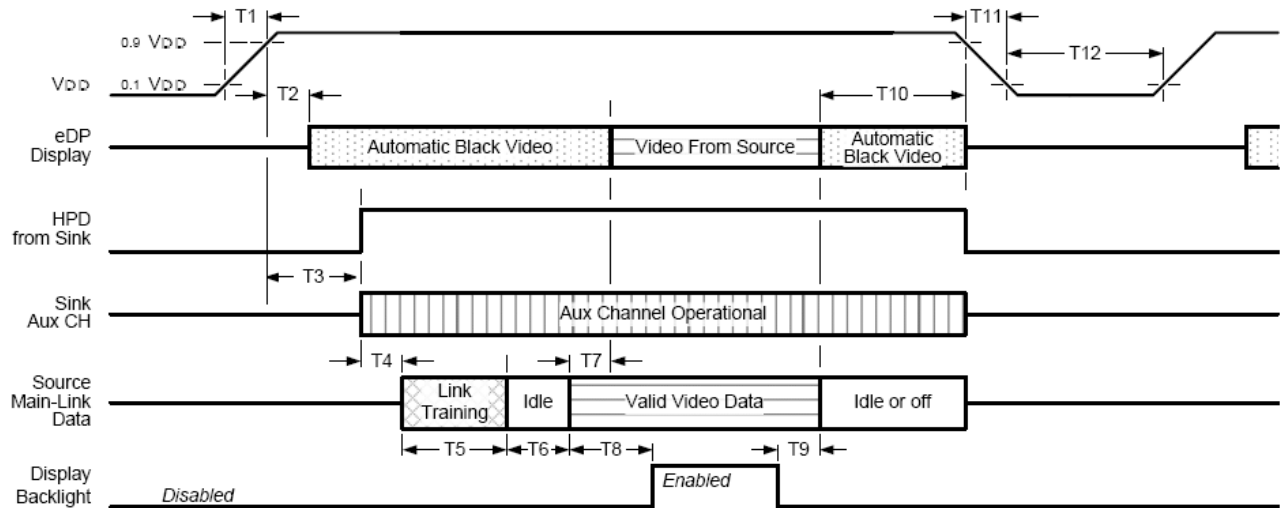
Power ON/OFF Sequence, Normal System Operation

Power ON/OFF Sequence, Aux Channel Transaction Only

Timing Parameter	Description	Required By	Limits		Notes
			Min	Max	
T1	Power rail rise time, 10% to 90%	Source	0.5ms	5ms	
T2	Delay from VDD to automatic Black Video generation	Sink	0ms	200ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes: 1 and 2 below)
T3	Delay from VDD to AUX channel	Sink	120ms	200ms	Source (system) must start sending AUX after TCON ready. (see Note: 3 below)
T4	Delay from HPD(AUX) high to link training initialization	Source	-	30ms	Allows for Source to read Link capability and initialize(EDID) (typ.=17ms)
T5	Link training duration	Source	-	45ms	Dependant on Source link training protocol(typ.=30ms)
T6	Link idle	Source	17ms	17ms	Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization.
T7	Delay from valid video data from Source to video on display	Sink	0ms	50ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video.
T8	Delay from valid video data from Source to backlight enable	Source	17ms	34ms	Source must assure display video is stable
T9	Delay from backlight disable to end of valid video data	Source	-	17ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 1 and 2 below)
T10	Delay from end of valid video data from Source to power off	Source	0ms	500ms	
T11	Power rail fall time, 90% to 10%	Source	-	10ms	
T12	Power off time	Source	500ms	-	

Note 1: The Sink must include the ability to automatically generate Black Video autonomously. The Sink must

automatically enable Black Video under the following conditions:

Upon V_{DD} power-on (within T2 max)When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source

(at the end of T9) When no Main Link data, or invalid video data, is received from the Source. Black Video must be

displayed within 50ms (max) from the start of either condition. Video data can be deemed invalid based on MSA and

timing information, for example.

Note 2: The Sink may implement the ability to disable the automatic Black Video function, as described in Note 1,

above, for system development and debugging purposes.

Note 3: The Sink (panel) can support AUX Channel polling by the Source after panel V_{DD} power-on for 120ms later. The Sink

must be able to respond to an AUX Channel transaction with the time specified within T3.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "4.3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	126	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		500	650	-	-	(2), (5) (7)
Response Time		$T_{on}+ T_{off}$		-	11	21	ms	(3),(7)
Luminance of White		L_{AVE}		255	300	-	cd/m²	(4), (6),(7)
Color Chromaticity	Red	Rx	θ_x=0°, θ_Y =0° Viewing Normal Angle	Typ – 0.03	0.626	Typ + 0.03	-	(1),(7)
		Ry			0.340		-	
	Green	Gx			0.349		-	
		Gy			0.590		-	
	Blue	Bx			0.158		-	
		By			0.073		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	40	45		Deg.	(1),(5) ,(7)
		θ_x-		40	45	-		
	Vertical	θ_Y+		15	20	-		
		θ_Y-		40	45	-		
White Variation of 5 Points		δW_{5p}	θ_x=0°, θ_Y =0°	80	-	-	%	(5),(6) (7)

Note (1) Definition of Viewing Angle (θx, θy):
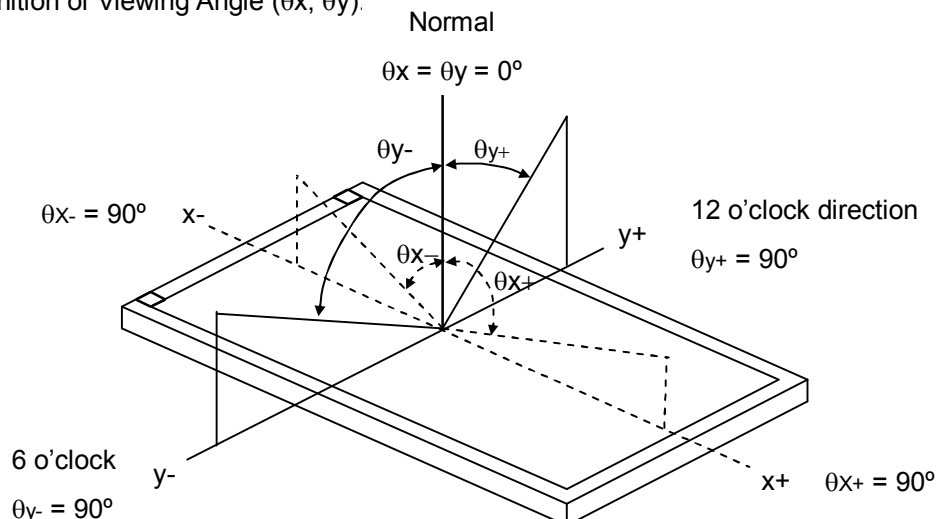
Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.
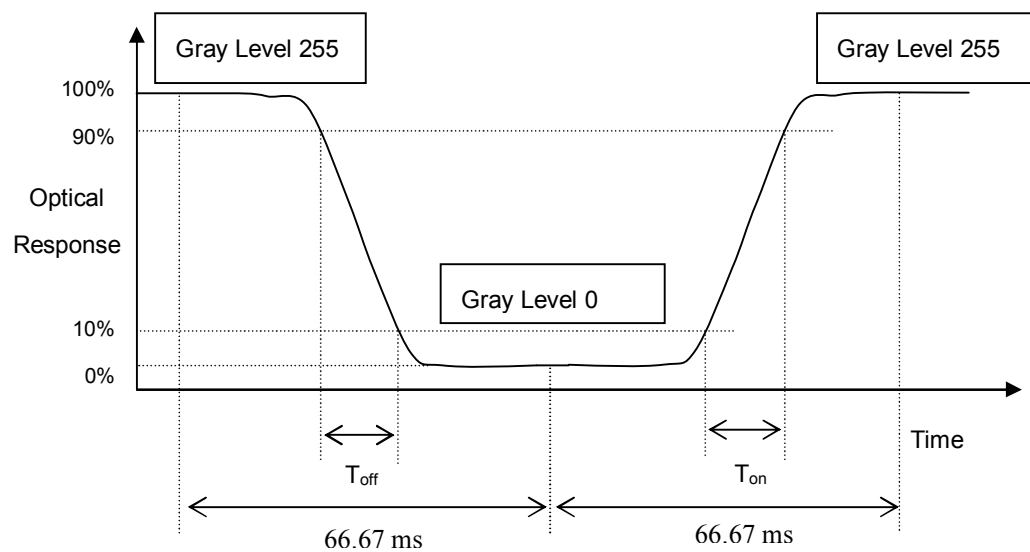
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_{on}, T_{off}):

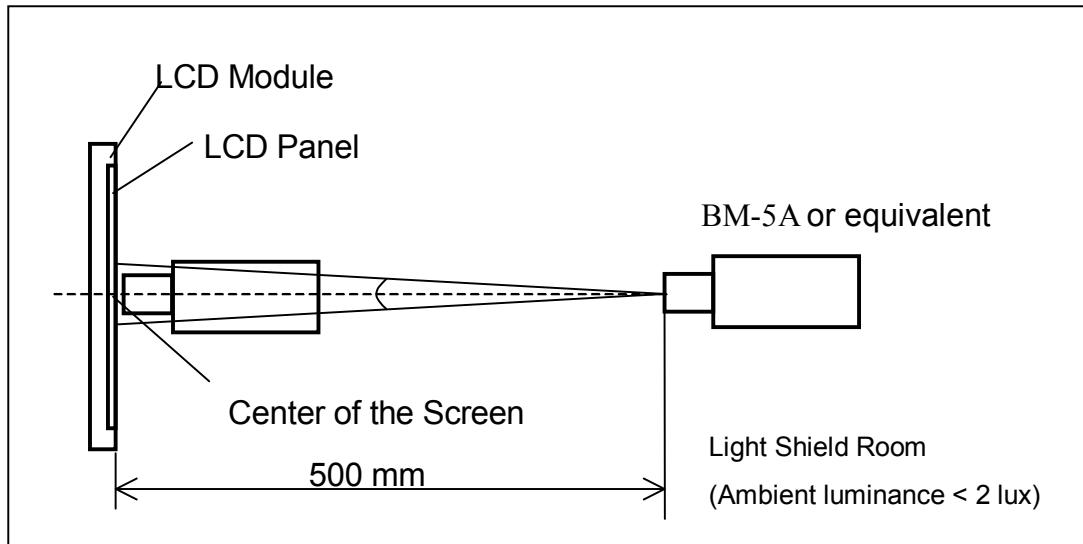
Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of gray level 255 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)
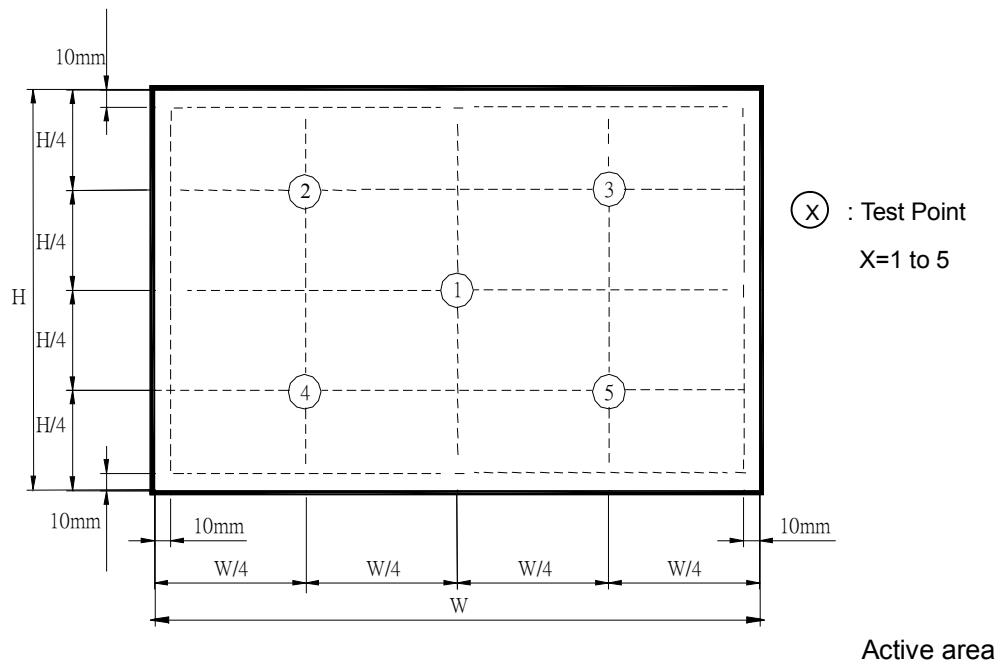
Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 10 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 10 minutes in a windless room.

LCD Module

LCD Panel

BM-5A or equivalent

Center of the Screen

500 mm

Light Shield Room

(Ambient luminance < 2 lux)

Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW_{5p} = {Minimum [L (1) ~ L (5)] / Maximum [L (1) ~ L (5)]}*100%

10mm

H/4

H/4

H

H/4

H/4

10mm

10mm

W/4   W/4   W/4   W/4

10mm

W

$\overline{X}$: Test Point

X=1 to 5

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEMS

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour⟷60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50ºC, RH 80%, 240hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) Criteria: Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hours.

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.
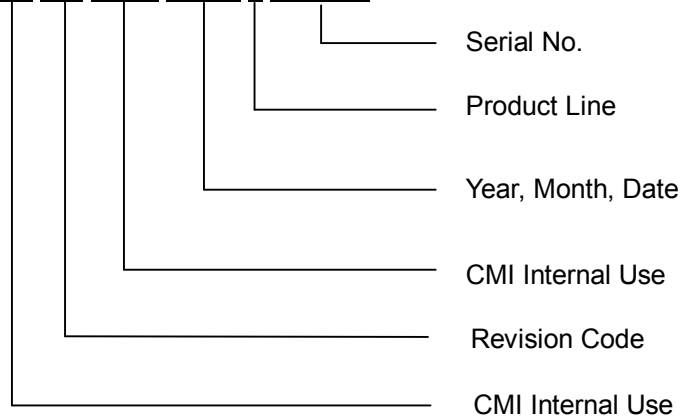
7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N144NGE – E41

(b) Serial ID: X X X X X X X Y M D L N N N N

- Serial No.
- Product Line
- Year, Month, Date
- CMI Internal Use
- Revision Code
- CMI Internal Use

Serial ID includes the information as below:

    (a) Manufactured Date: Year: 0~9, for 2010~2019

                        Month: 1~9, A~C, for Jan. ~ Dec.

                        Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

    (b) Revision Code: cover all the change

    (c) Serial No.: Manufacturing sequence of product

    (d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

    (e) UL logo: XXXX is UL factory ID

7.2 CARTON

```
Box Dimensions : 492(L)*397(W)*250(H)
(25 module .per. 1 box)
```


5pcs/set

LCD Module

Tray

Anti-static Bag

cushion

Paper cushion

cushion

Input

25pcs/Box

Outer Box

Carton Label

Tape

7.3 PALLET

天地蓋×1

70

1200

1000

Carton×18

765

255

1191

397

492

984

護角×4

765

50

50

1200

1000

隔板×1

棧板×1

140

1200

1000
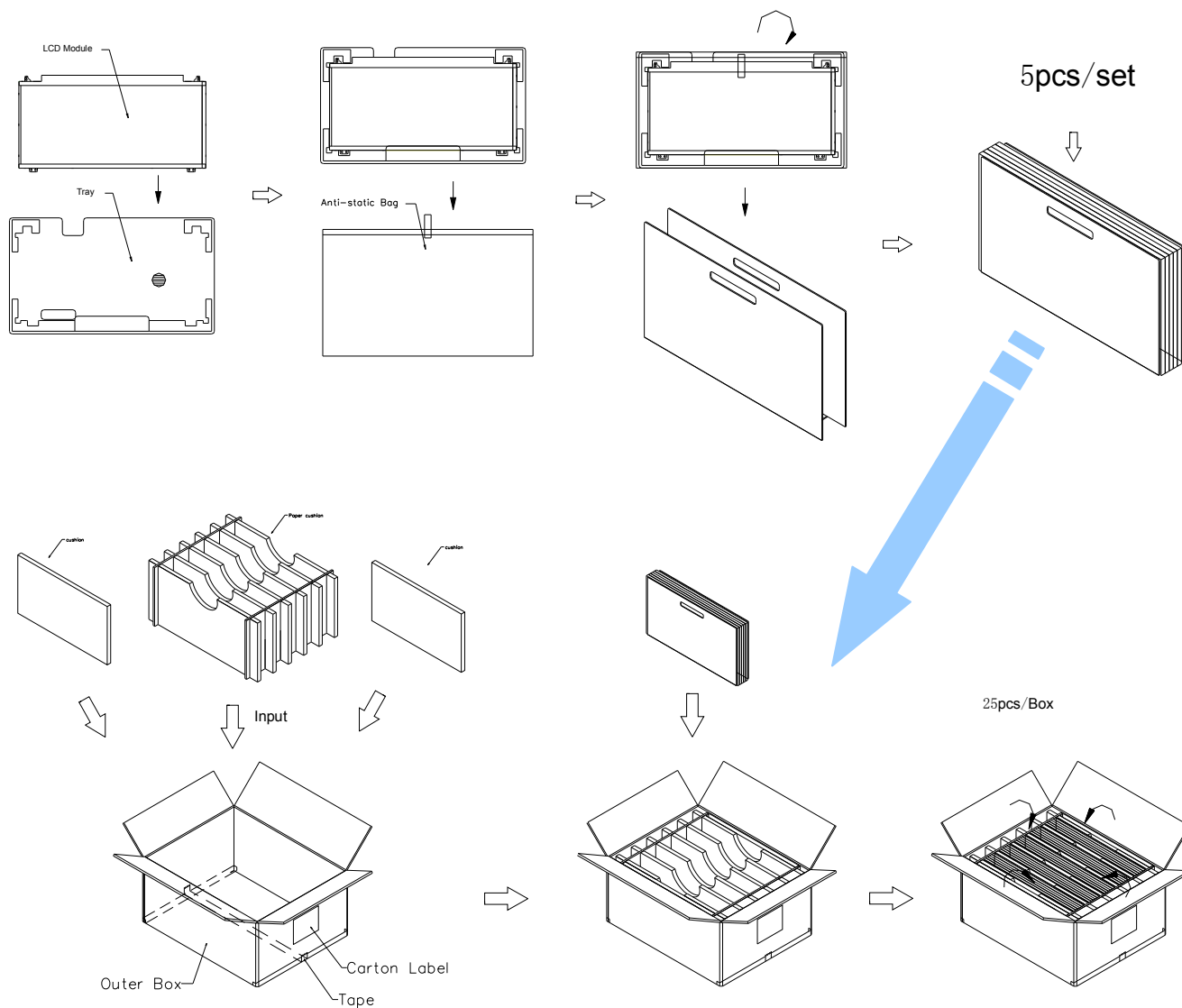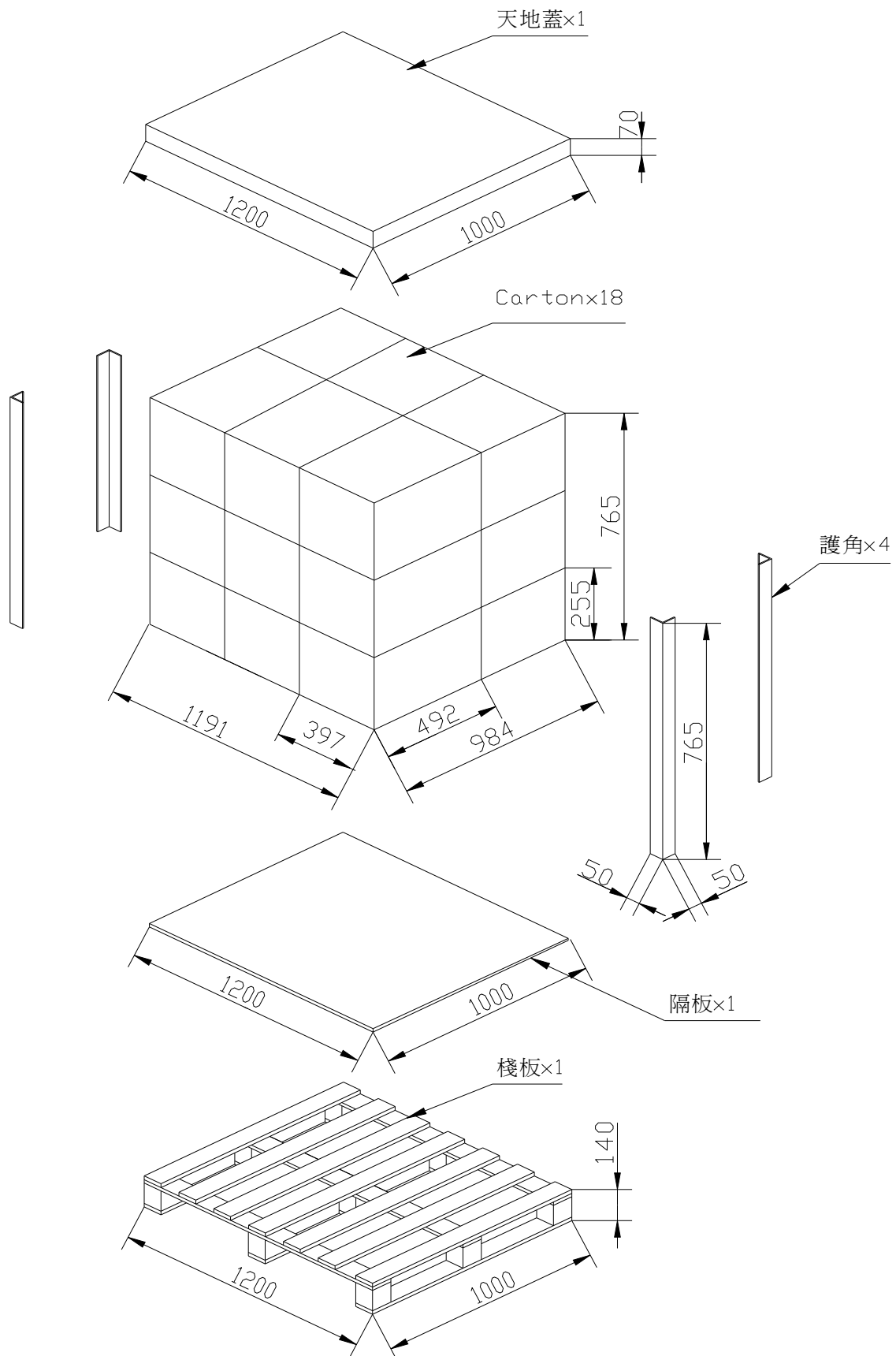
8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it could be assembled in the clean area only. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

APPENDIX. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data follows Standard format which are defined in the VESA Plug & Display and FPDI standards.
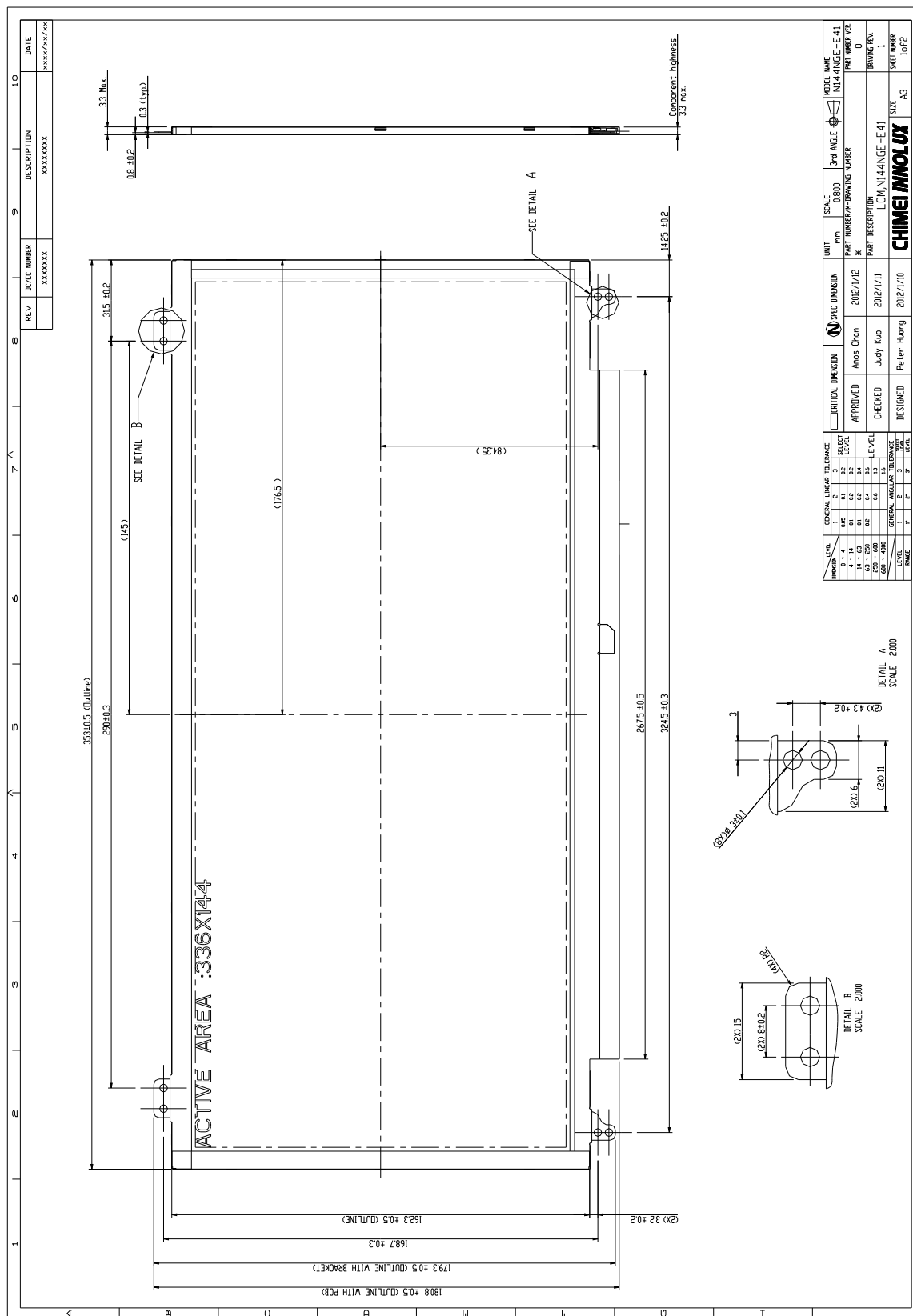
Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMN")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AE	10101110
10	0A	ID product code(00h if not used)	23	00100011
11	0B	ID product code (hex LSB first; 00h if not used)	11	00010001
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed "00H")	00	00000000
17	11	Year of manufacture (2012)	16	00010110
18	12	EDID structure version # ("1")	01	00000001
19	13	EDID revision # ("4")	04	00000100
20	14	Video I/P definition ("digital I/P")	A5	10100101
21	15	Max H image size ("33cm")	21	00100001
22	16	Max V image size ("14cm")	0E	00001110
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("Active off, RGB Color")	0A	00001010
25	19	Red/Green (Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0)	44	01000100
26	1A	Blue/White (Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0)	B5	10110101
27	1B	Red-x (Rx = "0.626")	A0	10100000
28	1C	Red-y (Ry = "0.340")	57	01010111
29	1D	Green-x (Gx = " 0.349")	59	01011001
30	1E	Green-y (Gy = " 0.590")	97	10010111
31	1F	Blue-x (Bx = " 0.158")	28	00101000
32	20	Blue-y (By = " 0.073")	12	00010010
33	21	White-x (Wx = " 0.313 ")	50	01010000
34	22	White-y (Wy = " 0.329")	54	01010100
35	23	Established timings 1(00h if not used)	00	00000000
36	24	Established timings 2(00h if not used)	00	00000000
37	25	Manufacturer's reserved timings(00h if not used)	00	00000000
38	26	Standard timing ID # 1(01h if not used)	01	00000001
39	27	Standard timing ID # 1(01h if not used)	01	00000001
40	28	Standard timing ID # 2(01h if not used)	01	00000001
41	29	Standard timing ID # 2(01h if not used)	01	00000001

42	2A	Standard timing ID # 3(01h if not used)	01	00000001
43	2B	Standard timing ID # 3(01h if not used)	01	00000001
44	2C	Standard timing ID # 4(01h if not used)	01	00000001
45	2D	Standard timing ID # 4(01h if not used)	01	00000001
46	2E	Standard timing ID # 5(01h if not used)	01	00000001
47	2F	Standard timing ID # 5(01h if not used)	01	00000001
48	30	Standard timing ID # 6(01h if not used)	01	00000001
49	31	Standard timing ID # 6(01h if not used)	01	00000001
50	32	Standard timing ID # 7(01h if not used)	01	00000001
51	33	Standard timing ID # 7(01h if not used)	01	00000001
52	34	Standard timing ID # 8(01h if not used)	01	00000001
53	35	Standard timing ID # 8(01h if not used)	01	00000001
54	36	#Pixel Clock (Pixel Clock=100MHz) (LSB) Fv=60Hz	10	00010000
55	37	#Pixel Clock (Pixel Clock=100MHz) (MSB)	27	00100111
56	38	# 1 H active ("1792")	00	00000000
57	39	# 1 H blank ("286")	1E	00011110
58	3A	# 1 H active : H blank ("1792 :286")	71	01110001
59	3B	# 1 V active ("768")	00	00000000
60	3C	# 1 V blank ("34")	22	00100010
61	3D	# 1 V active : V blank ("768 :34")	30	00110000
62	3E	# 1 H sync offset ("12")	0C	00001100
63	3F	# 1 H sync pulse width ("64")	40	01000000
64	40	# 1 V sync offset : V sync pulse width ("3 : 3")	33	00110011
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("12: 64 : 3 : 3")	00	00000000
66	42	# 1 H image size ("344 mm")	50	01010000
67	43	# 1 V image size ("193 mm")	90	10010000
68	44	# 1 H image size : V image size ("336 : 144")	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	Bit[7] 0:Non-interlace,1:Interlace Bit[6:5]00:Normal display, no stereo ,XX: See table xx for definition Bit[4:3]00:Analog composite,01:Bipolar analog composite,10:Digital composite,11:Digital separate Bit[2:1]:The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3-see Table 3.18 Bit[0]:See Table VESA EDID spec for definition Referenced Default=1Ah	1A	00011010
72	48	Monitor description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74	4A	# 2 Reserved	00	00000000
75	4B	# 2 FE (hex) defines ASCII string (Model Name "N144NGE-E41", ASCII)	FE	11111110
76	4C	# 2 Flag	00	00000000
77	4D	# 2 1st character of name ("N")	4E	01001110
78	4E	# 2 2nd character of name ("1")	31	00110001
79	4F	# 2 3rd character of name ("4")	34	00110100
80	50	# 2 4th character of name ("4")	34	00110100
81	51	# 2 5th character of name ("N")	4E	01001110
82	52	# 2 6th character of name ("G")	47	01000111

83	53	# 2 7th character of name ("E")	45	01000101
84	54	# 2 8th character of name ("-")	2D	00101101
85	55	# 2 9th character of name ("E")	45	01000101
86	56	# 2 9th character of name ("4")	34	00110100
87	57	# 2 New line character indicates end of ASCII string("1")	31	00110001
88	58	# 2 Padding with "Blank" character	0A	00001010
89	59	# 2 Padding with "Blank" character	20	00100000
90	5A	Monitor description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Vendor "CMN", ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 1st character of string ("C")	43	01000011
96	60	# 3 2nd character of string ("M")	4D	01001101
97	61	# 3 3rd character of string ("N")	4E	01001110
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with "Blank" character	20	00100000
100	64	# 3 Padding with "Blank" character	20	00100000
101	65	# 3 Padding with "Blank" character	20	00100000
102	66	# 3 Padding with "Blank" character	20	00100000
103	67	# 3 Padding with "Blank" character	20	00100000
104	68	# 3 Padding with "Blank" character	20	00100000
105	69	# 3 Padding with "Blank" character	20	00100000
106	6A	# 3 Padding with "Blank" character	20	00100000
107	6B	# 3 Padding with "Blank" character	20	00100000
108	6C	Monitor description # 4 (Not Used)	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 FE (hex) defines ASCII string	FE	00010000
112	70	# 4 Flag	00	00000000
113	71	# 2 1st character of name ("N")	4E	00000011
114	72	# 2 2nd character of name ("1")	31	01000001
115	73	# 2 3rd character of name ("4")	34	00000001
116	74	# 2 4th character of name ("4")	34	00011001
117	75	# 2 5th character of name ("N")	4E	00000000
118	76	# 2 6th character of name ("G")	47	00000000
119	77	# 2 7th character of name ("E")	45	00000000
120	78	# 2 8th character of name ("-")	2D	00000000
121	79	# 2 9th character of name ("E")	45	00001001
122	7A	# 2 9th character of name ("4")	34	00000001
123	7B	# 4 New line character indicates end of ASCII string("1")	31	00001010
124	7C	# 4 Padding with "Blank" character	0A	00100000
125	7D	# 4 Padding with "Blank" character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	B1	10110001

APPENDIX. OUTLINE DRAWING

Front view

Rear view