(V) Preliminary Specifications
( ) Final Specifications

Module	**13.3”(13.26”) FHD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	**G133HAN02.2**
Note ( )	***LED Backlight with driving circuit design***

Customer **Date**	**Approved by** **Date**
	_____ 2020/9/30
Checked & Approved by **Date**	**Prepared by** **Date**
	_____ 2020/9/30
Note: This Specification is subject to change without notice.	**AU Optronics corporation**

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1	All	First Edition		
0.2 2021/12/8	6	OP Temp:0~50℃	OP Temp:0~60℃(panel surface temp)	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.
13) Continuous displaying fixed pattern may induce image sticking or abnormal display . It's recommended to use screen saver or power off panel periodically.

2. General Description

G133HAN02.2 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x1080(V) screen and 16.2M colors with LED backlight driving circuit. All input signals are eDP (Embedded DisplayPort) interface compatible.

G133HAN02.2 is designed for industrial display applications.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	**Unit**	**Specifications**			
Screen Diagonal	[mm]	336.71			
Active Area	[mm]	293.472x165.078			
Pixels H x V		1920x3(RGB) x 1080			
Pixel Pitch	[mm]	0.1529 x 0.1529			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (I_{LED}=20mA) (Note: ILED is LED current)	[cd/m^2]	500 typ. (center point)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		800 typ			
Response Time	[ms]	27 typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	TBD			
Weight	[Grams]	280 max			
Physical Size **Include bracket**	[mm]		**Min.**	**Typ.**	**Max.**
		Length	**194.8**	**195.3**	**195.8**
		Width	**305.8**	**306.3**	**306.8**
		Thickness	**-**	**-**	**3.0 (Panel Side) 3.2 (PCBA Side)**
Electrical Interface		2 Lane eDP 1.2			

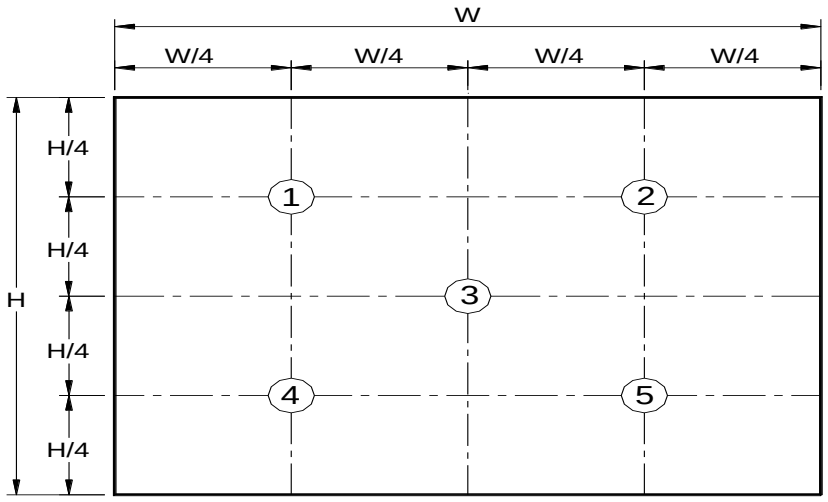
Glass Thickness	[mm]	0.4
Surface Treatment		Glare
Support Color		16.2M colors
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +60 (panel surface temp) -20 to +60
RoHS Compliance		RoHS Compliance

2.3 Optical Characteristics

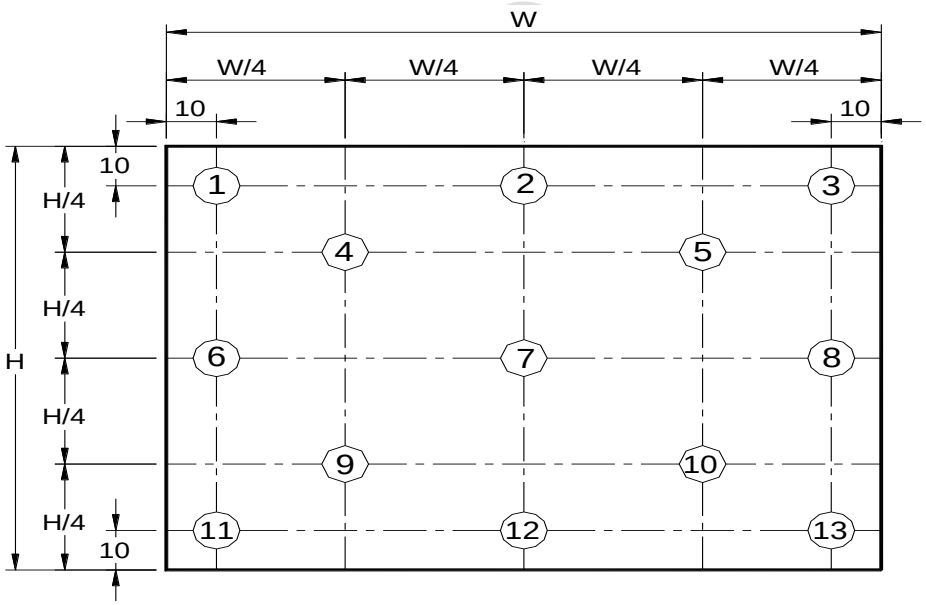
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=20mA (Base Panel Only)			Center point	400	500	-	cd/m2	1, 4, 5.
Viewing Angle		θR θL	Horizontal (Right) CR = 10 (Left)	80 80	89 89	- -	degree	4, 9
		ψH ψL	Vertical (Upper) CR = 10 (Lower)	80 80	89 89	- -		
Luminance Uniformity		δ5P	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ13P	13 Points	-	-	1.6		2, 3, 4
Contrast Ratio		CR		600	800	-		4, 6
Cross talk		%				1.5		4, 7
Response Time		TRT	Rising + Falling	-	27	-		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931		TBD		-	4
		Ry			TBD		-	
	Green	Gx			TBD		-	
		Gy			TBD		-	
	Blue	Bx			TBD		-	
		By			TBD		-	
	White	Wx		0.283	0.313	0.343	-	
		Wy		0.299	0.329	0.359		
NTSC		%		-	45	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

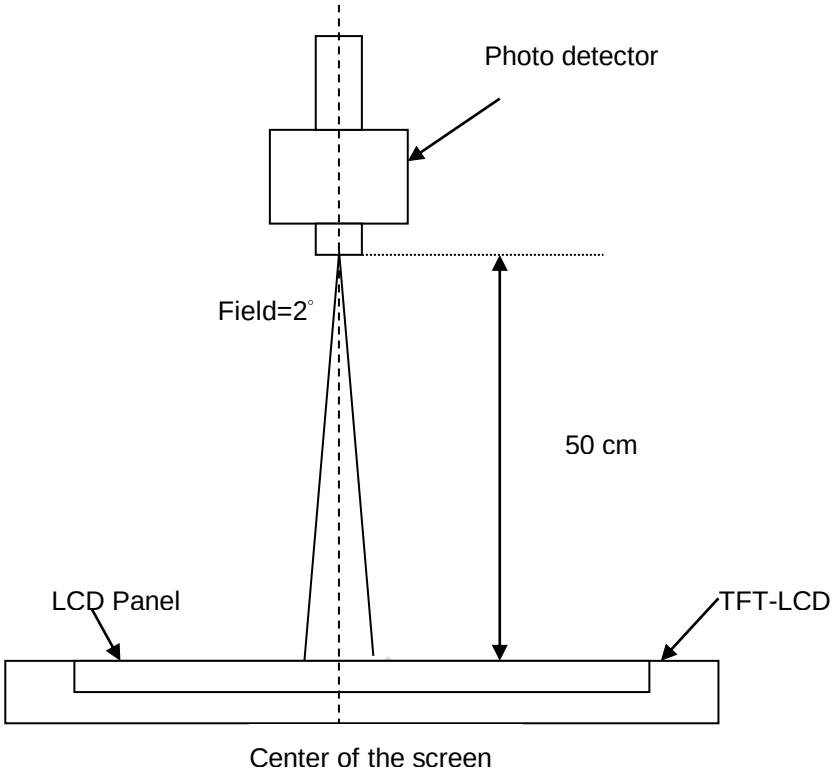
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after

lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

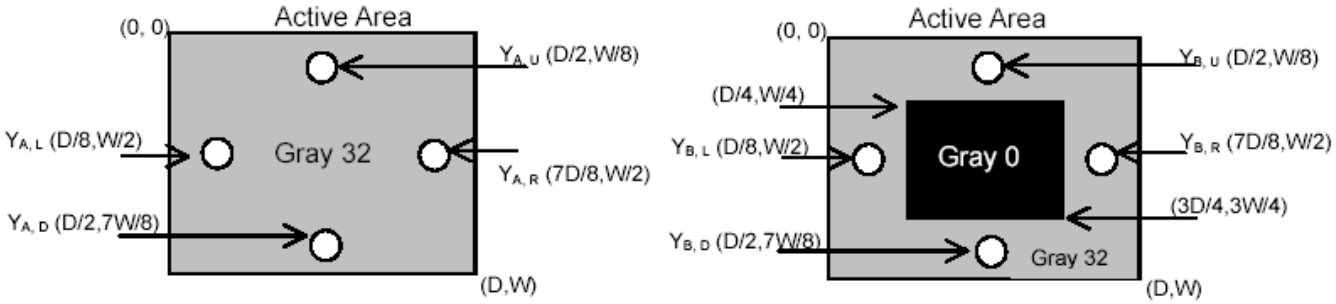
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where

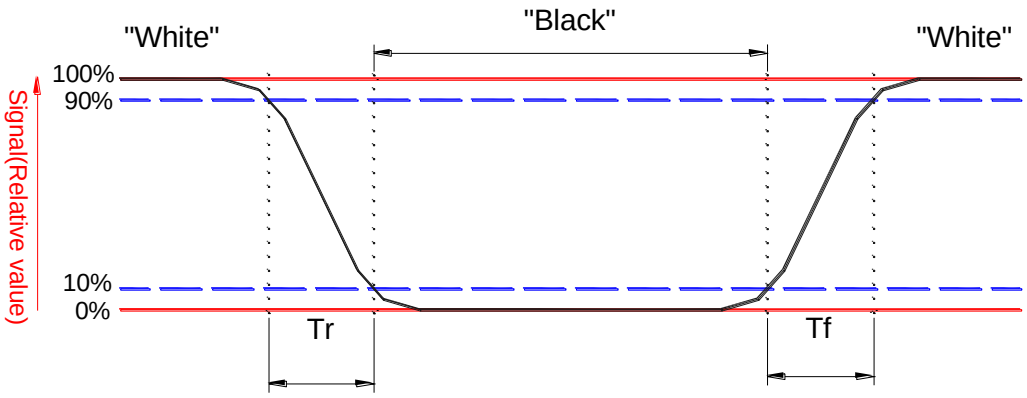
Y_A = Luminance of measured location without gray level 0 pattern (cd/m$_2$)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m$_2$)



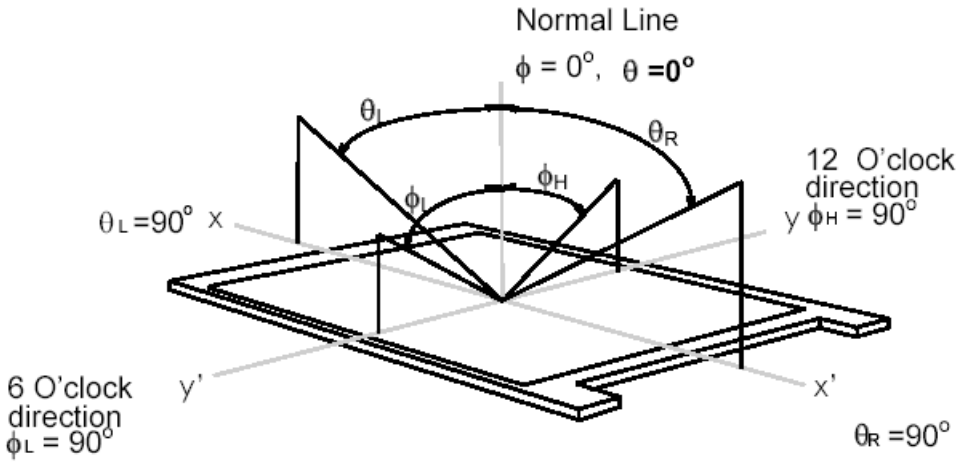
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.

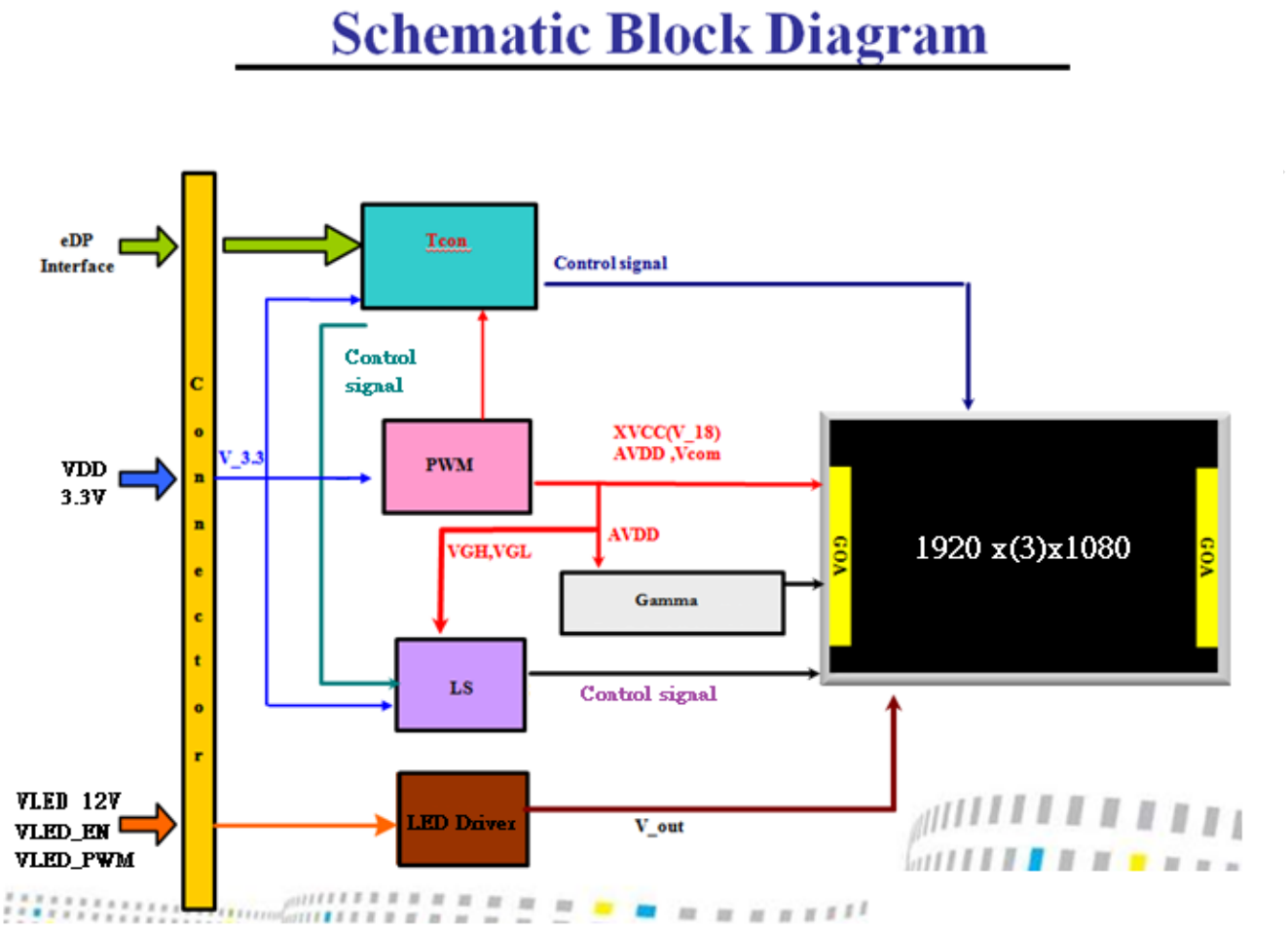


Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	VDD	-0.3	4	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

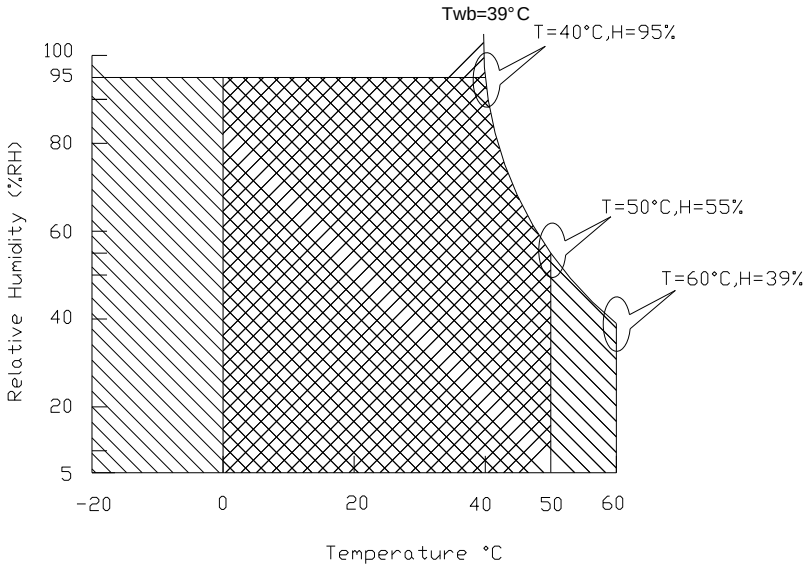
Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

Note 5: The packing material of system forbid to involve ammonium component

Note 6: The reliability test conditions of system do not exceed the verified conditions of TFT module

Note 7: Be sure the panel test condition do not exceed the component limitation of TFT module(TN Liquid crystal , for example)



5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows:

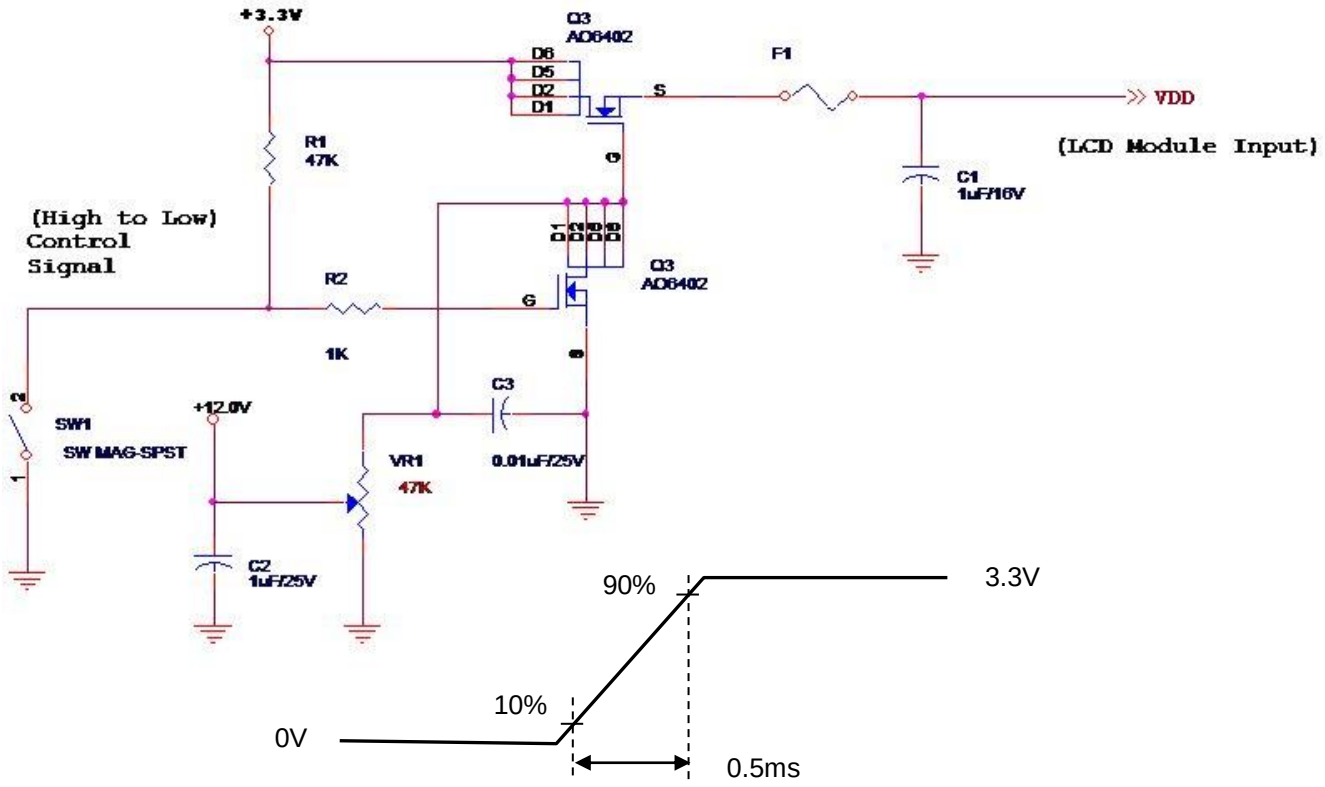
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Note 1
PDD	VDD Power	-	0.7	0.8	[Watt]	Note 2
IDD	IDD Current	-	231	242	[mA]	Note 2
IRush	Inrush Current	-	-	1500	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Measure in panel VDD

Note 2 : Maximum Measurement Condition：White pattern at VDD: 3.3V driving voltage.

Note 3：Measure Condition



Vin rising time

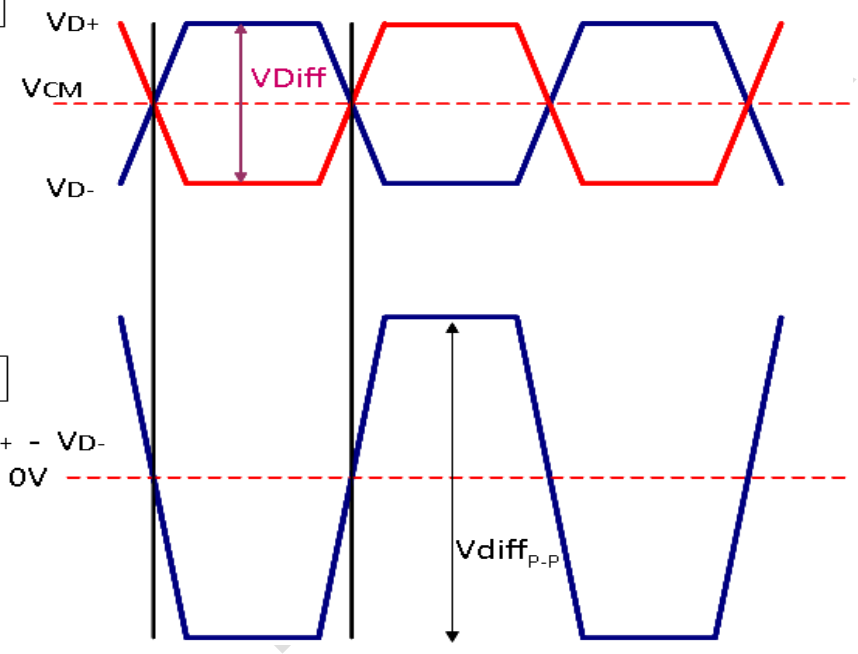
5.1.2 Signal Electrical Characteristics

Signal electrical characteristics are as follows;

Display Port main link signal:

Differential pair VD+ , VD- Which is one Display port Main link

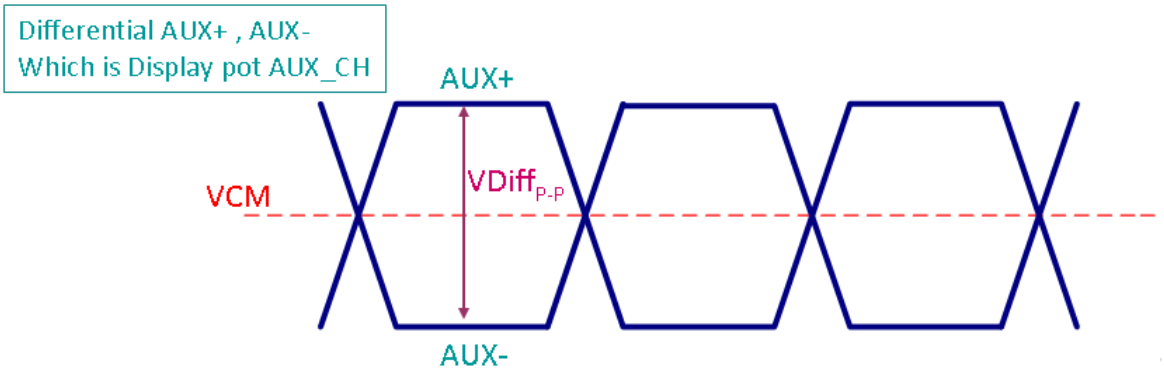
VCM of Display port Main link



$Vdiff_{P-P} = [(VD+) - (VD-)] \times 2$

Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	150		1380	mV

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	290		1380	mV

Display Port V_{HPD} signal:

Display port V_{HPD}					
		Min	Typ	Max	unit
V_{HPD}	HPD Voltage	3	-	3.6	V

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	TBD	[Watt]	**(Ta=25℃), Note 1**
LED Life-Time	N/A	50,000	-	-	Hour	**(Ta=25℃), Note 2**

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED (Note 1)	10.0	12.0	13.2	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN (Note 2)	2.2	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.6	[Volt]	
PWM Logic Input High Level	VLED_PWM (Note 2)	2.2	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.6	[Volt]	
PWM Input Frequency	FPWM	200	1K	20K	Hz	
PWM Duty Ratio	Duty	1 (Note 3)	--	100	%	

Note 1 : Measured in panel VLED

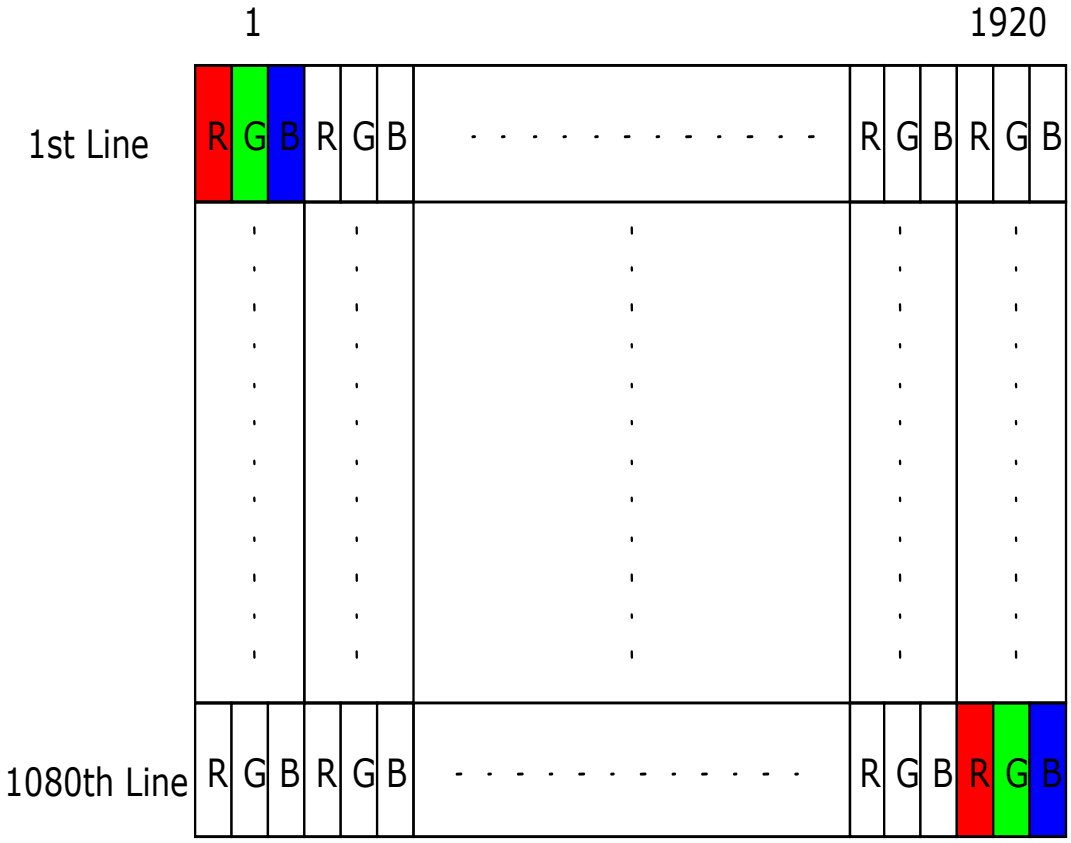
Note 2 : Recommend system pull up/down resistor no bigger than 10kohm

Note 3 : If the PWM duty ratio(min) is set between 5% to 1%，the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

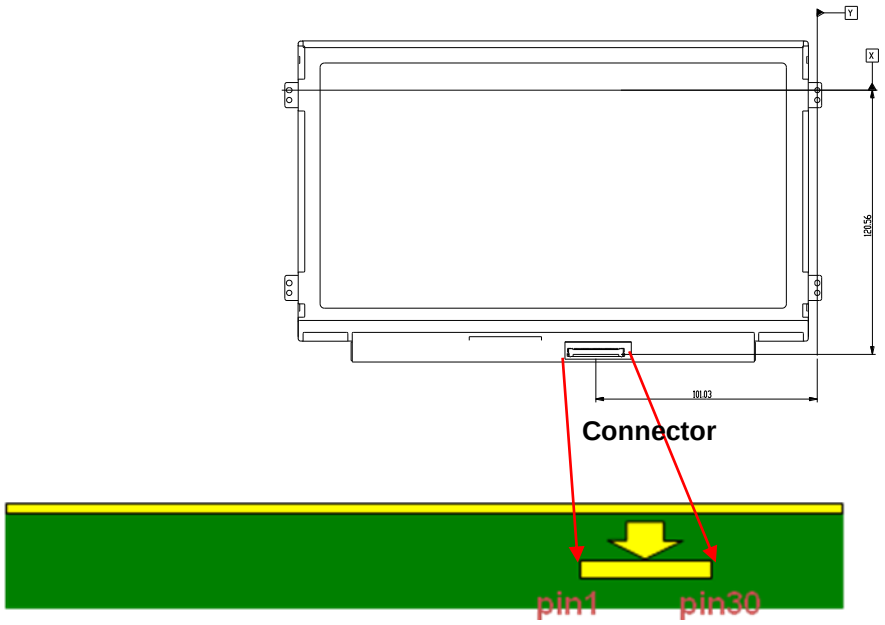
Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX
Type / Part Number	IPEX 20765-030E-11A (0.5mm pitch)
Mating Housing/Part Number	IPX or compatible

6.2.2 Pin Assignment

Pin	Symbol	Description
1	NC	Reserved for LCD supplier
2	GND	High Speed Ground
3	Lane1_N	Complement Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	GND	High Speed Ground
6	Lane0_N	Complement Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Channel
10	AUX_CH_N	Complement Signal Auxiliary Channel
11	GND	High Speed Ground
12	VDD	LCD logic power
13	VDD	LCD logic power
14	NC	LCD Panel Self Test Enable (Optional)
15	GND	LCD logic and driver ground
16	GND	LCD logic and driver ground
17	HPD	HPD Signal pin
18	BL_GND	LED Backlight ground
19	BL_GND	LED Backlight ground
20	BL_GND	LED Backlight ground
21	BL_GND	LED Backlight ground
22	VLED_EN	LED Backlight control on/off control
23	VLED_PWM	System PWM signal input for dimming
24	NC	Reserved for LCD supplier
25	NC	Reserved for LCD supplier
26	VLED	LED Backlight Power
27	VLED	LED Backlight Power
28	VLED	LED Backlight Power
29	VLED	LED Backlight Power
30	NC	Reserved for LCD supplier



Note1: Start from right side.
Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.

6.3 Interface Timing

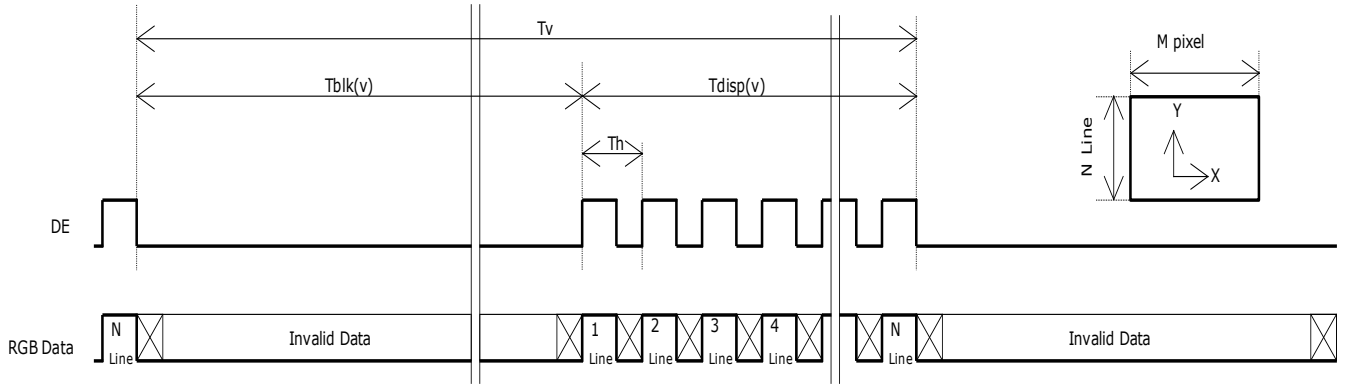
6.3.1 Timing Characteristics

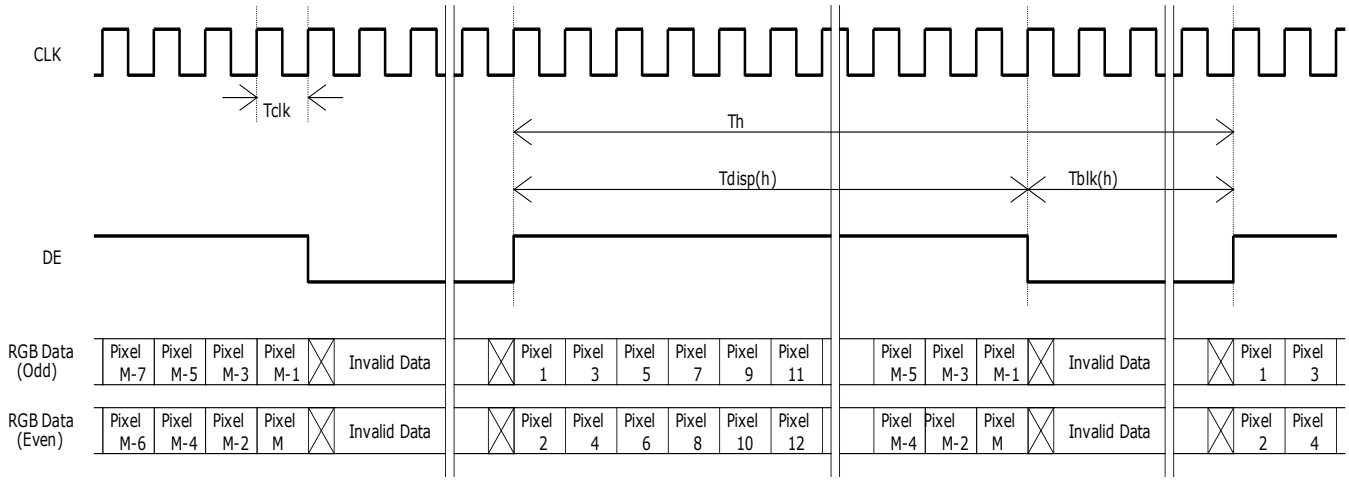
Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-		60	-	Hz
Clock frequency		1/ T_{Clock}	68	70.5	75.9	MHz
Vertical Section	Period	T_V	1100	1116	1150	T_{Line}
	Active	T_{VD}	1080			
	Blanking	T_{VB}	20	36	70	
Horizontal Section	Period	T_H	1030	1052	1100	T_{Clock}
	Active	T_{HD}	960			
	Blanking	T_{HB}	70	92	140	

Note 1 : The above is as optimized setting

6.3.2 Timing diagram

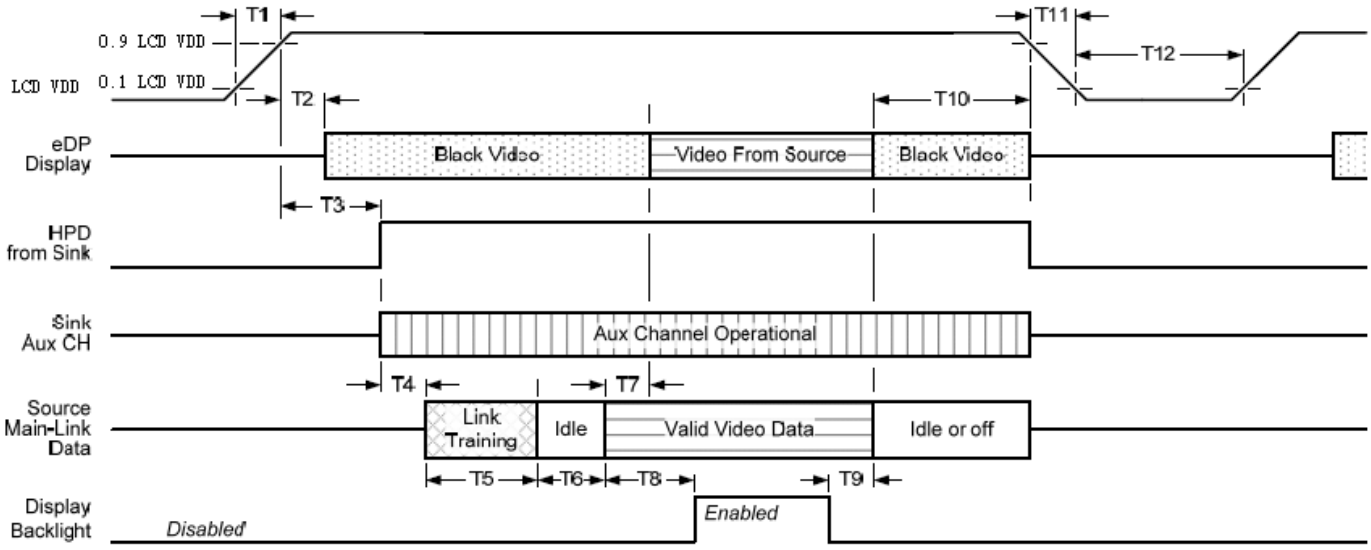




6.4 Power ON/OFF Sequence

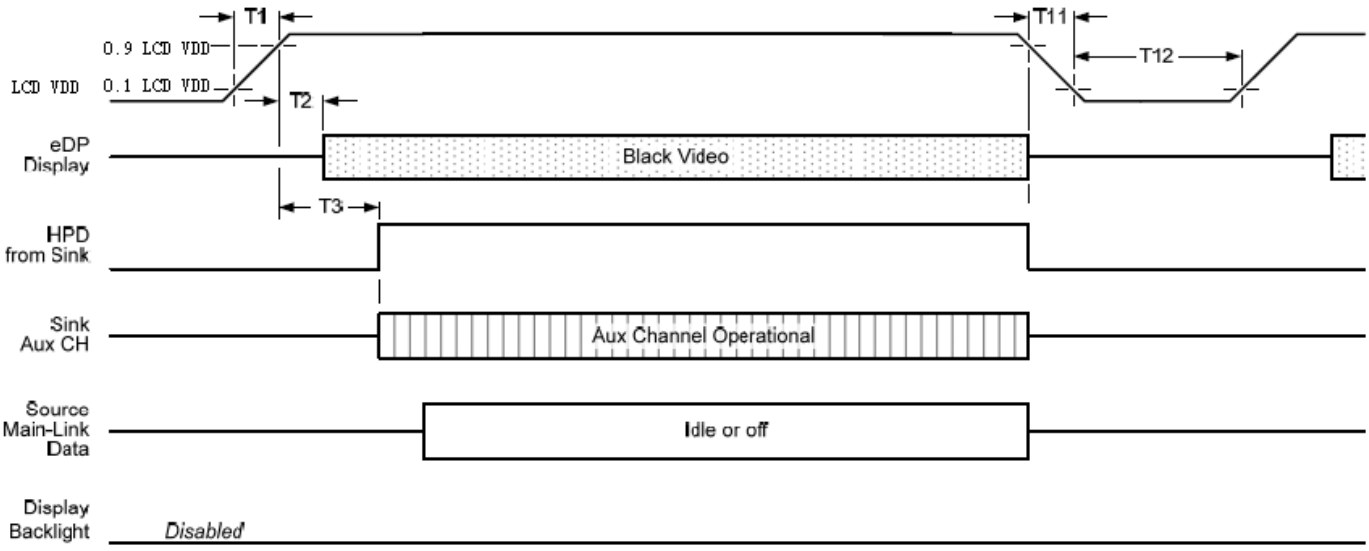
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

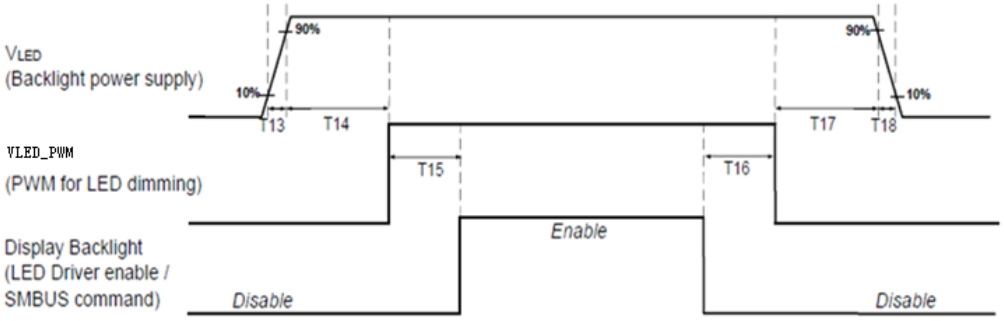
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCD VDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCD VDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:

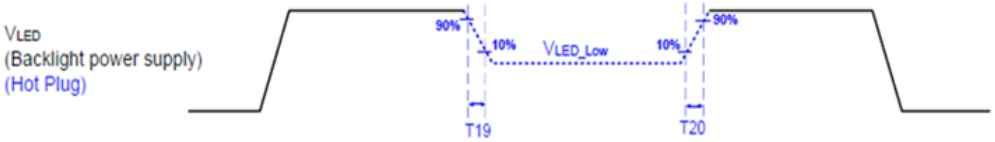


	Min (ms)	Max (ms)
T13	0.2	10
T14	0	-
T15	0	-
T16	0	-
T17	0	-
T18	0.2	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



Note 1 : If T14,T15,T16,T17<10ms，The display garbage may occur. We suggest T14,T15,T16,T17>10ms to avoid the display garbage.

Note 2：If T13 or T18<0.5ms，the inrush current may cause the damage of fuse. If T13 or T18<0.5ms，the inrush current I^2t is under typical melt of fuse Spec.，there is no mentioned problem.

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

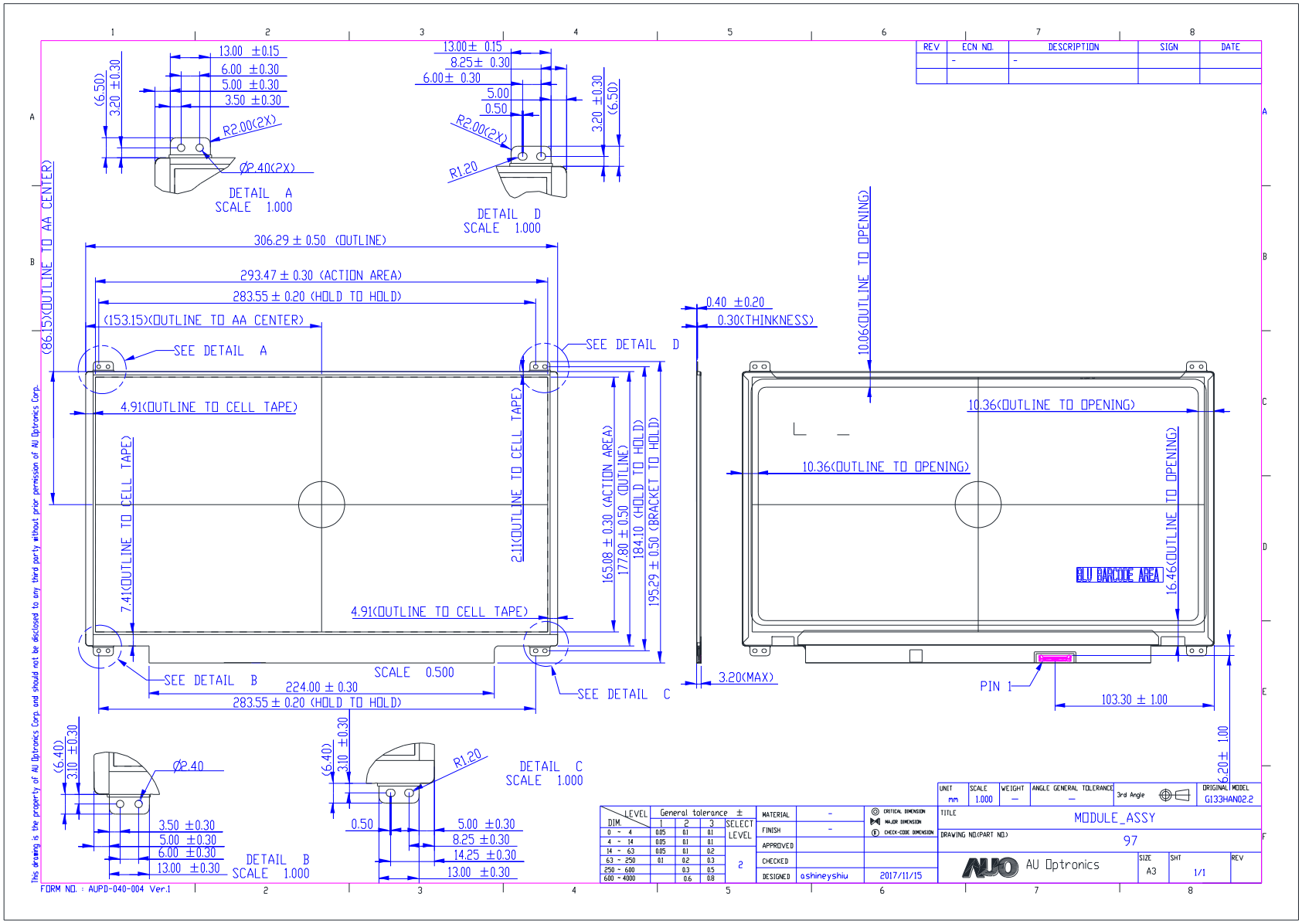
7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta=0℃, 300h	
High Temperature Storage	Ta= 60℃, 300h	
Low Temperature Storage	Ta= -20℃, 250h	
Thermal Shock Test	Ta=-20℃(30min) ~60℃(30min), 100cycles condition.	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

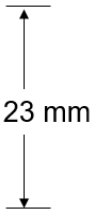
8. Mechanical Characteristics

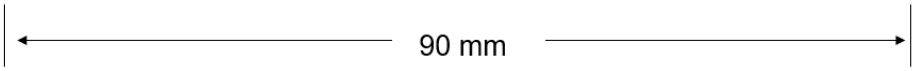
8.1 Outline Dimension



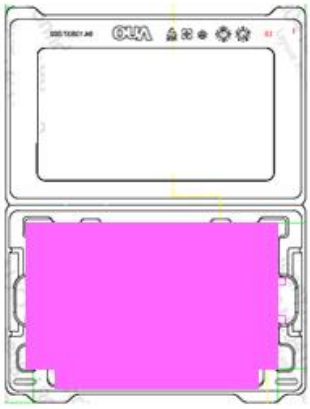
9. Shipping and Package

9.1 Shipping Label Format

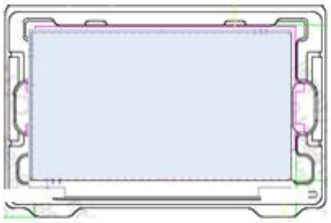




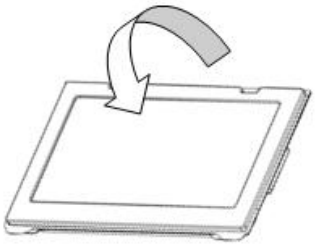
9.2 Carton Package



Spacer



Put TP Glass top



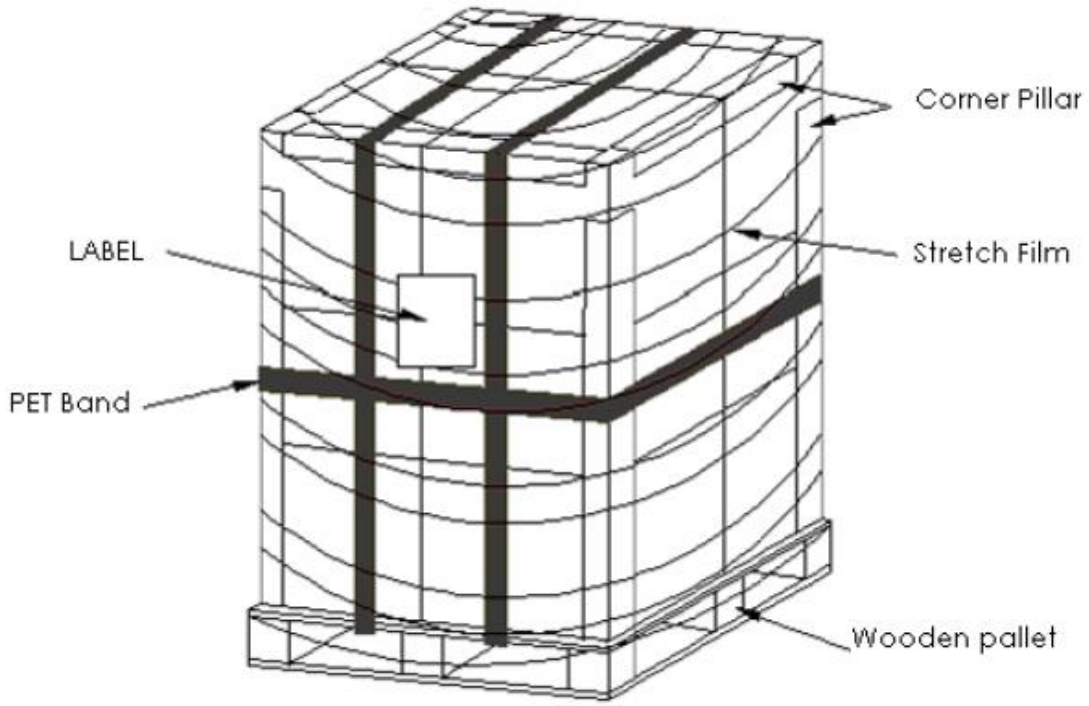
1 TRAY BOX with 5 pcs Panel
With 5 pcs spacer

9 TRAY box in carton

Put EPS BOX into ESD bag

Total 45 pcs /carton

9.3 Shipping Package of Palletizing Sequence



Item	Specification			Remark
	Q'ty	Dimension	Weight (kg)	
Packing Material	1	446(L)mm x373(W)mm x 293(H)mm	1.4	TRAY +Box
Packing	45 pcs/carton	446(L)mm x373(W)mm x 293(H)mm	11.8	with panel & cushion
Pallet	1	1150(L)mm x 910(W)mm x 132(H)mm	14	
Pallet after Packing	boxes/pallet	1150(L)mm x 910(W)mm x 1304(H)mm	300	24 carton

10. Appendix: EDID Description

Address	FUNCTION	Value
HEX		HEX
00	Header	00
01		FF
02		FF
03		FF
04		FF
05		FF
06		FF
07		00
08	EISA Manuf. Code LSB	06
09	Compressed ASCII	AF
0A	Product Code	2D
0B	hex, LSB first	22
0C	32-bit ser #	00
0D		00
0E		00
0F		00
10	Week of manufacture	28
11	Year of manufacture	1F
12	EDID Structure Ver.	01
13	EDID revision #	04
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	A0
15	**Max H image size** *(rounded to cm)*	1D
16	**Max V image size** *(rounded to cm)*	11
17	**Display Gamma** *(=(gamma*100)-100)*	78
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02
19	Red/green low bits **(Lower 2:2:2:2 bits)**	59
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	B5
1B	Red x **(Upper 8 bits)**	92
1C	Red y/ highER 8 bits	58
1D	Green x	58
1E	Green y	92
1F	Blue x	28
20	Blue y	1E
21	White x	50
22	White y	54
23	Established timing 1	00
24	Established timing 2	00
25	Established timing 3	00
26	Standard timing #1	01
27		01
28	Standard timing #2	01
29		01
2A	Standard timing #3	01
2B		01
2C	Standard timing #4	01

2D		01
2E	Standard timing #5	01
2F		01
30	Standard timing #6	01
31		01
32	Standard timing #7	01
33		01
34	Standard timing #8	01
35		01
36	Pixel Clock/10000 LSB	14
37	Pixel Clock/10000 USB	37
38	Horz active **Lower 8bits**	80
39	Horz blanking **Lower 8bits**	B8
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	70
3B	Vertical Active **Lower 8bits**	38
3C	Vertical Blanking **Lower 8bits**	24
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40
3E	HorzSync. Offset	10
3F	HorzSync.Width	10
40	VertSync.Offset : VertSync.Width	3E
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00
42	Horizontal Image Size **Lower 8bits**	25
43	Vertical Image Size **Lower 8bits**	A5
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10
45	Horizontal Border *(zero for internal LCD)*	00
46	Vertical Border *(zero for internal LCD)*	00
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18
48	Detailed timing/monitor	00
49	descriptor #2	00
4A		00
4B		0F
4C		00
4D		00
4E		00
4F		00
50		00
51		00
52		00
53		00
54		00
55		00
56		00
57		00
58		00
59		20
5A	Detailed timing/monitor	00
5B	descriptor #3	00
5C		00

5D		FE
5E		00
5F	Manufacture	41
60	Manufacture	55
61	Manufacture	4F
62		0A
63		20
64		20
65		20
66		20
67		20
68		20
69		20
6A		20
6B		20
6C	Detailed timing/monitor	00
6D	descriptor #4	00
6E		00
6F		FE
70		00
71	Manufacture P/N	47
72	Manufacture P/N	31
73	Manufacture P/N	33
74	Manufacture P/N	33
75	Manufacture P/N	48
76	Manufacture P/N	41
77	Manufacture P/N	4E
78	Manufacture P/N	30
79	Manufacture P/N	32
7A	Manufacture P/N	2E
7B	Manufacture P/N	32
7C		20
7D		0A
7E	Extension Flag	00
7F	Checksum	D8