AU OPTRONICS CORPORATION

Product Specification

12.1” WXGA Color TFT-LCD Module

Model Name: B121EW03 V1

Approved by	Prepared by

NBBU Marketing Division / AU Optronics corporation

Customer	Checked & Approved by

Product Specification

12.1” WXGA Color TFT-LCD Module
Model Name: B121EW03
V.1

( ) Preliminary Specifications
(V) Final Specifications

Note: This Specification is subject to change without notice.

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2005/12/12	All	First Edition for Customer		
0.2 2005/12/15	6	Anti-Glare, Hardness 2H, Haze 25%, Reflectance 4.3%	Anti-Glare, Hardness 3H, Haze 25%	
0.2 2005/12/15	14		VDD power Max 1.6 watt	
0.3 2006/3/13	6	180 typ. (5 points average) 160 min. (5 points average)	200 typ. (5 points average) 170 min. (5 points average)	
0.3 2006/3/13	7	White Luminance CCFL 6.0mA (5 points average) 180 typ. / 160 min.	White Luminance CCFL 6.0mA ((5 points average) 200 typ. / 170 min.	
0.3 2006/3/13	7	Viewing angle Vertical CR = 10 (Upper) 10 (Lower) 30	Viewing angle Vertical CR = 10 (Upper) 20 (Lower) 40	
0.4 2006/4/12	6	Contrast ratio 400 typ	500 typ.	
0.4 2006/4/12	7		Update Color / Chromaticity Coordinates (CIE 1931)	
0.4 2006/4/12	7	CR: Contrast Ratio typ 400	CR: Contrast Ratio typ 500	
0.4 2006/4/12	31		Update Shipping Label Format	
0.4 2006/4/12	33		Update 12. Appendix: EDID description	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

2. General Description

B121EW03 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter card of backlight is not included.

B121EW03 V1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	307.9 (12.1W")
Active Area	[mm]	261.12(H) X 163.2(V)
Pixels H x V		1280x3(RGB) x 800
Pixel Pitch	[mm]	0.204X0.204
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance (ICFL=6.0mA)	[cd/m^2]	200 typ. (5 points average) 170 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		500 typ.
Optical Rise Time/Fall Time	[msec]	10/15 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Typical Power Consumption	[Watt]	4.5W max.
Weight (without inverter)	[Grams]	250g typ. 265g max
Physical Size	[mm]	275.82x 178 x 5.2 max.
Electrical Interface		1 channel LVDS
Surface Treatment		Anti-Glare, Hardness 3H, Haze 25%
Support Color		Native 262K colors (RGB 6-bit data driver)

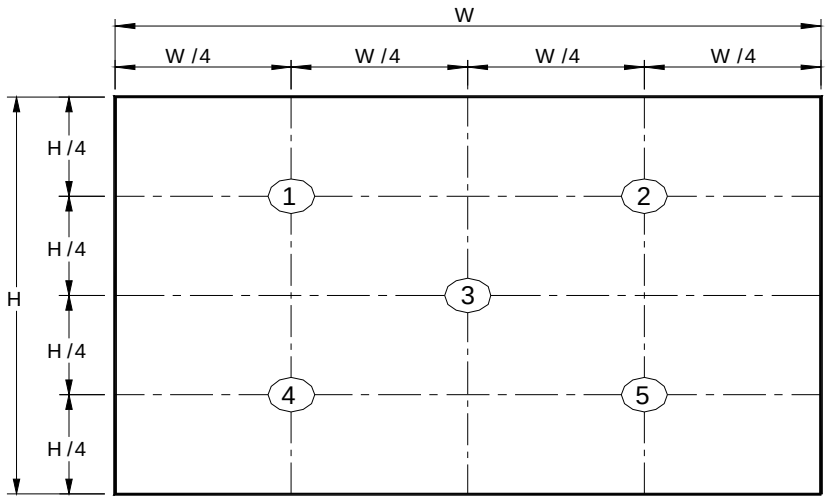
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -40 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

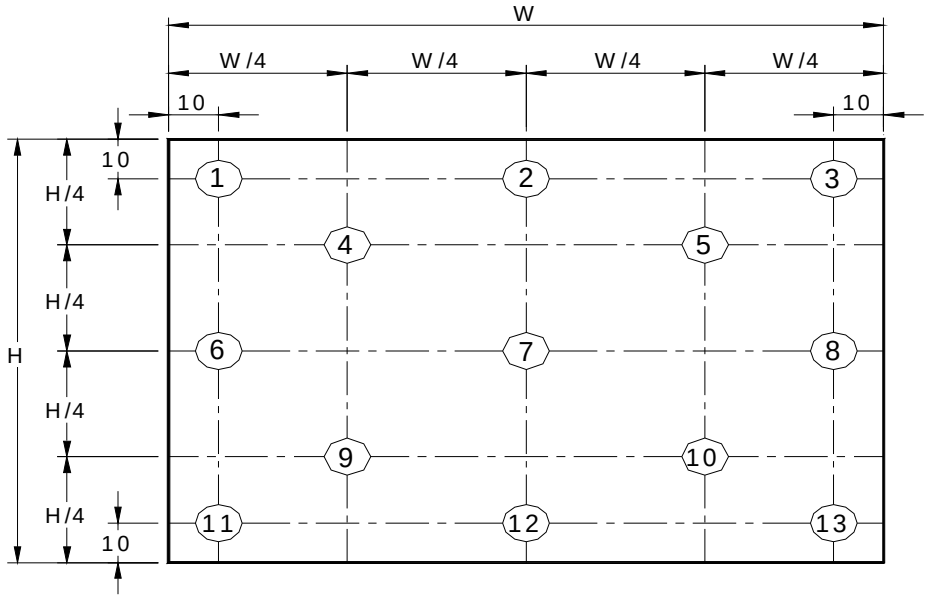
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance CCFL 6.0mA	[cd/m2]	5 points average	170	200	-	1,2,3
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	- -	40 40	- -	2,7
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	- -	20 40	- -	
Uniformity		5 Points			1.25	1
Uniformity		13 Points			1.6	
CR: Contrast Ratio			350	500	-	6
Cross talk	%				4	4
Response Time	[msec]	Rising	-	10	15	5
	[msec]	Falling	-	15	20	
	[msec]	Raising + Falling		25	35	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.560	0.580	0.600	2,7
		Red y	0.320	0.340	0.360	
		Green x	0.290	0.310	0.330	
		Green y	0.530	0.550	0.570	
		Blue x	0.135	0.155	0.175	
		Blue y	0.135	0.155	0.175	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	

Note 1: 5 points position (Display area : 261.12mm x 163.2mm)



Note 2: 13 points position



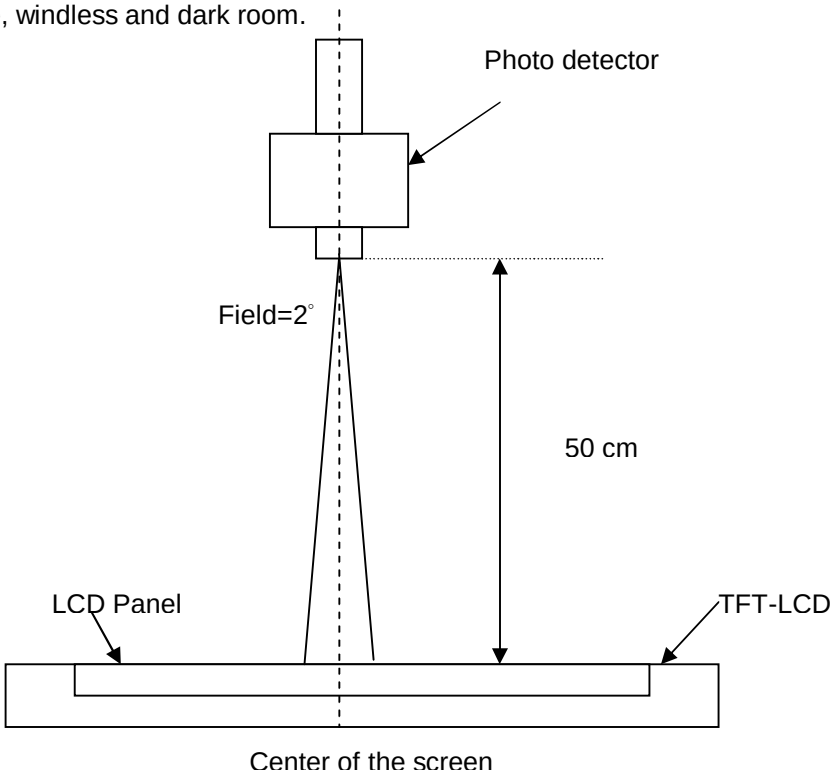
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



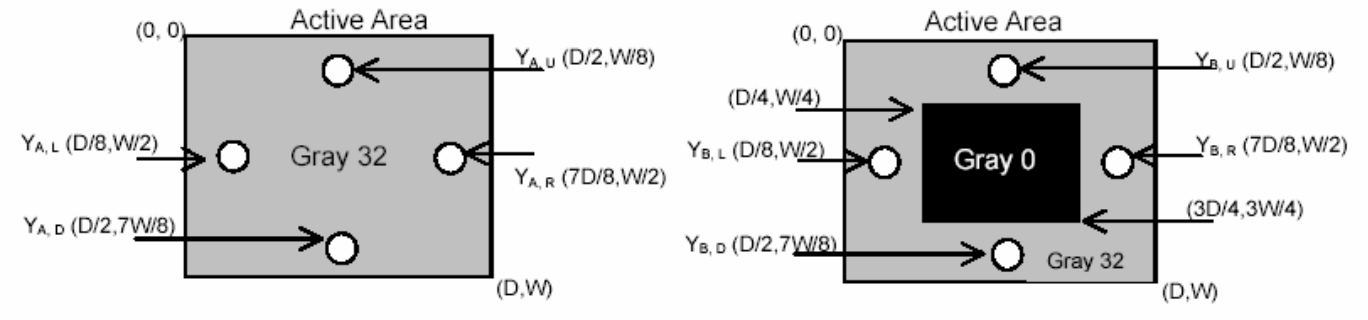
Note 5： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100\ (\%)$

Where

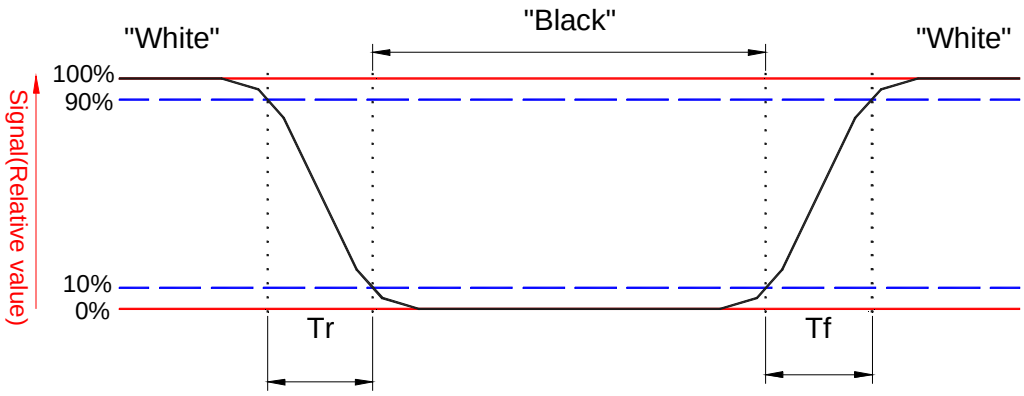
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



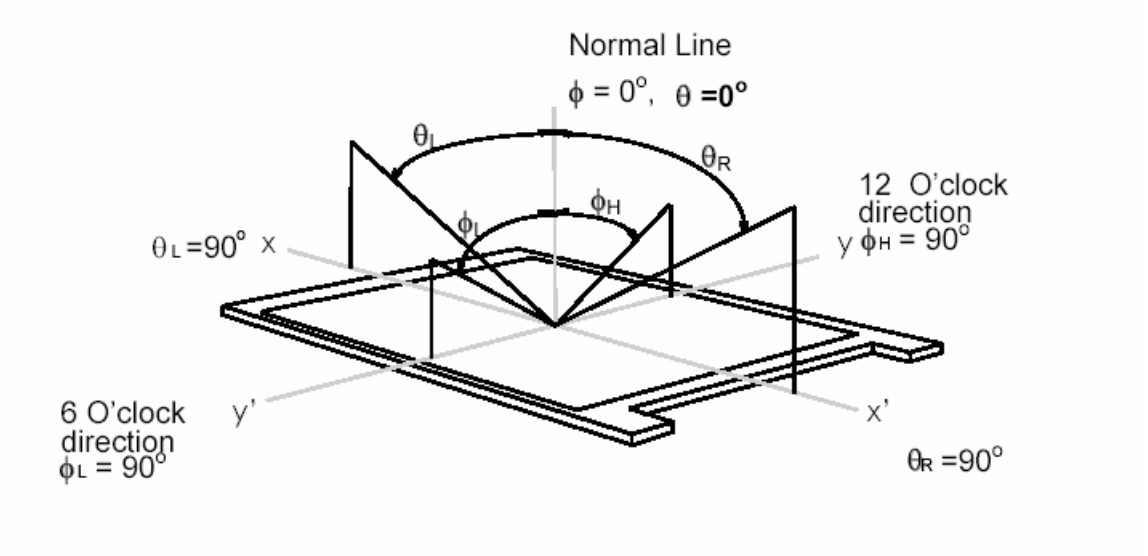
Note 6: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from“Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



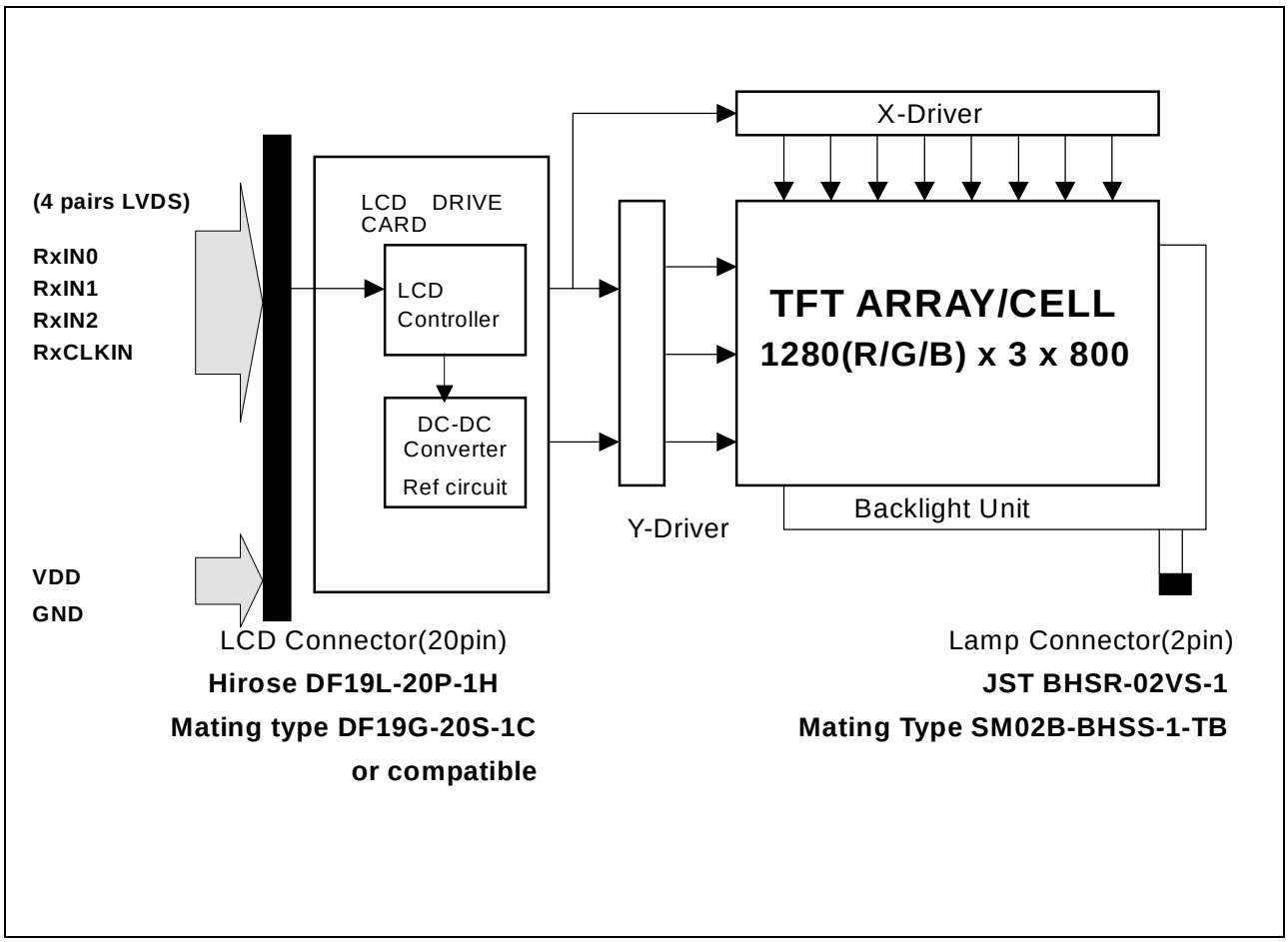
Note 7. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 12.1 inches wide Color TFT/LCD Module:



4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICFL	-	7	[mA] rms	Note 1,2

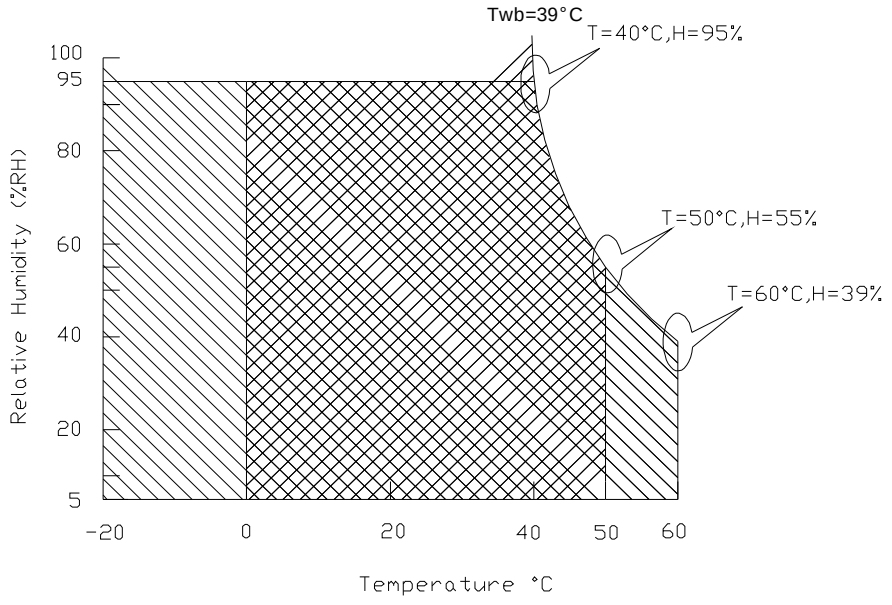
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-40	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: With in Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range Storage Range

5. Electrical characteristics

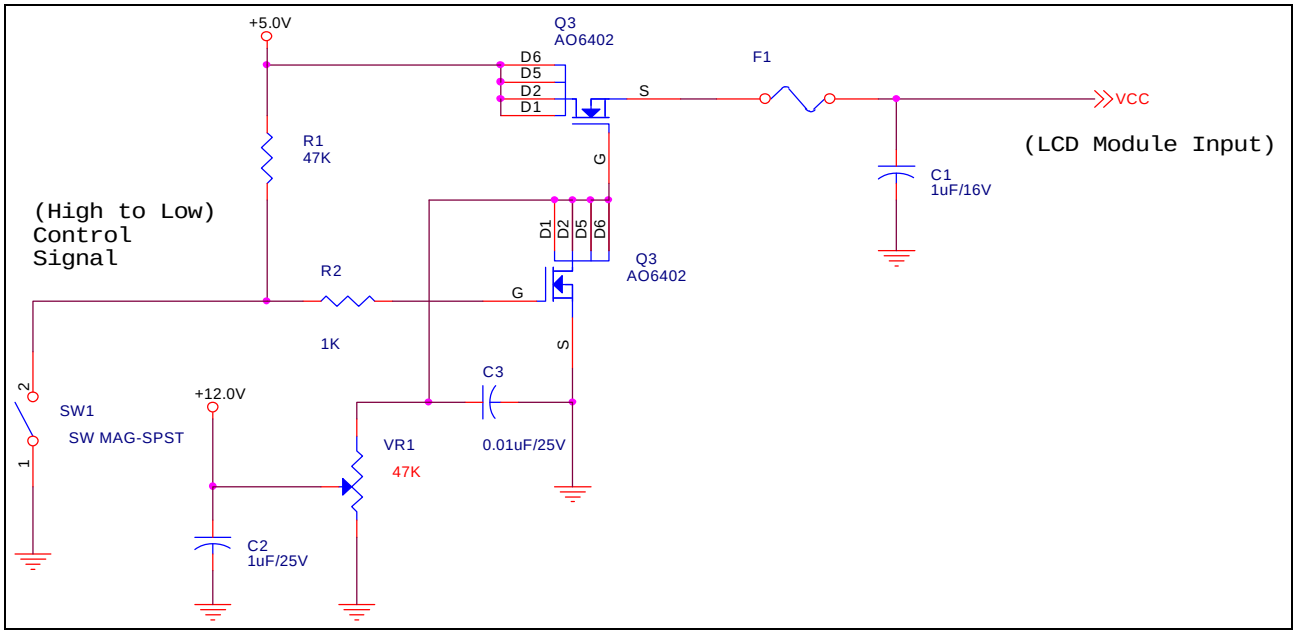
5.1 TFT LCD Module

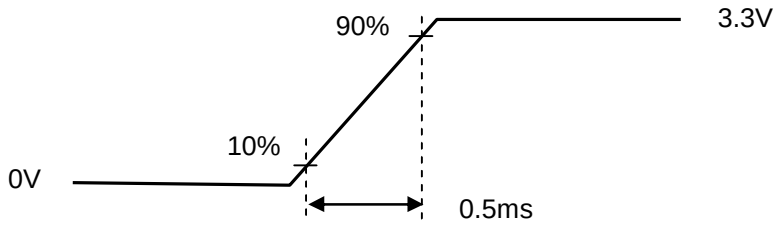
5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		1.0	1.6	[Watt]	Max:All Black Pattern
IDD	IDD Current		400	420	mA	Max:All Black Pattern
IRush	Inrush Current			1800	mA	
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			500	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mV] p-p	

Note 1 : Measurement conditions:





Vin rising time

5.1.2 Signal Electrical Characteristics

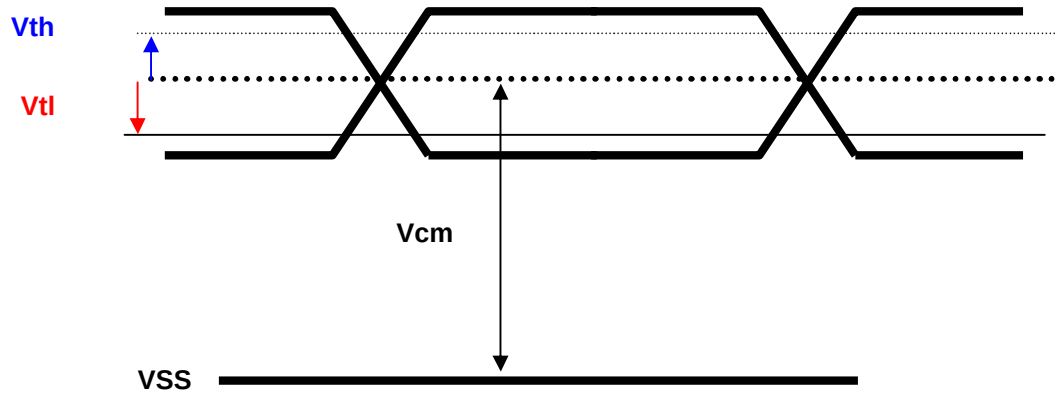
Input signals shall be low or Hi-Z state when VDD is off.

It is recommended to refer the specifications of SN75LVDS86DGG(Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]

Note: LVDS Signal Waveform



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	170	200	-	[cd/m^2]	(Ta=25℃)
CCFL current(ICFL)	5.5	6.0	6.5	[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(FCFL)	50	60	70	[KHz]	(Ta=25℃) Note 3,4
CCFL Ignition Voltage(Vs)	1400	-	-	[Volt] rms	(Ta= 0℃) Note 5
CCFL Voltage (Reference) (VCFL)	-	580	-	[Volt] rms	(Ta=25℃) Note 6
CCFL Power consumption (PCFL)	-	3.5	-	[Watt]	(Ta=25℃) Note 6

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.
*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.
*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.
*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has “Duty Dimming”, if ICFL is less than 4mA.

Note 3: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CFL inverter should be able to give out a power that has a generating capacity of over 1,430 voltage. Lamp units need 1,400 voltage minimum for ignition.

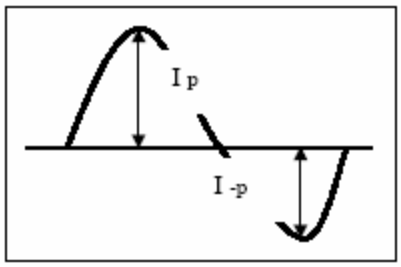
Note 6: Calculator value for reference (ICFL×VCFL=PCFL)

Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.
It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.

b. The distortion rate of the waveform should be within √2 ±10%.

* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

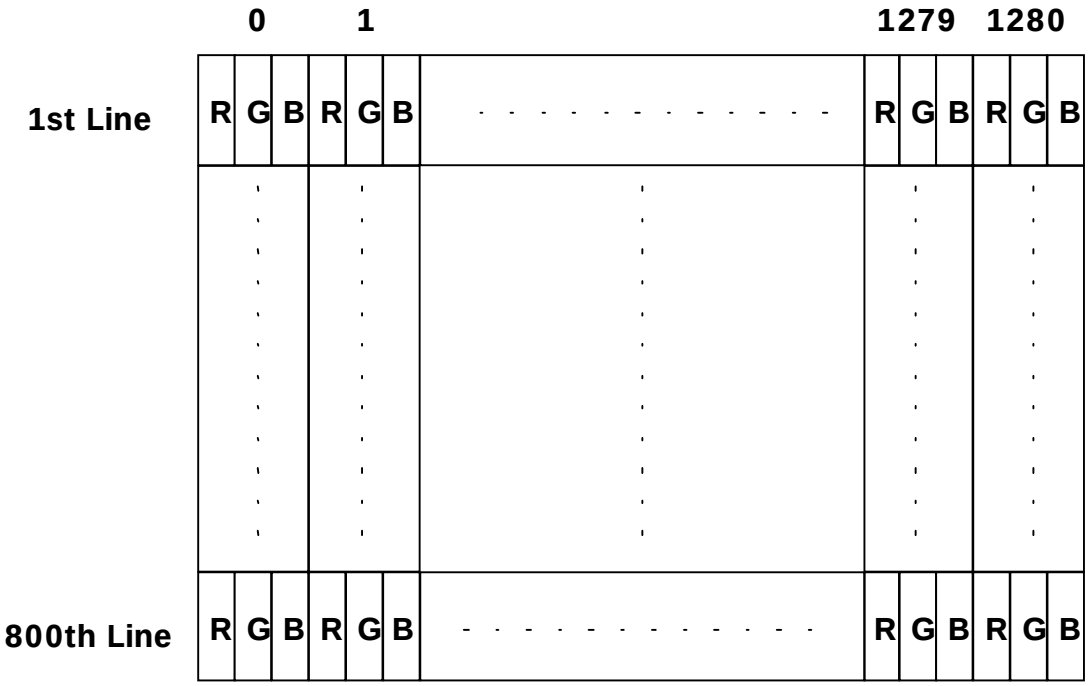
* Distortion rate

I_p (or I_{-p}) / I_{rms}

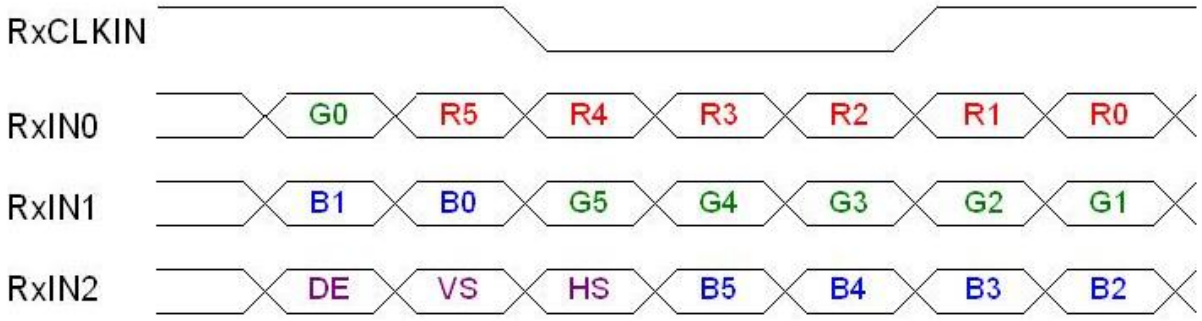
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description	
RED5 RED4 RED3 RED2 RED1 RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
GREEN 5 GREEN 4 GREEN 3 GREEN 2 GREEN 1 GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
BLUE 5 BLUE 4 BLUE 3 BLUE 2 BLUE 1 BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
DTCLK	Data Clock	The typical frequency is 68.9 MHZ.. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	Display Timing	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync	The signal is synchronized to -DTCLK .
HSYNC	Horizontal Sync	The signal is synchronized to -DTCLK .

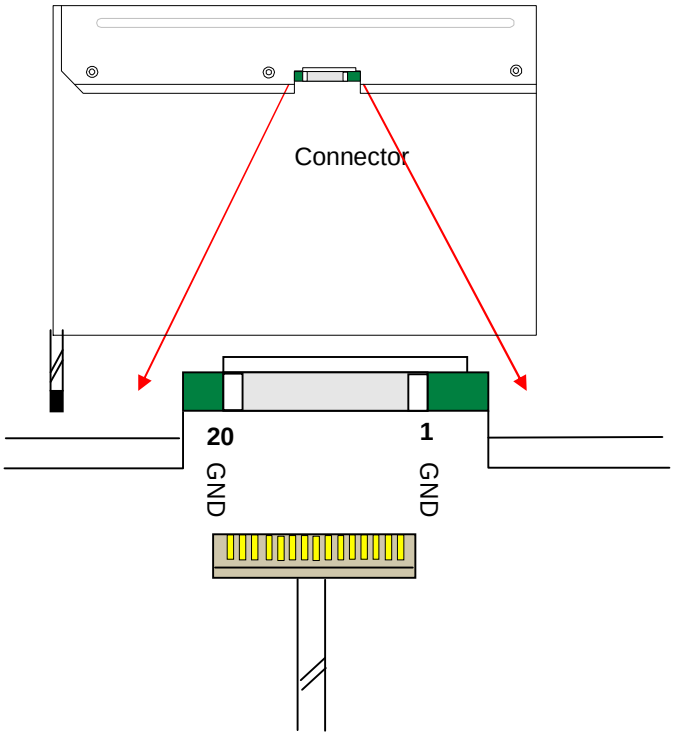
Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

6.3 Signal Description

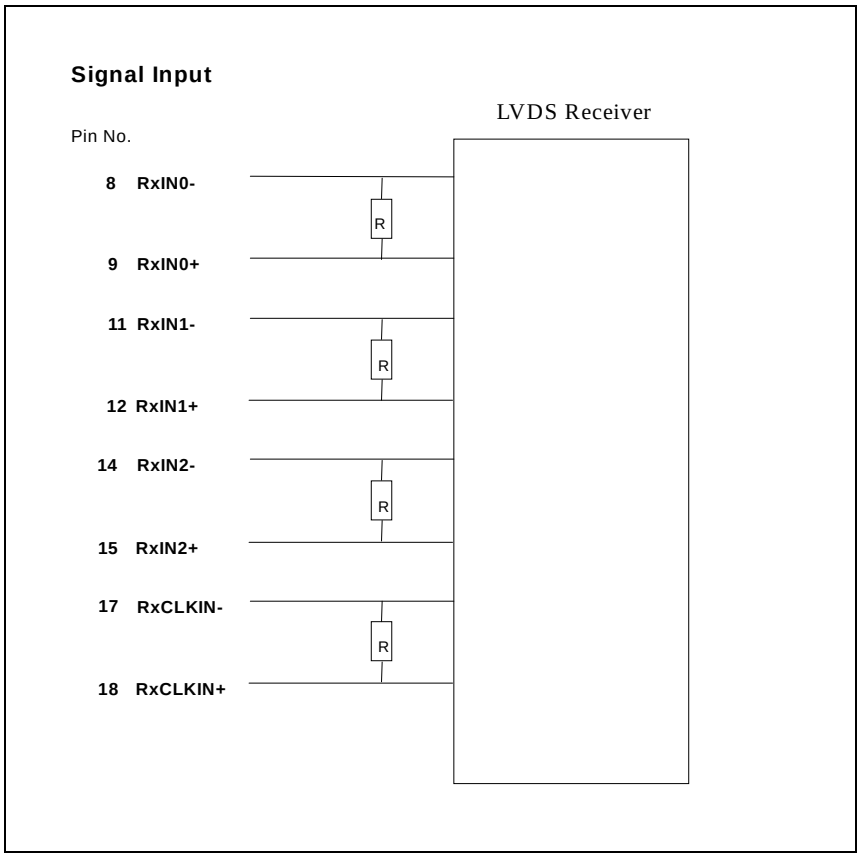
The LVDS receiver equipped in this LCD module is compatible with SN75LVDS86 standard. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.

Signal Name	Description
RxIN0N, RxIN0P	LVDS differential data input (Red0-Red5, Green0)
RxIN1N, RxIN1P	LVDS differential data input (Green1-Green5, Blue0-Blue1)
RxIN2N, RxIN2P	LVDS differential data input (Blue2-Blue5, Hsync, Vsync, DSPTMG)
RxCLKINN, RxCLKIN0P	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note1: Start from right side
Note2: Please follow VESA.
Note3: Input signals shall be low or Hi-Z state when VDD is off. Internal circuit of LVDS inputs are as following.



The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

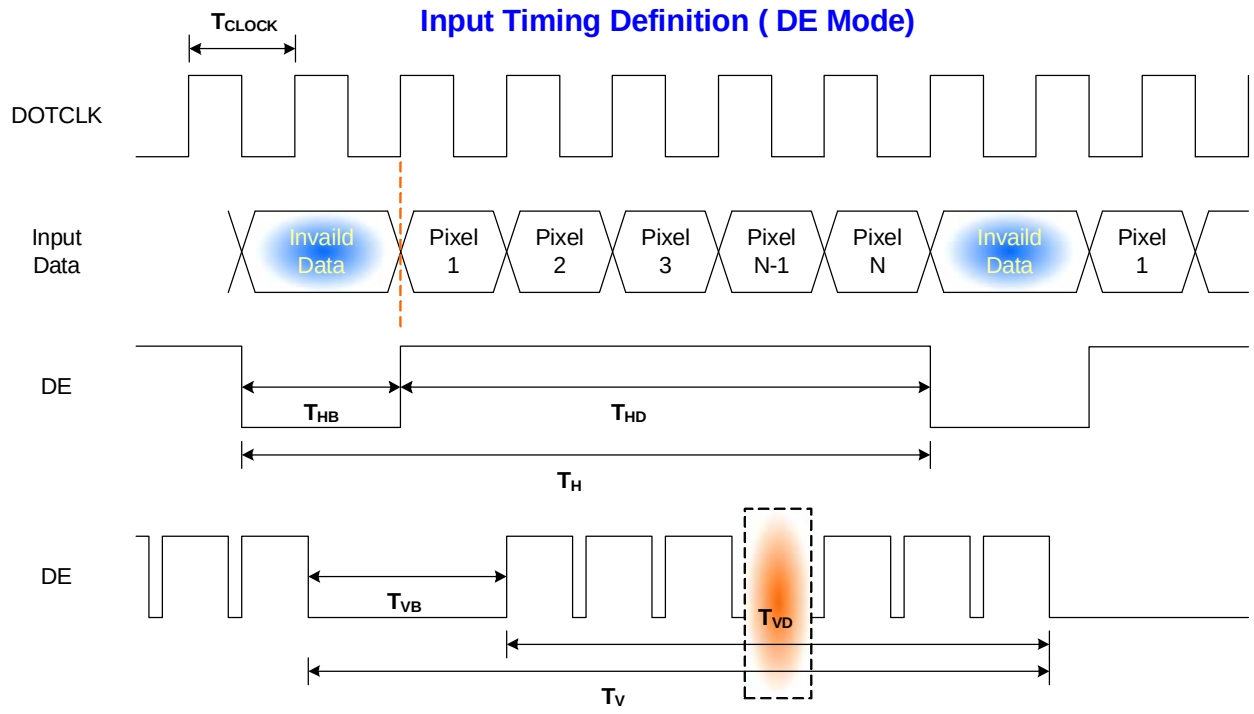
6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		1/ T_{Clock}	62	68.9	72	MHz
Vertical Section	Period	T_V	803	816	832	T_{Line}
	Active	T_{VD}	800	800	800	
	Blanking	T_{VB}	3	16	32	
Horizontal Section	Period	T_H	1302	1408	1700	T_{Clock}
	Active	T_{HD}	-	1280	-	
	Blanking	T_{HB}	22	128	420	
End-frame checking period		tEF	2			T_{Line}
DE checking period		tDE	6400			T_{Line}

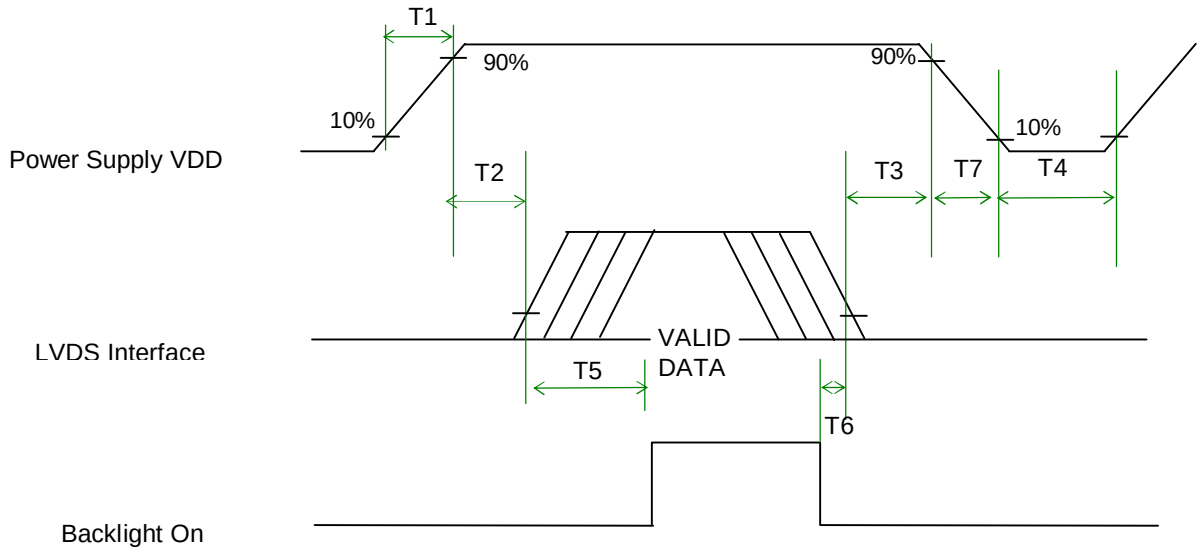
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	500	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

7. Connector & Pin Assignment

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

(A) CONNECTOR

Connector Name / Designation	For Signal Connector
Manufacturer	Hirose
Type / Part Number	DF19L-20P-1H
Mating Housing/Part Number	DF19G-20S-1C or compatible

(B) Signal Pin

Pin#	Signal Name	Pin#	Signal Name
1	GND	2	VDD
3	VDD	4	VDD_{EDID}
5	AGING	6	CLK_{EDID}
7	$DATA_{EDID}$	8	RxIN0N
9	RxIN0P	10	GND
11	RxIN1N	12	RxIN1P
13	GND	14	RxIN2N
15	RxIN2P	16	GND
17	RxCLKINN	18	RxCLKINP
19	GND	20	GND

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage

8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5G
- Frequency: 26 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 180 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	40℃/95%,250Hr	
High Temperature Operation	50℃/Dry,250Hr	
Low Temperature Operation	0℃,250Hr	
On/Off Test	ON/30 sec. OFF/30sec., 30,000 cycles.	
Hot Storage	65℃/20% RH ,250 hours	
Cold Storage	-40℃/50% RH ,250 hours	
Thermal Shock Test	-40℃/20 min ,65℃/20 min 300cycles	
Hot Start Test	50℃/1 Hr min. power on/off per 5 minutes, 5 times	
Cold Start Test	0℃/1 Hr min. power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	180G, 2ms, Half-sine wave	
Vibration Test (Non-Operating)	Random vibration, 1.5 G zero-to-peak, 26 to 500 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact : ±8KV/ operation Air : ±15KV / operation	Note 1
Room temperature Test	25℃, 2000hours, Operating with loop pattern	

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

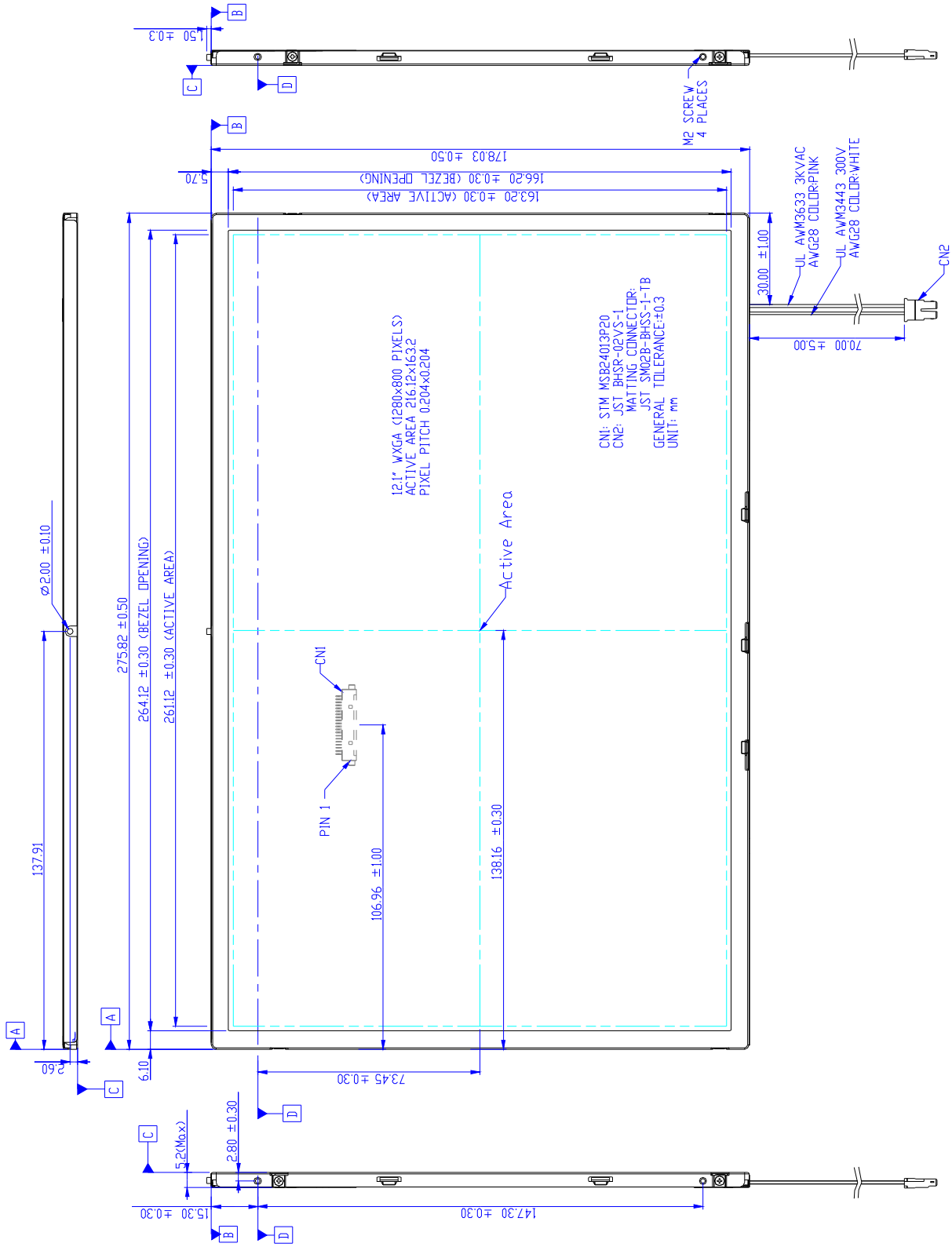
. Self-recoverable. No hardware failures.

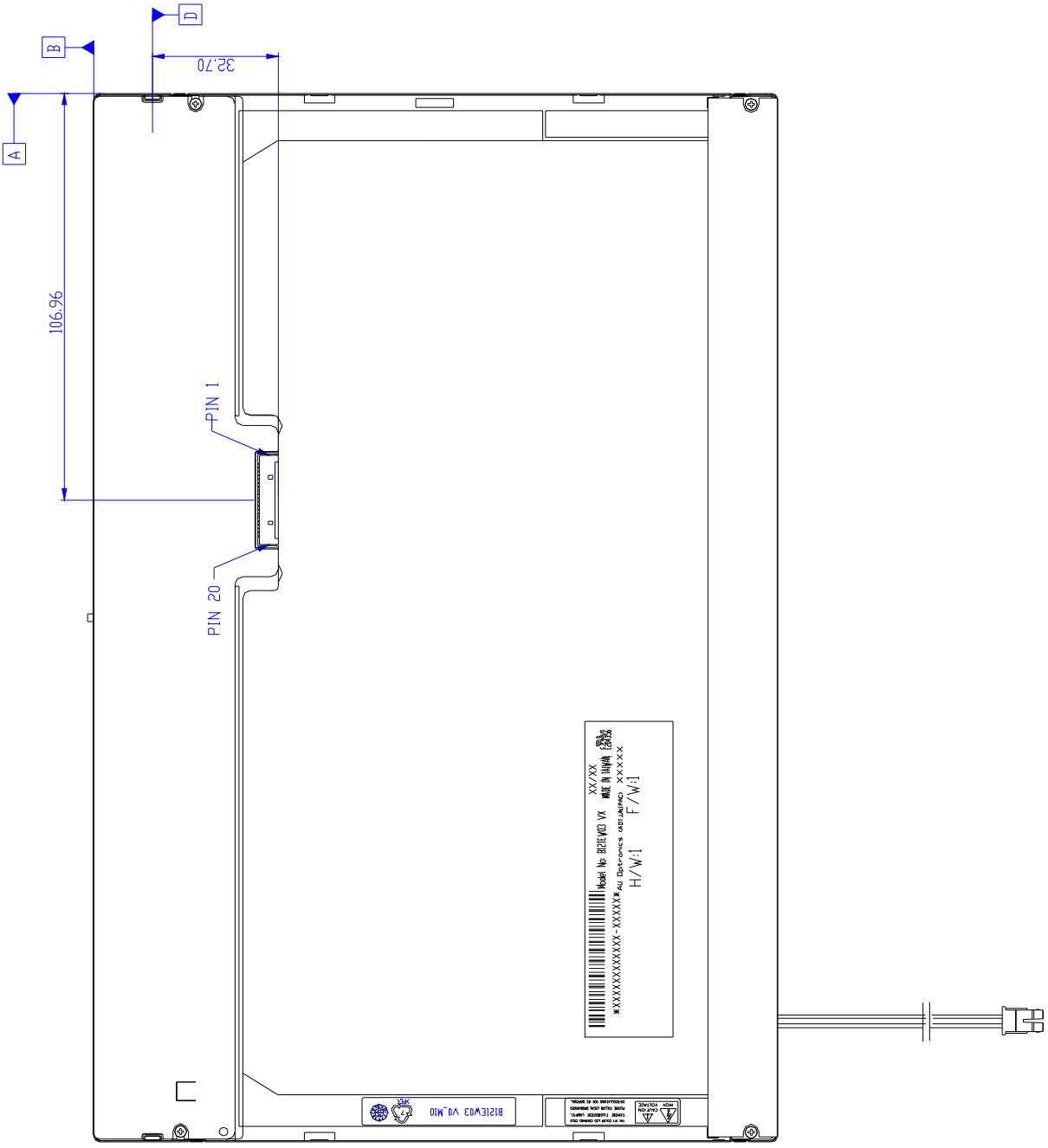
Note2: CCFL Life time: 10,000 hours minimum under normal module usage.

Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

10. Mechanical Characteristics

10.1 LCM Outline Dimension

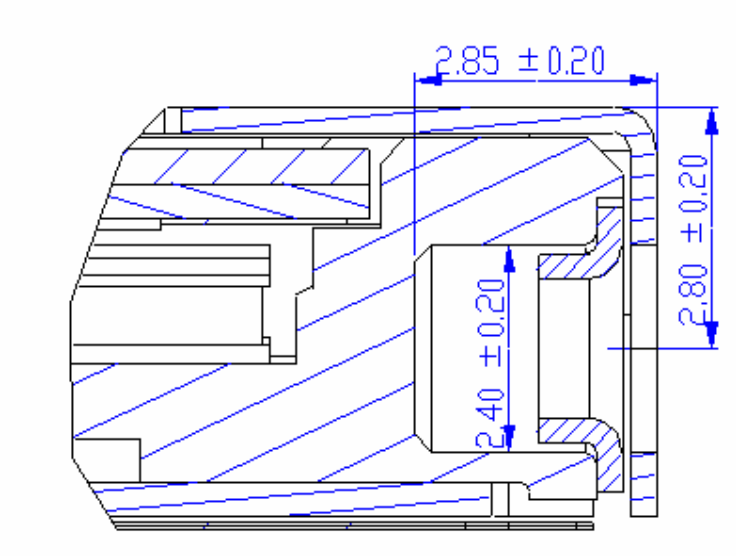



D
B
A
32.70
106.96
PIN 1
PIN 20
B121EW03 V0_M10
H/W:1
F/W:1

10.2 Screw Hole Depth and Center Position

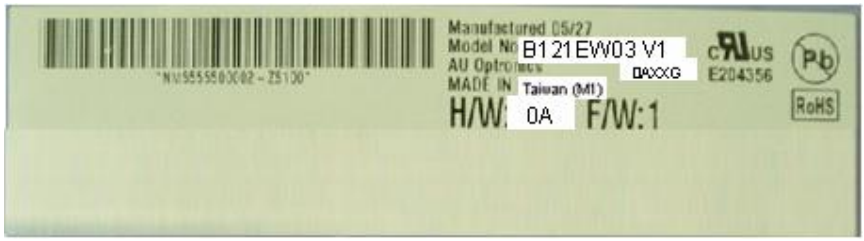
Screw hole minimum depth, from side surface =2.85 mm (See drawing)

Screw hole center location, from front surface = 328 ± 0.2mm (See drawing)
Screw Torque: Maximum 2.2 kgf-cm



11. Shipping and Package

11.1 Shipping Label Format

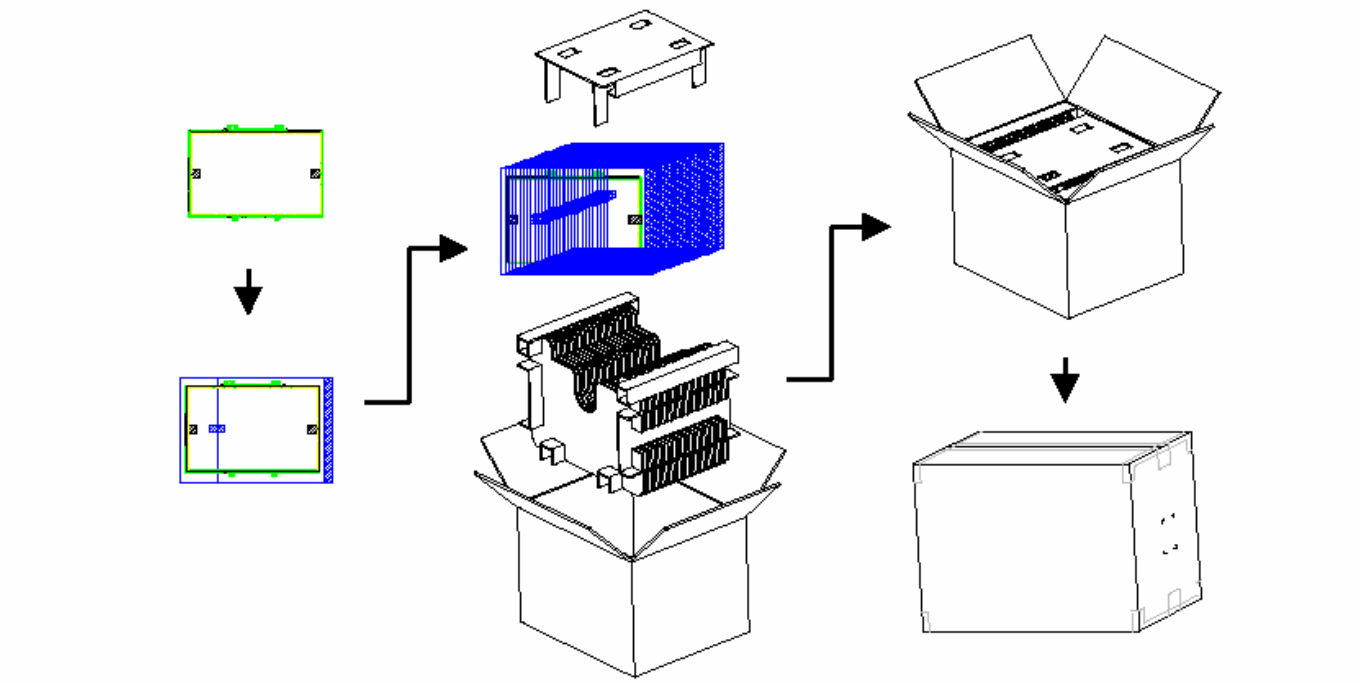


Note 1:

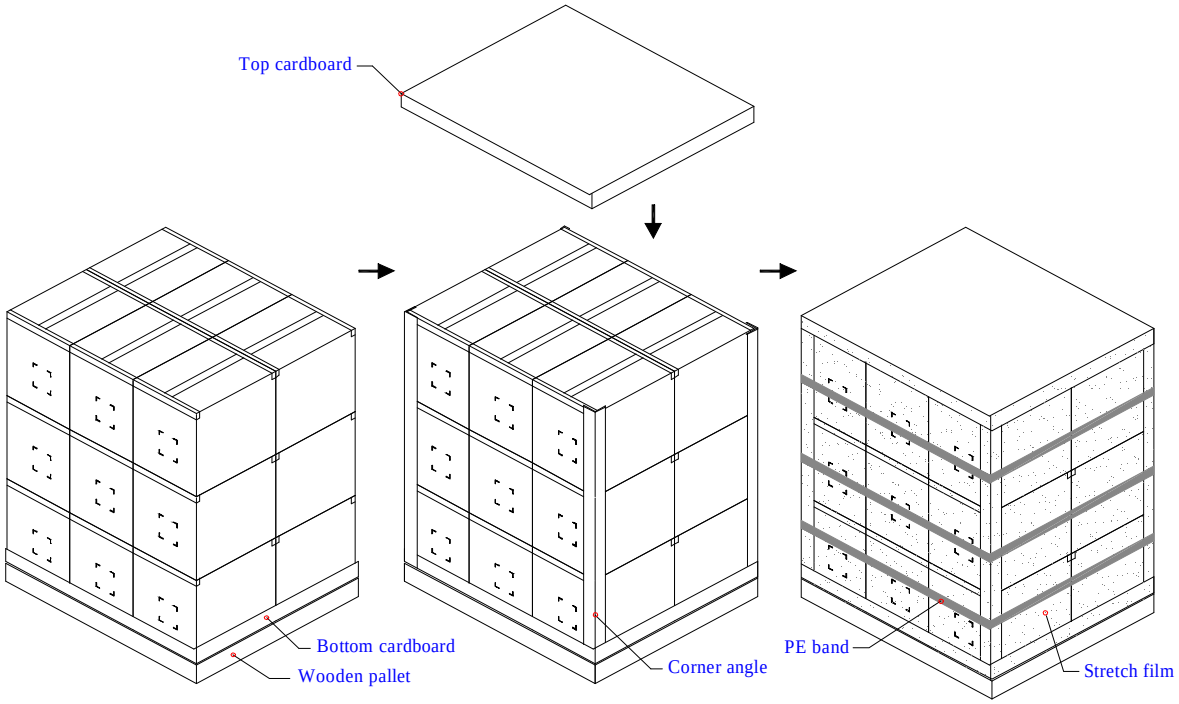
IC Combination	Control Code	H/W
Source IC:Novaek Gate IC: Novatek	0AXXX	0A

11.2. Carton package

The outside dimension of carton is 486 (L)mm x 286 (W)mm x 360 (H)mm



11.3 Shipping package of palletizing sequence



Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)

12. Appendix: EDID description

Address	FUNCTION	Value	Value
HEX		HEX	BIN
00	Header	00	00000000
01		FF	11111111
02		FF	11111111
03		FF	11111111
04		FF	11111111
05		FF	11111111
06		FF	11111111
07		00	00000000
08	EISA Manuf. Code LSB	06	00000110
09	Compressed ASCII	AF	10101111
0A	Product Code	14	00010100
0B	hex, LSB first	31	00110001
0C	32-bit ser #	00	00000000
0D		00	00000000
0E		00	00000000
0F		00	00000000
10	Week of manufacture	01	00000001
11	Year of manufacture	10	00010000
12	EDID Structure Ver.	01	00000001
13	EDID revision #	03	00000011
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	80	10000000
15	**Max H image size** *(rounded to cm)*	1A	00011010
16	**Max V image size** *(rounded to cm)*	10	00010000
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	0A	00001010
19	Red/green low bits **(Lower 2:2:2:2 bits)**	87	10000111
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	FE	11111110
1B	Red x **(Upper 8 bits)**	94	10010100
1C	Red y/ highER 8 bits	57	01010111
1D	Green x	4F	01001111
1E	Green y	8C	10001100
1F	Blue x	27	00100111
20	Blue y	27	00100111
21	White x	50	01010000
22	White y	54	01010100
23	Established timing 1	00	00000000
24	Established timing 2	00	00000000
25	Established timing 3	00	00000000
26	Standard timing #1	01	00000001
27		01	00000001
28	Standard timing #2	01	00000001
29		01	00000001
2A	Standard timing #3	01	00000001
2B		01	00000001

2C	Standard timing #4	01	00000001
2D		01	00000001
2E	Standard timing #5	01	00000001
2F		01	00000001
30	Standard timing #6	01	00000001
31		01	00000001
32	Standard timing #7	01	00000001
33		01	00000001
34	Standard timing #8	01	00000001
35		01	00000001
36	Pixel Clock/10000 LSB	EA	11101010
37	Pixel Clock/10000 USB	1A	00011010
38	Horz active **Lower 8bits**	00	00000000
39	Horz blanking **Lower 8bits**	80	10000000
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	50	01010000
3B	Vertical Active **Lower 8bits**	20	00100000
3C	Vertical Blanking **Lower 8bits**	10	00010000
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30	00110000
3E	HorzSync. Offset	15	00010101
3F	HorzSync.Width	20	00100000
40	VertSync.Offset : VertSync.Width	44	01000100
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000
42	Horizontal Image Size **Lower 8bits**	05	00000101
43	Vertical Image Size **Lower 8bits**	A3	10100011
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000
45	Horizontal Border *(zero for internal LCD)*	00	00000000
46	Vertical Border *(zero for internal LCD)*	00	00000000
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000
48	Detailed timing/monitor	00	00000000
49	descriptor #2	00	00000000
4A		00	00000000
4B		0F	00001111
4C		00	00000000
4D		00	00000000
4E		00	00000000
4F		00	00000000
50		00	00000000
51		00	00000000
52		00	00000000
53		00	00000000
54		00	00000000
55		00	00000000
56		00	00000000
57		00	00000000
58		00	00000000
59		20	00100000
5A	Detailed timing/monitor	00	00000000
5B	descriptor #3	00	00000000
5C		00	00000000

5D		FE	11111110
5E		00	00000000
5F	Manufacture	41	01000001
60	Manufacture	55	01010101
61	Manufacture	4F	01001111
62		0A	00001010
63		20	00100000
64		20	00100000
65		20	00100000
66		20	00100000
67		20	00100000
68		20	00100000
69		20	00100000
6A		20	00100000
6B		20	00100000
6C	Detailed timing/monitor	00	00000000
6D	descriptor #4	00	00000000
6E		00	00000000
6F		FE	11111110
70		00	00000000
71	Manufacture P/N	42	01000010
72	Manufacture P/N	31	00110001
73	Manufacture P/N	32	00110010
74	Manufacture P/N	31	00110001
75	Manufacture P/N	45	01000101
76	Manufacture P/N	57	01010111
77	Manufacture P/N	30	00110000
78	Manufacture P/N	33	00110011
79	Manufacture P/N	20	00100000
7A	Manufacture P/N	56	01010110
7B	Manufacture P/N	31	00110001
7C		20	00100000
7D		0A	00001010
7E	Extension Flag	00	00000000
7F	Checksum	21	00100001