



Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications

() Final Specifications

Module	15.4" WXGA Color TFT-LCD
Model Name	B154EW08 V1(HW 0A / 1A / 4A)

Customer

Date

Checked &
Approved by

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2007/03/28

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2007/03/28

Note: This Specification is subject to change without notice.

NBBU Marketing Division /
AU Optronics corporation



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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2007/01/04	All	First Edition for Customer		
0.2 2007/03/19	33	Old EDID (checksum 45)	New EDID (checksum 43)	
0.3 2007/03/22	1	B154EW08 V1(HW 0A) B154EW08 V1(HW 1A) B154EW08 V1(HW 4A)	B154EW08 V1(HW 0A & 1A & 4A)	
0.4 2007/03/28	19	6.3 Signal Description/Pin Assignment PIN 25 NC / No Connection (Reserve for AUO test)	6.3 Signal Description/Pin Assignment PIN 25 GND / Ground	
0.4 2007/03/28	22	6.4.1 Timing Characteristics Clock frequency typ.: 68.9 MHz Vertical section Period: 816 Vertical section Blanking: 16 Horizontal section Period: 1408	6.4.1 Timing Characteristics Clock frequency typ.: 71.1 MHz Vertical section Period: 823 Vertical section Blanking: 23 Horizontal section Period: 1440	



1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
- 14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

2. General Description

B154EW08 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA



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(1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter of backlight is not included.

B154EW08 V1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	391 (15.4W")
Active Area	[mm]	331.2 X 207.0
Pixels H x V		1280x3(RGB) x 800
Pixel Pitch	[mm]	0.2588X0.2588
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (I _{CCFL} =6.0mA) Note: I _{CCFL} is lamp current	[cd/m ²]	200 typ. (5 points average) 170 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		400 typ 300 min.
Optical Rise Time/Fall Time	[msec]	6/2 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption	[Watt]	6.0 max.(without inverter)
Weight	[Grams]	525 typ. 550 max.
Physical Size	[mm]	344.0 typ. x 222.0 typ. x 6.1 max.
Electrical Interface		1 channel LVDS
Surface Treatment		Glare, Hardness 3H, Reflectance 4.3%
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60



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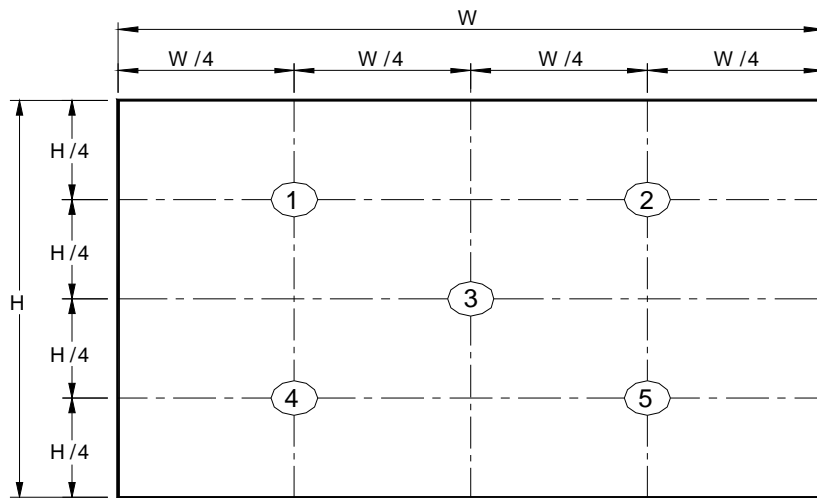
RoHS Compliance		RoHS Compliance
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2.2 Optical Characteristics

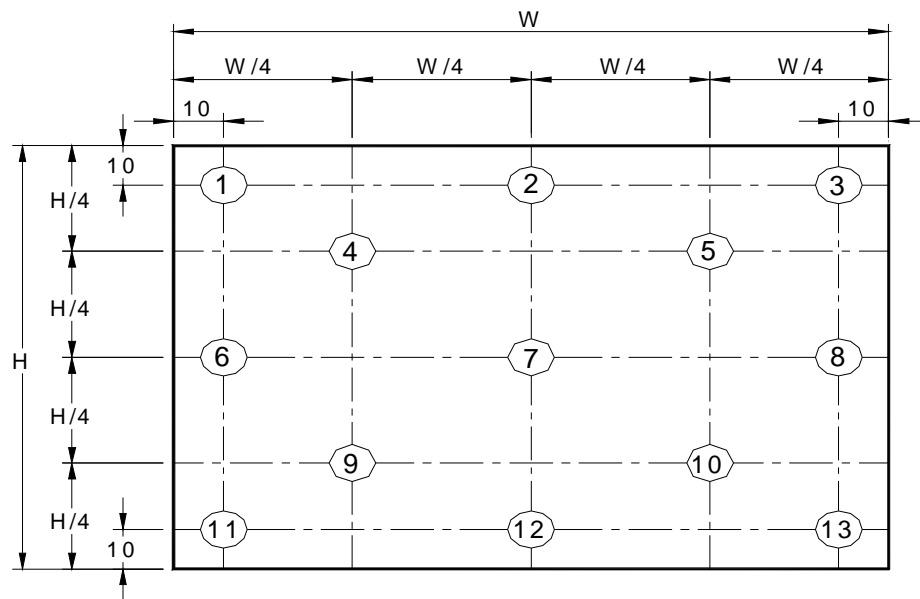
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance I _{CCFL} =6.0mA	[cd/m ²]	5 points average	170	200	-	1, 4, 5.
Viewing Angle	[degree]	Horizontal (Right)	-	45	-	8
	[degree]	CR = 10 (Left)	-	45	-	
	[degree]	Vertical (Upper)	-	15	-	
	[degree]	CR = 10 (Lower)	-	35	-	
Luminance Uniformity		5 Points			1.25	1
Luminance Uniformity		13 Points			1.50	2
CR: Contrast Ratio			300	400	-	6
Cross talk	%				4	7
Response Time	[msec]	Rising	-	6	10	8
	[msec]	Falling	-	2	5	
	[msec]	Rising + Falling		8	15	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.560	0.590	0.620	2,8
		Red y	0.315	0.345	0.375	
		Green x	0.285	0.315	0.345	
		Green y	0.520	0.555	0.585	
		Blue x	0.125	0.155	0.185	
		Blue y	0.125	0.155	0.185	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	

Note 1: 5 points position (Display area : 331.2mm x 207.0mm)



Note 2: 13 points position



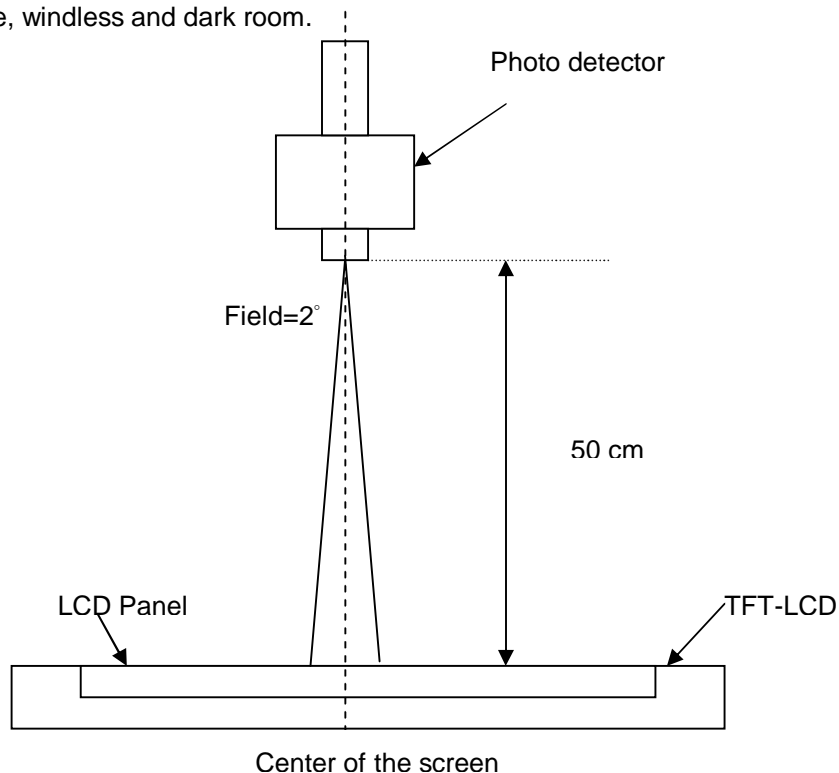
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

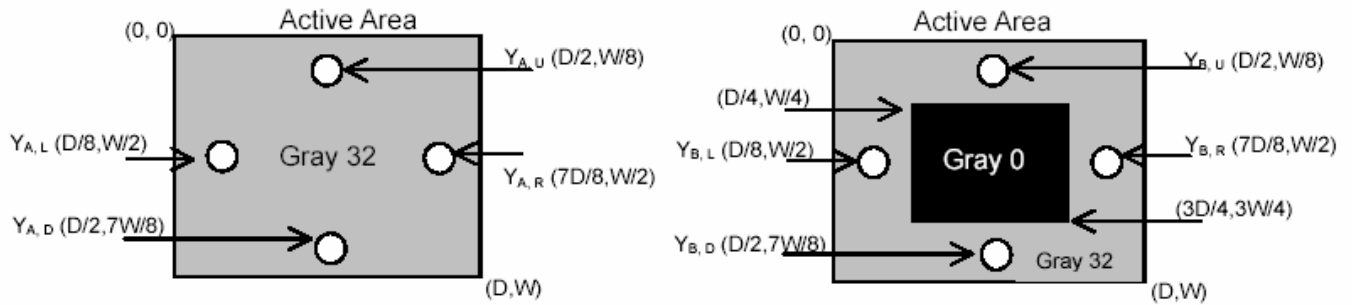
Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

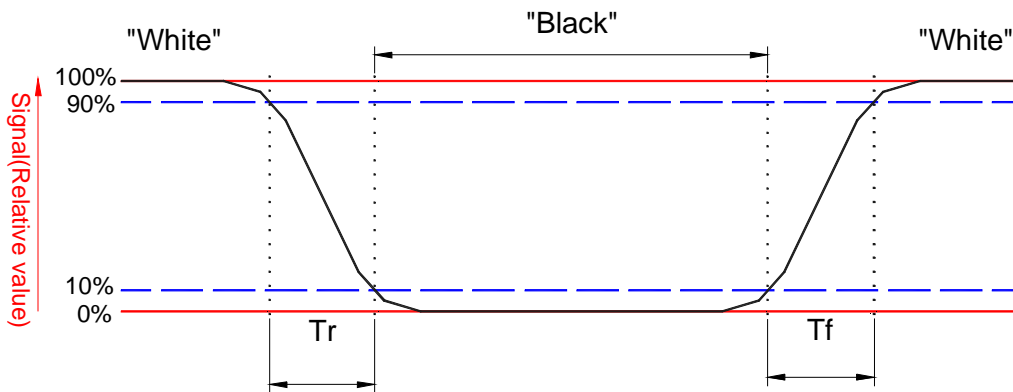
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



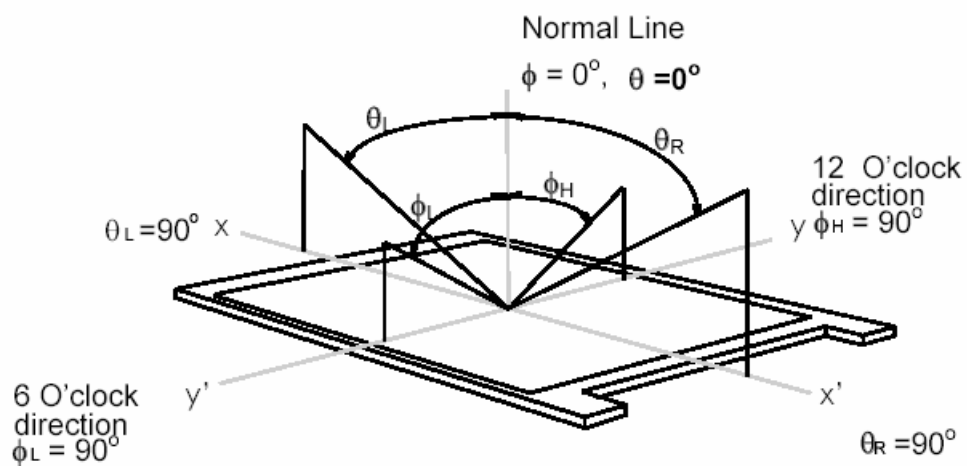
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



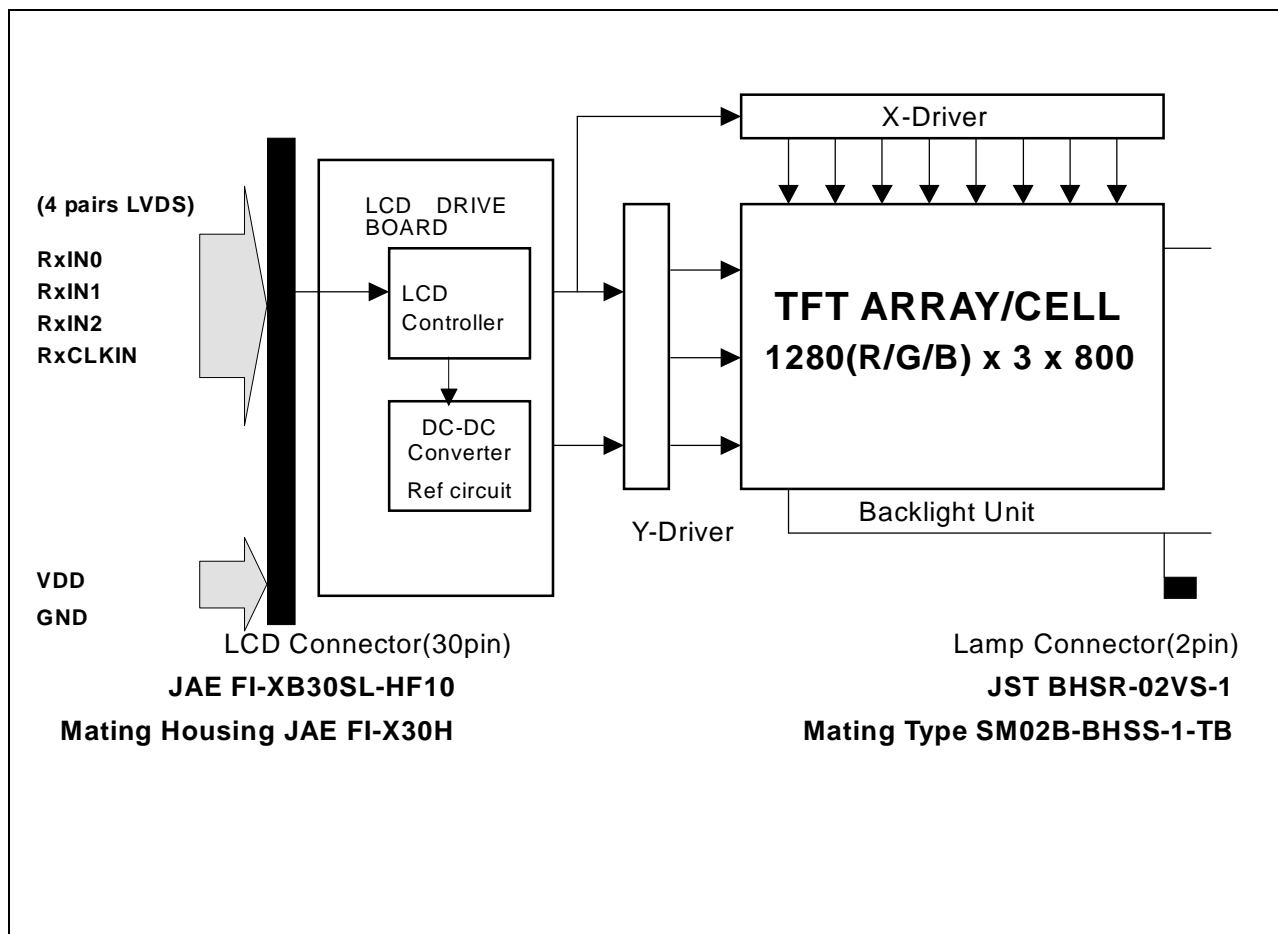
Note 8. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.4 inches wide Color TFT/LCD Module:





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4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	-	7.0	[mA] rms	Note 1,2

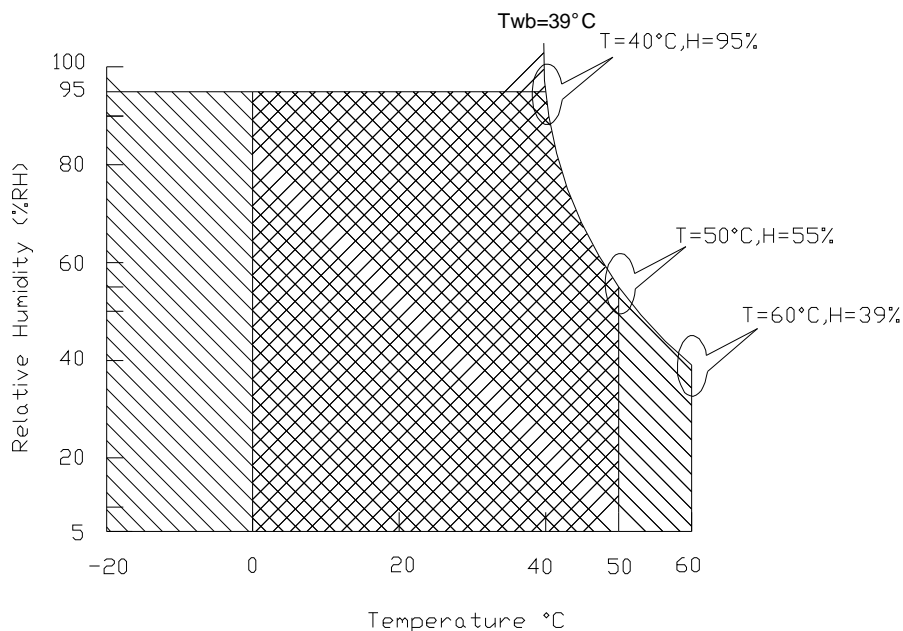
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

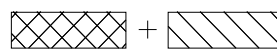
Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range



Storage Range





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5. Electrical characteristics

5.1 TFT LCD Module

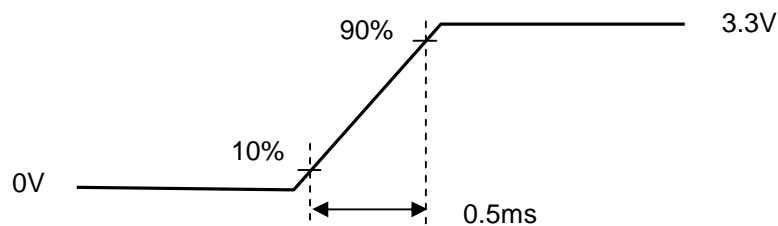
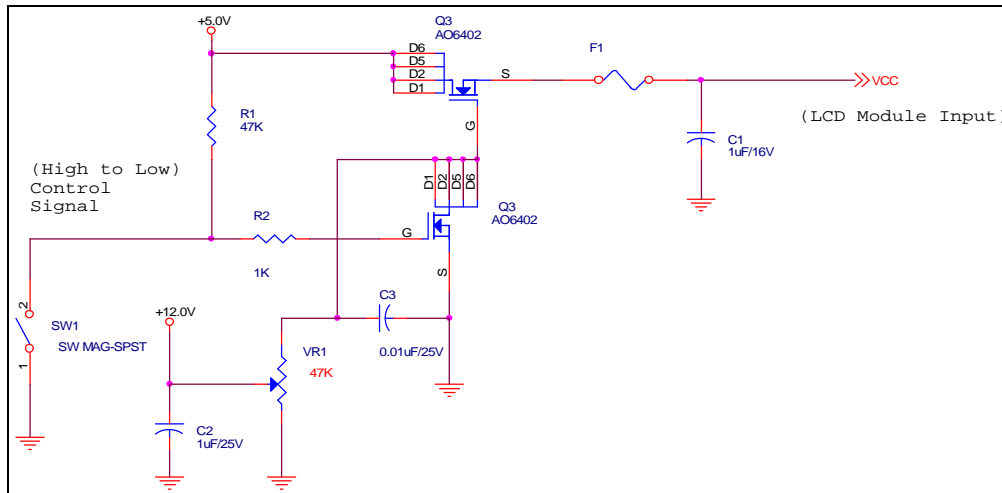
5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power			1.6	[Watt]	Note 1
IDD	IDD Current		350	450	[mA]	Note 1
IRush	Inrush Current			2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Measure Condition



Vin rising time



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5.1.2 Signal Electrical Characteristics

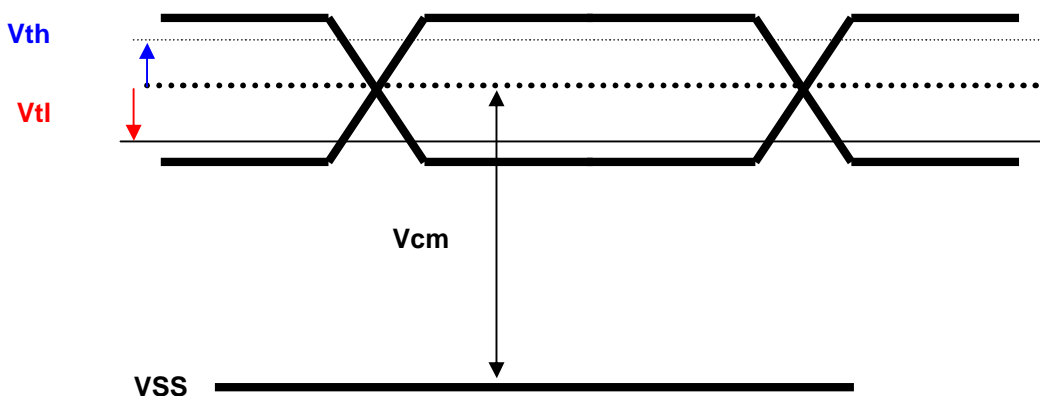
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A(Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform





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5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	170	200	-	[cd/m ²]	(Ta=25°C)
CCFL current(I _{CCFL})	2.0	6.0	7.0	[mA] rms	(Ta=25°C) Note 2
CCFL Frequency(F _{CCFL})	50	62	70	[KHz]	(Ta=25°C) Note 3,4
CCFL Ignition Voltage(Vs)			1750	[Volt] rms	(Ta= 0°C) Note 5
CCFL Ignition Voltage(Vs)			1460	[Volt] rms	(Ta= 25°C) Note 5
CCFL discharge time(sec)	1				(Ta= 25°C) Note 1
CCFL Voltage (Reference) (V _{CCFL})	628	700	792	[Volt] rms	(Ta=25°C) Note 6
CCFL Power consumption (P _{CCFL})	-	4.20	4.40	[Watt]	(Ta=25°C) Note 6

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully.

Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has "Duty Dimming", if ICCFL is less than 4mA.



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Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,430 voltage.

Lamp units need 1,400 voltage minimum for ignition.

Note 6: Calculator value for reference ($I_{CCFL} \times V_{CCFL} = P_{CCFL}$)

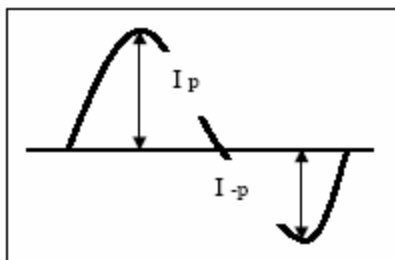
Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.

b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$.

* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$$|I_p - I_{-p}| / I_{rms} * 100\%$$

* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{rms}$$

6. Signal Characteristic

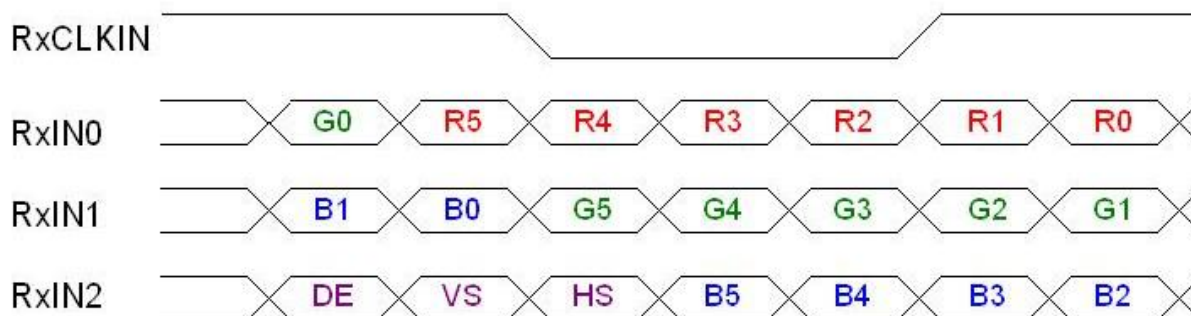
6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

	0						1						1278						1279					
1st Line	R	G	B	R	G	B	- - - - -						R	G	B	R	G	B						
								
								
								
								
								
								
								
								
								
800th Line	R	G	B	R	G	B	- - - - -						R	G	B	R	G	B						



6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The typical frequency is 68.9 MHZ.. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.



6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

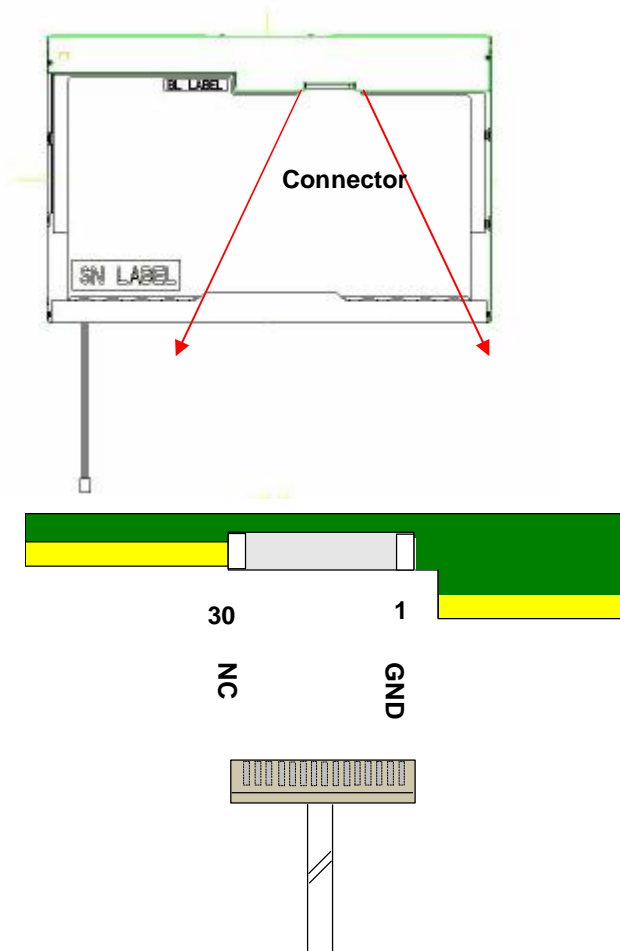
PIN#	Signal Name	Description
1	GND	Ground
2	VDD	+3.3V Power Supply
3	VDD	+3.3V Power Supply
4	V _{EDID}	+3.3V EDID Power
5	NC	No Connection (Reserve for AUO test)
6	CLK _{EDID}	EDID Clock Input
7	DATA _{EDID}	EDID Data Input
8	RxIN0-	LVDS differential data input(R0-R5, G0)
9	RxIN0+	LVDS differential data input(R0-R5, G0)
10	GND	Ground
11	RxIN1-	LVDS differential data input(G1-G5, B0-B1)
12	RxIN1+	LVDS differential data input(G1-G5, B0-B1)
13	GND	Ground
14	RxIN2-	LVDS differential data input(B2-B5, HS, VS, DE)
15	RxIN2+	LVDS differential data input(B2-B5, HS, VS, DE)
16	GND	Ground
17	RxCLKIN-	LVDS differential clock input
18	RxCLKIN+	LVDS differential clock input
19	GND	Ground
20	NC	No Connection (Reserve for AUO test)
21	NC	No Connection (Reserve for AUO test)
22	GND	Ground
23	NC	No Connection (Reserve for AUO test)
24	NC	No Connection (Reserve for AUO test)
25	GND	Ground
26	NC	No Connection (Reserve for AUO test)
27	NC	No Connection (Reserve for AUO test)
28	GND	Ground
29	NC	No Connection (Reserve for AUO test)
30	NC	No Connection (Reserve for AUO test)



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Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.

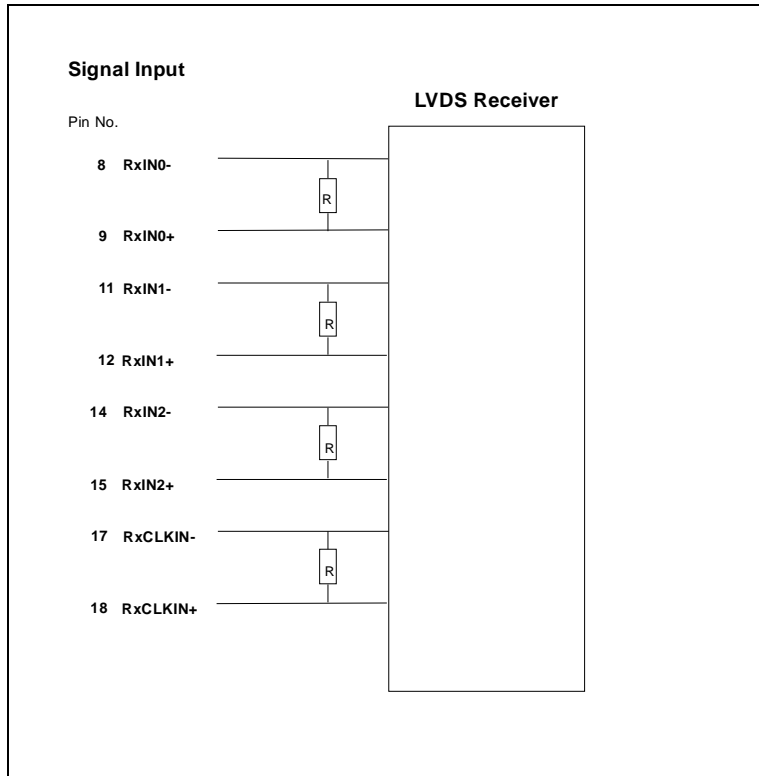


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internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input





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6.4 Interface Timing

6.4.1 Timing Characteristics

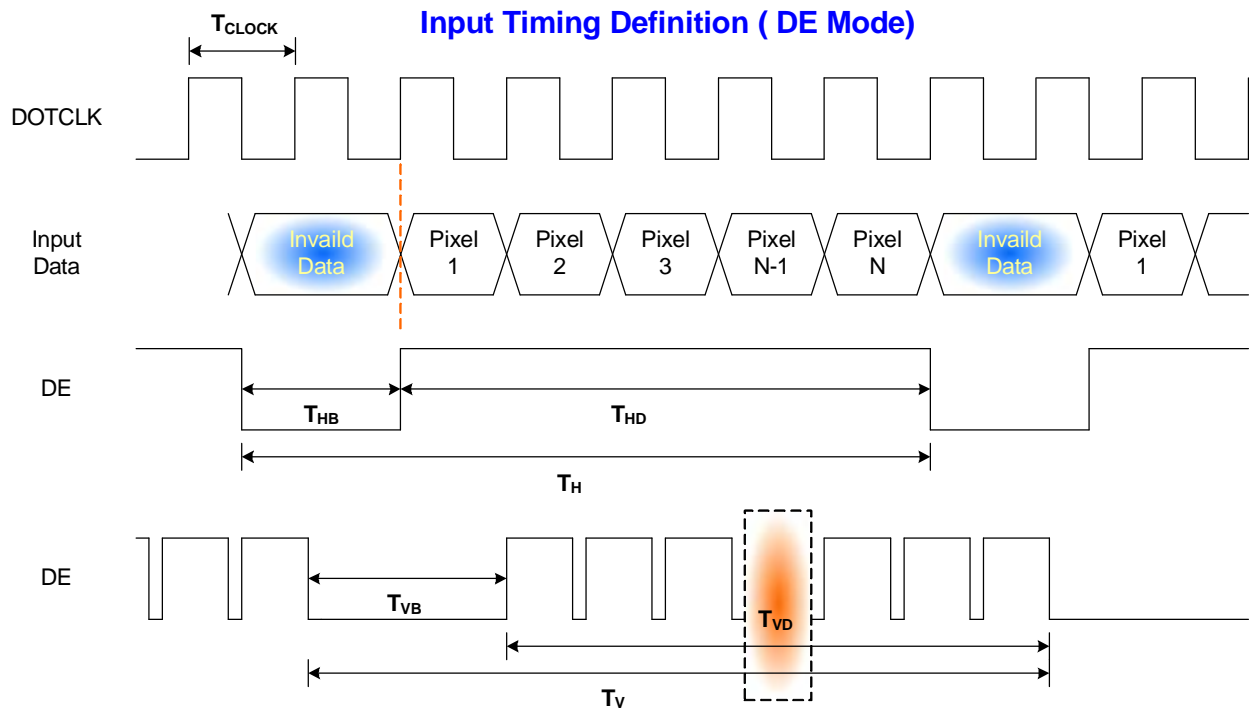
Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		$1/T_{\text{Clock}}$	50	71.11	80	MHz
Vertical Section	Period	T_V	803	823	1023	T_{Line}
	Active	T_{VD}	800	800	800	
	Blanking	T_{VB}	3	23	223	
Horizontal Section	Period	T_H	1303	1440	2047	T_{Clock}
	Active	T_{HD}	-	1280	-	
	Blanking	T_{HB}	23	160	767	

Note : DE mode only



6.4.2 Timing diagram



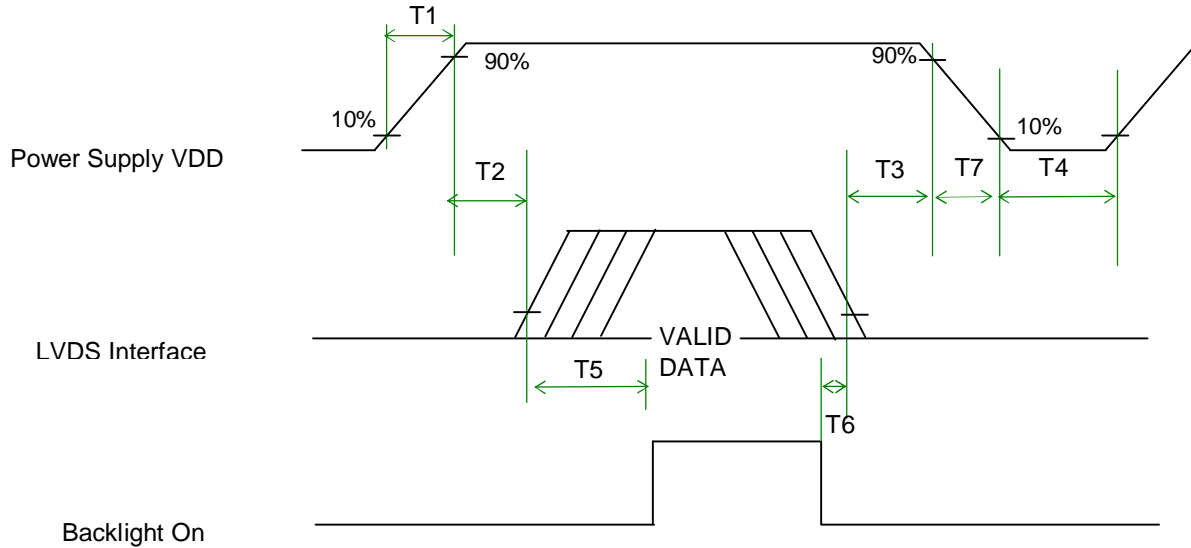


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6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)



7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SL-HF10 or compatible
Mating Housing/Part Number	FI-X30H or compatible

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage



8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- I Test method: Non-Operation
- I Acceleration: 1.5 G
- I Frequency: 10 - 500Hz Random
- I Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

- I Test method: Non-Operation
- I Acceleration: 220 G , Half sine wave
- I Active time: 2 ms
- I Pulse: X,Y,Z .one time for each side



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9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	40°C/90%,300Hr	
High Temperature Operation	50°C/Dry,300Hr	
Low Temperature Operation	0°C,300Hr	
On/Off Test	25°C,150hrs(ON/10 sec. OFF/10sec., 10,000 cycles)	
Hot Storage	60°C/35% RH ,250 hours	
Cold Storage	-20°C/50% RH ,250 hours	
Thermal Shock Test	-20°C/30 min ,60°C/30 min 100cycles	
Hot Start Test	50°C/1 Hr min. power on/off per 5 minutes, 5 times	
Cold Start Test	0°C/1 Hr min. power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	220G, 2ms, Half-sine wave	
Vibration Test (Non-Operating)	Random vibration, 1.5 G zero-to-peak, 10 to 500 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact : $\pm 8KV$ / operation Air : $\pm 15KV$ / operation	Note 1
Room temperature Test	25°C , 2000hours, Operating with loop pattern	

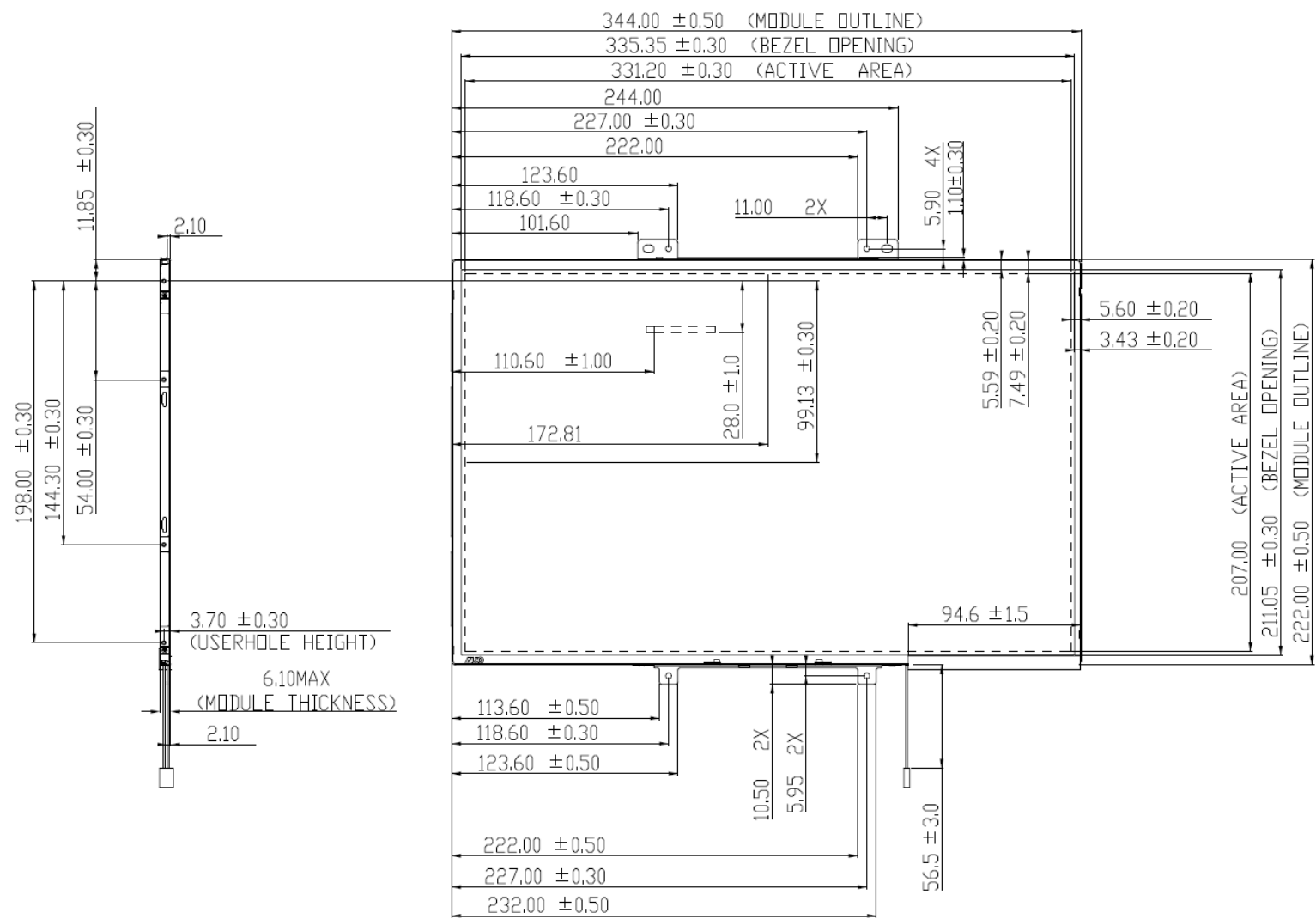
Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost
Self-recoverable. No hardware failures.

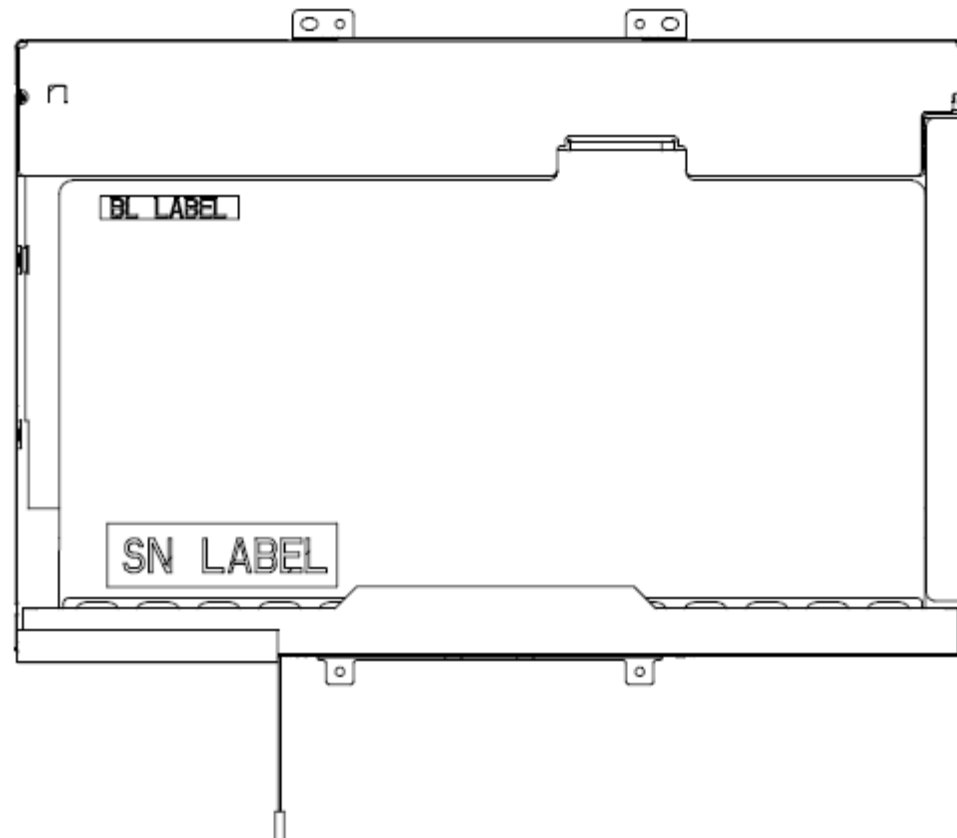
Note2: CCFL Life time: 12,000 hours minimum under normal module usage.

Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

10. Mechanical Characteristics

10.1 LCM Outline Dimension



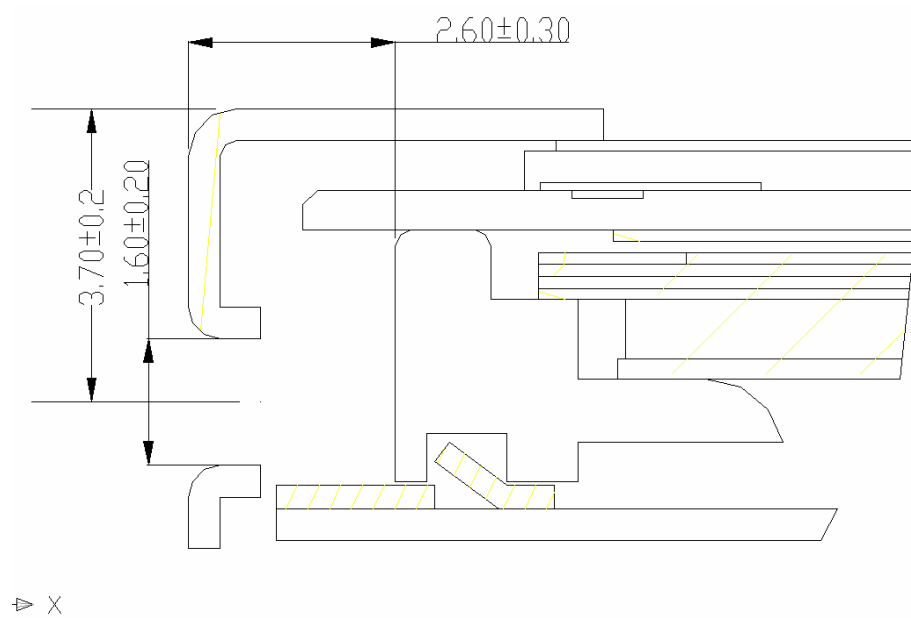


10.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface = 2.3 mm (See drawing)

Screw hole center location, from front surface = 3.7 ± 0.2 mm (See drawing)

Screw Torque: Maximum 2.5 kgf-cm



11. Shipping and Package

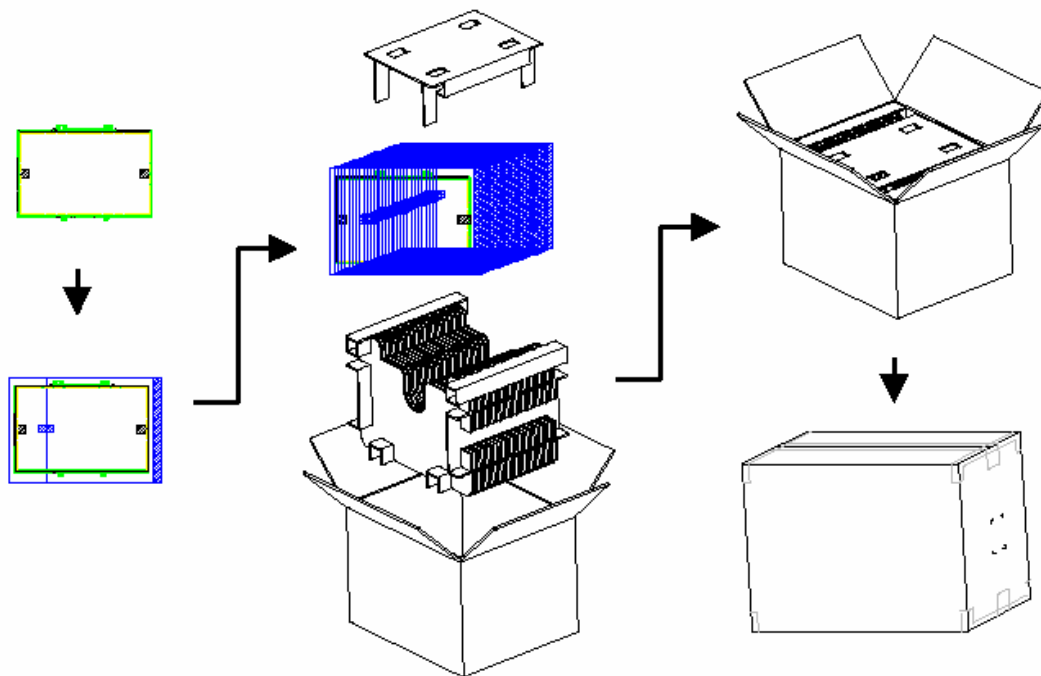
11.1 Shipping Label Format



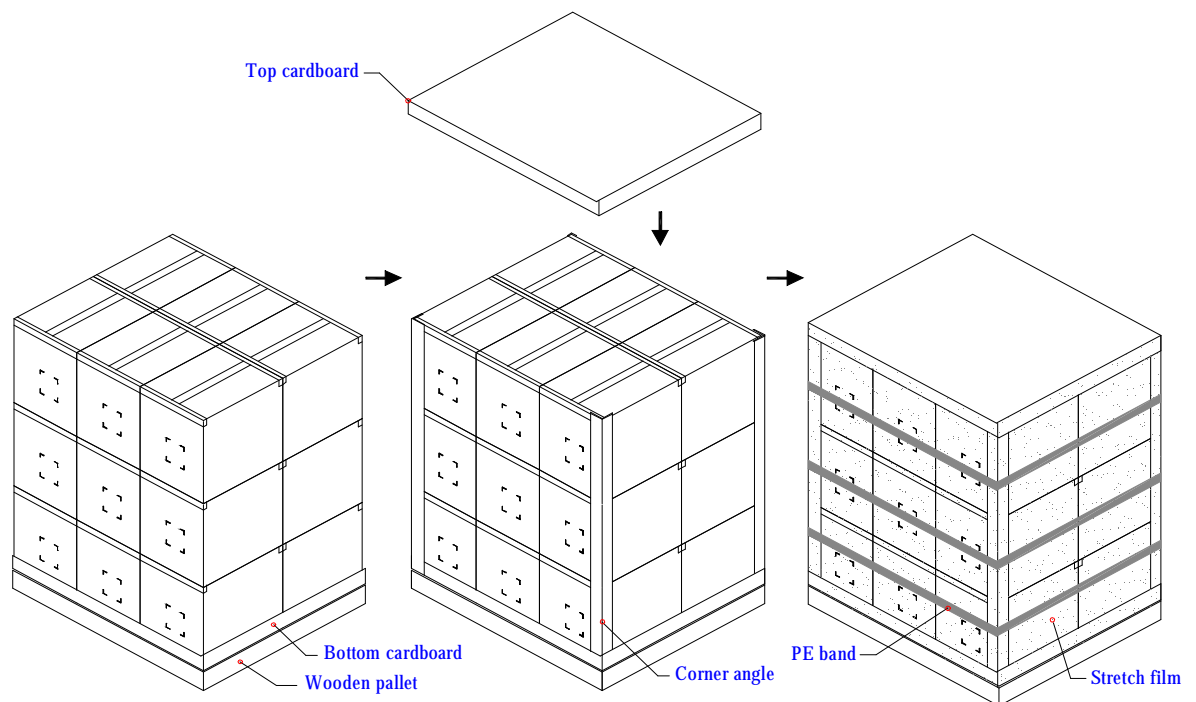
*Note#1: H/W 0A & 4A represents Novatek source driver and MEC gate driver combination
*Note#2: H/W 1A represents Radium source driver and TSB gate driver combination

11.2. Carton package

The outside dimension of carton is 455 (L)mm x 380 (W)mm x 355 (H)mm



11.3 Shipping package of palletizing sequence



Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)

12. Appendix: EDID description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	74	01110100	116	
0B	hex, LSB first	81	10000001	129	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	01	00000001	1	
11	Year of manufacture	10	00010000	16	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	03	00000011	3	
14	Video input def. <i>(digital I/P, non-TMDS, CRGB)</i>	80	10000000	128	
15	Max H image size <i>(rounded to cm)</i>	21	00100001	33	
16	Max V image size <i>(rounded to cm)</i>	15	00010101	21	
17	Display Gamma <i>(=(gamma*100)-100)</i>	78	01111000	120	
18	Feature support <i>(no DPMS, Active OFF, RGB, tmg Blk#1)</i>	0A	00001010	10	
19	Red/green low bits (Lower 2:2:2:2 bits)	1C	00011100	28	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	F5	11110101	245	
1B	Red x (Upper 8 bits)	97	10010111	151	
1C	Red y/ highER 8 bits	58	01011000	88	
1D	Green x	50	01010000	80	
1E	Green y	8E	10001110	142	
1F	Blue x	27	00100111	39	
20	Blue y	27	00100111	39	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	

28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	C7	11000111	199	
37	Pixel Clock/10000 USB	1B	00011011	27	
38	Horz active Lower 8bits	00	00000000	0	
39	Horz blanking Lower 8bits	A0	10100000	160	
3A	HorzAct:HorzBlnk Upper 4:4 bits	50	01010000	80	
3B	Vertical Active Lower 8bits	20	00100000	32	
3C	Vertical Blanking Lower 8bits	17	00010111	23	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	00110000	48	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	36	00110110	54	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
42	Horizontal Image Size Lower 8bits	4B	01001011	75	
43	Vertical Image Size Lower 8bits	CF	11001111	207	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16	
45	Horizontal Border <i>(zero for internal LCD)</i>	00	00000000	0	
46	Vertical Border <i>(zero for internal LCD)</i>	00	00000000	0	
47	Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i>	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	

54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	35	00110101	53	5
74	Manufacture P/N	34	00110100	52	4
75	Manufacture P/N	45	01000101	69	E
76	Manufacture P/N	57	01010111	87	W
77	Manufacture P/N	30	00110000	48	0
78	Manufacture P/N	38	00111000	56	8
79	Manufacture P/N	20	00100000	32	
7A	Manufacture P/N	56	01010110	86	V
7B	Manufacture P/N	31	00110001	49	1
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	43	01000011	67	

