Product Functional Specification

15 inch SXGA+ Color TFT LCD Module
Model Name : B150PG01 V.0

( ) Preliminary Specification
(◆) Final Specification

Note: This Specification is subject to change without notice.

I. Contents

II Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1. 2001/8/13	All	First Edition for Customer	All	
0.2 2001/12/12	5	(Tr, Tf)= (35,15)	(Tr, Tf)= (15,35)	
0.3 2002/3/5	8		Update CIE	
0.3 2002/3/5	9		Update pin assignment	
0.4 2002/4/23	5,8		Add luminance uniformity	
0.5 2003/2/07	16	Lamp off falling time = 0ms	Lamp off falling time = 180ms	
0.6 2003/10/03	9		Optical measurement position	
0.7 2004/7/28	20	N/A	Add EDID information	

1.0 Handing Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(2.11, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit(2.4, IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

2.0 General Description

This specification applies to the 15.0 inch Color TFT/LCD Module B150PG01.

This module is designed for a display unit of notebook style personal computer.

The screen format is intended to support the SXGA+ (1400(H) x 1050(V)) screen and 262k colors (RGB 6-bits data driver).

All input signals are LVDS interface compatible.

This module does not contain an inverter card for backlight.

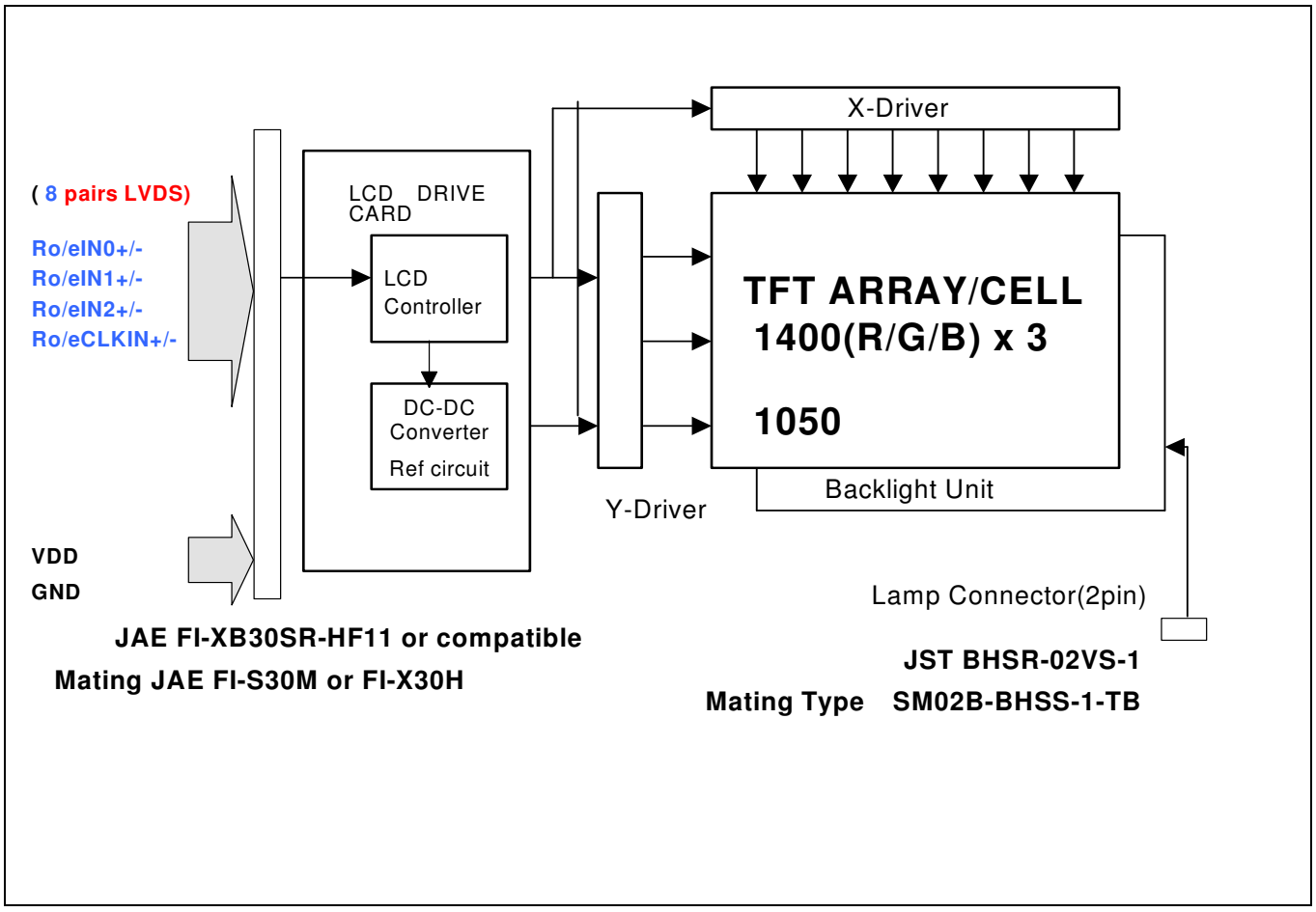
2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	381
Active Area	[mm]	304.5 X 228.375
Pixels H x V		1400(x3) x 1050
Pixel Pitch	[mm]	0.2175X0.2175
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance (ICFL=6.0mA)	[cd/m^2]	150 (5 point average/ typ .) 120 (5 point average/ min.)
Luminance Uniformity		1.25 max. (5 pts) 1.65 max. (13pts)
Contrast Ratio		250
Optical Rise Time/Fall Time	[msec]	15/35
Nominal Input Voltage VDD	[Volt]	+3.3 Typ.
Typical Power Consumption (VDD line + VCFL line)	[Watt]	5.7W
Weight	[Grams]	550g typ.
Physical Size	[mm]	317.3 x 242.0 x 6.0 max.
Electrical Interface		2 channel LVDS
Support Color		Native 262K colors (RGB 6-bit data driver)
Temperature Range Operating Storage (Shipping)	 [^{o}C] [^{o}C]	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of the 15.0 inches Color TFT/LCD Module:



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	[Volt]	
Input Voltage of Signal	Vin	-0.3	VDD+0.3	[Volt]	
CCFL Current	ICFL	-	7	[mA] rms	
CCFL Ignition Voltage	Vs	-	1150	Vrms	
Operating Temperature	TOP	0	+50	[^{o}C]	Note 1
Operating Humidity	HOP	8	95	[%RH]	Note 1
Storage Temperature	TST	-20	+60	[^{o}C]	Note 1
Storage Humidity	HST	5	95	[%RH]	Note 1
Vibration			1.5 10-500 (random)	G Hz	2hr/axis, X,Y,Z
Shock			220 , 2	G ms	Half sine wave

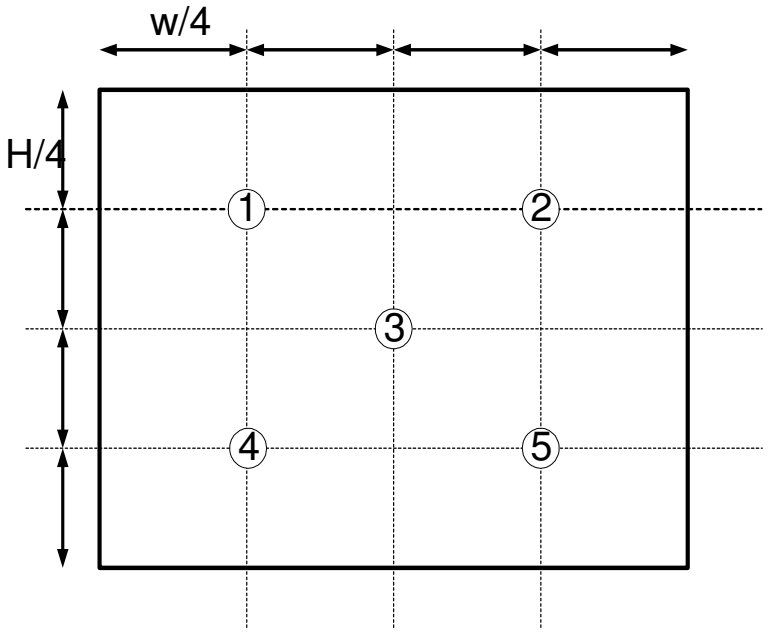
Note 1 : Maximum Wet-Bulb should be 39℃ and No condensation.

4.0 Optical Characteristics

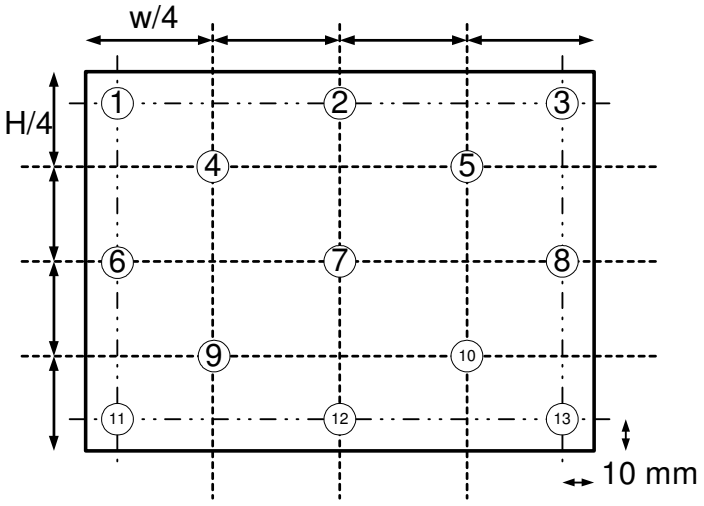
The optical characteristics are measured under stable conditions as follows under 25℃ condition:

Item		Conditions	Min.	Typ.	Max.
Viewing Angle K: Contrast Ratio	[degree] [degree] [degree] [degree]	Horizontal (Right) K = 10 (Left) Vertical (Upper) K = 10 (Lower)	40 40 10 30		
Contrast ratio				250	
Luminance Uniformity					1.25 (5pts) 1.65 (13pts)
Response Time (Room Temp.)	[msec] [msec]	Rising Falling		15 35	45(Max.) 45(Max.)
Color Chromaticity Coordinates (CIE)		Red x	0.538	0.568	0.598
		Red y	0.301	0.331	0.361
		Green x	0.275	0.305	0.335
		Green y	0.518	0.548	0.578
		Blue x	0.121	0.151	0.181
		Blue y	0.102	0.132	0.162
		White x	0.283	0.313	0.343
		White y	0.299	0.329	0.359
White Luminance (CCFL 6.0 mA)	[cd/m^2]		120 (5 points average)	150 (5 points average)	

Note 1: 5 points position (Display area)



Note 2: 13 points position



5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SR-HF11 or compatible
Mating Housing/Part Number	FI-X30M, FI-X30C or FI-X30H
Mating Contact/Part Number	FI-C3-A1

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

5.2 Signal Pin

Pin#	Signal Name	Pin#	Signal Name
1	GND	2	VDD
3	VDD	4	VEDID
5	AGmode	6	CLKEDID
7	DATAEDID	8	RoIN0-
9	RoIN0+	10	GND
11	RoIN1-	12	RoIN1+
13	GND	14	RoIN2-
15	RoIN2+	16	GND
17	RoCLKIN-	18	RoCLKIN+
19	GND	20	ReIN0-
21	ReIN0+	22	GND
23	ReIN1-	24	ReIN1+
25	GND	26	ReIN2-
27	ReIN2+	28	GND
29	ReCLKIN-	30	ReCLKIN+

5.3 Signal Description

The module using a LVDS receiver. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.

Signal Name	Description
RoIN0-, RoIN0+	LVDS differential Odd data input(Red0-Red5, Green0)
RoIN1-, RoIN1+	LVDS differential Odd data input(Green1-Green5, Blue0-Blue1)
RoIN2-, RoIN2+	LVDS differential Odd data input(Blue2-Blue5, Hsync, Vsync, DSPTMG)
RoCLKIN-, RoCLKIN0+	LVDS Odd differential clock input
ReIN0-, ReIN0+	LVDS differential Even data input(Red0-Red5, Green0)
ReIN1-, ReIN1+	LVDS differential Even data input(Green1-Green5, Blue0-Blue1)
ReIN2-, ReIN2+	LVDS differential Even data input(Only Blue2-Blue5)
ReCLKIN-, ReCLKIN0+	LVDS Even differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note: Input signals shall be low or Hi-Z state when VDD is off.

Internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input

Signal Name	Description	
RED5 RED4 RED3 RED2 RED1 RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
GREEN 5 GREEN 4 GREEN 3 GREEN 2 GREEN 1 GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
BLUE 5 BLUE 4 BLUE 3 BLUE 2 BLUE 1 BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
DTCLK	Data Clock	The typical frequency is 54.0 MHZ.. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	Display Timing	This signal is strobed at the falling edge of DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync	The signal is synchronized to DTCLK .
HSYNC	Horizontal Sync	The signal is synchronized to DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

5.4 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

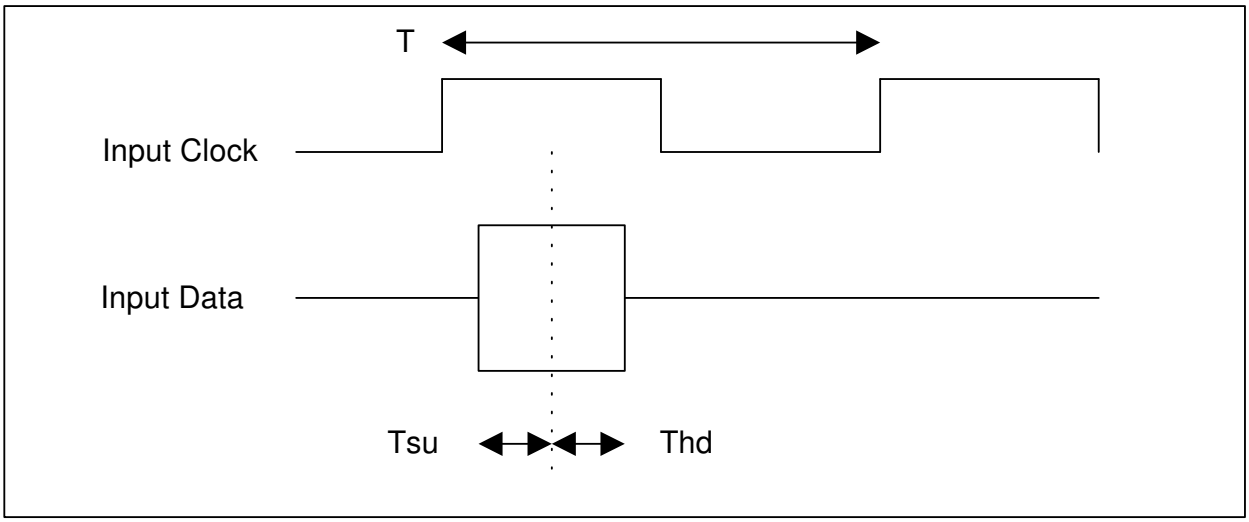
It is recommended to refer the specifications of SN75LVDS86DGG(Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Voltage(Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Voltage(Vcm=+1.2V)	-100		[mV]

LVDS Macro AC characteristics are as follows:

	Min.	Max.
Clock Frequency (T)	51MHZ	57MHZ
Data Setup Time (Tsu)	500ps	
Data Hold Time (Thd)	500ps	

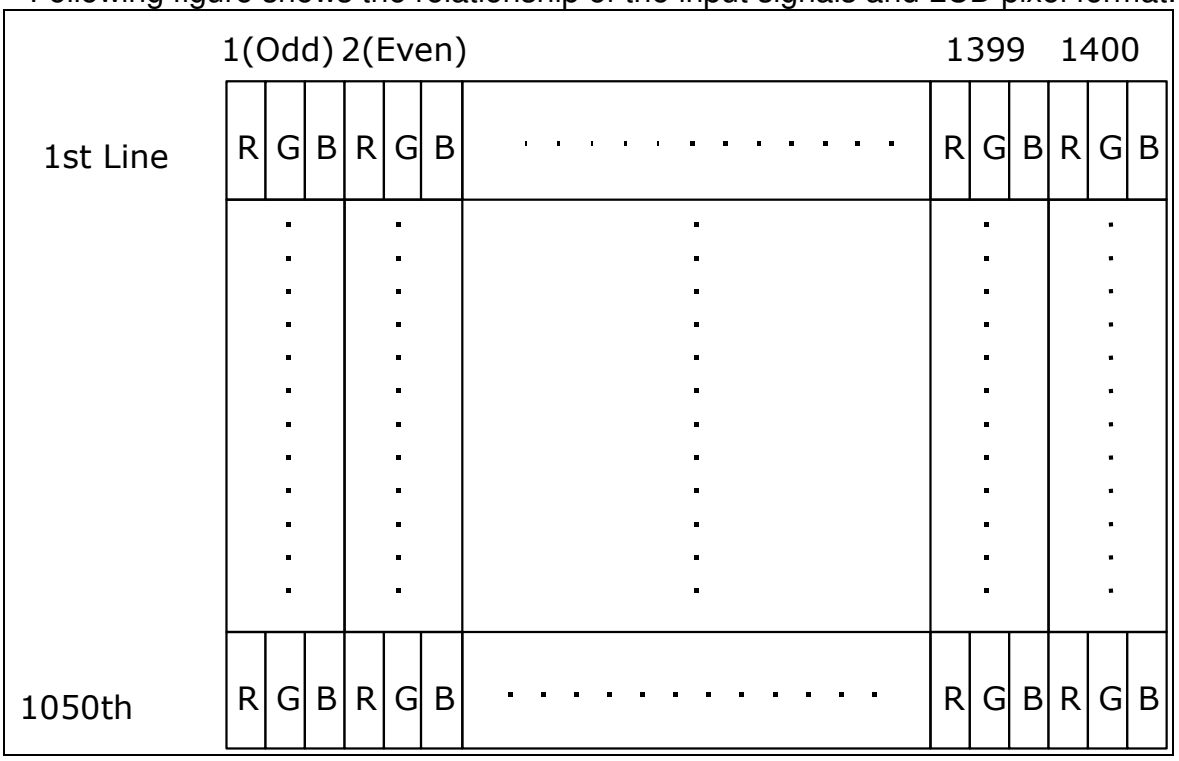


5.5 Signal for Lamp connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



7.0 Parameter guide line for CFL Inverter

Parameter	Min	DP-1	Max	Units	Condition
White Luminance 5 points average	-	150	—	[cd/m^2]	(Ta=25℃)
CCFL current(ICFL)	3.0	5.5	7.0	[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(FCFL)	50	60	70	[KHz]	(Ta=25℃) Note 3
CCFL Ignition Voltage(Vs)		—	1,150	[Volt] rms	(Ta= 0℃) Note 4
CCFL Voltage (Reference) (VCFL)	—	700	—	[Volt] rms	(Ta=25℃) Note 5
CCFL Power consumption (PCFL)	—	3.9	—	[Watt]	(Ta=25℃) Note 5

Note 1: DP-1 are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
*3 In designing an inverter, it is suggested to check safety circuit ver carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.
*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.
*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be emplyed the inverter which has “Duty Dimming”, if ICFL is less than 4mA.
Note 3: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.
Note 4: CFL inverter should be able to give out a power that has a generating capacity of over 1,400 voltage. Lamp units need 1,400 voltage minimum for ignition.
Note 5: Calculator value for reference (ICFL×VCFL=PCFL)

8.0 Interface Timings

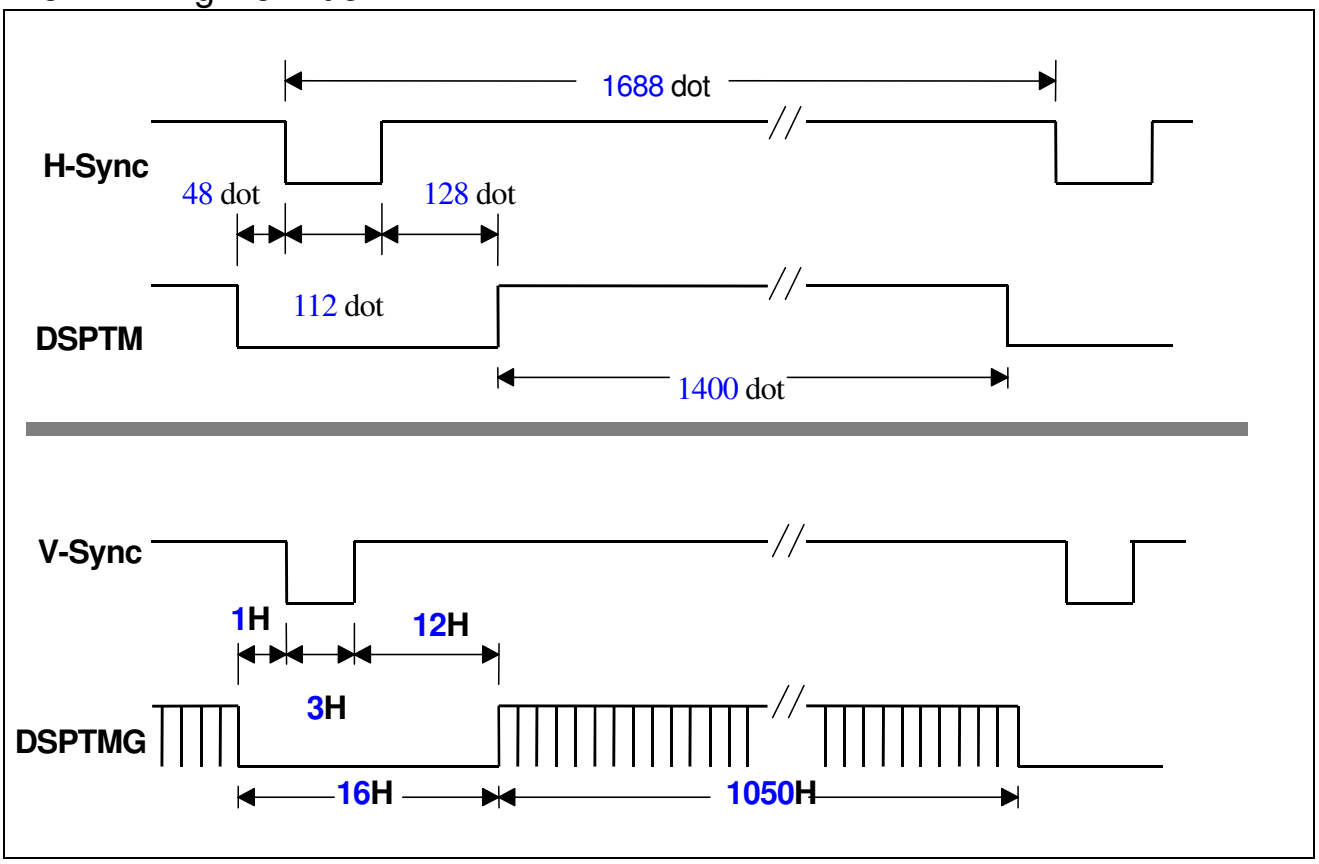
Basically, interface timings should match the manufacturing guide line timing.

8.1 Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
fdck	DTCLK Frequency	51	54.00	57	[MHz]
tck	DTCLK cycle time		18.5		[nsec]
tx	X total time	780	844	1024	[tck]
tacx	X active time	700	700	700	[tck]
tbkx	X blank time	80	144	324	[tck]
Hsync	H frequency		63.98		[KHz]
Hsw	H-Sync width	4	56		[tck]
Hbp	H back porch	4	64		[tck]
Hfp	H front porch	4	24		[tck]
ty	Y total time	1060	1066	2048	[tx]
tacy	Y active time	1050	1050	1050	[tx]
Vsync	Frame rate	(55)	60	61	[Hz]
Vw	V-sync Width	1	3		[tx]
Vfp	V-sync front porch	1	1	34	[tx]
Vbp	V-sync back porch	7	12	63	[tx]

Note: Hsw(H-sync width) + Hbp(H-sync back porch) should be less than 515 tck.

8.2 Timing Definition



9.0 Power Consumption

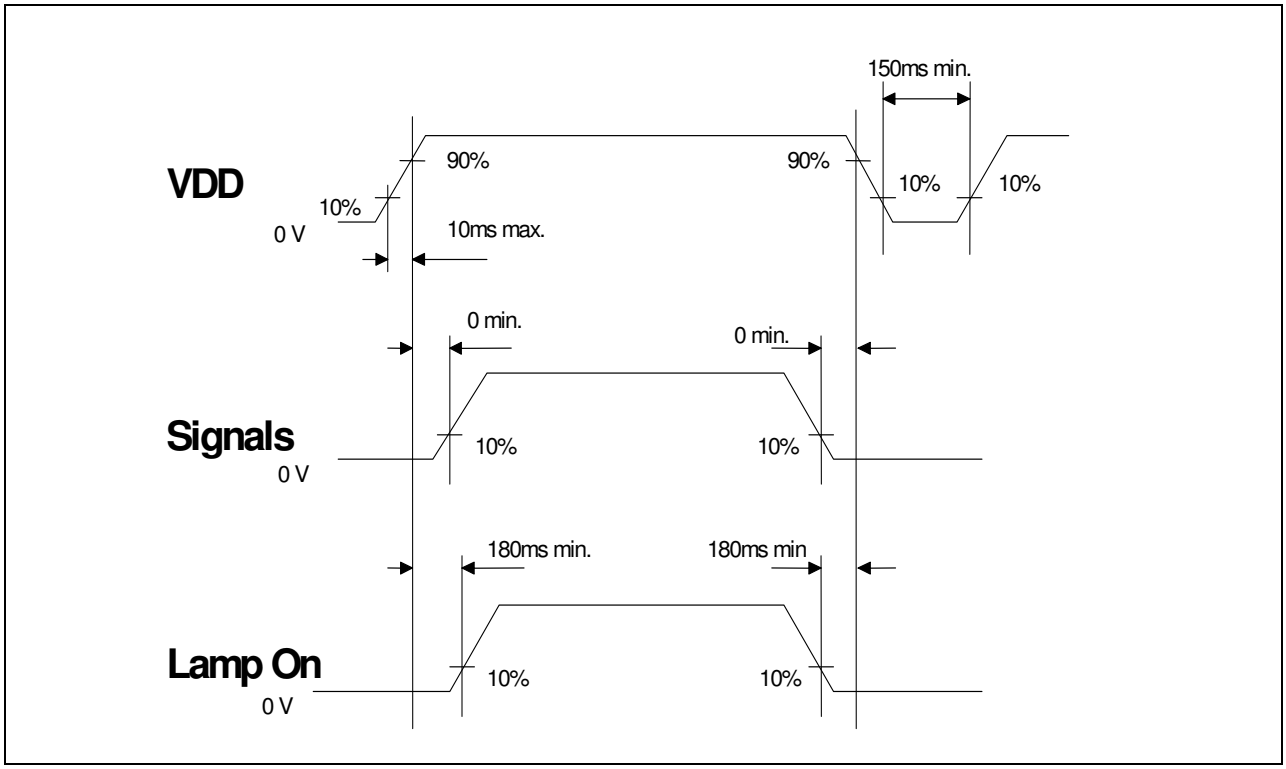
Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		1.8		[Watt]	All Black Pattern
PDD Max	VDD Power max			2.47	[Watt]	Max Pattern Note
IDD	IDD Current		530		mA	All Black Pattern
IDD Max	IDD Current max			750	mA	Max Pattern Note
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mV] p-p	

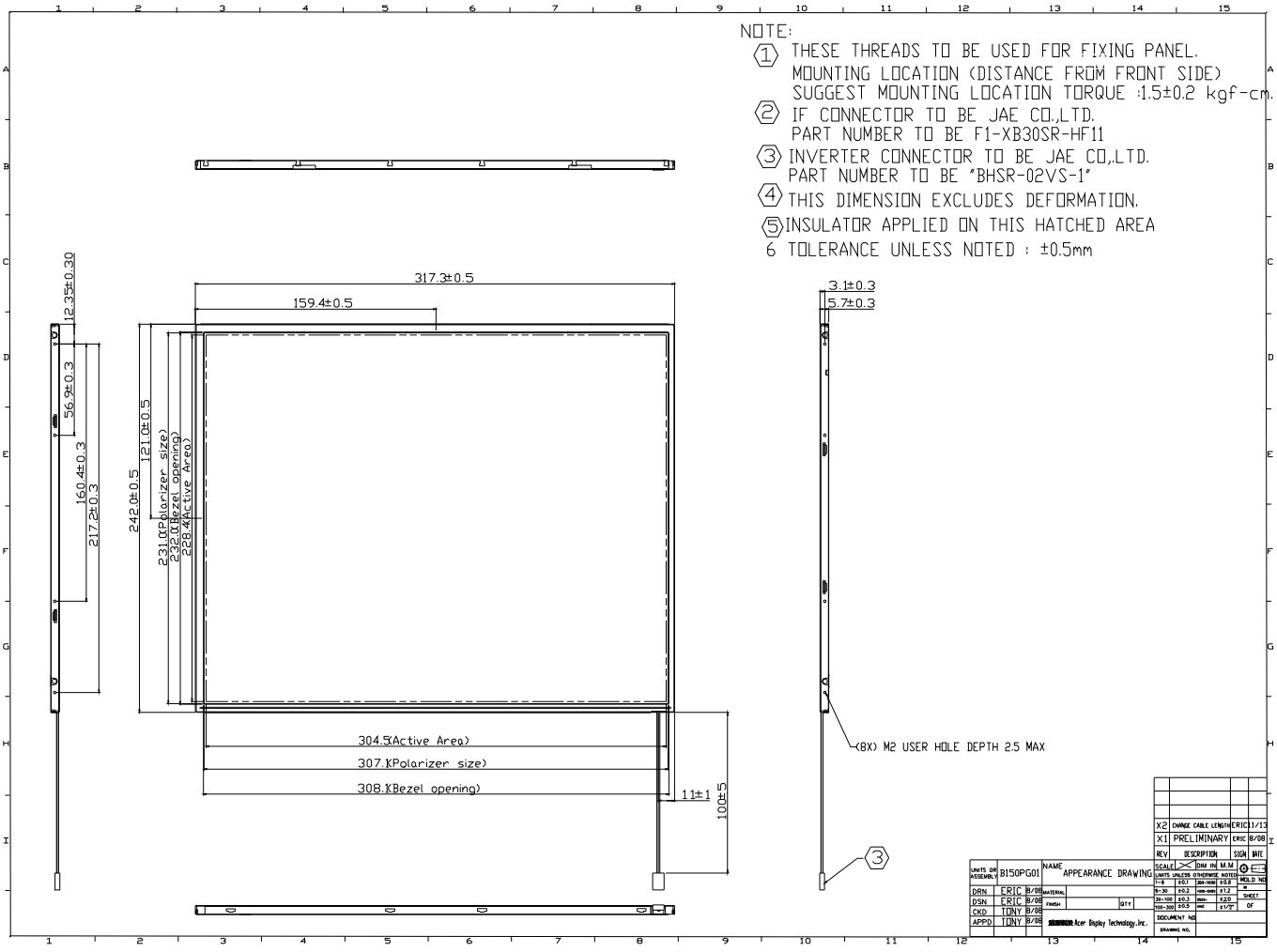
Note : VDD=3.3V

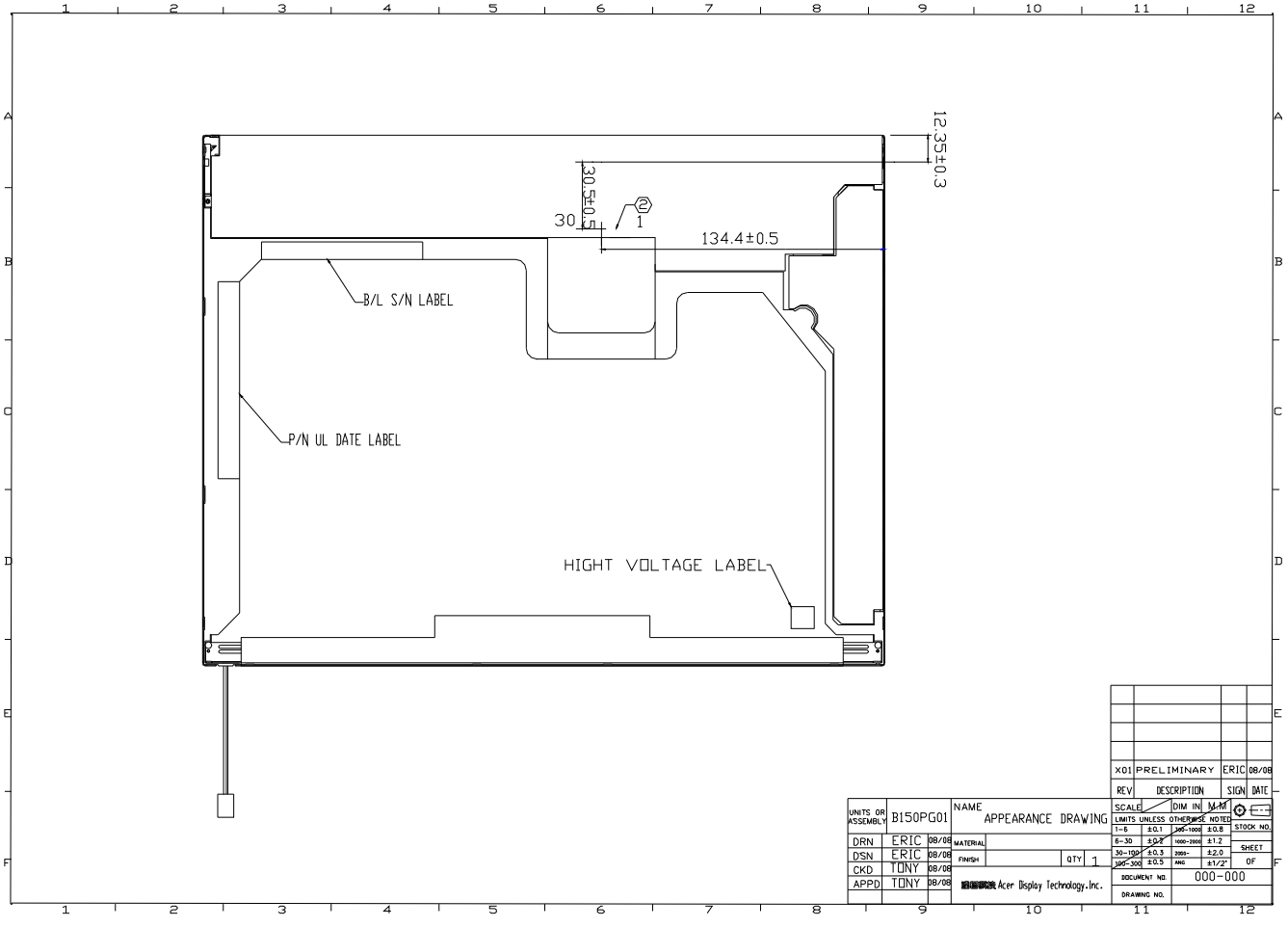
10. Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



11. Mechanical Characteristics





12. EDID Information

	ISP Enhanced Extended Display Identification Data (EDID) Requirements			AU 15.0" SXGA B150PG01
Ver 8	Byte# (dec)	Byte# (hex)	Field Name and Comments	Byte# (hex)
Header	0	00	Header	00
	1	01		FF
	2	02		FF
	3	03		FF
	4	04		FF
	5	05		FF
	6	06		FF
	7	07		00
Vender/ Product ID	8	08	EISA manufacturer code = (1st byte)	06
	9	09	(2nd byte)	AF
	10	0A	Product code LSB =	03
	11	0B	Product code MSB =	0F
	12	0C	ID (32-bit) serial number (preferred, but optional, zero if not used)	01
	13	0D		01
	14	0E		01
	15	0F		01
	16	10	Week of manufacture = (preferred, but optional, zero if not used)	00
	17	11	Year of manufacture = (preferred, but optional, zero if not used)	0C
EDID Version/ Revision	18	12	EDID Structure version # =	01
	19	13	EDID Revision # =	02
Display Parameter	20	14	Video input definition = Digital I/P, non TMDS CRGB typ 80h	80
	21	15	Max H image size (xx) (rounded to cm)	1E
	22	16	Max V image size (xx) (rounded to cm)	17
	23	17	Display gamma = x.x (=(gamma*100)-100)	78
	24	18	Feature (no DPMS, Active off, RGB, timing BLK1)	0A
Color Characteristic	25	19	Red/Green low Bits	76
	26	1A	Blue/White Low Bits	C5
	27	1B	Red X Rx =0.xxx	91
	28	1C	Red Y Ry =0.xxx	54
	29	1D	Green X Gx =0.xxx	4E
	30	1E	Green Y Gy =0.xxx	8C
	31	1F	Blue X Bx =0.xxx	26
	32	20	Blue Y By =0.xxx	22
	33	21	White X Wx = 0.xxx	50

	34	22	White Y Wy = 0.xxx	54
Established Timings	35	23	Established Timing I (00h if not used)	00
	36	24	Established Timing II (00h if not used)	00
	37	25	Manufacturer's Timings (00h if not used)	00
Standard Timing ID	38	26	Standard Timing Identification 1 (01h if not used)	01
	39	27	Standard Timing Identification 1 (01h if not used)	01
	40	28	Standard Timing Identification 2 (01h if not used)	01
	41	29	Standard Timing Identification 2 (01h if not used)	01
	42	2A	Standard Timing Identification 3 (01h if not used)	01
	43	2B	Standard Timing Identification 3 (01h if not used)	01
	44	2C	Standard Timing Identification 4 (01h if not used)	01
	45	2D	Standard Timing Identification 4 (01h if not used)	01
	46	2E	Standard Timing Identification 5 (01h if not used)	01
	47	2F	Standard Timing Identification 5 (01h if not used)	01
	48	30	Standard Timing Identification 6 (01h if not used)	01
	49	31	Standard Timing Identification 6 (01h if not used)	01
	50	32	Standard Timing Identification 7 (01h if not used)	01
	51	33	Standard Timing Identification 7 (01h if not used)	01
	52	34	Standard Timing Identification 8 (01h if not used)	01
	53	35	Standard Timing Identification 8 (01h if not used)	01
Detailed Timing Description #1	54	36	Pixel Clock/10,000 (LSB)	30
	55	37	Pixel Clock/10,000 (MSB)	2A
	56	38	Horizontal Active = xxxx pixels (lower 8 bits)	78
	57	39	Horizontal Blanking (Thbp)= xxxx pixels (lower 8 bits)	F0
	58	3A	Horizontal Active : Horizontal Blanking (Thbp) (upper 4:4bits)	50
	59	3B	Vertical Avtive = xxx lines	1A
	60	3C	Vertical Blanking (Tvbp) = xxxx (DE Blanking min for DE-only panels) lines	0F
	61	3D	Vertical Active : Vertical Blanking (Tvbp) (upper 4:4bits)	40
	62	3E	Horizontal Sync. Offset = xxxx pixels	30
	63	3F	Horizontal Sync Pulse Width = xxxx pixels	70
	64	40	Vertical Sync Offset (Tvfp) = xx lines, Sync Width = xx lines	13
	65	41	Horizontal Vertical Sync Offset/Width upper 2bits	00
	66	42	Horizontal Image Size = xxx mm (lower 8 bits)	31
	67	43	Vertical Image Size = xxx mm (lower 8 bits)	E4
	68	44	Horizontal & Vertical Image Size (upper 4:4bits)	10
	69	45	Horizontal Border (Zero for internal LCD)	00
	70	46	Vertical Border (Zero for internal LCD)	00
	71	47	Non-interlaced,Normal display,no stereo,Digital separate sync,H/V pol negatives	18
	72	48	Flag	00

	73	49	Flag	00
	74	4A	Flag	00
	75	4B	Data Type Tag: Descriptor Defined by Manufacturer	0F
	76	4C	Flag	00
	77	4D	value = HSPWmin/2 (pixel clks)	02
Detailed	78	4E	value = HSPWmax/2 (pixel clks)	3F
Timing	79	4F	value = Thbpmin/2 (pixel/clks) (for DE-only timing also, with Thfp=0)	02
Description	80	50	value = Thbpmax/2 (pixel/clks) (for DE-only timing also, with Thfp=0)	7F
#2	81	51	value = VSPWmin/2 (pixel clks)	01
	82	52	value = VSPWmax/2 (pixel clks)	1C
	83	53	value = Tvbpmin/2 (pixel clks)	04
	84	54	value = Tvbpmax/2 (pixel clks)	3B
	85	55	Thpmin = value*2 + HApixelClks (pixel clks) Note 2.	28
	86	56	Thpmax = value*2 + HApixelClks (pixel clks) Note 2.	A2
	87	57	Tvpmin = value*2 + Valines (line pulse)	05
	88	58	Tvpmax = value*2 + Valines (line pulse)	FF
	89	59	Module revision	02
	90	5A	Flag	00
	91	5B	Flag	00
	92	5C	Flag	00
	93	5D	Data Type Tag: (Monitor) ASCII string	FE
	94	5E	Flag	00
	95	5F		41
	96	60		55
Detailed	97	61		4F
Timing	98	62		00
Description	99	63		00
#3	100	64		00
	101	65		00
	102	66		00
	103	67		00
	104	68		00
	105	69		0A
	106	6A		20
	107	6B	(if<13 char, then terminate with ASCII code 0Ah, and set remaining char = 20h)	20
	108	6C	Flag	00
	109	6D	Flag	00
	110	6E	Flag	00
	111	6F	Data Type Tag : (Monitor) ASCII String	FE
	112	70	Flag	00

Detailed Timing Description #4	113	71		42
	114	72		31
	115	73		35
	116	74		30
	117	75		50
	118	76		47
	119	77		30
	120	78		31
	121	79		00
	122	7A		0A
	123	7B		20
	124	7C		20
	125	7D	(if<13 char, then terminate with ASCII code 0Ah, and set remaining char = 20h)	20
Extension Flag	126	7E	Extension flag (#of optional 128-byte EDID extension blocks to follow, typ=0)	00
Checksum	127	7F	Checksum (the 1-bype sum of all 128 bytes in this EDID block shall equal zero)	00