Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications
(V) Final Specifications

Module	**11.6”(11.58”) WXGA 16:9 Color TFT-LCD with LED Backlight design**
Model Name	B116XAN03.0 (H/W:0A)
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**
Checked & Approved by	**Date**

Approved by	**Date**
Kevin KH Shen	11/14/2013
Prepared by	
Lanie Huang	11/14/2013

Note: This Specification is subject to change without notice.

DMPBU Marketing Division
AU Optronics corporation

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2013/11/13	All	First Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B116XAN03.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HDTV, 1366(H) x768(V) screen and 16.7M colors (RGB 6-bits+Hi-FRC data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B116XAN03.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	294.09 (11.58W")			
Active Area	[mm]	256.125(H) x 144(V)			
Pixels H x V		1366 x 3(RGB) x 768			
Pixel Pitch	[mm]	0.1875 X 0.1875			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (I_{LED}=21mA) **(Note: ILED is LED current)**	[cd/m^2]	400 typ. (5 points average) 340 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		800 typ			
Response Time	[ms]	25 typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.4 max. (Include Logic and Blu power)			
Weight	[Grams]	200 max.			
Physical Size (panel only) **without bracket**	[mm]		Min.	Typ.	Max.
		Length	267.5	268	268.5
		Width	158	158.5	159
		Thickness	---	---	4.5
Electrical Interface		LVDS			
Glass Thickness	[mm]	0.25			

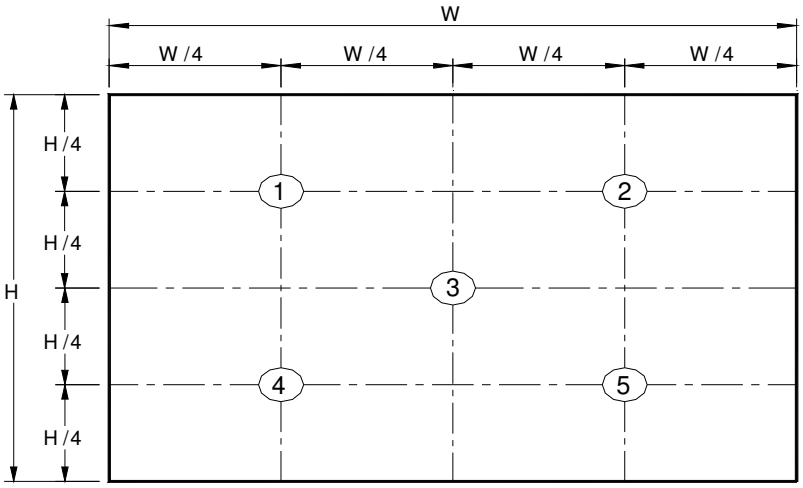
Surface Treatment(panel only)		Anti-Glare
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

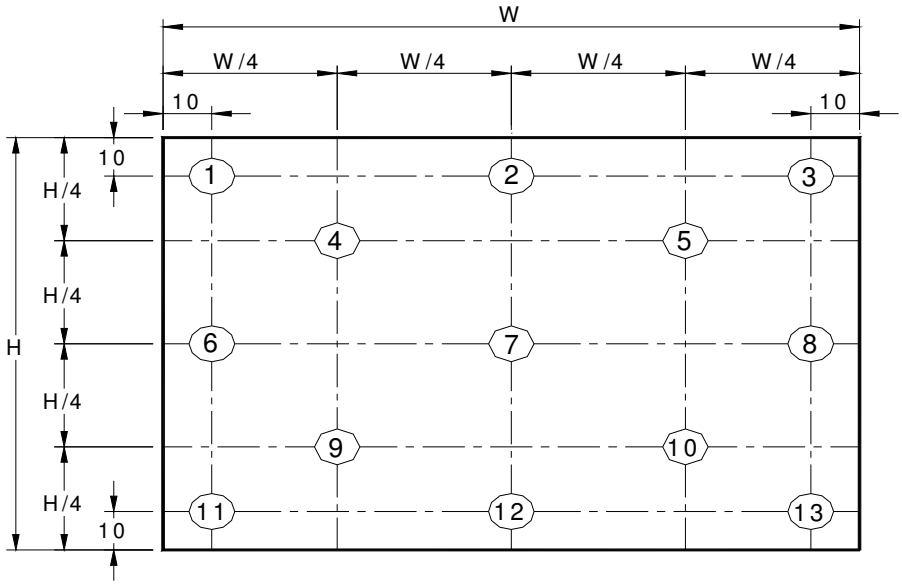
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=21mA			5 points average	340	400	---	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)		85 85	--- ---	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)		85 85	--- ---		
Luminance Uniformity		δ_{5P}	5 Points	---	---	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	---	---	1.67		2, 3, 4
Contrast Ratio		CR			800	-		4, 6
Cross talk		%		---	---	4		4, 7
Response Time		T_{RT}	Rising + Falling	---	25	35	msec	4, 8
Color / Chromaticity Coordinates	Red	Rx	CIE 1931	0.559	0.589	0.619		4
		Ry		0.307	0.337	0.367		
	Green	Gx		0.299	0.329	0.359		
		Gy		0.558	0.588	0.618		
	Blue	Bx		0.126	0.156	0.186		
		By		0.098	0.128	0.158		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	50	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



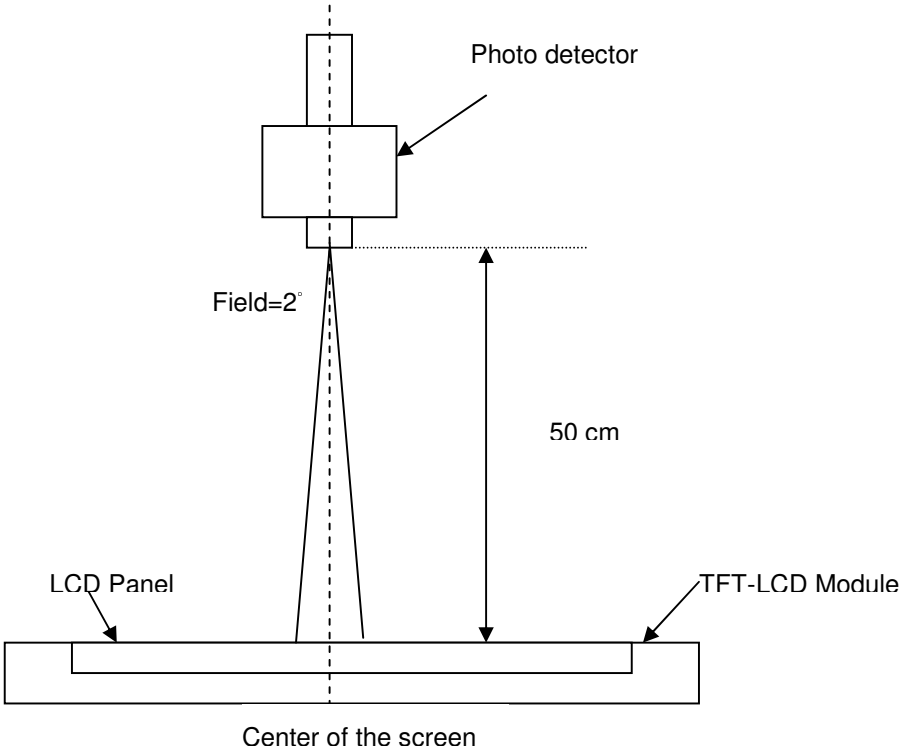
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

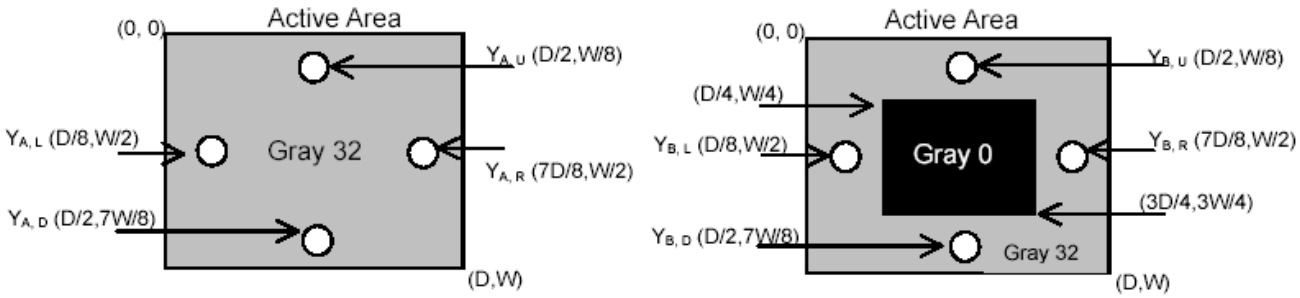
Note 7 : Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where

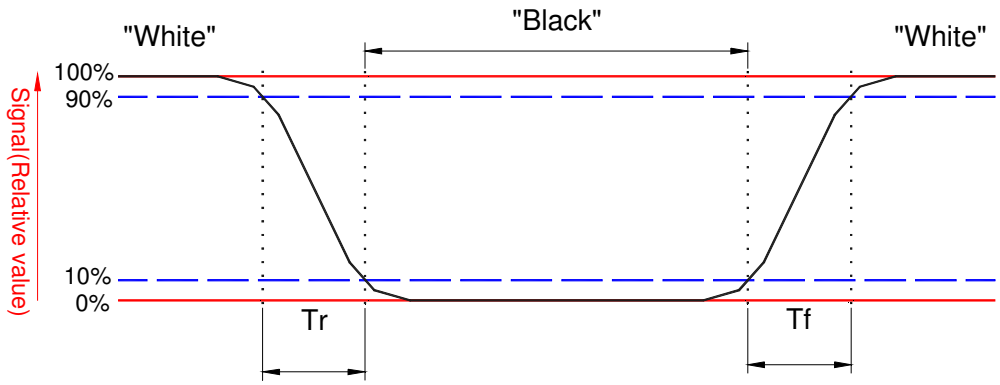
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



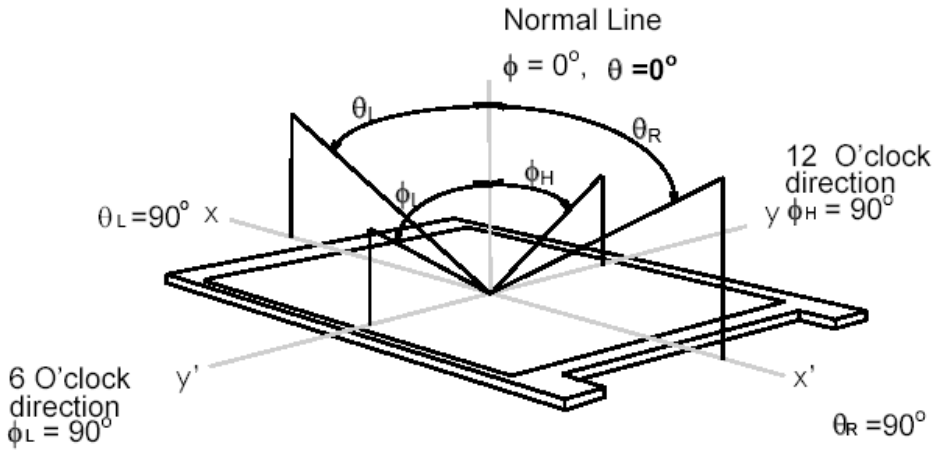
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



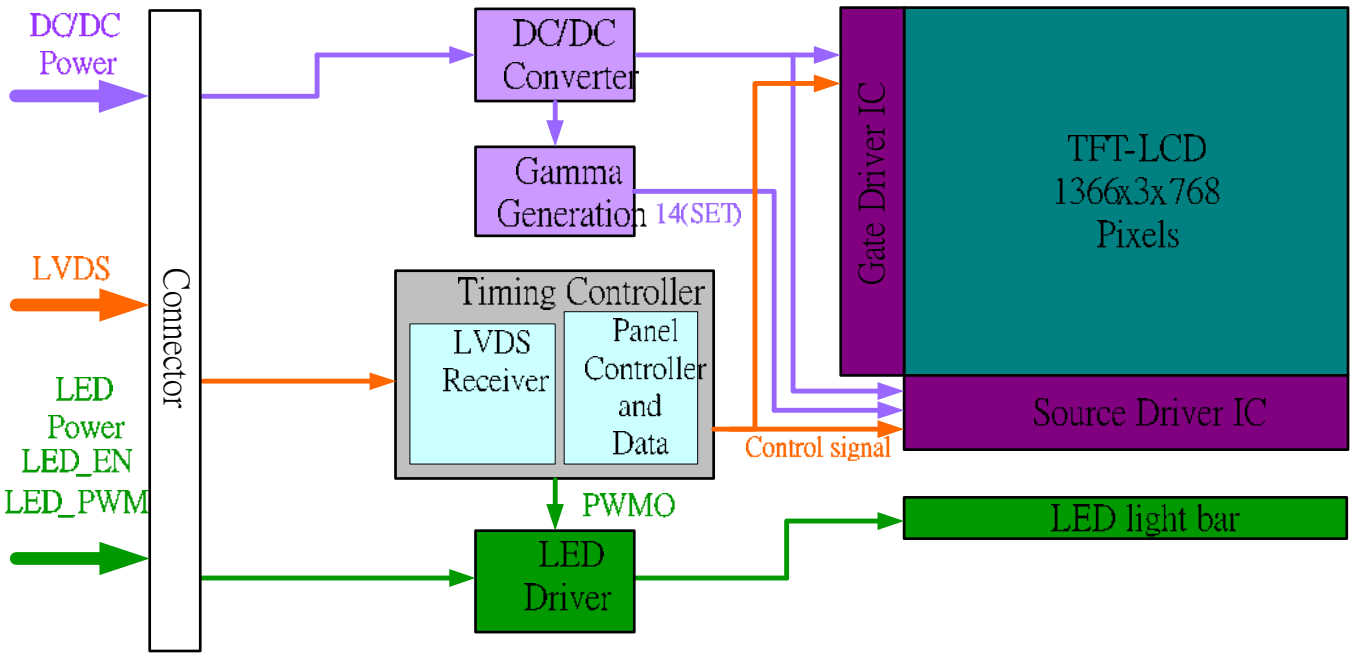
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 40 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

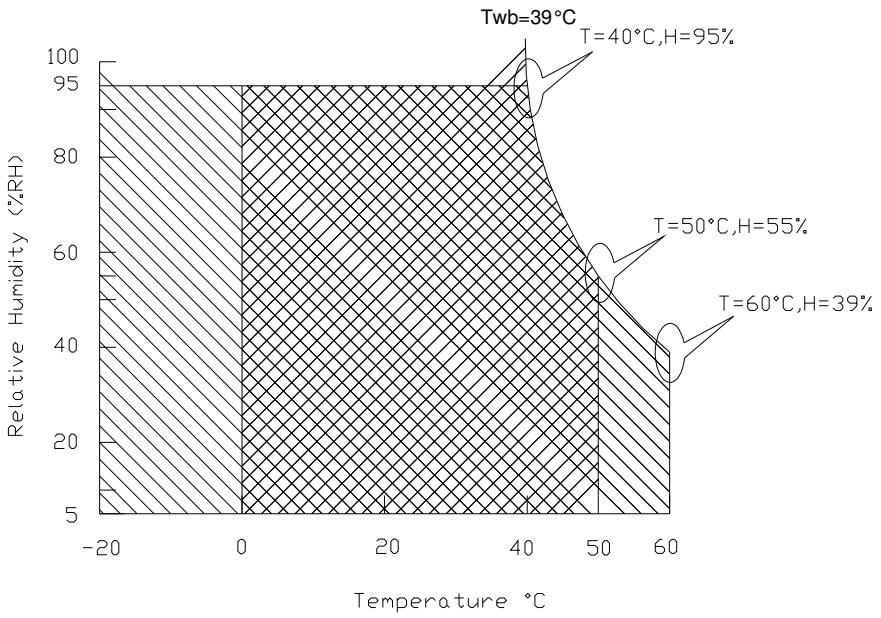
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	**50**	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

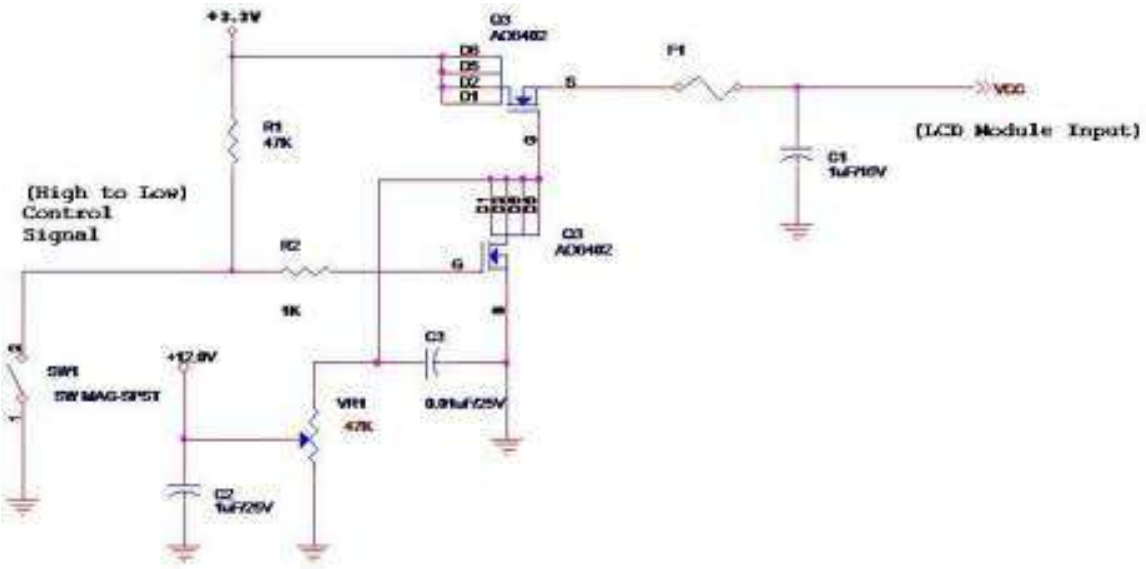
Input power specifications are as follows;

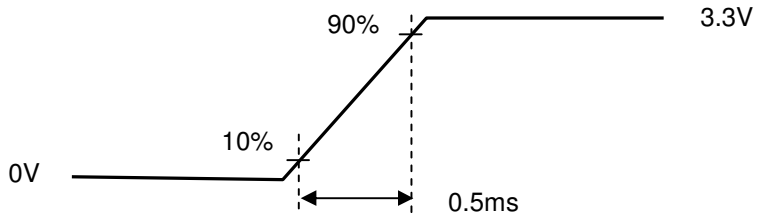
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.9	[Watt]	Note 1
IDD	IDD Current	-	-	300	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2：Measure Condition





Vin rising time

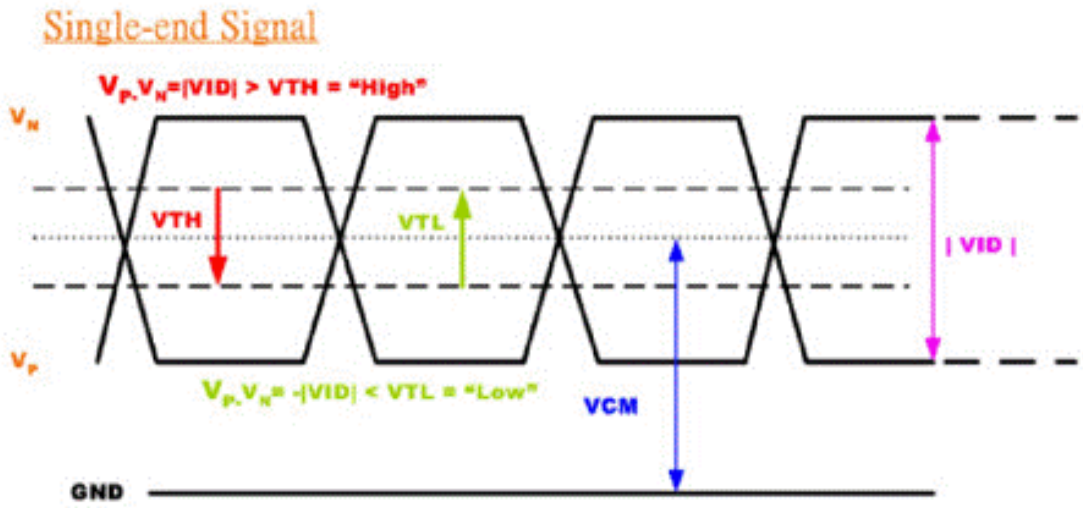
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical Characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{TH}	Differential Input High Threshold (Vcm=+1.2V)	---	100	[mV]
V_{TL}	Differential Input Low Threshold (Vcm=+1.2V)	-100	----	[mV]
$\|V_{ID}\|$	Differential Input Voltage	100	600	[mV]
V_{CM}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



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5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.5	[Watt]	(Ta=25℃), Note 1 Vin =3V
LED Life-Time	N/A	>15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=20mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Dist.ribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

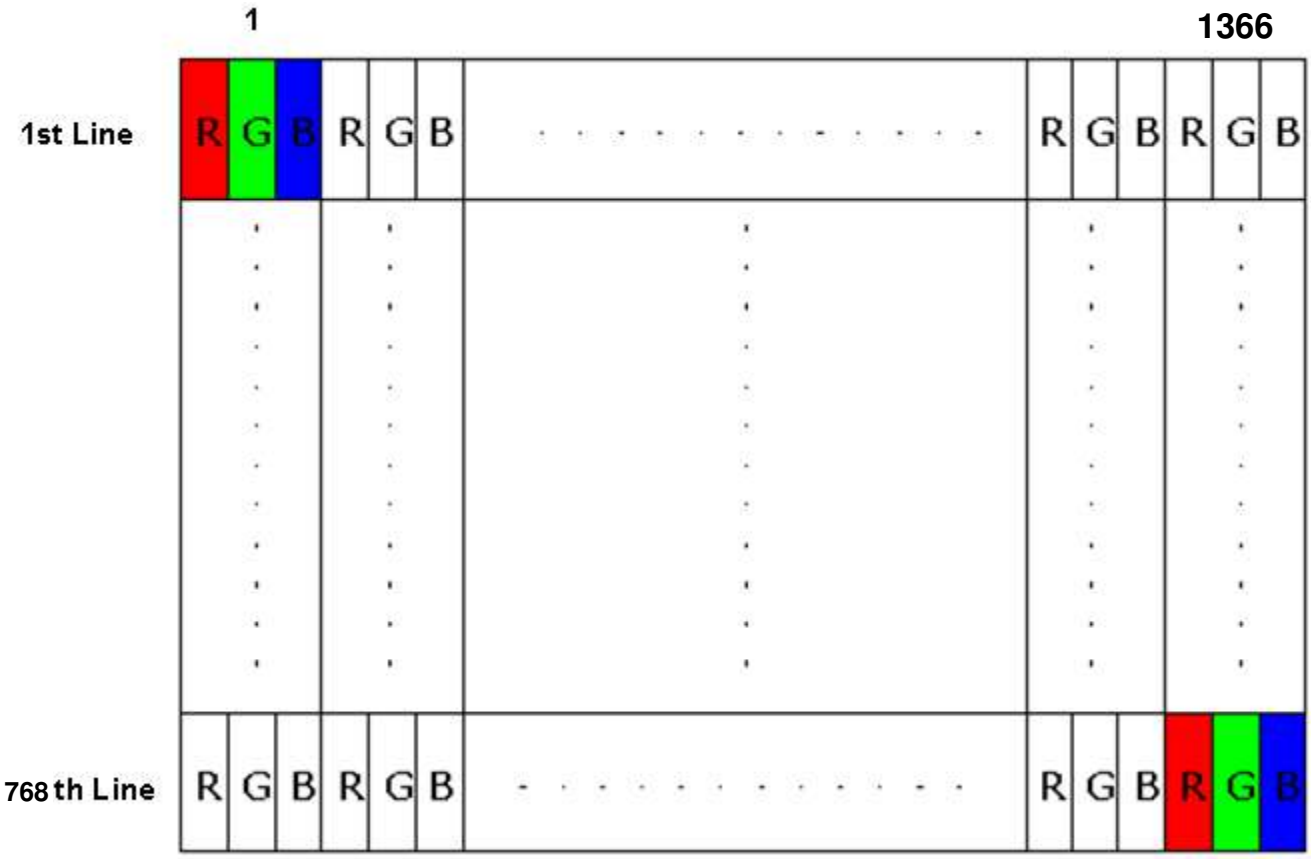
5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5	12.0	20.0	[Volt]	Define as Connector Interface (Ta=25℃)
PWM Logic Input High Level	VPWM_EN	2.5	3.3	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	200	1K	15K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	I-PEX
Type / Part Number	20455-040E-12R
Mating Housing/Part Number	20453-040T

6.2.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

No.	Pin Name	I/O	Power Rail	Description
1	NC			No Connection (Reserve)
2	VDD			Power Supply +3.3V
3	VDD			Power Supply +3.3V
4	VEDID			EDID +3.3V Power
5	AGING			Aging Mode Power Supply
6	CLK_EDID			EDID Clock Input (3.3V) note2
7	DAT_EDID			EDID Data Input (3.3V) note2
8	Rin0-			-LVDSdifferential data input(R0-R5,G0)
9	Rin0+			+LVDSdifferential data input(R0-R5,G0)
10	GND			Ground
11	Rin1-			-LVDSdifferential data input(G1-G5,B0-B1)
12	Rin1+			+LVDSdifferential data input(G1-G5,B0-B1)
13	GND			Ground
14	Rin2-			-LVDSdifferential data input(B2-B5,HS,VS,DE)
15	Rin2+			+LVDSdifferential data input(B2-B5,HS,VS,DE)
16	GND			Ground
17	ClkIN-			-LVDSdifferential clock input
18	ClkIN+			+LVDSdifferential clock input
19	NC			No Connection (Reserve)
20	NC			No Connection (Reserve)

21	NC			No Connection (Reserve)
22	GND			Ground–Shield
23	NC			No Connection (Reserve)
24	GND			Ground–Shield
25	NC			No Connection (Reserve)
26	GND			Ground–Shield
27	NC			No Connection (Reserve)
28	GND			Ground–Shield
29	NC			No Connection (Reserve)
30	NC			No Connection (Reserve)
31	VLED_GND			LED Ground
32	VLED_GND			LED Ground
33	VLED_GND			LED Ground
34	NC			No Connection (Reserve)
35	LED_PWM			System PWM Logic Input Level
36	VLED_EN			LED enable input level (2.5V Min)
37	CABC_EN			No Connection (Reserve)
38	VLED			LED Power Supply (5~20V)
39	VLED			LED Power Supply (5~20V)
40	VLED			LED Power Supply (5~20V)

6.3 Interface Timing

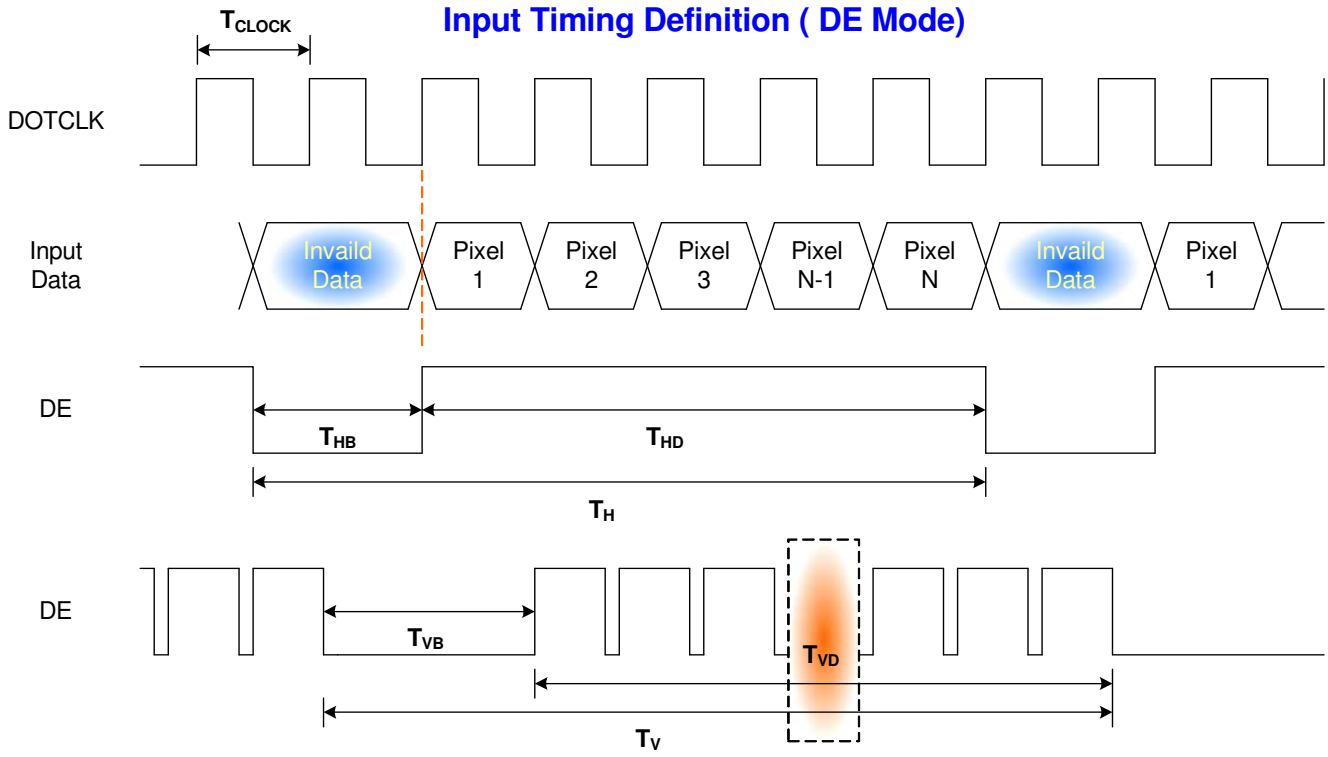
6.3.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T_{Clock}	67.69	76.3	87.41	MHz
Vertical Section	Period	T_V	778	**794**	813	T_{Line}
	Active	T_{VD}	768			
	Blanking	T_{VB}	10	**26**	45	
Horizontal Section	Period	T_H	1450	**1600**	1792	T_{Clock}
	Active	T_{HD}	1366			
	Blanking	T_{HB}	84	**234**	426	

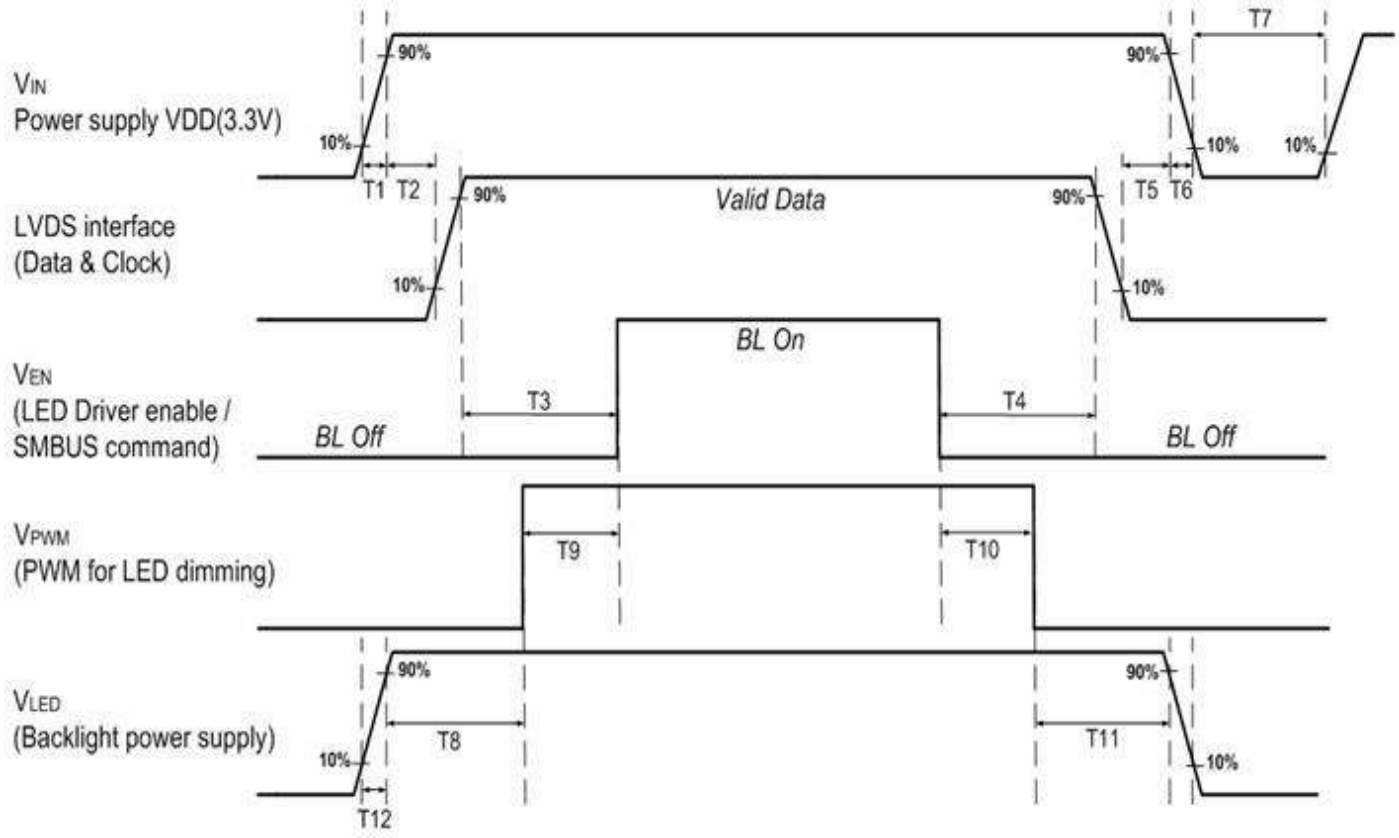
Note : DE mode only

6.3.2 Timing diagram



6.4 Power On Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Parameter	Value	
	Min.(ms)	Max.(ms)
T1	0.5	10
T2	0	50
T3	200	-
T4	200	-
T5	0	50
T6	0	10
T7	500	-
T8	10	-
T9	10	180
T10	10	180
T11	10	-
T12	0.5	10

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 300h	
Low Temperature Storage	Ta= -20℃, 300h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

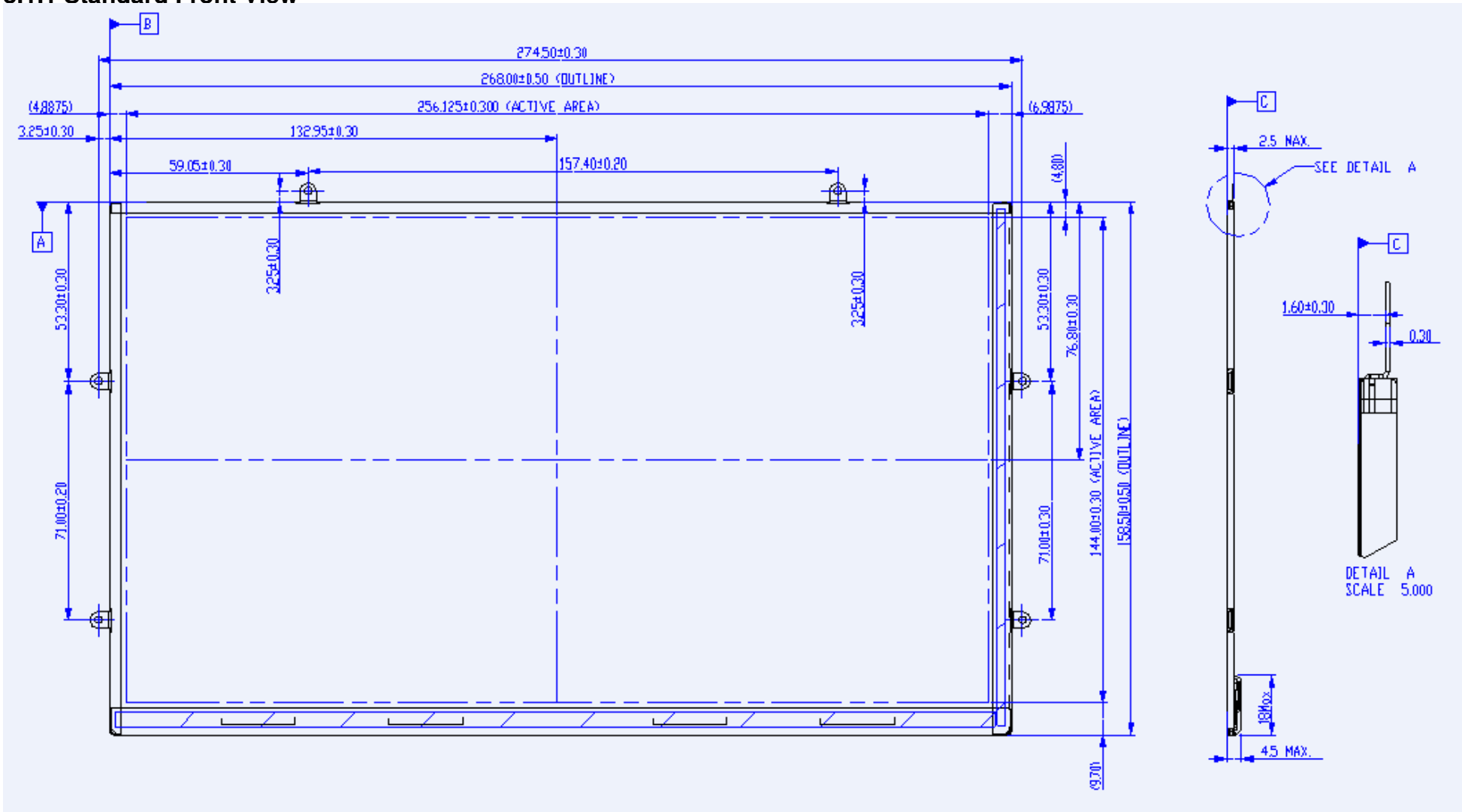
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

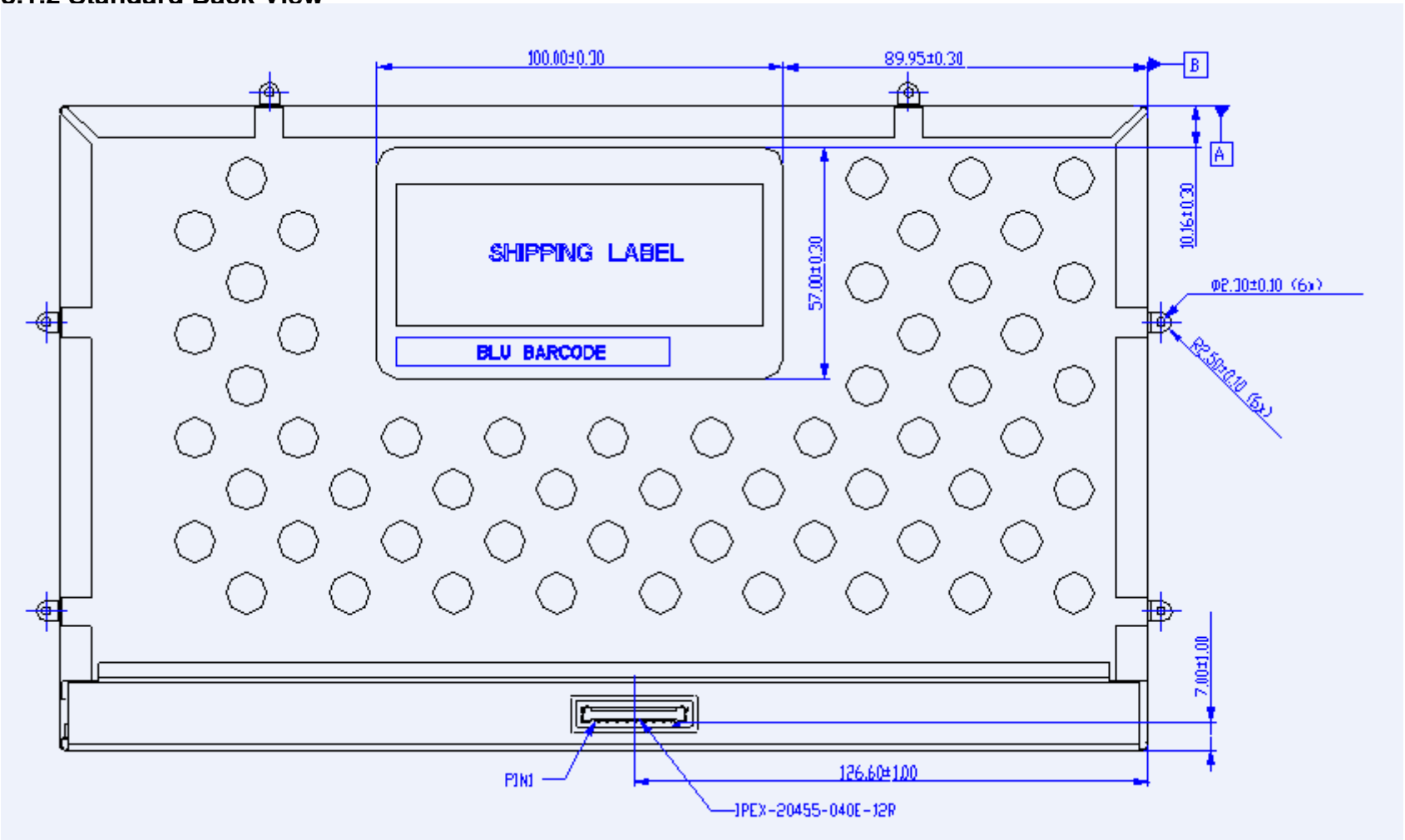
8. Mechanical Characteristics

8.1 Outline Dimension

8.1.1 Standard Front View



8.1.2 Standard Back View



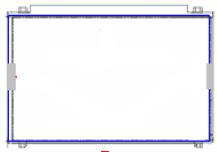
9. Shipping and Package

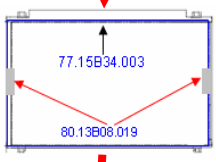
9.1 Shipping Label Format

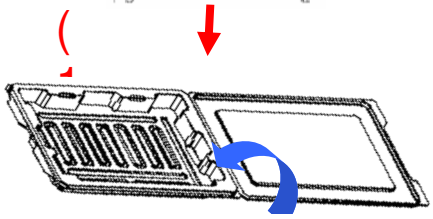
Shipping label

Carton Label

9.2 Carton Package



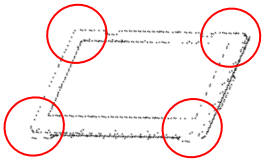




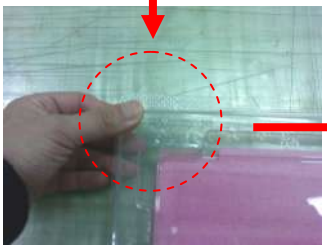
(2)

面板朝上先放入 1PCS SPACER 再放入 1PCS PANEL，共放入 4PCS PANEL ＋4PCS SPACER

將 TRAY BOX 上蓋蓋上

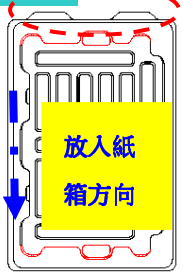


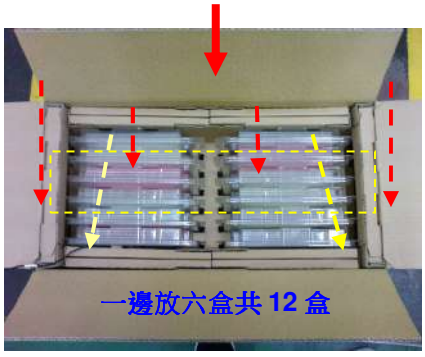
Check TRAY BOX
四周是否確實緊配合

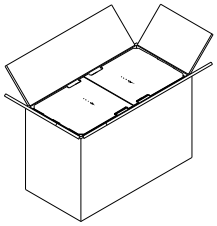


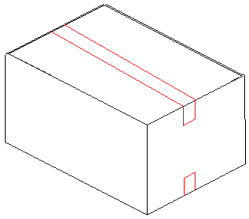
➢Tray Box 左右放置，面板面朝箭頭前方
➢面板可視區朝向紙箱折蓋（搖蓋）印有 AUO Logo 方向放置

TRAY BOX 字朝箭頭前

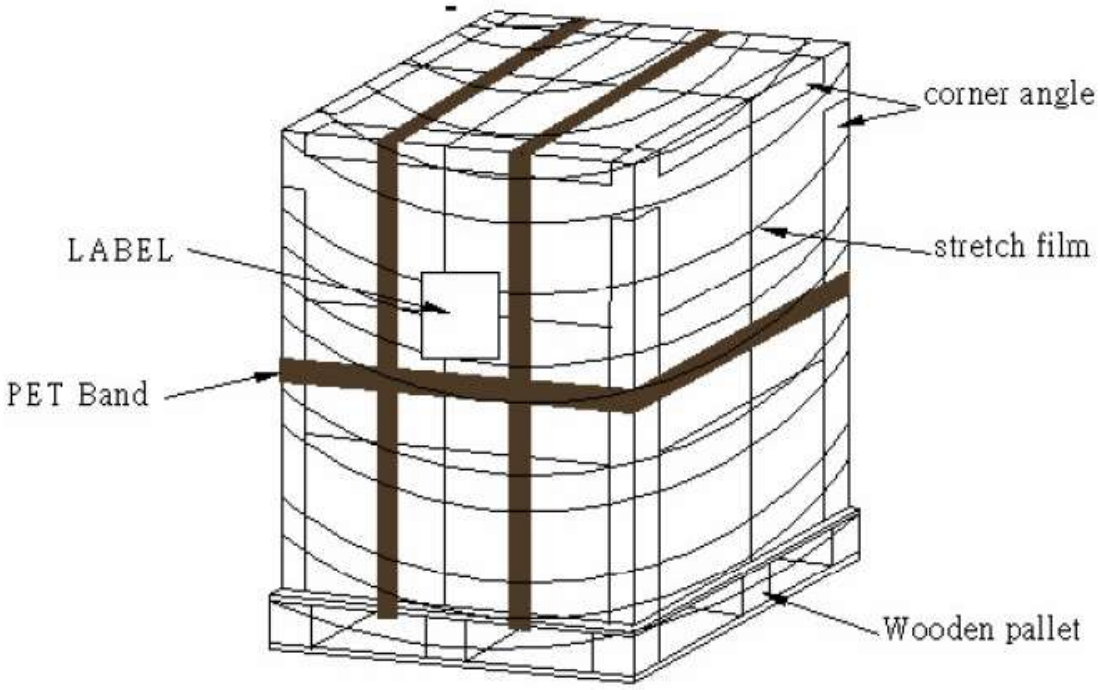








9.3 Shipping Package of Palletizing Sequence



10. Appendix

10.1 EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	5C	01011100	92	
0B	hex, LSB first	30	00110000	48	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	16	00010110	22	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	A0	10100000	160	
15	**Max H image size** *(rounded to cm)*	1A	00011010	26	
16	**Max V image size** *(rounded to cm)*	0E	00001110	14	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	99	10011001	153	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	85	10000101	133	
1B	Red x **(Upper 8 bits)**	95	10010101	149	
1C	Red y/ highER 8 bits	55	01010101	85	
1D	Green x	56	01010110	86	
1E	Green y	92	10010010	146	
1F	Blue x	28	00101000	40	
20	Blue y	22	00100010	34	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	

29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	CE	11001110	206	
37	Pixel Clock/10000 USB	1D	00011101	29	
38	Horz active **Lower 8bits**	56	01010110	86	
39	Horz blanking **Lower 8bits**	EA	11101010	234	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	50	01010000	80	
3B	Vertical Active **Lower 8bits**	00	00000000	0	
3C	Vertical Blanking **Lower 8bits**	1A	00011010	26	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30	00110000	48	
3E	HorzSync. Offset	28	00101000	40	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	36	00110110	54	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	00	00000000	0	
43	Vertical Image Size **Lower 8bits**	90	10010000	144	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Pixel Clock/10,000 (LSB)	DF	11011111	223	
49	Pixel Clock/10,000 (MSB)	13	00010011	19	40Hz frame rate
4A	Horizontal Addressable Pixels, lower 8 bits	56	01010110	86	
4B	Horizontal Blanking Pixels, lower 8 bits	EA	11101010	234	
4C	H Pixels, upper nibble : H Blanking, upper nibble	50	01010000	80	
4D	Vertical Addressable Lines, lower 8 bits	00	00000000	0	
4E	Vertical Blanking Lines, lower 8 bits	1A	00011010	26	
4F	V lines, upper nibble : V blanking, upper nibble	30	00110000	48	
50	Horizontal Front Porch, lower 8 bits	28	00101000	40	
51	Horizontal Sync Pulse, lower 8 bits	20	00100000	32	
52	V Front Porch, lower nibble : V Sync Pulse, lower nibble	36	00110110	54	
53	VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits	00	00000000	0	
54	Horizontal Image Size in mm, lower 8 bits	00	00000000	0	
55	Vertical Image Size in mm, lower 8 bits	90	10010000	144	

56	H Image Size, upper nibble : V Image Size, upper nibble	10	00010000	16	
57	Horizontal Border	00	00000000	0	
58	Vertical Border	00	00000000	0	
59	Bit Encode Sync Information	18	00011000	24	
5A	DC	00	00000000	0	
5B	HTOTAL	00	00000000	0	
5C	HA	00	00000000	0	
5D	HBL	00	00000000	0	
5E	HFP	00	00000000	0	
5F	HFPe	00	00000000	0	
60	HBP	00	00000000	0	
61	HB	00	00000000	0	
62	HSO	00	00000000	0	nVDPS Reserved 00
63	HS	00	00000000	0	
64	VTOTAL	00	00000000	0	
65	VA	00	00000000	0	
66	VBL	00	00000000	0	
67	VFP	00	00000000	0	
68	VBP	00	00000000	0	
69	VB	00	00000000	0	
6A	VSO	00	00000000	0	
6B	VS	00	00000000	0	
6C	Detail Timing Description #4	00	00000000	0	
6D	Flag	00	00000000	0	
6E	Reserved	00	00000000	0	
6F	For Brightness Table and Power Consumption	02	00000010	2	
70	Flag	00	00000000	0	Header
71	PWM % [7:0] @ Step 0	0C	00001100	12	
72	PWM % [7:0] @ Step 5	26	00100110	38	
73	PWM % [7:0] @ Step 10	E5	11100101	229	
74	Nits [7:0] @ Step 0	0A	00001010	10	
75	Nits [7:0] @ Step 5	3C	00111100	60	
76	Nits [7:0] @ Step 10	C8	11001000	200	Brightness Table
77	Panel Electronics Power @ 32x32 Chess Pattern =	10	00010000	16	
78	Backlight Power @ 60 nits =	09	00001001	9	
79	Backlight Power @ Step 10 =	1E	00011110	30	
7A	Nits @ 100% PWM Duty =	E1	11100001	225	Power Consumption
7B	Flag	20	00100000	32	
7C	Flag	20	00100000	32	
7D	Flag	20	00100000	32	
7E	Extension Flag	00	00000000	0	
7F	Checksum	DE	11011110	222	