Doc. Number:

☐ Tentative Specification
■ Preliminary Specification
☐ Final Specification

MODEL NO.: HJ070IA-02C

Customer: Standard Products

APPROVED BY   **SIGNATURE**

<u>Name / Title</u>
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Stanley CW Leung	Cosmo Zhou Green Fu	Jackie Fan

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
0.0	Jun,26th,2012	All	Spec Ver.0.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

HJ070IA-02C is a 7" (6.95" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 39 pins LVDS interface. This module supports 1280 x 800 WXGA mode.

1.2 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	6.95" diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1280 x R.G.B. x 800	pixel	-
Pixel Pitch	0.117 (H) x 0.117 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16777216 (8 bit)	color	-
Transmissive Mode	Normally Black	-	-
Surface Treatment	Hard coating (3H), Glare	-	-
Luminance, White	350	Cd/m2	-

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	160.8	161	161.2	mm	
	Vertical (V)	106.8	107	107.2	mm	(1)
	Thickness_ Top (T)	-	2.5	2.7	mm	
	Thickness_ Bottom (T)	-	4.26	4.46	mm	
	Thickness_ Bottom w/ Label(T)		4.39	4.59		
Bezel Area	Horizontal	151.46	151.76	152.06	mm	
	Vertical	95.3	95.6	95.9	mm	
Active Area	Horizontal	149.46	149.76	150.06	mm	
	Vertical	93.3	93.6	93.9	mm	
Weight		-	85	95	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE
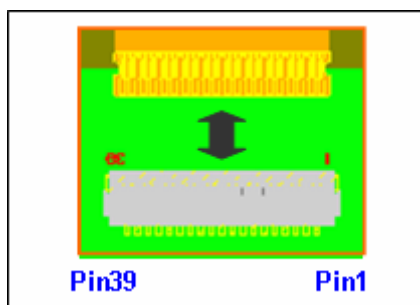
Please refer Appendix Outline Drawing for detail design.

User's connector Part No: FCI-10064555-392120HLF or equivalent.

3. ABSOLUTE MAXIMUM RATINGS
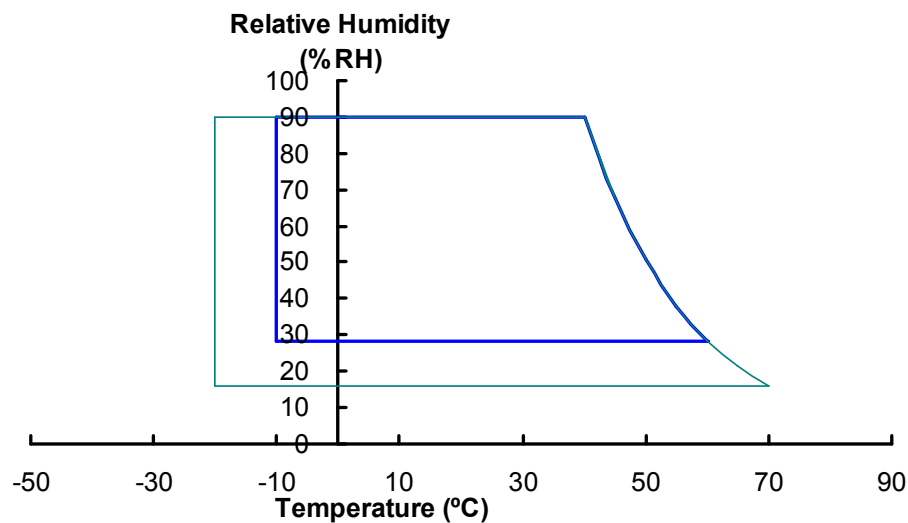
3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value Min.	Value Max.	Unit	Note
Storage Temperature	T_{ST}	-20	+70	ºC	(1)
Operating Ambient Temperature	T_{OP}	-10	+60	ºC	(1), (2)

Note (1)　　(a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2)　　The temperature of panel surface should be -10 ºC min. and 70 ºC max.

Relative Humidity (%RH)

[Graph: Relative Humidity (%RH) vs Temperature (ºC). Y-axis 0 to 100. X-axis -50 to 90. Curve at 90%RH constant until 40ºC then declining; lower boundary at 30%RH declining from 60ºC.]

3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Value Min.	Value Typ	Value Max.	Unit	Note
Driver Digital Power	VCCS	-0.3	-	5	V	(1)
Data Driver Analog power	AVDD	-0.5	-	15	V	(1)
TFT Turn-on Voltage	VGG	-0.3	-	40	V	(1)
TFT Turn-off Voltage	VEE	-20	-	0.3	V	(1)
Supply range, VGG-VEE	VGG-VEE	-0.3	-	40	V	(1)
Digital Input Voltage	Vi	-0.3	-	4	V	(1)
VCOM Voltage	VCOM	-	(4)	-	V	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM
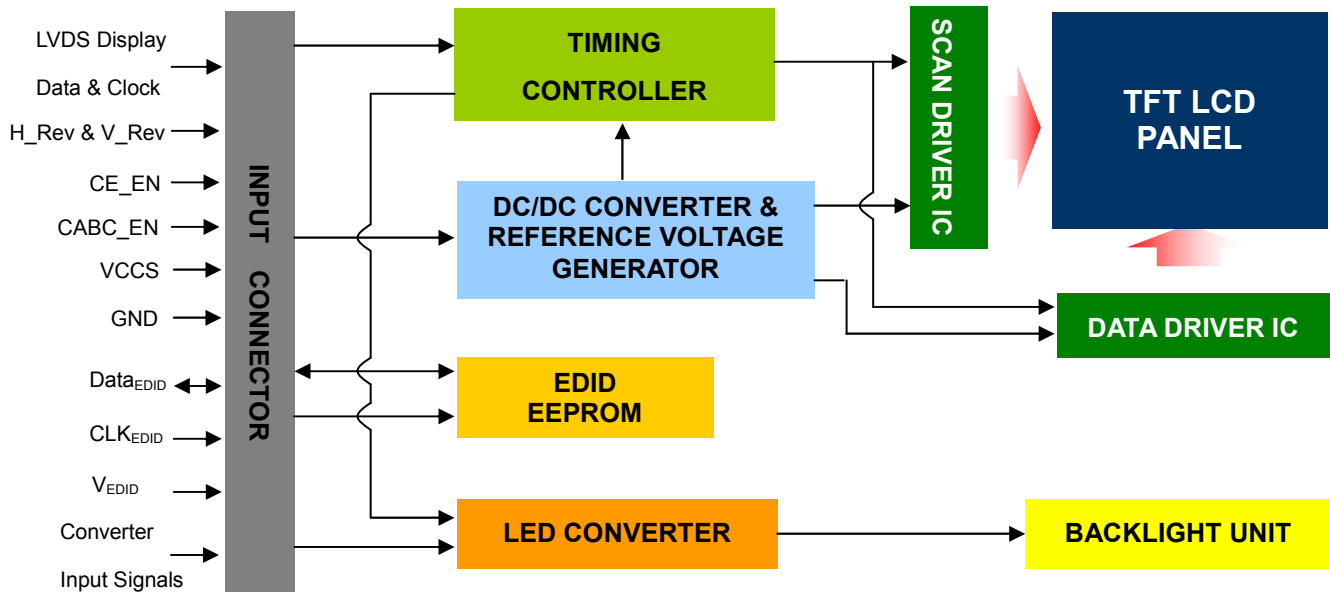
4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

| Pin	Symbol	Description	Remark
1	VCCS	Power Supply (3.3V typ.)	
2	VCCS	Power Supply (3.3V typ.)	
3	VEDID	DDC 3.3V power	
4	NC	No Connection (Reserved for CMI test)	
5	CLKEDID	DDC clock	
6	DATAEDID	DDC data	
7	Rxin0-	LVDS differential data input	R0-R5, G0
8	Rxin0+	LVDS differential data input	
9	VSS	Ground	
10	Rxin1-	LVDS differential data input	G1~G5, B0, B1
11	Rxin1+	LVDS differential data input	
12	VSS	Ground	
13	Rxin2-	LVDS Differential Data Input	B2-B5,HS,VS, DE
14	Rxin2+	LVDS Differential Data Input	
15	VSS	Ground	
16	RxCLK-	LVDS differential clock input	LVDS CLK
17	RxCLK+	LVDS differential clock input	
18	VSS	Ground	
19	Rxin3-	LVDS Differential Data Input	R[6], R[7], G[6], G[7], B[6], B[7]
20	Rxin3+	LVDS Differential Data Input	
21	VSS	Ground	
22	CE_EN	Color Engine Function Enable	(3)
23	NC	No Connection (Reserve)	

24	VSS	Ground	
25	NC	No Connection (Reserve)	
26	NC	No Connection (Reserve)	
27	VSS	Ground	
28	H_Rev	Reverse Scanning Display in Horizontal	(2)
29	V_Rev	Reverse Scanning Display in Vertical	(2)
30	LED_GND	LED Ground	
31	LED_GND	LED Ground	
32	LED_GND	LED Ground	
33	NC	No Connection (Reserve)	
34	LED_PWM	PWM Control Signal of LED Converter	
35	LED_EN	Enable Control Signal of LED Converter	(3)
36	CABC_EN	CABC Enable Input	(3)
37	LED_VCCS	LED Power Supply	
38	LED_VCCS	LED Power Supply	
39	LED_VCCS	LED Power Supply	

Note (1) The first pixel is odd as shown in the following figure.
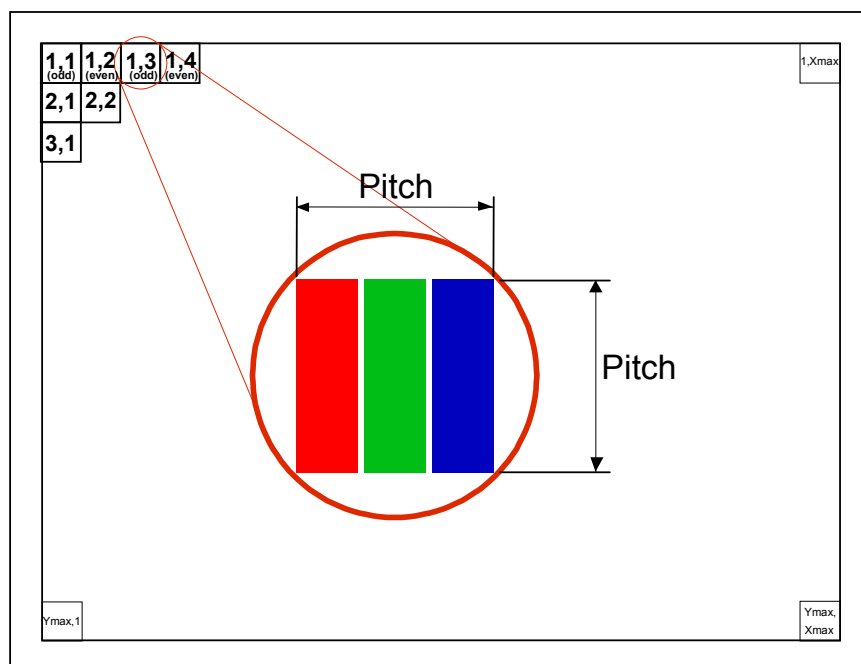
Note (2) The scanning display setting of H_Rev and V_Rev function are as follows.

Pin	Hi	Lo or Open
H_Rev	From Right to Left in Horizontal	From Left to Right in Horizontal
V_Rev	From Bottom to Top in Vertical	From Top to Bottom in Vertical

Hi = High level, Lo = Low level.

Note (3) The setting of CE/CABC function are as follows.

Pin	Enable	Disable
CE_EN	Hi	Lo or Open
LED_EN	Hi	Lo or Open
CABC_EN	Hi	Lo or Open

Hi = High level, Lo = Low level.

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)-
Ripple Voltage		V_{RP}	-	50	-	mV	(1)-
CABC_EN, CE_EN H_Rev, V_Rev Input Voltage	High Level	V_{IH}	(2.3)	-	(3.6)	V	
	Low Level	V_{IL}	(0)	-	(0.5)	V	
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	Icc	-	(249)	(272)	mA	(3)a
	White		-	(273)	(300)	mA	(3)b

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.
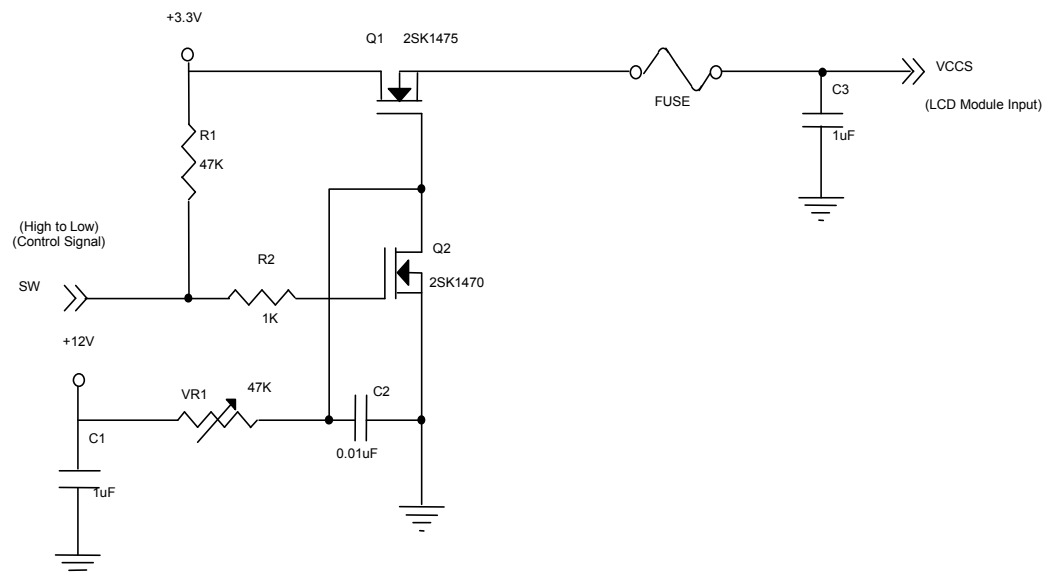
VCCS rising time is 0.5ms

Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ℃, DC

Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern
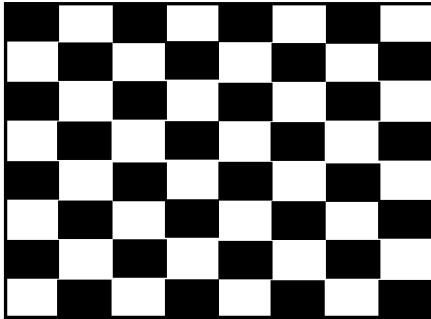
b. White Pattern

Active Area

Active Area

4.3.2 LED CONVERTER SPECIFICATION

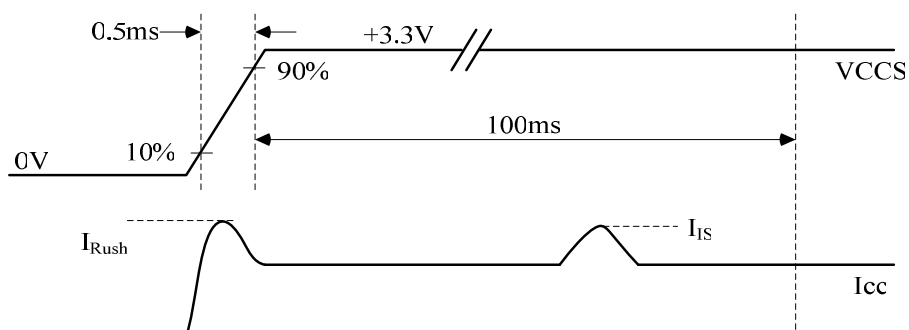| Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	(6.0)	(12.0)	(21.0)	V	
Converter Inrush Current		ILED$_{RUSH}$	-	-	(1.5)	A	(1)
EN Control Level	Backlight On		(2.3)	-	(5.0)	V	
	Backlight Off		0	-	(0.5)	V	
PWM Control Level	PWM High Level		(2.3)	-	(5.0)	V	
	PWM Low Level		0	-	(0.5)	V	
PWM Control Duty Ratio			(10)	-	100	%	
PWM Control Permissive Ripple Voltage		VPWM_pp	-	-	100	mV	
PWM Control Frequency		f$_{PWM}$	(190)	-	(20K)	Hz	(2)
LED Power Current LED_VCCS =Typ.		ILED	(83)	(104)	(125)	mA	(3)

Note (1) ILED$_{RUSH}$: the maximum current when LED_VCCS is rising,

ILED$_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 °C, f$_{PWM}$ = 200 Hz, Duty=100%.
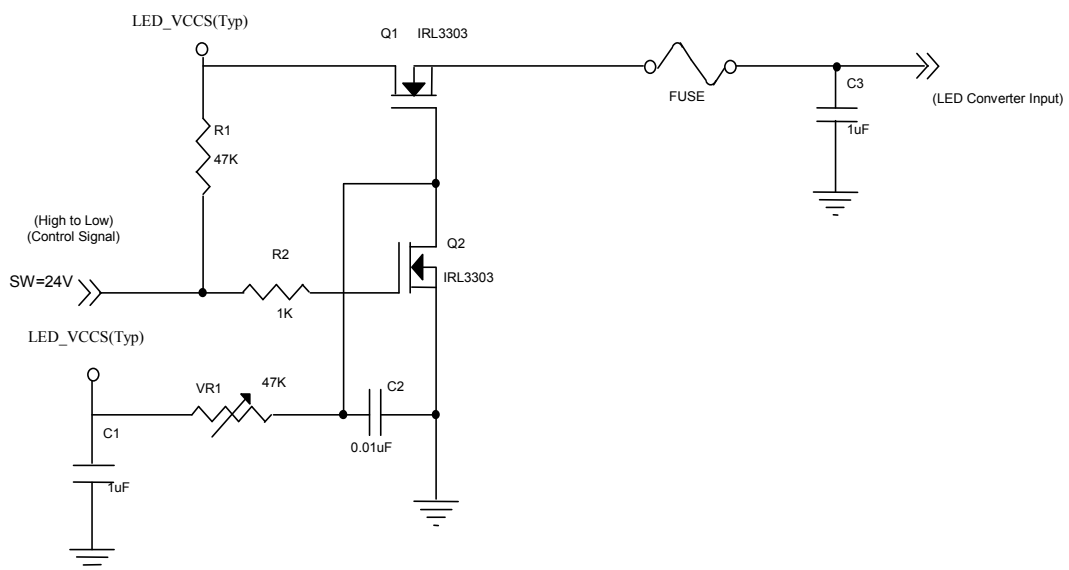
VLED rising time is 0.5ms
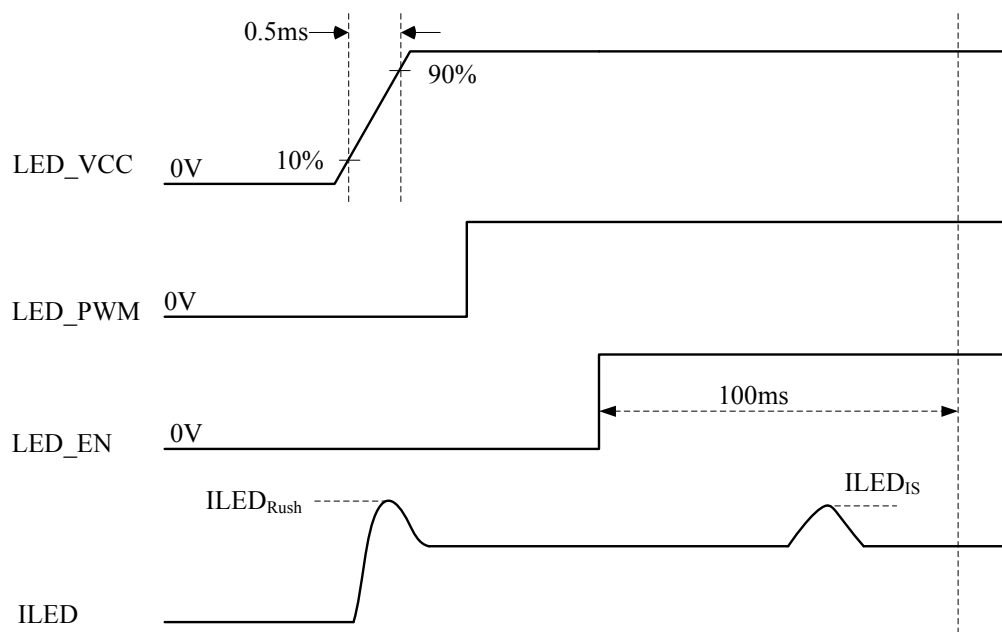
Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

$$N : \text{Integer} \quad (N \geq 3)$$

$$f : \text{Frame rate}$$

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ℃

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	22.5	26.1	27	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	38	40	42	mA	
Power Consumption	P_L	0.86	1.04	1.13	W	(3)
LED Life Time	L_{BL}	12000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :

V_L, I_L

LED
Light Bar

Light Bar Feedback
Channels
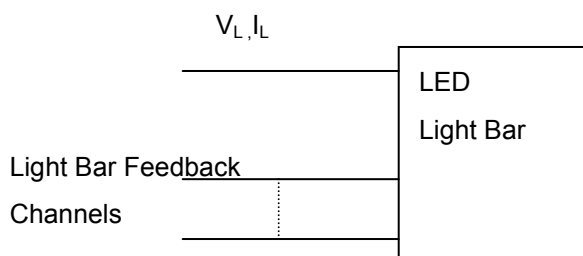
Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 ℃ and I_L = 20 mA(Per EA) until the brightness becomes $\cong$ 50% of its original value.

4.4 LVDS INPUT SIGNAL TIMING SPECIFICATIONS

4.4.1 LVDS DC SPECIFICATIONS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LVDS Differential Input High Threshold	$V_{TH(LVDS)}$	-	-	+100	mV	(1), V_{CM}=1.2V
LVDS Differential Input Low Threshold	$V_{TL(LVDS)}$	-100	-	-	mV	(1) V_{CM}=1.2V
LVDS Common Mode Voltage	V_{CM}	1.125	-	1.375	V	(1)
LVDS Differential Input Voltage	$|V_{ID}|$	100	-	600	mV	(1)
LVDS Terminating Resistor	R_T	-	100	-	Ohm	-

Note (1) The parameters of LVDS signals are defined as the following figures.

4.4.2 LVDS DATA FORMAT

Rxin3	IN27	IN26	IN25	IN24	IN23	IN22	IN21
	---	B7	B6	G7	G6	R7	R6
Rxin2	IN20	IN19	IN18	IN17	IN16	IN15	IN14
	DE	Vsync	Hsync	B5	B4	B3	B2
Rxin1	IN13	IN12	IN11	IN10	IN9	IN8	IN7
	B1	B0	G5	G4	G3	G2	G1
Rxin0	IN6	IN5	IN4	IN3	IN2	IN1	IN0
	G0	R5	R4	R3	R2	R1	R0

CLK+   T/7
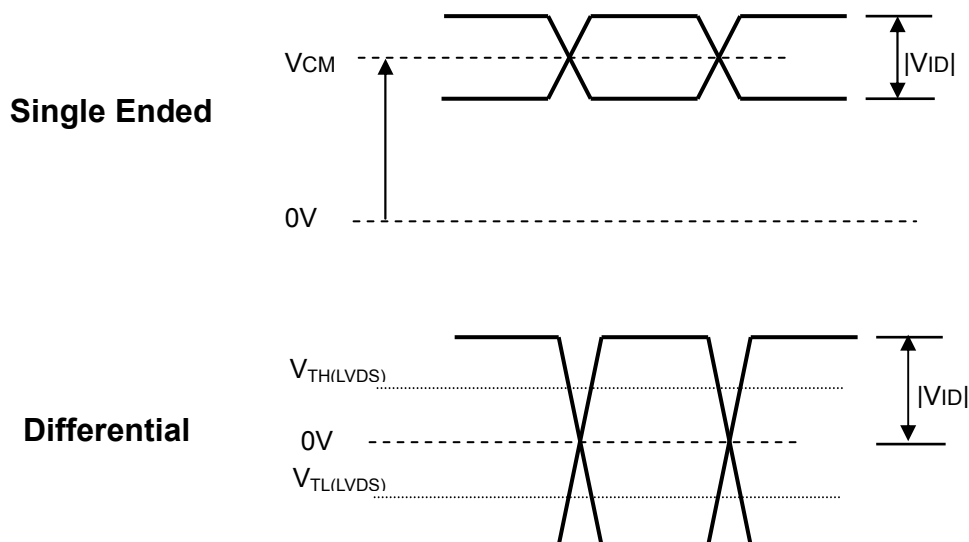
Signal for 1 DCLK Cycle (T)
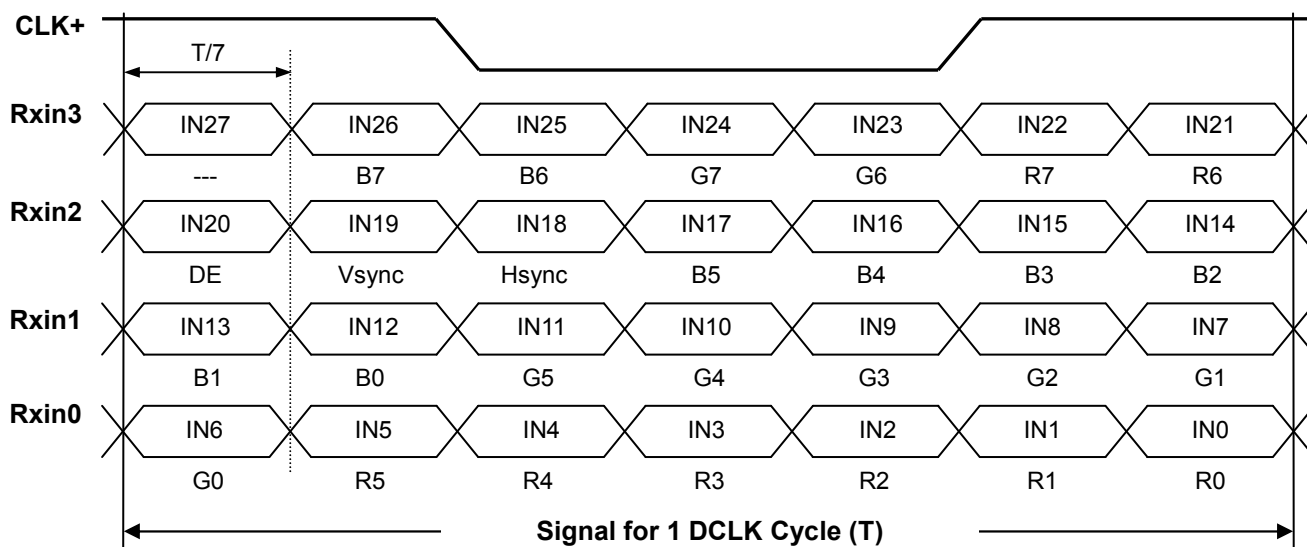
4.4.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R7	R6	…	R2	R1	R0	G7	G6	…	G2	G1	G0	B7	B6	…	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	(67.55)	(71.11)	(78.22)	MHz	-
DE	Vertical Total Time	TV	(813)	(823)	(833)	TH	-
	Vertical Active Display Period	TVD	800	800	800	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	(23)	TV-TVD	TH	-
	Horizontal Total Time	TH	(1410)	(1440)	(1470)	Tc	-
	Horizontal Active Display Period	THD	1280	1280	1280	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	(160)	TH-THD	Tc	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.
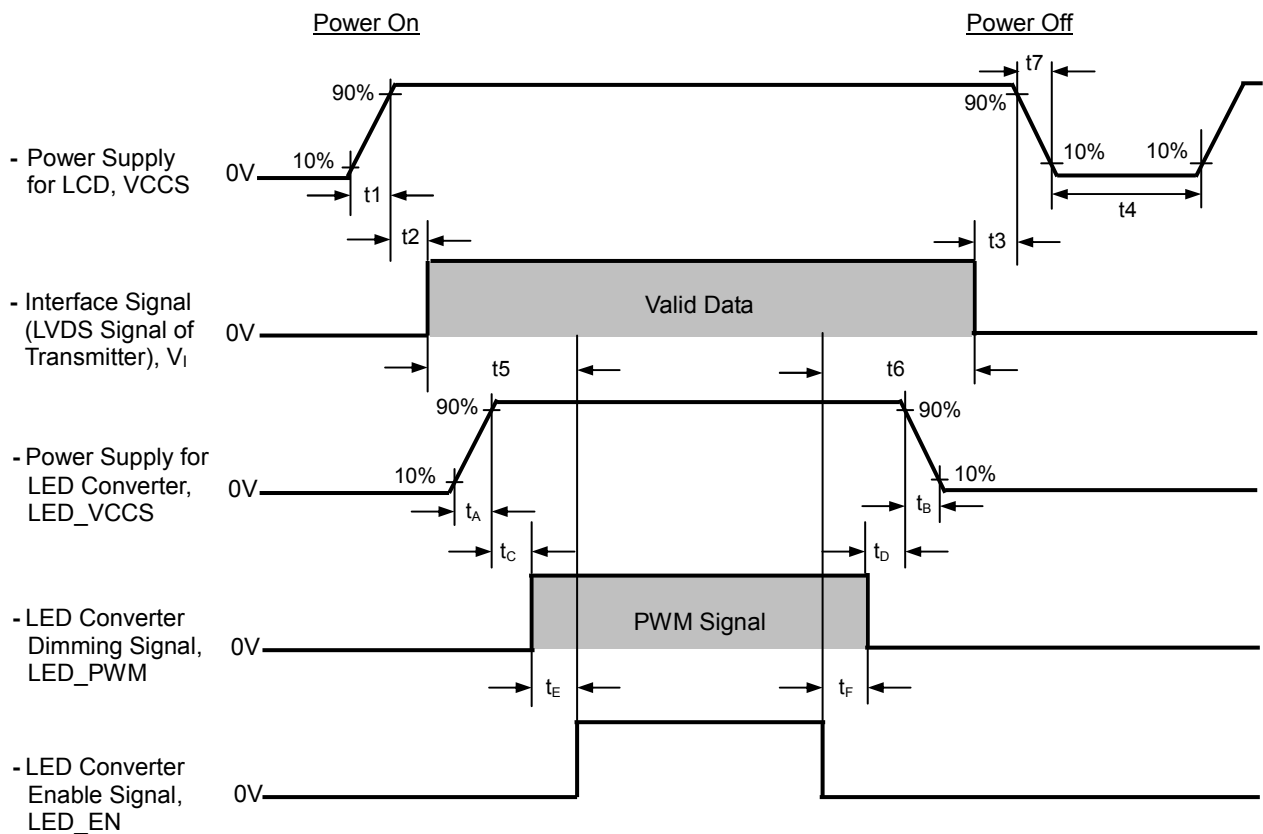
INPUT SIGNAL TIMING DIAGRAM
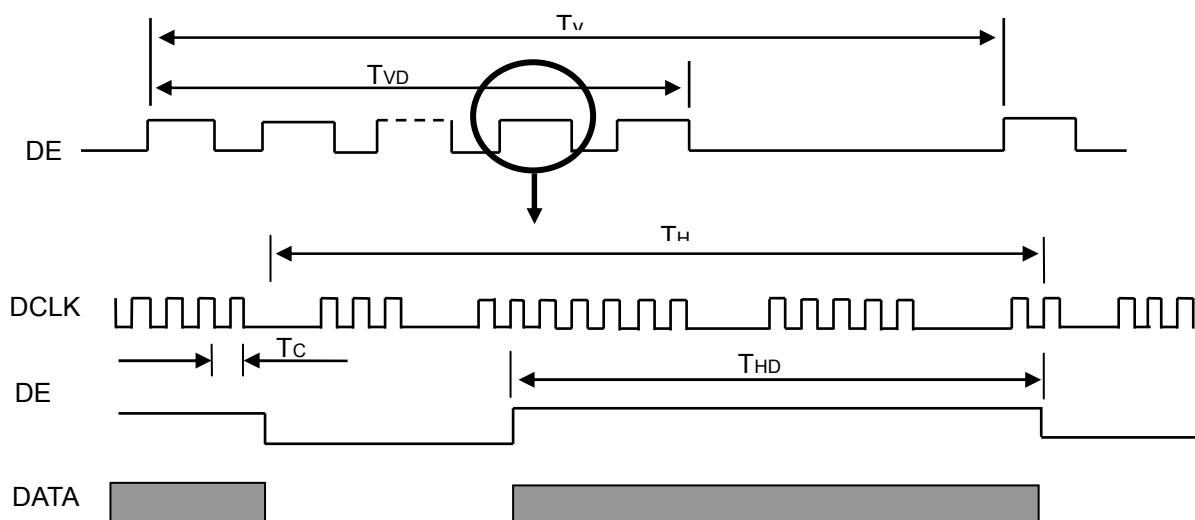
4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.

Symbol	Value			Unit	Note
	Min.	Typ.	Max.		
t1	0.5	-	10	ms	
t2	0	-	50	ms	
t3	0	-	50	ms	
t4	500	-	-	ms	
t5	200	-	-	ms	
t6	200	-	-	ms	
t7	0.5	-	10	ms	
t_A	0.5	-	10	ms	
t_B	0	-	10	ms	
t_C	10	-	-	ms	
t_D	10	-	-	ms	
t_E	10	-	-	ms	
t_F	10	-	-	ms	

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) Please avoid floating state of the interface signal during signal invalid period.

Note (3) It is recommended that the backlight power must be turned on after the power supply for LCD and the interface signal is valid.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	40	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		600	800	-	-	(2),(5),(9)
Response Time		T_R		-	14	17	ms	(3),(9)
		T_F		-	11	14	ms	
Average Luminance of White		L_{AVE}		340	400	-	cd/m²	(4),(6),(9)
Color Chromaticity	Red	Rx	$\theta_x=0°$, $\theta_Y=0°$ Viewing Normal Angle	Typ - 0.03	0.596	Typ + 0.03	-	(1),(9)
		Ry			0.340		-	
	Green	Gx			0.305		-	
		Gy			0.568		-	
	Blue	Bx			0.147		-	
		By			0.120		-	
	White	Wx			(0.308)		-	
		Wy			(0.324)		-	
	Color Gamut	C.G		45	50	-	%	
Viewing Angle	Horizontal	θ_x+	CR≥10	80	89	-	Deg.	(1),(5),(9)
		θ_x-		80	89	-		
	Vertical	θ_Y+		80	89	-		
		θ_Y-		80	89	-		
Flicker		-	-	-	-	-30	dB	(7),(9)
Gamma		-	-	1.9	2.2	2.5	-	-
Crosstalk		△CT	-	-	1.08	1.10	-	(8),(9)
White Variation of 9 Points		δW_{9p}	$\theta_x=0°$, $\theta_Y=0°$	70	80	-	%	(5),(6),(9)

Note (1) Definition of Viewing Angle (θx, θy)
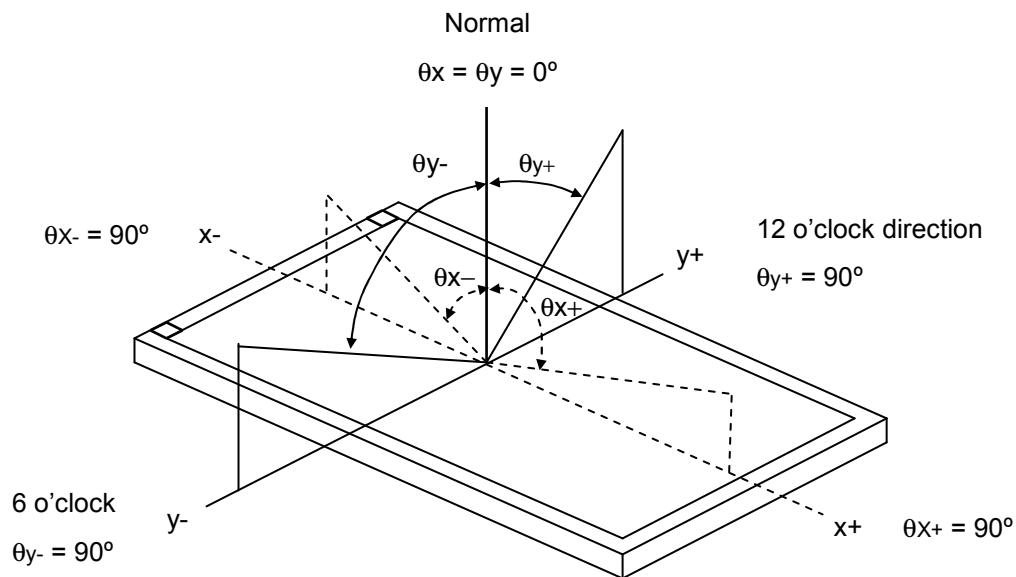
Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

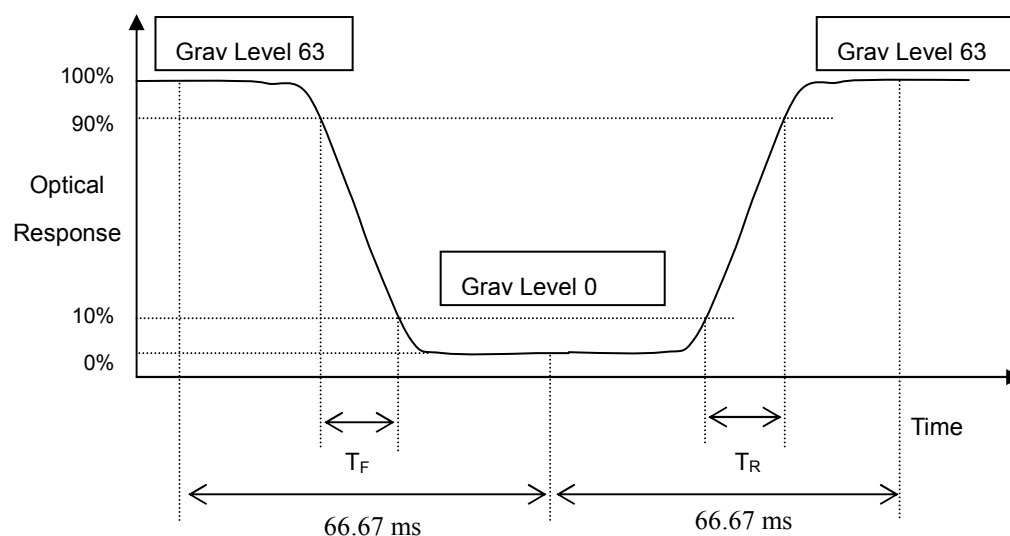L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):

Note (4) Definition of Average Luminance of White (L_{AVE}):

    Measure the luminance of gray level 63 at 5 points

        L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

    L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

    The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.
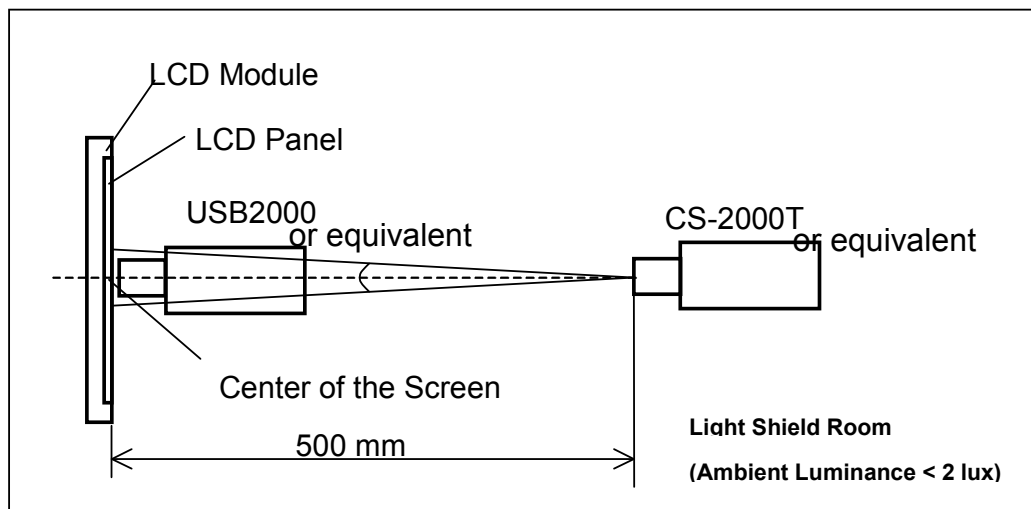
Note (6) Definition of White Variation (δW):

    Measure the luminance of gray level 63 at 9 points

    $δW_{9p}$ = {Minimum [L (1)+ L (6)+ L (7)+ L (8)+ L (9)+ L (10)+ L (11) +L (12) +L (13)] / Maximum [L (1)+ L (6)+ L (7)+ L (8)+ L (9)+ L (10)+ L (11) +L (12) +L (13)]}*100%
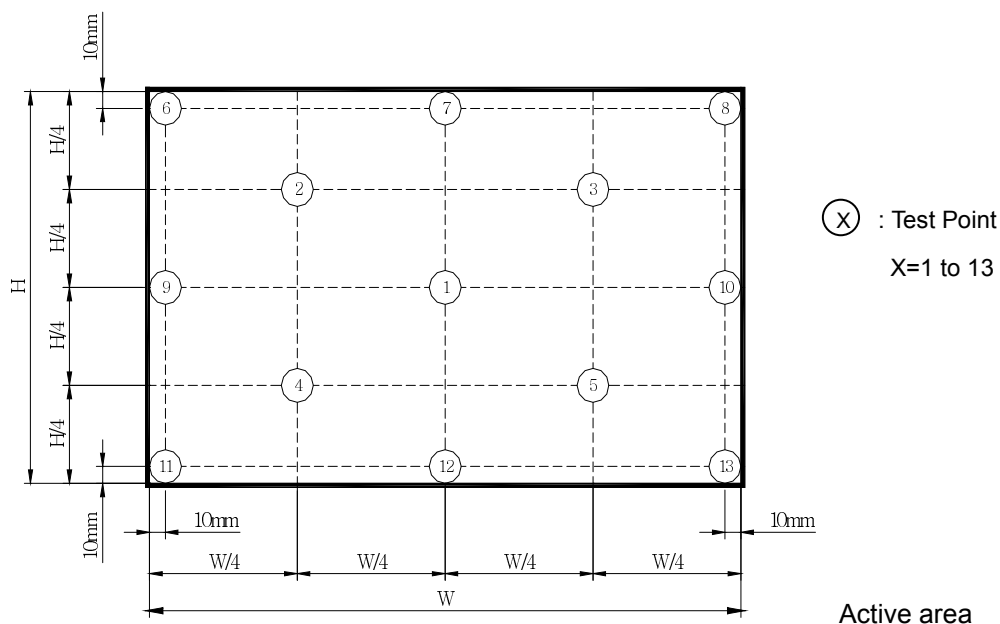
Note (7) Definition for Flicker:

    Measurement equipment: CA-210

    Measuring temperature: Ta=25℃ .

    Test method: JEITA method

    Test pattern: Refer to below (Test Pattern should be full-fill of display screen)
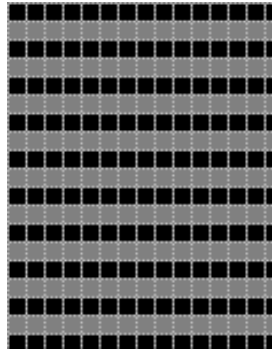
For Dot Inversion	For Line Inversion	For Frame Inversion
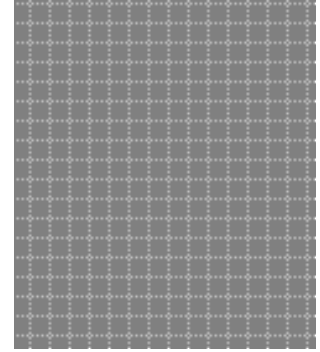
The point should be marked is, the background of Flicker Test Pattern-"gray " are defined as middle gray scale . For example, RGB 24bit "gray" defined as below:

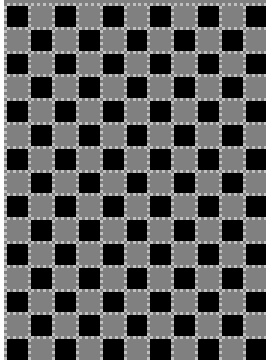| R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Frame Frequency Requirement before test：The LCD must be tuned to more than 65HZ before measurement .

Measurement Point: the center of display active area

Conversion of Flicker ratio:

    Flicker[dB] = 10xlog[Px/P0]

Where

    Px: Maximum power spectrum of AC component after passing through integrator

    P0: Power spectrum of DC component after passing through integrator

    AC component=b (Refer to below diagram)

    DC component=a (Refer to below diagram)

$$b: Vmax - Vmin$$

$$a: (Vmax + Vmin)/2$$

Vmin   Vmax

500mV   5ms
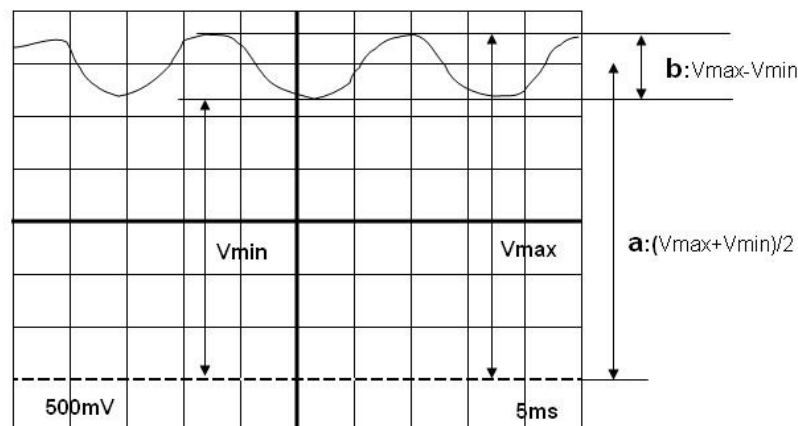
Note (8) Crosstalk

There should be no visible cross-talk in normal direction of the display when the "Cross-talk Test Pattern " below are loaded.

Measurement equipment：CS2000

The point should be marked is, the background of Cross-talk Test Pattern-"gray " are defined as middle gray scale . For example , 262K (RGB18bit) as below

R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1

$\triangle$Bpn = Bpn (gray) / Bpn (white)

Which n means the dot No. In the Cross-talk Test Pattern;

Bpn (gray) means the brightness of the No.n spots in Cross-talk Test Pattern;

Bpn (white) means the brightness of the No.n spots in Full white Test Pattern;

$\triangle$Bp (Max.) = Maximum value in $\triangle$Bp1~$\triangle$Bp9, except the No. 5 spot.

$\triangle$Bp (Min.) = Minimum value in $\triangle$Bp1~$\triangle$Bp9, except the No.5 spot.

$\triangle$CT=$\triangle$Bp (Max.)/ $\triangle$Bp(Min.).

$\triangle$CT must less than 1.10
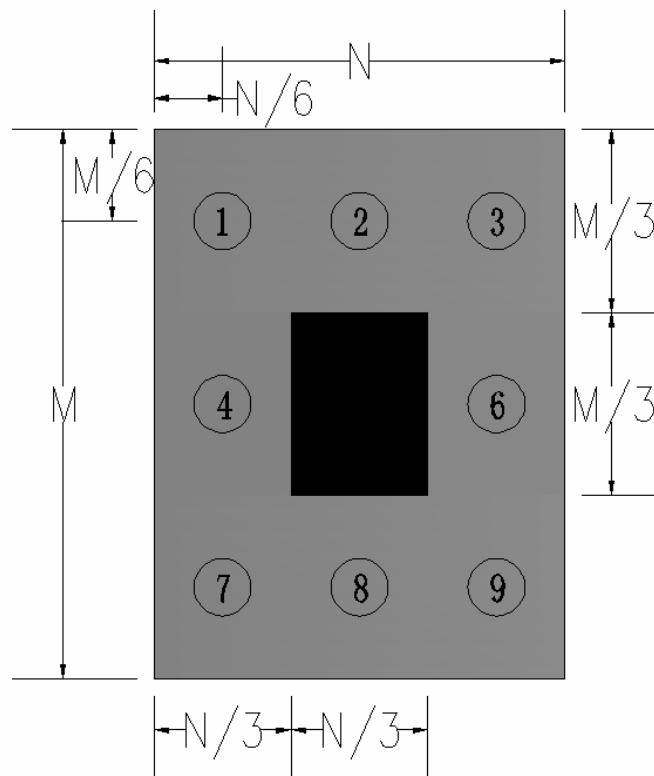
Cross-talk Test Pattern

Note(9) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	70ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour ⟷ 70℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	60ºC, 240 hours	
Low Temperature Operation Test	-10ºC, 240 hours	
High Temperature & High Humidity Operation Test	60ºC, 90%RH, 240hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	180G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 60 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) Criteria: Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

7.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N070ICG – LD1

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X X Y M D L N N N N

          Serial No.

          Product Line

          Year, Month, Date

          CMO Internal Use

          Revision

          CMO Internal Use
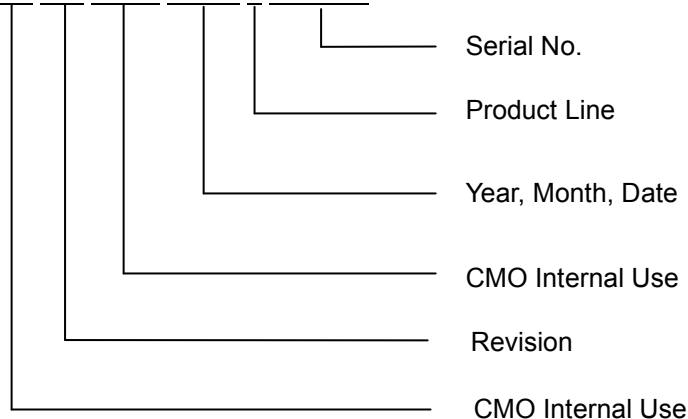
Serial ID includes the information as below:

  (a) Manufactured Date: Year: 0~9, for 2010~2019

          Month: 1~9, A~C, for Jan. ~ Dec.

          Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

  (b) Revision Code: cover all the change

  (c) Serial No.: Manufacturing sequence of product

  (d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

7.2 CARTON

Box Dimensions : 435(L)*350(W)*275(H)
Weight: Approx. 7.5kg(60 module .per. 1 box)
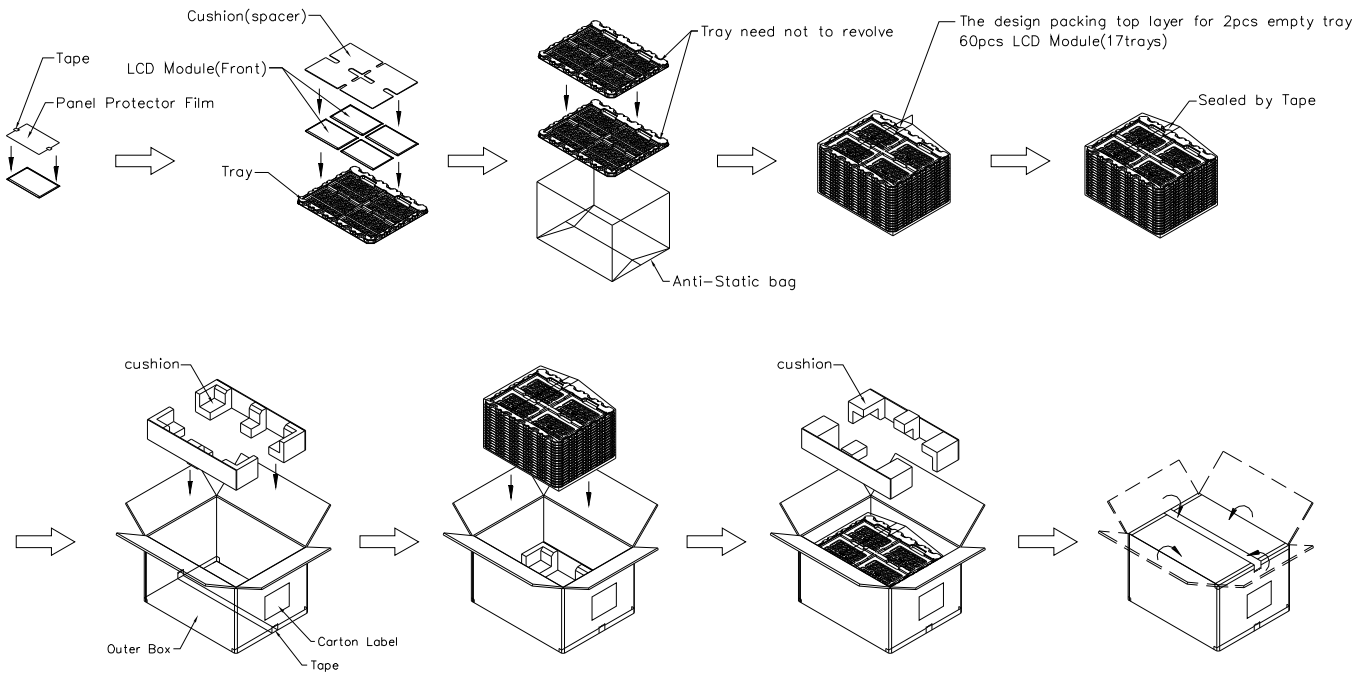
Figure. 7-2 Packing method

7.3 PALLET

Sea & Land Transportation
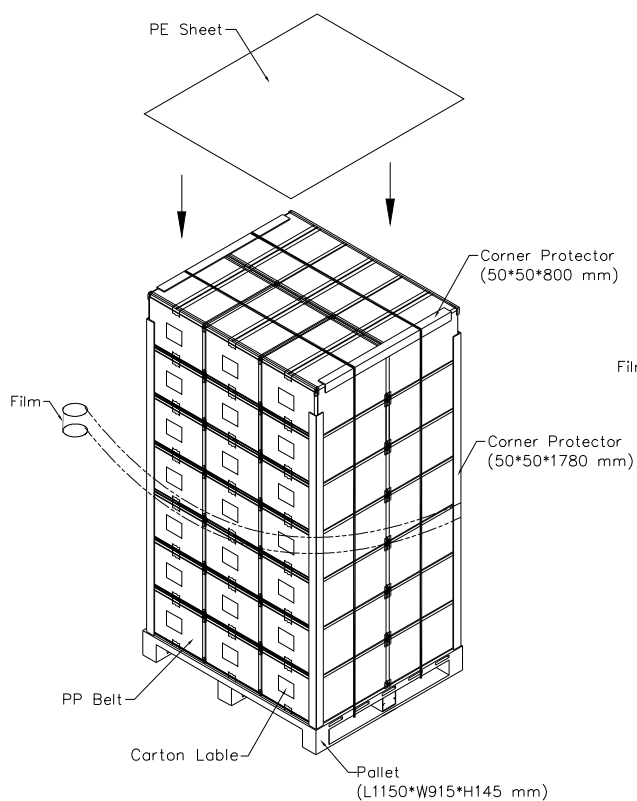
Air Transportation
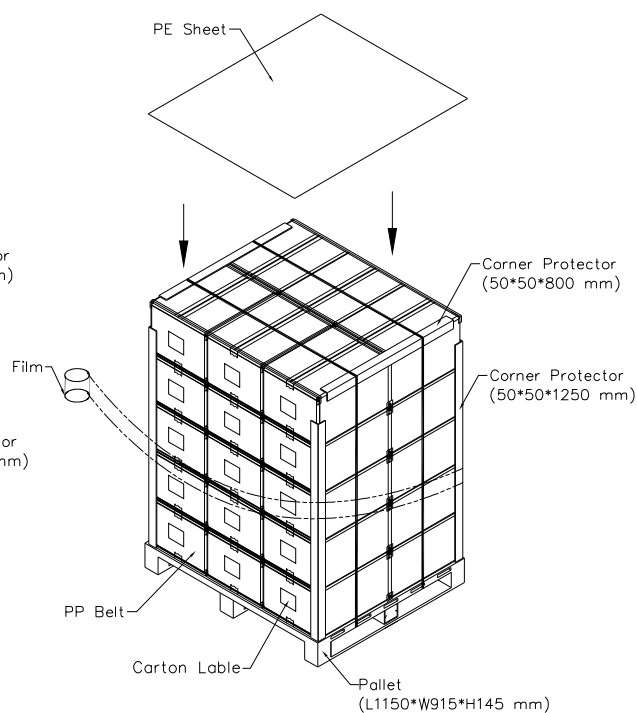
Figure. 7-3 Packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the

VESA Plug & Display and FPDI standards.

Byte #(decimal)	Byte #(hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMO")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N070ICG-LD1)	02	00000010
11	0B	ID product code (hex LSB first; N070ICG-LD1)	07	00000111
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	0E	00001110
17	11	Year of manufacture (fixed year code)	15	00010101
18	12	EDID structure version # ("1")	01	00000001
19	13	EDID revision # ("3")	03	00000011
20	14	Video I/P definition ("digital")	80	10000000
21	15	Max H image size ("15.0cm")	0F	00001111
22	16	Max V image size ("9.4cm")	09	00001001
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("Active off, RGB Color")	0A	00001010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	5B	01011011
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	00	00000000
27	1B	Rx=0.591	97	10010111
28	1C	Ry=0.341	57	01010111
29	1D	Gx=0.303	4D	01001101
30	1E	Gy=0.565	90	10010000
31	1F	Bx=0.146	25	00100101
32	20	By=0.117	1E	00011110
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("71.11MHz", According to VESA CVT Rev1.1)	C7	11000111
55	37	# 1 Pixel clock (hex LSB first)	1B	00011011
56	38	# 1 H active ("1280")	00	00000000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank ("1280 : 160")	50	01010000
59	3B	# 1 V active ("800")	20	00100000
60	3C	# 1 V blank ("23")	17	00010111
61	3D	# 1 V active : V blank ("800:23")	30	00110000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 6")	36	00110110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48 : 32 : 3 : 6")	00	00000000
66	42	# 1 H image size ("150 mm")	96	10010110
67	43	# 1 V image size ("94 mm")	5E	01011110
68	44	# 1 H image size : V image size ("150 : 94")	00	00000000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2 Pixel clock ("47.41MHz", According to VESA CVT Rev1.1)	85	10000101
73	49	# 2 Pixel clock (hex LSB first)	12	00010010
74	4A	# 2 H active ("1280")	00	00000000
75	4B	# 2 H blank ("160")	A0	10100000
76	4C	# 2 H active : H blank ("1280 : 160")	50	01010000
77	4D	# 2 V active ("800")	20	00100000
78	4E	# 2 V blank ("23")	17	00010111
79	4F	# 2 V active : V blank ("800:23")	30	00110000
80	50	# 2 H sync offset ("48")	30	00110000
81	51	# 2 H sync pulse width ("32")	20	00100000
82	52	# 2 V sync offset : V sync pulse width ("3 : 6")	36	00110110
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width ("48 : 32 : 3 : 6")	00	00000000
84	54	# 2 H image size ("150 mm")	96	10010110
85	55	# 2 V image size ("94 mm")	5E	01011110

86	56	# 2 H image size : V image size (”150 : 94”)	00	00000000
87	57	# 2 H boarder (”0”)	00	00000000
88	58	# 2 V boarder (”0”)	00	00000000
89	59	# 2 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Vendor “CMO”, ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 1st character of string (“C”)	43	01000011
96	60	# 3 2nd character of string (“M”)	4D	01001101
97	61	# 3 3rd character of string (“O”)	4F	01001111
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with “Blank” character	20	00100000
100	64	# 3 Padding with “Blank” character	20	00100000
101	65	# 3 Padding with “Blank” character	20	00100000
102	66	# 3 Padding with “Blank” character	20	00100000
103	67	# 3 Padding with “Blank” character	20	00100000
104	68	# 3 Padding with “Blank” character	20	00100000
105	69	# 3 Padding with “Blank” character	20	00100000
106	6A	# 3 Padding with “Blank” character	20	00100000
107	6B	# 3 Padding with “Blank” character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 FE (hex) defines ASCII string (Model Name“N070ICG-LD1”, ASCII)	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 1st character of name (“N”)	4E	01001110
114	72	# 4 2nd character of name (“0”)	30	00110000
115	73	# 4 3rd character of name (“7”)	37	00110111
116	74	# 4 4th character of name (“0”)	30	00110000
117	75	# 4 5th character of name (“I”)	49	01001001
118	76	# 4 6th character of name (“C”)	43	01000011
119	77	# 4 7th character of name (“G”)	47	01000111
120	78	# 4 8th character of name (“-”)	2D	00101101
121	79	# 4 9th character of name (“L”)	4C	01001100
122	7A	# 4 Ath character of name (“D”)	44	01000100
123	7B	# 4 Bth character of name (“1”)	31	00110001
124	7C	# 4 New line character indicates end of ASCII string	0A	00001010
125	7D	# 4 Padding with “Blank” character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	C3	11000011

Appendix. OUTLINE DRAWING

NOTES:
1. MODULE FLATNESS : 0.5mm MAX.
2. FPC INPUT CONNECTOR : FCI-10064555-392120HLF OR EQUIVALENT.
3. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT,
   NO OVERL APPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA,
   WLAN, WAM OR OTHER FOREIGN OBJECTS OVER TCON AND VR LOCATION.
4. FPC CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
5. "( )" MARKS THE REFERENCE DIMENSIONS.

TITLE	OUTLINE DRAWING N070ICG-LDI(801/811)			REV.	A
Approved	SHUNNAN	Drawing No.	N07064101A		
Checked	S.S. CHEN	Part No.	NA		
Drawer	K.S. LIN	Material	NA	Sheet 1 / 3	A2
Designer	K.S. LIN	Date 16-Feb-2011	Scale 1:1	Unit:mm	

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(29)(PCB WIDTH)

THICKNESS W/ MODULE LABEL IS MAX.1.459 MM

PIN 1   36.8±1

(2.69)

22.7±1

PCBA OUTLINE

(3.41)   (152.6)(PCB LENGTH)

TITLE	OUTLINE DRAWING N070ICG-LDI(801/811)			REV.	A
Approved	SHUNNAN	Drawing No.	N07064101A		
Checked	S.S. CHEN	Part No.	NA		
Drawer	K.S. LIN	Material	NA	Sheet 2 / 3	A2
Designer	K.S. LIN	Date 16-Feb-2011	Scale 1:1	Unit mm	

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Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

DRIVER IC, FPC, TCON, AND VR LOCATIONS
SEE NOTES FOR EXPLANATION

TITLE	OUTLINE DRAWING N070ICG-LDI(801/811)		REV.	A
Approved	SHUNNAN	Drawing No.	N07064101A	
Checked	S.S. CHEN	Part No.	NA	
Drawer	K.S. LIN	Material	NA	Sheet 3 / 3 A2
Designer	K.S. LIN	Date 16-Feb-2011	Scale 1:1	Unit:mm

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Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark