Chunghwa Picture Tubes, Ltd.
Technical Specification

To : **Studio Technology Co.,Ltd**
Date : October 15, 2004

TFT LCD
CLAA140WA01

ACCEPTED BY:

APPROVED BY	CHECKED BY	PREPARED BY
	Aurice	TFT-LCD Product Planning Management Division

Prepared by : TFT-LCD Product Planning Management Division

CHUNGHWA PICTUER TUBES, LTD.
1127 Hopin Rd., Padeh, Taoyuan, Taiwan 334, R.O.C.
TEL: +886-3-3675151 FAX: +886-3-377-3001

Doc.No:	**CLAA140WA01- STUDIO-V1-2004/10/15**	**Issue Date: 2004/10/15**

T- 3650002- 000- A
NEW

REVISION STATUS

Revision Notice	Description	Rev. Date
V1	First version	2004/10/15

1. OVERVIEW

CLAA140WA01(with LVDS interface) is 14" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel , driver ICs , control circuit , and backlight.

By applying 6 bits digital data, 1280×768, 262K color images are displayed on the 14" diagonal screen. Input power voltage is single 3.3V for LCD driving.

Inverter for backlight is not included in this module. General specifications are summarized in the following table:

ITEM	SPECIFICATION
Display Area(mm)	305.28(H) x 183.168(V) (14-inch diagonal)
Number of Pixels	1280 x 3(H) x 768(V)
Pixel Pitch(mm)	0.2385(H) x 0.2385(V)
Color Pixel Arrangement	RGB vertical stripe
Display Mode	normally white TN
Number of Colors	262144 colors
Optimum Viewing Angle	6 o'clock
Brightness(cd/m^2)	200(center);185(5 point),lamp current 6mA(typ)
Power consumption(W)	5.8W (typ)
Module Size(mm)	320x199x5.7(max)
Module Weight(g)	445(typ)
Backlight Unit	CCFL , 1 tube
Surface Treatment	Anti-Glare ; Hardness: 3H

[Note] :

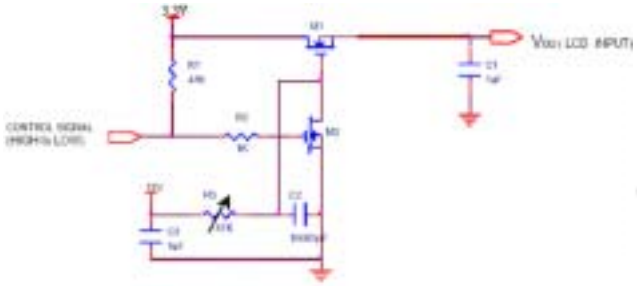
The LCD Products listed on this document are not suitable for use of aerospace equipment, submarine cables, nuclear reactor control system and life support systems. If customers intend to use these LCD products for above application or not listed in "Standard" as follows, please contact our sales people in advance.

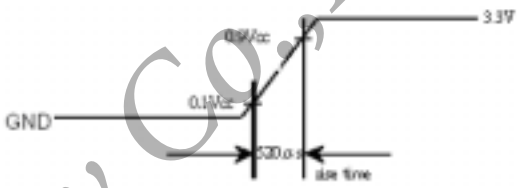
Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tool, Industrial robot, Audio and Visual equipment, Other consumer products.

2. ABSOLUTE MAXIMUM RATINGS

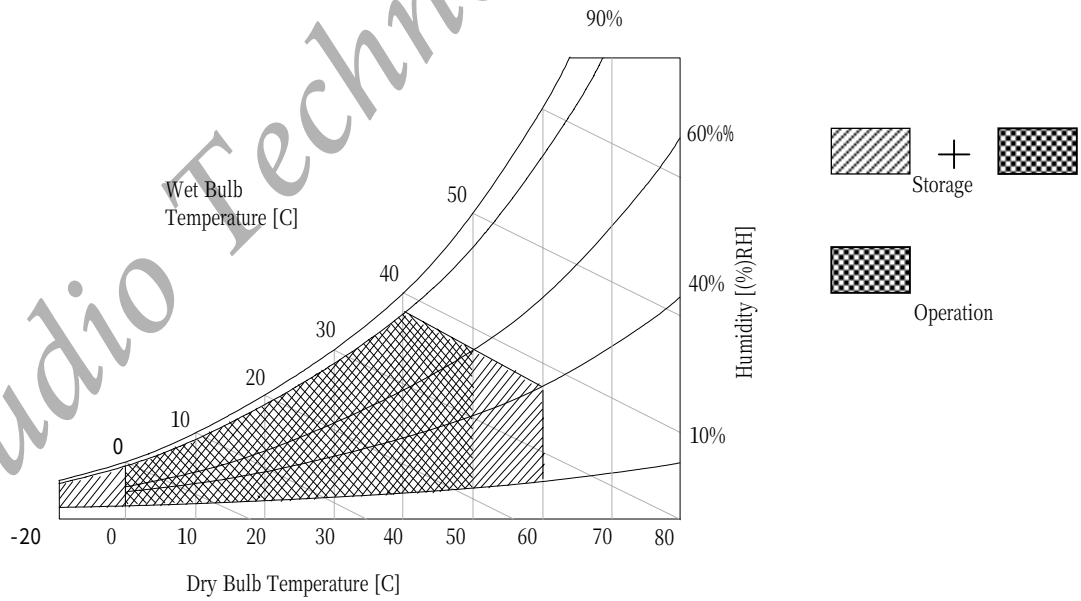
ITEM	SYMBOL	MIN.	MAX.	UNIT
Power Supply Voltage for LCD	VCC	-0.3	4.0	V
LVDS input Voltage	VIN	-0.3	VCC+0.3	V
Static Electricity *1)*	VESDt	-250	250	V
	VESDc	-15	15	KV
ICC Rush Current *2)*	I_{RUSH}		0.75	A
Operation Temperature *3)*	Top	0	50	℃
Storage Temperature *3)*	Tstg	-20	60	℃
Starting Lamp Voltage	V_{SL}	-	1420	V

[Note] ： *1) Test Condition: IEC 1000-4-2 ,
VESDt ：Contact discharge to input connector
VESDc：Contact discharge to module
*2) 4msec(measure with below circuit), If Vcc rise time increase then I_{RUSH} decrease.





*3) Humidity ≦85% RH. without condensation.



3. ELECTRICAL CHARACTERISTICS

(1)TFT-LCD Ta = 25°C

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	Remark
Power Supply Voltage for LCD		VCC	3.0	3.3	3.6	V	
Power Supply Current for LCD*1)		ICC	-	340	360	mA	
ICC Rush Current*2)		I_{RUSH}			0.5	A	
Logic input Voltage	Input Voltage	VIN	0	-	VCC	V	
	Common Mode Voltage	VCM	1.125	1.25	1.375	V	
	Differential Input Voltage	|VID|	250	350	450	mV	
	Threshold Voltage(High)	VTH	-	-	100	mV	When VCM = +1.2V
	Threshold Voltage(Low)	VTL	-100	-	-	mV	
Tolerance of VID		ΔVID	-	-	35	mV	
Tolerance of VCM		ΔVCM	-	-	35	mV	

[Note]：*1)Power Supply Current is in Gray-128 pattern and operation frequency is 68.25MHz.

*2)Vcc rise time is 520 μ sec

[Note 1]

VCC=3.3V

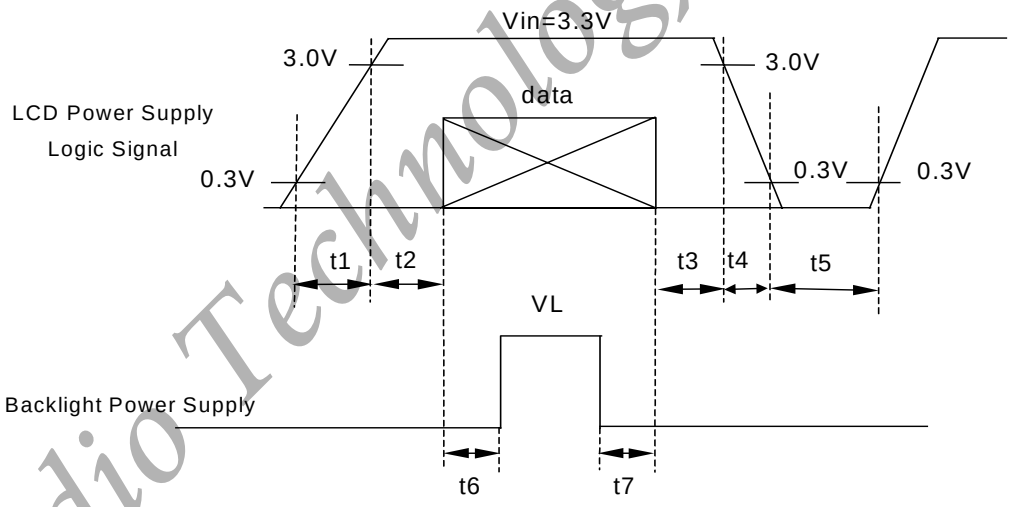
● VCC turn on conditions :

t1≦10ms　　1 sec≦t5

0.01 ms＜t2≦50 ms　　300 ms≦t6

0.01 ms＜t3≦50 ms　　300 ms≦t7

0.01 ms＜t4≦10 ms



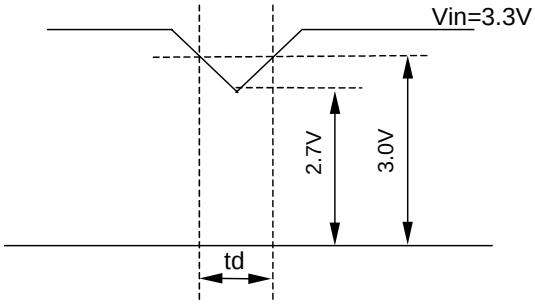
Data: RGB DATA, DCLK, HD, VD, DENA

● VCC dip conditions :

1) When 2.7V≦VCC<3.0V, td≦10 ms

2) When VCC<2.7V

VCC dip conditions should follow VCC turn on conditions.

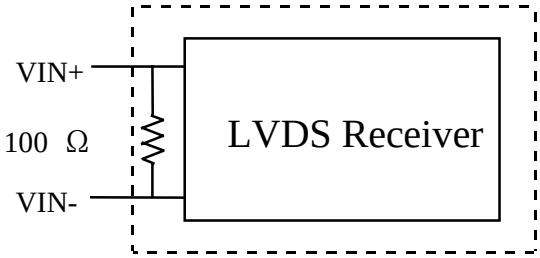


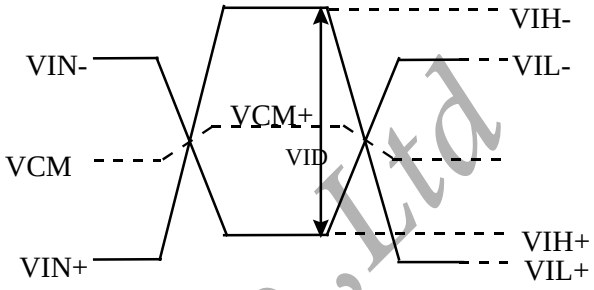
[Note 2]

- Typical value is measured when displaying horizontal gray scale line pattern
  64 gray level
  768 line mode
  VCC = +3.3V

[Note 3]

- LVDS Signal definition :





VID = VIN_+ - VIN-
△VCM = | VCM_+ - VCM- |
△VID = | VID_+ - VID- |
VID_+ = | VIH_+ - VIH- |
VID- = | VIL_+ - VIL- |
VCM = (VIN_+ - VIN-) / 2
VCM_+ = (VIH_+ - VIH-) / 2
VCM- = (VIL_+ - VIL-) / 2

VIN_+ = Positive differential DATA & CLK Input
VIN- = Negative differential DATA & CLK Input

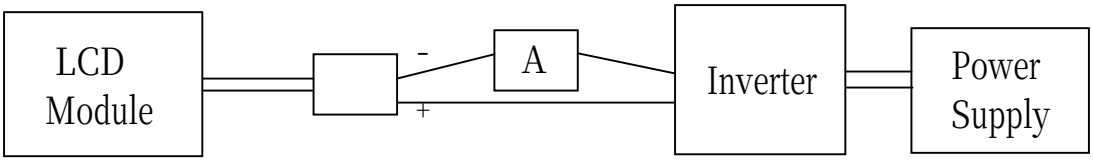
(2) Backlight system

Ta = 25°C

ITEM		SYMBOL	MIN	TYP	MAX	UNIT
Lamp Voltage		VL	-	640	-	V
Lamp Current ****1)***		IL	3.0	6.0	6.5	mA
Inverter Frequency		FI	-	52	-	KHz
Lamp life time ****2)***		Life L	10,000	-	-	hr
Starting Lamp Voltage	Ta = 25°C	-	-	-	1420	V
	Tb = 0°C	-	-	-	1610	

[Note 1]

*1) Lamp Current measurement method (The current meter is inserted in cold line)
Standard inverter : HIU766(52k) , typical luminance = (185) cd/m^2 (5 point).
The time that module luminance reduced to 50% of initial value .
Base on Vs = (1420) V , Ta = 25°C, IL=6.0 mA continuous.

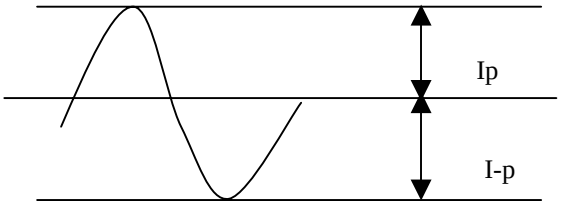


The lamp shall be stably lighted. Slide up method shall be used for input voltage application. The voltage is applied voltage to both ends of the lamp as the established starting voltage.

[Note 2]

Lamp frequency of inverter may produce interference with horizontal synchronous frequency,and this may cause horizontal beat on the display.Therefore,please adjust lamp frequency,and keep inverter as far from module as possible or use electronic shielding between inverter and module to avoid the interference.

The degrees of unbalance: less than 10%
The ratio of wave height: less than $\sqrt{2}$ ±10%



The degrees of umbalance = $|Ip-I-p|/Irms*100(\%)$
The ratio of wave height = Ip(or I-p)/Irms
Ip: lamp current high side peak, I-p: lamp current low side peak

[Note 3]

Definition of the lamp life time
Luminance: L under 50% of specification
Starting Lamp Voltage: VS < 1420 V, Ta=25°C
VS < 1610 V, Tb=0°C

4. INTERFACE CONNECTION

(1) CN1 (INTERFACE SIGNAL)

＊Connector type : 093B30-B000R0 (STARCONN made)

pin	Symbol	Function
1	VSS	Ground
2	VCC	+3.3V
3	VCC	+3.3V
4	V_EDID	DDC 3.3V Power
5	NC	VCOM test provided , but customer-end unused ; No Connect (open)
6	CLK_EDID	DDC Clock
7	DATA_EDID	DDC Data
8	R0M	minus signal of channel 0(LVDS)
9	R0P	plus signal of channel 0(LVDS)
10	Ground	Ground
11	R1M	minus signal of channel 1(LVDS)
12	R1P	plus signal of channel 1(LVDS)
13	Ground	Ground
14	R2M	minus signal of channel 2(LVDS)
15	R2P	plus signal of channel 2(LVDS)
16	Ground	Ground
17	RCLKM	minus signal of clock channel (LVDS)
18	RCLKP	plus signal of clock channel (LVDS)
19	Ground	Ground
20	NC	No Connect (Open)
21	NC	No Connect (Open)
22	NC	No Connect (Open)
23	NC	No Connect (Open)
24	NC	No Connect (Open)
25	NC	No Connect (Open)
26	NC	No Connect (Open)
27	NC	No Connect (Open)
28	NC	No Connect (Open)
29	NC	No Connect (Open)
30	NC	No Connect (Open)

(2) CN2 (BACKLIGHT)

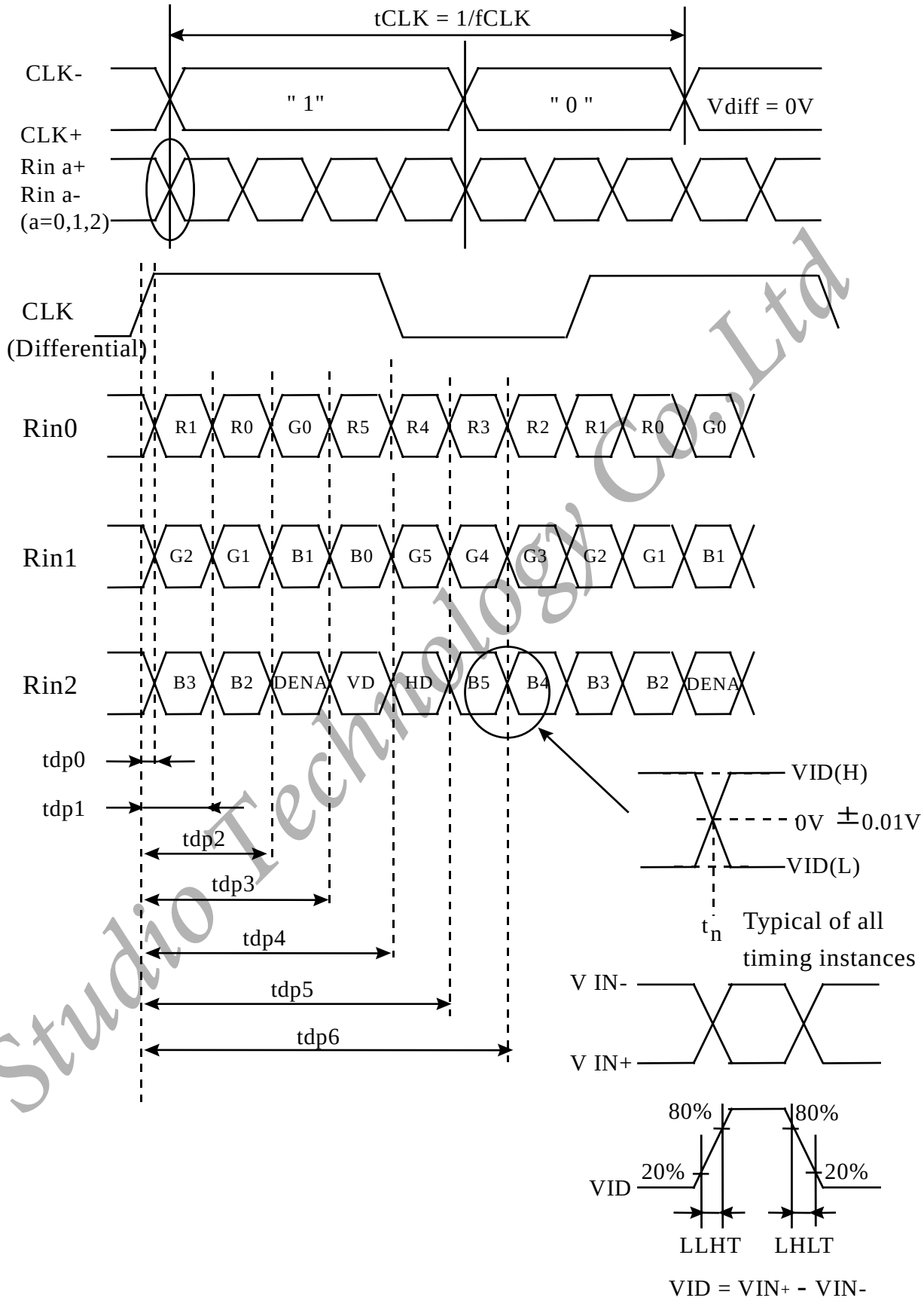
- Backlight-side connector: SBHS-002T-P0.5 (JST)
- Inverter-side connector: SM02B-BHSS-1(JST)

Pin No.	Symbol	Function
1	CTH	VBLH (High voltage)
2	CTL	VBLL (Low voltage)

[Note] VBLH-VBLL = VL

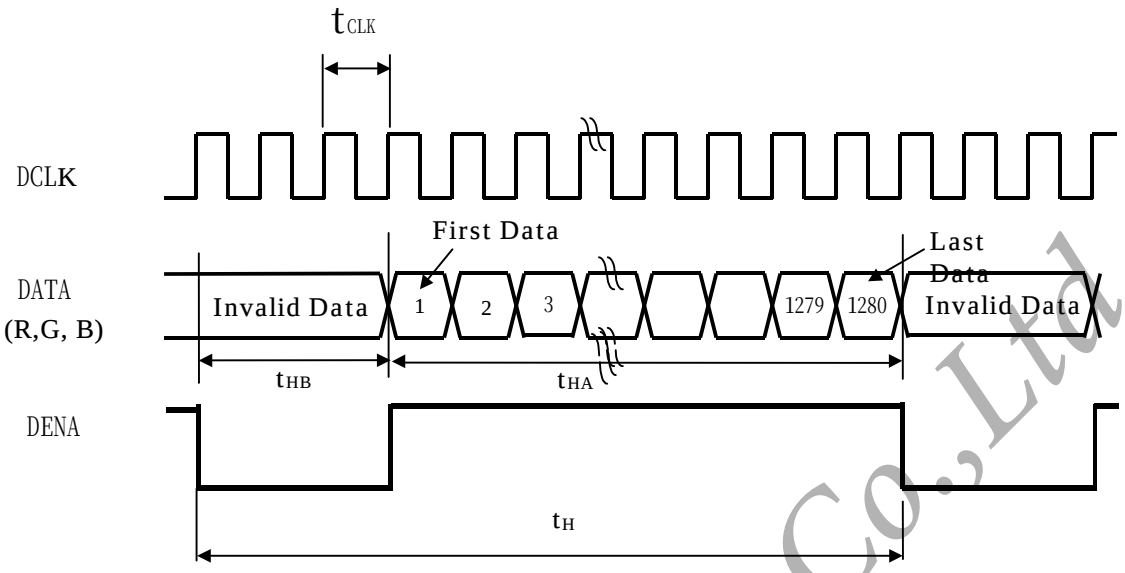
5. Input Signal Timing

(1)LVDS (Rx) Input Signal Timing Chart

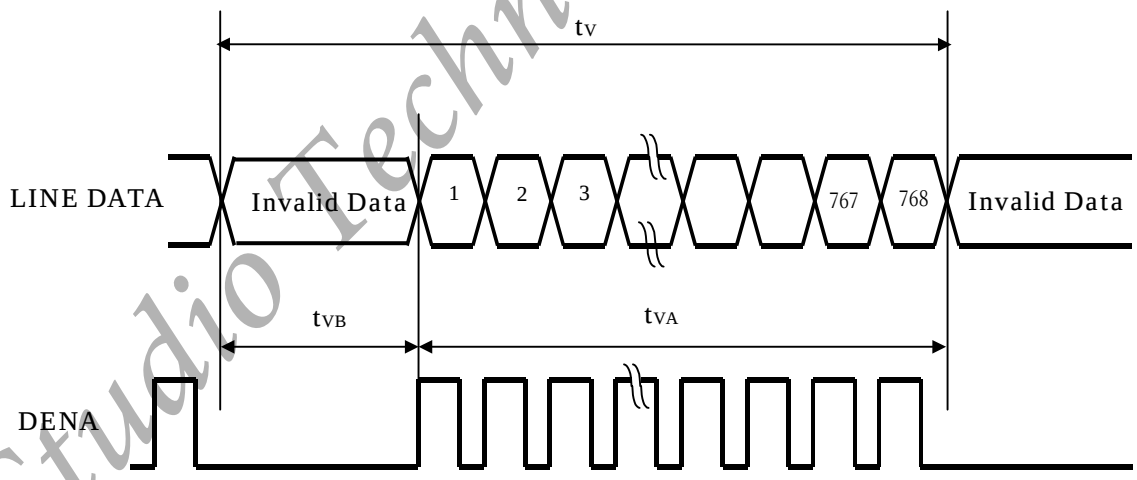


(2) LCD (Tx) Input Signal Timing Chart: (Rx output)

● Horizontal Timing:



● Vertical Timing



(3)Timing Specifications

ITEM				SYMBOL	MIN	TYP	MAX	UNIT
LVDS Input Timing	CLK frequency			fCLKin	-	68.25	-	MHz
	CLK period			tCLKin	-	14.65	-	ns
	LVDS High to Low transition time			LLHT	-	0.75	1.5	ns
	LVDS Low to High transition time			LHLT	-	0.75	1.5	ns
	Strobe position of Bit 0		f = 68.9MHz	Rspos0	0.7	1.1	1.4	ns
	Strobe position of Bit 1			Rspos1	2.9	3.3	3.6	ns
	Strobe position of Bit 2			Rspos2	5.1	5.5	5.8	ns
	Strobe position of Bit 3			Rspos3	7.3	7.7	8.0	ns
	Strobe position of Bit 4			Rspos4	9.5	9.9	10.2	ns
	Strobe position of Bit 5			Rspos5	11.7	12.1	12.4	ns
	Strobe position of Bit 6			Rspos6	13.9	14.3	14.6	ns
LCD input signal (LVDS Tx Input , Rx output)	DENA	Horizonta	Total	t_H	-	1440	-	tCLK
			Active	t_{HA}	-	1280	-	tCLK
			Blank	t_{HB}	-	160	-	tCLK
		Vertical	Frame Rate	fV	-	60	-	Hz
			Tatol	t_V	-	790	-	t_H
			Active	t_{VA}	-	768	-	t_H
			Blank	t_{VB}	-	22	-	t_H

[Note]

1) Data is latched at fall edge of DCLK in this specification.
2) DENA (Data Enable) should always be positive polarity as shown in the timing specification.
3) CLKIN should appear during all invalid period.

(4) Color data definition

COLOR	INPUT DATA	R_DATA						G_DATA						B_DATA					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
		MSB					LSB	MSB					LSB	MSB					LSB
Basic Color	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	BLUE(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENTA	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	RED(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	GREEN(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	GREEN(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	BLUE(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	BLUE(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

[Note]

(1) Definition of gray scale:

Color(n) : n means level of gray scale .

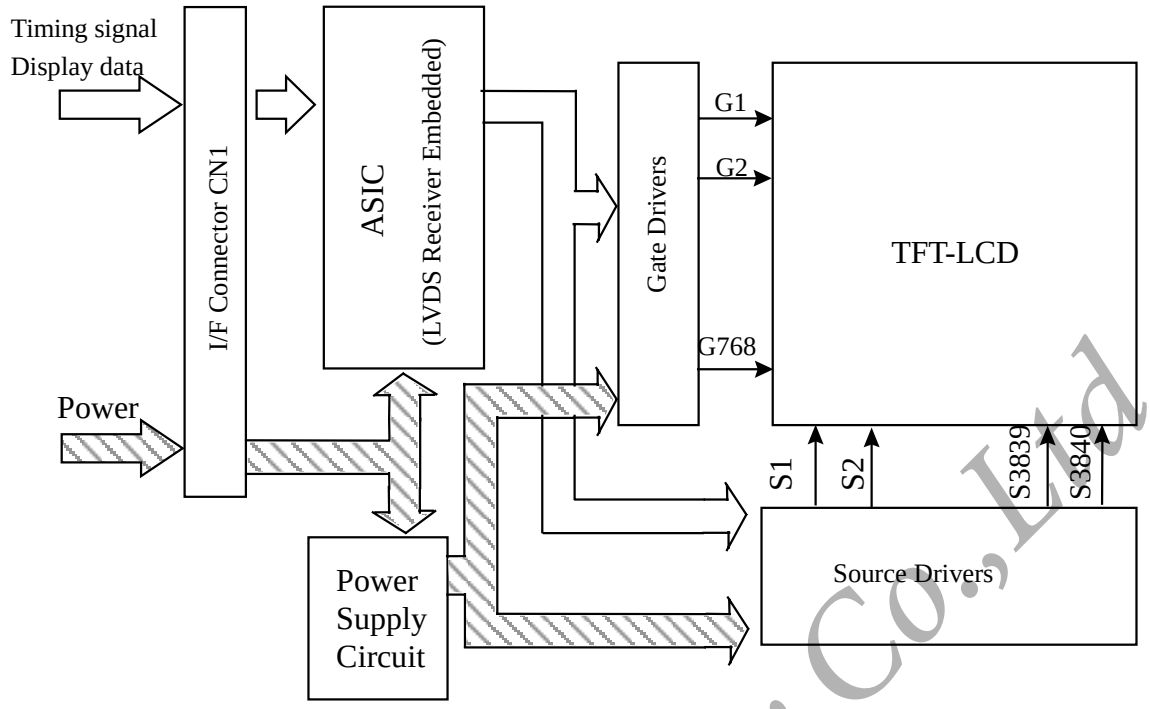
Bigger n means brighter level.

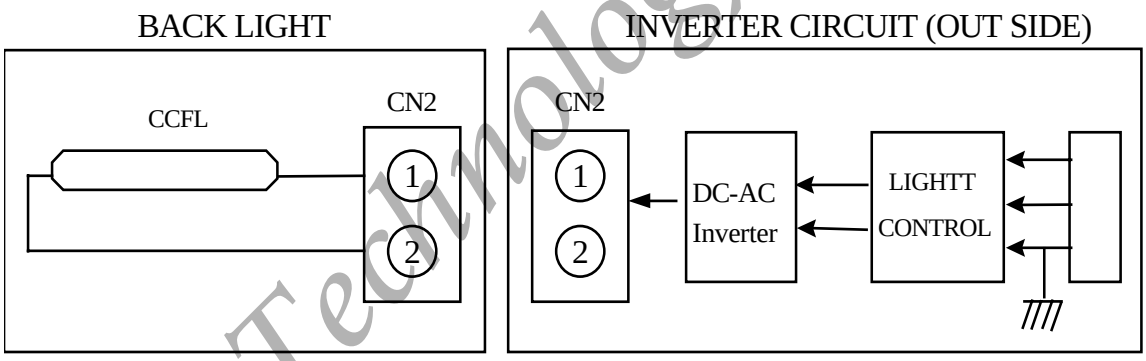
(2)Data : 1= High , 0 = Low

(5)Color Data Assignment

D(1,1)	D(2,1)	--	D(X,1)	--	D(1279,1)	D(1280,1)
D(1,2)	D(2,2)	--	D(X,2)	--	D(1279,2)	D(1280,2)
|	|	+	..	+	|	|
D(1,Y)	D(2,Y)	--	D(X,Y)	--	D(1279,Y)	D(1280,Y)
|	|	+	..	+	|	|
D(1,767)	D(2, 767)	--	D(X, 767)	--	D(1279,767)	D(1280,767)
D(1,768)	D(2, 768)	--	D(X, 768)	--	D(1279,768)	D(1280,768)

6. BLOCK DIAGRAM

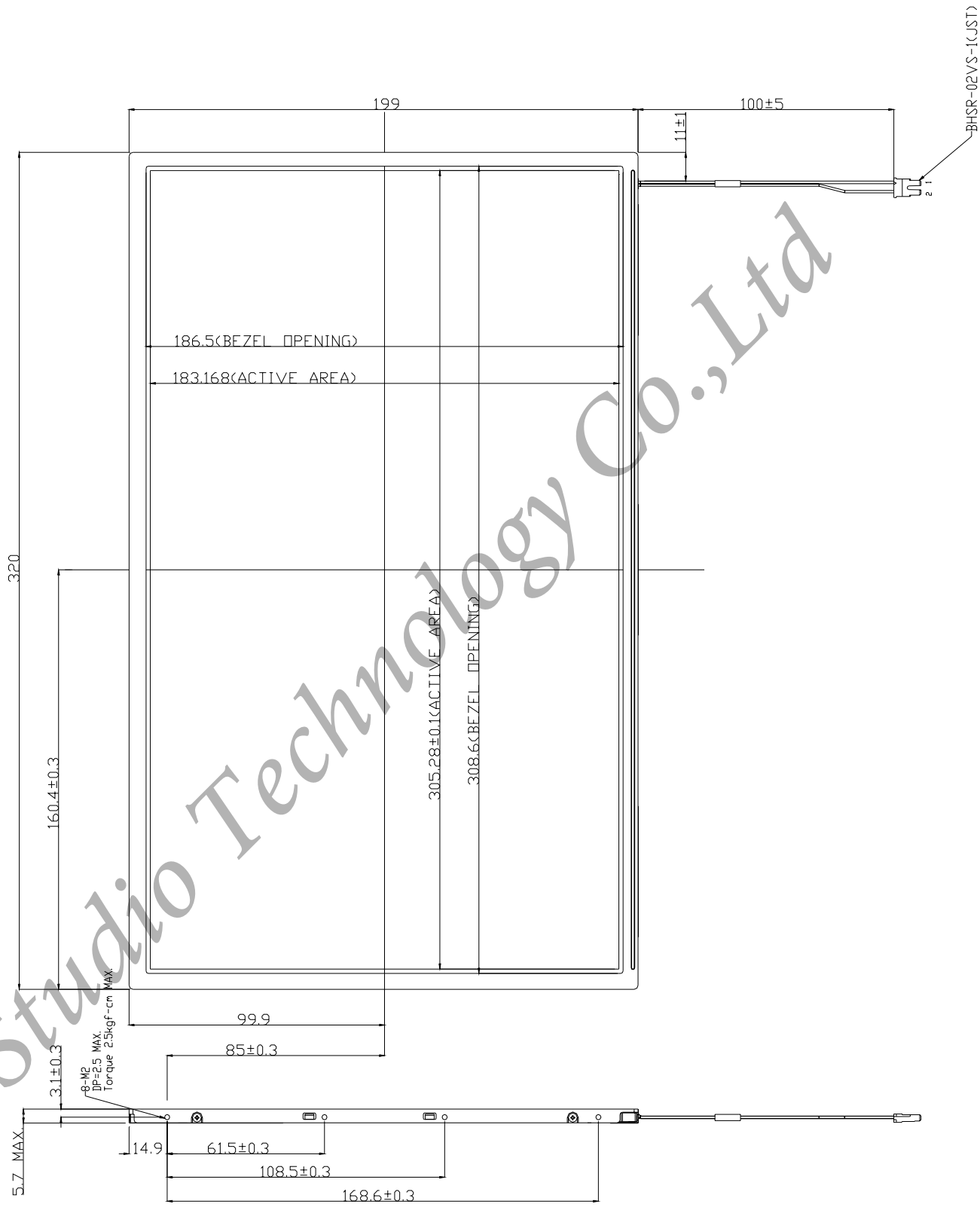




7. MECHANICAL DIMENSION

(1) Front side

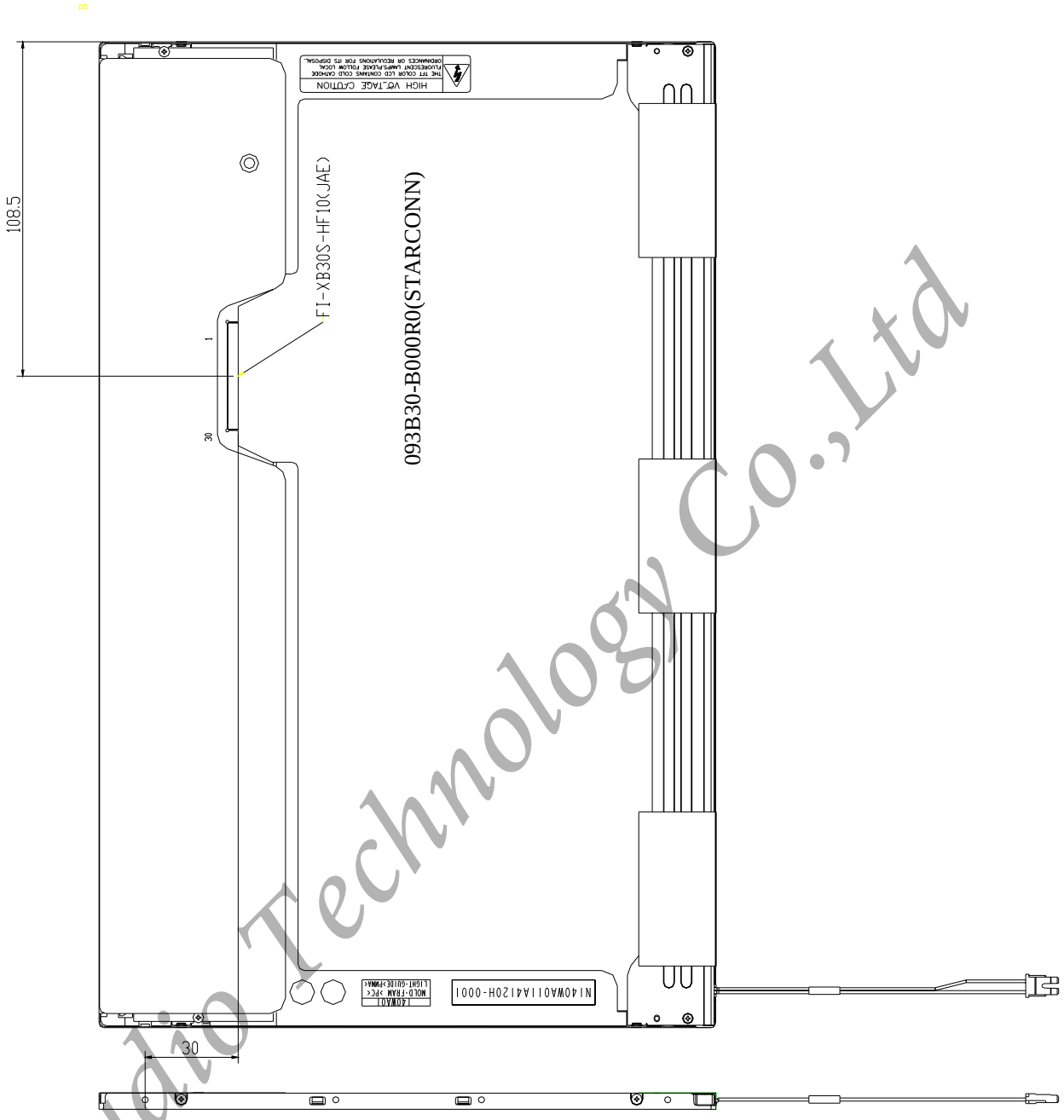
Unit : mm



[Note] Undefined tolerances to be ±0.5 mm

(2) Rear side

Unit : mm



[Note] Undefined tolerances to be ±0.5 mm

8. OPTICAL CHARACTERISTICS

Ta = 25°C

ITEM			SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Contrast Ratio			CR	θ = ψ = 0°	280	350	--	--
Luminance	Center		L	θ = ψ = 0°	160	200	--	cd/m²
	5 point		L	θ = ψ = 0°	150	185	--	
	Uniformit	5 point	ΔL	θ = ψ = 0°	--	--	25	%
		13 point	ΔL	θ = ψ = 0°	--	--	50	%
Response Time			Tr	θ = ψ = 0°	--	9	13	ms
			Tf	θ = ψ = 0°	--	16	22	ms
Image Sticking			Tis	2hour	--	--	2	Sec
Crosstalk			CMR	θ = ϕ = 0° *3)	-	-	1	%
Viewing Angle	Horizontal		ψ	CR≧10	-35~35	-40~40	--	°
	Vertical		θ		-35~15	-40~20	--	°
Color Coordinates	White		Wx Wy	θ = ψ = 0°	0.283 0.299	0.313 0.329	0.343 0.359	--
	Red		Rx Ry		0.559 0.296	0.589 0.326	0.619 0.356	
	Green		Gx Gy		0.285 0.510	0.315 0.540	0.345 0.570	
	Blue		Bx By		0.123 0.095	0.153 0.125	0.183 0.155	

[Note]

These items are measured using BM-5A(TOPCON)under the dark room condition(no ambient light) after more than 30 minutes from turning on the lamp unless noted.

Condition: IL=6.0 mA, Inverter Frequency=50kHz.

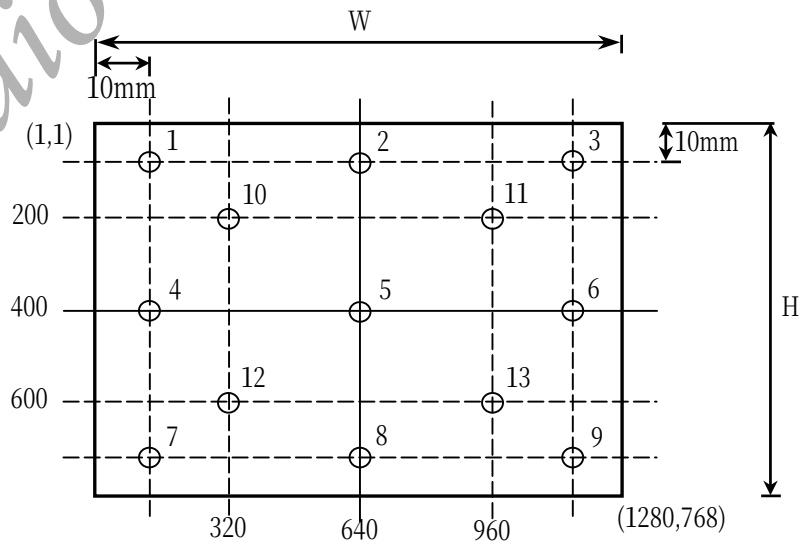
Definition of these measurement items are as follows:

(1)Definition of Contrast Ratio： CR=ON(White)Luminance/OFF(Black)Luminance

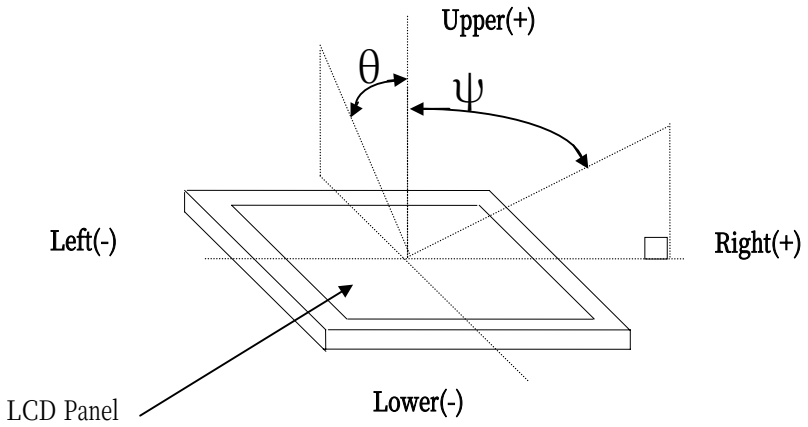
(2)Definition of Luminance and Luminance uniformity：

Measure White Luminance on the below center(5), 5 point(5,10,11,12,13)

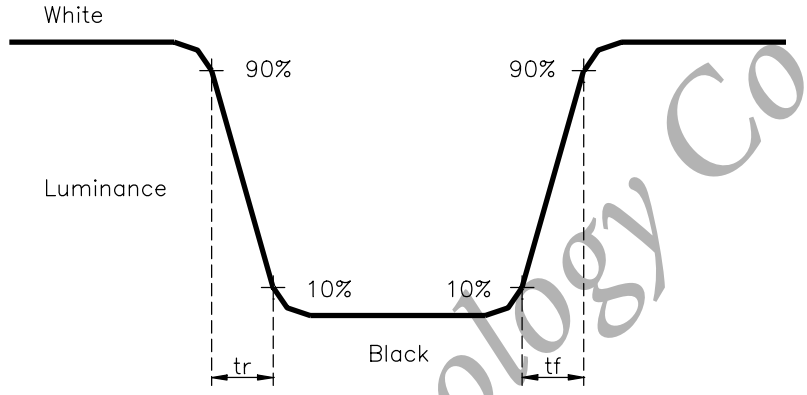
5 and 13 point Uniformity：$\Delta L = [(L_{MAX} - L_{MIN})/L_{MIN}] \times 100\%$



(3)Definition of Viewing Angle(θ , ψ)



(4)Definition of Response Time



(5)Definition of Contrast Ratio Uniformity

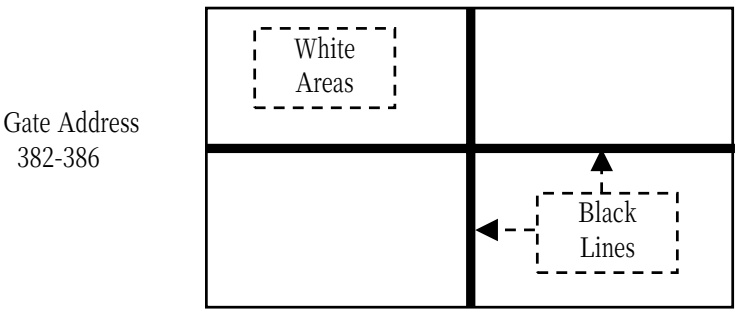
△ CR = [CR(MAX) / CR(MIN) - 1] x 100

(6)Definition of Luminance Uniformity

△ L = [L(MAX) / L(MIN)-1] x 100

(7) Definition of Image Sticking

Continuously display the test pattern shown in the figure below for two-hours. Then display a completely white screen. The previous image shall not persist more than two seconds at 25°C.



Gate Address
382-386

Source Address
638-642

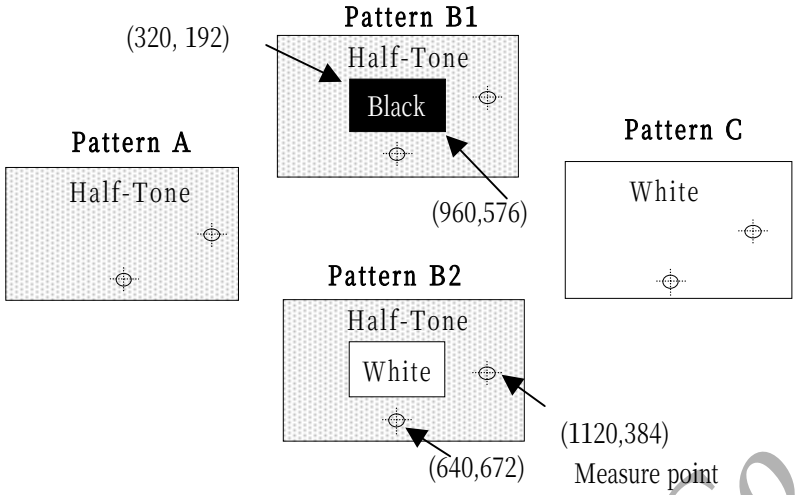
(8) Definition of Cross talk Modulation Ratio

CMR = MAX (***(| (LB1-LA) / LC |) ×100*** , ***(| (LB2 – LA) / LC |) ×100***)

LA：Pattern A(Half-Tone pattern) Measure point Luminance

LB1,LB2： Pattern B1、 Pattern B2 Measure point Luminance

LC：Pattern C(white pattern) Measure point Luminance



9. RELIABILITY TEST CONDITIONS

(1)Temperature and Humidity

TEST ITEMS	CONDITIONS
HIGH TEMPERATURE OPERATION	50°C,240h
HIGH TEMPERATURE STORAGE	60°C,240h
LOW TEMPERATURE OPERATION	0°C,240h
LOW TEMPERATURE STORAGE	-20°C,240h
HIGH TEMPERATURE HIGH HUMIDITY OPERATION	50°C, 90%RH ,240h
HIGH TEMPERATURE HIGH HUMIDITY STORAGE	60°C, 90%RH(Max), 48h
THERMAL SHOCK(No operation)	BETWEEN -20°C(1h)AND 60°C(1h),100 CYCLES

(2)Shock & Vibration

ITEMS	CONDITIONS
SHOCK (NON-OPERATION)	● Shock level: 2156 m/s^2 (220G) ● Waveform: half sinusoidal wave, 2ms ● Number of shocks: one shock input in each direction of three mutually perpendicular axes for a total of six shock inputs.
VIBRATION (NON-OPERATION)	● Vibration level: 14.7 m/s^2 (1.5G) , sinusoidal wave, perpendicular axis(each x,y,z axis: 1hr , total 3 hrs) ● Frequency range: 10 to 500 Hz ● Sweep speed : 0.5 octave / min

(3)ESD

ITEMS	CONDITIONS
ESD	● Contact mode：200pF, 0Ω, ±250V to I/F connector pins ● Air mode：150pF, 330Ω, ±15KV to LCD glass and metal bezel

(4)Judgment standard

The judgment of the above test should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect. Partial transformation of the module parts should be ignored.

Fail: No display image, obvious non-uniformity, or line defects.

10. HANDLING PRECAUTIONS FOR TFT-LCD MODULE

Please pay attention to the followings in handling- TFT-LCD products:

(A) ASSEMBLY PRECAUTION

(1) Please use the mounting hole on the module side in installing and do not beading or wrenching LCD in assembling. And please do not drop, bend or twist LCD module in handling.

(2) Please design display housing in accordance with the following guidelines.

(2.1) Housing case must be destined carefully so as not to put stresses on LCD all sides and not to wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.

(2.2) Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. Approximately 1.0 mm of the clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.

(2.3) When some parts, such as, FPC cable and ferrite plate, are installed underneath the LCD module, still sufficient clearance is required, such as 0.5mm. This clearance is, especially, to be reconsidered when the additional parts are implemented for EMI countermeasure.

(2.4) Design the inverter location and connector position carefully so as not to give stress to lamp cable, or not to interface the LCD module by the lamp cable.

(2.5) Keep sufficient clearance between LCD module and the others parts, such as inverter and speaker so as not to interface the LCD module. Approximately 1.0mm of the clearance in the design is recommended.

(3) Please do not push or scratch LCD panel surface with any-thing hard. And do not soil LCD panel surface by touching with bare hands. (Polarizer film, surface of LCD panel is easy to be flawed.)

(4) Please do not press any parts on the rear side such as source TCP, gate TCP, control circuit board and FPCs during handling LCD module. If pressing rear part is unavoidable, handle the LCD module with care not to damage them.

(5) Please wipe out LCD panel surface with absorbent cotton or soft of cloth in case of it being soiled.

(6) Please wipe out drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.

(7) Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.

(8) Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.

(9) Please pay attention to handling lead wire of backlight so that it is not tugged in connecting wit inverter.

(B) OPERATING PRECAUTIONS

(1) Please be sure to turn off the power supply before connecting and disconnecting signal input cable.

(2) Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification.

(3) Please consider that LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.

(4) A condensation might happen on the surface and inside of LCD module in case of sudden charge of ambient temperature.

(5) Please pay attention to displaying the same pattern for very long time. Image might stick on LCD.

(6) Please obey the same caution descriptions as ones that need to pay attention to ordinary electronic parts.

(C) PRECAUTFONS WITHELECTROSTATICS

(1) This LCD module use CMOS-IC on circuit board and TFT-LCD panel, and so it is easy to be affected by electrostatics. Please be careful with electrostatics by the way of your body connecting to the ground and so on.

(2) Please remove protection film very slowly on the surface of LCD module to prevent from electrostatics occurrence.

(D) STORAGE PRECAUTIONS

(1) When you store LCDs for a long time, it is recommended to keep the temperature between 0°C-40°C without the exposure of sunlight and to keep the humidity less than 90%RH.

(2) Please do not leave the LCDs in the environment of high humidity and high temperature such as 60°C 90%RH.

(3) Please do not leave the LCDs in the environment of low temperature below -20°C.

(E) SAFETY PRECAUTIONS

(1) When you waste LCDS, it is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

(2) If any liquid leaks out of a damaged-glass cell and comes in contact with the hands, wash off throughly with soap and water.

(F) OTHERS

(1) A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight Land strong UV rays.

(2) Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.

(3) For the packaging box, please pay attention to the followings:

(3.1) Packaging box and inner case for LCD are designed to protect the LCDs from the damage or scratching during transportation. Please do not open except picking LCDs up from the box.

(3.2) Please do not pile them up more than 5 boxes. (They are not designed so.) And please do not turn over.

(3.3) Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.

(3.4) Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)

11. APPENDIX - ISP Enhanced Extended Display Identification Data (EEDID)

APPENDIX - ISP Enhanced Extended Display Identification Data (EEDID)
SPWG V2.1 LCD Model : CLAA140WA01

Byte# (dec)	Byte# (hex)	Field Name and Comments	Value (hex)	Value (binary)
		Header		
0	0		0	0000 0000
1	1		FF	1111 1111
2	2		FF	1111 1111
3	3		FF	1111 1111
4	4		FF	1111 1111
5	5		FF	1111 1111
6	6		FF	1111 1111
7	7		0	0000 0000
		Vender / Product ID / EDID Version		
8	8	EISA manufacturer code = CPT *(1st byte)*	0E	0000 1110
9	9	*(2nd*	14	0001 0100
10	0A	Product code LSB =71	71	0111 0001
11	0B	Product code MSB =17	17	0001 0111
12	0C	ID (32-bit) serial number *(preferred, but optional, zero if not used)*	0	0000 0000
13	0D		0	0000 0000
14	0E		0	0000 0000
15	0F		0	0000 0000
16	10	Week of manufacture *(preferred, but optional, zero if not used)*	2A	0010 1010
17	11	Year of manufacture *(preferred, but optional, zero if not used)*	E	0000 1110
18	12	EDID Structure version # = 1	1	0000 0001
19	13	EDID Revision # = 3	3	0000 0011
		Display Parameter		
20	14	Video input definition *(Digital I/P, non TMDS CRGB)*	80	1000 0000
21	15	Max H image size (31) *(rounded to cm)*	1F	0001 1111
22	16	Max V image size (18) *(rounded to cm)*	12	0001 0010
23	17	Display gamma =2.2 *(=(gamma*100)-100)*	78	0111 1000
24	18	Features *(no DPMS, Active off, RGB, timing BLK1)*	0A	0000 1010
		Panel Color Coordinates		
25	19	Red/Green low Bits	AD	1010 1101
26	1A	Blue/White Low Bits	D	0000 1101
27	1B	Red X Rx = 0.589	96	1001 0110
28	1C	Red Y Ry = 0.326	53	0101 0011
29	1D	Green X Gx = 0.315	50	0101 0000
30	1E	Green Y Gy = 0.54	8A	1000 1010
31	1F	Blue X Bx = 0.153	27	0010 0111
32	20	Blue Y By = 0.125	20	0010 0000
33	21	White X Wx = 0.313	50	0101 0000
34	22	White Y Wy = 0.329	54	0101 0100
		Established Timings		
35	23	Established Timing I not used	0	0000 0000
36	24	Established Timing II not used	0	0000 0000
37	25	Manufacturer's Timings not used	0	0000 0000
		Standard Timing ID		
38	26	Standard Timing Identification 1 not used	1	0000 0001
39	27	Standard Timing Identification 1 not used	1	0000 0001
40	28	Standard Timing Identification 2 not used	1	0000 0001
41	29	Standard Timing Identification 2 not used	1	0000 0001
42	2A	Standard Timing Identification 3 not used	1	0000 0001

APPENDIX - ISP Enhanced Extended Display Identification Data (EEDID)
SPWG V2.1 LCD Model : CLAA140WA01

Byte# (dec)	Byte# (hex)	Field Name and Comments	Value (hex)	Value (binary)
43	2B	Standard Timing Identification 3 not used	1	0000 0001
44	2C	Standard Timing Identification 4 not used	1	0000 0001
45	2D	Standard Timing Identification 4 not used	1	0000 0001
46	2E	Standard Timing Identification 5 not used	1	0000 0001
47	2F	Standard Timing Identification 5 not used	1	0000 0001
48	30	Standard Timing Identification 6 not used	1	0000 0001
49	31	Standard Timing Identification 6 not used	1	0000 0001
50	32	Standard Timing Identification 7 not used	1	0000 0001
51	33	Standard Timing Identification 7 not used	1	0000 0001
52	34	Standard Timing Identification 8 not used	1	0000 0001
53	35	Standard Timing Identification 8 not used	1	0000 0001
Detailed Timing Descriptor #1				
54	36	Pixel Clock (LSB)	A9	1010 1001
55	37	Pixel Clock (MSB)	1A	0001 1010
56	38	Horizontal Active = 1280 pixels Notes2 (lower 8 bits)	0	0000 0000
57	39	Horizontal Blanking = 160 pixels (lower 8 bits)	A0	1010 0000
58	3A	Horizontal Active : Horizontal Blanking(thbp) (upper 4:4 bits)	50	0101 0000
59	3B	Vertical Avtive = 768 lines	0	0000 0000
60	3C	Vertical Blanking(tvbp) = 22 lines (DE Blanking min for DE-only panels) lines	16	0001 0110
61	3D	Vertical Active : Vertical Blanking(tvbp) (upper 4:4 bits)	30	0011 0000
62	3E	Horizontal Sync. Offset (thfp)= 48 pixels	30	0011 0000
63	3F	Horizontal Sync Pulse Width = 32 pixels(WHL)	20	0010 0000
64	40	Vertical Sync Offset (tvfp)= 3 lines,Sync Width(tWVL) = 6 lines	36	0011 0110
65	41	Horizontal Vertical Sync Offset/Width upper 2bits	0	0000 0000
66	42	Horizontal Image Size = 305mm (lower 8bits)	31	0011 0001
67	43	Vertical Image Size = 183mm (lower 8bits)	B7	1011 0111
68	44	Horizontal & Vertical Image Size (upper 4:4bits)	10	0001 0000
69	45	Horizontal Border = X (Zero for internal LCD)	0	0000 0000
70	46	Vertical Border = X (Zero for internal LCD)	0	0000 0000
71	47	Non-interlaced,Normal display,no stereo, Digital separate sync,H/V pol negatives	19	0001 1001
Detailed Timing Descriptor #2: Alternative Panel Timing				
72	48	Flag	0	0000 0000
73	49	Flag	0	0000 0000
74	4A	Flag	0	0000 0000
75	4B	Data Type Tag: Descriptor Defined by Manufacture	0F	0000 FFFF
76	4C	Flag	0	0000 0000
77	4D	value=HSPWmin/2 (pixel clks)WHL	20	0010 0000
78	4E	value=HSPWmax/2 (pixel clks)WHL	20	0010 0000
79	4F	value=Thbpmin/2 (pixel clks) (for DE-only timing also, with Thfp=0)	20	0010 0000
80	50	value=Thbpmax/2 (pixel clks) (for DE-only timing also, with Thfp=0)	20	0010 0000
81	51	value=VSPWmin/2 (line pulses)WVL	20	0010 0000
82	52	value=VSPWmax/2 (line pulses)WVL	20	0010 0000
83	53	value=Tvbpmin/2	20	0010 0000
84	54	value=Tvbpmax/2	20	0010 0000
85	55	Thpmin=value*2+HApixelClks (pixel clks) Note2	14	0001 0100
86	56	Thpmax=value*2+HApixelClks (pixel clks) Note2	A0	1010 0000
87	57	Tvpmin=value*2+Valines (line pulses)	2	0000 0010
88	58	Tvpmax=value*2+Valines (line pulses)	29	0010 1001
89	59	Module revision	0	0000 0000

Nites 1.See figure A1 Timing Waveform Parameter for definitions

APPENDIX - ISP Enhanced Extended Display Identification Data (EEDID)
SPWG V2.1 LCD Model : CLAA140WA01

Byte# (dec)	Byte# (hex)	Field Name and Comments	Value (hex)	Value (binary)
		2.Horizontal Active(HA) (byte 38h) is ture active pixels. HApixelClks value (bytes 55&56) is HA for XGA, and HA/2 for SXGA and above		
Detailed Timing Descriptor #3: ASCII String: Supplier Name				
90	5A	Flag	0	0000 0000
91	5B	Flag	0	0000 0000
92	5C	Flag	0	0000 0000
93	5D	Data Type Tag: *(Monitor)* ASCII String	FE	1111 1110
94	5E	Flag	0	0000 0000
95	5F	"C",67	43	0100 0011
96	60	"P",80	50	0101 0000
97	61	"T",84	54	0101 0100
98	62		0A	0000 1010
99	63		20	0010 0000
100	64		20	0010 0000
101	65		20	0010 0000
102	66		20	0010 0000
103	67		20	0010 0000
104	68		20	0010 0000
105	69		20	0010 0000
106	6A		20	0010 0000
107	6B	*(if <13 char, then terminate with ASCII code 0Ah, and set remaining char = 20h)*	20	0010 0000
Detailed Timing Descriptor #4: ASCII String: Supplier P/N				
108	6C	Flag	0	0000 0000
109	6D	Flag	0	0000 0000
110	6E	Flag	0	0000 0000
111	6F	Data Type Tag: *(Monitor)* ASCII String	FE	1111 1110
112	70	Flag	0	0000 0000
113	71	"C",67	43	0100 0011
114	72	"L",76	4C	0100 1100
115	73	"A",65	41	0100 0001
116	74	"A",65	41	0100 0001
117	75	"1",49	31	0011 0001
118	76	"4",52	34	0011 0100
119	77	"0",48	30	0011 0000
120	78	"W",87	57	0101 0111
121	79	"A",65	41	0100 0001
122	7A	"0",48	30	0011 0000
123	7B	"1",49	31	0011 0001
124	7C		20	0100 0001
125	7D	*(if <13 char, then terminate with ASCII code 0Ah, and set remaining char = 20h)*	20	0010 0000
126	7E	Extension Flag *(# of optional 128-byte EDID extension blocks to follow, typ=0)*	0	0000 0000
127	7F	Checksum *(the 1-byte sum of all 128 bytes in this EDID block shall equal zero)*	B	0000 1011