# CUSTOMER APPROVAL SHEET

| | |
|---|---|
| Company Name | |
| MODEL | |
| CUSTOMER APPROVED | Title :<br>Name : |

- ☐ APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)
- ☐ APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.____)
- ☐ APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver.____)
- ☐ CUSTOMER REMARK :

**AUO PM :**

**P/N :** _____

**Comment :**

| | |
|---|---|
| Doc. version : | 0.2 |
| Total pages : | 53 |
| Date : | 2009/10/07 |

# Product Specification

# Model Name： A024CN03 V2

| | |
|---|---|
| **Planned Lifetime:** | From 2009/Aug. To 2011/Jun. |
| **Phase-out Control:** | From 2011/Mar. To 2011/Jun. |
| **EOL Schedule:** | 2011/Jun. |

< ◆ > Preliminary Specification

< > Final Specification

Note: The content of this specification is subject to change.



## Record of Revision

| Version | Revise Date | Page | Content |
|---|---|---|---|
| 0.0 | 2009/08/07 | | Draft |
| 0.1 | 2009/10/07 | 9 | Modify VCDC value. |
| 0.2 | 2009/10/30 | 46 ~ 53 | Modify power on/off setting. |
| 0.3 | 2009/11/30 | 9 | Modify $V_{CDC}$ voltage value. |

## Contents:

## A. Physical specifications

| NO. | Item | Specification | Remark |
|---|---|---|---|
| 1 | Display resolution (dot) | 480(W)×234(H) | |
| 2 | Active area (mm) | 48.0 (W) × 35.685 (H) | |
| 3 | Screen size (inch) | 2.36 (Diagonal) | |
| 4 | Dot pitch (mm) | 0.10 (W) × 0.1525 (H) | |
| 5 | Color configuration | R. G. B. delta | |
| 6 | Overall dimension (mm) | 54.9 (W) × 47.45 (H) × 2.6 (D) | Note 1 |
| 7 | Weight (g) | 10.9 | |
| 8 | Panel surface treatment | Hard coating | |

Note 1: Refer to Fig.1

# B. Electrical specifications

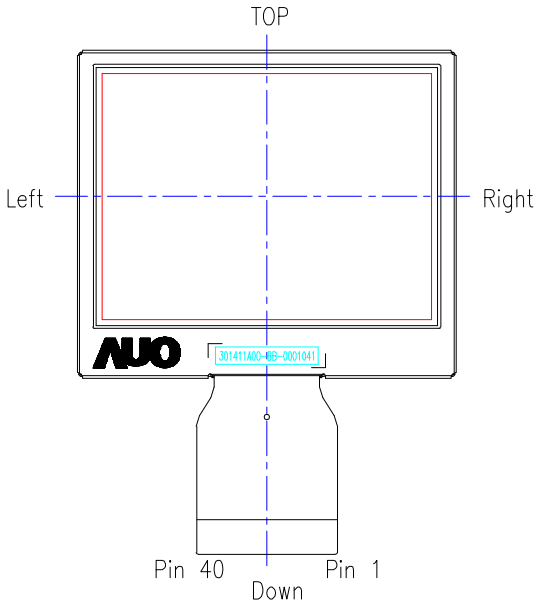
## 1. Pin assignment

| Pin no | Symbol | I/O | Description | Remark |
|---|---|---|---|---|
| 1 | VCOM | I | Common electrode driving voltage | |
| 2 | DUMMY | NC | No connection | |
| 3 | VGL | C | Negative low power supply for gate driver output: -12.5V | |
| 4 | C4P | C | Pins to connect capacitance for power circuitry | |
| 5 | C4M | C | Pins to connect capacitance for power circuitry | |
| 6 | VGH | C | Positive power supply for gate driver output: +12.5V | |
| 7 | FRP | O | Frame polarity output for VCOM | |
| 8 | VCAC | C | Define the amplitude of the VCOM swing | |
| 9 | Vint3 | C | Intermediate voltage for charge Pump | |
| 10 | C3P | C | Pins to connect capacitance for power circuitry | |
| 11 | C3M | C | Pins to connect capacitance for power circuitry | |
| 12 | Vint2 | C | Intermediate voltage for charge Pump | |
| 13 | C2P | C | Pins to connect capacitance for power circuitry | |
| 14 | C2M | C | Pins to connect capacitance for power circuitry | |
| 15 | Vint1 | C | Intermediate voltage for charge Pump | |
| 16 | C1P | C | Pins to connect capacitance for power circuitry | |
| 17 | C1M | C | Pins to connect capacitance for power circuitry | |
| 18 | PGND | P | Charge Pump Power GND | |
| 19 | PVDD | P | Charge Pump Power VDD | |
| 20 | DRV | O | Gate signal for the power transistor of the boost converter | |
| 21 | LED+ | P | For Led Anode voltage | |
| 22 | DUMMY | NC | No connection | |
| 23 | FB | P/I | Led Cathode and main boost regulator feedback input | |
| 24 | DUMMY | NC | No connection | |
| 25 | GND | P | Digital GND | |
| 26 | VCC | P | Digital power supply | |
| 27 | CS | I | Serial communication chip select | |
| 28 | SDA | I/O | Serial communication data input/output | |
| 29 | SCL | I | Serial communication clock input | |
| 30 | HSYNC | I | Horizontal sync input | |
| 31 | VSYNC | I | Vertical sync input | |
| 32 | DCLK | I | Clock Input: | |
| 33 | D7 | I | Data Input: MSB | |

| | | | | |
|---|---|---|---|---|
| 34 | D6 | I | Data Input: | |
| 35 | D5 | I | Data Input: | |
| 36 | D4 | I | Data Input: | |
| 37 | D3 | I | Data Input: | |
| 38 | D2 | I | Data Input: | |
| 39 | D1 | I | Data Input: | |
| 40 | D0 | I | Data Input: LSB | |

I: Input; O: Output. P: Power. I/O input/output C: Capacitor pin. P/I: power / input.

Note: Definition of scanning direction. Refer to figure as below




## 2. Absolute maximum ratings

| Item | Symbol | Condition | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| Power voltage | $V_{CC}$ | GND=0 | -0.5 | 7.0 | V | |
| | $PV_{DD}$ | PGND=0 | -0.5 | 7.0 | V | |
| Input signal voltage | D0~D7 | - | -0.3 | 3.6 | V | |
| Input signal voltage | VCOM | - | -2.9 | 5.2 | V | VCOM DC Voltage |
| Operating temperature | Topa | - | 0 | 60 | □ | Ambient temperature |
| Storage temperature | Tstg | - | -25 | 70 | □ | Ambient temperature |

## 3. Electrical characteristics

### a. Typical operating conditions (GND=0V)

| Item | | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Power Voltage | | $V_{CC}$ | 2.7 | 3.3 | 3.6 | V | Note 1 |
| | | $PV_{DD}$ | 3.0 | 3.3 | 3.6 | V | Note 1 |
| TFT-LCD Power Voltage | | VGH | 11.0 | 12.5 | 14.0 | V | GND=PGND=0V |
| | | VGL | -14.0 | -12.5 | -11.0 | V | GND=PGND=0V |
| Output Signal Voltage | H Level | $V_{OH}$ | Vcc-0.4 | - | Vcc | V | |
| | L Level | $V_{OL}$ | GND | - | GND+0.4 | V | |
| Input Signal Voltage | H Level | $V_{IH}$ | 0.7x$V_{CC}$ | - | $V_{CC}$ | V | |
| | L Level | $V_{IL}$ | GND | - | 0.3x$V_{CC}$ | V | |
| VCOM Voltage | | $V_{CAC}$ | 4.4 | 5.0 | 5.1 | V | V |
| | | $V_{CDC}$ | 1.0 | 1.1 | 1.2 | V | V |
| DRV output voltage | | $V_{DRV}$ | 0 | - | $PV_{DD}$ | V | V |

Note 1: A build-in power on reset circuit for $PV_{DD}$ and $V_{CC}$ is provided within the integrated LCD driver IC.

### b. Current characteristics (GND=0V)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Input Current for $V_{CC}$ | $I_{VCC}$(Pin 26) | $V_{CC}$=3.3V | -- | 0.1 | 0.3 | mA | Note 1 |
| Input Current for $PV_{DD}$ | $I_{PVDD}$(Pin 19) | $PV_{DD}$=3.3V | -- | 8 | 10 | mA | Note 1 |
| Output current | H Level | IOH | - | 400 | - | uA | |
| | L Level | IOL | - | -400 | - | uA | |
| Analog stand by current | $I_{PVDD}$ | $PV_{DD}$=3.3V | - | 7.5 | 10 | uA | DCLK is stopped |
| Digital stand by current | $I_{VCC}$ | $V_{CC}$=3.3V | - | -- | 110 | uA | |
| DRV output current | $I_{DRV}$ | $V_{CC}$ = 3.0V DRV = 0.7V | - | - | 10 | mA | |

Note 1: Use UPS052 mode and $F_{DCLK}$=24.54MHz,.other registers are default setting.

### c. LED driving conditions

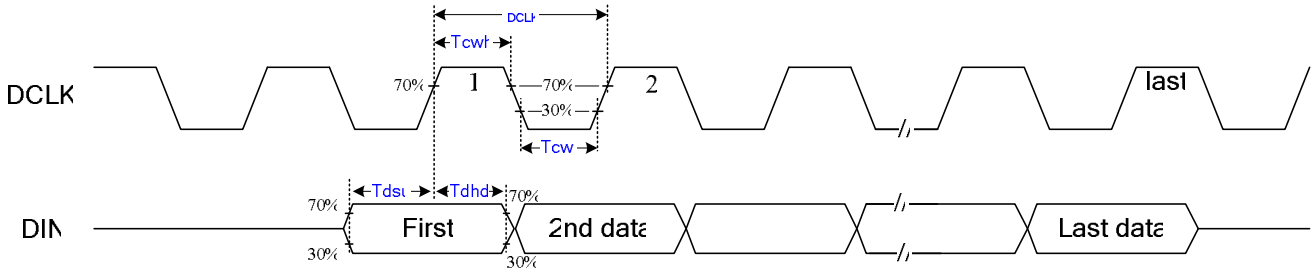
| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| LED current | $I_L$ | | 25 | 27.5 | mA | |
| LED voltage | $V_L$ | - | 3.8 | 4.4 | V | Note1 |

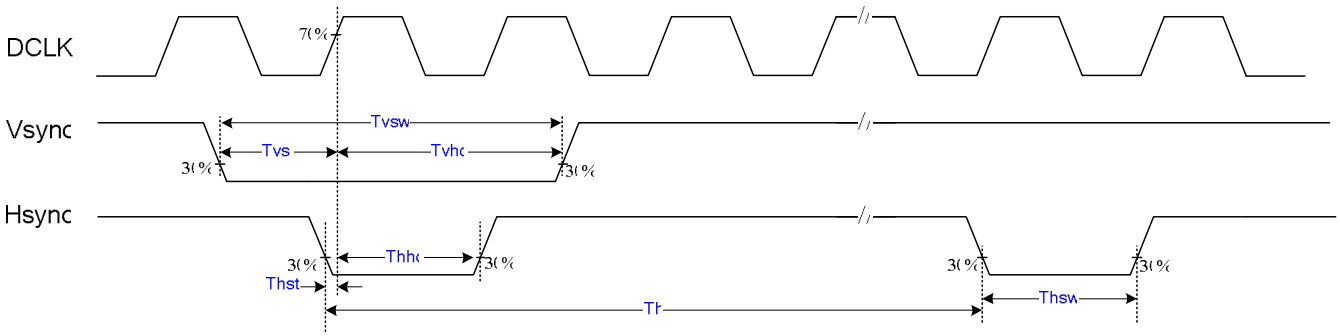
Note 1 : Typical LED voltage : 3.2V/pcs,FB=0.6V, LED voltage: $V_L$ =3.2+0.6=3.8V . Refer to application circuit.

## 4. AC Timing

### a. Digital Signal AC Characteristic

| Parameter | Symbol | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|
| DCLK duty cycle | Tcwh/Tcwl | 40 | 50 | 60 | % $t_{DCLK}$ |
| VSYNC setup time | Tvst | 12 | - | - | ns |
| VSYNC hold time | Tvhd | 12 | - | - | ns |
| HSYNC setup time | Thst | 12 | - | - | ns |
| HSYNC hold time | Thhd | 12 | - | - | ns |
| Data set-up time | Tdsu | 12 | - | - | ns |
| Data hold time | Tdhd | 12 | - | - | ns |
| HSYNC width | Thsw | 1 | 1 | 254 | $t_{DCLK}$ |
| VSYNC width | Tvsw | 1 $t_{DCLK}$ | 1 $t_{DCLK}$ | $6t_H$ | |



**b. UPS051 Timing conditions**

| Parameter | | | Symbol | Min. | Typ. | Max. | Unit. | Remark |
|---|---|---|---|---|---|---|---|---|
| DCLK Frequency | | | $1/t_{DCLK}$ | 8.4 | 9.7 | 11 | MHz | |
| HSYNC | Period | | $t_H$ | 580 | 617 | 695 | $t_{DCLK}$ | Note 1 |
| | Display period | | $t_{hd}$ | 480 | | | $t_{DCLK}$ | |
| | Back porch | | $t_{hbp}$ | 84 | 100 | 115 | $t_{DCLK}$ | |
| | Front porch | | $t_{hfp}$ | $t_H - t_{hd} - t_{hbp}$ | | | $t_{DCLK}$ | |
| | Pulse width | | $t_{hsw}$ | 1 | 1 | 50 | $t_{DCLK}$ | |
| VSYNC | Period | Odd | $t_V$ | 247.5 | 262.5 | 277.5 | $t_H$ | Note 2, 3, 4 |
| | | Even | | | | | | |
| | Display period | Odd | $t_{vd}$ | 234 | | | $t_H$ | |
| | | Even | | | | | | |
| | Back porch | Odd | $t_{vbp}$ | 9 | 16 | 24 | $t_H$ | |
| | | Even | | 9.5 | 16.5 | 24.5 | | |
| | Front porch | Odd | $t_{vfp}$ | $t_V - t_{vd} - t_{vbp}$ | | | $t_H$ | |
| | | Even | | | | | | |
| | Pulse width | Odd | $t_{vsw}$ | 1 $t_{DCLK}$ | $1t_H$ | $6t_H$ | | |
| | | Even | | | | | | |

Note 1: UPS051 Horizontal back porch time ($t_{hbp}$) is adjustable by setting register DDL; requirement of minimum back porch time and minimum front porch time must be satisfied.

Note 2: UPS051 Vertical back porch time ($t_{vbp}$) is adjustable by setting register HDL; requirement of minimum back porch time and minimum front porch time must be satisfied.

Note 3: Both interlace and non-interlace mode can be accepted.

Note 4: AUO suggests frame rate at least 50 Hz to get the better display quality.

**Fig.1 UPS051 Input Horizontal Timing Chat**

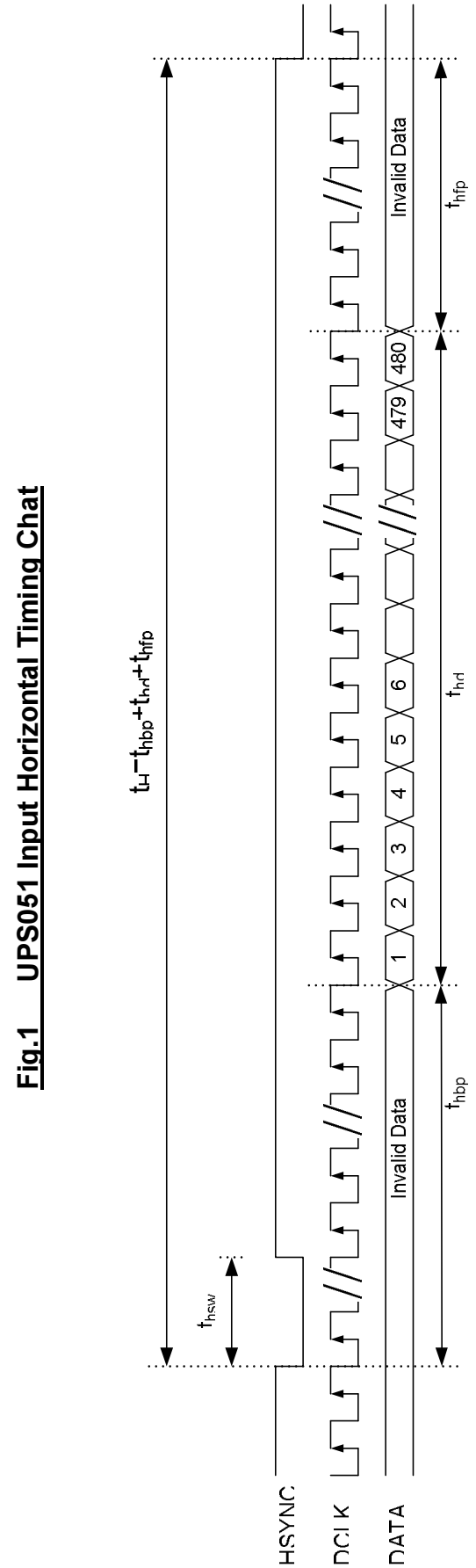



**Fig.2 UPS051 Input Horizontal Data Sequence**

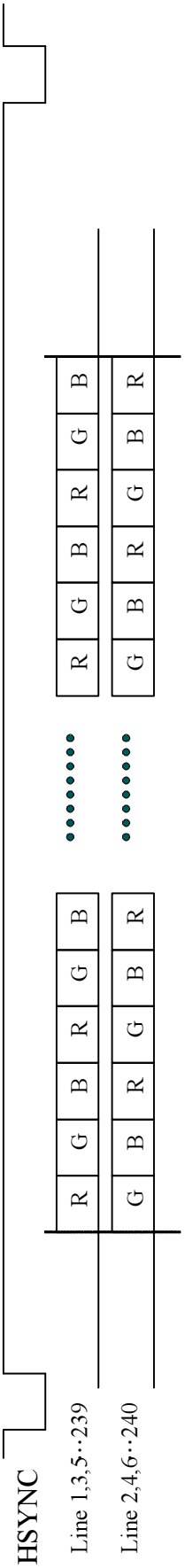
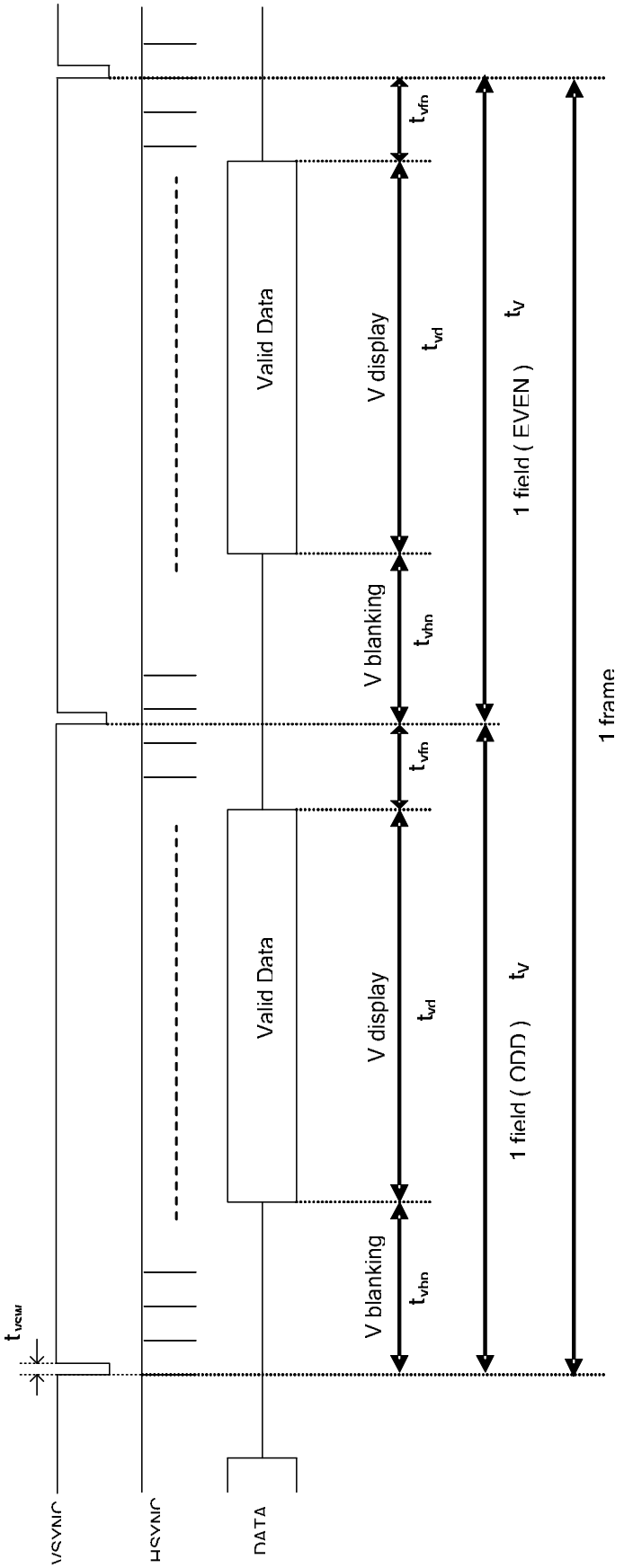


**Fig.3 UPS051 Input Vertical Timing Chat**



### c. UPS052 Timing conditions

c - 1. UPS052 (320 mode 24.55MHz) timing specifications

| Parameter | | | Symbol | Min. | Typ. | Max. | Unit. | Remark |
|---|---|---|---|---|---|---|---|---|
| DCLK Frequency | | | $1/t_{DCLK}$ | 21.07 | 24.55 | 28.06 | MHz | |
| HSYNC | Period | | $t_H$ | 1524 | 1560 | 1644 | $t_{DCLK}$ | |
| | Display period | | $t_{hd}$ | 1280 | | | $t_{DCLK}$ | |
| | Back porch | | $t_{hbp}$ | 236 | 252 | 267 | $t_{DCLK}$ | |
| | Front porch | | $t_{hfp}$ | $t_H - t_{hd} - t_{hbp}$ | | | $t_{DCLK}$ | |
| | Pulse width | | $t_{hsw}$ | 1 | 1 | 96 | $t_{DCLK}$ | |
| VSYNC | Period | Odd | $t_V$ | 247.5 | 262.5 | 277.5 | $t_H$ | Note 1, 2 |
| | | Even | | | | | | |
| | Display period | Odd | $t_{vd}$ | 240 | | | $t_H$ | |
| | | Even | | | | | | |
| | Back porch | Odd | $t_{vbp}$ | 6 | 13 | 21 | $t_H$ | |
| | | Even | | 6.5 | 13.5 | 21.5 | | |
| | Front porch | Odd | $t_{vfp}$ | $t_V - t_{vd} - t_{vbp}$ | | | $t_H$ | |
| | | Even | | | | | | |
| | Pulse width | Odd | $t_{vsw}$ | 1 $t_{DCLK}$ | $1t_H$ | $6t_H$ | | |
| | | Even | | | | | | |

Note 1: AUO suggests frame rate at least 50 Hz to get the better display quality.

Note 2: Both interlace and non-interlace mode can be accepted.

c - 2. UPS052 (360 mode 27MHz) timing specifications

| Parameter | | | Symbol | Min. | Typ. | Max. | Unit. | Remark |
|---|---|---|---|---|---|---|---|---|
| DCLK Frequency | | | $1/t_{DCLK}$ | 23.1 | 27 | 30.9 | MHz | |
| HSYNC | Period | | $t_H$ | 1684 | 1716 | 1807 | $t_{DCLK}$ | |
| | Display period | | $t_{hd}$ | 1440 | | | $t_{DCLK}$ | |
| | Back porch | | $t_{hbp}$ | 236 | 252 | 267 | $t_{DCLK}$ | |
| | Front porch | | $t_{hfp}$ | $t_H - t_{hd} - t_{hbp}$ | | | $t_{DCLK}$ | |
| | Pulse width | | $t_{hsw}$ | 1 | 1 | 96 | $t_{DCLK}$ | |
| VSYNC | Period | Odd | $t_V$ | 247 | 262 | 277 | $t_H$ | Note 1, 2 |
| | | Even | | | | | | |
| | Display period | Odd | $t_{vd}$ | 240 | | | $t_H$ | |
| | | Even | | | | | | |
| | Back porch | Odd | $t_{vbp}$ | 6 | 13 | 21 | $t_H$ | |
| | | Even | | 6.5 | 13.5 | 21.5 | | |
| | Front porch | Odd | $t_{vfp}$ | $t_V - t_{vd} - t_{vbp}$ | | | $t_H$ | |
| | | Even | | | | | | |
| | Pulse width | Odd | $t_{vsw}$ | 1 $t_{DCLK}$ | $1t_H$ | $6t_H$ | | |
| | | Even | | | | | | |

Note 1: AUO suggests frame rate at least 50 Hz to get the better display quality.

Note 2: Both interlace and non-interlace mode can be accepted.

**Fig.4 UPS052 Input Horizontal Timing Chart**

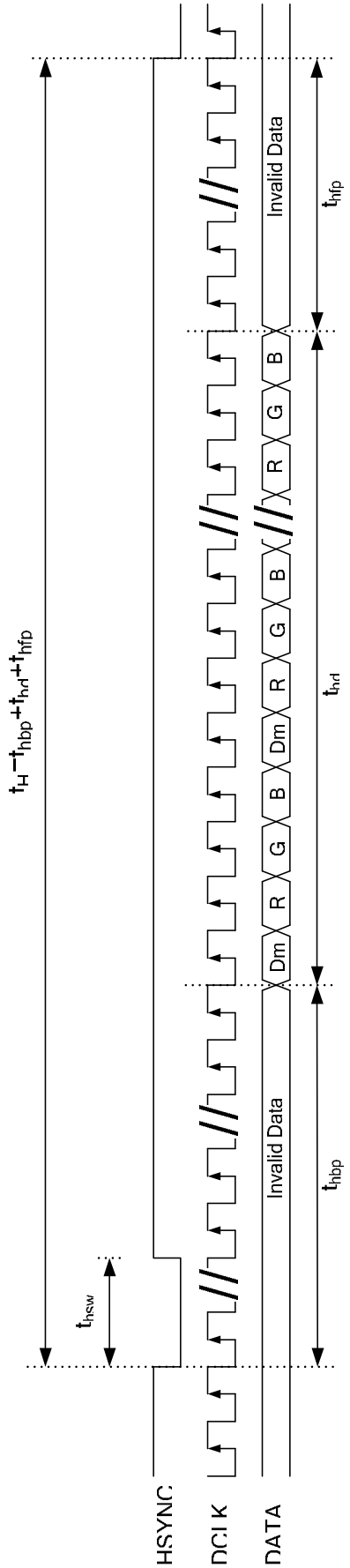
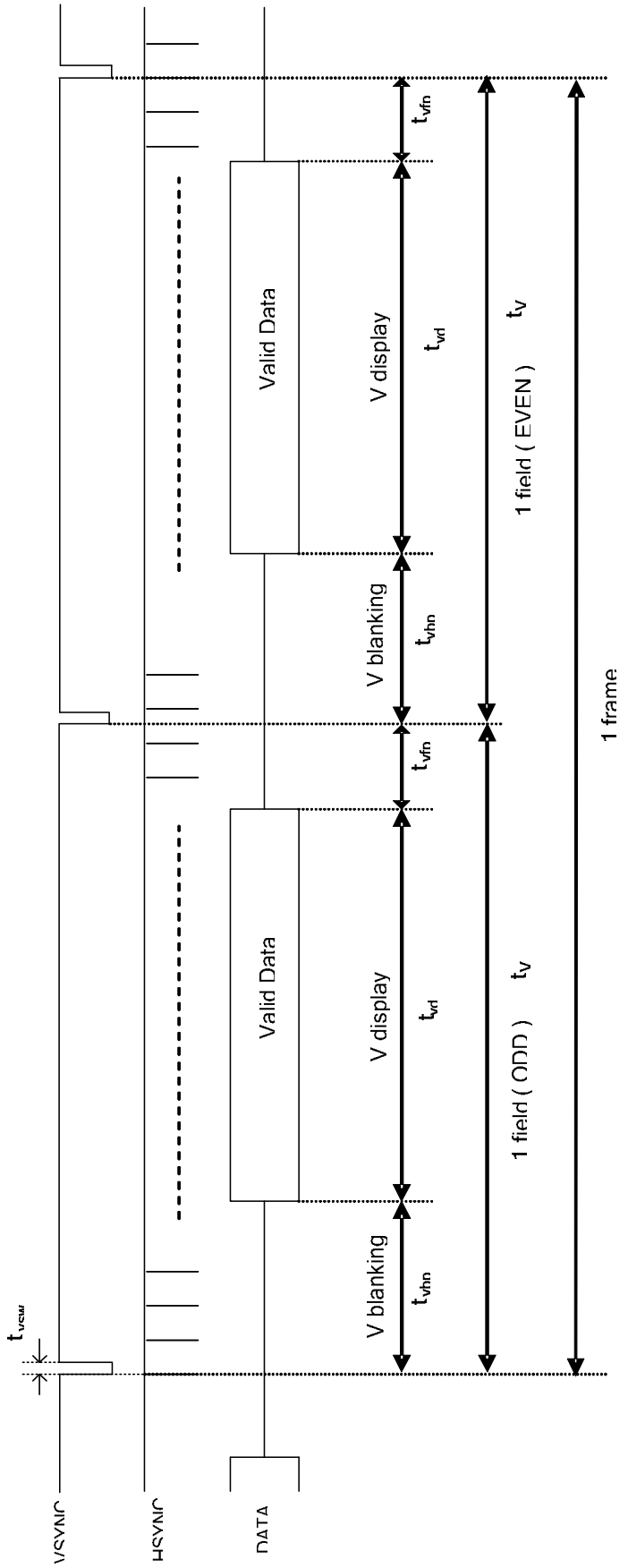
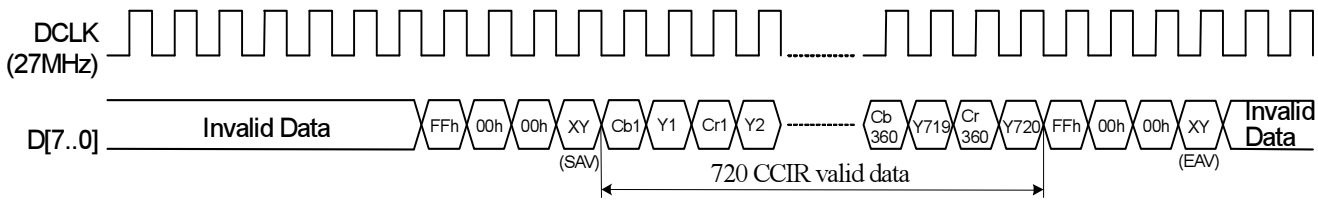


**Fig.5 UPS052 Input Vertical Timing Chart**



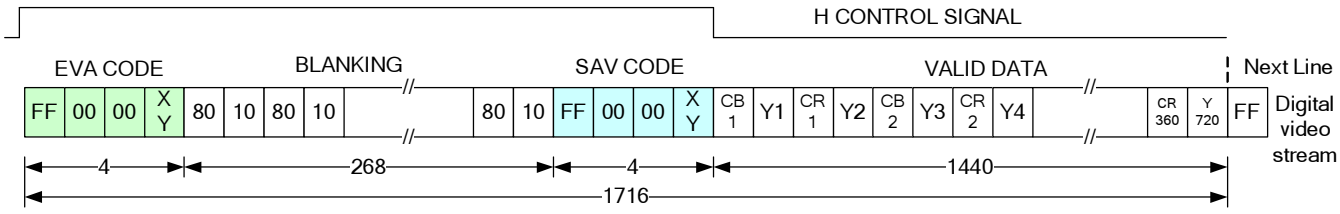
### d. CCIR656 Timing conditions

d - 1. CCIR656 timing specifications




## CCIR656 Data input format

Example:
H control signal =1 at EAV;
H control signal =0 at SAV;




d- 2. CCIR656 decoding

FF 00 00 XY signals are involved with HSYNC,VSYNC and Field

XY encode following bits:

F=field select

V=indicate vertical blanking

H=1 if EAV else 0 for SAV

P3-P0=protection bits

P3=V□H P2=F□H P1=F□V P0=F□V□H

□represents the exclusive-OR function.

Control is provided through “End of Video” (EAV) and “Start of Video” (SAV) timing references.

Horizontal blanking section consists of repeating pattern 80 10 80 10

| XY | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
| 1 | F | V | H | P3 | P2 | P1 | P0 |

d- 3. CCIR656 to RGB conversion

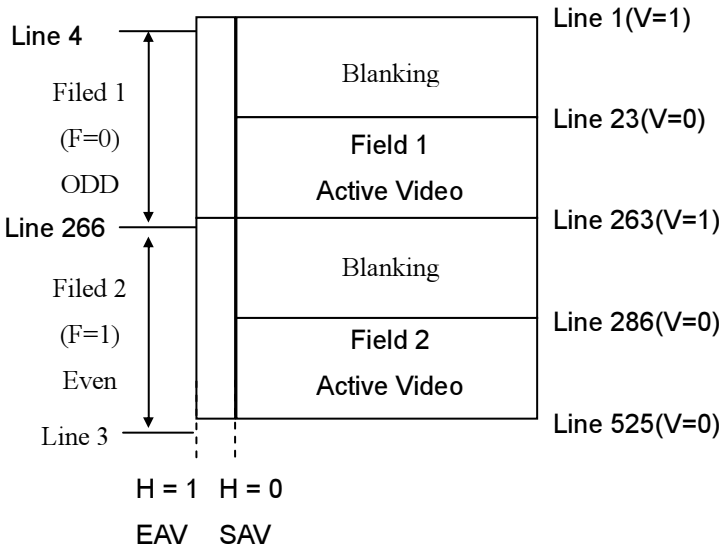
R=1.164 (Y-16) +1.596(Cr-128)

G=1.164 (Y-16) -0.813(Cr-128)-0.392(Cb-128)

B=1.164 (Y-16) +2.017(Cb-128)

Where Y: 0~255 Cr: 0~255 Cb: 0~255

d- 4. CCIR656 Vertical Timing Format (NTSC)




| Line Number | F | V | H (EAV) | H (SAV) |
|---|---|---|---|---|
| 1-3 | 1 | 1 | 1 | 0 |
| 4-22 | 0 | 1 | 1 | 0 |
| 23-262 | 0 | 0 | 1 | 0 |
| 263-265 | 0 | 1 | 1 | 0 |
| 266-285 | 1 | 1 | 1 | 0 |
| 286-525 | 1 | 0 | 1 | 0 |

| | F | H | V |
|---|---|---|---|
| 1 | Even Field | EAV | Blanking |
| 0 | Odd Field | SAV | Active Video |

**Note: After setting CCIR656 vertical timing value, the frame might be shift. AUO suggests to set the register R5 = "04h", then the frame should be fulled.**

### e. YUV Timing

e - 1. YUV 640 timing specifications

| Parameter | | | Symbol | Min. | Typ. | Max. | Unit. | Remark |
|---|---|---|---|---|---|---|---|---|
| DCLK Frequency | | | $1/t_{DCLK}$ | 21.07 | 24.55 | 28.06 | MHz | |
| HSYNC | Period | | $t_H$ | 1524 | 1560 | 1644 | $t_{DCLK}$ | |
| | Display period | | $t_{hd}$ | 1280 | | | $t_{DCLK}$ | |
| | Back porch | | $t_{hbp}$ | 236 | 252 | 267 | $t_{DCLK}$ | |
| | Front porch | | $t_{hfp}$ | $t_H - t_{hd} - t_{hbp}$ | | | $t_{DCLK}$ | |
| | Pulse width | | $t_{hsw}$ | 1 | 1 | 96 | $t_{DCLK}$ | |
| VSYNC | Period | Odd | $t_V$ | 247.5 | 262.5 | 277.5 | $t_H$ | Note 1, 2 |
| | | Even | | | | | | |
| | Display period | Odd | $t_{vd}$ | 240 | | | $t_H$ | |
| | | Even | | | | | | |
| | Back porch | Odd | $t_{vbp}$ | 6 | 13 | 21 | $t_H$ | |
| | | Even | | 6.5 | 13.5 | 21.5 | | |
| | Front porch | Odd | $t_{vfp}$ | $t_V - t_{vd} - t_{vbp}$ | | | $t_H$ | |
| | | Even | | | | | | |
| | Pulse width | Odd | $t_{vsw}$ | 1 $t_{DCLK}$ | $1t_H$ | $6t_H$ | | |
| | | Even | | | | | | |

Note 1: AUO suggests frame rate at least 50 Hz to get the better display quality.

Note 2: Both interlace and non-interlace mode can be accepted.

e - 2. YUV 720 timing specifications

| Parameter | | | Symbol | Min. | Typ. | Max. | Unit. | Remark |
|---|---|---|---|---|---|---|---|---|
| DCLK Frequency | | | $1/t_{DCLK}$ | 23.1 | 27 | 30.9 | MHz | |
| HSYNC | Period | | $t_H$ | 1684 | 1716 | 1807 | $t_{DCLK}$ | |
| | Display period | | $t_{hd}$ | 1440 | | | $t_{DCLK}$ | |
| | Back porch | | $t_{hbp}$ | 236 | 252 | 267 | $t_{DCLK}$ | |
| | Front porch | | $t_{hfp}$ | $t_H - t_{hd} - t_{hbp}$ | | | $t_{DCLK}$ | |
| | Pulse width | | $t_{hsw}$ | 1 | 1 | 96 | $t_{DCLK}$ | |
| VSYNC | Period | Odd | $t_V$ | 247.5 | 262.5 | 277.5 | $t_H$ | Note 1, 2 |
| | | Even | | | | | | |
| | Display period | Odd | $t_{vd}$ | 240 | | | $t_H$ | |
| | | Even | | | | | | |
| | Back porch | Odd | $t_{vbp}$ | 6 | 13 | 21 | $t_H$ | |
| | | Even | | 6.5 | 13.5 | 21.5 | | |
| | Front porch | Odd | $t_{vfp}$ | $t_V - t_{vd} - t_{vbp}$ | | | $t_H$ | |
| | | Even | | | | | | |
| | Pulse width | Odd | $t_{vsw}$ | 1 $t_{DCLK}$ | $1t_H$ | $6t_H$ | | |
| | | Even | | | | | | |

Note 1: AUO suggests frame rate at least 50 Hz to get the better display quality.

Note 2: Both interlace and non-interlace mode can be accepted.

**Fig.8 YUV640 Input Horizontal Timing Chart**

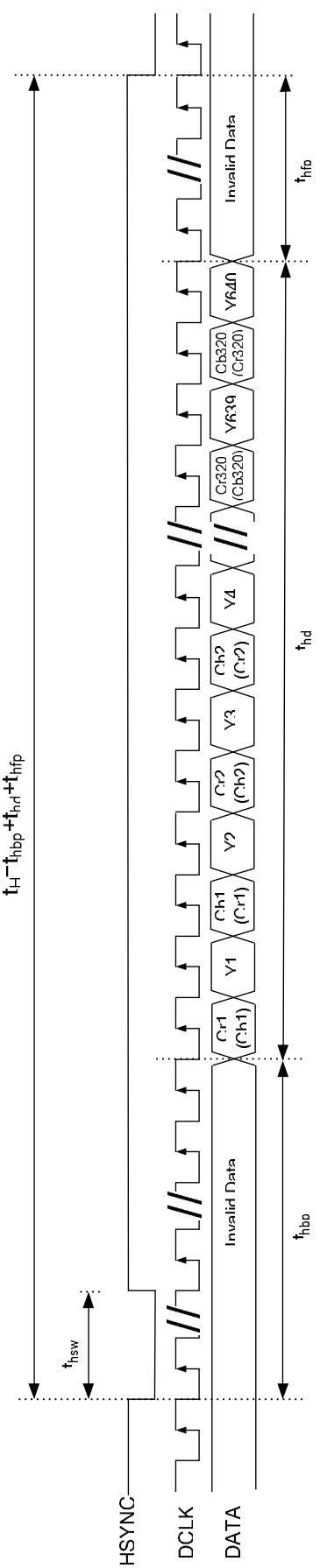



**Fig.7 YUV720 Input Horizontal Timing Chart**

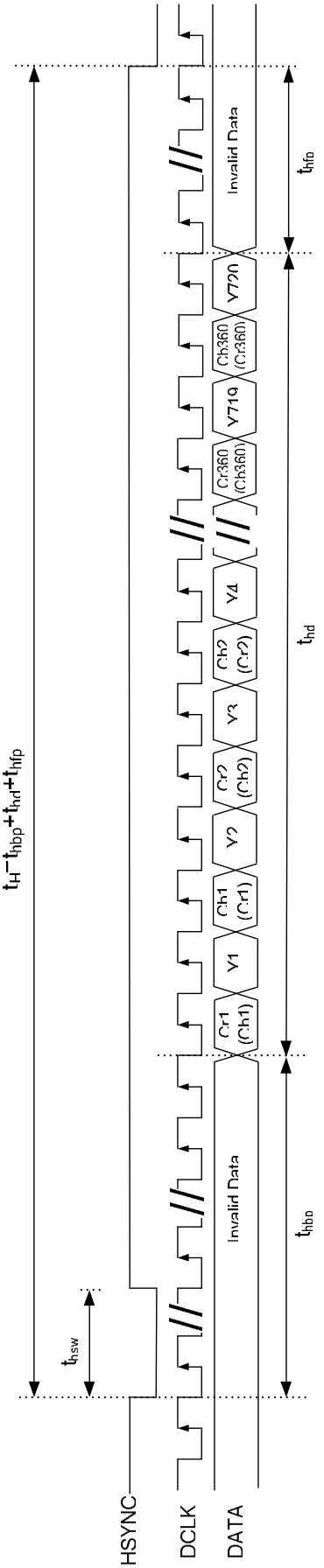
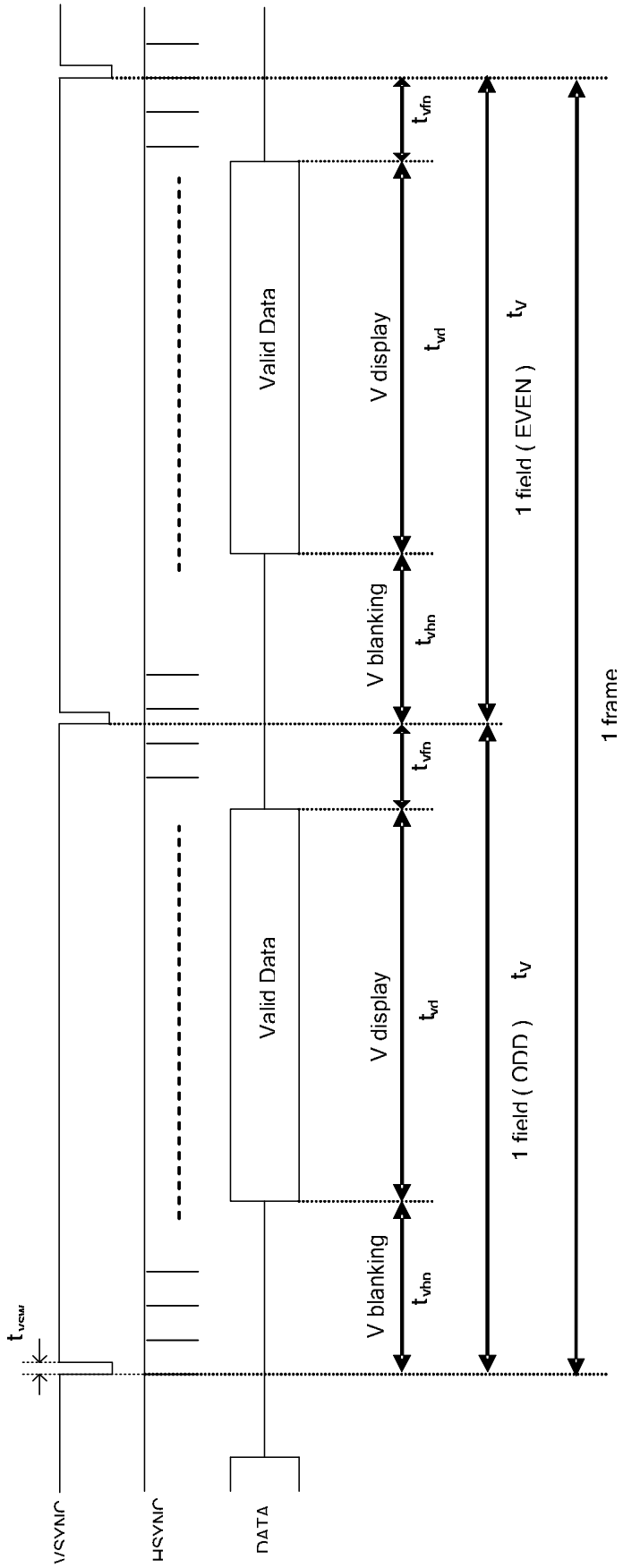
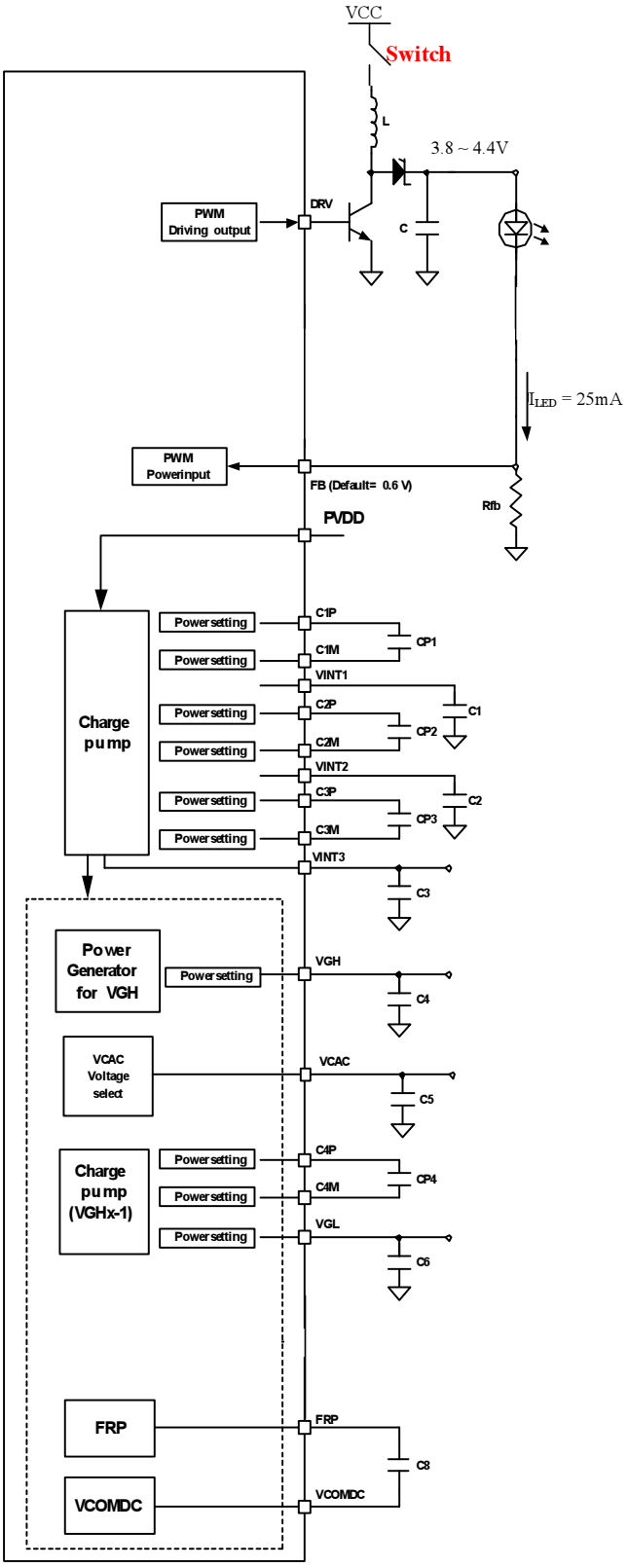


**Fig.5 YUV Input Vertical Timing Chart**

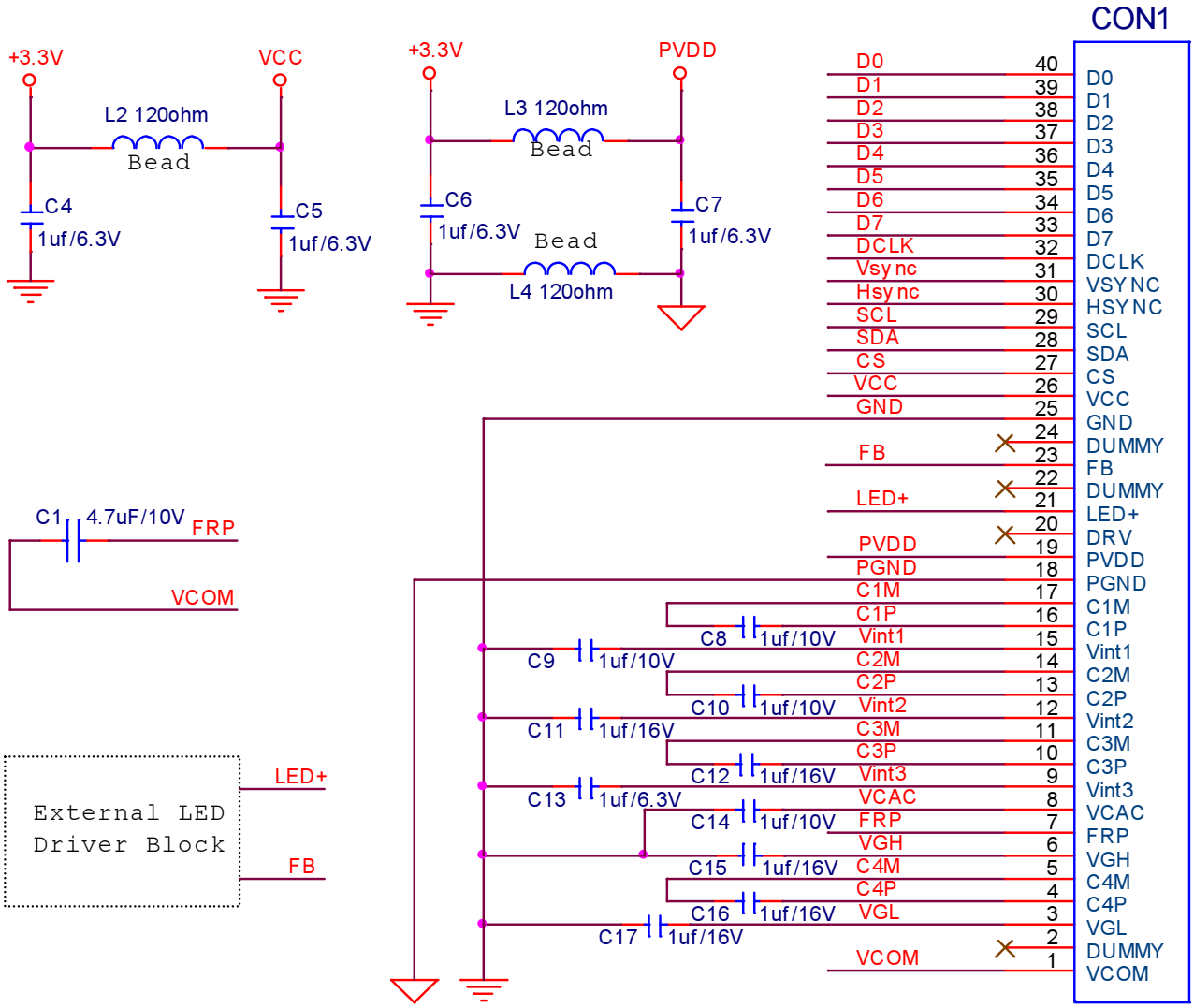


## 5. Charge Pump Structure



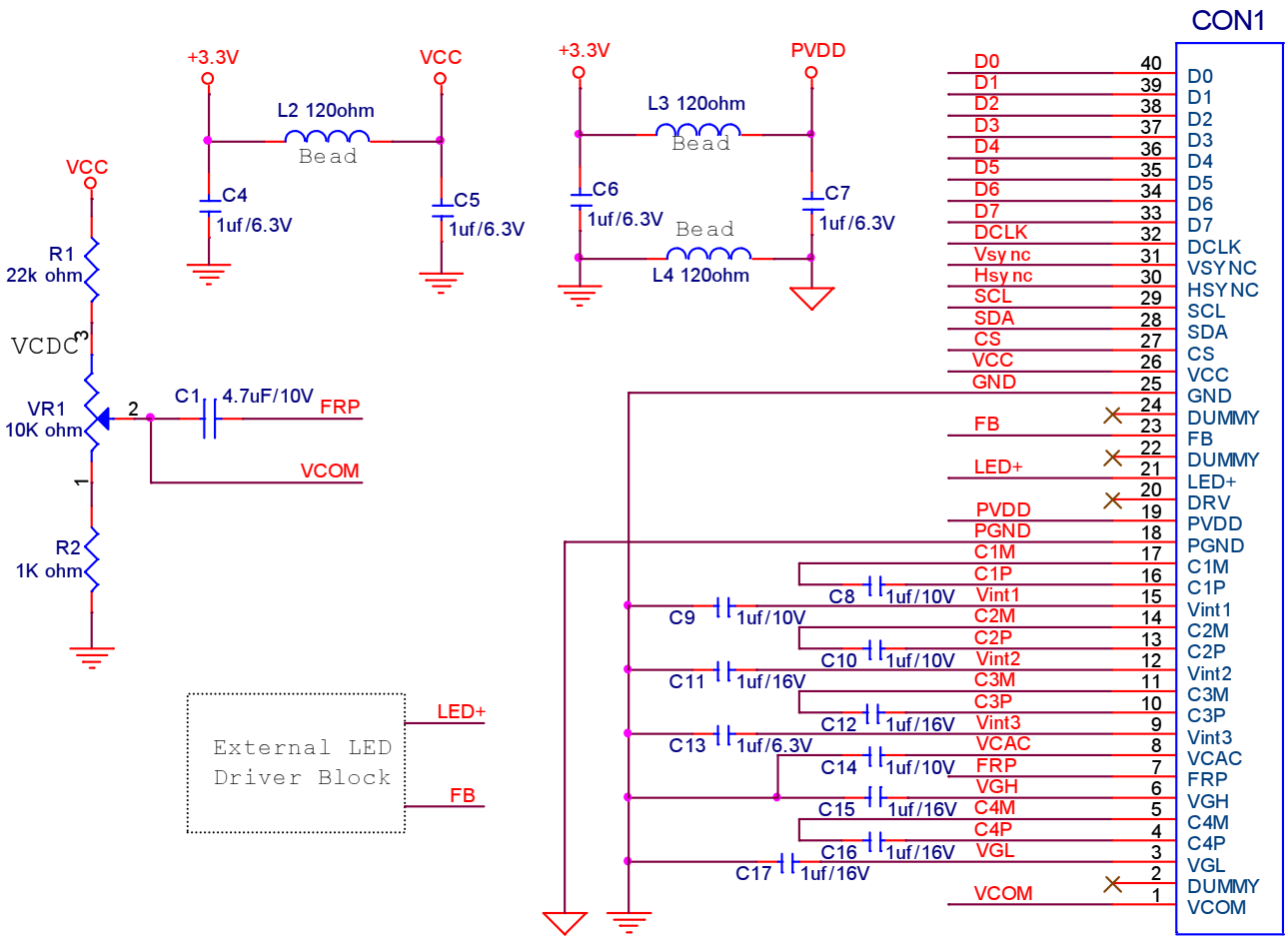
## 6. Reference Circuit

➢ External LED driver + Internal VCOMDC application circuit



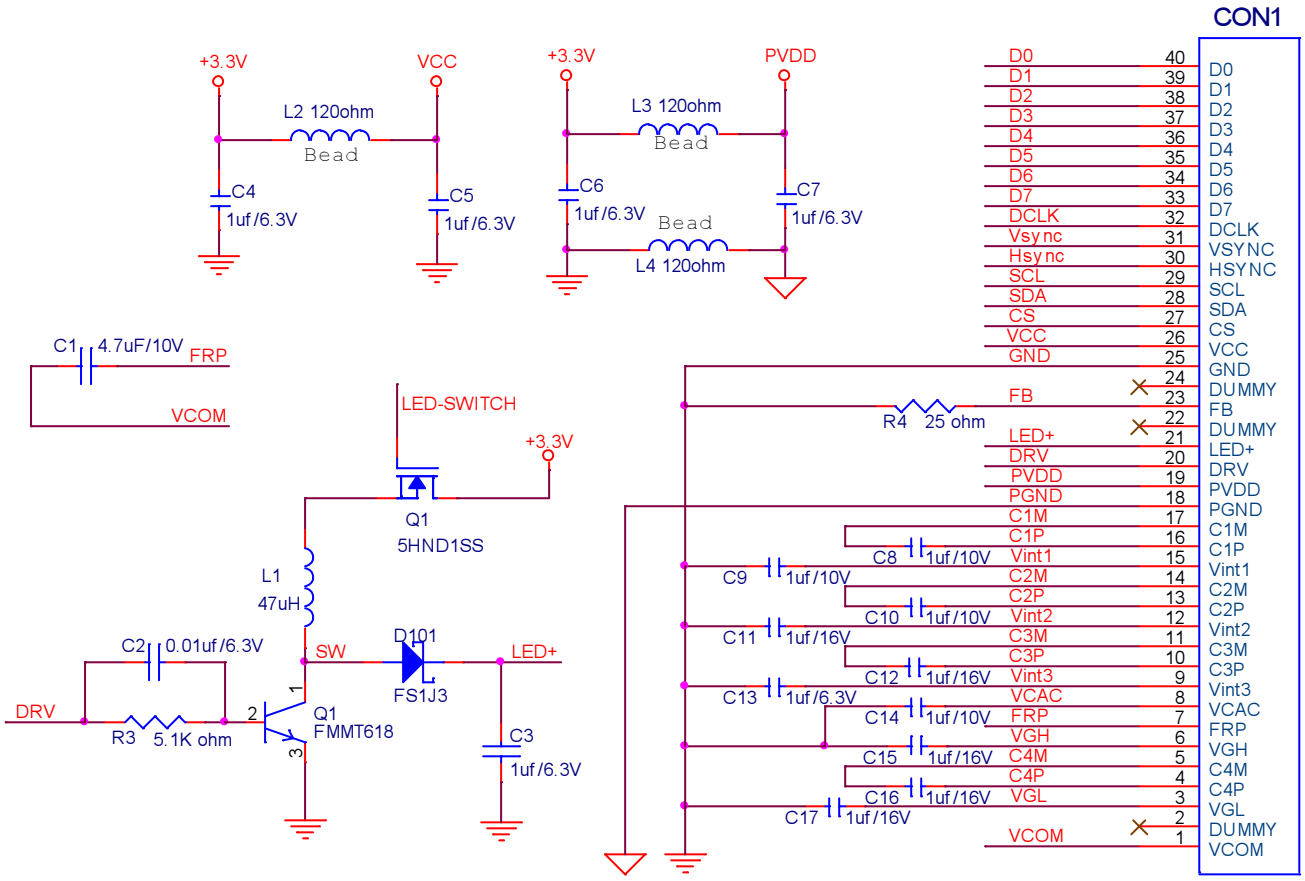

**Note:** +3.3V is provided from system.

➢ External LED driver + External VCOMDC application circuit




**Note:** +3.3V is provided from system.

➢ Internal LED driver + Internal VCOMDC application circuit




**Note:** PWM R/C/L (R3/C2/L1) parameters and component characteristics will effects efficiency and wave like noise. The application circuit is for reference only. If efficiency is not god or wave like noise is serious, please adjust RCL parameters to get best efficiency and display quality.

**Note:** +3.3V is provided from system.

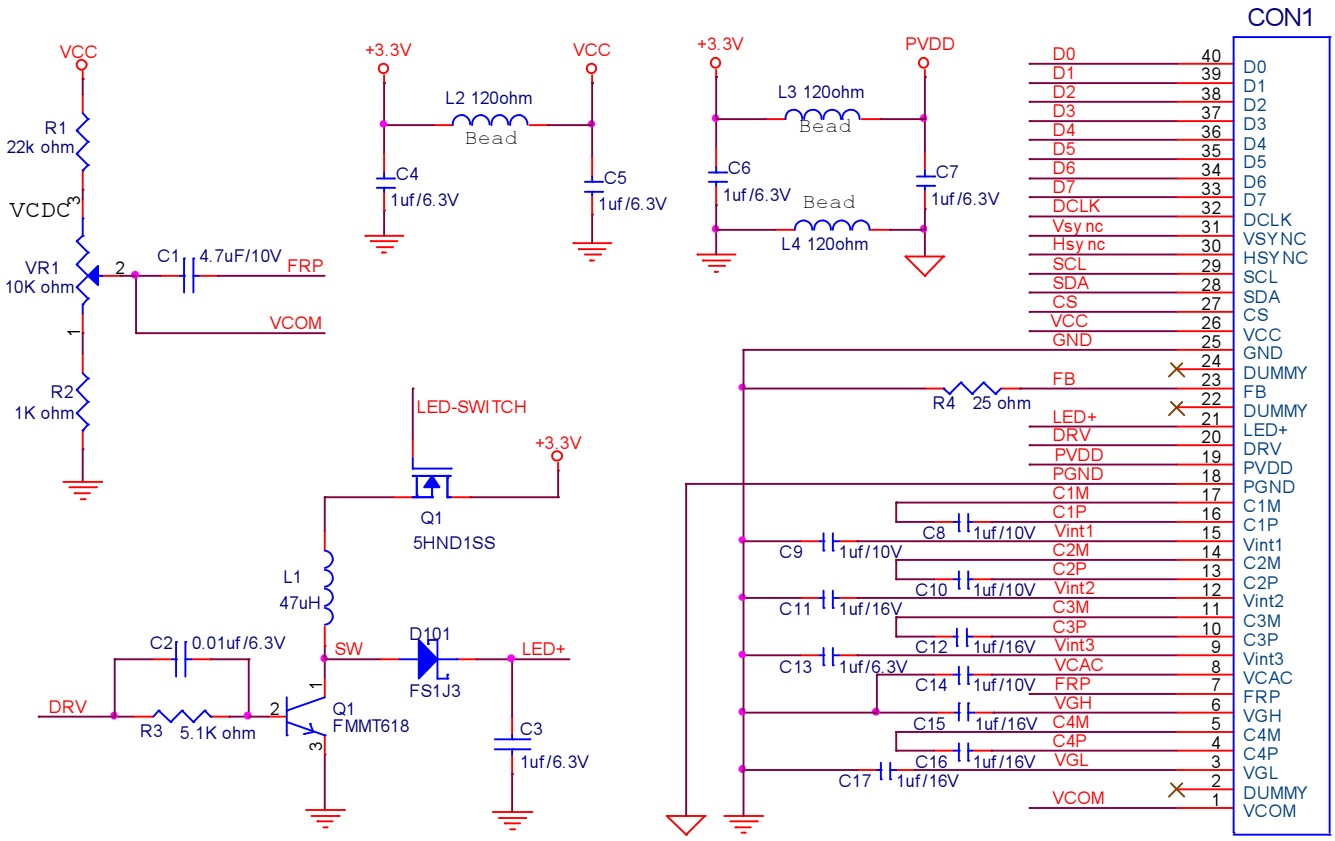
**Note:** Q1 is control backlight turn on/off function.

* LED-SWITCH is “H” ➔ backlight turn on.

* LED-SWITCH is “L” ➔ backlight turn off.

Please refer to suggestion standby and power on/off sequence.

➢ Internal LED driver + External VCOMDC application circuit




**Note:** PWM R/C/L (R3/C2/L1) parameters and component characteristics will effects efficiency and wave like noise. The application circuit is for reference only. If efficiency is not god or wave like noise is serious, please adjust RCL parameters to get best efficiency and display quality.

**Note:** +3.3V is provided from system.

**Note:** Q1 is control backlight turn on/off function.

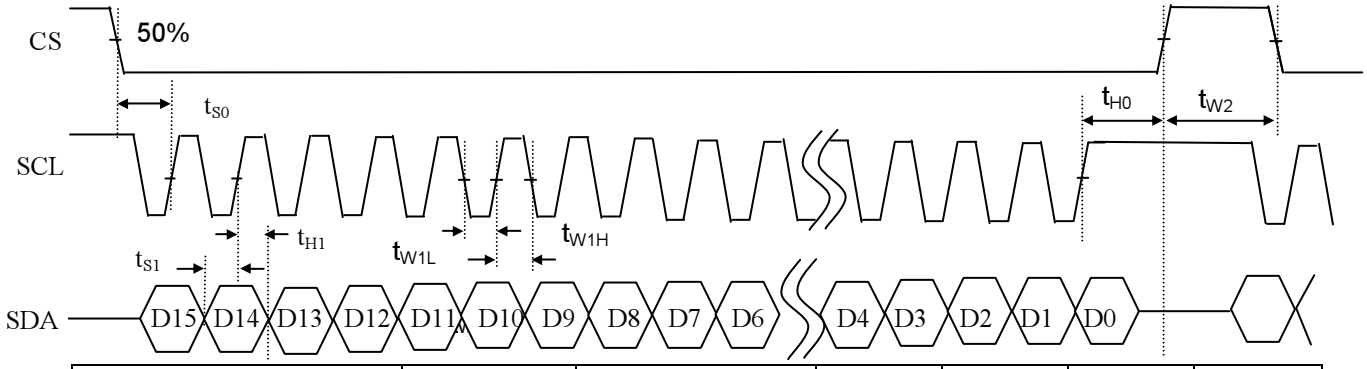
* LED-SWITCH is “H” ➔ backlight turn on.

* LED-SWITCH is “L” ➔ backlight turn off.

Please refer to suggestion standby and power on/off sequence.

## 7. Serial Interface & Register Table

### a. Serial Interface format




| Item | Symbol | Conditions | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| Data Setup Time | $t_{S0}$ | SCL to CS | 120 | | | ns |
| | $t_{S1}$ | SCL to SDA | 120 | | | ns |
| Data Hold Time | $t_{H0}$ | SCL to CS | 120 | | | ns |
| | $t_{H1}$ | SCL to SDA | 120 | | | ns |
| Pulse Width | $t_{W1L}$ | SCL pulse width | 120 | | | ns |
| | $t_{W1H}$ | SCL pulse width | 120 | | | ns |
| | $t_{W2}$ | CS pulse width | 1000 | | | ns |

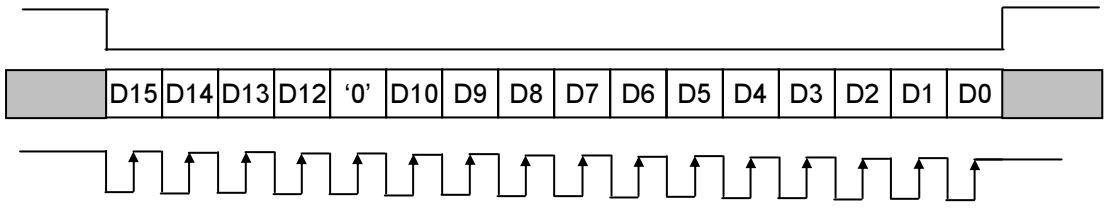
### b. The configuration of serial data at SDA terminal is at below

MSB LSB

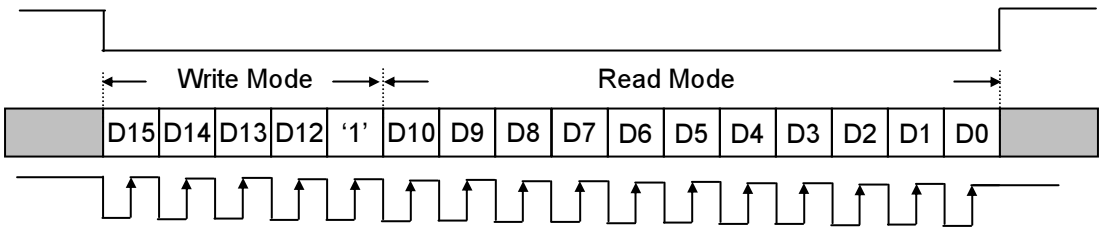
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Register address** | | | | R/W | DATA | | | | | | | | | | |

Note: R/W = '0' ➔ Write mode R/W = '1' ➔ Read mode

#### b1 – Write Mode waveform




#### b2 – Read Mode waveform



### c. Register parameters

| No | ADDRESS | | | | R/W | | CONTENT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D15 | D14 | D13 | D12 | D11 | D[10 : 8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R0 | 0 | 0 | 0 | 0 | W | x | x | x | x | x | GRB | STB | SHDB | SHCB |
| R1 | 0 | 0 | 1 | 0 | W | x | x | x | Reserved | | | Reserved | PFON | Reserved |
| R2 | 0 | 1 | 0 | 0 | W | x | x | x | x | x | FPOL | x | U/D | SHL |
| R3 | 0 | 1 | 1 | 0 | W | x | x | x | x | PALM | PAL | SEL | | |
| R4 | 1 | 0 | 0 | 0 | W | x | x | x | x | DDL | | | | |
| R5 | 1 | 0 | 1 | 0 | W | x | x | x | OEA | | HDL | | | |
| R6 | 1 | 1 | 0 | 0 | W | x | x | x | x | x | x | VCSL | | |
| R7 | 1 | 1 | 1 | 0 | W | x | x | x | x | GAMSEL | x | VLNC | AVGY | Reserved |
| T0 | 0 | 0 | 0 | 1 | W | x | AVDDADJ | | | PDTY | | FBV2 | FBV1 | FBV0 |
| T1 | 0 | 0 | 1 | 1 | W | x | x | AVG | x | T352 | CONST | | | |
| T2 | 0 | 1 | 0 | 1 | W | x | x | VDCEN | VCOMDC | | | | | |
| T3 | 0 | 1 | 1 | 1 | W | x | x | BRADJ | | | | | | |
| T4 | 1 | 0 | 0 | 1 | W | x | x | x | x | x | x | x | VNSEL | |
| T5 | 1 | 0 | 1 | 1 | W | x | SAT | | | | HUE | | | |
| T6 | 1 | 1 | 0 | 1 | R | x | Reserved | | | | | | | |

Note 1: Please keep all the Reserved register at "**Default Value**" to avoid abnormal display.

Note 2: Register T6 is read only.

c1 - Default register settings

| No | D15 | D14 | D13 | D12 | D11 | D[10 : 8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R0 | 0 | 0 | 0 | 0 | R/W | x | x | x | x | x | 1 | 1 | 0 | 1 |
| R1 | 0 | 0 | 1 | 0 | R/W | x | x | x | 0 | 0 | 0 | 0 | 0 | 1 |
| R2 | 0 | 1 | 0 | 0 | R/W | x | x | x | x | x | 0 | x | 1 | 1 |
| R3 | 0 | 1 | 1 | 0 | R/W | x | x | x | x | 0 | 0 | 0 | 0 | 1 |
| R4 | 1 | 0 | 0 | 0 | R/W | x | x | x | x | 0 | 0 | 0 | 0 | 0 |
| R5 | 1 | 0 | 1 | 0 | R/W | x | x | x | 0 | 0 | 0 | 0 | 0 | 0 |
| R6 | 1 | 1 | 0 | 0 | R/W | x | x | x | x | x | x | 1 | 1 | 0 |
| R7 | 1 | 1 | 1 | 0 | R/W | x | x | x | x | 0 | x | 0 | 1 | 1 |
| T0 | 0 | 0 | 0 | 1 | R/W | x | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| T1 | 0 | 0 | 1 | 1 | R/W | x | x | 0 | x | 0 | 1 | 0 | 0 | 0 |
| T2 | 0 | 1 | 0 | 1 | R/W | x | x | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| T3 | 0 | 1 | 1 | 1 | R/W | x | x | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| T4 | 1 | 0 | 0 | 1 | R/W | x | x | x | x | x | x | x | 0 | 0 |
| T5 | 1 | 0 | 1 | 1 | R/W | x | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| T6 | 1 | 1 | 0 | 1 | R | x | Reserved | | | | | | | |

"X" => Don't care.

### d. Detail Register Description

d1. Register R0

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 0000 | [3..0] | Bit3 (GRB) | Global reset. | 1101b |
| | | Bit2 (STB) | Standby mode setting. | |
| | | Bit1 (SHDB) | DC-DC converter shutdown setting. | |
| | | Bit0 (SHCB) | Charge Pump shutdown setting. | |

| Bit3 | GRB function |
|---|---|
| **0** | The controller is resets, DCDC is off.<br>Reset all register to default value. |
| 1 | Normal operation. (default) |

Note: When setting GRB='0', charge pump is still on, because of default value.

| Bit2 | STB function |
|---|---|
| 0 | T-CON, source driver and DC-DC converter are off. All outputs are High-Z. |
| 1 | Normal operation. (default) |

Note: GRB have higher priority than STB. Therefore, two mode is set in the same time, STB isn't executed.

| Bit1 | SHDB function |
|---|---|
| 0 | DC-DC converter is off. (default) |
| 1 | DC-DC converter is on.<br>DC-DC controls by STB and power on/off sequence. |

| Bit0 | SHCB function |
|---|---|
| 0 | Charge Pump converter is off. |
| 1 | Charge Pump converter is on. (default)<br>Charge Pump controls by STB and power on/off sequence. |

d2. Register R1:

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 0010 | [5..0] | Reserved | Reserved | 00_0001b |
| | | Reserved | Reserved | |
| | | Bit1 (PFON) | Pre-filter setting. | |
| | | Bit0 (D/S) | Select Delta or Stripe mode for Data arrangement. | |

| Bit1 | Pre-filter setting. |
|---|---|
| 0 | Pre-filter off (default) |
| 1 | Pre-filter on |

Note:Disable this function in UPS051mode.

| Bit0 | D/S function |
|---|---|
| 0 | Stripe mode. Q1H always stays High.<br>Data alignment always odd line. |
| 1 | Delta mode Q1H toggles each line. Data alignment switches between Odd/even lines. (default) |

Note:Disable this function in UPS051mode.

d3. Register R2:

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 0100 | [3..0] | Bit3 (FPOL) | FRP source driver polarity inversion polarity inversion selection. | 0011b |
| | | Bit1 (U/D) | Vertical shift direction selection. | |
| | | Bit0 (SHL) | Horizontal shift direction selection. | |

| Bit3 | FPOL function |
|---|---|
| 0 | FRP=0 when positive polarity<br>FRP=1 when negative polarity (default) |
| 1 | FRP=1 when positive polarity<br>FRP=0 when negative polarity |

| Bit1 | UD function |
|---|---|
| 0 | Scan down: First line=G241 → G239 → … → G2 → Last line=G0. |
| 1 | Scan up: First line=G0→ G2 →…→ G239 → Last line=G241. (default) |

| Bit0 | SHL function |
|---|---|
| 0 | Shift left; First data=S640 → S639 → …→ S2 → Last data=S1. |
| 1 | Shift right: First data=S1→ S2 → …→ S639→ Last data=S640. (default) |

d4. Register R3:

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 0110 | [4..0] | Bit4 (PALM) | PAL 1/6, PAL1/6,8 selection. | 0_0001b |
| | | Bit3 (PAL) | PAL/NTSC selection. | |
| | | Bit2-0 (SEL) | Input data format selection. | |

| Bit4 | PALM function |
|---|---|
| 0 | PAL 1/6,8 Input format. (280 active line). (default) |
| 1 | PAL1/6 Input format. (288 active line). |

Note:Disable this function in UPS051mode.

| Bit3 | PAL function |
|---|---|
| 0 | NTSC Input format (240 active line). (default) |
| 1 | PAL Input format. |

Note:Disable this function in UPS051mode.

| Bit2-0 | SEL function |
|---|---|
| 000 | UPS051 path, special data format: DDX. |
| 001 | UPS052 320RGB 24.54MHz data format. (default) |
| 010 | UPS052 360RGB 27MHz data format. |
| 011 | YUV mode A 640Y 320CrCb 24.54MHz data format. |
| 100 | YUV mode A 720Y 360CrCb 27MHz data format. |
| 101 | YUV mode B 640Y 320CrCb 24.54MHz data format. |
| 110 | YUV mode B 720Y 360CrCb 27MHz data format. |
| 111 | CCIR 656 720Y 360CrCb 27MHz data format. |

d5. Register R4:

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 1000 | [4..0] | Bit4-0 (DDL) | Horizontal Data start delay selection. | 0_0000b |

| D4 | D3 | D2 | D1 | D0 | Value | Unit |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | +0 | DCLK |
| 0 | 0 | 0 | 0 | 1 | +1 | |
| 0 | 0 | 0 | 1 | 0 | +2 | |
| 0 | 0 | 0 | 1 | 1 | +3 | |
| 0 | 0 | 1 | 0 | 0 | +4 | |
| 0 | 0 | 1 | 0 | 1 | +5 | |
| 0 | 0 | 1 | 1 | 0 | +6 | |
| 0 | 0 | 1 | 1 | 1 | +7 | |
| 0 | 1 | 0 | 0 | 0 | +8 | |
| 0 | 1 | 0 | 0 | 1 | +9 | |
| 0 | 1 | 0 | 1 | 0 | +10 | |
| 0 | 1 | 0 | 1 | 1 | +11 | |
| 0 | 1 | 1 | 0 | 0 | +12 | |
| 0 | 1 | 1 | 0 | 1 | +13 | |
| 0 | 1 | 1 | 1 | 0 | +14 | |
| 0 | 1 | 1 | 1 | 1 | +15 | |
| 1 | 0 | 0 | 0 | 0 | -1 | |
| 1 | 0 | 0 | 0 | 1 | -2 | |
| 1 | 0 | 0 | 1 | 0 | -3 | |
| 1 | 0 | 0 | 1 | 1 | -4 | |
| 1 | 0 | 1 | 0 | 0 | -5 | |
| 1 | 0 | 1 | 0 | 1 | -6 | |
| 1 | 0 | 1 | 1 | 0 | -7 | |
| 1 | 0 | 1 | 1 | 1 | -8 | |
| 1 | 1 | 0 | 0 | 0 | -9 | |
| 1 | 1 | 0 | 0 | 1 | -10 | |
| 1 | 1 | 0 | 1 | 0 | -11 | |
| 1 | 1 | 0 | 1 | 1 | -12 | |
| 1 | 1 | 1 | 0 | 0 | -13 | |
| 1 | 1 | 1 | 0 | 1 | -14 | |
| 1 | 1 | 1 | 1 | 0 | -15 | |
| 1 | 1 | 1 | 1 | 1 | -16 | |

d6. Register R5:

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 1010 | [5..0] | Bit5-4 (OEA) | Odd Even advance selection. | 00_0000b |
| | | Bit3-0 (HDL) | Vertical delay selection. | |

| Bit5-4 | OEA function |
|---|---|
| 00 | Display start @HDL delay for Odd and Even field (default) |
| 01 | Display start @HDL delay for Odd field and @HDL+1 for Even field |
| 1X | Display start @HDL+1 delay for Odd field and @HDL for Even field |

| Bit3-0 | HDL function | | | | |
|---|---|---|---|---|---|
| HDL3 | HDL2 | HDL1 | HDL0 | Value | Unit |
| 0 | 0 | 0 | 0 | +0 | H |
| 0 | 0 | 0 | 1 | +1 | |
| 0 | 0 | 1 | 0 | +2 | |
| 0 | 0 | 1 | 1 | +3 | |
| 0 | 1 | 0 | 0 | +4 | |
| 0 | 1 | 0 | 1 | +5 | |
| 0 | 1 | 1 | 0 | +6 | |
| 0 | 1 | 1 | 1 | +7 | |
| 1 | 0 | 0 | 0 | +8 | |
| 1 | 0 | 0 | 1 | -1 | |
| 1 | 0 | 1 | 0 | -2 | |
| 1 | 0 | 1 | 1 | -3 | |
| 1 | 1 | 0 | 0 | -4 | |
| 1 | 1 | 0 | 1 | -5 | |
| 1 | 1 | 1 | 0 | -6 | |
| 1 | 1 | 1 | 1 | -7 | |

d7. Register R6:

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 1100 | [3..0] | Bit2-0 (VCOM_AC) | VCAC level adjustment. Step 0.1V/LSB. | 110b |

| VCSL2 | VCSL1 | VCSL0 | VCAC level | Unit |
|---|---|---|---|---|
| 0 | 0 | 0 | 4.4 | V |
| 0 | 0 | 1 | 4.5 | |
| 0 | 1 | 0 | 4.6 | |
| 0 | 1 | 1 | 4.7 | |
| 1 | 0 | 0 | 4.8 | |
| 1 | 0 | 1 | 4.9 | |
| 1 | 1 | 0 | 5 (Default) | |
| 1 | 1 | 1 | 5.1 | |

d8. Register R7:

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 1110 | [4..0] | Bit4 (GAMSEL) | Gamma select function | 0_0011 |
| | | Bit2 (VLNC) | YUV vertical line function | |
| | | Bit1 (AVGY) | Average YUV interface Luminance Y setting | |
| | | Bit0 (DMDA) | Delta data alignment | |

| Bit4 | Gamma select function |
|---|---|
| 0 | Non- Linear Gamma (default) |
| 1 | Gamma 2.2 |

| Bit2 | YUV vertical line function |
|---|---|
| 0 | Vertical line are 240 (default) |
| 1 | Vertical line are 234<br>NTSC: 240 lines scaling to 234-skip 6 lines. (1/40)<br>PAL: 288 lines scaling to 234-skip 54 lines (3/16) @ PALM = 'H'<br>280 lines scaling to 234-skip 46 lines (1/6) @ PALM = 'L' |

Note:Use UPS051 mode , this bit must set "0".

| Bit1 | Average YUV interface Luminance Y setting |
|---|---|
| 0 | Only used odd Y sample for YUV conversion |
| 1 | Used odd and even Y sample for YUV conversion (default) |

| Bit0 | Delta data alignment |
|---|---|
| 0 | Data alignment by default setting |
| 1 | Data alignment please reference UPS052 timing graph II. (default)<br>(This function disable in UPS051 mode.) |

d9. Register T0:

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 0001 | [7..0] | Bit5-7 (AVDDADJ) | Select internal AVDD voltage | 0000_0100b |
| | | Bit3-4 (PDTY) | PWM duty control for DC to DC converter | |
| | | Bit2-0 (FBV) | FB voltage adjust | |

| Bit 5- 7 | Select internal AVDD voltage |
|---|---|
| 000 | 4.3V(Default) |
| 001 | 4.4V |
| 010 | 4.5V |
| 011 | 4.6V |
| 100 | 4.7V |
| 101 | 4.8V |
| 110 | 4.9V |
| 111 | 5.0V |

| Bit3-4 | PWM duty control for DC to DC converter |
|---|---|
| 00 | 75 %(Default) |
| 01 | 55 % |
| 10 | 60 % |
| 11 | 65 % |

| Bit2-0 | FB voltage adjust |
|---|---|
| 000 | 0.4V |
| 001 | 0.45V |
| 010 | 0.5V |
| 011 | 0.55V |
| 100 | 0.6V (Default) |
| 101 | 0.65V |
| 110 | 0.7V |
| 111 | 0.75V |

d10. Register T1:

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 0011 | [6..0] | Bit6 (AVG) | Data alignment to scaling down function select | 000_1000b |
| | | Bit4 (T352) | Select UPS052 path and input data format for 352 RGB | |
| | | Bit3-0 (CONST) | RGB contrast level adjustment | |

| Bit6 | Data alignment to scaling down function select |
|---|---|
| 0 | Data alignment by DMDA settling (Default) |
| 1 | Data alignment with averaged and input data.(R1, (G1+3G2)/4, (3B2+B3)/4…….) |

| Bit4 | Select UPS052 path and input data format for 352 RGB |
|---|---|
| 0 | SEL setting timing (Default) |
| 1 | SEL setting don't care, input data for 352 RGB(27MHZ) |

| Bit3-0 | RGB contrast level adjustment |
|---|---|
| 0x0 | 0 |
| 0x8 | 1.00 (Default) |
| 0xF | 1.875 |

d11. Register T2:

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 0101 | [6..0] | Bit6 (VDCEN) | Setting FRP output to add DC level | 010_0000b |
| | | Bit5-0 (VCOM DC) | VCOM DC level adjustment (16mV/Bit) | |

| Bit6 | Setting FRP output to add DC level |
|---|---|
| 0 | External VCOM DC |
| 1 | Internal VCOM DC |

| Bit5-0 | VCOM DC level adjustment |
|---|---|
| 0x00 | 0.688V |
| 0x20 | 1.2V (Default) |
| 0x3F | 1.696V |

d12. Register T3:

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 0111 | [6..0] | Bit6-0 (BRADJ) | Brightness level adjustment (4/Bit) | 100_0000b |

| Bit6 | Brightness level adjustment |
|---|---|
| 0x00 | -256 |
| 0x40 | 0 (Default) |
| 0x7F | +256 |

d13. Register T4:

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 1001 | [2..0] | Bit1-0 (WNSEL) | Wide and narrow display select | 000b |

| Bit1-0 | Wide and narrow display select |
|---|---|
| 00 | Normal display (Default) |
| 01 | Narrow display |
| 10 | Wide display |
| 11 | Normal display |

d14. Register T5:

| Address | Bit | Description | | Default |
|---|---|---|---|---|
| 1011 | [7..0] | Bit7-4 (SAT) | YUV saturation constant adjustment (0.125/Bit) | 1000_1000b |
| | | Bit3-0 (HUE) | YUV Hue adjustment (5Deg/Bit) | |

| Bit7-4 | YUV saturation constant adjustment |
|---|---|
| 0x0 | 0 |
| 0x8 | 1.00 |
| 0xF | 1.875 |

| Bit3-0 | YUV Hue adjustment (5Deg/Bit) |
|---|---|
| 0x0 | -40θ° |
| 0x8 | 0θ° |
| 0xF | 35 θ° |

Note: Register T5 is for YUV only.

## C. Optical specification (Note 1,Note 2, Note 3 )

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|---|
| Response time | Rise | Tr | θ=0° | - | 20 | 30 | ms | Note 4, 6 |
| | Fall | Tf | | - | 30 | 40 | ms | |
| Contrast ratio | | CR | At optimized viewing angle | 150 | 250 | - | | Note 5, 6 |
| Viewing angle | Top | | CR≧10 | 10 | 20 | - | deg. | Note 6, 7 |
| | Bottom | | | 30 | 40 | - | | |
| | Left | | | 40 | 45 | - | | |
| | Right | | | 40 | 45 | - | | |
| Brightness | | | θ=0° | 200 | 250 | - | nits | Note 8 |
| White chromaticity shift | | X | θ=0° | 0.28 | 0.33 | 0.38 | | |
| | | y | | 0.30 | 0.35 | 0.40 | | |
| Uniformity | | $\Delta Y_L$ | % | 70 | 75 | -- | % | Note 10 |

Note 1. Ambient temperature =25±5°.

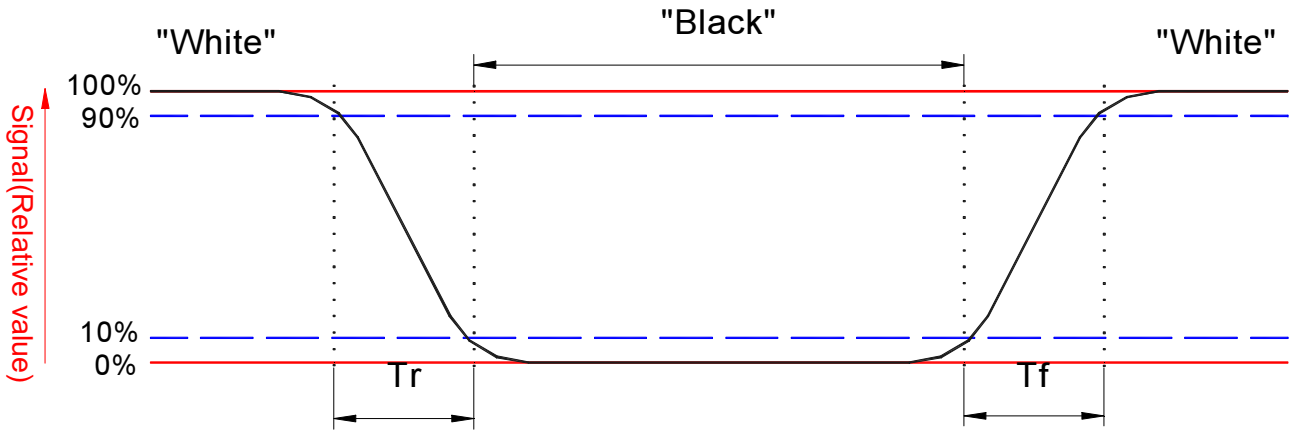
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation under 25 mA.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.




Note 5. Definition of contrast ratio:

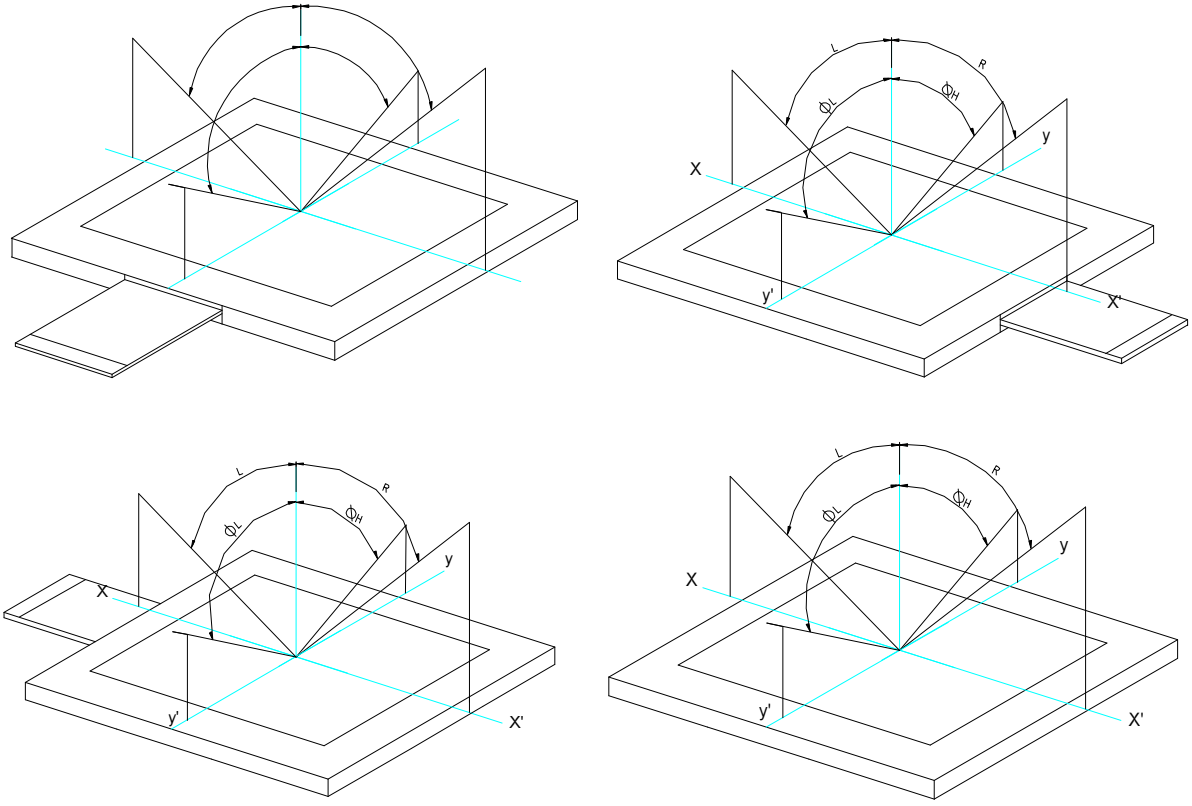
Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. White Vi=$V_{i5}$ $\overline{+}$1.5V
Black Vi=$V_{i50}$ ± 2.0V
"±" Means that the analog input signal swings in phase with COM signal.
" $\overline{+}$ " Means that the analog input signal swings out of phase with COM signal.
$V_{i50}$ : The analog input voltage when transmission is 50%
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

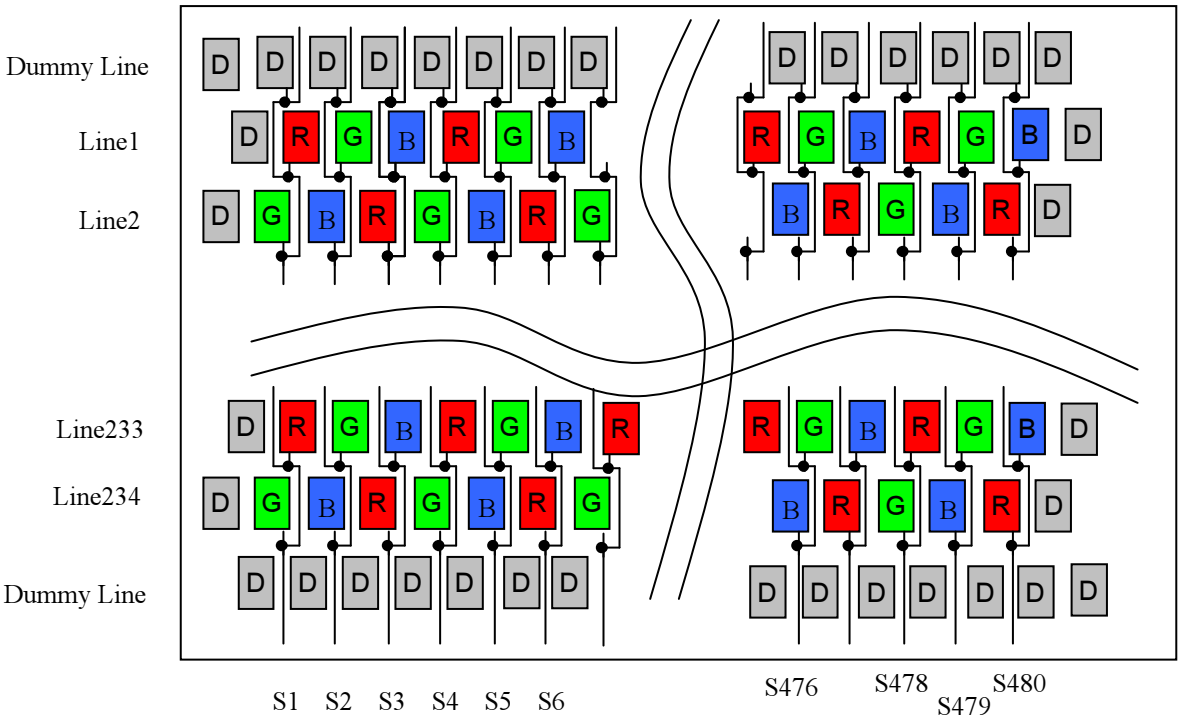
Note 7. Definition of viewing angle:

Refer to figure as below.

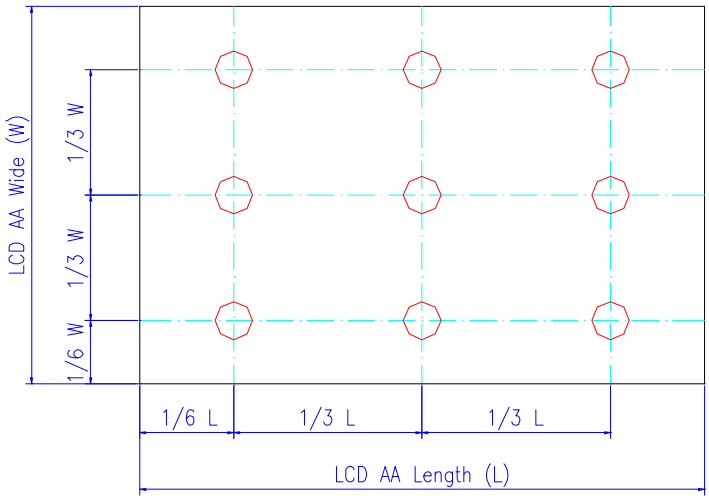



Note 8. Measured at the center area of the panel in gray level 255

Note 9 CF Arrangement




Note 10. Luminance Uniformity of these 9 points is defined as below:



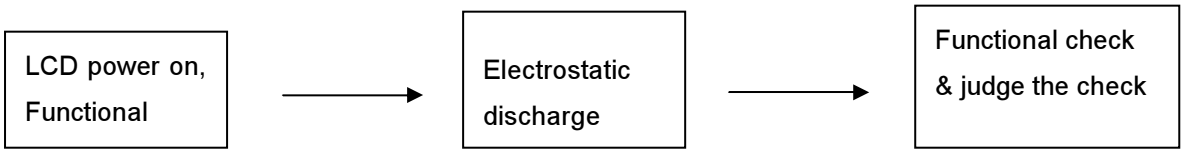

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

## D. Reliability test items:

| No. | Test items | Conditions | Remark |
|---|---|---|---|
| 1 | High temperature storage | Ta= 70□ 240Hrs | |
| 2 | Low temperature storage | Ta= -25□ 240Hrs | |
| 3 | High temperature operation | Ta= 60□ 240Hrs | |
| 4 | Low temperature operation | Ta= 0□ 240Hrs | |
| 5 | High temperature and high humidity | Ta= 60□. 90% RH 240Hrs | Operation |
| 6 | Heat shock | -25□~80□/50 cycle 2Hrs/cycle | Non-operation |
| 7 | Electrostatic discharge | Air mode:+/- 8KV<br>Contact mode: +-4kV | Base on AUO's<br>Standard testing method |
| 8 | Vibration (with carton) | Random vibration:<br>0.015G$^2$/Hz from 5~200Hz<br>–6dB/Octave from 200~500Hz | IEC 68-34 |
| 9 | Drop (with carton) | Height: 60cm<br>1 corner, 3 edges, 6 surfaces | |

Note: Ta: Ambient temperature.

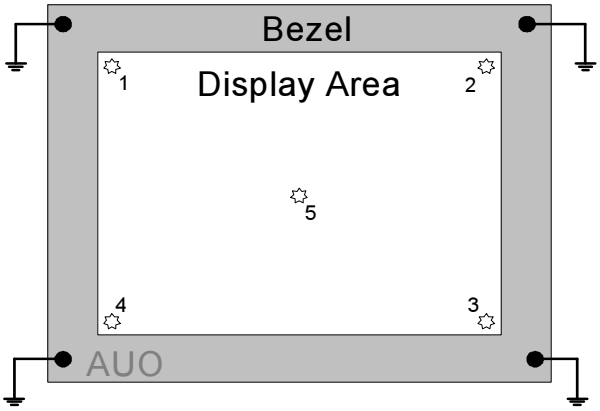
Note 2. ESD Testing Flow as the below




Note 3. ESD testing method.

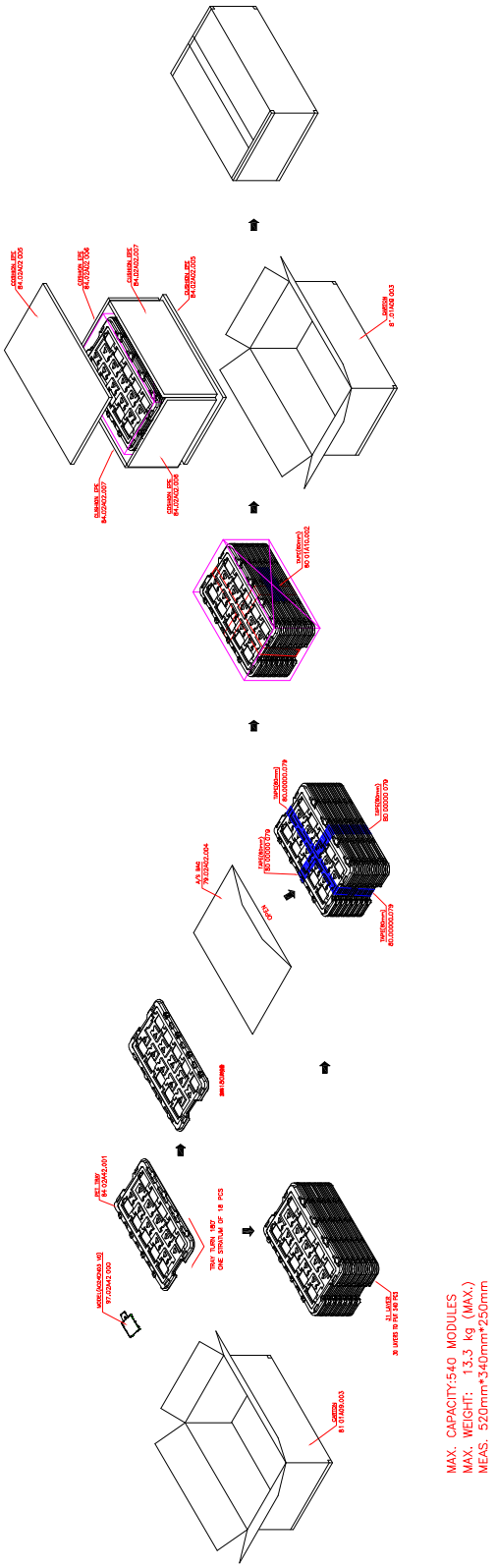
1. Ambient: 24~26□, 56~65%RH
2. Instruments:NoisekenESS-2000,
3. Operation System: "CT30AA-A" and adapter "A024CN02 VXT0"
4. Test Mode: Operating mode, test pattern: colorbar+8Gray scale
5. Test Method:
   a. Contact Discharge: Max±20KV, 150pF(330Ω) 1sec, 5 points, 10 times/point
   b. Air Discharge: Max ±20KV, 150pF(330Ω) 1sec, 5 points, 10 times/point

6. Test point:




7. The metal casing is connected to ground (0V) at four corners.
8. All register commands are repeating transfer.

## E. Packing form



## F. Outline dimension

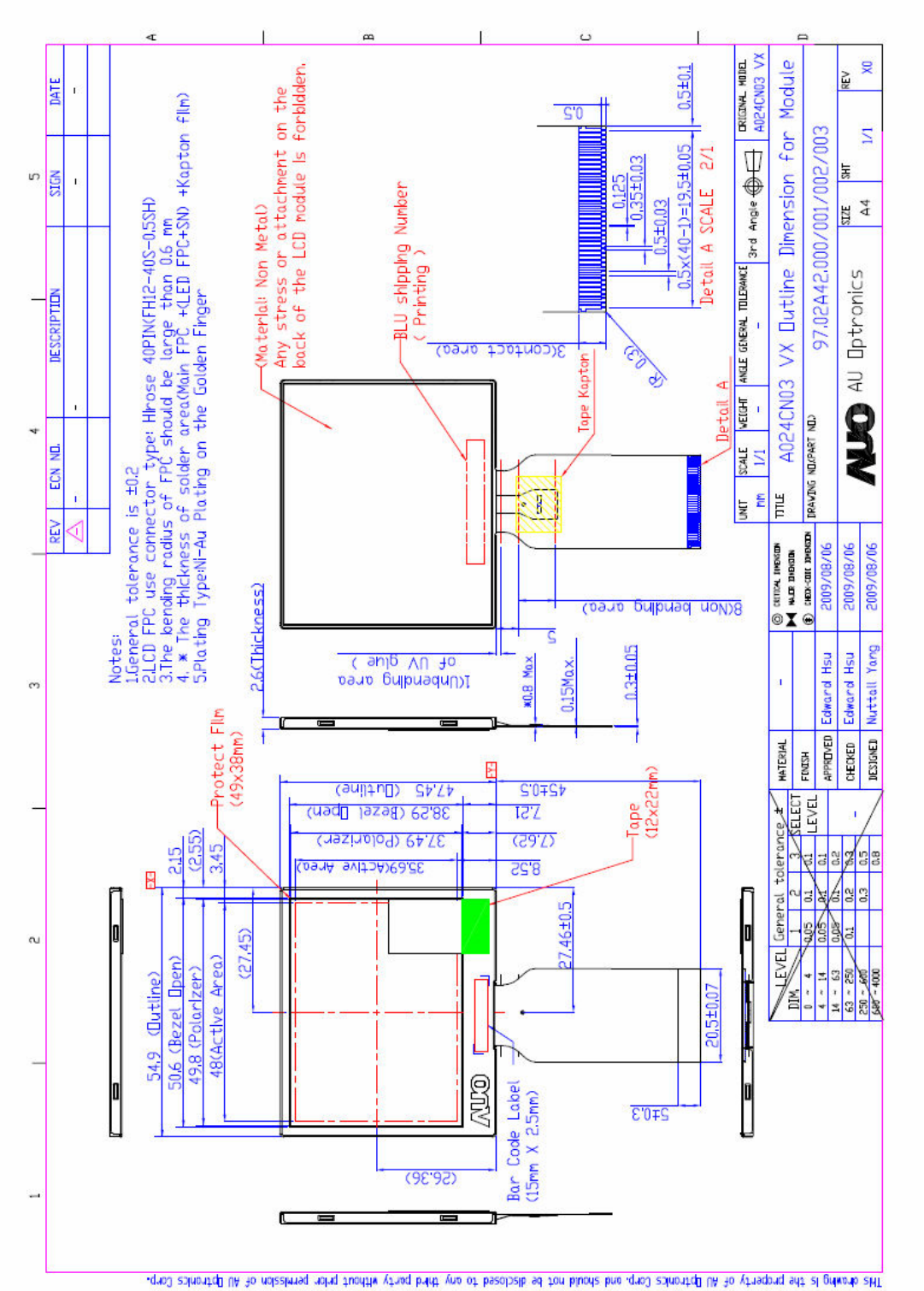



Fig. 1 Outline dimension of TFT-LCD module

"To avoid applying pressure or stress on the products. These will cause visual defects or luminance non-uniformity on the lighting area."

"The protection film in the back side of LCM should be tear off before assembly."

# G. Application Notes

## 1. Stand-by timing

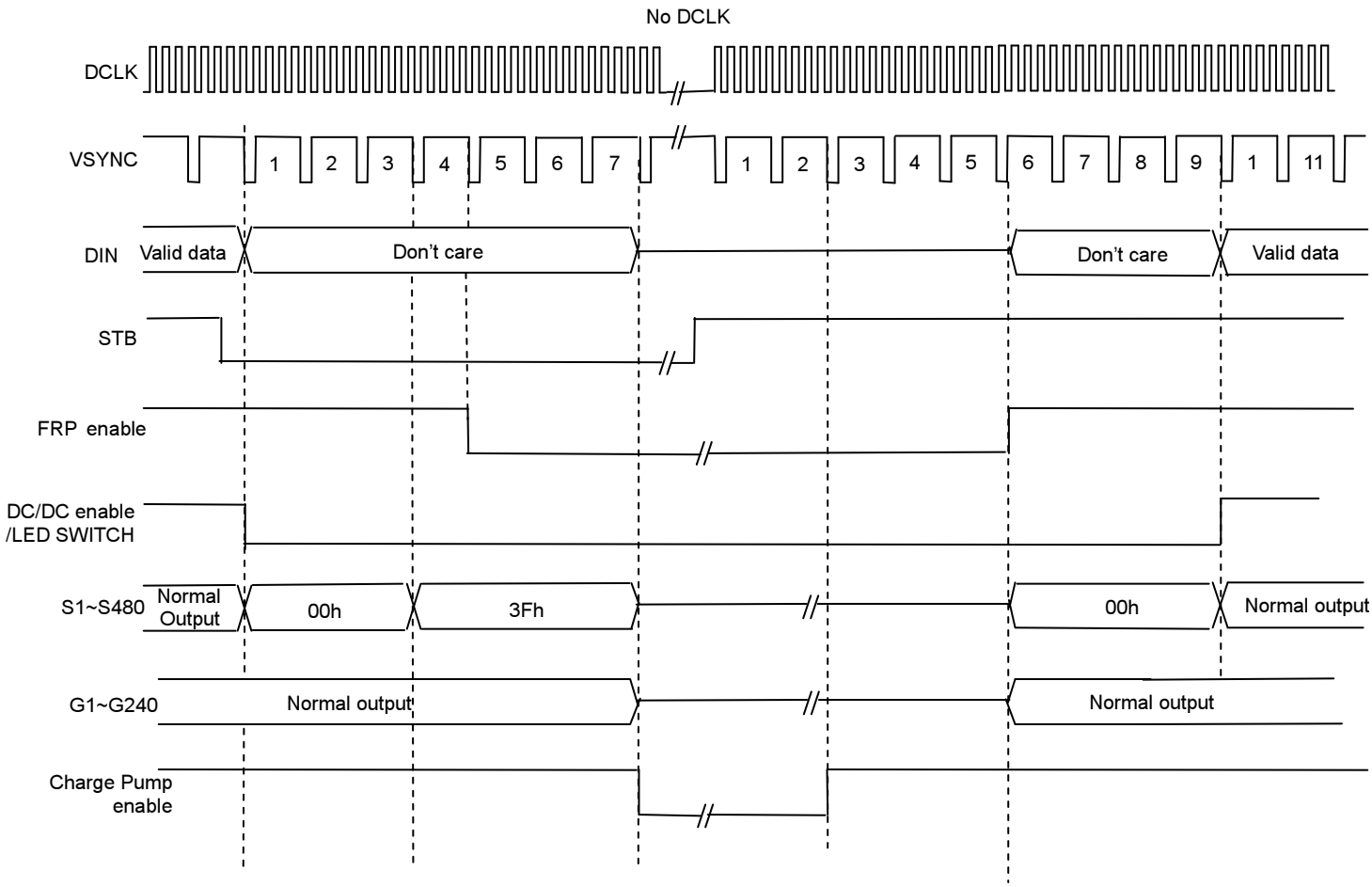


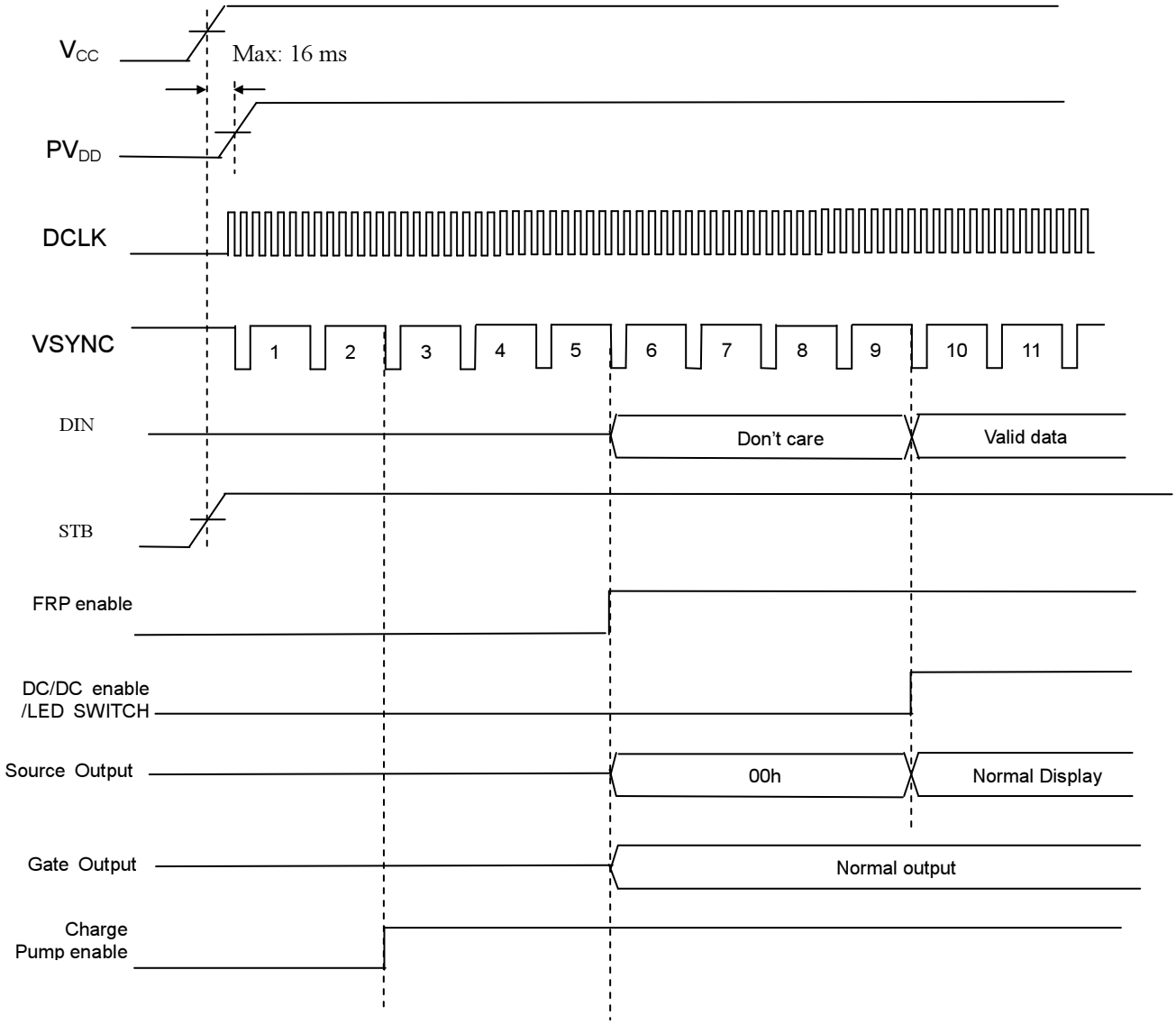

**Fig. 1 Stand-by timing diagram**

Note 1:During No DCLK, HSYNC and VSYNC can be stopped. But in all other cases HSYNC and VSYNC must be active.

Note 2: External signal: DCLK, VSYNC, DIN (D0 ~ D7), STB (By register)

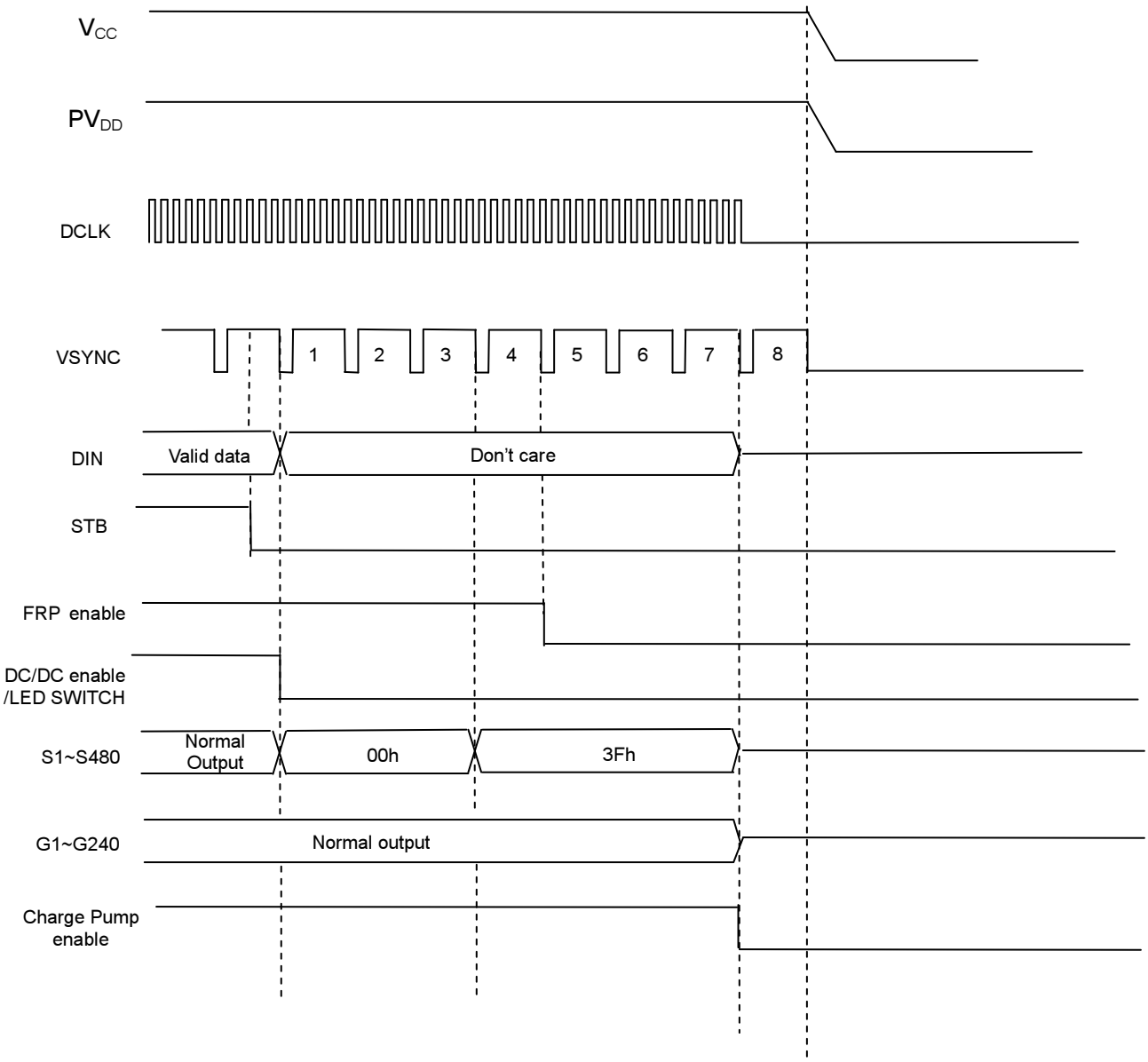
Internal signal: DC/DC enable S1 ~ S480 (Source Driver output signal), FRP enable G1 ~ G240 (Gate Driver output signal) and Charge Pump enable.

## 2. Power on sequence




Note 1: External signal: $V_{CC,}$ $PV_{DD,}$ DCLK, VSYNC, DIN (D0 ~ D7), STB (By register)
Internal signal: DC/DC enable S1 ~ S480 (Source Driver output signal), FRP enable,
G1 ~ G240 (Gate Driver output signal) and Charge Pump enable.

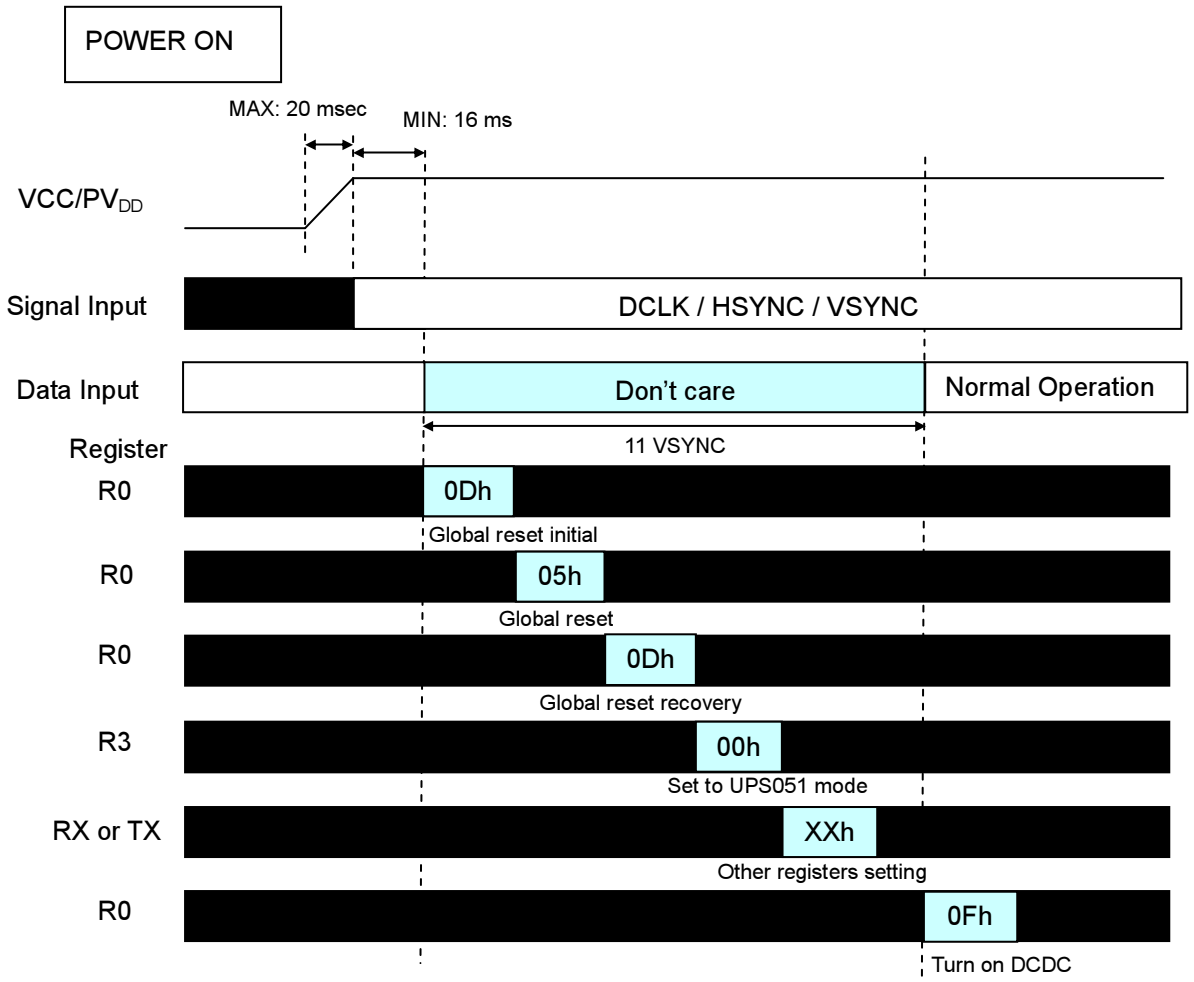
### 3. Power off sequence

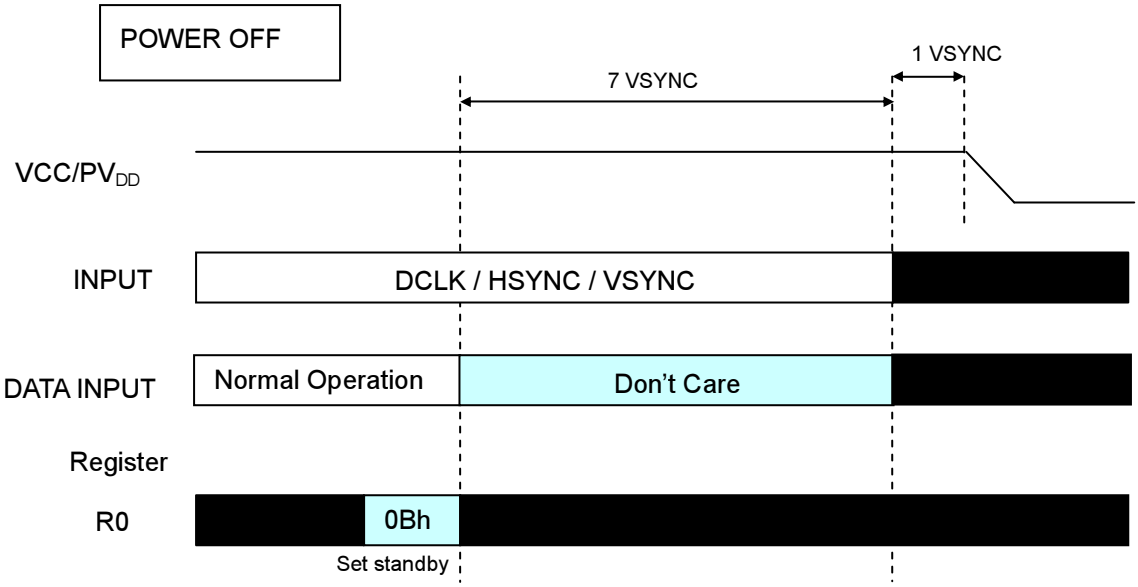



Note 1: External signal: $V_{CC,}$ $PV_{DD,}$ DCLK, VSYNC, DIN (D0 ~ D7), STB (By register)
Internal signal: DC/DC enable S1 ~ S480 (Source Driver output signal), FRP enable,
G1 ~ G240 (Gate Driver output signal) and Charge Pump enable.

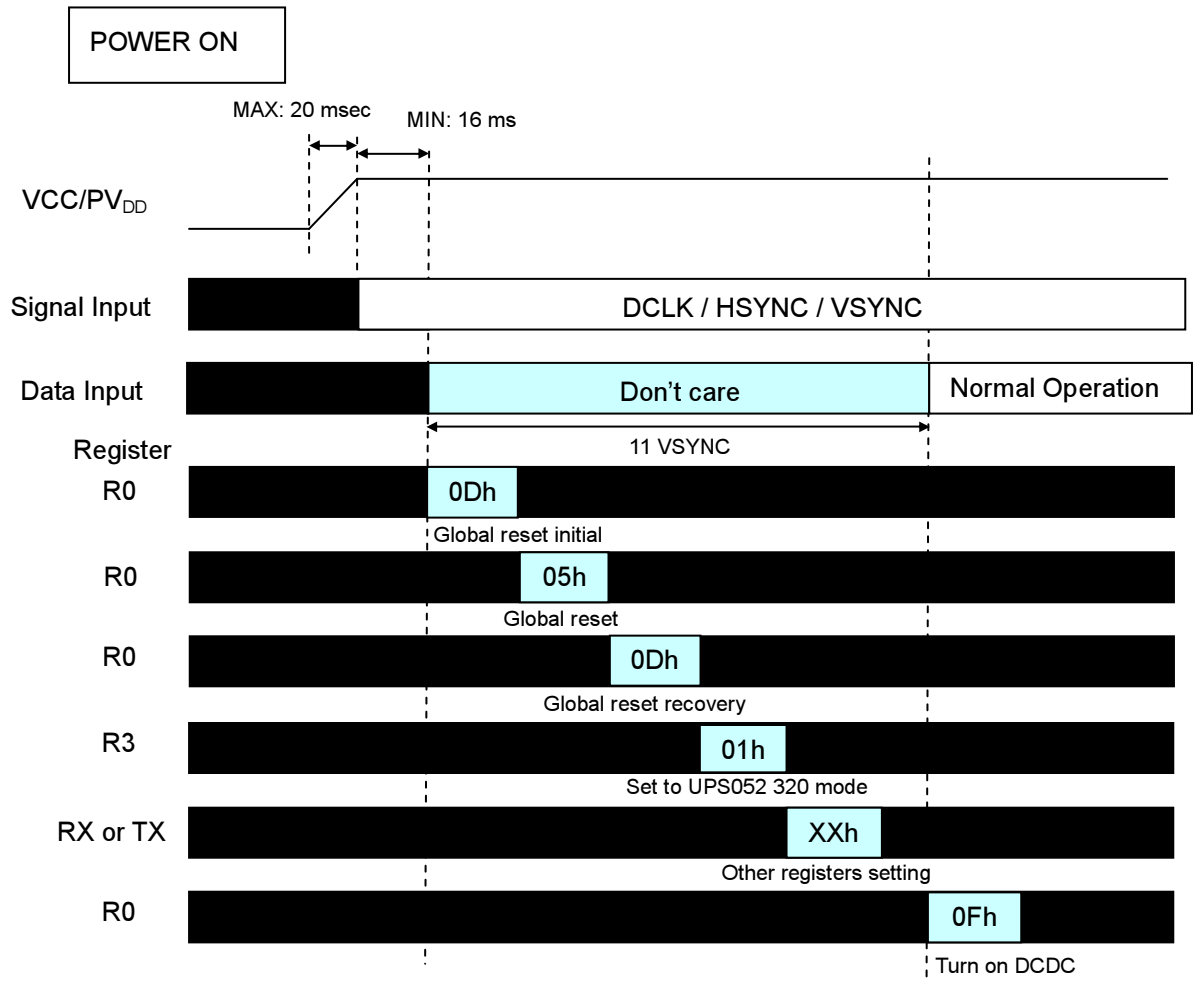
## 4. Recommended power on/off serial command settings

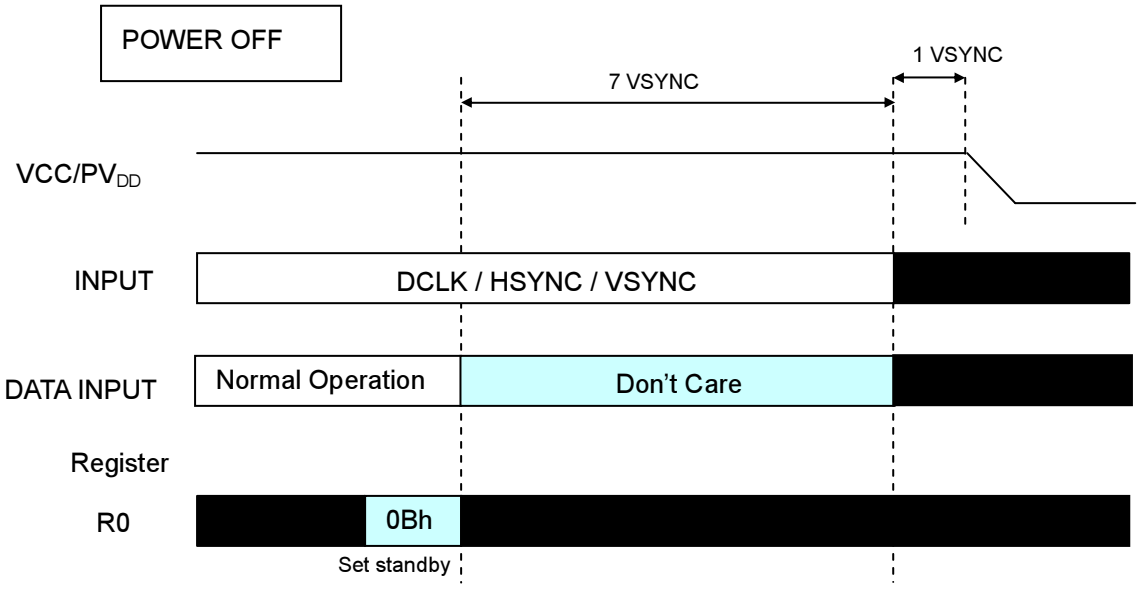
### 4.1. Recommend UPS051 (9.7 MHz) power on/off setting



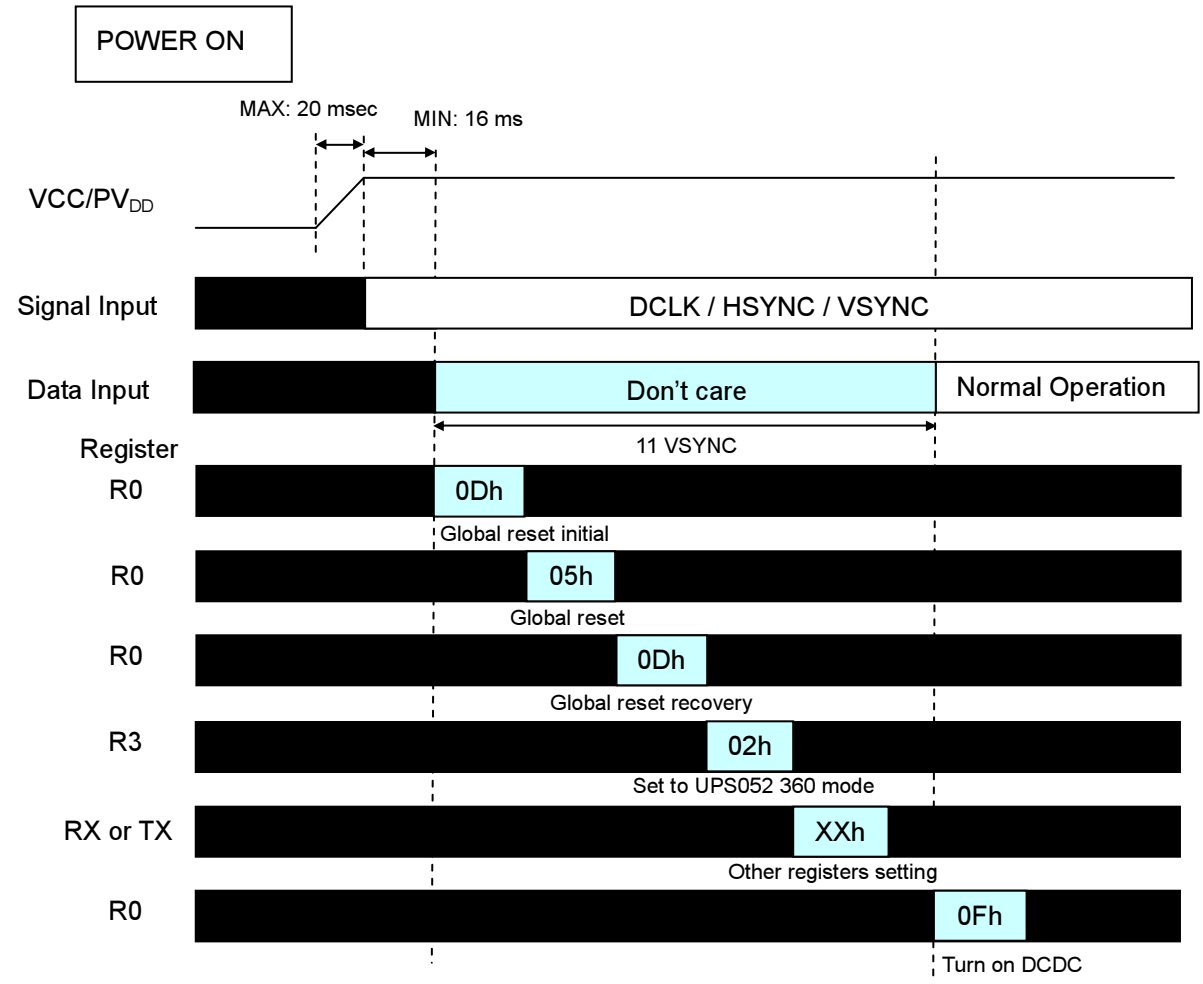



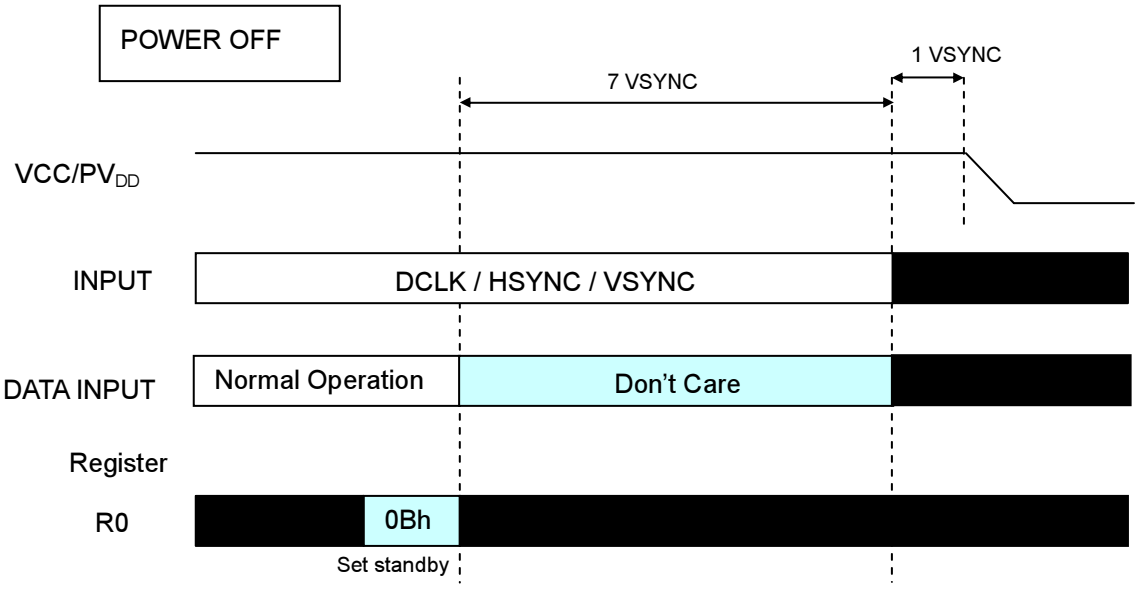
### 4.2. Recommend UPS052 320RGB mode (24.54 MHz) power on/off setting



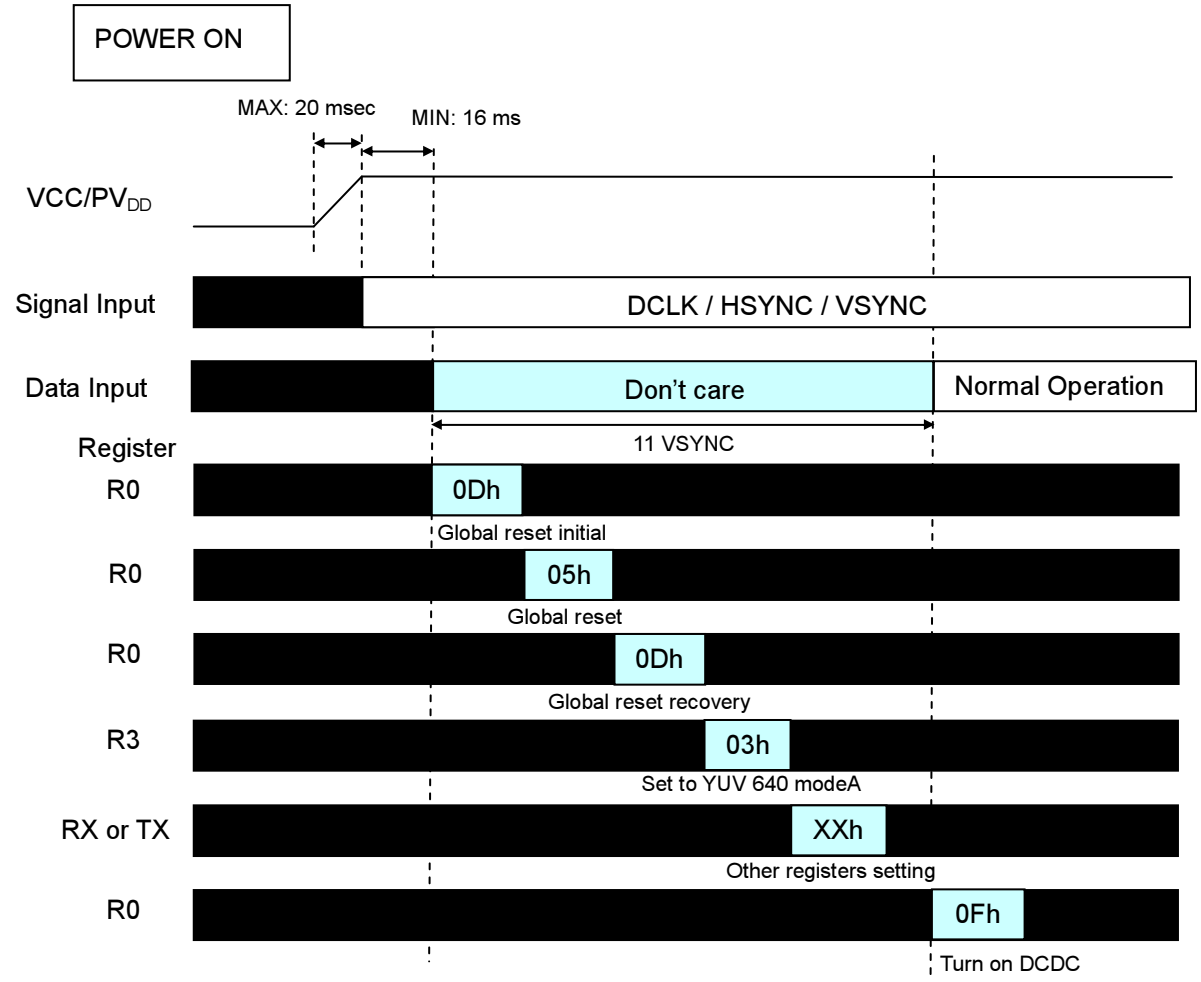



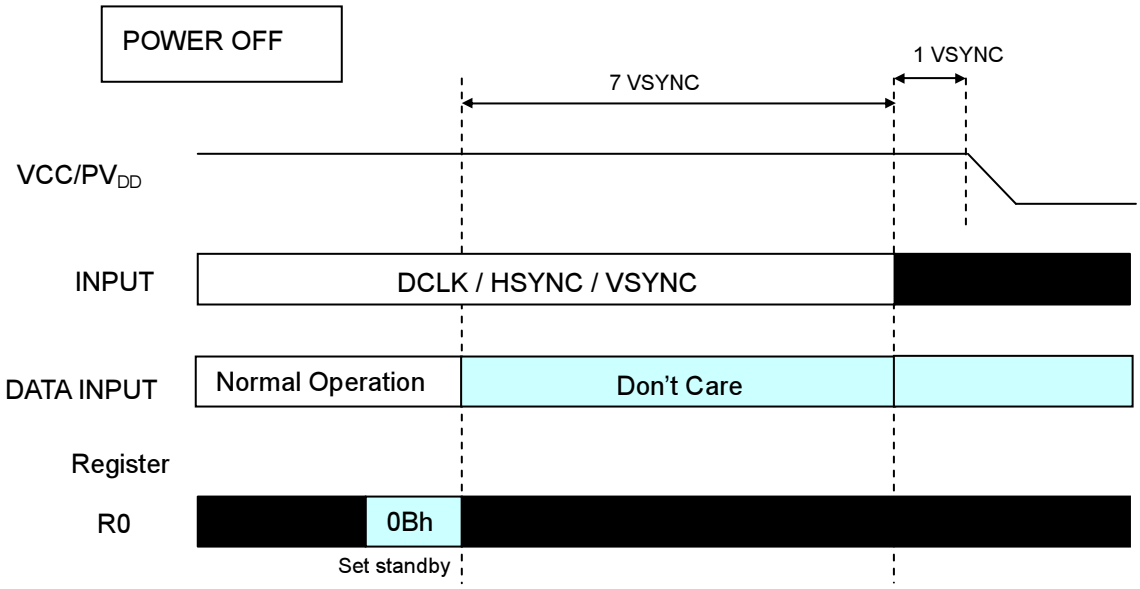
### 4.3. Recommend UPS052 360RGB mode (27MHz) power on/off setting



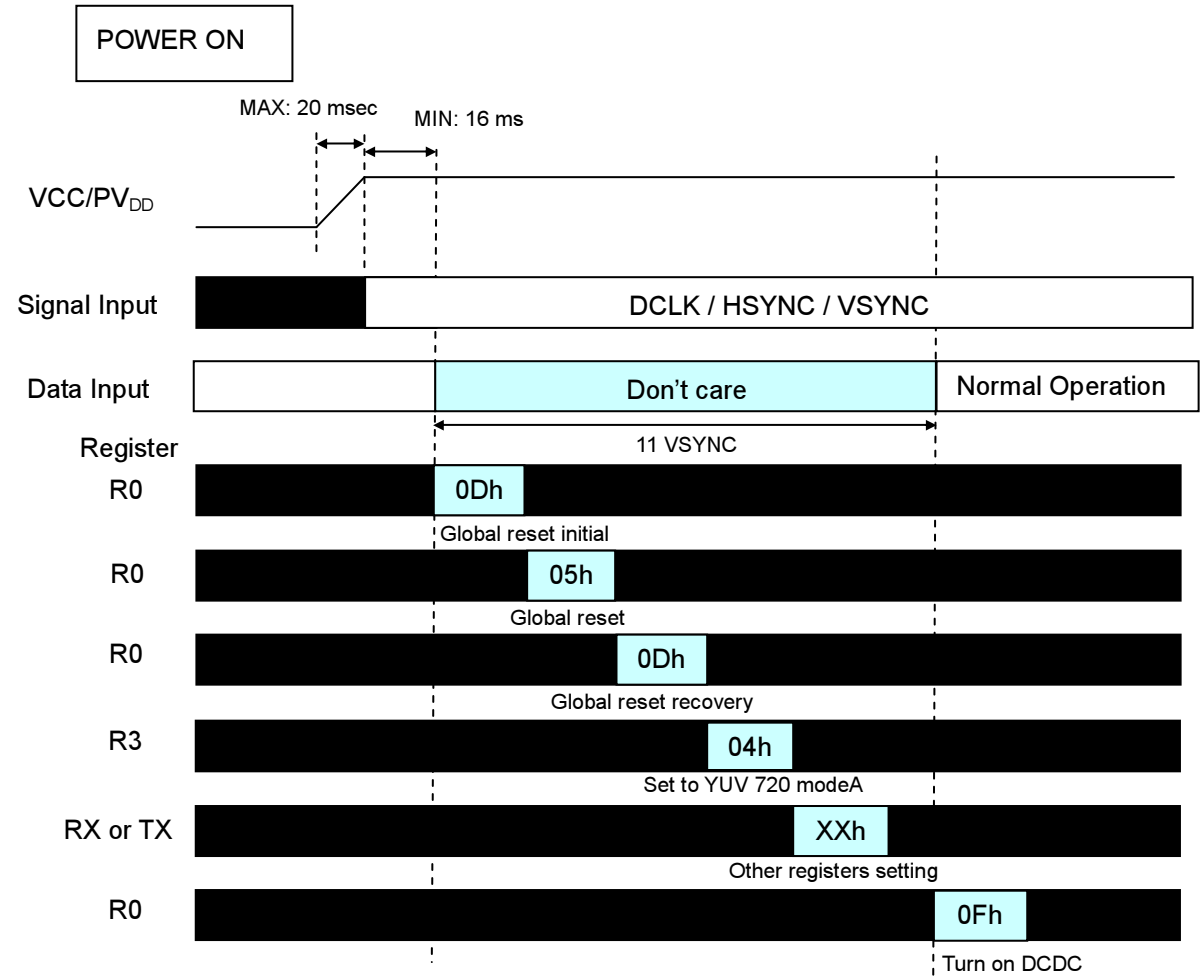



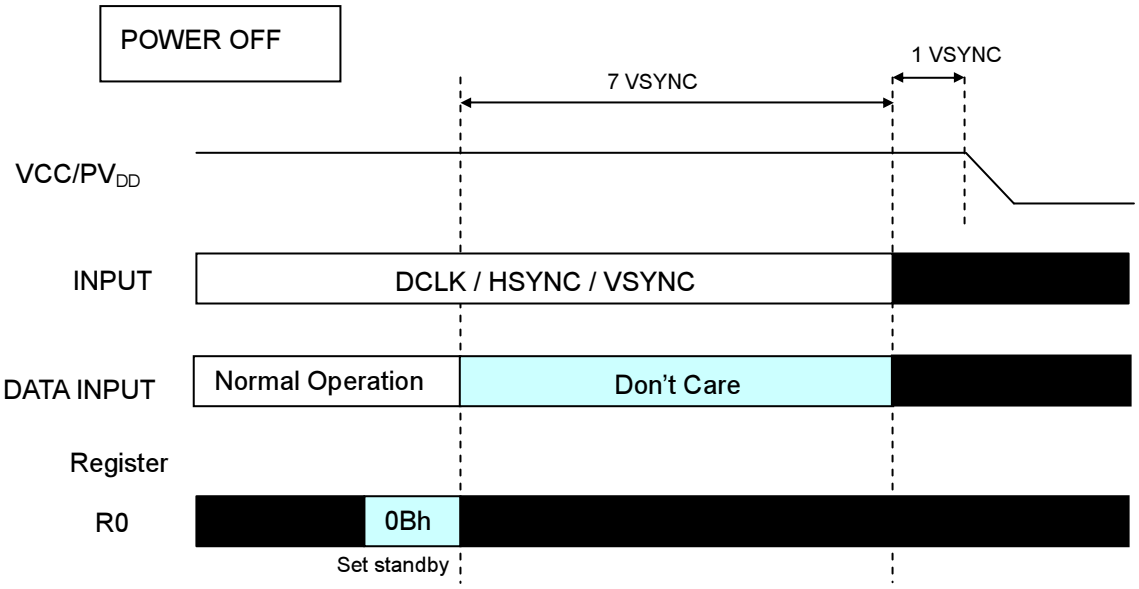
### 4.4. Recommend YUV mode A 640Y 320CrCb (24.54 MHz) power on/off setting



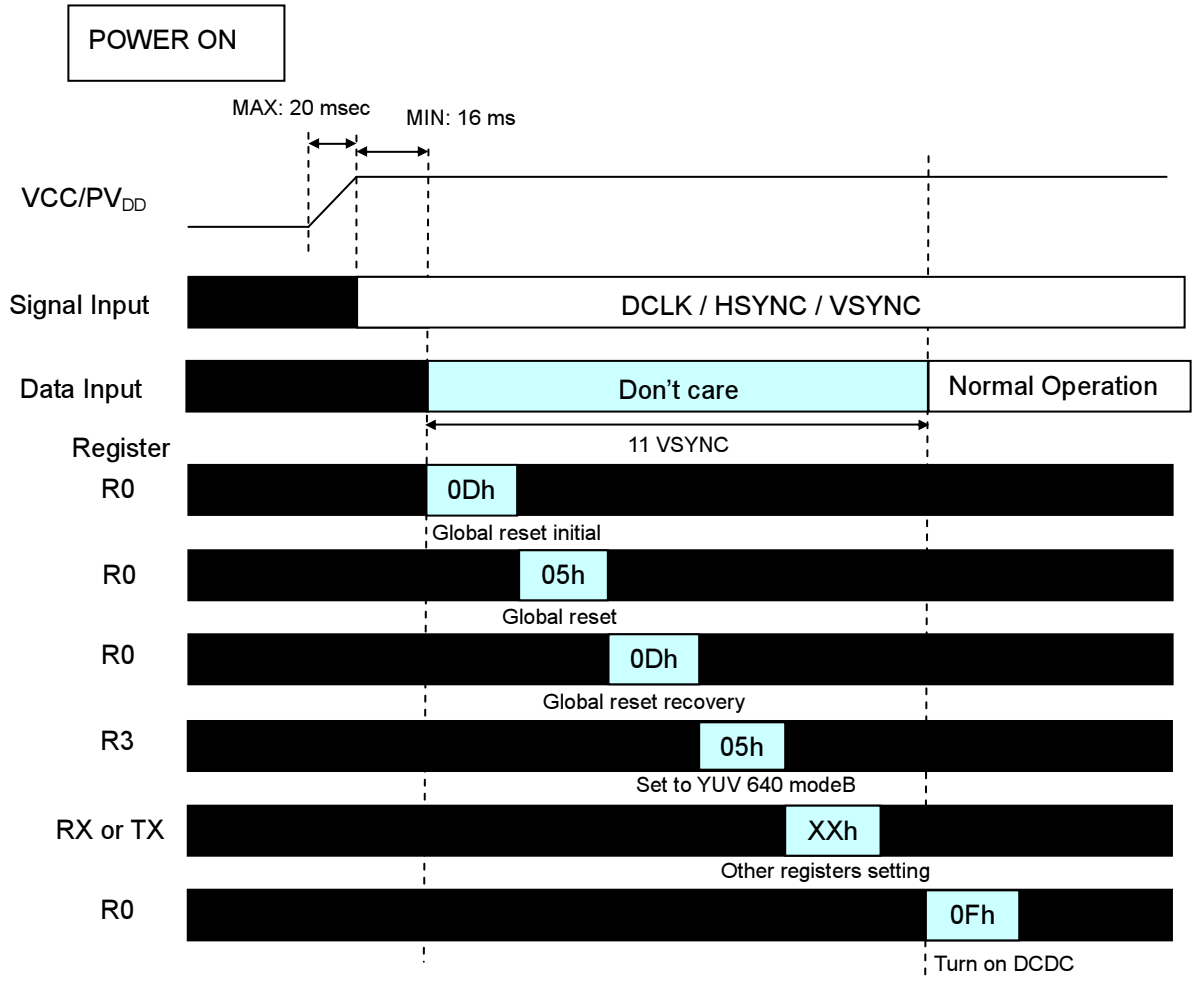



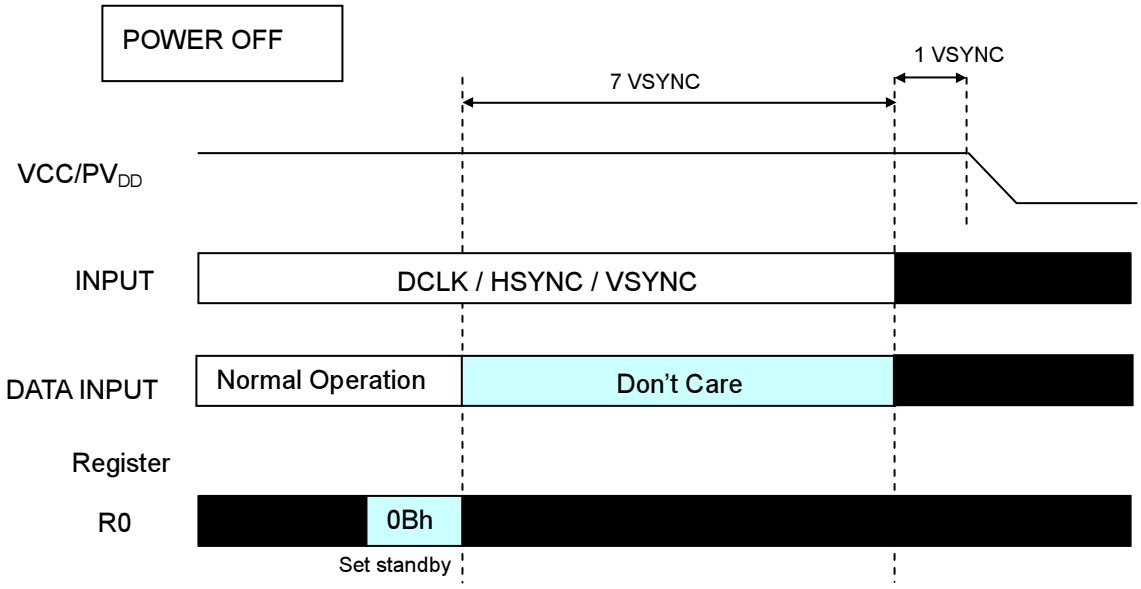
### 4.5. Recommend YUV mode A 720Y 360CrCb (27 MHz) power on/off setting



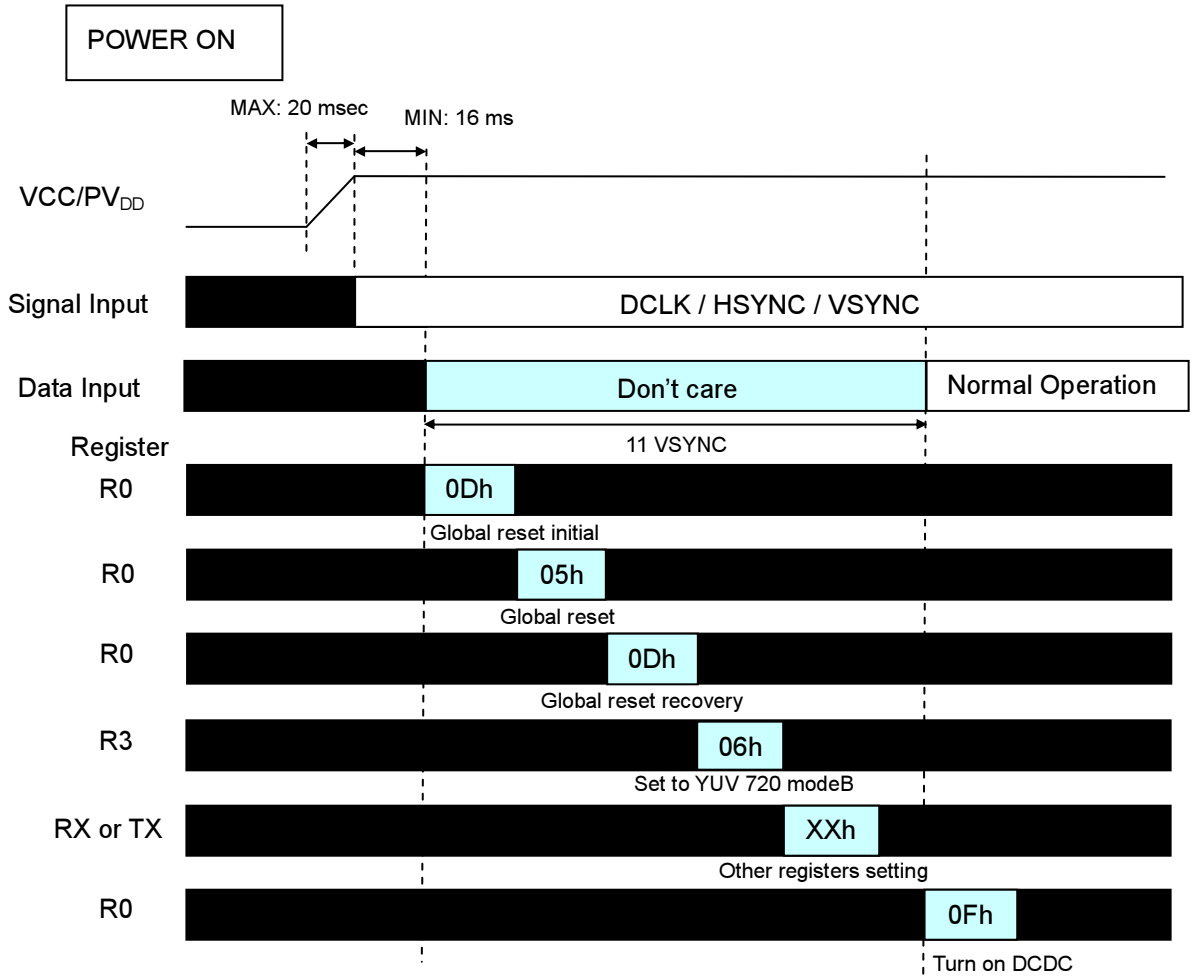



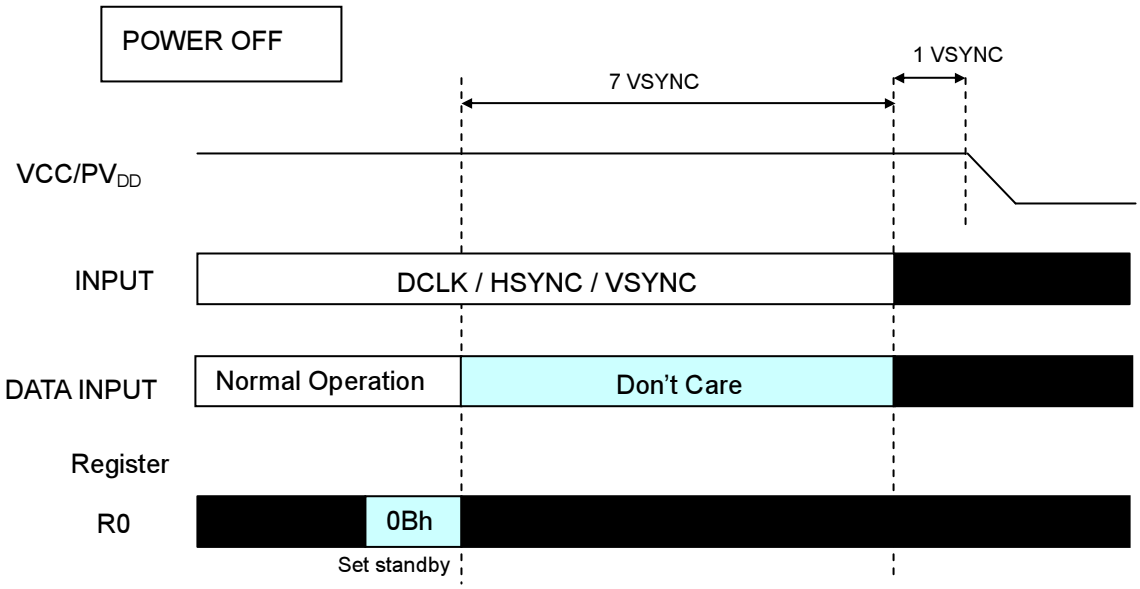
### 4.6. Recommend YUV mode B 640Y 320CrCb (24.54 MHz) power on/off setting



### 4.7. Recommend YUV mode B 720Y 320CrCb (27 MHz) power on/off setting



### 4.8. Recommend CCIR656 mode (27 MHz) power on/off setting