(   ) Preliminary Specifications
(✓) Final Specifications

Module	12.5"(12.49") FHD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B125HAN03.0 (H/W:1A)
Note (🔆)	*LED Backlight with driving circuit design*

Customer	Date
Checked & Approved by	**Date**

Note: This Specification is subject to change without notice.

Approved by	Date
	11/02/16
Prepared by	**Date**
	11/02/16

MPBU Marketing Division
AU Optronics corporation

Product Specification

AU OPTRONICS CORPORATION

Contents

Record of Revision

Version and Date		Page	Old description	New Description	Remark
0.1	2016/06/24	All	First Edition for Customer		
0.2	2016/08/17	6	Add RGB coodinates		
		26~27	2D drawing		
		29-30	Shipping Package of Palletizing Sequence		
		31	Add EDID		
1.0	2016/08/25	6	NTSC & Contract ratio min value		
1.1	2016/09/01	23~24 26~27	Update drawing		
1.2	2016/09/06	23~24 26~27	Update drawing		
1.3	2016/11/02	23~24 26~27	Update drawing		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.

7) Do not open nor modify the Module Assembly.

8) Do not press the reflector sheet at the back of the module to any directions.

9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.

11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.

13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B125HAN03.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x1080(V) screen and 16.2M colors (RGB 6-bits data with FRC) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B125HAN03.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	317.5			
Active Area	[mm]	276.48 X 155.52			
Pixels H x V		1920x3(RGB) x 1080			
Pixel Pitch	[mm]	0.144X0.144			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (ILED=19mA) **(Note: ILED is LED current)**	[cd/m²]	300 typ. (5 points average) 255 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		1000 typ			
Response Time	[ms]	25typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.02 max. (Include Logic and Blu power)			
Weight	[Grams]	160 max.			
Physical Size **Include bracket**	[mm]		Min.	Typ.	Max.
		Length	281.9	282.4	282.9
		Width	171.72	172.22	172.72
		Thickness		-	2.0
Electrical Interface		2 lane eDP 1.2			
Glass Thickness	[mm]	0.2			
Surface Treatment		HG			
Support Color		16.2M colors (RGB 6-bits data with FRC)			
Temperature Range Operating Storage (Non-Operating)	[ºC] [ºC]	0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=20mA			**5 points average**	255	300		cd/m²	1, 4, 5
Viewing Angle		θR θL	**Horizontal (Right)** CR = 10 **(Left)**	80 80	85 85		degree	4, 9
		ψH ψL	**Vertical (Upper)** CR = 10 **(Lower)**	80 80	85 85			
Luminance Uniformity		δ5P	**5 Points**			1.25		1, 3, 4
Luminance Uniformity		δ13P	**13 Points**			1.50		2, 3, 4
Contrast Ratio		CR		800	1000			4, 6
Cross talk		%				4		4, 7
Response Time		TRT	**Rising + Falling**		25	35	msec	4, 8
Color / Chromaticity Coodinates	**Red**	Rx	CIE 1931	0.613	0.643	0.673		4
		Ry		0.306	0.336	0.366		
	Green	Gx		0.285	0.315	0.345		
		Gy		0.584	0.614	0.644		
	Blue	Bx		0.121	0.151	0.181		
		By		0.021	0.051	0.081		
	White	Wx		0.275	0.305	0.335		
		Wy		0.290	0.320	0.350		
NTSC		%		62	72			

Note 1: 5 points position (Ref: Active area)
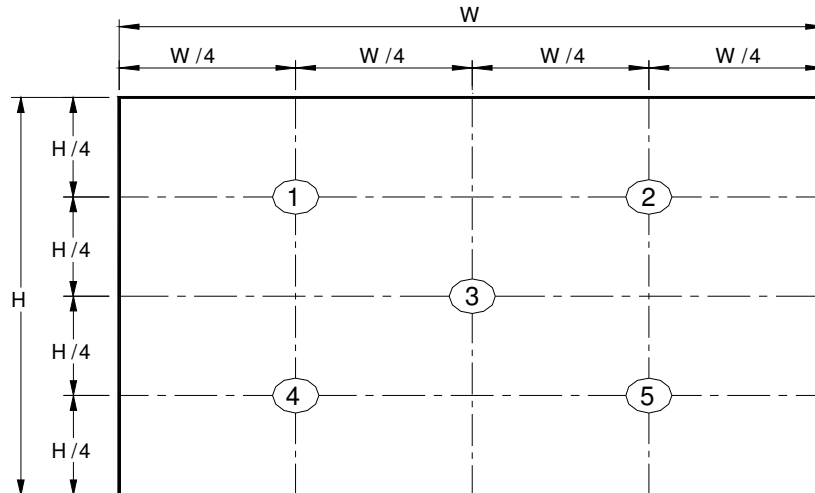
Note 2: 13 points position (Ref: Active area)
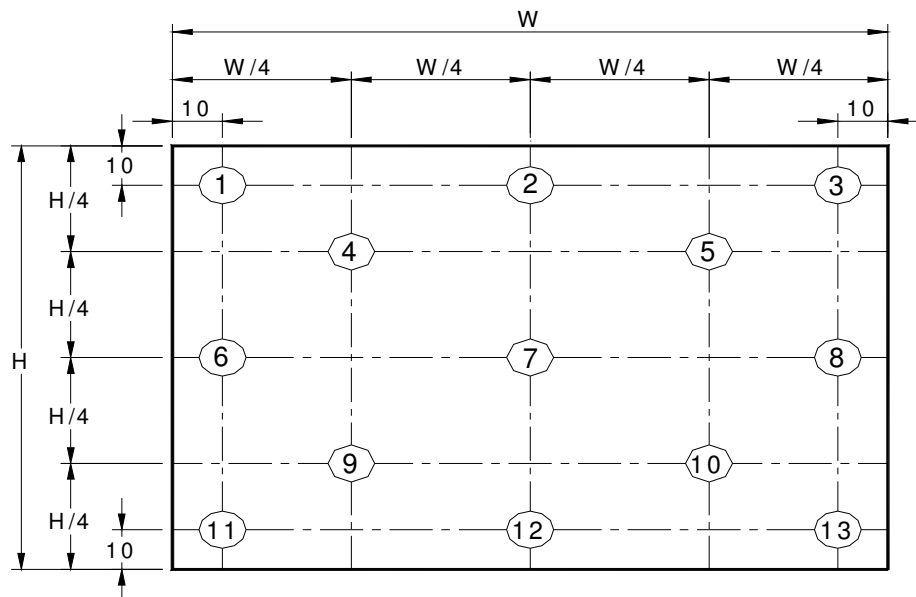
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt

temperature change during measuring. In order to stabilize the luminance, the measurement should

be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.

Center of the screen
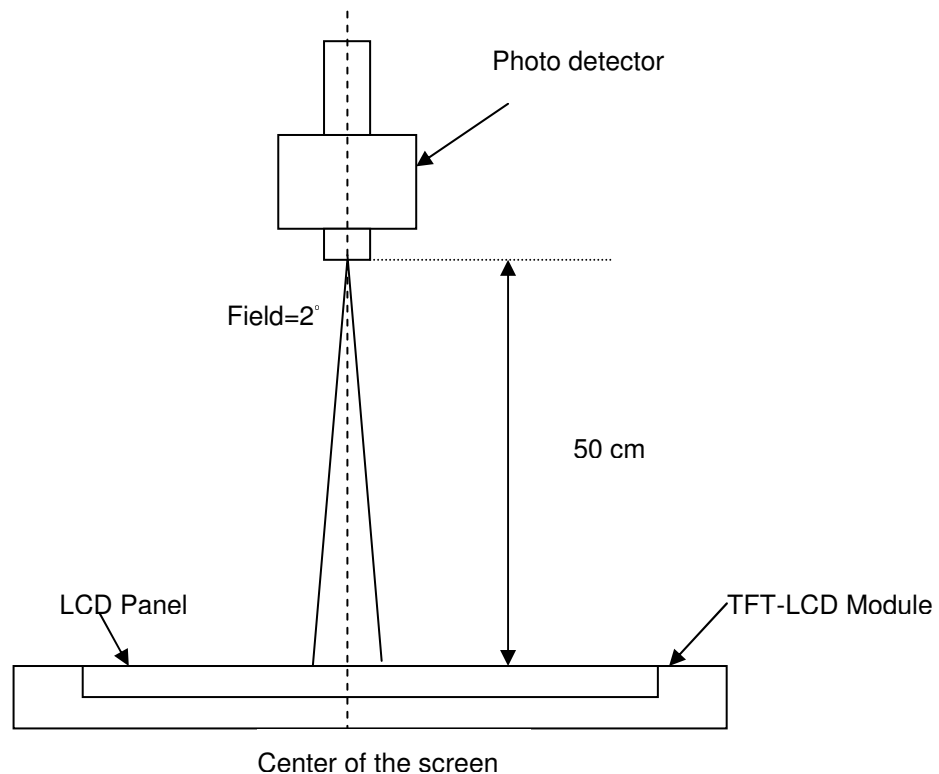
Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$
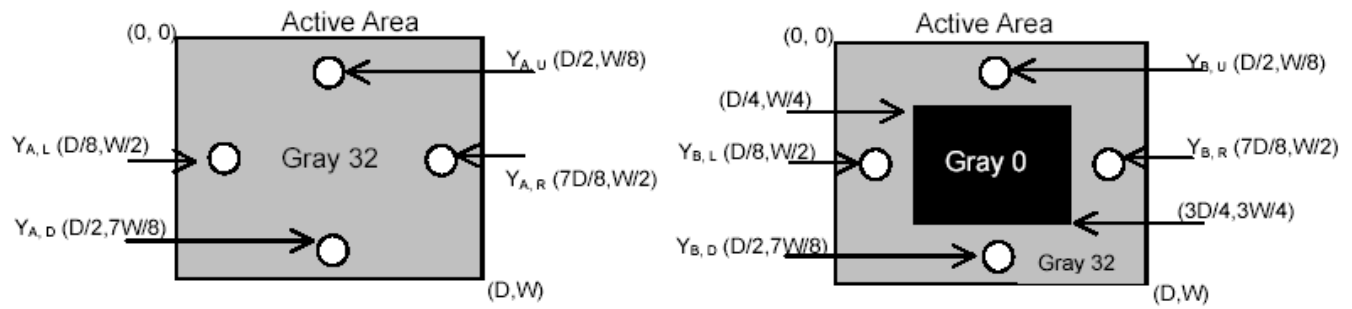
Note 7： Definition of Cross Talk (CT)

CT = | Y_B – Y_A | / Y_A × 100 (%)

Where

Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)

Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.
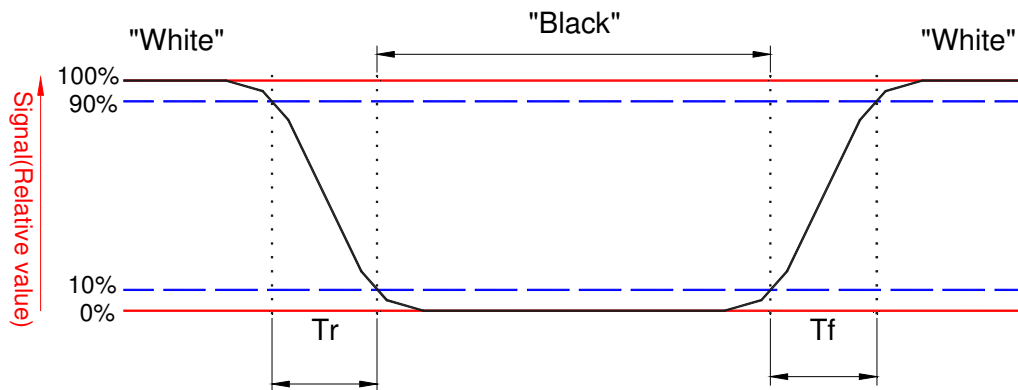
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio $\geqq 10$, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.
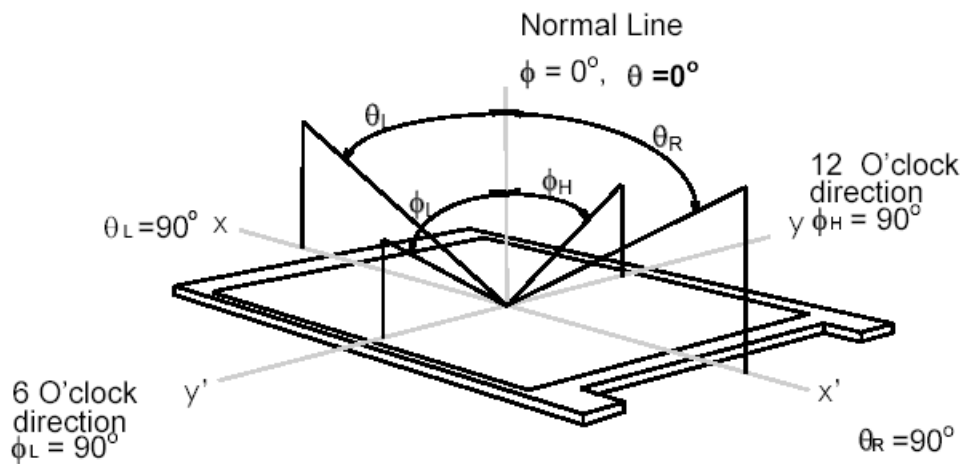
3. Functional Block Diagram

The following diagram shows the functional block of the 12.5 inches wide Color TFT/LCD 30 Pin
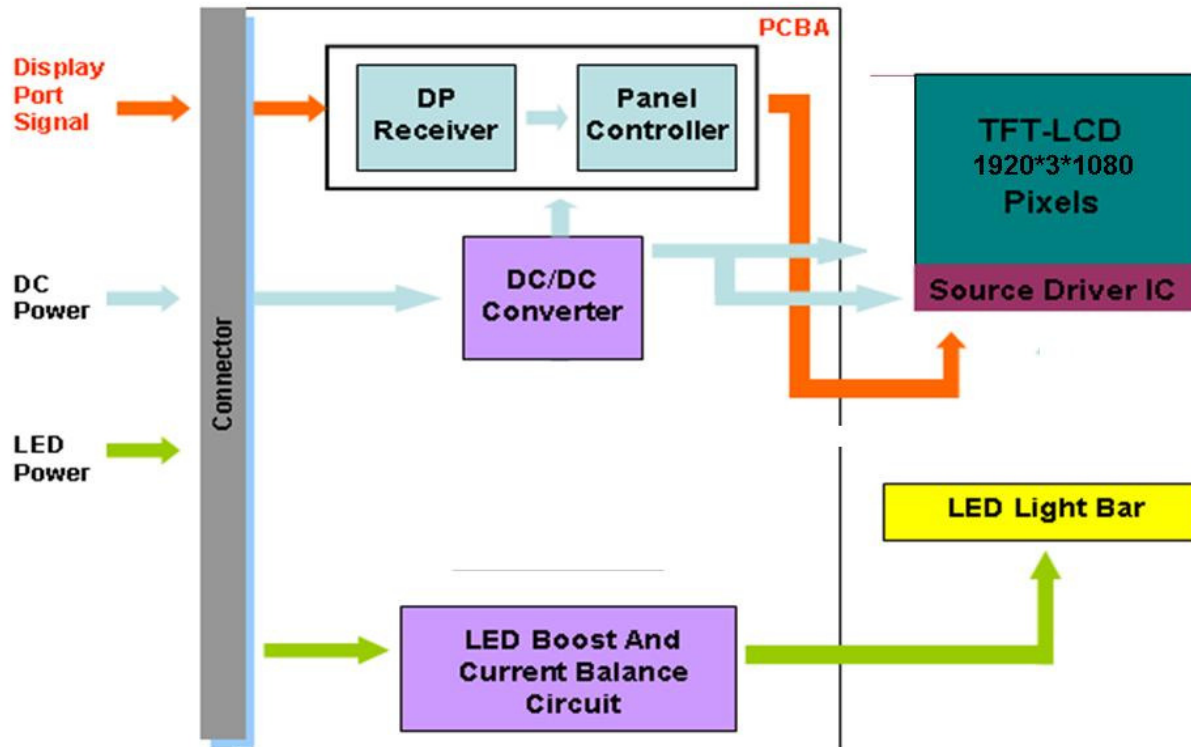
4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	90	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	90	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).
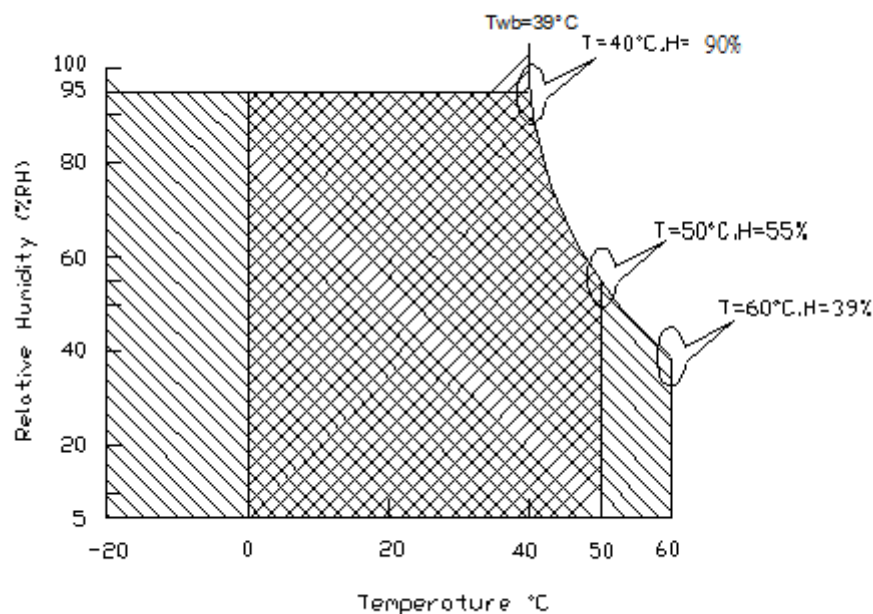
Operating Range   Storage Range

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power			1.1	[Watt]	Note 1, 2
IDD	IDD Current			303	[mA]	Note 1
IRush	Inrush Current			2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Mosaic pattern (PDD (max) = VDD(min) x IDD(max))

Typical Measurement Condition : Mosaic Pattern

Note 2 : 1.9W max at worse pattern

Note 3： Measure Condition

Vin rising time
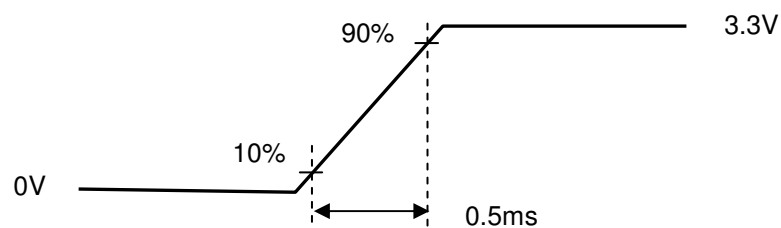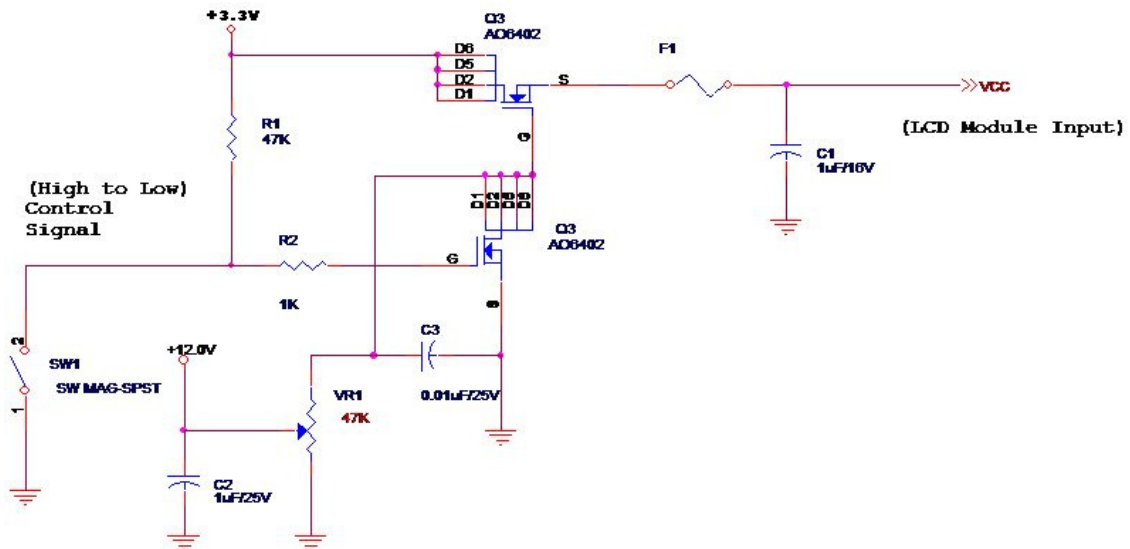
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Display Port main link signal:
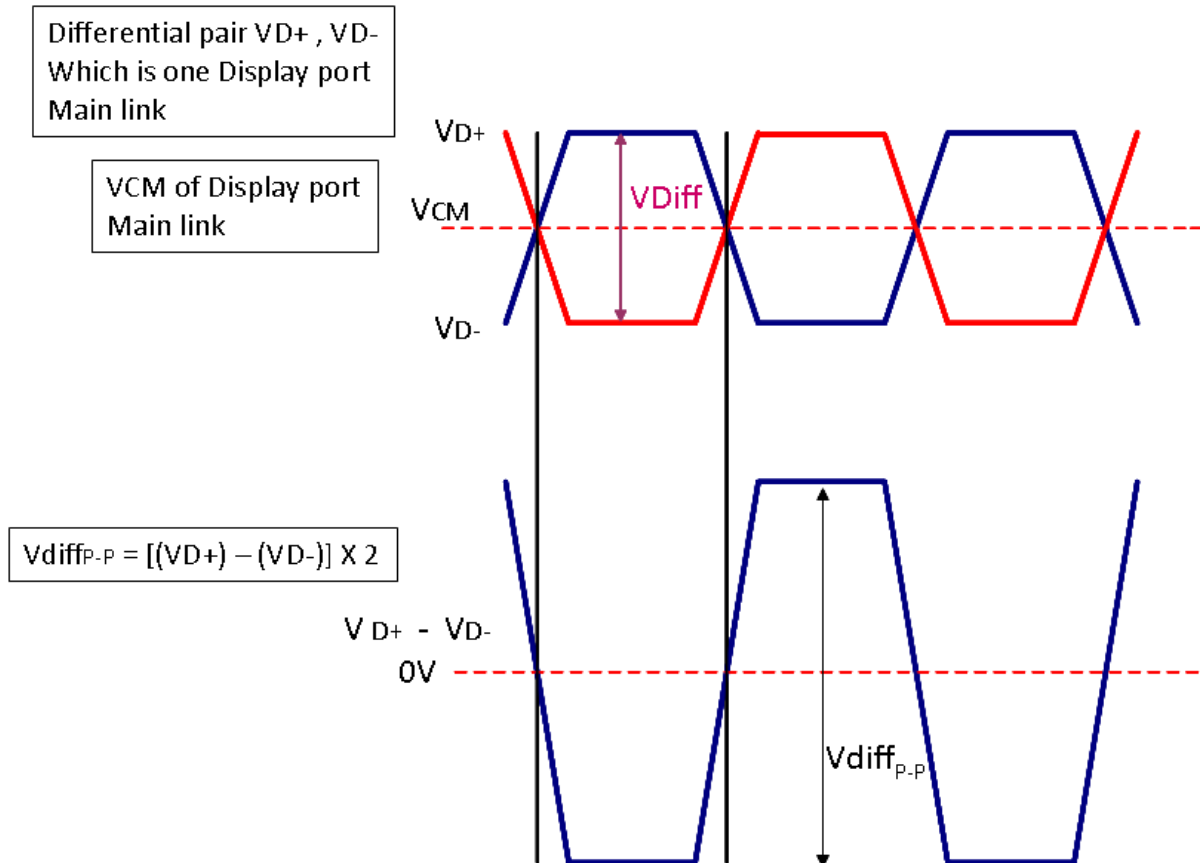
Display port main link		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff$_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Follow as VESA display port standard V1.2

Display Port AUX_CH signal:
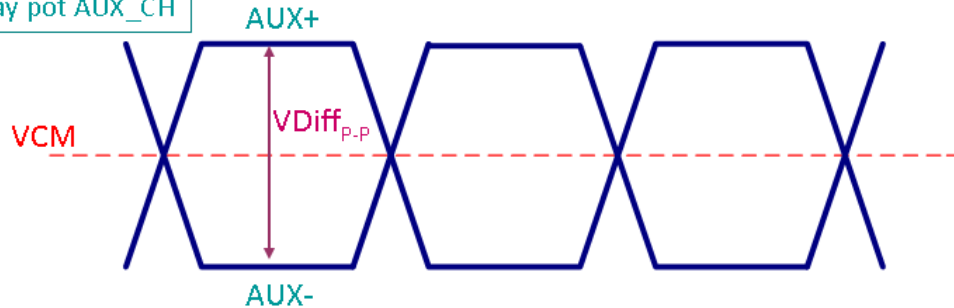
Display port AUX_CH		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff$_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Follow as VESA display port standard V1.2.

Display Port VHPD signal:

Display port V$_{HPD}$		Min	Typ	Max	unit
V$_{HPD}$	HPD Voltage	2.25		3.6	V

Follow as VESA display port standard V1.2.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.92	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=19 mA

Note 1: Calculator value for reference P$_{LED}$ = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.0	12.0	21.0	[Volt]	
LED Enable Input High Level	VLED_EN	2.2	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	Define as Connector Interface (Ta=25℃)
PWM Logic Input High Level	VPWM_EN	2.2	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	1 Note 2		100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

Note 2 : If the PWM duty ratio(min) is set between 5% to 1%，the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.
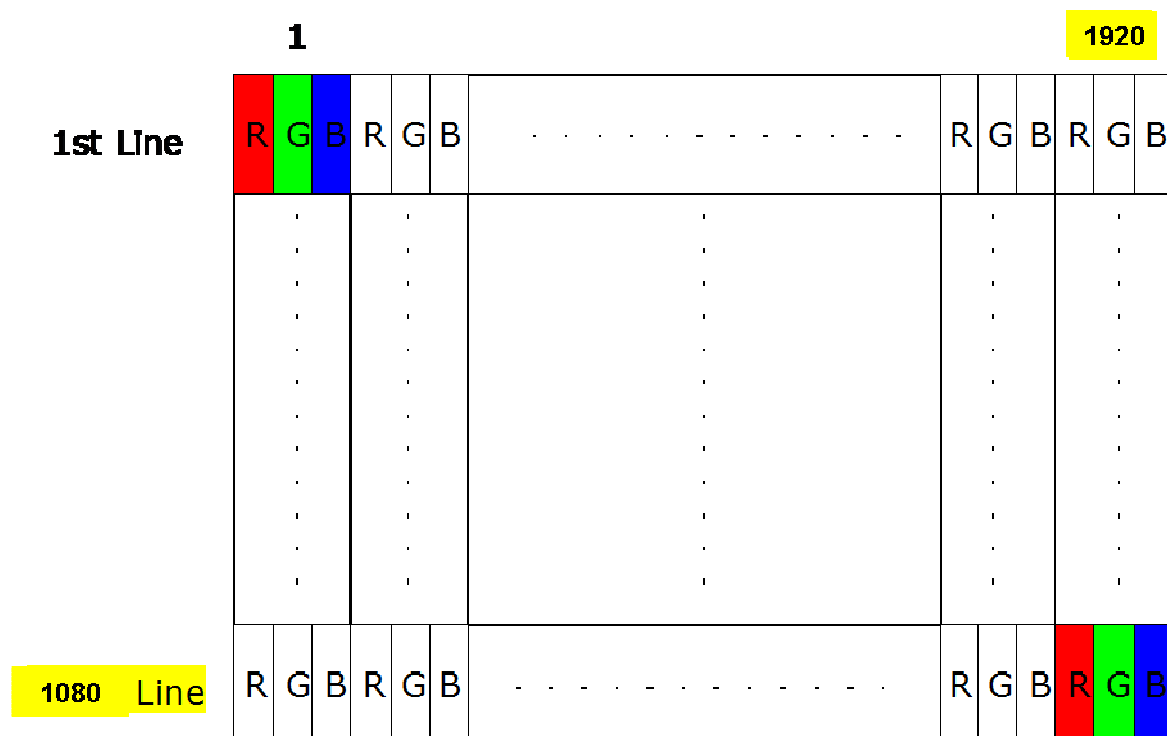
6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	Panasonic
Type / Part Number	AXT630124
Mating Housing/Part Number	AXT530124

6.2.2 Pin Assignment (2 Lane)

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Signal Name
1	LCD_PWM_CON
2	GND
3	GND
4	Lane0_P
5	LCD_BLEN_CON
6	Lane0_N
7	HPD
8	GND
9	GND
10	Lane1_P
11	3VS_LCD
12	Lane1_N
13	3VS_LCD
14	GND
15	3VS_LCD
16	Lane2_P
17	3VS_LCD
18	Lane2_N
19	LCD_Self_Test
20	GND
21	NC - RESERVED
22	Lane3_P
23	AC_BAT_SYS_LCD
24	Lane3_ N
25	AC_BAT_SYS_LCD
26	GND
27	AC_BAT_SYS_LCD
28	AUX_N
29	AC_BAT_SYS_LCD
30	AUX_P

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

Note1: Start from right side.
Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.
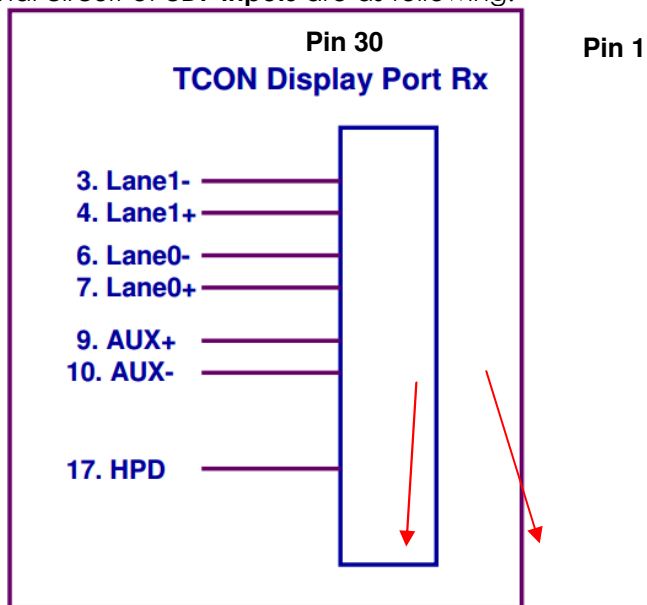
6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1920X1080 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		$1/T_{Clock}$	-	141	-	MHz
Vertical Section	Period	T_V	1090	1116	3080	T_{Line}
	Active	T_{VD}		1080		
	Blanking	T_{VB}	10	36	2000	
Horizontal Section	Period	T_H	2000	2104	2320	T_{Clock}
	Active	T_{HD}		1920		
	Blanking	T_{HB}	80	184	400	

6.4 Power ON/OFF Sequence

Display Port panel power sequence:
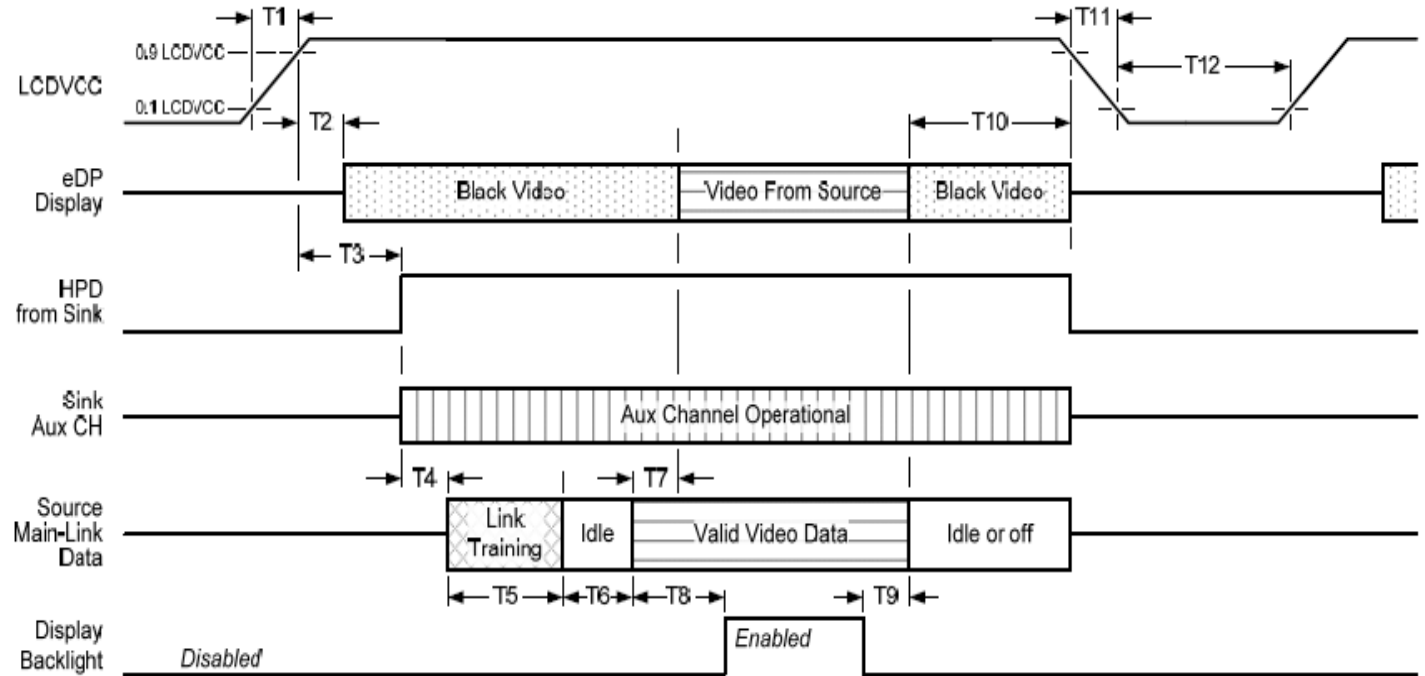
Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:

Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

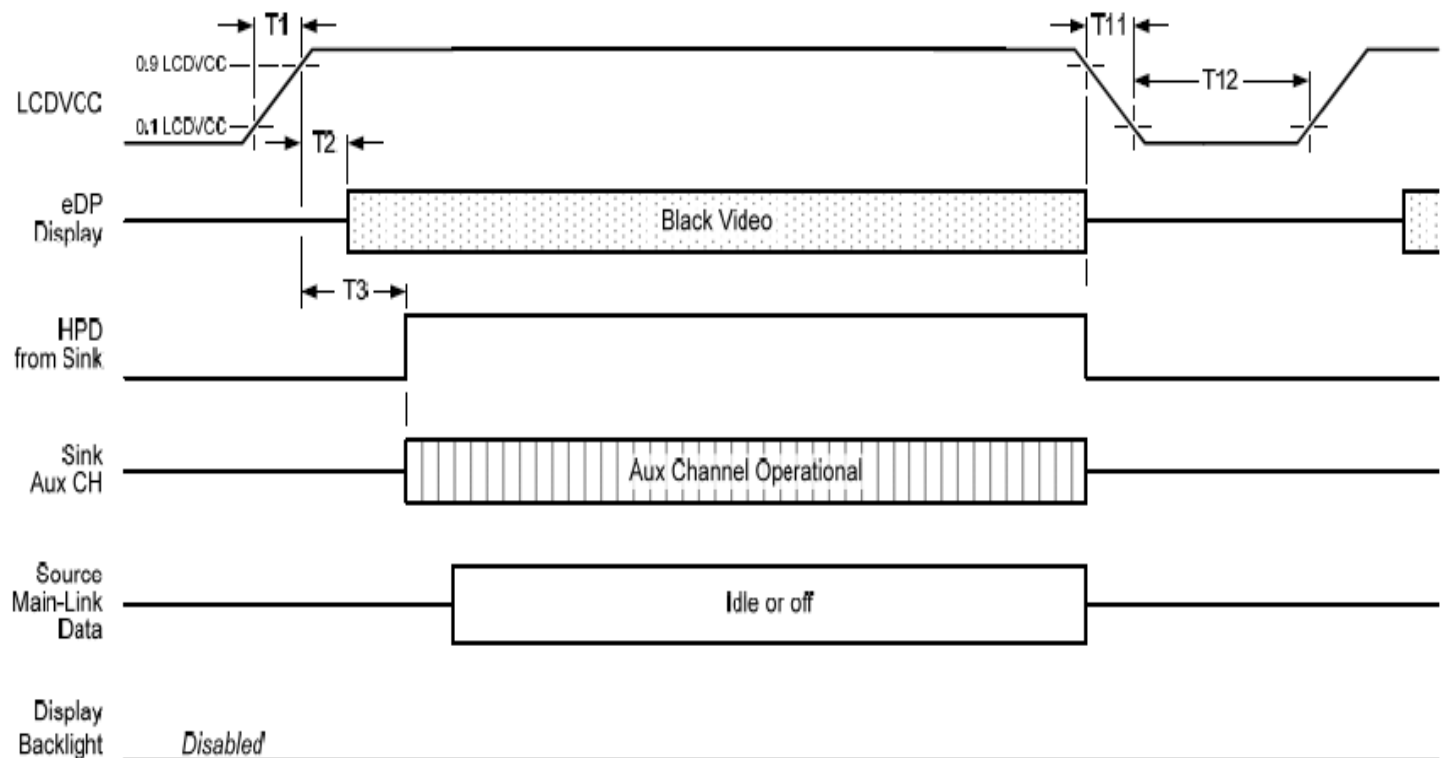| Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
  -upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
  -when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:

	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	0	-
T16	0	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT$_{PWM}$*

*T$_{PWM}$= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.

Note 1 : If T14,T15,T16,T17<10ms，The display garbage may occur. We suggest T14,T15,T16,T17>10ms to avoid the display garbage.

Note 2 : If T13 or T18<0.5ms，the inrush current may cause the damage of fuse. If T13 or T18<0.5ms，the inrush current I2t is under typical melt of fuse Spec.，there is no mentioned problem.

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed.

Self-recoverable.

No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension
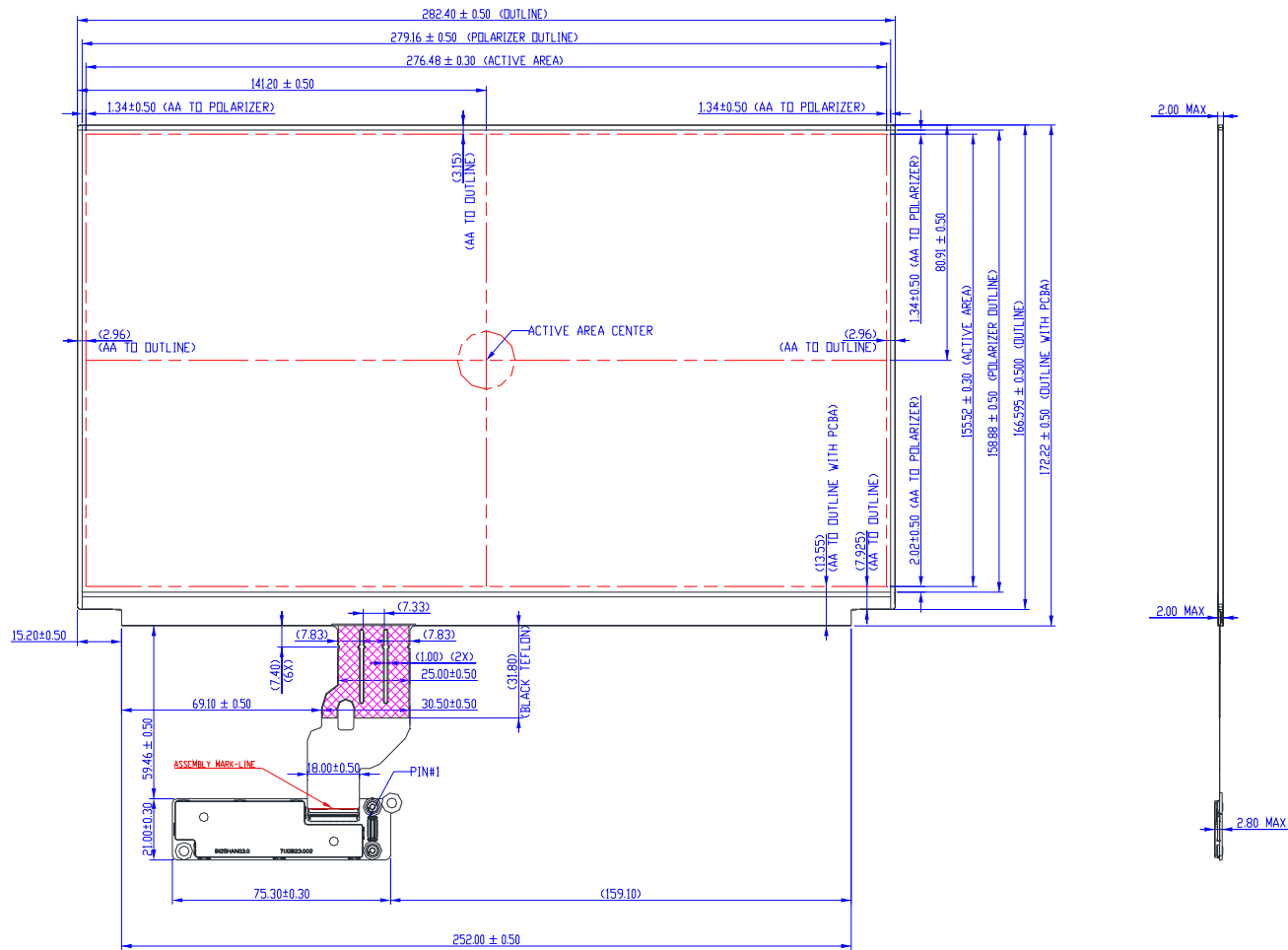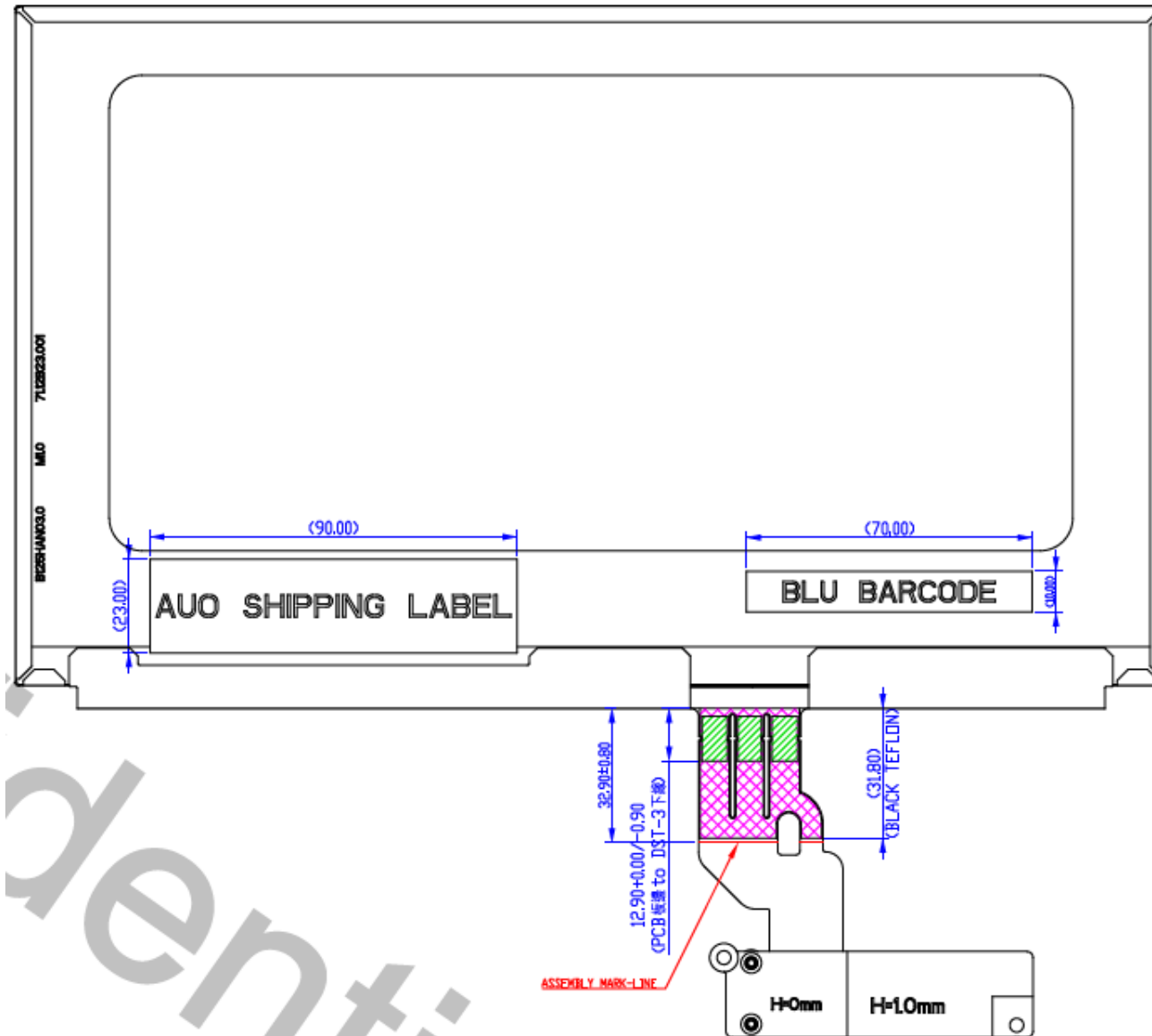
Note: Prevention IC damage, IC positions not allowed any overlap over these areas

9. Shipping and Package

9.1 Shipping Label Format

Manufactured YY / WW
Model No: B125HAN03.0
AU Optronics
MADE IN CHINA (S01)

H/W: 1A F/W:1

c ᴿᵁ us
E204356

Pb

RoHS

15

B125HAN03.0

9.2 Carton Package

```
AU Optronics          QTY :              [RoHS]
MODEL NO :    B125HAN03.0                (Pb)
PART NO :     97.12B23 001
CUSTOMER NO :                            (15)
CARTON NO :

            |||||||||||||||||||||||||

MADE IN CHINA            XXXXX-XXXXXXXXXXX
```

9.3 Shipping Package of Palletizing Sequence

Panel*2 & Spacer*3   Panel*2 & Spacer*3
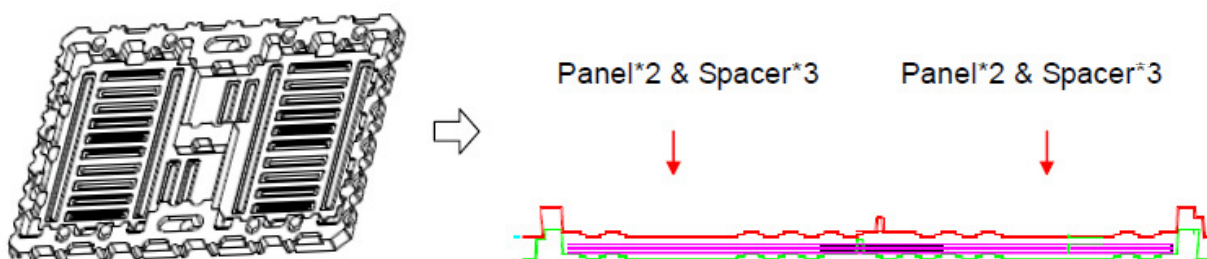
PET Tray，1Tray 共 2 格，每格放 **2** 片 Panel，Panel 間放置 EPE spacer 共 **3** 片，下方先放 EPE 再放 Panel(如上圖所示)，POL 面必須朝上放置，故 1 tray 共有 **4** 片 Panel ，**6** 片 Spacer，放滿後於其上再旋轉放置空 Tray，Tray 依序旋转堆叠。
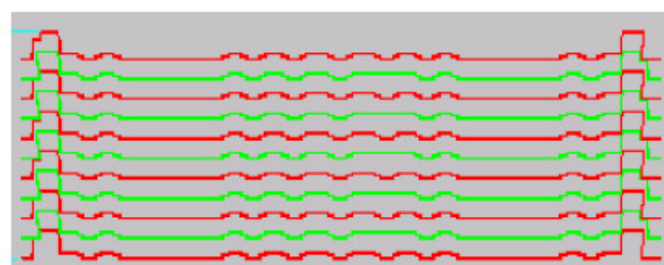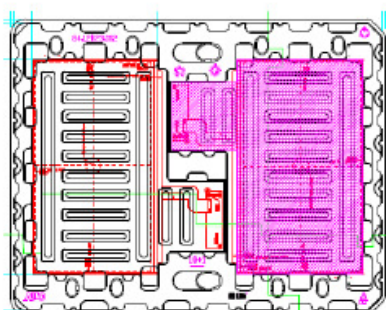
（10+1Tray 旋转堆叠 ）

堆疊 **10** 層 Tray 盤後，上附 1 空 Tray，共 **11** 個 Tray，堆疊 Tray 後，底部加上 PP 瓦愣板，再以静電袋包覆。放入四周上下如圖加上 EPE Cushion 的紙箱中，封箱，完成。

Anti-static bag

PET Tray **11pcs**

EPE SPACER **40pcs**

EPE CUSHION * 4

PP瓦楞板

共 **40pcs Panel**
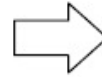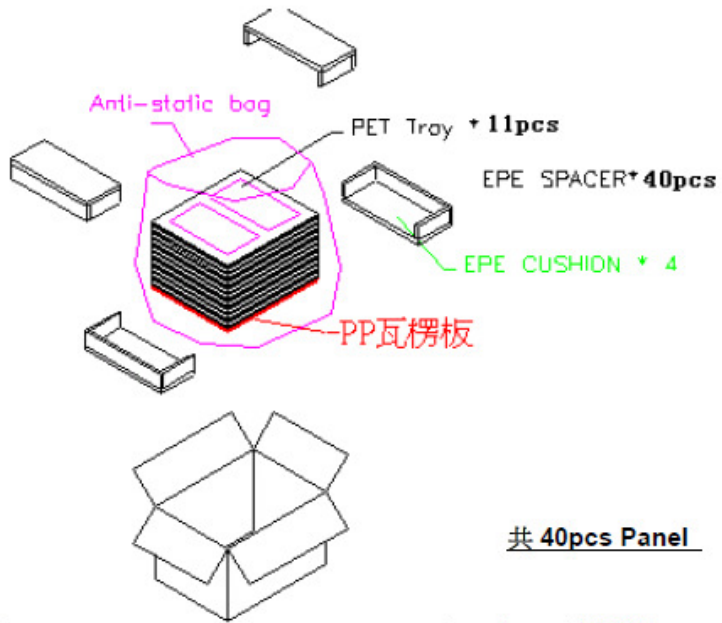
finish

10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Note
HEX		**HEX**	**DEC**	
0	Header	00	0	
1		FF	255	
2		FF	255	
3		FF	255	
4		FF	255	
5		FF	255	
6		FF	255	
7		00	0	
8	EISA Manuf. Code LSB	06	6	
9	Compressed ASCII	AF	175	
0A	Product Code	6D	109	
0B	hex, LSB first	30	48	
0C	32-bit ser #	00	0	
0D		00	0	
0E		00	0	
0F		00	0	
10	Week of manufacture	00	0	
11	Year of manufacture	1A	26	
12	EDID Structure Ver.	01	1	
13	EDID revision #	04	4	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	95	149	
15	**Max H image size** *(rounded to cm)*	1C	28	
16	**Max V image size** *(rounded to cm)*	10	16	
17	**Display Gamma** *(=(gamma*100)-100)*	78	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	2	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	78	120	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	60	96	
1B	Red x **(Upper 8 bits)**	A4	164	
1C	Red y/ highER 8 bits	55	85	
1D	Green x	52	82	
1E	Green y	9C	156	
1F	Blue x	27	39	
20	Blue y	0A	10	
21	White x	4E	78	
22	White y	52	82	
23	Established timing 1	00	0	
24	Established timing 2	00	0	
25	Established timing 3	00	0	
26	Standard timing #1	01	1	
27		01	1	

28	Standard timing #2	01	1	
29		01	1	
2A	Standard timing #3	01	1	
2B		01	1	
2C	Standard timing #4	01	1	
2D		01	1	
2E	Standard timing #5	01	1	
2F		01	1	
30	Standard timing #6	01	1	
31		01	1	
32	Standard timing #7	01	1	
33		01	1	
34	Standard timing #8	01	1	
35		01	1	
36	Pixel Clock/10000 LSB	14	20	
37	Pixel Clock/10000 USB	37	55	
38	Horz active **Lower 8bits**	80	128	
39	Horz blanking **Lower 8bits**	B8	184	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	70	112	
3B	Vertical Active **Lower 8bits**	38	56	
3C	Vertical Blanking **Lower 8bits**	24	36	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40	64	
3E	HorzSync. Offset	10	16	
3F	HorzSync.Width	10	16	
40	VertSync.Offset : VertSync.Width	3E	62	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	0	
42	Horizontal Image Size **Lower 8bits**	14	20	
43	Vertical Image Size **Lower 8bits**	9B	155	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	16	
45	Horizontal Border *(zero for internal LCD)*	00	0	
46	Vertical Border *(zero for internal LCD)*	00	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	24	
48	Detailed timing/monitor	10	16	
49	descriptor #2	2C	44	
4A		80	128	
4B		B8	184	
4C		70	112	
4D		38	56	
4E		24	36	
4F		40	64	
50		10	16	
51		10	16	
52		3E	62	

53		00	0	
54		14	20	
55		9B	155	
56		10	16	
57		00	0	
58		00	0	
59		18	24	
5A	Detailed timing/monitor	00	0	
5B	descriptor #3	00	0	
5C		00	0	
5D		FE	254	
5E		00	0	
5F	Manufacture	41	65	
60	Manufacture	55	85	
61	Manufacture	4F	79	
62		0A	10	
63		20	32	
64		20	32	
65		20	32	
66		20	32	
67		20	32	
68		20	32	
69		20	32	
6A		20	32	
6B		20	32	
6C	Detailed timing/monitor	00	0	
6D	descriptor #4	00	0	
6E		00	0	
6F		FE	254	
70		00	0	
71	Manufacture P/N	42	66	
72	Manufacture P/N	31	49	
73	Manufacture P/N	32	50	
74	Manufacture P/N	35	53	
75	Manufacture P/N	48	72	
76	Manufacture P/N	41	65	
77	Manufacture P/N	4E	78	
78	Manufacture P/N	30	48	
79	Manufacture P/N	33	51	
7A	Manufacture P/N	2E	46	
7B	Manufacture P/N	30	48	
7C		20	32	
7D		0A	10	

7E	Extension Flag	00	0	
7F	Checksum	9A	154	