



## Product Specification

AU OPTRONICS CORPORATION

( V ) Preliminary Specifications

( ) Final Specifications

Module	~8" XGA 4:3 Color TFT-LCD with LED Backlight design
Model Name	B080XAN02.0 (HW:0A)
Note	<i>LED Backlight without driving circuit design</i>

Customer	Date
Checked & Approved by	Date
Note: This Specification is subject to change without notice.	

Approved by	Date
Prepared by	
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## Contents

<b>1. Handling Precautions .....</b>	<b>4</b>
<b>2. General Description .....</b>	<b>5</b>
2.1 General Specification .....	5
2.2 Optical Characteristics .....	6
<b>3. Functional Block Diagram .....</b>	<b>11</b>
<b>4. Absolute Maximum Ratings .....</b>	<b>12</b>
4.1 Absolute Ratings of TFT LCD Module .....	12
4.2 Absolute Ratings of Environment .....	12
<b>5. Electrical Characteristics .....</b>	<b>13</b>
5.1 TFT LCD Module .....	13
5.2 Backlight Unit .....	17
<b>6. Signal Interface Characteristic .....</b>	<b>18</b>
6.1 Pixel Format Image .....	18
6.2 Integration Interface Requirement .....	19
6.4 MIPI Interface Timing .....	22
6.5 Power ON/OFF Sequence .....	23
<b>7. Panel Reliability Test .....</b>	<b>26</b>
7.1 Vibration Test .....	26
7.2 Shock Test .....	26
7.3 Reliability Test .....	26
<b>8. Mechanical Characteristics .....</b>	<b>27</b>
8.1 LCM Outline Dimension .....	27
9.1 Shipping Label Format .....	29
9.2 Carton Package .....	30
9.3 Shipping Package of Palletizing Sequence .....	30
<b>10. Appendix .....</b>	<b>30</b>
10.1 EDID Description (default) .....	30

## Record of Revision

[illegible]

## 1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

## 2. General Description

B080XAN02.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 4:3 XGA, 768(H) x 1024(V) screen and 262k colors (RGB 6-bits data driver) without LED backlight driving circuit. All input signals are MIPI interface compatible.

B080XAN02.0 is designed for a display unit of tablet style and industrial machine.

## 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	~8"			
Active Area	[mm]	119.808 (H) x 159.744 (V)			
Pixels H x V		768 x 3 (RGB) x 1024			
Pixel Pitch	[mm]	0.156 (V) x 3 x 0.052 X (H)			
Pixel Format		768 (RGB stripe, H) X 1024 (V)			
Display Mode		Normally Black			
White Luminance	[cd/m <sup>2</sup> ]	300 (5 points)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		600:1 typ.			
Response Time	[ms]	25 typ			
Nominal Input Voltage VDD	[Volt]	+3.7 typ.			
Power Consumption	[Watt]	0.8_max. (Logic) 1.54_max. (B/L without LED efficiency)			
Weight	[Grams]	90 max.			
Physical Size (panel only)	[mm]		Min.	Typ.	Max.
		Length	172.69	173.19	173.69
		Width	130.20	130.70	131.20
		Thickness	--	--	2.55 Panel side 4.35 PCBA side



# Product Specification

AU OPTRONICS CORPORATION

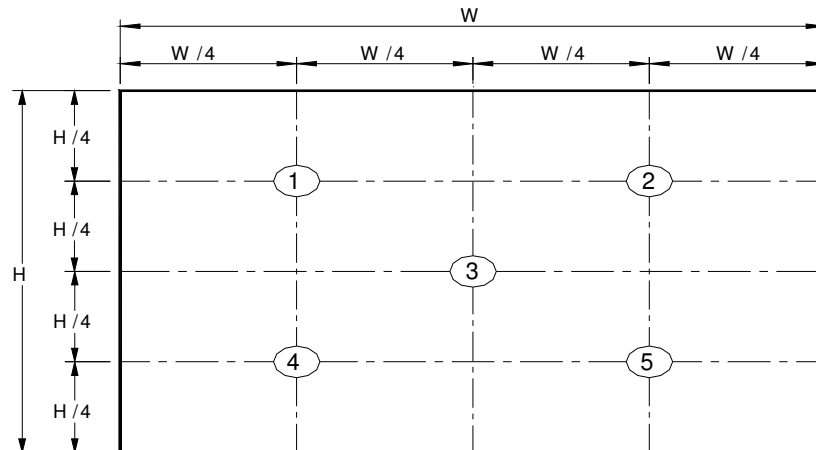
Electrical Interface		MIPI
Surface Treatment		HC
Support Color		262K colors ( RGB 6-bit )
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

## 2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance		5 Points	240	300	--	cd/m <sup>2</sup>	1, 3, 4
Viewing Angle	$\theta_R$ $\theta_L$	Horizontal (Right) CR = 10 (Left)	--	85 85	--	degree	3, 8
	$\psi_H$ $\psi_L$	Vertical (Upper) CR = 10 (Lower)	--	85 85	--		
Luminance Uniformity	$\delta_{5P}$	5 Points	--	--	1.25		1, 2, 3
Contrast Ratio	CR		--	600	--		3, 5
Cross talk	%		--	--	4		3, 6
Response Time	$T_{RT}$	Rising + Falling	--	25	35	msec	3, 7
Color / Chromaticity Coordinates	Red	Rx	CIE 1931	0.609			3
		Ry		0.359			
	Green	Gx		0.343			
		Gy		0.595			
	Blue	Bx		0.149			
		By		0.136			
	White	Wx		0.295	0.325	0.355	
		Wy		0.33	0.36	0.39	
NTSC	%		--	50	--		

**Note 1:** 5 points position (Ref: Active area)



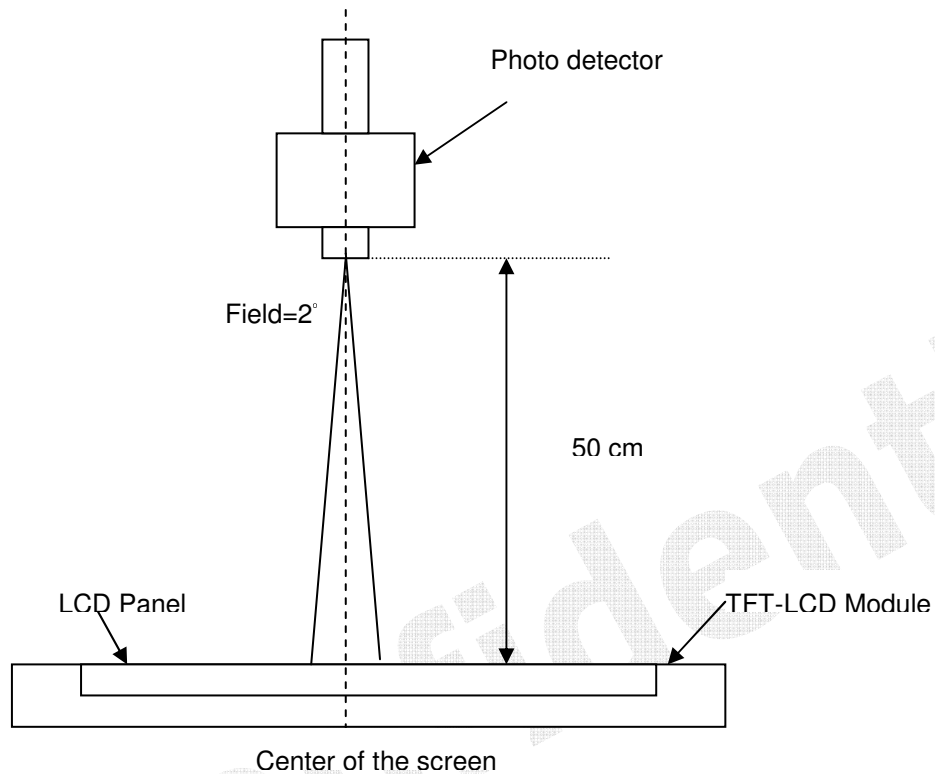
**Note 2:** The luminance uniformity of 5 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

**Note 3:** Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.





**Note 4 :** Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 63 at 5 points ,  $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$  is corresponding to the luminance of the point X at Figure in Note (1).

**Note 5 :** Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

**Note 6 :** Definition of Cross Talk (CT)

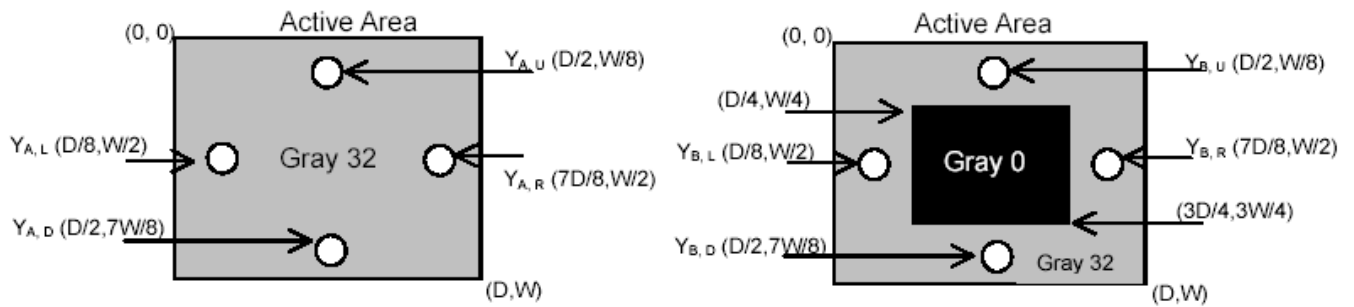
$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

$Y_A$  = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

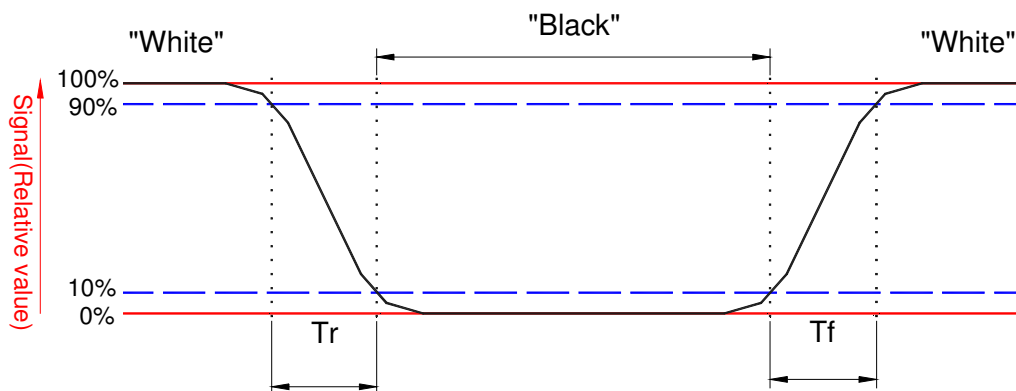
$Y_B$  = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)





**Note 7:** Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



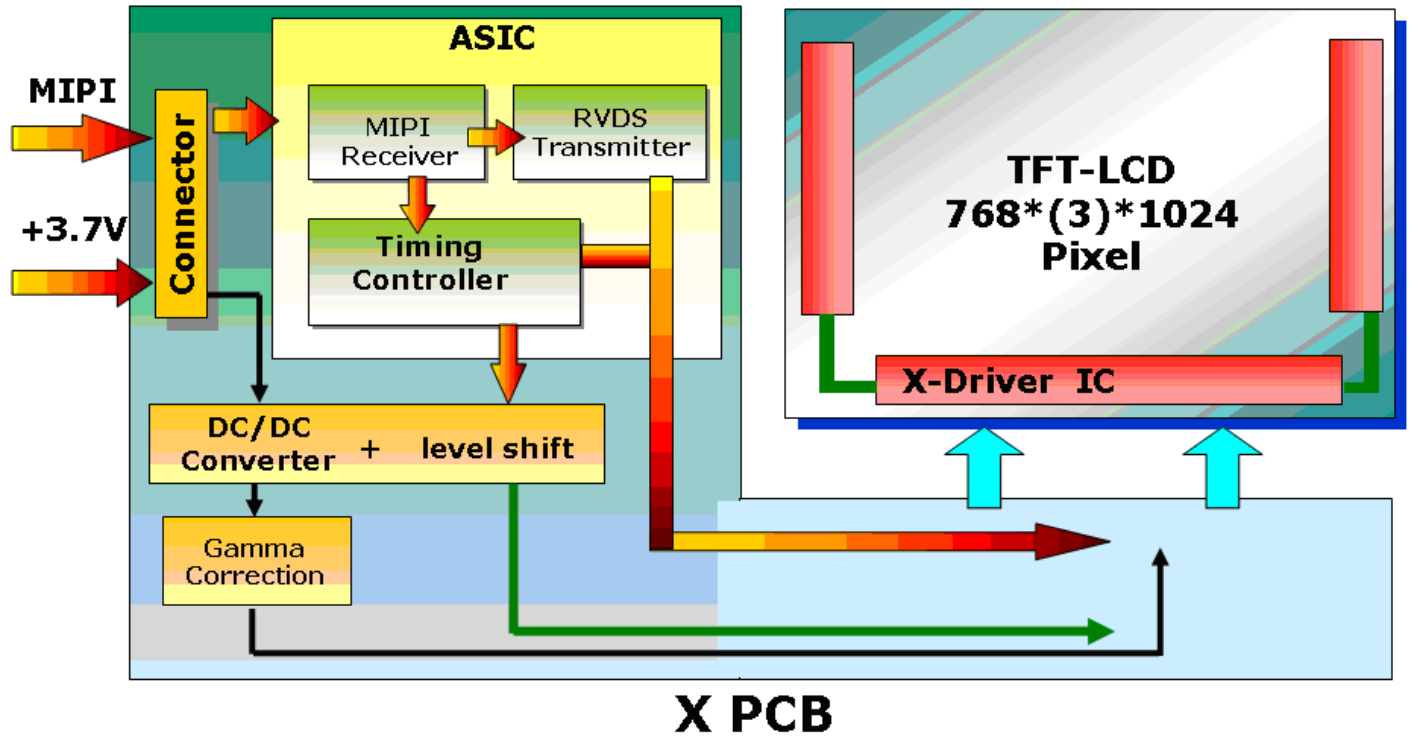
## Note 8. Definition of viewing angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a  $180^\circ$  horizontal and  $180^\circ$  vertical range (off-normal viewing angles). The  $180^\circ$  viewing angle range is broken down as follows;  $90^\circ$  ( $\theta$ ) horizontal left and right and  $90^\circ$  ( $\Phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



## 3. Functional Block Diagram

The following diagram shows the functional block of the ~8" inches wide Color TFT/LCD



## 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

### 4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

### 4.2 Absolute Ratings of Environment

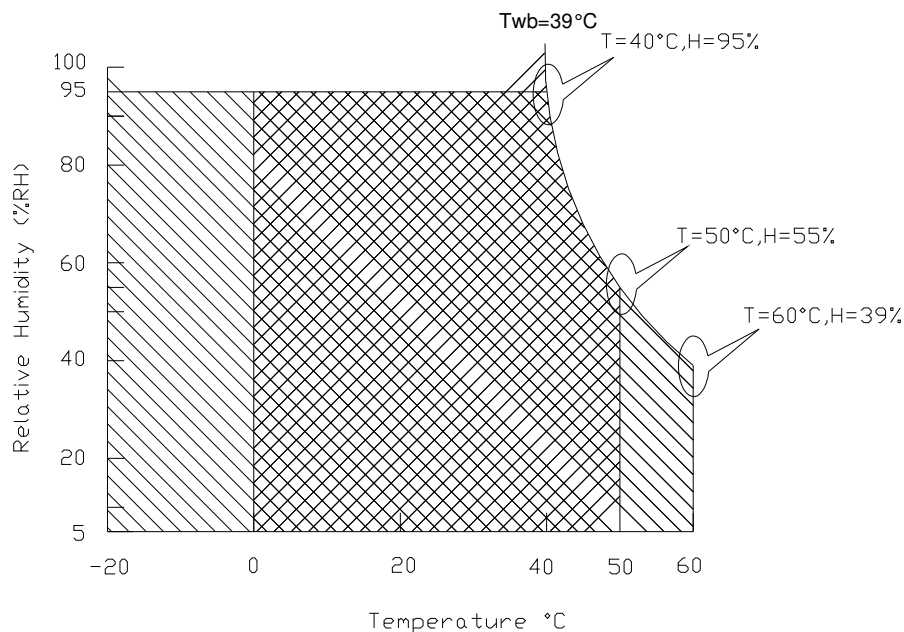
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C )

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

## 5. Electrical Characteristics

### 5.1 TFT LCD Module

#### 5.1.1 Power Specification

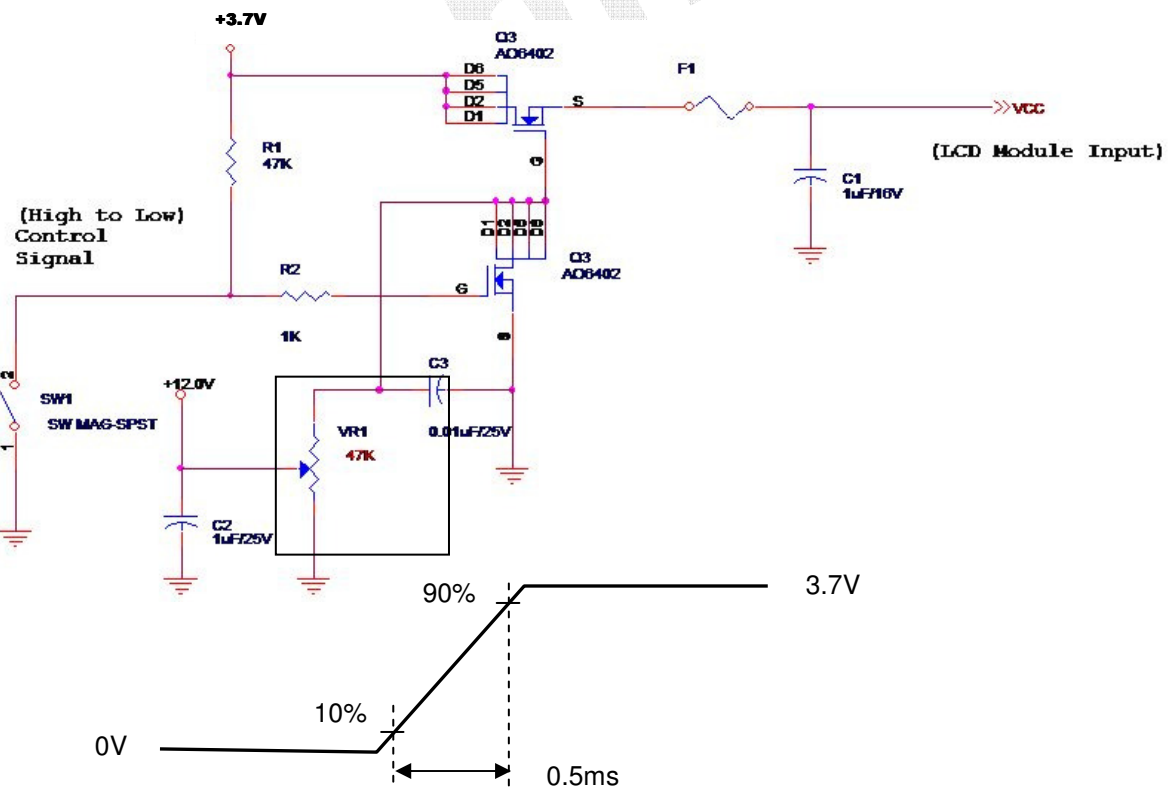
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.4	3.7	4.3	[Volt]	
PDD	VDD Power		0.7	0.8	[Watt]	Note 1
IDD	IDD Current		190	217	[mA]	Note 1
IRush	Inrush Current			1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition : White Pattern at 3.7V driving voltage. ( $P_{max}=V_{3.7} \times I_{white}$ )

Note 2 : Measure Condition



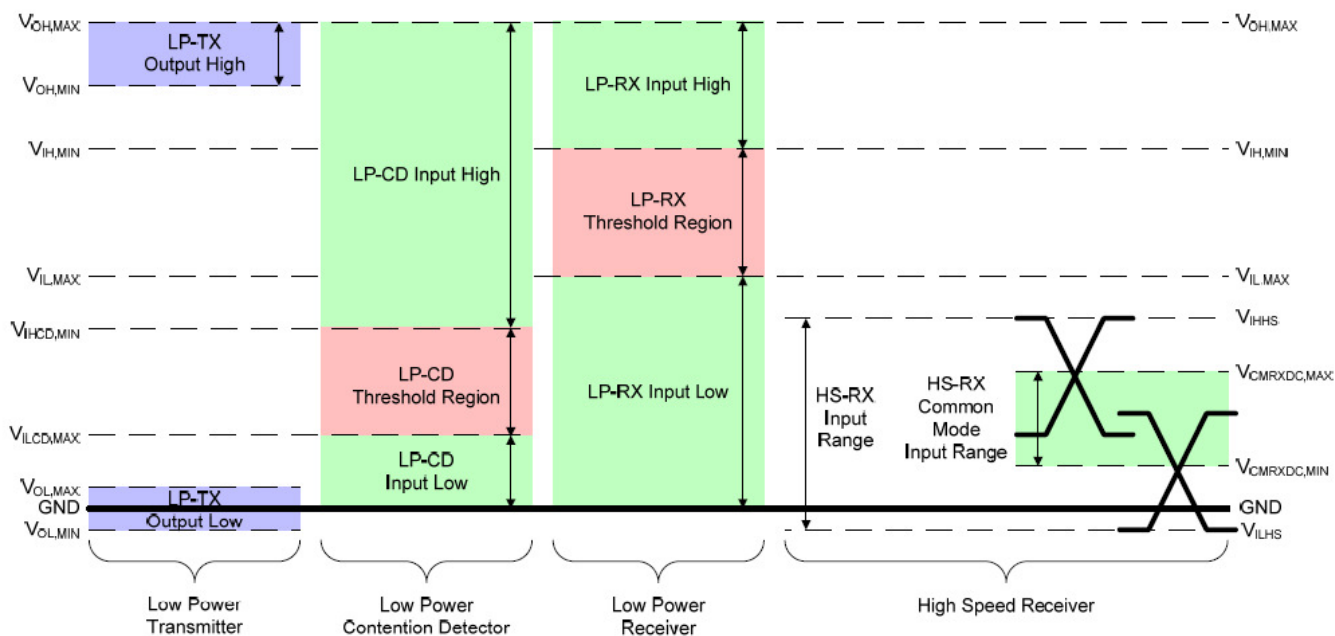
Vin rising time

## 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

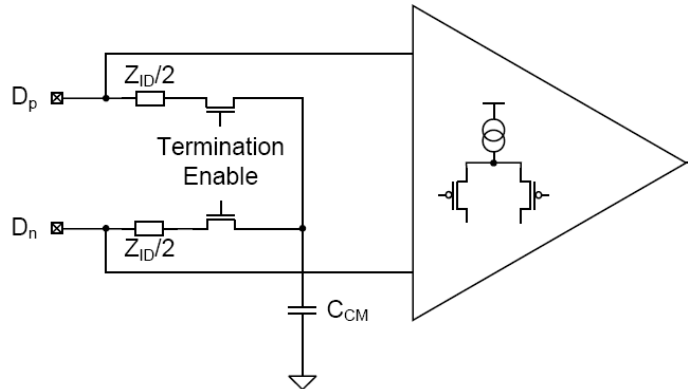
MIPI DC/AC Characteristics are as follows:

MIPI Receiver Differential Input (DC Characteristics)					
Symbol	Parameter	Min	Typ	Max	Unit
BR <sub>MIPI</sub>	Input data bit rate	-	513	560	Mbps
V <sub>IDTH</sub>	Differential input high threshold (HS Rx mode)	-	-	70	mV
V <sub>IDTL</sub>	Differential input low threshold (HS Rx mode)	-70	-	-	mV
V <sub>IHHS</sub>	Single-end input high voltage (HS Rx mode)	-	-	460	mV
V <sub>ILHS</sub>	Single-end input low voltage (HS Rx mode)	-40	-	-	mV
Z <sub>ID</sub>	Differential input impedance	80	100	125	Ω
V <sub>IHLP</sub>	Logic 1 input voltage (LP Rx mode)	880	-	-	mV
V <sub>ILLP</sub>	Logic 0 input voltage (LP Rx mode)	-	-	550	mV
V <sub>HYST</sub>	Input hysteresis	25	-	-	V
V <sub>IHCD</sub>	Logic 1 contention threshold	450	-	-	mV
V <sub>ILCD</sub>	Logic 0 contention threshold	-	-	200	mV



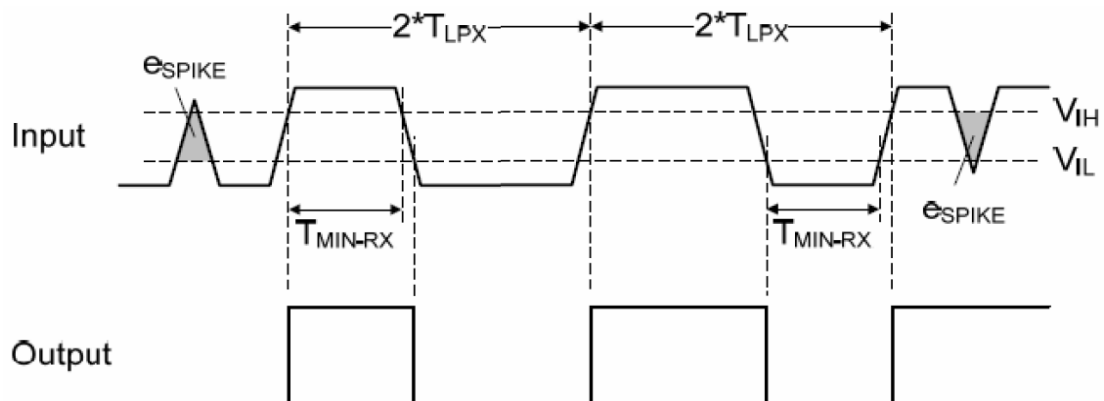
MIPI Receiver Input AC Electrical Characteristics						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz		-	-	100	mV
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz ~ 450MHz		-50	-	50	mV
$C_{CM}$	Common-mode termination		-	-	60	pF

HS RX Scheme

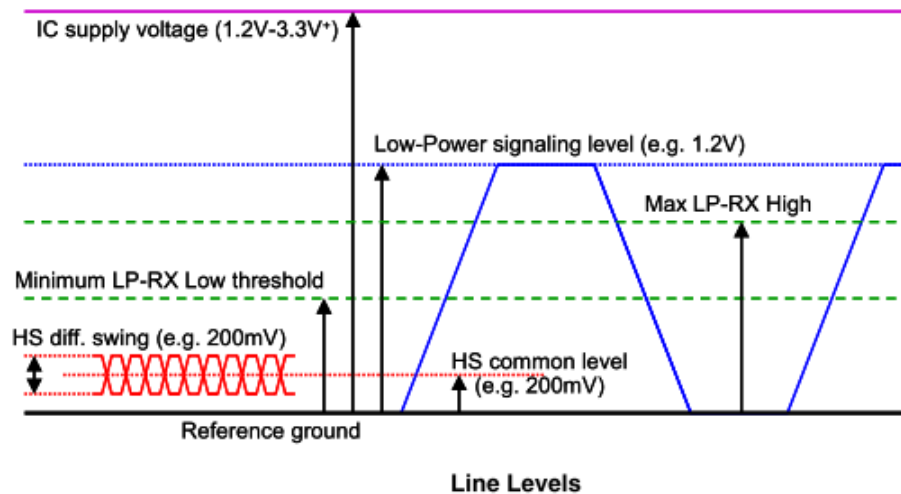


LP Receiver AC Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$e_{SPIKE}$	Input pulse rejection				300	V · ps
$T_{MIN-RX}$	Minimum pulse width response		20		-	ns
$V_{INT}$	Peak interference amplitude				200	mV
$f_{INT}$	Interference frequency		450			MHz

Input Glitch Rejection of Low-Power Receivers







## MIPI Special Requirement:

**Resolution : 768 x 3 x 1024, Frame rate : 60Hz, 6 bit, RGB6-6-6, 4 Lane**

### 1. HS Mode

To decode LP command correctly, MIPI clock lane should be in HS-Mode. If the escape mode entry procedure is followed-up by the entry command for Low-Power Data Transmission, data can be communicated by the protocol at low speed, while the lane remains in Low-Power mode. Data is self-clocked by the applied bit-encoding and does not rely on the clock lane.

### 2. Support Payload $\geq 2$ Bytes

The TCON cannot support long package with payload size is less than 2 Bytes.

### 3. 500Mbps $\leq$ MIPI bit rate $\leq$ 560M bps

Due to keep RVDS (Tcon output) frequency to 100MHz (Original setting). The MIPI bit rate must keep 500Mbps ~ 560Mbps (Nominal : 513Mbps)

(MIPI Operation frequency = 250MHz ~ 280MHz).

## MIPI Display ON Command

- DCS Short Write

### Ex . Power ON command

0x0602 = 0x1005 (Short packet, Data ID = 0x05)

0x0604 = 0x0000 (WC1,WC0=0 for DSC short write)

0x0610 = 0x0029 (Data1= 0,DCS Command)

0x0600 = 0x0001 (Start transfer)

Hex	Description	Packet Type
11h	Exit Sleep Mode	Short LP Mode
28h	Set Display Off	Short LP Mode
29h	Set Display On	Short LP Mode

## 5.2 Backlight Unit

### 5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	--	--	1.54	[Watt]	(Ta=25℃ @300nits)
LED Life-Time	N/A	-	5000	-	Hour	(Ta=25℃ @300nit) Note1.
LED Forward Voltage	VF	--	3.2	3.5	[Volt]	(Ta=25℃)
LED Forward Voltage of every LED string	VF-string	--	12.8	14	[Volt]	(Ta=25℃) Note2.
LED Forward Current	IF	--	23	--	[mA]	(Ta=25℃)

**Note 1.** The LED life-time define as the estimated time to 50% degradation of initial luminous.

**Note 2.** Every LED string consists of 4 pcs LED chip

## 6.1 Pixel Format Image

1 768

1st Line

24th Line

## 6.2 Integration Interface Requirement

### 6.2.1 MIPI Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	HIROSE
Type / Part Number	FH35W-35S-0.3SHW(50)

### 6.2.2 MIPI Pin Assignment

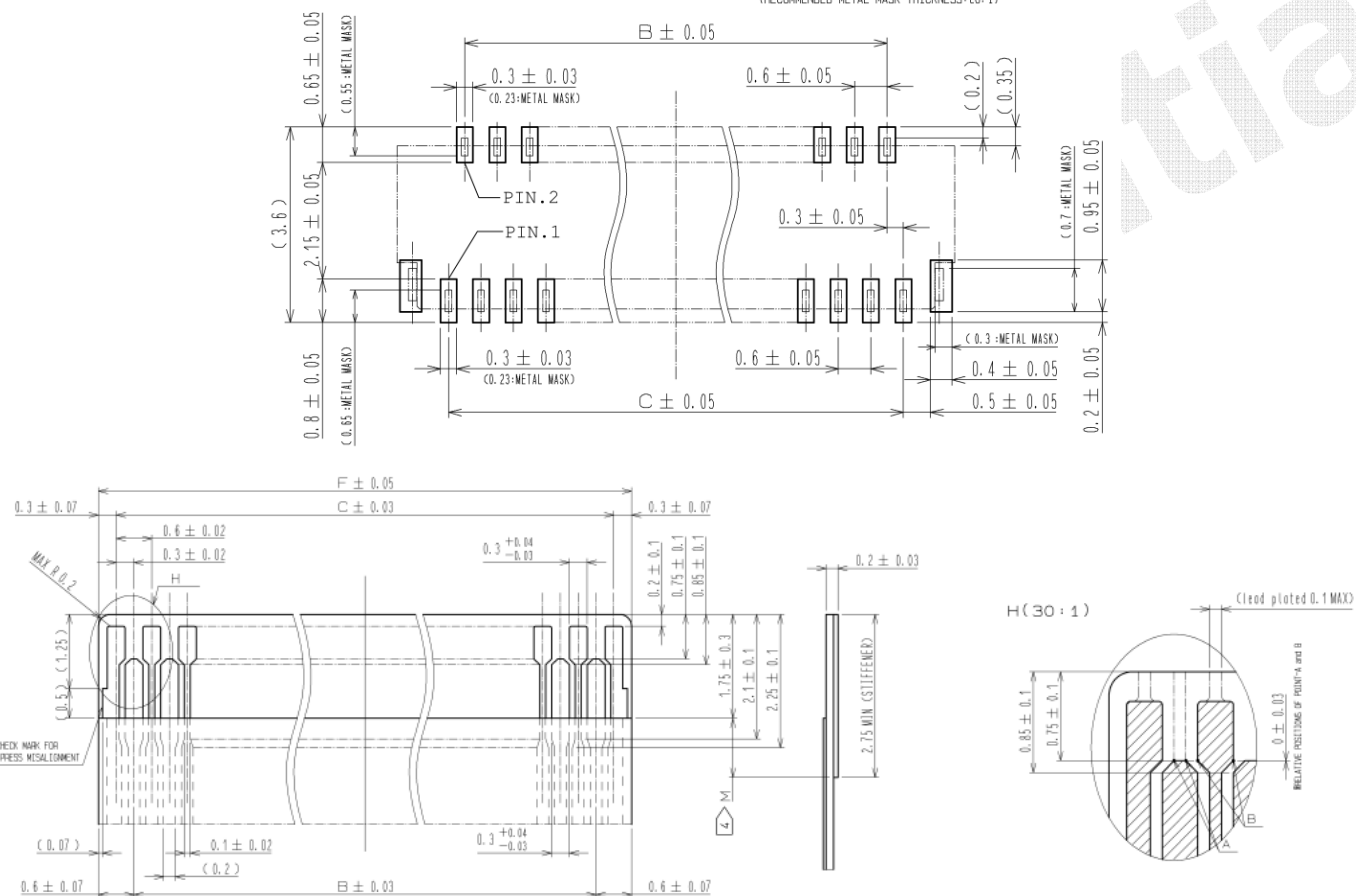
MIPI is a differential signal technology for LCD interface and high speed data transfer device.

Pin No		
1	AGING	AGING for BIST mode (allow 3.2~3.7V) AUO use only
2	NC	No connection
3	VDD	Panel power 3.7V
4	VDD	Panel power 3.7V
5	VDD	Panel power 3.7V
6	RST_MLC_L	Mipi T-con Reset (allow 3.2~3.7V)
7	GND	Ground
8	MIPI_D3N	Negative Mipi Differential Data INPUT pair 3
9	MIPI_D3P	Positive Mipi Differential Data INPUT pair 3
10	GND	Ground
11	MIPI_D2N	Negative Mipi Differential Data INPUT pair 2
12	MIPI_D2P	Positive Mipi Differential Data INPUT pair 2
13	GND	Ground
14	MIPI_D1N	Negative Mipi Differential Data INPUT pair 1
15	MIPI_D1P	Positive Mipi Differential Data INPUT pair 1
16	GND	Ground
17	MIPI_D0N	Negative Mipi Differential Data INPUT pair 0
18	MIPI_D0P	Positive Mipi Differential Data INPUT pair 0
19	GND	Ground
20	MIPI_CN	Negative Mipi Differential Clock INPUT
21	MIPI_CP	Positive Mipi Differential Clock INPUT
22	GND	Ground
23	FB_1	LED Feedback PIN 1
24	FB_2	LED Feedback PIN 2
25	FB_3	LED Feedback PIN 3
26	FB_4	LED Feedback PIN 4

27	FB_5	LED Feedback PIN 5
28	FB_6	LED Feedback PIN 6 (Spare)
29	NC	No connection
30	VLED	LED power
31	VLED	LED power
32	VLED	LED power
33	NC	No connection
34	PCLK	I2C CLK ( AUO use only )
35	PDATA	I2C DATA ( AUO use only )

#### RECOMMENDED PCB MOUNTING PATTERN

(RECOMMENDED METAL MASK THICKNESS:  $\leq 0.1$ )

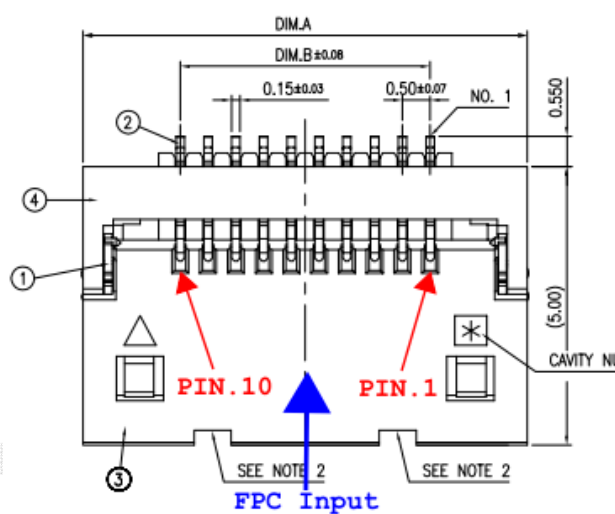


### 6.2.3 LED Connector Description

Connector Name / Designation	For Signal Connector
Manufacturer	STARCONN
Type / Part Number	112G10-000001-A2-R

## 6.2.4 LED Connector Description

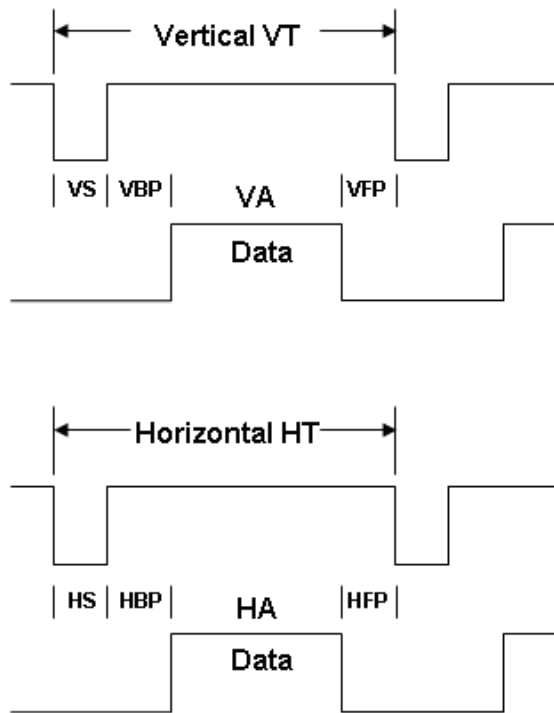
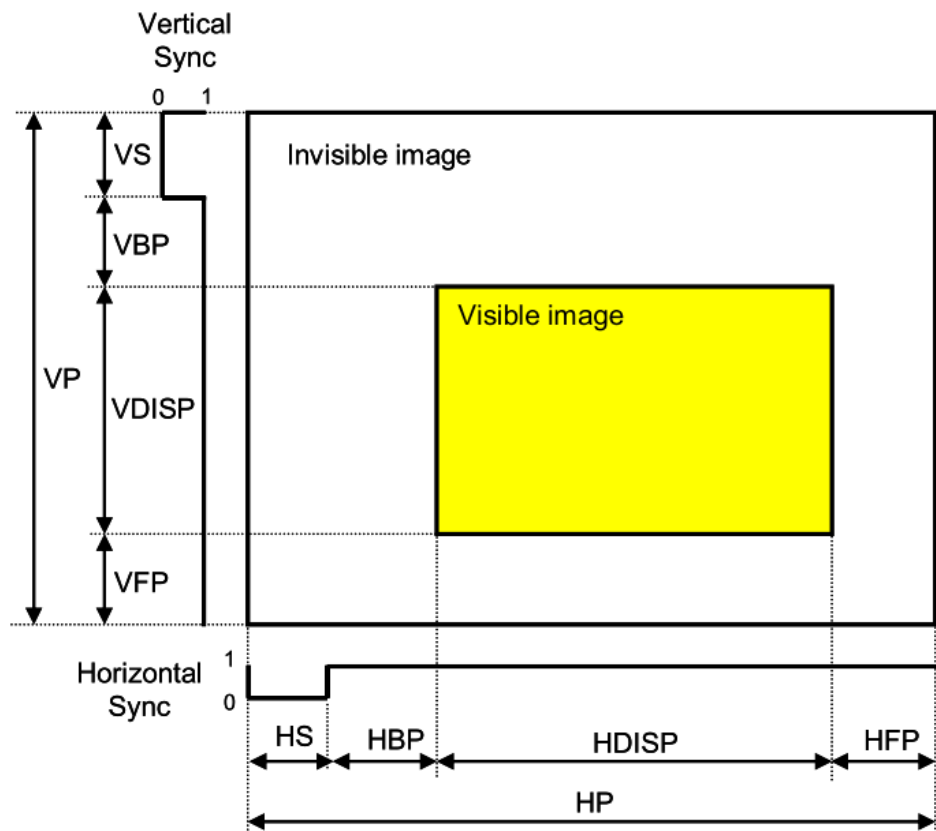
Pin No	09/05 AUO 1st version	
1	VOUT	LED Output
2	VOUT	LED Output
3	VOUT	LED Output
4	GND	Ground
5	Dummy	Dummy
6	FB1	LED Feedback PIN 1
7	FB2	LED Feedback PIN 2
8	FB3	LED Feedback PIN 3
9	FB4	LED Feedback PIN 4
10	FB5	LED Feedback PIN 5



## 6.4 MIPI Interface Timing

### 6.4.1 Timing Characteristics

Basically, interface timings should match the 768 x 1024 /60Hz manufacturing guide line timing.



Vertical Total	VT (tv)	1140	line
Vertical Front-Porch	VFP (tvfp)	36	line
Vertical Active	VA (tvd)	1024	line
Vertical Sync	VS (tvw)	50	line
Vertical Back-Porch	VBP (tvbp)	30	line
Horizontal Total	HT (th)	948	clk(pixel)
Horizontal Front-Porch	HFP (thfp)	60	clk(pixel)
Horizontal Active	HA (thd)	768	clk(pixel)
Horizontal Sync	HS (thw)	64	clk(pixel)
Horizontal Back-Porch	HBP (thbp)	56	clk(pixel)
Pixel Frequency	CLK (fc)	64.8	MHz



## 6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.

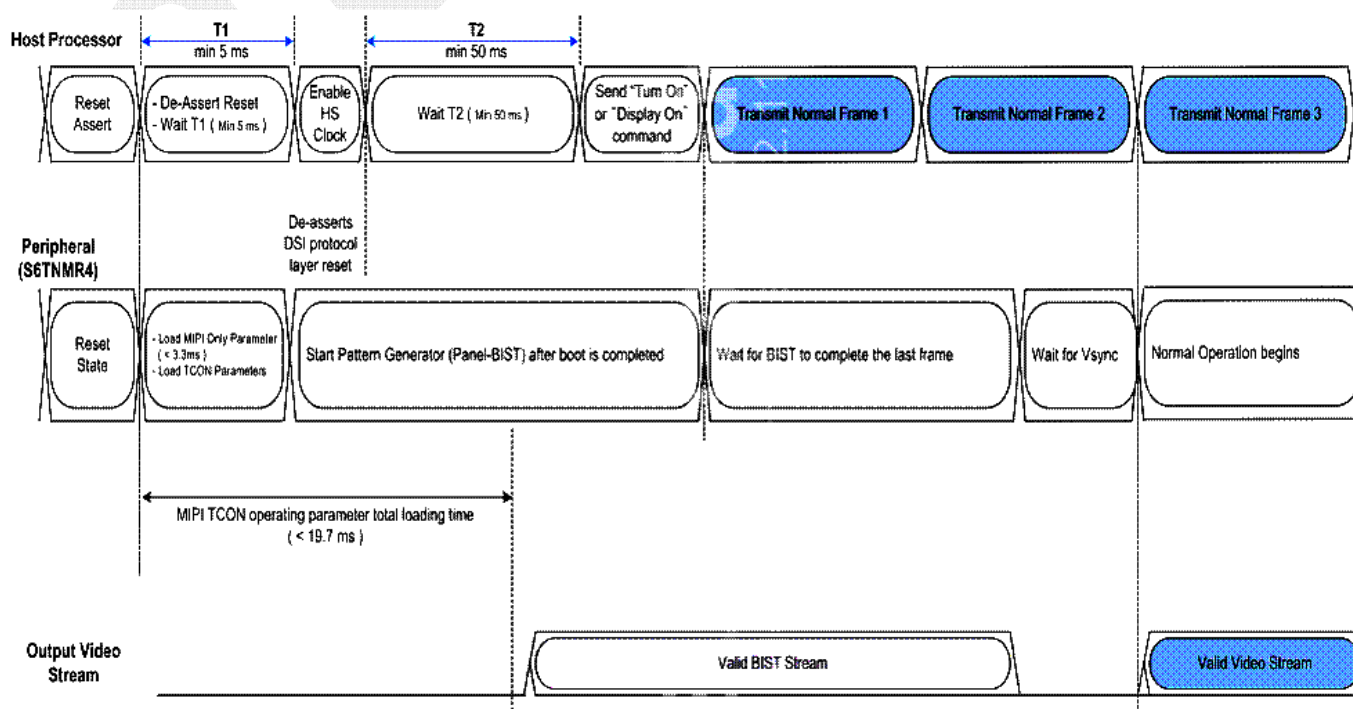
### Power ON Sequence

#### System Initialize and Power-On Sequence

#### System Initialize and Power On Sequence

Step	Host Processor	Peripheral (TCON)
1	Assert Reset	Reset State
2	De-Assert Reset	Start to load TCON parameter via serial EEPROM mounted on Display module
3	Wait for (T1) ms (min. required (T1) time is 5 ms)	Initializes MIPI-DSI slave and interface immediately after related parameter loading operation finished (< 3.3 ms)
4	Enable High-Speed Clock (NOTE)	De-asserts DSI protocol layer reset
5	Wait for (T2) ms (min. required (T2) time is 50 ms)	Start Pattern Generator (Panel-BIST) after all parameter loading are completed
6	Sends "Turn On" or "Display On" Command	—
7	Transmit Normal Frame	Stops Panel BIST operation and normal operation begins when valid Vsync (from mipi-interface) received

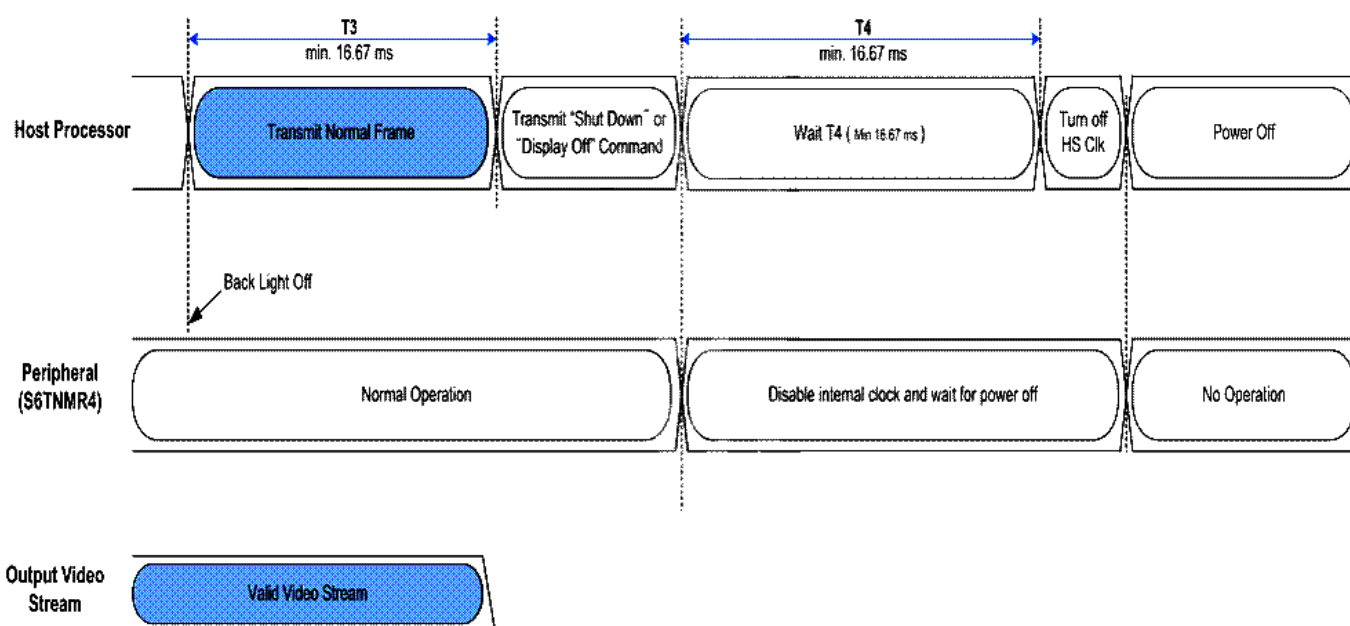
**NOTE:** Host should maintain its high-speed clock to guarantee continuous clock behavior on the Clock Lane



## Power OFF Sequence

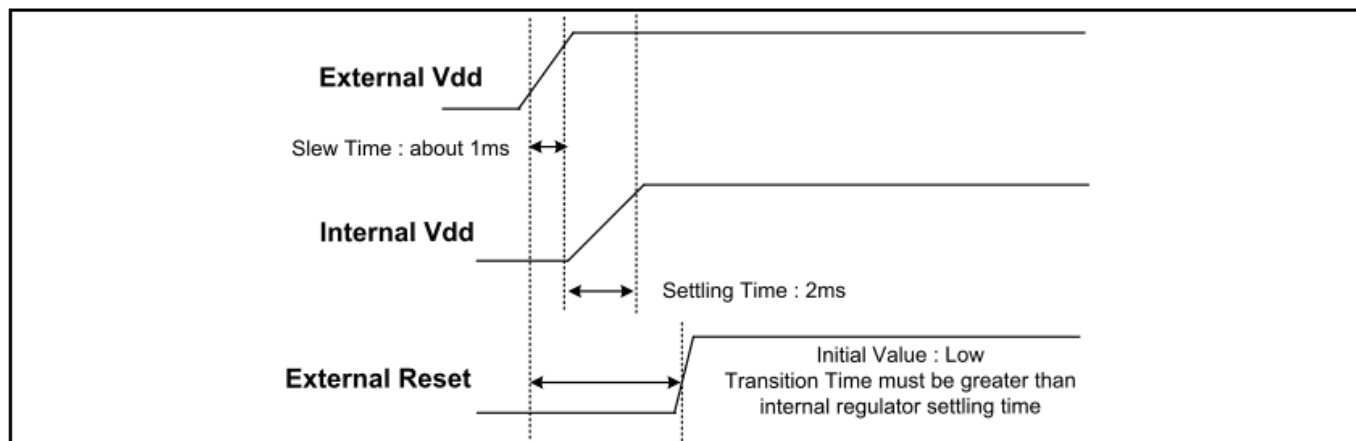
System Shut Down and Power Off Sequence

Step	Host Processor	Peripheral
1	Back Light Off	Normal operation <b>(TCON)</b>
2	Wait for (T3) ms (min. required (T3) time is 16.67 ms)	Normal operation
3	Sends "Shut Down" or "Display Off" Command	1) Wait for generated frame is transmitted by RVDS 2) Disable internal clock and wait power off
4	Wait for (T4) ms (min. required (T4) time is 16.67 ms)	—
5	Turn Off HS_CLK	—
6	Power Off	—



## Reset Period

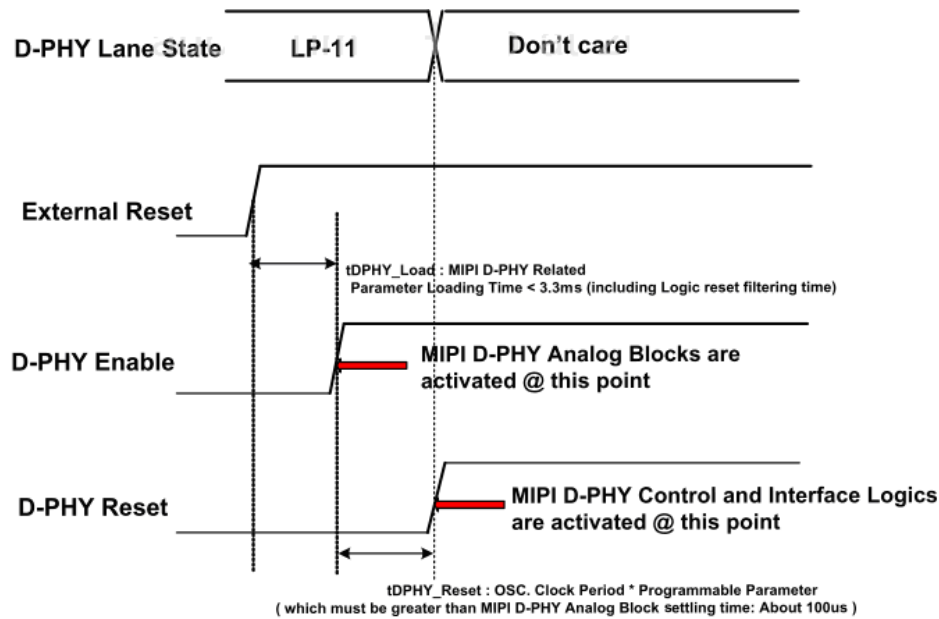
TCON needs at least 3 ms of reset period for internal LDO stabilization.



Timing Diagram of Reset Period

**MIPI D-PHY Lane State**

MIPI D-PHY lane state must be in stop (LP-11) state for proper slave D-PHY initialization. MIPI slave D-PHY analog block would be activated after finishing related parameter loading procedure.



**MIPI D-PHY Lane State Timing Diagram**

## 7. Panel Reliability Test

### 7.1 Vibration Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

### 7.2 Shock Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

### 7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C , 90%RH, 300h	
High Temperature Operation	Ta= 50°C , Dry, 300h	
Low Temperature Operation	Ta= 0°C , 300h	
High Temperature Storage	Ta= 60°C , 300h	
Low Temperature Storage	Ta= -20°C , 300h	
Thermal Shock Test	Ta=-20°C to 60°C , Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

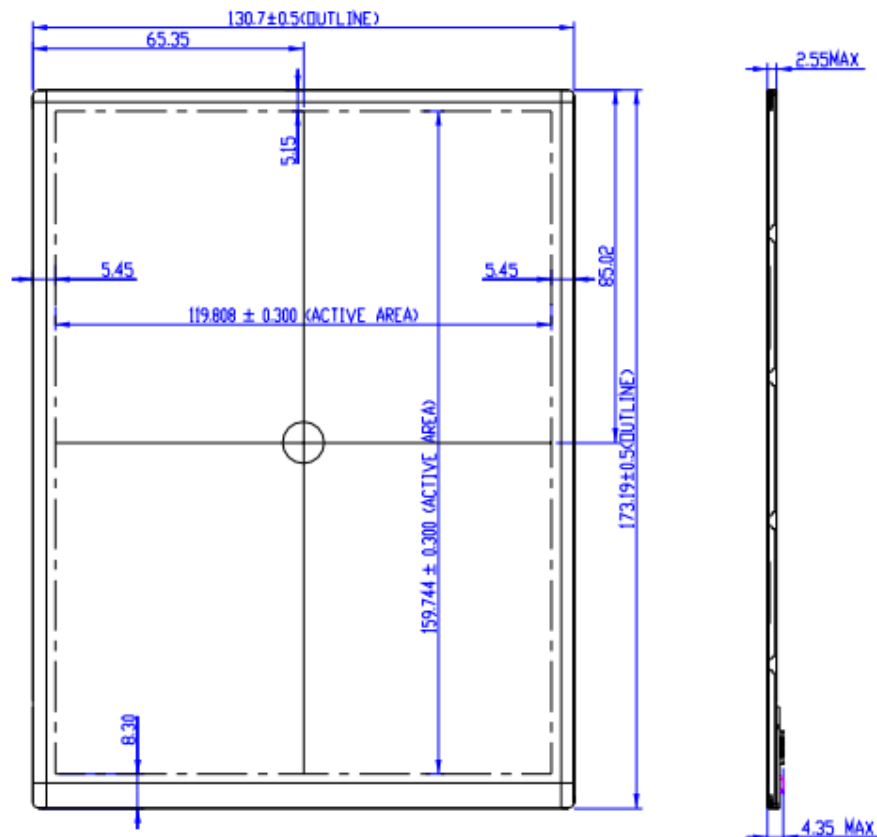
**Note1:** According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost  
. Self-recoverable. No hardware failures.

**Remark:** MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

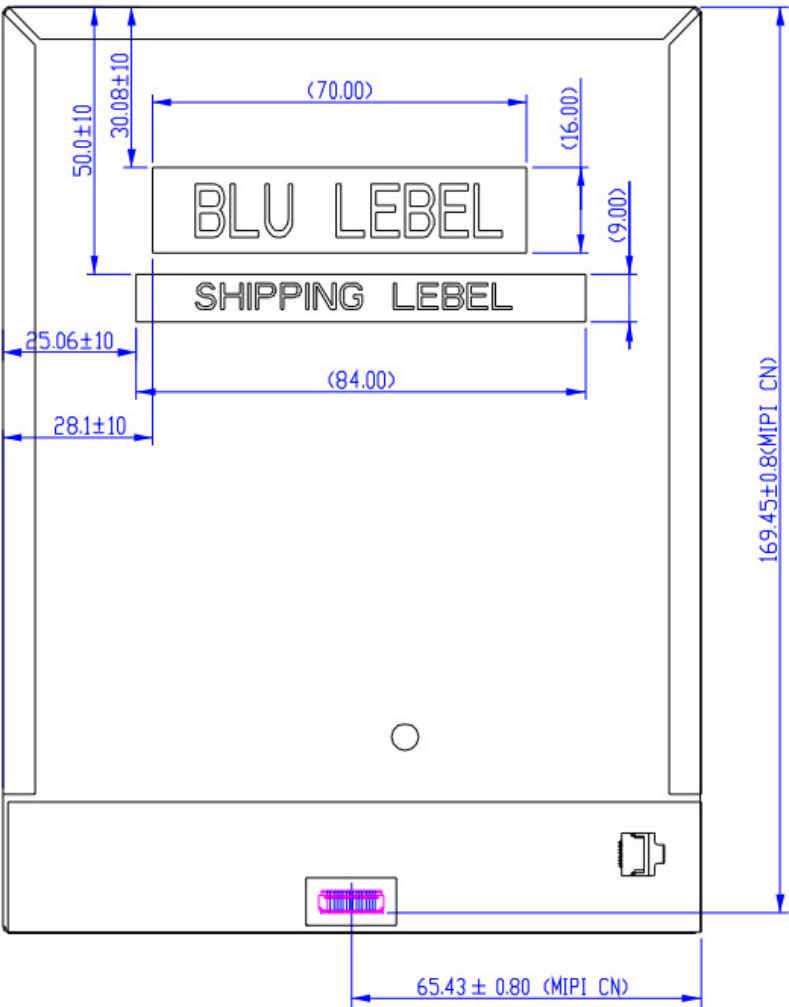
## 8. Mechanical Characteristics

### 8.1 LCM Outline Dimension

#### 8.1.1 Standard Front View





8.1.2 Standard Rear View







# 9.1 Shipping Label Format

## Shipping label

  
\*XXXXXXXXXXXXX.XXXXXX

  
B080XAN02.0

Manufactured YY/WW  
Model No: B080XAN02.0  
AU Optronics  
Made in China (Z30)  
H/W: 0A F/W:1





## **9.2 Carton Package**

TBD

## **9.3 Shipping Package of Palletizing Sequence**

TBD

## **10. Appendix**

### **10.1 EDID Description (default)**

TBD

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