



Product Specification

AU OPTRONICS CORPORATION

B141PW01 V4

() Preliminary Specifications

(V) Final Specifications

Module	14.1" WXGA+ Color TFT-LCD
Model Name	B141PW01 V4

Customer	Date
_____	_____
Checked & Approved by	
_____	_____
Note: This Specification is subject to change without notice.	

Approved by	Date
_____	_____
Prepared by	
_____	_____
NBBU Marketing Division / AU Optronics corporation	



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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2006/10/30		First Edition for Customer		
1.0 2007/5/9	1	Preliminary Specifications	Final Specifications	



1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
- 14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.



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2. General Description

B141PW01 V4 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA+ (1440(H) x 900(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter of backlight is not included.

B141PW01 V4 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	357.7 (14.1W")
Active Area	[mm]	303.48 X 189.675
Pixels H x V		1440x3(RGB) x 900
Pixel Pitch	[mm]	0.21075X0.21075
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (I _{CCFL} =6.0mA) Note: I _{CCFL} is lamp current	[cd/m ²]	200 typ. (5 points average) 185 min. (5 points average) (Note1)
Luminance Uniformity		1.2 max. (5 points)
Contrast Ratio		500 typ
Optical Rise Time/Fall Time	[msec]	5/11 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption	[Watt]	5.5 typ .(without inverter)
Weight	[Grams]	400 typ.(without inverter)
Physical Size	[mm]	320.5(W) x 206 (H) x 5.5(D) Max.
Electrical Interface		2 channel LVDS
Surface Treatment		Hard coating 3H,Glare
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance



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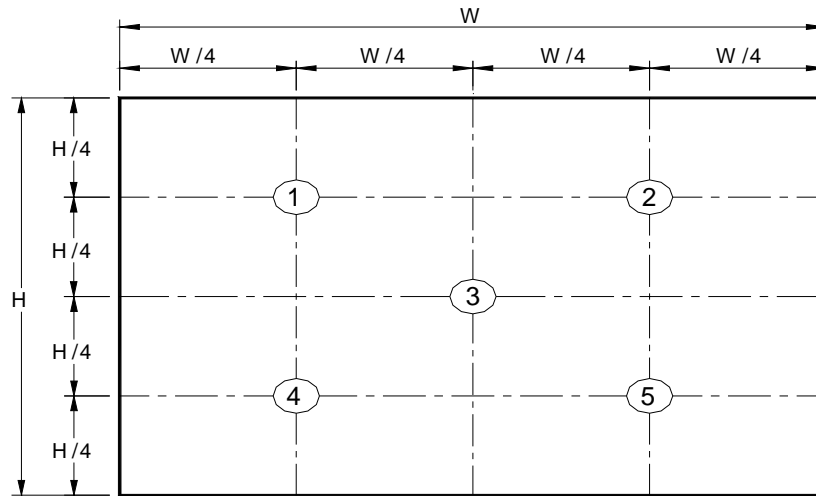
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2.2 Optical Characteristics

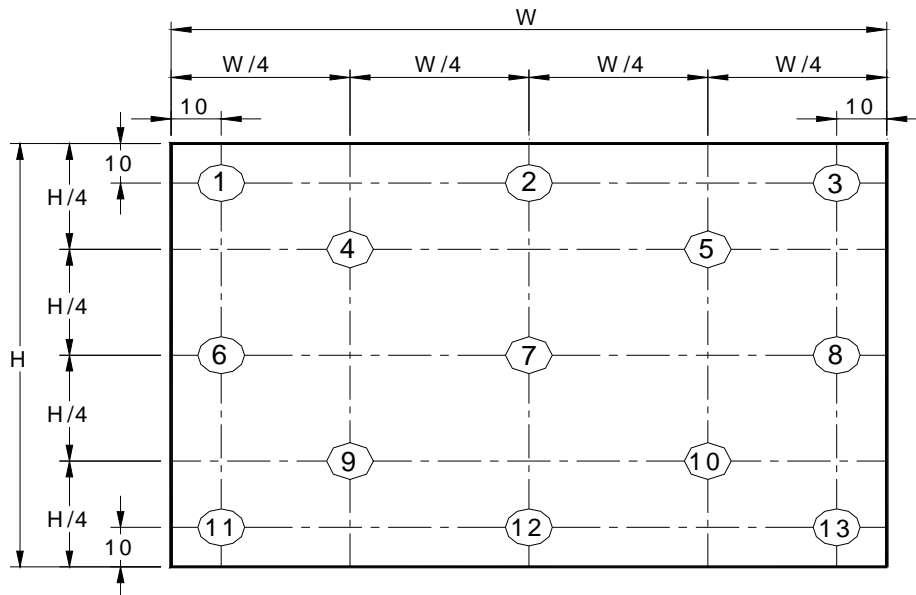
The optical characteristics are measured under stable conditions at 25 (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance I _{CCFL} =6.0mA	[cd/m ²]	5 points average	185	200	-	1, 4, 5.
Viewing Angle	[degree]	Horizontal (Right) CR = 10 (Left)	-	45	-	8
	[degree]		-	45	-	
	[degree]	Vertical (Upper) CR = 10 (Lower)	-	20	-	
	[degree]		-	35	-	
Luminance Uniformity		5 Points			1.2	1
Luminance Uniformity		13 Points			1.8	2
CR: Contrast Ratio			400	500	-	6
Cross talk	%				1.4	7
Response Time	[msec]	Rising	-	5	6	8
	[msec]	Falling	-	11	14	
	[msec]	Rising + Falling		16	20	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.550	0.580	0.610	2,8
		Red y	0.310	0.340	0.370	
		Green x	0.280	0.310	0.340	
		Green y	0.520	0.550	0.580	
		Blue x	0.125	0.155	0.185	
		Blue y	0.115	0.145	0.175	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	

Note 1: 5 points position (Display area : 303.48mm x 189.675mm)



Note 2: 13 points position



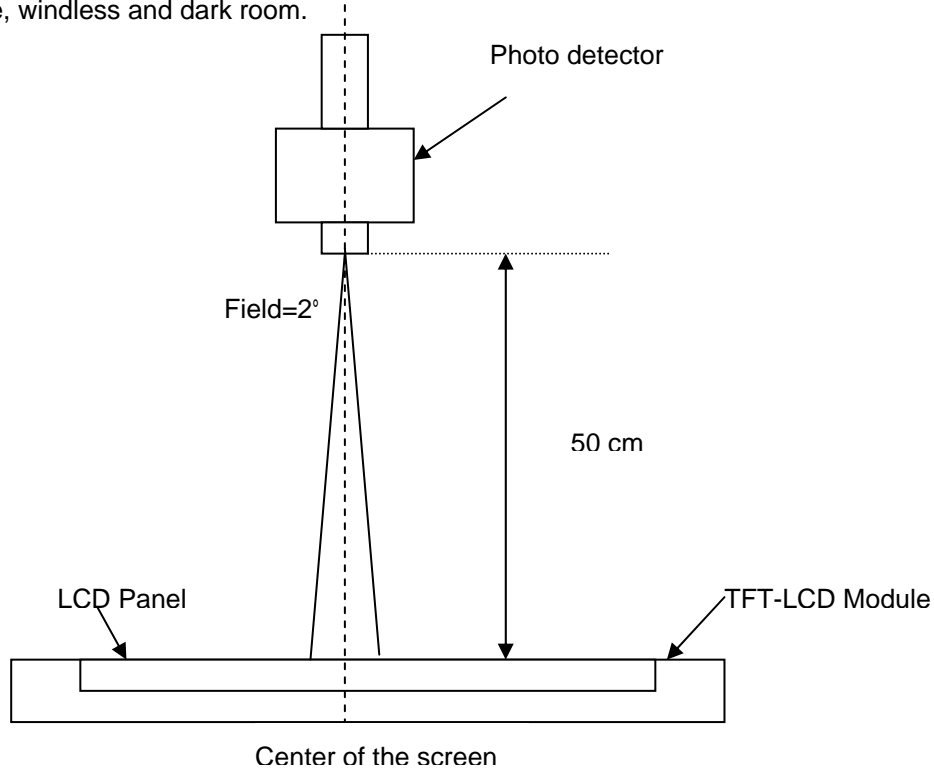
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$W_5 = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$W_{13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5$

$L (x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

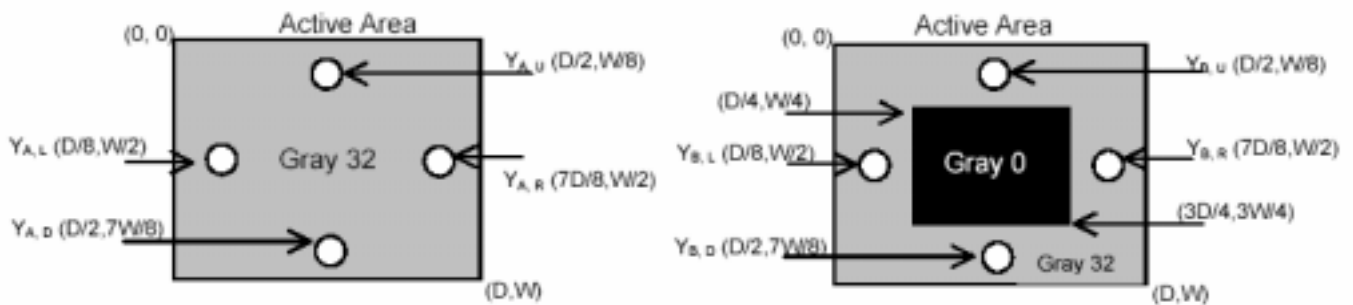
Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

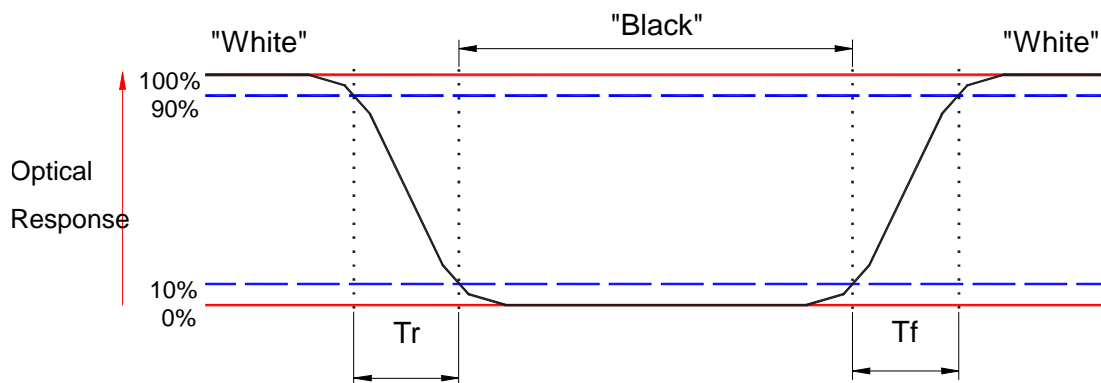
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



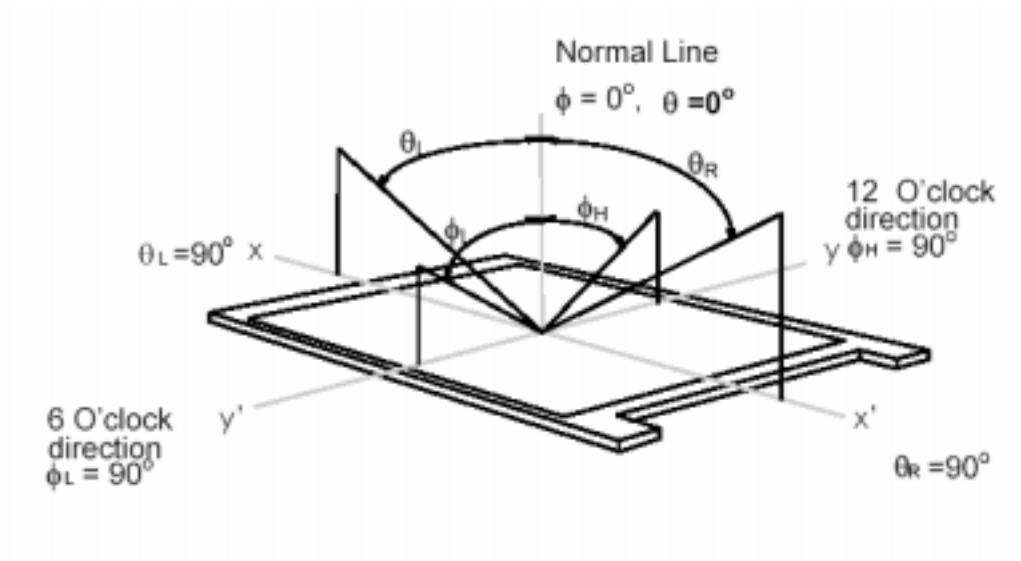
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 8. Definition of viewing angle

Viewing angle is the measurement of contrast ratio 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° () horizontal left and right and 90° () vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.





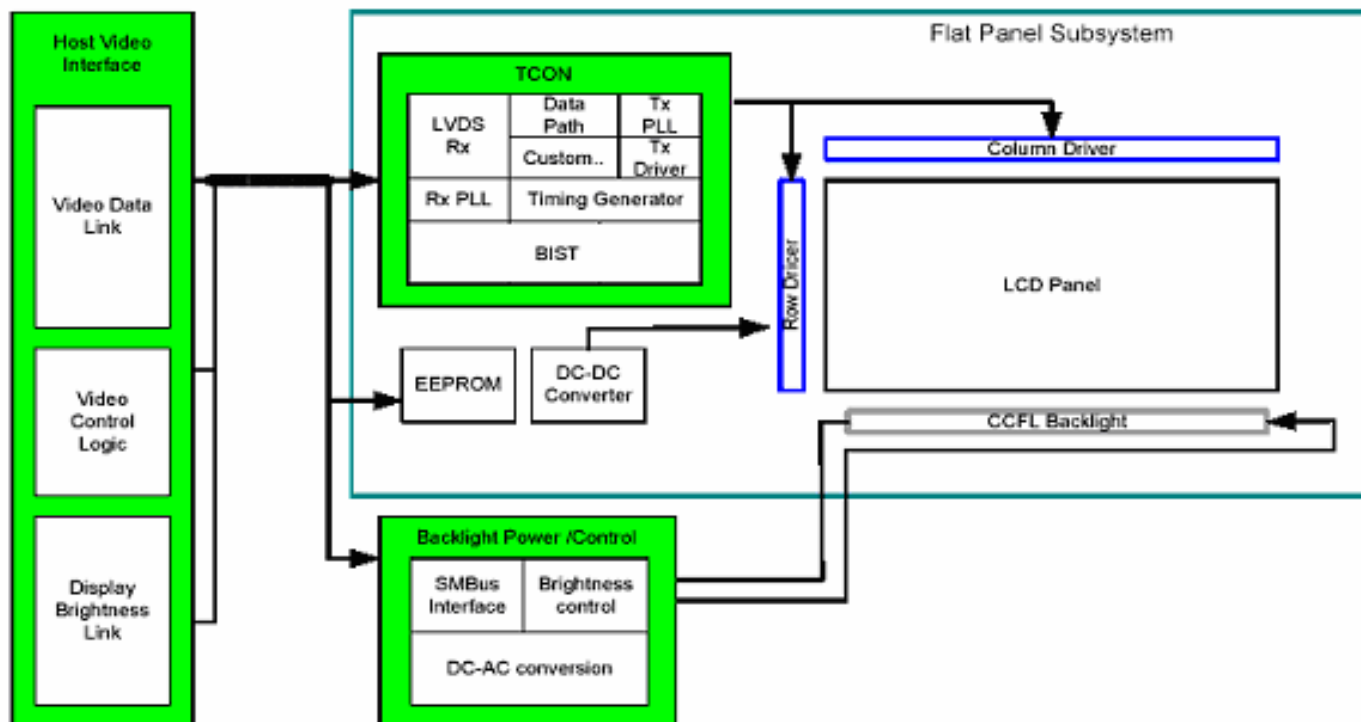
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3. Functional Block Diagram

The following diagram shows the functional block of the 14.1 inches wide Color TFT/LCD Module:





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4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	2.5	7	[mA] rms	Note 1,2

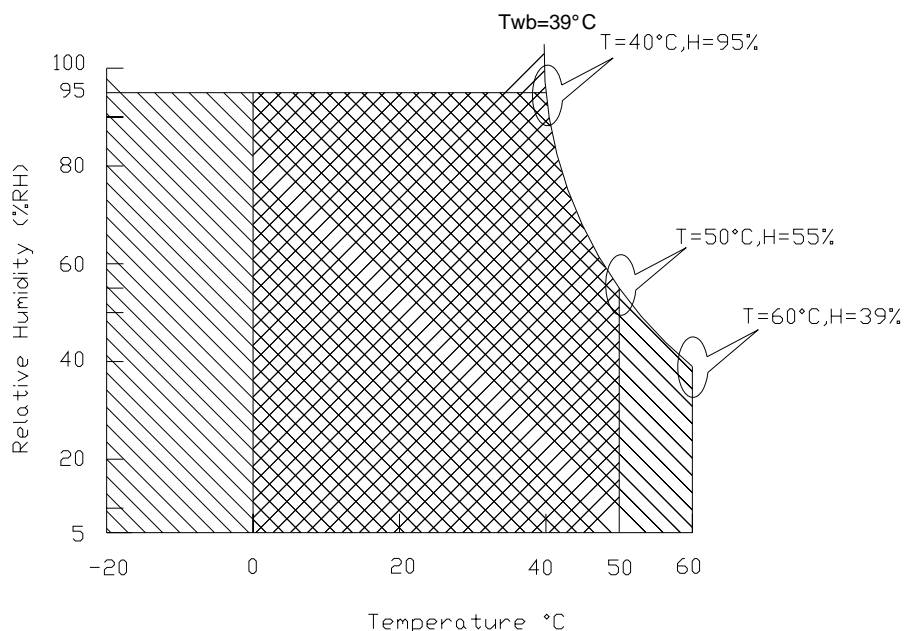
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25)

Note 2: Permanent damage to the device may occur if exceed maximum values

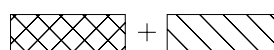
Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range



Storage Range





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5.1.2 Signal Electrical Characteristics

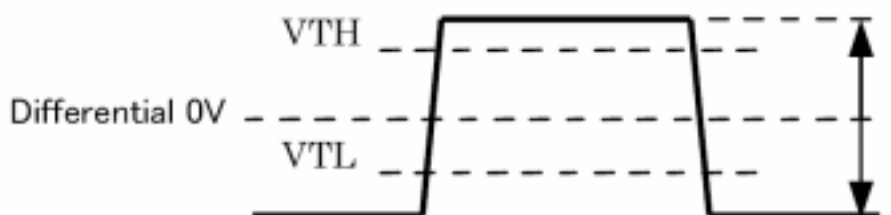
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of SN75LVDS86DGG (Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Differential Voltage





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5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	185	200	-	[cd/m ²]	(Ta=25)
CCFL current(I _{CCFL})	2.5	6.0	7	[mA] rms	(Ta=25) Note 2
CCFL Frequency(F _{CCFL})	50	60	65	[KHz]	(Ta=25) Note 3,4
CCFL Ignition Voltage(V _s)	-	1000	1200	[Volt] rms	(Ta= 0) Note 5
CCFL Voltage (Reference) (V _{CCFL})	-	650	-	[Volt] rms	(Ta=25) Note 6
CCFL Power consumption (P _{CCFL})	-	4.2	-	[Watt]	(Ta=25) Note 6

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has "Duty Dimming", if ICCFL is less than 4mA.

Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,430 voltage. Lamp units need 1,400 voltage minimum for ignition.



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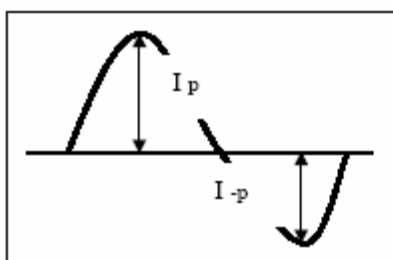
Note 6: Calculator value for reference ($I_{CCFL} \times V_{CCFL} = P_{CCFL}$)

Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

- The asymmetry rate of the inverter waveform should be less than 10%.
- The distortion rate of the waveform should be within $2 \pm 10\%$.

* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$$\frac{|I_p - I_{-p}|}{I_{rms}} \times 100\%$$

* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{rms}$$

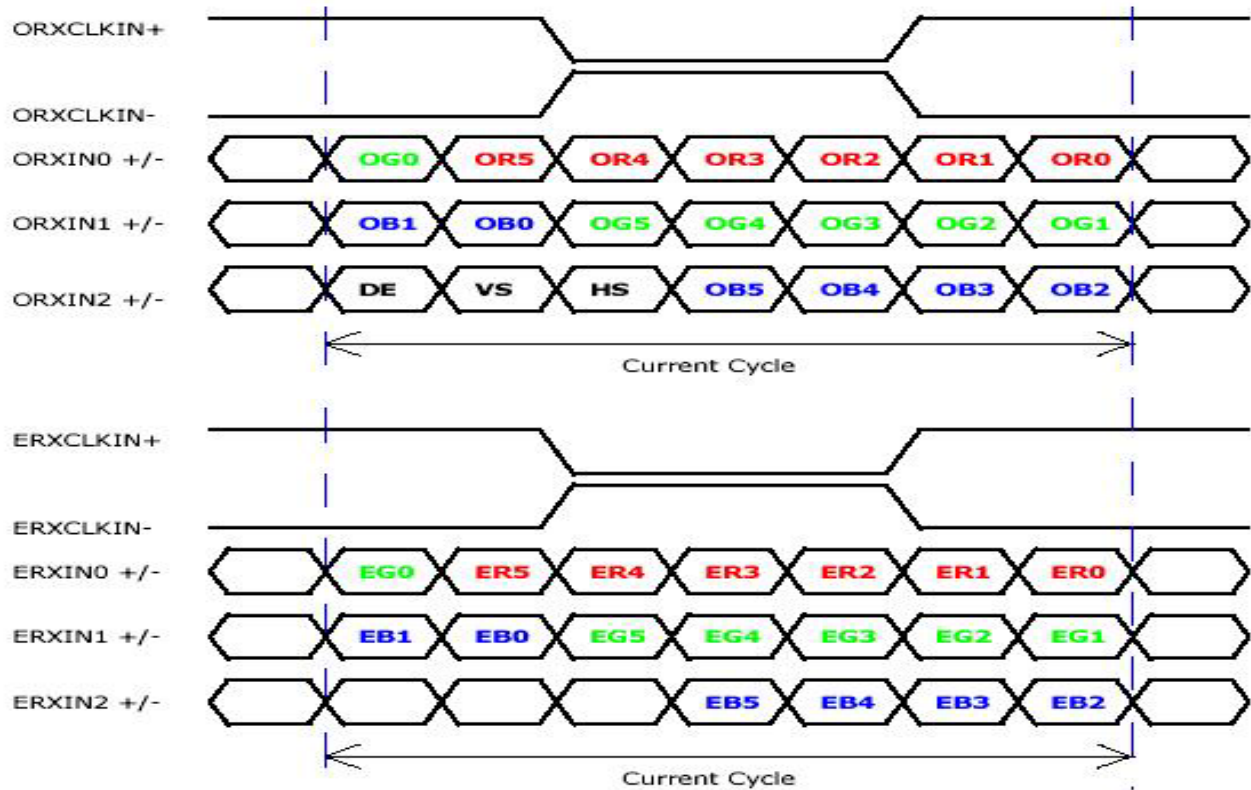
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

[illegible]

6.2 The input data format



6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Signal Name	Description
V _{EDID}	+3.3V EDID Power
CLK _{EDID}	EDID Clock Input
DATA _{EDID}	EDID Data Input
ORXIN0-, ORXIN0+	Odd LVDS differential data input(ORed0-ORed5, OGreen0)
ORXIN1-, ORXIN1+	Odd LVDS differential data input(OGreen1-OGreen5, OBlue0-OBue1)
ORXIN2-, ORXIN2+	Odd LVDS differential data input(OBlue2-OBlue5, Hsync, Vsync, DE)
ORXCLKIN-, ORXCLKIN+	Odd LVDS differential clock input
ERXIN0-, ERXIN0+	Even LVDS differential data input(ERed0-ERed5, EGreen0)
ERXIN1-, ERXIN1+	Even LVDS differential data input(EGreen1-EGreen5, EBlue0-EBue1)
ERXIN2-, ERXIN2+	Even LVDS differential data input(EBlue2-EBlue5)
ERXCLKIN-, ERXCLKIN+	Even LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground



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Pin no	Symbol	Function	Etc.
1	GND	Ground	
2	VDD	Power supply ,3.3 V (typical)	
3	VDD	Power supply ,3.3 V (typical)	
4	V _{DDP}	DDC 3.3V power	
5	NC	No Connection (Reserved for AUO) test	
6	CLK _{DDIO}	DDC Clock	
7	Data _{DDIO}	DDC data	
8	Odd_RxIN0-	-LVDS differential data input	
9	Odd_RxIN0+	+LVDS differential data input	
10	GND	Ground	
11	Odd_RxIN1-	-LVDS differential data input	
12	Odd_RxIN1+	+LVDS differential data input	
13	GND	Ground	
14	Odd_RxIN2-	-LVDS differential data input	
15	Odd_RxIN2+	+LVDS differential data input	
16	GND	Ground	
17	Odd_RxCLKIN-	-LVDS differential clock input	
18	Odd_RxCLKIN+	+LVDS differential clock input	
19	GND	Ground	
20	Even_RxIN0-	-LVDS differential data input	
21	Even_RxIN0+	+LVDS differential data input	
22	GND	Ground	
23	Even_RxIN1-	-LVDS differential data input	
24	Even_RxIN1+	+LVDS differential data input	
25	GND	Ground	
26	Even_RxIN2-	-LVDS differential data input	
27	Even_RxIN2+	+LVDS differential data input	
28	GND	Ground	
29	Even_RxCLKIN-	-LVDS differential clock input	
30	Even_RxCLKIN+	+LVDS differential clock input	

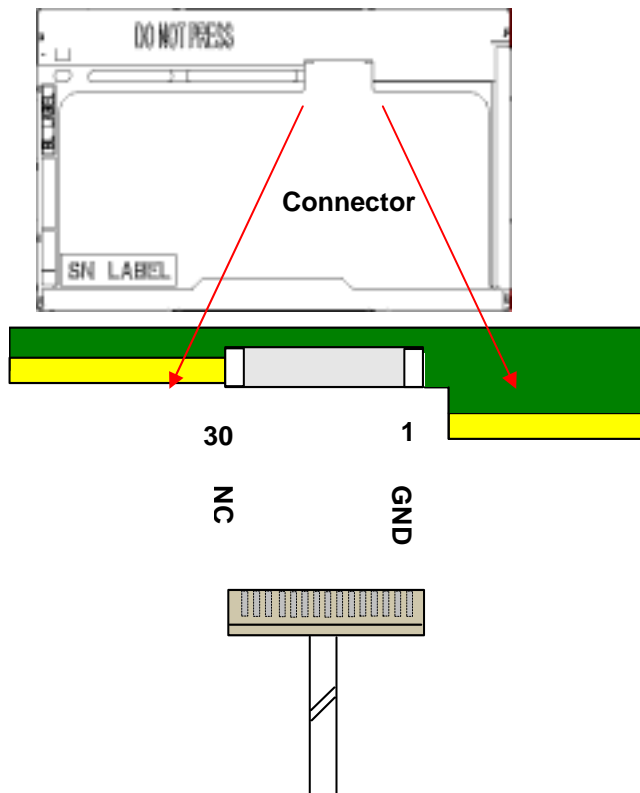


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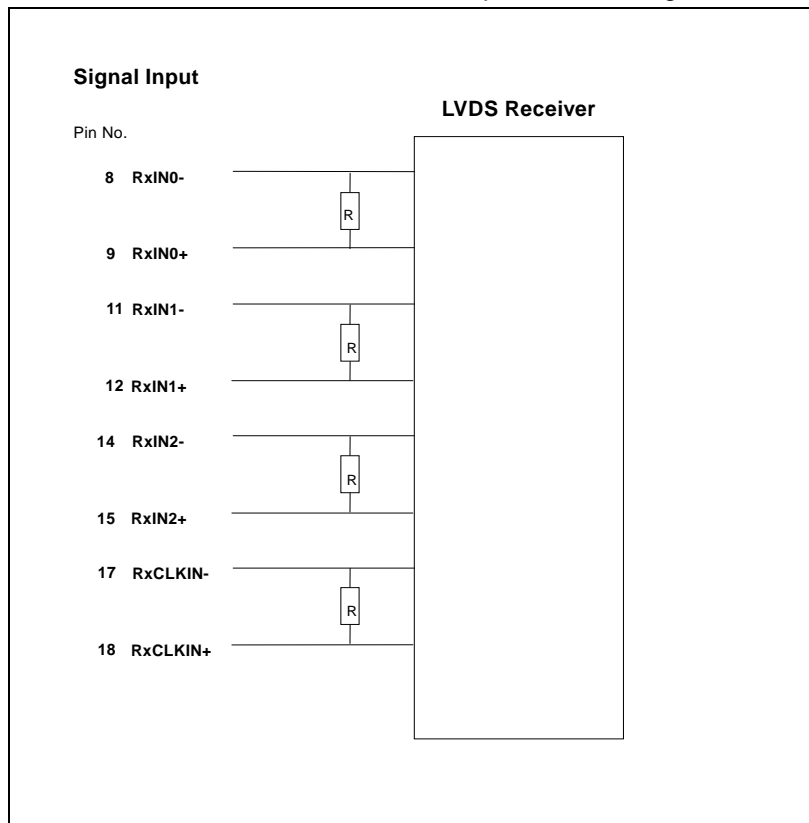
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Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.
internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input





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6.4 Interface Timing

6.4.1 Timing Characteristics

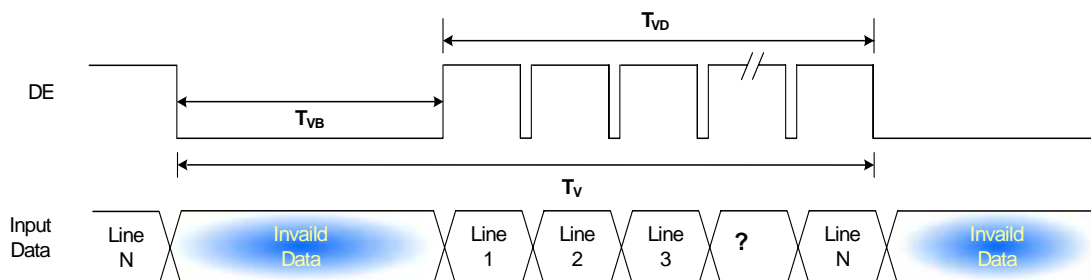
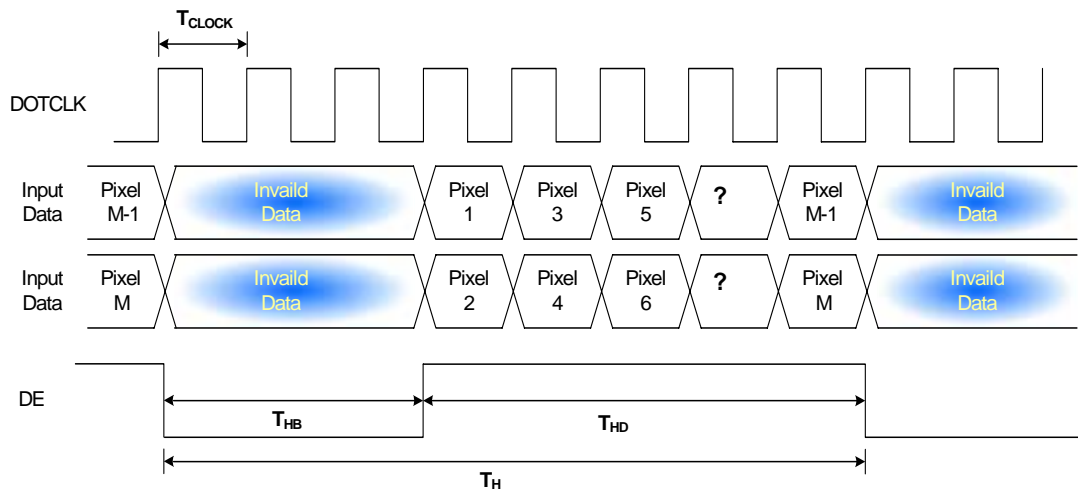
Basically, interface timings should match the 1440x900 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		$1/T_{\text{Clock}}$	-	48.2	-	MHz
Vertical Section	Period	T_V	904	912	2048	T_{Line}
	Active	T_{VD}	900	900	900	
	Blanking	T_{VB}	4	12	-	
Horizontal Section	Period	T_H	760	880	1024	T_{Clock}
	Active	T_{HD}	720	720	720	
	Blanking	T_{HB}	40	160	-	

Note : DE mode only

6.4.2 Timing diagram

Input Timing Definition





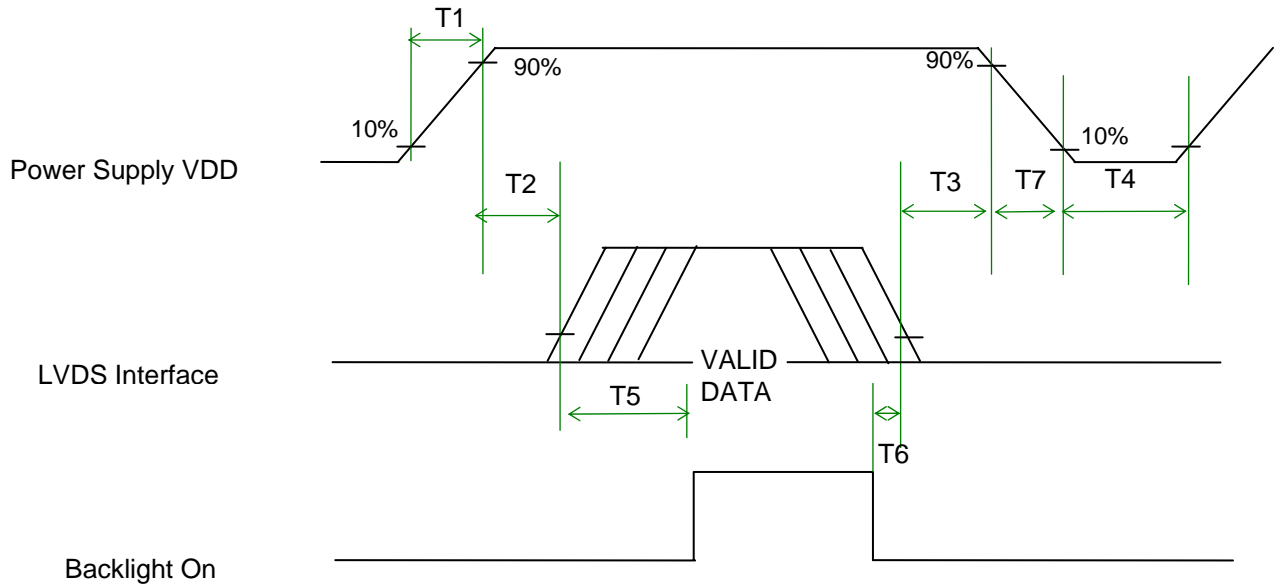
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6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	200	-	-	(ms)
T5	200	-	-	(ms)
T6	0	-	-	(ms)
T7	0	-	10	(ms)



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7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SL-HF10 or compatible
Mating Housing/Part Number	FI-X30H or compatible

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Pink	Lamp High Voltage
2	White	Lamp Low Voltage



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8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 2.16G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 240 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side



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9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	40 /90%,300Hr	
High Temperature Operation	60 /Dry,300Hr	
Low Temperature Operation	0 ,300Hr	
On/Off Test	25 , ON/30 sec. OFF/30sec., 10,000 cycles)	
Hot Storage	60 /35% RH ,250 hours	
Cold Storage	-20 /50% RH ,250 hours	
Thermal Shock Test	-20 /30 min ,60 /30 min 100cycles	
Hot Start Test	50 /1 Hr min. power on/off per 5 minutes, 5 times	
Cold Start Test	0 /1 Hr min. power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	240G, 2ms, Half-sine wave	
Vibration Test (Non-Operating)	Random vibration, 2.16 G zero-to-peak, 10 to 500 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact : $\pm 8\text{KV}$ / operation Air : $\pm 15\text{KV}$ / operation	Note 1
Room temperature Test	25 , 2000hours, Operating with loop pattern	

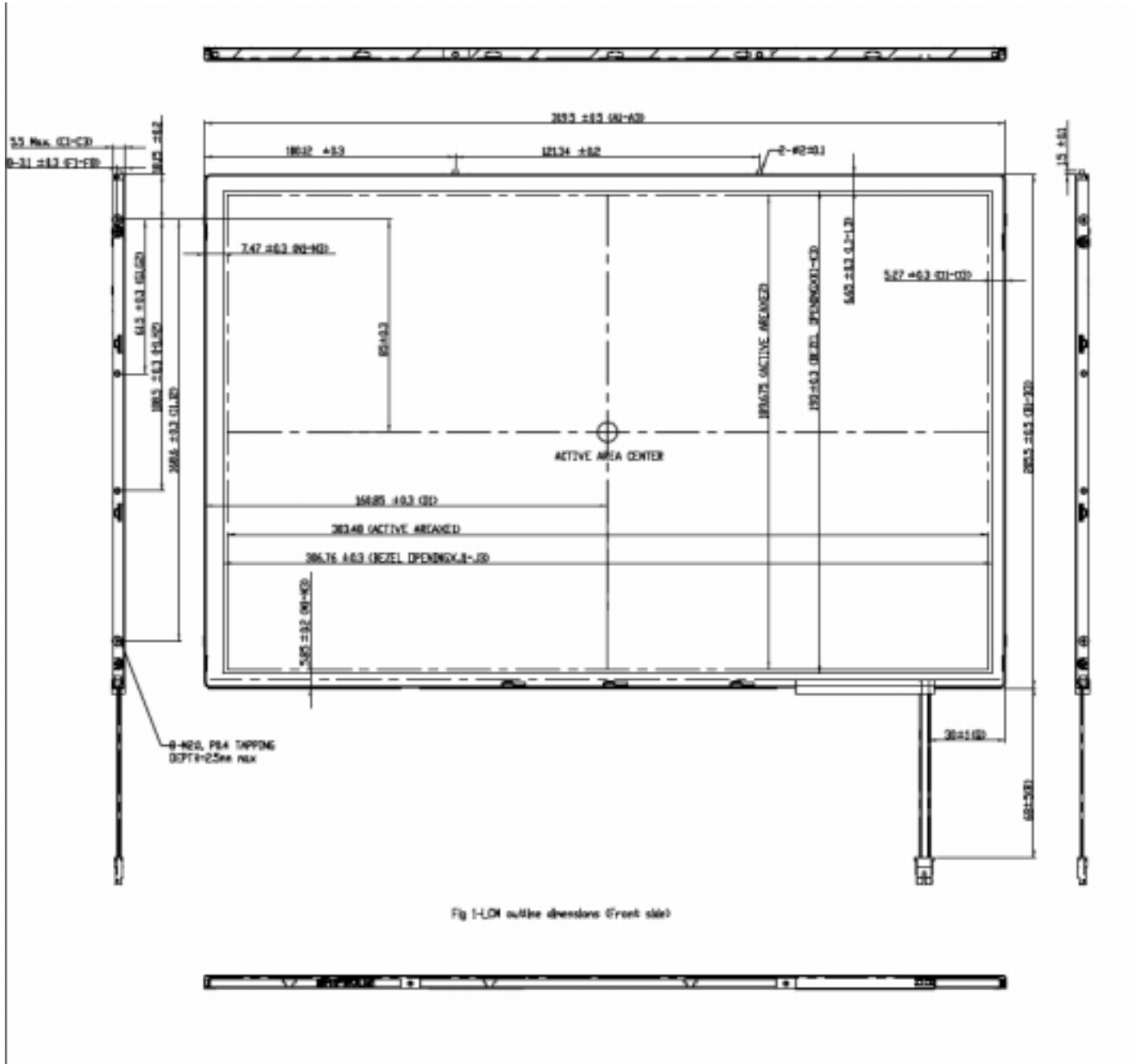
Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Note2: CCFL Life time: 10,000 hours minimum under normal module usage.

Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

10. Mechanical Characteristics

10.1 LCM Outline Dimension





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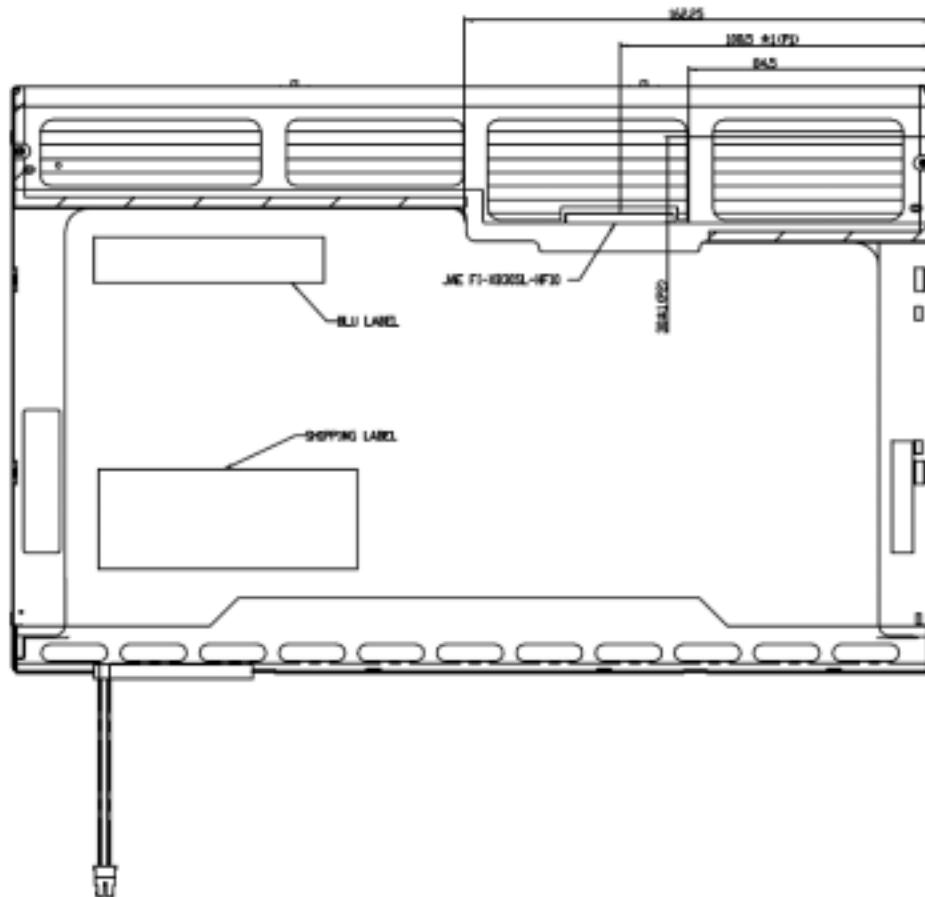


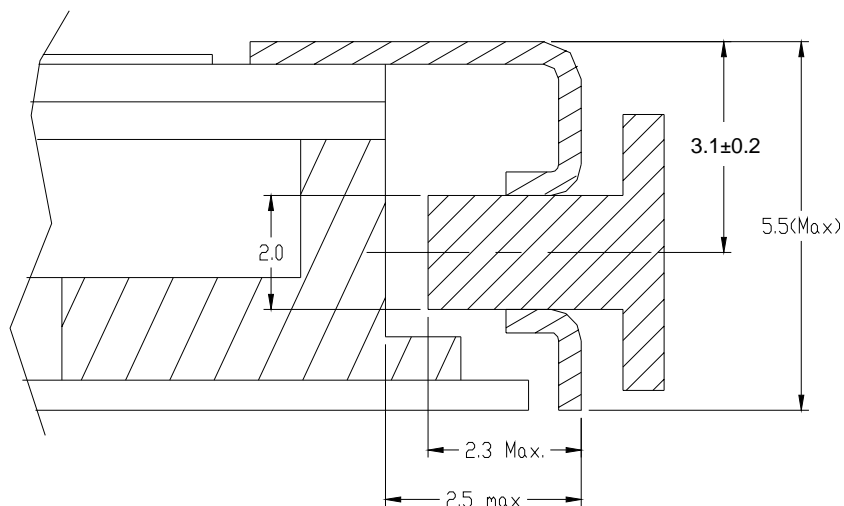
Fig. 2-LDI outline dimensions (Back side)

10.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface = 2.5 mm (See drawing)

Screw hole center location, from front surface = 3.1 ± 0.2 mm (See drawing)

Screw Torque: Maximum 2.5 kgf-cm






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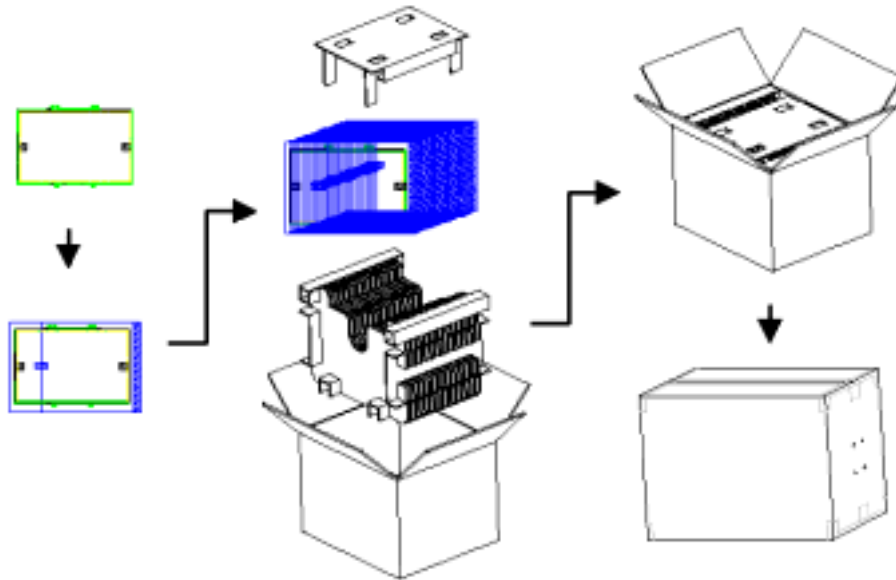
11. Shipping and Package

11.1 Shipping Label Format

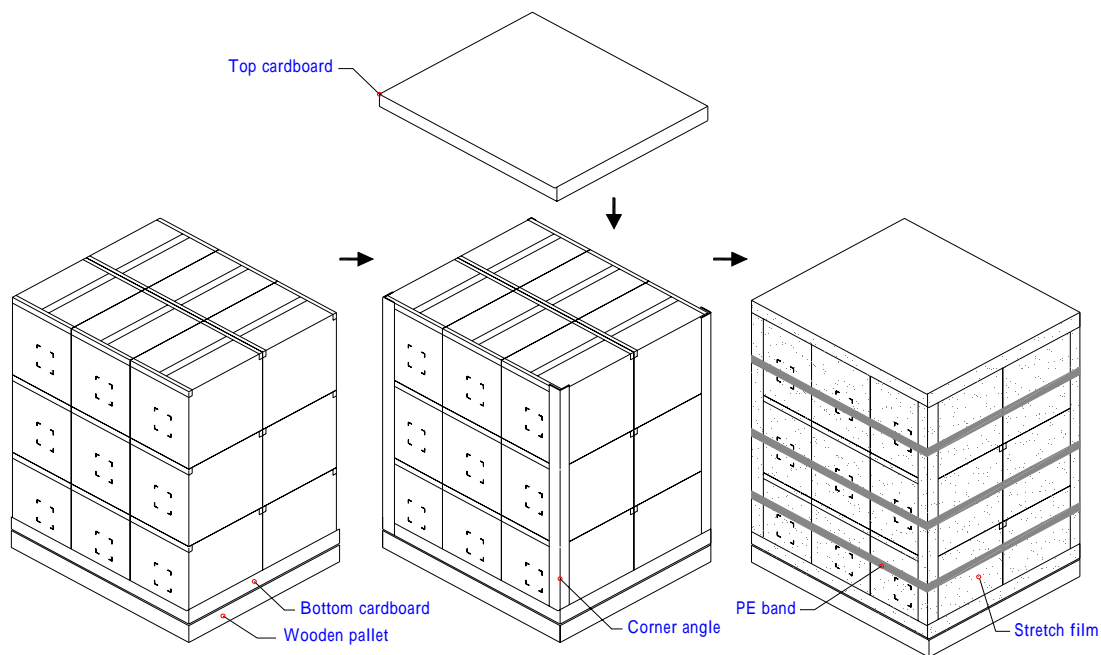
 *XXXXXXXXXXXX-XXXX*	Manufactured 05/52 Model No: B141PW01 AU Optronics MADE IN TAIWAN (S01) H/W: 3A F/W:1	V.4 3AXXG	C  US E204356	 RoHS
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11.2. Carton package

The outside dimension of carton is 455 (L)mm x 388 (W)mm x 355 (H)mm



11.3 Shipping package of palletizing sequence



Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)



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12. Appendix: EDID description

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	47	01000111	71
0B	hex, LSB first	14	00010100	20
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	01	00000001	1
11	Year of manufacture	10	00010000	16
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	03	00000011	3
14	Video input def. (<i>digital I/P, non-TMDS, CRGB</i>)	80	10000000	128
15	Max H image size (<i>rounded to cm</i>)	1E	00011110	30
16	Max V image size (<i>rounded to cm</i>)	13	00010011	19
17	Display Gamma (<i>=(gamma*100)-100</i>)	78	01111000	120
18	Feature support (<i>no DPMS, Active OFF, RGB, tmg Blk#1</i>)	0A	00001010	10
19	Red/green low bits (Lower 2:2:2 bits)	87	10000111	135
1A	Blue/white low bits (Lower 2:2:2 bits)	F5	11110101	245
1B	Red x (Upper 8 bits)	94	10010100	148
1C	Red y/ highER 8 bits	57	01010111	87
1D	Green x	4F	01001111	79
1E	Green y	8C	10001100	140
1F	Blue x	27	00100111	39
20	Blue y	27	00100111	39
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1



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28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	9E	10011110	158
37	Pixel Clock/10000 USB	25	00100101	37
38	Horz active Lower 8bits	A0	10100000	160
39	Horz blanking Lower 8bits	40	01000000	64
3A	HorzAct:HorzBlnk Upper 4:4 bits	51	01010001	81
3B	Vertical Active Lower 8bits	84	10000100	132
3C	Vertical Blanking Lower 8bits	0C	00001100	12
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	00110000	48
3E	HorzSync. Offset	40	01000000	64
3F	HorzSync.Width	20	00100000	32
40	VertSync.Offset : VertSync.Width	33	00110011	51
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0
42	Horizontal Image Size Lower 8bits	2F	00101111	47
43	Vertical Image Size Lower 8bits	BD	10111101	189
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16
45	Horizontal Border <i>(zero for internal LCD)</i>	00	00000000	0
46	Vertical Border <i>(zero for internal LCD)</i>	00	00000000	0
47	Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i>	18	00011000	24
48	Detailed timing/monitor	00	00000000	0
49	descriptor #2	00	00000000	0
4A		00	00000000	0
4B		0F	00001111	15
4C		00	00000000	0
4D		00	00000000	0
4E		00	00000000	0
4F		00	00000000	0
50		00	00000000	0
51		00	00000000	0
52		00	00000000	0
53		00	00000000	0



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54		00	00000000	0
55		00	00000000	0
56		00	00000000	0
57		00	00000000	0
58		00	00000000	0
59		20	00100000	32
5A	Detailed timing/monitor	00	00000000	0
5B	descriptor #3	00	00000000	0
5C		00	00000000	0
5D		FE	11111110	254
5E		00	00000000	0
5F	Manufacture	41	01000001	65
60	Manufacture	55	01010101	85
61	Manufacture	4F	01001111	79
62		0A	00001010	10
63		20	00100000	32
64		20	00100000	32
65		20	00100000	32
66		20	00100000	32
67		20	00100000	32
68		20	00100000	32
69		20	00100000	32
6A		20	00100000	32
6B		20	00100000	32
6C	Detailed timing/monitor	00	00000000	0
6D	descriptor #4	00	00000000	0
6E		00	00000000	0
6F		FE	11111110	254
70		00	00000000	0
71	Manufacture P/N	42	01000010	66
72	Manufacture P/N	31	00110001	49
73	Manufacture P/N	34	00110100	52
74	Manufacture P/N	31	00110001	49
75	Manufacture P/N	50	01010000	80
76	Manufacture P/N	57	01010111	87
77	Manufacture P/N	30	00110000	48
78	Manufacture P/N	31	00110001	49
79	Manufacture P/N	20	00100000	32
7A	Manufacture P/N	56	01010110	86
7B	Manufacture P/N	34	00110100	52
7C		20	00100000	32
7D		0A	00001010	10
7E	Extension Flag	00	00000000	0
7F	Checksum	21	00100001	33