(V) Preliminary Specifications
( ) Final Specifications

Module	**10.1" WQXGA 16:10 Color TFT-LCD With LED Backlight design**
Model Name	B101QAN01.0 (H/W:0A)
Note ( )	***LED Backlight without driving circuit design***

Customer **Date**	**Approved by** **Date**
	Marcus Yen 9/3/2015
Checked & Approved by **Date**	**Prepared by** **Date**
	Th lee 9/3/2015
Note: This Specification is subject to change without notice.	**MDBU Marketing Division AU Optronics corporation**

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2015/09/03	All	First Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B101QAN01.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 SD, 1600(H) x2560(V) screen and RGB 8-bits data driver without LED backlight driving circuit. All input signals are MIPI interface compatible.

B101QAN01.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

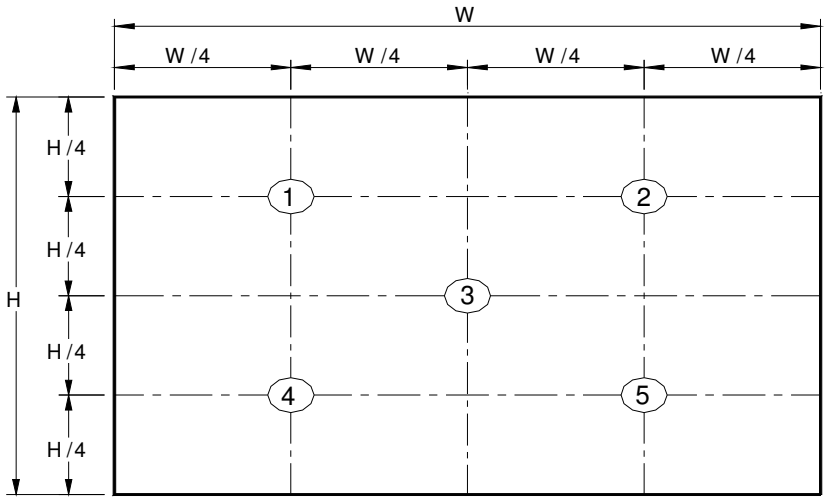
Items	Unit	Specifications			
Screen Diagonal	[mm]	255.40			
Active Area	[mm]	135.36x216.576			
Pixels H x V		1600x3(RGB) x 2560			
Pixel Pitch	[mm]	0.0846x 0.0846			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black (AHVA mode)			
White Luminance	[cd/m^2]	400 typ. @center 340 min. @center			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		800:1 typ., 600:1 min.			
Response Time	[ms]	25 Typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	(+1.8V, +5.6V, -5.6V)			
Power Consumption	[Watt]	Logic power 0.5 max BLU power 2.2 max (w/o LED Driver)			
Weight	[Grams]	120 max.			
Physical Size **Include bracket**	[mm]		Min.	Typ.	Max.
		Length	227.84	228.04	228.24
		Width	142.76	142.96	143.16
		Thickness w/o FPCa w/ FPCa	-	-	 2.20 3.90
Electrical Interface		8 channel MIPI			
Glass Thickness	[mm]	0.2/0.2			
Surface Treatment		Glare			
Support Color		RGB 8-bit			
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

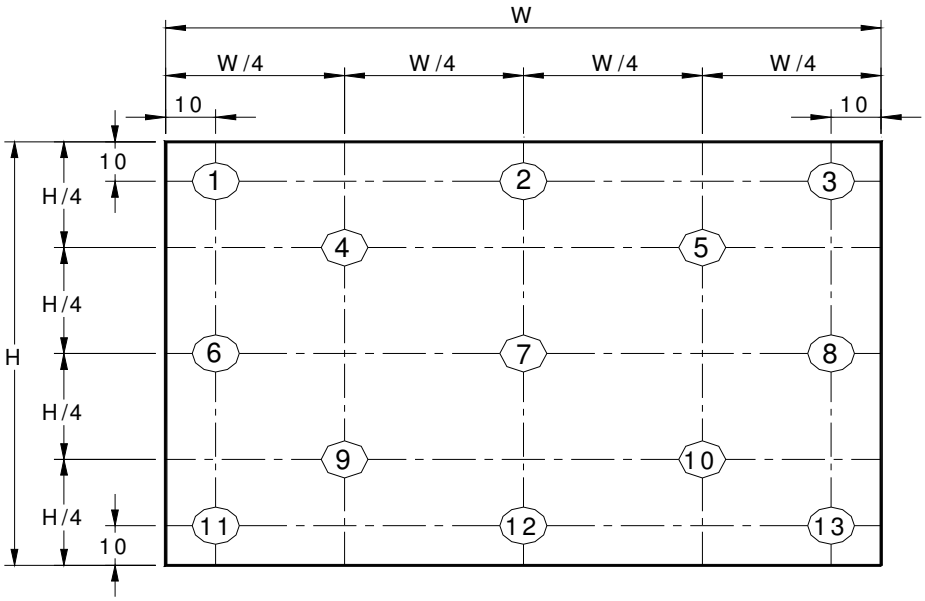
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=20mA			Center	340	400	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10 (Left)	80	85	-	degree	4, 9
		θ_L		80	85	-		
		ϕ_H	Vertical (Upper) CR = 10 (Lower)	80	85	-		
		ϕ_L		80	85	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.6		2, 3, 4
Contrast Ratio		CR		600	800			4, 6
Cross talk		%		-	-	4		4, 7
Response Time		T_{RT}	Rising + Falling	-	25	35	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	TBD	TBD	TBD		4
		Ry		TBD	TBD	TBD		
	Green	Gx		TBD	TBD	TBD		
		Gy		TBD	TBD	TBD		
	Blue	Bx		TBD	TBD	TBD		
		By		TBD	TBD	TBD		
	White	Wx		0.270	0.300	0.330		
		Wy		0.290	0.320	0.350		
NTSC		%		-	70	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



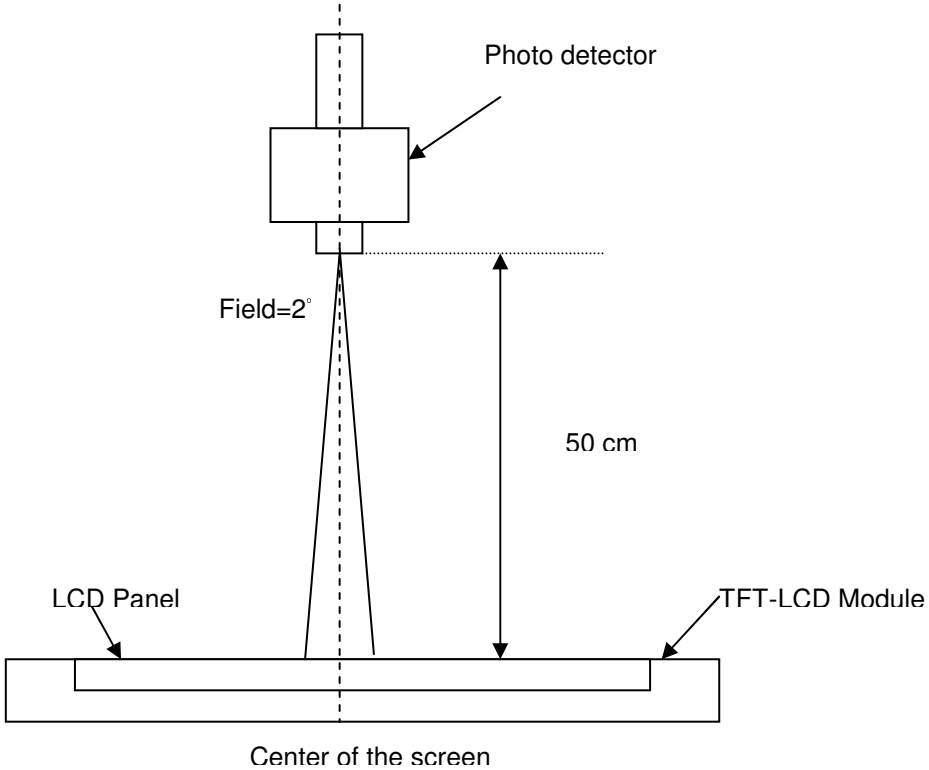
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, measurement should be executed in the center of screen unless otherwise noted.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at center points

center points is corresponding to the luminance of the point 3 at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

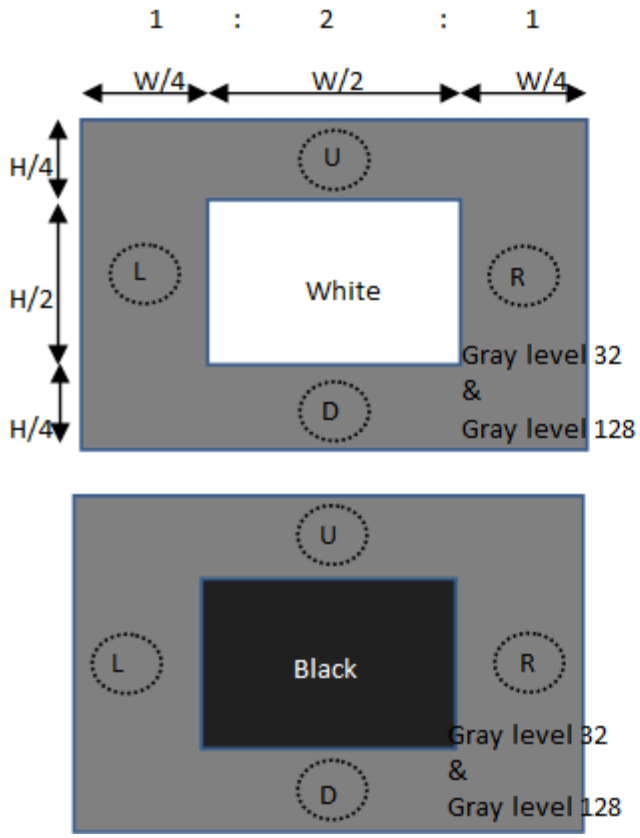
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$

Where

Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)

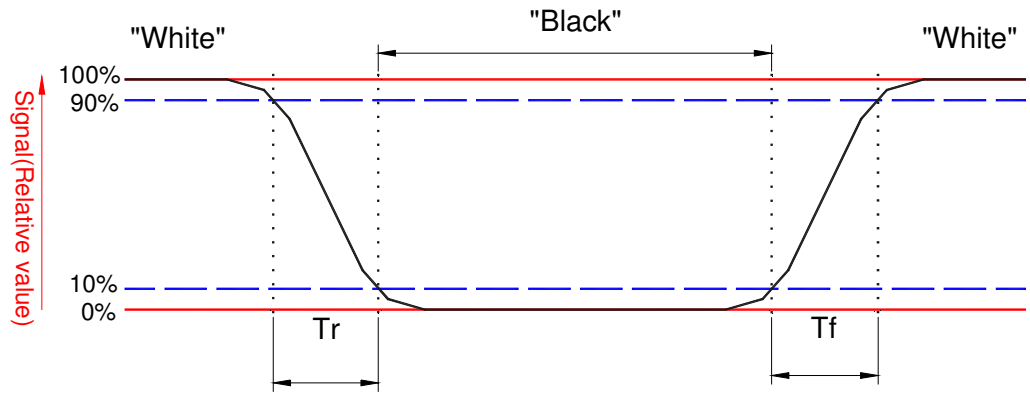


$$Cross\ talk = \frac{Black_{U,D,R,L} - Gray_{U,D,R,L}}{Black_{U,D,R,L}}$$

$$Cross\ talk = \frac{White_{U,D,R,L} - Gray_{U,D,R,L}}{White_{U,D,R,L}}$$

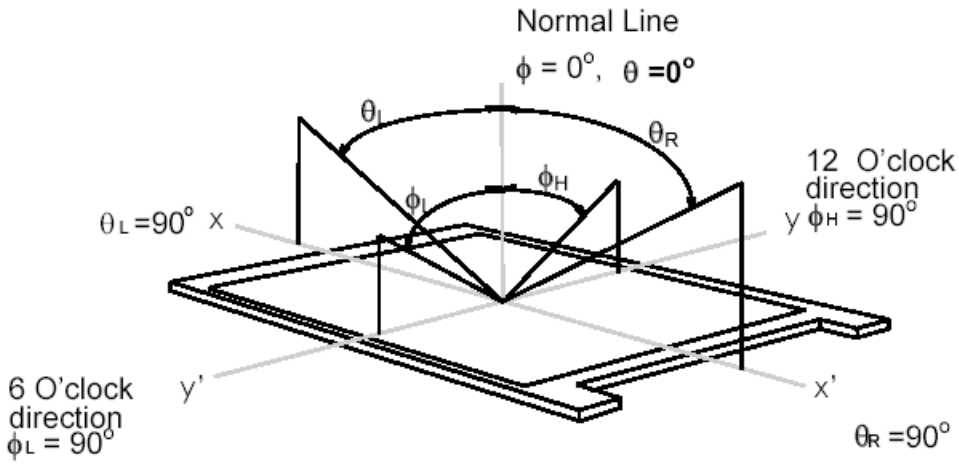
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time is interval between the 10% and 90% of amplitudes. Refer to figure as below.

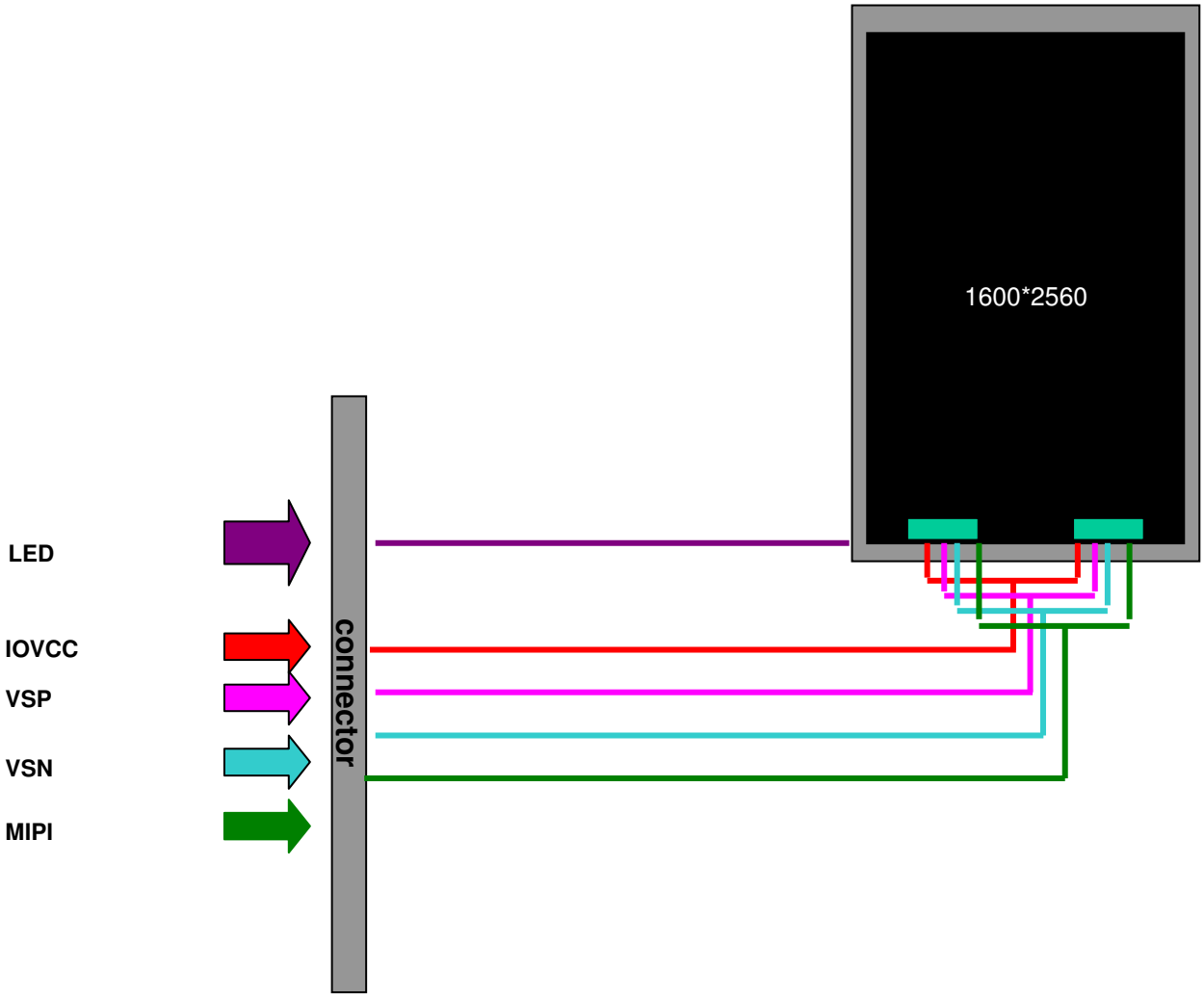


Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.


Normal Line
ϕ = 0°, θ =0°
θL
θR
ϕL
ϕH
θL =90° X
12 O'clock direction
y ϕH = 90°
6 O'clock direction
ϕL = 90°
y'
x'
θR =90°

3. Functional Block Diagram



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDDIN	-0.3	+3.3	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP			[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST			[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Parameter		Symbol	Values			Units	Notes
			Min	Typ	Max		
LCD Input Analog Voltage		IOVCC	1.7	1.8	1.9	V	
LCD Input Analog Voltage		VSP	5.3	5.6	5.9	V	
LCD Input Analog Voltage		VSN	-5.9	-5.6	-5.3	V	
“H” Level Input Voltage		VIH	0.7 IOVCC		IOVCC	V	Applicable Pin： LCD_RST
“L” Level Input Voltage		VIL	0		0.3 IOVCC	V	Applicable Pin： LCD_RST
“H” Level Output Voltage		VOH	0.8 IOVCC		IOVCC	V	Applicable Pin：PWM output, TE
“L” Level Output Voltage		VOL	0		0.2 IOVCC	V	Applicable Pin：PWM output, TE
Input high level leakage current		I IH			1	μA	For the digital, I/O circuit (Not include thepull-up/down)
Input low level leakage current		PN	-1			uA	
LCD	Normal	PD			500	mW	

5.1.2 Logic Power Consumption

The power specification are measured under 25℃ and frame frenquency under 60Hz

Parameter	Symbol	Values		Units	Notes
		Typ	Max		
Normal Mode	IIOVCC		45	mA	White Pattern
	IVSP		30	mA	White Pattern
	IVSN		30	mA	White Pattern
Sleep Mode	IIOVCC		300	uA	
	IVSP		15	uA	
	IVSN		15	uA	

5.1.3 MIPI DC Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
MIPI digital operation current	IMVDDA	MVDDA=1.5V, Data Rate=1000Mbps	-	10		mA
MIPI digital stand-by current	IMVDDAST	MVDDA input current. All input signal are stopped.	-	100	-	uA
MIPI Characteristics for High Speed Receiver						
Single-endedl input low voltage	VILHS		-40	-	-	mV
Single-endedl input high voltage	VIHHS		-	-	460	mV

Common-mode voltage	VCMRXDC		70	-	330	mV
Differential input impedance	ZID		80	100	125	ohm
Differential input high threshold	VIDTH			-	70	mV
Differential input low threshold	VIDTL		-70	-	-	mV
MIPI Characteristics for Low Power Mode						
Pad signal voltage range	VI		-50	-	1350	mV
Ground shift	VGNDSH		-50	-	50	mV
Output low level	VOL		-50		50	mV
Output high level	VOH		1.1	1.2	1.3	V

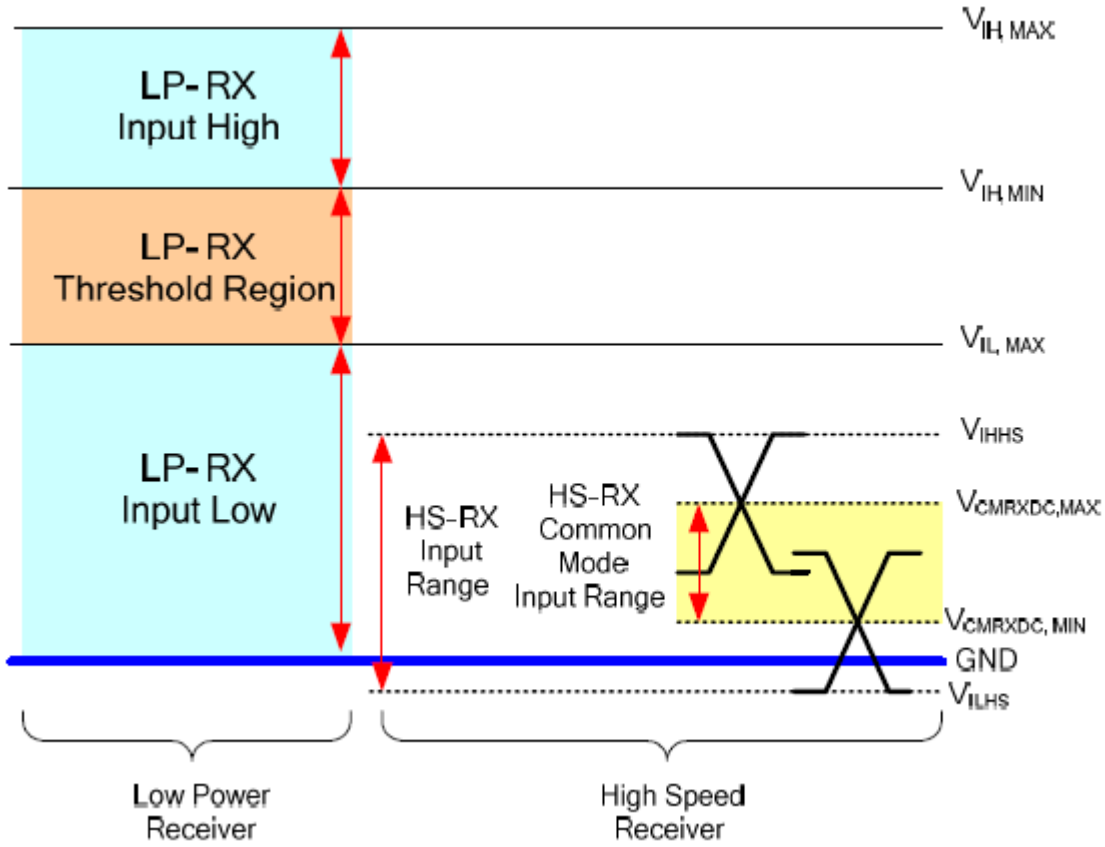


Figure: MIPI DC Diagram

5.1.4 MIPI AC Characteristics

5.1.4.1 LP Transmission

(IOVCC= 1.7V to 1.9V, GND=DGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
15%-85% rise time and fall time	TRLP / TFLP	-	-	25	ns
Pulse width of the LP exclusive-OR clock	TLP-PULSE-TX	50	-	75	ns
Period of the LP exclusive-OR clock	TLP-PER-TX	100	-	150	ns

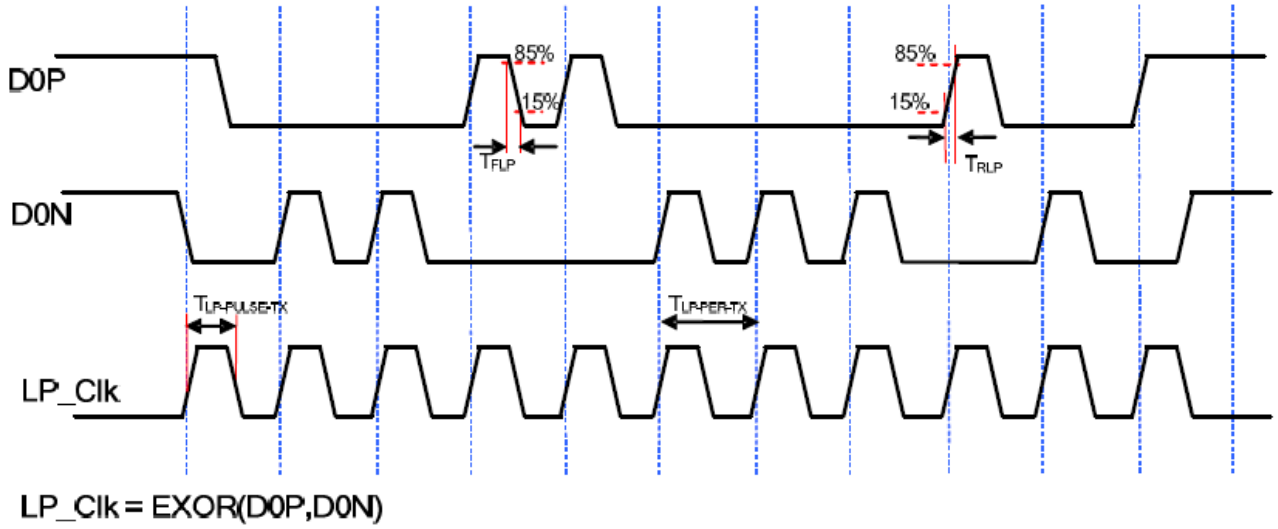


Figure: LP Transmitter Timing Definitions

5.1.4.2 High Speed Transmission

Data-Clock Timing Specifications

(IOVCC= 1.7V to 1.9V, GND=DGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
UI instantaneous	UIINST	1	-	2.5	ns
Data to Clock Setup Time	TSETUP	0.15	-	-	UIINST
Data to Clock Hold Time	THOLD	0.15	-	-	UIINST

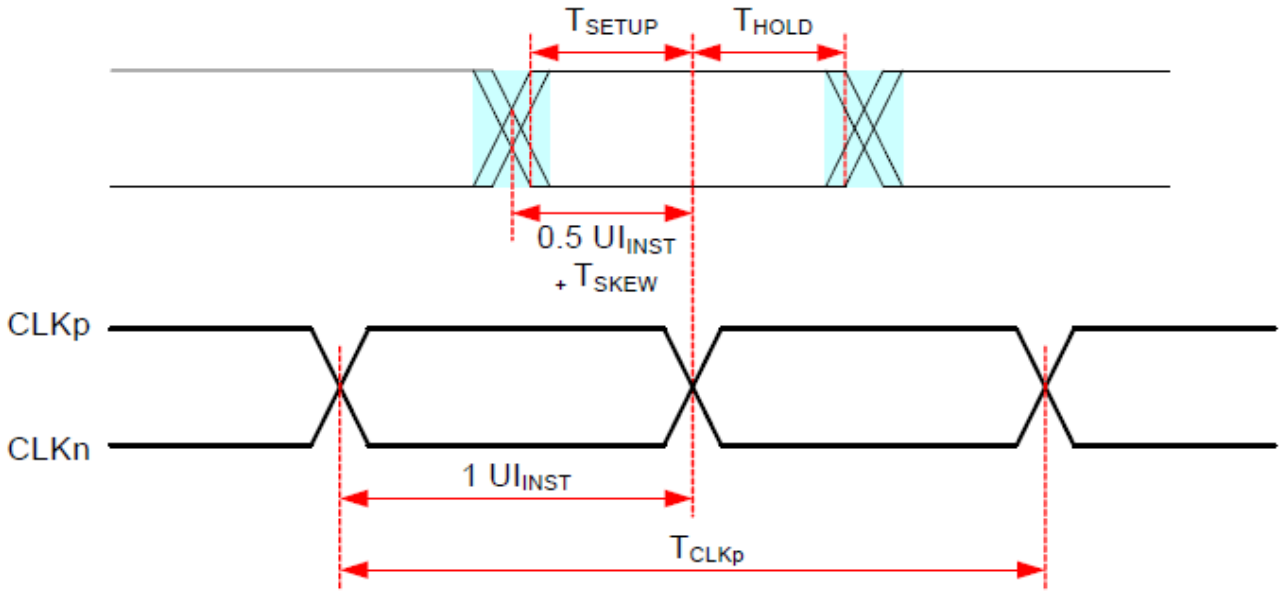


Figure: Data to Clock Timing Definitions

5.1.5 High-Speed Data Transmission in Bursts

(IOVCC= 1.7V to 1.9V, GND=DGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
Time to drive LP-00 to prepare for HS transmission	THS-PREPARE	40+4*UI	-	85+6*UI	ns

Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state	TEOT			105 ns +	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	THS-TERM-EN	-	-	35+4*UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	THS-TRAIL	60+4*UI	-	-	ns
Time-out at RX to ignore transition period of EoT	THS-SKIP	40	-	55+4*UI	ns
Time to drive LP-11 after HS burst	THS-EXIT	100	-	-	ns
Length of any Low-Power state period	TLPX	50	-		ns
Sync sequence period	THS-SYNC	145 ns + 10*UI			ns
Minimum lead HS-0 drive period before the Sync sequence	THS-ZERO	105ns+ 6*UI		60ns+ 4*UI	ns

Note:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

2. UI means Unit Interval, equal to one half HS clock period on the Clock Lane.

3. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

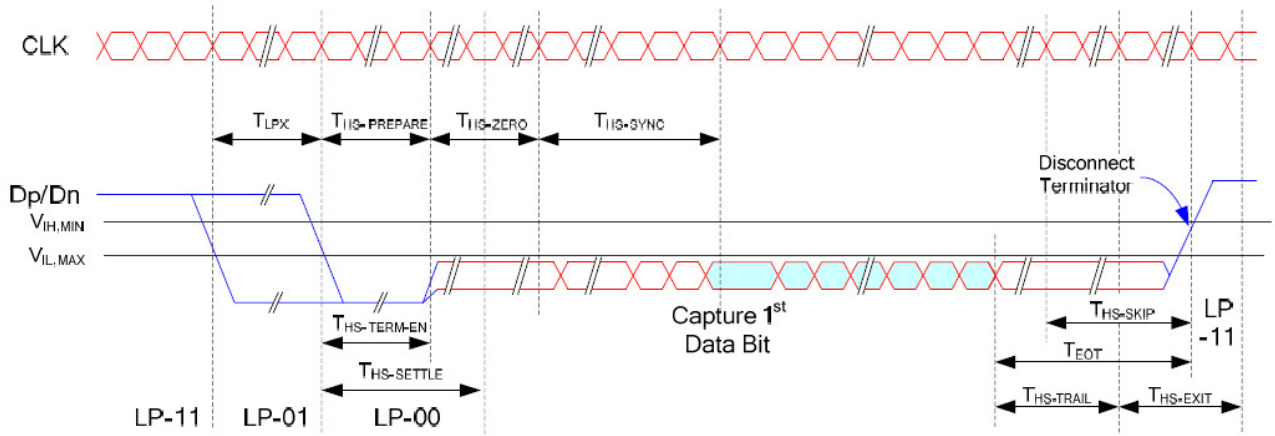


Figure : High-Speed Data Transmission in Bursts

5.1.6 High-Speed Clock Transmission

Switching the Clock Lane Operation Timing Parameters

(IOVCC= 1.7V to 1.9V, GND=DGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	TCLK-POST	60+52*UI	-	-	ns
Detection time that the clock has stopped toggling	TCLK-MISS			60	ns
Time to drive LP-00 to prepare for HS clock transmission	TCLK-PREPARE	38	-	95	ns
Minimum lead HS-0 drive period before starting Clock	TCLK-PREPARE +TCLK-ZERO	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross	THS-TERM-EN	-	-	38	ns

VIL,MAX					
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	TCLK-PRE	8*UI	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	TCLK-TRAIL	60	-	-	ns

Note:

The DSI host processor shall support continuous clock on the Clock Lane for NT chip that require it, so the host processor needs to keep the HS serial clock running.

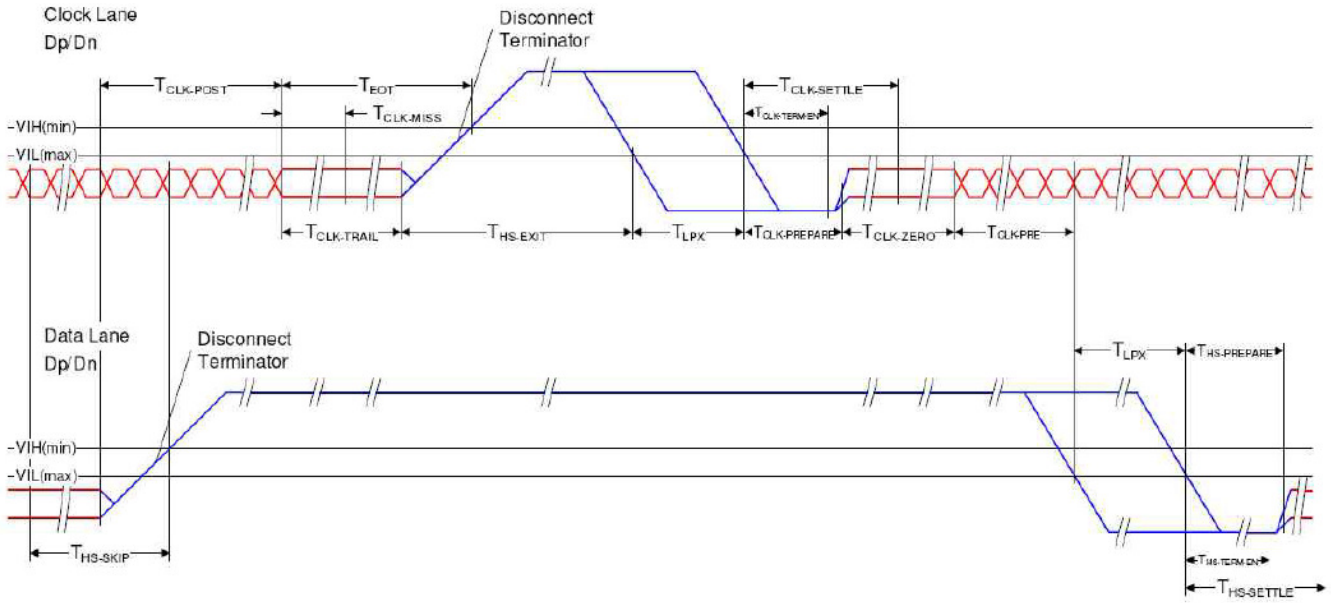


Figure: Switching the Clock Lane between Clock Transmission and Low-Power Mode

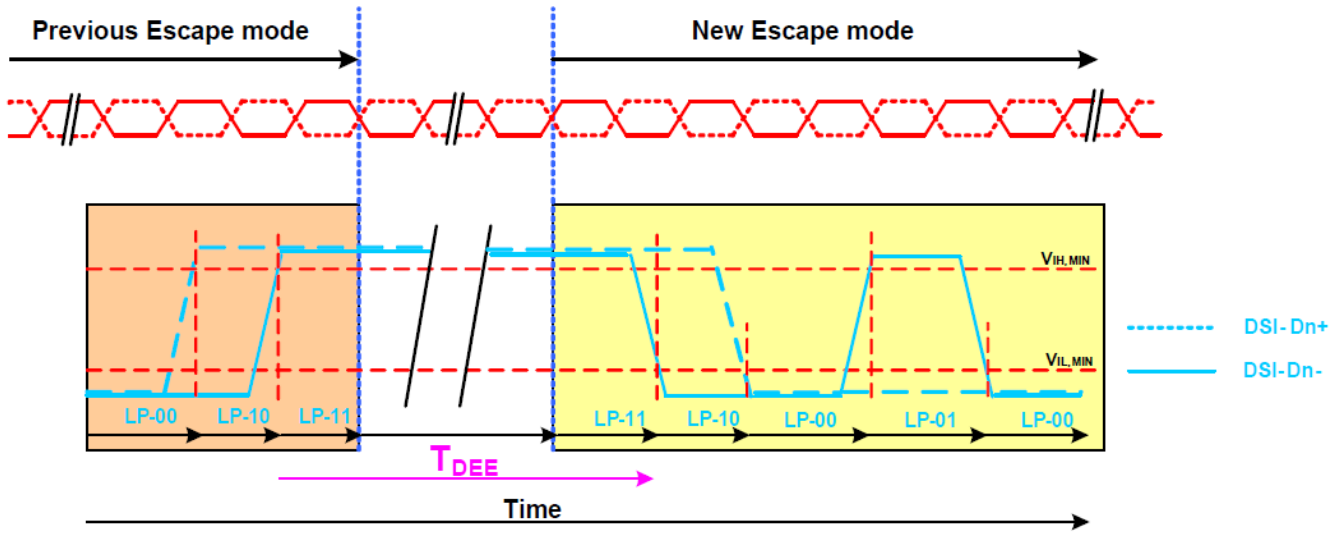
5.1.6 LP11 timing request between data transformation

When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Lowpower mode.

If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode.

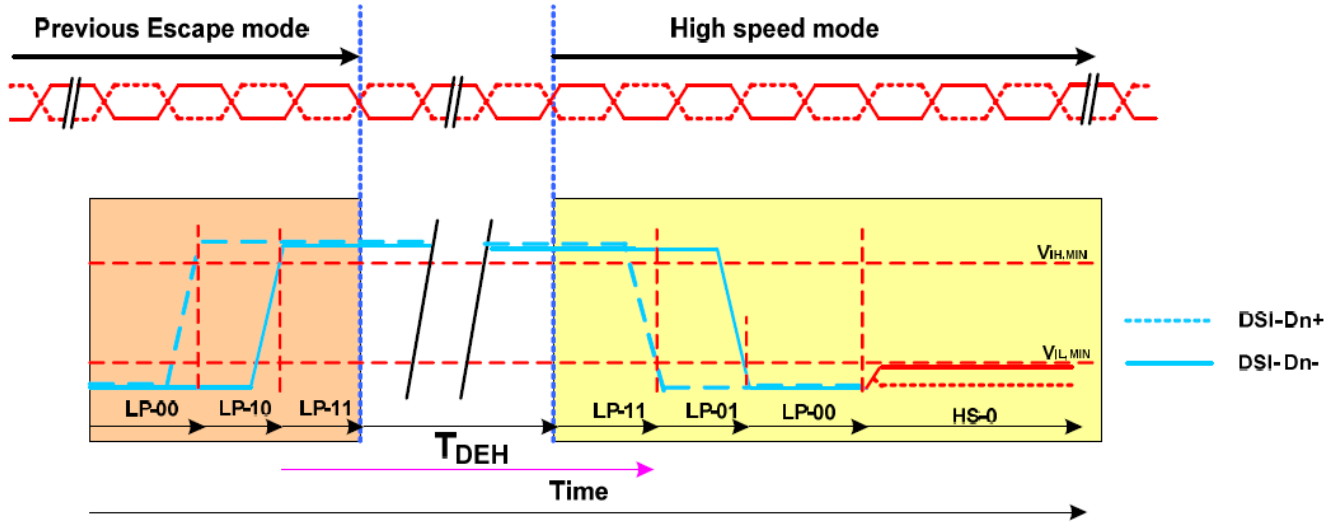
The LP-11 minimum timing is required for RX chip in the following 9 conditions, include of LP - LP, LP - HS, HS - LP, and HS – HS. This rule is suitable for short or long packet between TX and RX data transmission.

(1) Timing between LP - LP command



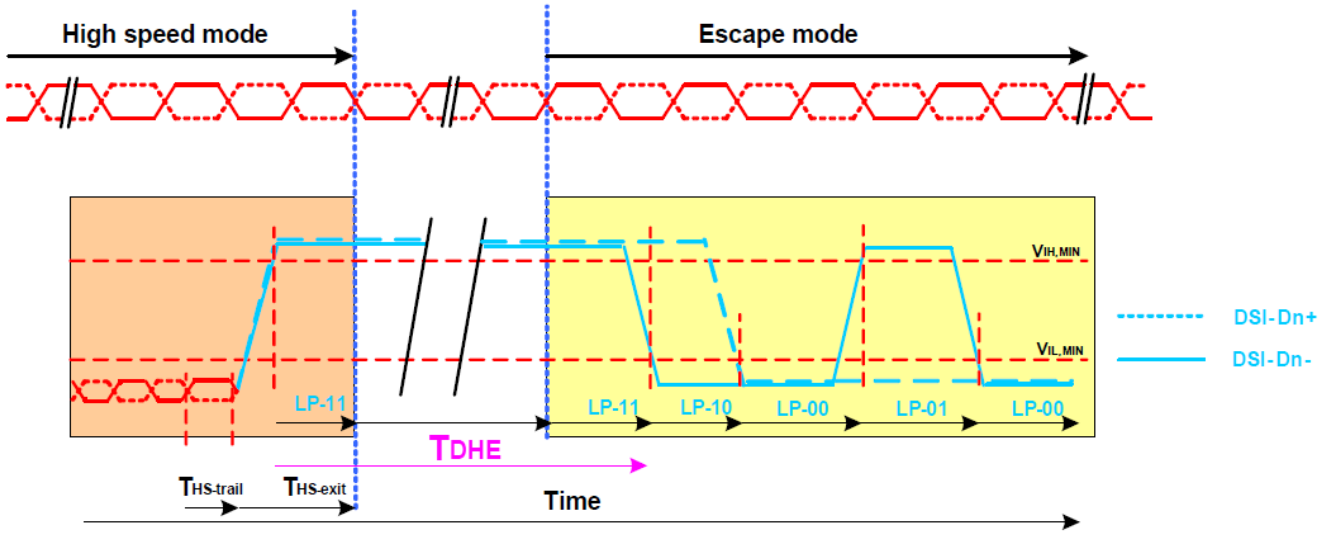
Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the new Escape Mode Entry	TDEE	100			ns

(2)Timing between LP - HS command



Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the Entering High Speed Mode	TDEH	100			ns

(3)Timing between HS - LP command



Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the Escape Mode Entry	TDHE	100			ns

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power (w/o efficiency)	PLED	-	-	2.2	[Watt]	(Ta=25℃)
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃) Note1.
LED Forward Voltage	VF	-	2.9	3.2	[Volt]	(Ta=25℃)
LED Forward Voltage of every LED string	VF-string	-	17.4	.	[Volt]	(Ta=25℃) Note2.
LED Forward Current	IF	-	20	-	[mA]	(Ta=25℃)

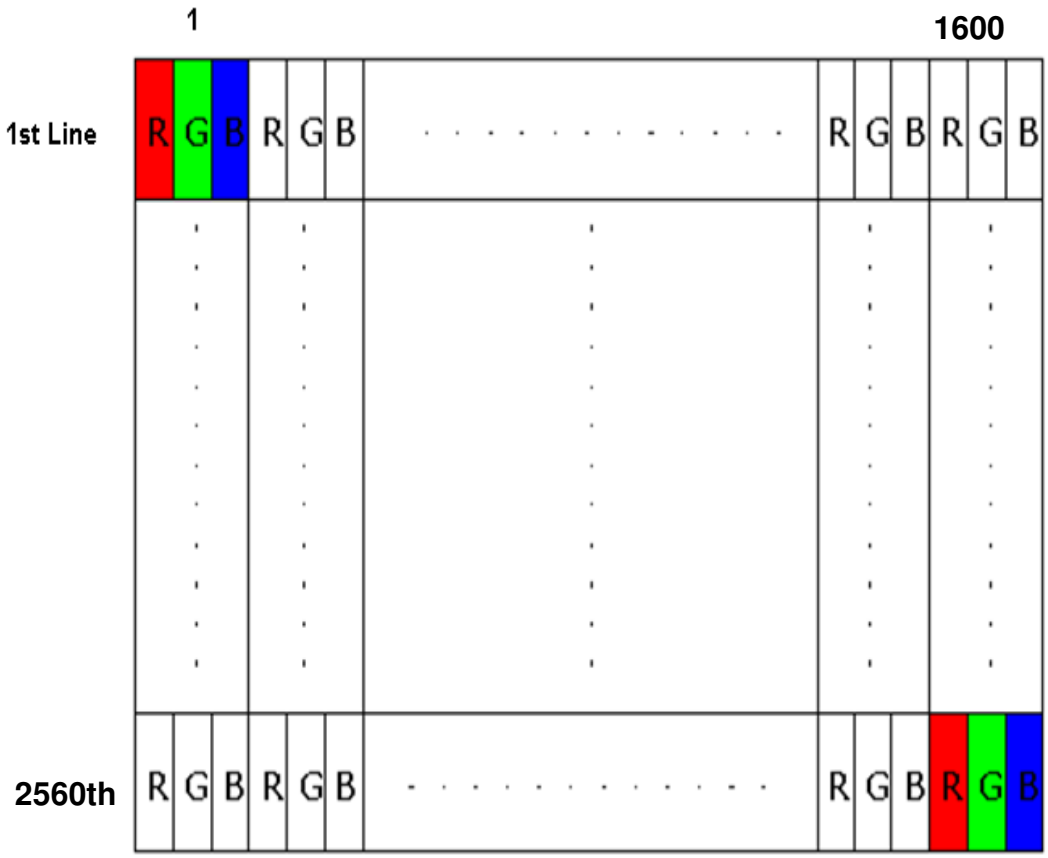
Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution), w/o efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

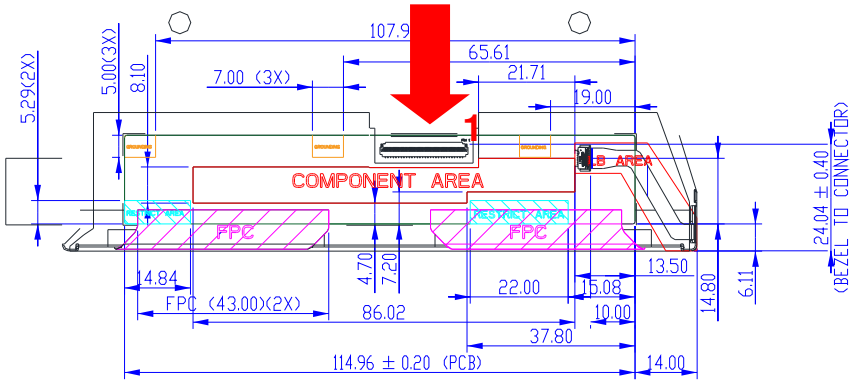
Connector Name / Designation	For Signal Connector
Manufacturer	Hirose
Type / Part Number	FH26W-61S-0.3SHW(60)
Mating Housing/Part Number	FPC

6.2.2 Pin Assignment

MIPI lane is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Symbol	I/O	Description
1	GND		AGND
2	GND		AGND
3	NC		
4	FB6	I	LED-
5	FB5	I	LED-
6	FB4	I	LED-
7	FB3	I	LED-
8	FB2	I	LED-
9	FB1	I	LED-
10	NC		
11	VLED2	I	LED+
12	VLED1	I	LED+
13	NC		
14	VSP	I	+5.6V
15	VSP	I	+5.6V
16	NC		
17	VSN	I	-5.6V
18	VSN	I	-5.6V
19	NC		
20	IOVCC	I	+1.8V
21	IOVCC	I	+1.8V
22	NC		for AUO internal aging
23	LCD_RST	I	Reset +1.8V
24	PWM output	O	+1.8V

25	TE	O	+1.8V
26	ID	O	connect 10k ohm to GND
27	NC		For AUO internal OTP
28	GND		DGND
29	GND		DGND
30	D0PA	I	MIPI input Data pair
31	D0NA	I	MIPI input Data pair
32	GND		DGND
33	D1PA	I	MIPI input Data pair
34	D1NA	I	MIPI input Data pair
35	GND		DGND
36	CLKPA	I	MIPI input CLK pair
37	CLKNA	I	MIPI input CLK pair
38	GND		DGND
39	D2PA	I	MIPI input Data pair
40	D2NA	I	MIPI input Data pair
41	GND		DGND
42	D3PA	I	MIPI input Data pair
43	D3NA	I	MIPI input Data pair
44	GND		DGND
45	D0PB	I	MIPI input Data pair
46	D0NB	I	MIPI input Data pair
47	GND		DGND
48	D1PB	I	MIPI input Data pair
49	D1NB	I	MIPI input Data pair
50	GND		DGND
51	CLKPB	I	MIPI input CLK pair
52	CLKNB	I	MIPI input CLK pair
53	GND		DGND
54	D2PB	I	MIPI input Data pair
55	D2NB	I	MIPI input Data pair
56	GND		DGND
57	D3PB	I	MIPI input Data pair
58	D3NB	I	MIPI input Data pair
59	GND		DGND
60	GND		DGND
61	GND		DGND


107.9
65.61
21.71
19.00
7.00 (3X)
5.00(3X)
8.10
5.29(2X)
1
COMPONENT AREA
FPC
FPC
B AREA
24.04 ± 0.40
(BEZEL TO CONNECTOR)
14.84
FPC (43.00)(2X)
4.70
7.20
22.00
15.08
13.50
14.80
6.11
86.02
10.00
37.80
114.96 ± 0.20 (PCB)
14.00

6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1600x2560 manufacturing guide line timing.

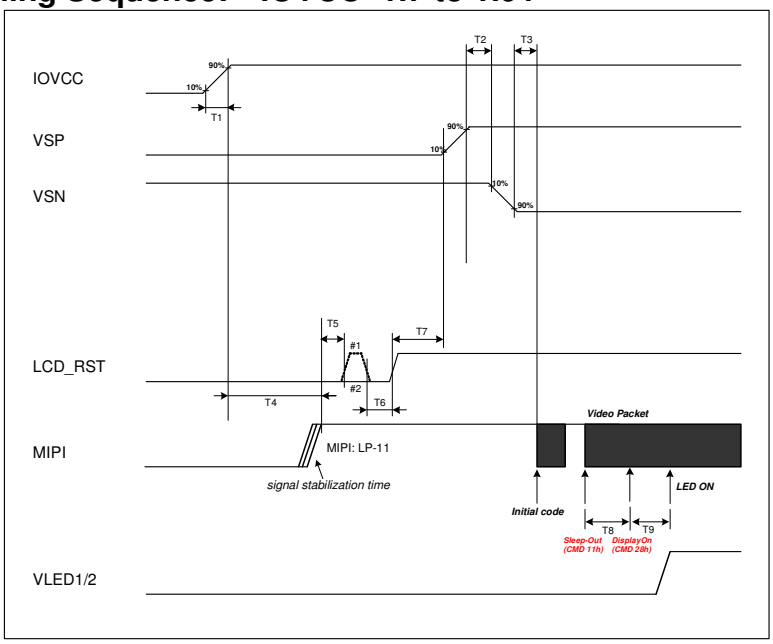
Signal	Item	Symbol	Min.	Typ.	Max.	Unit
	MIPI Data frequency	FDATA		943		MHz
DCLK	Frequency	1/Tc		158		MHz
DE	Vertical Total Time	TV	-	2608	-	TH
	Vertical Active Display Period	TVD	-	2560	-	TH
	Vertical Front Porch Period	TVFP	Note2	16	Note2	TH
	Vsync pulse width	TVPW	Note2	8	Note2	TH
	Vertical Back Porch Period	TVBP	note2	24	Note2	TH
	Horizontal Total Time	TH	-	1008		Tc
	Horizontal Active Display Period	THD	-	800	-	Tc
	Horizontal Front Porch Period	THFP	Note3	120		Tc
	Horizontal pulse width	THPW	-	8	-	Tc
	Horizontal Back Porch Period	THBP	Note3	80		Tc

Note1: Frame rate=60Hz
Note2: Vertical Period are dependent on GOA timing, and don't modify. TVFP+TVPW+TVBP>16
Note3: tHFP = 0.65us (min), tHBP= 0.64us (min)
Note4: Horizontal Period is set by per port
Note5: DCLK=Frame rate*TV*TH.
TV=TVD+TVFP+TVPW+TVBP
TH=THD+THFP+THPW+THBP

6.4 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.

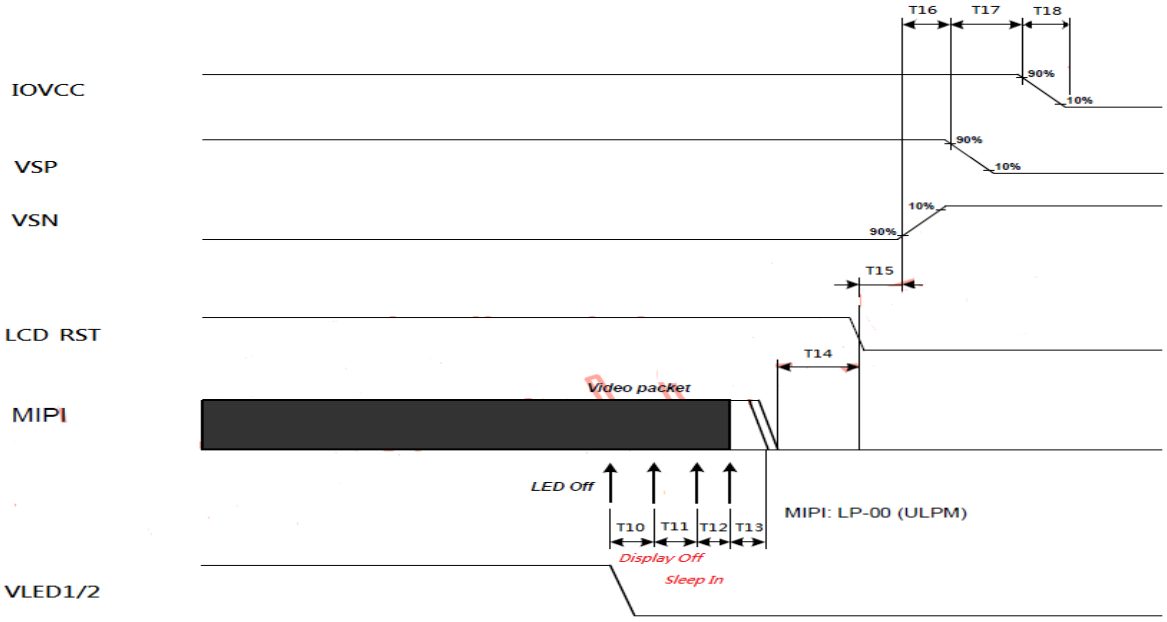
6.4.1 Power on Timing Sequence: IOVCC=1.7 to 1.9V



Note1: LCD_RST signal H to L to H (#1) is better than only L to H(#2)

Power Sequence Timing			
Parameter	Value		Unite
	Min.	Max.	
T1	0.5	2	ms
T2	10	-	ms
T3	0	-	ms
T4	15	-	ms
T5	1	-	ms
T6	10	-	us
T7	20	-	ms
T8	6	-	frame
T9	3	-	frame

6.4.2 Power off Timing Sequence: IOVCC=1.7 to 1.9V

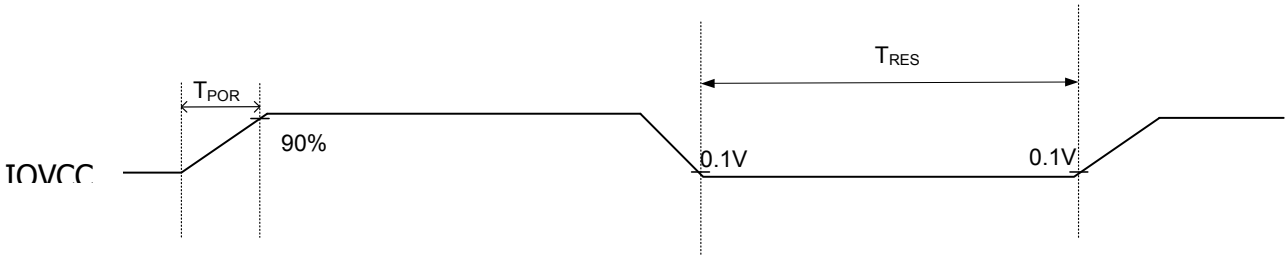


Power Sequence Timing			
Parameter	Value		Unite
	Min.	Max.	
T10	50	-	ms
T11	80	-	ms
T12	100	-	ms
T13	0	-	ms
T14	10	-	ms
T15	1	-	ms
T16	10	-	ms
T17	0	-	ms
T18	-	10	ms

a. IOVCC AC characteristic:

IOVCC= 1.8V, GND=AGND= 0V, TA= -20 to +85°C)

6.4.3 Power reset Timing Sequence: IOVCC=1.7 to 1.9V



Parameter Symbol	Symbol	Min.	Typ.	Max.	Unit	Conditions
IOVCC power source slew time	TPOR	0.5		2	ms	From 0V to 90% IOVCC
IOVCC resettle time	TRES			500	ms	

6.5 Power ON/OFF MIPI comment

6.5.1 Power On Set Table

Step	Register Setting		Operation
	Register	Data	
1	Reset = LOW		
2	Power (IOVCC) ON		
3	15ms or more		
4	MIPI LP-11 status ON		
5	1ms or more		
6	Reset = HIGH		
7	20ms or more		
8	Power (VSP, VSN,) ON		

6.5.2 Power Off Set Table

Step	Register Setting		Operation
	Register	Data	
1	MIPI Video Pixel Stream OFF		
2	MIPI LP-11 Status OFF(LP-00)		
3	10ms or more		
4	Reset = LOW		
5	1ms or more		
6	Power (VSN, VSP, IOVCC) Off VSN → 10ms or more → VSP Off → IOVCC Off		

6.5.3 Display On & Sleep Out Set Table

Step	Data Type	Register Setting		Operation
		Register	Data	
1	39h	F0h	55h,AAh,52h,08h,00h	Switch page0
2	15h	C0h	0Dh	ESD detect signal
3	39h	B8h	03h,06h,00h,00h	Source EQ off
4	39h	FFh	AAh,55h,A5h,80h	Switch cmd3 on
5	15h	6Fh	0Fh	Set index
6	15h	F7h	01h	Set ESD protect command
7	39h	FFh	AAh,55h,A5h,00h	Switch cmd3 off
8	15h	62h	01h	Set ESD protect command
9	15h	55h	02h	CABC Enable STILL MODE
10	15h	53h	24h	PWM signal enable
11	15h	51h	80h	Manually PWM 50%
12	05h	11	-	Sleep Out
13	05h	29	-	Display On
14	MIPI Video Pixel Stream ON			
15	120ms or more			

6.5.4 Display Off & Sleep In Set Table

Step	Data Type	Register Setting		Operation
		Register	Data	
1	0x05	28	-	Display Off
2		20ms or more		
3	0x05	10	-	Sleep In
4		100ms or more		
5		MIPI Video Pixel Stream OFF		

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 200Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: ±X, ±Y, ±Z .1 time for each side

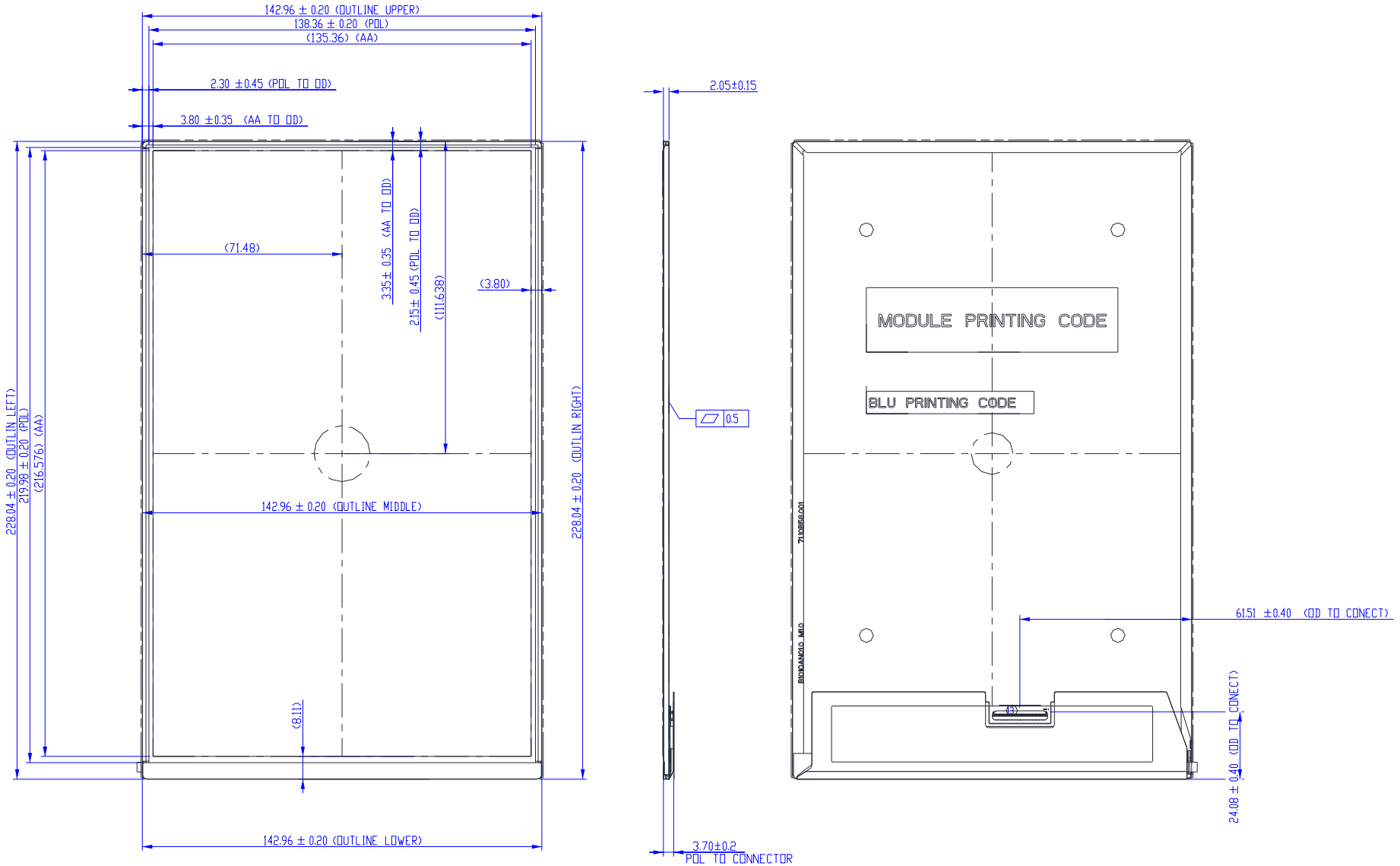
7.3 Reliability Test

Items	Required Condition	Note
High Temperature Storage	Ta= 60℃, 300h	
Low Temperature Storage	Ta= -20℃, 240h	
High Temperature/ High Humidity Storage	Ta= 40℃, 90%RH, 240h	
High Temperature Operation	Ta= 50℃, 240h	
Low Temperature Operation	Ta= 0℃, 240h	
Thermal Shock Test	-20℃(30min)~60℃(30min) , 27 cycle	Non-operation
Flicker	under -30dB	
Image sticking	30mins (5x5 chess board)/L128/1s recovery	
Packing drop test	Drop height 762mm, 1 corner, 3 edges, 6 flats	
ESD	Contact : ±8 KV, Air : ±15 KV, IC and connector excluded	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

8. Mechanical Characteristics

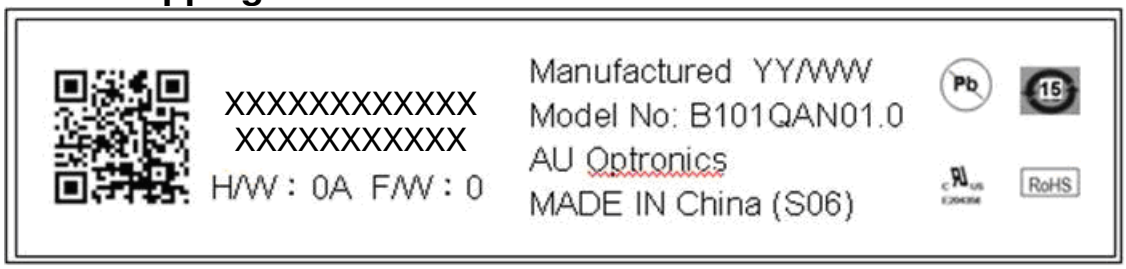
8.1 LCM Outline Dimension



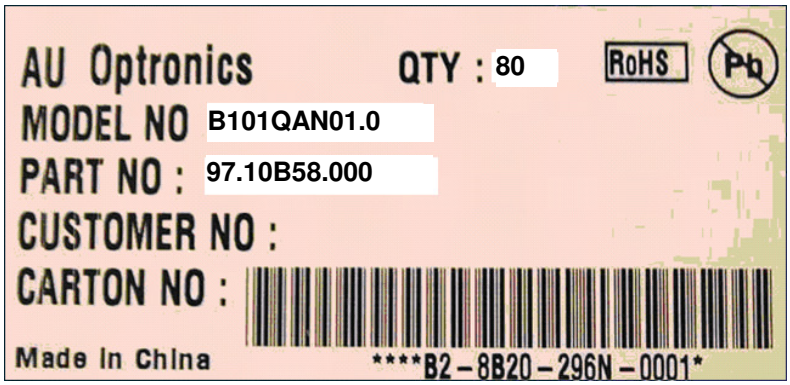
Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

9. Shipping and Package

9.1 Shipping Label Format

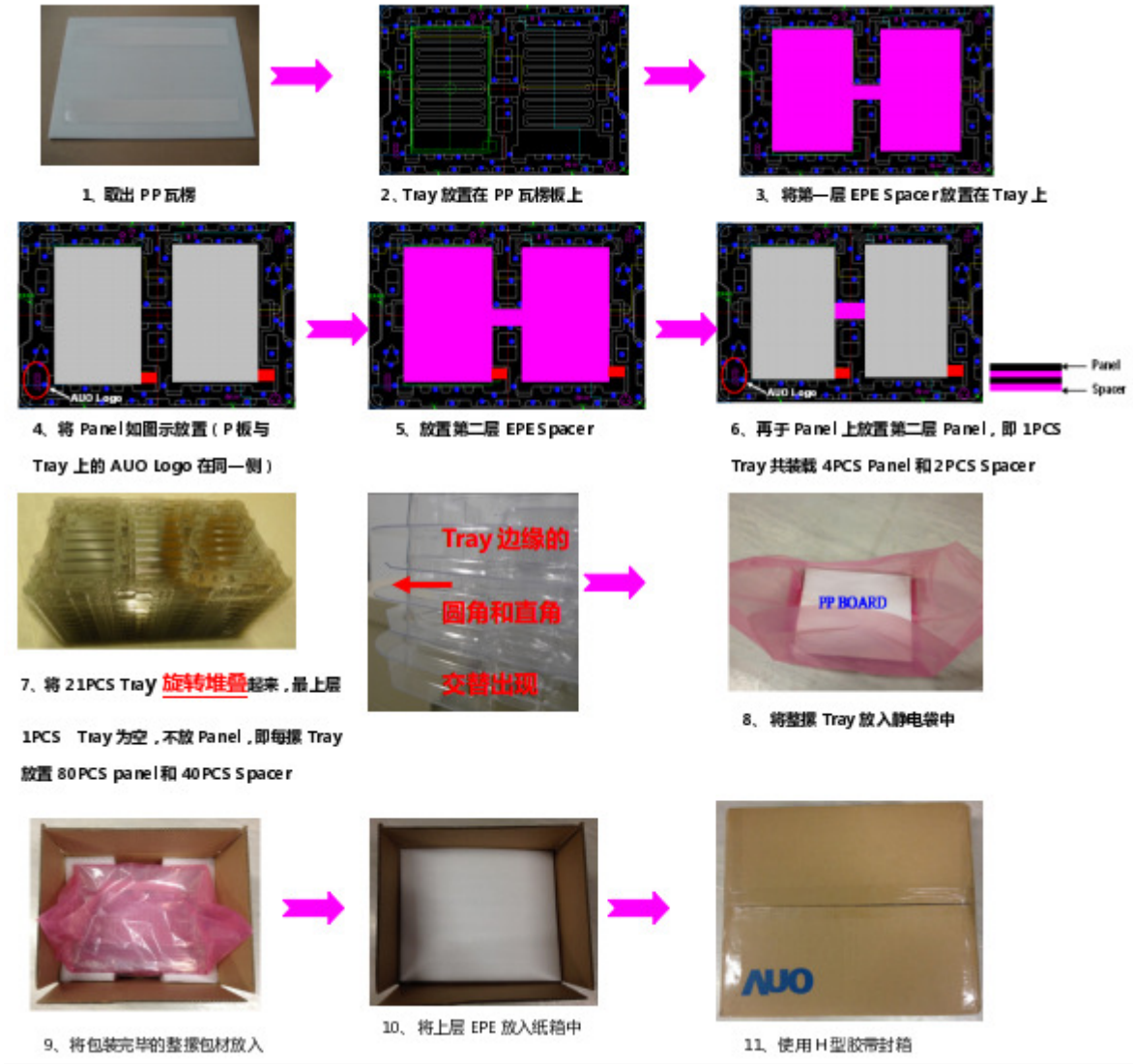


9.2 Carton Label Format



9.3 Carton Package

80PCS/Carton



9.4 Shipping Package of Palletizing Sequence