Doc. Version	**1.7**
Total Pages	**19**
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Product Specification

5.0” COLOR TFT-LCD MODULE

MODEL NAME: A050VN01 V0

<◆>Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

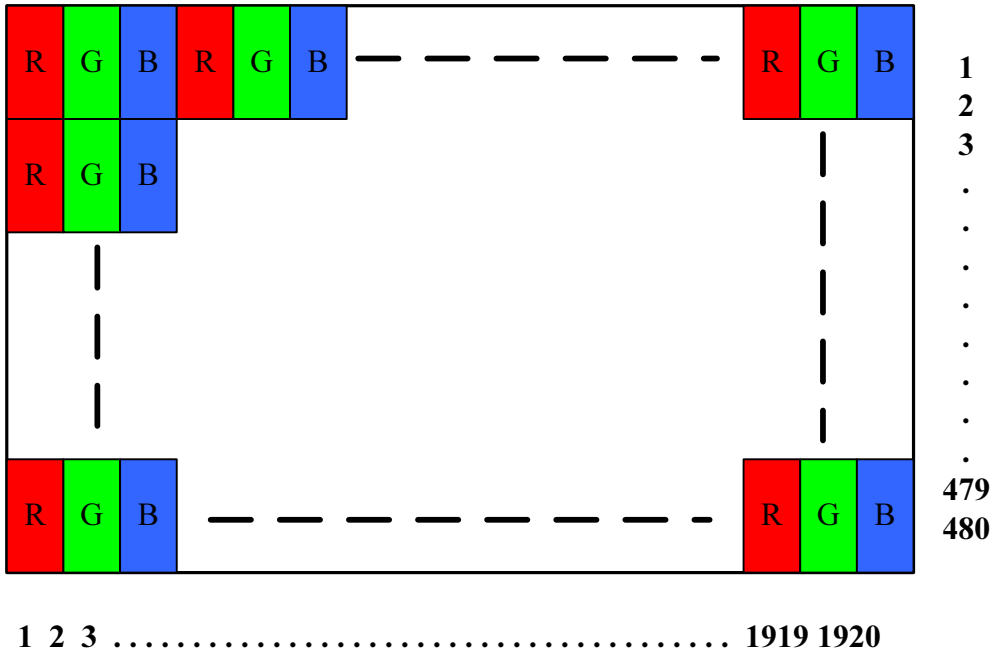
Version	Revise Date	Page	Content
0.0	2006/12/08	---	First draft.
0.1	2006/12/14	---	Update EE part
1.0	2007/05/04	4 9 11 12 13~14 19 20	Update weight Change register setting Update vertical and horizontal timing Update data input timing parameters Update power On/Off and standby On/Off sequence diagrams Update outline drawing Update packing form
1.1	2007/06/25	7 9,10 12 13, 14	Added Dim remark Updated Control register bit settings and definitions Updated PixClk and Data Input Timing Parameters Updated Power On/Off and Standby On/Off Sequence diagrams
1.2	2007/10/24	5,6 6 7 9 13 15	Added FPC pin assignment note Remove temp. condition of Absolute Maximum Ratings Added operation condition Updated Control register bit settings and definitions Updated power on sequence Update Note 1 description
1.3	2007/12/10	17	Update Vibration discription.
1.4	2008/01/04	9	Updated Control register bit settings and definitions
1.5	2008/06/05	4 18 19	Update overall dimension Update Packing Form Update Outline Drawing
1.6”	2008/07/07	4 19	Update overall thickness Update Outline Drawing
1.7	2008/08/12	4 19	Correct: Surface Treatment Update Outline Drawing

Contents

A. Physical specifications

NO.	Item	Specification	Remark
1	Display Resolution (dot)	640RGB (H) X 480 (V)	
2	Active Area (mm)	101.76 (H) X 76.32 (V)	
3	Screen Size (inch)	5.0” (Diagonal)	
4	Dot Pitch (mm)	0.053 (H) X 0.159 (V)	
5	Color Configuration	R. G. B. Stripe	Note 1
6	Color Depth	262K Colors	Note 2
7	Overall Dimension (mm)	126.1 (H) X 98.23 (V) X 14.96 (T)	Note 3
8	Weight (g)	82.6	
9	Surface Treatment	Anit-glare	
10	Display Mode	Normally White	

Note 1: Below figure shows dot stripe arrangement.



Note 2: Full color display depends on 6-bit data signal (pin 12~17, 19~24 and 26~31).

Note 3: Not include FPC. Refer to next page to get further information

B. Electrical Specifications

1. FPC Pin Assignment

Pin No.	Symbol	Type	Description	Remark
1	VLED	PI	Power for LED backlight (+5 VDC)	Note 1
2	VLED	PI	Power for LED backlight (+5 VDC)	Note 1
3	VLED	PI	Power for LED backlight (+5 VDC)	Note 1
4	DIM	I	Dimmer Control for Backlight (PWM signal)	Refer section C2
5	LEDGND	PI	Ground for LED Backlight	
6	LEDGND	PI	Ground for LED Backlight	
7	LEDGND	PI	Ground for LED Backlight	
8	GND	PI	Ground	
9	VDD	PI	Power Supply (+3.3V)	Note 2
10	VDD	PI	Power Supply (+3.3V)	Note 2
11	GND	PI	Ground	
12	R0	I	Red Data (LSB)	
13	R1	I	Red Data	
14	R2	I	Red Data	
15	R3	I	Red Data	
16	R4	I	Red Data	
17	R5	I	Red Data (MSB)	
18	GND	PI	Ground	
19	G0	I	Green Data (LSB)	
20	G1	I	Green Data	
21	G2	I	Green Data	
22	G3	I	Green Data	
23	G4	I	Green Data	
24	G5	I	Green Data (MSB)	
25	GND	PI	Ground	

Pin No.	Symbol	Type	Description	Remark
26	B0	I	Blue Data (LSB)	
27	B1	I	Blue Data	
28	B2	I	Blue Data	
29	B3	I	Blue Data	
30	B4	I	Blue Data	
31	B5	I	Blue Data (MSB)	
32	GND	PI	Ground	
33	PXLCLK	I	Pixel Clock	
34	HSYNC	I	Horizontal Sync Signal	
35	VSYNC	I	Vertical Sync Signal	
36	DE	I	Data Enable	
37	GND	PI	Ground	
38	SPENA	I	Serial Port Data Enable (Normally High)	
39	SPCK	I	Serial Port Clock (Normally High)	
40	SPDA	I/O	Serial Port Data Input/Output	

Note : I: Input; O: Output; P: Power.

Note 1: VLED current supply must be greater than 330mA.

Note 2: VDD current supply must be greater than 300mA.

2. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remark
Power voltage	VDD	-0.3	5.0	V	Note 1
Input signal voltage	Vi	-0.3	VDD+ 0.3	V	

Note 1: Functional operation should be restricted under normal ambient temperature.

C. Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

1. TFT- LCD Typical Operation Condition

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
VDD voltage input	VDD	3.1	3.3	3.5	V	
VDD current input	IVDD	300			mA	
Input high voltage	Vh	0.7*VDD	-	VDD	V	
Input low voltage	Vl	0	-	0.3*VDD		
PXLCLK frequency	f_{DCLK}	-	25.175	28	MHz	
LED Life Time		20000	50000		hr	20mA, 25℃

2. VLED and Dimmer signal Operation Condition

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
VLED voltage input	VLED	4.8	5.0	5.2	V	
VLED current input	ILED	330			mA	
DIM signal	V_{DIM}		3.3		V	0V = light on 3.3V = light off
DIM Frequency	f_{DIM}		24.5		KHz	

3. 3-Wire Serial Interface and Register Parameters

The 3-wire serial port is the communication interface for all the function and parameter setting. The communication is bi-directional controlled by the “R/W” bit (read not write) in the address field.

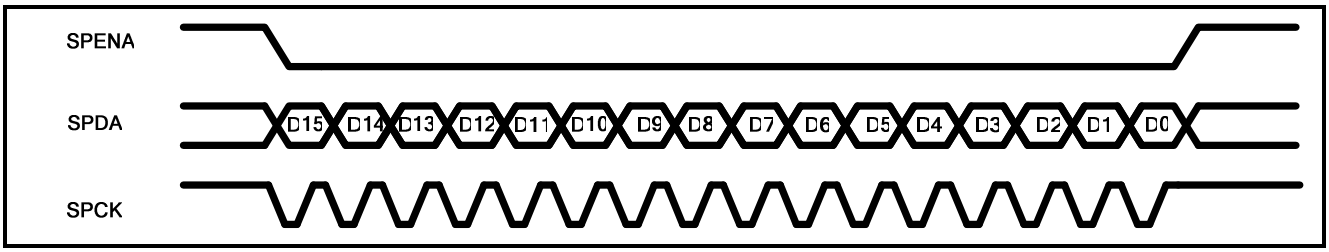
Under the read mode, the 3-Wire engine will return the data during “Data phase” (refer to figure below). The returned data should be latched at the rising edge of the SPCK signal by the external controller. During the read operation, the external controller should float the SPDA signal during “Hi-Z phase” and “Data phase”. Under the write mode, data in the “Hi-Z phase” will be ignored by the 3-Wire engine.

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a SPENA Low period will be ignored by 3-Wire engine.

Register settings must send to panel’s master source IC and slave source IC. The slave address has a 0x20 offset to the master address. For example,

Master R02: 3-wire address D[15:10] = 000010b.

Slavev R02: 3-wire address D[15:10] = 100010b.



3-Wire comment format

Bit	Description
D15-D10	Register Address [5:0].
D9	W/R control bit. “1” for Write; “0” for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7-D0	Data for the W/R operation to the address indicated by Address phase

Write format

MSB LSB															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						1	X	DATA (Issue by external controller)							

Read format

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						0	Hi-Z	DATA (Issue by 3-Wire engine)							

Control register bit settings and definitions

Name	D[15]	D[14:10]	Bit [9]	Bit [8]	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R00	M/S	00000	R/W	X	0	0	0	0	0	1	STBYB [1]	RESETB [1]
R01	M/S	00001	R/W	X	1	1	1	0	0	0	1	0
R02	M/S	00010	R/W	X	0	0	0	1	0	1	0	0
R03	M/S	00011	R/W	X	1	1	0	0	1	1	0	0
R04	M/S	00100	R/W	X	DDLY7	DDLY6	DDLY5	DDLY4	DDLY3	DDLY2	DDLY1	DDLY0
R05	M/S	00101	R/W	X	X	HDLY6	HDLY5	HDLY4	HDLY3	HDLY2	HDLY1	HDLY0
R07	M/S	00111	R/W	X	0	0	1	1	0	0	1	0

Note1: Register function active at the falling edge of Vsync signal except STBYB, RESETB and R03 register bits.

Note2: Master(M) = 0 / Slave(S) = 1.

Note3: Read(R) = 0 / Write(W) = 1.

Note4: X = don't care.

R00: System Control Register

Bit	Name	Initial	R/W	Description
Bit [1]	STBYB	1b	R/W	Standby Mode function control. STBYB = "0", TCON, Source output will turn off and outputs are High-Z. STBYB = "1", Normal operation
Bit [0]	RESETB	1b	R/W	Global Reset Register. Write "0" to reset whole chip. This bit will set to "1" automatically after chip was reset.

R04 : Contrast Control Register

Bit	Name	Initial	R/W	Description
Bit [7:0]	DDLY[7:0]	45h	R/W	Select the HSD signal to 1st input data delay timing. Refer to "Thbp" symbol in Section 4.

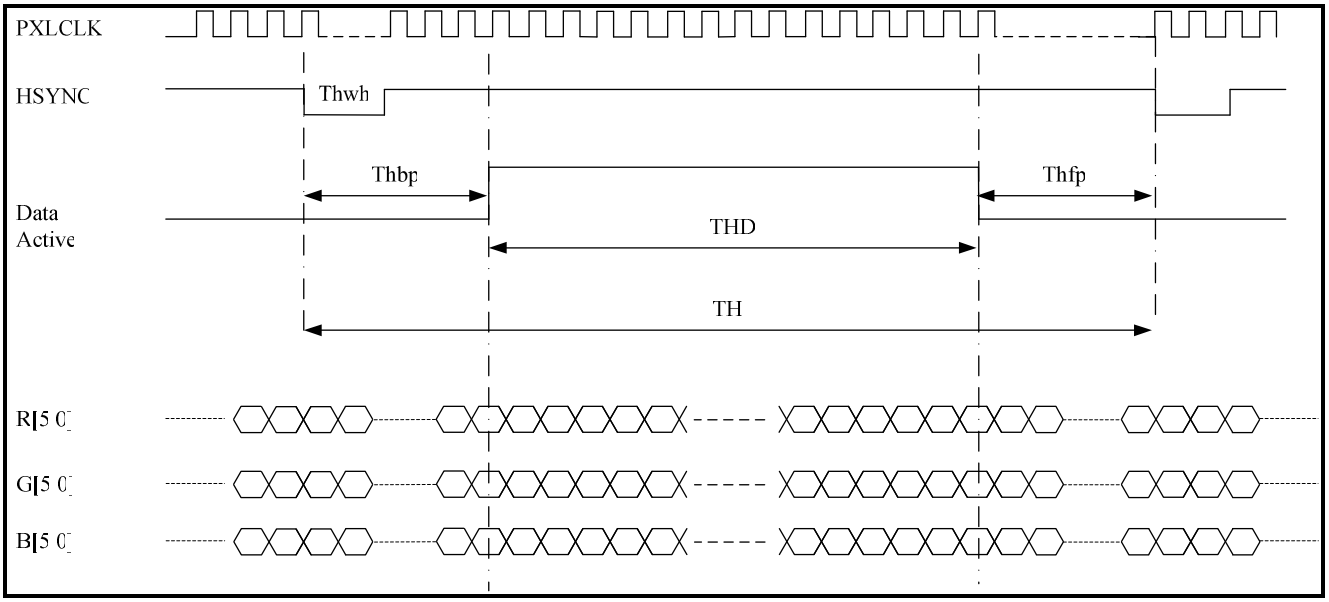
R05: Gate Timing Delay Cotnrol Register

Bit	Name	Initial	R/W	Description
Bit [7]	-	0b	-	Reserve
Bit [6:0]	HDLY[6:0]	0Ch	R/W	Select the Gate start pulse output delay timing Refer to “Tvbp” symbol in Section 4.

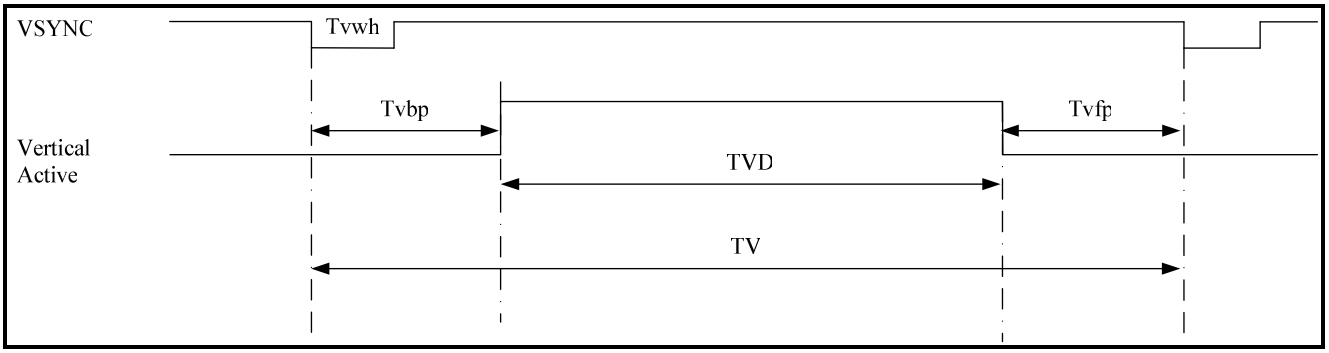
4. AC Timing

a. Timing Diagram

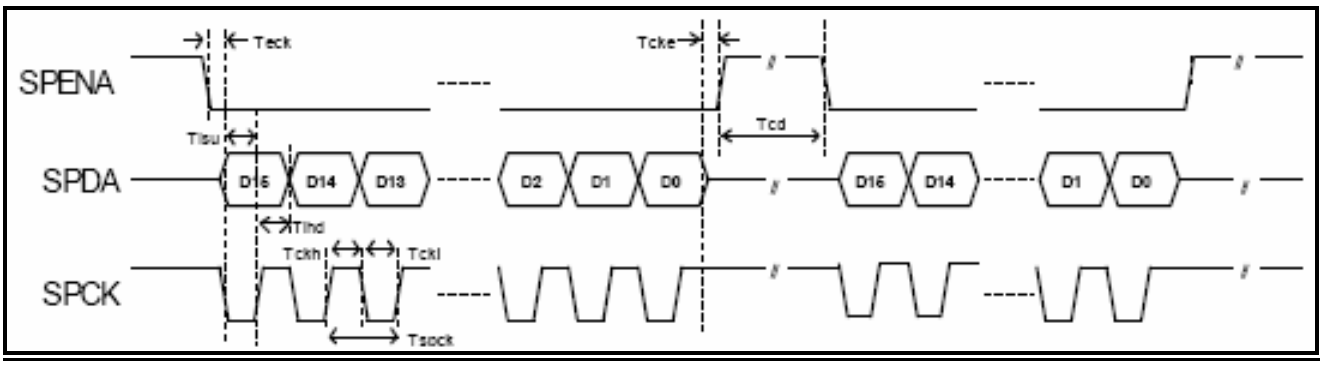
Horizontal Input Data Timing Diagram



Vertical Input Data Timing Diagram



3-wire Timing Diagram



b. Timing Condition

PixClk and Data Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
CLKIN clock time	Tdclk		35.714	39.72	ns	CLKIN = 28 MHz
H-sync width	Thwh	1	10	255	Tdclk	
Horizontal back portch	Thbp	40	70	255	Tdclk	
Horizontal front portch	Thfp	8	90	255	Tdclk	
Horizontal data active time	THD	640	640	640	Tdclk	
Horizontal period	TH	688	800	1150	Tdclk	1TH = 1 line
V-sync width	Tvwh	1	2	255	TH	
Vertical back portch	Tvbp	6	13	128	TH	
Vertical front portch	Tvfp	4	32	255	TH	
Vertical data active time	TVD	480	480	480	TH	
Vertical period	TV	490	525	863	TH	1 TV = 1 field

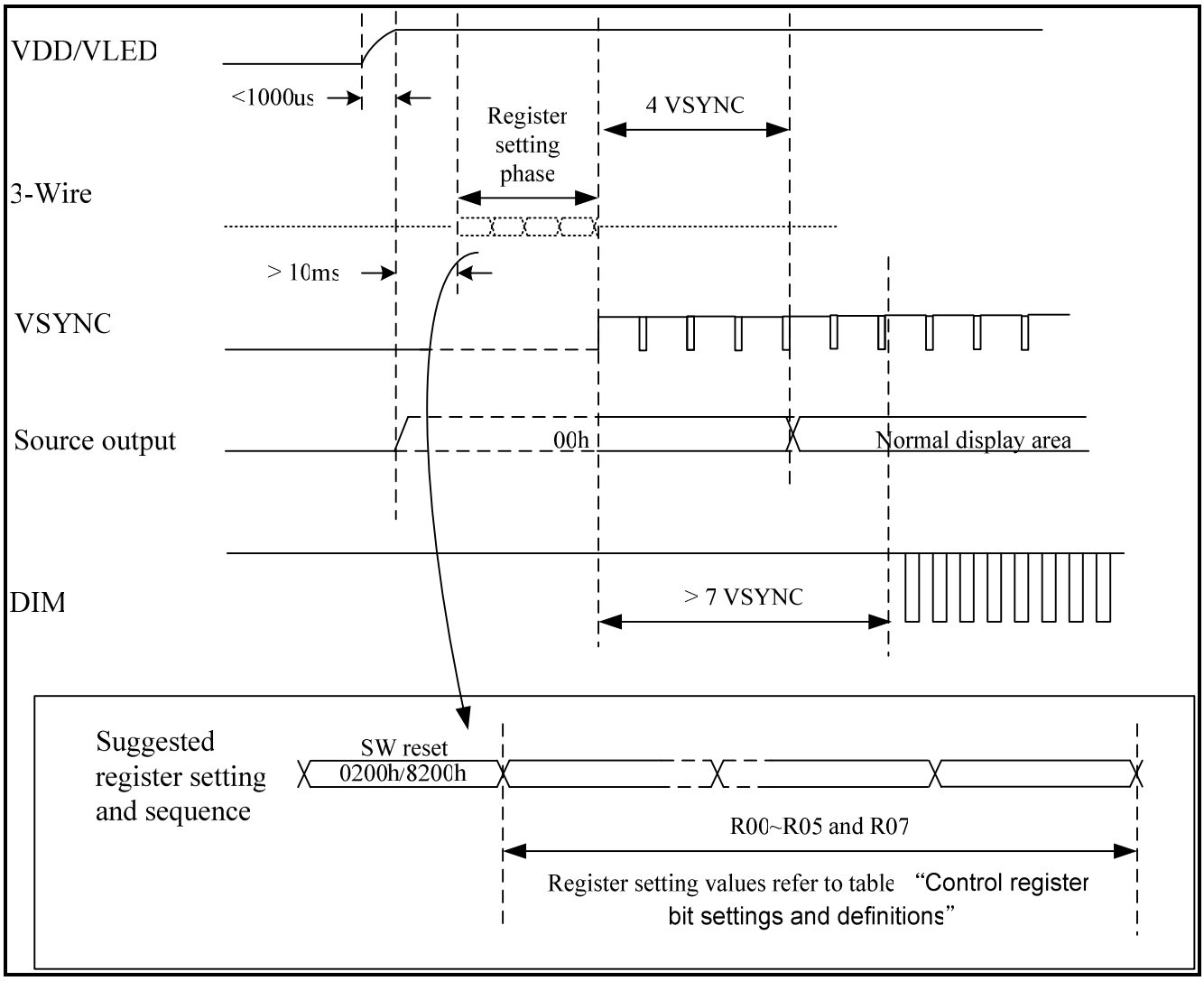
3-Wire Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Serial Clock Period Time	Tspck	320	-	-	ns	
SPCK pulse duty cycle	Tscdut	40	50	60	%	
Serial data setup time	Tisu	120	-	-	ns	
Serial data hold time	Tihd	120	-	-	ns	
Serial clock high/low	Tssw	120	-	-	ns	
SPENB select distinguish	Tcd	1	-	-	us	

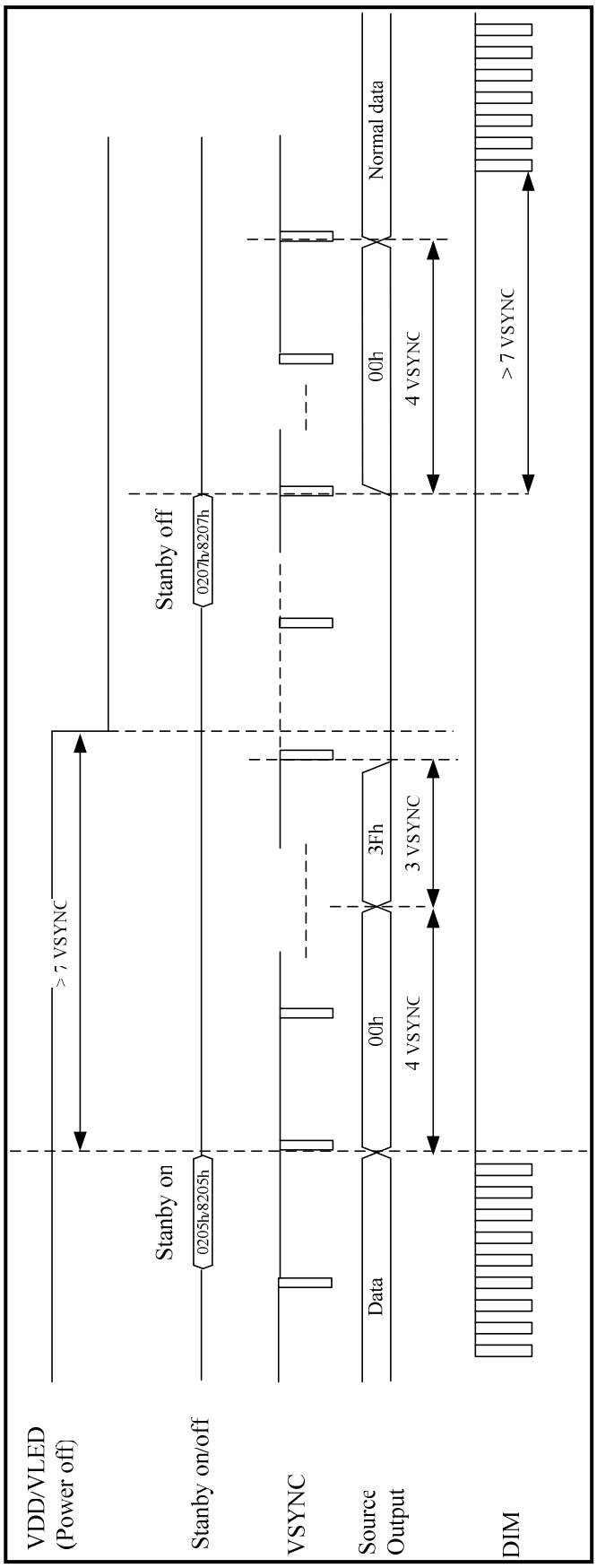
5. Power On/Off and Standby On/Off Sequence

The LCD apopts high voltage driver IC, so it could be permanently damaged under a wrong power on/off sequence. The suggested LCD power sequence is below:

Power On Sequence



Power off and Standby On/Off Sequence



D. Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	θ =0°	-	15	-	ms	Note 4
Fall	Tf		-	25	-	ms	
Contrast ratio	CR	At optimized viewing angle	400	500			Note 6, 7
Viewing Angle							
Top			35	45	-		
Bottom		CR≧10	55	65	-	deg.	Note 8
Left			55	65	-		
Right			55	65			
Brightness	Y_L	θ =0°	250	350	-	cd/m^2	Note 9
White Chromaticity	X	θ =0°	0.26	0.31	0.36		
	y	θ =0°	0.28	0.33	0.38		

Note 1: Measurement is in the dark room, optical ambient temperature =25℃, and backlight current IL=120 mA

Note 2: To be measured in the dark room.

Note 3:To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

Note 5. From liquid crystal characteristics, response time will become slower and the color of panel will become darker when ambient temperature is below 25℃.

Note 6. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrastratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 7. White $Vi=V_{i50} + \overline{-}1.5V$

Black $Vi=V_{i50} \pm 2.0V$

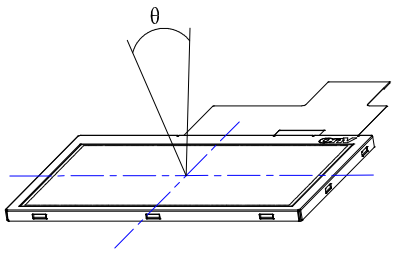
“±” means that the analog input signal swings in phase with COM signal.

“$+$” means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 8. Definition of viewing angle: refer to figure as below.



Note 9. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

E. Reliability test items:

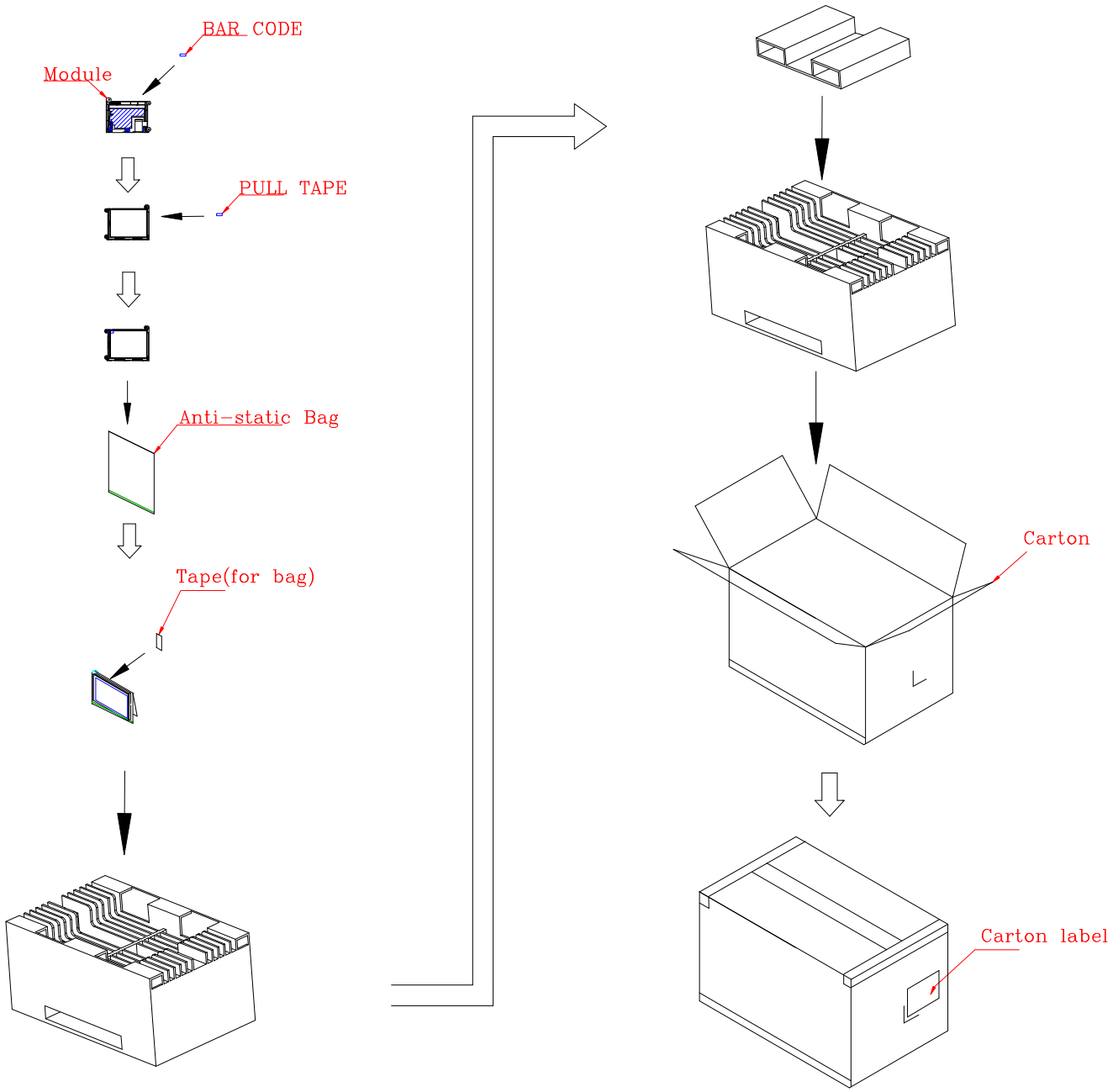
No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70℃ 240Hrs	
2	Low Temperature Storage	Ta= -10℃ 240Hrs	
3	High Ttemperature Operation	Tp= 60℃ 240Hrs	
4	Low Temperature Operation	Ta= 0℃ 240Hrs	
5	High Temperature & High Humidity	Tp= 60℃, 90% RH 240Hrs	Operation
6	Heat Shock	-10℃~70℃/50 cycles 2Hrs/cycle	
7	Electrostatic Discharge	±200V,200pF(0Ω), once for each terminal	
8	Vibration	Frequency range 10~55Hz Stoke 1.5mm Sweep 10~55~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A 240Hrs
9	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1: Ta: Ambient Temperature.

Note 2: Squarely inspect all LCD function before and after ambient environment test.

Note3: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

F. Packing Form



Max. Capacity: 40 Pcs Modules
Max. Weight: 9.0 Kg
Carton outline.: 520mm*340mm*250mm

G. Outline Drawing: