CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A050VVN01.0**
CUSTOMER APPROVED	Title : Name :

☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.0)**

☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver. 0.0)**

☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver. 0.0)**

☐ **CUSTOMER REMARK :**

AUO PM :

P/N : 97.05A16.000

Comment :

Doc. version :	0.0
Total pages :	27

Date : 2011/10/19

Product Specification

5" COLOR TFT-LCD MODULE/PANEL

Model Name： **A050VVN01.0**

Planned Lifetime:	From 2010/Oct To 2012/Dec
Phase-out Control:	From 2012/July To 2012/Dec
EOL Schedule:	2012/ Dec

<◆>Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	20111019		First Draft

Contents

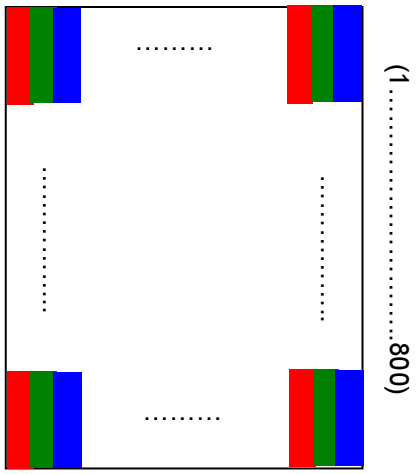
A. General Information

This product is for PND application.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	5(Diagonal)	
2	Display Resolution	dot	480RGB(H)×800(V)	
3	Overall Dimension	mm	71.2(H)X119.5(V)X2.61(T)	Note 1
4	Active Area	mm	64.8(H)×108.0(V)	
5	Pixel Pitch	mm	0.045(H)×0.135(V)	
6	Color Configuration	--	R. G. B. Stripe	Note 2
7	Color Depth	--	16.7M Colors	
8	NTSC Ratio	%	50	
9	Display Mode	--	Normally Black	
11	Weight	g	46.5±5	
12	Power Consumption	mW	878(typ)	Note 3
13	Interface	--	24 bit RGB	

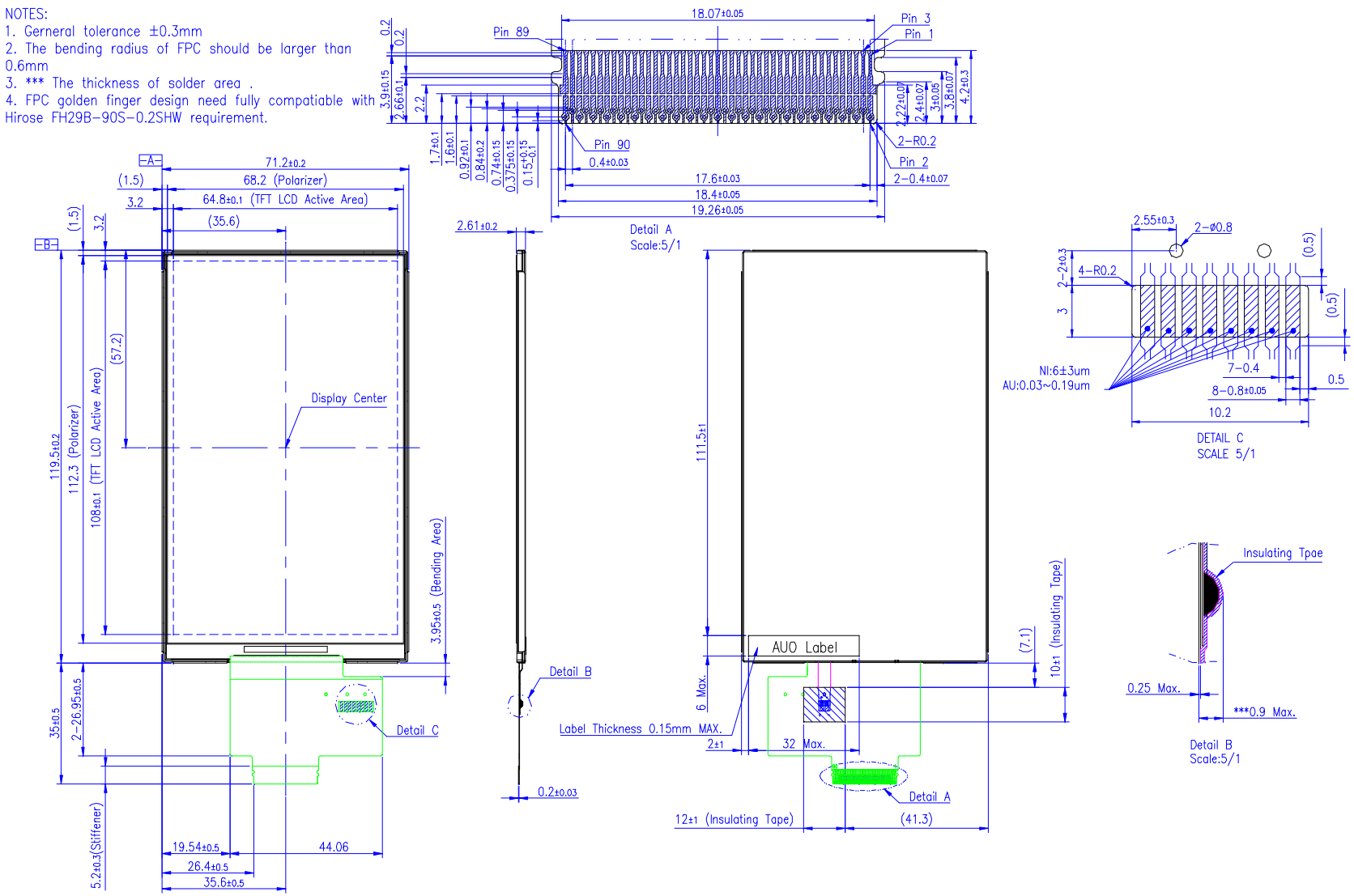
Note 1: Not include blacklight cable and FPC. Refer next page to get further information.

Note 2: Below figure shows dot stripe arrangement.



Note 3: Please refer to Electrical Characteristics chapter.

B. Outline Dimension



C. Electrical Specifications

1. TFT LCD Panel Pin Assignment

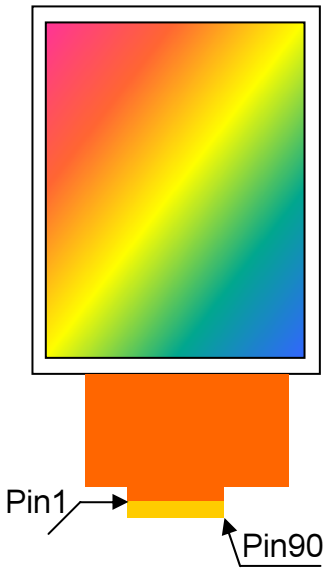
Recommended connector : FH29B-90S-0.2SHW

Pin no	Symbol	I/O	Description	Remark
1	VCOM	C	Stabilizing capacitor	
2	VGL	C	Stabilizing capacitor	
3	C51N	C	Booster capacitor	
4	C51P	C	Booster capacitor	
5	VGH	C	Stabilizing capacitor	
6	C41N	C	Booster capacitor	
7	C41P	C	Booster capacitor	
8	DVDD	C	Stabilizing capacitor	
9	C32N	C	Booster capacitor	
10	C32P	C	Booster capacitor	
11	C31N	C	Booster capacitor	
12	C31P	C	Booster capacitor	
13	VCL	C	Stabilizing capacitor	
14	VCI	P	Power supply for DC-DC circuit	
15	C24N	C	Booster capacitor	
16	C24P	C	Booster capacitor	
17	C23N	C	Booster capacitor	
18	C23P	C	Booster capacitor	
19	C22N	C	Booster capacitor	
20	C22P	C	Booster capacitor	
21	C21N	C	Booster capacitor	
22	C21P	C	Booster capacitor	
23	AVEE	C	Stabilizing capacitor	
24	AVDD	C	Stabilizing capacitor	
25	C14N	C	Booster capacitor	
26	C14P	C	Booster capacitor	
27	C13N	C	Booster capacitor	
28	C13P	C	Booster capacitor	
29	C12N	C	Booster capacitor	
30	C12P	C	Booster capacitor	
31	C11N	C	Booster capacitor	
32	C11P	C	Booster capacitor	
33	VREFCP	C	Stabilizing capacitor	
34	VCI	P	Power supply for DC-DC circuit	

35	LED_PWM	O	PWM type control signal for brightness of the LED backlight	If not used, please open this pin.
36	VDDI	P	Power supply for interface system	
37	VS	I	Vertical sync input	
38	GND	P	Ground	
39	HS	I	Horizontal sync input	
40	GND	P	Ground	
41	PCLK	I	Data clock Input	
42	GND	P	Ground	
43	DE	I	Data enable input. Active level is high.	Please connect to GND, if do not use.
44	GND	P	Ground	
45	DB0	I	Blue Data input; LSB	
46	DB1	I	Blue Data input	
47	DB2	I	Blue Data input	
48	DB3	I	Blue Data input	
49	DB4	I	Blue Data input	
50	DB5	I	Blue Data input	
51	DB6	I	Blue Data input	
52	DB7	I	Blue Data input; MSB	
53	DG0	I	Green Data input; LSB	
54	DG1	I	Green Data input	
55	DG2	I	Green Data input	
56	DG3	I	Green Data input	
57	DG4	I	Green Data input	
58	DG5	I	Green Data input	
59	DG6	I	Green Data input	
60	DG7	I	Green Data input ; MSB	
61	DR0	I	Red Data input; LSB	
62	DR1	I	Red Data input	
63	DR2	I	Red Data input	
64	DR3	I	Red Data input	
65	DR4	I	Red Data input	
66	DR5	I	Red Data input	
67	DR6	I	Red Data input	
68	DR7	I	Red Data input; MSB	
69	GND	P	Ground	
70	VDDI	P	Power supply for interface system	

71	RESX	I	Reset pin. (Low active)	
72	CSX	I	Chip select (Low active) of SPI	
73	SCL	I	Clock input of SPI	
74	SDI	I	Data input of SPI	
75	GND	P	Ground	
76	GND	P	Ground	
77	GND	P	Ground	
78	GND	P	Ground	
79	VREF_PWR	C	Stabilizing capacitor	
80	VLED-	P	LED backlight cathode	
81	VLED+	P	LED backlight anode	
82	dummy	NC	No connection	Please open this pin.
83	TP1	I/O	TP1 control signal	If not used, please open this pin.
84	TP2	I/O	TP2 control signal	If not used, please open this pin.
85	TP3	I/O	TP3 control signal	If not used, please open this pin.
86	TP4	I/O	TP4 control signal	If not used, please open this pin.
87	TP5	I/O	TP5 control signal	If not used, please open this pin.
88	TP6	I/O	TP6 control signal	If not used, please open this pin.
89	TP7	I/O	TP7 control signal	If not used, please open this pin.
90	TP8	I/O	TP8 control signal	If not used, please open this pin.

Note 1: I: Input pin; O: Output pin; P: Power pin; G: Ground pin; C: Capacitor; NC: No connection



2. Absolute Maximum Ratings

Items	Symbol	Values		Unit
		Min.	Max.	
Supply Voltage	VCI	-0.3	+5.5	V
Supply Voltage	VDDI	-0.3	+5.5	V

Note : If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

3. Electrical DC Characteristics

a. Typical Operation Condition (GND = 0V)

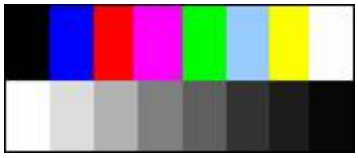
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Analog operating voltage	VCI	2.6	2.8	3.3	V	
Logic operating voltage	VDDI	1.65	2.8	3.3	V	
Logic high level input voltage	VIH	0.7VDDI	-	VDDI	V	
Logic low level input voltage	VIL	GND	-	0.3 VDDI	V	

b. Power Consumption (GND=0V)

Mode	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Normal	P_N	VCI = 2.8V VDDI = 2.8V	-	110	130	mW	Note 1,2
Sleep	P_S		-	30	35	mW	

Note 1: Test Condition is under typical Electrical DC and AC characteristics.

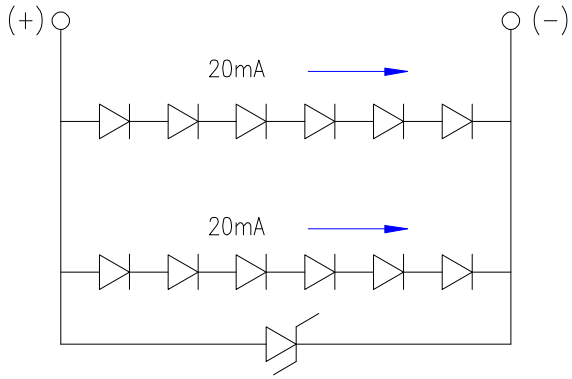
Note 2: Test pattern is the following picture (color bar).



c. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Supply Current	I_L		20	22	mA	single serial
Power Consumption	P_{BL}		768	937	mW	
LED Life Time	L_L	10,000	---	---	Hr	Note 2

Note 1: LED backlight is 12 LEDs serial type. Suggestion is driven by current 20mA for each LED string.



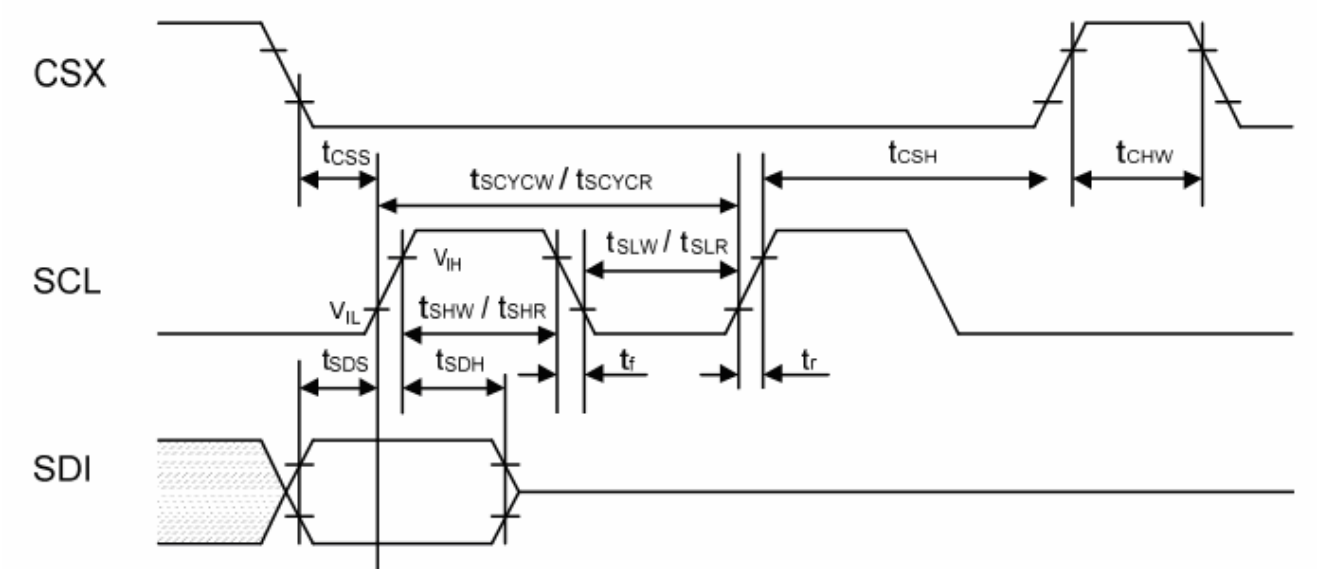
Note 2: Define “LED Lifetime”: brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25℃ and LED lightbar current = 20 mA.

Note 3: If it uses larger LED lightbar voltage/ current more than 22mA, it maybe decreases the LED lifetime

4. Electrical AC Characteristics

a. SPI Interface Characteristics

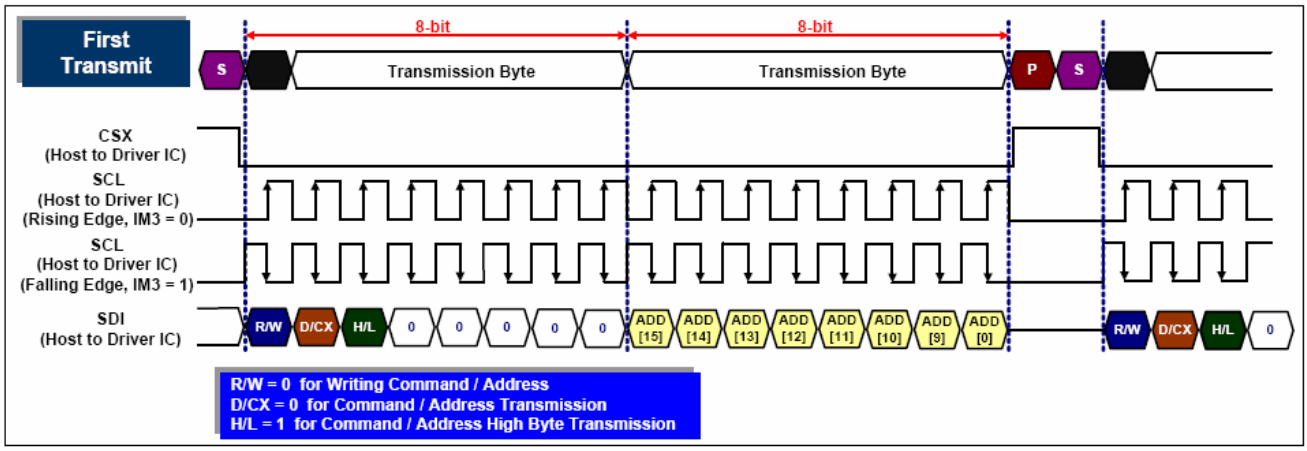
(a) Signal AC Characterics

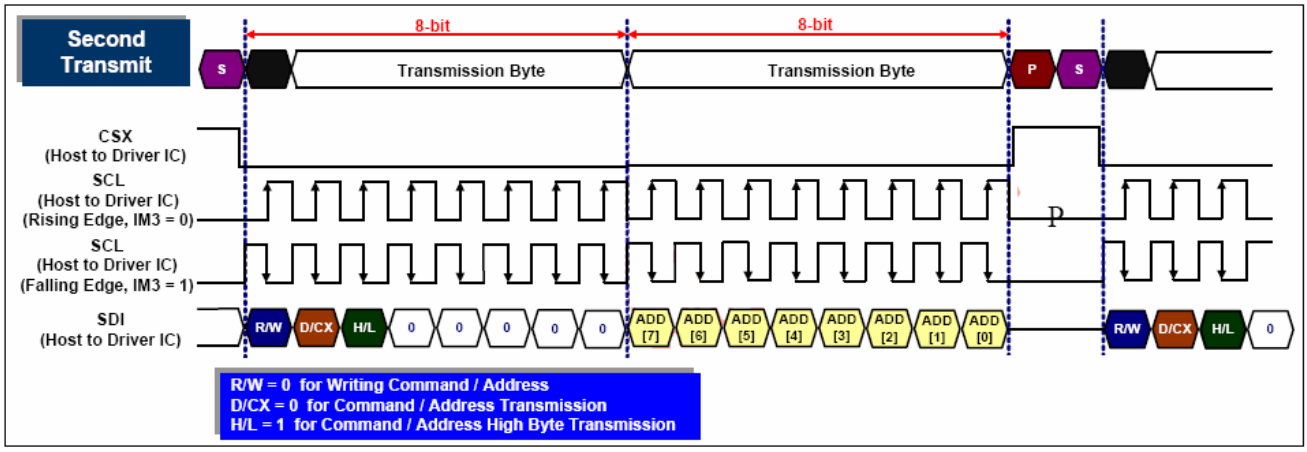


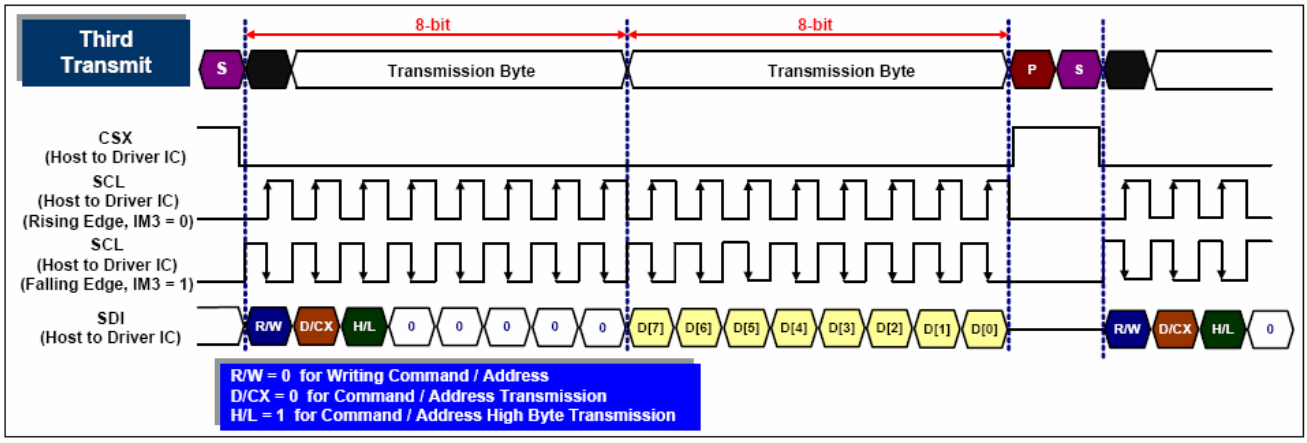
VDDI=1.65~3.3V, VCI=2.6~3.3V, TA=25℃

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
SCL	t_{SCYCW}	Serial clock cycle (Write)	100	-	ns	
	t_{SHW}	SCL “H” pulse width (Write)	40	-	ns	
	t_{SLW}	SCL “L” pulse width (Write)	40	-	ns	
	t_{SCYCR}	Serial clock cycle (Read GRAM)	300	-	ns	
	t_{SHR}	SCL “H” pulse width (Read GRAM)	140	-	ns	
	t_{SLR}	SCL “L” pulse width (Read GRAM)	140	-	ns	
	t_{SCYCR}	Serial clock cycle (Read ID)	300	-	ns	
	t_{SHR}	SCL “H” pulse width (Read ID)	140	-	ns	
	t_{SLR}	SCL “L” pulse width (Read ID)	140	-	ns	
SDI	t_{SDS}	DE setup time	20	-	ns	
	t_{SDH}	DE hold time	20	-	ns	
CSX	t_{CHW}	Chip select “H” pulse width	45	-	ns	
	t_{CSS}	Chip select setup time	20	-	ns	
	t_{CSH}	Chip select hold time	50	-	ns	

(b) Write Mode

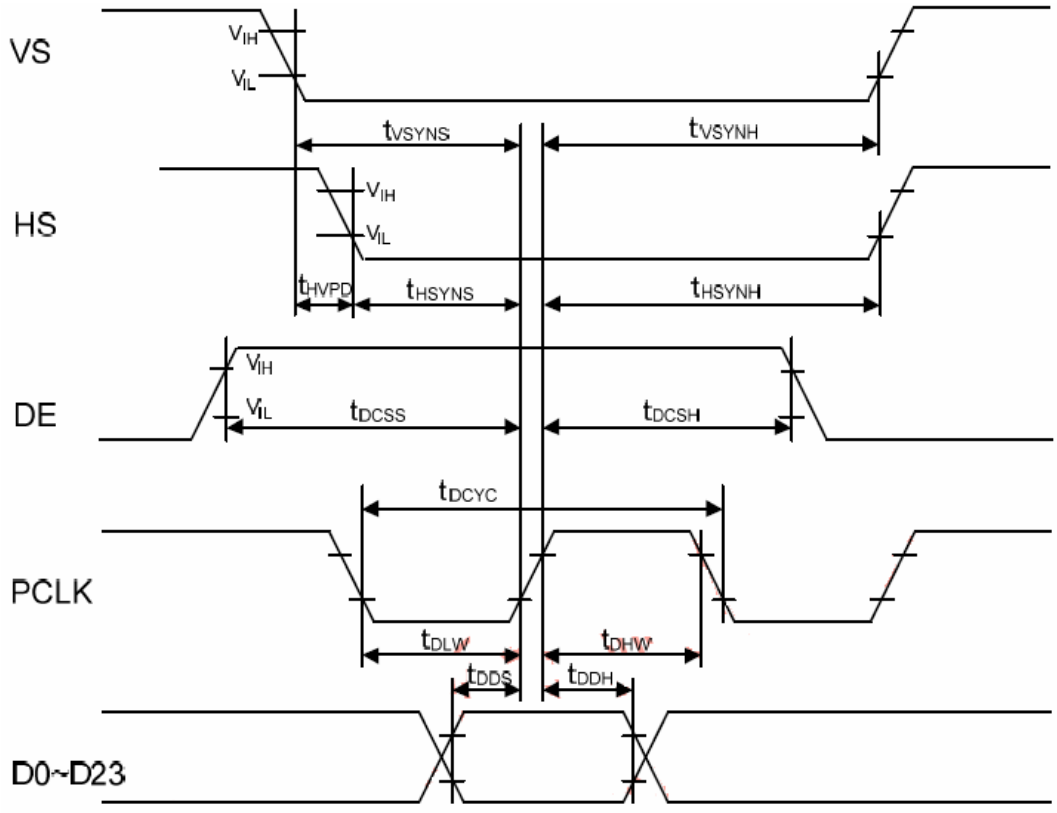






b. RGB Interface Characteristics

(a) Signal AC Characterics



VDDI=1.65~3.3V, VCI=2.6~3.3V, TA=25℃

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit
VS	t_{VSYNS}	VSYNC setup time	10			ns
	t_{VSYNH}	VSYNC hold time	10			ns
HS	t_{HSYNS}	HSYNC setup time	10			ns
	t_{SCYCR}	HSYNC hold time	10			ns
	t_{HVPD}	HSYNC to VSYNC falling edge	400			ns
PCLK	t_{DCYC}	PCLK cycle time	36.5	-	46.1	ns
	t_{DFREQ}	PCLK frequency	21.7	-	27.4	MHz
	t_{DLW}	PCLK “L” pulse width	11			ns
	t_{DHW}	PCLK “H” pulse width	11			ns
DE	t_{DCSS}	DE setup time	10			ns
	t_{DCSH}	DE hold time	10			ns
D0~D23	t_{DDS}	RGB Data setup time	10			ns
	t_{DDH}	RGB Data hold time	10			ns

Note 1: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

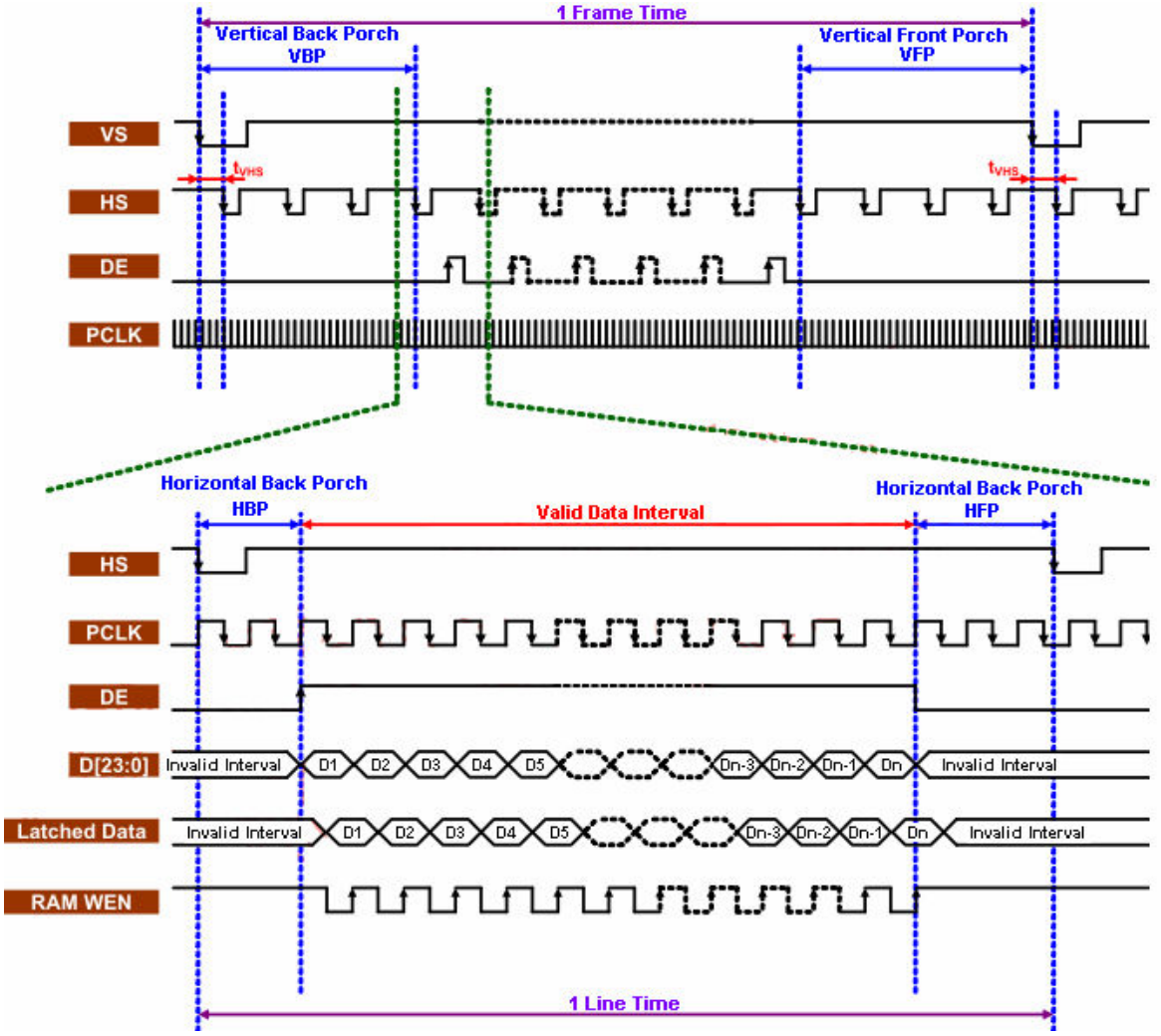
Note 2: Measuring of input signals are 0.30 x VDDI for low state and 0.7 x VDDI for high state.

(b) RGB Interface Mode Set

RGB I/F Mode	PCLK	DE	D23-D0	VS	HS	Register VFP[7:0], VBP[7:0]
RGB Mode 1 (SYNC + DE)	Used	Used	Used	Used	Used	Not used
RGB Mode 2 (SYNC Only)	Used	Not used	Used	Used	Used	Used

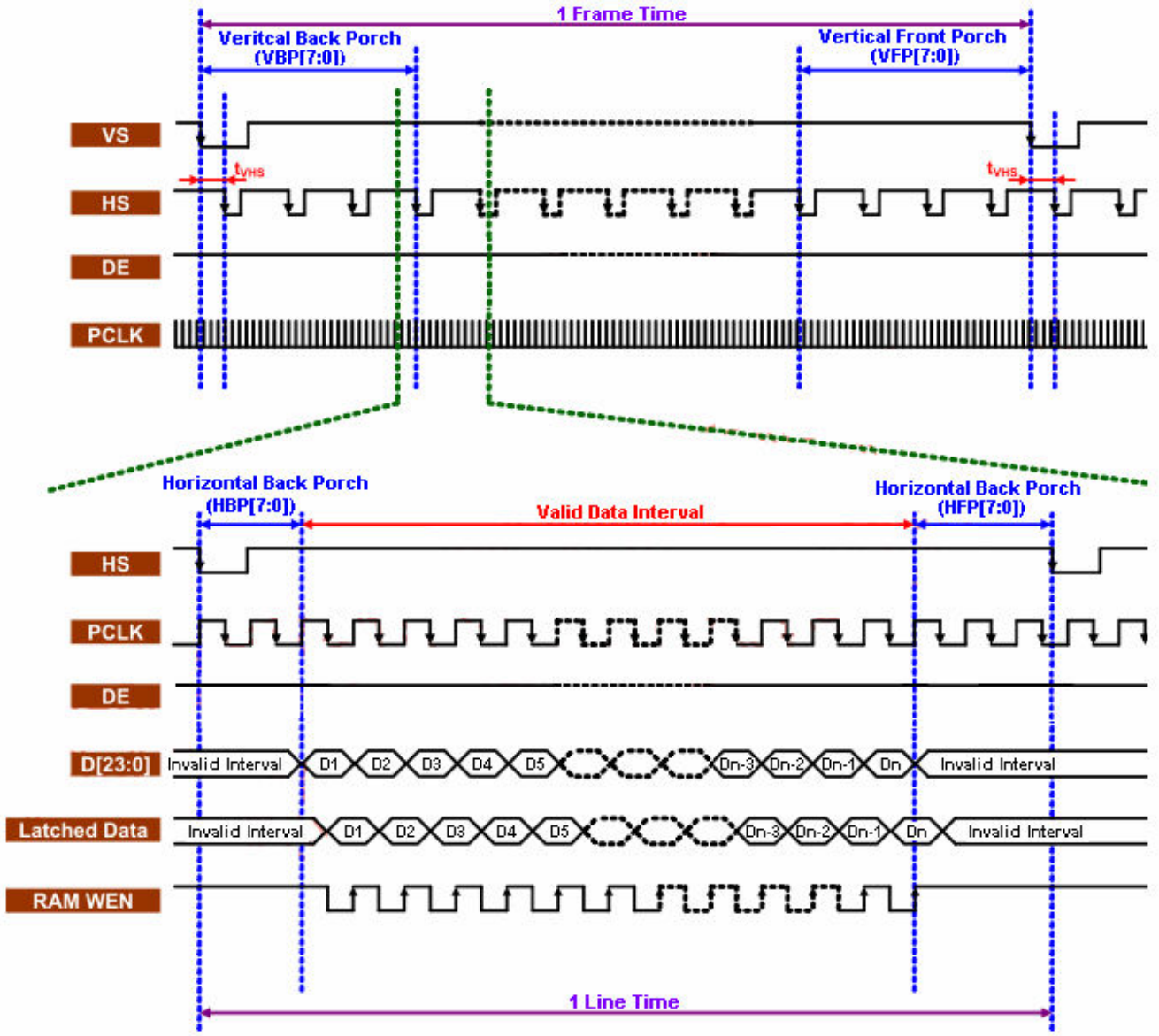
In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D23 to D0), when DE is high state. The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to IC DDI.
In RGB Mode 2, back porch of Vsync VBP is defined by VBP[7:0] of RGBCTR command. And back porch of Hsync HBP is defined by HBP[7:0] of RGRCTR command. Front porch of Vsync VFP is defined by VFP[7:0] of RGBCTR command. And front porch of Hsync HFP is defined by HFP[7:0] of RGBCTR command.

(c) Video signal data writing method in RGB Mode 1 Interface



Notes:
1. Constraint:
   V-Back Porch (Vsync+VBP)≧ 5 HS lines, V-Front-Borch (VFP) ≧ 5 HS lines
   H-Back Porch (Hsync+HBP)□ 5 PCLK clocks, H-Front-Porch (HFP) □ 2 PCLK clocks
2. t VHS□ 400ns
3. D[23:0] (DR[7:0], DG[7:0], DB[7:0])

(d) Video signal data writing method in RGB Mode 2 Interface



Notes:

1. Constraint:

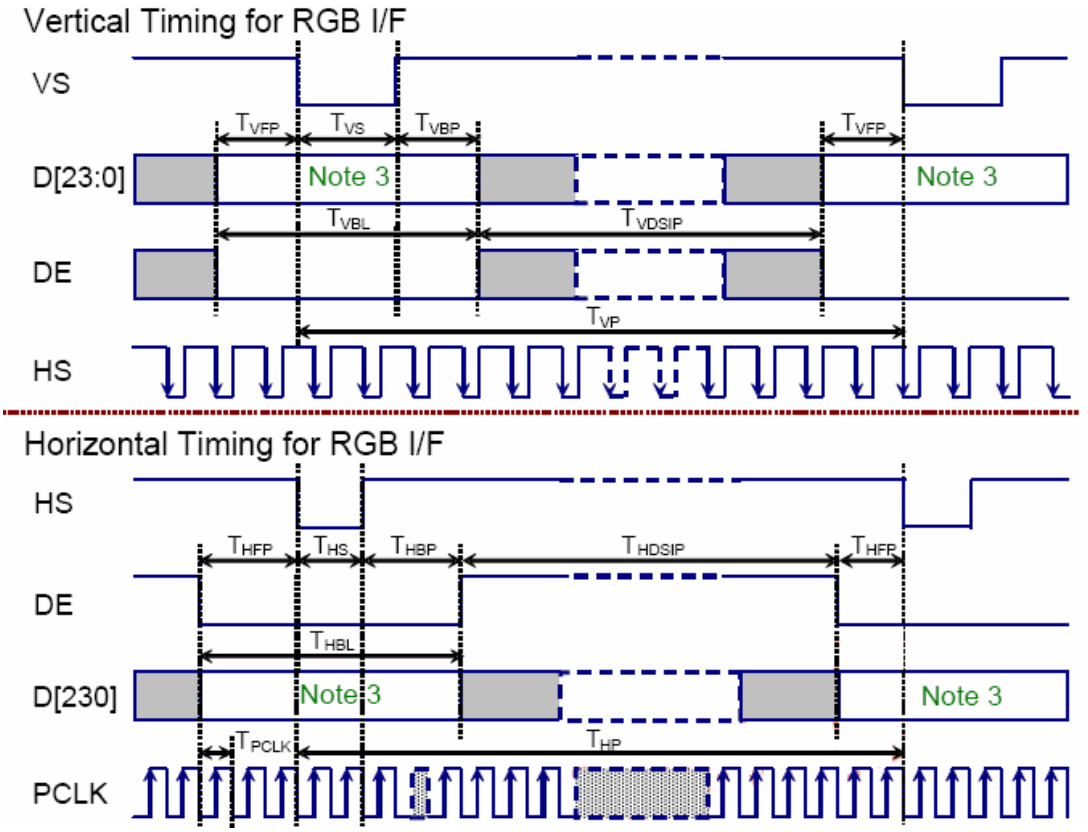
   V-Back Porch (VBP[7:0]) □ 5 HS lines, V-Front Porch (VFP[7:0]) □ 5 HS lines

   H-Back Porch (HBP[7:0]) □ 5 PCLK clocks, H-Back Porch (HFP[7:0]) □ 2 PCLK clocks

2. t VHS≧ 400ns

3. D[23:0] (DR[7:0], DG[7:0], DB[7:0])

(e) Vertical and horizontal timing



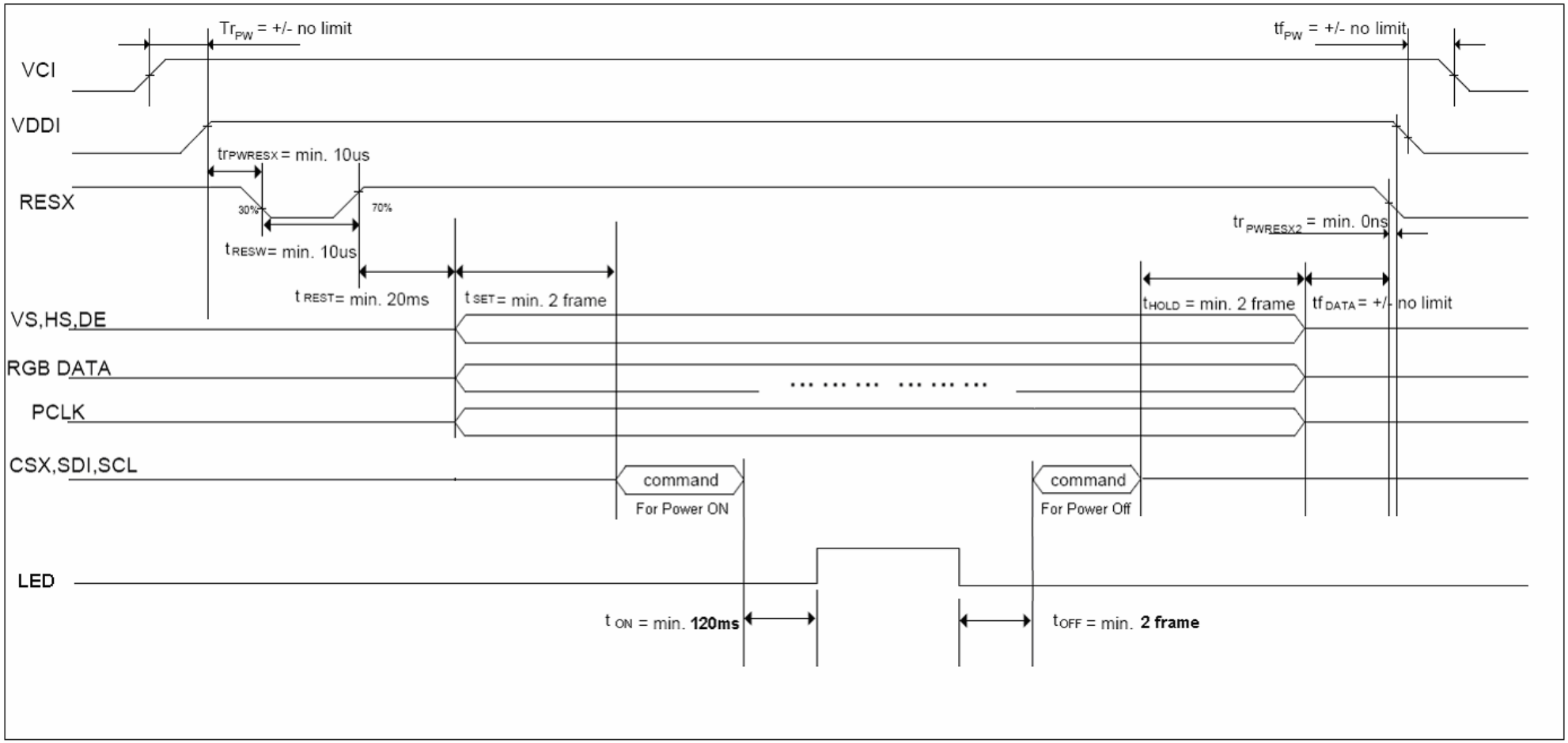
VDDI=1.65~3.3V, VCI=2.6~3.3V, TA=25℃

Veritcal Timing						
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
Vertical cycle period	T_{VP}	810	832	930	HS	
Vertical low pulse width	T_{VS}	2	-	-	HS	
Vertical front porch	T_{VFP}	5	-	64	HS	VFP[5:0]
Vertical back porch	T_{VBP}	3	-	64	HS	
Vertical data start line	$T_{VS} + T_{VBP}$	5	-	128	HS	VBP[5:0]
Vertical blanking period	$T_{VBL} = T_{VS} + T_{VBP} + T_{VFP}$	10	32	-	HS	
Vertical active area	T_{VDISP}	-	800	-	HS	
Vertical refresh rate	T_{VRR}	55	60	70	Hz	
Horizontal Timing						
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	
Horizontal cycle period	T_{HP}	487	512	610	PCLK	Note 2
Horizontal low pulse width	T_{HS}	2	-	-	PCLK	
Horizontal front porch	T_{HFP}	2	-	64	PCLK	HFP[5:0]
Horizontal back porch	T_{HBP}	3	-	64	PCLK	
Horizontal data start point	$T_{HS} + T_{HBP}$	5	-	128	PCLK	HBP[5:0]
Horizontal blanking period	$T_{HBL} = T_{HS} + T_{HBP} + T_{HFP}$	7	32	-	PCLK	
Horizontal active area	T_{HDISP}	-	480	-	PCLK	
Pixel clock cycle	$F_{PCLKCYC}$	21.7	25.6	27.4	MHz	

5. Power On / Off Characteristics

a. Recommended Power On/Off Sequence

The LCD adopts high voltage driver IC, so it could be permanently damaged under a wrong power on/off sequence. The suggested LCD power sequence is below:



6. Command Descriptions

a. User Command Set

Instruction	Address	D7	D6	D5	D4	D3	D2	D1	D0	Function
SLPIN	10h	No Argument								Sleep in & booster off
SLPOUT	11h	No Argument								Sleep out & booster on
DISPOFF	28h	No Argument								Display off
DISPON	29h	No Argument								Display on

b. Recommended Power On Register Setting

Number	Address	Data	Description
1	F000h	55h	Enable Manufacture Command for Page 0
2	F001h	AAh	
3	F002h	52h	
4	F003h	08h	
5	F004h	00h	
6	B100h	0Ch	Display Option Control
7	B101h	00h	
8	BC00h	05h	Inversion Driving Control
9	BC01h	05h	
10	BC02h	05h	
11	F000h	55h	Enable Manufacture Command for Page1
12	F001h	AAh	
13	F002h	52h	
14	F003h	08h	
15	F004h	01h	
16	**TBD**	**TBD**	**Power Control**
17	**TBD**	**TBD**	**Gamma Correction**
18	1100h	-	EXIT_SLEEP_MODE
Wait for more than 120ms			
19	2900h	-	SET_DISPLAY_ON

c. Recommended Power Off Register Setting

Number	Address	Data	Description
1	2800h	-	SET_DISPLAY_OFF
2	1000h	-	ENTER_SLEEP_MODE

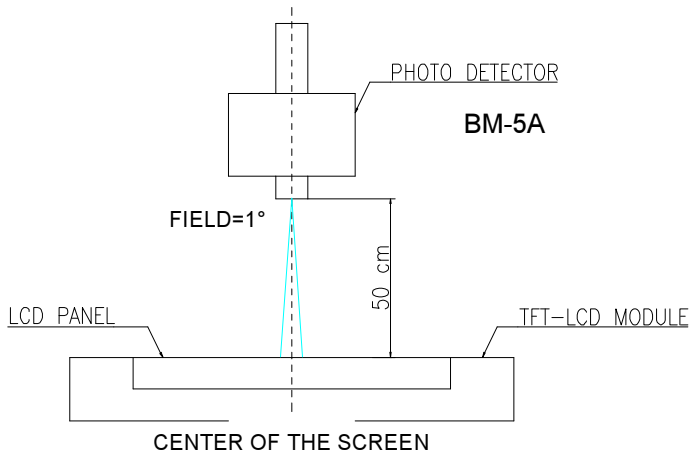
D. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall		 Tr Tf	θ=0°	 -- --	 20 15		 ms ms	Note 3
Contrast ratio		CR	At optimized viewing angle	650	800	--		Note 4
Viewing Angle	Top		CR≧10	60	80	--	deg.	Note 5
	Bottom			60	80	--		
	Left			60	80	--		
	Right			60	80	--		
Brightness		Y_L	θ=0°	360	450	--	cd/m^2	Note 6
Chromaticity	White	X	θ=0°	0.28	0.33	0.38		Tentative
		Y	θ=0°	0.30	0.35	0.40		Tentative
	Red	X	θ=0°	0.548	0.598	0.648		Tentative
		Y	θ=0°	0.306	0.356	0.406		Tentative
	Green	X	θ=0°	0.311	0.361	0.411		Tentative
		Y	θ=0°	0.536	0.586	0.636		Tentative
	Blue	X	θ=0°	0.095	0.145	0.195		Tentative
		Y	θ=0°	0.107	0.157	0.207		Tentative
Uniformity		ΔY_L	%	70	80	--	%	Note 7

Note 1: Measurement should be performed in the dark room, optical ambient temperature =25°C, and backlight current IL=20 mA.

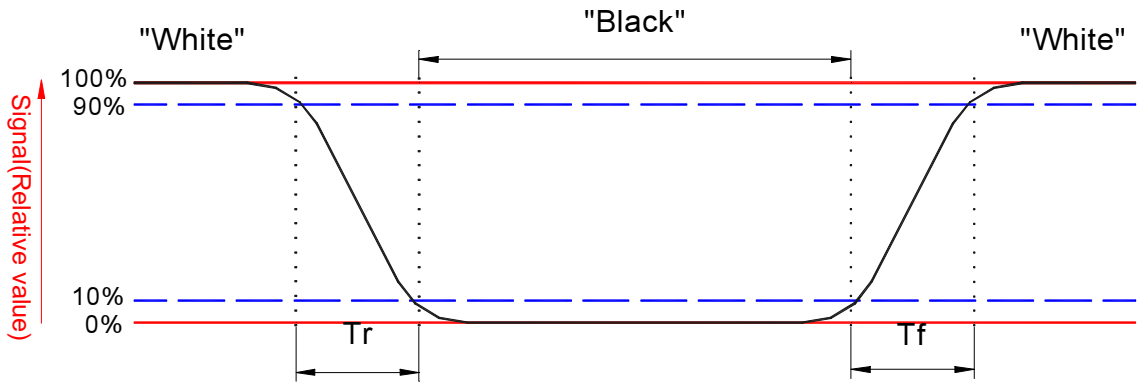
Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.



Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

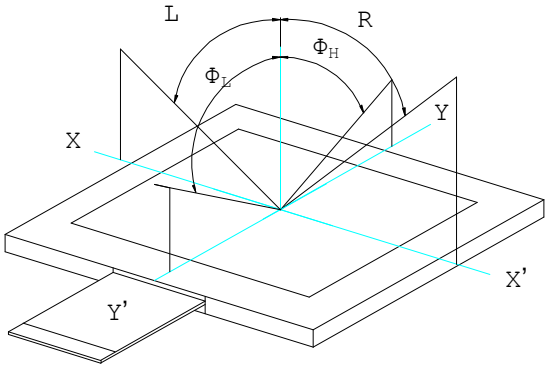


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

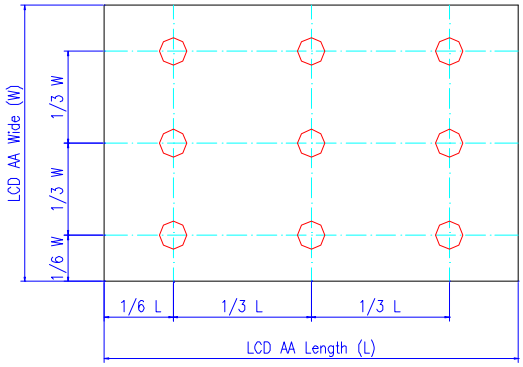
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

E. Reliability Test Items

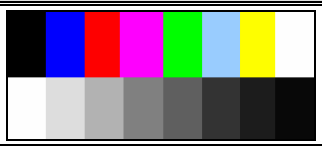
No.	Test items	Conditions		Remark
1	High Temperature Storage	Ta= 80°C	240Hrs	Note 1 & Note 2
2	Low Temperature Storage	Ta= -20°C	240Hrs	Note 1 & Note 2
3	High Temperature Operation	Ta= 70°C	240Hrs	Note 1 & Note 2
4	Low Temperature Operation	Ta= -10°C	240Hrs	Note 1 & Note 2
5	High Temperature & High Humidity	Ta= 60°C. 90% RH	240Hrs	Note 1 & Note 2
6	Heat Shock	-20°C ~70°C, 50 cycle, 2Hrs/cycle		Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B		Note 4
8	Vibration	Frequency range	: 8~33.3Hz	Non-operation JIS C7021, A-10 condition A : 15 minutes
		Stoke	: 1.3mm	
		Sweep	: 2.9G ,33.3~400Hz	
		2 hours for each direction of X,Y,Z		
		4 hours for Y direction		

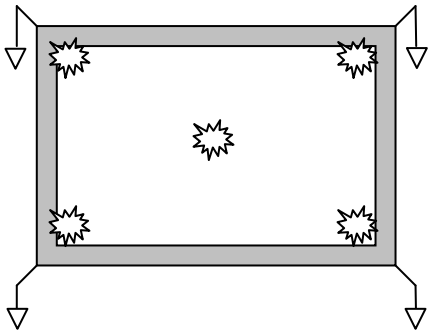
Note 1: Ta: Ambient Temperature.

Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

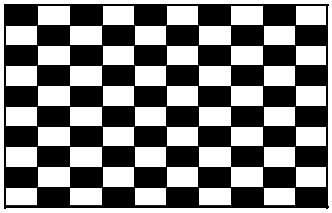
Note 3: All the cosmetic specification is judged before the reliability stress.

Note 4 : All test techniques follow IEC6100-4-2 standard.

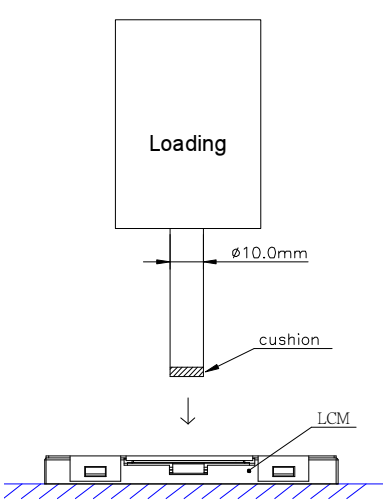
Test Condition		Note
Pattern		
Procedure And Set-up	Contact Discharge：330Ω, 150pF, 1sec, 5point, 10times/point Air Discharge：330Ω, 150pF, 1sec, 5 point, 10times/point	

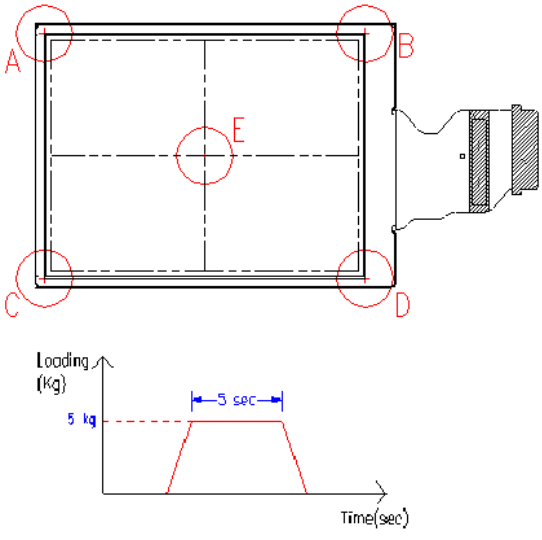
	 Note : 1. The metal casing is connected to ground (0V) at four corners. 2. All register commands are repeating transferred. 3. Judging the result after discharging.	
Criteria	B – Some performance degradation allowed. No data lost. Self-recoverable hardware failure.	
Others	1. Gun to Panel Distance 2. No SPI command, keep default register settings.	

Note 5: Operate with chess board pattern as figure and lasting time and temperature as the conditions. Then judge with 50% gray level, the mura is less than JND 2.8



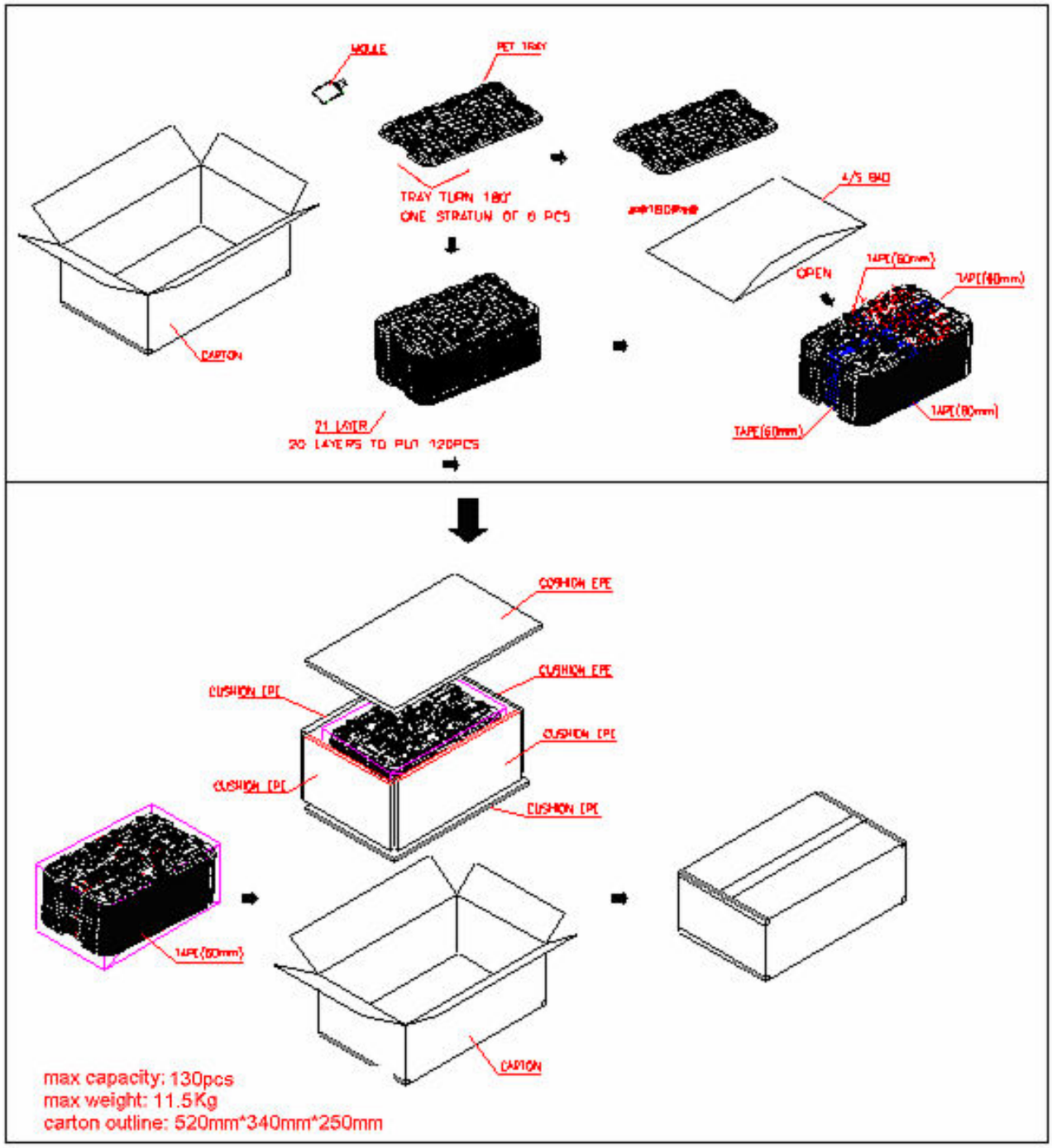
Note 6: The panel is tested as figure. The jig is ϕ 10 mm made by Cu with rubber and the loading speed is 3mm/min on position A~E. After the condition, no glass crack will be found and panel function check is OK.(no guarantee LC mura、LC bubble)



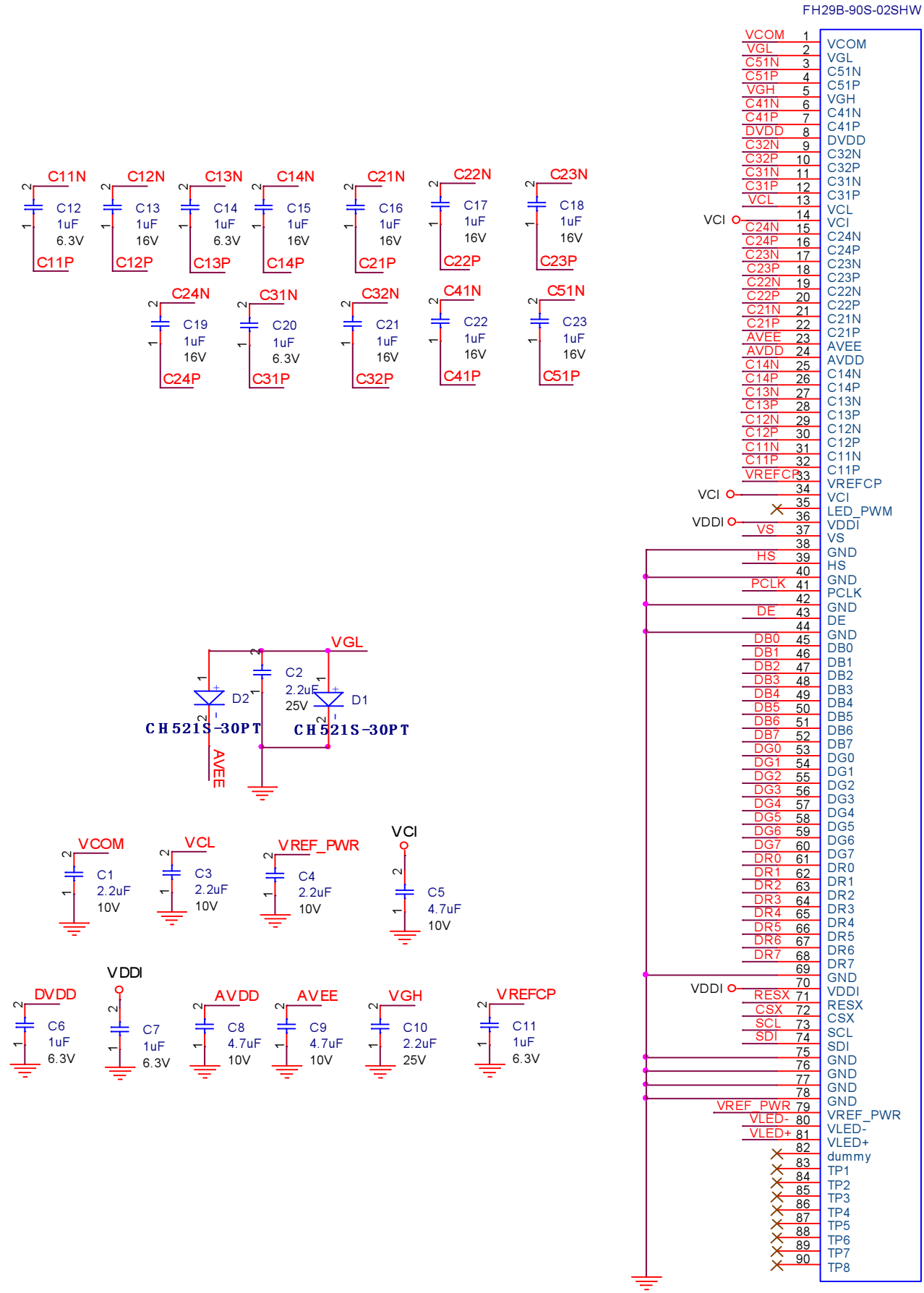


G. Packing and Marking

1. Packing Form



H. Application Circuit



I . Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.