




## Product Specification

AU OPTRONICS CORPORATION

( V ) Preliminary Specifications

( ) Final Specifications

Module	11.6"(11.57") HD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B116XTN02.3 (H/W:0A)
Note (  )	<i>LED Backlight with driving circuit design</i>

Customer

Date

Checked &  
Approved by

Date

Note: This Specification is subject to change without notice.

Approved by

Date

Luke Lin

12/06/2013

Prepared by

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12/18/2013

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### Record of Revision

Version and Date		Page	Old description	New Description	Remark
0.1	2013/12/06	All	First Edition for Customer		
0.2	2013/12/18	P.25	LCM O.D 158.5	LCM O.D 157.5	



### 1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



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### 2. General Description

B116XTN02.3 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x 768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B116XTN02.3 is designed for a display unit of notebook style personal computer and industrial machine.

### 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	293.8			
Active Area	[mm]	256.125 X 144.0			
Pixels H x V		1366x3(RGB) x 768			
Pixel Pitch	[mm]	0.1875 x 0.1875			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (I <sub>LED</sub> =20mA) (Note: I <sub>LED</sub> is LED current)	[cd/m <sup>2</sup> ]	220 typ. (5 points average)			
Luminance Uniformity		1.6 max. (13 points)			
Contrast Ratio		400 typ			
Response Time	[ms]	8 typ			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	2.65			
Weight	[Grams]	220 max.			
Physical Size Include bracket	[mm]		Min.	Typ.	Max.
		Length	277.5	278	278.5
		Width	167.5	168	168.5
		Thickness	-	-	3.0
Electrical Interface		1 lane eDP			
Glass Thickness	[mm]	0.4			



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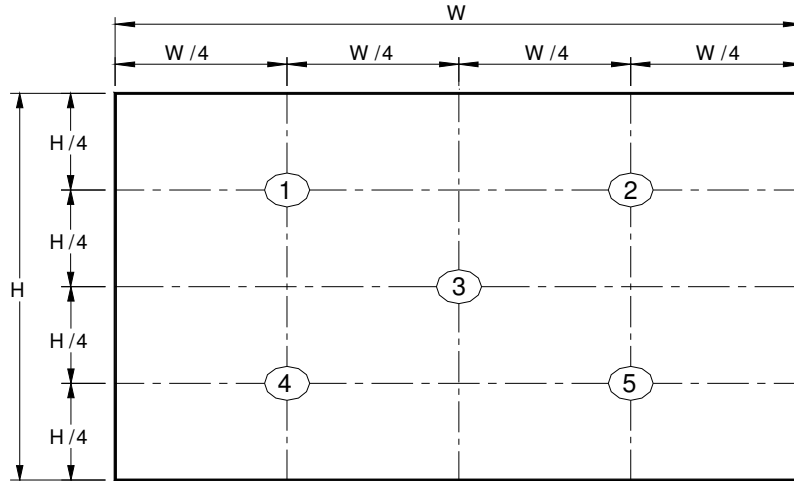
Surface Treatment		Anti-Glare, Hardness 3H,
Support Color		262K colors ( RGB 6-bit )
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

## 2.2 Optical Characteristics

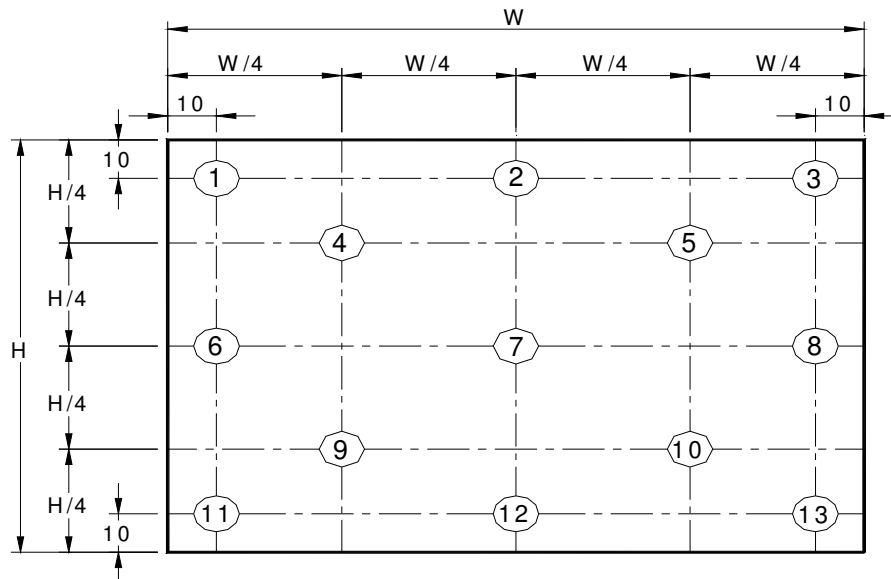
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I <sub>LED</sub> =20mA			5 points average	185	220	-	cd/m <sup>2</sup>	1, 4, 5.
Viewing Angle		$\theta_R$	Horizontal (Right) CR = 10 (Left)	40	45	-	degree	4, 9
		$\theta_L$		40	45	-		
		$\phi_H$	Vertical (Upper) CR = 10 (Lower)	10	15	-		
		$\phi_L$		30	35	-		
Luminance Uniformity		$\delta_{5P}$	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		$\delta_{13P}$	13 Points	-	-	1.6		2, 3, 4
Contrast Ratio		CR		-	400	-		4, 6
Cross talk		%				4		4, 7
Response Time		T <sub>r</sub>	Rising	-		-	msec	4, 8
		T <sub>f</sub>	Falling	-		-		
		T <sub>RT</sub>	Rising + Falling	-	8	16		
Color / Chromaticity Coordinates	Red	R <sub>x</sub>	CIE 1931	0.537	0.567	0.597	-	4
		R <sub>y</sub>		0.304	0.334	0.364		
	Green	G <sub>x</sub>		0.300	0.330	0.360		
		G <sub>y</sub>		0.539	0.569	0.599		
	Blue	B <sub>x</sub>		0.125	0.155	0.185		
		B <sub>y</sub>		0.106	0.136	0.166		
	White	W <sub>x</sub>		0.283	0.313	0.343		
		W <sub>y</sub>		0.299	0.329	0.359		
NTSC		%		-	45	-		

**Note 1:** 5 points position (Ref: Active area)



**Note 2:** 13 points position (Ref: Active area)



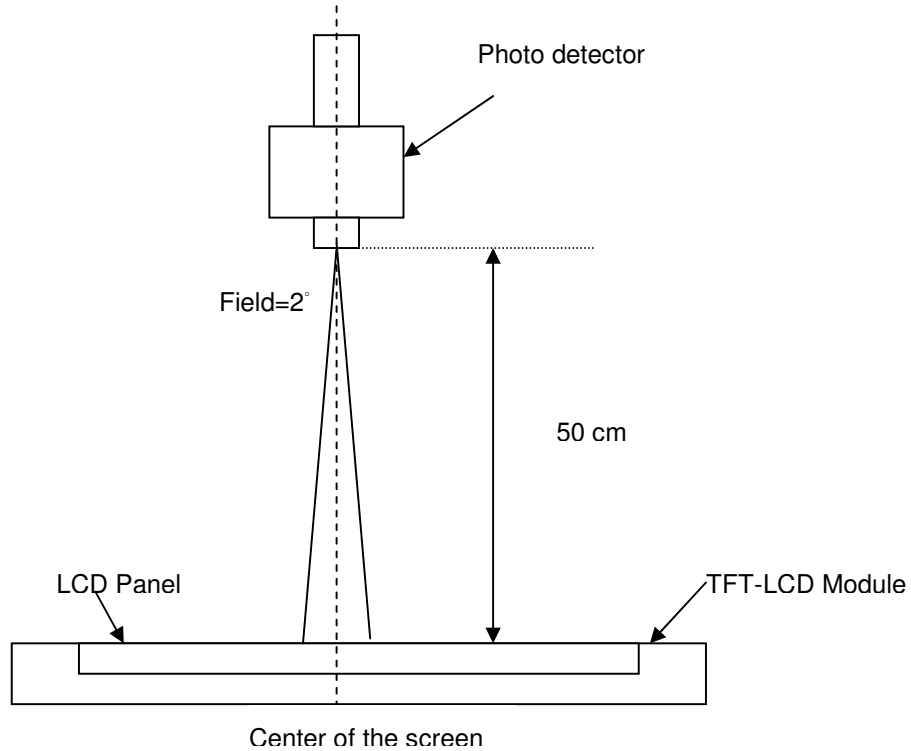
**Note 3:** The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

## Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



## Note 5 : Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 63 at 5 points ·  $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$  is corresponding to the luminance of the point X at Figure in Note (1).

## Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

## Note 7 : Definition of Cross Talk (CT)

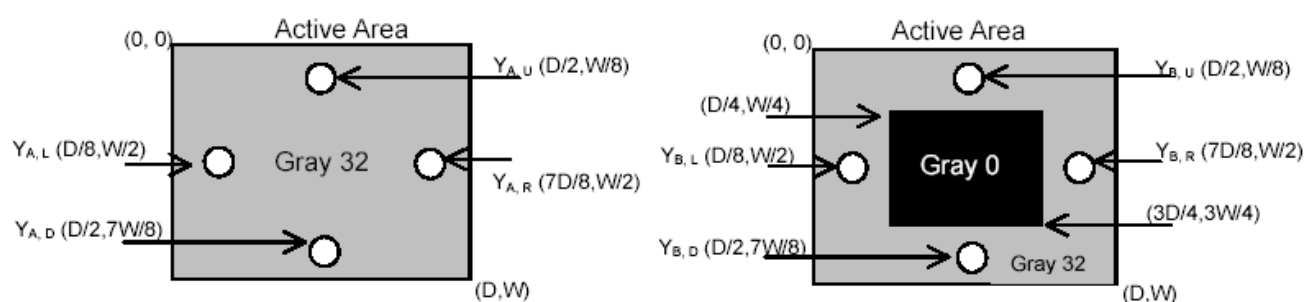
$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$



Where

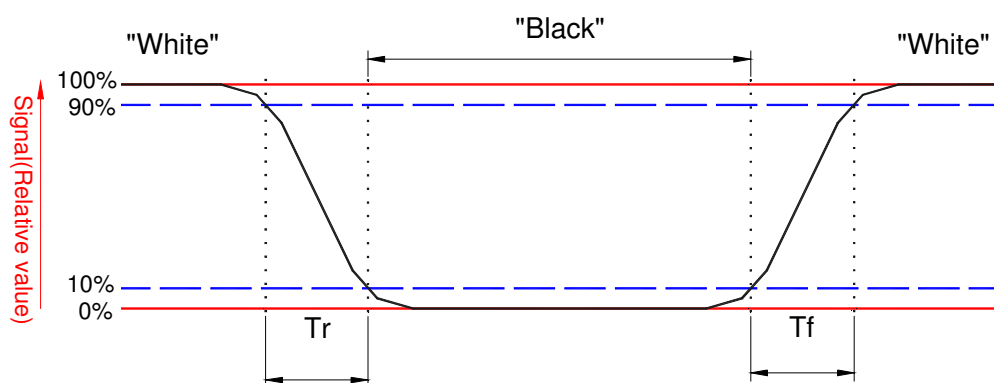
$Y_A$  = Luminance of measured location without gray level 0 pattern ( $\text{cd/m}^2$ )

$Y_B$  = Luminance of measured location with gray level 0 pattern ( $\text{cd/m}^2$ )



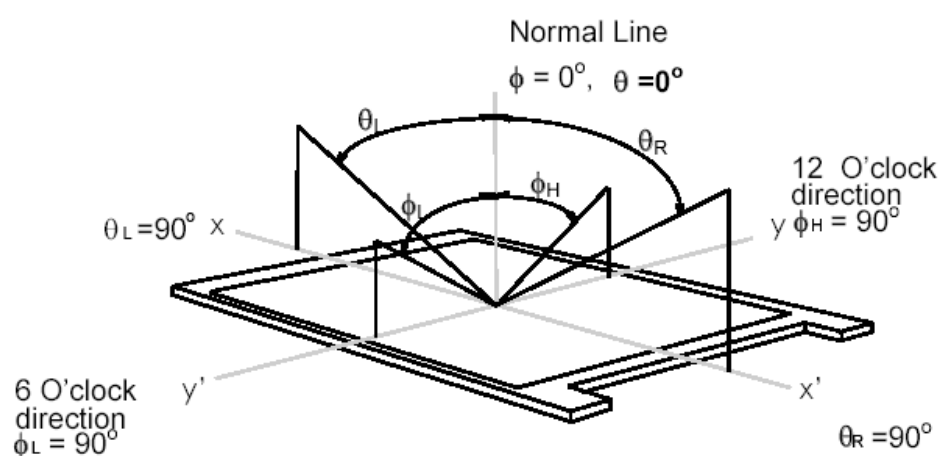
**Note 8:** Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



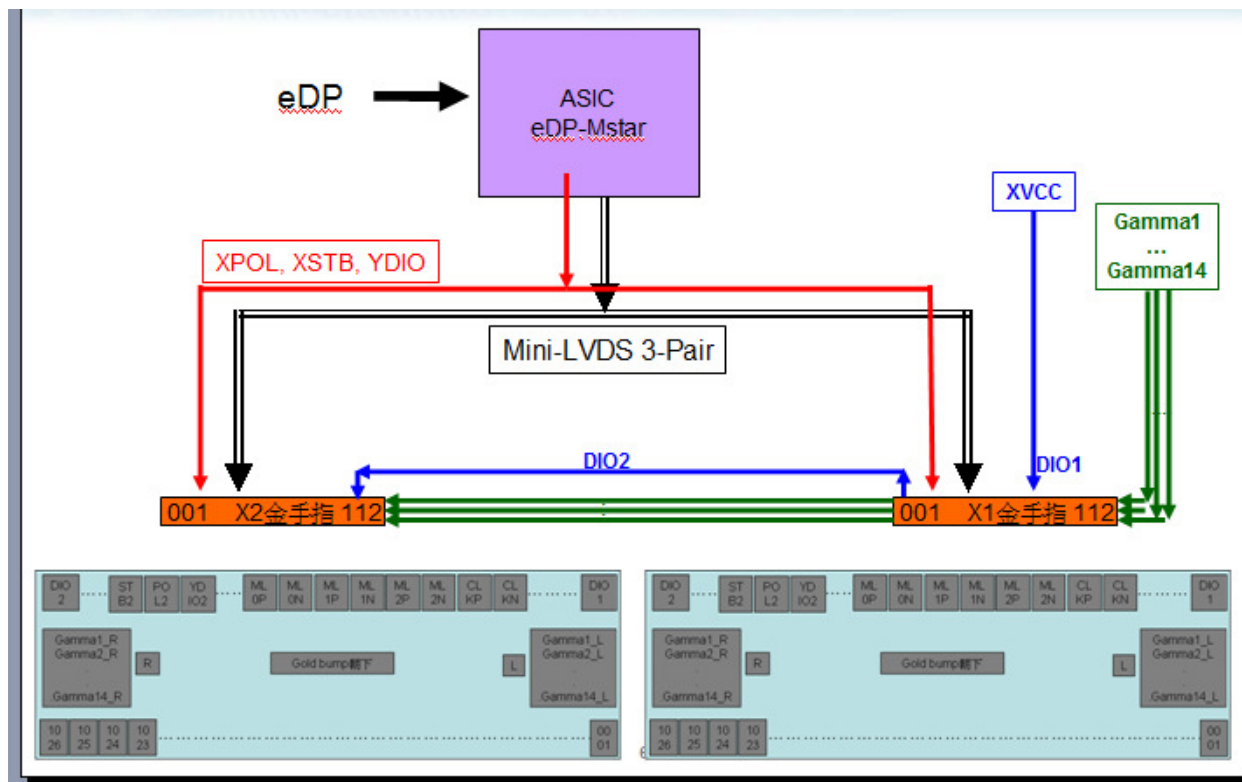
## Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a  $180^\circ$  horizontal and  $180^\circ$  vertical range (off-normal viewing angles). The  $180^\circ$  viewing angle range is broken down as follows;  $90^\circ$  ( $\theta$ ) horizontal left and right and  $90^\circ$  ( $\Phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



## 3. Functional Block Diagram

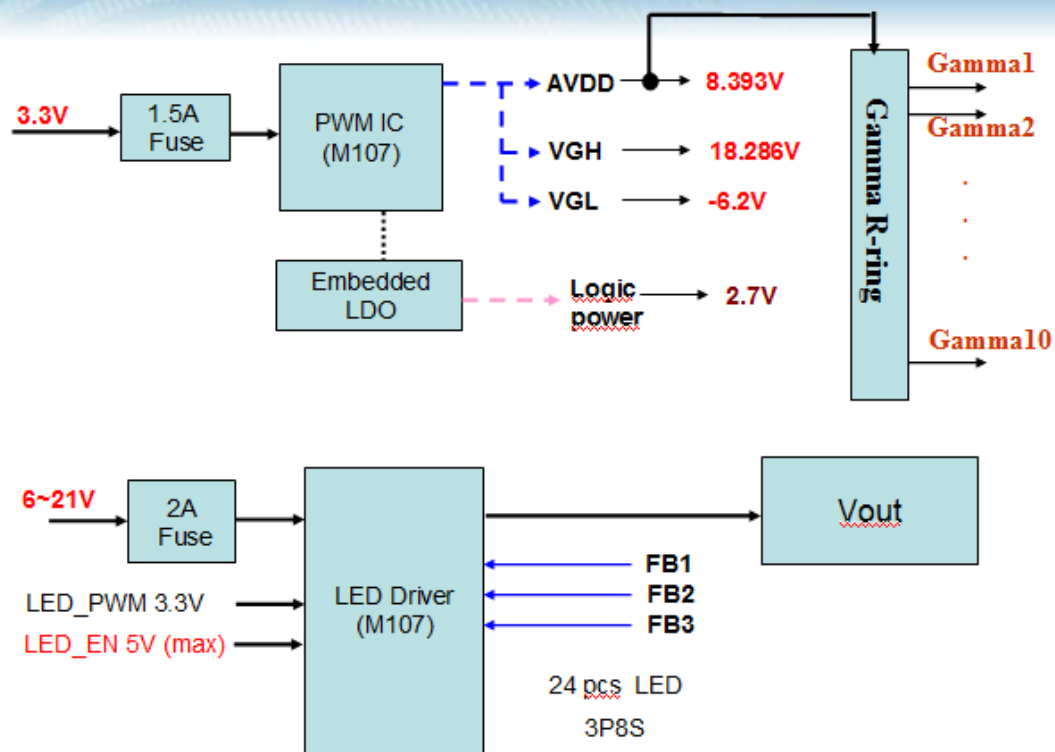
The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 40 Pin one channel Module





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### 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

#### 4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

#### 4.2 Absolute Ratings of Environment

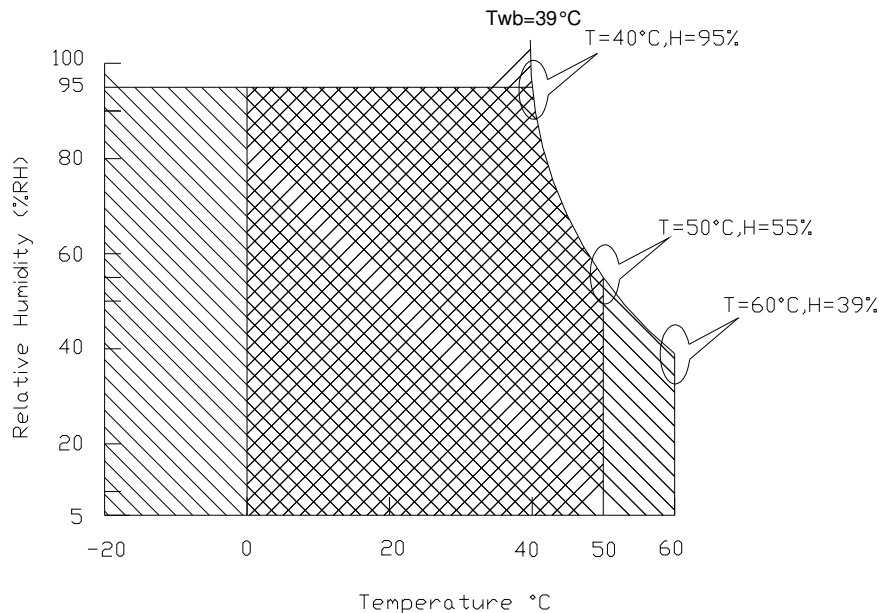
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C )

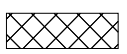
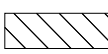
Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

## 5. Electrical Characteristics

### 5.1 TFT LCD Module

#### 5.1.1 Power Specification

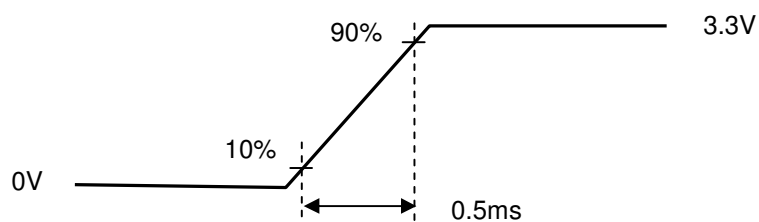
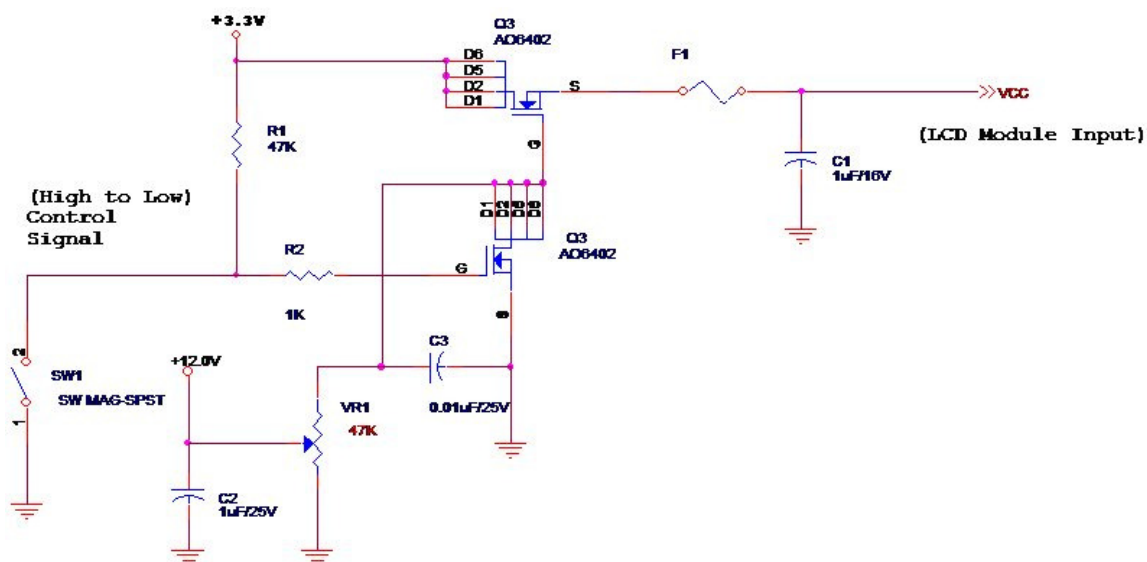
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.8	[Watt]	Note 1
IDD	IDD Current	-	-	242	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ( $P_{max}=V_{3.3} \times I_{black}$ )

Note 2 : Measure Condition



## 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

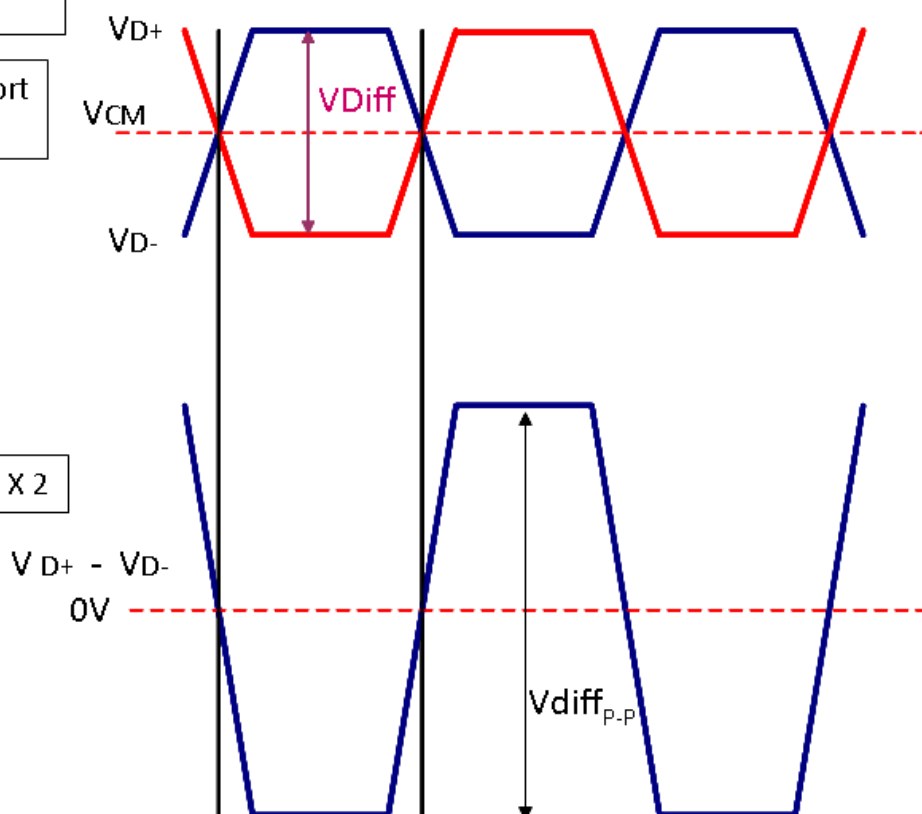
Signal electrical characteristics are as follows;

### Display Port main link signal:

Differential pair VD+ , VD-  
Which is one Display port  
Main link

VCM of Display port  
Main link

$$V_{diffP-P} = [(VD+) - (VD-)] \times 2$$

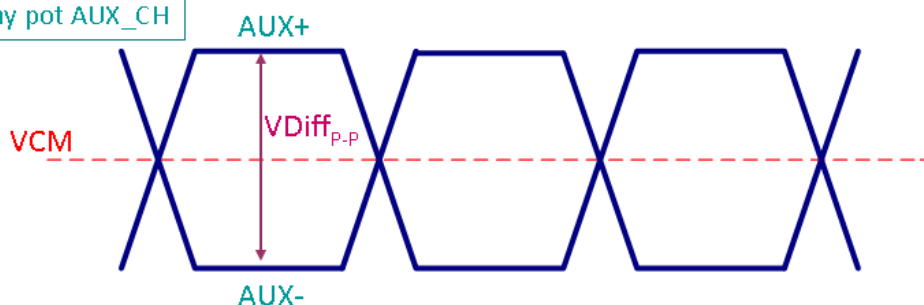


Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff <sub>P-P</sub>	Peak-to-peak Voltage at a receiving Device	120		1320	mV

Follow as VESA display port standard V1.2

## Display Port AUX\_CH signal:

Differential AUX+ , AUX-  
Which is Display port AUX\_CH



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff <sub>P-P</sub>	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Follow as VESA display port standard V1.2

## Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2		3.6	V

Follow as VESA display port standard V1.2





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### 5.2 Backlight Unit

#### 5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	1.95	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 IF=20 mA

**Note 1:** Calculator value for reference  $P_{LED} = V_F$  (Normal Distribution) \*  $I_F$  (Normal Distribution) / Efficiency

**Note 2:** The LED life-time define as the estimated time to 50% degradation of initial luminous.

#### 5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	200	-	2K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	



## 6.2 Integration Interface Requirement

### 6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	SMT
Type / Part Number	MSK24036P8
Mating Housing/Part Number	LED Light bar

### 6.2.2 Pin Assignment

eDP is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Signal Name	Signal Name	Pin	Signal Name	Signal Name
1	DCR_EN_IN	DCR_EN(NC)	16	LCD_GND	LCD logic and driver ground
2	H_GND	High Speed Ground	17	HPD	HPD signale pin
3	Lane1_N	Comp Signal Link Lane 1	18	BL_GND	Backlight ground
4	Lane1_P	True Signal Link Lane 1	19	BL_GND	Backlight ground
5	H_GND	High Speed Ground	20	BL_GND	Backlight ground
6	Lane0_N	Comp Signal Link Lane 0	21	BL_GND	Backlight ground
7	Lane0_P	True Signal Link Lane 0	22	BL_Enable	Backlight On / Off
8	H_GND	High Speed Ground	23	BL_PWM_DIM	System PWM signal Input
9	AUX_CH_P	True Signal Auxiliary Ch.	24	NC	Reserved for LCD manufacture's use
10	AUX_CH_N	Comp Signal Auxiliary Ch.	25	NC	Reserved for LCD manufacture's use
11	H_GND	High Speed Ground	26	BL_PWR	Backlight power
12	LCD_VCC	LCD logic and driver power	27	BL_PWR	Backlight power
13	LCD_VCC	LCD logic and driver power	28	BL_PWR	Backlight power
14	LCD_Self_Test	LCD Panel Self Test Enable	29	BL_PWR	Backlight power
15	LCD_GND	LCD logic and driver ground	30	CM_EN_IN	CM_EN(NC)

## 6.3 Interface Timing

### Timing Characteristics

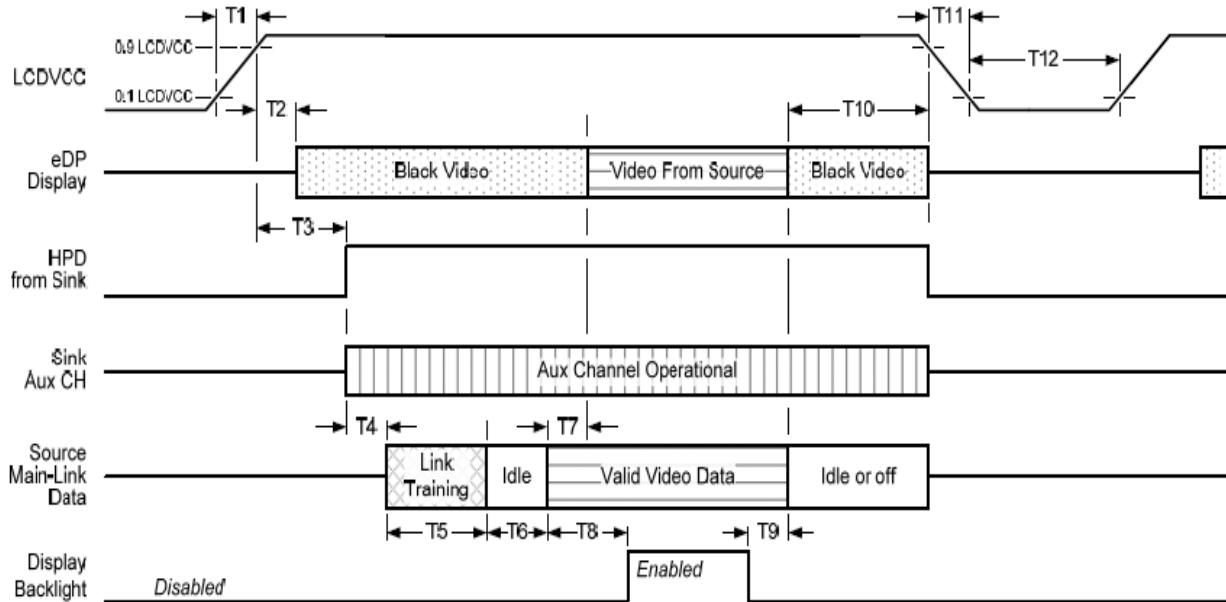
Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-		60	-	Hz
Clock frequency		1/ T <sub>Clock</sub>	66.4	TBD	80	MHz
Vertical Section	Period	T <sub>V</sub>	776	TBD	1000	T <sub>Line</sub>
	Active	T <sub>VD</sub>	768			
	Blanking	T <sub>VB</sub>	8	TBD	232	
Horizontal Section	Period	T <sub>H</sub>	1426	TBD	2000	T <sub>Clock</sub>
	Active	T <sub>HD</sub>	1366			
	Blanking	T <sub>HB</sub>	60	TBD	634	

## 6.4 Power ON/OFF Sequence

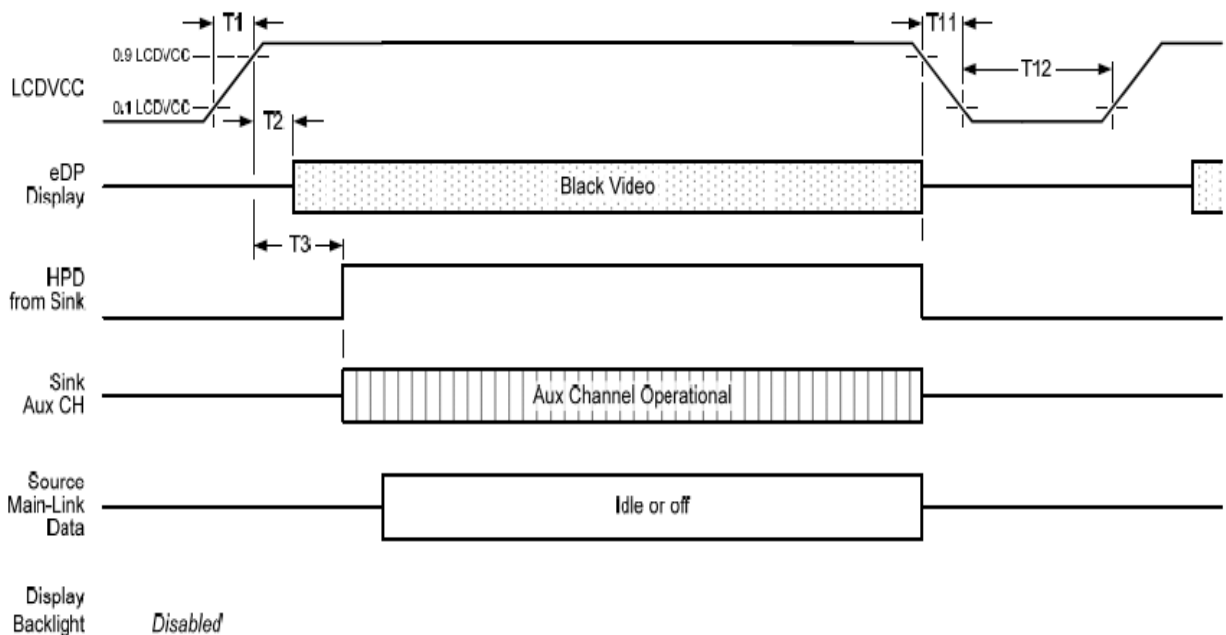
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.

### Display Port panel power sequence:



### Display port interface power up/down sequence, normal system operation

### Display Port AUX\_CH transaction only:



### Display port interface power up/down sequence, AUX\_CH transaction only



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## Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

Note 1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

- upon LCDVDD power on (within T2 max)-when the "Novideostream\_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
- when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

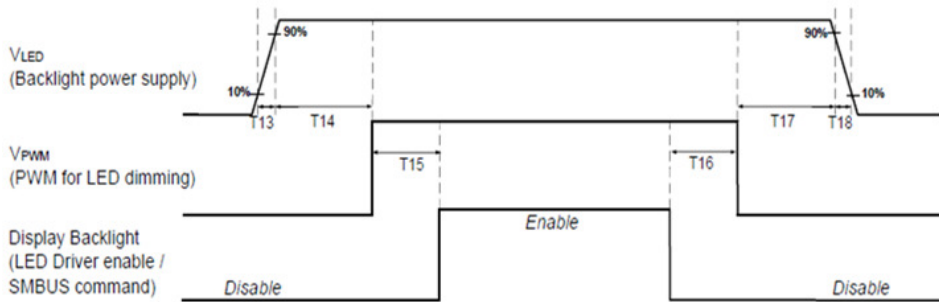
Note 3: The sink must support AUX\_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX\_CH transaction with the time specified within T3 max.



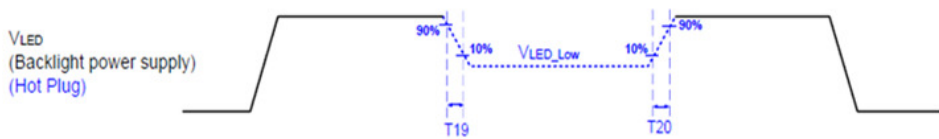
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## Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change:  $T19/T20 = 5 \times T_{PWM}^*$

\* $T_{PWM} = 1/PWM \text{ Frequency}$

## 7. Panel Reliability Test

### 7.1 Vibration Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

### 7.2 Shock Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

### 7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C , 90%RH, 300h	
High Temperature Operation	Ta= 50°C , Dry, 300h	
Low Temperature Operation	Ta= 0°C , 300h	
High Temperature Storage	Ta= 60°C , 35%RH, 300h	
Low Temperature Storage	Ta= -20°C , 50%RH, 250h	
Thermal Shock Test	Ta=-20°C to 60°C , Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

**Note1:** According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost  
 . Self-recoverable. No hardware failures.

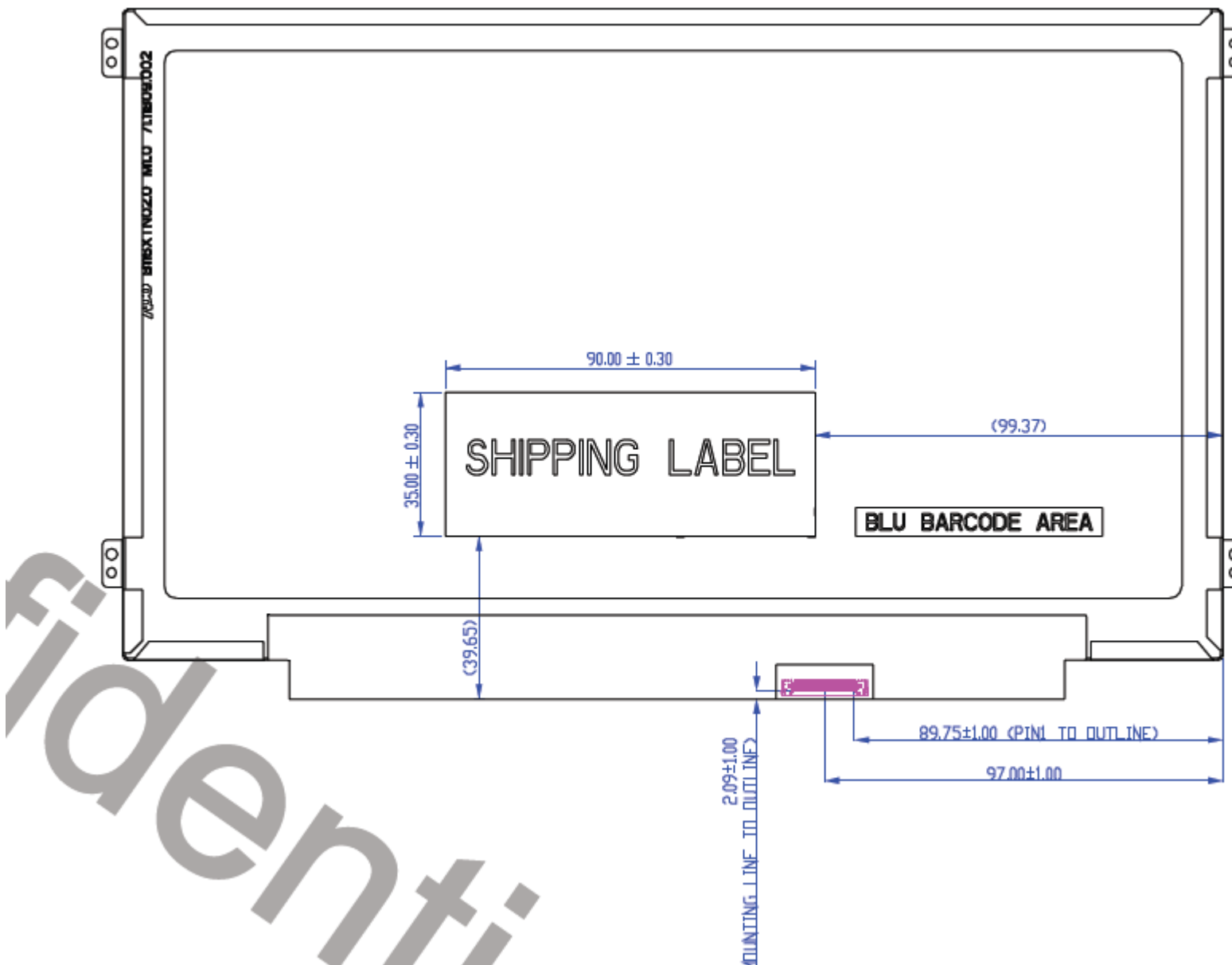
**Remark:** MTBF (Excluding the LED): 30,000 hours with a confidence level 90%



## 8. Mechanical Characteristics

### 8.1 LCM Outline Dimension










## 9. Shipping and Package

### 9.1 Shipping Label Format

#### Shipping label

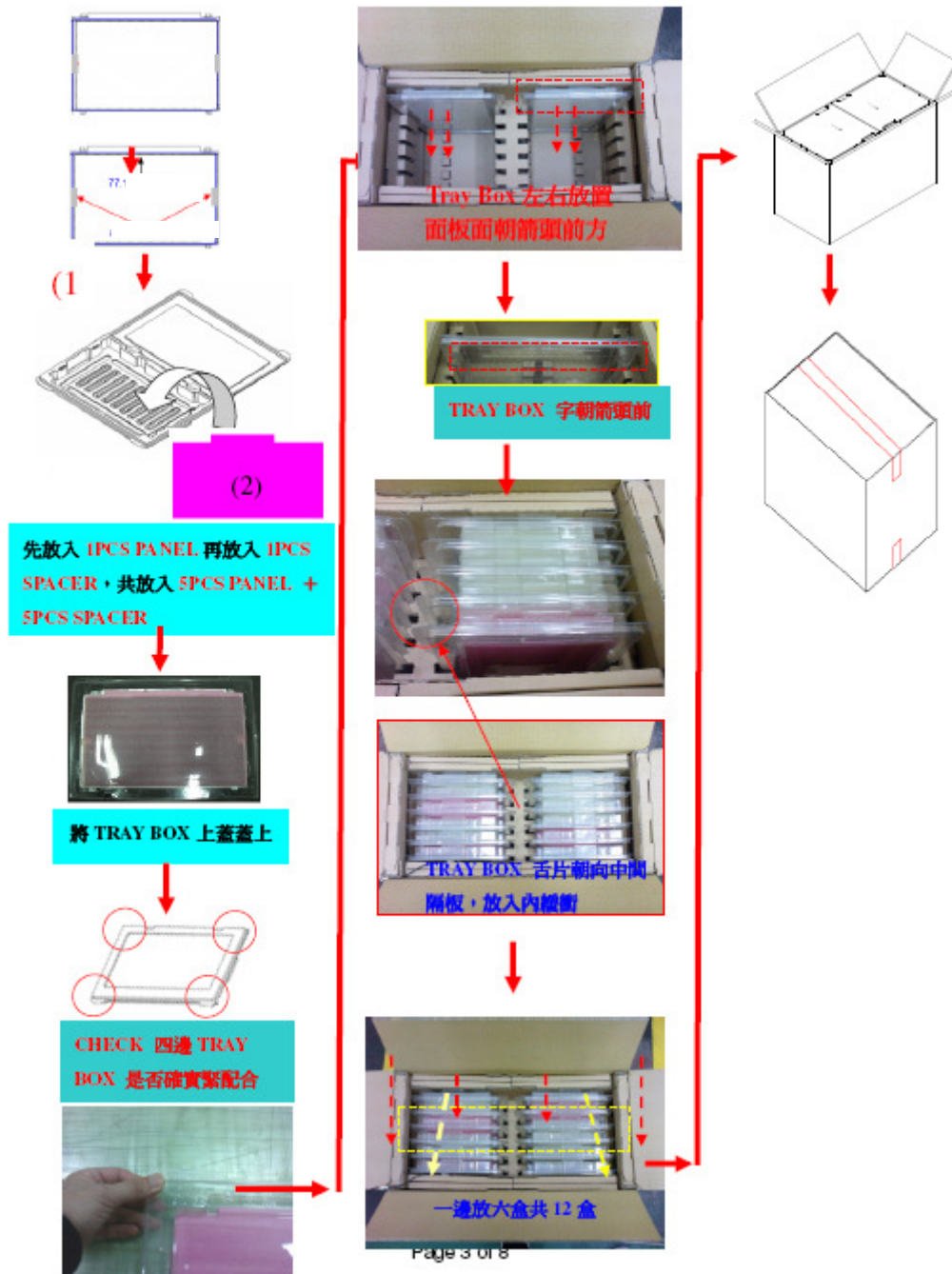
 *XXXXXXXXXXXX-XXXXXX	Manufactured YY/WW Model No: <b>B116XTN02.3</b> AU Optronics Made in China (Z30) H/W: <b>0A</b> F/W:0	   
 B116XTN02.3		

#### Carton label

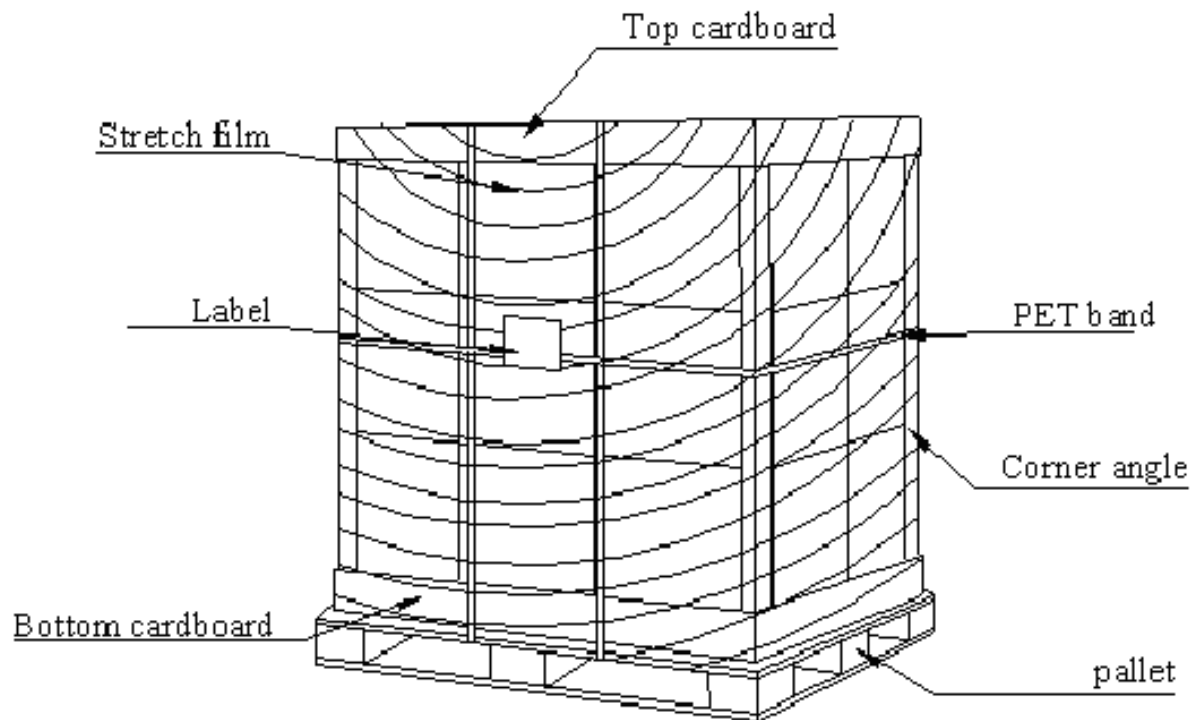
AU Optronics	QTY : 60		
MODEL NO : B116XTN02.3			
PART NO : 97.11B09.300			
CUSTOMER NO :			
CARTON NO :			
Made in China	*ZM100-0652300205*		

## 9.2 Carton Package

The outside dimension of carton is 553(L)mm\* 275(W)mm\* 379(H)mm



### 9.3 Shipping Package of Palletizing Sequence



## 10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	5C	01011100	92	
0B	hex, LSB first	23	00100011	35	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	30	00110000	48	
11	Year of manufacture	17	00010111	23	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	<b>Video input def.</b> (digital I/P, non-TMDS, CRGB)	95	10010101	149	
15	<b>Max H image size</b> (rounded to cm)	1A	00011010	26	
16	<b>Max V image size</b> (rounded to cm)	0E	00001110	14	
17	<b>Display Gamma</b> (=(gamma*100)-100)	78	01111000	120	
18	<b>Feature support</b> (no DPMS, Active OFF, RGB, tmg Blk#1)	02	00000010	2	
19	Red/green low bits ( <b>Lower 2:2:2:2 bits</b> )	6B	01101011	107	
1A	Blue/white low bits ( <b>Lower 2:2:2:2 bits</b> )	F5	11110101	245	
1B	Red x ( <b>Upper 8 bits</b> )	91	10010001	145	
1C	Red y/ higher 8 bits	55	01010101	85	
1D	Green x	54	01010100	84	
1E	Green y	91	10010001	145	
1F	Blue x	27	00100111	39	
20	Blue y	22	00100010	34	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	CE	11001110	206	
37	Pixel Clock/10000 USB	1D	00011101	29	
38	Horz active <b>Lower 8bits</b>	56	01010110	86	
39	Horz blanking <b>Lower 8bits</b>	E2	11100010	226	
3A	HorzAct:HorzBlnk <b>Upper 4:4 bits</b>	50	01010000	80	
3B	Vertical Active <b>Lower 8bits</b>	00	00000000	0	
3C	Vertical Blanking <b>Lower 8bits</b>	1E	00011110	30	