




Product Specification

AU OPTRONICS CORPORATION

() Preliminary Specifications

(V) Final Specifications

Module	11.6" SD 16:9 Color TFT-LCD
Model Name	B116AW02 V0
Note ()	LED Backlight with driving circuit design

Customer	Date
<u>All</u>	<u>7/15/2009</u>
Checked & Approved by	Date
_____	_____
Note: This Specification is subject to change without notice.	

Approved by	Date
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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2009/05/06	All	First Edition for Customer		
0.2 2009/07/02	5	Weight 235g max	Weight 255g max	
0.3 2009/07/03	24~25		Update drawing	
	26	HW code control table (Raydium : 1A)	Cancel Raydium IC (1A)	
1.0 2009/07/15	28~31		Update EDID	

1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B116AW02 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support 1024(H) x 600(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B116AW02 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	293.88(11.57")			
Active Area	[mm]	256.05(H) X 144.0(V)			
Pixels H x V		1024x3(RGB) x 600			
Pixel Pitch	[mm]	0.25005 (H) x 0.24 (V)			
Pixel Arrangement		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance Note: I _{LED} is LED current	[cd/m ²]	200 typ (Note1)			
Luminance Uniformity (5P)		1.25 max			
Contrast Ratio		500 typ			
Response Time	[ms]	16 typ, 25 max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption (max)	[Watt]	2.7@ Black Pattern / V_{in} = 12V 2.8@ Black Pattern / V_{in} = 5V			
Weight	[Grams]	255 max.			
Physical Size	[mm]		L	W	T
		Max	268.5	162.0	5.2
		Typical	268.0	161.5	-
		Min	267.5	161.0	-
Electrical Interface		1 channel LVDS			
Glass Thickness	[mm]	0.5			



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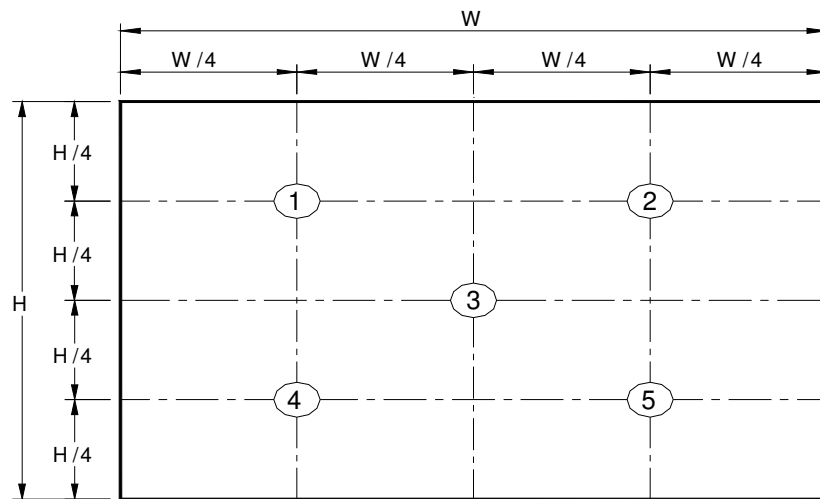
Surface Treatment		Glare
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

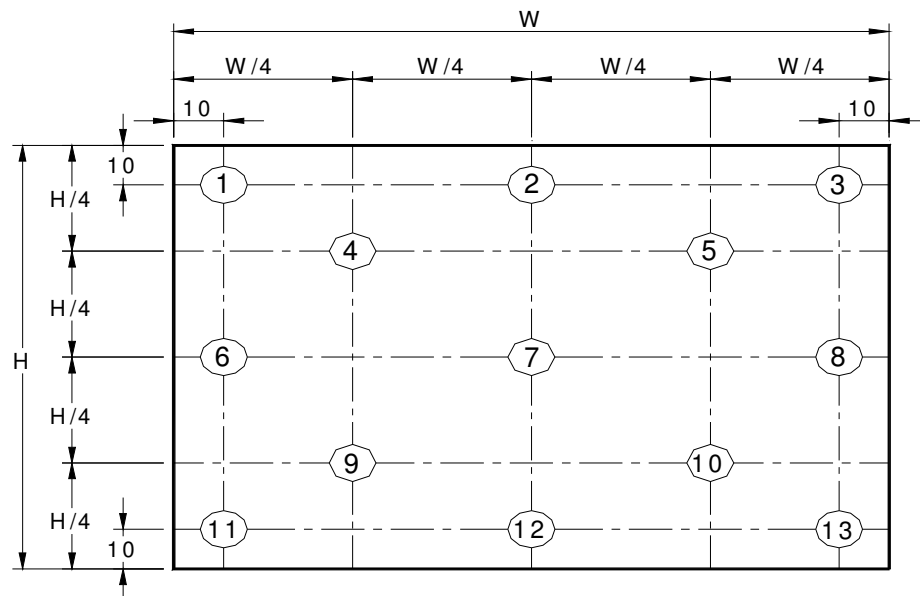
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=20mA			5 points average	170	200	-	cd/m ²	1, 4, 5
Viewing Angle		θ_R	Horizontal (Right)	40	45	-	degree	4, 9
		θ_L	CR = 10 (Left)	40	45	-		
		ϕ_H	Vertical (Upper)	10	15	-		
		ϕ_L	CR = 10 (Lower)	30	35	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio		CR		400	500	-		4, 6
Cross talk		%						4, 7
Response Time		T_r	Rising	-	12	17	msec	4, 8
		T_f	Falling	-	4	8		
		T_{RT}	Rising + Falling	-	16	25		
Color / Chromaticity Coordinates	Red	Rx	CIE 1931	0.550	0.580	0.61		4
		Ry		0.315	0.345	0.375		
	Green	Gx		0.295	0.325	0.355		
		Gy		0.520	0.550	0.580		
	Blue	Bx		0.125	0.155	0.185		
		By		0.110	0.130	0.160		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
		NTSC		%	-	45		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



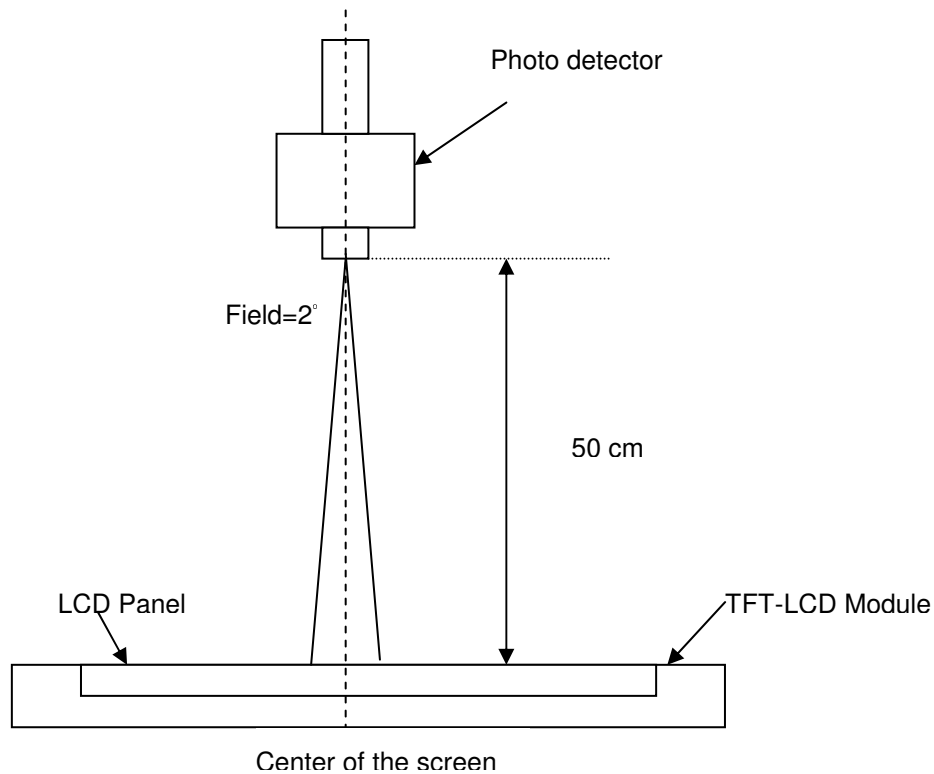
Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

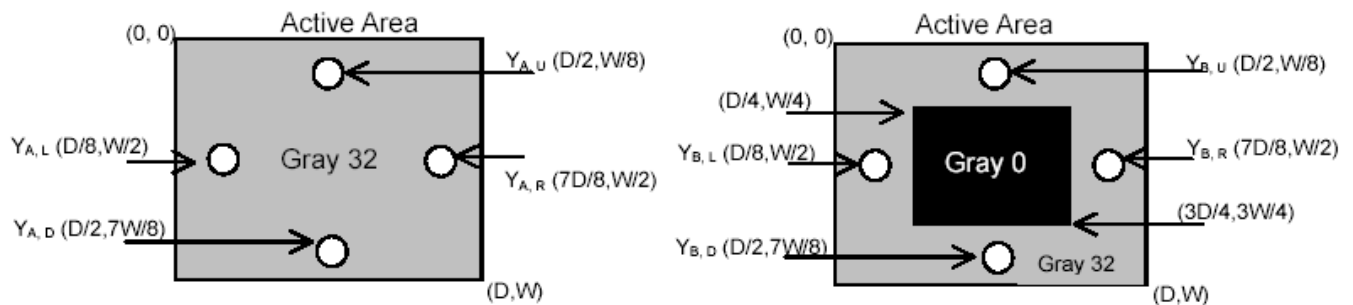
Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

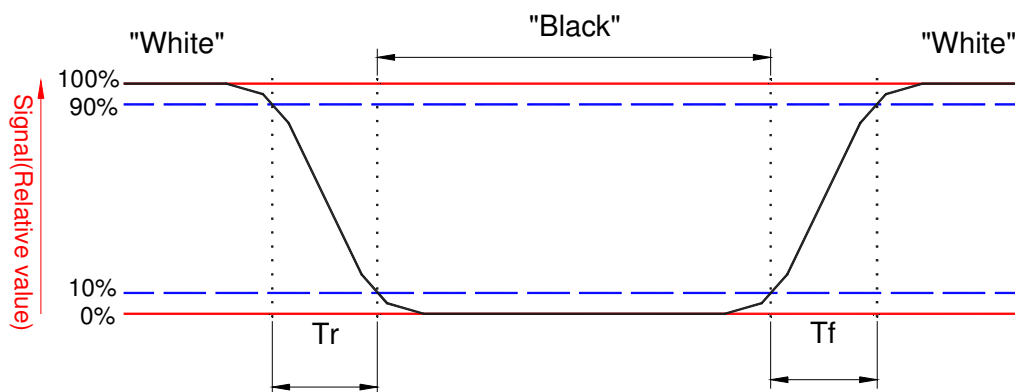
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



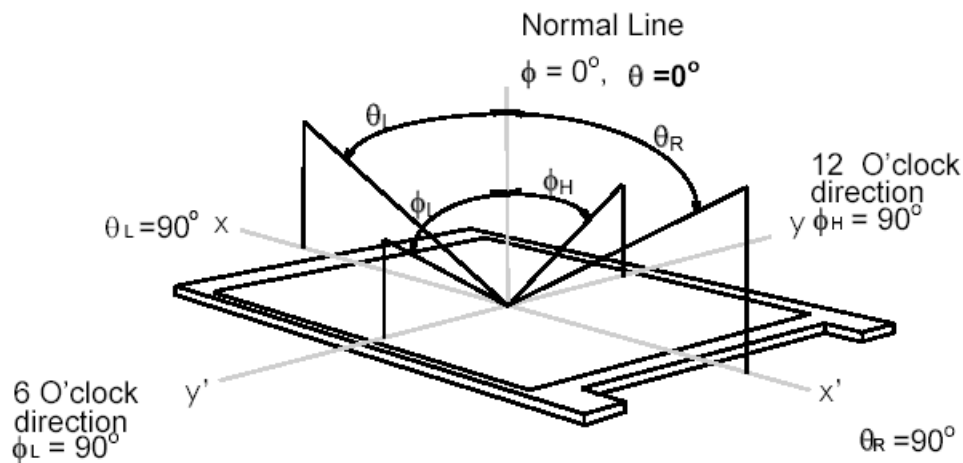
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



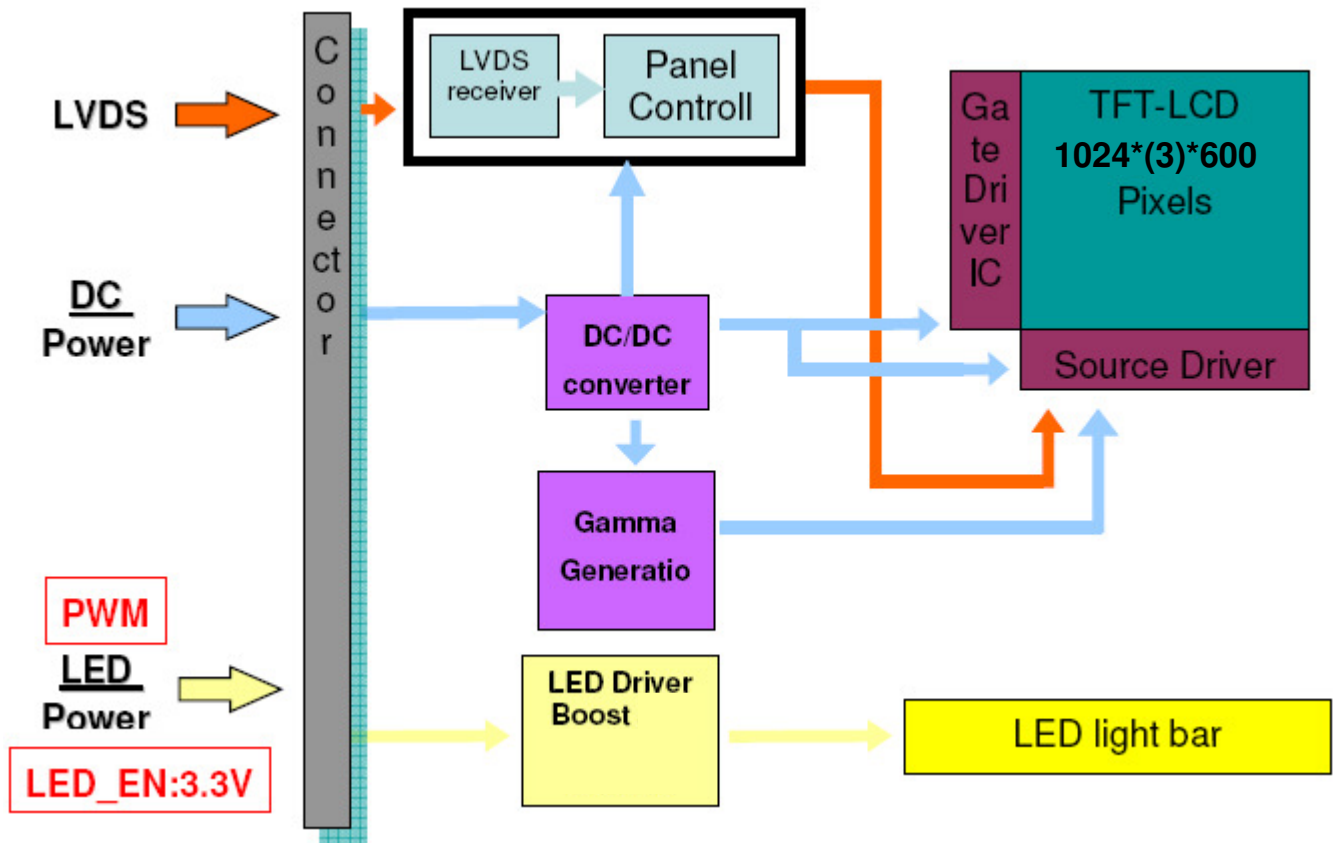
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (ϕ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 40 Pin (One ch/connector Module).



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V _{in}	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

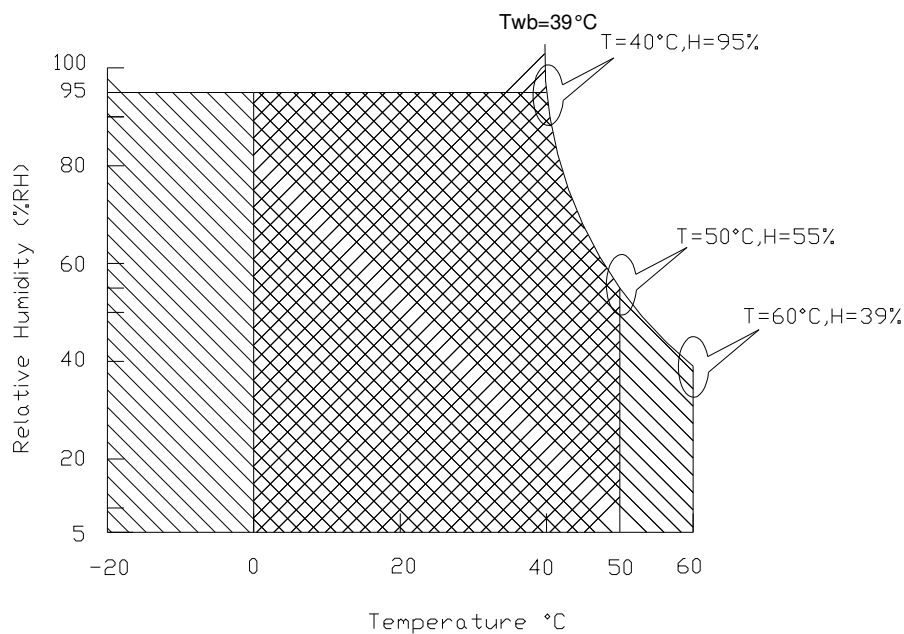
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

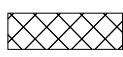
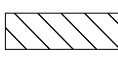
Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

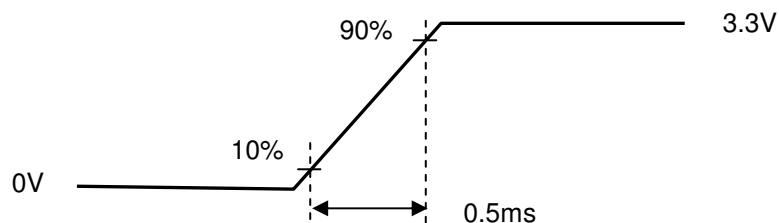
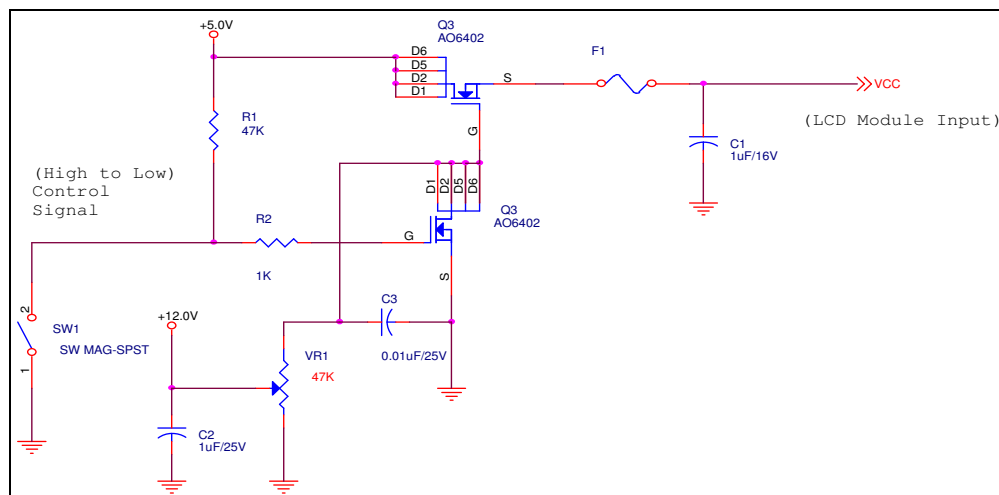
Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Unit	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.55	[Watt]	Note 1/2
IDD	IDD Current	-	-	180	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Typical Measurement Condition: Mosaic Pattern

Note 3 : Measure Condition



Vin rising time

5.1.2 Signal Electrical Characteristics

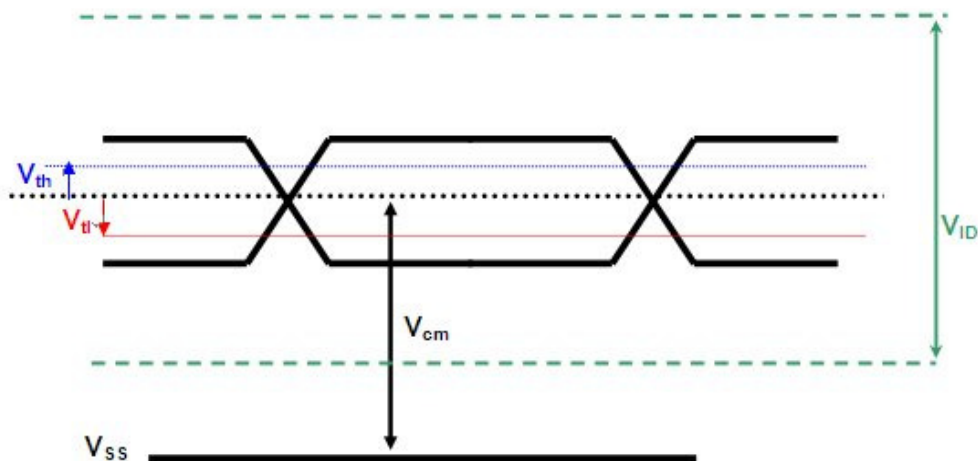
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of SN75LVDS82DGG (Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{th}	Differential Input High Threshold ($V_{cm}=+1.2V$)		100	[mV]
V_{tl}	Differential Input Low Threshold ($V_{cm}=+1.2V$)	-100	-	[mV]
V_{ID}	Differential Input Voltage	100	600	[mV]
V_{cm}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.15	[Watt]	(Ta=25°C), Note 1 Type I, V_{in} =12V
		-	-	2.25	[Watt]	(Ta=25°C), Note 1 Type II, V_{in}=5V
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25°C), Note 2 I _F =20 mA

Note 1: Calculator value for reference $P_{LED} = V_F \text{ (Normal Distribution)} * I_F \text{ (Normal Distribution)} / \text{Efficiency}$

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous

Note 3: This panel will support lower duty ratio at PWM conditional frequency. The PWM frequency constrain between 100 Hz to 300 Hz and a same typical 200Hz. The duty ratio support from 5% to 100%.

5.2.2 Backlight input signal characteristics

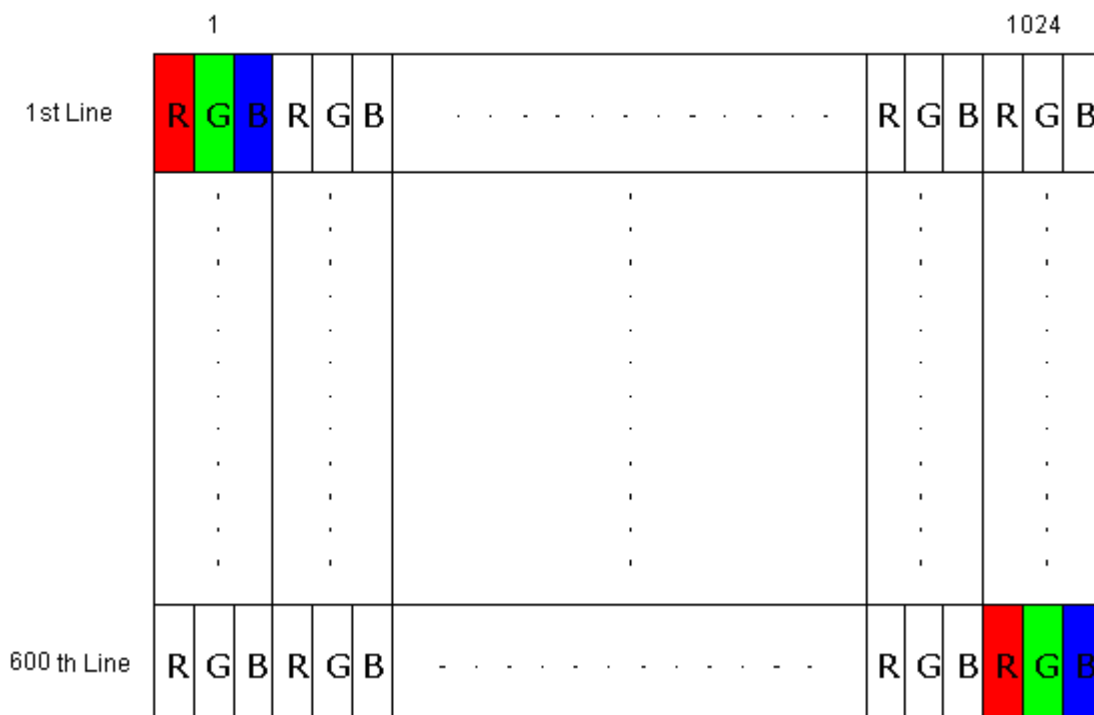
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Type I, Note 1
		4.5	5	5.5	[Volt]	Type II, Note 1
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	PWM Frequency <500 Hz PWM Frequency ≥500 Hz
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	100	-	1K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	
PWM Duty Ratio	Duty	15	--	100	%	

Note 1: **Type I** and **II** is an independent of design parameter. It should be separated from system design.

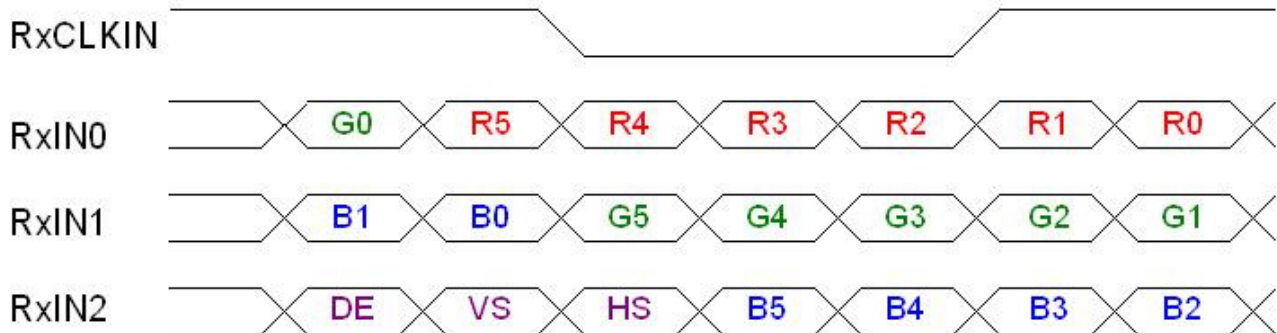
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The typical frequency is 54.2MHZ. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20455-040E-12 or compatible
Mating Housing/Part Number	IPEX 20453-040T-11 or compatible

6.3.2 Pin Assignment

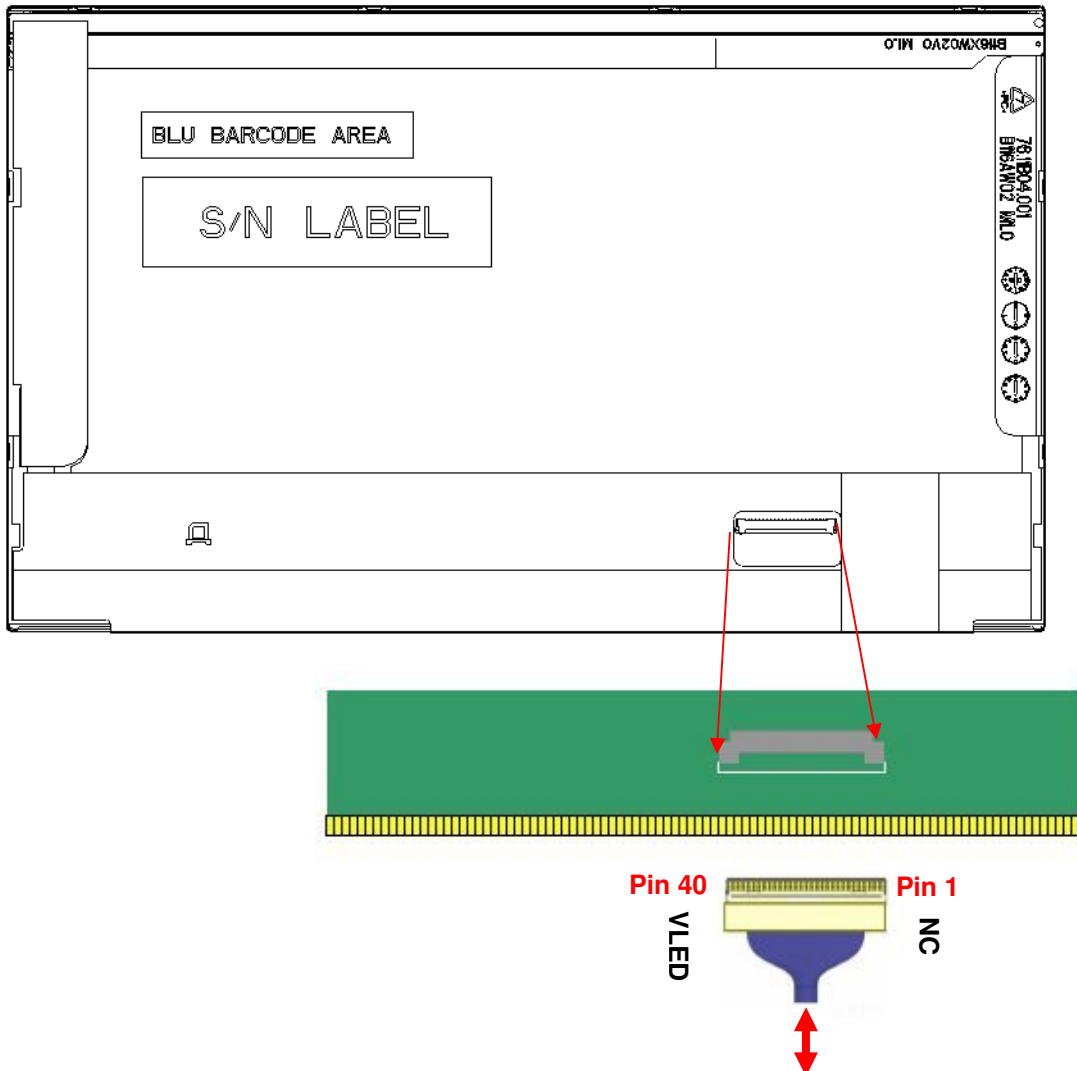
LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Signal	Description
1	NC	No Connection (Reserve)
2	AVDD	Power Supply +3.3V
3	AVDD	Power Supply +3.3V
4	VEDID	EDID +3.3V Power
5	NC	No Connection (Reserve)
6	CLK_EDID	EDID Clock Input
7	DAT_EDID	EDID Data Input
8	Rin0-	-LVDSdifferential data input(R0-R5,G0)
9	Rin0+	+LVDSdifferential data input(R0-R5,G0)
10	GND	Ground
11	Rin1-	-LVDSdifferential data input(G1-G5,B0-B1)
12	Rin1+	+LVDSdifferential data input(G1-G5,B0-B1)
13	GND	Ground
14	Rin2-	-LVDSdifferential data input(B2-B5,HS,VS,DE)
15	Rin2+	+LVDSdifferential data input(B2-B5,HS,VS,DE)
16	GND	Ground
17	ClkIN-	-LVDSdifferential clock input
18	ClkIN+	+LVDSdifferential clock input
19	GND	Ground–Shield
20	NC	No Connection (Reserve)
21	NC	No Connection (Reserve)
22	GND	Ground–Shield
23	NC	No Connection (Reserve)
24	NC	No Connection (Reserve)
25	GND	Ground–Shield
26	NC	No Connection (Reserve)
27	NC	No Connection (Reserve)
28	GND	Ground–Shield
29	NC	No Connection (Reserve)

30	NC	No Connection (Reserve)
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection (Reserve)
35	VPWM_EN	System PWM Logic Input Level
36	VLED_EN	LED enable input level
37	NC	No Connection (Reserve)
38	VLED	LED Power Supply
39	VLED	LED Power Supply
40	VLED	LED Power Supply

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Note1: Start from right side



Note1: Input signals shall be low or High-impedance state when VDD is off.

6.4 Interface Timing

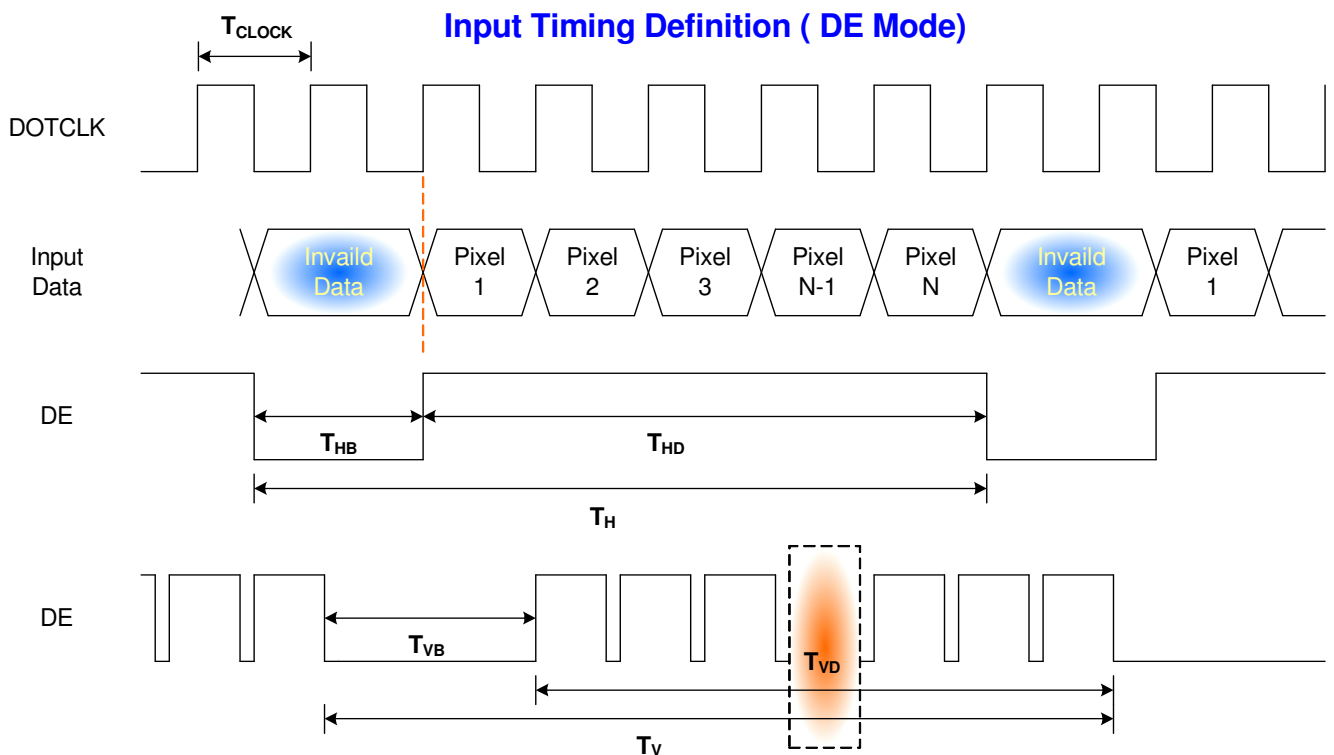
6.4.1 Timing Characteristics

Basically, interface timings should match the 1024 x 600 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-		60		Hz
Clock frequency		$1/T_{\text{Clock}}$	38.5	48.5	80	MHz
Vertical Section	Period	T_V	608	612	1023	T_{Line}
	Active	T_{VD}	600	600	600	
	Blanking	T_{VB}	8	12	423	
Horizontal Section	Period	T_H	1054	1320	2047	T_{Clock}
	Active	T_{HD}	1024	1024	1024	
	Blanking	T_{HB}	30	296	1023	

Note : DE mode only

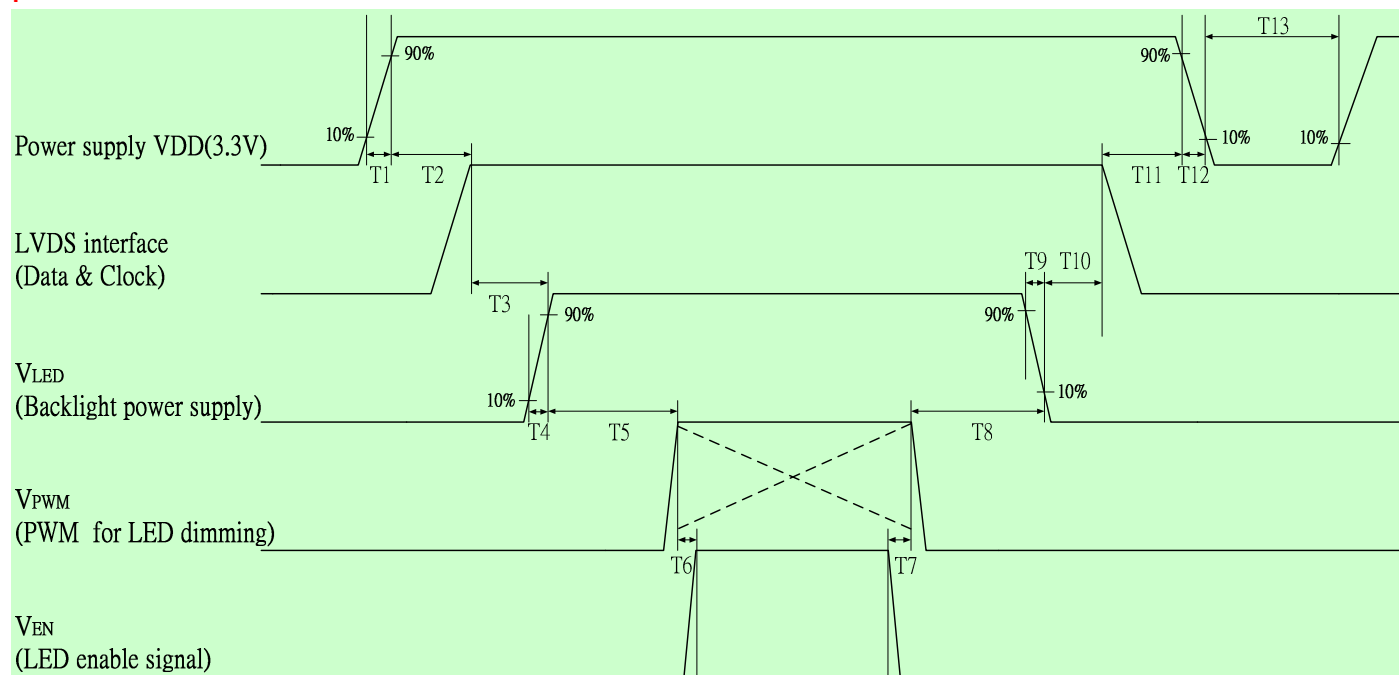
6.4.2 Timing diagram



6.5 Power Sequence

6.5.1 Panel Power Sequence

VDD power and LED on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing				
Parameter	Value			Condition
	Min.(ms)	Typ.(ms)	Max.(ms)	
T1	0.5	-	10	
T2	0	-	50	
T3	200	-	-	
T4	0.5	-	10	
T5	10	-	-	
T6	10	-	-	
T7	0	-	-	
T8	10		200	VLED=6~21V(Type I)
	10	-	-	VLED=5V(type II)
T9	0	-	10	
T10	200	-	-	
T11	0.5	-	50	
T12	0	-	10	
T13	400	-	-	

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 35%RH, 300h	
Low Temperature Storage	Ta= -20°C, 50%RH, 250h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost
 . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

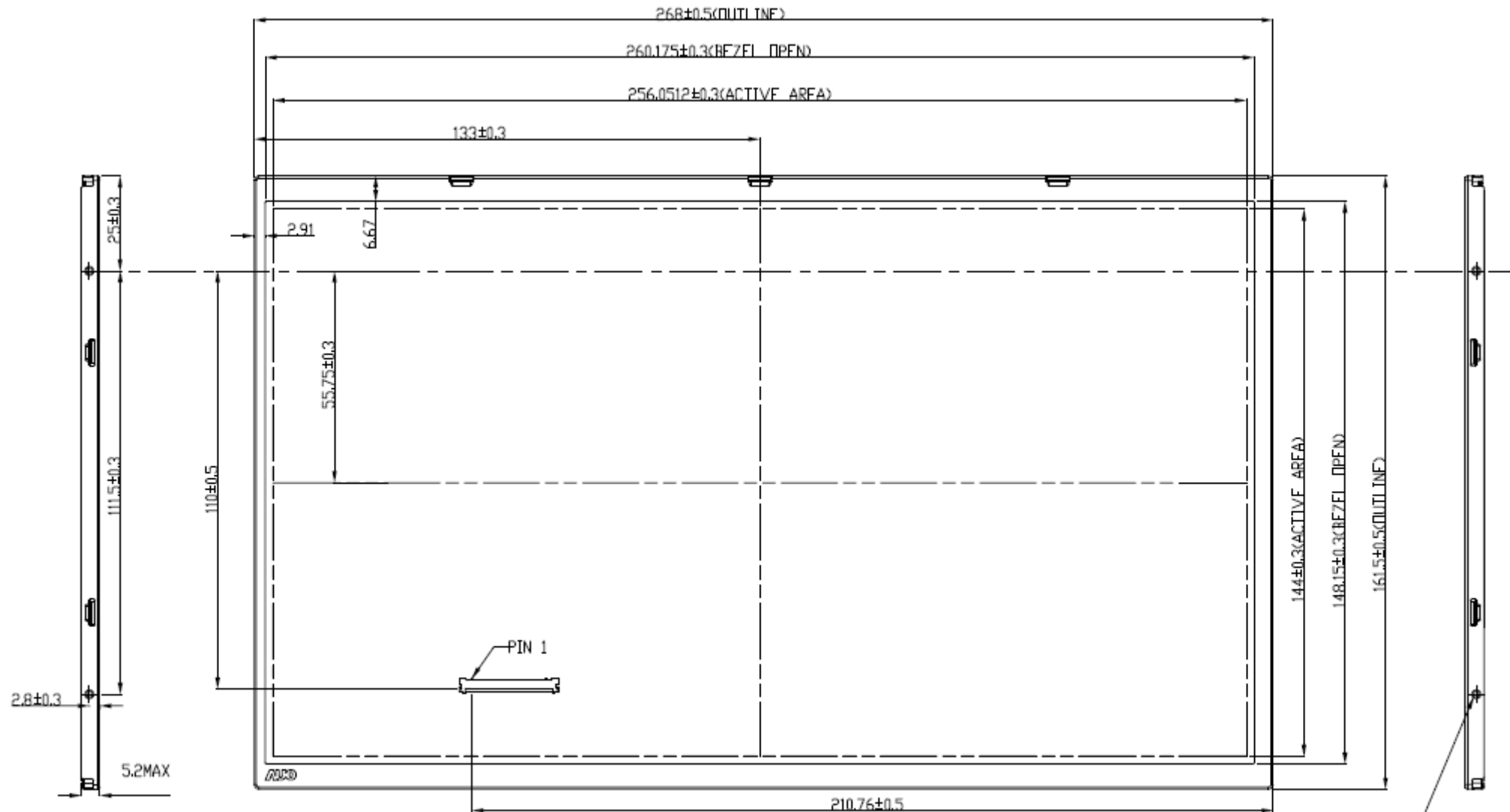


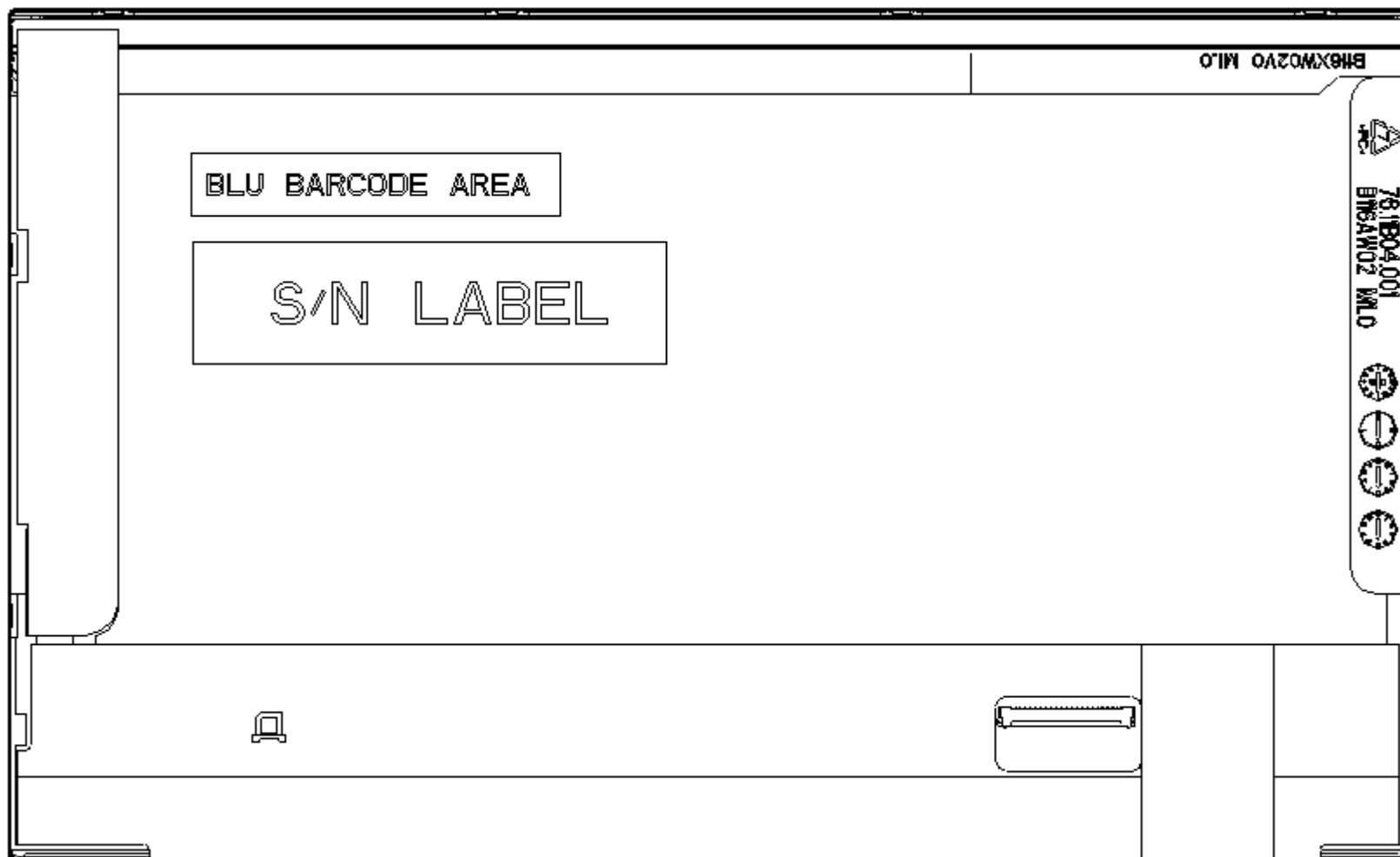
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8. Mechanical Characteristics

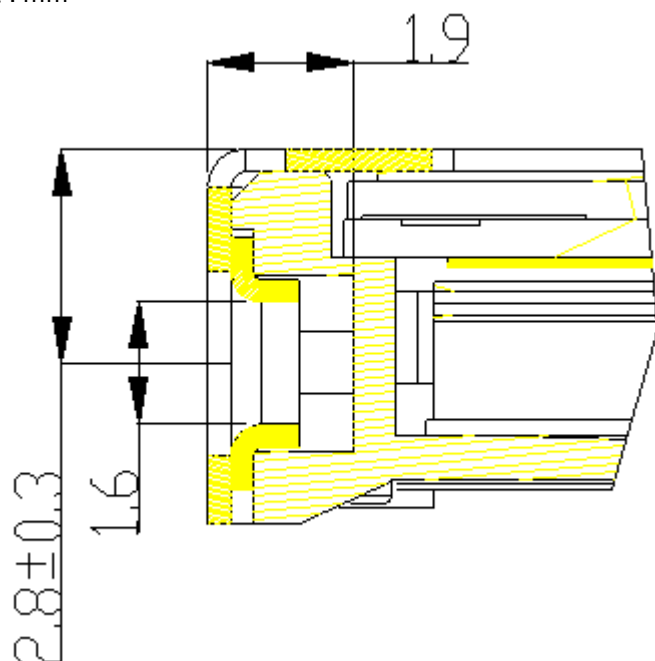
8.1 LCM Outline Dimension





8.2 Screw Hole Depth and Center Position

Unit : mm





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9. Shipping and Package

9.1 Shipping Label Format

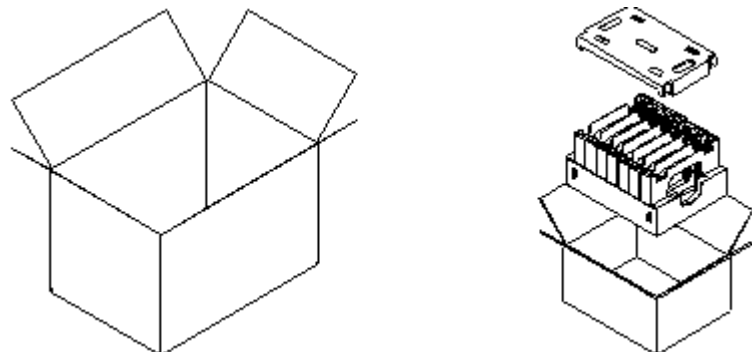


* H/W code control table :

IC Combination		H/W
Source	Novatek	0A
Gate	Novatek	

9.2 Carton package

The outside dimension of carton is 405(L)mm* 375(W)mm* 268(H)mm, carton and cushion weight are 2080g

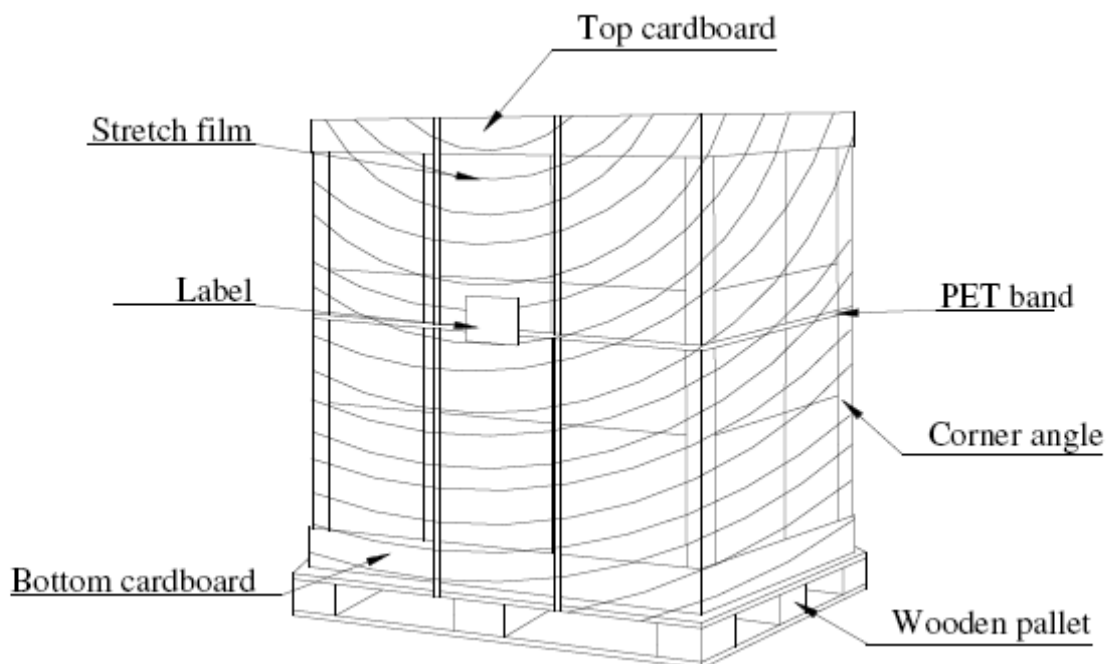


9.3 Shipping package of palletizing sequence

The outside dimension of Pallet is 114(L)mm* 89(W)mm* 13.8(H)mm

By air : 6 *5 layers, one pallet put 30 boxes, total 900 pcs module.

By sea : 6 *7 layers, one pallet put 42 boxes, total 1260 pcs module.





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10. Appendix: EDID description

B116AW02 V0 EDID Code

Address	FUNCTION	Value	Value
HEX		HEX	BIN
00	Header	00	00000000
01		FF	11111111
02		FF	11111111
03		FF	11111111
04		FF	11111111
05		FF	11111111
06		FF	11111111
07		00	00000000
08	EISA Manuf. Code LSB	06	00000110
09	Compressed ASCII	AF	10101111
0A	Product Code	52	01010010
0B	hex, LSB first	20	00100000
0C	32-bit ser #	00	00000000
0D		00	00000000
0E		00	00000000
0F		00	00000000
10	Week of manufacture	01	00000001
11	Year of manufacture	13	00010011
12	EDID Structure Ver.	01	00000001
13	EDID revision #	03	00000011
14	Video input def. (digital I/P, non-TMDS, CRGB)	80	10000000
15	Max H image size (rounded to cm)	1A	00011010
16	Max V image size (rounded to cm)	0E	00001110
17	Display Gamma $(=(\text{gamma} \times 100) - 100)$	78	01111000
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	0A	00001010
19	Red/green low bits (Lower 2:2:2:2 bits)	2B	00101011
1A	Blue/white low bits (Lower 2:2:2:2 bits)	65	01100101
1B	Red x (Upper 8 bits)	97	10010111
1C	Red y/ highER 8 bits	57	01010111
1D	Green x	55	01010101
1E	Green y	96	10010110
1F	Blue x	29	00101001
20	Blue y	21	00100001
21	White x	50	01010000
22	White y	54	01010100
23	Established timing 1	00	00000000
24	Established timing 2	00	00000000
25	Established timing 3	00	00000000



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26	Standard timing #1	01	00000001
27		01	00000001
28	Standard timing #2	01	00000001
29		01	00000001
2A	Standard timing #3	01	00000001
2B		01	00000001
2C	Standard timing #4	01	00000001
2D		01	00000001
2E	Standard timing #5	01	00000001
2F		01	00000001
30	Standard timing #6	01	00000001
31		01	00000001
32	Standard timing #7	01	00000001
33		01	00000001
34	Standard timing #8	01	00000001
35		01	00000001
36	Pixel Clock/10000 LSB	4B	01001011
37	Pixel Clock/10000 USB	14	00010100
38	Horz active Lower 8bits	00	00000000
39	Horz blanking Lower 8bits	4C	01001100
3A	HorzAct:HorzBlnk Upper 4:4 bits	41	01000001
3B	Vertical Active Lower 8bits	58	01011000
3C	Vertical Blanking Lower 8bits	26	00100110
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	20	00100000
3E	HorzSync. Offset	30	00110000
3F	HorzSync.Width	20	00100000
40	VertSync.Offset : VertSync.Width	36	00110110
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000
42	Horizontal Image Size Lower 8bits	00	00000000
43	Vertical Image Size Lower 8bits	90	10010000
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000
45	Horizontal Border (zero for internal LCD)	00	00000000
46	Vertical Border (zero for internal LCD)	00	00000000
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000
48	Detailed timing/monitor	00	00000000
49	descriptor #2	00	00000000
4A		00	00000000
4B		0F	00001111
4C		00	00000000
4D		00	00000000
4E		00	00000000
4F		00	00000000
50		00	00000000



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51		00	00000000
52		00	00000000
53		00	00000000
54		00	00000000
55		00	00000000
56		00	00000000
57		00	00000000
58		00	00000000
59		20	00100000
5A	Detailed timing/monitor	00	00000000
5B	descriptor #3	00	00000000
5C		00	00000000
5D		FE	11111110
5E		00	00000000
5F	Manufacture	41	01000001
60	Manufacture	55	01010101
61	Manufacture	4F	01001111
62		0A	00001010
63		20	00100000
64		20	00100000
65		20	00100000
66		20	00100000
67		20	00100000
68		20	00100000
69		20	00100000
6A		20	00100000
6B		20	00100000
6C	Detailed timing/monitor	00	00000000
6D	descriptor #4	00	00000000
6E		00	00000000
6F		FE	11111110
70		00	00000000
71	Manufacture P/N	42	01000010
72	Manufacture P/N	31	00110001
73	Manufacture P/N	31	00110001
74	Manufacture P/N	36	00110110
75	Manufacture P/N	41	01000001
76	Manufacture P/N	57	01010111
77	Manufacture P/N	30	00110000
78	Manufacture P/N	32	00110010
79	Manufacture P/N	20	00100000
7A	Manufacture P/N	56	01010110
7B	Manufacture P/N	30	00110000



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7C		20	00100000
7D		0A	00001010
7E	Extension Flag	00	00000000
7F	Checksum	90	10010000