Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications
(V) Final Specifications

Module	15.4” WXGA+ Color TFT-LCD
Model Name	B154PW02 V0

Customer	**Date**	**Approved by**	**Date**
Checked & Approved by		**Prepared by**	
Note: This Specification is subject to change without notice.		NBBU Marketing Division / AU Optronics corporation	

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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2006/05/22	All	First Edition for Customer		
0.2 2006/06/26	31		Add 12. Appendix: EDID	
0.3 2006/08/18	5	White luminance (I_{CCFL}=6.0mA) 230 min (5-point)	White luminance (I_{CCFL}=6.5mA) 220 min (5-point)	
0.3 2006/08/18	31		Modify 12. Appendix: EDID	
0.4 2006/08/23	31		Modify 12. Appendix: EDID	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

2. General Description

B154PW02 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA+

(1440(H) x 900(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter of backlight is included.

B154PW02 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

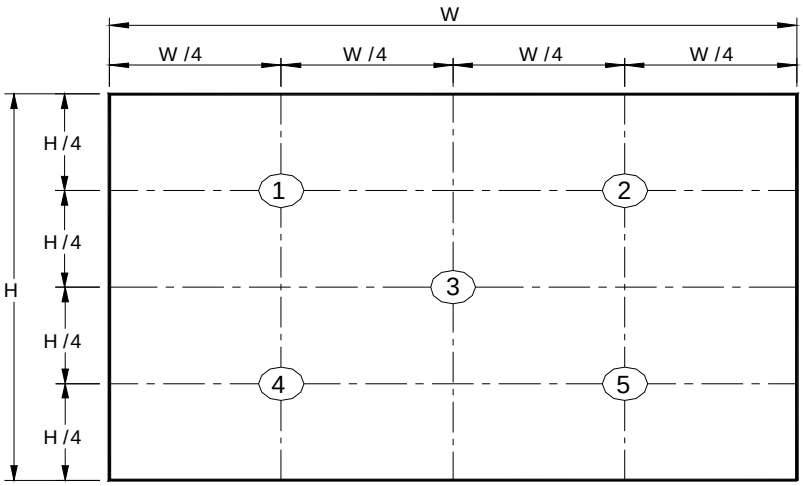
Items	Unit	Specifications
Screen Diagonal	[mm]	391 (15.4W")
Active Area	[mm]	331.2 X 207.0
Pixels H x V		1440x3(RGB) x 900
Pixel Pitch	[mm]	0.23025X0.23025
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (I_{CCFL}=6.5mA) Note: I_{CCFL} is lamp current	[cd/m^2]	250 typ. (5 points average) 220 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		400 typ
Optical Rise Time/Fall Time	[msec]	4/12 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption	[Watt]	7.5max.(with inverter)
Weight	[Grams]	550 max. (with inverter)
Physical Size	[mm]	344.0 typ. x 222.0 typ. x 6.1 max.
Electrical Interface		2 channel LVDS
Surface Treatment		Glare, Hardness 3H, Reflectance 4.3%
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [^{o}C] [^{o}C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

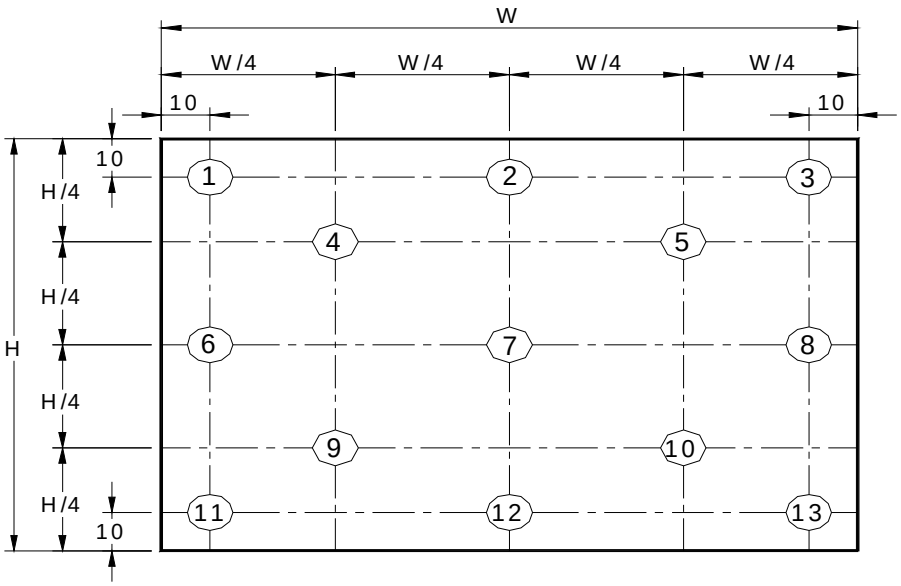
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance I_{CCFL}=6.5mA	[cd/m^2]	5 points average	220	250	-	1, 4, 5.
Viewing Angle	[degree]	Horizontal (Right) CR = 10	50	60	-	9
	[degree]	(Left)	50	60	-	
	[degree]	Vertical (Upper) CR = 10	50	60	-	
	[degree]	(Lower)	50	60	-	
Luminance Uniformity		5 Points			1.25	1
Luminance Uniformity		13 Points			1.50	2
CR: Contrast Ratio			-	400	-	6
Cross talk	%				4	7
Response Time	[msec]	Rising	-	4	8	8
	[msec]	Falling	-	12	17	
	[msec]	Rising + Falling		16	25	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.560	0.590	0.620	2,8
		Red y	0.315	0.345	0.375	
		Green x	0.285	0.315	0.345	
		Green y	0.520	0.555	0.580	
		Blue x	0.125	0.155	0.185	
		Blue y	0.115	0.145	0.175	
		White x	0.290	0.313	0.343	
		White y	0.299	0.329	0.350	

Note 1: 5 points position (Display area : 331.2mm x 207.0mm)



Note 2: 13 points position



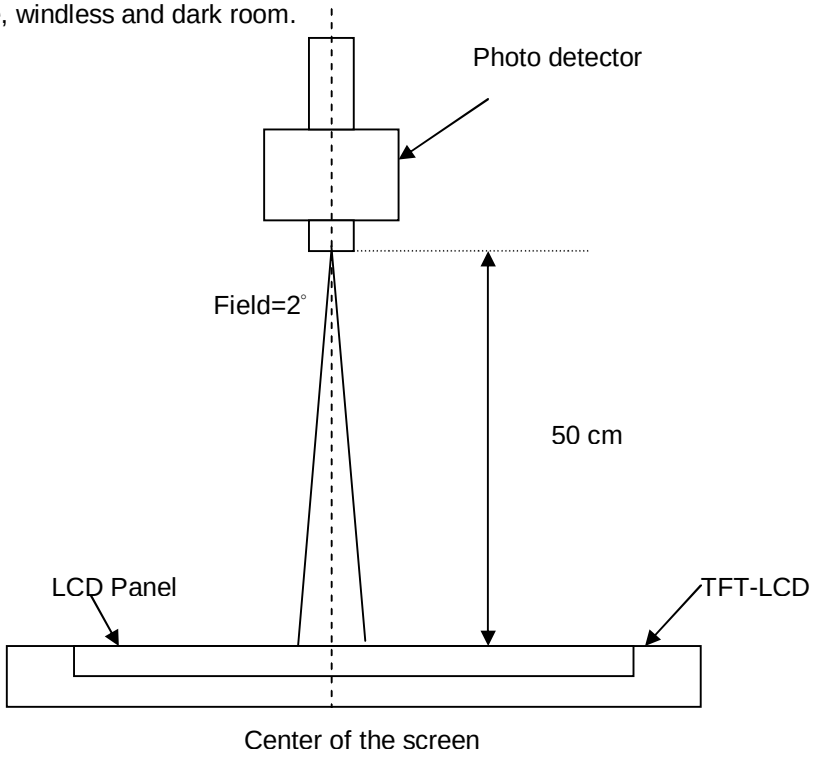
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

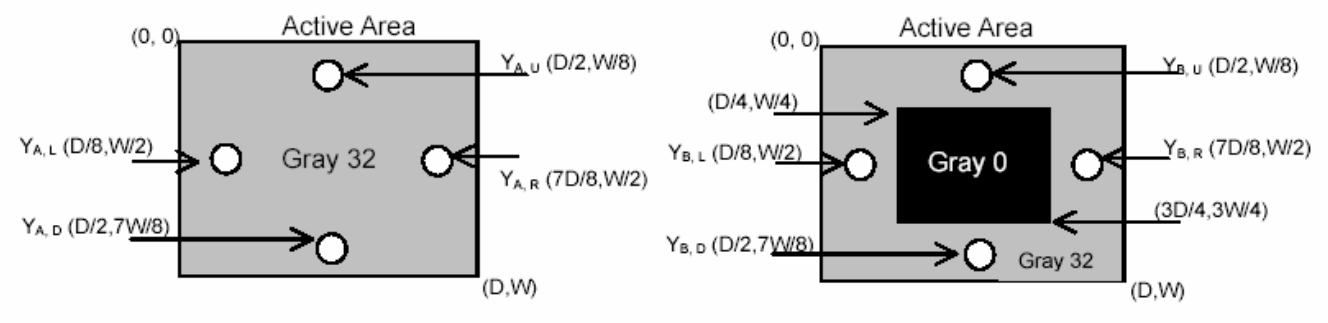
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where

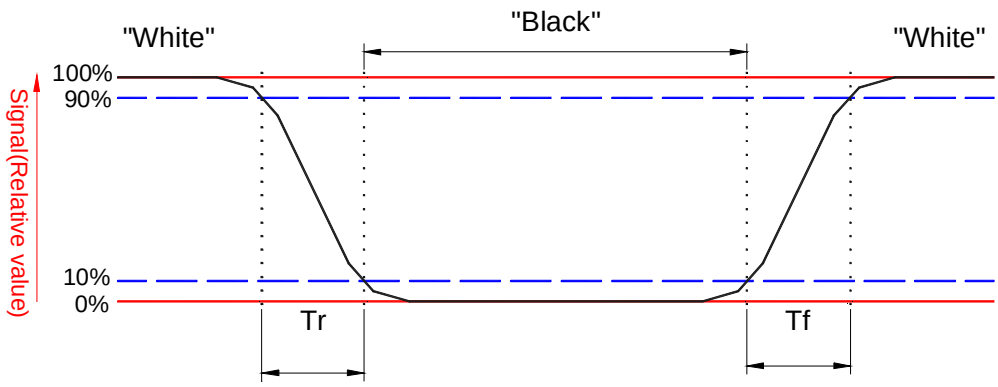
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



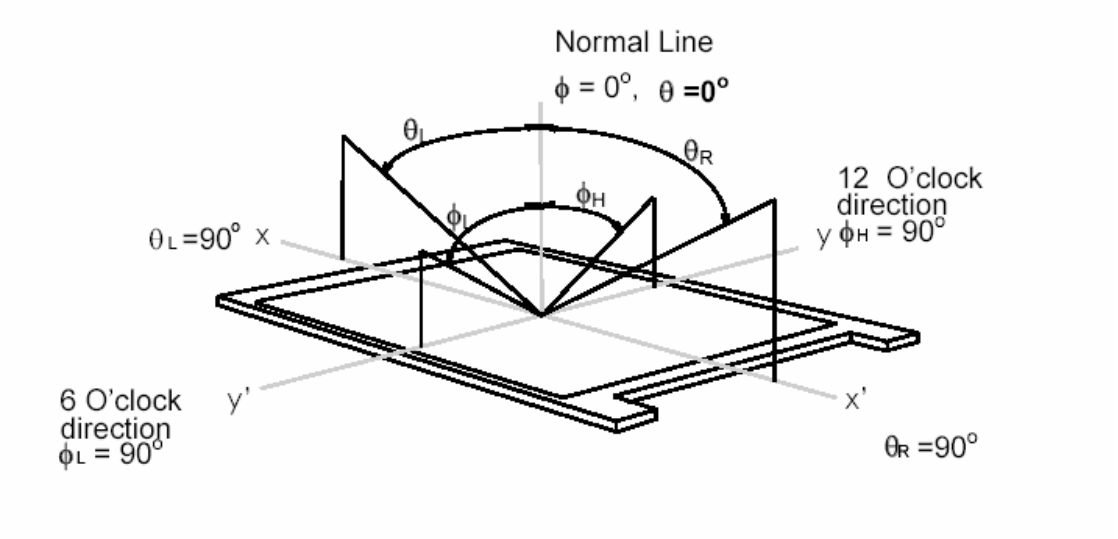
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



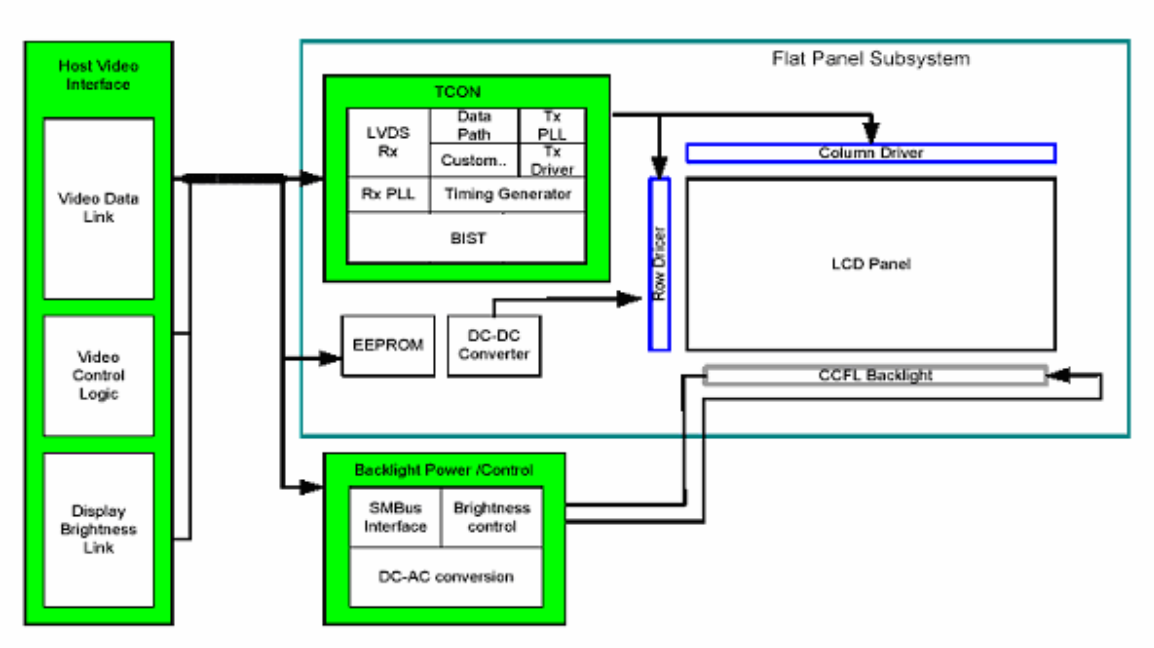
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.4WXGA+ TFT/LCD Module:



4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	-	6.5	[mA] rms	Note 1,2

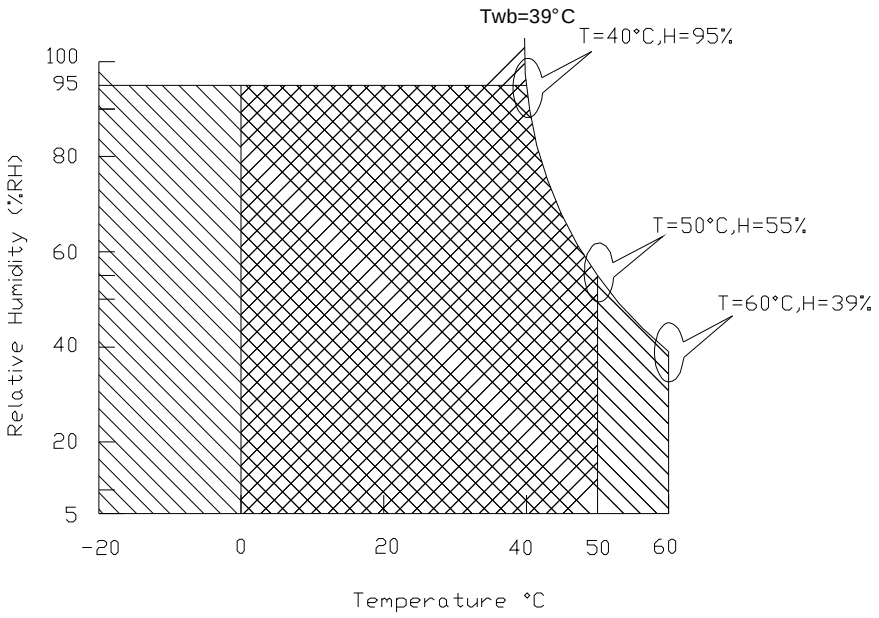
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	--	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range Storage Range

5. Electrical characteristics

5.1 TFT LCD Module

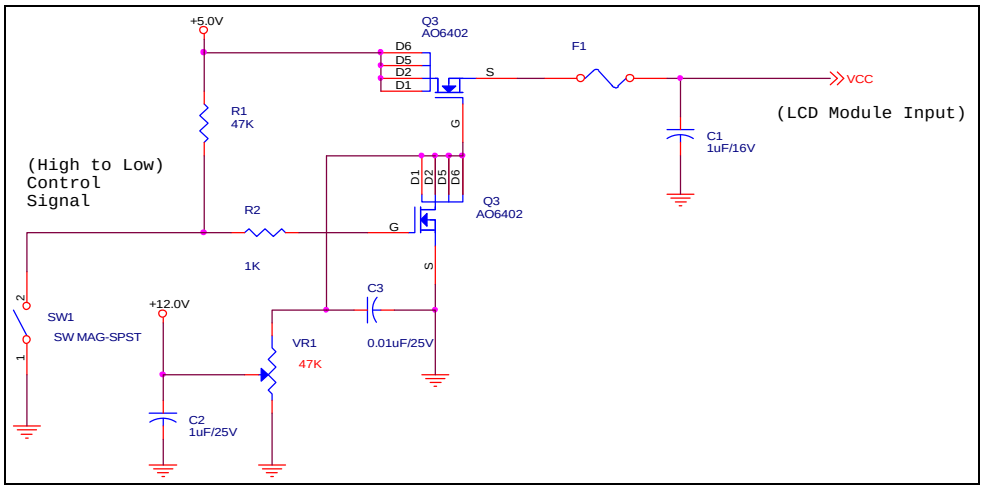
5.1.1 Power Specification

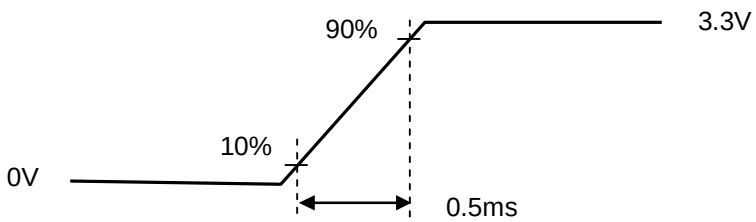
Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power			1.5	[Watt]	Note 1
IDD	IDD Current		400	500	[mA]	Note 1
IRush	Inrush Current			2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Patterm

Note 2：Measure Condition





Vin rising time

5.1.2 Signal Electrical Characteristics

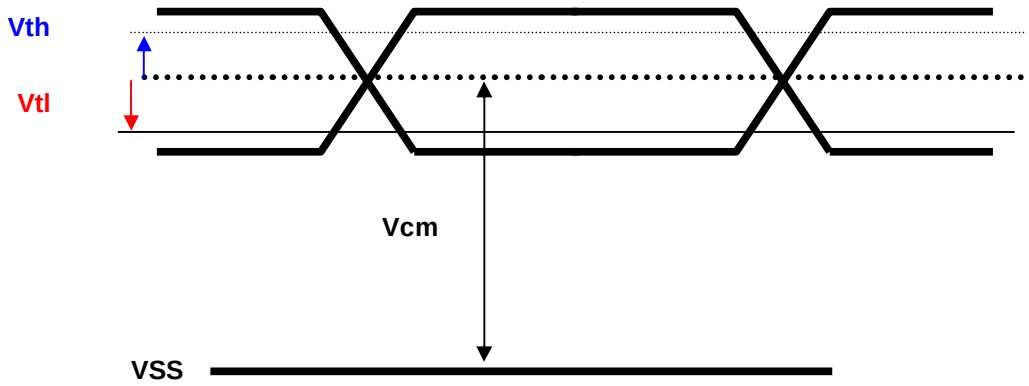
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A(Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	220	250	-	[cd/m^2]	(Ta=25℃)
CCFL current(I_{CCFL})		6.5		[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(F_{CCFL})		62		[KHz]	(Ta=25℃) Note 3,4
CCFL Ignition Voltage(Vs)	1340			[Volt] rms	(Ta= 0℃) Note 5
CCFL Ignition Voltage(Vs)	1030			[Volt] rms	(Ta= 25℃) Note 5
CCFL Voltage (Reference) (V_{CCFL})	620	720	910	[Volt] rms	(Ta=25℃) Note 6
CCFL Power consumption (P_{CCFL})	-	4.30	4.70	[Watt]	(Ta=25℃) Note 6

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has “Duty Dimming”, if ICCFL is less than 4mA.

Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,340 voltage. Lamp units need 1,300 voltage minimum for ignition.

Note 6: Calculator value for reference ($I_{CCFL} \times V_{CCFL} = P_{CCFL}$)

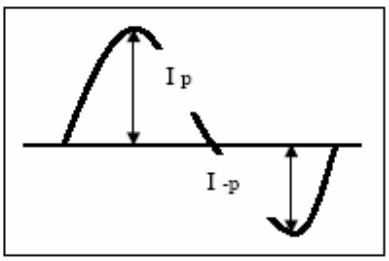
Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.

b. The distortion rate of the waveform should bewithin √2 ±10%.

* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

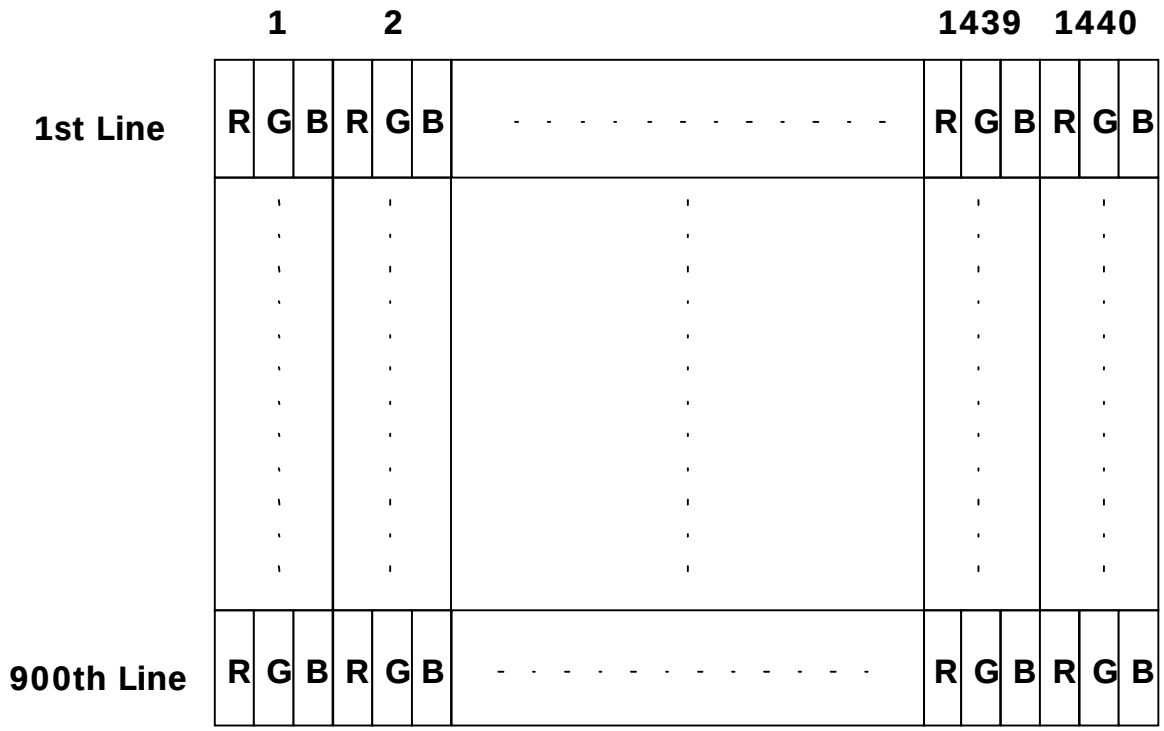
* Distortion rate

I_p (or I_{-p}) / I_{rms}

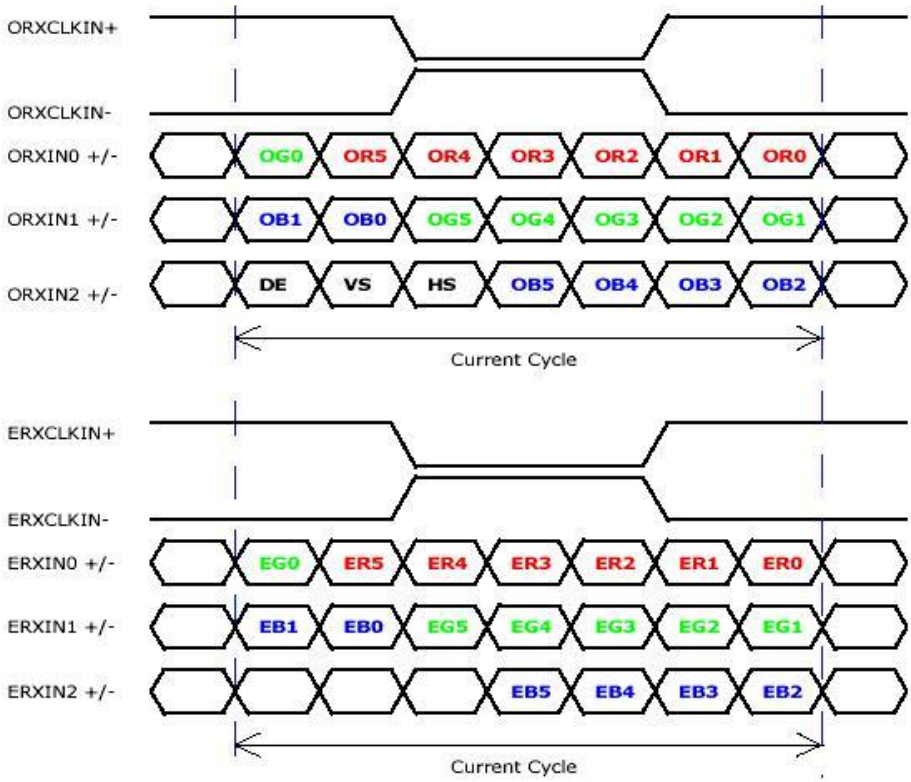
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description
V_{EDID}	+3.3V EDID Power
CLK_{EDID}	EDID Clock Input
$DATA_{EDID}$	EDID Data Input
ORXIN0-, ORXIN0+	Odd LVDS differential data input(ORed0-ORed5, OGreen0)
ORXIN1-, ORXIN1+	Odd LVDS differential data input(OGreen1-OGreen5, OBlue0-OBlue1)
ORXIN2-, ORXIN2+	Odd LVDS differential data input(OBlue2-OBlue5, Hsync, Vsync, DE)
ORXCLKIN-, ORXCLKIN+	Odd LVDS differential clock input
ERXIN0-, ERXIN0+	Even LVDS differential data input(ERed0-ERed5, EGreen0)
ERXIN1-, ERXIN1+	Even LVDS differential data input(EGreen1-EGreen5, EBlue0-EBlue1)
ERXIN2-, ERXIN2+	Even LVDS differential data input(EBlue2-EBlue5)
ERXCLKIN-, ERXCLKIN+	Even LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

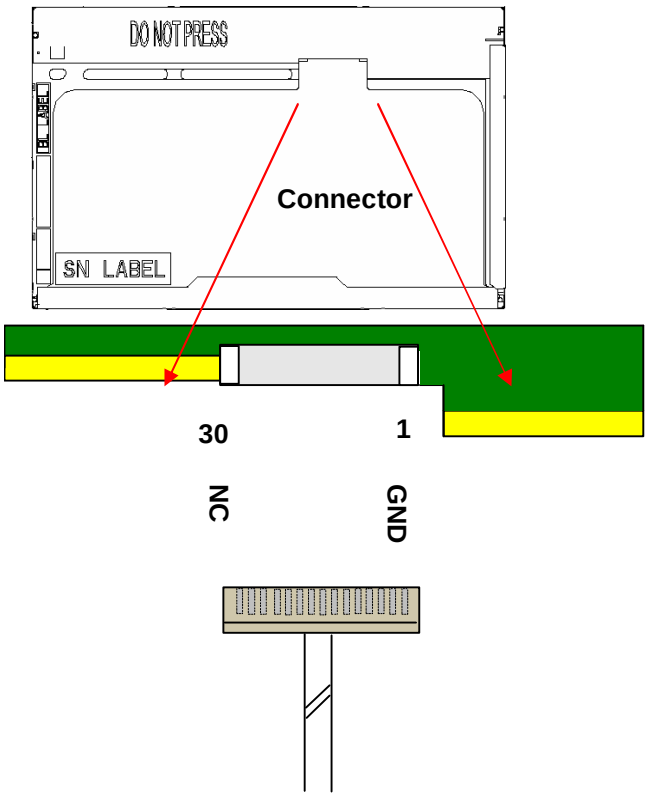
Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN #	SIGNAL NAME	DESCRIPTION
1	VSS	Power Ground
2	VDD	+ 3.3V Power Supply
3	VDD	+ 3.3V Power Supply
4	V_{EDID}	+ 3.3V EDID Power
5	AGING	Aging Mode Power Supply
6	CLK_{EDID}	EDID Clock Input
7	$DATA_{EDID}$	EDID Data Input
8	Odd_Rin0-	-LVDS Differential Data Input
9	Odd_Rin0+	+LVDS Differential Data Input
10	VSS	Power Ground
11	Odd_Rin1-	-LVDS Differential Data Input
12	Odd_Rin1+	+LVDS Differential Data Input
13	VSS	Power Ground
14	Odd_Rin2-	-LVDS Differential Data Input
15	Odd_Rin2+	+LVDS Differential Data Input
16	VSS	Power Ground
17	Odd_ClkIN-	-LVDS Differential Clock Input
18	Odd_ClkIN+	+LVDS Differential Clock Input
19	VSS	Power Ground
20	Even_Rin0-	-LVDS Differential Data Input
21	Even_Rin0+	+LVDS Differential Data Input
22	VSS	Power Ground
23	Even_Rin1-	-LVDS Differential Data Input
24	Even_Rin1+	+LVDS Differential Data Input
25	VSS	Power Ground
26	Even_Rin2-	-LVDS Differential Data Input
27	Even_Rin2+	+LVDS Differential Data Input
28	VSS	Power Ground
29	Even_ClkIN-	-LVDS Differential Clock Input
30	Even_ClkIN+	+LVDS Differential Clock Input

Note1: Start from right side



6.4 Interface Timing

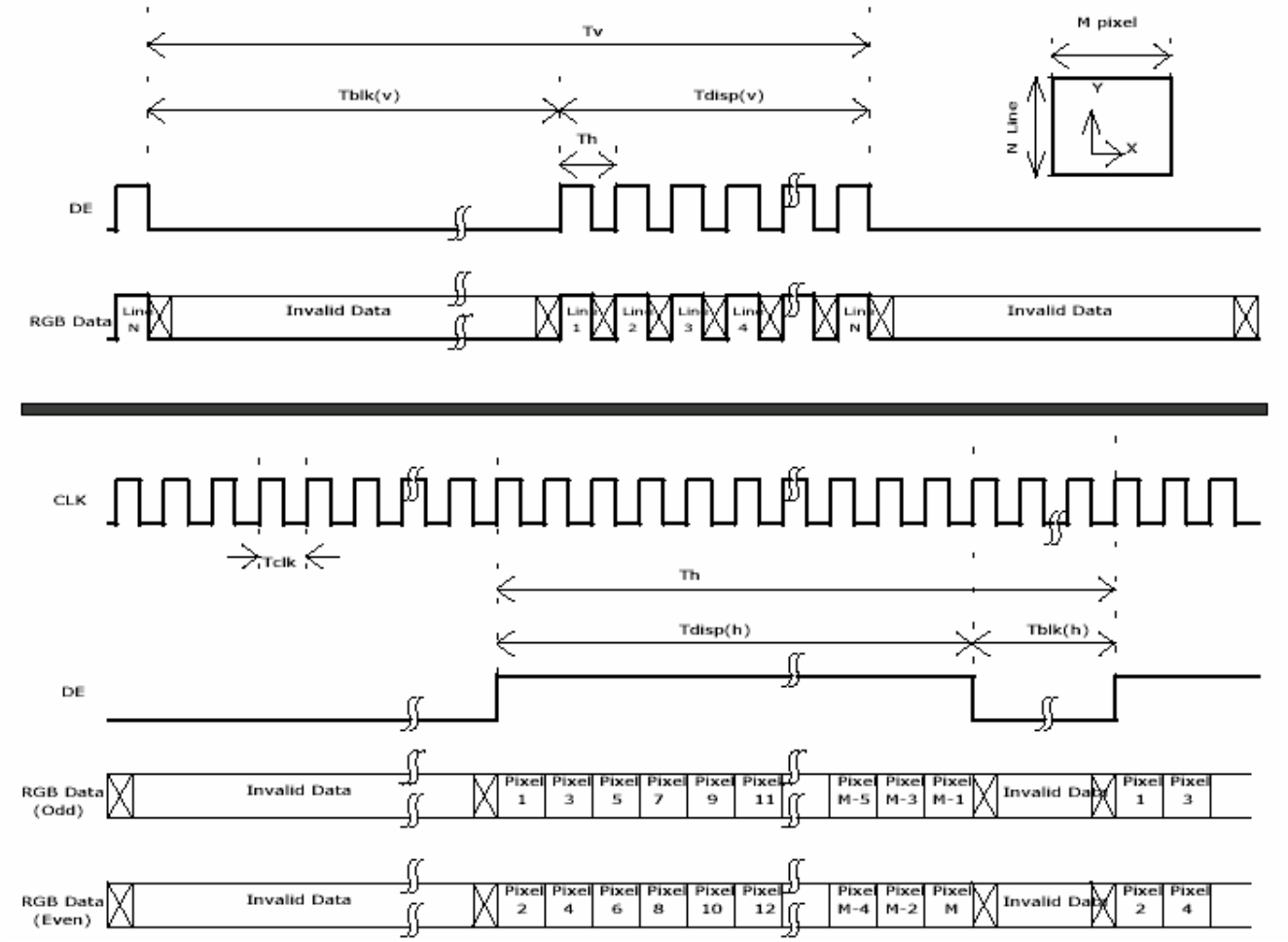
6.4.1 Timing Characteristics

Basically, interface timings should match the 1440X900 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		1/ T_{Clock}	50	48.2	60.2	MHz
Vertical Section	Period	T_V	904	912	2048	T_{Line}
	Active	T_{VD}	900	900	900	
	Blanking	T_{VB}	4	12	-	
Horizontal Section	Period	T_H	760	880	1024	T_{Clock}
	Active	T_{HD}	720	720	720	
	Blanking	T_{HB}	40	160	-	

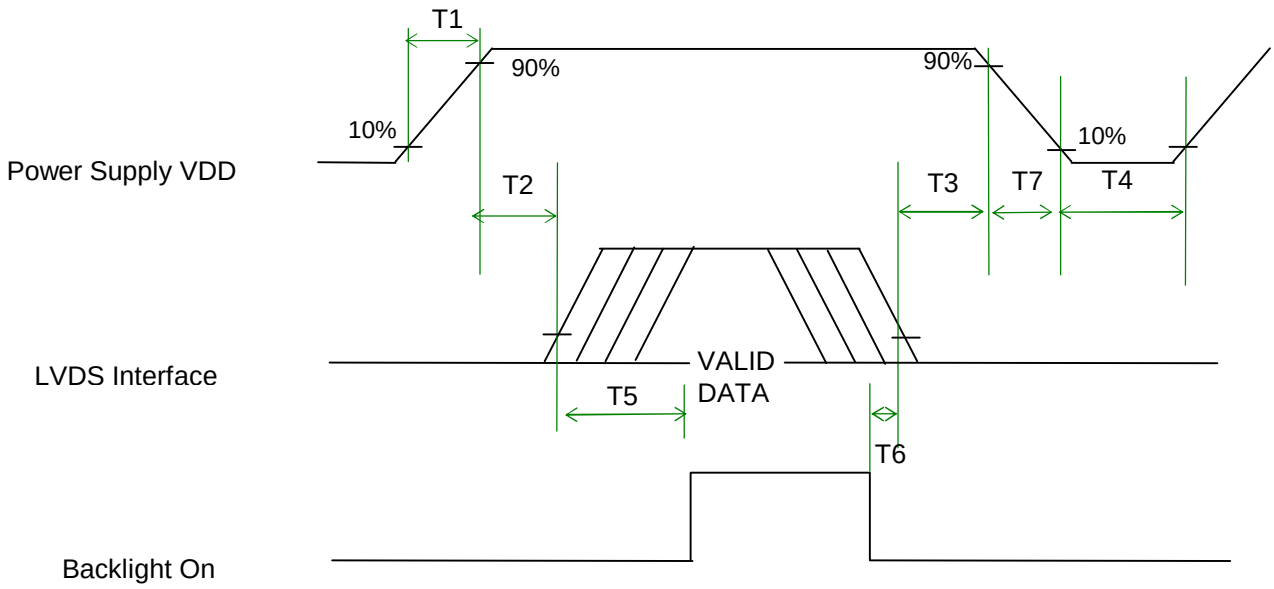
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	5	-	50	(ms)
T3	0.5	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SL-HF10 or compatible
Mating Housing/Part Number	FI-X30H or compatible

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage

8. Vibration and Shock Test (Stand alone)

8.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5G
- Frequency: 26 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 260 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

9. Reliability

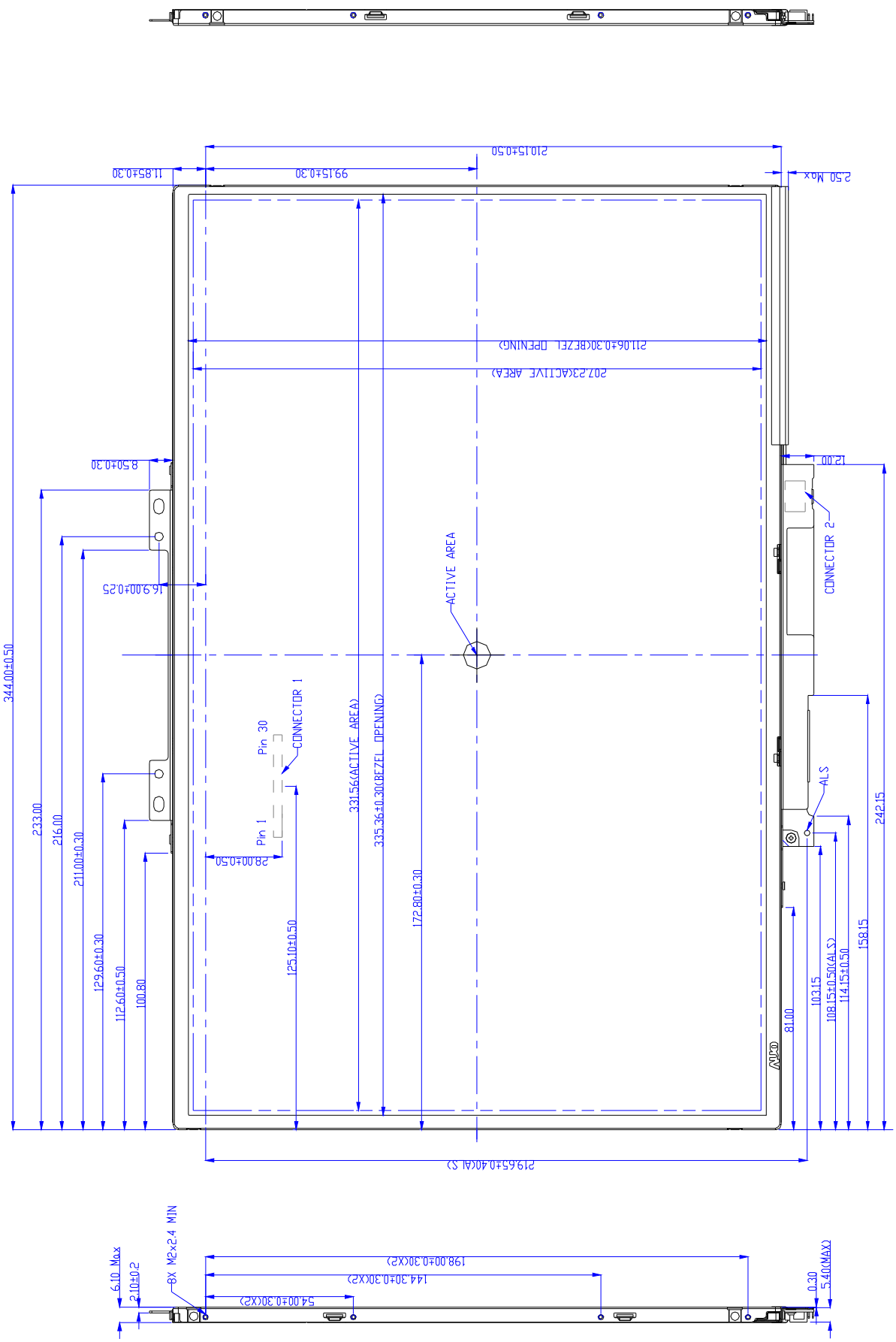
Items	Required Condition	Note
Temperature Humidity Bias	40℃/95%,300Hrs	
High Temperature Operation	50℃/Dry,300Hrs	
Low Temperature Operation	0℃,300Hrs	
On/Off Test	25℃,150hrs(ON/30 sec. OFF/30sec., 10,000 cycles)	
Hot Storage	65℃/20% RH ,300 hours	
Cold Storage	-25℃/50% RH ,300 hours	
Thermal Shock Test	-25℃/30 min ,65℃/30 min 100cycles non-OP	
Shock Test (Non-Operating)	260G, 2ms, Half-sine wave, +/- X, Y,Z direction,1 cycle	
Vibration Test (Non-Operating)	Sinusoidal vibration, 3.0 G zero-to-peak, 10 to 150 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact : ±8KV/ operation Air : ±15KV / operation	Note 1
Image sticking	10X10 checker pattern, 10 hrs, 25℃. The persisting pattern should be disappeared in 5 minutes	

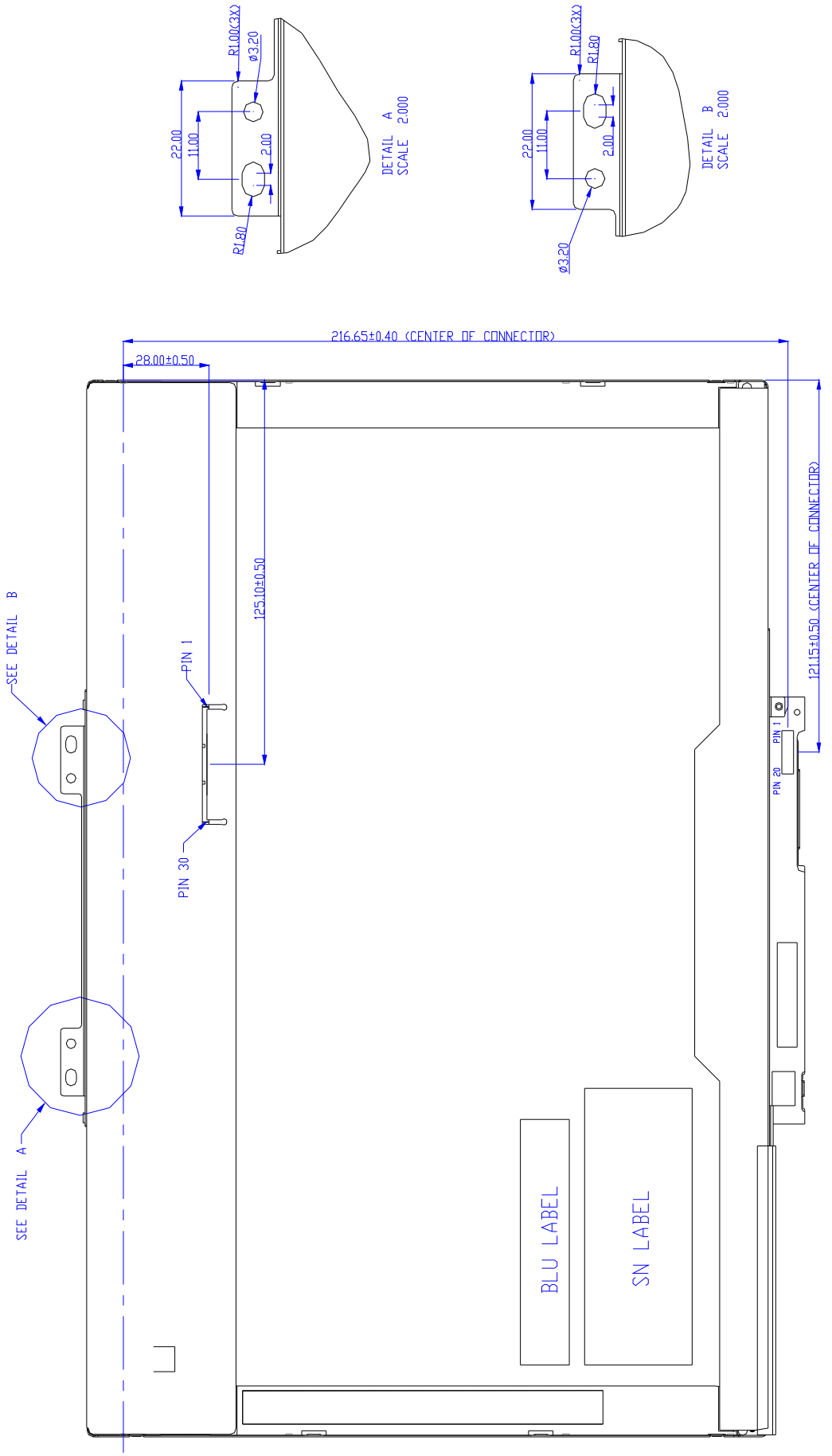
Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

. Self-recoverable. No hardware failures.

10. Mechanical Characteristics

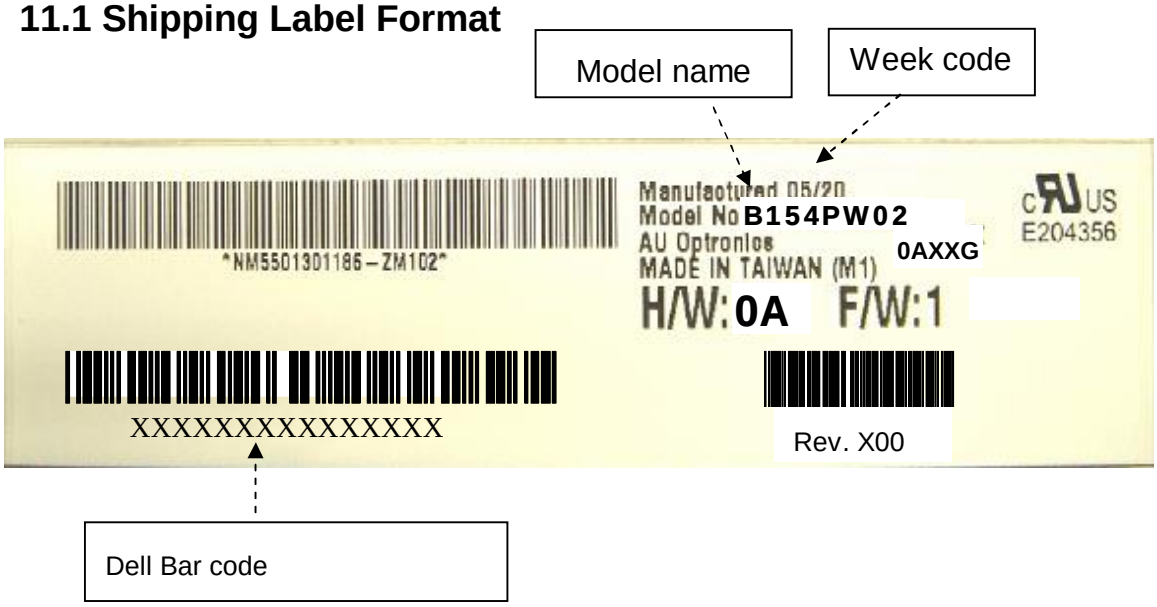
10.1 LCM Outline Dimension




R1.00(3X)
Ø3.20
22.00
11.00
2.00
R1.80
DETAIL A
SCALE 2.000
R1.00(3X)
R1.80
22.00
11.00
2.00
Ø3.20
DETAIL B
SCALE 2.000
216.65±0.40 (CENTER OF CONNECTOR)
28.00±0.50
125.10±0.50
121.15±0.50 (CENTER OF CONNECTOR)
SEE DETAIL B
PIN 1
PIN 30
PIN 1
PIN 20
SEE DETAIL A
BLU LABEL
SN LABEL

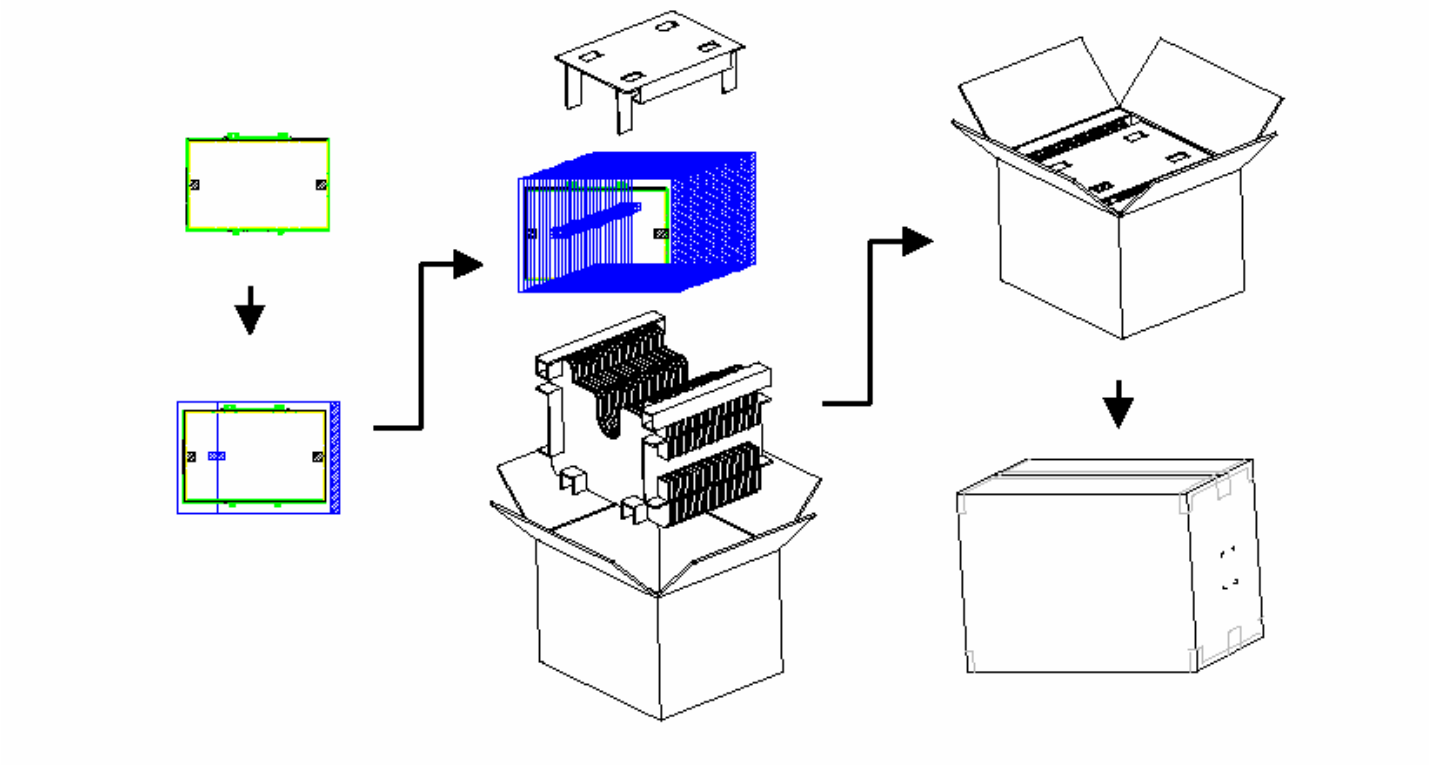
11. Shipping and Package

11.1 Shipping Label Format

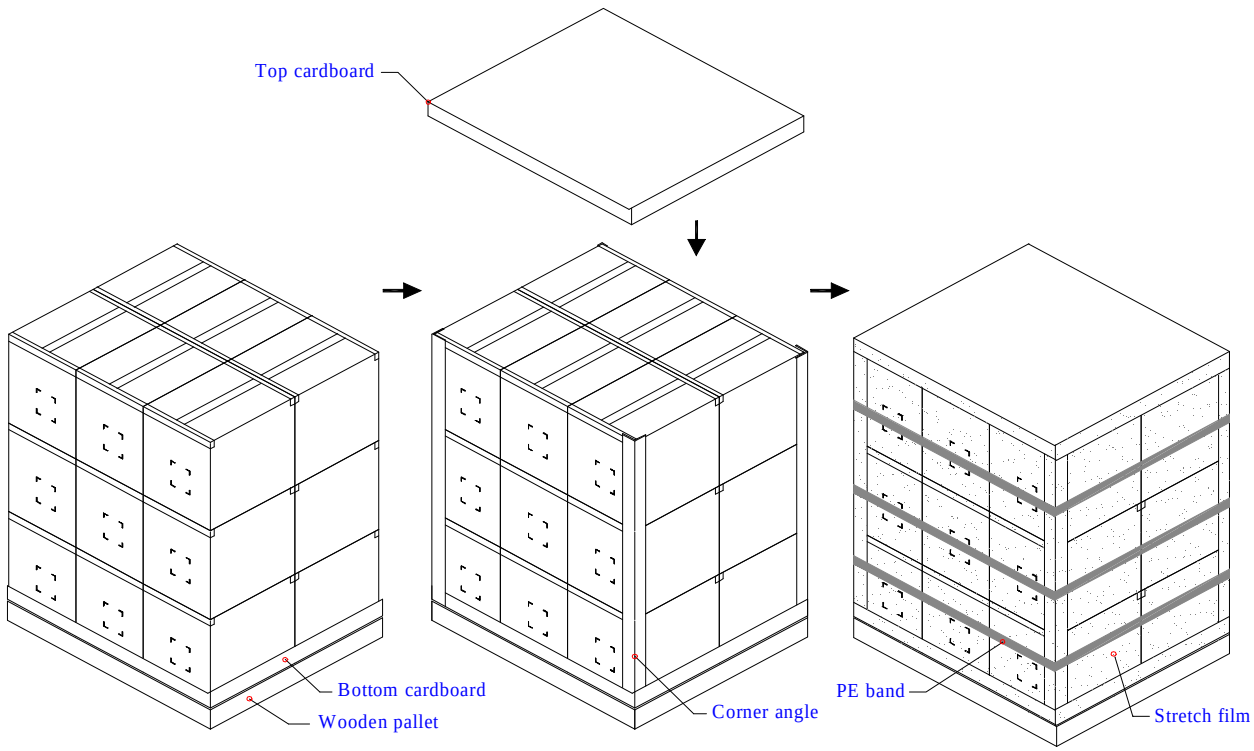


11.2. Carton package

The outside dimension of carton is 455 (L)mm x 380 (W)mm x 355 (H)mm



11.3 Shipping package of palletizing sequence



Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)

12. Appendix: EDID description

	Byte (hex)	Field Name and Comments	Value (hex)
Header	0	Header	00
	1	Header	FF
	2	Header	FF
	3	Header	FF
	4	Header	FF
	5	Header	FF
	6	Header	FF
	7	Header	00
Vendor / Product EDID Version	8	EISA manufacture code = 3 Character ID	06
	9	EISA manufacture code (Compressed ASCII)	AF
	0A	Panel Supplier Reserved – Product Code	77
	0B	Panel Supplier Reserved – Product Code	20
	0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	10	Week of manufacture	01
	11	Year of manufacture	10
	12	EDID structure version # = 1	01
	13	EDID revision # = 3	03
Display Parameters	14	Video I/P definition = Digital I/P (80h)	80
	15	Max H image size = (Rounded to cm)	21
	16	Max V image size = (Rounded to cm)	15
	17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78
	18	Feature support (no DPMS, Active off, RGB, timing BLK 1)	0A
Panel Color Coordinates	19	Red/Green Low bit (RxRy/GxGy)	1C
	1A	Blue/White Low bit (BxBy/WxWy)	F5
	1B	Red X Rx = 0.xxx	97
	1C	Red Y Ry = 0.xxx	58
	1D	Green X Gx = 0.xxx	50
	1E	Green Y Gy = 0.xxx	8E
	1F	Blue X Bx = 0.xxx	27
	20	Blue Y By = 0.xxx	27
	21	White X Wx = 0.xxx	50
	22	White Y Wy = 0.xxx	54
Established Timings	23	Established timings 1 (00h if not used)	00
	24	Established timings 2 (00h if not used)	00
	25	Manufacturer’s timings (00h if not used)	00
Standard Timing ID	26	Standard timing ID1 (01h if not used)	01
	27	Standard timing ID1 (01h if not used)	01
	28	Standard timing ID2 (01h if not used)	01

	29	Standard timing ID2 (01h if not used)	01
	2A	Standard timing ID3 (01h if not used)	01
	2B	Standard timing ID3 (01h if not used)	01
	2C	Standard timing ID4 (01h if not used)	01
	2D	Standard timing ID4 (01h if not used)	01
	2E	Standard timing ID5 (01h if not used)	01
	2F	Standard timing ID5 (01h if not used)	01
	30	Standard timing ID6 (01h if not used)	01
	31	Standard timing ID6 (01h if not used)	01
	32	Standard timing ID7 (01h if not used)	01
	33	Standard timing ID7 (01h if not used)	01
	34	Standard timing ID8 (01h if not used)	01
	35	Standard timing ID8 (01h if not used)	01
Timing Descripter #1	36	Pixel Clock/10,000 (LSB)	**9E**
	37	Pixel Clock/10,000 (MSB)	**25**
	38	Horizontal Active = 1024 pixels (lower 8 bits)	A0
	39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	40
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	51
	3B	Vertical Active = 768 lines	84
	3C	Vertical Blanking (Tvbp) = 38 lines (DE Blanking typ. for DE only panels)	0C
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30
	3E	Horizontal Sync, Offset (Thfp) = 26 pixels	40
	3F	Horizontal Sync, Pulse Width = 136 pixels	20
	40	Vertical Sync, Offset (Tvfp) = 3 lines Sync Width = 6 lines	33
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00
	42	Horizontal Image Size =304 mm	4B
	43	Vertical image Size = 228 mm	CF
	44	Horizontal Image Size / Vertical image size	10
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00
	46	Vertical Border = 0 (Zero for Notebook LCD)	00
	47	Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives, **DE only note: LSB is set to "1" if panel is DE-timing only. H/V can be ignored.**	19
Timing Descripter #2	48	Pixel Clock/10,000 (LSB)	5A
	49	Pixel Clock/10,000 (MSB)	1F
	4A	Horizontal Active = xxxx pixels (lower 8 bits)	A0
	4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	40
	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4	51

		bits)	
	4D	Vertical Active = xxxx lines	84
	4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	0C
	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30
	50	Horizontal Sync, Offset (Thfp) = xxxx pixels	40
	51	Horizontal Sync, Pulse Width = xxxx pixels	20
	52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	33
	53	Horizontal Vertical Sync Offset/Width upper 2 bits	00
	54	Horizontal Image Size =xxx mm	4B
	55	Vertical image Size = xxx mm	CF
	56	Horizontal Image Size / Vertical image size	10
	57	Horizontal Border = 0 (Zero for Notebook LCD)	00
	58	Vertical Border = 0 (Zero for Notebook LCD)	00
	59	Module “A” Revision = Example: 00, 01, 02, 03, etc.	00
Timing Descripter #3 Dell specific information	5A	Flag	00
	5B	Flag	00
	5C	Flag	00
	5D	Dummy Descriptor	FE
	5E	Flag	00
	5F	Dell P/N 1st Character	52
	60	Dell P/N 2nd Character	50
	61	Dell P/N 3rd Character	36
	62	Dell P/N 4th Character	34
	63	Dell P/N 5th Character	31
	64	LCD Supplier EEDID Revision #	00
	65	Manufacturer P/N	42
	66	Manufacturer P/N	31
	67	Manufacturer P/N	35
	68	Manufacturer P/N	34
	69	Manufacturer P/N	50
	6A	Manufacturer P/N	57
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	32
Timing Descripter #4	6C	Flag	00
	6D	Flag	00
	6E	Flag	00
	6F	Data Type Tag:	FE
	70	Flag	00
	71	SMBUS Value = XX nits	26
	72	SMBUS Value = XX nits	35
	73	SMBUS Value = XX nits	40
	74	SMBUS Value = XX nits	48
	75	SMBUS Value = XX nits	66
	76	SMBUS Value = XXX nits	8B
	77	SMBUS Value = XXX nits	BC

	78	SMBUS Value = max nits (Typically = 00h, XXX nits)	FF
	79	Number of LVDS receiver chips = '01' or '02'	02
	7A	BIST Enable: Yes = '01' No = '00'	01
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A
	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20
Checksum	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	**12**