CUSTOMER APPROVAL SHEET

Company Name	
MODEL	
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☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.___)**

☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.___)**

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☐ **CUSTOMER REMARK :**

AUO PM :

P/N : _____

Comment :

Doc. version :	0.0
Total pages :	54
Date :	2009/05/04

Product Specification

6″ COLOR TFT-LCD MODULE

Model Name : A060FW03 V0

Planned Lifetime:	From 2009/Apr. To 2011/Jun.
Phase-out Control:	From 2011/Mar. To 2011/Jun.
EOL Schedule:	2011/Jun.

< ◆ > Preliminary Specification

< > Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2009/05/04		Draft

Contents:

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution (dot)	480(W)×272(H) (tri-gate)	
2	Active area (mm)	132.48 (W) × 75.072 (H)	
3	Screen size (inch)	6 (Diagonal)	
4	Dot pitch (mm)	0.276 (W) × 0.092 (H)	
5	Color configuration	R. G. B. strip tri-gate	
6	Overall dimension (mm)	143.9 (W) × 88.3 (H) × 3.9 (D)	Note 1
7	Weight (g)	87±10	
8	Panel surface treatment	Hard coating	

Note 1: Refer to F. Outline Dimension

B. Electrical specifications

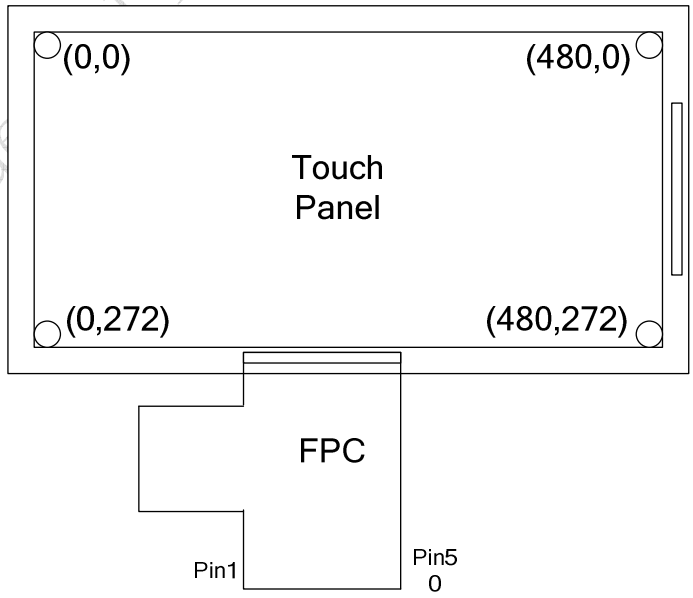
1. Pin assignment

No.	Pin Name	I/O	I/O structure	Description	Remarks
1	GND	G	--	GND	
2	GND	G	--	GND	
3	VDD	P	--	Power supply	
4	VDD	P	--	Power supply	
5	GRB	I	Type 3	Global Reset Pin (active low),	
6	INT_R	O	Type 1	Interrupt signal for touch panel function	
7	SCL	I	Type 3	Serial command clock input pin	
8	SDA	I/O	Type 4	Serial command data input pin	
9	CSB	I	Type 3	Serial command chip select pin	
10	R0	I	Type 2	Red Data Signal (LSB)	
11	R1	I	Type 2	Red Data Signal	
12	R2	I	Type 2	Red Data Signal	
13	R3	I	Type 2	Red Data Signal	
14	R4	I	Type 2	Red Data Signal	
15	R5	I	Type 2	Red Data Signal	
16	R6	I	Type 2	Red Data Signal	
17	R7	I	Type 2	Red Data Signal (MSB)	
18	INT_T	O	Type 1	Touch indicator signal.	
19	GND	G	--	GND	
20	GND	G	--	GND	
21	DE	I	Type 2	Data enable input	
22	DCLK	I	Type 2	Data clock input	
23	VSYNC	I	Type 2	Vertical synchronizing signal	
24	HSYNC	I	Type 2	Horizontal synchronizing signal	
25	G0	I	Type 2	Green Data Signal (LSB)	
26	G1	I	Type 2	Green Data Signal	
27	G2	I	Type 2	Green Data Signal	
28	G3	I	Type 2	Green Data Signal	
29	G4	I	Type 2	Green Data Signal	
30	G5	I	Type 2	Green Data Signal	
31	G6	I	Type 2	Green Data Signal	

32	G7	I	Type 2	Green Data Signal (MSB)	
33	B0	I	Type 2	Blue Data Signal (LSB)	
34	B1	I	Type 2	Blue Data Signal	
35	B2	I	Type 2	Blue Data Signal	
36	B3	I	Type 2	Blue Data Signal	
37	B4	I	Type 2	Blue Data Signal	
38	B5	I	Type 2	Blue Data Signal	
39	B6	I	Type 2	Blue Data Signal	
40	B7	I	Type 2	Blue Data Signal (MSB)	
41	GND	G	--	GND	
42	GND	G	--	GND	
43	GND	G	--	GND	
44	GND	G	--	GND	
45	VLED-	P	--	LED backlight cathode	
46	VLED+	P	--	LED backlight anode	
47	GND	G	--	GND	
48	GND	G	--	GND	
49	GND	G	--	GND	
50	GND	G	--	GND	

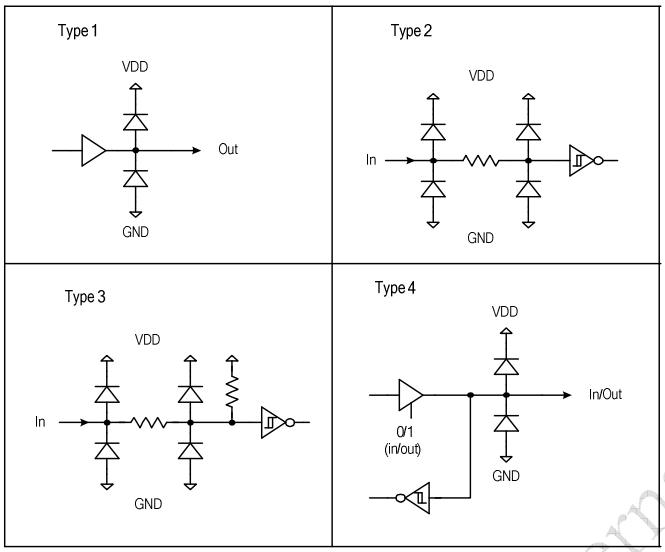
I: Input; O: Output. P: Power. I/O input/output

Note: Definition of scanning direction. Refer to figure as below



I/O Pin Structure:

Pull high/low resistor is **800kΩ**



2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VDD	GND=0	-0.5	5.0	V	
Input signal voltage	CSB,SDA,SCL, VSYNC,HSYNC, DCLK,R0~R7,G0~G7, B0~B7	GND=0	-0.3	3.6	V	
Operating temperature	Topa	-	--	--	℃	Ambient temperature
Storage temperature	Tstg	-	--	--	℃	Ambient temperature

3. Electrical characteristics

3.1 Operating conditions (GND=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	Note 1
Input Signal voltage	H Level	V_{IH}	0.7* VDD	-	VDD	V	
	L Level	V_{IL}	GND	-	0.3* VDD	V	
Touch Panel Sensing Rate			--	60	--	Hz	Note 2
Touch Panel Data Update			--	60	--	Hz	Note 2

Note 1: A build-in power on reset circuit for VDD is provided within the integrated LCD driver IC.

Note 2: Touch panel sensing rate and data update rate are synchronized with frame frequency.

3.2 Electrical characteristics (GND=AGND=0V)

Paramete	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for V_{DD}	I_{DD}	VDD=3.3V		20		mA	Note 1
	$I_{DD(STANDBY)}$			TBD		uA	Note 1

Note 1: Test Condition: black pattern,DCLK=27MHz, Frame rate: 60Hz, other registers are default setting.

3.3 Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	I_L		80	--	mA	
LED voltage	V_L	2.95	3.2	3.45	V	

4. Input timing AC characteristic

(VDD=3.0 ~3.6V, GND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK time	T_{DCLK}	72.25	105.49	110.62	ns	
CLK High time	PW_{CH}	38.91	--	--	ns	
CLK Low time	PW_{CL}	38.91	--	--	ns	
DCLK duty cycle		40	50	60	%	
HSYNC setup time	T_{HS}	5	-	-	ns	
HSYNC hold time	PW_{HH}	10	-	-	ns	
Data setup time	T_{DS}	5	-	-	ns	
Data hold time	PW_{DH}	10	-	-	ns	
DE setup time	T_{ES}	5	-	-	ns	
DE hold time	PW_{HE}	10	-	-	ns	

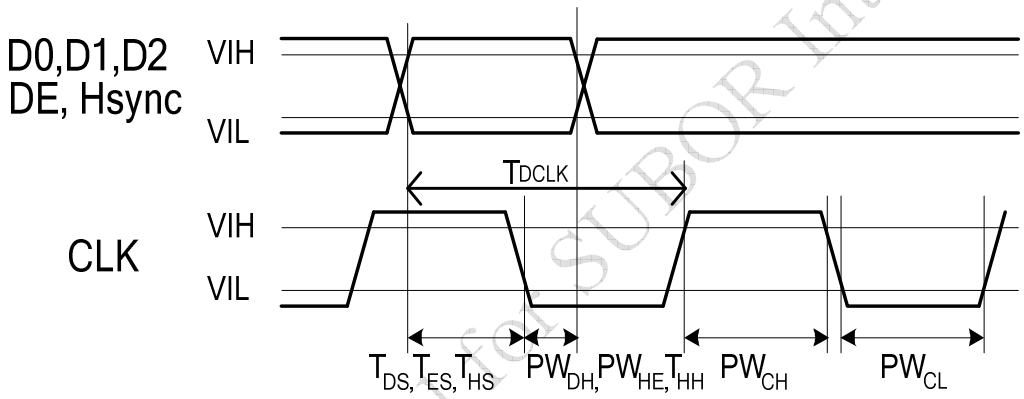


Fig1. Input timing detail

5. Input timing condition

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency		$1/T_{DCLK}$	9.04	9.48	13.84	MHz	
Frame Frequency	Cycle	PW_V		16.7		ms	
1 Frame Scanning Time	Cycle	PW_V	293	301	308	H	
	Display Period	PW_{VD}		272		H	
	Front porch	PW_{VF}	--	2	--	H	
	Pulse width	PW_{VW}	2	10	--	H	
	V Blanking	PW_{VE}	19	27	34	H	
1 Line Scanning Time	Cycle	PW_H	514	525	749	DCLK	
	Display Period	PW_{HD}		480		DCLK	
	Front porch	PW_{HF}	2	2	139	DCLK	
	Pulse width	PW_{HW}	2	41		DCLK	
	H Blanking	PW_{HE}	32	43	130	DCLK	

Vertical Timing of Input

HV mode (default)

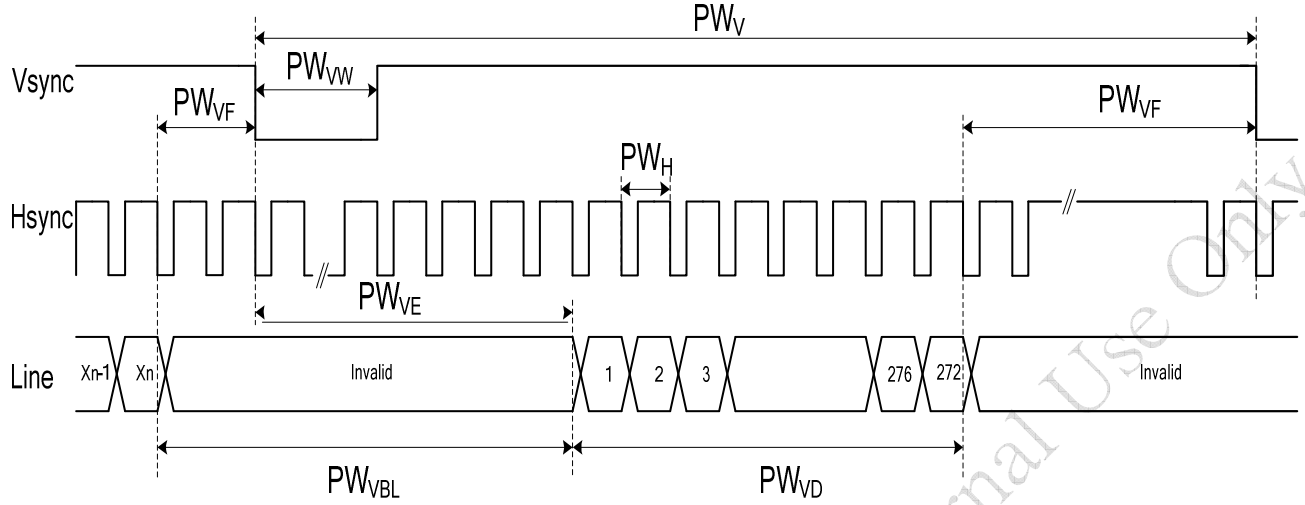


Fig2. HV mode - Vertical Input timing chart

DE mode (set by SPI command)

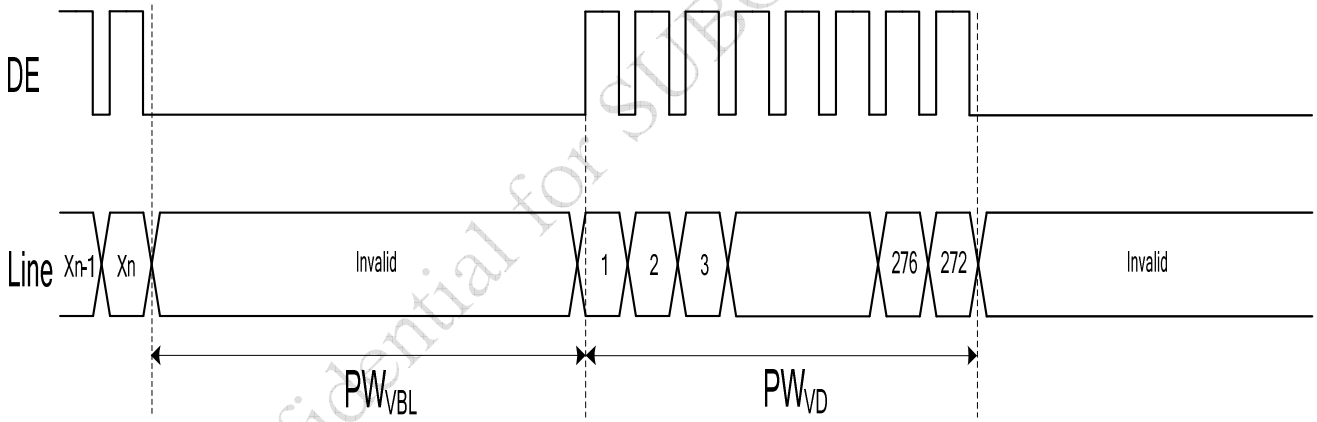


Fig3. DE mode - Vertical Input timing chart

Horizontal Timing of Input

HV mode (default)

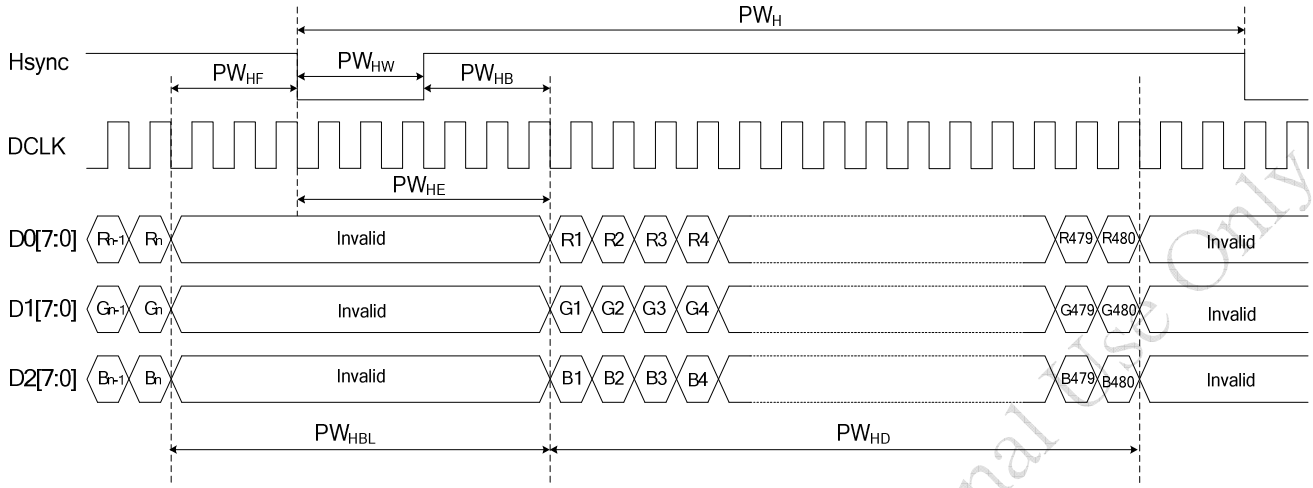


Fig4. HV mode - Horizontal Input timing chart

DE mode (set by SPI command)

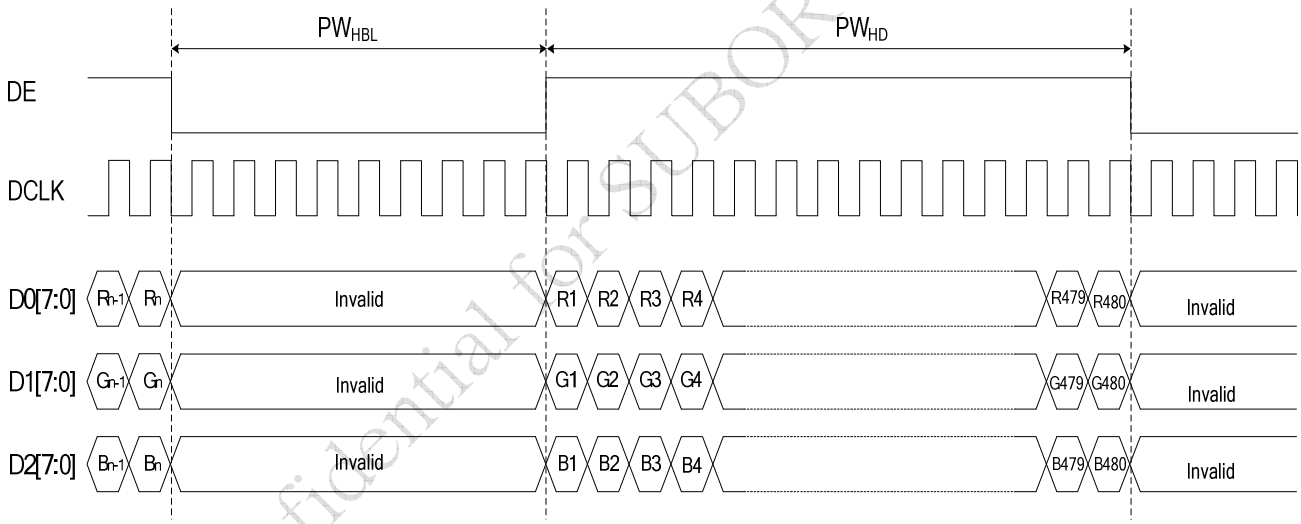
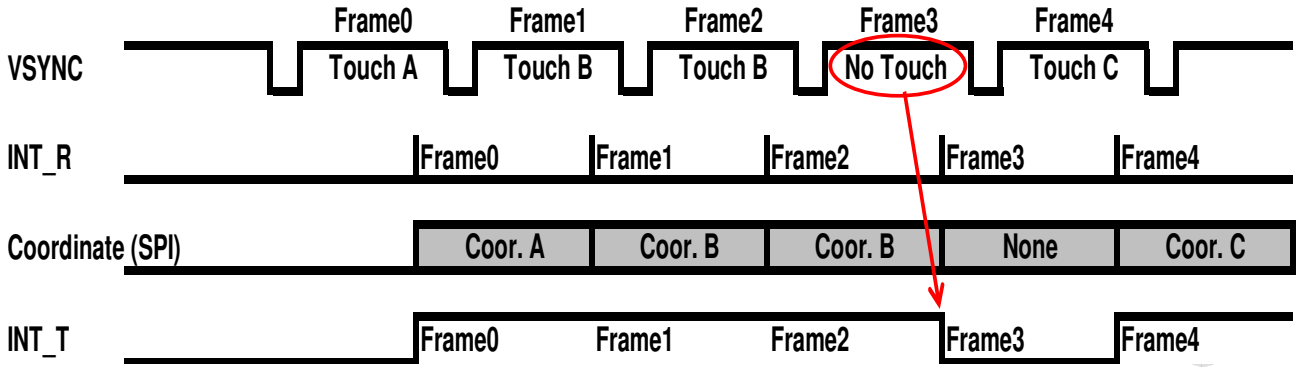


Fig5. DE mode - Horizontal Input timing chart

6. Touch Function Timing Diagram



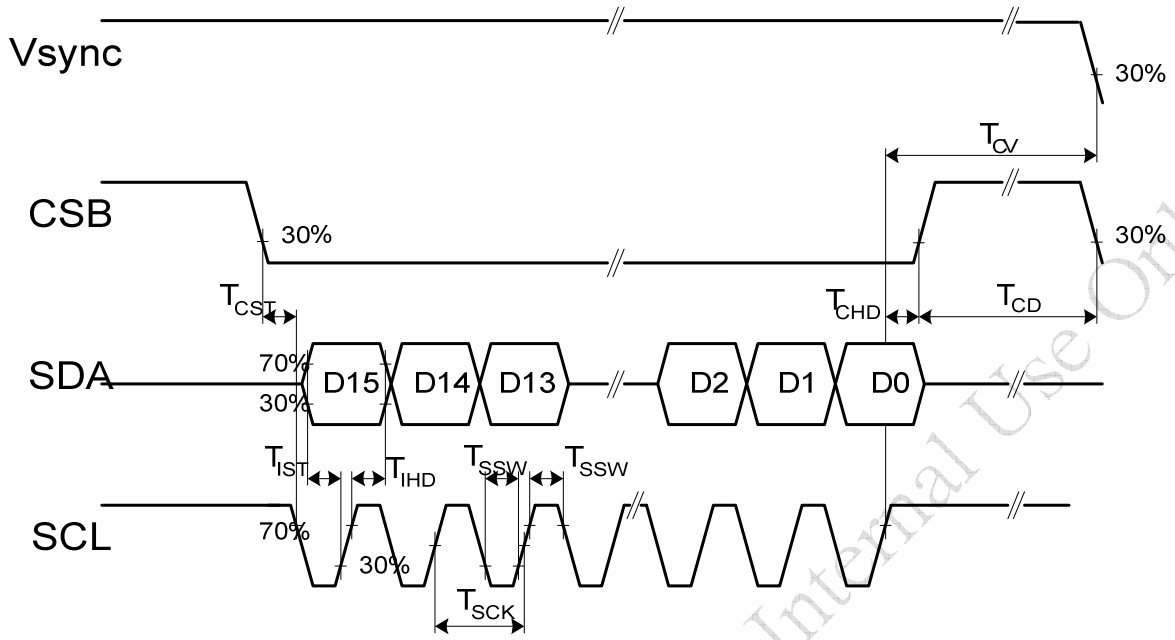
Note 1: INT_R : The interrupt signal when coordinate is ready.
INT_T : The indicator signal of touch.

Note 2: The COORDINATE DATA must read out at INT_R rising edge.

Note 3: INT_T is same with conventional touch panel interrupt signal.
When INT_T = HIGH means touch; when INT_T = LOW means no touch.

Note 4: Update Rate is synchronized with VSYNC frequency.

7. Serial control interface AC characteristic



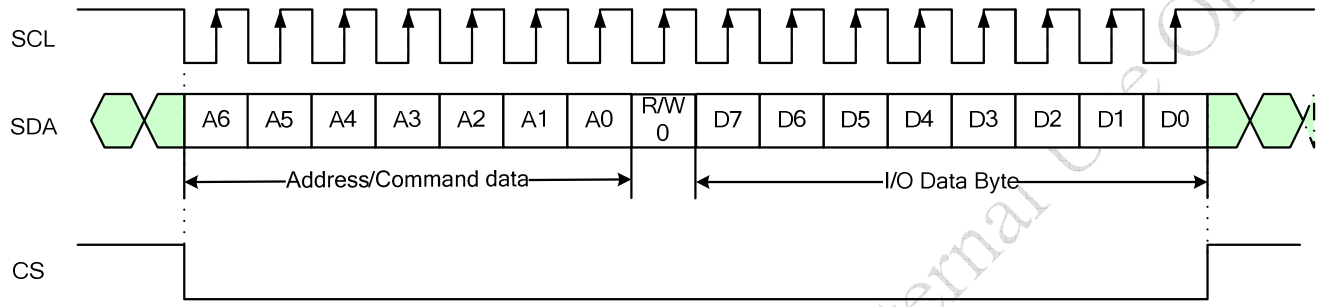
Parameter	Symbol	Min.	Typ.	Max.	Unit.
Serial clock	T_{SCK}	100			ns
SCL pulse duty	T_{SCW}	40	50	60	%
Serial data setup time	T_{IST}	50			ns
Serial data hold time	T_{IHD}	50			ns
Serial clock high/low	T_{SSW}	50			ns
CSB setup time	T_{CST}	50			ns
CSB hold time	T_{CHD}	50			ns
Chip select distinguish	T_{CD}	400			ns
Delay from CSB to Vsync	T_{CV}	1			us

7.1 The configuration of serial data at SDA terminal is at below

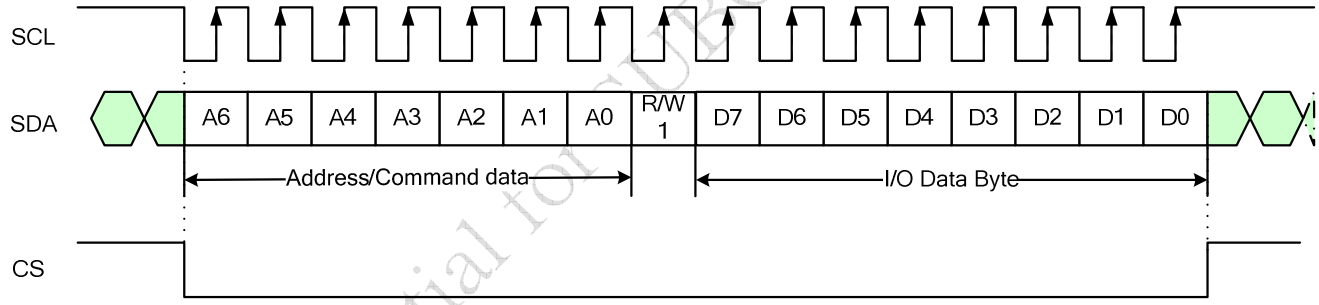
MSB LSB

A6	A5	A4	A3	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
Address							R/W	DATA							

7.2 SPI write mode timing chart



7.3 SPI read mode timing chart



1. At power-on, the default values specified for each parameter (in Figure 1) are taken.
2. If less than 16-bit data are read during the CSB low time period, the data is cancelled.
   a. The write operation is cancelled.
   b. The read operation is interrupt.
3. If more than 16-bit data are read during the CSB low time period, the last 16 bits are kept.
   a. Address & R/W are always defined form CSB falling edge.
   b. The write operation load last 8 bit data before CSB rising edge.
   c. The read operation is “D0” which output to SDA until CSB rising edge.
4. All items are setting in anytime and enable at the falling edge of the VSYNC(HV mode) or the rising edge of the End Frame(DE mode), except GRB.
5. When GRB is activated through the serial interface, all registers are cleared except the GRB value.
6. Register R/W setting: D8 = “L” → write mode; D8 = “H” → read mode.

7. The register values are valid when VCC already goes to high and after VSYNC(HV mode) or End Frame(DE mode) starts.
8. It is suggested that VSYNC, HSYNC, DCLK(for HV mode) or DE,DCLK(for DE mode) always exists in the same time. But if HSYNC, DE, DCLK stops, only VSYNC operating, the register setting is still valid.
9. If the chip goes to standby mode, the register value will still keep. MCU can wake up the chip only by changing standby mode value from low to high.
10. The register setting values are rewritten by the influence of static electricity, a noise, etc. to unsuitable value, incorrect operating may occur. It is suggested that the SPI interface will setup as frequently as possible.

1. Serial setting table

(1) Initial register settings:

Reg No.	ADDRESS							R/W	DATA							
	A6	A5	A4	A3	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
R4	0	0	0	0	1	0	0	0	0	1	0	1	1	0	1	0
R5	0	0	0	0	1	0	1	0	0	1	1	1	0	0	0	0
R48	0	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0
R49	0	1	1	0	0	0	1	0	0	0	1	0	0	1	1	0
R50	0	1	1	0	0	1	0	0	1	0	0	0	0	1	0	0
R51	0	1	1	0	0	1	1	0	0	0	0	1	1	1	1	0
R52	0	1	1	0	1	0	0	0	1	0	0	1	0	1	0	0
R53	0	1	1	0	1	0	1	0	0	0	0	0	0	0	1	1

Note: This initial register settings need to be registered before using.

(2) Register settings:

Reg No.	ADDRESS							R/W	DATA							
	A6	A5	A4	A3	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	0	1	0	1	X	0	0	GRB(1)
R1	0	0	0	0	0	0	1	0	STB (1)	1	X	0	1	101		
R2	0	0	0	0	0	1	0	0	DEM (0)	X	0	1	VDL(1000)			
R3	0	0	0	0	0	1	1	0	HDL(1000_0000)							
R23	0	0	1	0	1	1	1	0	010			010			CHLR(0)	0
R47	0	1	0	1	1	1	1	0	10111					X	SENSING_RATE(0 0)	
R65	1	0	0	0	0	0	1	X	RDCOORDATA							
R67	1	0	-	0	0	1	1	0	0	0	0	0	0	X	AEN (0)	X

Note: “X” is “don’t care”.

Register R0

Bit0	GRB setting
0	The controller is reset. Reset all registers to default value.
1	Normal operation(default)

Register R1

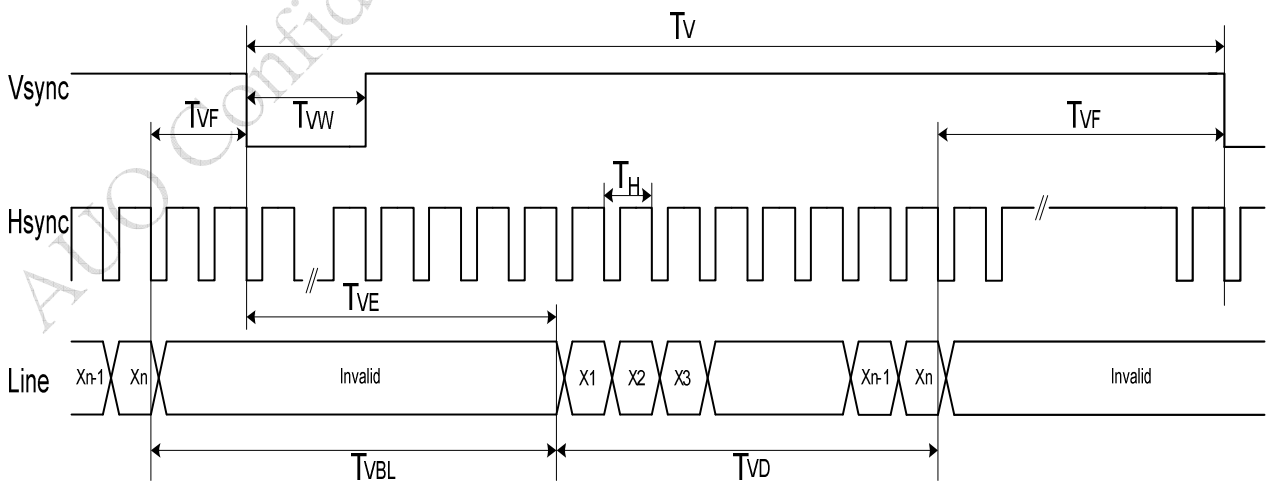
Bit7	STB setting
0	T-CON, source driver and DC-DC converters are off, all outputs are GND, and all level shift outputs are high Z.
1	Normal operation(default)

Register R2

Bit7	DEM setting
0	The setting is HV mode.
1	The setting is DE mode.

Bit3-0	VDL setting.
0000	T_{VE} = T_{Vetyp} – 8 Hs period.
0001	T_{VE} = T_{Vetyp} – 7 Hs period.
0010	T_{VE} = T_{Vetyp} – 6 Hs period.
0011	T_{VE} = T_{Vetyp} – 5 Hs period.
0100	T_{VE} = T_{Vetyp} – 4 Hs period.
0101	T_{VE} = T_{Vetyp} – 3 Hs period.
0110	T_{VE} = T_{Vetyp} – 2 Hs period.
0111	T_{VE} = T_{Vetyp} – 1 Hs period.
1000	T_{VE} = T_{Vetyp}. (T_{VE}=27 (typ)). (default)
1001	T_{VE} = T_{Vetyp} + 1 Hs period.
1010	T_{VE} = T_{Vetyp} + 2 Hs period.
1011	T_{VE} = T_{Vetyp} + 3 Hs period.
1100	T_{VE} = T_{Vetyp} + 4 Hs period.
1101	T_{VE} = T_{Vetyp} + 5 Hs period.
1110	T_{VE} = T_{Vetyp} + 6 Hs period.
1111	T_{VE} = T_{Vetyp} + 7 Hs period.

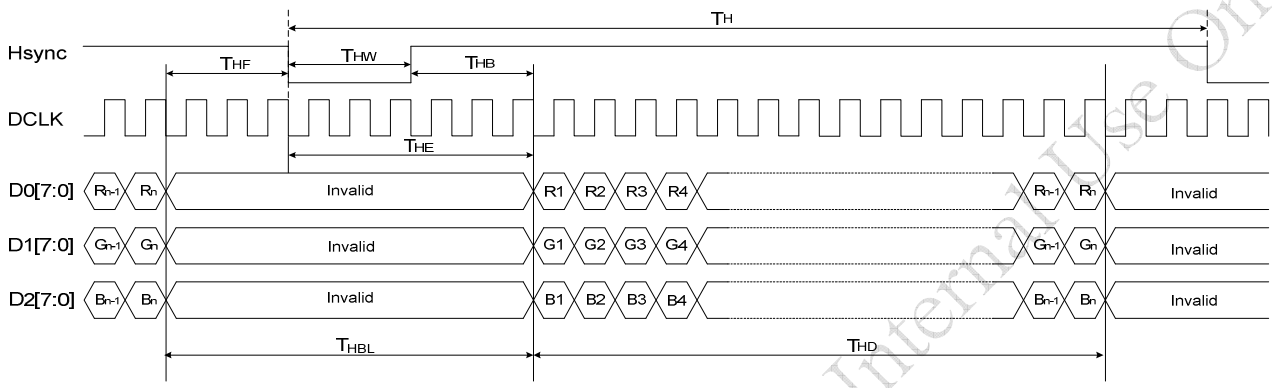
Vertical input timing. (HV mode)



Register R3

Bit7-0	HDL setting.
00100110	Prohibited
00100111	$T_{HE} = T_{Hetyp}$ – 39 CLK period (T_{HE}= 4 (min)).
10000000	$T_{HE} = T_{Hetyp}$ (T_{HE}=43 (typ)). (default)
11010111	$T_{HE} = T_{Hetyp}$ + 87 CLK period (T_{HE}= 130 (max)).
11011000	Prohibited

Horizontal input timing. (HV mode)



Register R23

Bit1	CHLR setting
0	Shift from left to right: D1→D2→D3…….→Dm.
1	Shift from right to left: Dm→Dm-1…….→D2→D1.

Note: m=480

Register R47

Bit1-0	SENSING_RATE (Sensing rate setting) (M)
00	M = 0 (60Hz) (default)
01	M = 1 (30Hz)
10	M = 2 (15Hz)
11	M = 31

Note: 1. “M=0”(60Hz) setting just can be used in coordinates mode.

2. Sensing rate setting (M) will affect outputting frequency of coordinates.

Register R67

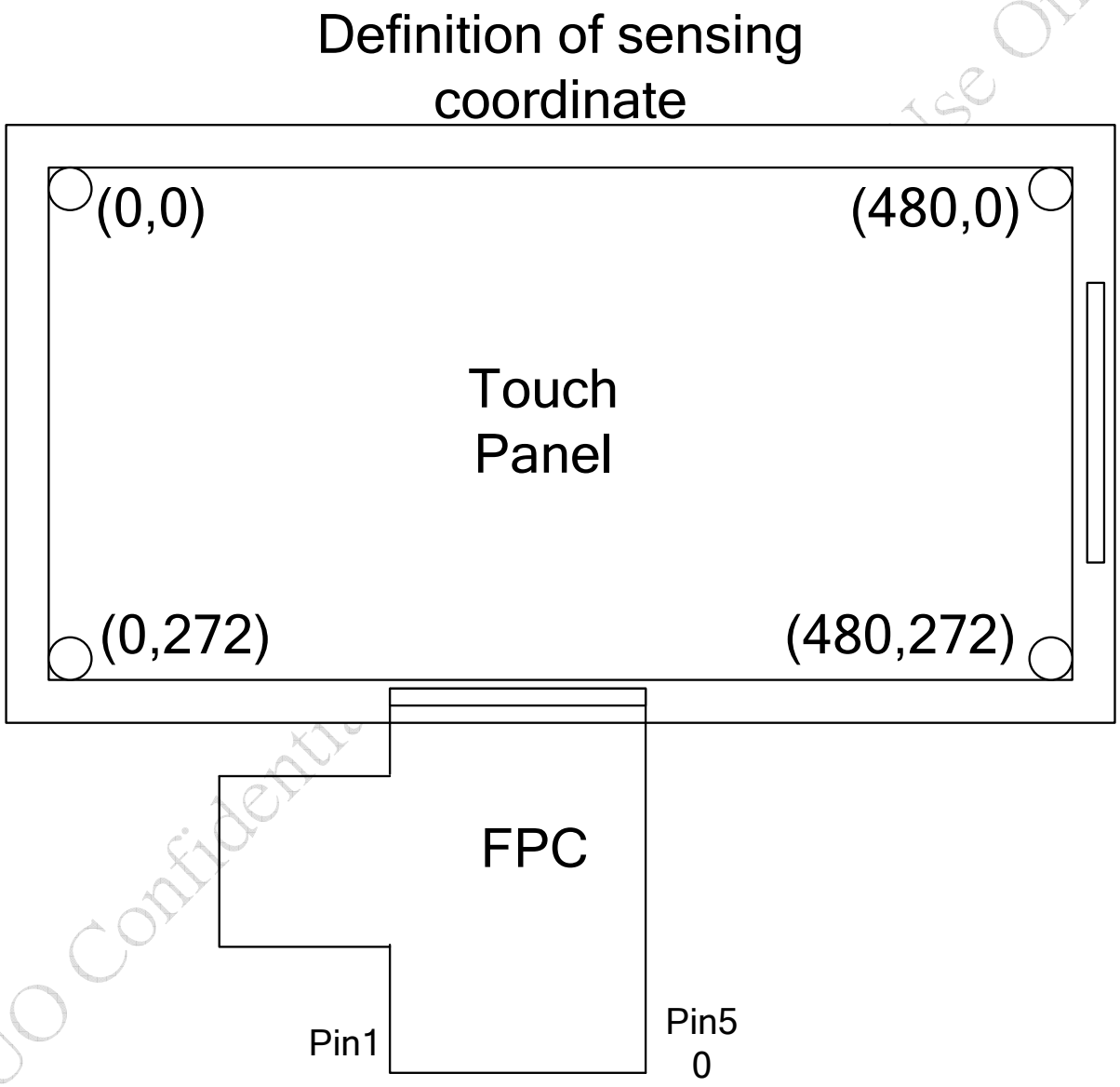
Bit1	AEN (Enable Touch Panel Algorithm)
0	Touch Panel algorithm is disabled (default)
1	Touch Panel algorithm is enable

Register R65

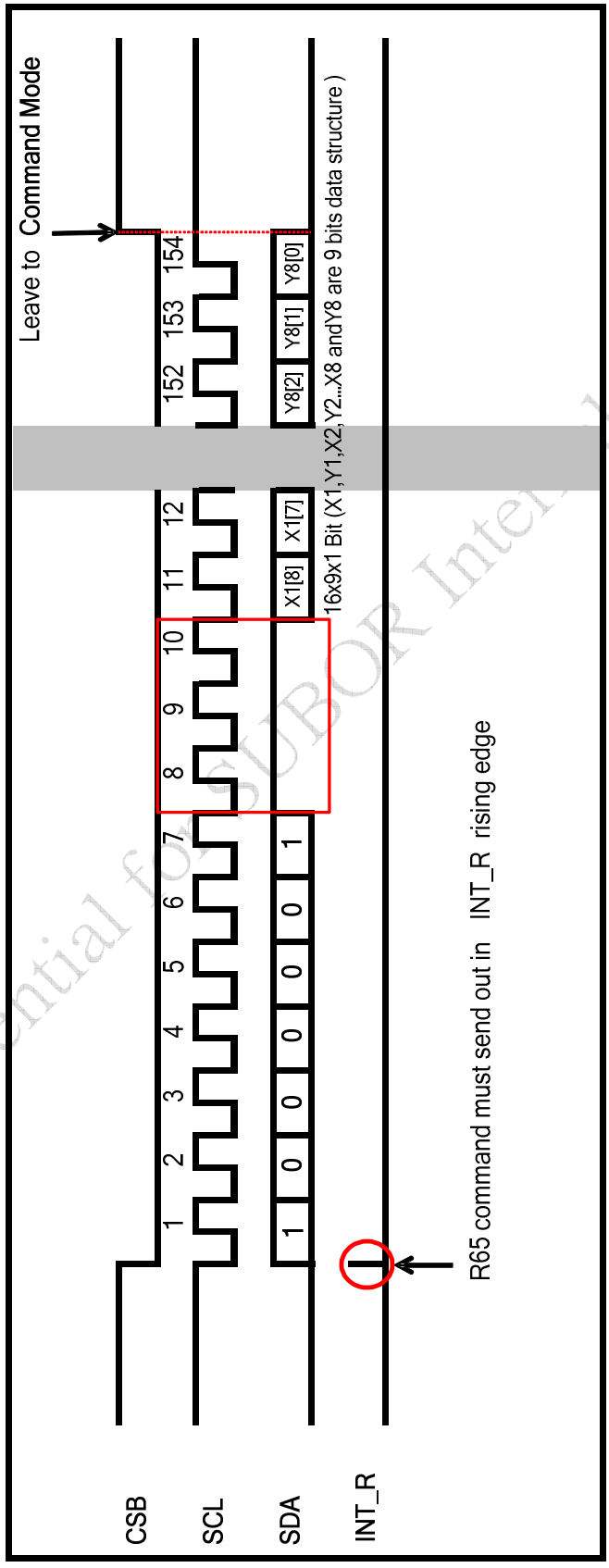
Reg No	ADDRESS							R/W	DATA							
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R65	1	0	0	0	0	0	1	R	RDCOORDATA (Read Sensing Coordinates from SPI directly)							

Note 1: This register (command) will output 8*2*9bit data, so the SPI clock must be faster than 10KHz (8*2*9*60≒10K).

Note 2: Definition of sensing coordinates (X1,Y1)~(X8,Y8) are mapping to display physical coordinates as shown in figure below.



Note 3: User can use this register (command) to reading sensing coordinate directly and the SPI sequence is different with other commands. The SPI sequence is as follows:



C. Optical specification (Note 1,Note 2, Note 3)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise	Tr	θ=0°	-	10	40	ms	Note 4, 6
	Fall	Tf		-	25	50	ms	
Contrast ratio		CR	At optimized viewing angle	200	300	-		Note 5, 6
Viewing angle	Top		CR≧10	60	70	-	deg.	Note 6, 7
	Bottom			60	70	-		
	Left			60	70	-		
	Right			60	70	-		
Brightness			θ=0°	150	180	-	nits	Note 8
White chromaticity		X	θ=0°	0.26	0.31	0.36		
		y		0.28	0.33	0.38		
Red chromaticity		X	θ=0°	0.53	0.58	0.63		
		y		0.29	0.34	0.39		
Green chromaticity		X	θ=0°	0.29	0.34	0.39		
		y		0.51	0.56	0.61		
Blue chromaticity		X	θ=0°	0.09	0.14	0.19		
		y		0.09	0.14	0.19		
Uniformity		ΔY_L	%	75	80	--	%	Note 10

Note 1. Ambient temperature =25℃.

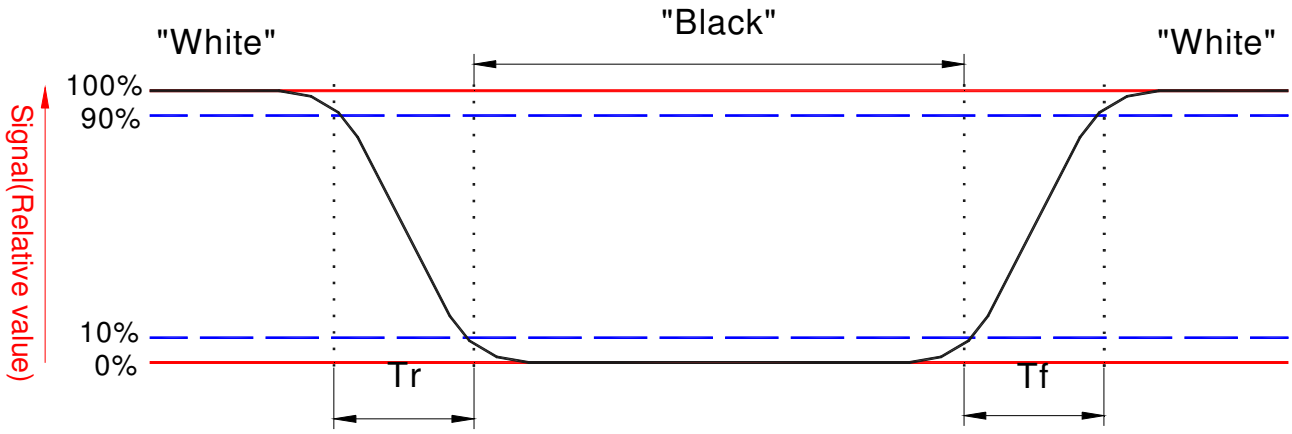
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation under 25 mA.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. White $Vi=V_{i5} \overline{+}1.5V$

Black $Vi=V_{i50} \pm 2.0V$

“±” Means that the analog input signal swings in phase with COM signal.

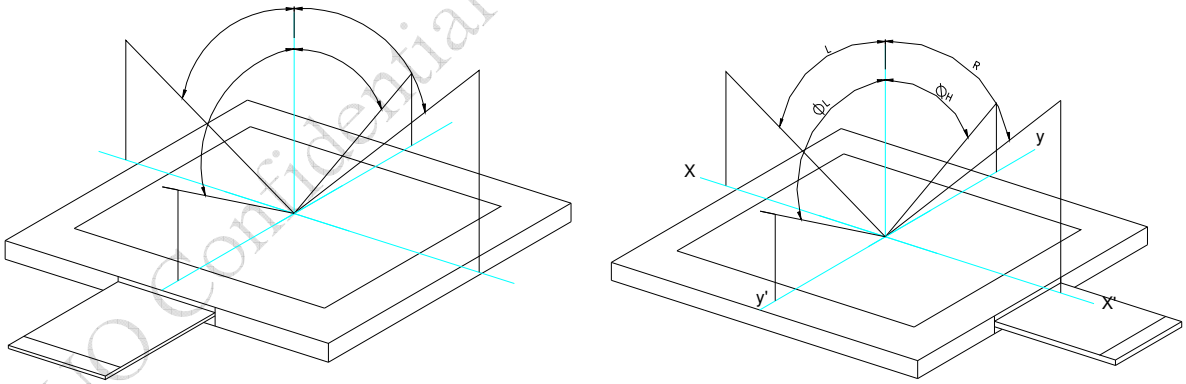
“ $\overline{+}$ ” Means that the analog input signal swings out of phase with COM signal.

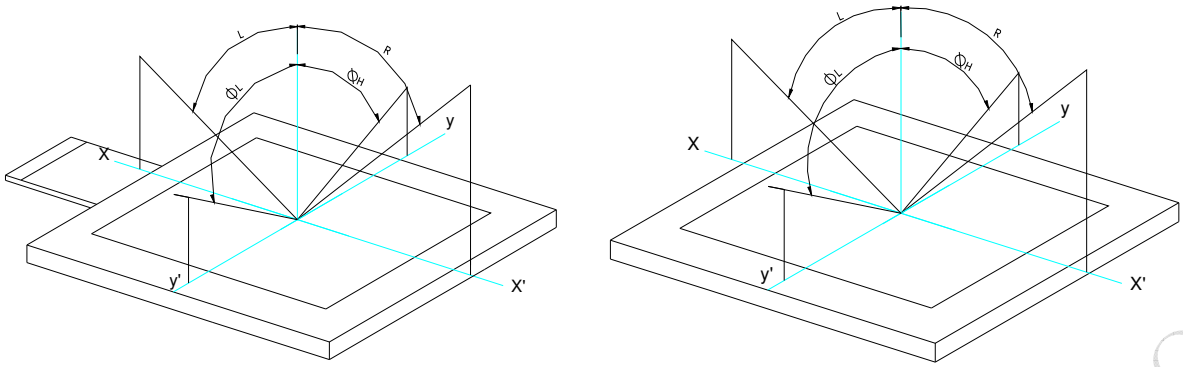
V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:

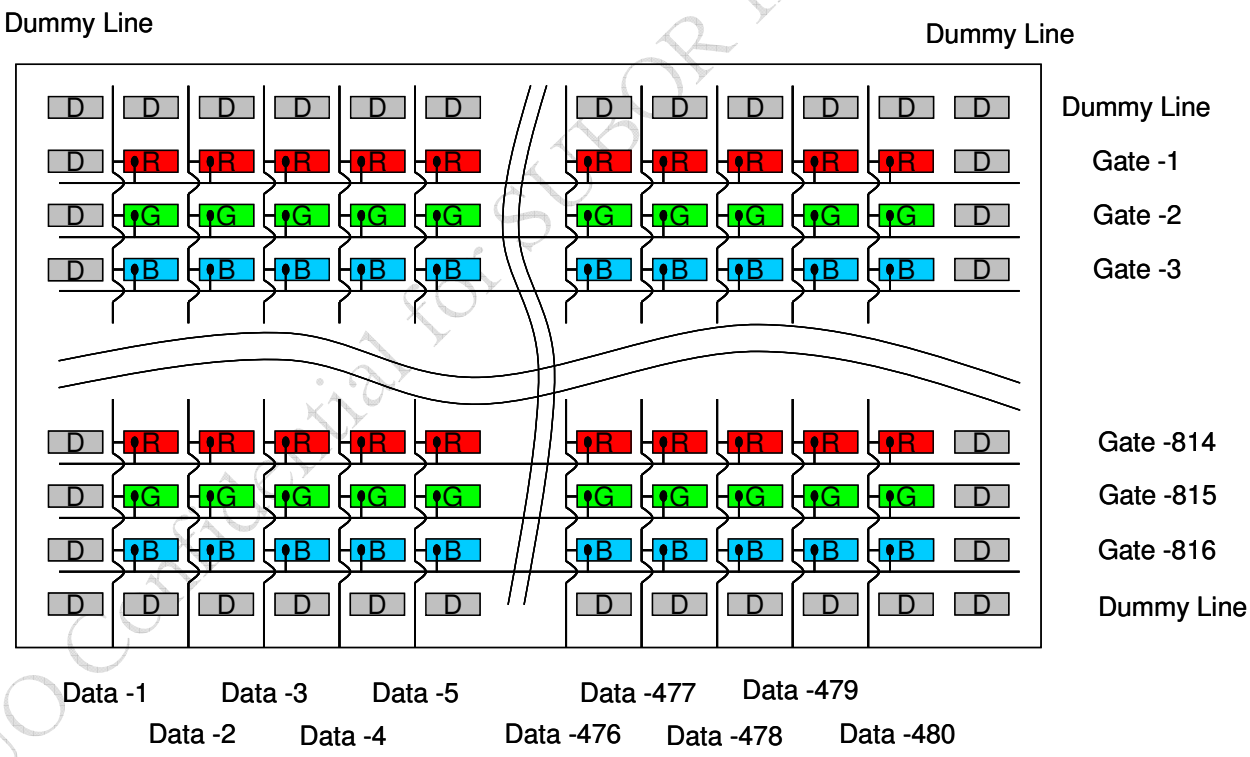
Refer to figure as below.



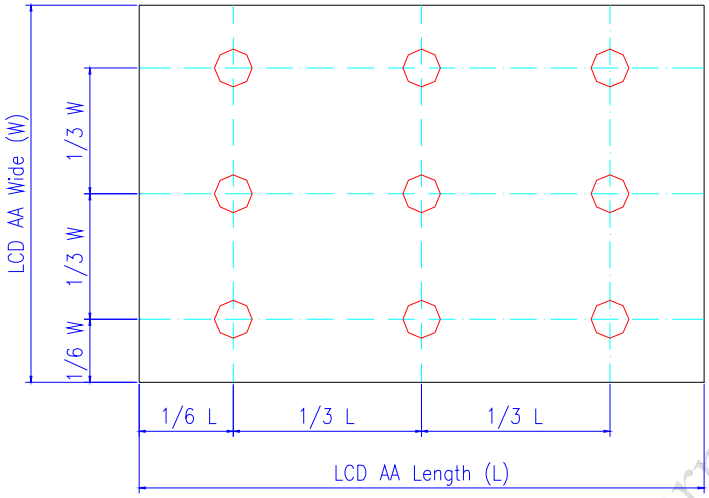


Note 8. Measured at the center area of the panel in gray level 255

Note 9 CF Arrangement



Note 10. Luminance Uniformity of these 9 points is defined as below:



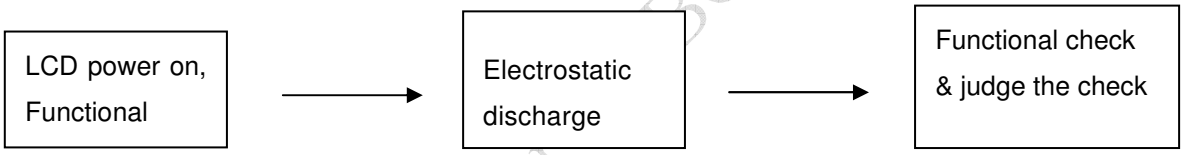
$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

D. Reliability test items:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70℃ 240Hrs	
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	Air mode:+/- 8KV Contact mode: +-4kV	Base on AUO's Standard testing method
8	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
9	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

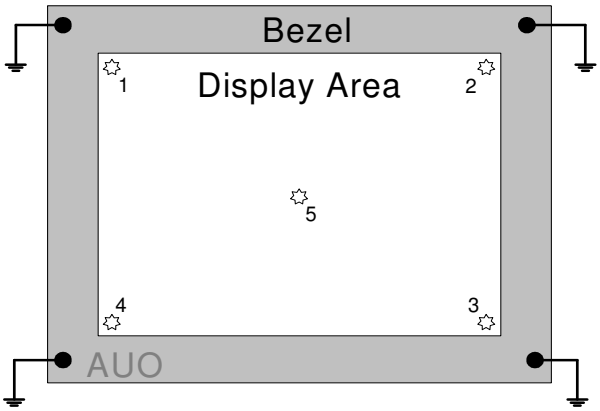
Note: Ta: Ambient temperature.

Note 2. ESD Testing Flow as the below



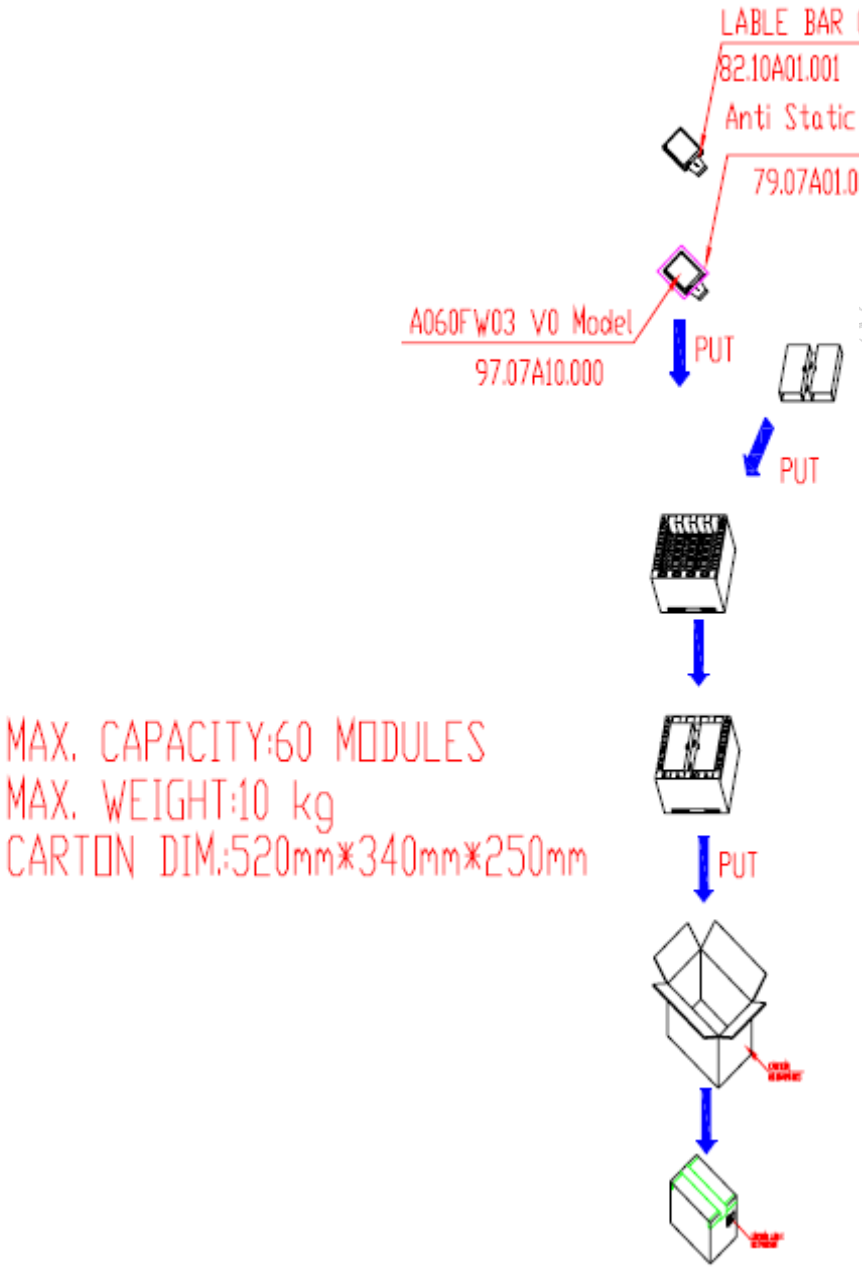
Note 3. ESD testing method.

1. Ambient: 24~26℃, 56~65%RH
2. Instruments:NoisekenESS-2000,
3. Operation System: TBD
4. Test Mode: TBD
5. Test Method:
   a. Contact Discharge: Max±20KV, 150pF(330Ω) 1sec, 5 points, 10 times/point
   b. Air Discharge: Max ±20KV, 150pF(330Ω) 1sec, 5 points, 10 times/point
6. Test point:



7. The metal casing is connected to ground (0V) at four corners.
8. All register commands are repeating transfer.

E. Packing form



F. Outline dimension

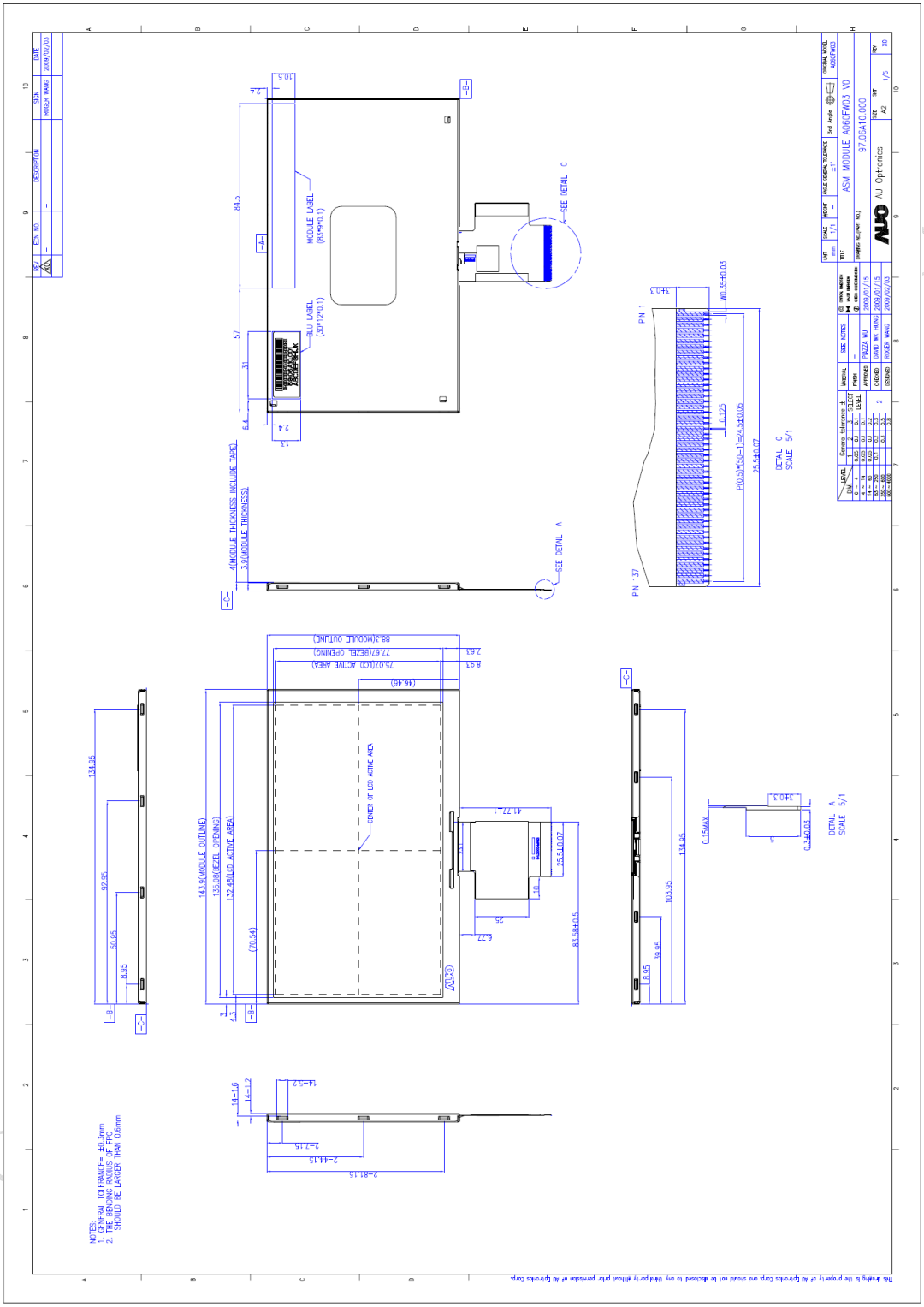


Fig. 1 Outline dimension of TFT-LCD module

"To avoid applying pressure or stress on the products. These will cause visual defects or luminance non-uniformity on the lighting area."

"The protection film in the back side of LCM should be tear off before assembly."