CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A101EVN01.0**
CUSTOMER APPROVED	Title : Name :

- ☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.0)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver. 0.0)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver. 0.0)**
- ☐ **CUSTOMER REMARK :**

Doc. version :	0.0
Total pages :	33
Date :	2011/07/12

Product Specification

10.1" COLOR TFT-LCD PANEL

Model Name：	**A101EVN01.0**
Planned Lifetime:	From 2011/Aug To 2012/Dec
Phase-out Control:	From 2012/Aug To 2012/Dec
EOL Schedule:	2011/Aug

< □ >Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2011/07/12	All	First Draft

Contents

A. General Information

This product is for Netbook application. This product is include cell, POL, driver IC, and FPC.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	10.1 (Diagonal)	
2	Display Resolution	dot	1280 (H) × 800 RGB (V)	
3	Overall Dimension	mm	225.21(H) x145.3(V) x 1.123(T)	Note 1
4	Active Area	mm	216.96(H)×135.6(V)	
5	Pixel Pitch	mm	0.1695(H)×0.1695(V)	
6	Color Configuration	--	R. G. B. Stripe	
7	Color Depth	--	262K Colors	Note 2
8	NTSC Ratio	%	45	
9	Display Mode	--	Normally Black	
10	Panel surface Treatment	--	3H	
11	Weight	g	TBD	
12	Panel Power Consumption	W	TBD	Note 3

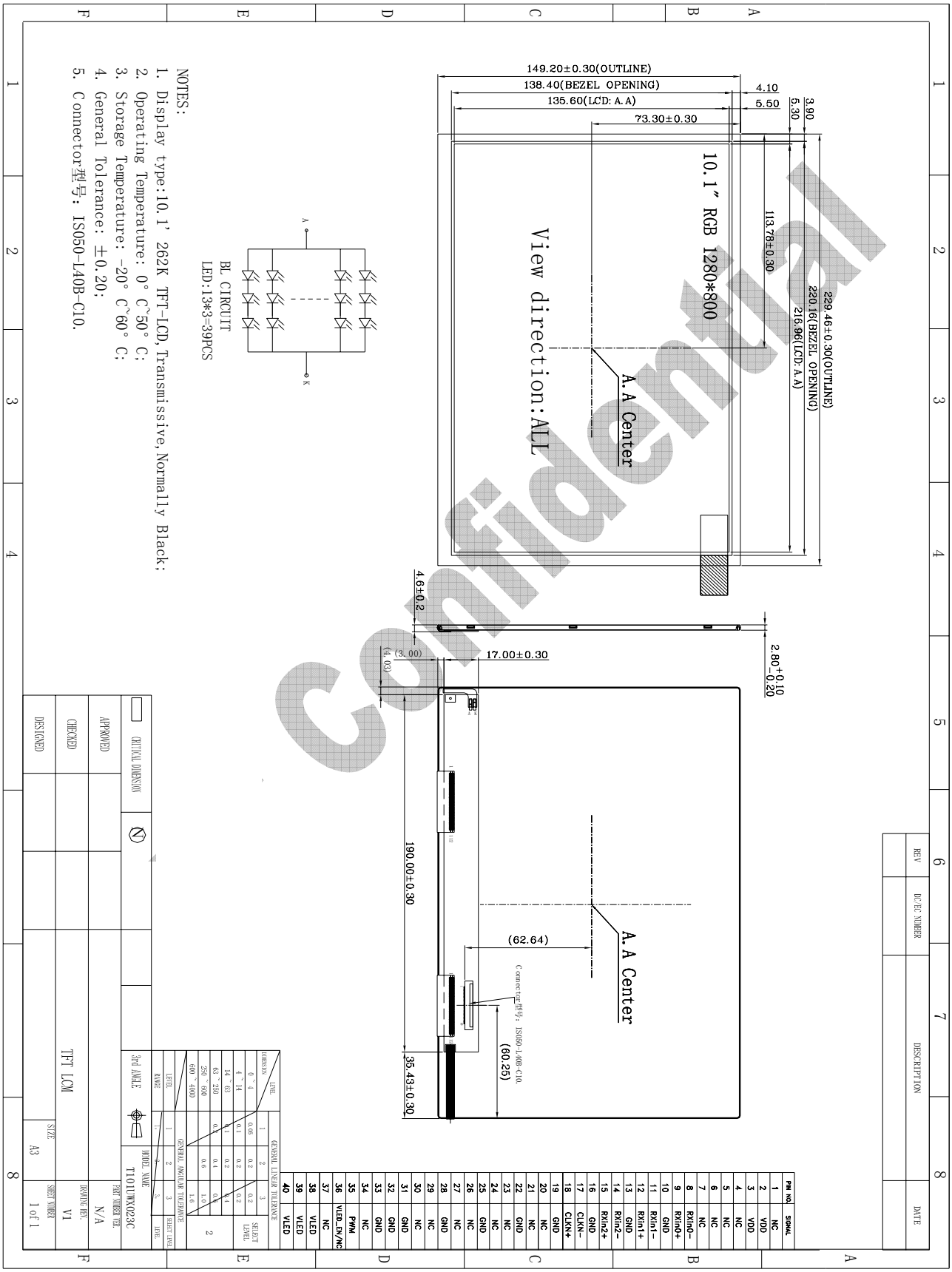
Note 1: Not include blacklight cable and FPC. Refer next page to get further information.

Note 2: The full color display depends on 18-bit data signal (pin 4~27).

Note 3: Please refer to Electrical Characteristics chapter.

B. Outline Dimension

1. TFT-LCD Module



NOTES:

1. Display type:10.1' 262K TFT-LCD, Transmissive, Normally Black;
2. Operating Temperature: 0° C~50° C;
3. Storage Temperature: -20° C~60° C;
4. General Tolerance: ±0.20;
5. Connector型号: IS050-L40B-C10.

BL CIRCUIT
LED:13*3=39PCS

PIN NO.	SIGNAL
1	NC
2	VDD
3	VDD
4	NC
5	NC
6	NC
7	NC
8	RXinD-
9	RXinD+
10	GND
11	RXin1-
12	RXin1+
13	GND
14	RXin2-
15	RXin2+
16	GND
17	CLKN-
18	CLKN+
19	GND
20	NC
21	NC
22	GND
23	NC
24	NC
25	GND
26	NC
27	NC
28	GND
29	NC
30	NC
31	GND
32	GND
33	GND
34	NC
35	PWM
36	VLED_EN/NC
37	NC
38	VLED
39	VLED
40	VLED

REV	DC/EC NUMBER	DESCRIPTION	DATE

DESIGNED		TFT LCM	SIZE A3
CHECKED			DRAWING REV. V1
APPROVED			SHEET NUMBER 1 of 1

CRITICAL DIMENSION

3rd ANGLE

MODEL NAME T101UWX02SC

PART NUMBER REV. N/A

GENERAL LINEAR TOLERANCE				
LEVEL	1	2	3	SELECT LEVEL
DIMENSION				
0 ~ 4	0.05	0.2	0.2	
4 ~ 14	0.1	0.2	0.2	
14 ~ 63	0.1	0.2	0.4	
63 ~ 250	0.1	0.2	0.4	
250 ~ 600	0.1	0.4	0.4	
600 ~ 4000	0.2	0.6	1.0	2

GENERAL ANGULAR TOLERANCE				
LEVEL	1	2	3	SELECT LEVEL
RANGE				
0 ~ 10	0.5°	1°	2°	
10 ~ 50	0.5°	1°	1°	
50 ~ 120	0.5°	0.5°	1°	
120 ~ 400	0.25°	0.5°	1°	
400 ~	0.25°	0.5°	0.5°	2

C. Electrical Specifications

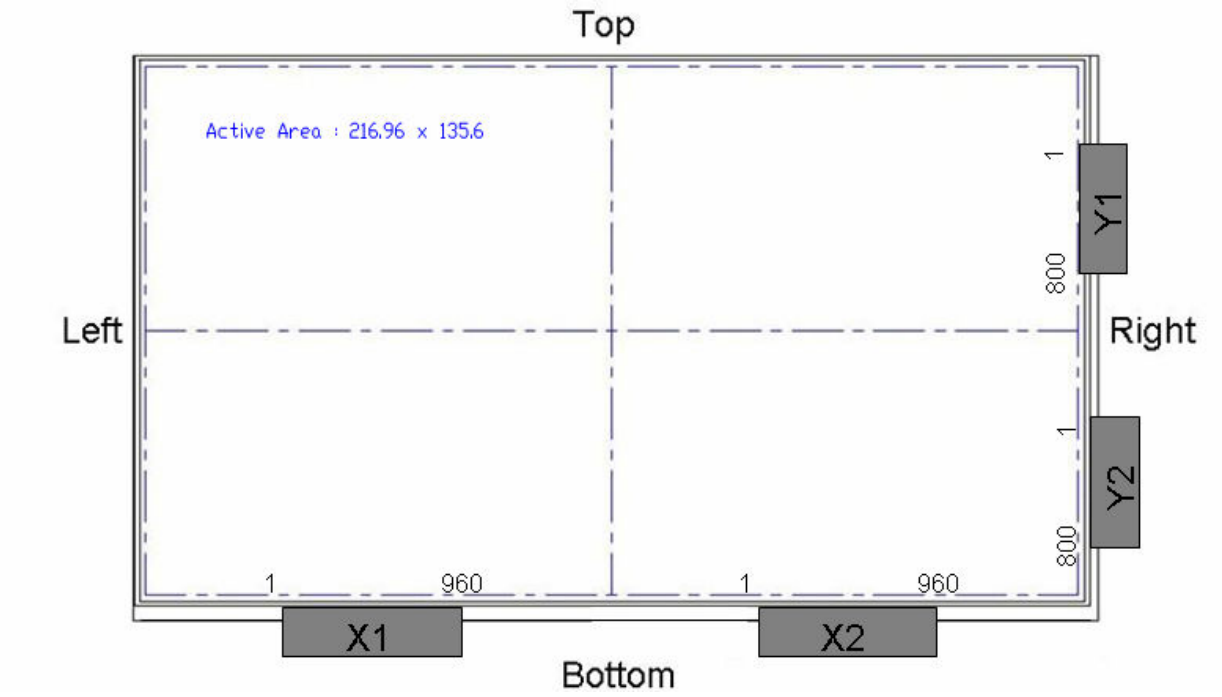
1. FPC Pin Assignment

Pin no	Symbol	I/O	Description
1	VCOM	P	VCOM signal
2	Repair 2	-	RESCUE signal
3	DOI	I/O	Gate start pulse input/output
4	VGL	P	Gate driver negative power supply
5	VGL	P	Gate driver negative power supply
6	VGH	P	Gate driver positive power supply
7	VGH	P	Gate driver positive power supply
8	Vbias	P	Switch driver outputs
9	VCC	P	Gate driver digital power.
10	GND	G	Ground
11	adj	I	Adjustable shading output control pin.
12	YV1C	P	Gate Pulse Modulation
13	OE	I/O	Input/Output pin for the output enable control.
14	XON	I/O	Input/Output pin for the output global on control.
15	CPV	-	Shift clock.Clock signal for internal shift register.
16	CST	-	The internal bypass paths
17	LDIO	I/O	Gate start pulse input/output
18	STB2	O	Data latch control signal for source driver
19	POL2	O	Polarity inversion signal for source driver
20	YDIO2	I/O	Gate start pulse input/output
21	CS0_L	I	control the Charge-Sharing.
22	CS1_L	I	control the Charge-Sharing.
23	RT_SEL0	I	PPmL embedded Rterm control function.
24	RT_SEL	I	
25	SRC_L	I	Slew Rate Control selection pin
26	PATH4R	-	The internal connector bypass paths.
27	PATH3R	-	
28	SEL2	I	Output channel number select pin.
29	DP_SEL1	I	Selects mini-LVDS input mode.
30	DP_SEL0	I	
31	SHL1	I	SHL 1/2 selects start pulse(DIO) left or right shift.
32	SHL2	I	
33	DGND	G	Ground pin for digital circuit.
34	DVDD	P	Power supply for digital circuit

35	AGND	G	Ground pin for analog circuit.
36	AGND	G	Ground pin for analog circuit.
37	AVDD	P	Power supply for analog circuit
38	AVDD	P	Power supply for analog circuit
39	VTOP	P	Power supply for analog circuit
40	VTOP	P	
41	VBOT	P	Power supply for analog circuit
42	VBOT	P	
43	O_HAMP	O	HAMP output pin.
44	O_HAMP	O	HAMP output pin.
45	N_HAMP	I	HAMP negative feedback input pin.
46	I_HAMP	I	HAMP input pin.
47	DGND	G	Ground pin for digital circuit.
48	DGND	G	Ground pin for digital circuit.
49	DVDD	P	Power supply for digital circuit
50	DVDD	P	Power supply for digital circuit
51	LV0P	I	LVDS input RGB data
52	LV0N	I	LVDS input RGB data
53	Shielding GND	G	Shielding Ground.
54	LV1P	I	LVDS input RGB data
55	LV1N	I	LVDS input RGB data
56	Shielding GND	G	Shielding Ground.
57	LV2P	I	LVDS input RGB data
58	LV2N	I	LVDS input RGB data
59	Shielding GND	G	Shielding Ground.
60	LCLKP	I	LVDS input clock.
61	LCLKN	I	LVDS input clock.
62	Shielding GND	G	Shielding Ground.
63	RV0P	I	LVDS input RGB data
64	RV0N	I	LVDS input RGB data
65	Shielding GND	G	Shielding Ground.
66	RV1P	I	LVDS input RGB data
67	RV1N	I	LVDS input RGB data
68	Shielding GND	G	Shielding Ground.
69	RV2P	I	LVDS input RGB data

70	RV2N	I	LVDS input RGB data
71	Shielding GND	G	Shielding Ground.
72	RCLKP	I	LVDS input clock.
73	RCLKN	I	LVDS input clock.
74	DGND	G	Ground pin for digital circuit.
75	DGND	G	Ground pin for digital circuit.
76	AGND	G	Ground pin for analog circuit.
77	AGND	G	Ground pin for analog circuit.
78	VBOT	P	Power supply for analog circuit
79	VBOT	P	
80	VTOP	P	Power supply for analog circuit
81	VTOP	P	
82	AVDD	P	Power supply for analog circuit
83	AVDD	P	Power supply for analog circuit
84	DVDD	P	Power supply for digital circuit
85	PCU1	I	POL Control function
86	D_CON	P	Select control pin left or right shift.
87	PW_SEL	P	Static current control in haif AVDD function.
88	PCU	I	POL control function.
89	RP01	O	The structure of the line-repair amp is the
90	PATH2R	-	The internal connector bypass paths.
91	PATH1R	-	
92	PAVDD	P	Positive Power supply for analog circuit.
93	Dummy	-	Not connect
94	Dummy	-	Not connect
95	Dummy	-	Not connect
96	VGMA1-R	I	Gamma reference voltage.
97	VGMA2-R	I	Gamma reference voltage.
98	VGMA3-R	I	Gamma reference voltage.
99	VGMA4-R	I	Gamma reference voltage.
100	VGMA5-R	I	Gamma reference voltage.
101	VGMA6-R	I	Gamma reference voltage.
102	VGMA7-R	I	Gamma reference voltage.
103	VGMA8-R	I	Gamma reference voltage.
104	VGMA9-R	I	Gamma reference voltage.
105	VGMA10-R	I	Gamma reference voltage.
106	VGMA11-R	I	Gamma reference voltage.
107	VGMA12-R	I	Gamma reference voltage.

108	VGMA13-R	I	Gamma reference voltage.
109	VGMA14-R	I	Gamma reference voltage.
110	CST	-	The internal bypass paths.
111	Repair 1	-	RESCUE signal
112	VCOM	P	VCOM signal



2. Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	XVCC	GND=0	-0.3	2.5	V	Source driver digital power supply
	YVCCA	GND=0	-0.3	2.5	V	Gate driver digital power supply
	AVDD, VTOP	AGND=0	-0.5	+8.5	V	Analog power supply
	VEE – VGG	GND=0	VEE-0.3	VGG+0.3	V	Gate driver supply voltage
Gamma voltage	VGMA1~ VGMA7	AGND = 0	TBD	TBD	V	Gamma reference voltage
	VGMA8~ VGMA14	AGND = 0	TBD	TBD	V	
Input signal voltage	Data	GND=0	-0.5	XVCC+0.5	V	Digital signals

Note 1: Functional operation should be restricted under ambient temperature (25℃).

Note 2: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

3. Electrical DC Characteristics

a. Typical Operation Condition (AGND =GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power voltage	XVCC	2.3	3.3	3.6	V	Source driver digital power supply
	YVCCA	2.3	3.3	3.6	V	Gate driver digital power supply
	AVDD, VTOP		8.5		V	Analog power supply
	VGL		-6.2		V	Gate driver supply voltage
	VGH		23.6		V	
Gamma voltage	VGMA1		TBD		V	Gamma reference voltage (Preliminary only)
	VGMA2		TBD		V	
	VGMA3		TBD		V	
	VGMA4		TBD		V	
	VGMA5		TBD		V	
	VGMA6		TBD		V	
	VGMA7		TBD		V	
	VGMA8		TBD		V	
	VGMA9		TBD		V	
	VGMA10		TBD		V	
	VGMA11		TBD		V	
	VGMA12		TBD		V	
	VGMA13		TBD		V	
	VGMA14		TBD		V	
High level input voltage	V_{IH}	0.7*XVCC	-	XVCC	V	Digital signals
Low level input voltage	V_{IL}	0	-	0.3*XVCC	V	
VCOM	VCOM		2.8		V	

4. Electrical Characteristics

Please refer to Appendix A – Electrical characteristics.

5. Power On/Off Sequence

Please refer to Applendix A – Power on/off sequence

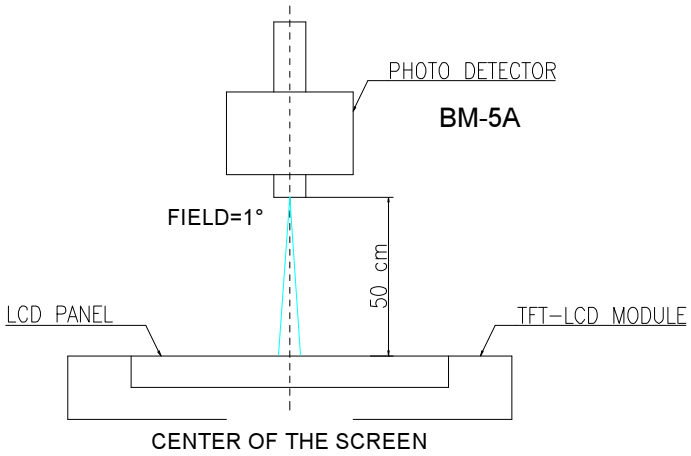
D. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

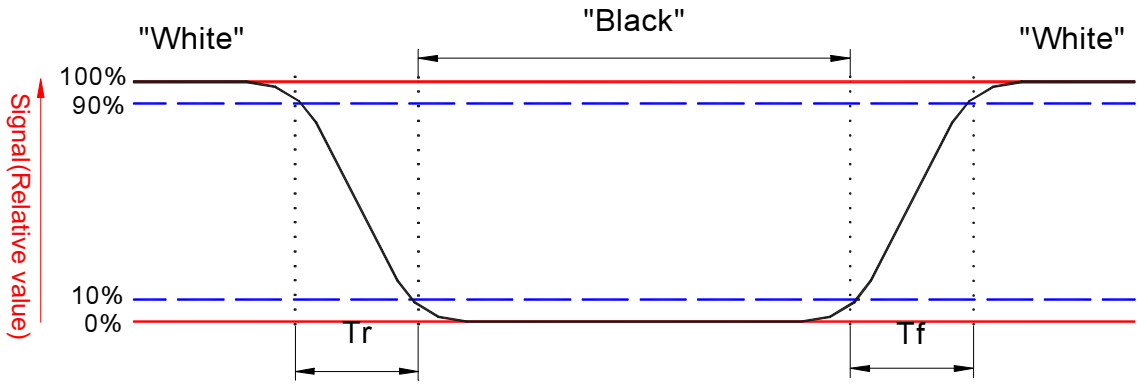
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise + Fall	T_{RT}	θ=0°	--	25	35	ms	Note 3
Contrast ratio	CR	At optimized viewing angle	1000	1300	--		Note 4, 7
Viewing Angle Top		CR□10	80	85	--	deg.	Note 5,7
Viewing Angle Bottom			80	85	--		
Viewing Angle Left			80	85	--		
Viewing Angle Right			80	85	--		
Transmittance	Y_L	θ=0°	4.3	4.64	--	%	Note 6

Note 1: Ambient temperature =25℃. To be measured in the dark room.

Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.



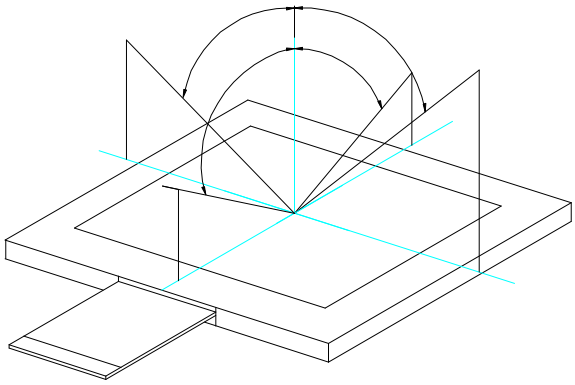
Note 3: Definition of response time:
The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.
The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 4.Definition of contrast ratio:
Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

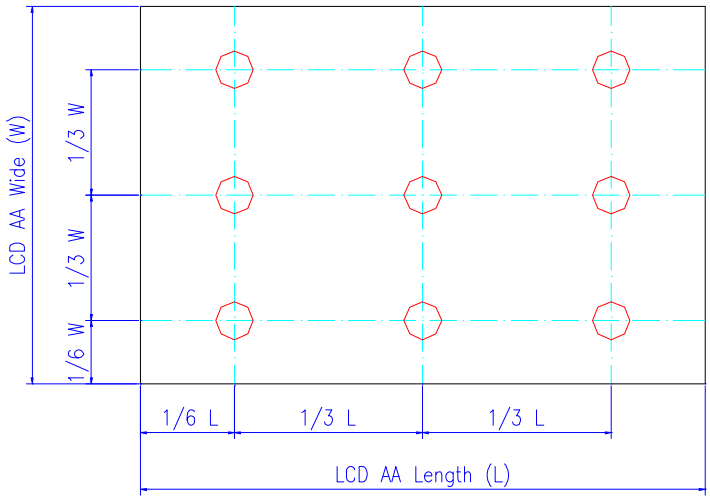
Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7. The data is from AUO model **B101EW05** with same panel of **A101EVN01.0**

Note 8: Luminance Uniformity of these 9 points is defined as below:



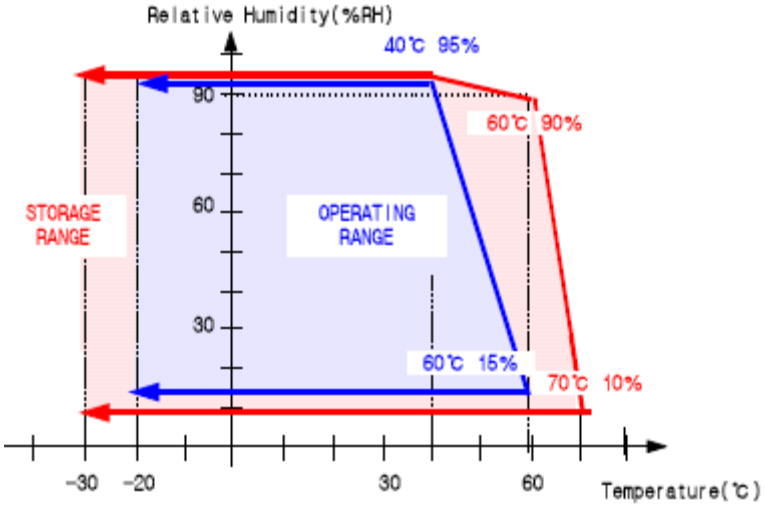
$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

E. Reliability Test Items

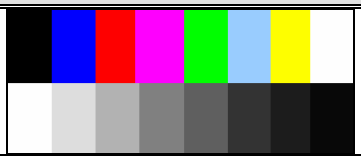
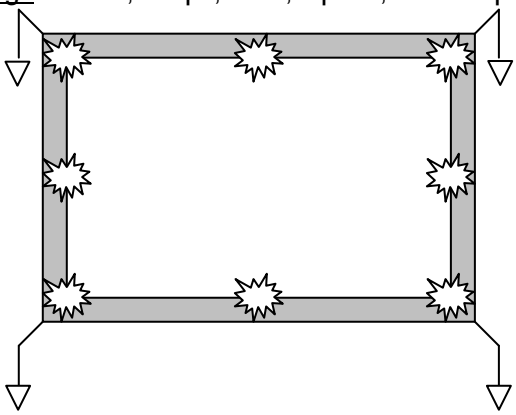
No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 60℃ 240Hrs	
2	Low Temperature Storage	Ta= -20℃ 240Hrs	
3	High Ttemperature Operation	Ta= 50℃ 240Hrs	
4	Low Temperature Operation	Ta= 0℃ 240Hrs	
5	High Temperature & High Humidity	Ta= 40℃. 90% RH 240Hrs	Operation
6	Heat Shock	-20℃~60℃, 50 cycle, 1Hrs/cycle	Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B	Note 5
8	Image Sticking	Romm temperature(室溫), 4hrs release 20mins	Note 6
9	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55~10Hz 2 hours for each direction of X,Y,Z	Non-operation JISC 7021
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1: Ta: Ambient Temperature. Tp: Panel Surface Temperature
Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.
Note 3: All the cosmetic specification is judged before the reliability stress.

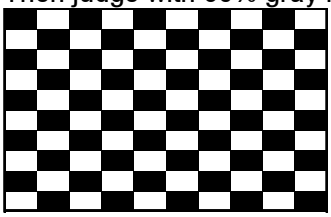
Note 4: temperature and relative umidity range is shown in the figure below



Note5 : All test techniques follow IEC6100-4-2 standard.

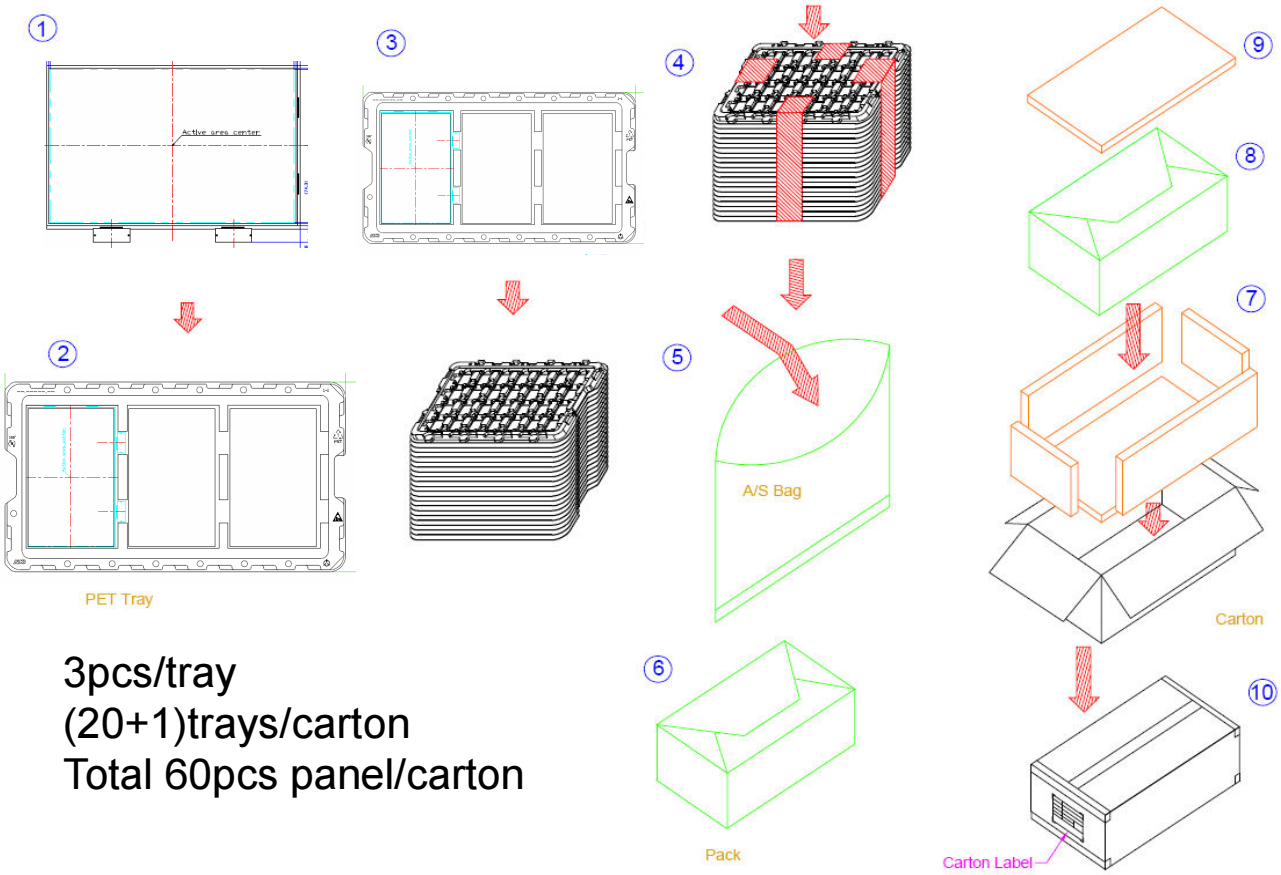
Test Condition		Note
Pattern		
Procedure And Set-up	Contact Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point Air Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point 	
Criteria	B – Some performance degradation allowed. No data lost. Self-recoverable hardware failure.	
Others	1. Gun to Panel Distance 2. No SPI command, keep default register settings.	

Note 6: Operate with chess board pattern as figure and lasting time and temperature as the conditions. Then judge with 50% gray level, the mura is less than JND 2.5



F. Packing and Marking

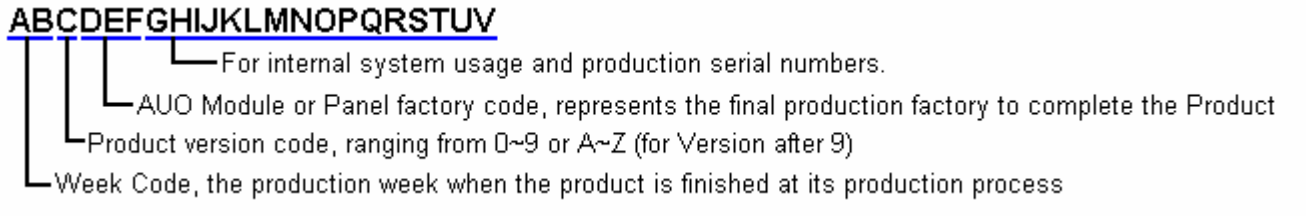
1. Packing Form



3pcs/tray
(20+1)trays/carton
Total 60pcs panel/carton

2. Panel Label Information

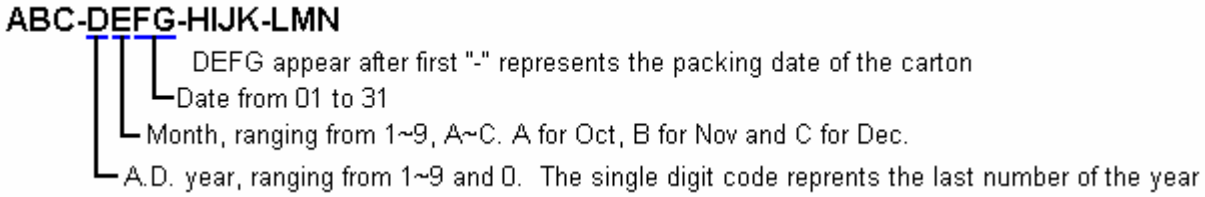
In the carton box, the panel (collectively called as the “Product”) will be with a label of Shipping Number which represents the identification of the Product at a specific location. The label is composed of a 22-digit serial number with the following definition:



Example:
501M06ZL06123456781Z05:
Product Manufacturing Week Code: WK50
Product Version: Version 1
Product Manufactuing Factory: M06

3. Carton Label Information

The packing carton will be attached with a carton label where packing Q’ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:



Refer to the drawing of packing format for the location and size of the carton label.

G. Application Note

1. Application Circuit

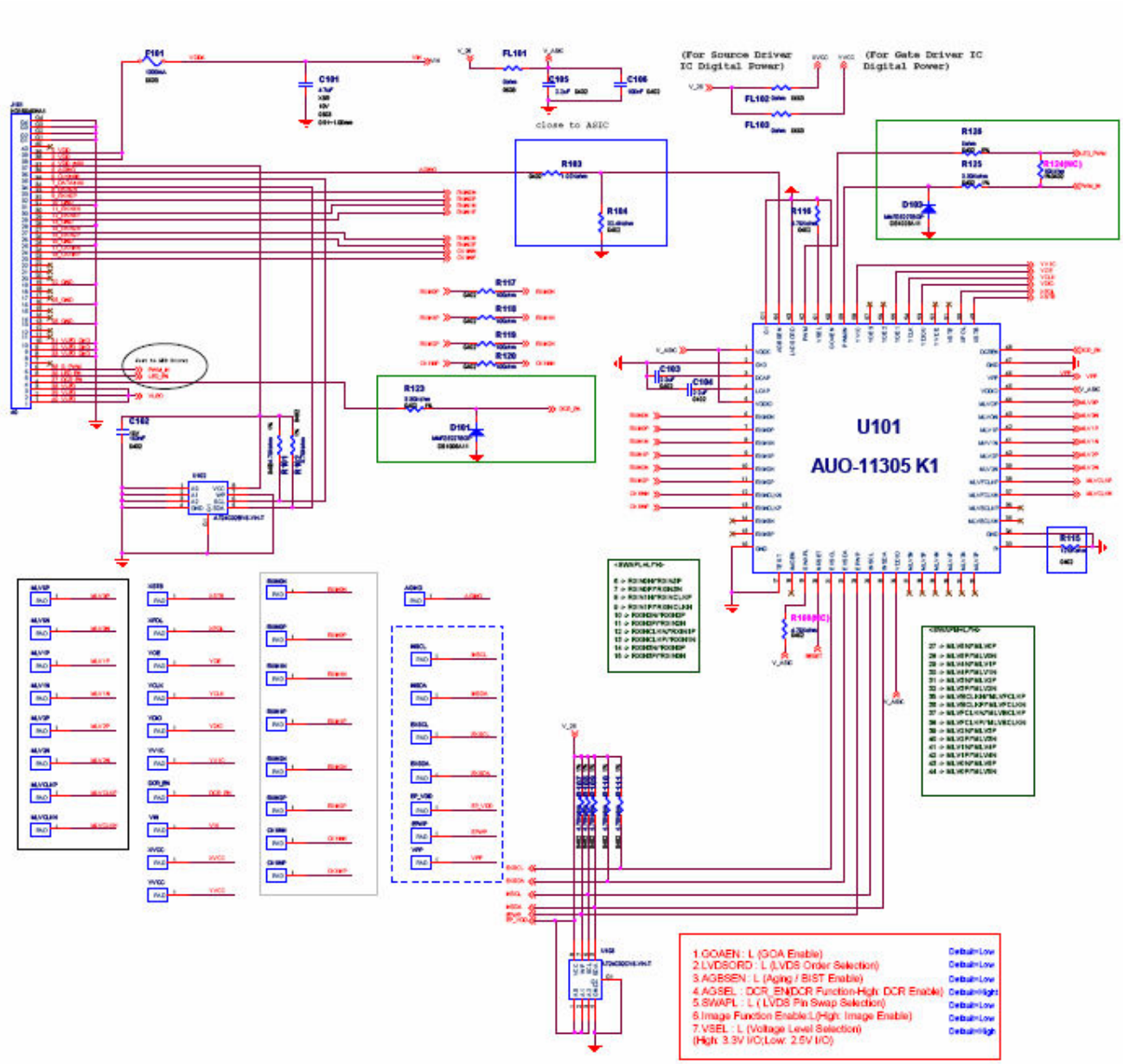
Please refer to Appendix A – Electrical characteristics.

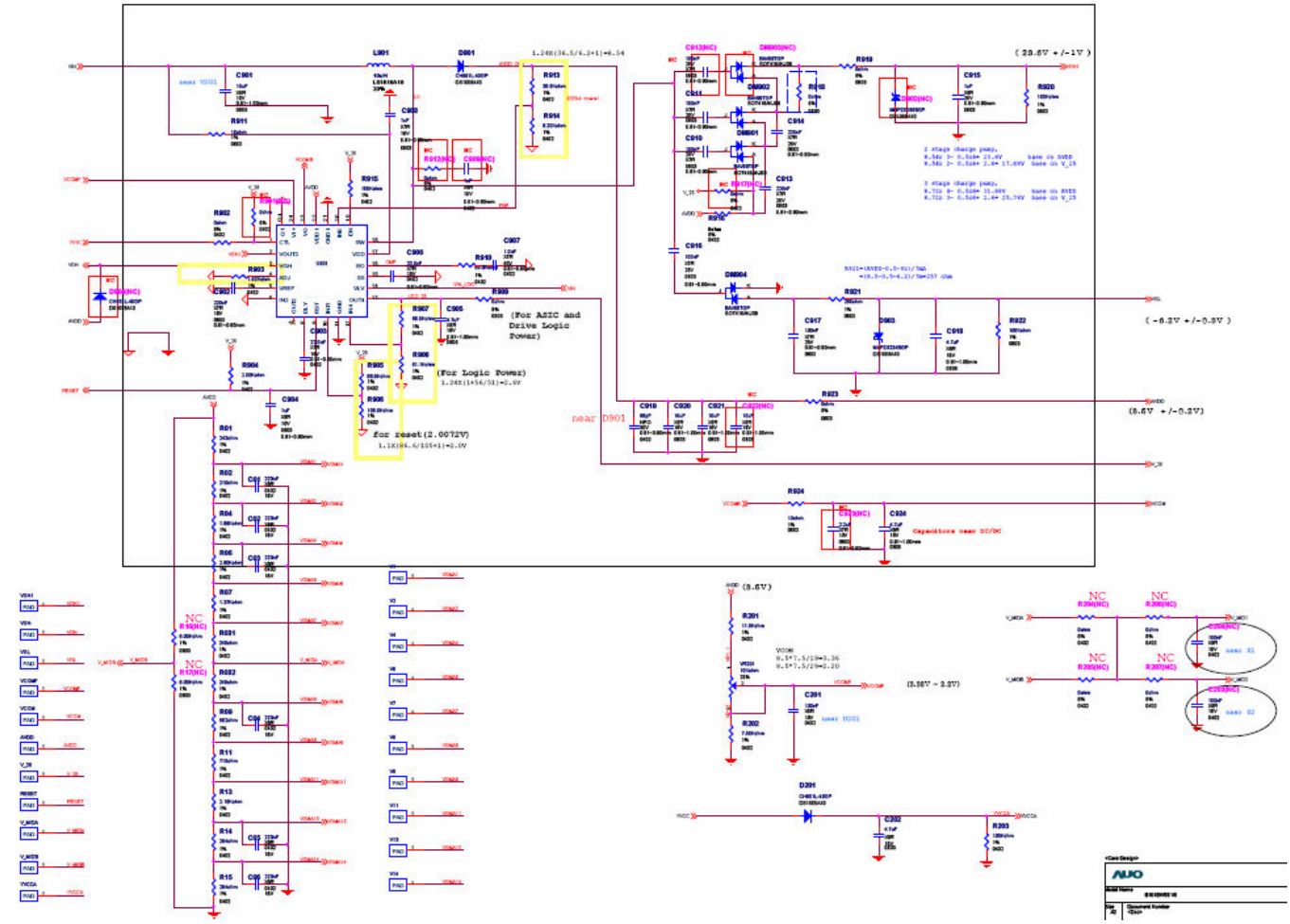
H. Precautions

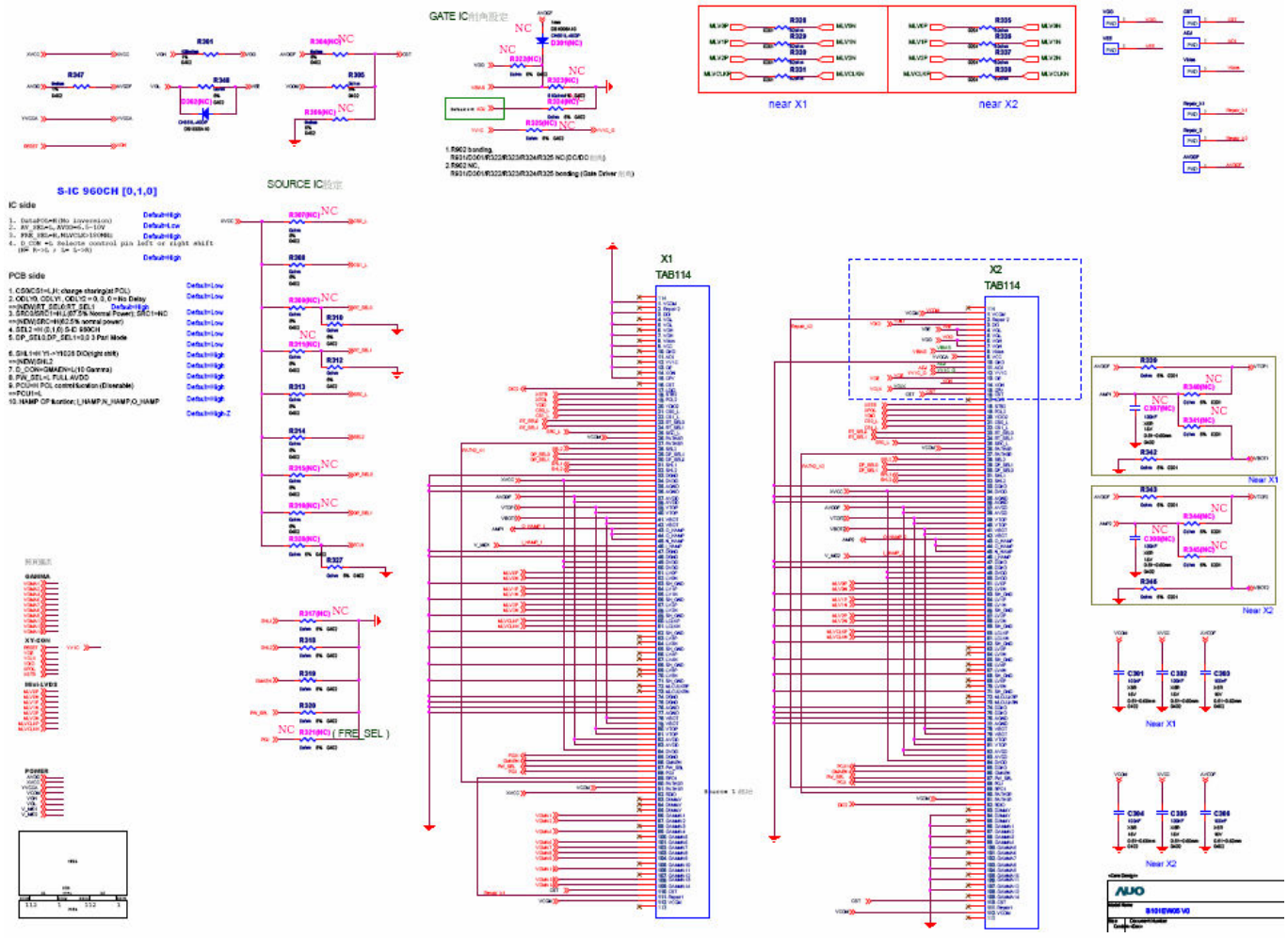
1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.

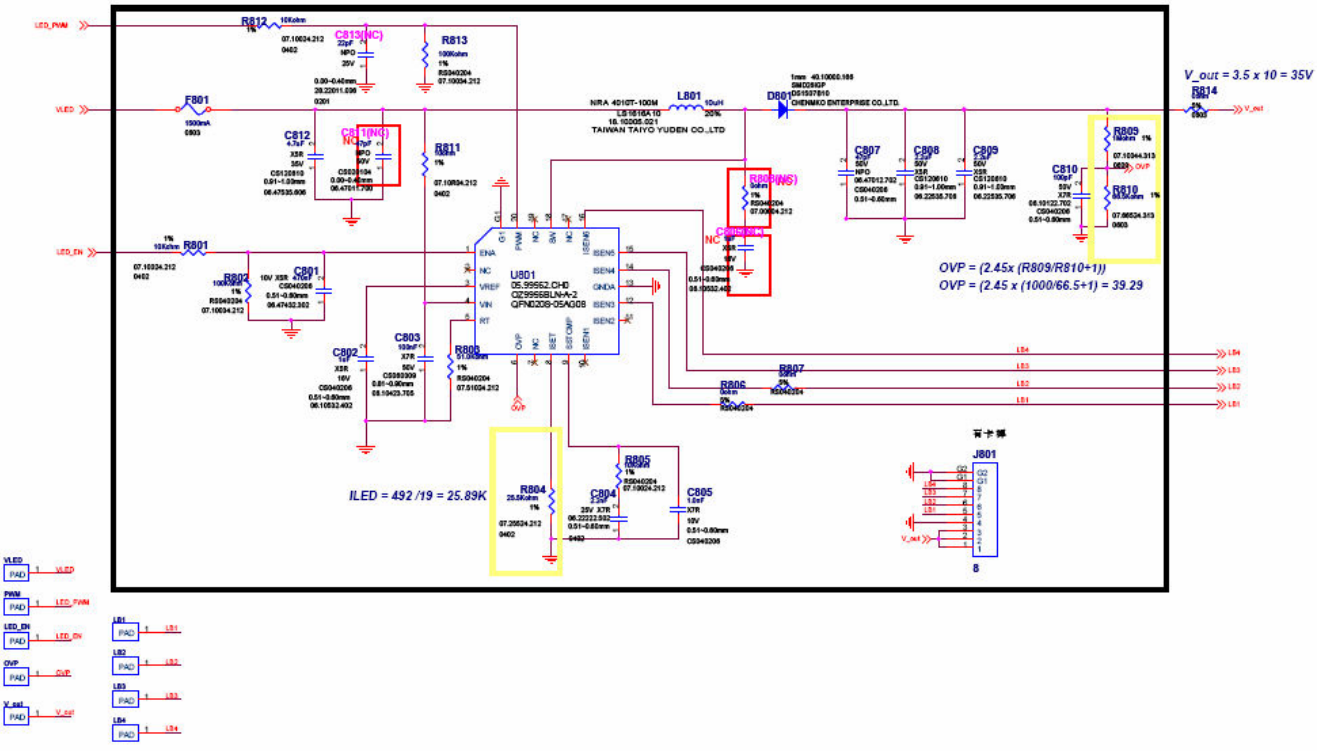
Appendix A: Recommended Application Circuits with specifications

A.1 Application circuit (Bill of material is different to these schematics)



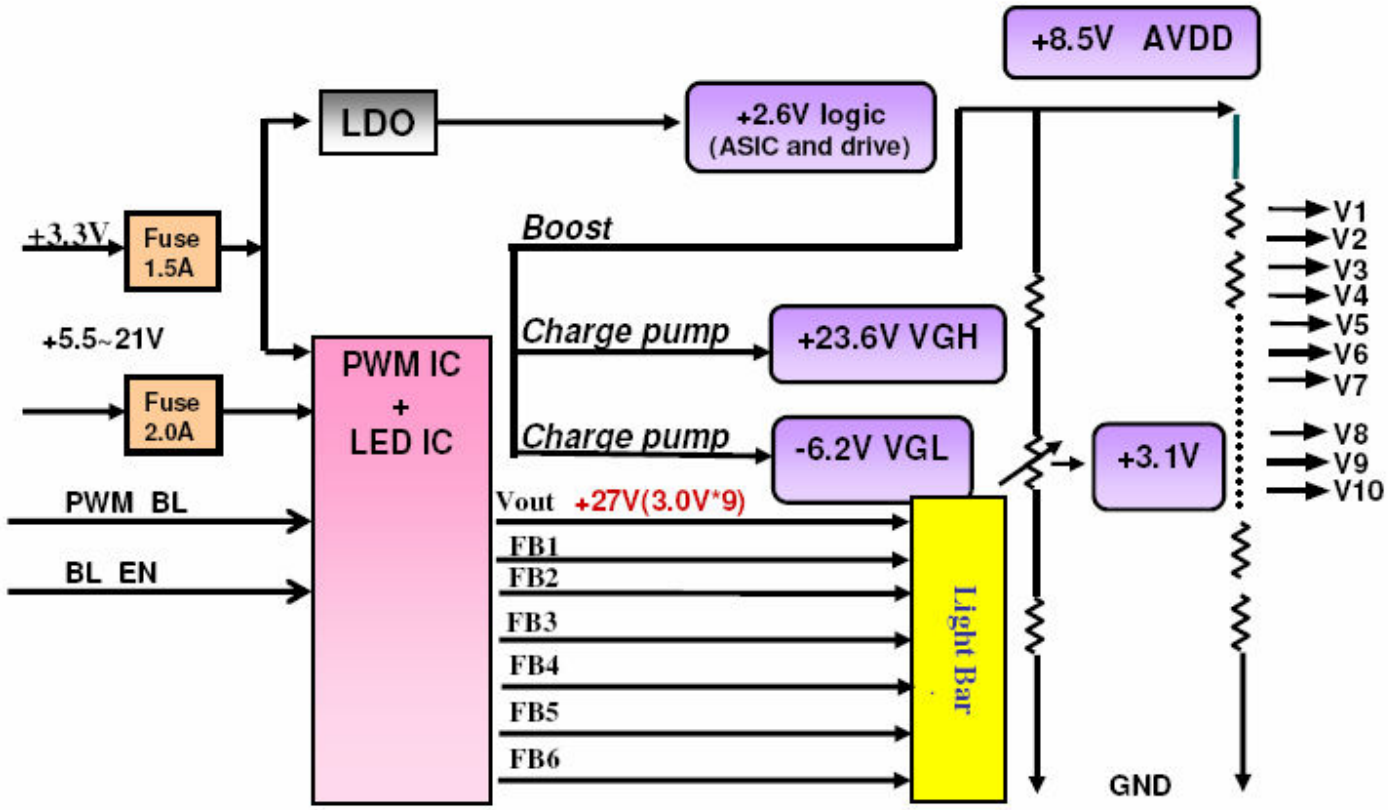

(28.6V +/-1V)
(-6.2V +/-0.5V)
(8.6V +/-0.2V)
(For ASIC and Drive Logic Power)
(For Logic Power)
for reset(2.0072V)
near D901


S-IC 960CH [0,1,0]
SOURCE IC
GATE IC
near X1
near X2
X1
TAB114
X2
TAB114
Near X1
Near X2
(FRE_SEL)

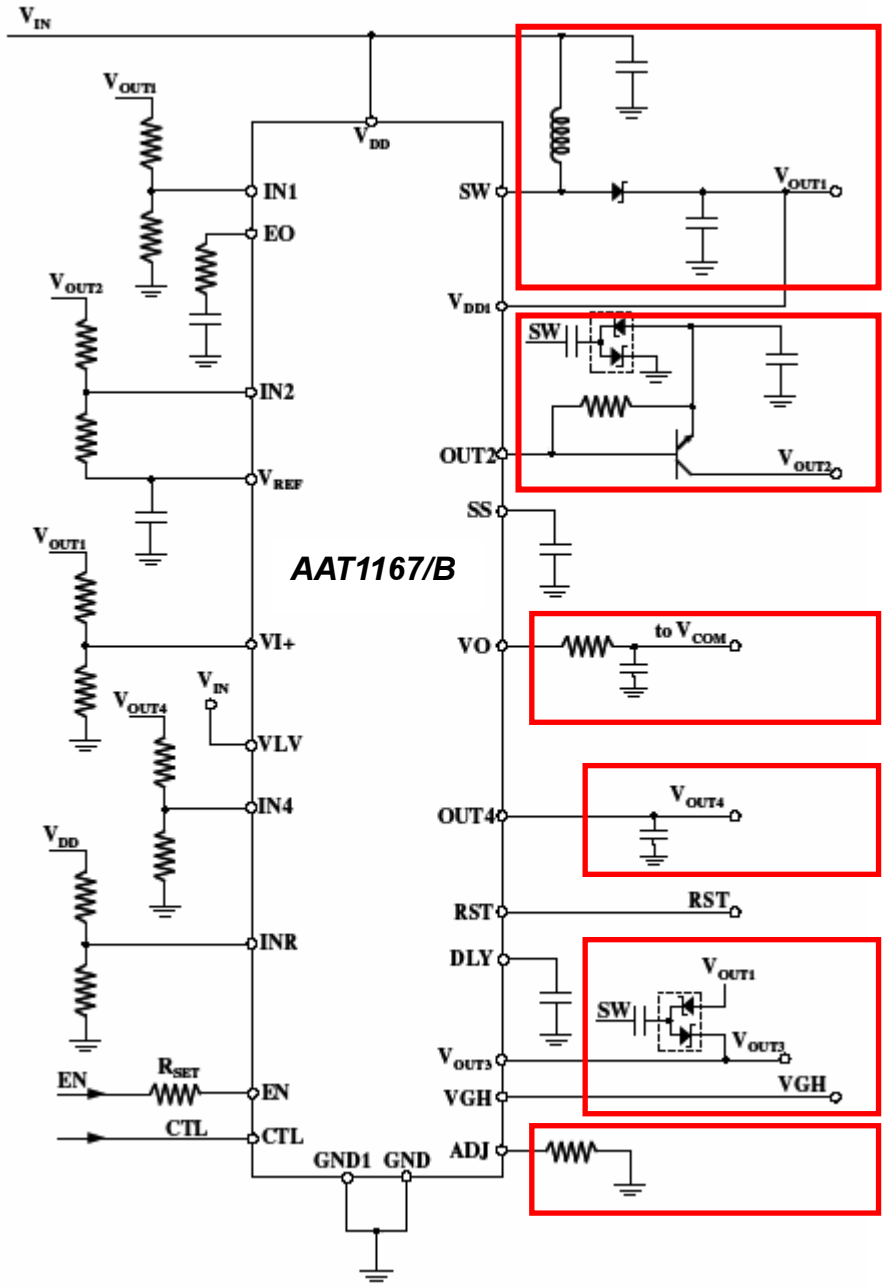

V_out = 3.5 x 10 = 35V
OVP = (2.45x (R809/R810+1))
OVP = (2.45 x (1000/66.5+1) = 39.29
ILED = 492 /19 = 25.89K
U801
QFN0208-05AG08
L801
D801
J801

1.Power Architecture: (for reference)

Item	Description	Voltage (V)
V_{in}	Input Voltage	3.30
AVDD	Analog Voltage	8.5
DVDD	Digital Voltage	2.6
VGH	Gate On Voltage	+ 23.6
VGL	Gate Off Voltage	- 6.2
Vcom		3.1



2.PWM Function Block: (for reference)



AVDD Block

VGL Block

VCOM Block

LDO Block

VGH Block

VGH Fall Time Setting

A.2 Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

A.2.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

A.3 Electrical characteristics

A.3.1 TFT LCD Module

A.3.1.1 Power Specification

Input power specifications are as follows;

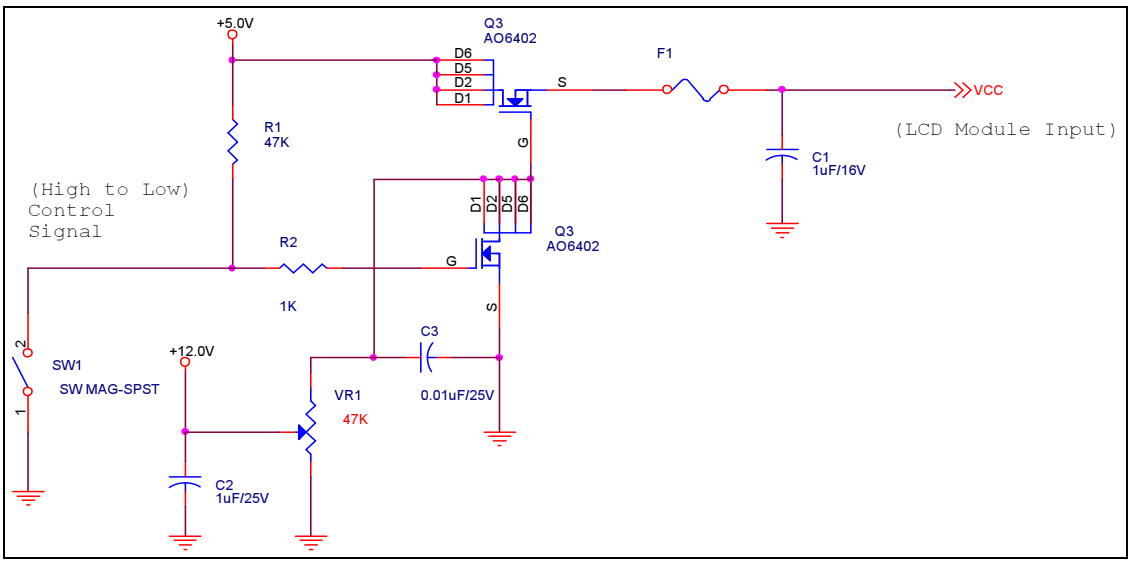
The power specification are measured under 25□ and frame frenquency under 60Hz

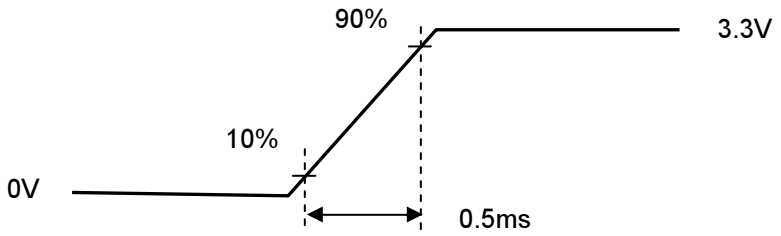
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.7	[Watt]	Note 1
IDD	IDD Current	-	-	212	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern at 3.3V driving voltage.(Pmax=3.3 x I_{black})

Note 2：Typical Measurement Condition: Mosaic Pattern

Note 3：Measure Condition





Vin rising time

A.3.1.2 Signal Electrical Characteristics:

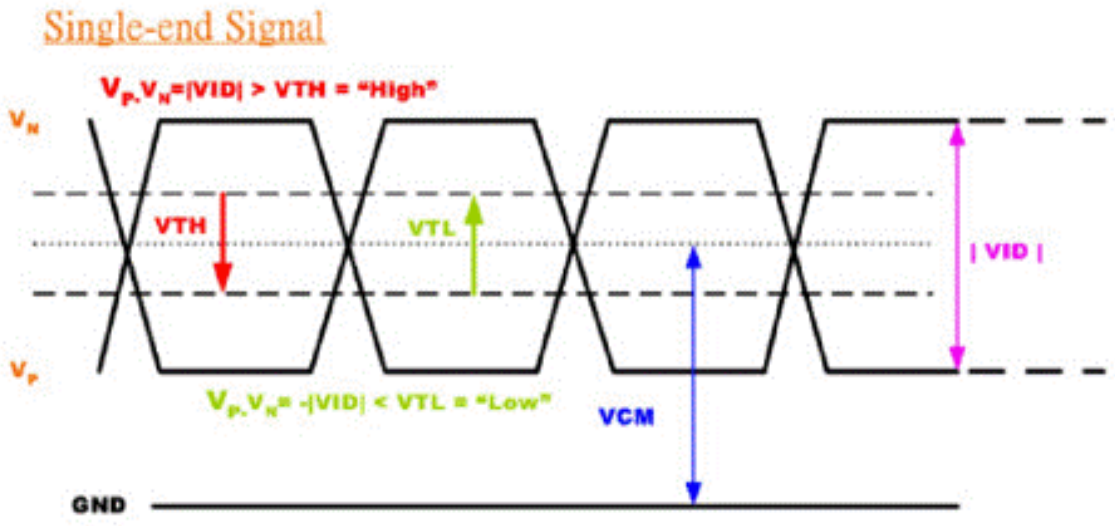
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of SN75LVDS82DGG (Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{TH}	Differential Input High Threshold (Vcm=+1.2V)	---	100	[mV]
V_{TL}	Differential Input Low Threshold (Vcm=+1.2V)	-100	----	[mV]
$\|V_{ID}\|$	Differential Input Voltage	100	600	[mV]

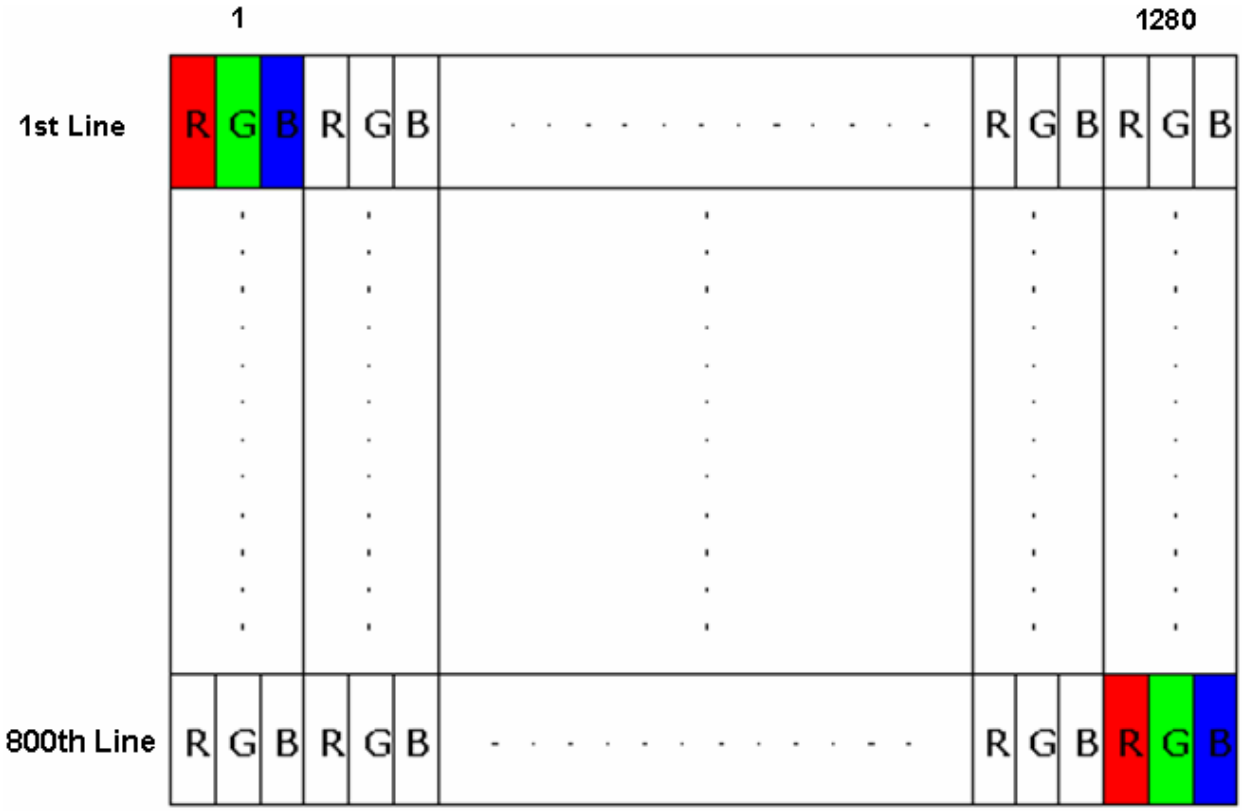
Note: LVDS Signal Waveform



A.4 Signal Characteristic

A.4.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



A.4.2 The input data format:

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

A.4.3 Input Interface:

4.3-1:LVDS connector and pin define and description:

PIN#	Signal Name	Description
1	NC	No Connection (Reserve)
2	AVDD	Power Supply +3.3V
3	AVDD	Power Supply +3.3V
4	VEDID	EDID +3.3V Power
5	NC	No Connection (Reserve)
6	CLK_EDID	EDID Clock Input
7	DAT_EDID	EDID Data Input
8	Rin0-	-LVDSdifferential data input(R0-R5,G0)
9	Rin0+	+LVDSdifferential data input(R0-R5,G0)
10	GND	Ground
11	Rin1-	-LVDSdifferential data input(G1-G5,B0-B1)
12	Rin1+	+LVDSdifferential data input(G1-G5,B0-B1)
13	GND	Ground
14	Rin2-	-LVDSdifferential data input(B2-B5,HS,VS,DE)
15	Rin2+	+LVDSdifferential data input(B2-B5,HS,VS,DE)
16	GND	Ground
17	ClkIN-	-LVDSdifferential clock input
18	ClkIN+	+LVDSdifferential clock input
19	GND	Ground–Shield
20	NC	No Connection (Reserve)
21	NC	No Connection (Reserve)
22	GND	Ground–Shield
23	NC	No Connection (Reserve)
24	NC	No Connection (Reserve)
25	GND	Ground–Shield
26	NC	No Connection (Reserve)
27	NC	No Connection (Reserve)
28	GND	Ground–Shield
29	NC	No Connection (Reserve)
30	NC	No Connection (Reserve)
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection (Reserve)
35	VPWM_EN	System PWM Logic Input Level
36	VLED_EN	LED enable input level

37	DCR_EN	DCR enable input level
38	VLED	LED Power Supply
39	VLED	LED Power Supply
40	VLED	LED Power Supply

A.5 Interface Timing

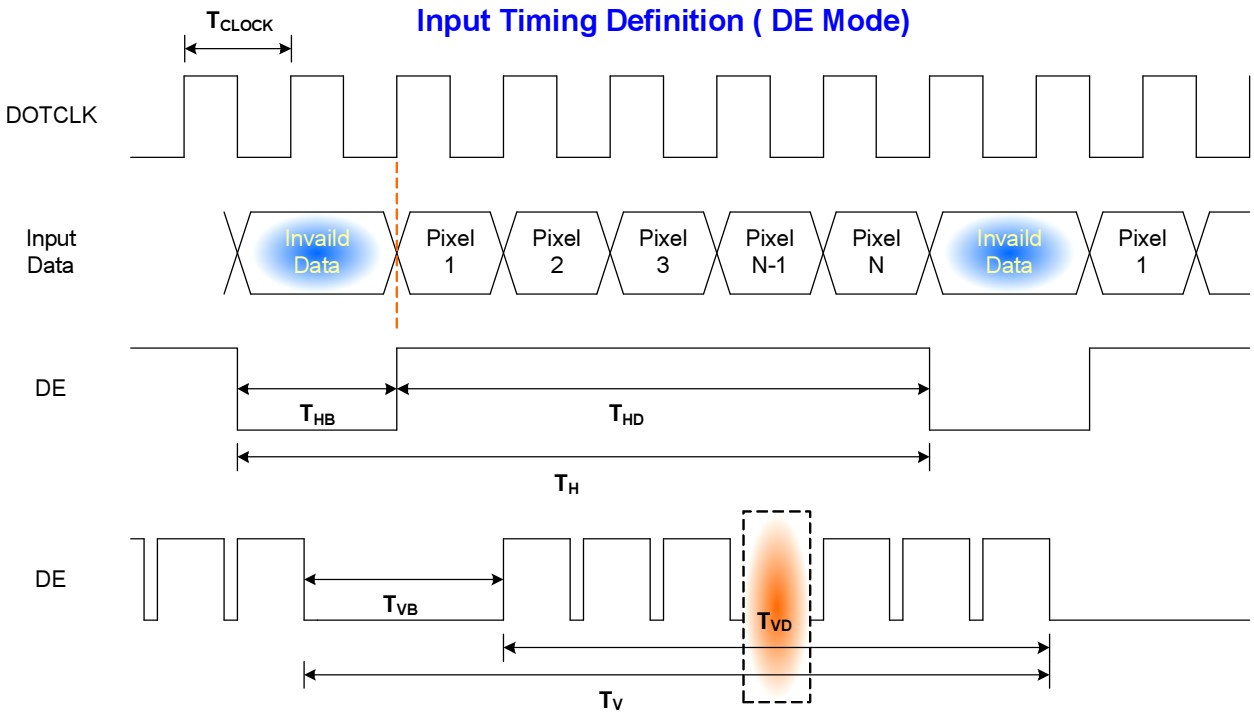
A.5.1 Timing Characteristics

Basically, interface timings should match the 1280 x 800 /60Hz manufacturing guide line timing..

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T_{Clock}	64	68.93	85	MHz
Vertical Section	Period	T_V	808	816	1023	T_{Line}
	Active	T_{VD}	800			
	Blanking	T_{VB}	8	16	223	
Horizontal Section	Period	T_H	1310	1408	2047	T_{Clock}
	Active	T_{HD}	1280			
	Blanking	T_{HB}	40	168	767	

Note : DE mode only

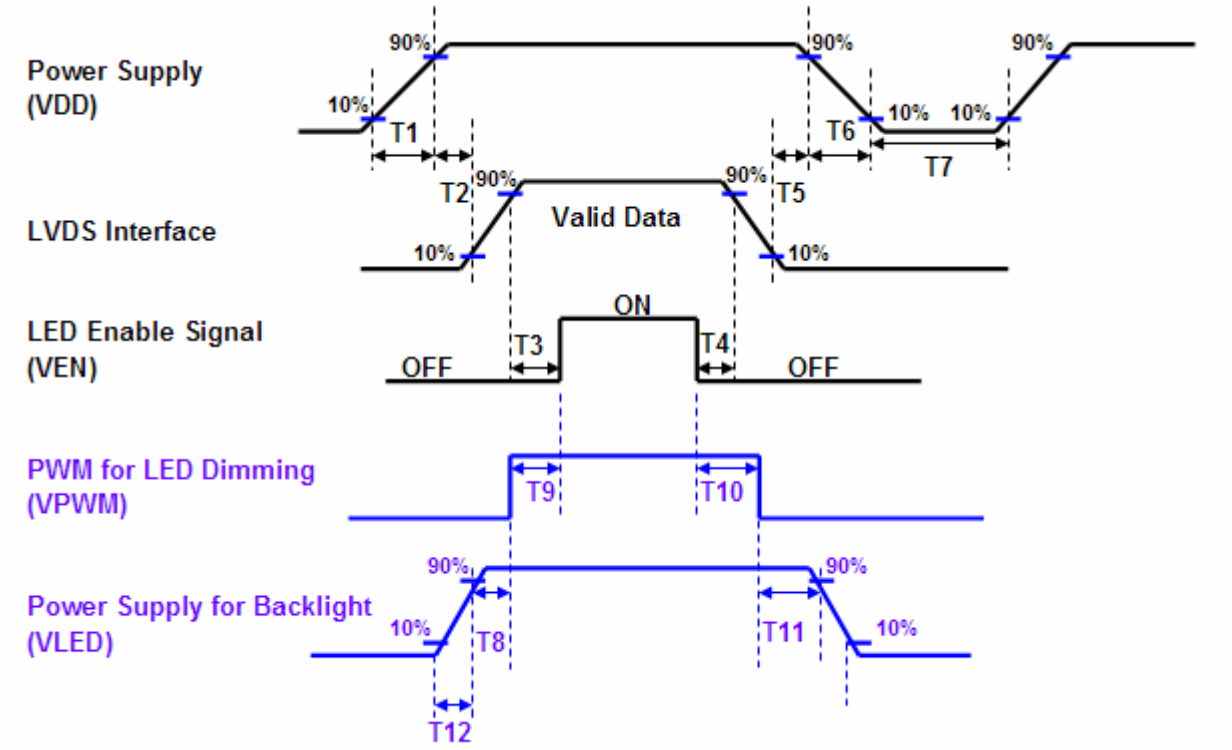
6.5.2 Timing diagram



A.6 Power ON/OFF Sequence:

A.6.1 Panel Power Sequence

VDD power and PWM on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



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Power Sequence Timing	Power Sequence Timing			Power Sequence Timing
	Parameter	Parameter	Parameter	
T1	T1	T1	T1	T1
T2	T2	T2	T2	T2
T3	T3	T3	T3	T3
T4	T4	T4	T4	T4
T5	T5	T5	T5	T5
T6	T6	T6	T6	T6
T7	T7	T7	T7	T7
T8	T8	T8	T8	T8
T9	T9	T9	T9	T9
T10	T10	T10	T10	T10
T11	T11	T11	T11	T11