(V) Preliminary Specifications
( ) Final Specifications

Module	20.1” WSXGA+ Color TFT-LCD
Model Name	B201SW01 V0

Customer	**Date**	**Approved by**	**Date**
Checked & Approved by	**Date**	**Prepared by**	**Date**
Note: This Specification is subject to change without notice.		NBBU Marketing Division / AU Optronics corporation	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2006/11/10	All	First Edition		
0.2 2006/12/13	30		Add shipping label format	
0.2 2006/12/13	32		Add EDID data	
0.3 2007/4/13	6	White Luminance (ICCFL=6.0mA)	White Luminance (ICCFL=7.5mA)	
0.4 2007/5/8	5~29		Add specifications	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

2. General Description

B201SW01 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WSXGA+ (1680(H) x 1050(V)) screen and 16.7M colors (RGB 6-bits data driver with frame rate control). All input signals are LVDS interface compatible. Inverter of backlight is not included.

B201SW01 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

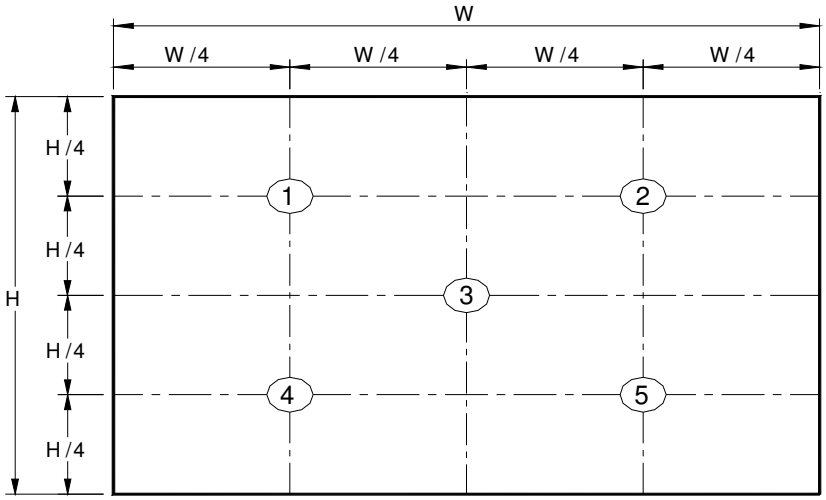
Items	Unit	Specifications
Screen Diagonal	[mm]	511.1 (20.1W")
Active Area	[mm]	433.4 X 270.9
Pixels H x V		1680x3(RGB) x 1050
Pixel Pitch	[mm]	0.258X0.258
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (I_{CCFL}=7.5mA) Note: I_{CCFL} is lamp current	[cd/m^2]	300 typ. (5 points average) 255 min. (5 points average) (Note1)
Luminance Uniformity		1.25 typ. (5 points)
Contrast Ratio		1000 typ 800 min.
Optical Rise Time/Fall Time	[msec]	max 8/typ 5
Nominal Input Voltage VDD	[Volt]	+5.0 typ.
Power Consumption	[Watt]	18.0 typ.(without inverter)
Weight	[Grams]	1250 typ. 1310 max.
Physical Size	[mm]	453.5 typ. x 296.5 typ. x 8.6 max
Electrical Interface		2-channel LVDS
Surface Treatment		Glare, Hardness 3H, Reflectance <=4.5%
Support Color		16.7M colors
Temperature Range Operating Storage (Non-Operating)	 [^{o}C] [^{o}C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

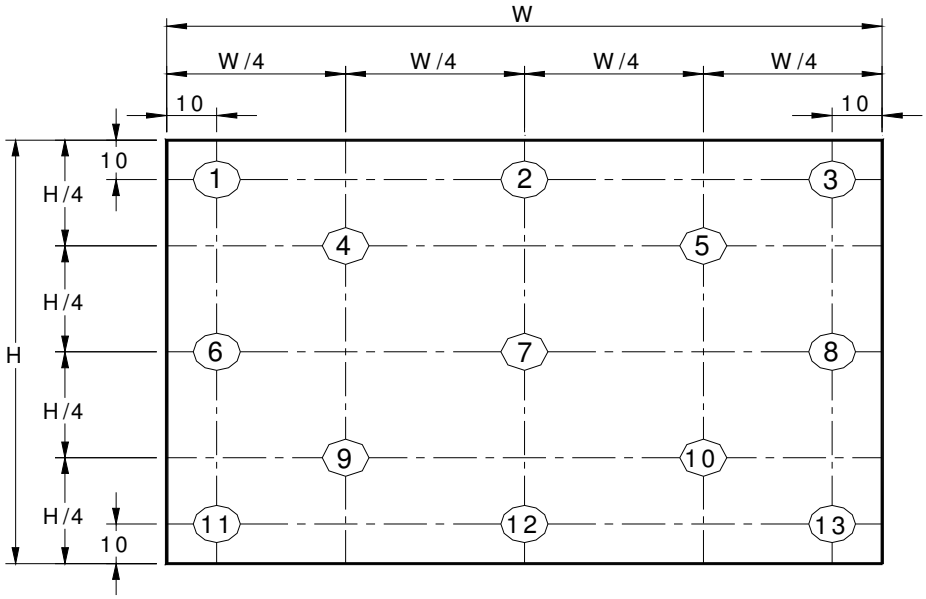
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance I_{CCFL}=7.5mA	[cd/m^2]	5 points average	255	300	-	1, 4, 5.
Viewing Angle	[degree]	Horizontal (Right) CR = 10	60	80	-	8
	[degree]	(Left)	60	80	-	
	[degree]	Vertical (Upper) CR = 10	60	80	-	
	[degree]	(Lower)	60	75	-	
Luminance Uniformity		5 Points		1.25	1.35	1
Luminance Uniformity		13 Points		1.67	2.00	2
CR: Contrast Ratio			800	1000	-	6
Cross talk	%				4	7
Response Time	[msec]	Rising	-	3.8	5.7	8
	[msec]	Falling	-	1.2	2.3	
	[msec]	Rising + Falling		5.0	8.0	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.619	0.649	0.679	2,8
		Red y	0.308	0.338	0.368	
		Green x	0.259	0.289	0.319	
		Green y	0.579	0.609	0.639	
		Blue x	0.116	0.146	0.176	
		Blue y	0.040	0.070	0.100	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	

Note 1: 5 points position (Display area : 433.4mm x 270.9mm)



Note 2: 13 points position



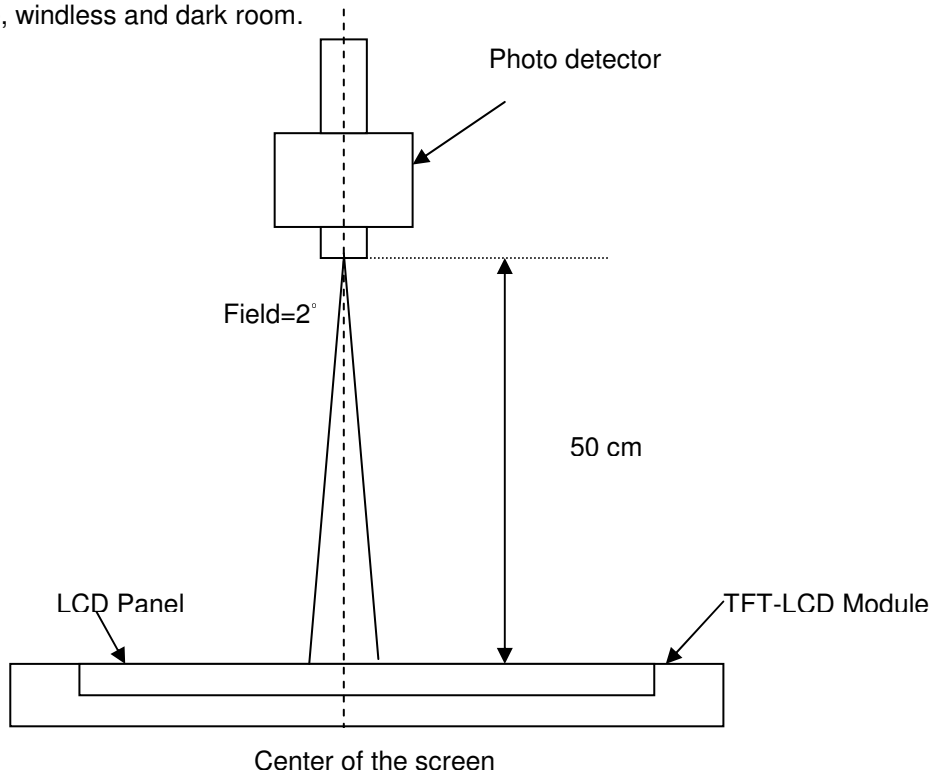
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

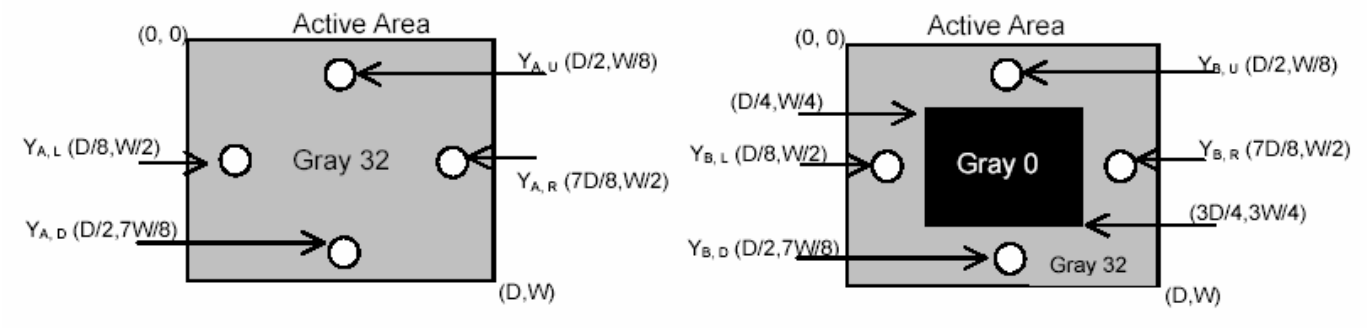
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

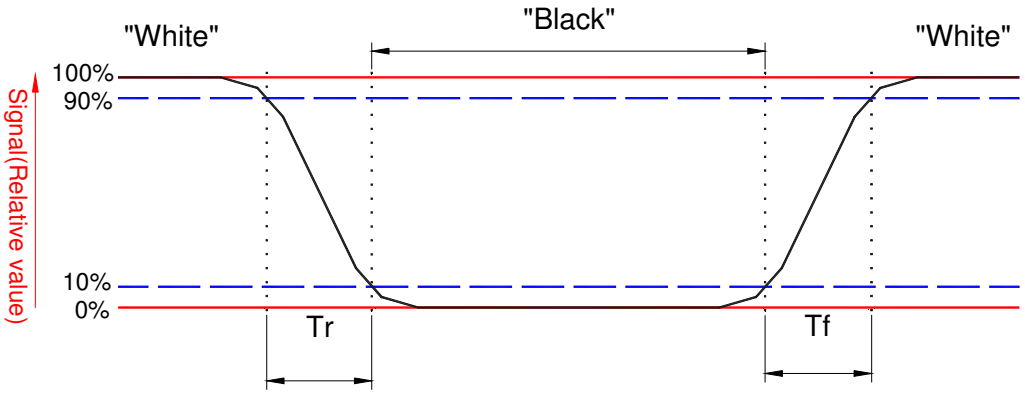
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



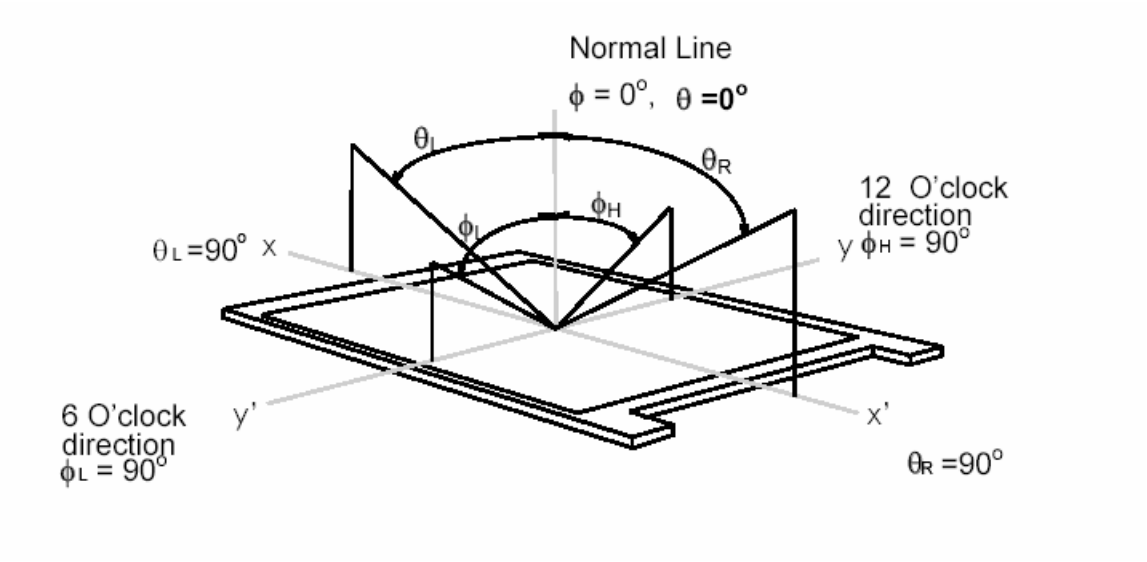
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



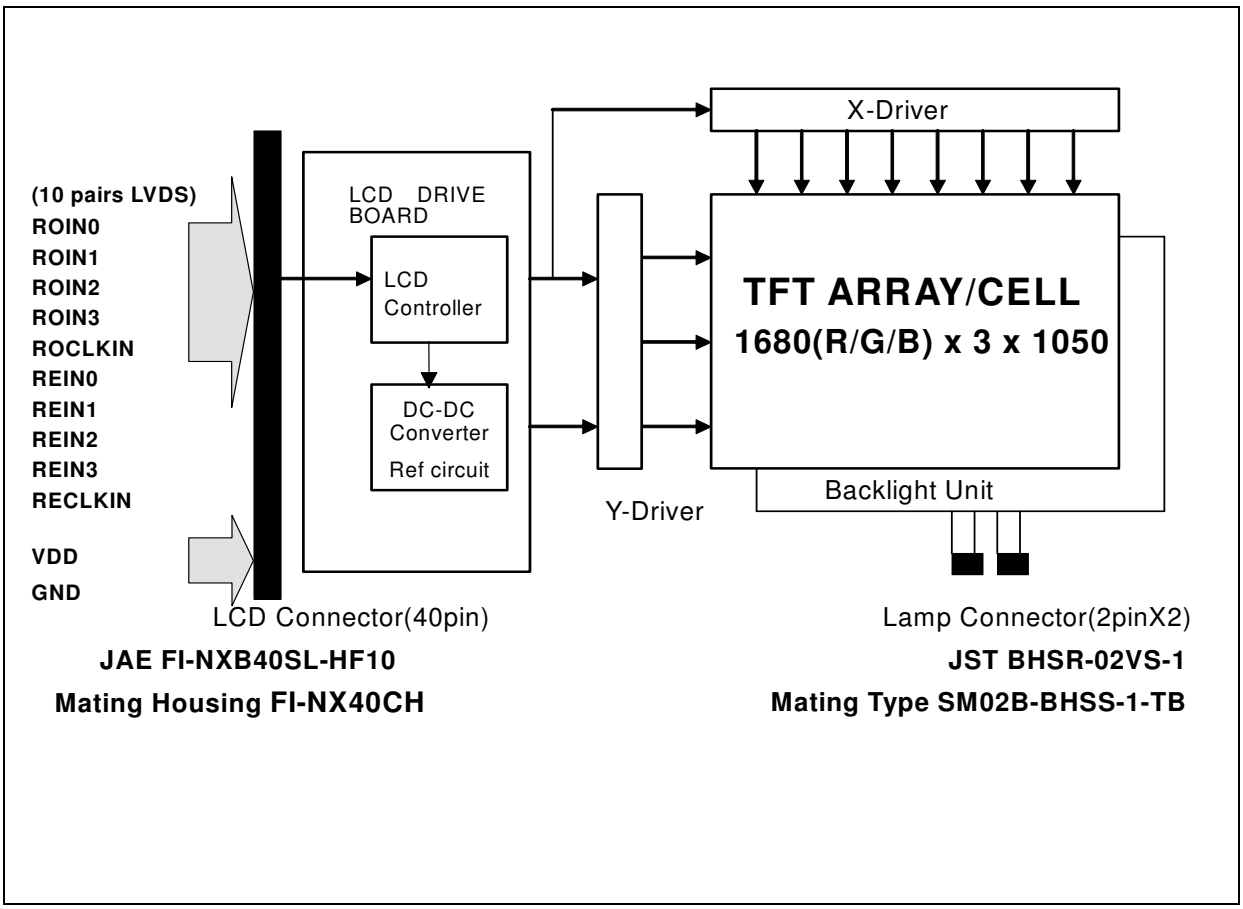
Note 8. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 20.1WSXGA+ TFT/LCD Module:



4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-	7	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	7.0	8.0	[mA] rms	Note 1,2

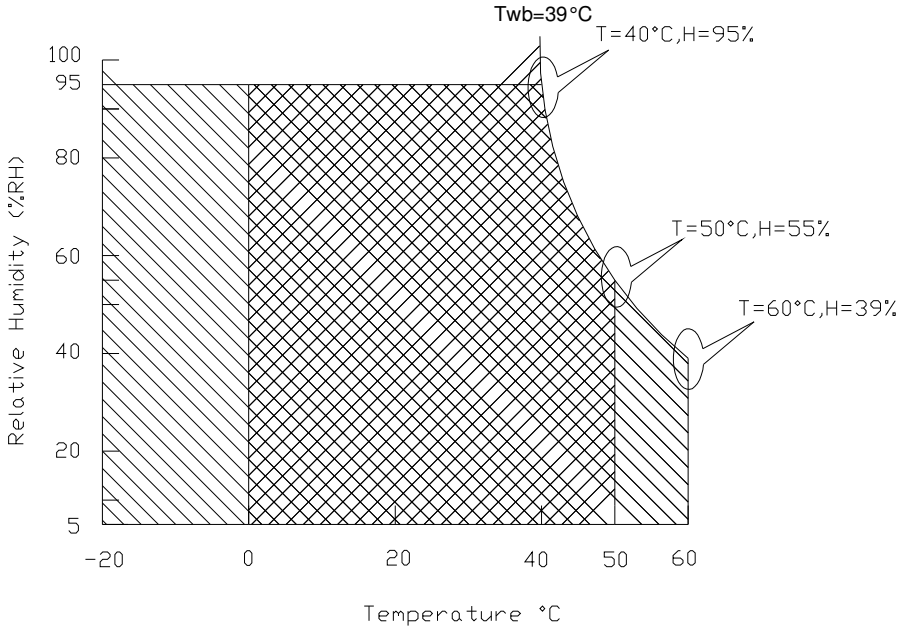
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range Storage Range

5. Electrical characteristics

5.1 TFT LCD Module

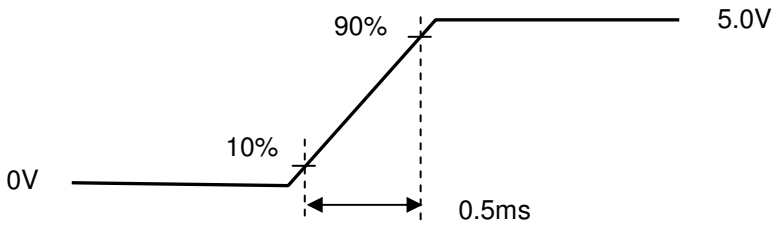
5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	4.5	5.0	5.5	[Volt]	
PDD	VDD Power		6		[Watt]	Note 1
IDD	IDD Current		1100	1400	[mA]	Note 1
IRush	Inrush Current			8000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			500	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern

Note 2：Measure Condition



Vin rising time

5.1.2 Signal Electrical Characteristics

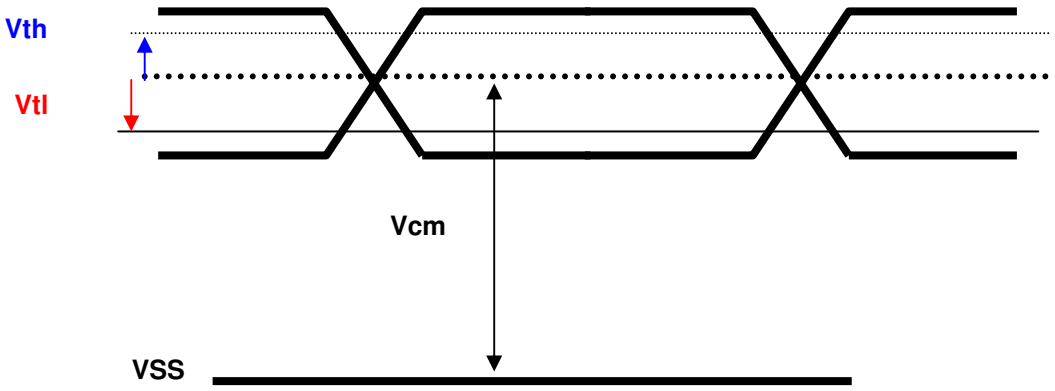
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A(Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	255	300	-	[cd/m^2]	(Ta=25℃)
CCFL current(I_{CCFL})	7.0	7.5	8.0	[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(F_{CCFL})	40	60	80	[KHz]	(Ta=25℃) Note 3,4
CCFL Ignition Voltage(Vs)	1550			[Volt] rms	(Ta= 0℃) Note 5
CCFL Ignition Voltage(Vs)	1250			[Volt] rms	(Ta= 25℃) Note 5
CCFL Voltage (Reference) (V_{CCFL})		750		[Volt] rms	(Ta=25℃) Note 6
CCFL Power consumption (P_{CCFL})	-	11.3		[Watt]	(Ta=25℃) Note 6

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CCFL is damaged.

*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has “Duty Dimming”, if ICCFL is less than 7mA.

Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,280 voltage. Lamp units need 1,250 voltage minimum for ignition.

Note 6: Calculator value for reference ($2lamp \times I_{CCFL} \times V_{CCFL} = P_{CCFL}$)

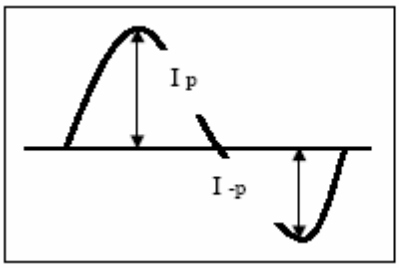
Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.

b. The distortion rate of the waveform should be within $\sqrt{2}$ ±10%.

* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

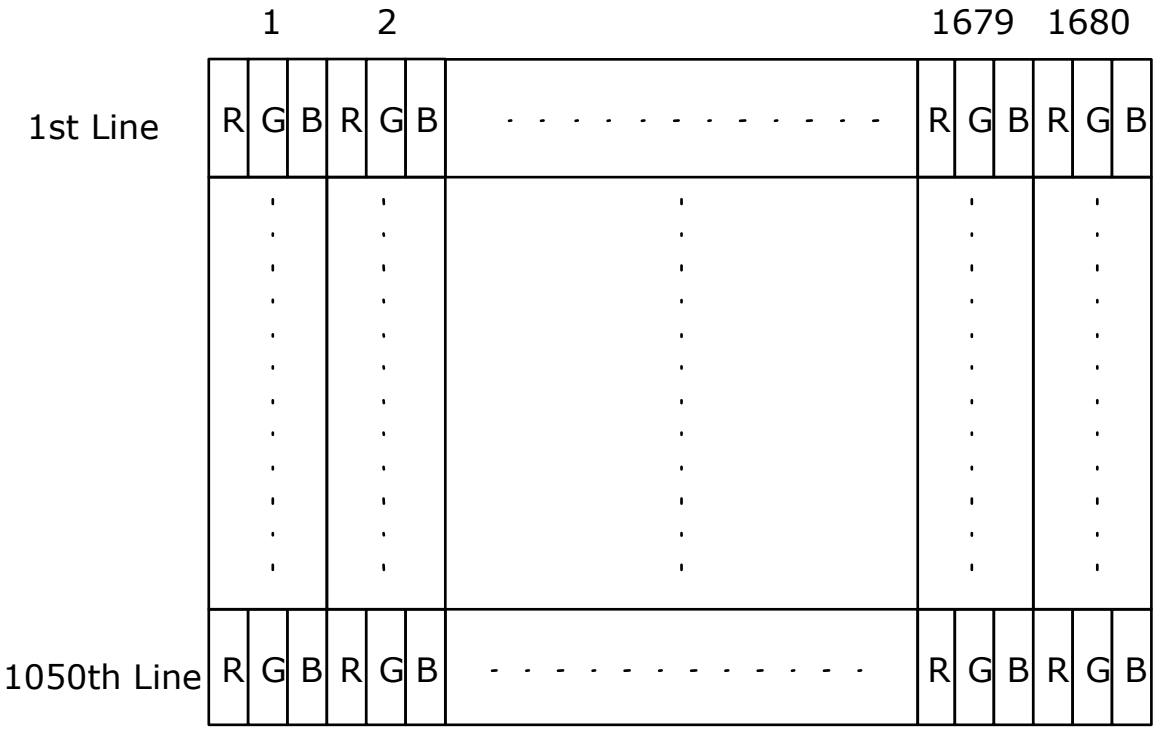
* Distortion rate

I_p (or I_{-p}) / I_{rms}

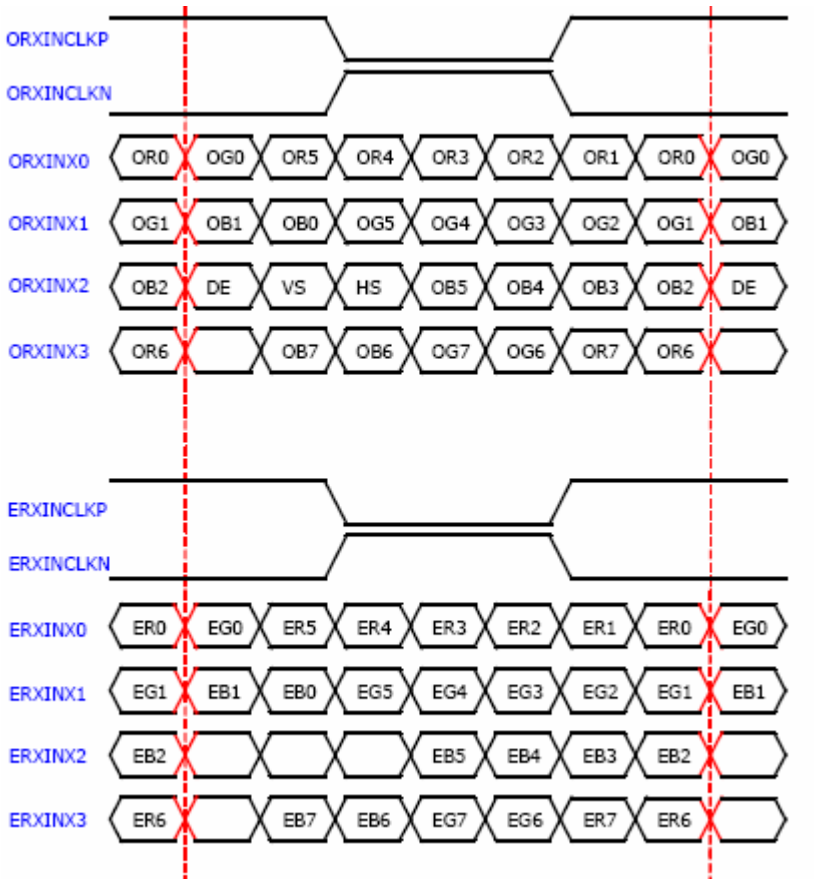
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	GND	Ground
2	GND	Ground
3	AVDD	Analog Power Supply
4	AVDD	Analog Power Supply
5	AVDD	Analog Power Supply
6	DVDD	Digital Power Supply
7	DVDD	Digital Power Supply
8	DDC_SCL	Two wire serial interface clock
9	DDC_SDA	Two wire serial interface data
10	RXinO0-	- LVDS differential data input, Chan 0-Odd
11	RXinO0+	+ LVDS differential data input, Chan 0-Odd
12	HGND	Ground
13	RXinO1-	- LVDS differential data input, Chan 1-Odd
14	RXinO1+	+ LVDS differential data input, Chan 1-Odd
15	HGND	Ground
16	RXinO2-	- LVDS differential data input, Chan 2-Odd
17	RXinO2+	+ LVDS differential data input, Chan 2-Odd
18	HGND	Ground
19	RXCLKO-	- LVDS Differential Clock input (Odd)
20	RXCLKO+	+ LVDS Differential Clock input (Odd)
21	HGND	Ground
22	RXinO3-	- LVDS differential data input, Chan 3-Odd
23	RXinO3+	+ LVDS differential data input, Chan 3-Odd
24	HGND	Ground
25	RXinE0-	- LVDS differential data input, Chan 0-Even
26	RXinE0+	+ LVDS differential data input, Chan 0-Even
27	HGND	Ground
28	RXinE1-	- LVDS differential data input, Chan 1-Even
29	RXinE1+	+ LVDS differential data input, Chan 1-Even
30	HGND	Ground
31	RXinE2-	- LVDS differential data input, Chan 2-Even
32	RXinE2+	+ LVDS differential data input, Chan 2-Even
33	HGND	Ground
34	RXCLKE-	- LVDS Differential Clock input (Even)

35	RXCLKE+	+ LVDS Differential Clock input (Even)
36	HGND	Ground
37	RXinE3-	- LVDS differential data input, Chan 3-Even
38	RXinE3+	+ LVDS differential data input, Chan 3-Even
39	HGND	Ground
40	NC	Reserved

6.4 Interface Timing

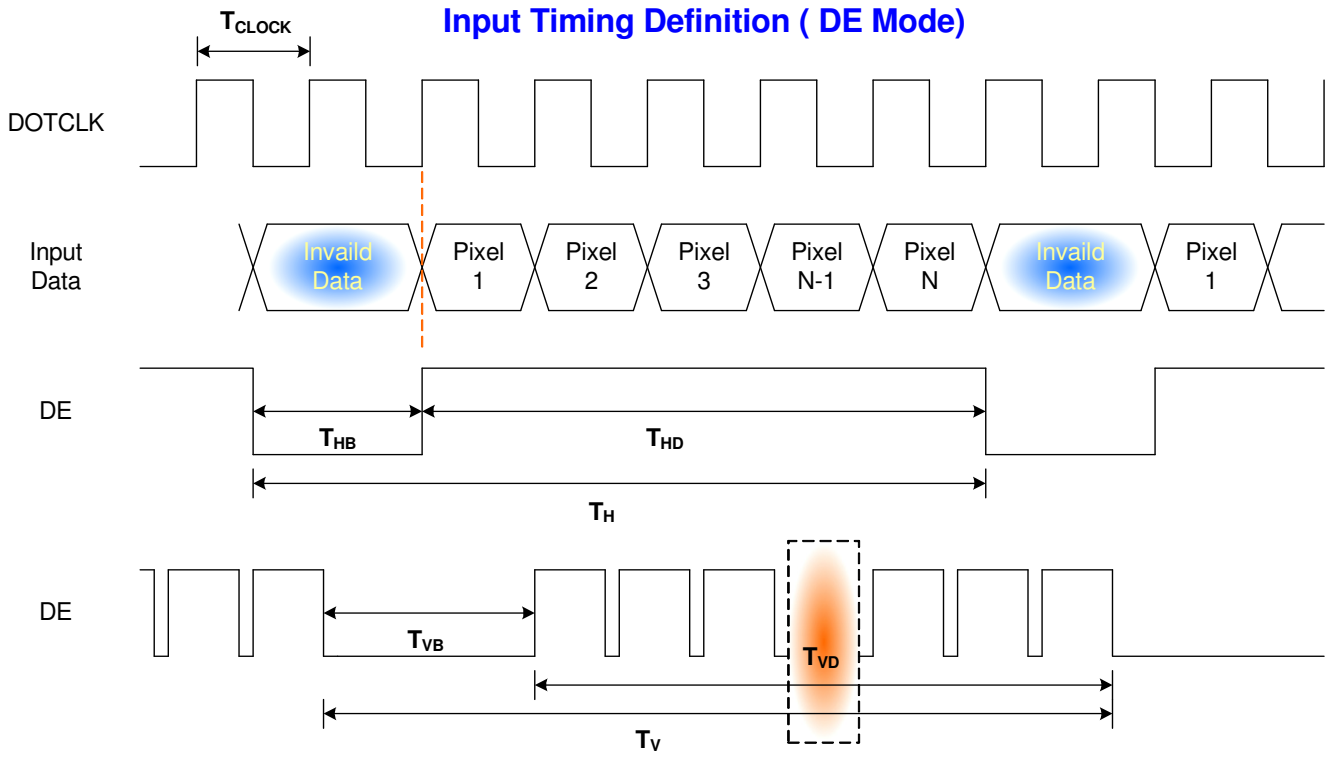
6.4.1 Timing Characteristics

Basically, interface timings should match the 1680x1050 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T_{Clock}	TBD	72.1	85	MHz
Vertical Section	Period	T_V	1058	1066	2048	T_{Line}
	Active	T_{VD}	1050	1050	1050	
	Blanking	T_{VB}	8	16	998	
Horizontal Section	Period	T_H	880	1128	2048	T_{Clock}
	Active	T_{HD}	840	840	840	
	Blanking	T_{HB}	40	288	1208	

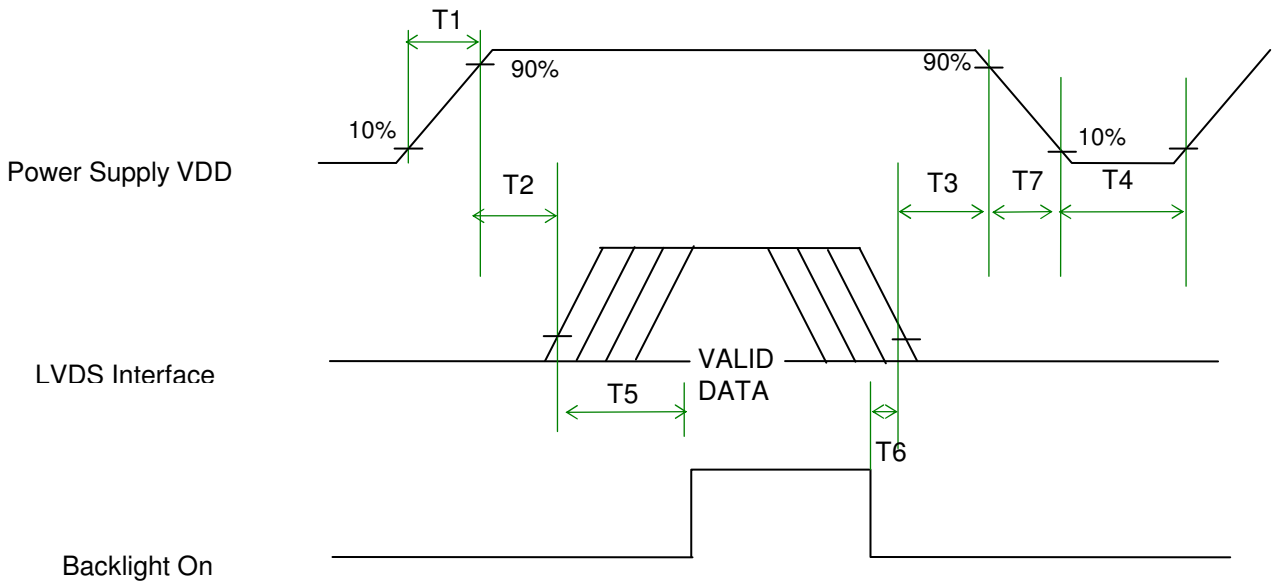
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	JAE, FI-NXB40SL-HF10 or compatible
Mating Housing/Part Number	FI-NX40CH or compatible

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage
3	Blue	Lamp High Voltage
4	Black	Lamp Low Voltage

8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5Grms
- Frequency: 10~500Hz
- Sweep: 30min/axis

8.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 160G
- Active time: 2ms
- Pulse: 1time/Axis

9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	40℃/90%,300Hr	
High Temperature Operation	50℃/Dry,300Hr	
Low Temperature Operation	0℃,300Hr	
On/Off Test	25℃,150hrs(ON/10 sec. OFF/10sec., 10,000 cycles)	
Hot Storage	60℃/35% RH ,250 hours	
Cold Storage	-20℃/50% RH ,250 hours	
Thermal Shock Test	-20℃/30 min ,60℃/30 min 100cycles	
Hot Start Test	50℃/1 Hr min. power on/off per 5 minutes, 5 times	
Cold Start Test	0℃/1 Hr min. power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	160G/2ms, 1time/axis	
Vibration Test (Non-Operating)	1.5.Grms, 10~500Hz , 30min/axis	
ESD	Contact : ±8KV/ operation Air : ±15KV / operation	Note 1
Room temperature Test	25℃, 2000hours, Operating with loop pattern	

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

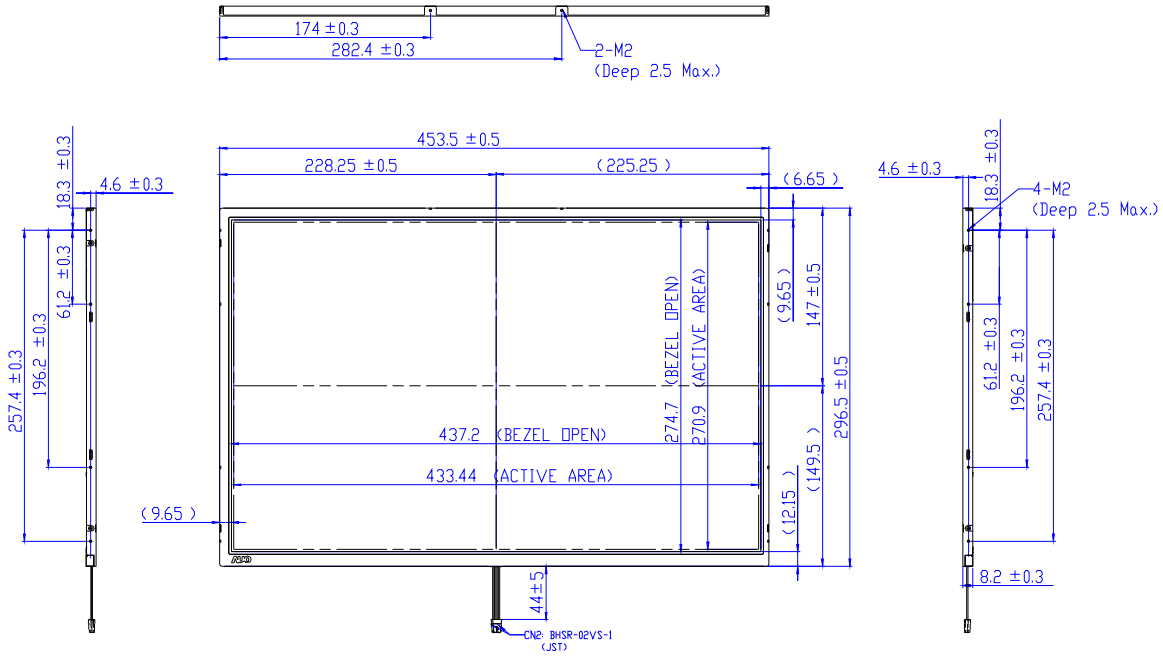
. Self-recoverable. No hardware failures.

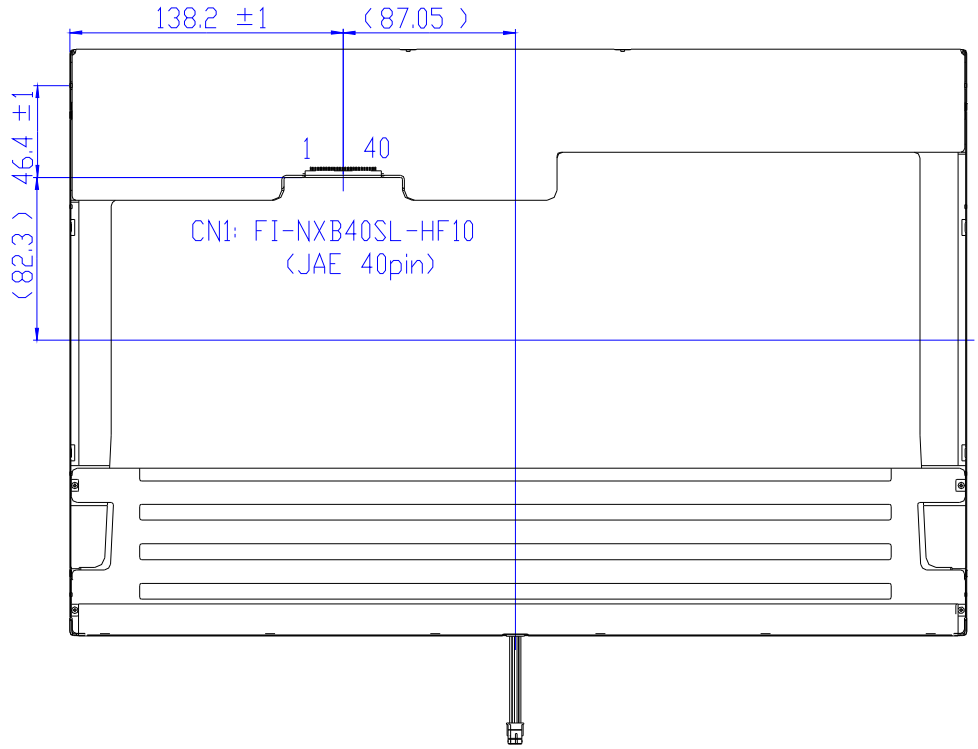
Note2: CCFL Life time: 10,000 hours minimum under normal module usage.

Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

10. Mechanical Characteristics

10.1 LCM Outline Dimension

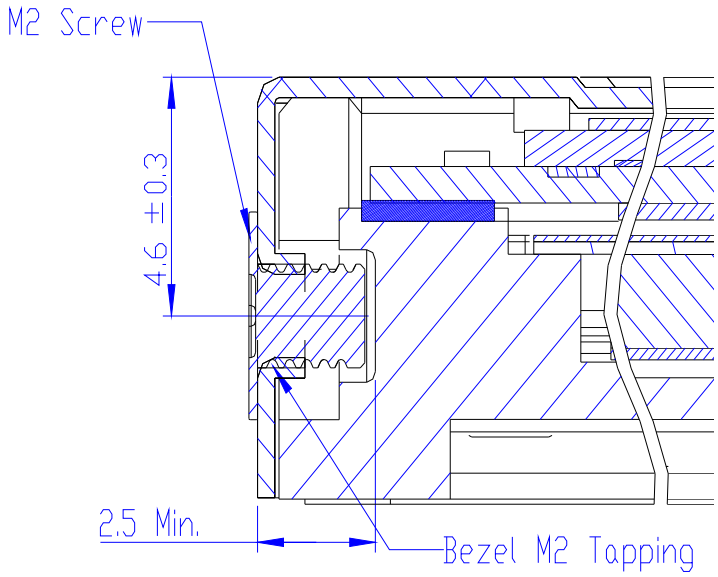




10.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface =2.5mm (See drawing)

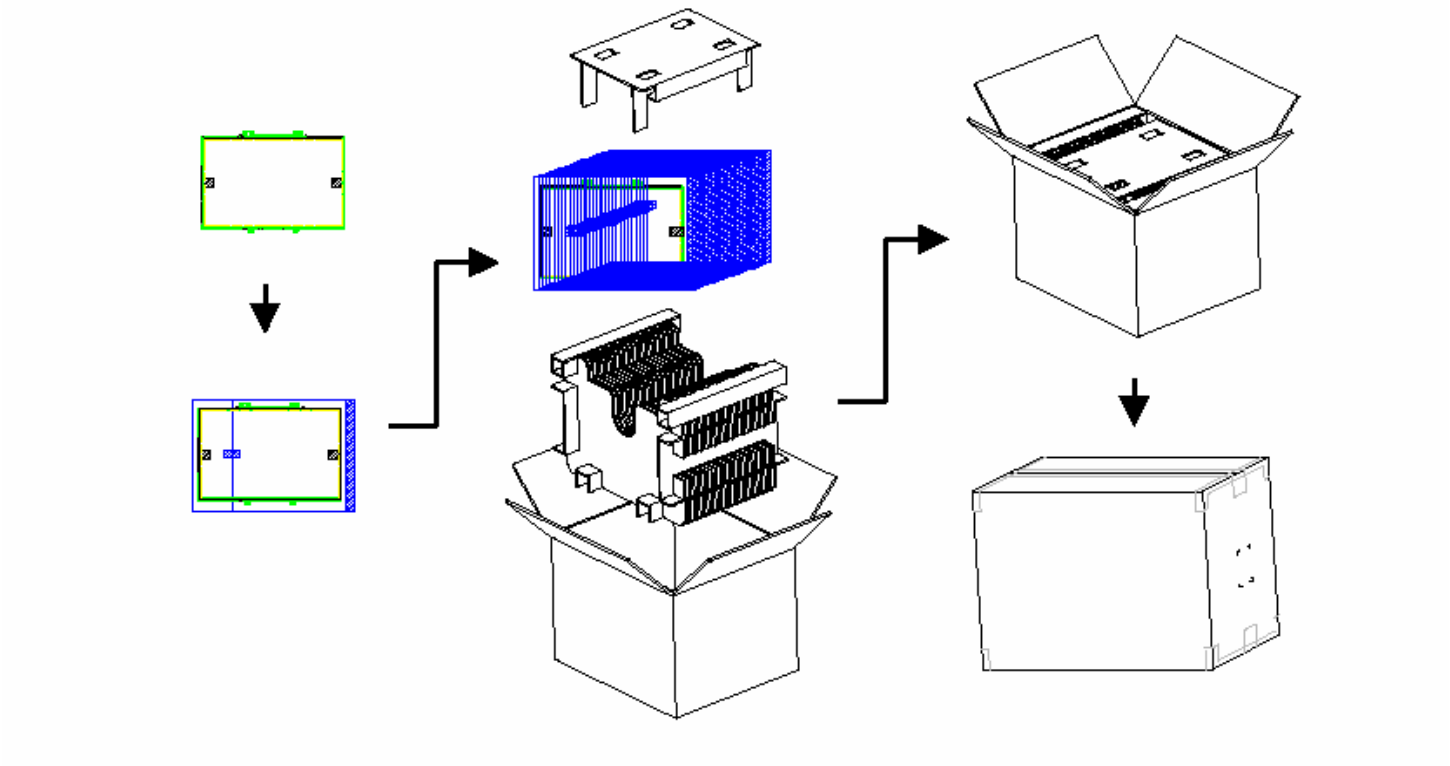
Screw hole center location, from front surface =4.6±0.3mm (See drawing)
Screw Torque: Maximum 2.5 kgf-cm



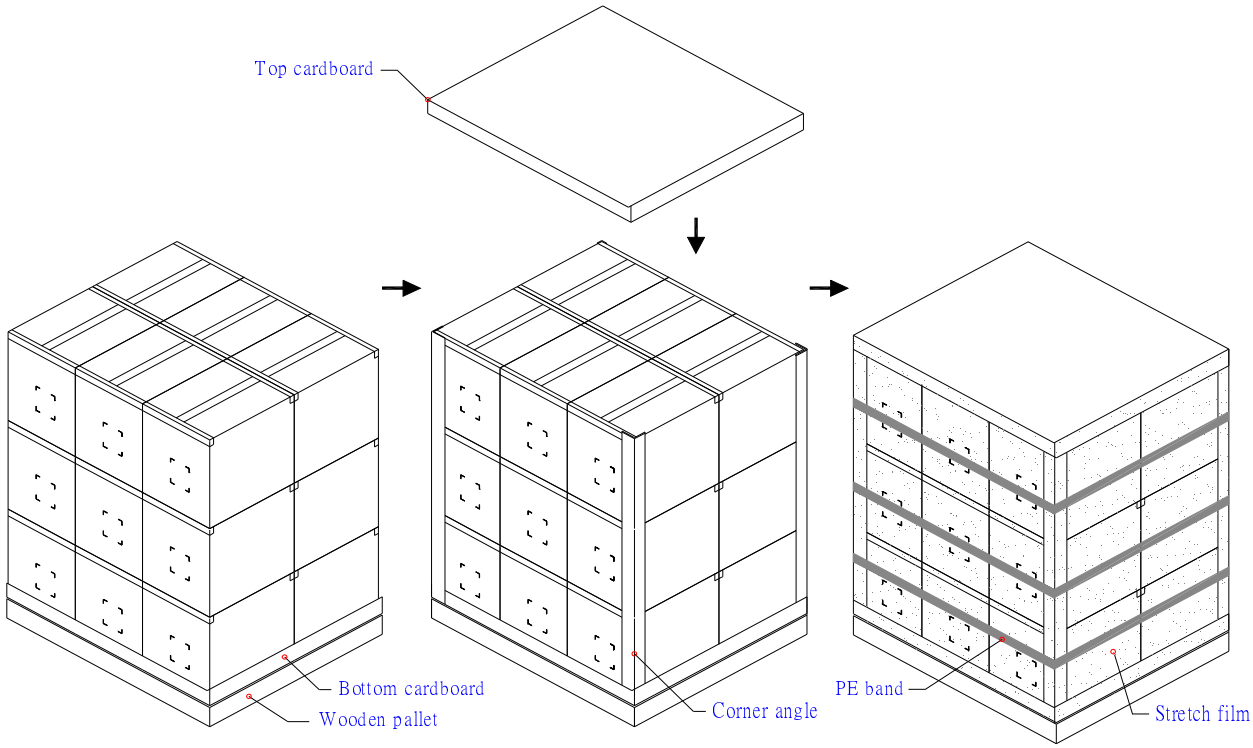
11. Shipping and Package

11.1 Shipping Label Format

11.2. Carton package



11.3 Shipping package of palletizing sequence



Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)

12. Appendix: EDID description

Address HEX	FUNCTION	Value HEX	Value BIN	Value DEC	Notes
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	ASCII Data String:B201SW01
09	Compressed ASCII	AF	10101111	175	AUO
0A	Product Code	AB	10101011	171	B201SW
0B	hex, LSB first	10	00010000	16	01 V0
0C	32-bit ser #	00	00000000	0	0
0D		00	00000000	0	0
0E		00	00000000	0	0
0F		00	00000000	0	0
10	Week of manufacture	01	00000001	1	Week 1
11	Year of manufacture	11	00010001	17	Year(2007-1990=17)
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	03	00000011	3	
14	Video input definition	80	10000000	128	Digital Input
15	Max H image size	2B	00101011	43	33.00cm
16	Max V image size	1B	00011011	27	19.90cm
17	Display Gamma	78	01111000	120	Gamma 2.2
18	Feature support	0A	00001010	10	no DPMS,Active off,RGB color
19	Red/green low bits	60	01100000	96	
1A	Blue/white low bits	85	10000101	133	
1B	Red x/ high bits	A6	10100110	166	Rx=0.649
1C	Red y	56	01010110	86	Ry=0.338
1D	Green x	4A	01001010	74	Gx=0.289
1E	Green y	9C	10011100	156	Gy=0.609
1F	Blue x	25	00100101	37	Bx=0.146
20	Blue y	12	00010010	18	By=0.070
21	White x	50	01010000	80	Wx=0.313
22	White y	54	01010100	84	Xy=0.329
23	Established timing 1	00	00000000	0	unused
24	Established timing 2	00	00000000	0	—
25	Manufacturer's Timing	00	00000000	0	
26	Standard timing #1	01	00000001	1	unused
27		01	00000001	1	

28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10,000 (LSB)	5E	01011110	94	Timing Descriptor #1
37	Pixel Clock/10,000 (MSB)	38	00111000	56	1680x1050 @60_mode:pixel clock=72.10MHz
38	Horiz. Active pixels(Lower 8 bits)	90	10010000	144	Horiz active=1680 pixels
39	Horiz.Blanking (Lower 8 bits)	40	01000000	64	Horiz blanking=576 pixels
3A	Horiz. Active pixels:Horiz. Blanking (Upper4:4 bits)	62	01100010	98	
3B		1A	00011010	26	Vertcal active=1050 lines
3C		10	00010000	16	Vertical blanking=16 lines
3D	Vert. Active pixels:Vert. Blanking (Upper4:4 bits)	40	01000000	64	
3E		40	01000000	64	Horiz sync. Offset=64 pixels
3F		C0	11000000	192	Horiz sync. Pulse Width=192 pixels
40	Vert. Sync. Offset=xx lines, Sync Width=xx lines	13	00010011	19	Verti sync. Offset=1 lines,Sync Width=3 lines
41	Horz. Ver. Sync/Width (upper 2 bits)	00	00000000	0	
42	Hori. Image size (Lower 8 bits)	B1	10110001	177	Hori image size= 433 mm
43	Vert. Image size (Lower 8 bits)	0F	00001111	15	Verti image size = 271mm
44	Hori. Image size : Vert. Image size (Upper 4 bits)	11	00010001	17	
45		00	00000000	0	Horizontal Border = 0
46		00	00000000	0	Vertical Border = 0
47		18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	ASCII Data String:B201SW01
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	

52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	ASCII Data String:B201SW01
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F		41	01000001	65	A
60		55	01010101	85	U
61		4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	Monitor Name: Color LCD
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71		42	01000010	66	B
72		32	00110010	50	2
73		30	00110000	48	0
74		31	00110001	49	1
75		53	01010011	83	S
76		57	01010111	87	W
77		30	00110000	48	0
78		31	00110001	49	1
79		20	00100000	32	
7A		56	01010110	86	V
7B		30	00110000	48	0
7C		20	00100000	32	
7D		0A	00001010	10	

7E	Extension Flag	**00**	00000000	0	
7F	Checksum	**6E**	01101110	110	