



Product Specification

AU OPTRONICS CORPORATION

B141EW02 V4

() Preliminary Specifications

(V) Final Specifications

Module	14.1" WXGA Color TFT-LCD
Model Name	B141EW02 V4

Customer	Date
_____	_____
Checked & Approved by	
_____	_____
Note: This Specification is subject to change without notice.	

Approved by	Date
Howard Lee	2007/04/11
Prepared by	
Emerson Huang	2007/04/11
NBBU Marketing Division / AU Optronics corporation	



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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2006/12/19	All	First Edition for Customer		
0.2 2007/2/14	21		Note of Frame rate	
	13		Note of VDD power	
	31~33		Change EDID	
	16		Notes of 15% duty	
	22		Power ON/OFF Sequence	
0.3 2007/3/30	25	CCFL life time10,000hrs	CCFL life time12,000hrs	
0.4 2007/4/11	5	Power consumption 5.1W	Power consumption 5.0W	
	5	Surface treatment: Haze 42%, Hardness 2H,	Surface treatment: Haze 42%, Hardness 2H, Reflection type LR, Reflection value $\leq 3\%$.	
	13		PDD:1.0W max., IDD:270mA max.	
	15		Power consumption 4.6W max.	
	16		Notes of 15% duty update	
	21	Clock frequency 71.1 MHz	Clock frequency 69.25 MHz	
	22	Power sequence time T6: 200ms	Power sequence time T6: 0ms	
	31~33		EDID change for WWAN	



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1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
- 14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.



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2. General Description

B141EW02 V4 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter of backlight is not included.

B141EW02 V4 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	357.7 (14.1 W")
Active Area	[mm]	303.36(H) x 189.6 (V)
Pixels H x V		1280x3(RGB) x 800
Pixel Pitch	[mm]	0.237
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (ICCFL=6.0mA) Note: ICCFL is lamp current	[cd/m ²]	200 Typ. (5 points average) 170 Min. (5 points average) (Note1)
Luminance Uniformity		1.2 max. (5 points), 1.5 max. (13 points)
Contrast Ratio		300:1 Typ.
Optical Rise Time/Fall Time	[msec]	25 Typ., 35 Max.
Nominal Input Voltage VDD	[Volt]	+3.3 Typ.
Power Consumption	[Watt]	5.0 Typ.
Weight	[Grams]	400 g Typ., 420g Max.
Physical Size	[mm]	320 max. (W) x 206 max. (H) x 5.5 max.(T).
Electrical Interface		R/G/B Data, 3 Sync, Signals, Clock (4 pairs LVDS)
Surface Treatment		Haze 42%, Hardness 2H, Reflection type LR, Reflection value ≤ 3%
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance



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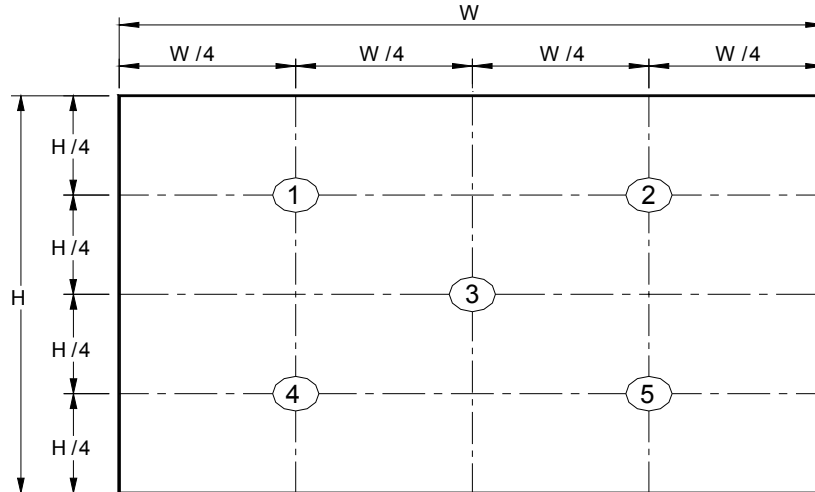
B141EW02 V4

2.2 Optical Characteristics

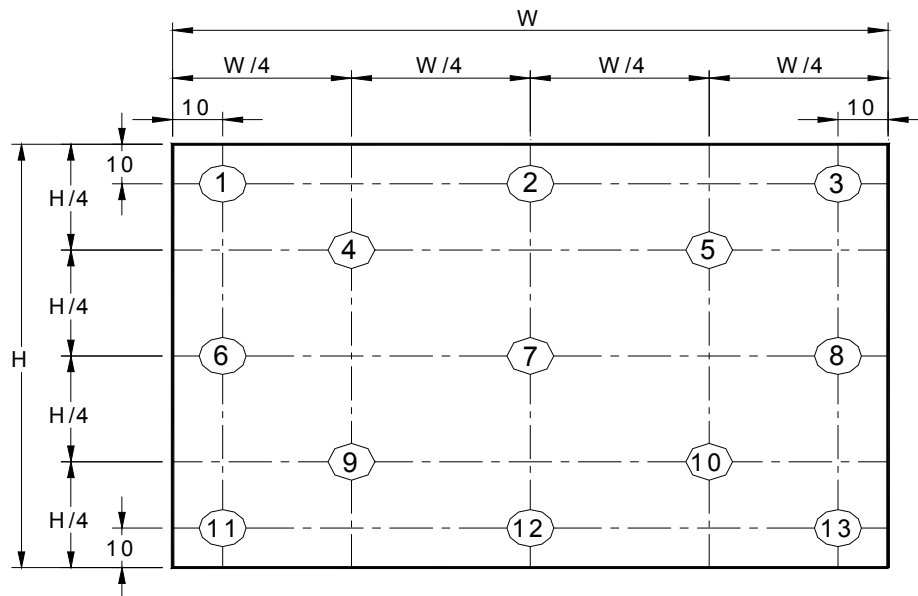
The optical characteristics are measured under stable conditions at 25 (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance I _{CCFL} =6.0mA	[cd/m ²]	5 points average	170	200	-	1, 4, 5.
Viewing Angle	[degree]	Horizontal (Right)	40	45	-	8
	[degree]	CR = 10 (Left)	40	45	-	
	[degree]	Vertical (Upper)	15	20	-	
	[degree]	CR = 10 (Lower)	35	40	-	
Luminance Uniformity		5 Points			1.20	1
Luminance Uniformity		13 Points			1.50	2
''''''	''	,	,	,	-	6
Cross talk	%				1.4	7
Response Time	[msec]	Rising	-	15	20	8
	[msec]	Falling	-	10	15	
	[msec]	Rising + Falling		25	35	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.550	0.580	0.610	2,8
		Red y	0.310	0.340	0.370	
		Green x	0.280	0.310	0.340	
		Green y	0.520	0.550	0.580	
		Blue x	0.125	0.155	0.185	
		Blue y	0.115	0.145	0.175	
		White x	0.285	0.313	0.341	
		White y	0.309	0.329	0.349	

Note 1: 5 points position (Display area : 303.36 (H) x 189.6(V)mm)



Note 2: 13 points position



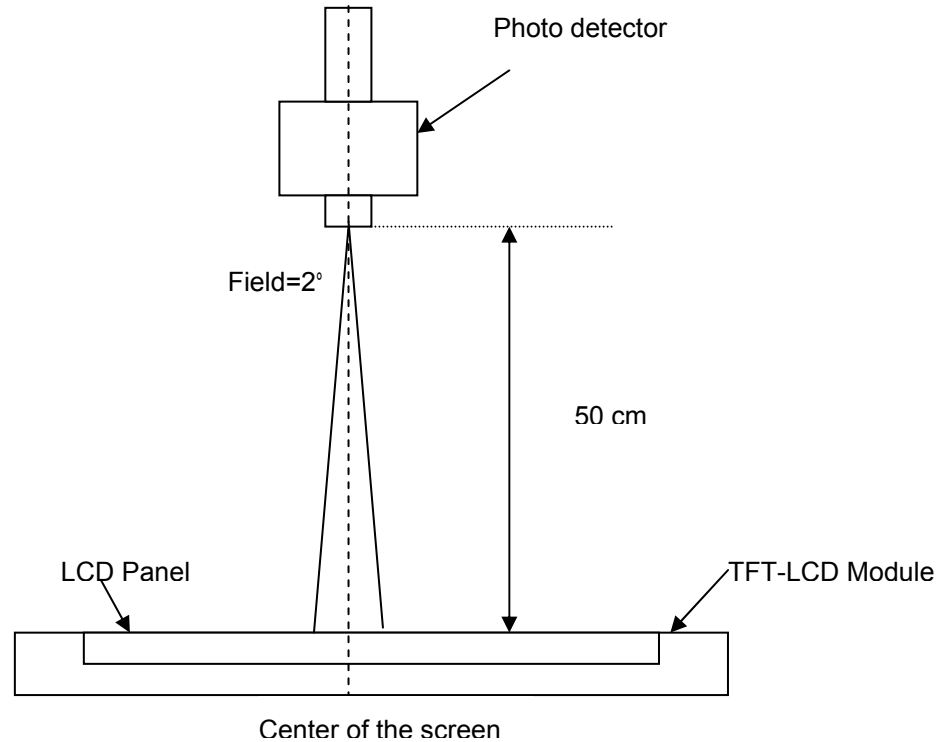
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$w_5 = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$w_{13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

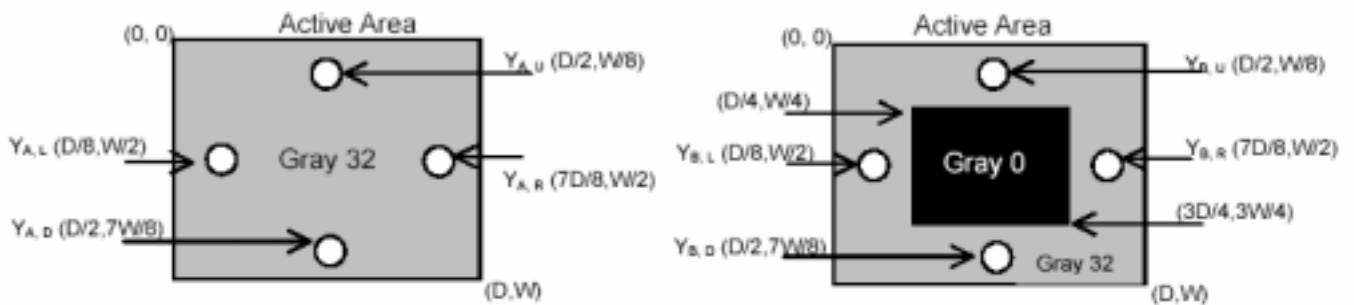
Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

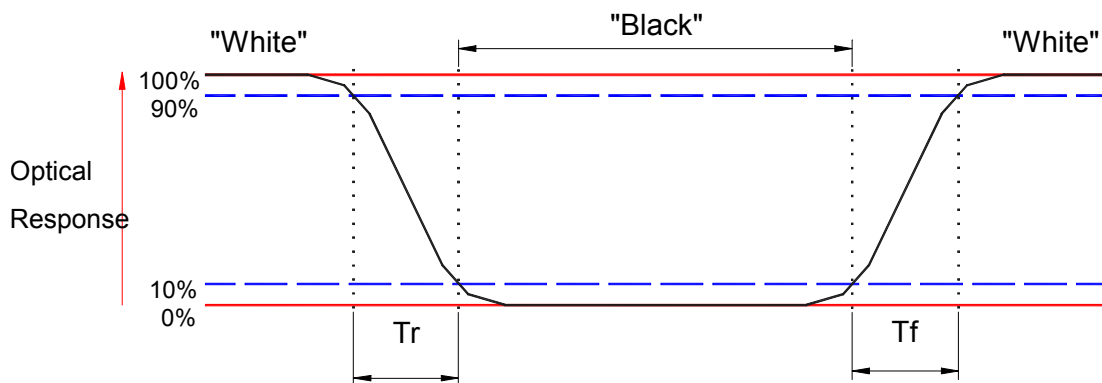
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



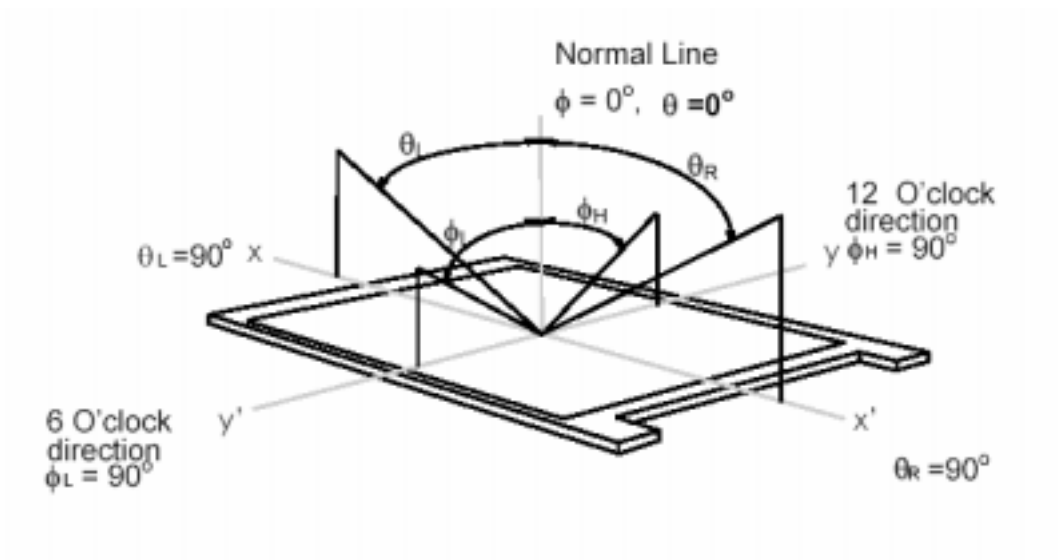
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



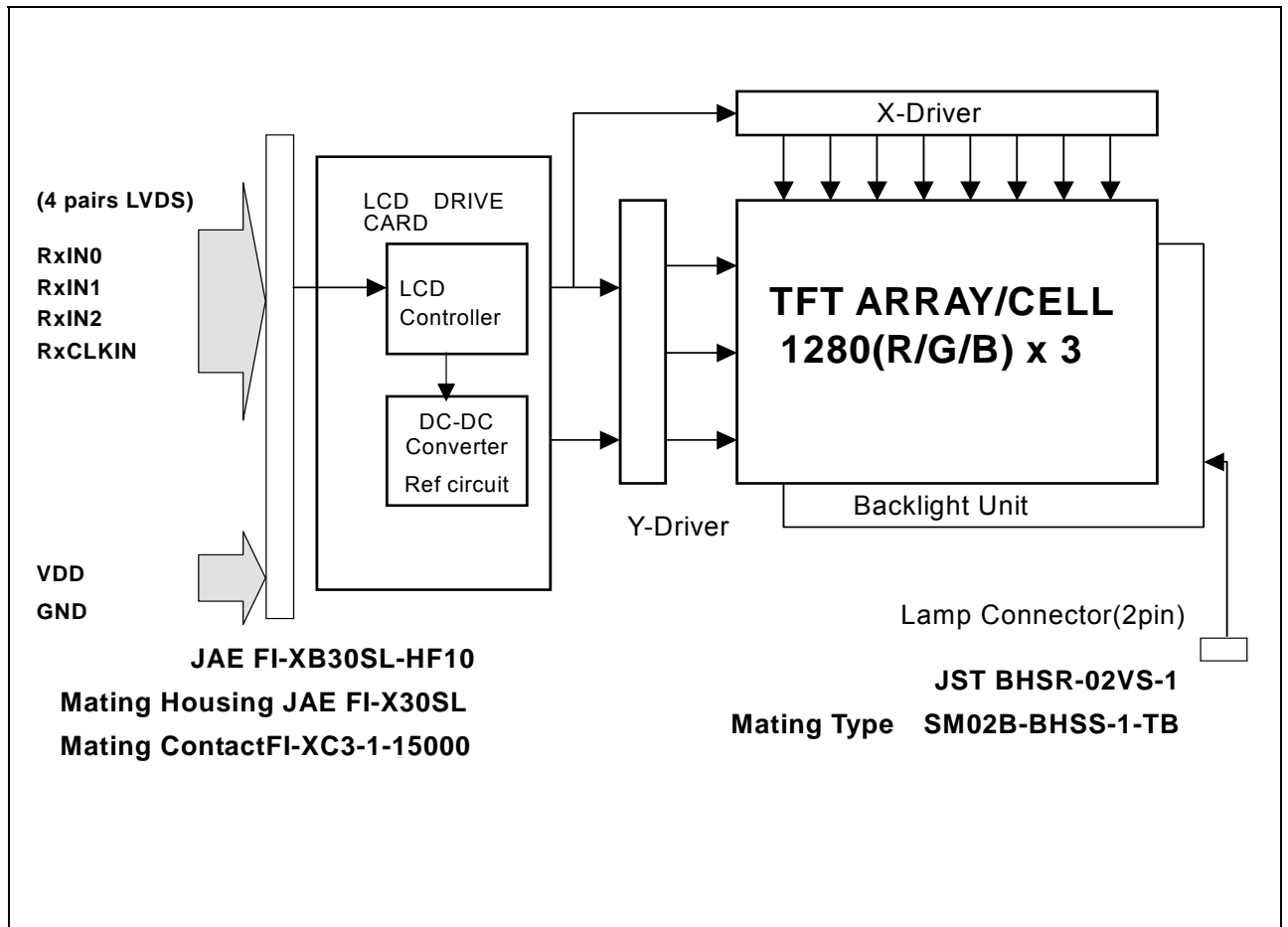
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° () horizontal left and right and 90° () vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 14.1 inches wide Color TFT/LCD Module:





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4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICFL	2.0	7.0	[mA] rms	Note 1,2

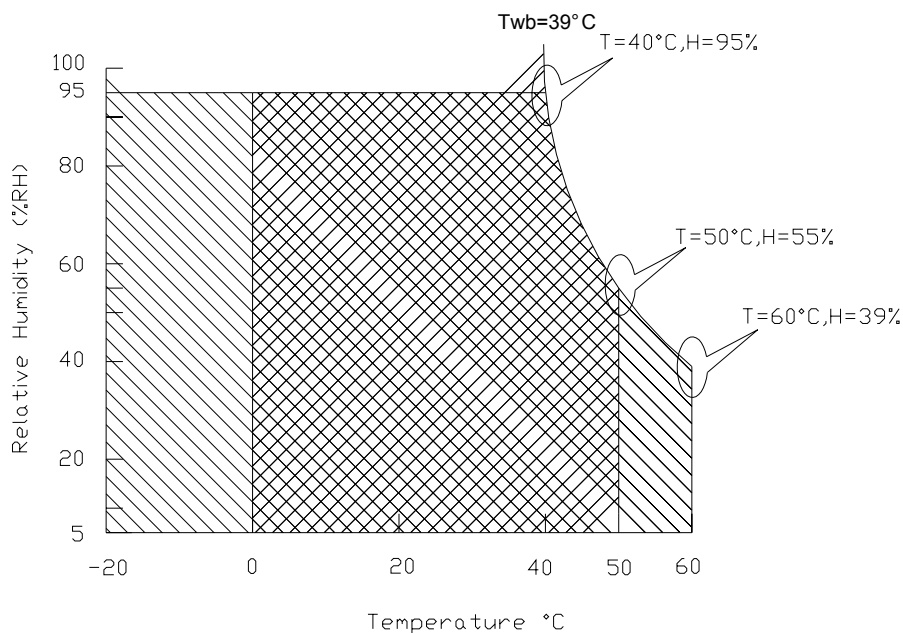
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25 °C)

Note 2: Permanent damage to the device may occur if exceed maximum values

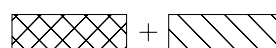
Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range



Storage Range



5. Electrical characteristics

5.1 TFT LCD Module

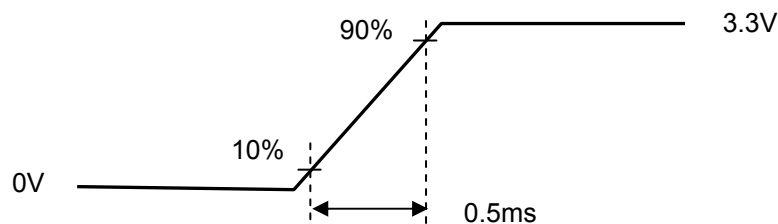
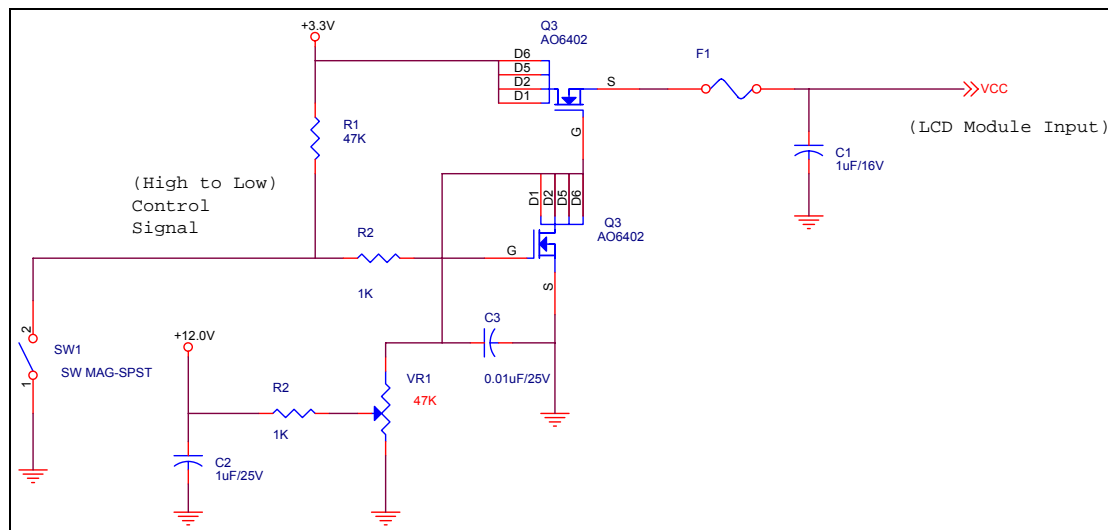
5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive	3.0	3.3	3.6	[Volt]	
PDD	VDD Power		0.8	1.0	[Watt]	Note 1
IDD	IDD Current		240	270	[mA]	Note 1
IRush	Inrush Current			1200	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern (Windows XP pattern VDD Power Typ.: 0.7W)

Note 2 : Measure Condition



Vin rising time

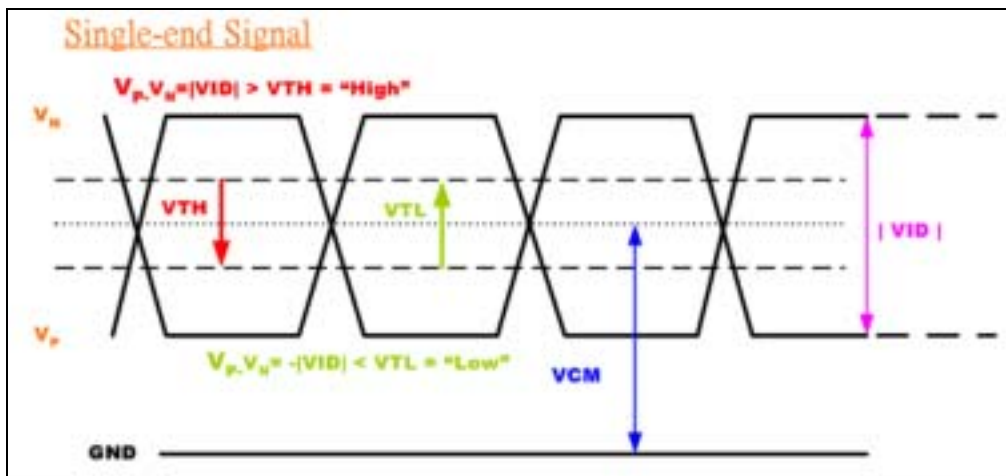
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Differential Voltage



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	170	200	-	[cd/m ²]	(Ta=25 °C)
CCFL current(ICCFL)	2.0	6.0	7.0	[mA] rms	(Ta=25 °C) Note 2
CCFL Frequency(FCCFL)	50	65	80	[KHz]	(Ta=25 °C) Note 3,4
CCFL Ignition Voltage(Vs)			1300	[Volt] rms	(Ta= 0 °C) Note 5
CCFL Ignition Voltage(Vs)			1125	[Volt] rms	(Ta= 25 °C) Note 5
CCFL Voltage (Reference) (VCCFL)		660		[Volt] rms	(Ta=25 °C) Note 6
CCFL Power consumption (PCCFL)	-	4.2	4.6	[Watt]	(Ta=25 °C) Note 6

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully.

Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has "Duty Dimming", if ICCFL is less than 4mA.

Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,430 voltage. Lamp units need 1,400 voltage minimum for ignition.

Note 6: Calculator value for reference ($I_{CCFL} \times V_{CCFL} = P_{CCFL}$)

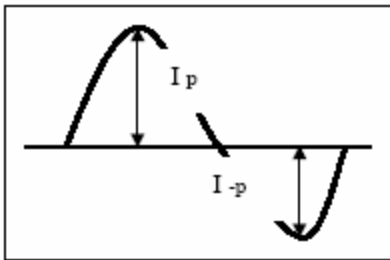
Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.

b. The distortion rate of the waveform should be within $2 \pm 10\%$.

* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$$\frac{|I_p - I_{-p}|}{I_{rms}} \times 100\%$$

* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{rms}$$

Note 8: When CCFL works at minimum working current (2mA), the duty percent has to maintain at 15% (min).

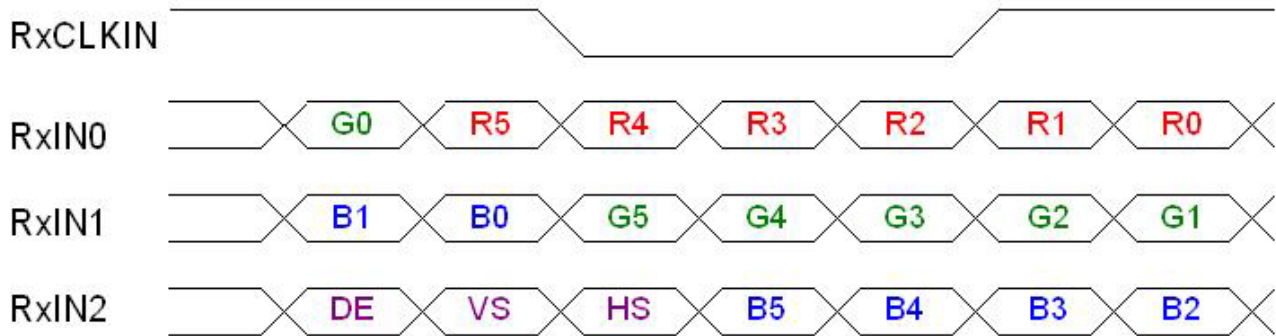
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

	0			1															1278			1279		
1st Line	R	G	B	R	G	B												R	G	B	R	G	B
	⋮			⋮			⋮												⋮			⋮		
	⋮			⋮			⋮												⋮			⋮		
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800th Line	R	G	B	R	G	B												R	G	B	R	G	B

6.2 The input data format



Signal Name	Description	
+R5 +R4 +R3 +R2 +R1 +R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
+G5 +G4 +G3 +G2 +G1 +G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
+B5 +B4 +B3 +B2 +B1 +B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The typical frequency is 71.1 MHz. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN.
HS	Horizontal Sync	The signal is synchronized to RxCLKIN.

Note: Output signals from any system shall be low or High-impedance state when VDD is off.



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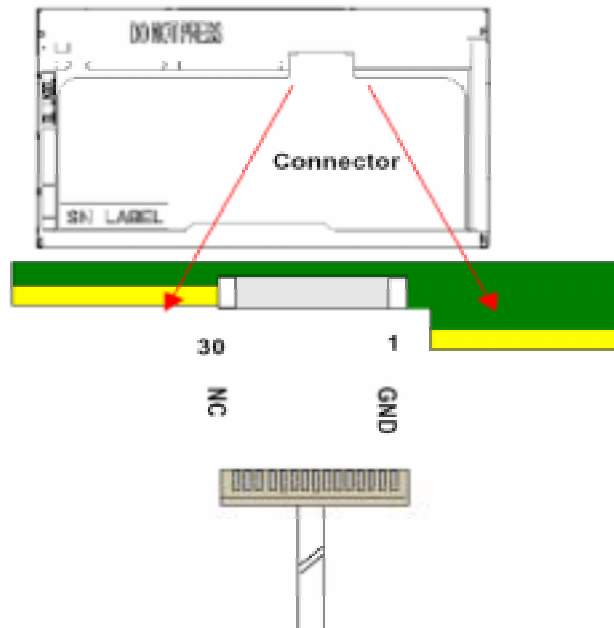
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6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

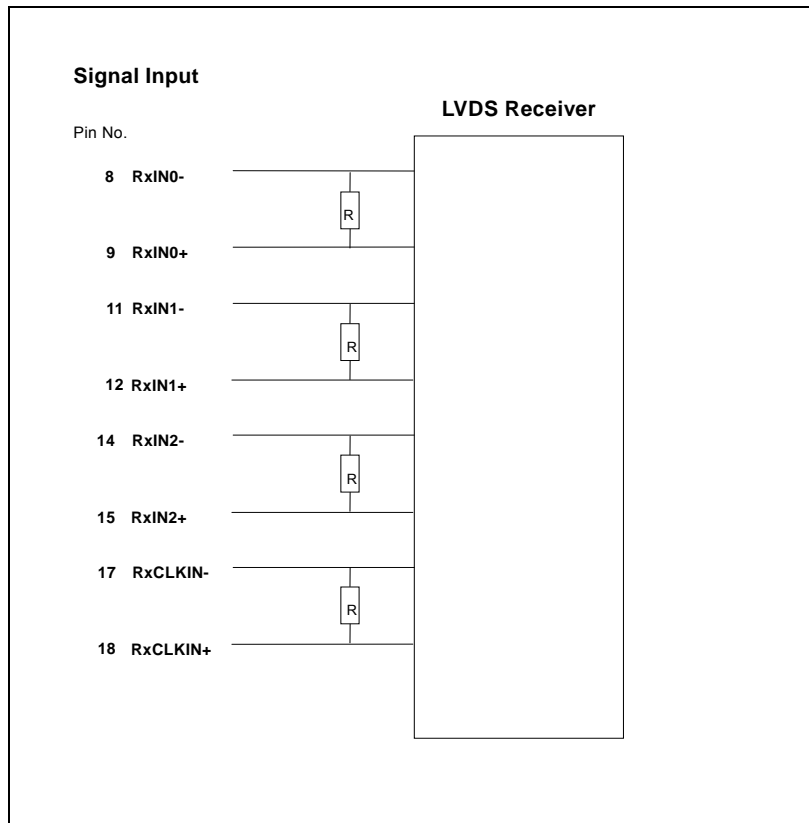
Pin#	Signal Name	Pin#	Signal Name
1	GND	2	VDD
3	VDD	4	V _{EDID}
5	Aging	6	CLK _{EDID}
7	DATA _{EDID}	8	RxIN0-
9	RxIN0+	10	GND
11	RxIN1-	12	RxIN1+
13	GND	14	RxIN2-
15	RxIN2+	16	GND
17	RxCLKIN-	18	RxCLKIN+
19	GND	20	NC
21	NC	22	GND
23	NC	24	NC
25	GND	26	NC
27	NC	28	GND
29	NC	30	NC

Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.
internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

6.4.1 Timing Characteristics

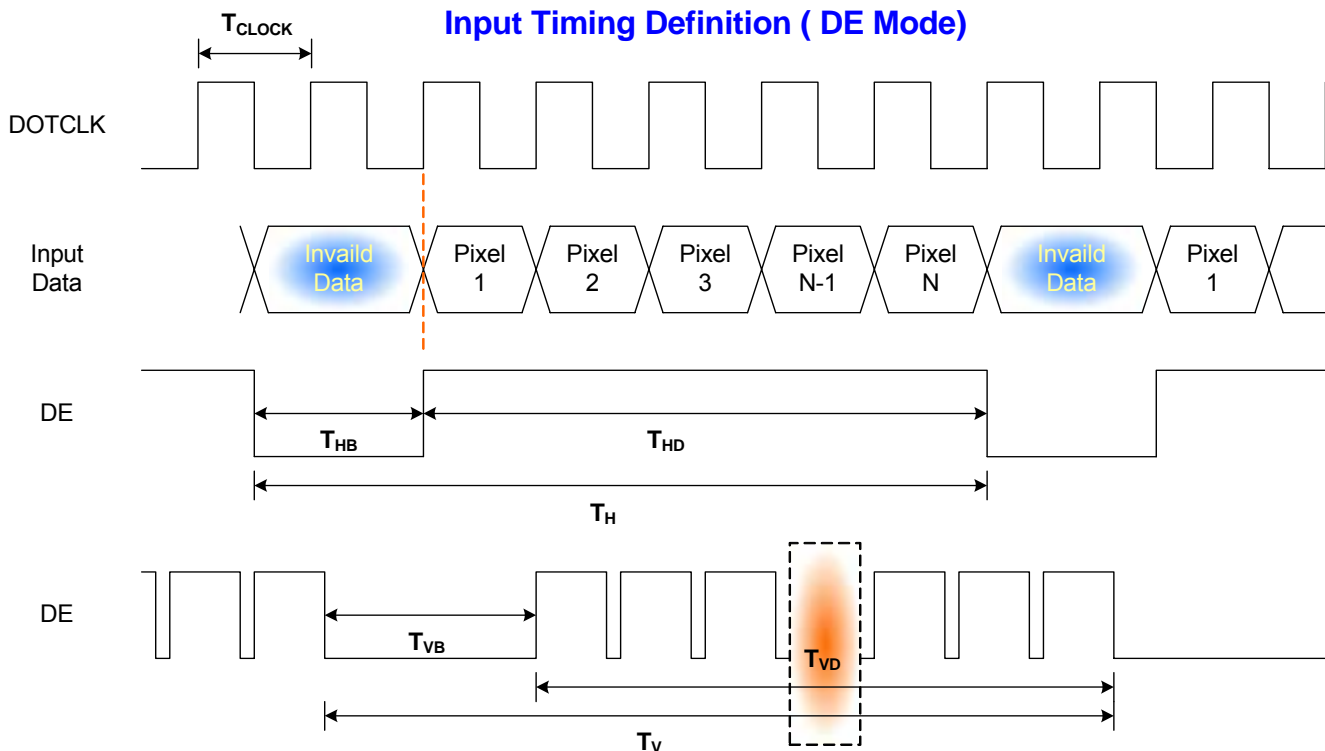
Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		$1/T_{\text{Clock}}$		69.25		MHz
Vertical Section	Period	T_V	803	823	1023	T_{Line}
	Active	T_{VD}	800	800	800	
	Blanking	T_{VB}	3	23	223	
Horizontal Section	Period	T_H	1303	1440	2047	T_{Clock}
	Active	T_{HD}	1280	1280	1280	
	Blanking	T_{HB}	23	160	767	

Note : 1. DE mode only

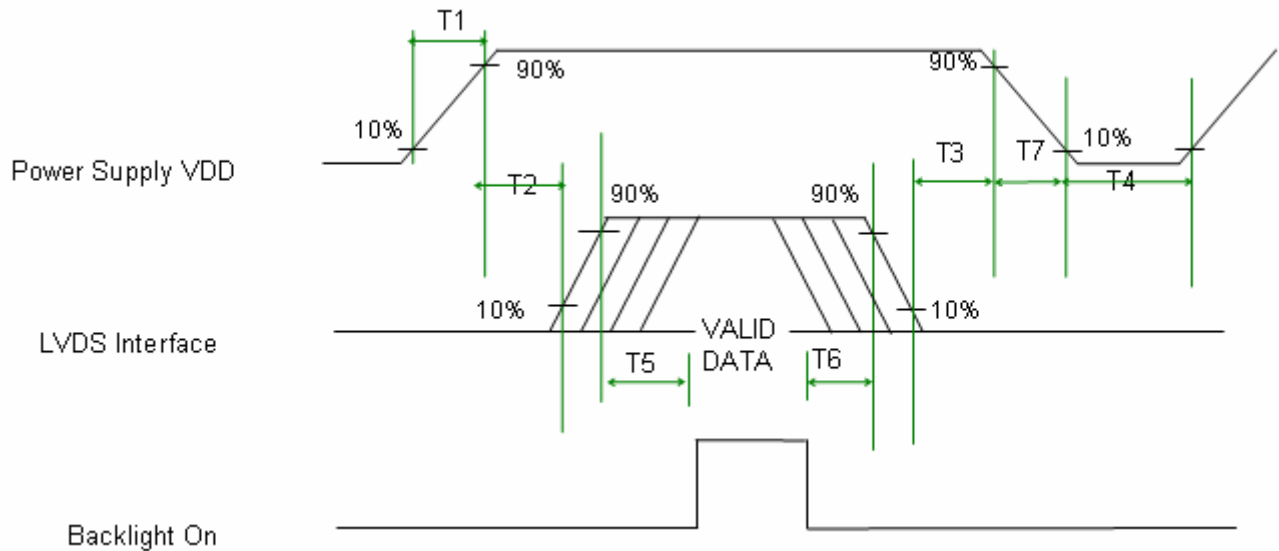
2. The designed minimum value of “Frame Rate” is 50 Hz. When “Frame Rate” is set to be 40 Hz, flicker syndrome may occur.

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.3	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	-	(ms)
T4	150	-	-	(ms)
T5	200	-	-	(ms)
T6	0	-	-	(ms)
T7	0	-	10	(ms)

Note: Minimum value of T6 parameter is designed to be 200 ms. If the value is set to be 0 ms, display garbage may occur



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7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XB30SL-HF10
Mating Housing/Part Number	F1-X30H
Mating Contact/Part Number	F1-XC3-1-15000

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage



8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5G
- Frequency: 10 - 200Hz ,X,Y,Z axis 30minutes for each axis

8.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: (1) 50G 18 msec trapezoidal(2)210G,3msec half sine,1 time for +/-x,+/-y,+/-z direction



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9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	50 /80~85%,1000Hr	
Low Temperature Operation	0 /,500Hr	
Life test	25 ,1000Hr	
On/Off Test	25 , ON/30sec. OFF/30sec., 30,000 cycles	
Hot Storage	60 ,240 hours	
Cold Storage	-20 ,24 0 hours	
Thermal Shock Test	-20 /30 min ,60 /30 min 100cycles	
Shock Test (Non-Operating)	(1)50G 18 msec trapezoidal(2)210G,3msec half sine,1 time for +/-x,+/-y,+/-z direction	
Vibration Test (Non-Operating)	10 - 200Hz ,X,Y,Z axis 30minutes for each axis	
ESD	Contact : ±8KV, operation, class B Air : ±15KV, operation, class B	Note 1

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost
Self-recoverable. No hardware failures.

Note2: CCFL Life time: 12,000 hours minimum under normal module usage.

Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

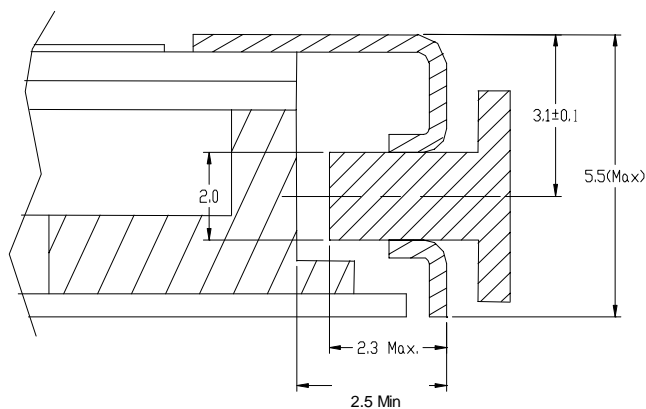
10.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface = 2.5 mm (See drawing)

Screw hole center location, from front surface = 3.1 ± 0.1 mm (See drawing)

Suggestions: Customers' Screw maximum length = 2.3 mm (See drawing)

Screw Torque: Maximum 2.5 kgf-cm





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11. Shipping and Package

11.1 Shipping Label Format



IC combination	Control code	H/W
Source IC:NEC Gate IC:MEC	0AXXG	0A
Source IC: Novatec Gate IC: Novatec	1AXXG	1A



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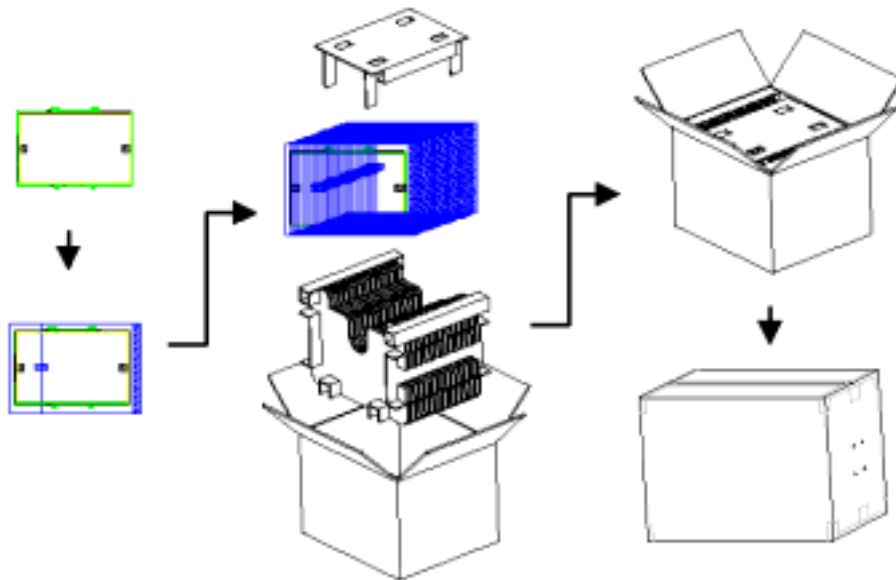
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11.2. Carton package

Carton Label: 80mm * 40mm



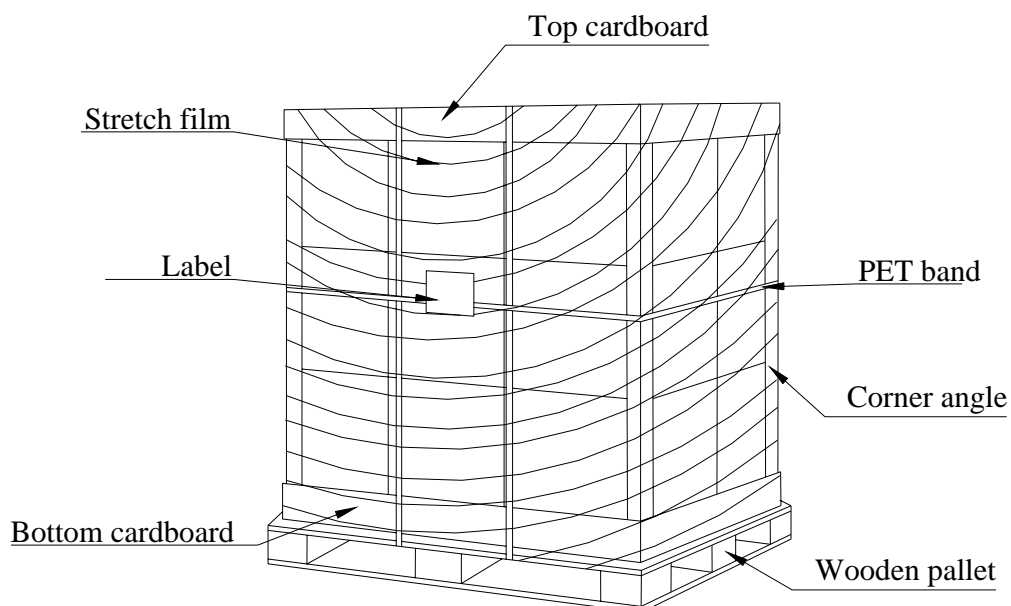
The outside dimension of carton is 454(L)mm* 388(W)mm* 352(H)mm, carton and cushion weight are 2920g.



11.3 Shipping package of palletizing

By air : 6 *4 layers, one pallet put 24 boxes, total 480 pcs module.

By sea : 6 *5 layers, one pallet put 30 boxes, total 600 pcs module.





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12. Appendix: EDID description

Byte# (decimal)	Byte# (HEX)	Field Name and Comments	Data (decimal)	Data (HEX)	Data (BIN)
0	00	Header	0	00	00000000
1	01	Header	255	FF	11111111
2	02	Header	255	FF	11111111
3	03	Header	255	FF	11111111
4	04	Header	255	FF	11111111
5	05	Header	255	FF	11111111
6	06	Header	255	FF	11111111
7	07	Header	0	00	00000000
8	08	ID system Manufacturer Name	48	30	00110000
9	09	Compressed ASCII	174	AE	10101110
10	0A	ID Product Code (LSB)	49	31	00110001
11	0B	ID Product Code (MSB)	64	40	01000000
12	0C	LCD Module Serial No.	0	00	00000000
13	0D	LCD Module Serial No.	0	00	00000000
14	0E	LCD Module Serial No.	0	00	00000000
15	0F	LCD Module Serial No.	0	00	00000000
16	10	Week of Manufacture	1	01	00000001
17	11	Year of Manufacture	16	10	00010000
18	12	EDID Structure version	1	01	00000001
19	13	EDID Revision	3	03	00000011
20	14	Video Input Definition	128	80	10000000
21	15	Max H image size(cm)	30	1E	00011110
22	16	Max V image size(cm)	19	13	00010011
23	17	Display gamma	120	78	01111000
24	18	Feature support(DPMS)	234	EA	11101010
25	19	Red/Green low Bits	135	87	10000111
26	1A	Blue/White Low Bits	197	C5	11000101
27	1B	Red X	148	94	10010100
28	1C	Red Y	87	57	01010111
29	1D	Green X	79	4F	01001111
30	1E	Green Y	140	8C	10001100
31	1F	Blue X	39	27	00100111
32	20	Blue Y	37	25	00100101
33	21	White X	80	50	01010000
34	22	White Y	84	54	01010100
35	23	Established Timing I	0	00	00000000
36	24	Established Timing II	0	00	00000000
37	25	Manufacturer's Timings	0	00	00000000
38	26	Standard Timing Identification 1	1	01	00000001
39	27	Standard Timing Identification 1	1	01	00000001



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40	28	Standard Timing Identification 2	1	01	00000001
41	29	Standard Timing Identification 2	1	01	00000001
42	2A	Standard Timing Identification 3	1	01	00000001
43	2B	Standard Timing Identification 3	1	01	00000001
44	2C	Standard Timing Identification 4	1	01	00000001
45	2D	Standard Timing Identification 4	1	01	00000001
46	2E	Standard Timing Identification 5	1	01	00000001
47	2F	Standard Timing Identification 5	1	01	00000001
48	30	Standard Timing Identification 6	1	01	00000001
49	31	Standard Timing Identification 6	1	01	00000001
50	32	Standard Timing Identification 7	1	01	00000001
51	33	Standard Timing Identification 7 was not used	1	01	00000001
52	34	Standard Timing Identification 8 was not used	1	01	00000001
53	35	Standard Timing Identification 8 was not used	1	01	00000001
54	36	Pixel Clock/10,000 (LSB)	13	0D	00001101
55	37	Pixel Clock/10,000 (MSB) /	27	1B	00011011
56	38	Horizontal Active	0	0	00000000
57	39	Horizontal Blanking	124	7C	01111100
58	3A	Horizontal Active : Horizontal Blanking	80	50	01010000
59	3B	Vertical Active	32	20	00100000
60	3C	Vertical Blanking	22	16	00010110
61	3D	Vertical Active : Vertical Blanking	48	30	00110000
62	3E	Horizontal Sync. Offset	48	30	00110000
63	3F	Horizontal Sync Pulse Width	32	20	00100000
64	40	Vertical Sync Offset : Sync Width	54	36	00110110
65	41	Horizontal Vertical Sync Offset/Width upper 2bits	0	0	00000000
66	42	Horizontal Image Size	48	30	00101111
67	43	Vertical Image Size	190	BE	10111110
68	44	Horizontal & Vertical Image Size (upper 4bit)	16	10	00010000
69	45	Horizontal Border = 0	0	0	00000000
70	46	Vertical Border = 0	0	0	00000000
71	47	Non-interlaced,Normal display,no stereo,Digital separate sync,H/V pol negatives	24	18	00011000
72	48	Pixel Clock/10,000 (LSB) 50Hz	139	8B	10001011
73	49	Pixel Clock/10,000 (MSB) / 50Hz	22	16	00010110
74	4A	Horizontal Active	0	0	00000000
75	4B	Horizontal Blanking	124	7C	01111100
76	4C	Horizontal Active : Horizontal Blanking	80	50	01010000
77	4D	Vertical Active	32	20	00100000
78	4E	Vertical Blanking	22	16	00010110
79	4F	Vertical Active : Vertical Blanking	48	30	00110000
80	50	Horizontal Sync. Offset	48	30	00110000
81	51	Horizontal Sync Pulse Width	32	20	00100000
82	52	Vertical Sync Offset : Sync Width	54	36	00110110
83	53	Horizontal Vertical Sync Offset/Width upper 2bits	0	00	00000000
84	54	Horizontal Image Size	48	30	00101111



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85	55	Vertical Image Size	190	BE	10111110
86	56	Horizontal & Vertical Image Size (upper 4bit)	16	10	00010000
87	57	Horizontal Border = 0	0	00	00000000
88	58	Vertical Border = 0	0	00	00000000
89	59	Non-interlaced,Normal display,no stereo,Digital separate sync,H/V pol negatives	24	18	00011000
90	5A	Detailed Timing Descriptor #3	0	00	00000000
91	5B		0	00	00000000
92	5C		0	00	00000000
93	5D		15	0F	00001111
94	5E		0	00	00000000
95	5F	(Horizontal active pixel /8)-31	129	81	10000001
96	60	Image Aspect Ratio(15:9)	10	0A	00001010
97	61	Low Refresh Rate #1(50Hz)	50	32	00110010
98	62	(Horizontal active pixel /8)-31	129	81	10000001
99	63	Image Aspect Ratio(16:10)	10	0A	00001010
100	64	Low Refresh Rate #2(40Hz)	40	28	00101000
101	65	Brightness(1/10nit)	18	12	00010010
102	66	Feature flag(TN mode)	1	01	00000001
103	67	Reserved 00h	0	00	00000000
104	68	EISA manufacturer code(3 Character ID)	6	06	00000110
105	69	Compressed ASCII	175	AF	10101111
106	6A	Panel Supplier Reserved - Product code	68	44	01000100
107	6B	(Hex, LSB first)	36	24	00100100
108	6C	Detailed Timing Descriptor #4	0	00	00000000
109	6D		0	00	00000000
110	6E		0	00	00000000
111	6F		254	FE	11111110
112	70		0	00	00000000
113	71	(Supplier S/N)	66	42	01000010
114	72	(Supplier S/N)	49	31	00110001
115	73	(Supplier S/N)	52	34	00110100
116	74	(Supplier S/N)	49	31	00110001
117	75	(Supplier S/N)	69	45	01000101
118	76	(Supplier S/N)	87	57	01010111
119	77	(Supplier S/N)	48	30	00110000
120	78	(Supplier S/N)	50	32	00110010
121	79	(Supplier S/N)	32	20	00100000
122	7A	(Supplier S/N)	86	56	01010110
123	7B	(Supplier S/N)	52	34	00110100
124	7C	(Supplier S/N)	32	20	00100000
125	7D	(Supplier S/N)	10	0A	00001010
126	7E	Extension flag = 00	0	00	00000000
127	7F	Checksum	193	C1	11000001