CUSTOMER APPROVAL SHEET

Company Name	
MODEL	A050FW02 V2
CUSTOMER APPROVED	Title : Name :

☐ APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.)

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☐ CUSTOMER REMARK :

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P/N : 97.05A10.200

: 97.05A10.201

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Product Specification

5" COLOR TFT-LCD MODULE/PANEL

MODEL NAME: A050FW02 V2

97.05A10.200

97.05A10.201

< >Preliminary Specification
<□>Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0			First Draft
0.1	2009/4/22	5,6	Modify pin NO. of SPI interface
0.2	2009/5/12	4 6	1)Drawing update 2)Pin 36：HV mode or DE mode control signal
0.3	2009/7/07	4 22	1)Drawing update：white-line mark change of connect 2) Reliability Test Items：pressure test
0.4	2009/7/16	4 12 17	1) Drawing update 2)Serial Command Setting 3)RGB chromaticity update
0.5	2009/8/12	4 12 20	1)Drawing update：conductive copper tape 2)Suggested Serial Command Settings 3)touch panel：operation force
0.6	2009/09/07	17	chromaticity tolerance from +/- 0.05 to +/- 0.04
0.7	2009/10/05	4 26 12	Drawing update:insulation tape Ordering information for touch panel Suggested Serial Command Settings

Contents

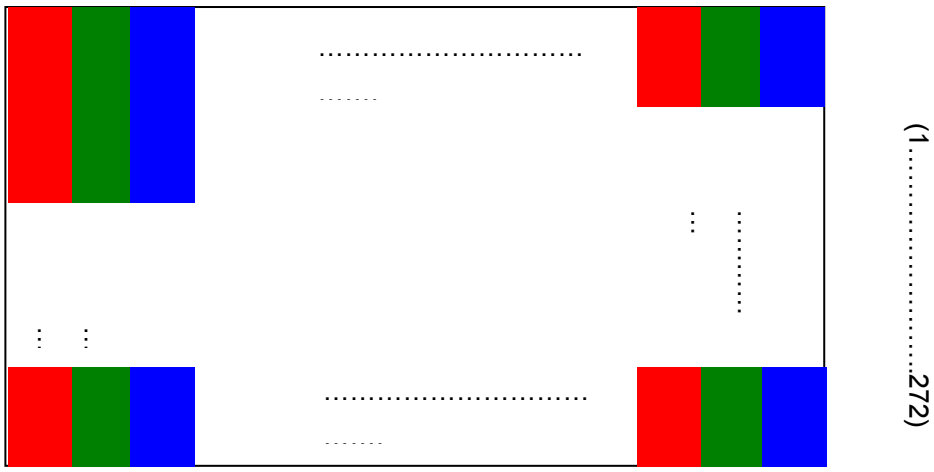
A. General Information

This product is for portable PND and digital photo frame application.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	5.0(Diagonal)	
2	Display Resolution	dot	480RGB (H) X 272 (V)	
3	Overall Dimension	mm	120.7(H) X 75.8(V) X 4.25(T)	Note 1
4	Active Area	mm	110.88 (H) X 62.832 (V)	
5	Pixel Pitch	mm	0.231 (H) X 0.231 (V)	
6	Color Configuration	--	R. G. B. Stripe	Note 2
7	Color Depth	--	16.7M Colors	Note 3
8	NTSC Ratio (Cell)	%	54	
9	Display Mode	--	Normally White	
10	Panel surface Treatment	--	Anti-Glare, 3H	
11	Weight	g	75	
12	Power Consumption	mW	930	Note 4
13	Viewing direction		6 o'clock (gray inversion)	

Note 1: Not include blacklight cable and FPC. Refer next page to get further information.

Note 2: Below figure shows dot stripe arrangement.

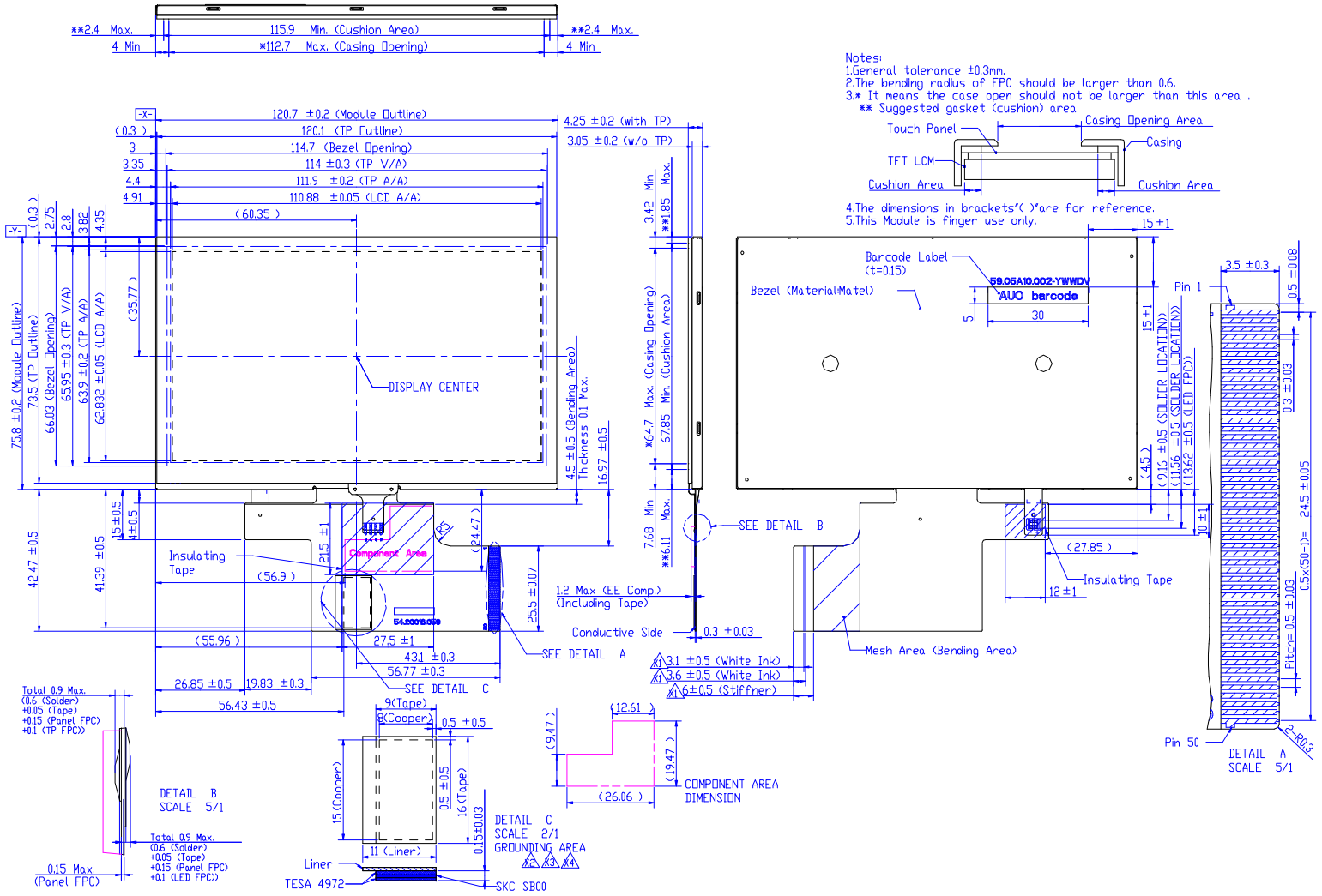


Note 3: The full color display depends on 24-bit data signal.

Note 4: Please refer to Electrical Characteristics chapter.

B. Outline Dimension

1. TFT-LCD Module – Front and Rear View



C. Electrical Specifications

1. TFT LCD Panel Pin Assignment

Recommended connector: 6702-E50N-00R

No.	Pin Name	I/O	Description	Remarks
1	GND	G	GND	
2	GND	G	GND	
3	AVDD	PI	Power supply for analog circuit	
4	DVDD	PI	Power supply for digital interface	
5	R0	I	Red Data Signal (LSB)	
6	R1	I	Red Data Signal	
7	R2	I	Red Data Signal	
8	R3	I	Red Data Signal	
9	R4	I	Red Data Signal	
10	R5	I	Red Data Signal	
11	R6	I	Red Data Signal	
12	R7	I	Red Data Signal (MSB)	
13	G0	I	Green Data Signal (LSB)	
14	G1	I	Green Data Signal	
15	G2	I	Green Data Signal	
16	G3	I	Green Data Signal	
17	G4	I	Green Data Signal	
18	G5	I	Green Data Signal	
19	G6	I	Green Data Signal	
20	G7	I	Green Data Signal (MSB)	
21	B0	I	Blue Data Signal (LSB)	
22	B1	I	Blue Data Signal	
23	B2	I	Blue Data Signal	
24	B3	I	Blue Data Signal	
25	B4	I	Blue Data Signal	
26	B5	I	Blue Data Signal	
27	B6	I	Blue Data Signal	
28	B7	I	Blue Data Signal (MSB)	
29	GND	G	GND	
30	DCLK	I	Pixel clock	
31	CSB	I	3-wire I/F chip select pin	
32	HSYNC	I	Horizontal synchronizing signal	
33	VSYNC	I	Vertical synchronizing signal	
34	DE	I	Data enable	
35	GND	G	GND	

No.	Pin Name	I/O	Description	Remarks
36	HVDSL	I	HV mode or DE mode control signal. HVDSL="H": Set under HV mode, VSD and HSD signal must be provide by system. HVDSL="L": Set under DE mode, DE signal must be provided by system.	
37	NC		No connect	
38	SCL	I	3-wire I/F clock input pin	
39	SDA	I	3-wire I/F data input pin	
40	GND	G	GND	
41	TP_R	I/O	X Right	
42	TP_B	I/O	Y Bottom	
43	TP_L	I/O	X Left	
44	TP_U	I/O	Y Up	
45	GND	G	GND	
46	VLED-	PI	LED backlight cathode	
47	NC	-	No connect	
48	VLED+	PI	LED backlight anode	
49	GND	G	GND	
50	GND	G	GND	

I: Digital signal input, O: Digital signal output, G: GND, PI: Power input, C: Capacitor

2. Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Analog Power Voltage	AVDD	GND=0	-0.3	5	V	
Logic Power Voltage	DVDD	GND=0	-0.5	5	V	
Input signal voltage	Data	GND=0	-0.3	3.6	V	Digital Signals

Note 1: Functional operation should be restricted under ambient temperature (25℃).

Note2: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

3. Electrical DC Characteristics

a. Typical Operation Condition (GND = 0V)

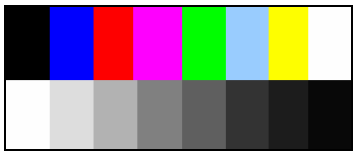
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Analog Power Voltage		AVDD	3.0	3.3	3.6	V	
Digital interface Power Voltage		DVDD	1.7	-	VDD	V	
Digital Input Signal Voltage	H Level	VIH	0.7 x DVDD	--	DVDD	V	
	L Level	VIL	GND	--	0.3 x DVDD	V	

b. Current Consumption (GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for AVDD	I_{VDD}	AVDD=3.3V	-	15	18	mA	Note 1, 2
	I_{VDD} (STANDBY)	AVDD=3.3V	-	15	20	uA	Note 3

Note 1:Test Condition is under typical Eletrical DC and AC characteristics.

Note 2: Test pattern is the following picture.



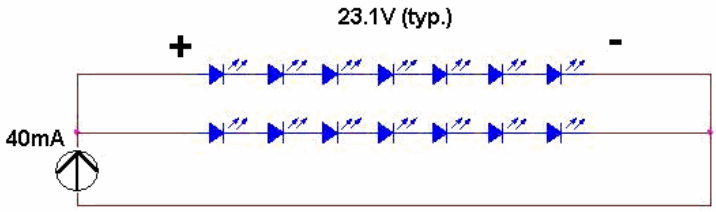
Note 3:In standby mode, all digital signals are stopped. Ex. DCLK,DE ..etc.

c. Backlight Driving Conditions

The backlight (LED module, Note 1) is suggested to drive by constant current with typical value.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	I_L	--	20	22	mA	Note 1
Power Consumption	V_L	--	924	1108.8	mW	
LED Life Time	L_L	10,000	--	--	Hr	Note 2, 3

Note 1:LED backlight is two parallel strings and one LED for each string is as below figure. Suggest to drive by 20mA for each LED string.



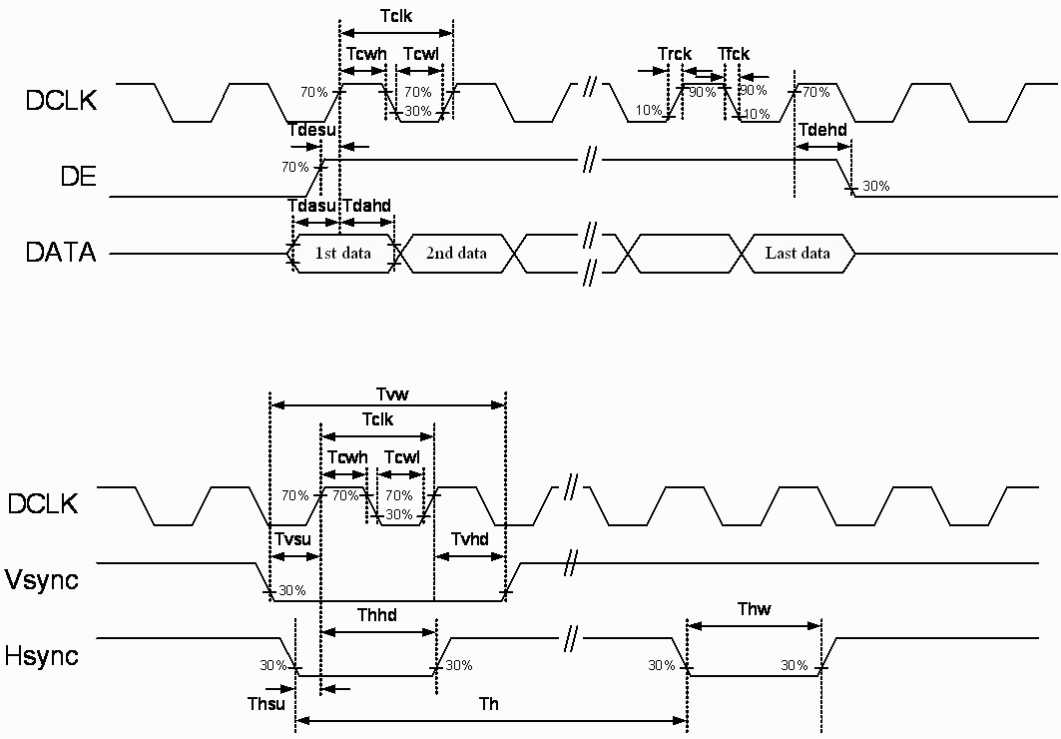
Note 2:Define “LED Lifetime”: brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25℃ and LED lightbar current = 20mA.

Note 3:If it uses larger LED lightbar voltage/ current more than 20mA, it maybe decreases the LED lifetime.

4. Electrical AC Characteristics

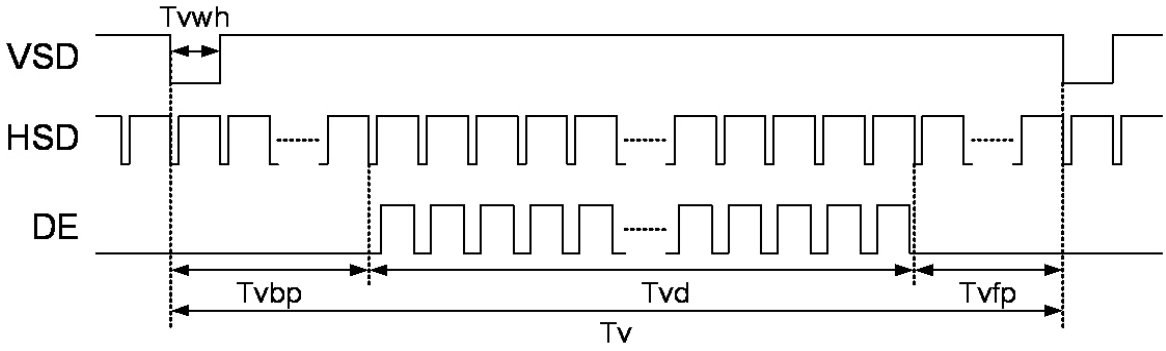
a. Signal AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK clock time	T_{clk}	83	-	-	ns	Parallel RGB Mode
Clock rising time	T_{rck}	9	-	-	ns	
Clock falling time	T_{fck}	9	-	-	ns	
HSD width	T_{hwh}	1	-	-	DCLK	
HSD period time	T_h	55	-	-	us	
HSD setup time	T_{hsu}	12	-	-	ns	
HSD hold time	T_{hhd}	12	-	-	ns	
VSD width	T_{vwh}	1	-	-	Th	
VSD setup time	T_{vsu}	12	-	-	ns	
VSD hold time	T_{vhd}	12	-	-	ns	
DE setup time	t_{desu}	12	-	-	ns	
DE hold time	t_{dehd}	12	-	-	ns	
Data setup time	t_{dst}	12	-	-	ns	
Data hold time	t_{dhd}	12	-	-	ns	



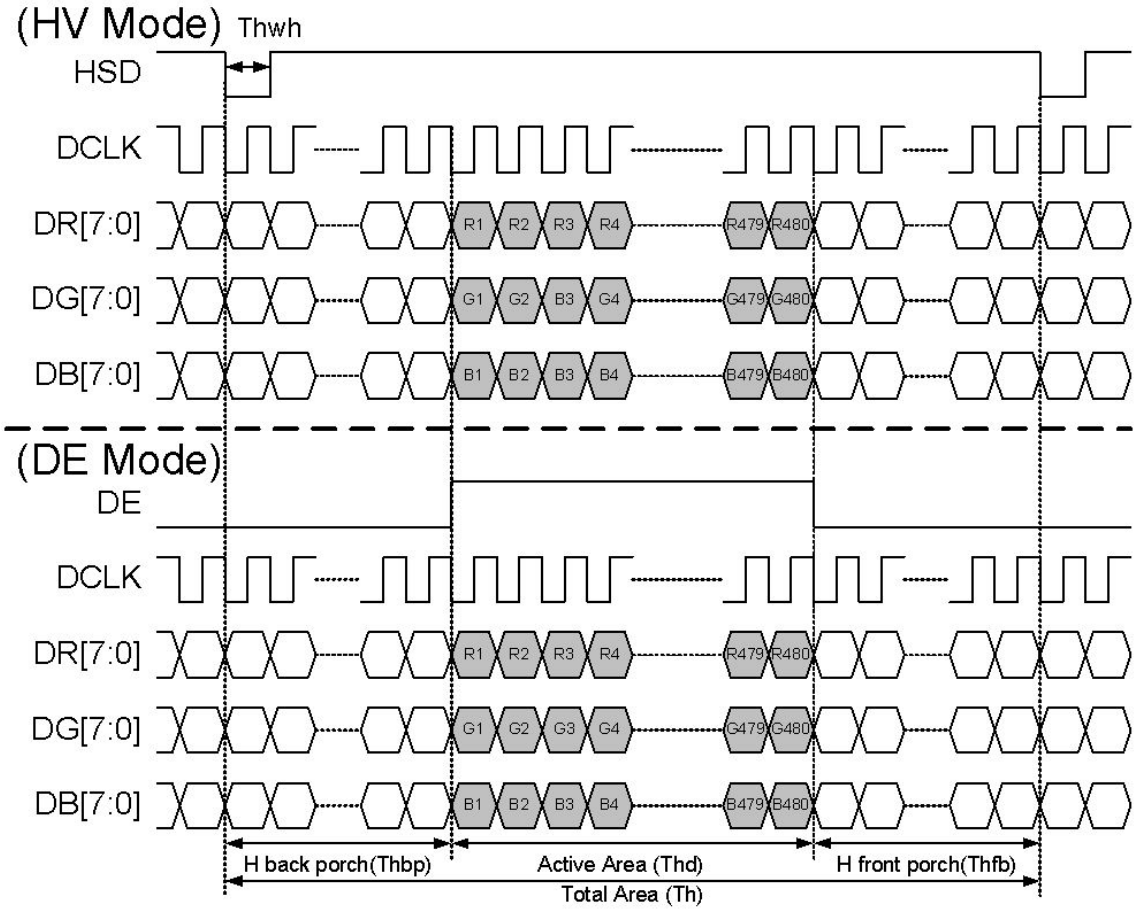
b. Input Timing

Vertical Timing of Input



Horizontal Timing of Input

Parallel RGB Mode Data format



Parallel RGB input timing table

PARAMETER	Symbol	Min	Typ	Max	Unit
DCLK frequency	fclk	5	9	12	MHz
Horizontal Signal					
HSD period time	Th	520	525	800	DCLK
HSD display area	Thd	-	480	-	DCLK
HSD back porch	Thbp	36	40	255	DCLK
HSD front porch	Thfp	4	5	65	DCLK
Vertical Signal					
VSD period time	Tv	277	288	400	H
VSD display area	Tvd	-	272	-	H
VSD back porch	Tvbp	3	8	31	H
VSD front porch	Tvfp	2	8	93	H

5. Serial Interface Characteristics

5.1 3-Wire Command Format

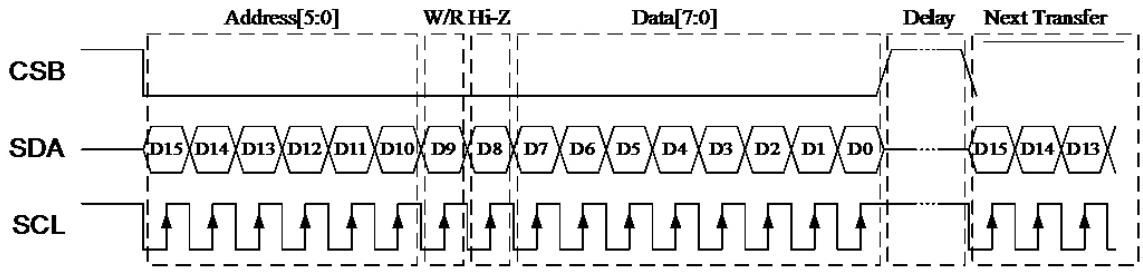
The 3-wire communication can be bi-directionally controlled by the “R/W” bit in the address field. The 3-wire engine acts as a “slave mode” at all times, and will not issue any command to the 3-wire bus itself.

Under read mode, the 3-wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by an external controller. Data in the “Hi-Z phase” will be ignored by the 3-wire engine during write operation, and should be ignored during read operation as well.

During read operation, an external controller should float the SDA pin under “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bits. To prevent incorrect setting of the internal register, any write operation with more or less than 16 bits of data during a CSB Low period will be ignored by the 3-wire engine.

To prevent incorrect setting of the internal register, refer to the section “3-Wire Timing Diagram” for detailed timing.



3-Wire Command Format:

Bit	Description
D15-D10	Register Address [5:0].
D9	W/R control bit. “0” for Write; “1” for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7-D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format:

MSB															**LSB**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Register Address [5:0]						**0**	**X**	DATA (Issue by external controller)							

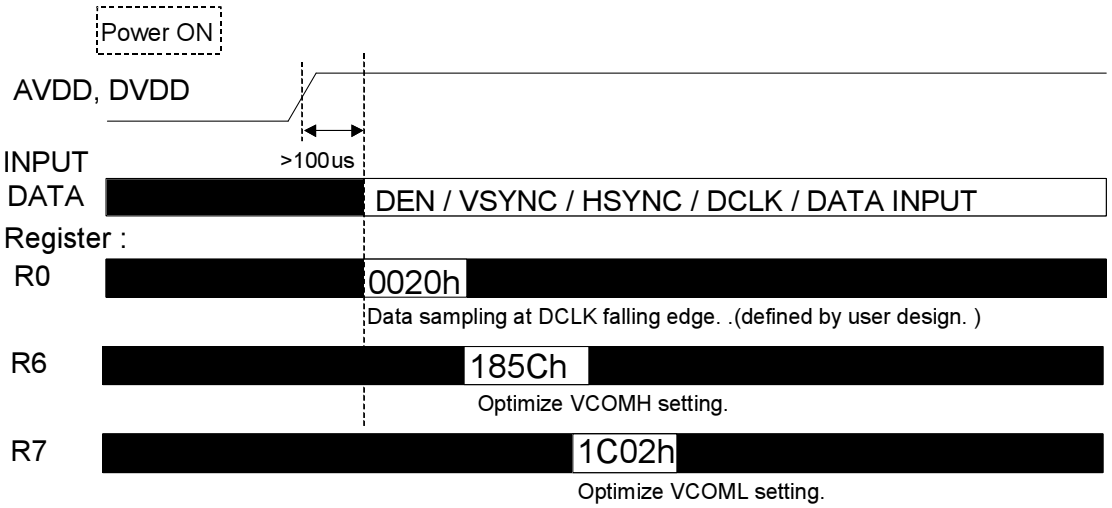
3-Wire Read Format:

MSB															**LSB**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Register Address [5:0]						**1**	Hi-Z	DATA (Issue by 3-Wire engine)							

5.2 3-Wire Control Register List

NO.	Address						R/W	D8	MSB	Initial value						LSB
	D15	D14	D13	D12	D11	D10	D9		D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	R/W(0)	X	HSDPOL	VSDPOL	CLKPOL	FPOL	NFSEL	00		DITHB
									0	0	0	0	0	0	0	0
R1	0	0	0	0	0	1	R/W(0)	X	0	0	0	1	STB	GRB	SHLR	UPDN
									0	0		1	1	1	1	1
R4	0	0	0	1	0	0	R/W(0)	X	DDL[7:0]							
									0	0	1	0	1	0	0	0
R5	0	0	0	1	0	1	R/W(0)	X	0	0	0	HDL[4:0]				
												0	1	0	0	0
R6	0	0	0	1	1	0	R/W(0)	X	0			VCOMH[6:0]				
									0	1	0	0	1	1	0	1
R7	0	0	0	1	1	1	R/W(0)	X	0	VCOML[6:0]						
									0	0	0	1	1	0	1	1
R8	0	0	1	0	0	0	R/W(0)	X	BRI[7:0]							
									0	1	0	0	0	0	0	0
R9	0	0	1	0	0	1	R/W(0)	X	CON_B[7:0]							
									0	1	0	0	0	0	0	0
R10	0	0	1	0	1	0	R/W(0)	X	0	SUB_BRI_R[6:0]						
										1	0	0	0	0	0	0
R11	0	0	1	0	1	1	R/W(0)	X	0	SUB_CON_R[6:0]						
										1	0	0	0	0	0	0
R12	0	0	1	1	0	0	R/W(0)	X	0	SUB_BRI_B[6:0]						
										1	0	0	0	0	0	0
R13	0	0	1	1	0	1	R/W(0)	X	0	SUB_CON_B[6:0]						
										1	0	0	0	0	0	0

5.3 Suggested Serial Command Settings

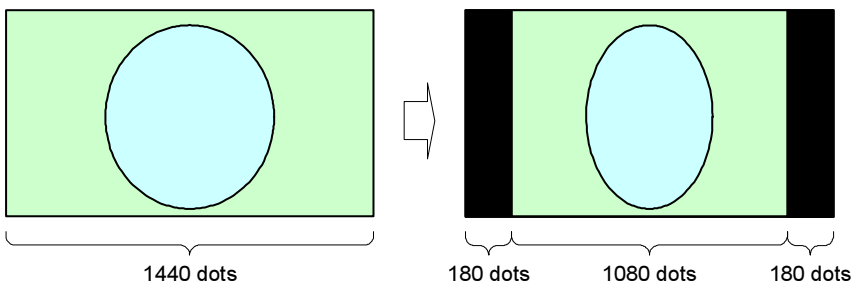


5.4 3-wire Registers Function Description

R0: Timing Controller Function Register

Designation	Address	Description
DITHB	R0[0]	Dithering control bit. DITHB=”1”, Dithering off, (7-bits resolution, truncation last 1-bits of the input data) DITHB=”0”, Dithering on, (Pseudo 8-bits resolution). (Default)
NFSEL	R0[3]	Narrow display mode selection bit. NFSEL=”1”: Narrow display format is enable. NFSEL=”0”: Normally display. (Default)
FPOL	R0[4]	VCOM polarity inverse control bit. When FPOL=”1”, VCOM inverse polarity. When FPOL=”0”, VCOM normal polarity. (Default)
CLKPOL	R0[5]	DCLK polarity control bit. CLKPOL=”1”: Data sampling at DCLK falling edge. CLKPOL=”0”: Data sampling at DCLK rising edge. (Default)
VSDPOL	R0[6]	VSD polarity control bit. VSDPOL=”1”: VSD positive polarity. VSDPOL=”0”: VSD negative polarity. (Default)
HSDPOL	R0[7]	HSD polarity control bit. VSDPOL=”1”: HSD positive polarity. VSDPOL=”0”: HSD negative polarity. (Default)

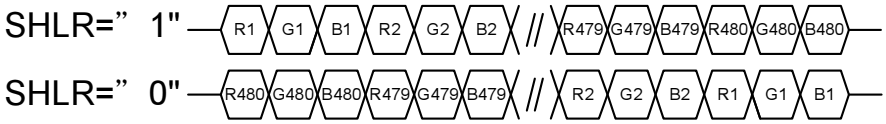
Narrow display mode



R1: Timing Controller Function Register

Designation	Address	Description
UPDN	R1[0]	Gate driver Up/Down scan control of gate driver. UPDN="1", Shift from up to down, First line=L1->L2-> … ->L543->L544=Last line (Default) UPDN="0", Shift from down to up, First line=L544->L543-> … ->L2->L1=Last line
SHLR	R1[1]	Right/Left sequence control of source driver. SHLR="1", Shift right: First data=S1->S2->S3 … ->S720=Last data (Default) SHLR="0", Shift left: Last data=S1<-S2<-S3 … <-S720=First data
GRB	R1[2]	Global reset bit. GRB="1", Normal operation. (Default) GRB="0", The controller is in reset state.
STB	R1[3]	Standby mode selection bit. STB="1", Normal operation. (Default) STB="0", Timing control, driver and DC-DC converter, are off, and all outputs are High-Z.

NOTE: When SHLR="0", input RGB sequence does not need to sweep in serial mode.



R4: Data Delay Setting

Designation	Address	Description			
DDL[7:0]	R4[7:0]	Select the HSD signal to 1'st input data delay timing.			
		DDL[7:0]	DDL function	Unit	
		24H	36(Minimum setting for Parallel mode)	DCLK	
		28H	40(Default setting for Parallel mode)		
		6CH	108(Minimum setting for Serial mode)		
		78H	120(Default setting for Serial mode)		
		FFH	255		

Note: DDL function will be disabled under 8/24 bit DE mode.

R5: HSD Delay Setting

Designation	Address	Description			
HDL[4:0]	R5[4:0]	Select the Gate start pulse output delay timing.			
		HDL[4:0]	HDL function	Unit	
		02H	2(minimum setting)	HSD	
		08H	8(Default)		
		1FH	31		

Note: HDL function will be disabled under 8/24 bit DE mode.

R6: VCOMH Level Control Register

Designation	Address	Description				
VCOMH[6:0]	R6[6:0]	VCOMH level adjustment. (20mV/LSB)				
			VCOMH[6:0]	VCOMH level	Unit	
			00H	2.46	V	
			1BH	3		
			4DH	4		
			7FH	5		
OTP_VCOMH	R6[7]	VCOMH data source selection register OTP_VCOMH="1", VCOMH is switched to the 3-wire register memory when the user wants to adjust the VCOMH level. OTP_VCOMH="0", VCOMH is read from OTP memory. (Default)				

Note: VCOMH setting have to greater then AVDD.

R7: VCOML Control Register

Designation	Address	Description				
VCOML[6:0]	R7[6:0]	VCOML level adjustment. (20mV/LSB)				
			VCOML[6:0]	VCOML level	Unit	
			00H	-0.46	V	
			1BH	-1(Default)		
			4DH	-2		
			7FH	-3		
OTP_VCOML	R7[7]	VCOML data source selection register OTP_VCOML="1", VCOML is switched to the 3-wire register memory when the user wants to adjust the VCOML level. OTP_VCOML="0", VCOML is read from OTP memory. (Default)				

R8: Brightness Control Register

Designation	Address	Description			
BRI[7:0]	R8[7:0]	Brightness level setting; gain changes 1 step/bit			
			BRI[7:0]	Brightness gain	
			00H	Dark (-64)	
			40H	Center (0) (Default)	
			FFH	Bright (+191)	

R9: Contrast Control Register

Designation	Address	Description			
CON[7:0]	R9[7:0]	Contrast level setting; gain changes (1/64)/bit			
			CON[7:0]	Contrast gain	
			00H	0	
			40H	1(Default)	
			FFH	3.984	

R10: SUB_Brightness_R Control Register

Designation	Address	Description			
SUB_BRI_R[6:0]	R10[6:0]	Red sub-pixel brightness level setting; setting accuracy: 1 step/bit			
			SUB_BRI_R[7:0]	R Brightness gain	
			00H	Dark (-64)	
			40H	Center (0) (Default)	
			7FH	Bright (+63)	

R11: SUB_Contrast_R Control Register

Designation	Address	Description			
SUB_CON_R[6:0]	R11[6:0]	Red sub-pixel contrast level setting; gain changes (1/256)/bit			
			SUB_CON_R[7:0]	R Contrast gain	
			00H	0.75	
			40H	1(Default)	
			7FH	1.246	

R12: SUB_Brightness_B Control Register

Designation	Address	Description			
SUB_BRI_B[6:0]	R12[6:0]	Blue sub-pixel brightness level setting; setting accuracy: 1 step/bit			
			SUB_BRI_B[7:0]	B Brightness gain	
			00H	Dark (-64)	
			40H	Center (0) (Default)	
			7FH	Bright (+63)	

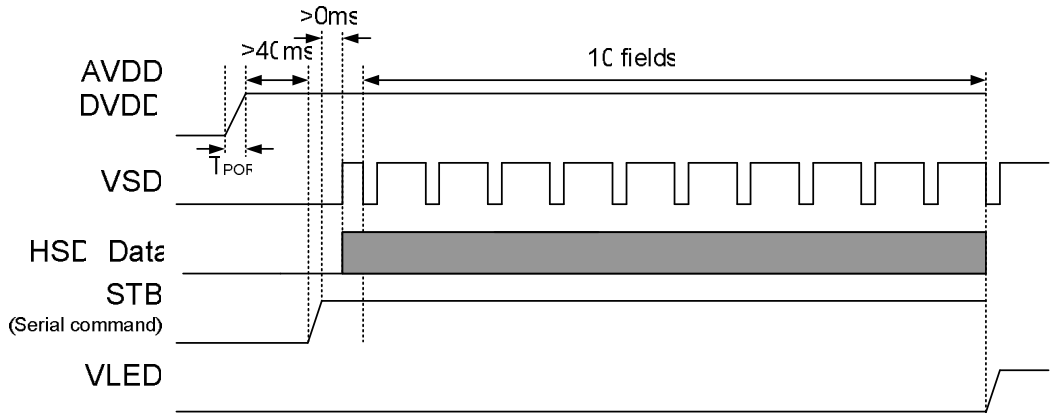
R13: SUB_Contrast_B Control Register

Designation	Address	Description			
SUB_CON_B[6:0]	R13[6:0]	Blue sub-pixel contrast level setting; gain changes (1/256)/bit			
			SUB_CON_B[7:0]	B Contrast gain	
			00H	0.75	
			40H	1(Default)	
			7FH	1.246	

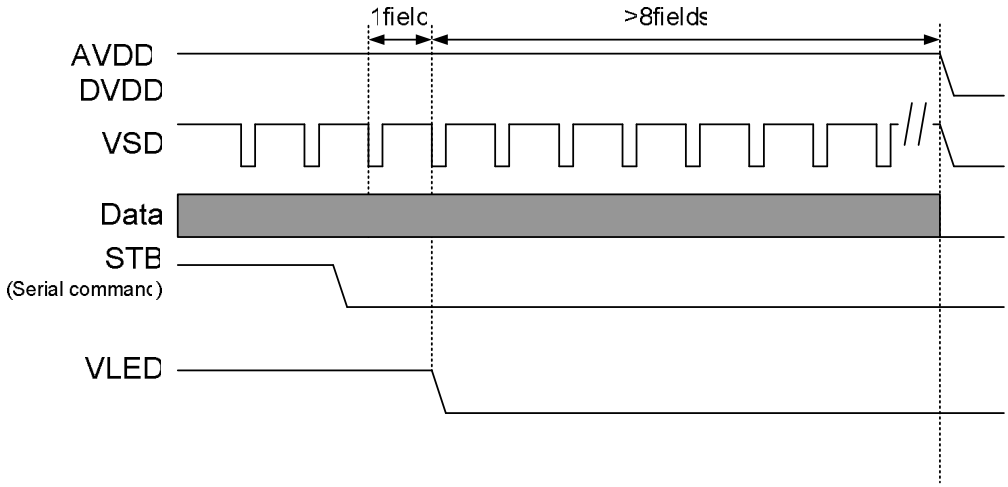
6. Power On/Off Characteristics

a. Recommended Power On Sequence

The LCD apopts high voltage driver IC, so it could be permanently damaged under a wrong power on/off sequence. The suggested LCD power sequence is below：



b. Recommended Power Off Sequence



Notes: IC internal default setting STB=”1”, Normal operation.

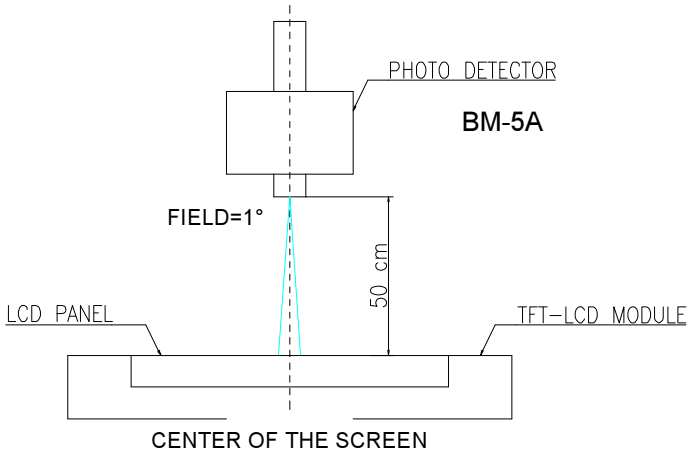
D. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall	Tr Tf	θ=0°	- -	7 23	- -	ms ms	Note 3
Contrast ratio	CR	At optimized viewing	400	500	-		Note 4
Viewing Angle Top Bottom Left Right		CR≧10	 - - - -	 40 60 70 70	 - - - 	 deg. 	Note 5
Brightness	Y_L	θ=0°	350	400	-	cd/m^2	Note 6
Chromaticity	Rx	θ=0°	0.568	0.608	0.648		
	Ry	θ=0°	0.311	0.351	0.391		
	Gx	θ=0°	0.290	0.330	0.370		
	Gy	θ=0°	0.536	0.576	0.616		
	Bx	θ=0°	0.113	0.153	0.193		
	By	θ=0°	0.042	0.082	0.122		
	Wx	θ=0°	0.27	0.31	0.35		
	Wy	θ=0°	0.29	0.33	0.37		

Note 1: Ambient temperature =25℃, and LED lightbar voltage V_L = 12 V. To be measured in the dark room.

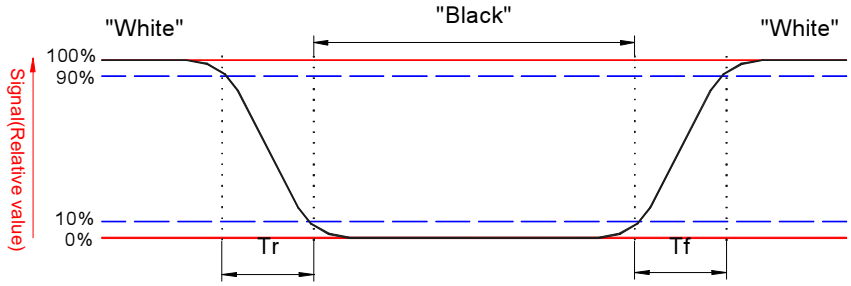
Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.



Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

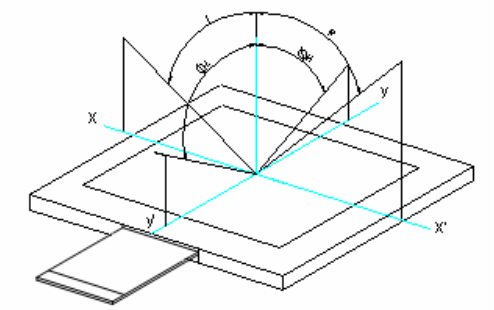


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

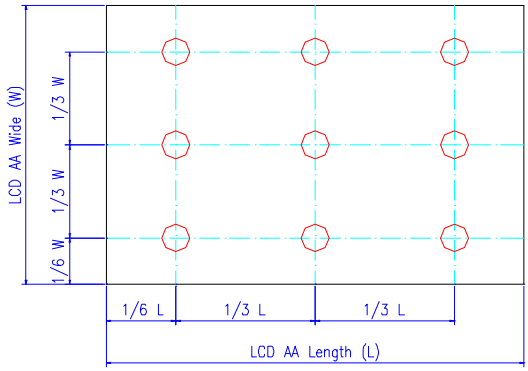
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

E. Touch Screen Panel Specifications

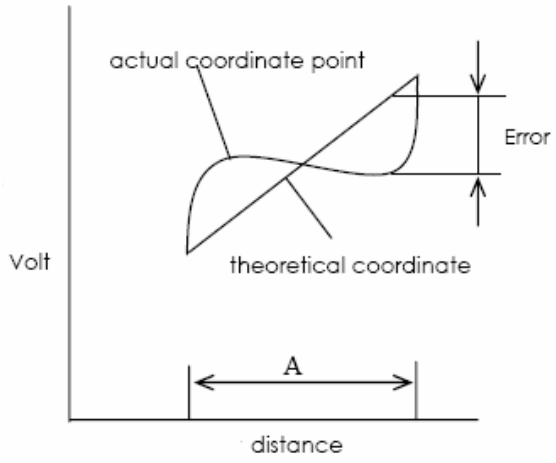
1. FPC Pin Assignment

Pin No.	Symbol	I/O	Description
1	X1	I/O	Touch panel right electrode (R)
2	Y2	I/O	Touch panel bottom electrode (B)
3	X2	I/O	Touch panel left electrode (L)
4	Y1	I/O	Touch panel top electrode (U)

2. Electrical Characteristics

Item		Min.	Typ	Max.	Unit	Remark
Rate DC Voltage		--	--	7	V	
Resistance	X (Film)	500	--	1500	Ω	At connector
	Y (Glass)	100	--	700		
Linearity		-1.5%		1.5%	--	Note 1
Response Time				30	ms	
Insulation Resistance		20			MΩ	DC 25V

Note 1: Measurement condition of Linearity: difference between actual voltage & theoretical voltage is an error at any points. Linearity is the value max. error voltage divided by voltage difference on active area.

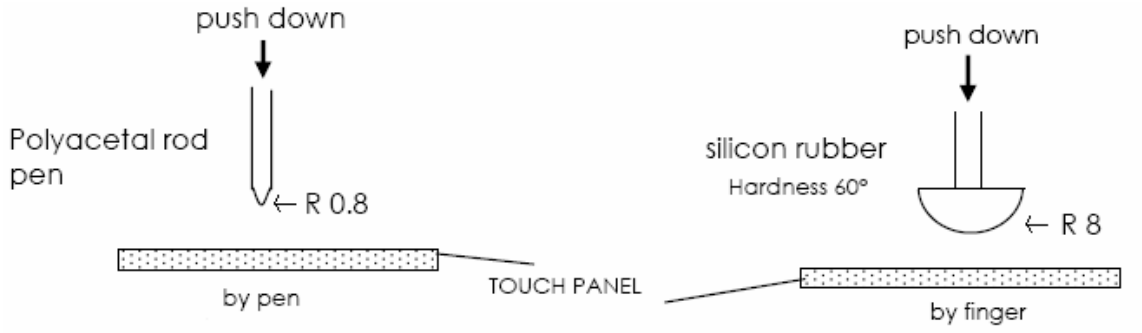


3. Mechanical Characteristics

Item	Min.	Max.	Unit	Remark
Hardness of Surface	3	--	H	JIS K-5600
Operation Force (Pen or Finger)	--	80	gf	Note 1, 2

Note 1: Within "active area", but not near the active area boundary and on the dot-spacer.

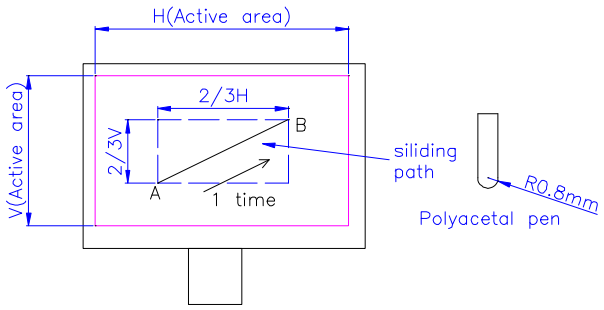
Note 2: Operation force measurement is under test condition as figure below.



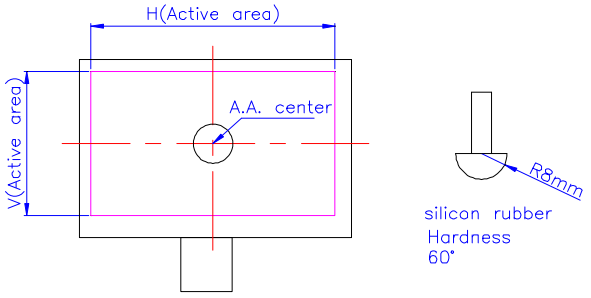
4. Life Test Condition

Item	Min.	Max.	Unit	Remark
Notes Life	10^5	--	lines	Note 1, 2
Input Life	10^6	--	times	Note 1, 3

Note 1: Notes Life test condition (by pen): slide on central 2/3 of active area and use R 0.8mm polyacecal pen, input force : 250gf, frequency : 60mm/sec. Sliding from A to B complete 1 time. shown as figure.



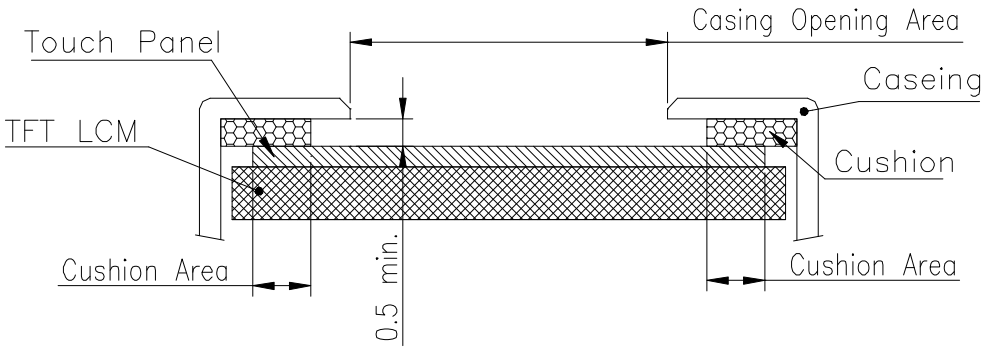
Note 2: Input Life test condition (by finger): test position on active area center and use R8.0mm silicon rubber (hardness 60˚), test force: 250gf, frequency : 2times/sec. shown as figure.



5. Attention

Please pay attention for below matters at mounting design of touch panel of LCD module.

1) Do not design casing opening area pressing the active area to prevent from miss input. Suggest casing opening area shown as mechanical drawing. Suggest the gap between caseing and touch panel surface at least 0.5mm to avoid miss input.
2) Cushion area must not contact with active area. Suggest cushion area shown as mechanical drawing.
3) Use elastic or non-conductive material to enclosure touch panel.
4) Do not bond film of touch panel with casing.
5) The touch panel edge is conductive. Do not touch it with any conductive part after mounting.



6) If user wants to cleaning touch panel by air gun, pressure 2kg/cm^2 below is suggested. Not to blow glass from FPC site to prevent FPC peeled off.
7) Do not put a heavy shock or stress on touch panel and film surface. Ex. Don't lift the panel by film face with vacuum.
8) Do not lift LCD module by FPC.
9) Please use dry cloth or soft cloth with neutral detergent (after wring dry) or one with ethanol at cleaning. Do not use any organic solvent, acid or alkali liquor.
10) Do not pile touch panel. Do not put heavy goods on touch panel.

F. Reliability Test Items

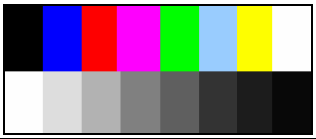
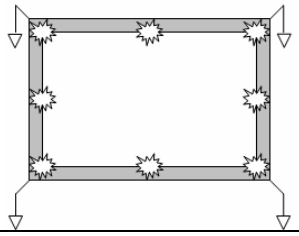
No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 80°C 240Hrs	
2	Low Temperature Storage	Ta= -30°C 240Hrs	
3	High Ttemperature Operation	Tp= 70°C 240Hrs	
4	Low Temperature Operation	Ta= -20°C 240Hrs	
5	High Temperature & High Humidity	Tp= 60°C, 90% RH 240Hrs	Operation
6	Heat Shock	-30 ~ 80℃, 30 cycles	Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B	Note 4
8	Image Sticking	25℃, 4hrs	Note 5
9	Vibration	Frequency range : 8~33.3Hz Stoke : 1.3mm Sweep : 2.9G ,33.3~400Hz 2 hours for each direction of X,Y,Z 4 hours for Y direction	Non-operation JIS C7021, A-10 condition A : 15 minutes
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	
13	Pressure	5kg, 5sec	Note 6

Note 1: Ta: Ambient Temperature. Tp: Panel Surface Temperature

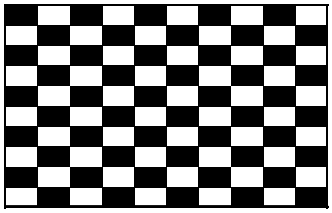
Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 3: All the cosmetic specification is judged before the reliability stress.

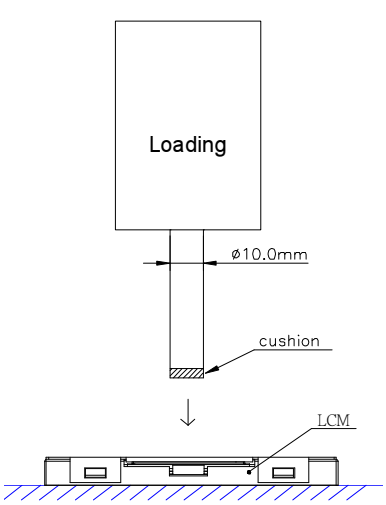
Note 4 : All test techniques follow IEC6100-4-2 standard.

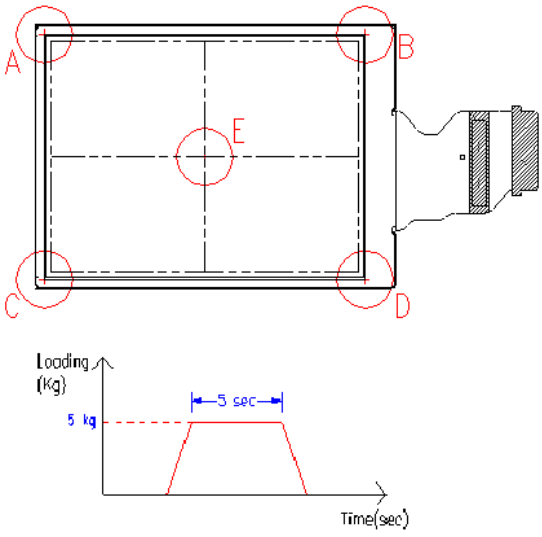
Test Condition		Note
Pattern		
Procedure And Set-up	Contact Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point Air Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point 	
Criteria	B – Some performance degradation allowed. No data lost. Self-recoverable hardware failure.	
Others	1. Gun to Panel Distance 2. No SPI command, keep default register settings.	

Note 5: Operate with chess board pattern as figure and lasting time and temperature as the conditions. Then judge with 50% gray level, the mura is less than JND 2.8



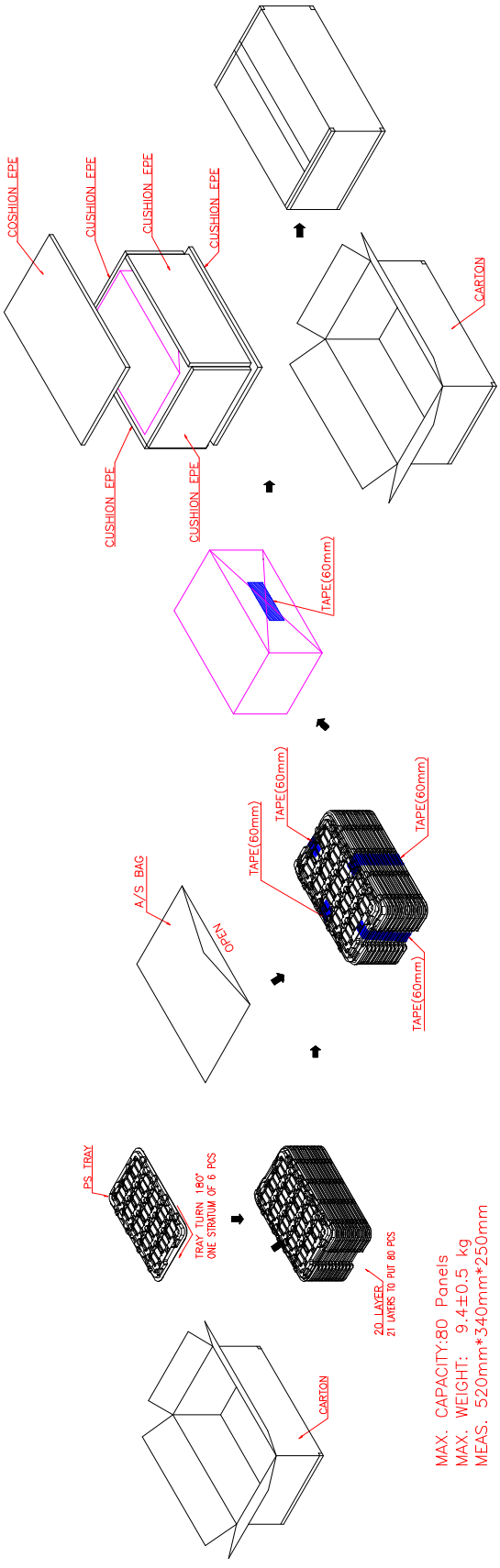
Note 6: The panel is tested as figure. The jig is ϕ 10 mm made by Cu with rubber and the loading speed is 3mm/min on position A~E. After the condition, no glass crack will be found and panel function check is OK.(no guarantee LC mura、LC bubble)





G. Packing and Marking

1. Packing Form



H. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.

I. Ordering Information:

Part Number	Description
97.05A10.200	Touch panel verdor: SWENC
97.05A10.201	Touch panelvendor: EELY