Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications
( ) Final Specifications

Module	**10.1”(10.1”) WUXGA 16:10 Color TFT-LCD with LED Backlight design**
Model Name	B101UAN01.1 (H/W:0A)
Note ( )	***LED Backlight without driving circuit design***

Customer	**Date**
Checked & Approved by	**Date**
Note: This Specification is subject to change without notice.	

Approved by	**Date**
Trista Jiang	10/12/2012
Prepared by	**Date**
Pei-Ching Huang	10/12/2012
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Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.0 2011/09/26	All	First Edition		
0.1 2011/11/24	8	Color / Chromaticity Coodinates -> TBD	CIE 1931: Rx 0.566 0.596 0.626; Ry 0.316 0.346 0.376; Gx 0.297 0.327 0.357; Gy 0.558 0.588 0.618; Bx 0.123 0.153 0.183; By 0.098 0.128 0.158	
	15	VDD power -> TBD	VDD power -> 1.0 W	
	15	IDD current -> TBD	IDD current -> 334 W	
	16	DCR Mode Duty Index -> TBD	DCR Mode Duty Index -> min:70%,max:100%	
	16	L0 Gray level -> TBD	L0 Gray level -> 0.95 W (typ)	
	16	L63 Gray level -> TBD	L63 Gray level -> 0.95 W (typ)	
	23	Clock frequency -> 160 MHz max	Clock frequency -> 163 MHz max	
0.2 2012/10/12			Updated model names	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B101UAN01.1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 WUXGA, 1,920(H) x1,200(V) screen and 2.56M colors (RGB 6-bits) without LED backlight driving circuit. All input signals are LVDS interface compatible.

B101UAN01.1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	256.42			
Active Area	[mm]	216.81 X 135.50 typ			
Pixels H x V		1,920x3(RGB) x 1,200			
Pixel Pitch	[mm]	0.113x 0.113			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		ASVA, Normally Black			
White Luminance (ILED=20mA) (Note: ILED is LED current)	[cd/m^2]	Base Panel 400 typ. (5 points average) 340 min. (5 points average)			
Luminance Uniformity		1.33 max. (5 points)			
Contrast Ratio		800 typ			
Response Time	[ms]	25 typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption (Column Inversion)	[Watt]	3.59W max.			
Weight	[Grams]	160g max (w/front bezel)			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	228.30	228.60	228.90
		Width	148.90	149.20	149.50

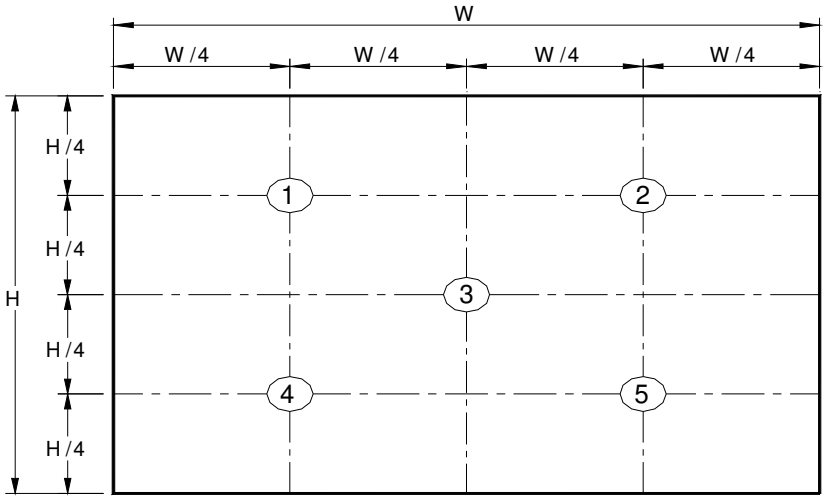
		Thickness	TBD	TBD	2.65 (Panel Side) 4.65 (PCBA Side)
Electrical Interface		2 channel LVDS			
Glass Thickness	[mm]	0.25			
Surface Treatment		Glare, Hardness 3H,			
Support Color		2.56M colors (RGB 6-bits)			
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 -20 to +60 -30 to +70			
RoHS Compliance		RoHS Compliance			

2.3 Optical Characteristics

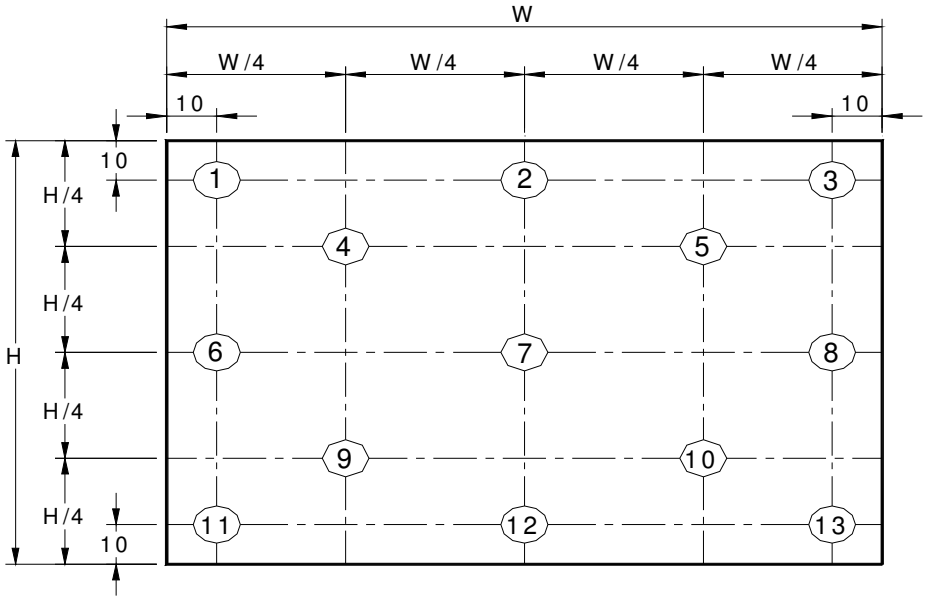
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=20mA			5 points average	340	400	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10 (Left)	-	85	-	degree	4, 9
		θ_L		-	85	-		
		ψ_H	Vertical (Upper) CR = 10 (Lower)	-	85	-		
		ψ_L		-	85	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.33		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.53		2, 3, 4
Contrast Ratio		CR		-	800	-		4, 6
Cross talk		%				-		4, 7
Response Time		T_r	Rising	-	-	-	msec	4, 8
		T_f	Falling	-	-	-		
		T_{RT}	Rising + Falling	-	25	35		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.566	0.596	0.626		4
		Ry		0.316	0.346	0.376		
	Green	Gx		0.297	0.327	0.357		
		Gy		0.558	0.588	0.618		
	Blue	Bx		0.123	0.153	0.183		
		By		0.098	0.128	0.158		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	52	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



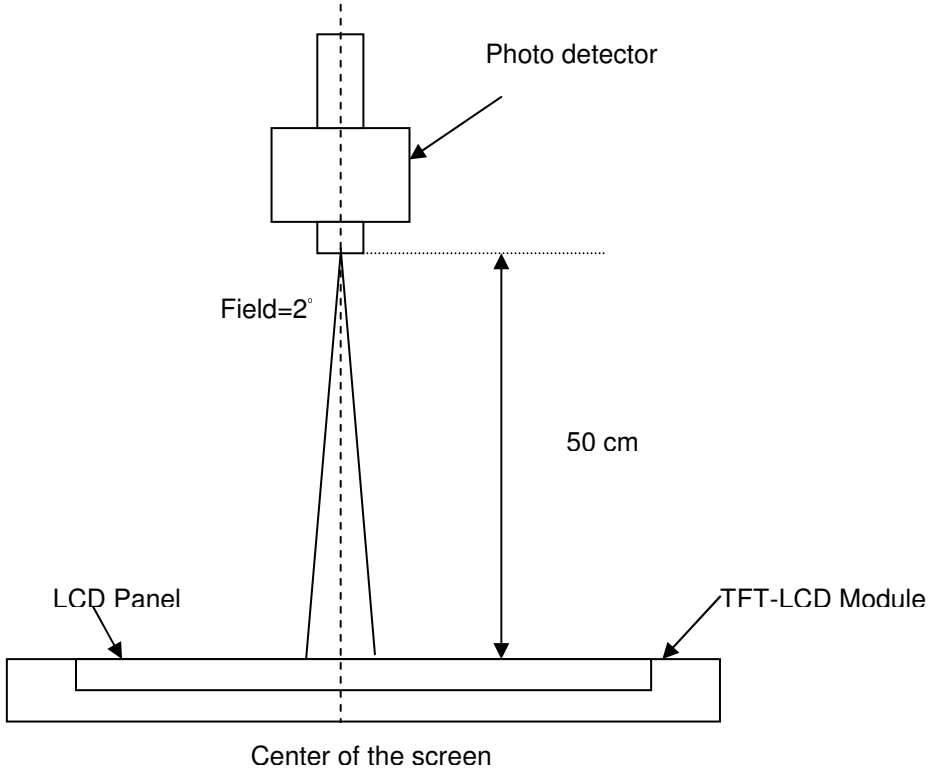
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points， Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

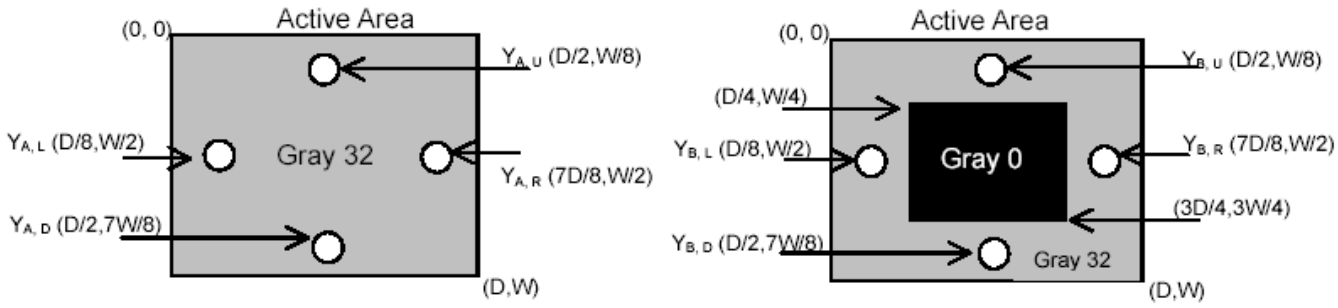
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100\ (\%)$

Where

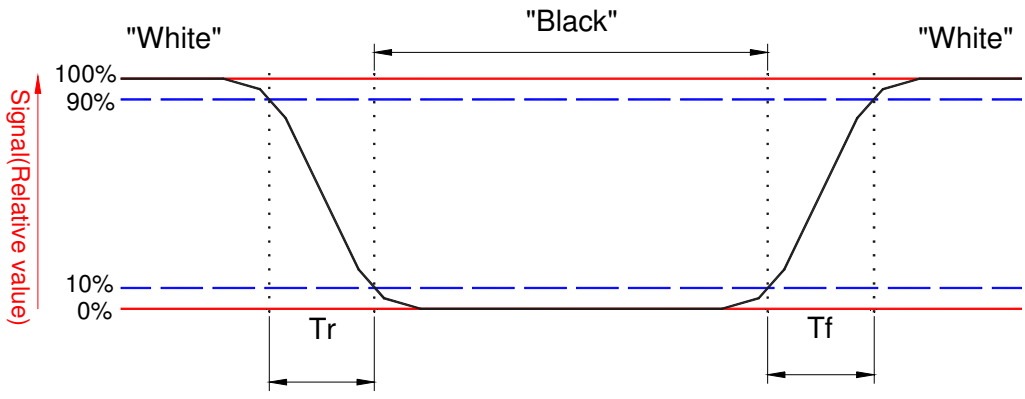
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



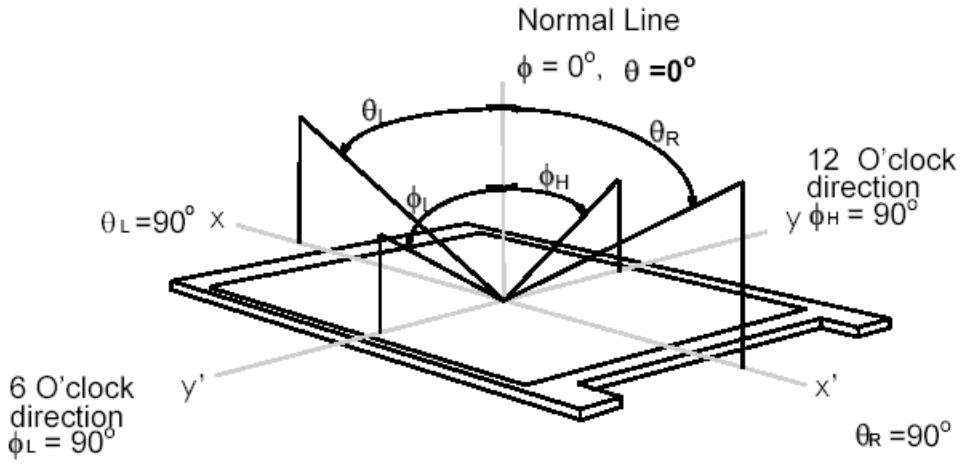
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



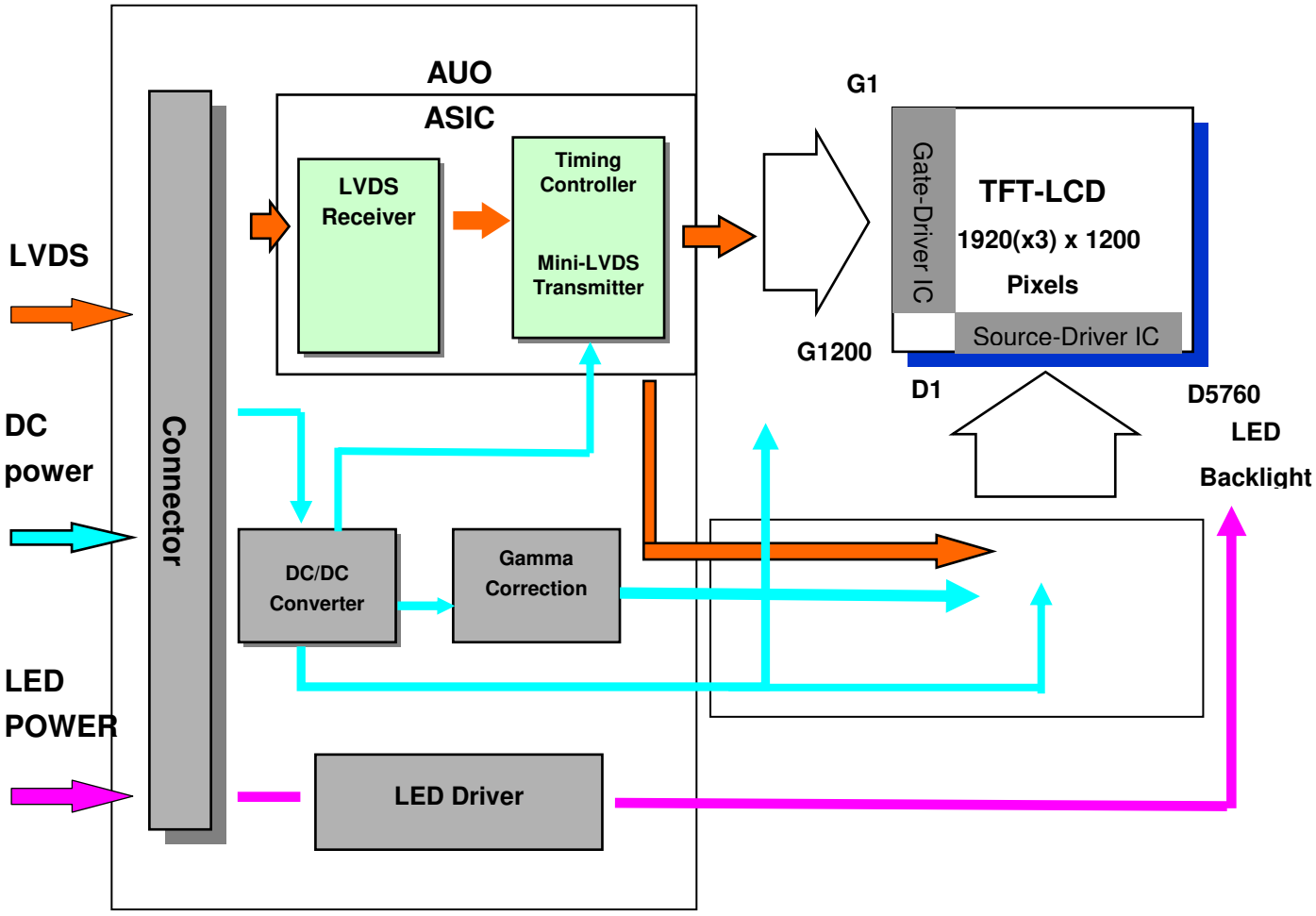
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 40 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	-20	+60	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-30	+70	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

[TBD]

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

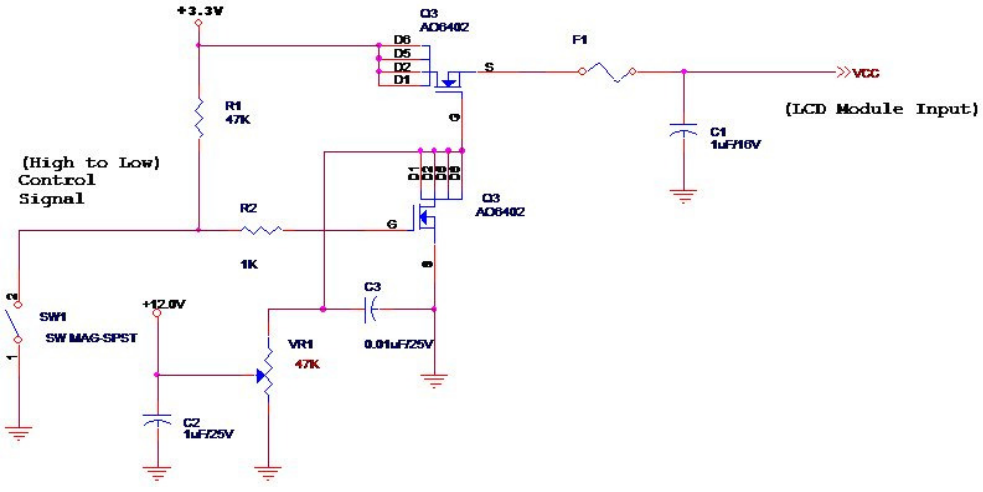
Input power specifications are as follows;

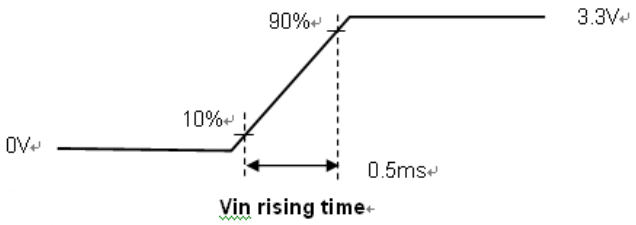
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.0	[Watt]	Note 1
IDD	IDD Current	-	-	334	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：White Pattern at 3.3V driving voltage. (P_{max}=$V_{3.3}$ x I_{white}) column inversion.

Note 2：Measure Condition





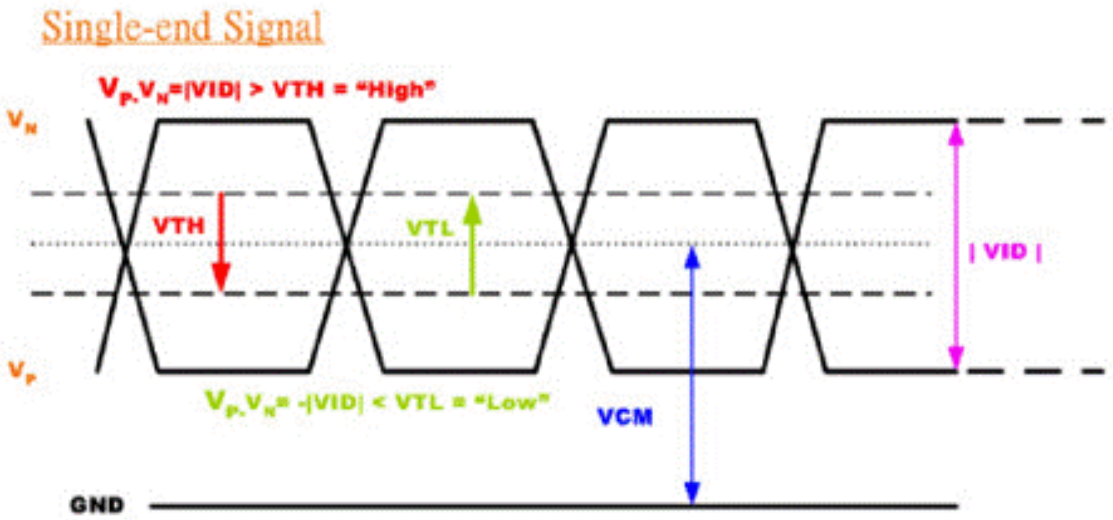
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{TH}	Differential Input High Threshold (Vcm=+1.2V)	---	100	[mV]
V_{TL}	Differential Input Low Threshold (Vcm=+1.2V)	-100	----	[mV]
$\|V_{ID}\|$	Differential Input Voltage	100	600	[mV]
V_{CM}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.1.3 Dynamic contrast ratio Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
Dynamic contrast ratio(DCR) Input High Level	DCR_EN	2.5	-	5.5	[Volt]	Define as Connector Interface (Ta=25℃)
Dynamic contrast ratio(DCR) Input Low Level		-	-	0.8	[Volt]	
DCR Mode Duty Index	Duty	70	-	100	%	Note 1
L0 Gray level	Power	-	0.95	-	Watt	Note 2
L63 Gray level	Power	-	0.95	-	Watt	

Note 1: The minimums dynamic contrast ratio is setting at darkness, and a maximum is setting at brightness.

Note 2: The power saving capability refer to original Backlight power consumption (P)

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.59	[Watt]	(Ta=25℃), Note 1 **Vin ≥ 3.2V,Note 2**

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: Vin means LED input voltage. Measured the voltage on LVDS connector. 3.2V ≤ Vin ≥ 12V.

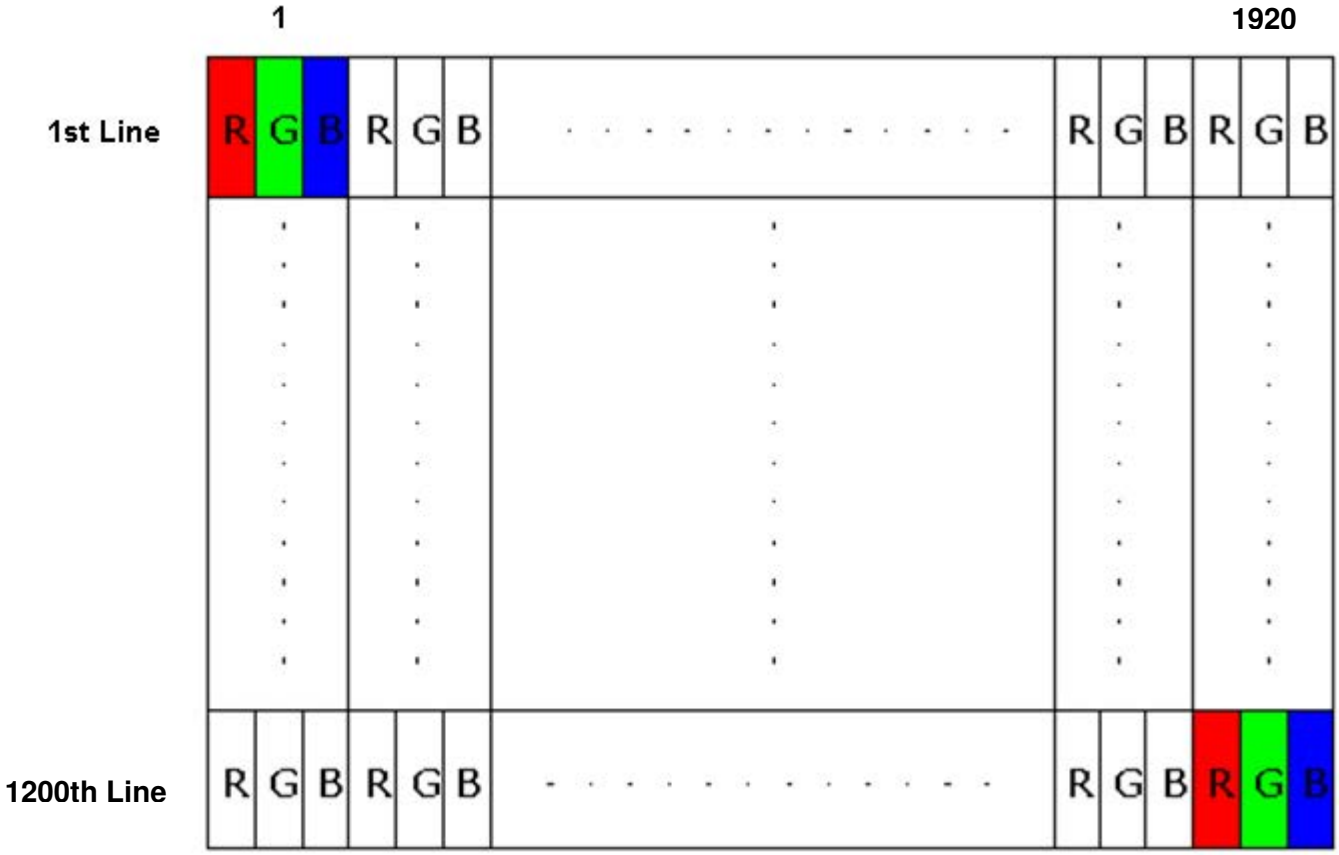
5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	3.2	-	12	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	200	-	20K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

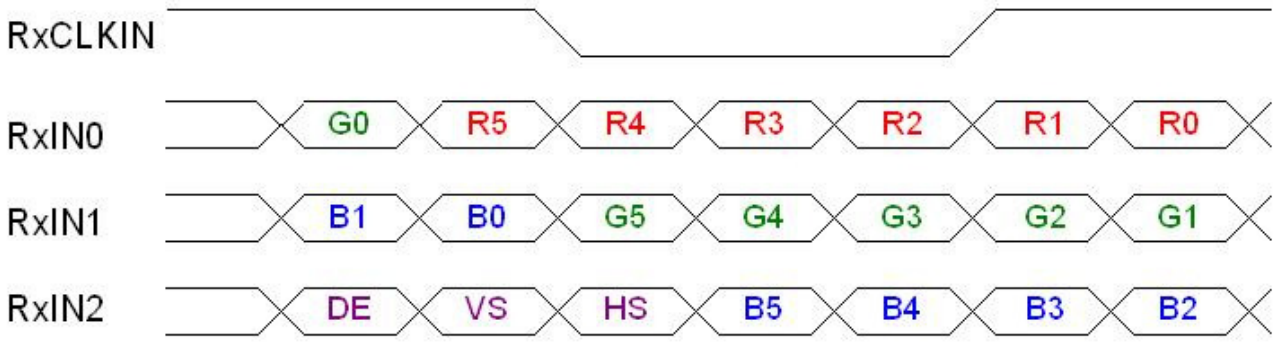
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format（2 Port）



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 LVDS Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

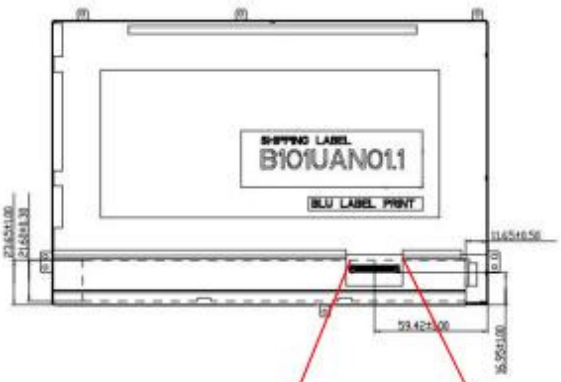
Connector Name / Designation	For Signal Connector
Manufacturer	IPEX
Type / Part Number	IPEX_20455-040E-12R
Mating Housing/Part Number	IPEX 20453-040T-11or Compatible

6.3.2 LVDS Pin Assignment

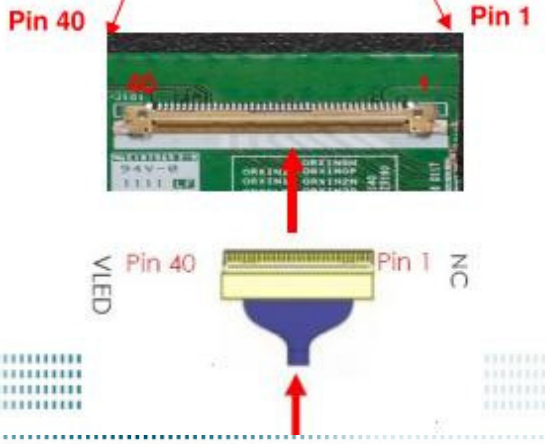
LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	NC	No connection
2	VDD	Power Supply +3.3V
3	VDD	Power Supply +3.3V
4	VDDEDID	EDID +3.3V Power
5	AGING	AGING Mode Enable
6	CLK_EDID	EDID Clock Input
7	DATA_EDID	EDID Data Input
8	RxOIN0-	Negative LVDS Differential Data INPUT for odd pixel(R0-R5, G0)
9	RxOIN0+	Positive LVDS Differential Data INPUT for odd pixel(R0-R5, G0)
10	GND	Ground
11	RxOIN1-	Negative LVDS Differential Data INPUT for odd pixel(G1-G5, B0-B1)
12	RxOIN1+	Positive LVDS Differential Data INPUT for odd pixel(G1-G5, B0-B1)
13	GND	Ground
14	RxOIN2-	Negative LVDS Differential Data INPUT for odd pixel(B2-B5, DE)
15	RxOIN2+	Positive LVDS Differential Data INPUT for odd pixel(B2-B5, DE)
16	GND	Ground
17	RxOCLKIN-	Negative LVDS Differential Clock INPUT for odd pixel
18	RxOCLKIN+	Positive LVDS Differential Clock INPUT for odd pixel
19	IMG_EN	Color Engine Enable (Color Matrix)
20	RxEIN0-	Negative LVDS Differential Data INPUT for even pixel(R0-R5, G0)
21	RxEIN0+	Positive LVDS Differential Data INPUT for even pixel(R0-R5, G0)
22	GND	Ground

23	RxEIN1-	Negative LVDS Differential Data INPUT for even pixel(G1-G5, B0-B1)
24	RxEIN1+	Positive LVDS Differential Data INPUT for even pixel(G1-G5, B0-B1)
25	GND	Ground
26	RxEIN2-	Negative LVDS Differential Data INPUT for even pixel(B2-B5, DE)
27	RxEIN2+	Positive LVDS Differential Data INPUT for even pixel(B2-B5, DE)
28	GND	Ground
29	RxECLKIN-	Negative LVDS Differential Clock INPUT for even pixel
30	RxECLKIN+	Positive LVDS Differential Clock INPUT for even pixel
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No connection
35	S_PWMIN	System PWM Logic input level
36	LED_EN	LED enable input level
37	DCR_EN	DCR Function Enable
38	VLED	LED Power Supply
39	VLED	LED Power Supply
40	VLED	LED Power Supply



Note1: Input signals shall be low or High-impedance state when VDD is off.



6.4 LVDS Interface Timing

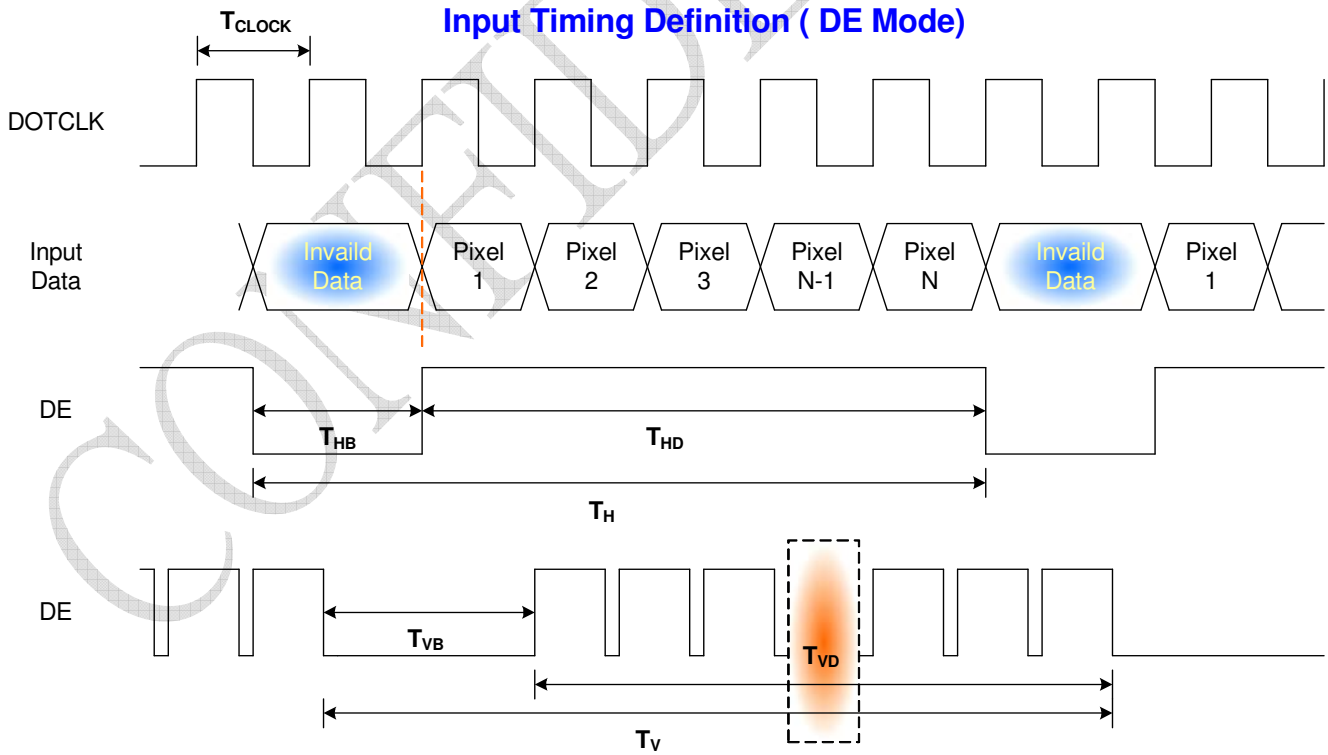
6.4.1 Timing Characteristics

Basically, interface timings should match the 1920x1200 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T_{Clock}	140	150	163	MHz
Vertical Section	Period	T_V	1208	1210	2047	T_{Line}
	Active	T_{VD}	1200			
	Blanking	T_{VB}	8	10	847	
Horizontal Section	Period	T_H	1000	1033	2047	T_{Clock}
	Active	T_{HD}	960			
	Blanking	T_{HB}	40	73	1087	

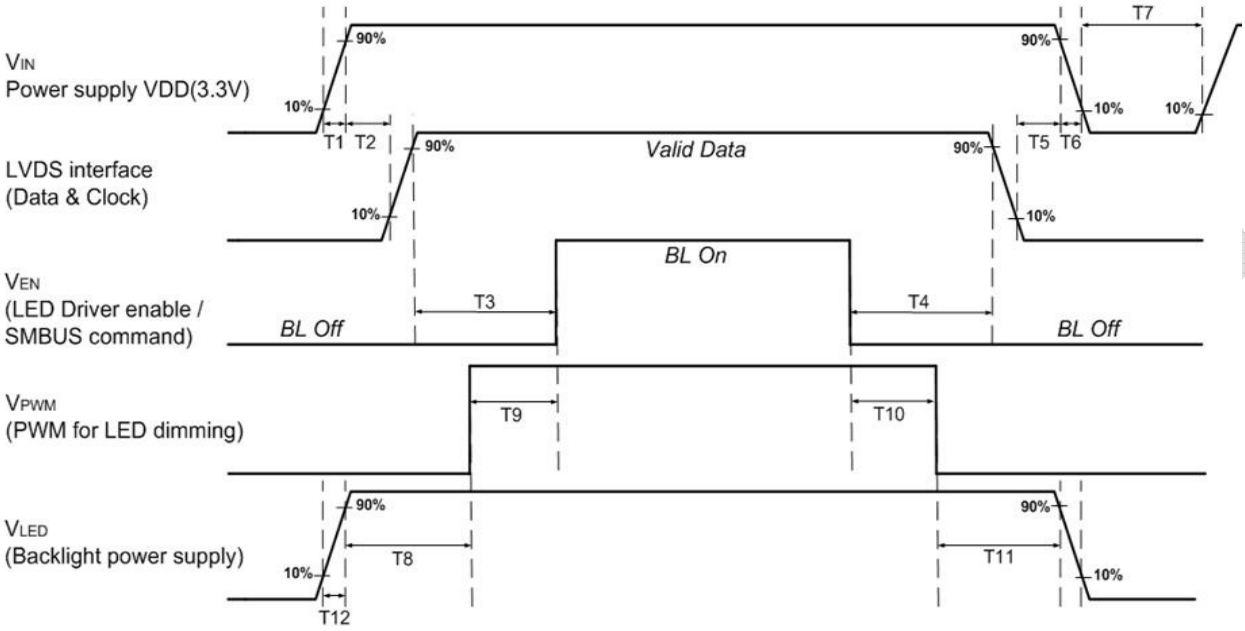
Note : DE mode only, **V blanking > 8, H blanking > 40**

6.4.2 Timing diagram

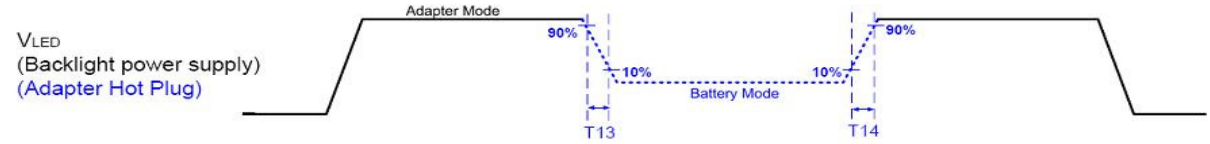


6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



Power Sequence Timing			
Parameter	Value		Units
	Min.	Max.	
T1	0.5	10	ms
T2	0	50	
T3	200	---	
T4	200	---	
T5	0	50	
T6	0	10	
T7	500	---	
T8	10	---	
T9	10	---	
T10	10	---	
T11	10	---	
T12	0.5	10	
T13	1*	---	
T14	1*	---	

Seamless change: T13/T14 = 5xT_{PWM}*
*T_{PWM}= 1/PWM Frequency

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 240h	
High Temperature Operation	Ta= 60℃, Dry, 240h	
Low Temperature Operation	Ta=-20℃, 240h	
High Temperature Storage	Ta= 70℃, 240h	
Low Temperature Storage	Ta= -20℃, 240h	
Thermal Shock Test	Ta=-30℃(30min) ~70℃(30min), 20cycles condition.	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

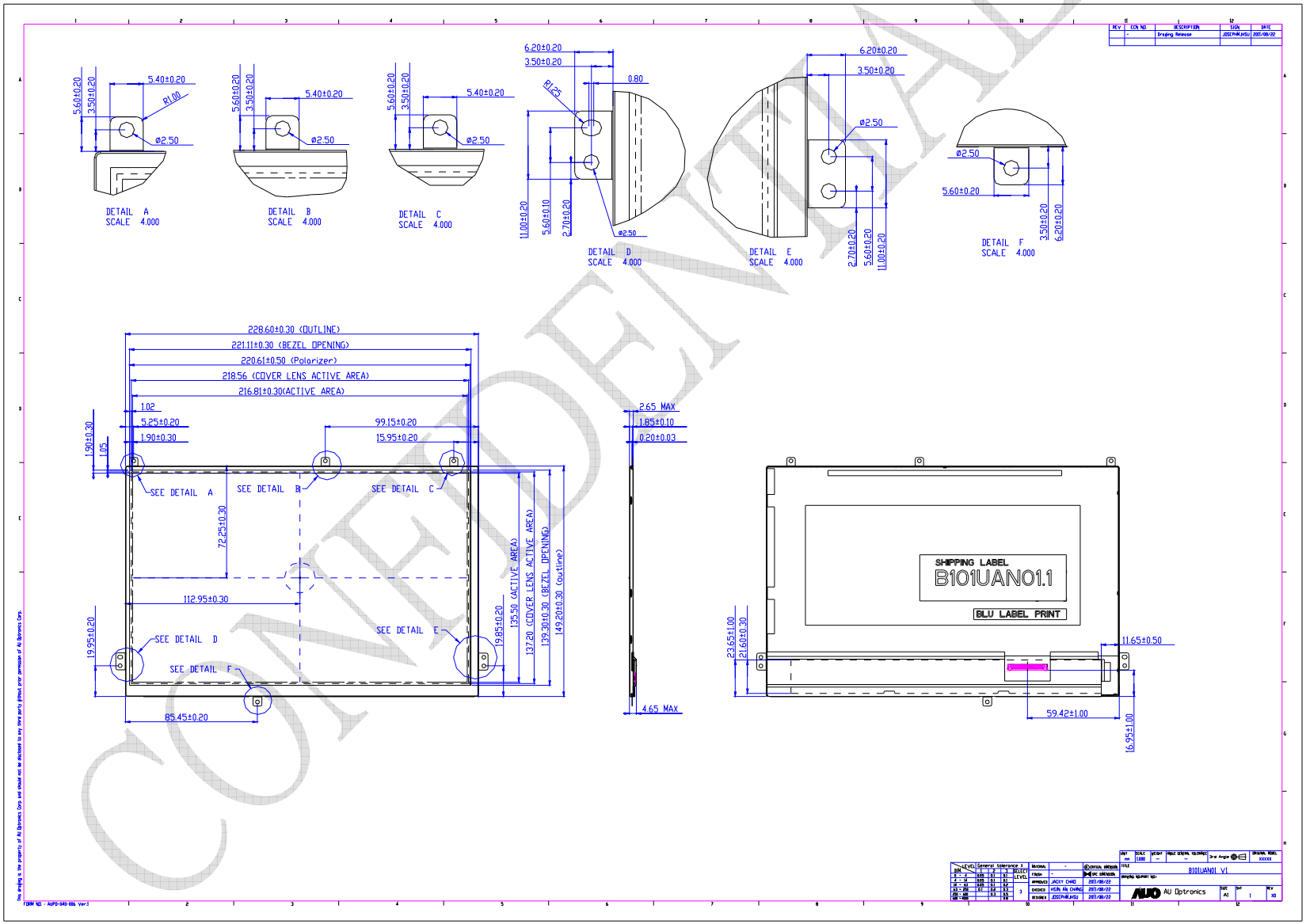
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

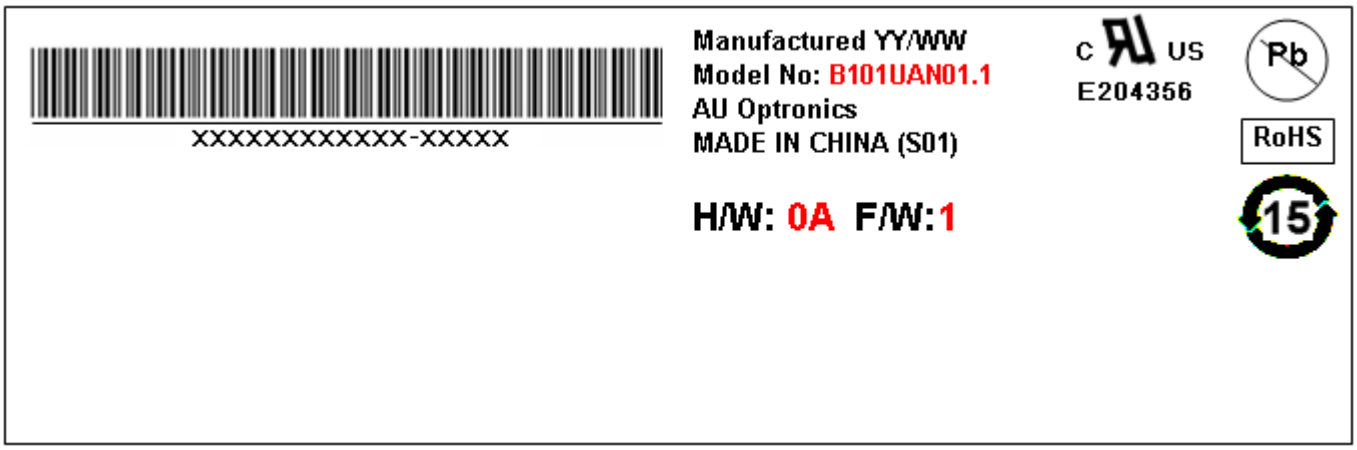
8.1 LCM Outline Dimension

Note: Prevention IC damage, IC positions not allowed any overlap over these areas.



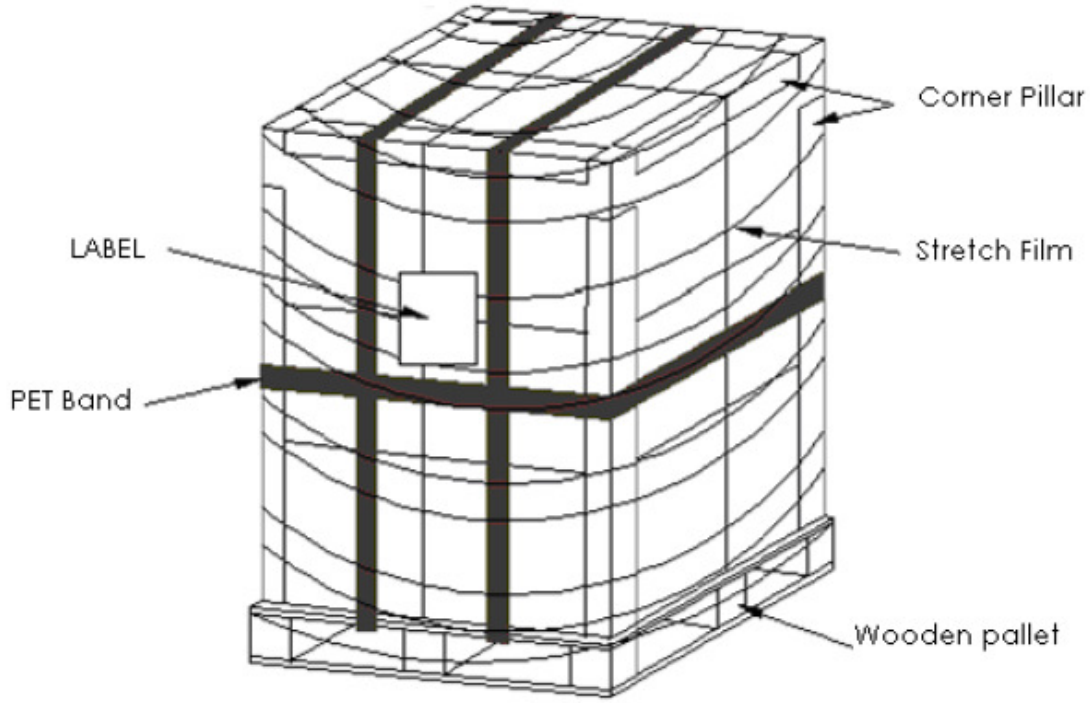
9. Shipping and Package

9.1 Shipping Label Format



9.2 Carton Label Format

9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

B101UAN01 1 EDID Code

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	D8	11011000	216	
0B	hex, LSB first	11	00010001	17	
0C	32-bit ser #	01	00000001	1	tting
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	15	00010101	21	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	90	10010000	144	
15	**Max H image size** *(rounded to cm)*	16	00010110	22	
16	**Max V image size** *(rounded to cm)*	0E	00001110	14	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	66	01100110	102	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	F5	11110101	245	
1B	Red x **(Upper 8 bits)**	A2	10100010	162	
1C	Red y/ highER 8 bits	55	01010101	85	
1D	Green x	4F	01001111	79	
1E	Green y	9A	10011010	154	
1F	Blue x	24	00100100	36	
20	Blue y	10	00010000	16	
21	White x	4F	01001111	79	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	

2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	98	10011000	152	
37	Pixel Clock/10000 USB	3A	00111010	58	
38	Horz active **Lower 8bits**	80	10000000	128	
39	Horz blanking **Lower 8bits**	92	10010010	146	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	70	01110000	112	
3B	Vertical Active **Lower 8bits**	B0	10110000	176	
3C	Vertical Blanking **Lower 8bits**	0A	00001010	10	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40	01000000	64	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	35	00110101	53	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	D8	11011000	216	
43	Vertical Image Size **Lower 8bits**	88	10001000	136	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	00	00000000	0	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Detailed timing/monitor	10	00010000	16	
49	descriptor #2	27	00100111	39	
4A		80	10000000	128	
4B		92	10010010	146	
4C		70	01110000	112	
4D		B0	10110000	176	
4E		0A	00001010	10	
4F		40	01000000	64	
50		30	00110000	48	
51		20	00100000	32	
52		35	00110101	53	
53		00	00000000	0	
54		D8	11011000	216	
55		88	10001000	136	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		18	00011000	24	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	

5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	30	00110000	48	0
74	Manufacture P/N	31	00110001	49	1
75	Manufacture P/N	55	01010101	85	U
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	4E	01001110	78	N
78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	31	00110001	49	1
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	31	00110001	49	1
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	55	01010101	85	