

Issued Date: Aug. 30, 2006 Model No.: M201P1-L03

Approval

TFT LCD Approval Specification

MODEL NO.: M201P1-L03

Customer:	
Approved by:	
Note:	





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REVISION HISTORY

Version	Date	Section	Description
Ver 2.0	Aug. 30, 06'	All	M201P1-L03 Specifications was first issued.

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

M201P1-L03 is an 20.1" TFT Liquid Crystal Display module with 4 CCFL Backlight unit and 30 pins 2ch-LVDS interface. This module supports 1400 x 1050 SXGA+ mode and can display 16.7M colors. The inverter module for Backlight is not built in.

1.2 FEATURES

- Wide viewing angle.
- High contrast ratio
- Super fast response time
- SXGA+ (1400 x 1050 pixels) resolution
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- RoHS Compliance

1.3 APPLICATION

- TFT LCD Monitor

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	408.24 (H) x 306.18 (V) (20.1" diagonal)	mm	(1)
Bezel Opening Area	413.0(H) x 311.0(V)	mm	(1)
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1400 x R.G.B. x 1050	pixel	-
Pixel Pitch	0.2916 (H) x 0.2916 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Transmissive Mode	Normally White	-	-
Surface Treatment	Anti - glare , Haze 25 , 3H	-	-

1.5 MECHANICAL SPECIFICATIONS

Ite	em	Min.	Тур.	Max.	Unit	Note
	Horizontal(H)	431.5	432.0	432.5	mm	
Module Size	Vertical(V)	331	331.5	332	mm	(1)
	Depth(D)	16.0	16.5	17.0	mm	
We	eight	-	-	2900	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

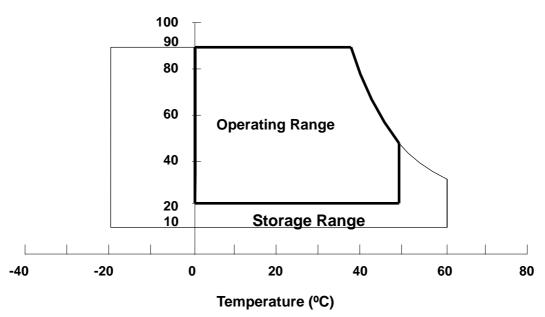
Item	Symbol	Va	Unit	Note	
item	Symbol	Min.	Max.	Offic	Note
Storage Temperature	T _{ST}	-20	60	٥C	(1)
Operating Ambient Temperature	T _{OP}	0	50	٥C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

- (a) 90 %RH Max. (Ta 40 °C).
- (b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).
- (c) No condensation.

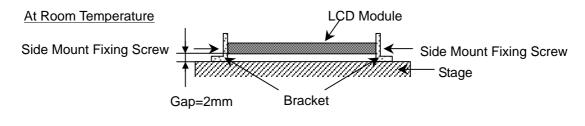
Note (2) The temperature of panel display surface area should be 0 °C Min. and 60 °C Max.

Relative Humidity (%RH)



- Note (3) 11ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.
- Note (4) 10 ~ 300 Hz, 10min/cycle, 3 cycles each X, Y, Z.
- Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:





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2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Itam	Cumbal	Value		Linit	Note
Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	Vcc	-0.3	+6.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	4.3	V	(1)

2.2.2 BACKLIGHT UNIT

Item	Symbol	Va	lue	Unit	Note
item	Symbol	Min.	Max.	Ullit	Note
Lamp Voltage	V_L		2.5K	V_{RMS}	(1), (2)
Lamp Current	ΙL	2.0	7.5	mA_RMS	(1) (2)
Lamp Frequency	FL	45	80	KHz	(1), (2)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

CHIMEI OPTOELECTRONICS CORP.

3. ELECTRICAL CHARACTERISTICS

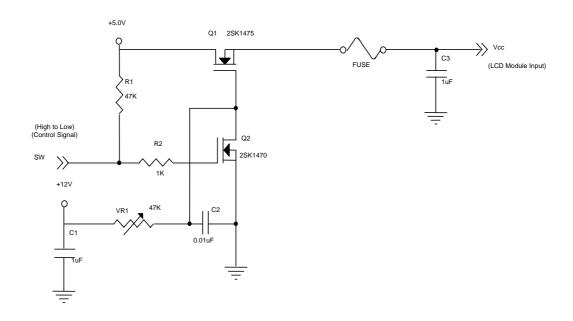
3.1 TFT LCD MODULE

Ta = 25 ± 2 °C

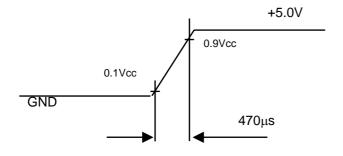
Parameter		Symbol		Value	Unit	Note	
Farame	lei	Symbol	Min.	Тур.	Max.	Offic	Note
Power Supply Voltage		Vcc	4.5	5.0	5.5	V	-
Ripple Voltage		V_{RP}	-	-	100	mV	-
Rush Current		I _{RUSH}	-	-	3.8	Α	(2)
	White		-	390	550	mA	(3)a
Power Supply Current	Black	lcc	-	800	1100	mA	(3)b
r ower Supply Current	$f_V = 75Hz$, Vcc=4.5V	100	-	-	1500	mA	(4)
LVDS differential input voltage		Vid	-100	-	+100	mV	
LVDS common input voltage		Vic	-	1.2	-	V	
Logic "L" input voltage		Vil	-	-	0.8	V	

Note (1) The module is recommended to operate within specification ranges listed above for normal function.

Note (2) Measurement Conditions:



Vcc rising time is 470µs

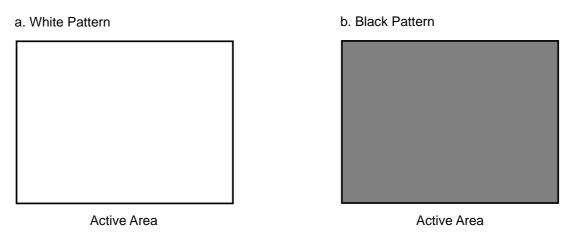




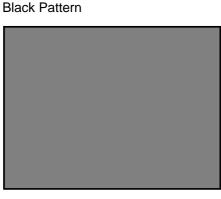
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Note (3) The specified power supply current is under the conditions at Vcc = 5.0 V, $Ta = 25 \pm 2 \, ^{\circ}\text{C}$, $f_v = 60 \, \text{Hz}$, whereas a power dissipation check pattern below is displayed.



Note (4) The specified power supply current is under the conditions at Vcc = 4.5 V, $Ta = 25 \pm 2 \,^{\circ}\text{C}$, $f_v = 75 \,^{\circ}\text{Hz}$, whereas a power dissipation check pattern (Black Pattern) below is displayed.





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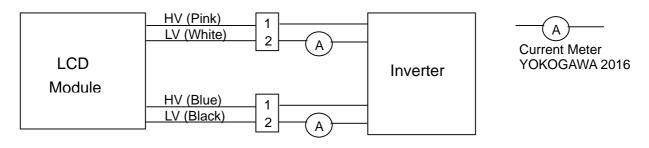
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3.2 BACKLIGHT UNIT

Ta = 25 ± 2 °C

Parameter	Symbol		Value	Unit	Note	
raiametei	Syllibol	Min.	Тур.	Max.	Offic	NOIG
Lamp Input Voltage	V_L	697	775	835	V_{RMS}	$(I_L = 7.0 \text{ mA})$
Lamp Current	ΙL	2.0	7.0	7.5	mA_{RMS}	(1)
Lower Turn On Valtage	Vs			1500(25)	V_{RMS}	(2)
Lamp Turn On Voltage				1710(0)	V_{RMS}	(2)
Operating Frequency	F_L	45		80	KHz	(3)
Lamp Life Time	L_BL	40000			Hrs	(5)
Power Consumption	P_L		21.73		W	$(4), (I_L = 7.0 \text{mA})$

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



- Note (2) The voltage that must be larger than Vs should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.
- Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.
- Note (4) $P_L = I_L \times V_L \times 4 \text{ CCFLs}$
- Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition $Ta = 25 \pm 2$ °C and $I_L = 7.0$ mArms until one of the following events occurs:
 - (a) When the brightness becomes or lower than 50% of its original value.
 - (b) When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)
- Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.



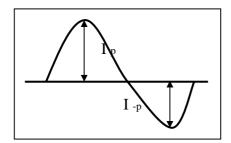
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The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Asymmetrical ratio is less than 10%) Please do not use the inverter which has asymmetrical voltage and asymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

- a. The asymmetry rate of the inverter waveform should be 10% below;
- b. The distortion rate of the waveform should be within $2 \pm 10\%$;
 - c. The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

$$|I_p - I_{-p}| / I_{rms} * 100\%$$

* Distortion rate

$$I_p (or I_{-p}) / I_{rms}$$

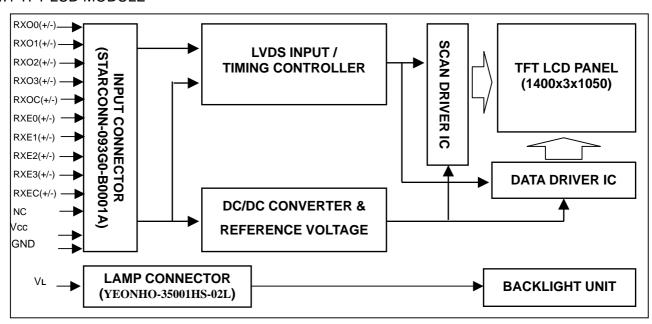


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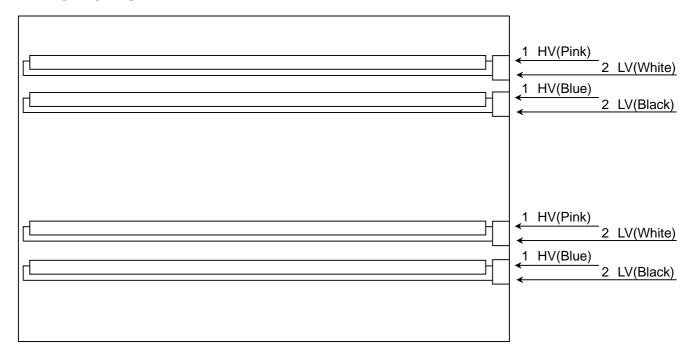
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4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT





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5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

2 RXO0+ Positive LVDS differential data input. Channel O0 (odd) 3 RXO1- Negative LVDS differential data input. Channel O1 (odd) 4 RXO1+ Positive LVDS differential data input. Channel O1 (odd) 5 RXO2- Negative LVDS differential data input. Channel O2 (odd) 6 RXO2+ Positive LVDS differential data input. Channel O2 (odd) 7 GND Ground 8 RXOC- Negative LVDS differential clock input. (odd) 9 RXOC+ Positive LVDS differential clock input. (odd) 10 RXO3- Negative LVDS differential data input. Channel O3 (odd) 11 RXO3+ Positive LVDS differential data input. Channel O3 (odd) 12 RXE0- Negative LVDS differential data input. Channel E0 (even) 13 RXE0+ Positive LVDS differential data input. Channel E0 (even) 14 GND Ground 15 RXE1- Negative LVDS differential data input. Channel E1 (even) 16 RXE1+ Positive LVDS differential data input. Channel E1 (even) 17 GND Ground 18 RXE2- Negative LVDS differential data input. Channel E2 (even) 19 RXE2+ Positive LVDS differential data input. Channel E2 (even) 20 RXEC- Negative LVDS differential data input. Channel E2 (even) 21 RXEC+ Positive LVDS differential clock input. (even) 22 RXE3- Negative LVDS differential clock input. (even) 23 RXE3+ Positive LVDS differential data input. Channel E3 (even) 24 GND Ground 25 NC Not connection (Should keep open). 26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open).	1	RXO0-	Negative LVDS differential data input. Channel CO (odd)
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14 GND Ground 15 RXE1- Negative LVDS differential data input. Channel E1 (even) 16 RXE1+ Positive LVDS differential data input. Channel E1 (even) 17 GND Ground 18 RXE2- Negative LVDS differential data input. Channel E2 (even) 19 RXE2+ Positive LVDS differential data input. Channel E2 (even) 20 RXEC- Negative LVDS differential clock input. (even) 21 RXEC+ Positive LVDS differential clock input. (even) 22 RXE3- Negative LVDS differential data input. Channel E3 (even) 23 RXE3+ Positive LVDS differential data input. Channel E3 (even) 24 GND Ground 25 NC Not connection (Should keep open). 26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	12	RXE0-	Negative LVDS differential data input. Channel E0 (even)
15 RXE1- Negative LVDS differential data input. Channel E1 (even) 16 RXE1+ Positive LVDS differential data input. Channel E1 (even) 17 GND Ground 18 RXE2- Negative LVDS differential data input. Channel E2 (even) 19 RXE2+ Positive LVDS differential data input. Channel E2 (even) 20 RXEC- Negative LVDS differential clock input. (even) 21 RXEC+ Positive LVDS differential clock input. (even) 22 RXE3- Negative LVDS differential data input. Channel E3 (even) 23 RXE3+ Positive LVDS differential data input. Channel E3 (even) 24 GND Ground 25 NC Not connection (Should keep open). 26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	13	RXE0+	Positive LVDS differential data input. Channel E0 (even)
16 RXE1+ Positive LVDS differential data input. Channel E1 (even) 17 GND Ground 18 RXE2- Negative LVDS differential data input. Channel E2 (even) 19 RXE2+ Positive LVDS differential data input. Channel E2 (even) 20 RXEC- Negative LVDS differential clock input. (even) 21 RXEC+ Positive LVDS differential clock input. (even) 22 RXE3- Negative LVDS differential data input. Channel E3 (even) 23 RXE3+ Positive LVDS differential data input. Channel E3 (even) 24 GND Ground 25 NC Not connection (Should keep open). 26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply	14	GND	Ground
17 GND Ground 18 RXE2- Negative LVDS differential data input. Channel E2 (even) 19 RXE2+ Positive LVDS differential data input. Channel E2 (even) 20 RXEC- Negative LVDS differential clock input. (even) 21 RXEC+ Positive LVDS differential clock input. (even) 22 RXE3- Negative LVDS differential data input. Channel E3 (even) 23 RXE3+ Positive LVDS differential data input. Channel E3 (even) 24 GND Ground 25 NC Not connection (Should keep open). 26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	15	RXE1-	Negative LVDS differential data input. Channel E1 (even)
18 RXE2- Negative LVDS differential data input. Channel E2 (even) 19 RXE2+ Positive LVDS differential data input. Channel E2 (even) 20 RXEC- Negative LVDS differential clock input. (even) 21 RXEC+ Positive LVDS differential clock input. (even) 22 RXE3- Negative LVDS differential data input. Channel E3 (even) 23 RXE3+ Positive LVDS differential data input. Channel E3 (even) 24 GND Ground 25 NC Not connection (Should keep open). 26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	16	RXE1+	Positive LVDS differential data input. Channel E1 (even)
19 RXE2+ Positive LVDS differential data input. Channel E2 (even) 20 RXEC- Negative LVDS differential clock input. (even) 21 RXEC+ Positive LVDS differential clock input. (even) 22 RXE3- Negative LVDS differential data input. Channel E3 (even) 23 RXE3+ Positive LVDS differential data input. Channel E3 (even) 24 GND Ground 25 NC Not connection (Should keep open). 26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	17	GND	Ground
20 RXEC- Negative LVDS differential clock input. (even) 21 RXEC+ Positive LVDS differential clock input. (even) 22 RXE3- Negative LVDS differential data input. Channel E3 (even) 23 RXE3+ Positive LVDS differential data input. Channel E3 (even) 24 GND Ground 25 NC Not connection (Should keep open). 26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	18	RXE2-	Negative LVDS differential data input. Channel E2 (even)
21 RXEC+ Positive LVDS differential clock input. (even) 22 RXE3- Negative LVDS differential data input. Channel E3 (even) 23 RXE3+ Positive LVDS differential data input. Channel E3 (even) 24 GND Ground 25 NC Not connection (Should keep open). 26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	19	RXE2+	Positive LVDS differential data input. Channel E2 (even)
22 RXE3- Negative LVDS differential data input. Channel E3 (even) 23 RXE3+ Positive LVDS differential data input. Channel E3 (even) 24 GND Ground 25 NC Not connection (Should keep open). 26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	20	RXEC-	Negative LVDS differential clock input. (even)
23 RXE3+ Positive LVDS differential data input. Channel E3 (even) 24 GND Ground 25 NC Not connection (Should keep open). 26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	21	RXEC+	Positive LVDS differential clock input. (even)
24 GND Ground 25 NC Not connection (Should keep open). 26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	22	RXE3-	Negative LVDS differential data input. Channel E3 (even)
25 NC Not connection (Should keep open). 26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	23	RXE3+	Positive LVDS differential data input. Channel E3 (even)
26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	24	GND	Ground
26 NC Not connection (Should keep open). 27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	25	NC	Not connection (Should keep open).
27 NC Not connection (Should keep open). 28 VCC +5.0V power supply 29 VCC +5.0V power supply	26	NC	
29 VCC +5.0V power supply	27	NC	
29 VCC +5.0V power supply	28	VCC	+5.0V power supply
1 117	29		
	30		+5.0V power supply

Note (1) Connector Part No.: 093G30-B0001A (Starconn).

Note (2) The first pixel is odd.

Note (3) Input signal of even and odd clock should be the same timing.



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LVDS interface receiver required input data mapping table								
LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
LVD3 Channel EU	Data order	EG0	ER5	ER4	ER3	ER2	ER1	ER0
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
LVD3 Channel E i	Data order	EB1	EB0	EG5	EG4	EG3	EG2	EG1
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
LVD3 Channel E2	Data order	DE	NA	NA	EB5	EB4	EB3	EB2
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
LVD3 Channel E3	Data order	NA	EB7	EB6	EG7	EG6	ER7	ER6
LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
LVDS Channel O0	Data order	OG0	OR5	OR4	OR3	OR2	OR1	OR0
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
LVD3 Channel O1	Data order	OB1	OB0	OG5	OG4	OG3	OG2	OG1
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
LVD3 Channel O2	Data order	DE	NA	NA	OB5	OB4	OB3	OB2
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
LVD3 Channel O3	Data order	NA	OB7	OB6	OG7	OG6	OR7	OR6



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5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Remark
1	HV	High Voltage	Pink
2	LV	Low Voltage	White
1	HV	High Voltage	Blue
2	LV	Low Voltage	Black

Note (1) Connector Part No.: BHSR-02VS-1 (JST) or equivalent

Note (2) User's connector Part No.:SM02B-BHSS-1-TB (JST) or equivalent

5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

		Data Signal																							
	Color				Re									reer							Blι				
	T	R7	R6	R5	R4	R3	R2	R1	R0	R7	R6	G5	G4	G3	G2	G1	G0	R7	R6	B5	B4	В3		B1	B0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
L . '	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Colors	,	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Scale	:		:	:	:	:	:	•	:	:	:		:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Red	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ļ	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	Ö	0	0	Ö	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	Ö	0	0	0	0	0
Gray	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	ı : l
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		:	ı :
Of	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
Green	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Gray	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Rluc	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

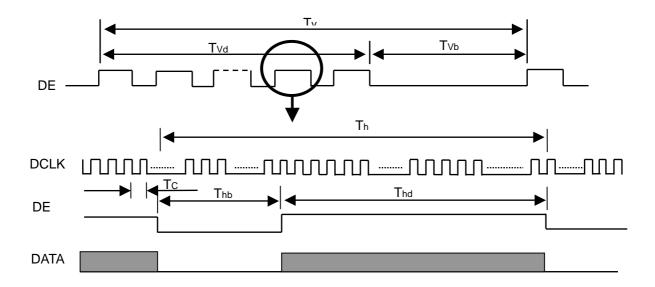
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

			_				
Signal	Item	Symbol	Min.	Тур.	Max.	Unit	Note
-	Frequency	Fc	-	54	67.5	MHz	-
LVDS Clock	Period	Tc	14.8	18.5	-	ns	
LVD3 Clock	High Time	Tch	-	4/7	-	Tc	-
	Low Time	Tcl	-	3/7	-	Tc	-
LVDS Data	Setup Time	Tlvs	600	-	-	ps	-
LVD3 Data	Hold Time	Tlvh	600	-	-	ps	-
	Frame Rate	Fr	56	60	75	Hz	Tv=Tvd+Tvb
Vertical Active Display Term	Total	Tv	1051	1066	1300	Th	-
Vertical Active Display Terri	Display	Tvd	1050	1050	1050	Th	-
	Blank	Tvb	Tv-Tvd	42	Tv-Tvd	Th	-
	Total	Th	740	844	980	Tc	Th=Thd+Thb
Horizontal Active Display Term	Display	Thd	700	700	700	Tc	-
	Blank	Thb	Th-Thd	144	Th-Thd	Tc	-

Note: Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

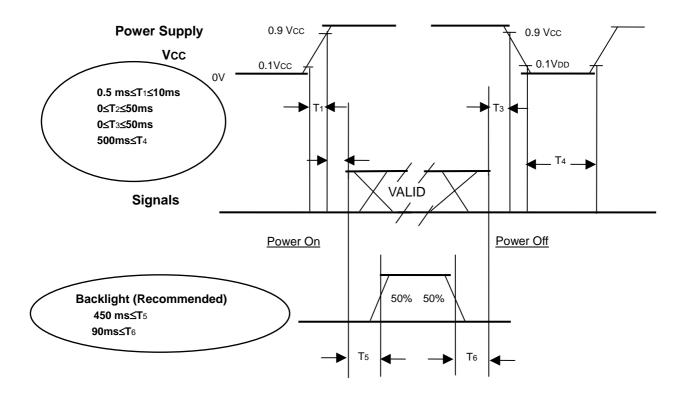
INPUT SIGNAL TIMING DIAGRAM





6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note.

- (1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.
- (2) Please apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation of the LCD turns off, the display may, instantly, function abnormally.
- (3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.
- (4) T4 should be measured after the module has been fully discharged between power of and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.



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7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit		
Ambient Temperature	Та	25±2	°C		
Ambient Humidity	Ha	50±10	%RH		
Supply Voltage	Vcc	5	V		
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"				
Lamp Current	IL	7.0	mA		
Inverter Operating Frequency	F_L	61	KHz		
Inverter	Sumida H05 5307				

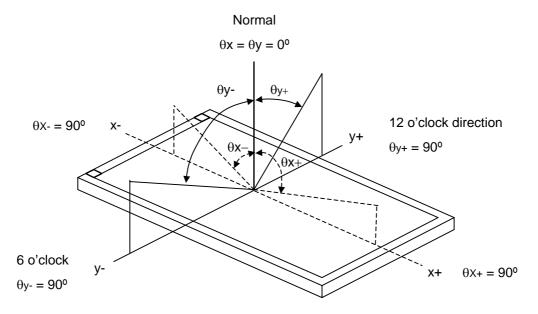
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

	Iter	n	Symbol	Condition	Min.	Тур.	Max.	Unit	Note	
		Red	Rx			0.640				
		Red	Ry			0.335				
		Green	Gx			0.289				
Color		Green	Gy		Тур –	0.597	Typ +		(1), (5)	
Chromatic	city	Blue	Bx	$\theta_x=0^\circ, \ \theta_Y=0^\circ$	0.03	0.154	0.03		(1), (3)	
		Dide	Ву	CS-1000T		0.081				
		White	Wx			0.313				
		VVIIILE	Wy			0.329				
Center Luminance of White		L _C		230	300		cd/m ²	(4), (5)		
Contrast Ratio		CR		700	1000		-	(2), (5)		
Response Time		T_R	0 -00 0 -00		1.3	6.3	ms	(2)		
			T_F	$\theta_x=0^\circ, \ \theta_Y=0^\circ$		3.7	8.7	ms	(3)	
White Var	iation		δW	$\theta_x=0^\circ$, $\theta_Y=0^\circ$		1.25	1.40	-	(5), (6)	
		Horizontal	θ_x +		75	85				
Viewing A	nale	Honzontai	θ _x -	CR 10	75	85		Deg.	(1), (5)	
violinig		Vertical	θ_{Y} +		70	80		Dog.	(1), (3)	
			θ _Y -		70	80				
	Lumir	nance uniformi Angular dep	•	CS-1000T			1.7		(7)	
Safety	Lumir	nance contrast Angular dep		R=G=B=255 Grayscale	0.8				(8)	
	Color	uniformity – Angular dep		R=G=B= 0 Grayscale			0.025		(7)(9)	



Note (1) Definition of Viewing Angle (θx , θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

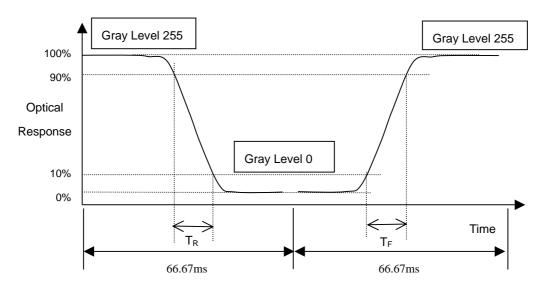
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR(7)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



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Note (4) Definition of Luminance of White (L_C):

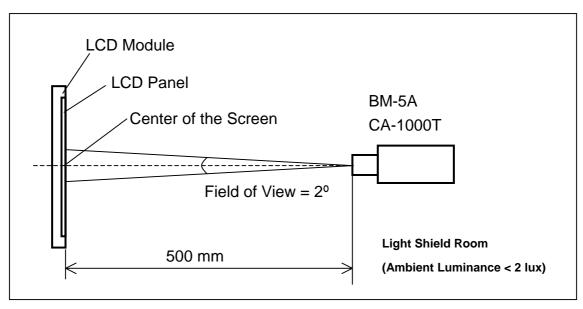
Measure the luminance of gray level 255 at center point

$$L_{C} = L(7)$$

L (x) is corresponding to the luminance of the point X at Figure in Note (6).

Note (5) Measurement Setup:

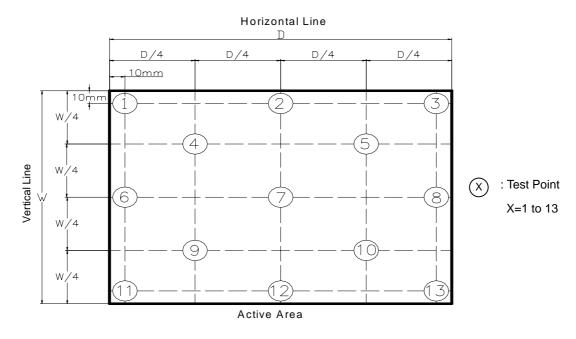
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 13 points

 $\delta W = Maximum [L (1), L (2)L (12), L (13)] / Minimum [L (1), L (2)L (12), L (13)]$



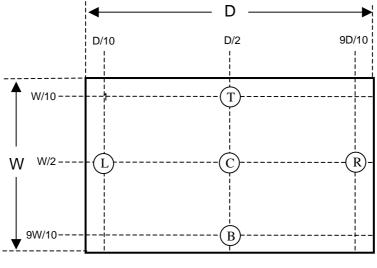
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Note (7) Definition of Luminance Uniformity – Angular dependent:

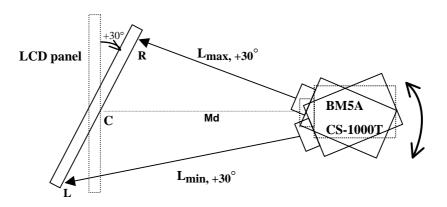


Active Area

Luminance is measured at the center measurement position "C" on the LCD panel. The optical axis of meter shall be aligned with the normal of the panel surface. The measuring distance between the meter and the surface of the panel is defined as:

Md (cm) = diagonal of the panel (cm) X 1.5 with minimum distance 50 cm.

a. Horizontal - mode

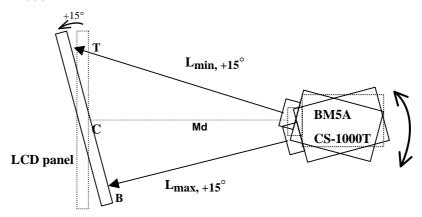


The LCD panel is then rotated to another azimuthal angle to -30°; and $L_{min, -30}$ ° and $L_{max, -30}$ ° are obtained by using the same procedure.

The Luminance Uniformity is calculated as follow:

$$((L_{max, +30}^{\circ}/L_{min, +30}^{\circ})+(L_{max, -30}^{\circ}/L_{min, -30}^{\circ}))/2.$$

b. Vertical - mode



The LCD panel is then rotated to another azimuthal angle to -15°; and $L_{min, -15}$ ° and $L_{max, -15}$ ° are obtained by using the same procedure.

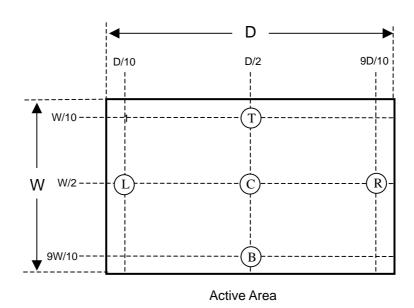
The Luminance Uniformity is calculated as follow:

$$L_{max, +15}^{\circ}/L_{min, +15}^{\circ}$$

$$L_{\text{max}, -15}^{\circ}/L_{\text{min}, -15}^{\circ}$$

The largest value shall be reported.

Note (8) Definition of Luminance Contrast - Angular dependent:



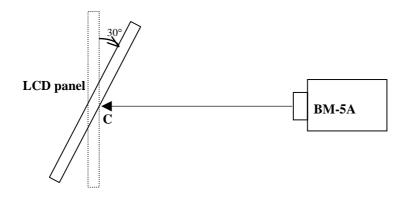
Luminance contrast is measured at the center point of the LCD panel "C" along with the normal of the display with the same distance described in Note 7. The display is then rotated around the vertical axis by changing its azimuthal axis to +30°; and this gives:



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 $L_{255~G.L., +30}^{\circ}$ and $L_{0~G.L., +30}^{\circ}$.



The LCD panel is then rotated to azimuthal angle to -30°; and $\rm L_{0~G~L.,~-30}^\circ$ and $\rm L_{63~G.L.,~-30}^\circ$ are obtained by using the same procedure. The Luminance Contrast is calculated:

$$(L_{255 \text{ G. L.}} - L_{0 \text{ G.L.}}) / (L_{255 \text{ G. L.}} + L_{0 \text{ G.L}})$$

For both $+30^{\circ}$ and -30° . The lowest value shall be reported.

Note (9) Definition of Colour uniformity - Angular dependence:

From Note (7), it can measure the data as below chart.

	Measurin	g point R	Measurin	u'v'	
	u' _R	v' _R	u' _L	v' _L	u v
+30°					
-30°					

$$\Delta u'v' = \sqrt{(u'_R - u'_L)^2 + (v'_R - v'_L)^2}$$

For both +30° and -30°. The largest value in u'v' shall be reported.

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8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: M201P1-L03

(b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.

(c) CMO barcode definition:

Serial ID: XX-XX-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMO internal use	-
XX	Revision	Cover all the change
Х	CMO internal use	-
	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4
YMD		Month: 1~12=1, 2, 3, ~, 9, A, B, C
		Day: 1~31=1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U.
L	Product line #	Line 1=1, Line 2=2, Line 3=3,
NNNN	Serial number	Manufacturing sequence of product

(d) Customer's barcode definition:

Serial ID: CM-20P13-X-X-X-X-L-XX-L-YMD-NNNN

Code	Meaning	Description
CM	Supplier code	CMO=CM
20P13	Model number	M201P1-L03=20P13
Χ	Revision code	Non ZBD: 0~9, ZBD: A~Z
Х	Source driver IC code	Century=1, CLL=2, Demos=3, Epson=4, Fujitsu=5, Himax=6, Hitachi=7, Hynix=8, LDI=9, Matsushita=A, NEC=B, Novatec=C,
Х	Gate driver IC code	OKI=D, Philips=E, Renasas=F, Samsung=G, Sanyo=H, Sharp=I, TI=J, Topro=K, Toshiba=L, Windbond=M
XX	Cell location	Tainan, Taiwan=TN
L	Cell line #	1~12=0~C
XX	Module location	Tainan, Taiwan=TN
L	Module line #	1~12=0~C
	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4
YMD		Month: 1~12=1, 2, 3, ~, 9, A, B, C
		Day: 1~31=1, 2, 3, ~, 9, A, B, C, ~, T, U, V
NNNN	Serial number	By LCD supplier



Issued Date: Aug. 30, 2006 Model No.: M201P1-L03

Approval

9. PRECAUTIONS

9.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.
- (4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- (5) Do not pull the I/F connector in or out while the module is operating.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.
- (9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (10) When ambient temperature is lower than 10°C may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

9.2 SAFETY PRECAUTIONS

- (1) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

