( ) **Preliminary Specifications**
(✓) **Final Specifications**

Module	**15.6"FHD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	**B156HAT01.0 (H/W: 0A)**
Note ( )	***e-TP Display***

Customer	**Date**	**Approved by**	**Date**
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Note: This Specification is subject to change without notice.

NBBU Marketing Division
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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2013/11/07	All	First Edition for Customer		
0.2 2013/12/17	P.30	Shipping Label (X10 version)	Shipping Label (X20 version)	
	P.33	EDID (X10 version)	EDID (X20 version)	
0.3 2014/01/8	P.7	Color / Chromaticity Coodinates TBD	Color / Chromaticity Coodinates information fill in	
1.0 2014/02/13	P19	value empty	Value fill in	
	P23	value empty	Value fill in	
	P.30	Shipping Label (X20 version)	Shipping Label (A00 version)	
	P.33	EDID (X20 version)	EDID (A00 version)	
1.1 2014/05/20	P.21	Connector Description update	Connector Description	
	P.24	Interface Time value empty	Interface Time value full in	
	P.31	Shipping Label (A00 version)	Shipping Label (A02 version)	
	P.34	EDID (A00 version)	EDID (A02 version)	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electronic breakdown.

2. General Description

B156HAT01.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD (1920(H) x 1080(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B156HAT01.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	**Unit**	**Specifications**			
Screen Diagonal	[mm]	394.9			
Active Area	[mm]	344.16 x 193.59			
Pixels H x V		1920 x 3(RGB) x 1080			
Pixel Pitch	[mm]	0.17925 x 0.17925			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (ILED= 20 mA) **(Note: ILED is LED current)**	[cd/m^2]	270 typ. (5 points average) (Total Solution) 230 min. (5 points average) (Total Solution)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		800:1 typ			
Response Time	[ms]	25 typ			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	6.2 (Include Logic and Blu power)			
Weight	[Grams]	400 max (Base panel only), 580 max			
Physical Size **Include bracket** **(Panel only)**	[mm]		Min.	Typ.	Max.
		Length	366.13	366.38	366.63
		Width	224.31	224.81	225.31
Thicknessss		Thickness	3.2 (Base panel) 4.2 (Total Solution_Panel Side) 5.4 (Total Solution _PCBA Side)		
Physical Size **Include bracket** **(Total Solution)**	[mm]		Min.	Typ.	Max.
		Length	366.13	366.38	366.63
		Width	224.31	224.81	225.31
Electrical Interface		2 Lane eDP			
Glass Thickness	[mm]	0.5			
Surface Treatment		Glare			
Support Color		262K colors (RGB 6-bit)			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.1.1 General Touch Specification

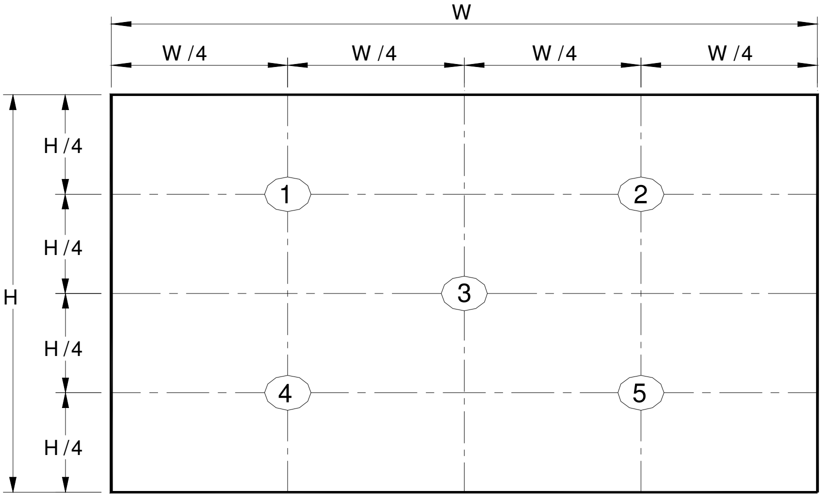
Item	Spec	Unit
Type of Touch Sensor	Projective Capacitive (OGS)	
Panel Size	15.6’	
Outline Dimension	357.83 X 205.32 typ	mm
Total Thickness	0.7 typ	mm
Total Weight	170 max	g
TP View Area	345.23 X 194.54 typ	mm
TP Active Area	346.23 X 195.54 typ	mm
Interface	USB and I2C	
Report Rate	Follow win8 – 100Hz	Hz
Multi-Touch Point	10 points	
Input method	Finger	
Touch panel sensor IC	Elan (eKTH3915)	
Channel	72 x 41	
Distance between 2 point	Follow win8 – 13	mm
Surface hardness	7	H
TP F/W version	TBD	
BM ink	PANTONE BLACK C	

2.2 Optical Characteristics

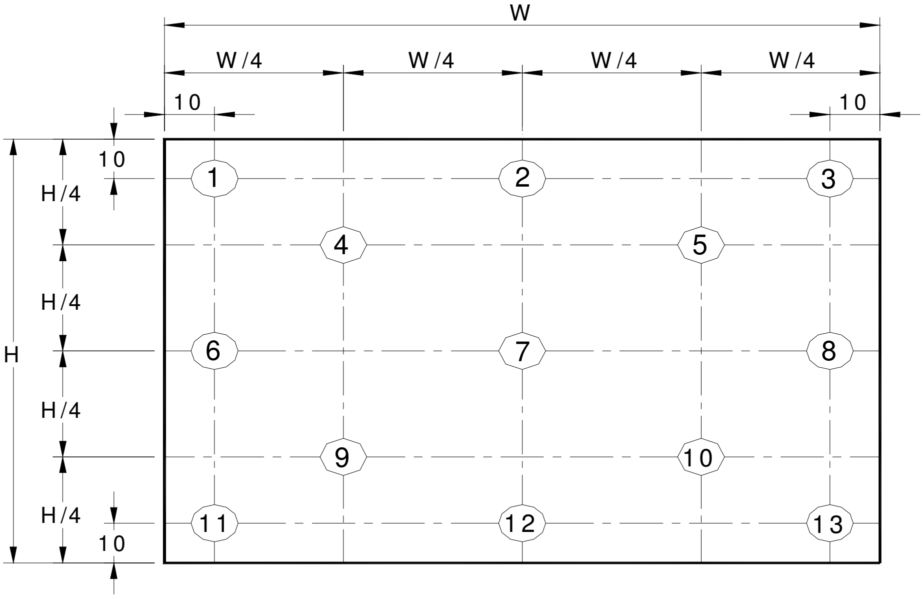
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=20mA			5 points average	230	270	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10	80	85	-	degree	4, 9
		θ_L	(Left)	80	85	-		
		ψ_H	Vertical (Upper) CR = 10	80	85	-		
		ψ_L	(Lower)	80	85	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio		CR		-	800	-		4, 6
Cross talk		%		-	-	4		4, 7
Response Time		T_{RT}	Rising + Falling	-	25	16		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.615	0.645	0.675		4
		Ry		0.305	0.335	0.365		
	Green	Gx		0.283	0.313	0.343		
		Gy		0.584	0.614	0.644		
	Blue	Bx		0.122	0.152	0.182		
		By		0.030	0.060	0.090		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	72	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



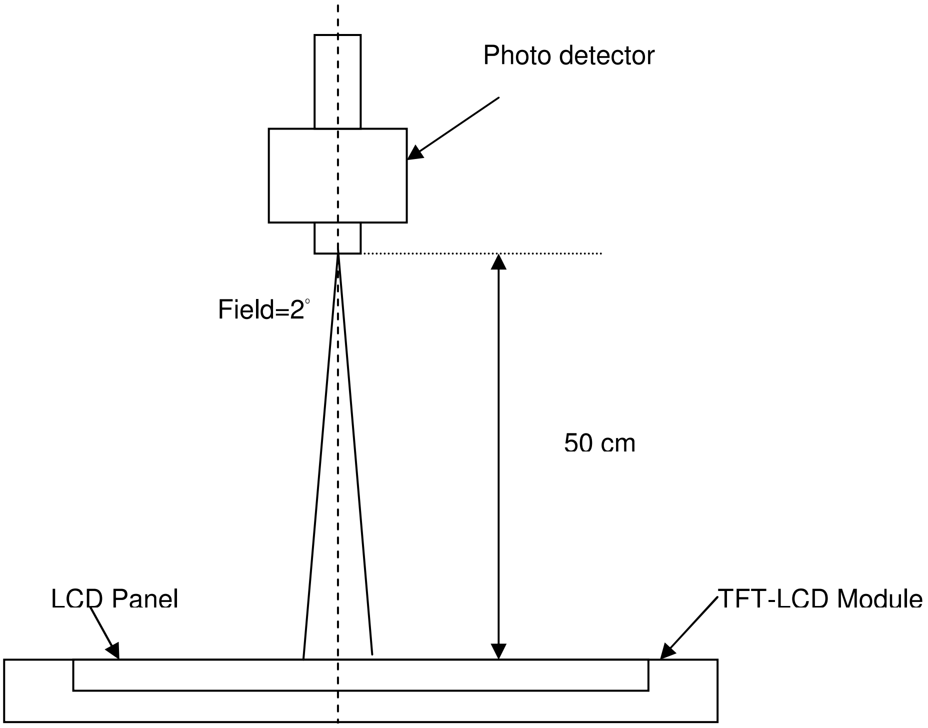
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Center of the screen

Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)=} \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

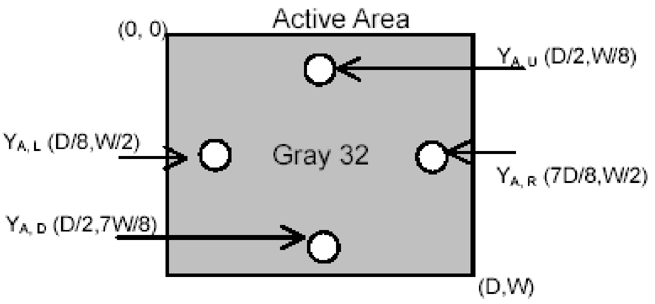
Note 7： Definition of Cross Talk (CT)

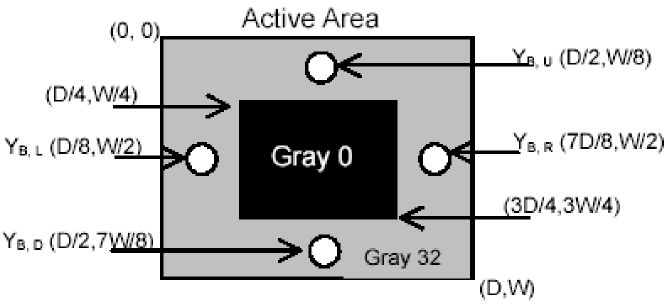
CT = ∣ YB – YA ∣ / YA × 100 (%)

Where

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

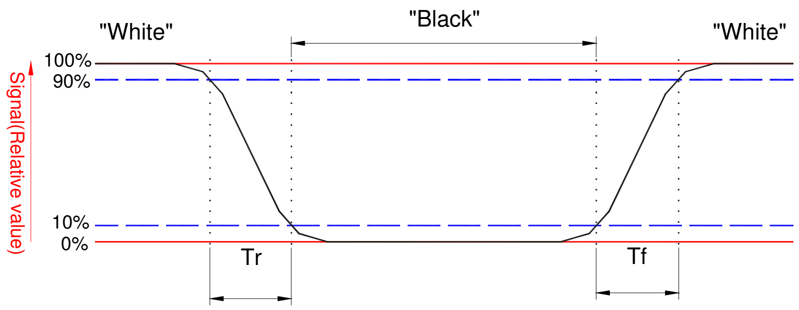
YB = Luminance of measured location with gray level 0 pattern (cd/m2)


Active Area
(0, 0)
YA, U (D/2,W/8)
YA, L (D/8,W/2)
Gray 32
YA, R (7D/8,W/2)
YA, D (D/2,7W/8)
(D,W)


Active Area
(0, 0)
YB, U (D/2,W/8)
(D/4,W/4)
YB, L (D/8,W/2)
Gray 0
YB, R (7D/8,W/2)
(3D/4,3W/4)
YB, D (D/2,7W/8)
Gray 32
(D,W)

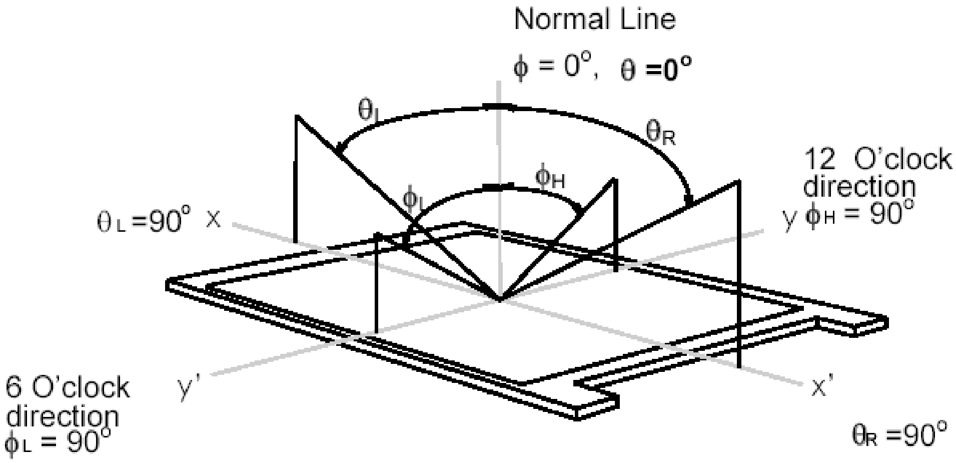
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



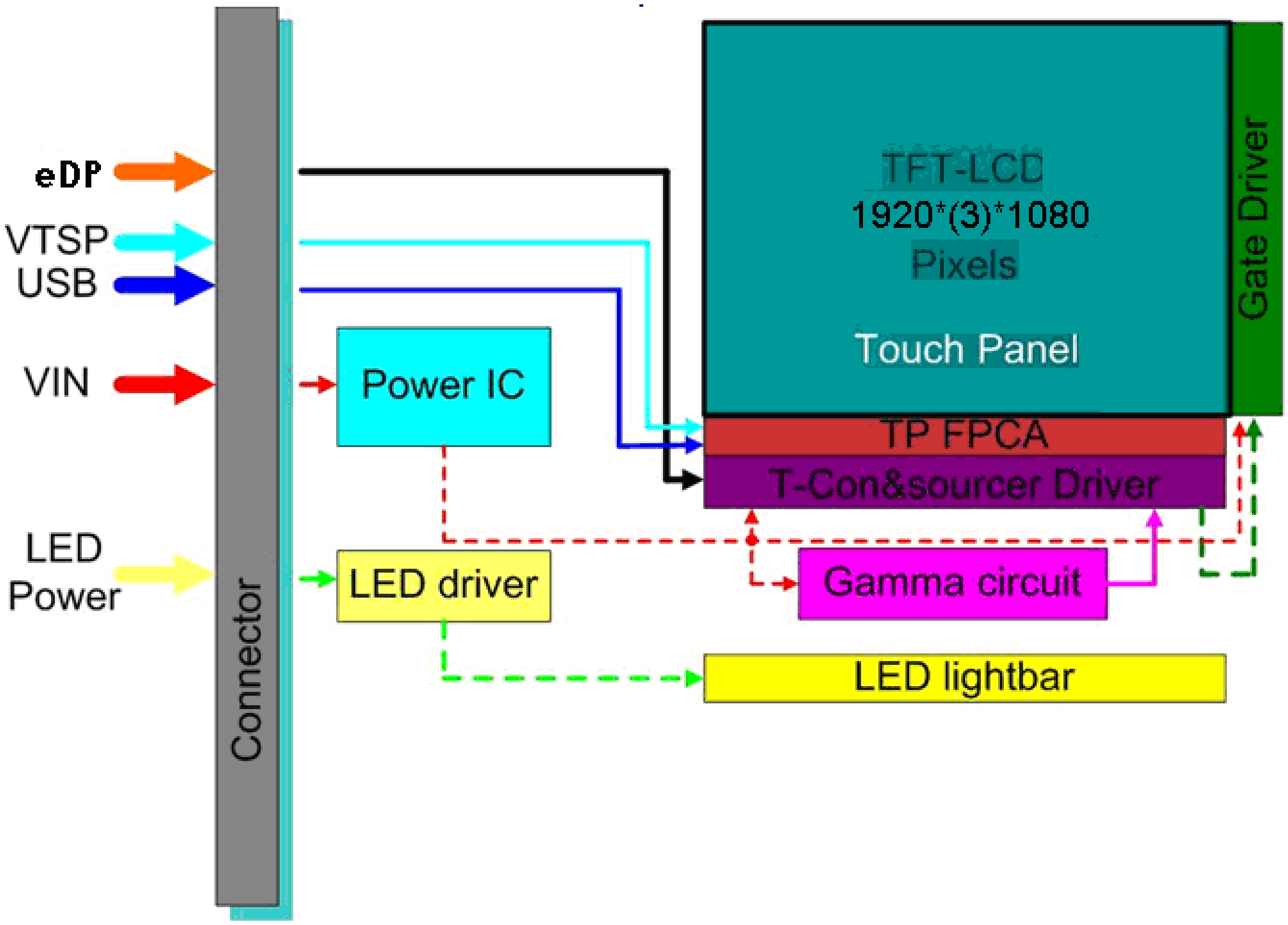
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.


Normal Line
ϕ = 0°, θ =0°
θL
θR
ϕH
ϕL
12 O'clock direction
y ϕH = 90°
θL =90° x
6 O'clock direction
ϕL = 90°
y'
x'
θR =90°

3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 40 Pin (One CH/connector Module)


eDP
VTSP
USB
VIN
LED
Power
Connector
Power IC
LED driver
TFT-LCD
1920*(3)*1080
Pixels
Touch Panel
Gate Driver
TP FPCA
T-Con&sourcer Driver
Gamma circuit
LED lightbar

4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

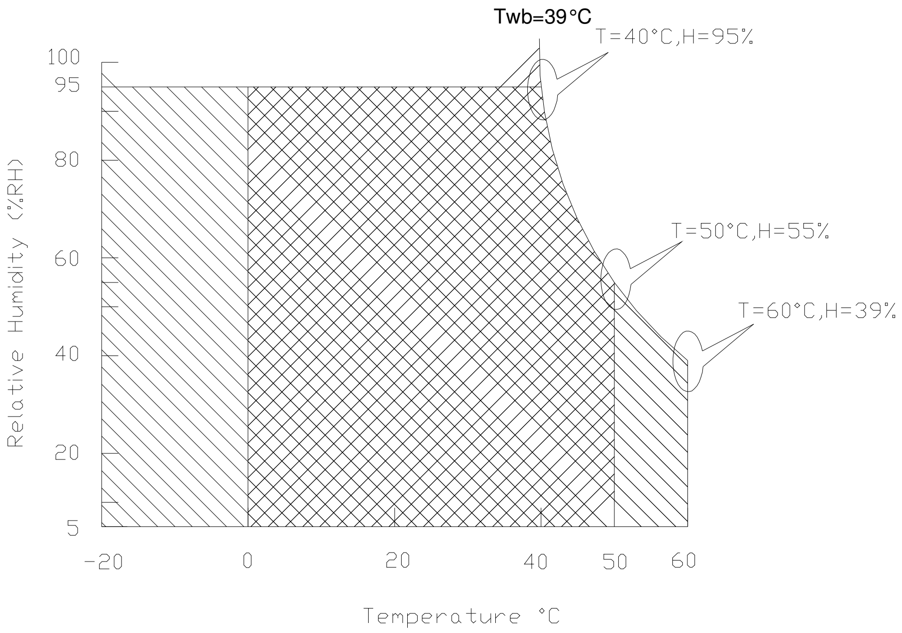
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[oC]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[oC]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range ▩

Storage Range ▩ + ▨

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

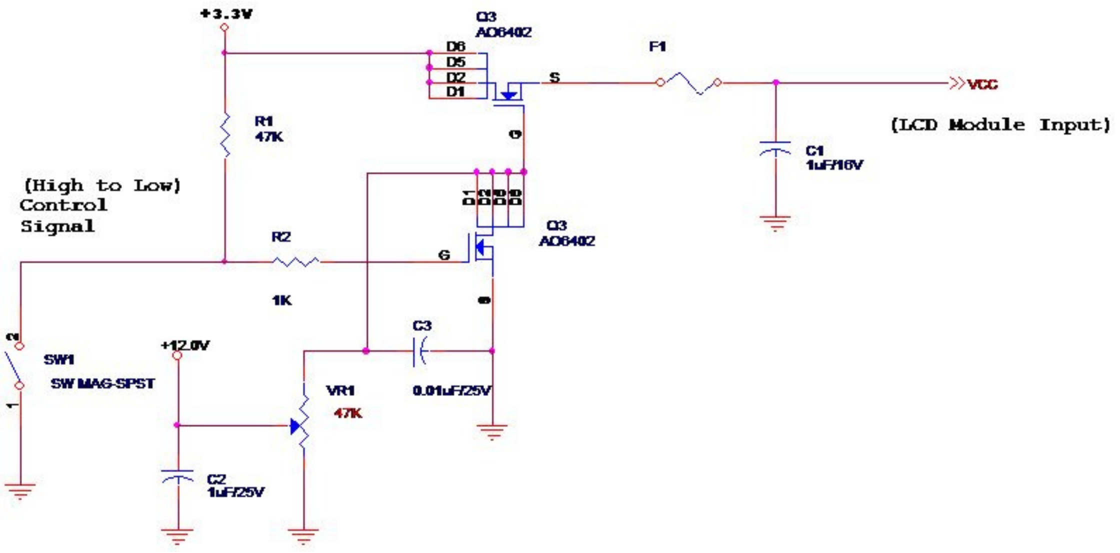
The power specification are measured under 25℃ and frame frenquency under 60Hz

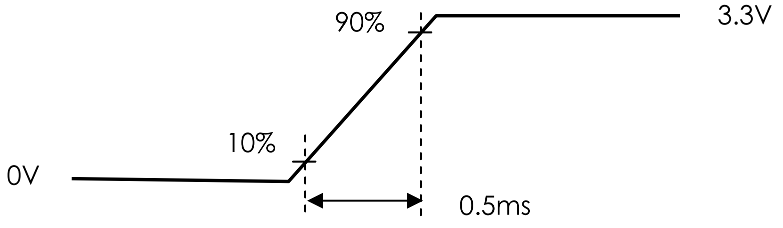
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.6	[Watt]	Note 1
IDD	IDD Current	-	-	22	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Typical Measurement Condition : Mosaic Pattern

Note 2：Measure Condition


+3.3V
Q3
AO6402
D6
D5
D2
D1
S
F1
>>VCC
(LCD Module Input)
C1
1uF/16V
R1
47K
(High to Low)
Control
Signal
R2
1K
G
Q3
AO6402
C3
0.01uF/25V
SW1
SW MAG-SPST
+12.0V
VR1
47K
C2
1uF/25V



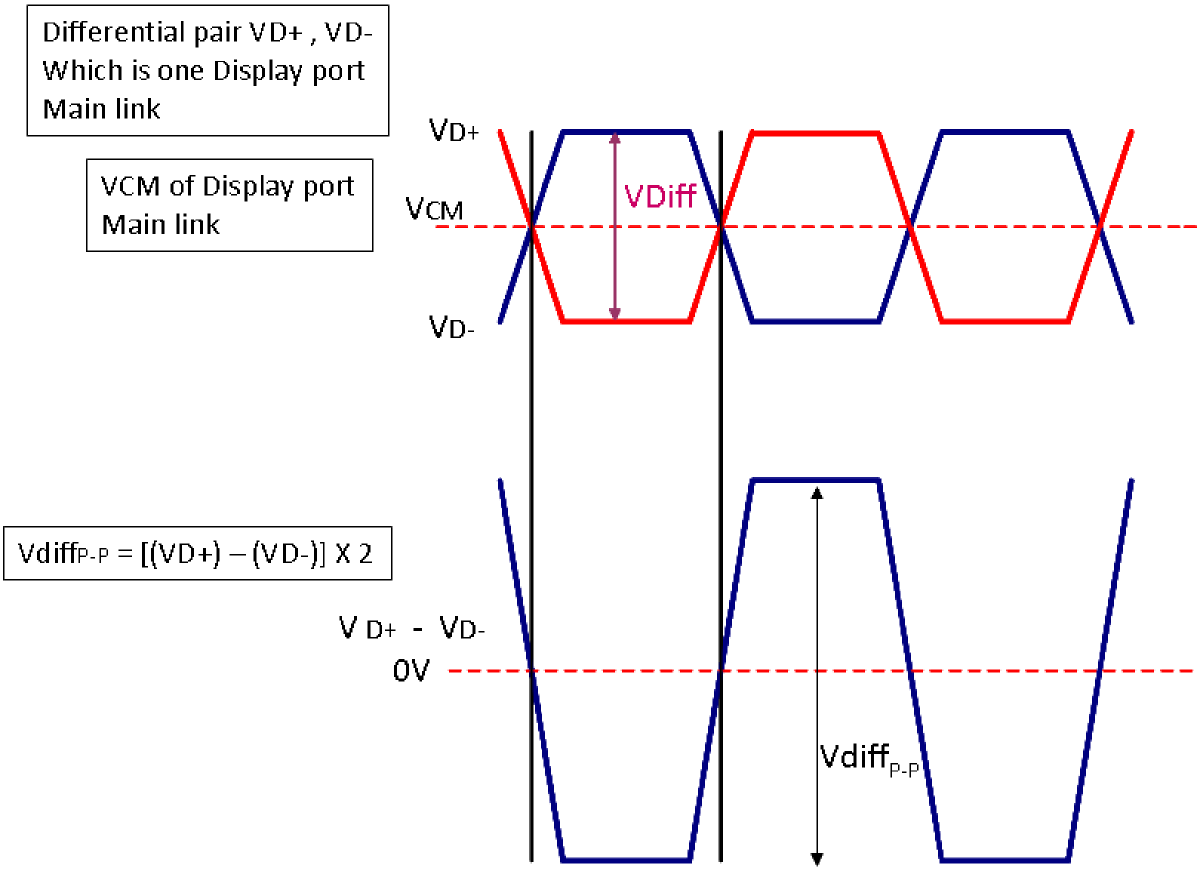
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

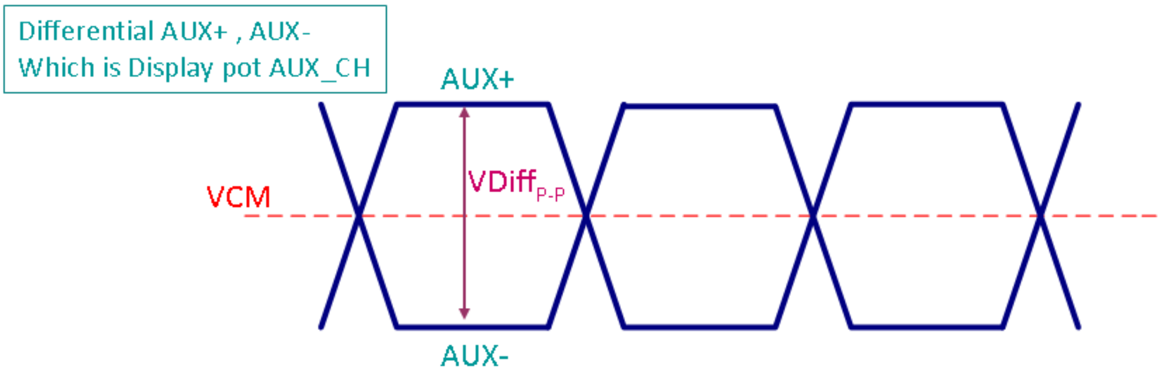
Display Port main link signal:


Differential pair VD+ , VD- Which is one Display port Main link
VCM of Display port Main link
VD+
VCM
VD-
VDiff
Vdiff$_{P-P}$ = [(VD+) – (VD-)] X 2
V D+ - VD-
0V
Vdiff$_{P-P}$

Display port main link					
		Min	**Typ**	**Max**	**unit**
VCM	RX input DC Common Mode Voltage		0		V
VDiff$_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Fallow as VESA display port standard V1.1a

Display Port AUX_CH signal:


Differential AUX+ , AUX-
Which is Display pot AUX_CH
AUX+
VCM
VDiffP-P
AUX-

Display port AUX_CH					
		Min	**Typ**	**Max**	**unit**
VCM	AUX DC Common Mode Voltage		0		V
VDiff$_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Fallow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display port VHPD					
		Min	**Typ**	**Max**	**unit**
VHPD	HPD Voltage	2.25		3.6	V

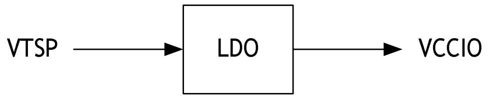
Fallow as VESA display port standard V1.1a.

5.2 Touch Sensor

5.2.1 Power Specification

Items	Symbol	Specifications			Unit	Notes
		Min.	Typ.	Max.		
Touch Panel Power Supply	VTSP	4.5	5	5.5	V	Ripple <100mV
Touch IC Power Voltage	VCCIO	1.8	3.3	3.6	V	
Input voltage	VIH	VCCIO×0.7	-	VCCIO	V	
	VIL	0	-	VCCIO×0.3	V	
Normal mode Current consumption @ Report rate 100Hz	INORMAL	-	-	45	mA	
Idle mode Current consumption	IIDLE	-	-	30	mA	
Sleep mode Current consumption	ISLEEP	-	60	130	uA	

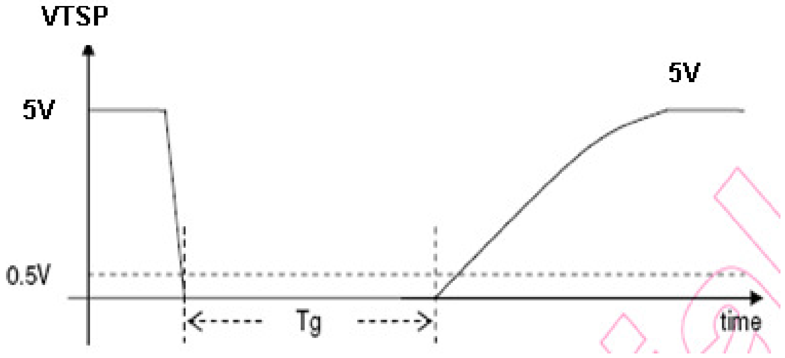
Note:



5.2.2 Touch Sensor TP_EN

TP_EN	TP Function
H	Ok
L	No function
NC	Ok

5.2.3 Touch Power off and then Power on Sequence



During power off, the VTSP must be lower than 0.5V for at least 10us (Tg>10us) to make sure the touch controller be correctly reset.

5.3 Backlight Unit

5.3.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	4.6	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.3.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	7	12	21	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN *Note 1	1.8			[Volt]	
LED Enable Input Low Level				0.5	[Volt]	
PWM Logic Input High Level$	VPWM_EN *Note 1	1.8			[Volt]	
PWM Logic Input Low Level$				0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5		100	%	

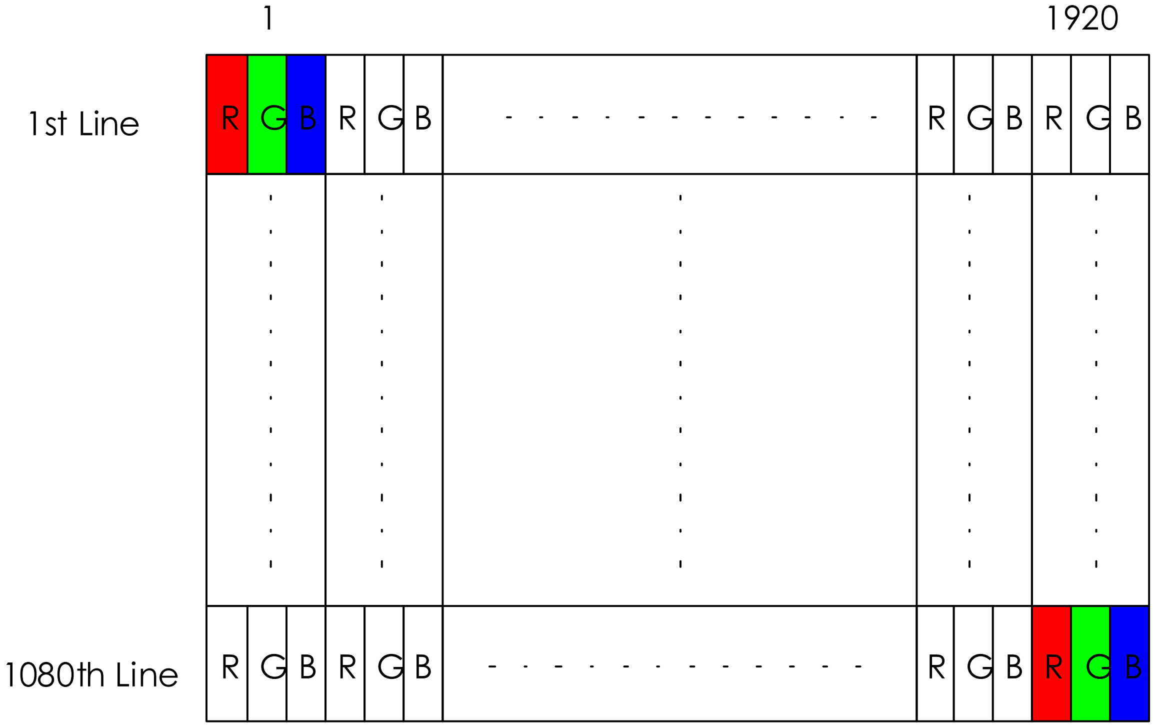
Note 1 : Recommanded system pull up/down resistor no bigger than 10kohm.

Note 2 : If the PWM duty ratio(min) is set between 5% to 1%，the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20455-040E-12R or compatible
Mating Housing/Part Number	IPEX 20453-040E-12 or compatible

6.2.2 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	DCR_EN	Dynamic Contrast Ratio Input Level
2	H_GND	High Speed Ground
3	Lane1_N	Comp Signal Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test or NC	LCD Panel Self Test Enable (Optional)
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	HPD	HPD signale pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL PWM DIM	System PWM signal Input
24	NC	Reverse for AUO TEST only
25	NC	Reverse for AUO TEST only
26	BL_PWR	Backlight power (5V~21V)
27	BL_PWR	Backlight power (5V~21V)
28	BL_PWR	Backlight power (5V~21V)
29	BL_PWR	Backlight power (5V~21V)
30	NC	No Connect
31	TP_D-	USB Data- for Touch
32	TP_D+	USB Data+ for Touch
33	GND	Ground–Shield
34	VTSP	Touch panel power supply (5.0V)
35	VTSP	Touch panel power supply (5.0V)
36	TP_EN	Reserve for Touch function enable

37	TP_CLK	I2C Clock for Touch (NC for USB input)
38	TP_Data	I2C Data for Touch (NC for USB input)
39	INT	Interrupt for Touch (NC for USB input)
40	RST	Reset for Touch (NC for USB input)

Note1：start from right side
Note2：Input signals shall be low or High-impedance state when VDD is off.

6.3 Interface Timing

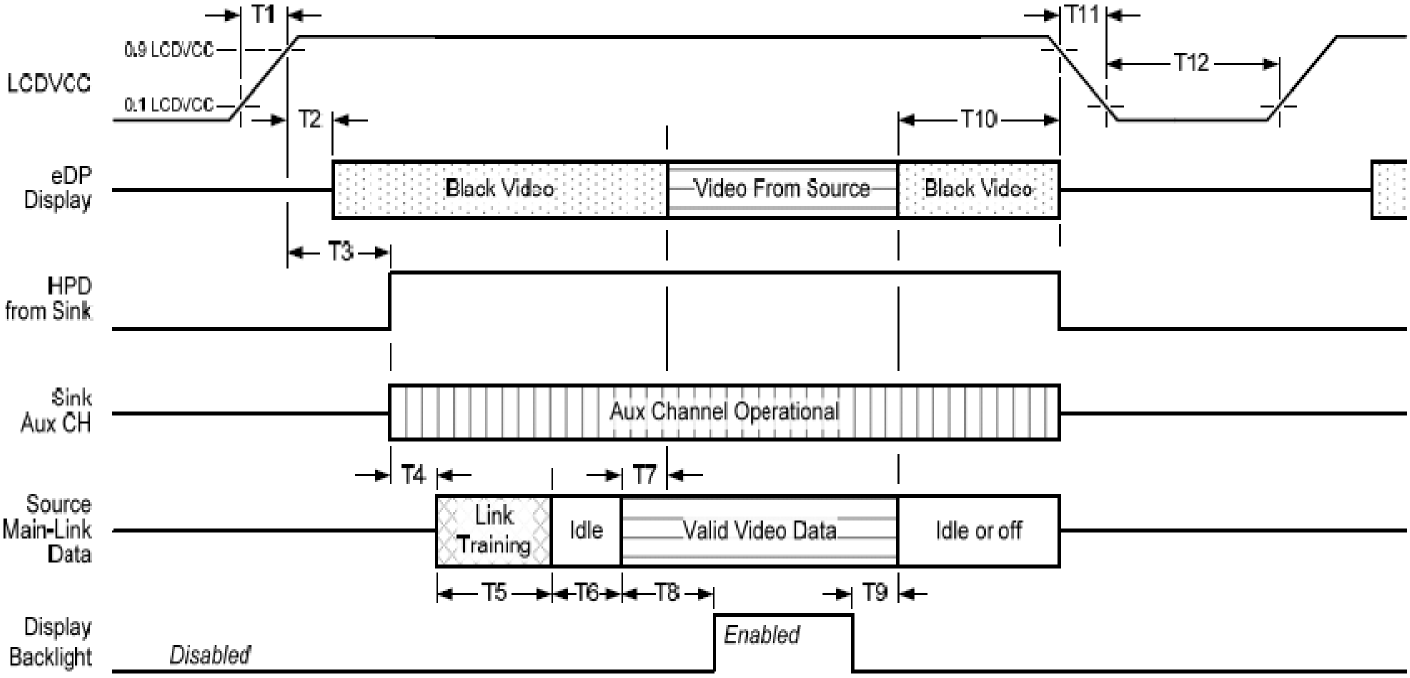
Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-		60		Hz
Clock frequency		$1/T_{Clock}$		141		MHz
Vertical Section	Period	T_V	1090	1116	3080	T_{Line}
	Active	T_{VD}	1080			
	Blanking	T_{VB}	10	36	2000	
Horizontal Section	Period	T_H	2000	2104	2320	T_{Clock}
	Active	T_{HD}	1920			
	Blanking	T_{HB}	80	184	400	

Note 1 : DE mode only
Note 2 : The maximum clock frequency = (960+B)*(1080+A)*60 < 80MHz

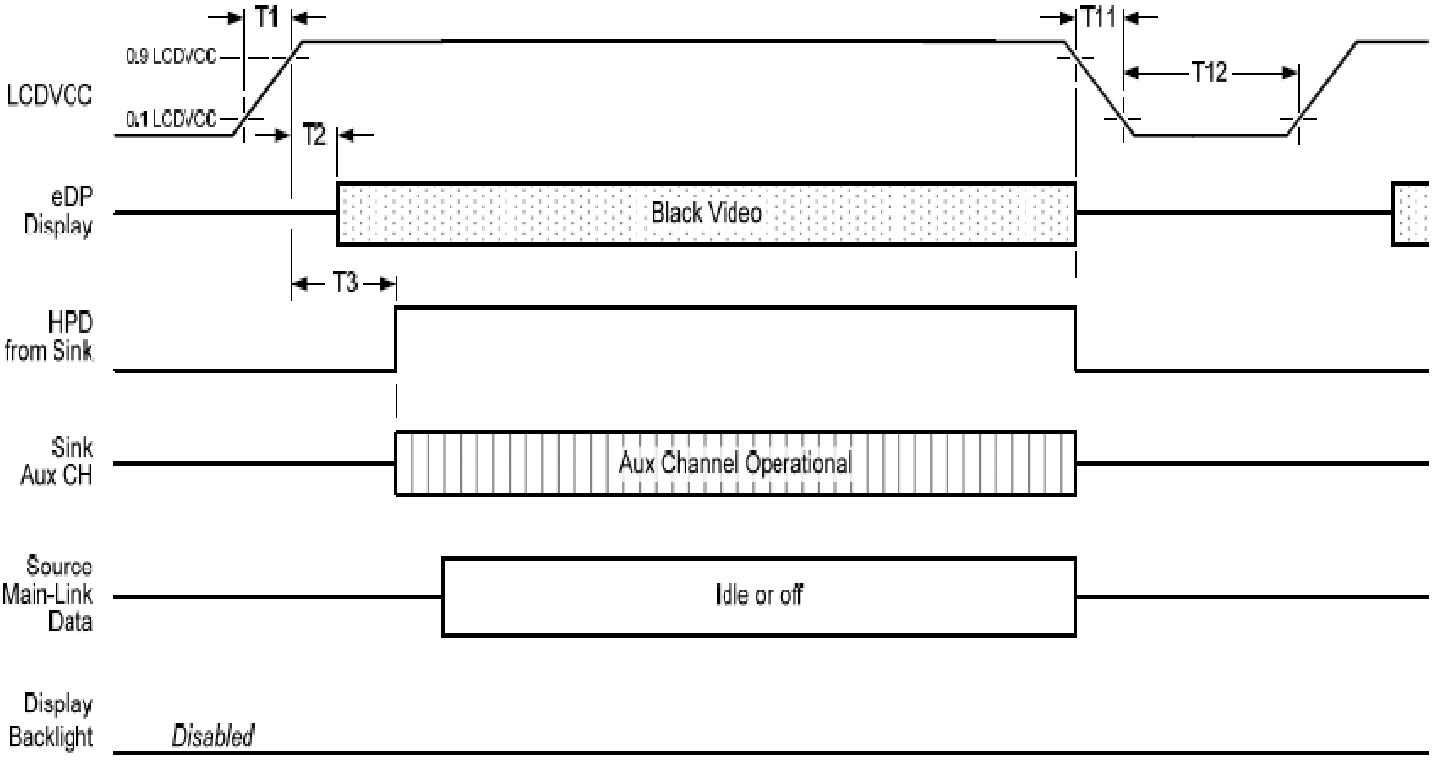
6.4 Power ON/OFF Sequence

Display Port panel power sequence:


T1
0.9 LCDVCC
0.1 LCDVCC
LCDVCC
T2
T11
T12
T10
eDP
Display
Black Video
Video From Source
Black Video
T3
HPD
from Sink
Sink
Aux CH
Aux Channel Operational
T4
T7
Source
Main-Link
Data
Link
Training
Idle
Valid Video Data
Idle or off
T5
T6
T8
T9
Display
Backlight
Disabled
Enabled

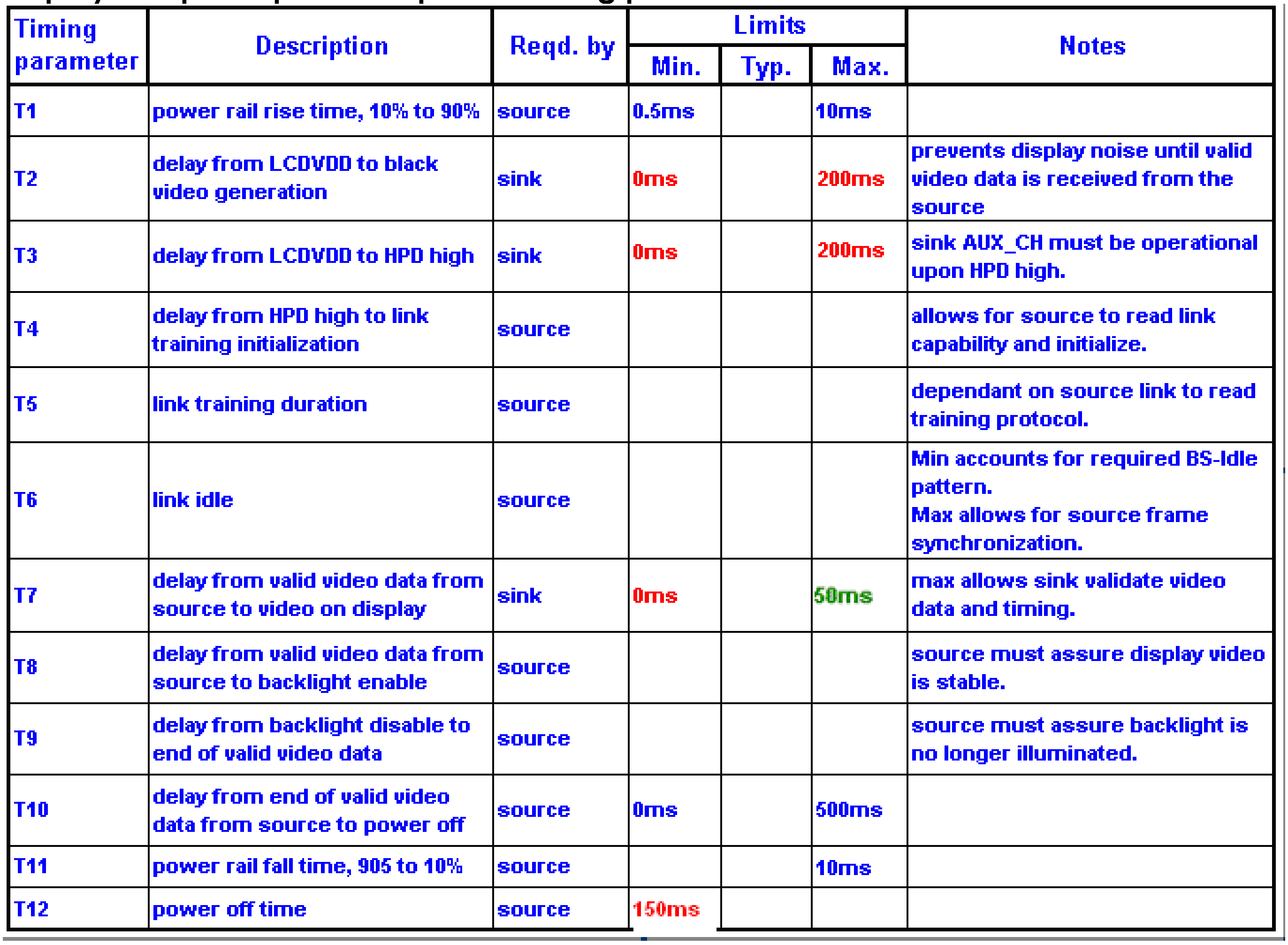
Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:


T1
0.9 LCDVCC
0.1 LCDVCC
LCDVCC
T2
T11
T12
eDP
Display
Black Video
T3
HPD
from Sink
Sink
Aux CH
Aux Channel Operational
Source
Main-Link
Data
Idle or off
Display
Backlight
Disabled

Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:



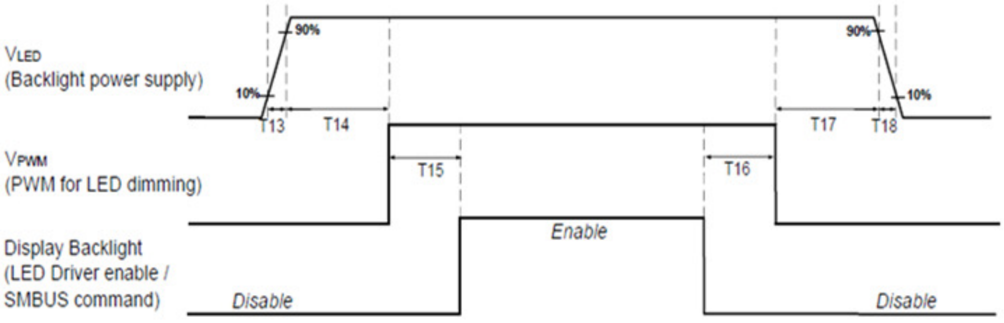
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	150ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

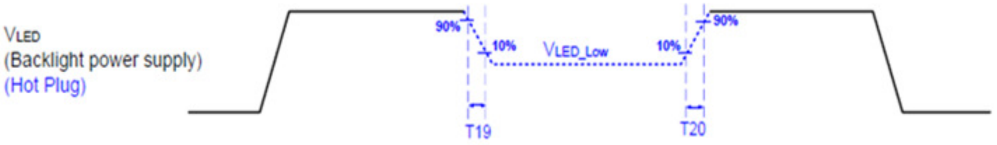
Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:


VLED
(Backlight power supply)
90%
10%
90%
10%
T13
T14
T17
T18
VPWM
(PWM for LED dimming)
T15
T16
Display Backlight
(LED Driver enable /
SMBUS command)
Enable
Disable
Disable

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.


VLED
(Backlight power supply)
(Hot Plug)
90%
10%
VLED_Low
10%
90%
T19
T20

	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃ to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

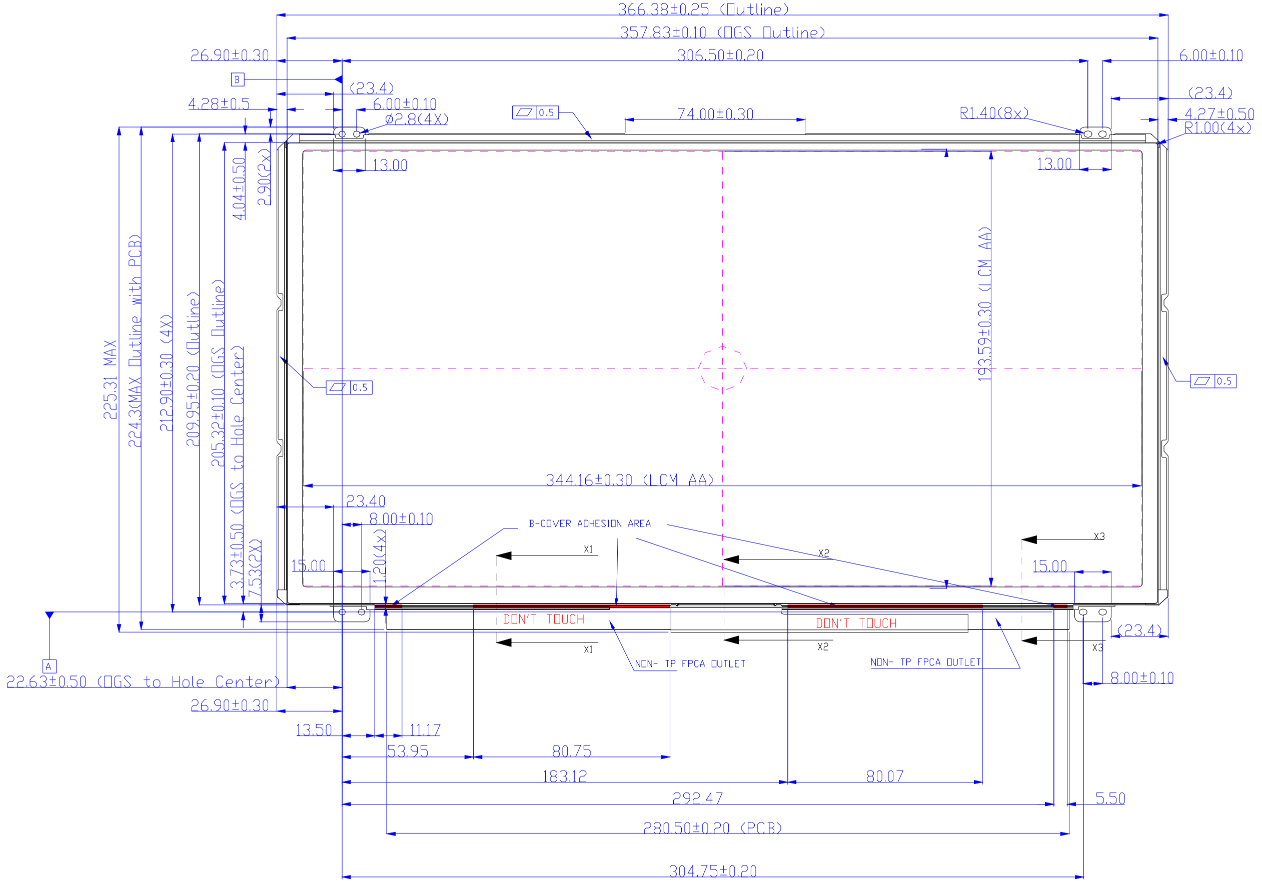
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

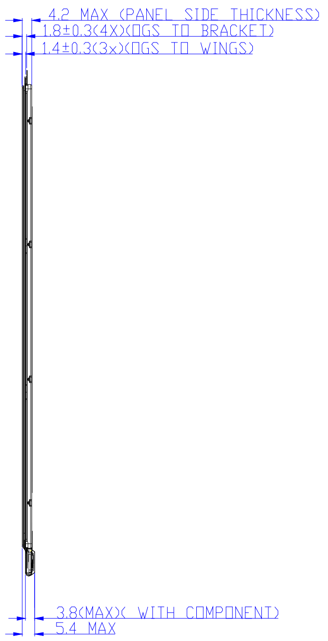
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

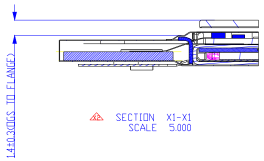
8. Mechanical Characteristics

8.1 LCM Outline Dimension

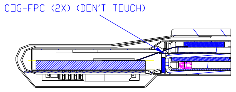
8.1.1 Standard Front View


366.38±0.25 (Outline)
357.83±0.10 (OGS Outline)
306.50±0.20
26.90±0.30
6.00±0.10
B
(23.4)
4.28±0.5
6.00±0.10
Ø2.8(4X)
0.5
74.00±0.30
R1.40(8x)
(23.4)
4.27±0.50
R1.00(4x)
13.00
13.00
4.04±0.50
2.90(2x)
225.31 MAX
224.3(MAX Outline with PCB)
212.90±0.30 (4X)
209.95±0.20 (Outline)
205.32±0.10 (OGS Outline)
3.73±0.50 (OGS to Hole Center)
7.53(2X)
193.59±0.30 (LCM AA)
0.5
0.5
344.16±0.30 (LCM AA)
23.40
8.00±0.10
B-COVER ADHESION AREA
X1
X2
X3
15.00
1.20(4x)
15.00
DON'T TOUCH
DON'T TOUCH
X1
X2
X3
NON- TP FPCA OUTLET
NON- TP FPCA OUTLET
(23.4)
A
22.63±0.50 (OGS to Hole Center)
26.90±0.30
8.00±0.10
13.50
11.17
53.95
80.75
183.12
80.07
292.47
5.50
280.50±0.20 (PCB)
304.75±0.20

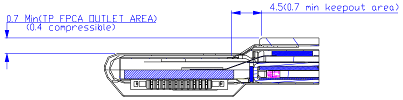

4.2 MAX (PANEL SIDE THICKNESS)
1.8±0.3(4X)(OGS TO BRACKET)
1.4±0.3(3x)(OGS TO WINGS)
3.8(MAX)(WITH COMPONENT)
5.4 MAX


1.4±0.3(OGS TO FLANGE)

SECTION X1-X1
SCALE 5.000

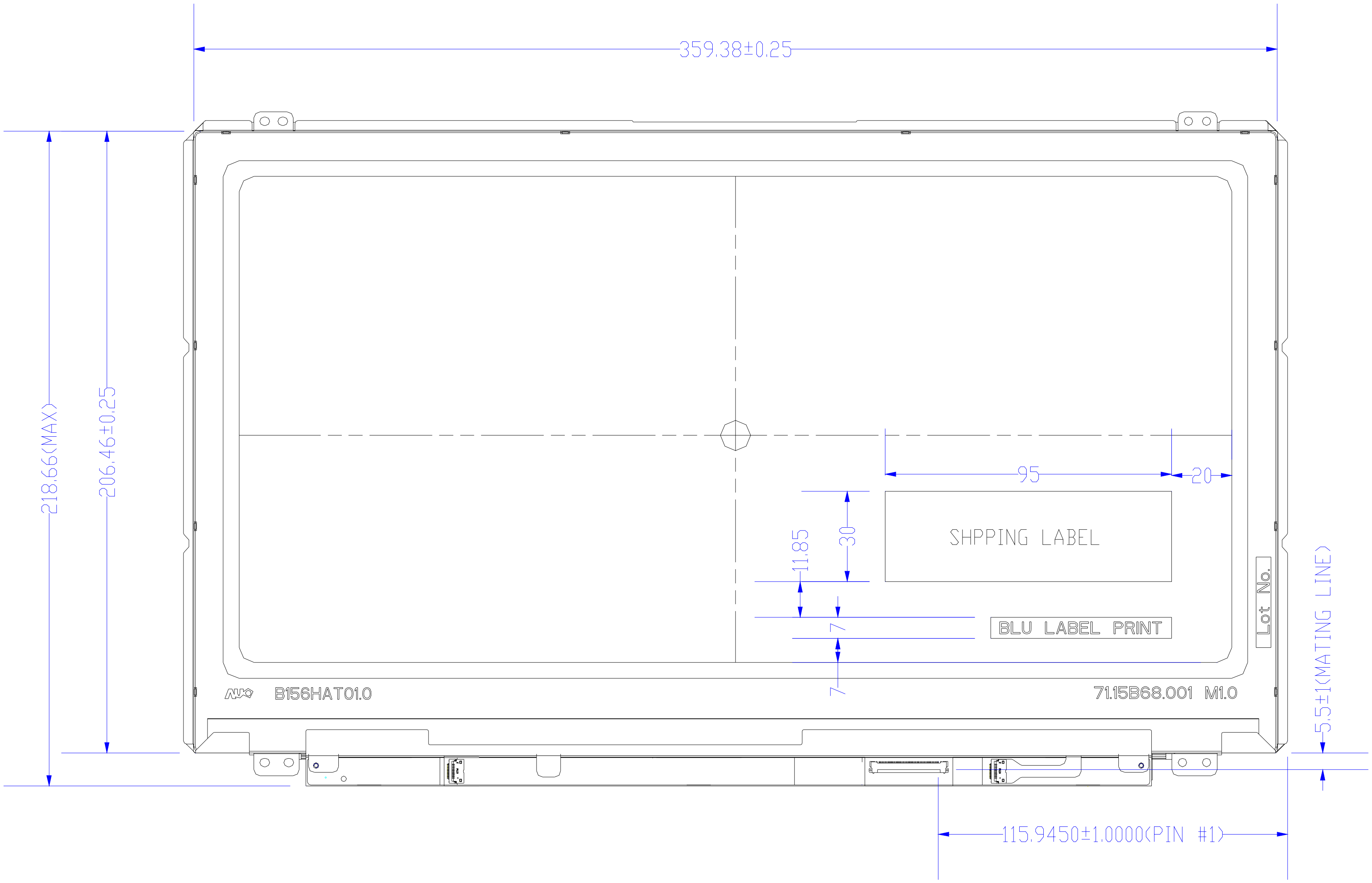

COG-FPC (2X) (DON'T TOUCH)

SECTION X2-X2
SCALE 5.000


0.7 Min(TP FPCA OUTLET AREA)
(0.4 compressible)
4.5(0.7 min keepout area)

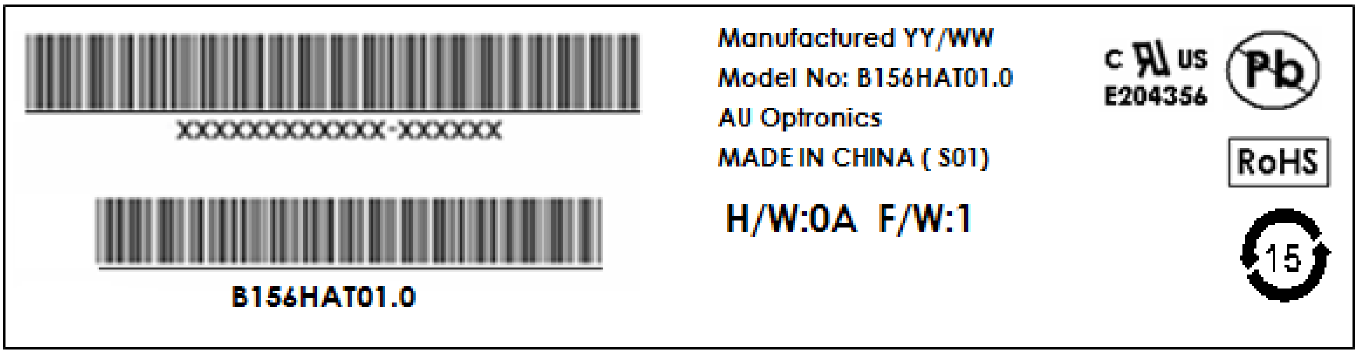
SECTION
X3-X3
SCALE 5.000

8.1.2 Standard Rear View


359.38±0.25
218.66(MAX)
206.46±0.25
95
20
SHPPING LABEL
30
11.85
7
BLU LABEL PRINT
7
Lot No.
5.5±1(MATING LINE)
B156HAT01.0
71.15B68.001 M1.0
115.9450±1.0000(PIN #1)

9. Shipping and Package

9.1 Shipping Label Format



XXXXXXXXXXXX-XXXXXX

B156HAT01.0

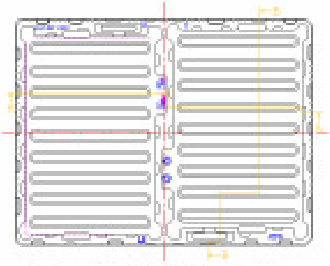
Manufactured YY/WW
Model No: B156HAT01.0
AU Optronics
MADE IN CHINA (S01)

H/W:0A F/W:1

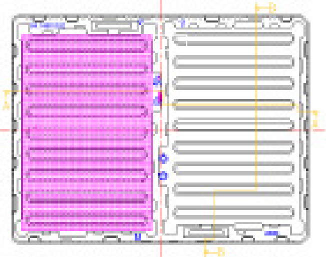
c UL us
E204356
Pb
RoHS
15

9.2 Carton Package

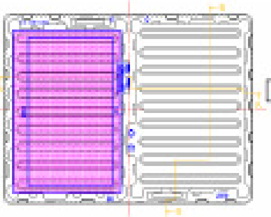
取出白色 PP 瓦楞板



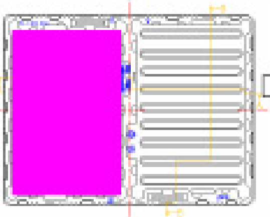
Tray 置放於 PP 瓦楞板上



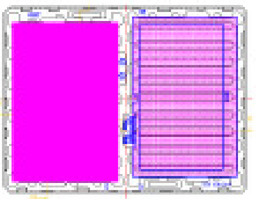
EPE spacer 放於 tray 盤上左側穴內



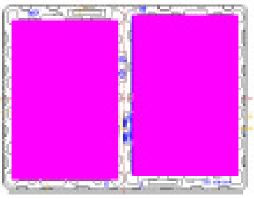
PANEL 放於 spacer 上, PCBA 側朝 tray 盤內側放入, sensor 面朝



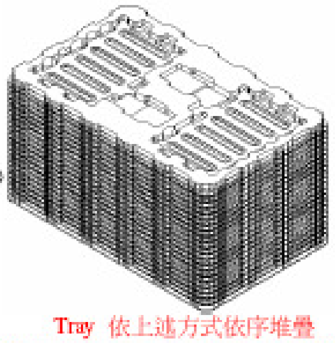
再放入 EPE spacer 於 SKD 上



EPE spacer 放於 tray 盤上右側穴內



先置 SKD 再放入 EPE spacer 於 SKD 上

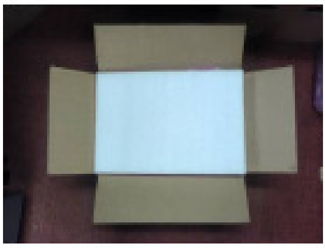


Tray 依上述方式依序堆疊
(TP 共 16 片, tray 共 17 片,最上面第 17 個 tray 是空的)

完成堆疊的 tray 放入靜電袋中,
並使用 tape 封口

EPE cushion 放入紙箱

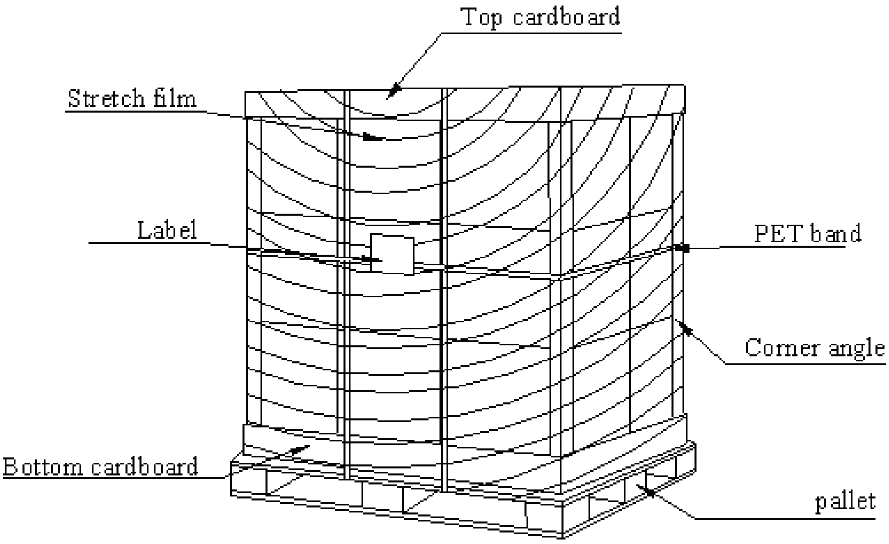
將包好靜電袋的 tray 整落放入紙箱中



放入 EPE cushion

Tape 封紙箱

9.3 Shipping Package of Palletizing Sequence


Top cardboard
Stretch film
Label
PET band
Corner angle
Bottom cardboard
pallet

10. Appendix: EDID Description

Address	Function	Value	Value	Value	Note
Hex		Hex	Bin	DEC	
0	Header	00	00000000	0	
1	Header	FF	11111111	255	
2	Header	FF	11111111	255	
3	Header	FF	11111111	255	
4	Header	FF	11111111	255	
5	Header	FF	11111111	255	
6	Header	FF	11111111	255	
7	Header	00	00000000	0	
8	EISA manufacture code = 3 Character ID	06	00000110	6	
9	EISA manufacture code (Compressed ASCII)	AF	10101111	175	
0A	Panel Supplier Reserved – Product Code	ED	11101101	237	
0B	Panel Supplier Reserved – Product Code	10	00010000	16	
0C	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0	
0D	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0	
0E	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0	
0F	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	18	00011000	24	
12	EDID structure version # = 1	01	00000001	1	
13	EDID revision # = 4	04	00000100	4	
14	Video I/P definition	95	10010101	149	
15	Max H image size = ?? cm(Rounded to cm)	22	00100010	34	
16	Max V image size = ?? cm(Rounded to cm)	13	00010011	19	
17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78	01111000	120	
18	Feature support	02	00000010	2	
19	Red/Green Low bit (RxRy/GxGy)	E2	11100010	226	
1A	Blue/White Low bit (BxBy/WxWy)	95	10010101	149	
1B	Red X Rx = 0.???	A3	10100011	163	
1C	Red Y Ry = 0.???	54	01010100	84	
1D	Green X Rx = 0.???	52	01010010	82	
1E	Green Y Ry = 0.???	99	10011001	153	
1F	Blue X Rx = 0.???	26	00100110	38	
20	Blue Y Ry = 0.???	0F	00001111	15	
21	White X Rx = 0.???	50	01010000	80	
22	White Y Ry = 0.???	54	01010100	84	

23	Established timings 1 (00h if not used)	00	00000000	0	
24	Established timings 2 (00h if not used)	00	00000000	0	
25	Manufacturer's timings (00h if not used)	00	00000000	0	
26	Standard timing ID1 (01h if not used)	01	00000001	1	
27	Standard timing ID1 (01h if not used)	01	00000001	1	
28	Standard timing ID2 (01h if not used)	01	00000001	1	
29	Standard timing ID2 (01h if not used)	01	00000001	1	
2A	Standard timing ID3 (01h if not used)	01	00000001	1	
2B	Standard timing ID3 (01h if not used)	01	00000001	1	
2C	Standard timing ID4 (01h if not used)	01	00000001	1	
2D	Standard timing ID4 (01h if not used)	01	00000001	1	
2E	Standard timing ID5 (01h if not used)	01	00000001	1	
2F	Standard timing ID5 (01h if not used)	01	00000001	1	
30	Standard timing ID6 (01h if not used)	01	00000001	1	
31	Standard timing ID6 (01h if not used)	01	00000001	1	
32	Standard timing ID7 (01h if not used)	01	00000001	1	
33	Standard timing ID7 (01h if not used)	01	00000001	1	
34	Standard timing ID8 (01h if not used)	01	00000001	1	
35	Standard timing ID8 (01h if not used)	01	00000001	1	
36	Pixel Clock/10,000 (LSB)	14	00010100	20	
37	Pixel Clock/10,000 (MSB)	37	00110111	55	
38	Horizontal Active = ???? pixels (lower 8 bits)	80	10000000	128	
39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	B8	10111000	184	
3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	70	01110000	112	
3B	Vertical Active = ??? lines	38	00111000	56	
3C	Vertical Blanking (Tvbp) = ?? lines (DE Blanking typ. for DE only panels)	24	00100100	36	
3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	40	01000000	64	
3E	Horizontal Sync, Offset (Thfp) = ?? pixels	10	00010000	16	
3F	Horizontal Sync, Pulse Width = ??? pixels	10	00010000	16	
40	Vertical Sync, Offset (Tvfp) = ? lines Sync Width = ? lines	3E	00111110	62	
41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0	
42	Horizontal Image Size =??? mm	58	01011000	88	
43	Vertical image Size = ??? mm	C1	11000001	193	
44	Horizontal Image Size / Vertical image size	10	00010000	16	
45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0	
46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0	

47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The int	1A	00011010	26	
48	Pixel Clock/10,000 (LSB)	10	00010000	16	
49	Pixel Clock/10,000 (MSB)	2C	00101100	44	
4A	Horizontal Active = xxxx pixels (lower 8 bits)	80	10000000	128	
4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	B8	10111000	184	
4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	70	01110000	112	
4D	Vertical Active = xxxx lines	38	00111000	56	
4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	24	00100100	36	
4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	40	01000000	64	
50	Horizontal Sync, Offset (Thfp) = xxxx pixels	10	00010000	16	
51	Horizontal Sync, Pulse Width = xxxx pixels	10	00010000	16	
52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	3E	00111110	62	
53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0	
54	Horizontal Image Size =xxx mm	58	01011000	88	
55	Vertical image Size = xxx mm	C1	11000001	193	
56	Horizontal Image Size / Vertical image size	10	00010000	16	
57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0	
58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0	
59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The int	1A	00011010	26	
5A	Flag	00	00000000	0	
5B	Flag	00	00000000	0	
5C	Flag	00	00000000	0	
5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254	
5E	Flag	00	00000000	0	
5F	Dell P/N 1st Character	39	00111001	57	
60	Dell P/N 2nd Character	46	01000110	70	
61	Dell P/N 3rd Character	38	00111000	56	
62	Dell P/N 4th Character	43	01000011	67	
63	Dell P/N 5th Character	38	00111000	56	

64	**EDID Revision** **Bit[6:0] See charts below** **Bit[7] 0: X-rev, 1: A-rev**	82	10000010	130	
65	Manufacturer P/N	42	01000010	66	
66	Manufacturer P/N	31	00110001	49	
67	Manufacturer P/N	35	00110101	53	
68	Manufacturer P/N	36	00110110	54	
69	Manufacturer P/N	48	01001000	72	
6A	Manufacturer P/N	41	01000001	65	
6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	54	01010100	84	
6C	Flag	00	00000000	0	
6D	Flag	00	00000000	0	
6E	Flag	00	00000000	0	
6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00	00000000	0	
70	Flag	00	00000000	0	
71	Color Management	00	00000000	0	
72	Panel Structure	41	01000001	65	
73	Frame Rate	22	00100010	34	
74	Light Controller Interface and Luminance	9E	10011110	158	
75	Outdoor Features	01	00000001	1	
76	Multi-Media Features	10	00010000	16	
77	Multi-Media Features	00	00000000	0	
78	Special Features #1	00	00000000	0	
79	Special Features #2	0A	00001010	10	
7A	Special Features #3	01	00000001	1	
7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10	
7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32	
7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32	
7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0	
7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	8C	10001100	140	