( ) Preliminary Specification
(V) Final Specification

Module	**11.6” (11.56”) HD 16:9 Color TFT-LCD**
Model Name	**B116XW05 V1 (0A)**
Note ( )	***LED Backlight without driving circuit design***

Customer	**Date**	**Approved by**	**Date**
		CH Lin	06/30/2011
Checked & Approved by	**Date**	**Prepared by**	**Date**
		Jonken Fan	06/30/2011
Note: This Specification is subject to change without notice.		**NBBU Marketing Division AU Optronics corporation**	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
1 2010/12/03 0.1	All	First Edition for Customer		
2 2011/04/11 0.2	All	First Edition for Customer		
3 2011/06/30 0.3	All		Final Specification	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electronic breakdown.

2. General Description

B116XW05 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) without LED backlight driving circuit.

B116XW05 V1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items		Unit	Specifications			
Screen Diagonal		[mm]	11.568”			
Active Area		[mm]	256.12 x 144.00			
Pixels H x V			1366 x 3(RGB) x 768			
Pixel Pitch		[mm]	0.1875(V) x 3 x 0.0625(H) mm			
Pixel Format			1366 (RGB stripe, H) x 768 (V)			
Display Mode			Normally White			
White Luminance (I_{LED}=20mA) **(Note: ILED is LED current)**		[cd/m^2]	200 typ. (5 points average) 170 min. (5 points average)			
Luminance Uniformity			1.25 max. (5 points)			
Contrast Ratio			600 typ, 500 min.			
Response Time		[ms]	16 typ / 20 Max			
Nominal Input Voltage VDD		[Volt]	+3.3 typ.			
Power Consumption		[Watt]	Logic 1.0 Max			
Weight		[Grams]	210 max.			
Physical Size Include bracket		[mm]		Min.	Typ.	Max.
			Length	282.5	283.0	283.5
			Width	166.5	167.0	167.5
			Thickness	-	-	3.6
Electrical Interface			1 channel eDP			
Glass Thickness		[mm]	0.3			
Polarizer	Top		Glossy Surface, 4H Hard Coating, EWV			
	Bottom		AG, 40% Haze, EWV			
Support Color			262K colors (RGB 6-bit)			

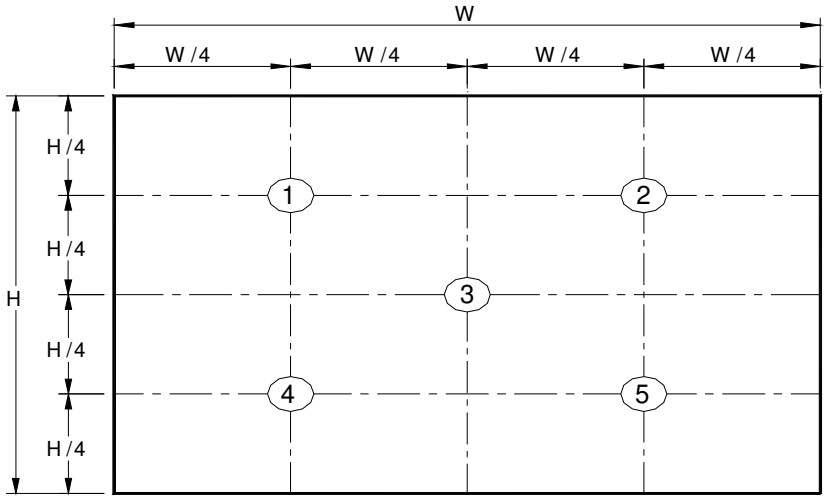
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

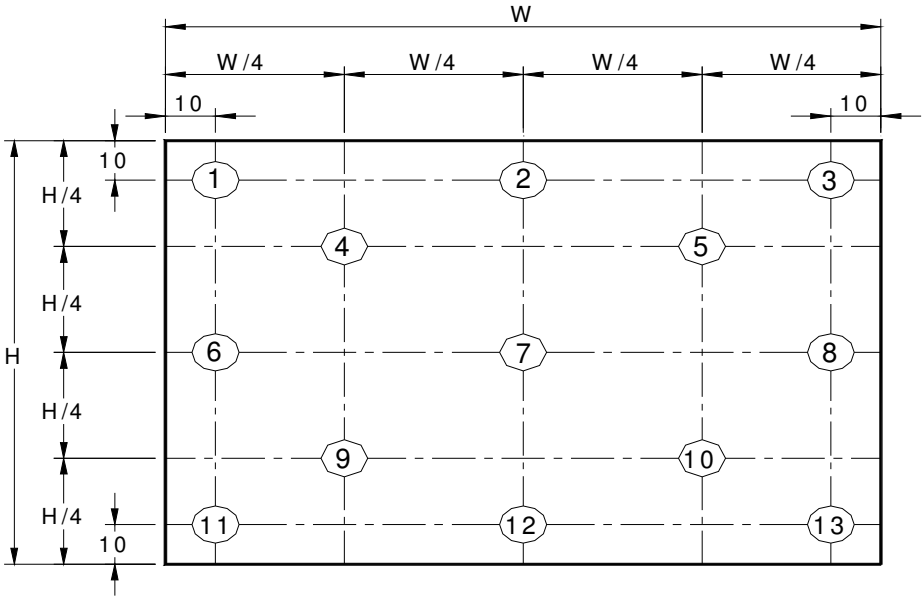
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=20mA			5 points average	170	200	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	65 65	70 70	- -	degree	4, 9
		ϕ_H ϕ_L	Vertical (Upper) CR = 10 (Lower)	50 50	60 60	- -		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio		CR		500	600	-		4, 6
Cross talk		%		-	-	4		4, 7
Response Time		T_{RT}	Rising + Falling	-	16	20	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.534	0.584	0.634		4
		Ry		0.291	0.341	0.391		
	Green	Gx		0.278	0.328	0.378		
		Gy		0.528	0.578	0.628		
	Blue	Bx		0.105	0.155	0.205		
		By		0.084	0.134	0.184		
	White	Wx		0.263	0.313	0.363		
		Wy		0.279	0.329	0.379		
NTSC		%		42	45	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

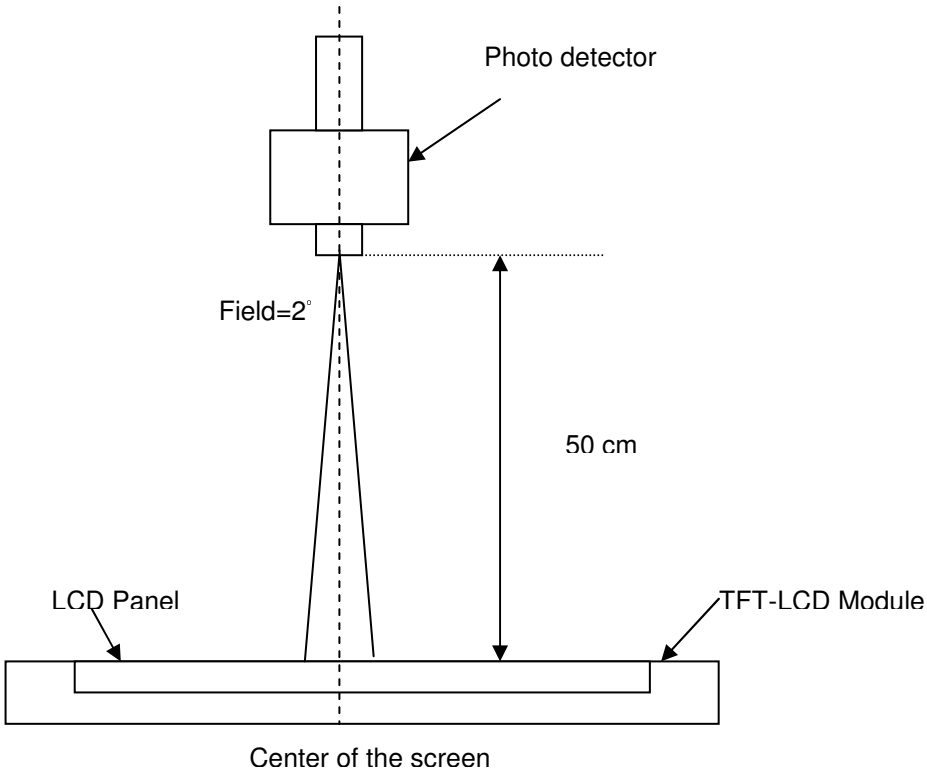
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

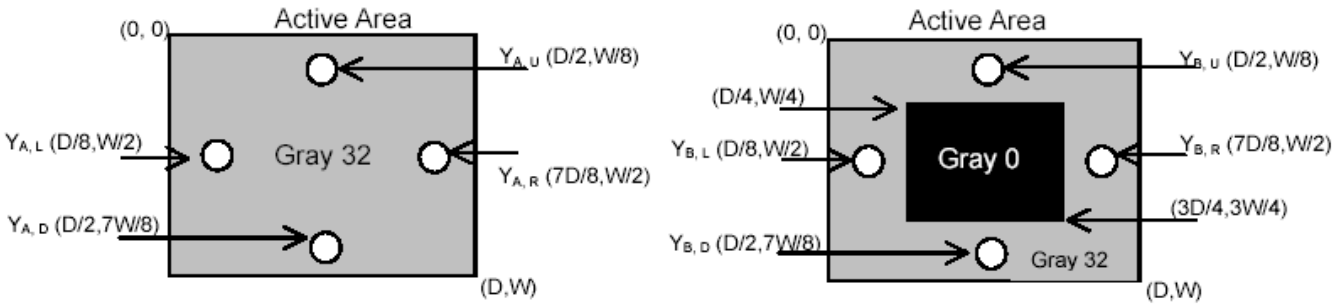
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

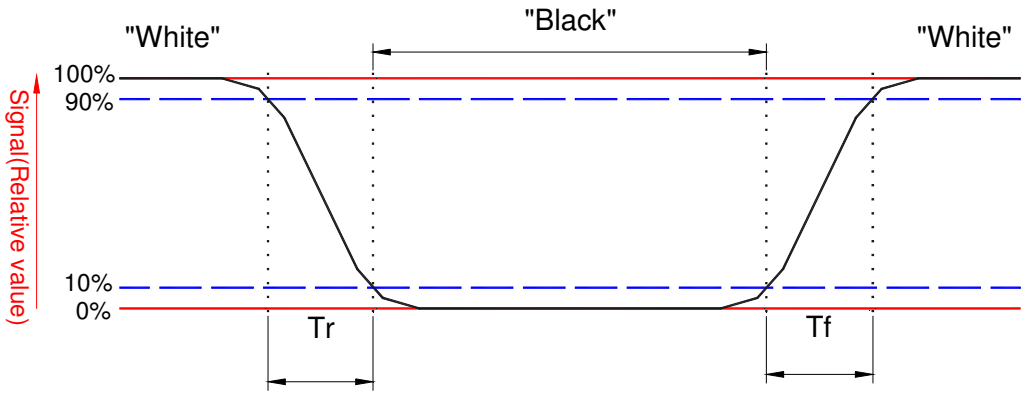
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



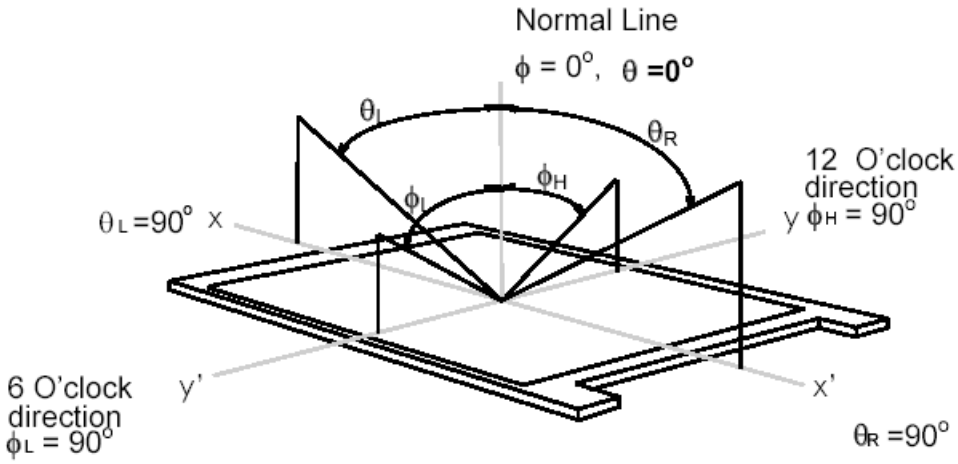
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



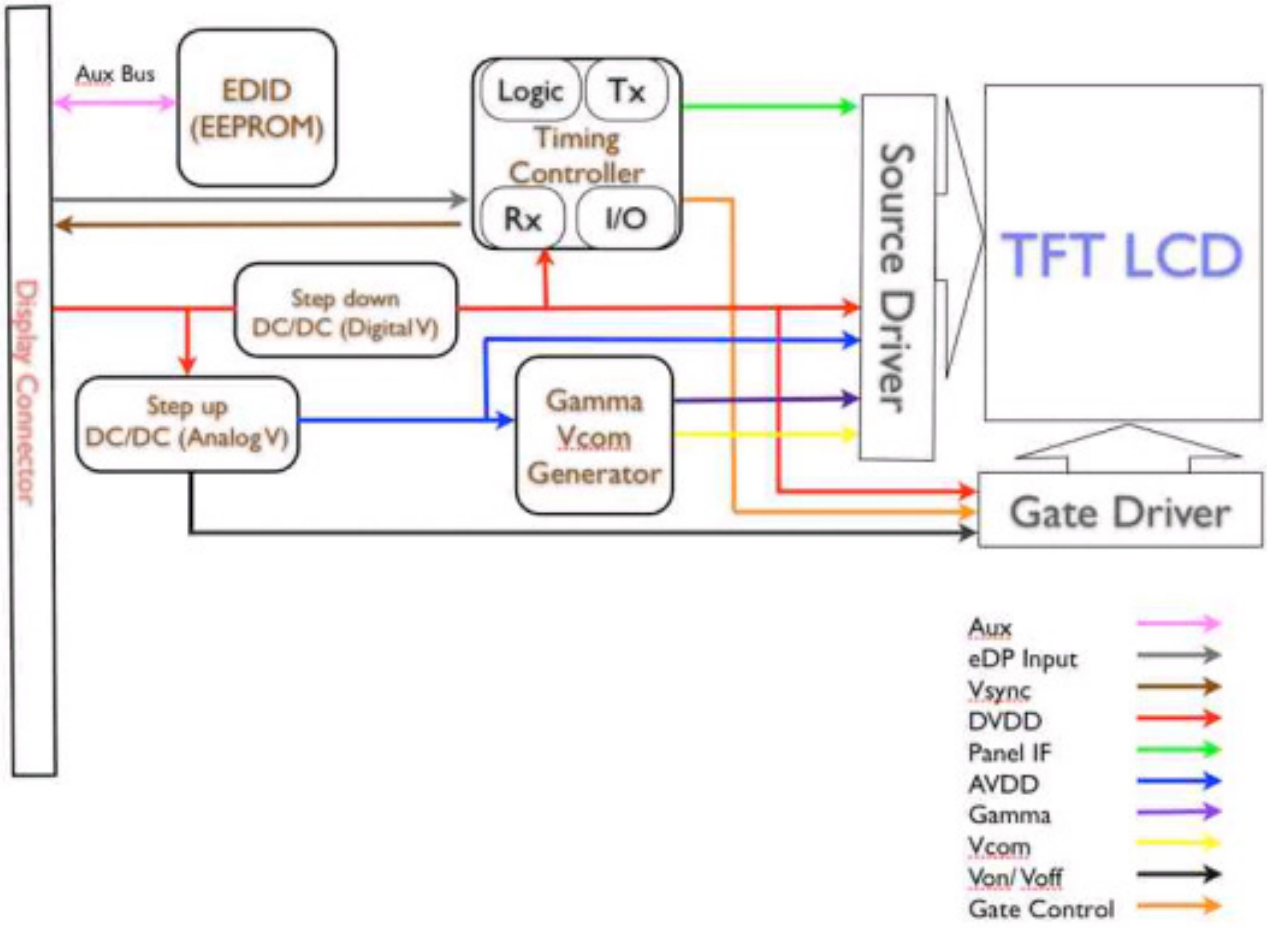
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 30 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

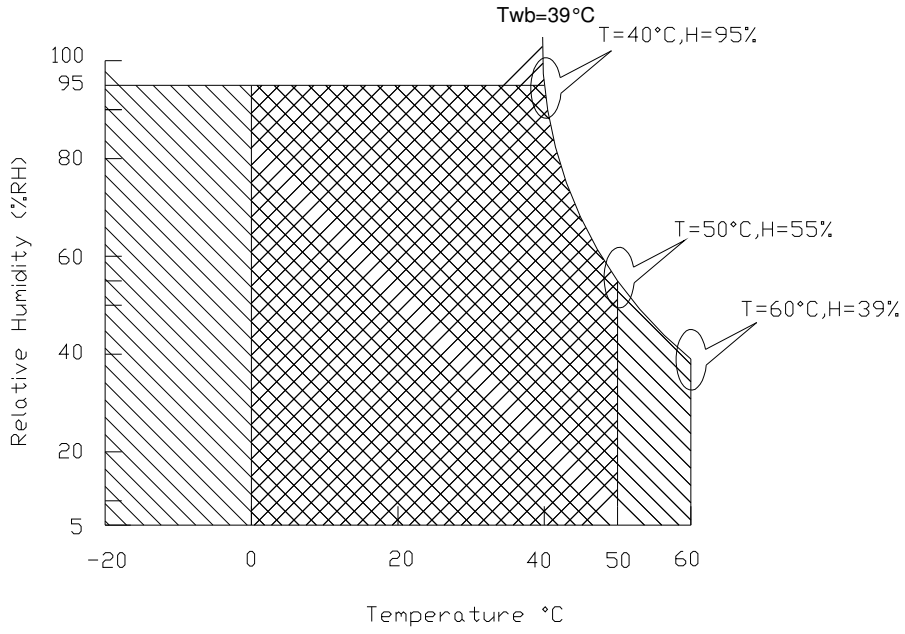
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

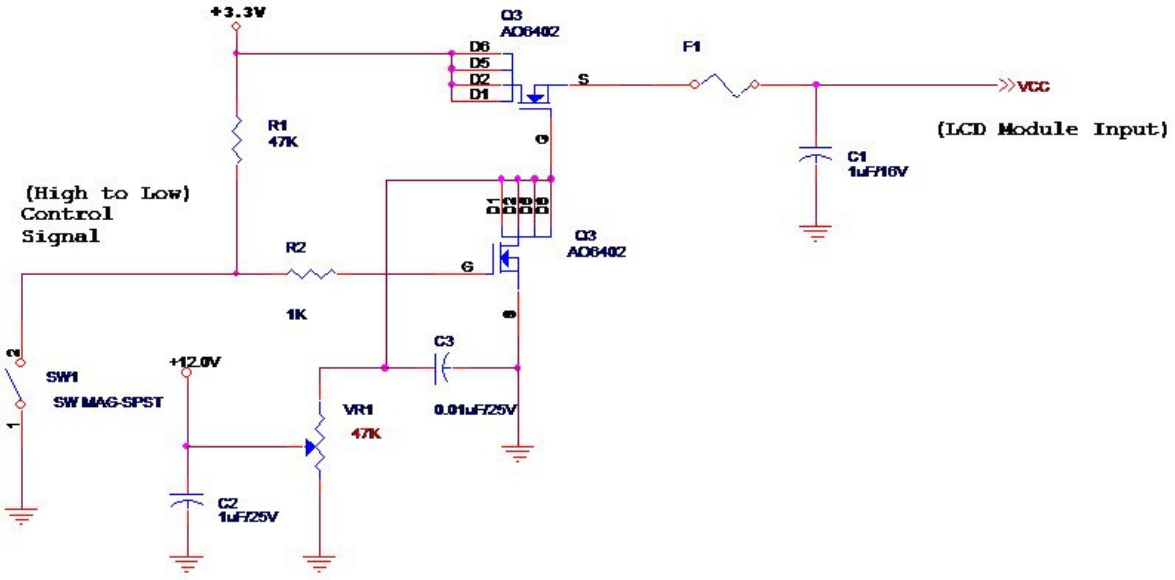
Input power specifications are as follows;

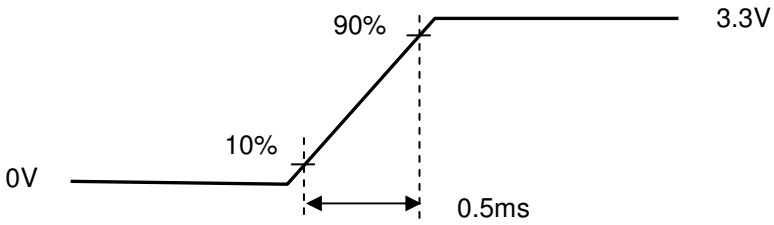
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symbol	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1	[Watt]	Note 1
IDD	IDD Current	-	-	333	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2 : Measure Condition



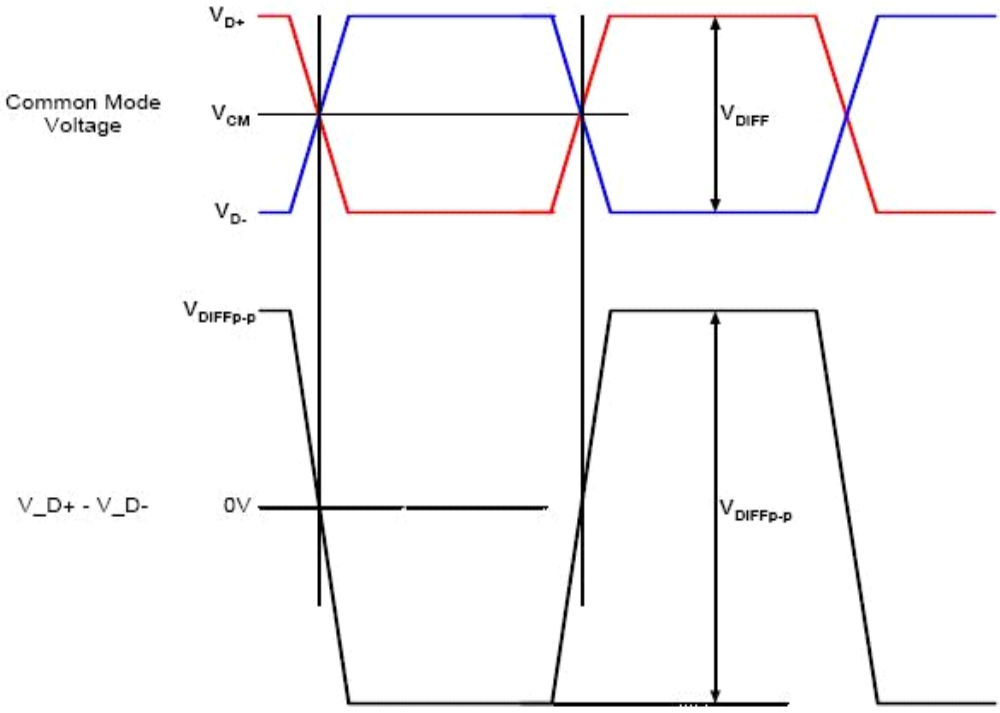


Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Display Port main link signal

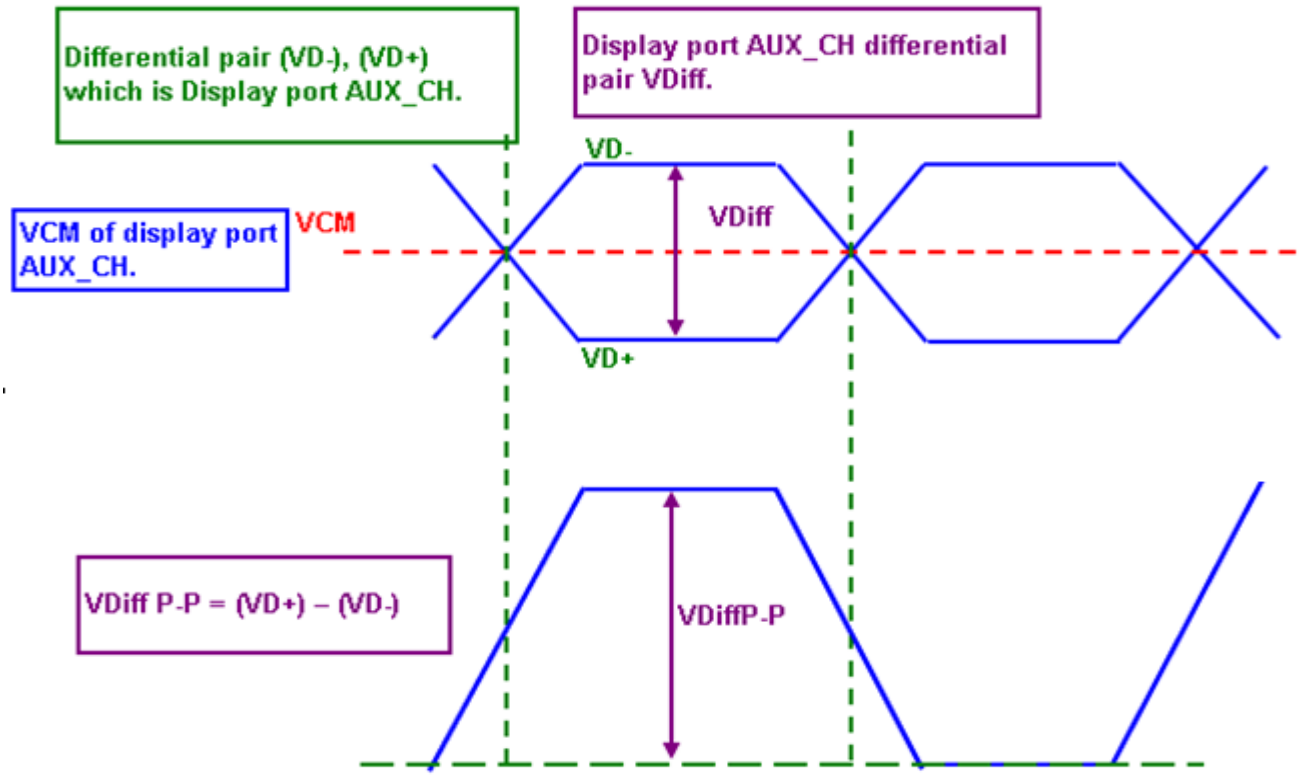


Display Port Main Link					
		Min	Typ	Max	Unit
V_{CM}	Differential common mode voltage	0	1.2 (1H301) 0.8 (PARADE) 1/2 VDD (IDT 1602/1604)	2	V
VDiffP-P level1	Differential peak to peak voltage level1	0.34	0.4	0.46	V
VDiffP-P level2	Differential peak to peak voltage level2	0.51	0.6	0.68	V
VDiffP-P level3	Differential peak to peak voltage level3	0.69	0.8	0.92	V
VDiffP-P level4	Differential peak to peak voltage level4	1.02	1.2	1.38	V

Remark: Reference VESA eDP standard

.

Display Port AUX_CH signal



Display Port AUX_CH					
		Min	Typ	Max	Unit
VCM	Differential common mode voltage	0	1.2 (1H301) 0.8 (PARADE) 1/2 VDD(IDT 1602/1604)	2	V
VDiff $_{P-P}$	Differential peak to peak voltage	0.39	-	1.38	V

Remark: Reference VESA eDP standard

Display Port V_{HPD} signal

Display Port AUX_CH					
		Min	Typ	Max	Unit
V_{HPD}	HPD Voltage	2.25	-	3.6	V

Remark: Reference VESA eDP standard

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
LED Life-Time	N/A	12,000	-	-	Hour	(Ta=25℃), Note 1 I_F=20 mA
LED Forward Voltage	V_F	2.8	-	3.0	V	I_F=20 mA
LED Reverse Current	I_R	-	-	2.0	μA	V_R=5 V

Note 1: The LED life-time define as the estimated time to 50% degradation of initial luminous.

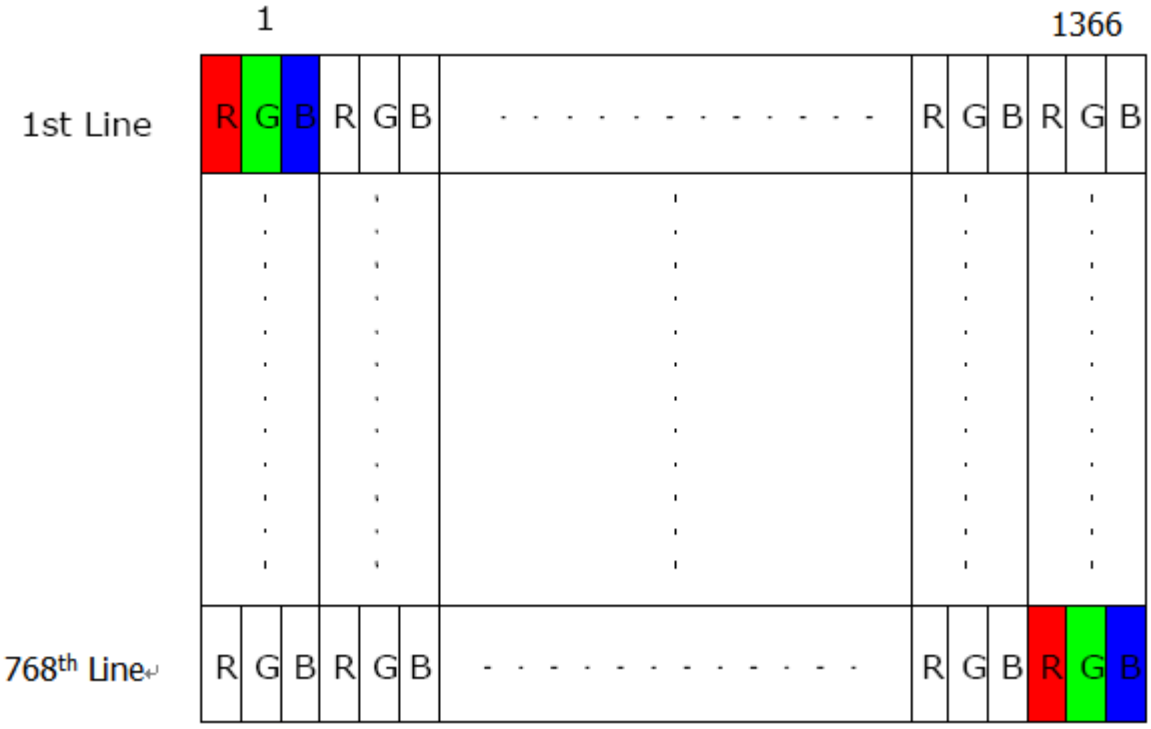
5.2.2 Suggested Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	900	-	1.1K	Hz	
PWM Duty Ratio	Duty	5	-	100	%	

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format

18bbp RGB Mapping to a One Lane Main Link

Lane 0
R0-5:0 | G0-5:4
G0-3:0 | B0-5:2
B0-1:0 | R1-5:0
G1-5:0 | B1-5:4
B1-3:0 | R2-5:2
R2-1:0 | G2-5:0
B2-5:0 | R3-5:4
R3-3:0 | G3-5:2
3-1:0 | B3-5:0

6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20525-030E-02 or compatible
Mating Housing/Part Number	IPEX 20523-030T-01 or compatible

6.3.2 Pin Assignment

Pin	Symbol	Description
1	NC-Reserved	NC – Reserved (I2C Data for LCD supplier)
2	NC	NC
3	Vdc(1 to 6)	LED Anode (Positive)
4	Vdc(1 to 6)	LED Anode (Positive)
5	NC	NC
6	Vdc6	LED Cathode (Negative)
7	Vdc5	LED Cathode (Negative)
8	Vdc4	LED Cathode (Negative)
9	Vdc3	LED Cathode (Negative)
10	Vdc2	LED Cathode (Negative)
11	Vdc1	LED Cathode (Negative)
12	Vsync	LED Sync Signal
13	FSS	Frame Sync Signal
14	HDP	Hot Plug Detect Signal Pin
15	LCD_GND	Ground
16	LCD_GND	Ground
17	LCD_Self_Test	LCD Panel Self Test
18	LCD_VCC	LCD logic & driver power
19	LCD_VCC	LCD logic & driver power
20	H_GND	High Speed Ground
21	AUX_CH_N	Complement Signal Aux Ch.
22	AUX_CH_P	True Signal Aux Ch.
23	H_GND	High Speed Ground
24	Lane0_P	True Signal Link 0
25	Lane0_N	Complement Signal Link 0
26	H_GND	High Speed Ground
27	Reserved (Lane1_P)	True Signal Link 1
28	Reserved (Lane1_N)	Complement Signal Link 1
29	H_GND	High Speed Ground
30	NC-Reserved	Reserved (I2C CLK for LCD supplier)

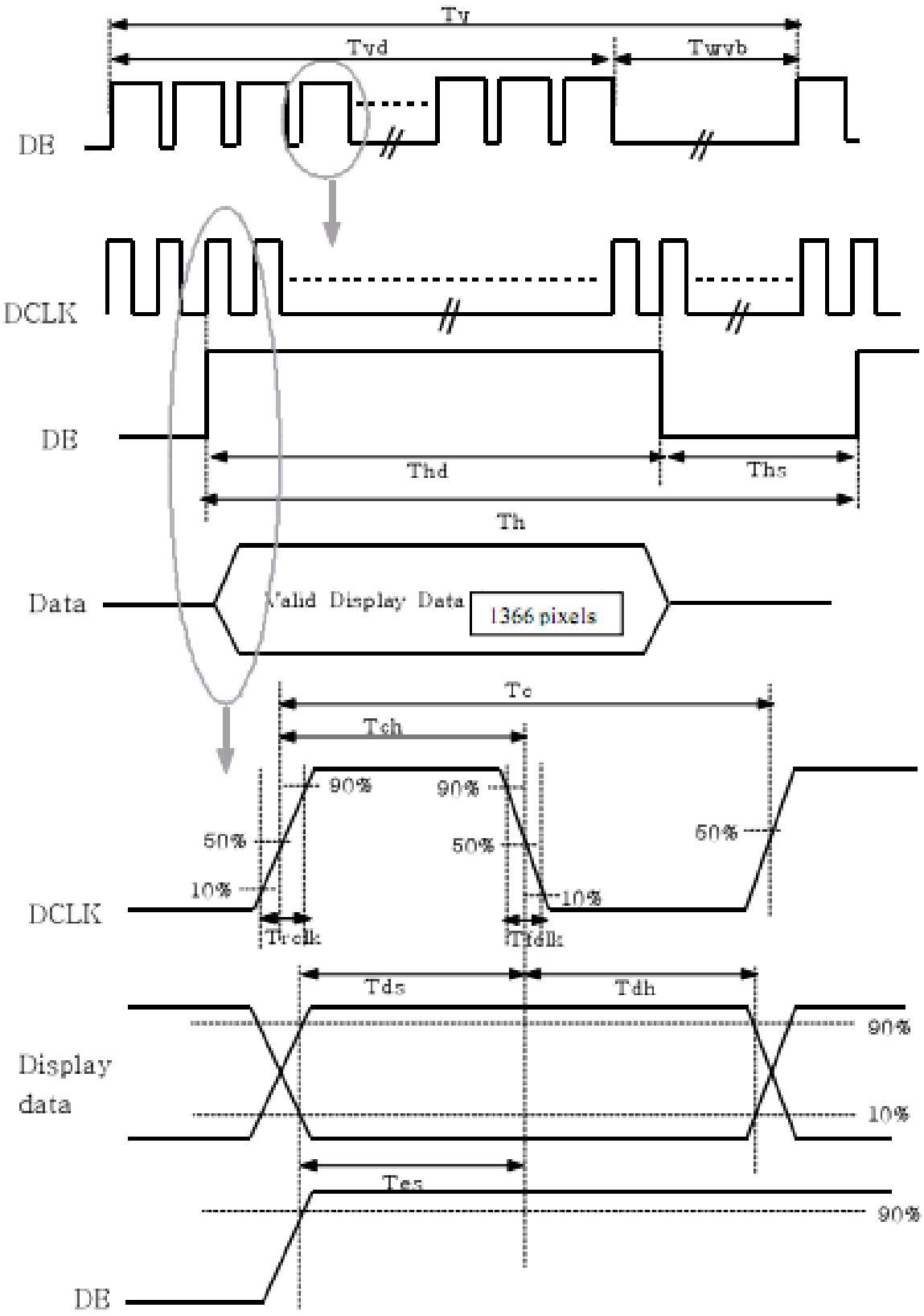
6.4 Interface Timing

6.4.1 Timing Characteristics

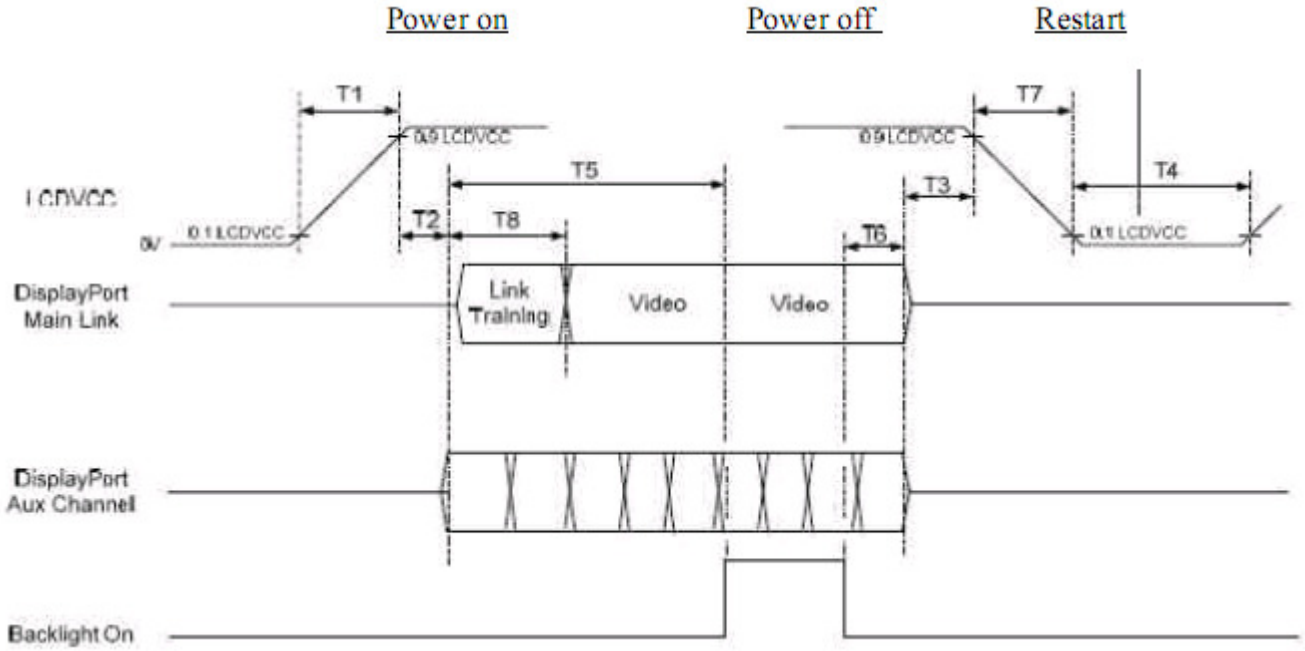
Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Signal	Parameter	Symbol	Min	Typ	Max	Unit	Note
D_{CLK}	Clock Period	T_C		13.89		ns	1
	Clock Frequency	f_C		72		MHz	$1/T_C$
	Duty Ratio (% High)	K_{dr}	40	50	60	%	T_{Ch}/T_C
	Rise Time	$T_{R\,CLK}$	-	4.42	-	ns	
	Fall Time	$T_{F\,CLK}$	-	4.42	-	ns	
DE	DE Setup Time	T_{se}	4	-	-	ns	
(Data Enable	Data Setup Time	T_{sd}	4	-	-	ns	
Only)	Data Hold Time	T_{hd}	2	-	-	ns	
(DTMG)	Horizontal Period	T_H		1500		T_C	2
Data	Horizontal Blank Period	T_{hb}		134		T_C	
	Vertical Period	T_V		800		T_H	f_V=59.90 Hz, 3
	Vertical Blank Period	T_{vb}		32		T_H	
H_{sync}	H_{sync} Back Porch	H_{bp}	48	64		T_C	
	H_{sync} Pulse Width	T_{wH}	24	54		T_C	
	H_{sync} Front Porch	H_{fp}	8	14		T_C	

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence



Parameter	Limit Values		Units	Description
	Min	Max		
T1	0.5	10	ms	Power rail rise time 10% to 90%
T2	0	50	ms	Delay from power on to Sink Aux Channel response ready (note 1)
T3	0	50	ms	Delay from Main Link activity to power off
T4	500	-	ms	Power off time
T5	200	-	ms	Delay from Main Link enable to backlight enable
T6	200	-	ms	Delay from backlight disable to Main Link disable
T7	-	10	ms	Power rail fall time 90% to 10%
T8	-	10	ms	Link training duration, active video enabled by the end of this period

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

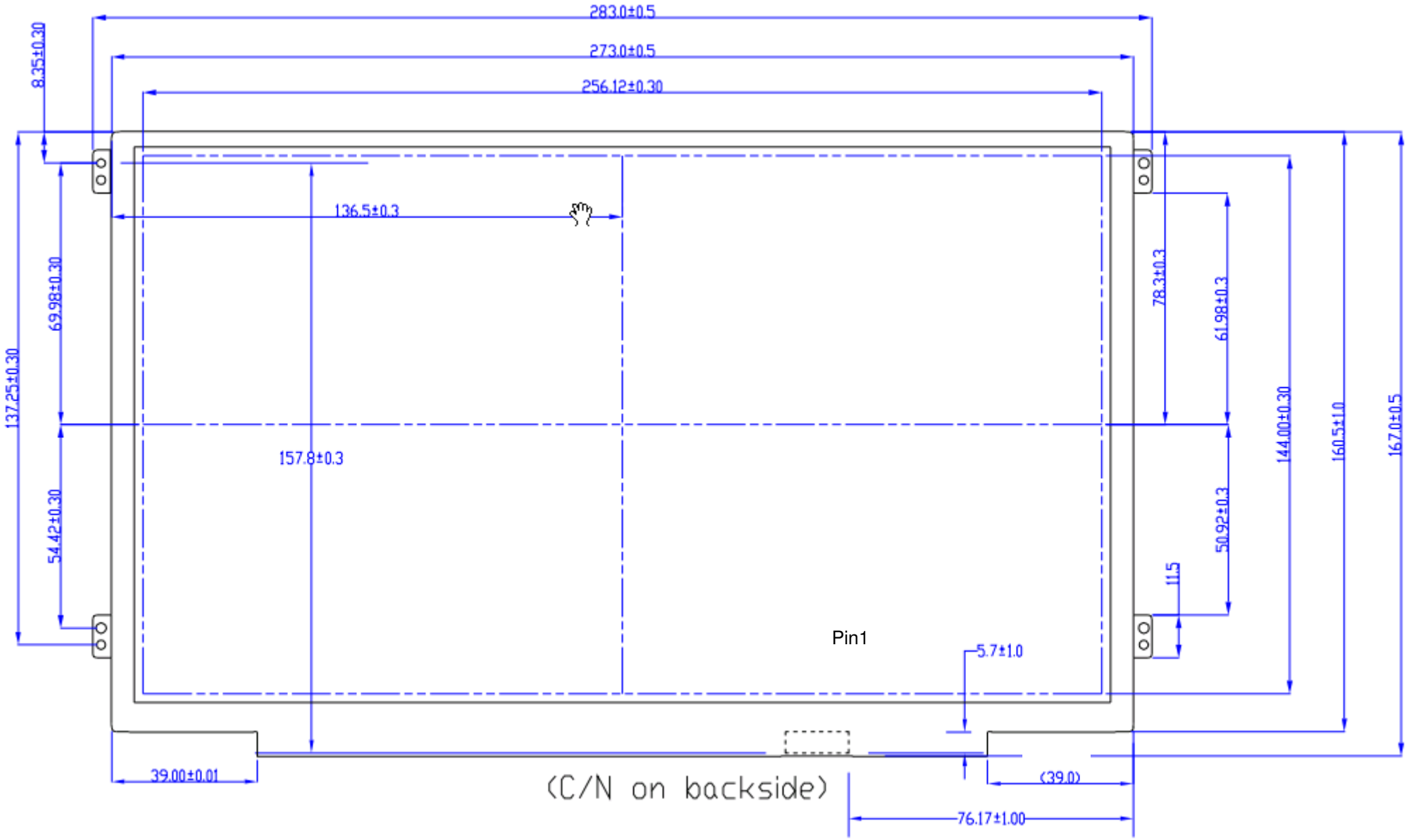
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension



9. Shipping and Package

9.1 Shipping Label Format

9.2 Carton Package

TBD.

9.3 Shipping Package of Palletizing Sequence

TBD.

10. Appendix: EDID Description

Address	FUNCTION	B116XW05 V001	Note
HEX	Header	HEX	
00		00	
01		FF	
02		FF	
03		FF	
04		FF	
05		FF	
06		FF	
07		00	
08	EISA Manuf. Code LSB	06	
09	Compressed ASCII	10	
0A	Product Code	F4	
0B	hex, LSB first	9C	
0C	32-bit ser #	01	unused
0D		01	
0E		01	
0F		01	
10	Week of manufacture	01	Week
11	Year of manufacture	14	20(2010-1990=20)
12	EDID Structure Ver.	01	
13	EDID revision #	03	
14	Video input definition	80	Digital Input
15	Max H image size	1A	25.6cm
16	Max V image size	0E	14.4cm
17	Display Gamma	78	Gamma 2.2
18	Feature support	0A	no DPMS,Active off,RGB color
19	Red/green low bits	50	
1A	Blue/white low bits	C5	
1B	Red x/ high bits	98	
1C	Red y	58	

1D	Green x	52	
1E	Green y	8E	
1F	Blue x	27	
20	Blue y	25	
21	White x	50	
22	White y	54	
23	Established timing 1	00	unused
24	Established timing 2	00	.
25	Manufacturer's Timing	00	
26	Standard timing #1	01	unused
27		01	
28	Standard timing #2	01	
29		01	
2A	Standard timing #3	01	
2B		01	
2C	Standard timing #4	01	
2D		01	
2E	Standard timing #5	01	
2F		01	
30	Standard timing #6	01	
31		01	
32	Standard timing #7	01	
33		01	
34	Standard timing #8	01	
35		01	
36	Pixel Clock/10,000 (LSB)	20	Timing Descriptor #1
37	Pixel Clock/10,000 (MSB)	1C	1366x768 @60_mode:pixel clock=72MHz
38	Horiz. Active pixels(Lower 8 bits)	56	Horiz active=1366 pixels
39	Horiz.Blanking (Lower 8 bits)	88	Horiz blanking=768 pixels
3A	Horiz. Active pixels:Horiz. Blanking (Upper4:4 bits)	50	
3B		00	
3C		20	
3D	Vert. Active pixels:Vert. Blanking (Upper4:4 bits)	30	
3E		E	Horiz sync. Offset=56 pixels
3F		38	Horiz sync. Pulse Width=56 pixels
40	Vert. Sync. Offset=xx lines, Sync Width=xx lines	13	Verti sync. Offset=1 lines,Sync Width=3 lines

41	Horz. Ver. Sync/Width (upper 2 bits)	00	
42	Hori. Image size (Lower 8 bits)	00	Hori image size= 256.125 mm
43	Vert. Image size (Lower 8 bits)	90	Verti image size = 144mm
44	Hori. Image size : Vert. Image size (Upper 4 bits)	10	
45		00	Horizontal Border = 0
46		00	Vertical Border = 0
47		18	
48	Detailed timing/monitor	00	
49	descriptor #2	00	
4A		00	
4B		01	
4C	Version	00	
4D	Apple edid signature	06	
4E	Apple edid signature	10	
4F	Link Type (LVDS Link,MSB justified)	30	
50	Pixel and link component format (6-bit panel interface)	00	
51	Panel features (No inverter)	00	
52		00	
53		00	
54		00	
55		00	
56		00	
57		00	
58		0A	
59		20	
5A	Detailed timing/monitor	00	
5B	descriptor #3	00	
5C		00	
5D		FE	
5E		00	
5F		42	B
60		31	1
61		31	1
62		36	6

63		58	X
64		57	W
65		30	0
66		35	5
67		20	
68		56	V
69		30	0
6A		0A	
6B		20	
6C	Detailed timing/monitor	00	Monitor Name: Color LCD
6D	descriptor #4	00	
6E		00	
6F		FE	
70		00	
71		43	C
72		6F	o
73		6C	l
74		6F	o
75		72	r
76		20	
77		4C	L
78		43	C
79		44	D
7A		0A	
7B		20	
7C		20	
7D		20	
7E	Extension Flag	00	
7F	Checksum	E4	