CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A070STN01.3**
CUSTOMER APPROVED	**Title :** **Name :**

- ☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.0)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.0.0)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver. 0.0)**
- ☐ **CUSTOMER REMARK :**

AUO PM : Mio Li

P/N : 91.07A24.300

Comment :

Doc. version :	0.0
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Date : 2012/01/10

Product Specification

7" COLOR TFT-LCD MODULE

MODEL NAME: A070STN01.2

Model Name：	A070STN01.2
Planned Lifetime:	From 2012/Mar To 2013/June
Phase-out Control:	From 2012/Jan To 2013/June
EOL Schedule:	2013/June

< □ >Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2012/01/10	All	First Draft.

Contents

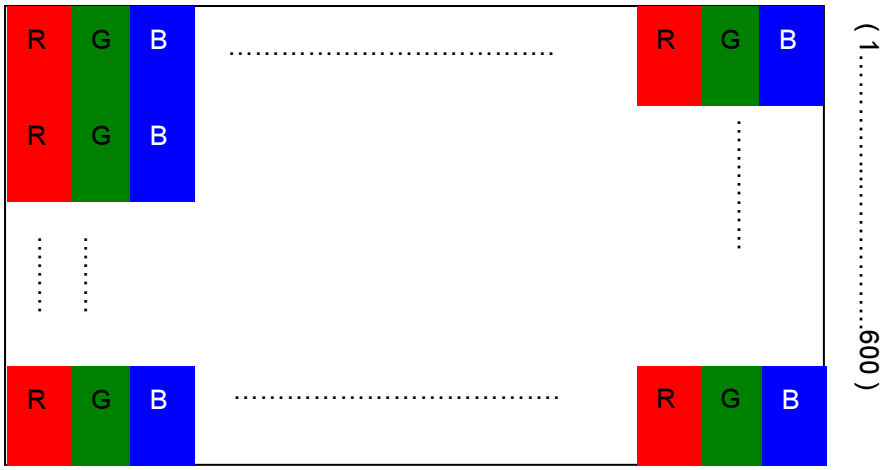
A. General Information

This product is for car after-market. digital photo frame and other suitable application.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	7(Diagonal)	
2	Display Resolution	dot	1024RGB(W)x600(H)	
3	Overall Dimension	mm	161.78(W) x 101.20(H)x 1.23(T)	Note 1
4	Active Area	mm	153.6(W) x 90.0(H)	
5	Pixel Pitch	mm	0.150(W)x0.150(H)	
6	Color Configuration	--	R. G. B. Stripe	Note 2
7	Color Depth	--	16.2M Colors	Note 3
8	NTSC Ratio	%	45	
9	Display Mode	--	Normally White	
10	Panel surface Treatment	--	Anti-Glare, 3H	
11	Weight	g	42	
12	Panel Power Consumption	mW	TBD	Note 4
13	Backlight Power Consumption	W	-	
	Viewing direction		6 o'clock	

Note 1: Not include FPC. Refer next page to get further information.

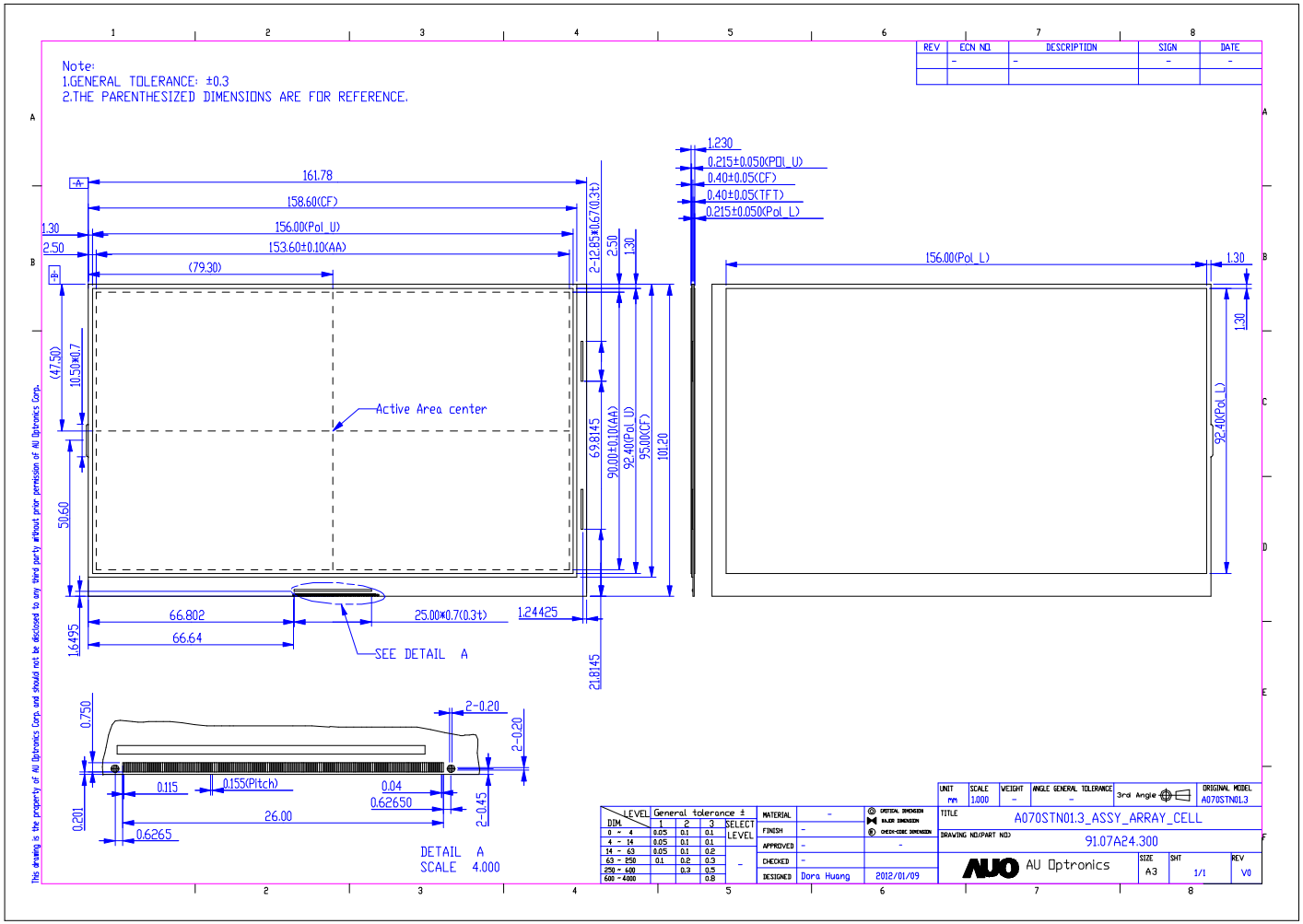
Note 2: Below figure shows dot stripe arrangement.



Note 3: Please refer to Electrical Characteristics chapter.

B. Outline Dimension

1. TFT-LCD Module – Front & Rear View



C. Electrical Specifications

1. TFT LCD Panel Pin Assignment

Pin NO	Pin Name	Description
1	DUMMY(1)	NC
2	VCOM(2)	VCOM To Cell
3		
4	VCOMO(2)	VCOM buffer out
5		
6	NC	NC
7		
8	AVDDG(2)	AVDD regulate output
9		
10	NC	NC
11		
12	PWR_EN(1)	POWER enable. Normally pull low PWR_EN = H , enable PWM , Charge pump and VCOM buffer PWR_EN = L , disable PWM , Charge pump and VCOM buffer
13	VCOMI(2)	VCOM buffer in
14		
15	AGND(3)	Ground pins for analog circuits
16		
17		
18	AVDD(3)	Power supply for analog circuits
19		
20		
21	GND(3)	Ground pins for digital circuits
22		
23		
24	VDD(3)	Power supply for digital circuits
25		
26		
27	UPDN(1)	Gate Up or Down scan control. Normally pull low. UPDN = “L”, UP to DOWN UPDN = “H”, DOWN to UP
28	SHLR(1)	Source Right or Left sequence control. Normally pull high. SHLR = “L”, shift left SHLR = “H”, shift right
29	GRB(1)	Global reset pin. Active Low to enter Reset State. Normally pull high.

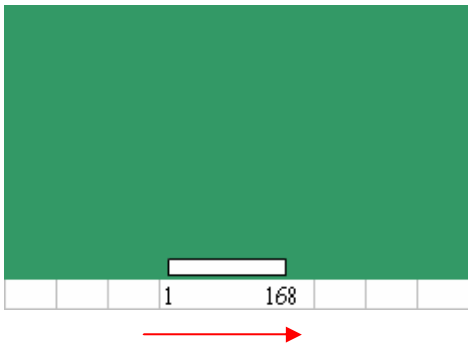
30	STBYB(1)	Standby mode, Normally pulled high. STBYB = “1”, normal operation STBYB = “0”, timing controller, source driver will turn off, all output are High-Z
31	RES1(1)	Connect to GND
32	RES0(1)	Connect to GND
33	BIST(1)	Normal Operation/BIST pattern select. Normally pull low BIST = H : BIST(DCLK input is not needed) BIST = L : Normal Operation
34	IFSEL(1)	Connect to VDD
35	MODE(1)	DE / SYNC mode select under TTL mode. H : DE mode. L : HSD/VSD mode.
36	OPDRV(1)	Source OP driving selection. Normally pull low OPDRV = H : 133% OPDRV = L : normal
37	CABC_EN[1](1)	CABC H/W enable pin. Normally pull low. When CABC_EN=”00”, CABC OFF. (Default mode) When CABC_EN=”01”, User interface Image. When CABC_EN=”10”, Still Picture. When CABC_EN=”11”, Moving Image.
38	CABC_EN[0](1)	
39	MASLOC(1)	Connect to GND
40	MASL(1)	Connect to VDD
41	DUAL(1)	Connect to VDD
42	VDD(4)	Power supply for digital circuits
43		
44		
45		
46	GND(4)	Ground pins for digital circuits
47		
48		
49		
50	AVDD(4)	Power supply for analog circuits
51		
52		
53		
54	AGND(4)	Ground pins for analog circuits (Pin 54~ 57)
55		
56		

57		
58	V14(2)	When INTERNAL Gamma Table is used GAMH tied to AVDDG via resistor for PWR_EN= H , enable PWM or tied to AVDD for PWR_EN = L , disable PWM GAML tied to GND and V1~V14 pad are un-used. When using external gamma voltage, GAMH and GAML are floaging , and V1~V14 the external gamma correction points. The voltage of these pins must be: AGND<V14<V13<V12<V11<V10<V9<V8;V7<V6<V5<V4<V3<V2<V1<AVDD .
59		
60	V13(2)	
61		
62	V12(2)	
63		
64	V11(2)	
65		
66	V10(2)	
67		
68	V9(2)	
69		
70	V8(2)	
71		
72	GAML(2)	When using INTERNAL Gamma Table , tied to GND . Otherwise floating.
73		
74	GND(4)	Ground pins for digital circuits
75		
76		
77		
78	VDD_LVDS(4)	LVDS power
79		
80		
81		
82	NINC	Negative LVDS differential clock input.
83	DCLK	Positive LVDS differential clock input.
84	RXIN0-	LVDS differential signal
85	RXIN0+	LVDS differential signal
86	RXIN1-	LVDS differential signal
87	RXIN1+	LVDS differential signal
88	RXIN2-	LVDS differential signal
89	RXIN2+	LVDS differential signal
90	RXIN3-	LVDS differential signal
91	RXIN3+	LVDS differential signal
92	GND_LVDS(4)	LVDS ground (Pin 92~95)
93		

94		
95		
96	DEN	Connect to GND
97	HSD	Used as 6-bit/8-bit input select HSD = L , 8-bit HSD = H , 6-bit
98	VSD	Connect to GND
99	GAMH(2)	When INTERNAL Gamma Table is used GAMH tied to AVDDG via resistor for PWR_EN= H , enable PWM or tied to AVDD for PWR_EN = L , disable PWM. Otherwise floating.
100		
101	V7(2)	When INTERNAL Gamma Table is used GAMH tied to AVDDG via resistor for PWR_EN= H , enable PWM or tied to AVDD for PWR_EN = L , disable PWM GAML tied to GND and V1~V14 pad are un-used. When using external gamma voltage, GAMH and GAML are floaging , and V1~V14 the external gamma correction points. The voltage of these pins must be: AGND<V14<V13<V12<V11<V10<V9<V8;V7<V6<V5<V4<V3<V2<V1<AVDD .
102		
103	V6(2)	
104		
105	V5(2)	
106		
107	V4(2)	
108		
109	V3(2)	
110		
111	V2(2)	
112		
113	V1(2)	
114		
115	AGND(4)	Ground pins for analog circuits
116		
117		
118		
119	AVDD(4)	Power supply for analog circuits
120		
121		
122		
123	GND(4)	Ground pins for digital circuits
124		
125		
126		
127	VDD(4)	Power supply for digital circuits (Pin 127 ~ 130)

<table>
<tr><td>128
129
130</td><td></td><td></td></tr>
<tr><td>131</td><td>SCL(1)</td><td>Serial communication clock input. Normally pull low</td></tr>
<tr><td>132</td><td>SDA(1)</td><td>Serial communication data input. Normally pull low</td></tr>
<tr><td>133</td><td>CSB(1)</td><td>Serial communication chip select. Normally pull low</td></tr>
<tr><td>134</td><td>SEL[1](1)</td><td rowspan="2">Gate on sequence select. Normally pull low
<table><tr><th>SEL[0]</th><th>SEL[1]</th><th>Pin control function</th></tr><tr><td>1</td><td>1</td><td>Z+ 2</td></tr><tr><td>1</td><td>0</td><td>2</td></tr><tr><td>0</td><td>1</td><td>≦</td></tr><tr><td>0</td><td>0</td><td>Z</td></tr></table></td></tr>
<tr><td>135</td><td>SEL[0](1)</td></tr>
<tr><td>136</td><td>FRAME(1)</td><td>Frame inverse or not select. Normally pulled low
FRAME = “1”, Uniform
FRAME = “0”, Frame inverse (Default)</td></tr>
<tr><td>137</td><td>HFRC(1)</td><td>H-FRC selection. Normally pull low
HFRC = H : H-FRC enable
HFRC = L : H-FRC disable
If DITHER = “0” , disable dithering function(H-FRC and FRC disable)</td></tr>
<tr><td>138</td><td>DITHER(1)</td><td>Dithering function enable control. Normally pull low.
In LVDS 6-bit mode , IC don’t care DITHER and HFRC setting.
DITHER = “1”, Enable internal dithering function
DITHER = “0”, Disable internal dithering function.</td></tr>
<tr><td>139</td><td>DIMO(1)</td><td>Backlight dimmer signal for external controller.
DIMO = “0”, Turn off external backlight controller
DIMO = “1”, Logical control signal to turn on external backlight controller
NOTE : If CABC OFF , DIMO = DIMI . Else DIMO is controlled by CABC</td></tr>
<tr><td>140</td><td>PINCTL(1)</td><td>Enable pin control function. Normally pull high
PINCTL=”0”, Disable pin control function and enable 3-wire control register.
Following pin setting will be inactive:
MODE, RES[1:0], DITHER, HFRC, DCLKPOL, SHLR, UPDN, BIST,NBW, FRAME, SEL[1:0], CABC_EN[1:0], OPDRV, PWR_EN
PINCTL=”1”, Enable pin control function.
NOTE: The related 3-wire control register bit control will be disabled under PINCTL=”1”.</td></tr>
</table>

141	NBW(1)	Normally black or normally white setting. Normally pulled low. NBW = H : Normally black NBW = L : Normally white
142	DIMI(1)	Brightness control signal. Normally pull high
143	VDD(3)	Power supply for digital circuits
144		
145		
146	GND(4)	Ground pins for digital circuits
147		
148		
149		
150	AVDD(4)	Power supply for analog circuits
151		
152		
153		
154	AGND(4)	Ground pins for analog circuits
155		
156		
157		
158	VCOM(2)	VCOM To Cell
159		
160	VGG(2)	VGH Voltage
161		
162	VEE(2)	VGL Voltage
163		
164	VDD(2)	Power supply for digital circuits
165		
166	GND(2)	Ground pins for digital circuits
167		
168	DUMMY(1)	NC



2. Backlight Pin Assignment

N/A

3. Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VDDIO	GND=0	-0.5	5	V	
	AVDD	GND=0	-0.5	15	V	
	VGH	GND=0	-0.3	42	V	
	VGL	GND=0	-20	0.3	V	
Operating Temperature	Topa		-20	85	℃	
Storage temperature	Tstg		-55	125	℃	

Note 1:De, Digital Data

Note 2:Functional operation should be restricted under ambient temperature (25℃).

Note 3:Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

4. Electrical DC Characteristics

a. (VCC = +3.3V, AVDD = 12V, AGND=GND=0V)

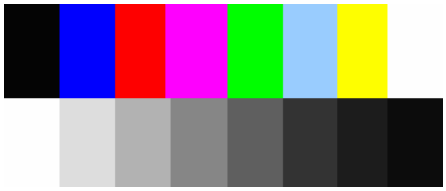
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Voltage		VCC	3.0	3.3	3.6	V	Digital power
		VDPA	10	11	13.5	V	Analog Power
		VGH	17	18	19	V	Positive power supply for gate driver
		VGL	-12.5	-12	-11.5	V	Negative power supply for gate driver
Input Signal Voltage	H Level	VIH	VDDx0.7	-	VDD	V	Note 1
	L Level	VIL	GND	-	0.3xVDD	V	
VCOM voltage		VCOM				V	

Note 1: DE , Digigal Data

b. Current Consumption (AGND=GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input current for VDD	I_{VDD}	VDD=3.3V		TBD		mA	Note 1
Inpur current for AVDD	I_{AVDD}	AVDD=11V		TBD		mA	Note 1
Inpur current for VGH	I_{VGH}	VGH=18V		TBD		mA	Note 1
Inpur current for VGL	I_{VGL}	VGL= -12V		TBD		mA	Note 1
Inpur current for VCOM	I_{VCOM}	VCOM=TBD		TBD		mA	Note 1

Note 1: The test pattern use the following pattern.



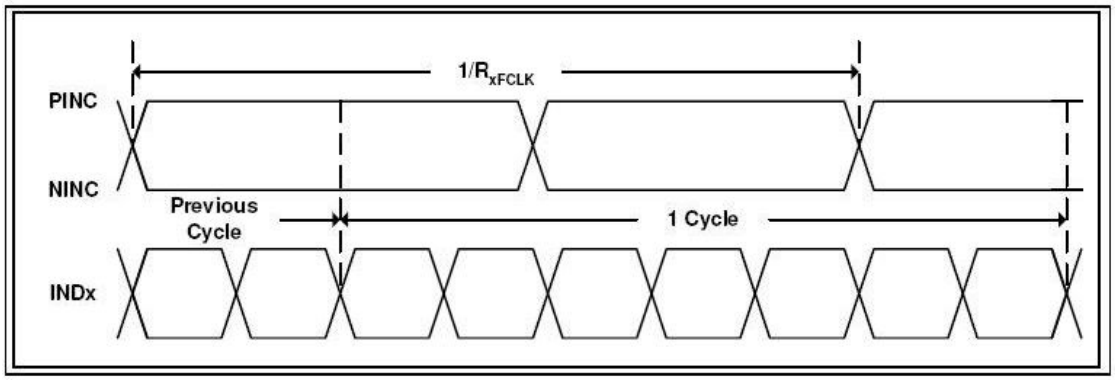
c. Backlight Driving Conditions

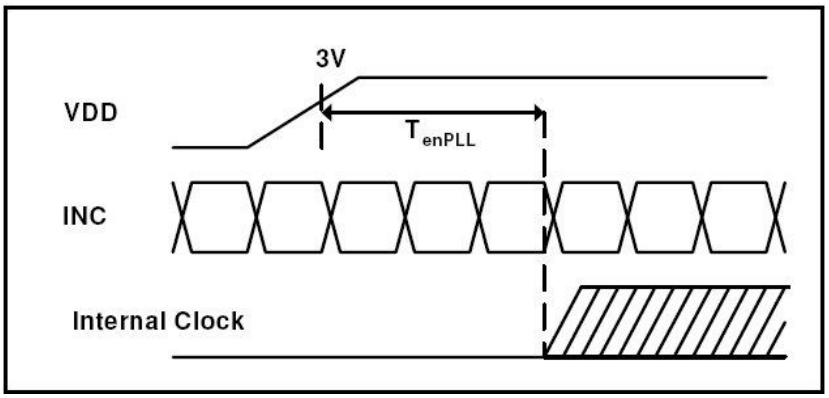
N/A

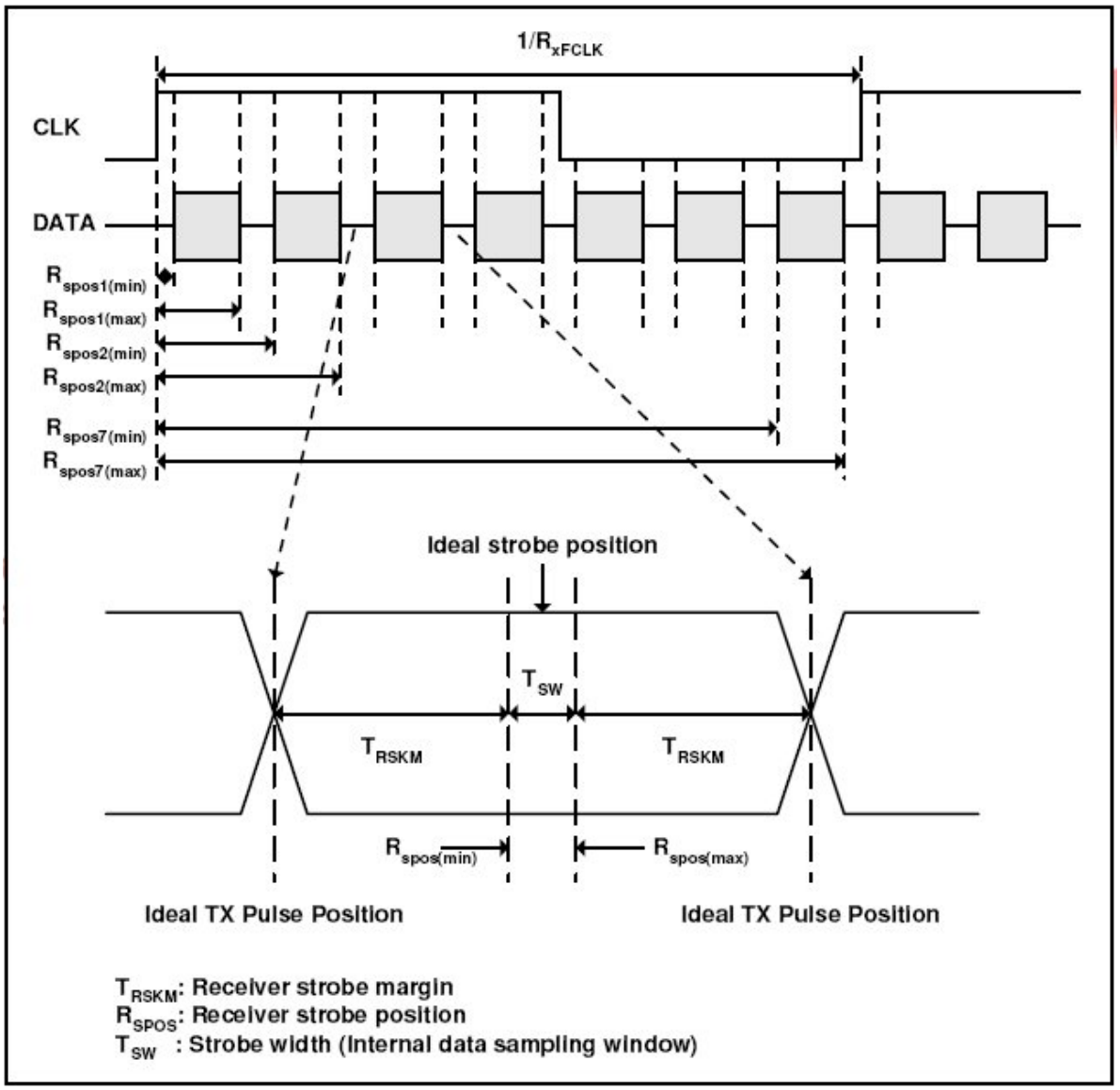
5. Electrical AC Characteristics

a. Signal AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency	R_{xFCLK}	20		71	MHz	
Input data skew margin	T_{RSKM}	500			pS	$\|V_{ID}\|$ = 400mV R_{xVCM} = 1.2V R_{xFCLK} = 71 MHz
Clock high time	T_{LVCH}		$4/(7* R_{xFCLK})$		ns	
Clock low time	T_{LVCL}		$3/(7* R_{xFCLK})$		ns	
PLL wake-up time	T_{enPLL}			150	uS	



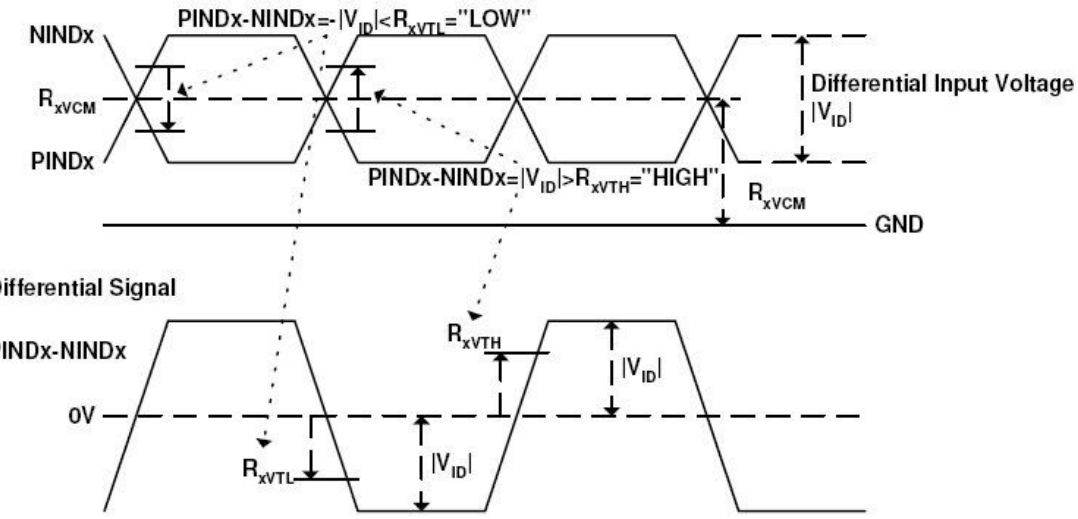




b. Signal DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential input high threshold voltage	R_{xVTH}			+0.1	V	R_{xVCM} =1.2V
Differential input low threshold voltage	R_{xVTL}	-0.1			V	
Input voltage range (singled-end)	R_{xVIN}	0		2.4	V	
Differential input common mode voltage	R_{xVCM}	$\|V_{ID}\|/2$		2.4-$\|V_{ID}\|/2$	V	
Differential input voltage	$\|V_{ID}\|$	0.2		0.6	V	
Differential input leakage current	RV_{xliz}	-10		+10	µA	
LVDS Digital Operating Current	Iddlvds	-	40	50	mA	Fclk=65 MHz, VDD=3.3V
LVDS Digital Stand-by Current	Istlvds	-	10	50	µA	Clock & all Functions are stopped

Single-end Signals

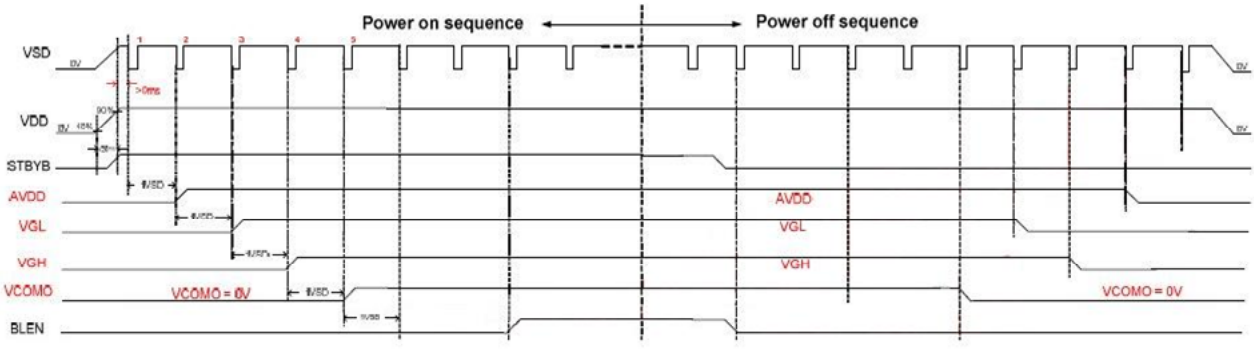


Differential Signal

6. Serial Interface Characteristics

N/A

7. Power On/Off Characteristics



8. Content-based Automatic Backlight Control (CABC) reference circuit

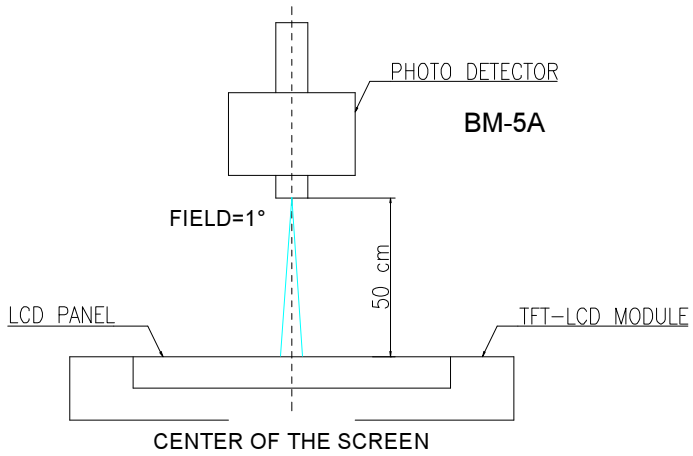
N/A

D. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall	 Tr Tf	 θ=0°	 -- --	 3 6	 6 12	 ms ms	Note 2
Contrast ratio	CR	At optimized viewing angle	600	800	--		Note 3
Viewing Angle Top Bottom Left Right		CR≧10	 55 60 60 60	 70 75 75 75		deg.	Note 4
Brightness	Y_L	θ=0°			--	cd/m^2	Note 5

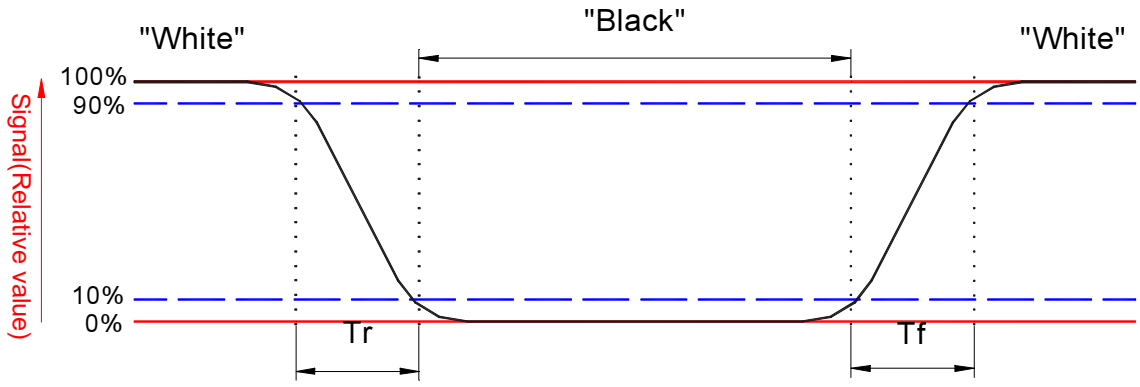
Note 1: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.



Note 2: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

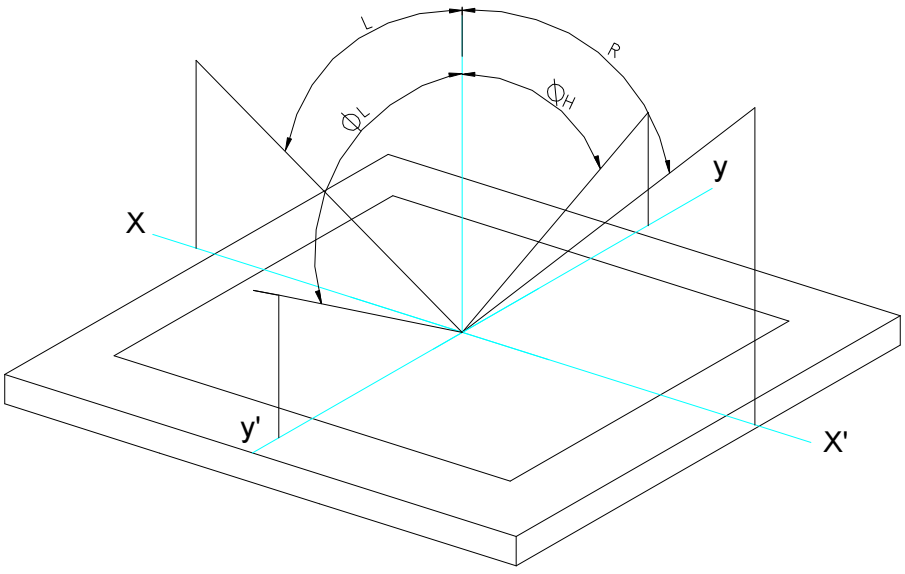


Note 3.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 4. Definition of viewing angle, θ, Refer to figure as below.



Note 5. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

E. Reliability Test Items

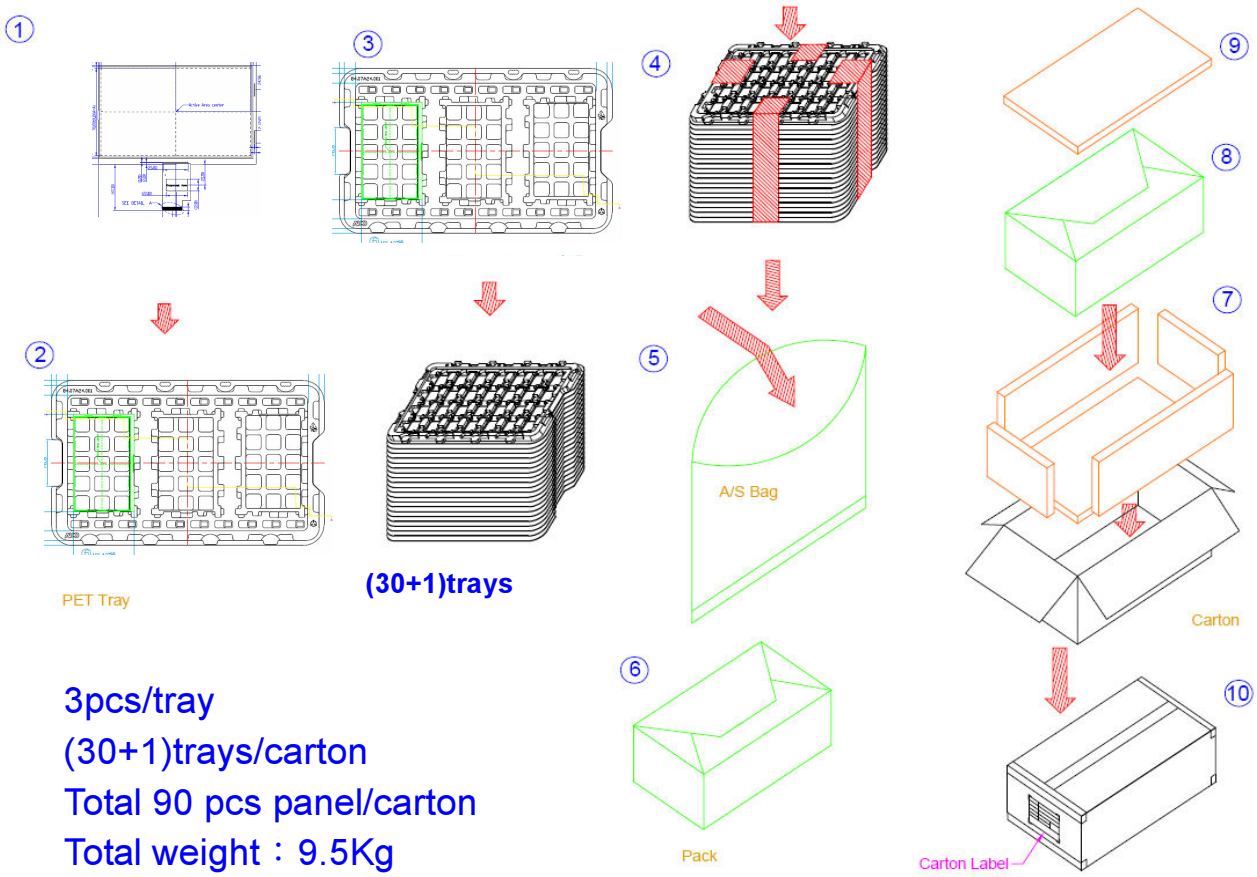
No.	Test items	Conditions		Remark
1	High Temperature Storage	Ta= 70□	240Hrs	
2	Low Temperature Storage	Ta= -30□	240Hrs	
3	High Ttemperature Operation	Tp= 60□	240Hrs	
4	Low Temperature Operation	Ta= -20□	240Hrs	
5	High Temperature & High Humidity	Tp= 40□. 90% RH	240Hrs	Operation
6	Heat Shock	-30□~70□, 100 cycle,	1Hrs/cycle	Non-operation

Note 1: Ta: Ambient Temperature. Tp: Panel Surface Temperature

Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

F. Packing and Marking

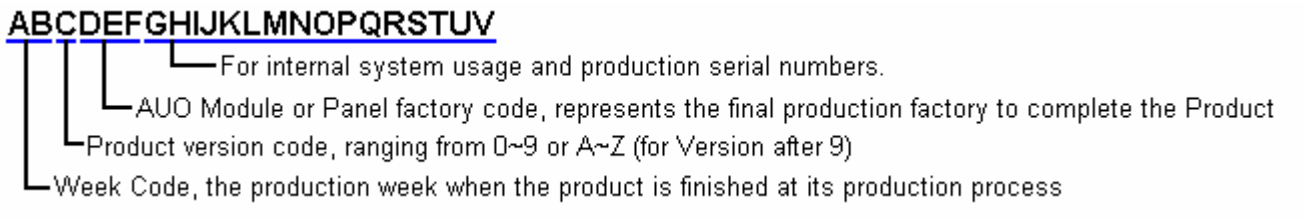
1. Packing Form



3pcs/tray
(30+1)trays/carton
Total 90 pcs panel/carton
Total weight：9.5Kg

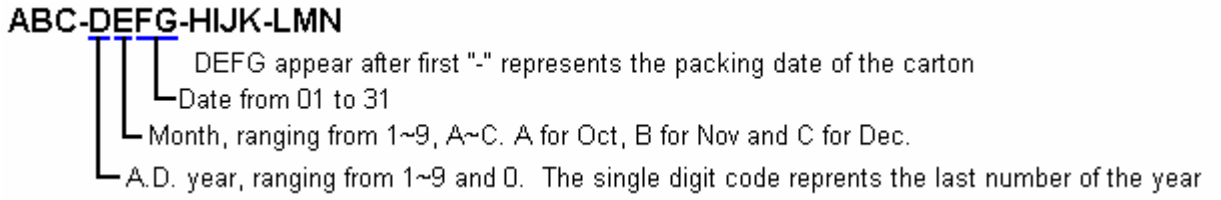
2. Module/Panel Label Information

The module/panel (collectively called as the “Product”) will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for detailed location and size of the label. The label is composed of a 22-digit serial number and printed with code 39/128 with the following definition:



3. Carton Label Information

The packing carton will be attached with a carton label where packing Q’ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:



Refer to the drawing of packing format for the location and size of the carton label.

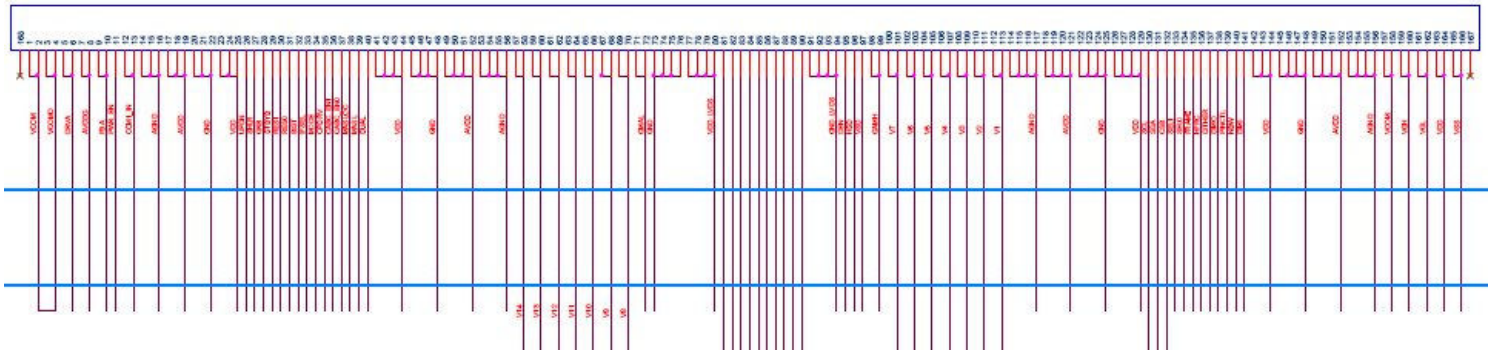
G. Reference application circuit

1.Recomonded Gamma Voltage

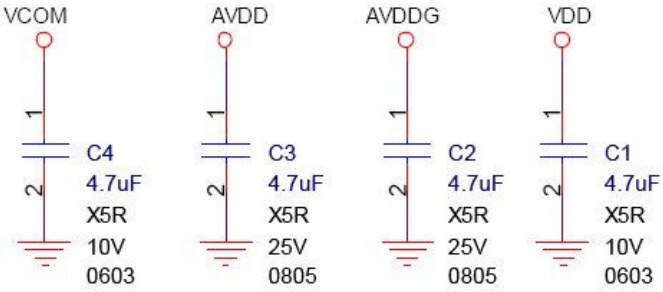
TBD

2.Application Circuit

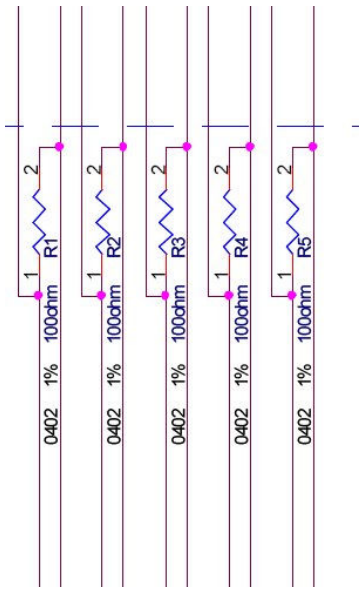
a.Cell pin



b.Power



c.LVDS signal bus



H. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.