



Product Specification

E133HVN-801

☐ Preliminary Specifications

☒ Final Specifications



Module	13.3" High Brightness FHD Color TFT-LCD
Model Name	E133HVN-801
Document Version	Rev.01

Customer

Approved by

Date

Notice: This Specification is subject to change without notice.

Approved By	Prepared By
	



Product Specification

E133HVN-801

CONTENTS

1	GENERAL DESCRIPTION	4
1.1	OVERVIEW	4
1.2	GENERAL SPECIFICATIONS	4
2	MECHANICAL SPECIFICATIONS	5
2.1	CONNECTOR TYPE	5
3	ABSOLUTE MAXIMUM RATINGS	6
3.1	ABSOLUTE RATINGS OF ENVIRONMENT	6
3.2	ELECTRICAL ABSOLUTE RATINGS	6
3.2.1	TFT LCD MODULE	6
4	ELECTRICAL SPECIFICATIONS.....	7
4.1	FUNCTION BLOCK DIAGRAM	7
4.2	INTERFACE CONNECTIONS	7
4.3	ELECTRICAL CHARACTERISTICS	7
4.3.1	LCD ELETRONICS SPECIFICATION	9
4.3.2	BACKLIGHT UNIT	11
4.4	DISPLAY PORT SIGNAL TIMING SPECIFICATION	12
4.4.1	ELECTRICAL SPECIFICATIONS.....	12
4.4.2	COLOR DATA INPUT ASSIGNMENT	13
4.5	DISPLAY TIMING SPECIFICATIONS	14
4.6	POWER ON/OFF SEQUENCE	15
5	OPTICAL CHARACTERISTICS	20
5.1	TEST CONDITIONS.....	20
5.2	OPTICAL SPECIFICATIONS	20
	Appendix. EDID DATA STRUCTURE	22
	Appendix. OUTLINE DRAWING	25



Product Specification

E133HVN-801

Revised Record				
Version	Date	Revised Content/Summary	Page	Remark
01	2018/09/21	First Edition	All	



Product Specification

E133HVN-801

1. GENERAL DESCRIPTION

1.1 OVERVIEW

13.3" diagonal TFT Liquid Crystal Display module with 30 pins eDP interface. This module supports 1920 x 1080 FHD mode and can display 262,144 colors.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	13.3" diagonal	inch	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch	0.1529 (H) x 0.1529 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally Black	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Luminance, White (Center)	800	cd/m2	
Power Consumption	Total 7.25W (Typ.)@cell 0.88W (Max.), BL 6.37W (Typ..)		(1)

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3

V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 °C, whereas

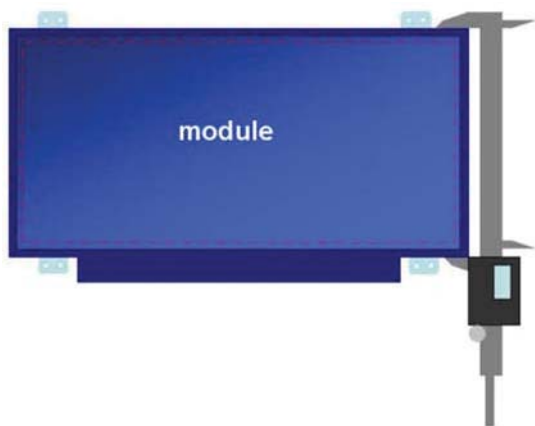
BLACK pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Glass	Thickness		0.4		mm	
Polarizer	Thickness		0.135		mm	
Module Size	Horizontal (H)	304.85	305.35	305.85	mm	(1) (2)
	Vertical (V) w/o PCB and Hinge	177.61	178.11	178.61	mm	
	Vertical (V) with PCB w/o Hinge	192.95	193.45	193.95	mm	
	Thickness (T)		2.70	2.85	mm	
	Thickness (T) (PCBA with Mylar)	-	2.88	3.09	mm	
Active Area	Horizontal	293.66	293.76	293.86	mm	
	Vertical	165.14	165.24	165.34	mm	
Weight		-	245	260	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Dimensions are measured by caliper.



2.1 CONNECTOR TYPE

Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-030E-12

User's connector Part No: IPEX-20453-030T-03



Product Specification

E133HVN-801

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

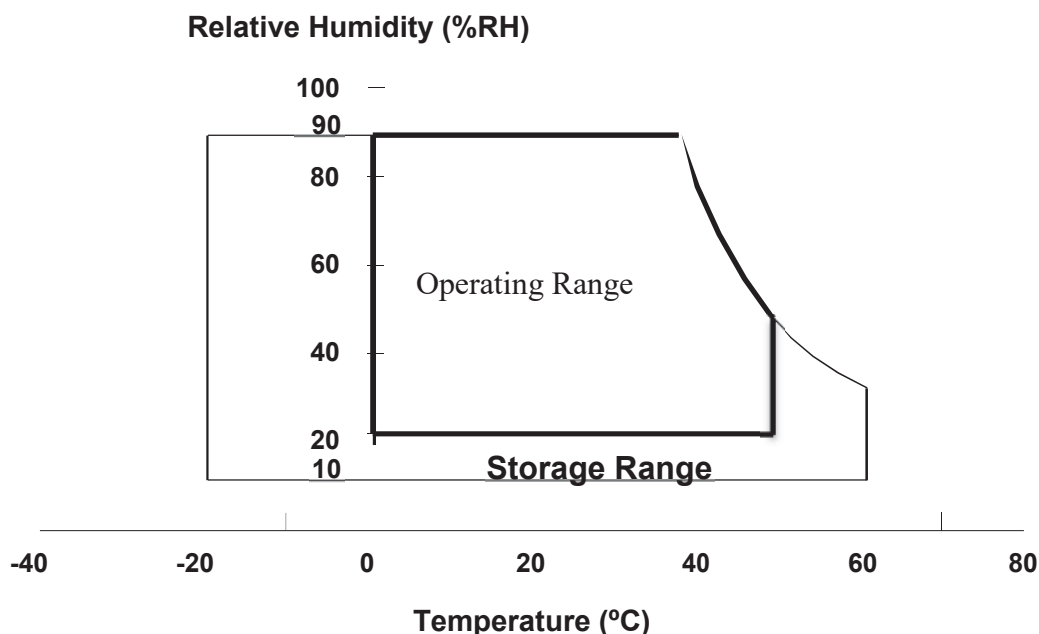
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)

Note (1) (a) 90 %RH Max. (Ta < 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta < 40 °C).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 °C min. and 60 °C max.



3.2 ELECTRICAL ABSOLUTE RATINGS

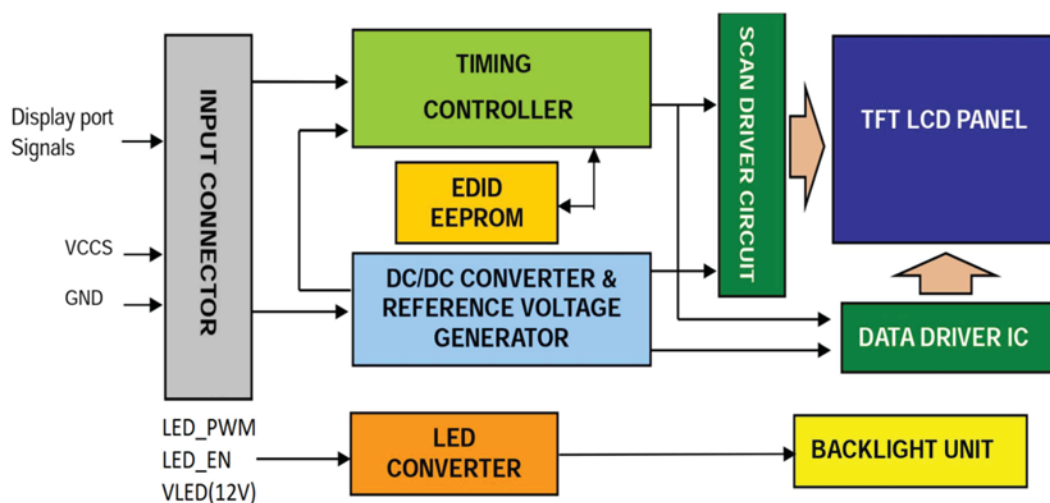
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max		
Power Supply Voltage	V _{CCS}	-0.3	+0.4	V	(1)
Logic input Voltage	V _{IN}	-0.3	V _{CCS} +0.3	V	

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2 INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	CABC_EN	CABC Enable Input	
2	H_GND	High Speed Ground	
3	ML1-	Complement Signal-Lane 1	
4	ML1+	True Signal-Main Lane 1	
5	H_GND	High Speed Ground	
6	ML0-	Complement Signal-Lane 0	
7	ML0+	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3 V (typical)	
13	VCCS	Power Supply +3.3 V (typical)	
14	NC	No Connection(Reserved for LCD Test)	
15	GND	Ground	
16	GND	Ground	
17	HPD	Hot Plug Detect	
18	NC	No Connection (Reserved)	
19	NC	No Connection (Reserved)	
20	NC	No Connection (Reserved)	
21	NC	No Connection (Reserved)	
22	NC	No Connection (Reserved)	
23	NC	No Connection (Reserved)	
24	NC	No Connection (Reserved)	
25	NC	No Connection (Reserved)	



Product Specification

E133HVN-801

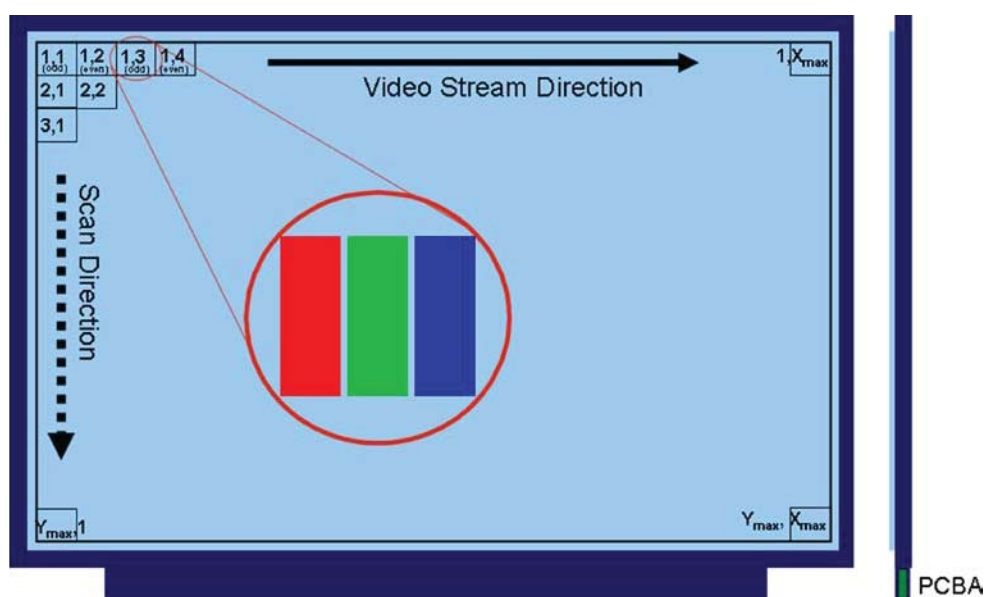
26	NC	No Connection (Reserved)	
27	NC	No Connection (Reserved)	
28	NC	No Connection (Reserved)	
29	NC	No Connection (Reserved)	
30	NC	No Connection (Reserved)	

Note (1) The first pixel is odd as shown in the following figure.

Note (2) The setting of CABC function are as follows.

Pin	Enable	Disable
CABC_EN	Hi	Lo or Open

Hi = High level, Lo = Low level.



4. 3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

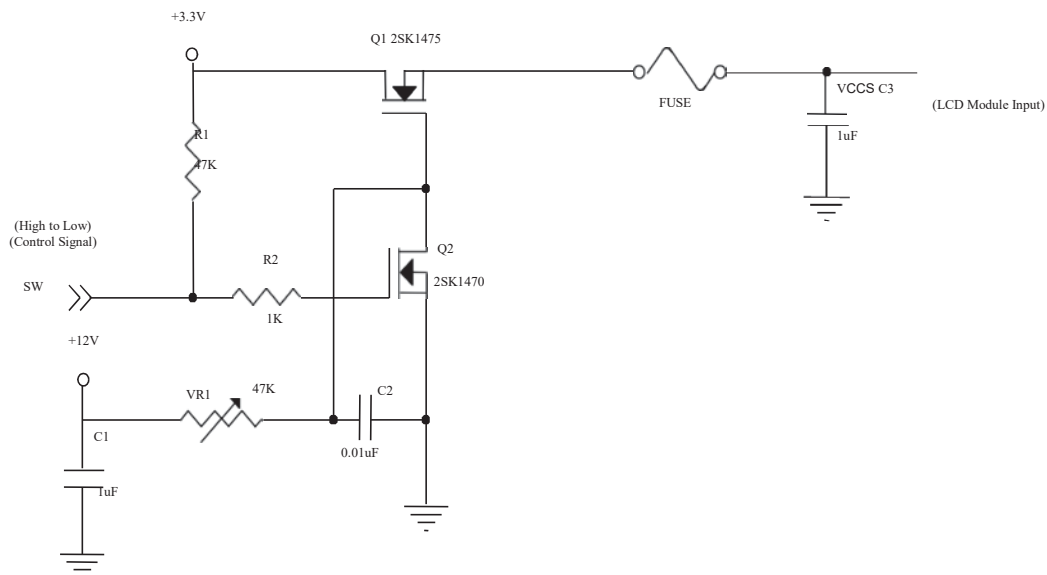
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)
HPD	High Level		2.0	-	2.5	V	(6)
	Low Level		0	-	0.6	V	(6)
HPD Impedance		R _{HPD}	30K			Ω	(5)
Ripple Voltage		V _{RP}	-	50	-	mV	(1)
CABC_EN Input Voltage	High Level	V _{IHCE}	2.0	-	2.5	V	(5)
	Low Level	V _{ILCE}	0	-	0.6	V	(5)
CABC_EN Impedance		R _{CABC_EN}	30K	-	-	Ω	(5)
Inrush Current		I _{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	I _{CC}		247	266	mA	(3)a
	Black			235	250	mA	(3)
Power per EBL WG		P _{EBL}		1.4	-	W	(4)

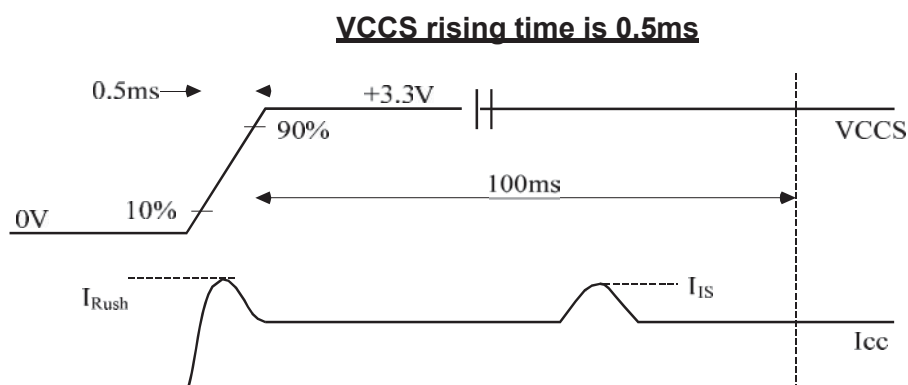
Note (1) The ambient temperature is $T_a = 25 \pm 2^\circ\text{C}$.

Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_S: the maximum current of the first 100ms after power-on

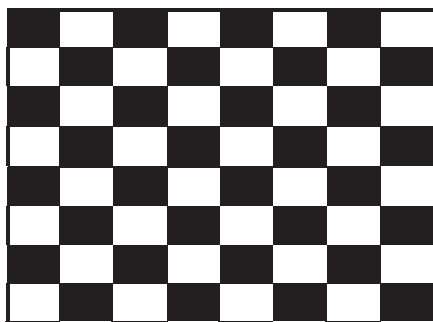
Measurement Conditions: Shown as the following figure. Test pattern: black.





Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, $T_a = 25 \pm 2^\circ\text{C}$, DC Current and $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

- (a) VCCS = 3.3 V, $T_a = 25 \pm 2^\circ\text{C}$, $f_v = 60\text{ Hz}$,
- (b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.
- (c) Luminance: 60 nits

Note (5) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 BACKLINE UNIT to obtain more information.

Note (6) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action

4.3.2 BACKLIGHT UNIT

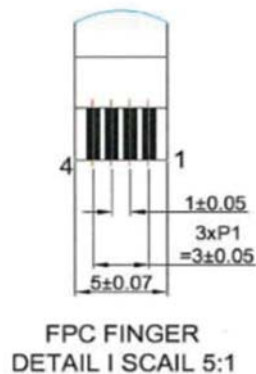
Ta = 25 ± 2 °C

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	VL	-	27.7	-	V	
LED Light Bar Power Supply Current	IL	-	230	-	mA	
Power Consumption	PL	-	6.37	-	W	
LED Life Time	L _{BL}	30000	-	-	Hrs	(1)

Note (1) Definition of life time

- Brightness of LED becomes to 50% of its original value.
- Test condition I_L=230mA and 25°C (Room Temperature)

4.3.3 LED PIN ASSIGNMENT



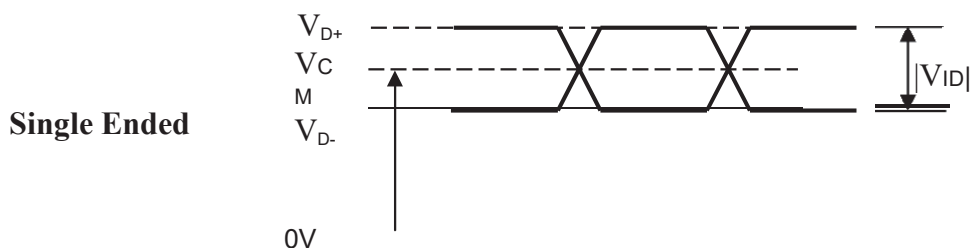
LED BAR	
PIN	PIN NAME
1	LED-GND
2	LED-GND
3	LED-Vin
4	LED-Vin

4.4 DISPLAY PORT SIGNAL TIMING SPECIFICATION

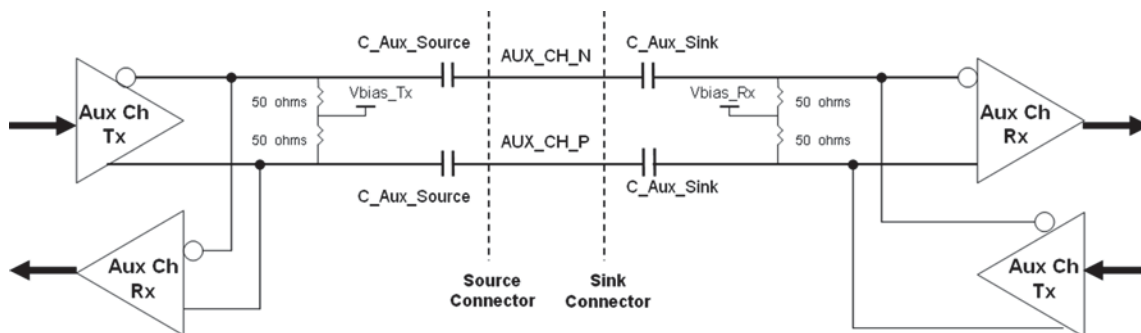
4.4.1 ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(3)

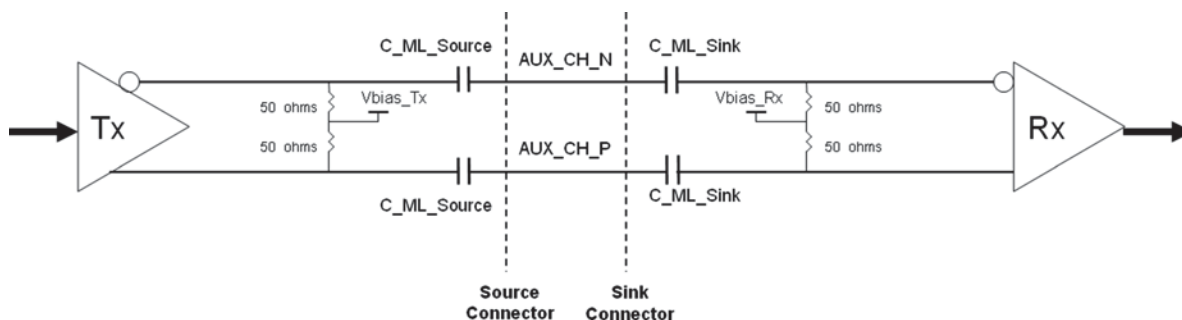
Note (1) Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.



(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



(4) The source device should pass the test criteria described in DisplayPort Compliance Test Specification (CTS) 1.1



Product Specification

E133HVN-801

4.4.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan Magenta	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	White	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage



Product Specification

E133HVN-801

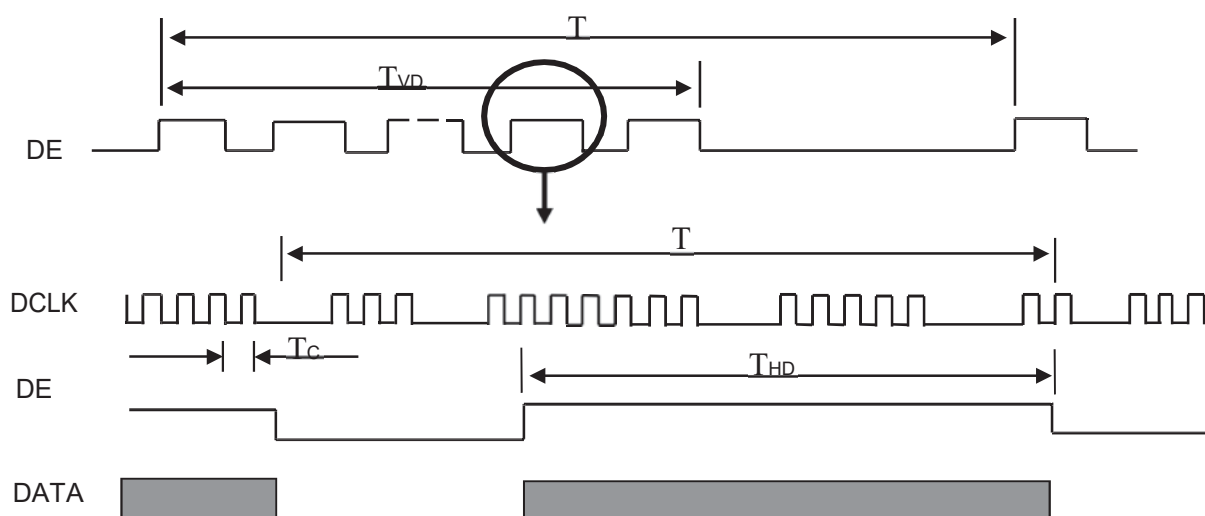
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Refresh Rate 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	152.08	152.84	153.60	MHz	-
DE	Vertical Total Time	TV	1128	1132	1136	TH	-
	Vertical Active Display Period	TVD	1080	1080	1080	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	52	TV-TVD	TH	-
	Horizontal Total Time	TH	2230	2250	2270	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	330	TH-THD	Tc	-

INPUT SIGNAL TIMING DIAGRAM

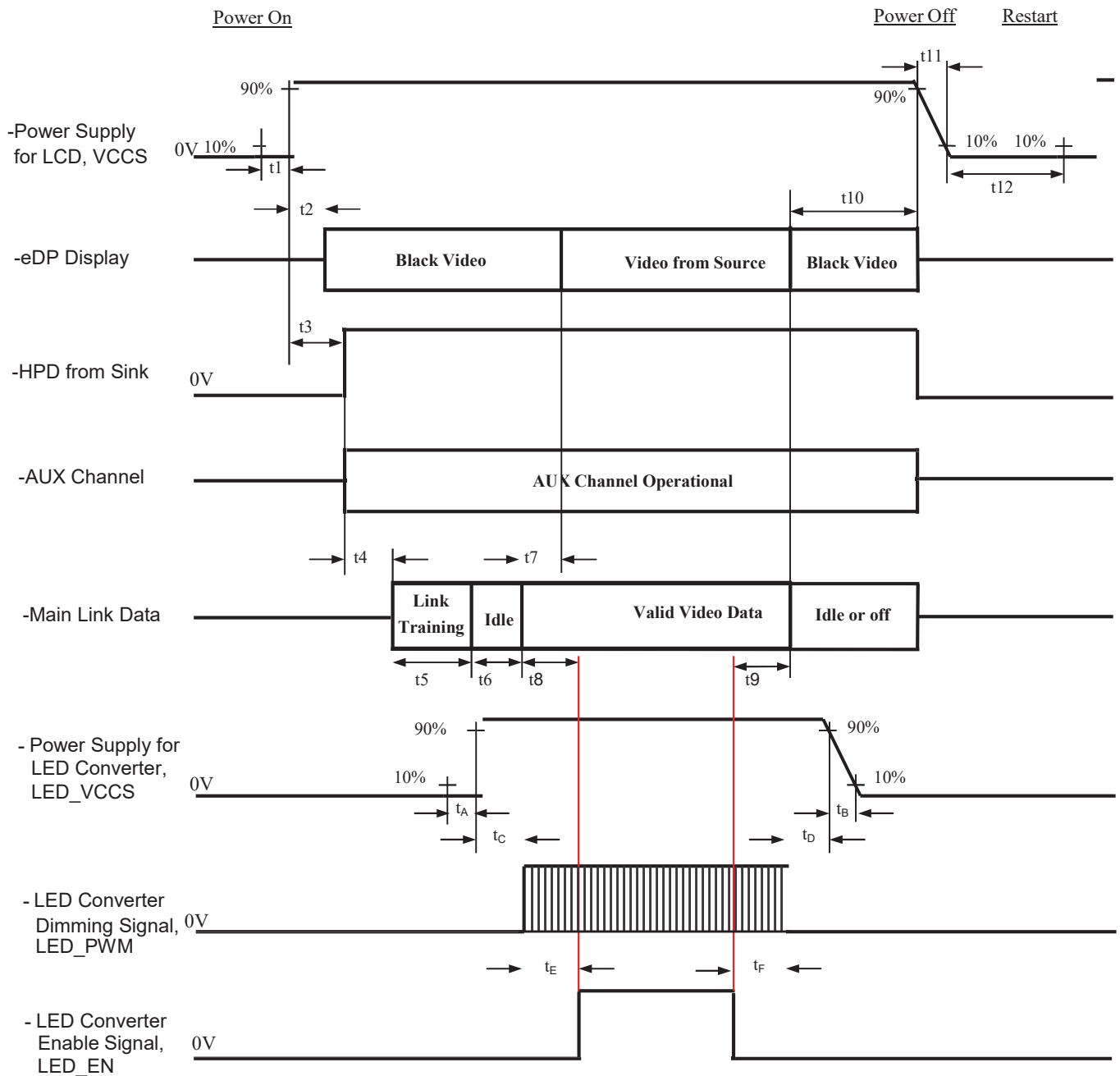




Product Specification

E133HVN-801

4.6 POWER ON/OFF SEQUENCE





Product Specification

E133HVN-801

Timing Specifications

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	0	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	0	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80	-	ms	Source must assure display video is stable *: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	50	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below) *: Recommended by INX. To avoid garbage image.
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-



Product Specification

E133HVN-801

t12	VCCS Power off time	Source	500	-	ms	-
t _A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t _B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t _C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t _D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t _E	Delay from LED dimming signal to LED enable signal	Source	0	-	ms	-
t _F	Delay from LED enable signal to LED dimming signal	Source	0	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on. Before LCD_VCCS and LED_VCCS are ready, it is recommended to pull down the backlight control signals

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.



Product Specification

E133HVN-801

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	T _a	25±2	°C
Ambient Humidity	H _a	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I _L	230	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing Normal Angle	600	800	-	-	(2), (5),(7)
Response Time		T _R		-	14	19	ms	(3),(7)
		T _F		-	11	16	ms	
Luminance of White		L _W		680	800	-	cd/m ²	(4), (6),(7)
Color Chromaticity	Re d	R _x		Typ – 0.03	0.643	Typ + 0.03	-	(1),(7)
		R _y			0.340		-	
	Green	G _x			0.313		-	
		G _y			0.608		-	
	Blu e	B _x			0.154		-	
		B _y			0.051		-	
	White	W _x			0.313		-	
		W _y			0.329		-	
	Color Gamut	C.G.	65		72		-	
Viewing Angle	Horizontal	θ_{x+}	CR≥10	80	85		Deg.	(1),(5), (7)
		θ_{x-}		80	85	-		
	Vertical	θ_{Y+}		80	85	-		
		θ_{Y-}		80	85	-		
White Variation of 5 and 13 Points		δW_{5p}	$\theta_x=0^\circ, \theta_Y=0^\circ$	80	90	-	%	(5),(6)
		δW_{13p}	$\theta_x=0^\circ, \theta_Y=0^\circ$	65	75	-	%	(7)

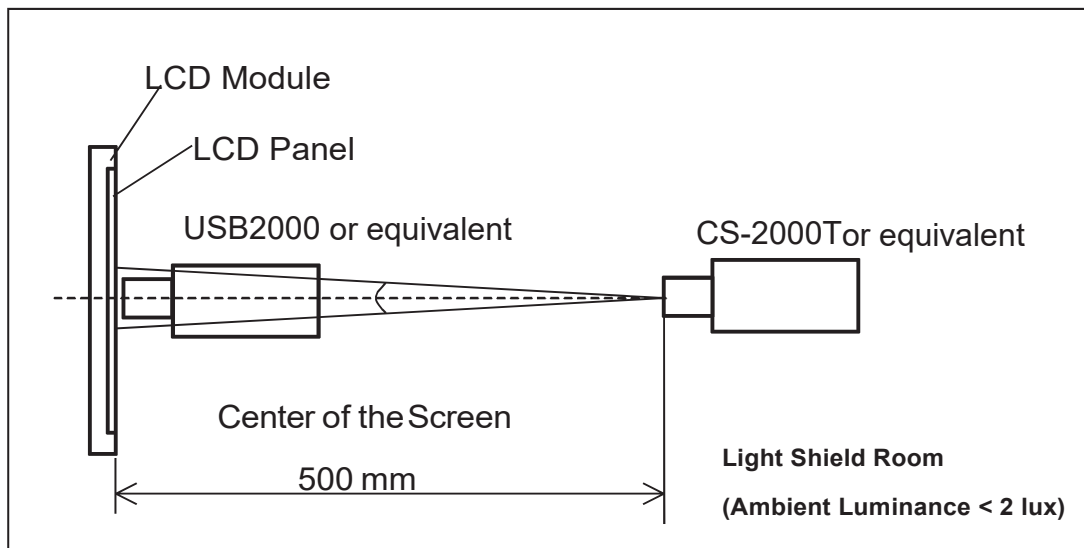
CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

The graph illustrates the optical response over time for a 60 Hz refresh rate. The y-axis represents 'Optical Response' from 0% to 100%, and the x-axis represents 'Time'. The signal is periodic with a total period of 66.67 ms. It consists of three segments: a high state at 100% optical response (labeled 'Gray Level 63'), a low state at 0% optical response (labeled 'Gray Level 0'), and a return to the high state. The high state duration is 16.67 ms, the low state duration is 16.67 ms, and the return duration is 16.67 ms. The signal is shown as a smooth curve that transitions between the high and low states.

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Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

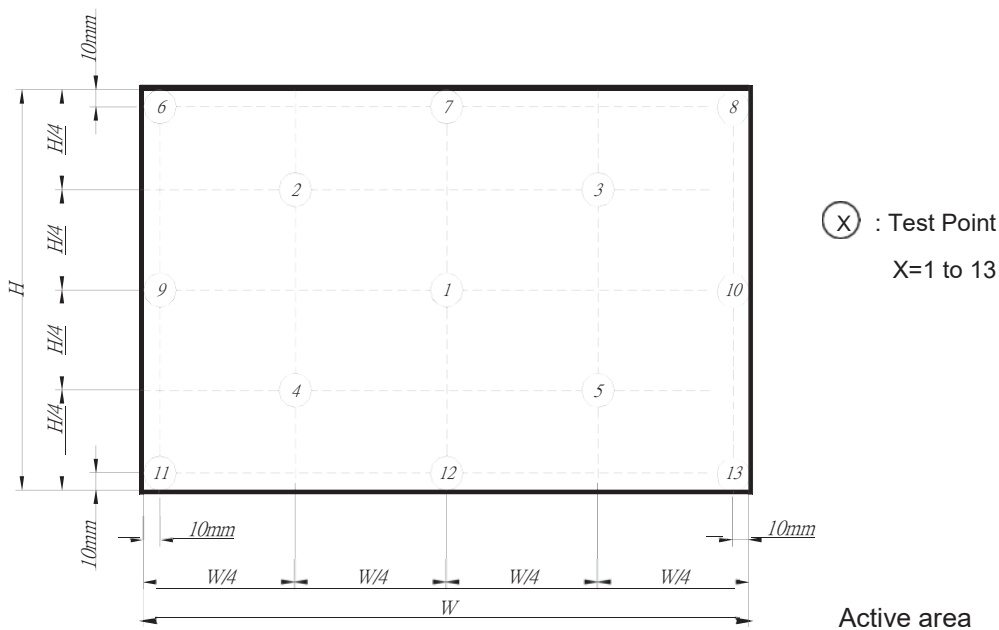


Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points / 13 points

$$\delta W_{5p} = \{ \text{Minimum} [L(1) \sim L(5)] / \text{Maximum} [L(1) \sim L(5)] \} * 100\%$$

$$\delta W_{13p} = \{ \text{Minimum} [L(1) \sim L(13)] / \text{Maximum} [L(1) \sim L(13)] \} * 100\%$$



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

Note (8) Definition of color gamut (C.G%):

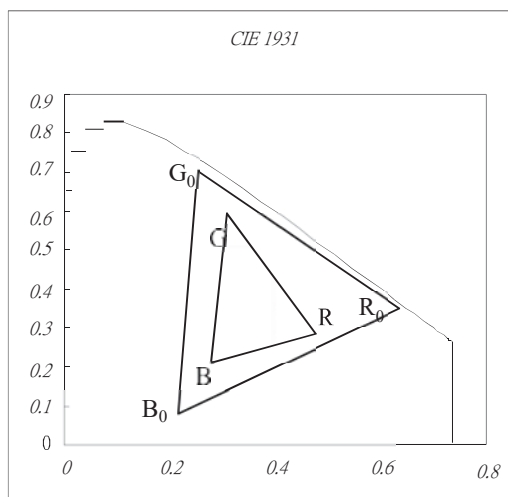
$$C.G\% = \frac{R G B}{R_0 G_0 B_0} \times 100\%$$

R_0, G_0, B_0 : color coordinates of red, green, and blue defined by NTSC, respectively.

R, G, B : color coordinates of module on 63 gray levels of red, green, and blue, respectively.

$R_0 G_0 B_0$: area of triangle defined by R_0, G_0, B_0

$R G B$: area of triangle defined by R, G, B





Product Specification

E133HVN-801

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	ID system manufacturer name ("CMN")	0D	00001101
9	9	ID system manufacturer name	AE	10101110
10	0A	ID system Product Code (LSB)	71	01110001
11	0B	ID system Product Code (MSB)	13	00010011
12	0C	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
13	0D	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
14	0E	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
15	0F	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
16	10	Week of manufacture (fixed week code)	0B	00001011
17	11	Year of manufacture (fixed year code)	1A	00011010
18	12	Version=1	01	00000001
19	13	Revision=4	04	00000100
20	14	Vedio Input Definition	95	10010101
21	15	Active area horizontal ("29.376cm")	1D	00011101
22	16	Active area vertical ("16.524cm")	11	00010001
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB, Non-continous")	02	00000010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	87	10000111
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	85	10000101
27	1B	Rx=0.643	A4	10100100
28	1C	Ry=0.340	57	01010111
29	1D	Gx=0.313	50	01010000
30	1E	Gy=0.608	9B	10011011
31	1F	Bx=0.154	27	00100111
32	20	By=0.051	0D	00001101
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	No manufacturer's specific timing	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001



Product Specification

E133HVN-801

42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("152.84MHz", According to VESA CVT Rev1.4)	B4	10110100
55	37	# 1 Pixel clock (hex LSB first)	3B	00111011
56	38	# 1 H active ("1920")	80	10000000
57	39	# 1 H blank ("330")	4A	01001010
58	3A	# 1 H active : H blank ("1920 :330")	71	01110001
59	3B	# 1 V active ("1080")	38	00111000
60	3C	# 1 V blank ("52")	34	00110100
61	3D	# 1 V active : V blank ("1080 :52")	40	01000000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 5")	35	00110101
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 3 : 5")	00	00000000
66	42	# 1 H image size ("293 mm")	25	00100101
67	43	# 1 V image size ("165 mm")	A5	10100101
68	44	# 1 H image size : V image size	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
72	48	Detailed timing description # 1 Pixel clock ("122.26MHz", According to VESA CVT Rev1.4)	C2	11000010
73	49	# 1 Pixel clock (hex LSB first)	2F	00101111
74	4A	# 1 H active ("1920")	80	10000000
75	4B	# 1 H blank ("330")	4A	01001010
76	4C	# 1 H active : H blank ("1920 :330")	71	01110001
77	4D	# 1 V active ("1080")	38	00111000
78	4E	# 1 V blank ("52")	34	00110100
79	4F	# 1 V active : V blank ("1080 :52")	40	01000000
80	50	# 1 H sync offset ("48")	30	00110000
81	51	# 1 H sync pulse width ("32")	20	00100000
82	52	# 1 V sync offset : V sync pulse width ("3 : 5")	35	00110101
83	53	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 3 : 5")	00	00000000
84	54	# 1 H image size ("293 mm")	25	00100101
85	55	# 1 V image size ("165 mm")	A5	10100101



Product Specification

E133HVN-801

86	56	# 1 H image size : V image size	10	00010000
87	57	# 1 H boarder ("0")	00	00000000
88	58	# 1 V boarder ("0")	00	00000000
89	59	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Flag	00	00000000
93	5D	Data Type Tag: Alphanumeric Data String (ASCII)	FE	11111110
94	5E	Flag	00	00000000
95	5F	Dell P/N 1st Character "0"	30	00110000
96	60	Dell P/N 2nd Character "C"	43	01000011
97	61	Dell P/N 3rd Character "K"	4B	01001011
98	62	Dell P/N 4th Character "H"	48	01001000
99	63	Dell P/N 5th Character "P"	50	01010000
100	64	EDID Revision	80	10000000
101	65	Manufacturer P/N "1"	31	00110001
102	66	Manufacturer P/N "3"	33	00110011
103	67	Manufacturer P/N "3"	33	00110011
104	68	Manufacturer P/N "H"	48	01001000
105	69	Manufacturer P/N "C"	43	01000011
106	6A	Manufacturer P/N "E"	45	01000101
107	6B	New line character indicates end of ASCII string	0A	00001010
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag: Manufacturer Specified Data 00	00	00000000
112	70	Flag	00	00000000
113	71	Color Management	00	00000000
114	72	Panel Type and Revision	41	01000001
115	73	Frame Rate	01	00000001
116	74	Light Controller Interface and Maximum Luminance	A3	10100011
117	75	Front Surface / Polarizer and Pixel Structure	00	00000000
118	76	Multi-Media Features	10	00010000
119	77	Multi-Media Features	00	00000000
120	78	Special Features	00	00000000
121	79	Special Features	0A	00001010
122	7A	Special Features	01	00000001
123	7B	New line character indicates end of ASCII string	0A	00001010
124	7C	Padding with "Blank" character	20	00100000
125	7D	Padding with "Blank" character	20	00100000
126	7E	No extension	00	00000000
127	7F	Checksum	57	01010111

