



SPECIFICATION FOR APPROVAL

()	Prel	iminary	Specification
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(4) Final	Spec	ifica	tion
\ V	,	Opos		

Title	14.0" Full HD TFT	14.0" Full HD TFT LCD				
Customer	SUPPLIER	LG Display Co., Ltd.				
MODEL	*MODEL	LP140WF1				
l l	Suffix	SPK1				

^{*}When you obtain standard approval, please use the above model name without suffix

SIGNATURE
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APPROVED BY	SIGNATURE
REVIEWED BY	
PREPARED BY	
Products Engineer LG Display Co	

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RECORD OF REVISIONS

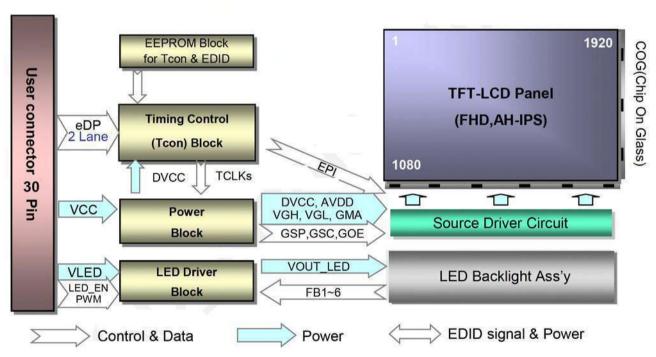
Revision No	Revision Date	Page	Description	EDID ver.
0.0	e.	=	Preliminary Specification	V0.0
1.0	Oct. 02. 2013	-	Final Specification	V1.0

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1. General Description

The LP140WF1 is a Color Active Matrix Liquid Crystal Display with an integral LED backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. This TFT-LCD has 14.0 inches diagonally measured active display area with FHD resolution (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into Red, Green and Blue subpixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors. The LP140WF1 has been designed to apply the interface method that enables low power, high speed, low EMI. The LP140WF1 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the subpixels, the LP140WF1 characteristics provide an excellent flat display for office automation products such as Notebook PC.



General Features

Active Screen Size	14.0 inches diagonal
Outline Dimension	320.4 (H, Typ.) × 205.1 (V, Typ.) × 3.0 (D, Max.) [mm] (with Bracket & PCB Board)
Pixel Pitch	0.1611 mm x 0.1611 mm
Pixel Format	1920 horiz. By 1080 vert. Pixels RGB strip arrangement
Color Depth	6-bit, 262,144 colors
Luminance, White	300 cd/m ² (Typ. 5 point)
Power Consumption	Total 5.0W (Typ.) Logic : 1.0W (Typ. @ Mosaic), B/L : 4.0W (Typ. @VLED12V)
Weight	300 g (Max.) / 290 g (Typ.)
Display Operating Mode	Normally Black
Surface Treatment	Anti glare treatment (3H) of the front Polarizer
RoHS Compliance	Yes
BFR / PVC / As Free	Yes for all

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2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

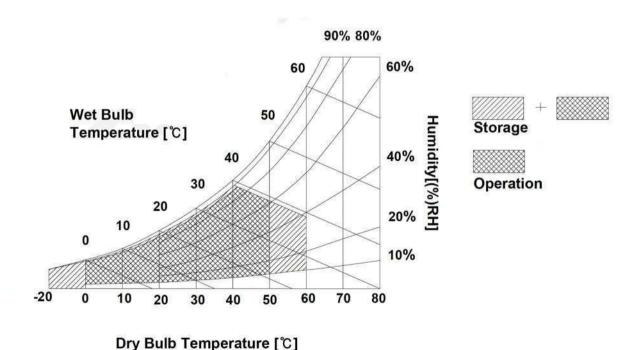
Table 1. ABSOLUTE MAXIMUM RATINGS

Dozomator	Values			Units	Notes	
Parameter	Symbol	Min	Max	Units	notes	
Power Input Voltage	VCC	-0.3	4.0	Vdc	at 25 ± 5°C	
Operating Temperature	Тор	0	50	³C	1	
Storage Temperature	Нѕт	-20	60	°C	1	
Operating Ambient Humidity	Нор	10	90	%RH	1	
Storage Humidity	Нѕт	10	90	%RH	1	

Note: 1. Temperature and relative humidity range are shown in the figure below.

Wet bulb temperature should be 39°C Max, and no condensation of water.

Note: 2. Storage Condition is guaranteed under packing condition.



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3. Electrical Specifications

3-1. Electrical Characteristics

The LP140WF1 requires two power inputs. The first logic is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second backlight is the input about LED BL with LED Driver.

Table 2. ELECTRICAL CHARACTERISTICS

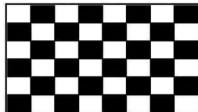
Dovometer		0 1 1		Values		- Unit V	Notes
Parameter	Symbol	Min	Тур	Max			
LOGIC : Power Supply Input Voltage					3.6		
		Vcc	3.0	3.3			
Power Supply Input Current	Mosaic	Icc	-	320	365	mA	2
Power Consumption		Pcc	-	1.0	1.2	W	2
Power Supply Inrush Current		Icc_p	-	-	1500	mA	3
Differential Impedance		Zm	90	100	110	Ω	4
BACKLIGHT : (with LED Drive	er)						
LED Power Input Voltage		VLED	6.0	12.0	21.0	٧	5
LED Power Input Current	ILED	-	335	345	mA	6	
LED Power Consumption		PLED	-	4.0	4.1	W	6
LED Power Inrush Current	***************************************	ILED_P	-	-	1500	mA	7
PWM Duty Ratio			5	-	100	%	8
PWM Jitter	alk onitin outside the district	-	0	-	0.2	%	9
PWM Impedance		Zpwm	20	40	60	kΩ	
PWM Frequency		FPWM	200	-	1000	Hz	10
PWM High Level Voltage		V _{PWM_H}	3.0	-	3.6	V	
PWM Low Level Voltage		V _{PWM_L}	0	-	0.3	٧	
LED_EN Impedance		Zpwm	20	40	60	kΩ	
LED_EN High Voltage		VLED_EN_H	3.0	-	3.6	V	
LED_EN Low Voltage		VLED_EN_L	0	-	0.3	V	
Life Time			15,000	:=:	-	Hrs	11

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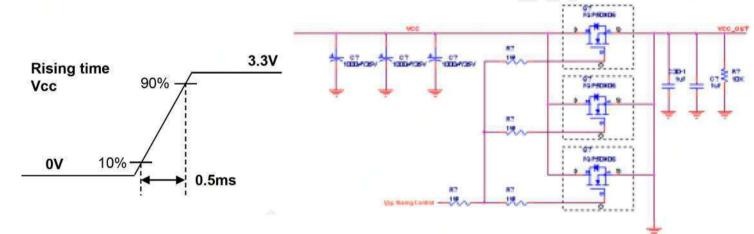


Note)

- 1. The measuring position is the connector of LCM and the test conditions are under 25 °C, fv = 60Hz, Black pattern.
- 2. The specified Icc current and power consumption are under the Vcc = 3.3V, 25°C, fv = 60Hz condition and Mosaic pattern.

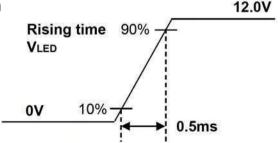


- 2. This Spec. is the max load condition for the cable impedance designing.
- 3. The below figures are the measuring Vcc condition and the Vcc control block LGD used. The Vcc condition is same as the minimum of T1 at Power on sequence.



- 4. This impedance value is needed for proper display and measured form eDP Tx to the mating connector.
- 5. The measuring position is the connector of LCM and the test conditions are under 25 °C.
- 6. The current and power consumption with LED Driver are under the Vled = 12.0V, 25°C, Dimming of Max luminance and White pattern with the normal frame frequency operated (60Hz).
- 7. The below figures are the measuring VIed condition and the Vled control block LGD used.

VLED control block is same with Vcc control block.



- 8. The operation of LED Driver below minimum dimming ratio may cause flickering or reliability issue.
- 9. If Jitter of PWM is bigger than maximum, it may induce flickering.
- 10. This Spec. is not effective at 100% dimming ratio as an exception because it has DC level equivalent to 0Hz. In spite of acceptable range as defined, the PWM Frequency should be fixed and stable for more consistent brightness control at any specific level desired.
- 11. The life time is determined as the time at which brightness of LCD is 50% compare to that of minimum value specified in table 7. under general user condition.

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3-2. Interface Connections

This LCD employs two interface connections, a 30 pin connector used for the module electronics interface and the other connector used for the integral backlight system.

Table 3. MODULE CONNECTOR PIN CONFIGURATION (CN1)

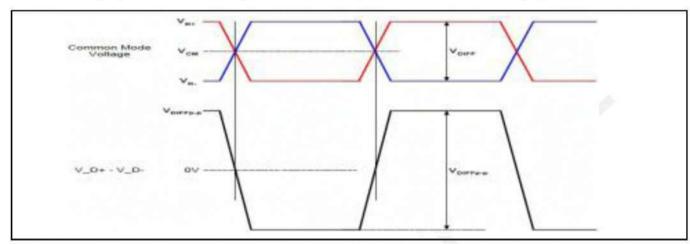
Pin	Symbol	Description	Notes
1	NC	No Connect	[Interface Chip]
2	GND	High Speed (Main Link) Ground	LCD: Parade, DP643 (LCD Controller
3	Lane1_N	Complement Signal-Lane 1	Including eDP Receiver.
4	Lane1_p	True Signal-Main Lane 1	
5	• • • • • • • • • • • • • • • • • • • •		[Connector] GT05Q-30S-H10, LSM, 30, 0.5
	GND	High Speed (Main Link) Ground	2100@ 000 1110, E0IM, 00, 0.0
6	Lane0_N	Complement Signal-Lane 0	
7	Lane0_p	True Signal-Main Lane 0	
8	GND	High Speed (Main Link) Ground	[Connector pin arrangement]
9	AUX_P	True Signal-Auxiliary Channel	30 1
10	AUX_N	Complement Signal-Auxiliary Channel	<u> </u>
11	GND	High Speed (Main Link) Ground	
12	VCC	LCD Logic and driver power (3.3V Typ.)	[LCD Module Rear View]
13	VCC	LCD Logic and driver power (3.3V Typ.)	•
14	NC	No Connect	
15	GND	Ground	
16	GND	Ground	
17	HPD	HPD signal pin	
18	GND	LED Backlight Ground	
19	GND	LED Backlight Ground	
20	GND	LED Backlight Ground	
21	GND	LED Backlight Ground	[LGD P-Vcom Share pin]
22	LED_EN	LED Backlight On/Off	1. Pin for P-Vcom : #24, #25
23	PWM	System PWM Signal input for dimming	2. P-Vcom Address : 01010000
24	NC	NO Connect	
25	NC	NO Connect	
26	VLED	LED Backlight Power (6.0V-21V)	
27	VLED	LED Backlight Power (6.0V-21V)	
28	VLED	LED Backlight Power (6.0V-21V)	
29	VLED	LED Backlight Power (6.0V-21V)	
30	NC	NO Connect	



3-3. eDP Signal Timing Specifications

3-3-1. DC Specification

The VESA Display Port related AC specification is compliant with the VESA Display Port Standard v1.1a.



Description	Symbol	Min	Max	Unit	Notes
Differential peak to peak input valtage	VDIFF p-p	120		mV	For high bit rate
Differential peak-to-peak Input voltage		40	<u> </u>	mv	For reduced bit rate
Rx DC common mode voltage	VcM	0	2.0	V	

3-3-2. AC Specification

The VESA Display Port related AC specification is compliant with the VESA Display Port Standard v1.1a.

Description	Symbol	Min	Тур	Max	Unit	Notes
Unit Interval for high bit rate (2.7Gbps/lane)	UI_High_Rate		370	1	ps	Range is nominal ±350ppm. DisplayPort Link Rx does not require local crystal for link
Unit Interval for high bit rate (1.62Gbps/lane)	UI_Low_Rate		617	-	ps	clock generation
Lane-to-Lane skew	V Rx-SKEW- INTER_PAIR			5200	ps	-
Laura Jahan mala alaun	V Rx-SKEW-	10	(2)	100	ps	For high bit rate
Lane intra-pair skew	INTRA_PAIR	я	1	300	ps	For reduced bit rate

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3-4. Signal Timing Specifications

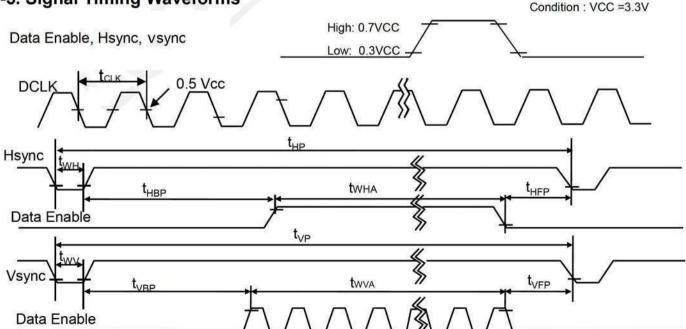
This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of eDP Tx/Rx for its proper operation.

Table 6. TIMING TABLE

ITEM	Symbol		Min	Тур	Max	Unit	Note
DCLK	OCLK Frequency		S=0	140.1		MHz	
	Period	t _{HP}		2092			
Hsync	Width	t _{wh}	(=)	36) = :	tCLK	
	Width-Active	t _{wha}		1920			
505	Period	t _{VP}		1116	, 18 1	7	
Vsync	Width	t _{wv}	187	5	14	tHP	
	Width-Active	t _{wva}		108C			
	Horizontal back porch	t _{HBP}	2 8 0	76	(#)	tCLK	
Data	Horizontal front porch	t _{HFP}	323	60	(全)	ICLK	
Enable	Vertical back porch	t _{VBP}		28		tHP	
	Vertical front porch	t _{VFP}	-	3			

Appendix) all reliabilities are specified for timing specification based on refresh rate of 60Hz. However, LP156WF4 has a good actual performance even at lower refresh rate (e.g. 40Hz or 50Hz) for power saving mode, whereas LP156WF4 is secured only for function under lower refresh rate. 60Hz at Normal mode, 50Hz, 40Hz at Power save mode. Don't care Flicker level (power save mode).

3-5. Signal Timing Waveforms



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3-6. Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 5. COLOR DATA REFERENCE

									Inp	out Co	olor D	ata							
,	Color			RE	D					GR	EEN		-			BL	UE		
	50101	MSE	3				LSB	MSE	3				LSB	MSE	3				LSB
		R 5	R4	R3	R 2	R 1	R 0	G 5	G 4	G 3	G 2	G 1	G 0	B 5	B 4	В3	B 2	B 1	В0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Color	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	RED (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (01)	0	0	0	0	υ	1	0	0	0	0	0	0	0	0	0	0	0	0
RED			•••••			••••						•••••			••••				
	RED (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
GREEN											 						 		
	GREEN (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	BLUE (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
BLUE		• • • • •		•••••	• • • • • •			••••	••••	•••••	 	••••	•••••				•••••	• • • • •	
	BLUE (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1



3-7. Power Sequence

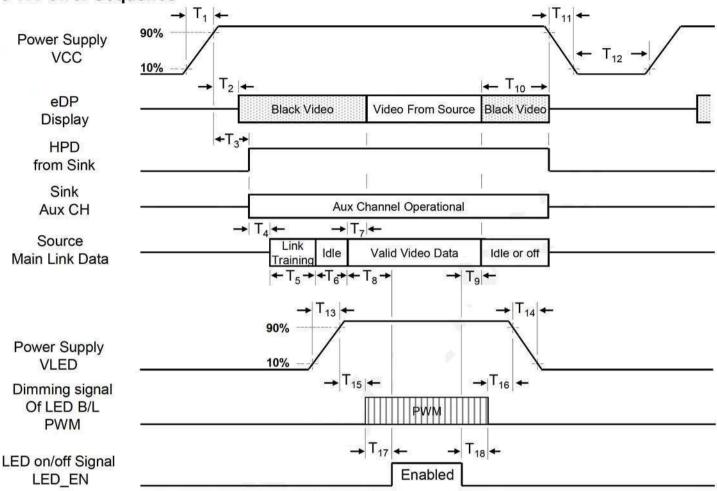


Table 6. POWER SEQUENCE TABLE

Therein	Required	Lin	nits	Linita	Notes
Timing	Ву	Min	Max	Units	Notes
Т1	Source	0.5	10	ms	11 2 0
T ₂	Sink	0	200	ms	(a)
T ₃	Sink	0	200	ms	72)
T ₄	Source	2.00	-	ms	(=)
T ₅	Source	2.73	=	ms	857
T ₆	Source		20 10 20 20 20	ms	
T ₇	Sink	0	50	ms	(12)
T ₈	Source	18 -1 1	7	ms	LGD recommend Min 200ms
T ₉	Source	822	=	ms	120

Timelma	Required			Units	Notes		
Timing	Ву	Min	Max	Units	Notes		
T ₁₀	Source	0	500	ms	.=:		
T ₁₁	Source	- 8	10	ms	3		
T ₁₂	Source	500	3 = 3	ms	VESA recommend Min 500ms		
T ₁₃	Source	0.5	10	ms	標度		
T ₁₄	Source	0.5	10	ms			
T ₁₅	Source	10	-	ms	8 4 51		
T ₁₆	Source	10	350	ms	5 = 3		
T ₁₇	Source	0	(50)	ms	ATT 20		
T ₁₈	Source	0	8 <u>2</u> 8	ms	2 5		

Limits

Required

- Note) 1. Do not insert the mating cable when system turn on.
 - 2. Valid Data have to meet "3-3. eDP Signal Timing Specifications"
 - 3. Video Signal, LED_EN and PWM need to be on pull-down condition on invalid status.
 - 4. LGD recommend the rising sequence of VLED after the Vcc and valid status of Video Signal turn on.

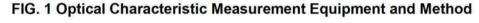
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4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0° .

FIG. 1 presents additional information concerning the measurement equipment and method.



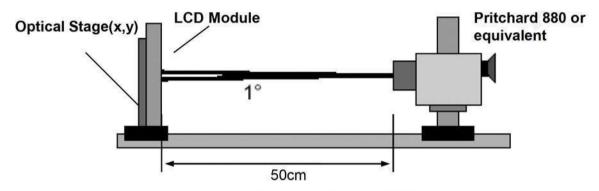


Table 9. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz, f_{CLK}= 69MHz

	0		Values	- 11	110200	Netes
Parameter	Symbol	Min	Тур	Max	Units	Notes
Contrast Ratio	CR	400	700			1
Surface Luminance, white	L _{WH}	255	300	-	cd/m ²	2
Luminance Variation	δ_{WHITE}	-	1.4	1.6		3
Response Time	Tr _R + Tr _D		35	50	ms	4
Color Coordinates					1	
RED	RX	0.610	0.640	0.670		,
	RY	0.315	0.345	0.375		
GREEN	GX	0.305	0.335	0.365		
	GY	0.595	0.625	0.655		
BLUE	вх	0.120	0.150	0.180		
***************************************	BY	0.022	0.052	0.082		
WHITE	WX	0.283	0.313	0.343		
(2,2,11,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,	WY	0.299	0.329	0.359		
Viewing Angle						5
x axis, right(Φ=0°)	Θr	80		=	degree	
x axis, left (Ф=180°)	Θl	80		=	degree	
y axis, up (Φ=90°)	Θu	80		_	degree	
y axis, down (⊕=270°)	Θd	80			degree	
Gray Scale				www.composition.events/green		6

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Note)

1. Contrast Ratio (CR) is defined mathematically as

Surface luminance is the average of 5 point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 1.

$$LWH = Average(L1, L2, ... L5)$$

 The variation in surface luminance, The panel total variation (δ WHITE) is determined by measuring LN at each test position 1 through 13 and then defined as following numerical formula.
 For more information see, FIG 2.

$$\delta$$
 WHITE = Maximum(L1,L2, ... L13) / Minimum(L1,L2, ... L13)

- 4. Response time is the time required for the display to transition from white to black (rise time, TrR) and from black to white (Decay Time, TrD). For additional information see FIG 3.
- 5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.
- Gray scale specification

*
$$fV = 60Hz$$

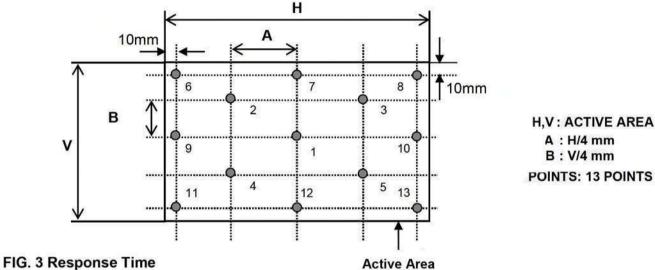
Gray Level	Luminance [%] (Typ)
L0	0.13
L7	0.70
L15	4.53
L23	10.80
L31	20.30
L39	33.00
L47	49.00
L55	73.00
L63	100.00

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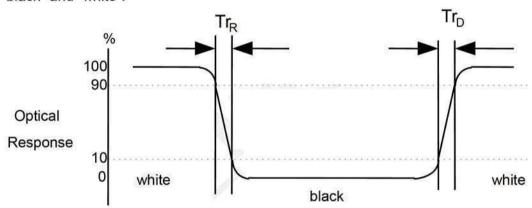


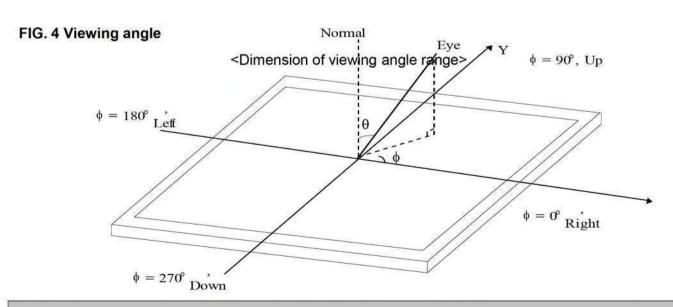
FIG. 2 Luminance

<Measuring point for Average Luminance & measuring point for Luminance variation>



The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".





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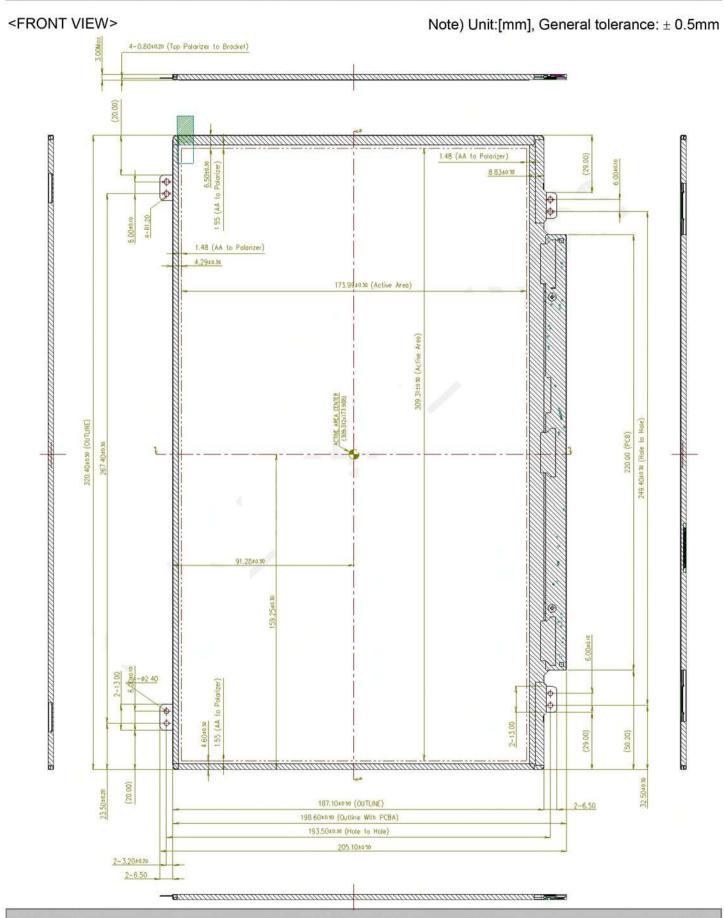
5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LP156WF4. In addition the figures in the next page are detailed mechanical drawing of the LCD.

	Horizontal	320.4 ± 0.5mm
Outline Dimension	Vertical	205.1 ± 0.5mm (with Bracket & PCB Board)
	Thickness	3.0mm (max.)
Pozel Area	Horizontal	312.50± 0.5mm
Bezel Area	Vertical	177.10 ± 0.5mm
Antive Display Area	Horizontal	309.31 ± 0.3mm
Active Display Area	Vertical	173.99 ± 0.3mm
Weight	300 g (Max.) / 290 g	(Typ.)
Surface Treatment	Anti-Glare treatme	ent of the front polarizer

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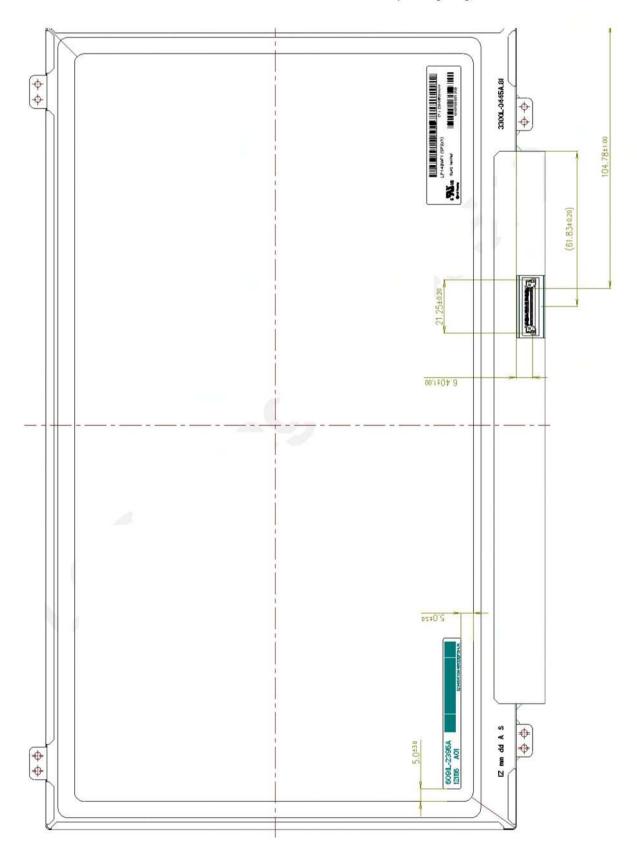






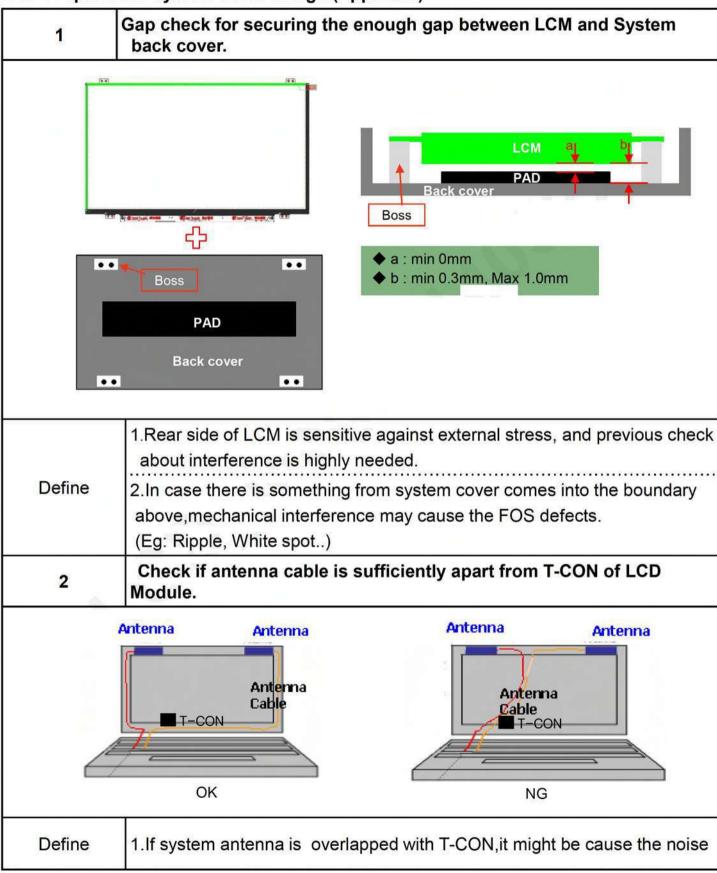
<REAR VIEW>

Note) Unit:[mm], General tolerance: ± 0.5mm



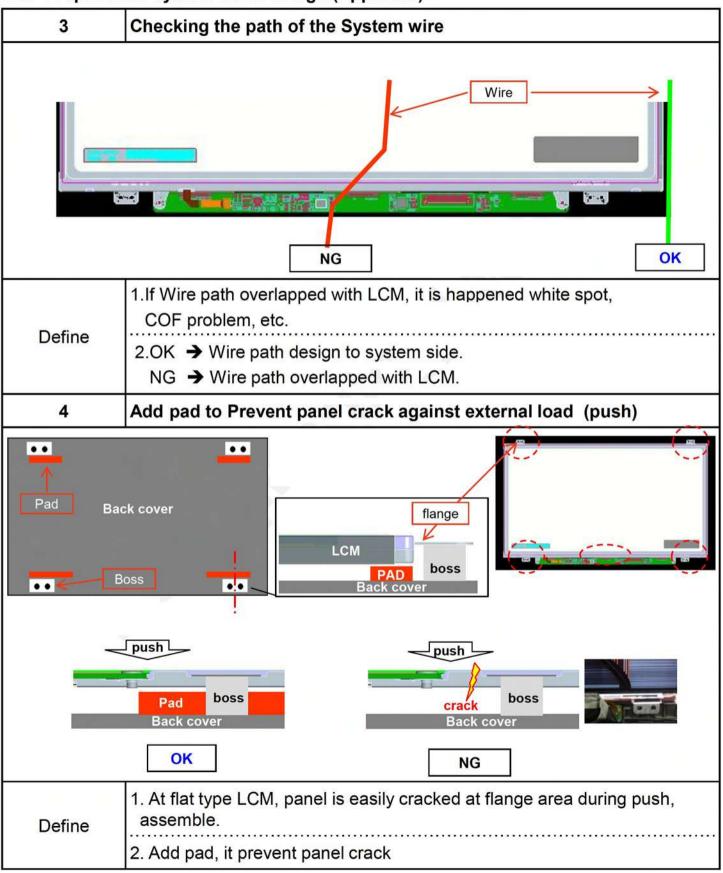


LGD Proposal for system cover design.(Appendix)



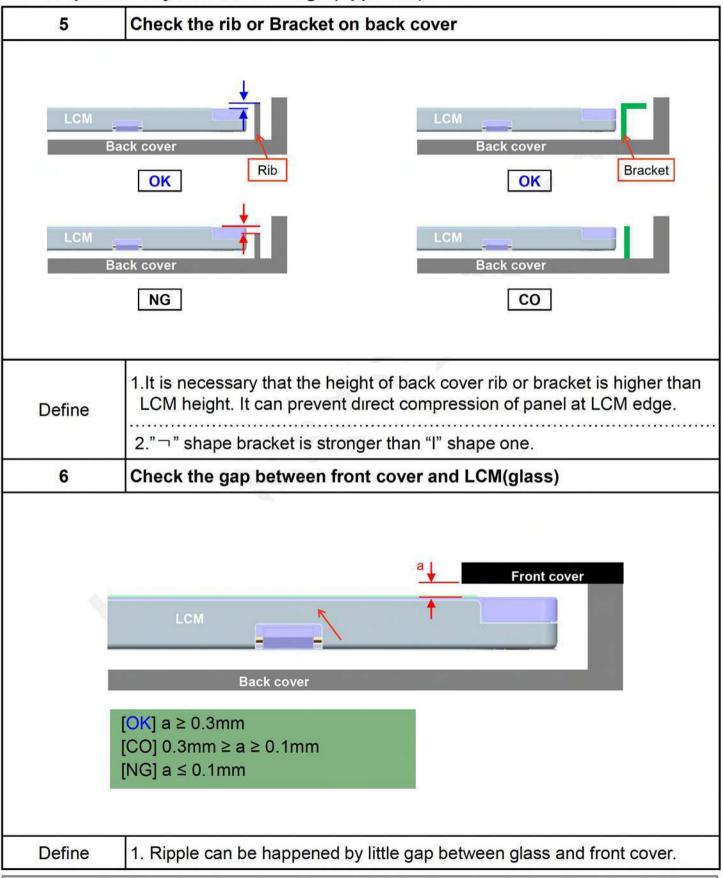


LGD Proposal for system cover design.(Appendix)





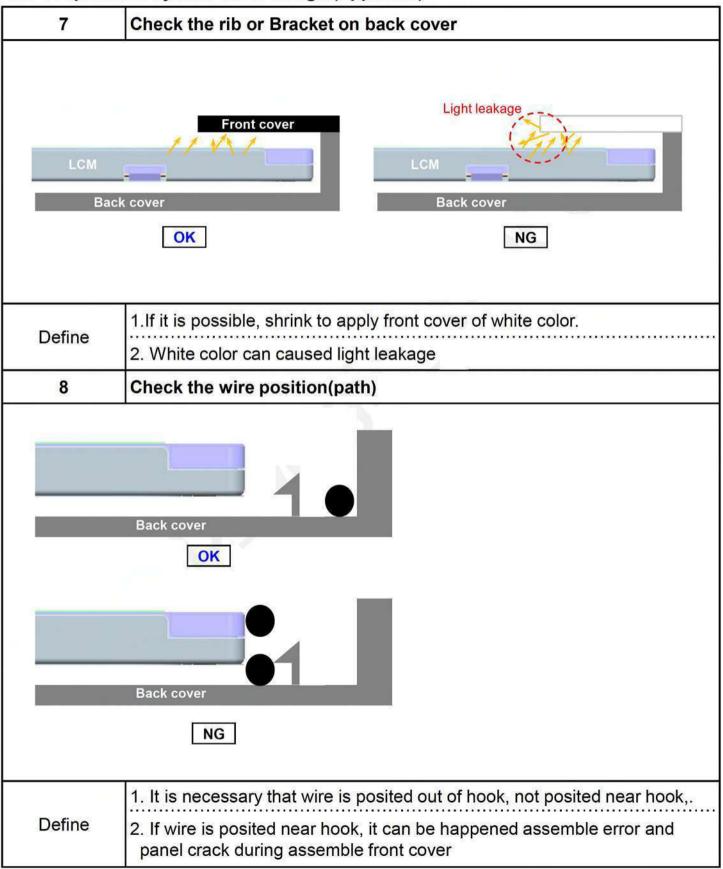
LGD Proposal for system cover design.(Appendix)



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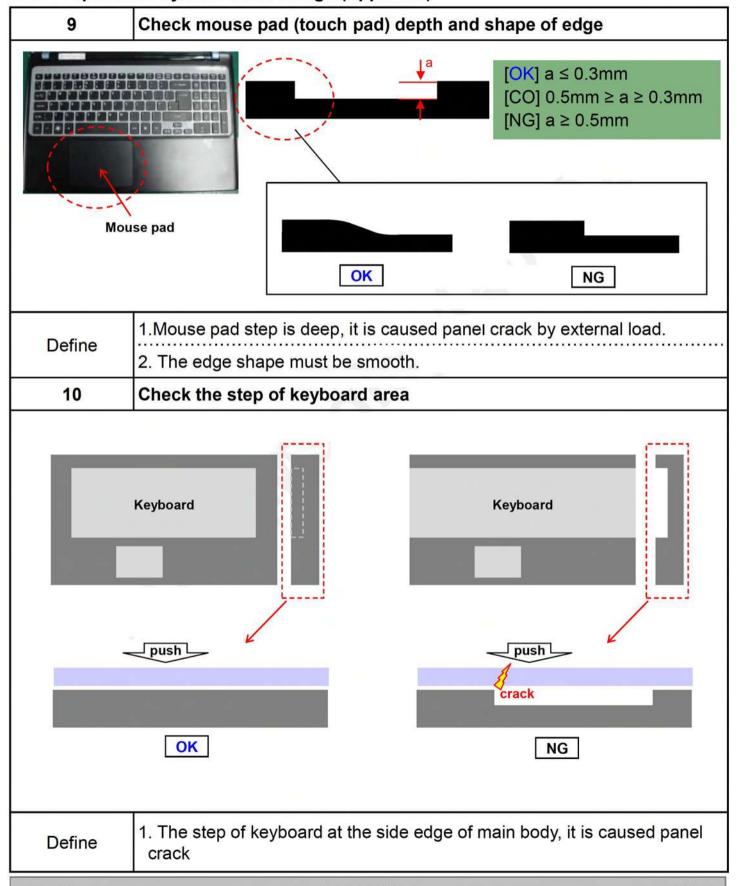


LGD Proposal for system cover design.(Appendix)





LGD Proposal for system cover design.(Appendix)



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6. Reliability

Environment test condition

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Vibration test (non-operating)	Sine wave, 5 ~ 150Hz, 1.5G, 0.37oct/min 3 axis, 30min/axis
6	Shock test (non-operating)	 No functional or cosmetic defects following a shock to all 6 sides delivering at least 180 G in a half sine pulse no longer than 2 ms to the display module No functional defects following a shock delivering at least 200 g in a half sine pulse no longer than 2 ms to each of 6 sides. Each of the 6 sides will be shock tested with one each display, for a total of 6 displays
7	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr

[{] Result Evaluation Criteria }

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There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.



7. International Standards

7-1. Safety

- a) UL 60950-1, Underwriters Laboratories Inc.
 Information Technology Equipment Safety Part 1: General Requirements.
- b) CAN/CSA-C22.2 No. 60950-1-07, Canadian Standards Association.
 Information Technology Equipment Safety Part 1: General Requirements.
- c) EN 60950-1, European Committee for Electrotechnical Standardization (CENELEC). Information Technology Equipment Safety Part 1 : General Requirements.
- d) IEC 60950-1, The International Electrotechnical Commission (IEC).
 Information Technology Equipment Safety Part 1: General Requirements

7-2. Environment

a) RoHS, Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011

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8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

Α	В	С	D	Е	F	G	Н	1	J	К	L	М	
---	---	---	---	---	---	---	---	---	---	---	---	---	--

A,B,C: SIZE(INCH)

E: MONTH F ~ M: SERIAL NO.

Note

1. YEAR

Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Mark	Α	В	С	D	Е	F	G	Н	J	K

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	Α	В	С

D: YEAR

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module. This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box:30 ea

b) Box Size: 478 × 365 × 288 mm

c) Box Label:

8-3. CT Code



CT : C AAAA XX XX XX XXX

HP Assembly Code (A.Code)

A.Code	HP P/N
DSYH	711939-292



9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1. MOUNTING PRECAUTIONS

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
 Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.
- (10) When handling the LCD module, it needs to handle with care not to give mechanical stress to the PCB and Mounting Hole area."

9-2. OPERATING PRECAUTIONS

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage : $V=\pm 200 mV$ (Over and under shoot voltage)
- (2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

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9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object.
 It is recommended that they be stored in the container in which they were shipped.

9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

- (1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition. etc
- (2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
 - Please carefully peel off the protection film without rubbing it against the polarizer.
- (3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
- (4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-nexane.

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APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 1/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
	0	00	Header	00	00000000
r	1	01	Header	FF	11111111
	2	02	Header	FF	11111111
de	3	03	Header	FF	11111111
Header	4	04	Header	FF	11111111
=	5	05	Header	FF	11111111
	6	06	Header	FF	111111111
	7	07	Header	00	00000000
	8	08	ID Manufacture Name LGD	30	00110000
12	9	09	ID Manufacture Name ID Product Code 040Ah	E4	11100100
Vendor / Product EDID Version	10 11	0A 0B	ID Product Code 040Ah (Hex LSB first.)	0A 04	00001010
endor / Produ EDID Version	12	0C	ID Serial No Optional ("00h" If not used, Number Only and LSB First)	00	00000100
Pre	13	0D	ID Serial No Optional ("00h" If not used, Number Only and LSB First)	00	00000000
2 2	14	0E	ID Serial No Optional ("00h" If not used, Number Only and LSB First)	00	00000000
10 10	15	0F	ID Serial No Optional ("00h" If not used, Number Only and LSB First)	00	00000000
and G	16	10	Week of Manufacture - Optinal 00 weeks	00	00000000
re L	17	11	Year of Manufacture 2013 years	17	00010111
	18	12	EDID structure version # = 1	01	00000001
	19	13	EDID revision # = 4	04	00000100
	20	99	Video input Definition = Input is a Digital Video signal Interface, Colo Bit Depth: 6 Bits per Primary Color, Digital Video	0.5	
	20	14	Interface Standard Supported: DisplayPort is supported	95	10010101
2	21	15	Horizontal Screen Size (Rounded cm) = 31 cm	1F	00011111
ay etc	22	16	Vertical Screen Size (Rounded cm) = 17 cm	11	00010001
ld:	23	17	Display Transfer Characteristic (Gamma) = (gamma*100)-100 = Example:(2.2*100)-100=120	78	01111000
Display Parameters	24	18	Feature Support [Display Power Management(DPM): Standby Mode is supported, Suspend Mode is not supported, Active Off = Very Low Power is supported ,Supported Color Encoding Formats: RGB 4:4:4 & YCrCb 4:4:4, Other Feature Support Flags: No_sRGB, Preferred Timing Mode, No_Display is continuous frequency (Multi-mode_Base EDID and Extension Block).]	EA	11101010
	25	19	Red/Green Low Bits (RxRy/GxGy)	DC	11011100
	26	1A	Blue/White Low Bits (BxBy/WxWy)	95	10010101
2 0	27	1B	Red X Rx=0.640	A3	10100011
Panel Color Coordinates	28	1C	Red Y Ry = 0.345	58	01011000
C III	29	1D	Green X Gx = 0.335	55	01010101
nel ora	30	1E	Green Y Gy = 0.625	A0	10100000
20.00	31	1F	Blue X Bx=0.150	26	00100110
	32	20	Blue Y By = 0.052	0D	00001101
	33	21	White X Wx=0.313	50	01010000
	34	22	White Y $Wy = 0.329$	54	01010100
7	25	22	ESTER LIVE TO A LANGE OF THE DESTRUCTION OF THE STATE OF	10	00000000
hed	35	23	Established timing 1 (Optional_00h if not used)	00	00000000
Established Timings	36	24	Established timing 2 (Optional_00h if not used)	00	00000000
Es	37	25	Manufacturer's timings (Optional_00h if not used)	00	00000000
	38	26	Standard timing ID1 (Optional 01h if not used)	01	00000001
	39	27	Standard timing ID1 (Optional_01h if not used)	01	00000001
	40	28	Standard timing ID2 (Optional_01h if not used) Standard timing ID2 (Optional_01h if not used)	01	00000001
9	41	29 2A	Standard timing ID2 (Optional_01h if not used) Standard timing ID3 (Optional_01h if not used)	01	00000001
Standard Timing ID	43	2B	Standard timing ID3 (Optional Oth it not used)	01	00000001
	44	2C	Standard timing ID4 (Optional Oth in not used)	01	00000001
	45	2D	Standard timing ID4 (Optional_01h if not used)	01	00000001
	46	2E	Standard timing ID5 (Optional 01h if not used)	01	00000001
	47	2F	Standard timing ID5 (Optional_01h if not used)	01	00000001
	48	30	Standard timing ID6 (Optional_01h if not used)	01	00000001
	49	31	Standard timing ID6 (Optional 01h if not used)	01	00000001
	50	32	Standard timing ID7 (Optional_01h if not used)	01	00000001
	51	33	Standard timing ID7 (Optional_01h if not used) Standard timing ID8 (Optional_01h if not used)	01	00000001
	52	34	Standard timing ID8 (Optional 01h if not used)	01	00000001
	53	35	Standard timing ID8 (Optional_01h if not used)	01	100000001



APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 2/3

Section		Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
55	I#	54	36	Pixel Clock/10,000 (LSB) 140.1 MHz @ 60 Hz	BA	10111010
ST		55	37	Pixel Clock/10,000 (MSB)	36	00110110
Section Sect		56	38	Horizontal Active (HA) (lower 8 bits) 1920 pixels	80	10000000
Section Sect		57	39	Horizontal Blanking (HB) (lower 8 bits) 172 pixels	AC	10101100
1985 1985		58	3A	Horizontal Active (HA) / Horizontal Blanking (HB) (upper 4:4bits)	70	01110000
67		59	3B	Vertical Avtive (VA) 1080 lines	38	00111000
67	10	60	3C	Vertical Blanking (VB) (DE Blanking typ.for DE only panels) 36 lines	24	00100100
67	ipt	61	3D	Vertical Active (VA) / Vertical Blanking (VB) (upper 4:4bits)	40	01000000
67	SCT	62	3E	Horizontal Front Porch in pixels (HF) (lower 8 bits) 60 pixels	3C	00111100
67	De	63	3F	Horizontal Sync Pulse Width in pixels (HS) (lower 8 bits) 36 pixels	24	00100100
67	00	64	40	Vertical Front Porch in lines (VF): Vertical Sync Pluse Width in lines (VS) (lower 4 bits) 3 lines: 5 lines	35	00110101
67	nin	65	41	Horizontal Front Porch/ Sync Pulse Width/ Vertical Front Porch/ Sync Pulse Width (upper 2bits)	00	00000000
67	Tin	66	42	Horizontal Vedio Image Size (mm) (lower 8 bits) 309 mm	35	00110101
100	2	67	43	Vertical Vedio Image Size (mm) (lower 8 bits) 175 mm	AF	10101111
10		68	44	Horizontal Image Size / Vertical Image Size (upper 4 bits)	10	00010000
1		69	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
172 48 Picel Clock 10,000 (LSB) 93.4 MHz @ 40 Hz 7C 0111 73 49 Picel Clock 10,000 (LSB) 24 0010 74 4A Horizontal Active (HA) (lower 8 bits) 1920 picels 80 1000 75 4B Horizontal Active (HA) (lower 8 bits) 172 picels AC 1010 76 4C Horizontal Active (HA) (Horizontal Blanking (HB) (upper 4-8 bits) 172 picels AC 1010 77 4D Vertical Active (VA) 1000 limes 38 0011 78 4E Vertical Blanking (VB) (DE Blanking (VB) (upper 4-8 bits) 36 lines 24 0010 80 50 Horizontal Force (VA) Vertical Blanking (VB) (upper 4-8 bits) 36 lines 24 0010 81 51 Horizontal Sync Puke Width in pixels (HS) (lower 8 bits) 60 pixels 3C 0011 82 52 Vertical Front Forch in pixels (HS) (lower 8 bits) 36 pixels 24 0010 83 53 Horizontal Sync Puke Width in pixels (HS) (lower 8 bits) 36 pixels 24 0010 84 54 Horizontal Vedio Image Size (mm) (lower 8 bits) 300 mm 35 0011 85 55 Vertical Vedio Image Size (mm) (lower 8 bits) 175 mm AF 1010 86 56 Horizontal Border = 0 (Zero for Notebook LCD) 00 0000 87 57 Horizontal Border = 0 (Zero for Notebook LCD) 00 0000 88 58 Vertical Border = 0 (Zero for Notebook LCD) 00 0000 90 5A Blank for nVDPS 00 0000 91 5B Blank for nVDPS 00 0000 92 5C Blank for nVDPS 00 0000 93 5D Blank for nVDPS 00 0000 94 5E Blank for nVDPS 00 0000 95 66 Blank for nVDPS 00 0000 96 66 Blank for nVDPS 00 0000 97 61 Blank for nVDPS 00 0000 98 62 Blank for nVDPS 00 0000 99 63 Blank for nVDPS 00 0000 100 64 Blank for nVDPS 00 0000 101 65 Blank for nVDPS 00 0000 102 66 Blank for nVDPS 00 0000 103 67 Blank for nVDPS 00 0000 105 69 Blank for nVDPS 00 0000 106 68 Blank for nVDPS 00 0000 107 66 Blank for nVDPS 00 0000 107 67 Blank for nVDPS		70	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
173		71	47	Non-Interlace, Normal display, no stereo, Digital Separate [Vsync_NEG, Hsync_POS (outside of V-sync)]	1A	00011010
Test		72	48	Pixel Clock/10,000 (LSB) 93.4 MHz @ 40 Hz	7C	01111100
Total Horizontal Blanking (HB) (lower 8 bits) 172 pixels AC 1010		73	49	Pixel Clock/10,000 (MSB)		00100100
The function of the function		74	4A	Horizontal Active (HA) (lower 8 bits) 1920 pixels	80	10000000
10		75	4B	Horizontal Blanking (HB) (lower 8 bits) 172 pixels	AC	10101100
S5 S5 Vertical Vedio Image Size (mm) (lower 8 bits) 175 mm AF 1010		76	4C	Horizontal Active (HA) / Horizontal Blanking (HB) (upper 4:4bits)	70	01110000
S5 S5 Vertical Vedio Image Size (mm) (lower 8 bits) 175 mm AF 1010	#2	77	4D	Vertical Avtive (VA) 1080 lines	38	00111000
S5 S5 Vertical Vedio Image Size (mm) (lower 8 bits) 175 mm AF 1010	26	78	4E	Vertical Blanking (VB) (DE Blanking typ.for DE only panels) 36 lines	24	00100100
S5 S5 Vertical Vedio Image Size (mm) (lower 8 bits) 175 mm AF 1010	ipte	79	4F	Vertical Active (VA) / Vertical Blanking (VB) (upper 4:4bits)	40	01000000
S5 S5 Vertical Vedio Image Size (mm) (lower 8 bits) 175 mm AF 1010	CT	80	50	Horizontal Front Porch in pixels (HF) (lower 8 bits) 60 pixels	3C	00111100
S5 S5 Vertical Vedio Image Size (mm) (lower 8 bits) 175 mm AF 1010	Des	81	51	Horizontal Sync Pulse Width in pixels (HS) (lower 8 bits) 36 pixels	24	00100100
S5 S5 Vertical Vedio Image Size (mm) (lower 8 bits) 175 mm AF 1010	00	82	52	Vertical Front Porch in lines (VF): Vertical Sync Pluse Width in lines (VS) (lower 4 bits) 3 lines: 5 lines	35	00110101
S5 S5 Vertical Vedio Image Size (mm) (lower 8 bits) 175 mm AF 1010	iii	83	53	Horizontal Front Porch/ Sync Pulse Width/ Vertical Front Porch/ Sync Pulse Width (upper 2bits)	00	00000000
S5 S5 Vertical Vedio Image Size (mm) (lower 8 bits) 175 mm AF 1010	Ţin.	84	54	Horizontal Vedio Image Size (mm) (lower 8 bits) 309 mm	35	00110101
S7 57 Horizontal Border = 0 (Zero for Notebook LCD)		85	55	Vertical Vedio Image Size (mm) (lower 8 bits) 175 mm	AF	10101111
S8		86	56	Horizontal Image Size / Vertical Image Size (upper 4 bits)	10	00010000
S9 59 Non-Interlace, Normal display, no stereo, Digital Separate [Vsync_NEG, Hsync_POS (outside of V-sync)] 1A 00011		87	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
90	l l	88	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
91 58 Blank for nvDPS 00 00000 92 5C Blank for nvDPS 00 00000 93 5D Blank for nvDPS 00 00000 94 5E Blank for nvDPS 00 00000 95 5F Blank for nvDPS 00 00000 96 60 Blank for nvDPS 00 00000 97 61 Blank for nvDPS 00 00000 98 62 Blank for nvDPS 00 00000 99 63 Blank for nvDPS 00 00000 100 64 Blank for nvDPS 00 00000 101 65 Blank for nvDPS 00 00000 102 66 Blank for nvDPS 00 00000 103 67 Blank for nvDPS 00 00000 104 68 Blank for nvDPS 00 00000 105 69 Blank for nvDPS 00 00000 105 69 Blank for nvDPS 00 000000 106 60 Blank for nvDPS 00 000000000 107 108 1		89	59	Non-Interlace, Normal display, no stereo, Digital Separate [Vsync_NEG, Hsync_POS (outside of V-sync)]	1A	00011010
92 5C Blank for nvDPS 00 000000 93 5D Blank for nvDPS 00 000000 94 5E Blank for nvDPS 00 000000 95 5F Blank for nvDPS 00 000000 96 60 Blank for nvDPS 00 000000 97 61 Blank for nvDPS 00 000000 98 62 Blank for nvDPS 00 000000 99 63 Blank for nvDPS 00 000000 100 64 Blank for nvDPS 00 000000 101 65 Blank for nvDPS 00 000000 102 66 Blank for nvDPS 00 000000 103 67 Blank for nvDPS 00 000000 104 68 Blank for nvDPS 00 000000000 105 69 Blank for nvDPS 00 000000000000000000000000000000		90	5A	Blank for nvDPS	00	00000000
93 5D Blank for nvDPS 00 00000 94 5E Blank for nvDPS 00 00000 95 5F Blank for nvDPS 00 00000 96 60 Blank for nvDPS 00 00000 97 61 Blank for nvDPS 00 00000 98 62 Blank for nvDPS 00 00000 99 63 Blank for nvDPS 00 00000 100 64 Blank for nvDPS 00 00000 101 65 Blank for nvDPS 00 00000 102 66 Blank for nvDPS 00 00000 103 67 Blank for nvDPS 00 00000 104 68 Blank for nvDPS 00 00000 105 69 Blank for nvDPS 00 000000 105 69 Blank for nvDPS 00 000000 106 107 108		91	5B	Blank for nvDPS	00	00000000
SE Blank for nvDPS 00 000000		92	5C	Blank for nvDPS	00	00000000
Page		93	5D	Blank for nvDPS	00	00000000
103 67 Blank for nvDPS 00 00000 104 68 Blank for nvDPS 00 00000 105 69 Blank for nvDPS 00 00000		94	5E	Blank for nvDPS	00	00000000
103 67 Blank for nvDPS 00 00000 104 68 Blank for nvDPS 00 00000 105 69 Blank for nvDPS 00 00000	#3	95	5F	Blank for nvDPS	00	00000000
103 67 Blank for nvDPS 00 00000 104 68 Blank for nvDPS 00 00000 105 69 Blank for nvDPS 00 00000	or	96	60	Blank for nvDPS	00	00000000
103 67 Blank for nvDPS 00 00000 104 68 Blank for nvDPS 00 00000 105 69 Blank for nvDPS 00 00000	ipt	97	61	Blank for nvDPS	00	00000000
103 67 Blank for nvDPS 00 00000 104 68 Blank for nvDPS 00 00000 105 69 Blank for nvDPS 00 00000	SCr	98	62	Blank for nvDPS	00	00000000
103 67 Blank for nvDPS 00 00000 104 68 Blank for nvDPS 00 00000 105 69 Blank for nvDPS 00 00000	De	99	63	Blank for nvDPS	00	00000000
103 67 Blank for nvDPS 00 00000 104 68 Blank for nvDPS 00 00000 105 69 Blank for nvDPS 00 00000	Timing 1	100	64	Blank for nvDPS	00	00000000
103 67 Blank for nvDPS 00 00000 104 68 Blank for nvDPS 00 00000 105 69 Blank for nvDPS 00 00000		101	65	Blank for nvDPS	00	00000000
103 67 Blank for nvDPS 00 00000 104 68 Blank for nvDPS 00 00000 105 69 Blank for nvDPS 00 00000		102	66	Blank for nvDPS	00	00000000
105 69 Blank for nvDPS 00000		103	67	Blank for nvDPS	00	00000000
		104	68	Blank for nvDPS	00	00000000
106 6A Blank for nvDPS 00 00000		105	69	Blank for nvDPS	00	00000000
		106	6A	Blank for nvDPS	00	00000000
107 6B Blank for nvDPS 00 00000		107	6B	Blank for nvDPS	00	00000000



APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 3/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
	108	6C	Detailed Timing Descriptions #4	00	00000000
	109	6D	Flag	00	00000000
	110	6E	Reserved	00	00000000
	111	6F	For Brightness Table and Power consumption	02	00000010
	112	70	Flag	00	00000000
7	113	71	PWM % [7:0] @ Step 0 5 % @ 15 nit	0C	00001100
Timing Descriptor #4	114	72	PWM % [7:0] @ Step 5 20 % @ 60 nit	33	00110011
	115	73	PWM % [7:0] @ Step 10 100 % @ 300 nit	FF	11111111
	116	74	Nits [7:0] @ Step 0	0F	00001111
	117	75	Nits [7:0] @ Step 5	3C	00111100
SI	118	76	Nits [7:0] @ Step 10	96	10010110
iii	119	77	Panel Electronicx Power @ 32 x 32 Chess Pattern = 1000 mW	19	00011001
iii.	120	78	Backlight Power @ 60 nits = 870 mW	16	00010110
	121	79	Backlight Power @ Step 10 = 4000 mW	32	00110010
	122	7A	Nits @ 100% PWM Duty = 300 nit	96	10010110
	123	7B	Flag	00	00000000
	124	7C	Flag	00	00000000
	125	7D	Flag	00	00000000
Checksum	126	7E	Extension flag (# of optional 128 panel ID extension block to follow, Typ = 0)	00	00000000
	127	7F	Check Sum (The 1-byte sum of all 128 bytes in this panel ID block shall = 0)	FB	11111011