☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: N140BGE
SUFFIX: L33

Customer:

APPROVED BY   **SIGNATURE**

<u>**Name / Title**</u>

Please return 1 copy for your confirmation with your signature and comments.

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2014-04-24	2014-04-17	2014-04-08
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PRODUCT SPECIFICATION
CONTENTS

REVISION HISTORY

Version	Date	Page	Description
0.0	Sep. 3, 2012	All	Tentative Spec Ver.0.0 was first issued.
1.0	Nov. 9, 2012	All	Preliminary Spec Ver.1.0 was first issued.
2.0	Feb. 5, 2013	All	Approval Spec Ver.2.0 was first issued.
3.0	Feb. 18, 2013	All	Approval Spec Ver.3.0 was first issued.
3.1	Apr. 4, 2014	P.5,P.12 P.14,P.19 , P28,	Spec was modified due to "Brightness changes from 200nits to 220nits"
		P.5	Add '' 2.MECHANICAL SPECIFICATIONS 'S Note (2) "
		P.33	Modify " Appendix. SYSTEM COVER DESIGN NOTICE"
		P.41	Add" Appendix. LCD MODULE HANDLING MANUAL"

PRODUCT SPECIFICATION

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N140BGE-L33 is a 14.0" (14.0" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 40 pins LVDS interface. This module supports 1366 x 768 HD mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 GENERAL SPECIFICATI0NS

| Item	Specification	Unit	Note
Screen Size	14.0" diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1366 x R.G.B. x 768	pixel	-
Pixel Pitch	0.2265 (H) x 0.2265 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Color Gamma	45%	NTSC	Typ.
Luminance, White	220	Cd/m2	
Power Consumption	Total 3.059 W (Max.) @ cell 0.739 W (Max.), BL 2.32 W (Max.)		(1)

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

	Item	Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	319.9	320.4	320.9	mm	(1) (2)
	Vertical (V)	186.6	187.1	187.6	mm	
	Vertical (V) with PCB & Bracket	204.6	205.1	205.6	mm	
	Thickness (T)	-	-	3.6	mm	
	Thickness (T) with PCB & Bracket	-	-	3.6	mm	Slim Bend
Polarizer Area	Horizontal	312.4	312.7	313.0	mm	
	Vertical	177.05	177.25	177.45	mm	
Active Area	Horizontal	309.299	309.399	309.499	mm	
	Vertical	173.852	173.952	174.052	mm	
Weight		-	310	320	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Dimensions are measured by caliper.
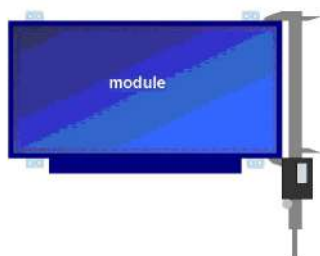
2.1 CONNECTOR TYPE
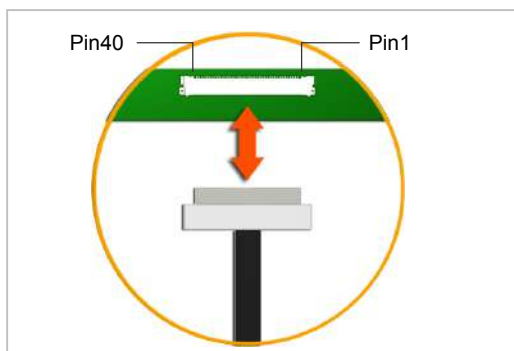
Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-040E-12

User's connector Part No: IPEX-20453-040T-01

3. ABSOLUTE MAXIMUM RATINGS

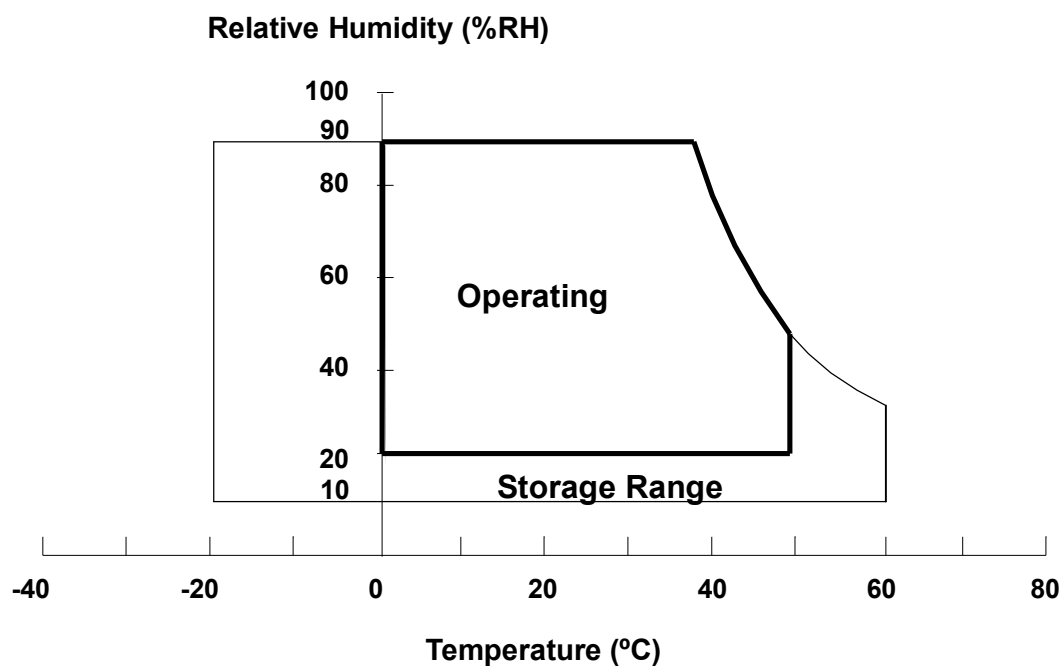## 3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	℃	(1)
Operating Ambient Temperature	T_{OP}	0	+50	℃	(1), (2)

Note (1)   (a) 90 %RH Max. (Ta < 40 ℃).

           (b) Wet-bulb temperature should be 39 ℃ Max. (Ta < 40 ℃).

           (c) No condensation.

Note (2)   The temperature of panel surface should be 0 ℃ min. and 60 ℃ max.

Relative Humidity (%RH)

Temperature (ºC)

3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	26.0	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	5.0	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	5.0	V	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM
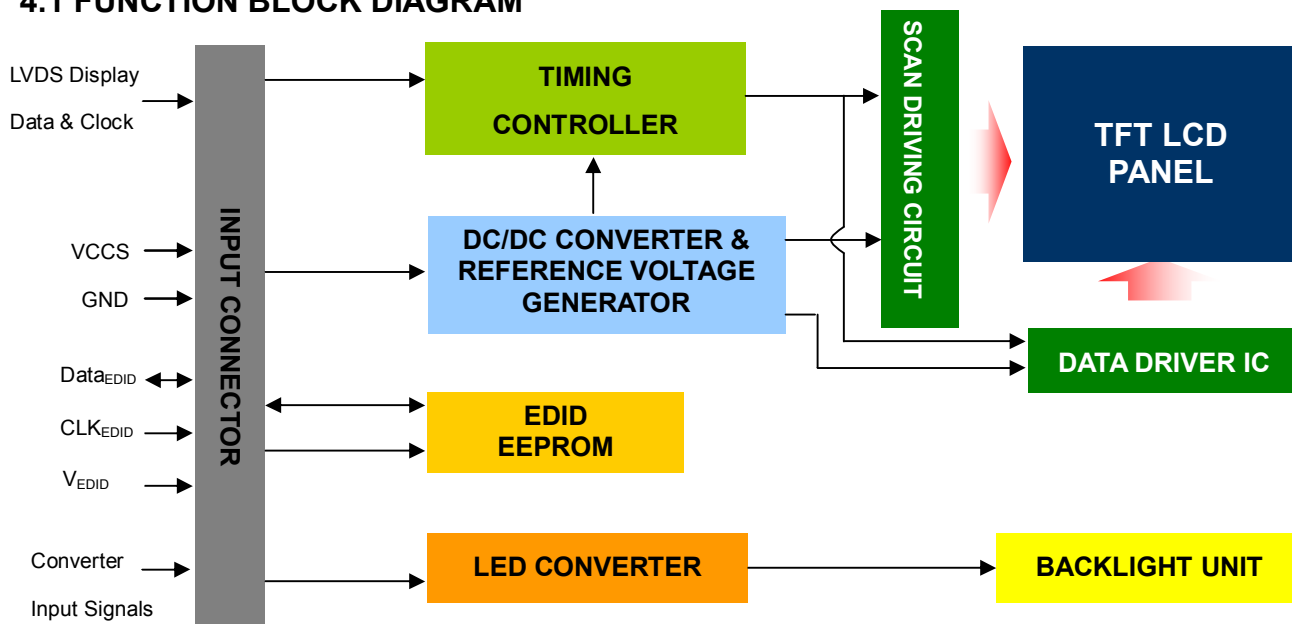

4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserve)	
2	VCCS	Power Supply (3.3V typ.)	
3	VCCS	Power Supply (3.3V typ.)	
4	VEDID	DDC 3.3V power	
5	NC	No Connection (Reserved for INNOLUX test)	
6	CLKEDID	DDC clock	
7	DATAEDID	DDC data	
8	Rxin0-	LVDS differential data input	R0-R5, G0
9	Rxin0+	LVDS differential data input	
10	VSS	Ground	
11	Rxin1-	LVDS differential data input	G1~G5, B0, B1
12	Rxin1+	LVDS differential data input	
13	VSS	Ground	
14	Rxin2-	LVDS Differential Data Input	B2-B5,HS,VS, DE
15	Rxin2+	LVDS Differential Data Input	
16	VSS	Ground	
17	RxCLK-	LVDS differential clock input	LVDS CLK
18	RxCLK+	LVDS differential clock input	
19	VSS	Ground	
20	NC	No Connection (Reserve)	
21	NC	No Connection (Reserve)	
22	VSS	Ground	

23	NC	No Connection (Reserve)	
24	NC	No Connection (Reserve)	
25	VSS	Ground	
26	NC	No Connection (Reserve)	
27	NC	No Connection (Reserve)	
28	VSS	Ground	
29	NC	No Connection (Reserve)	
30	NC	No Connection (Reserve)	
31	LED_GND	LED Ground	
32	LED_GND	LED Ground	
33	LED_GND	LED Ground	
34	NC	No Connection (Reserve)	
35	LED_PWM	PWM Control Signal of LED Converter	
36	LED_EN	Enable Control Signal of LED Converter	
37	NC	No Connection (Reserve)	
38	LED_VCCS	LED Power Supply	
39	LED_VCCS	LED Power Supply	
40	LED_VCCS	LED Power Supply	

Note (1)　The first pixel is odd as shown in the following figure.
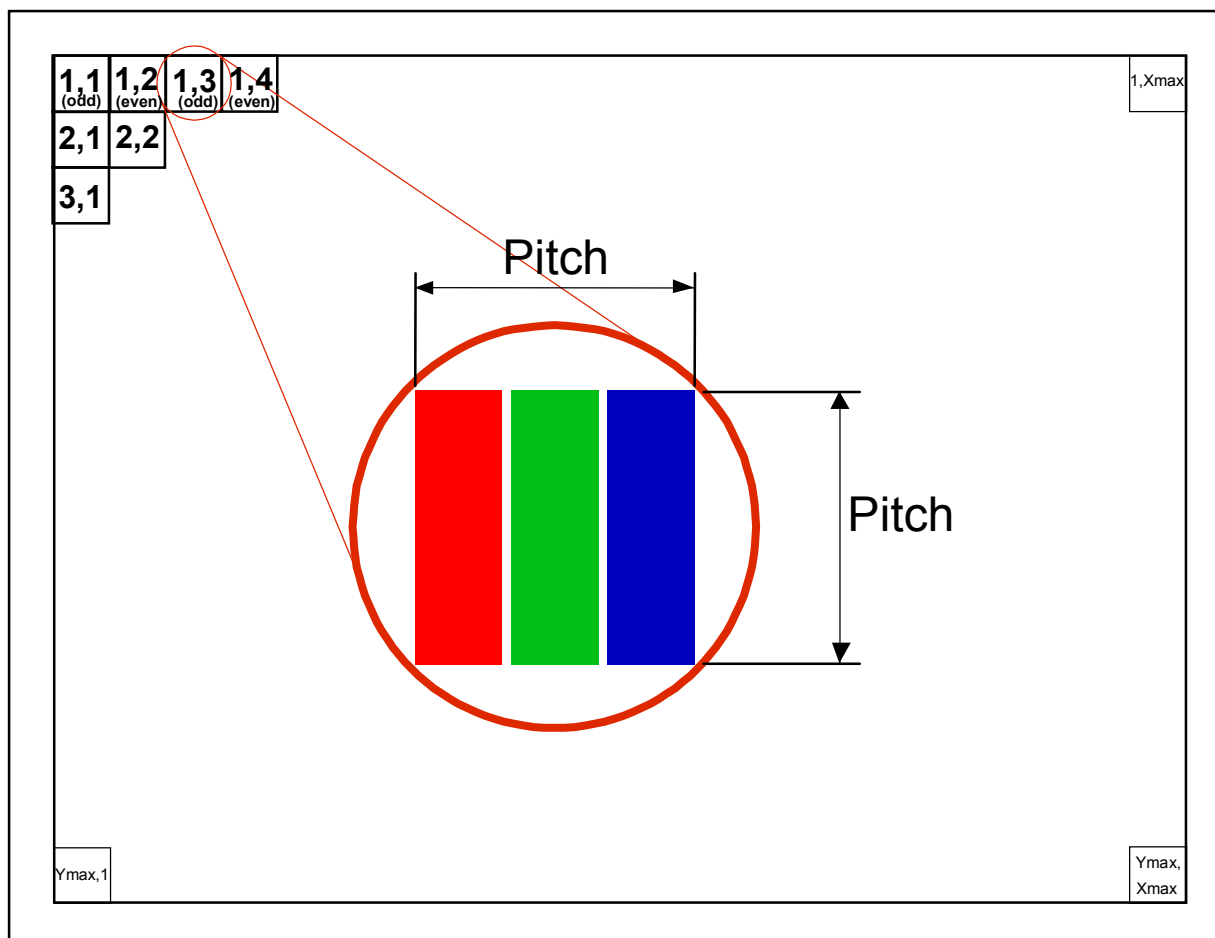
4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)
Ripple Voltage		V_{RP}	-	50	-	mV	(1)
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	Icc	-	206	224	mA	(3)a
	Black		-	201	219	mA	(3)

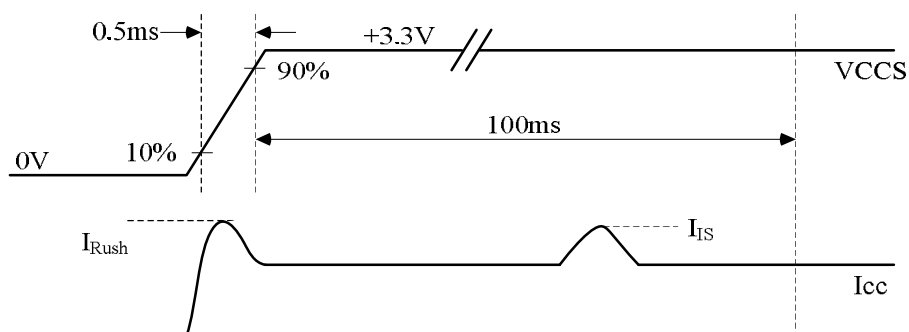Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

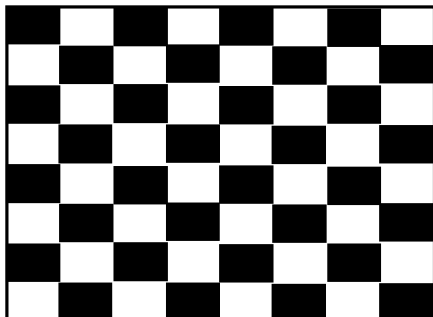Measurement Conditions: Shown as the following figure. Test pattern: black.
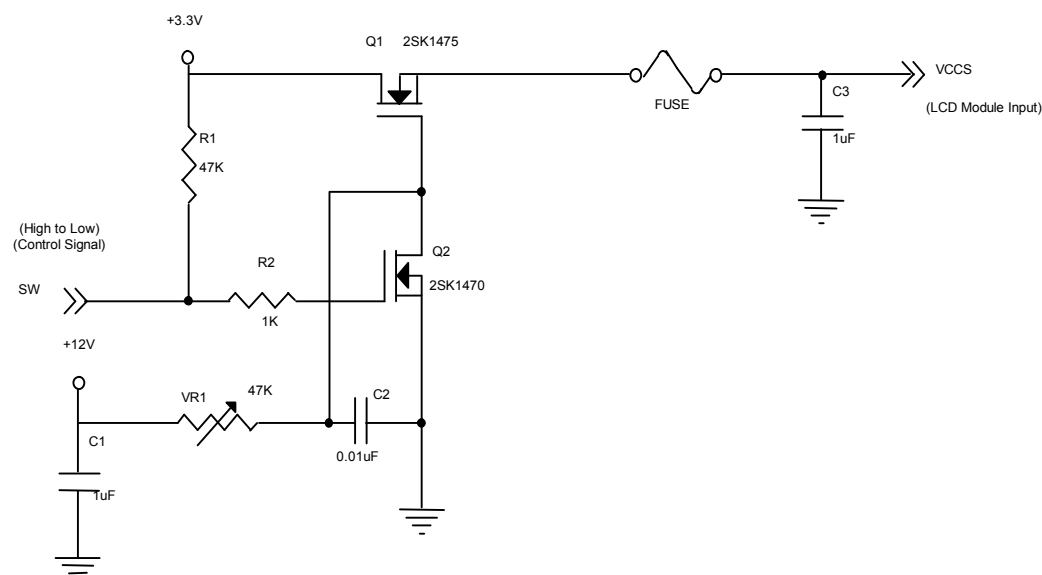
VCCS rising time is 0.5ms

Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ℃, DC

Current and f_v = 60 Hz, whereas a specified power dissipation check pattern is displayed.

a. Mosaic Pattern

Active Area

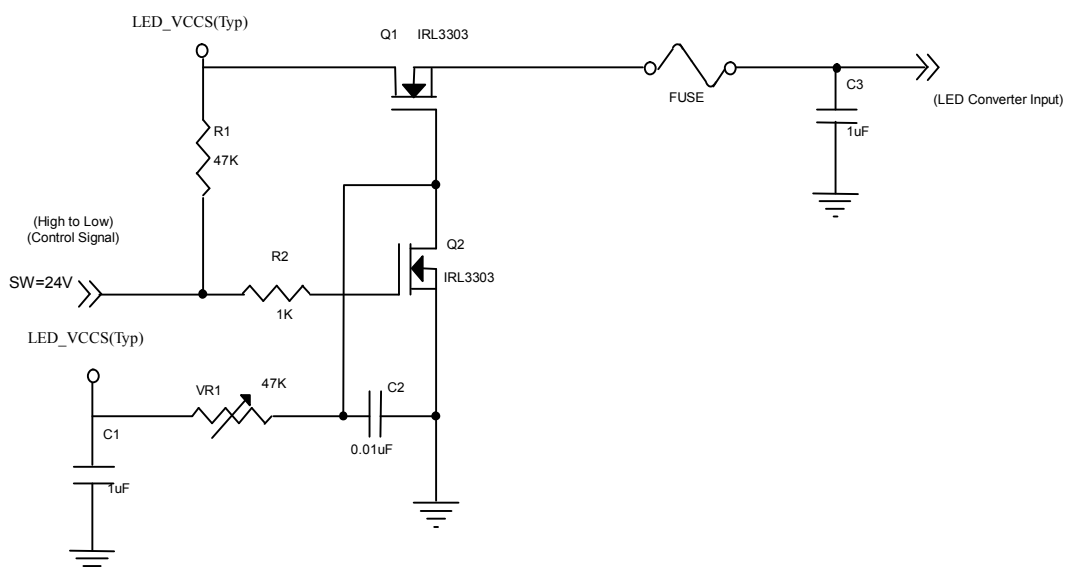### 4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	5.0	12.0	21.0	V	
Converter Inrush Current		ILED$_{RUSH}$	-	-	1.5	A	(1)
LED_EN Control Level	Backlight On		2.2	-	5.0	V	(4)
	Backlight Off		0	-	0.6	V	(4)
LED_EN Impedance		R$_{LED\_EN}$	30K	-	-	ohm	(4)
PWM Control Level	PWM High Level		2.2	-	5.0	V	(4)
	PWM Low Level		0	-	0.6	V	(4)
PWM Impedance		R$_{PWM}$	30K	-	-	ohm	(4)
PWM Control Duty Ratio			5	-	100	%	
PWM Control Permissive Ripple Voltage		VPWM_pp	-	-	100	mV	
PWM Control Frequency		f$_{PWM}$	190	-	2K	Hz	(2)
LED Power Current LED_VCCS =Typ.		ILED	157	184	193	mA	(3)

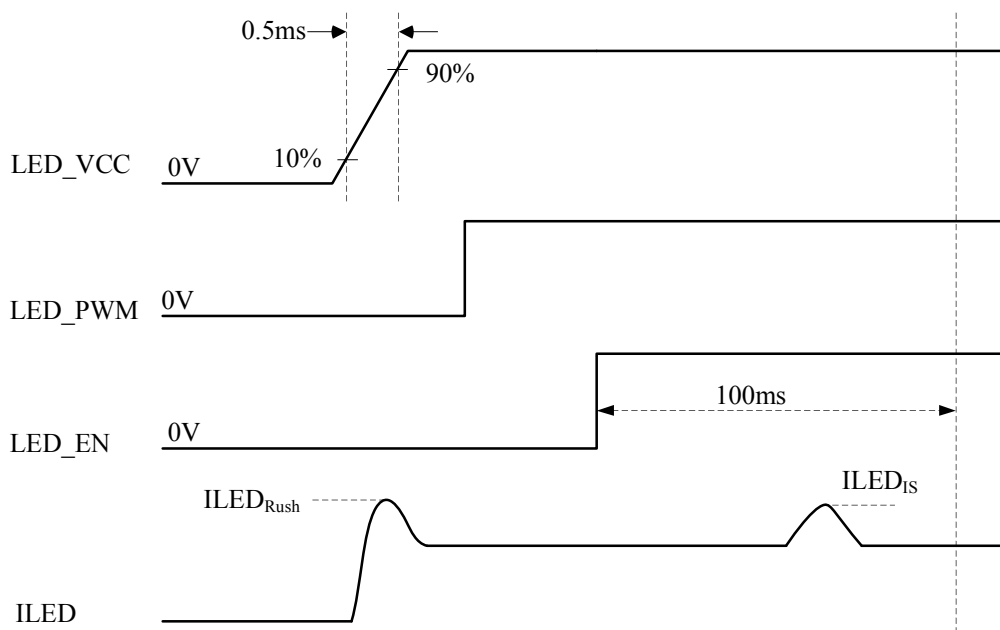Note (1) ILED$_{RUSH}$: the maximum current when LED_VCCS is rising,

ILED$_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ℃, f$_{PWM}$ = 200 Hz, Duty=100%.

PRODUCT SPECIFICATION

VLED rising time is 0.5ms

Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

$$N : \text{Integer} \ (N \geq 3)$$

$$f : \text{Frame rate}$$

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (If it exists). The rest pull down impedances of other signal (eg. PWM) are in the same concept.
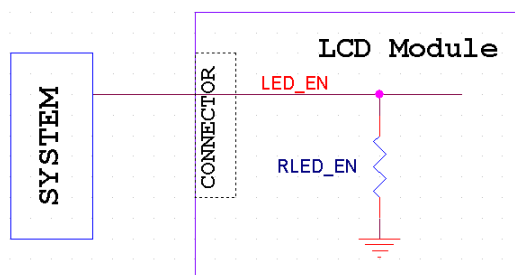
4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	23.4	26.1	27	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	-	69	-	mA	
Power Consumption	P_L	-	1.80	1.86	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1)   LED current is measured by utilizing a high frequency current meter as shown below :

$V_{L,} I_L$

LED
Light Bar

Light Bar Feedback

Channels
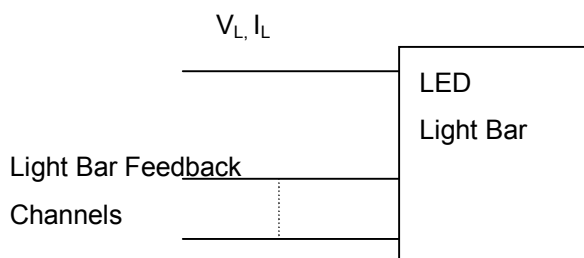
Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 ^{o}C and I_L = 23 mA(Per EA) until the brightness becomes $\leq$ 50% of its original value.

### 4.4 LVDS INPUT SIGNAL TIMING SPECIFICATIONS

4.4.1 LVDS DC SPECIFICATIONS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LVDS Differential Input High Threshold	$V_{TH(LVDS)}$	-	-	+100	mV	(1), V_{CM}=1.2V
LVDS Differential Input Low Threshold	$V_{TL(LVDS)}$	-100	-	-	mV	(1) V_{CM}=1.2V
LVDS Common Mode Voltage	V_{CM}	1.125	-	1.375	V	(1)
LVDS Differential Input Voltage	$|V_{ID}|$	100	-	600	mV	(1)
LVDS Terminating Resistor	R_T		100		Ohm	-

Note (1) The parameters of LVDS signals are defined as the following figures.
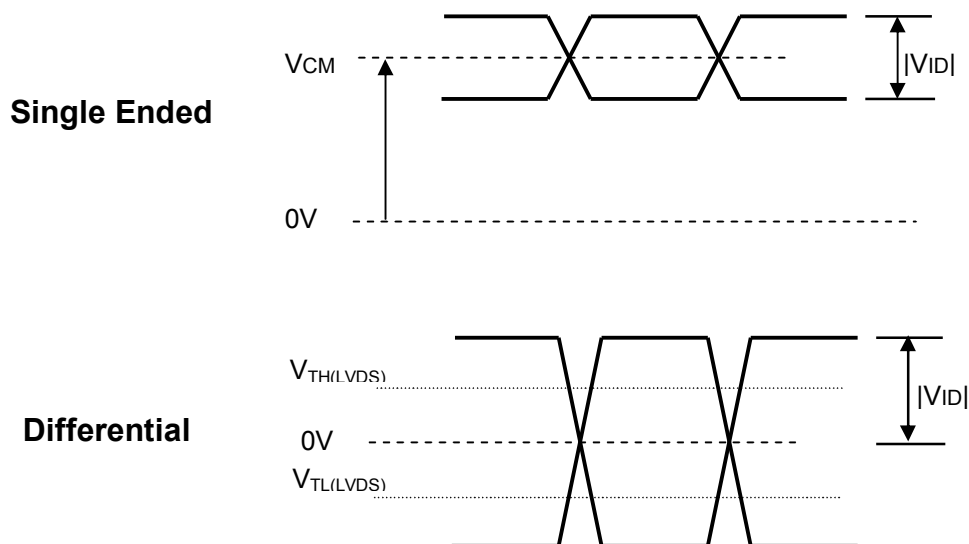
4.4.2 LVDS DATA FORMAT

Signal for 1 DCLK Cycle (T)
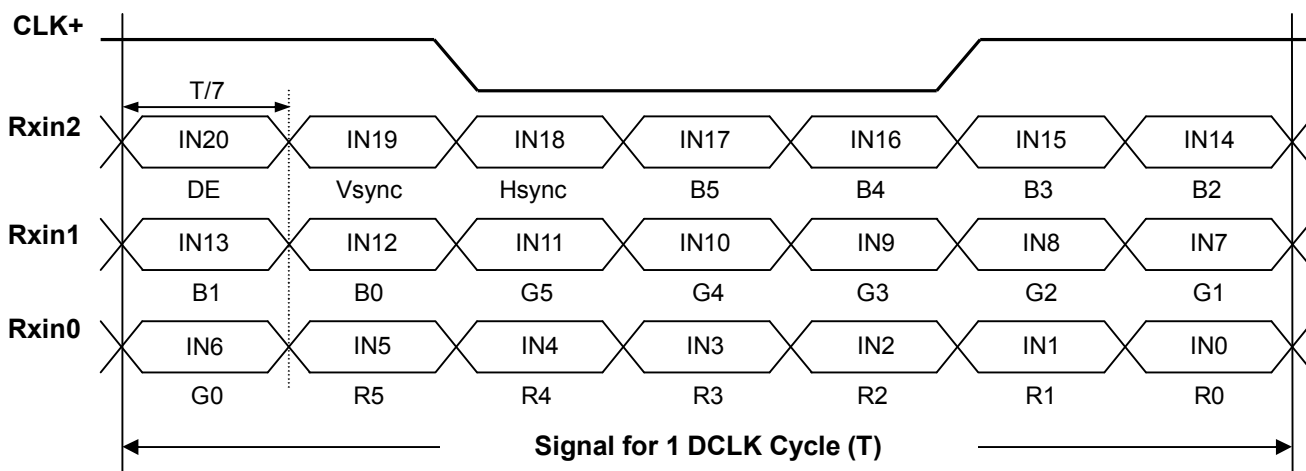
4.4.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	72.6	76.42	80.24	MHz	-
DE	Vertical Total Time	TV	775	800	808	TH	-
	Vertical Active Display Period	TVD	768	768	768	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	32	TV-TVD	TH	-
	Horizontal Total Time	TH	1466	1592	1648	Tc	-
	Horizontal Active Display Period	THD	1366	1366	1366	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	226	TH-THD	Tc	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

INPUT SIGNAL TIMING DIAGRAM
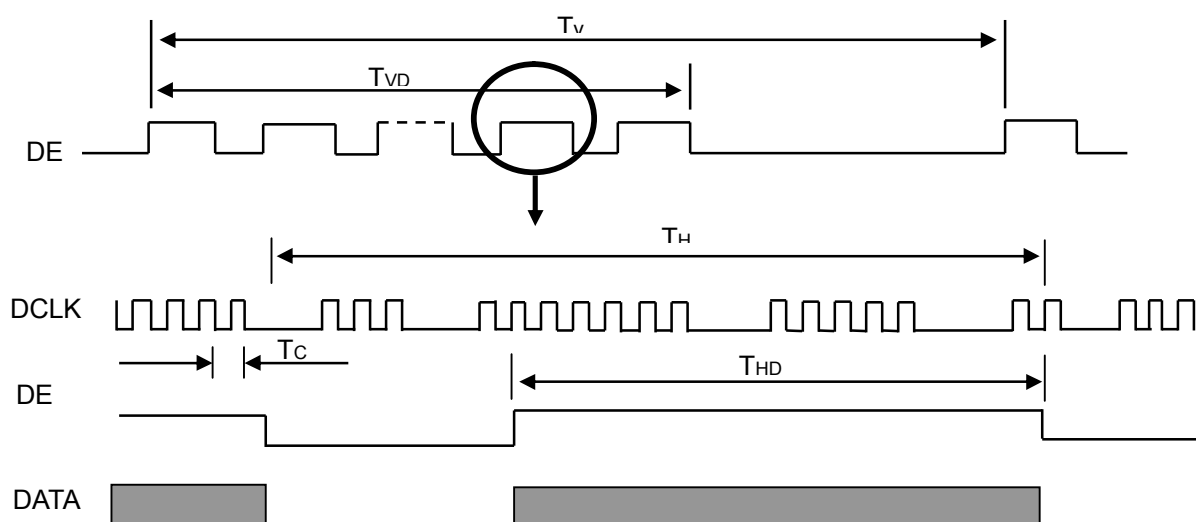
4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.

Symbol	Value			Unit	Note
	Min.	Typ.	Max.		
t1	0.5	-	10	ms	
t2	0	-	50	ms	
t3	0	-	50	ms	
t4	500	-	-	ms	
t5	200	-	-	ms	
t6	200	-	-	ms	
t7	0.5	-	10	ms	
t_A	0.5	-	10	ms	
t_B	0	-	10	ms	
t_C	1	-	-	ms	
t_D	1	-	-	ms	
t_E	1	-	-	ms	
t_F	1	-	-	ms	
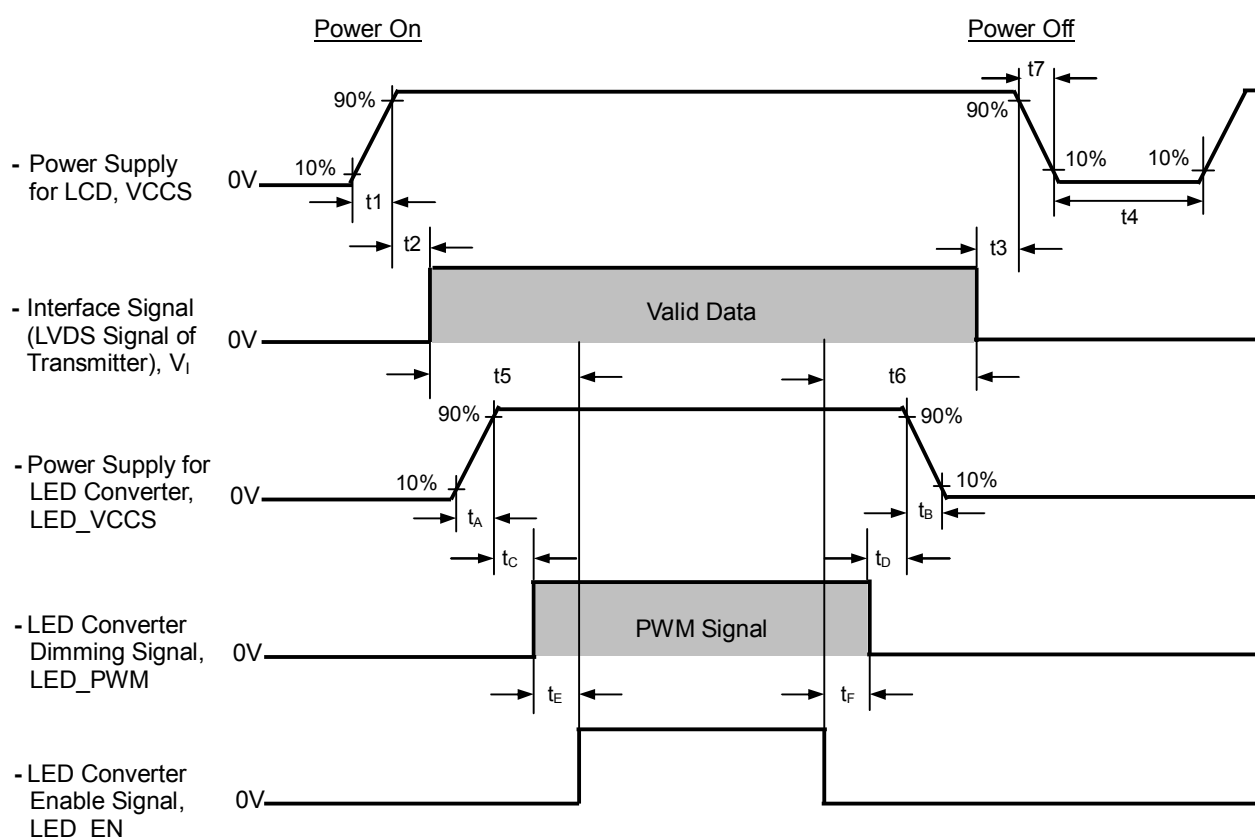
Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) Please avoid floating state of the interface signal during signal invalid period.

Note (3) It is recommended that the backlight power must be turned on after the power supply for LCD and the interface signal is valid.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	^oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	69	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		350	500	-	-	(2), (5) (7)
Response Time		T_R		-	3	8	ms	(3),(7)
		T_F		-	7	12	ms	
Average Luminance of White		L_{AVE}		187	220	-	cd/m²	(4), (6),(7)
Color Chromaticity	Red	Rx	θ_x=0°, θ_Y=0° Viewing Normal Angle	Typ – 0.03	0.575	Typ + 0.03	-	(1),(7)
		Ry			0.335		-	
	Green	Gx			0.327		-	
		Gy			0.580		-	
	Blue	Bx			0.157		-	
		By			0.137		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	40	45		Deg.	(1),(5), (7)
		θ_x-		40	45	-		
	Vertical	θ_Y+		15	20	-		
		θ_Y-		40	45	-		
White Variation of 5 Points		δW_{5p}	θ_x=0°, θ_Y=0°	80	-	-	%	(5),(6), (7)

Note (1) Definition of Viewing Angle (θx, θy):
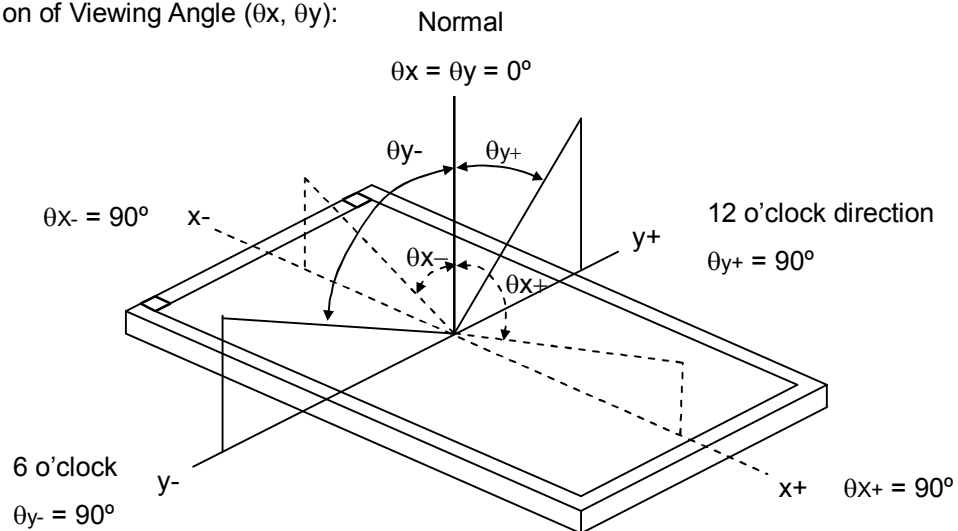
Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):
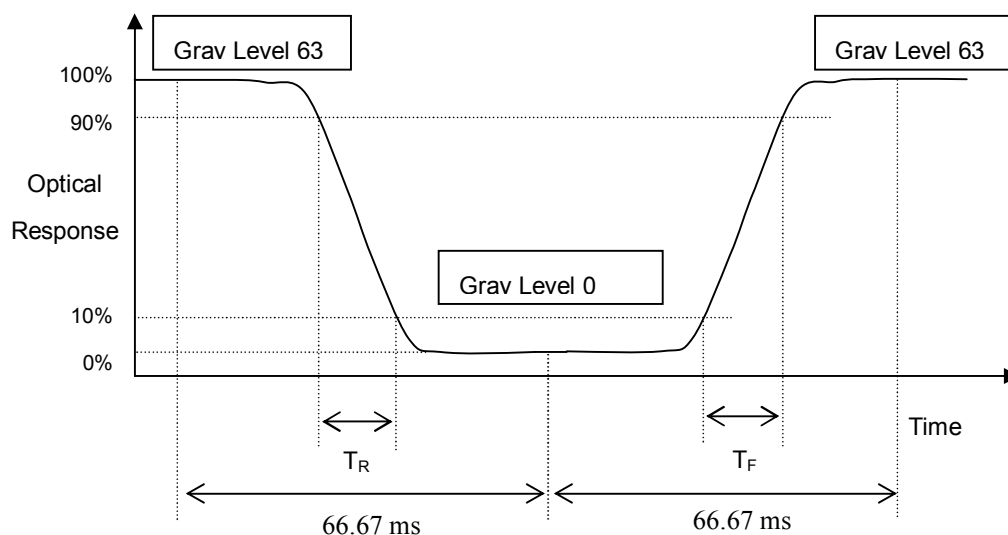
Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of White at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

LCD Module

LCD Panel

USB2000   or equivalent

CS-2000T   or equivalent

Center of the Screen

500 mm

Light Shield Room

(Ambient Luminance < 2 lux)
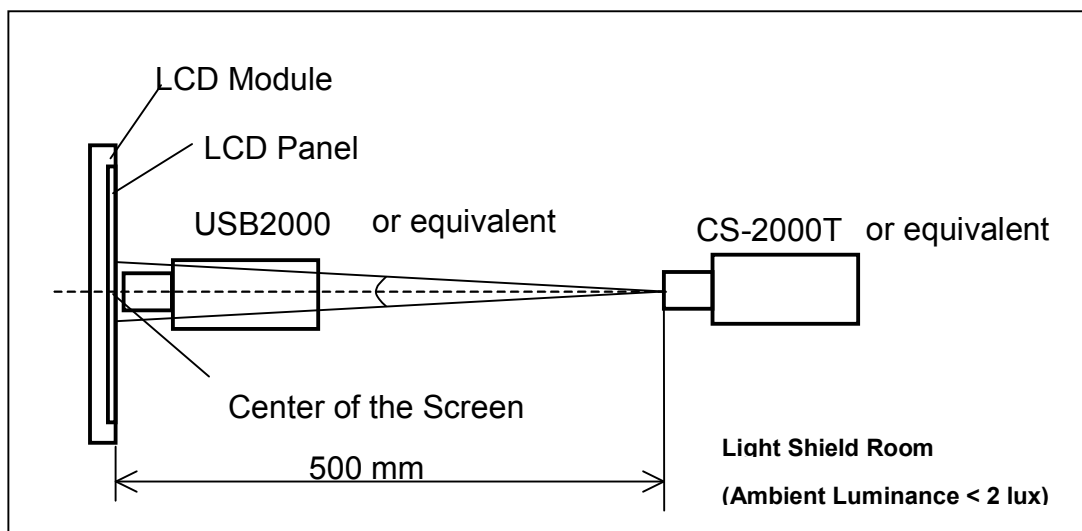
Note (6) Definition of White Variation (δW):

Measure the luminance of White at 5 points

δW_{5p} = {Minimum [L (1)~L (5)] / Maximum [L (1)~ L (5)]}*100%

$\bigotimes$: Test Point

X=1 to 13

Active area
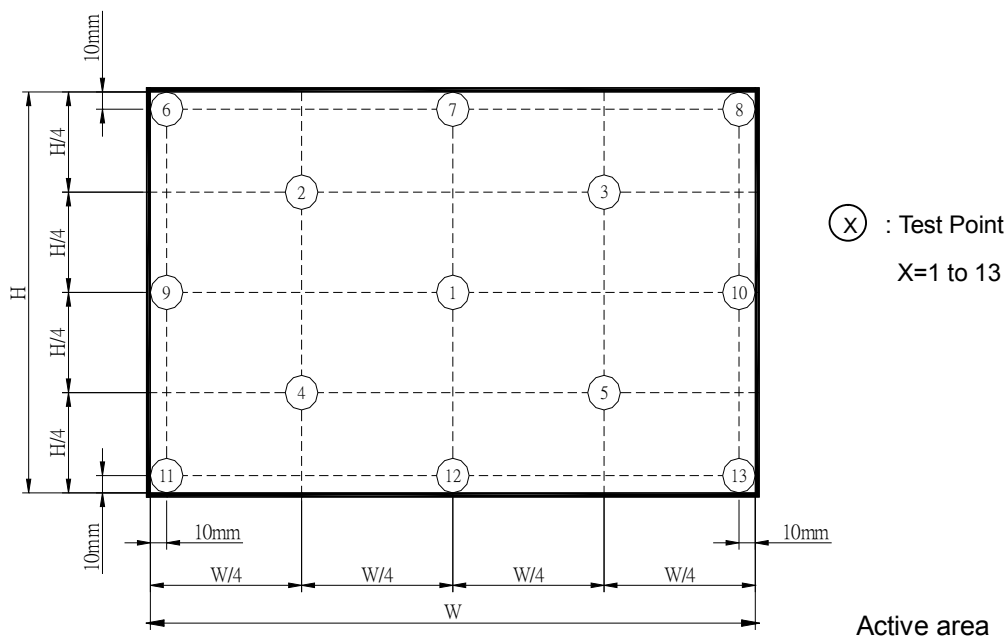
Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour ⟷ 60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	(1) (2)
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50°C, 80% RH, 240 hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N140BGE – L33

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X X Y M D X N N N N

- Serial No.
- INX Internal Use
- Year, Month, Date
- INX Internal Use
- Revision
- INX Internal Use
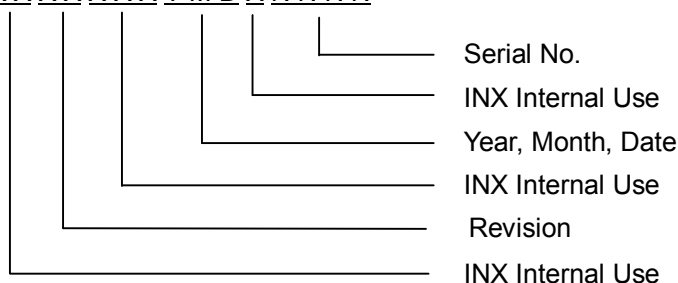
(d) Production Location: MADE IN XXXX.

(e) UL Logo：XXXX is UL factory ID.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

CT Label

S/N	CT: CEDQNRR5CXXXX
CT:	Title
C	LCD Display Module
EDQN	Assembly Code
XX	Revision (Current is 02)
5C	Supplier /Site of MFG
XX	Week/Year of MFG
XXX	Serial number. From 000000 to 999999

7.2 CARTON

(1)Box Dimensions : 435(L)*350(W)*275(H)
(2)20 Modules/Carton
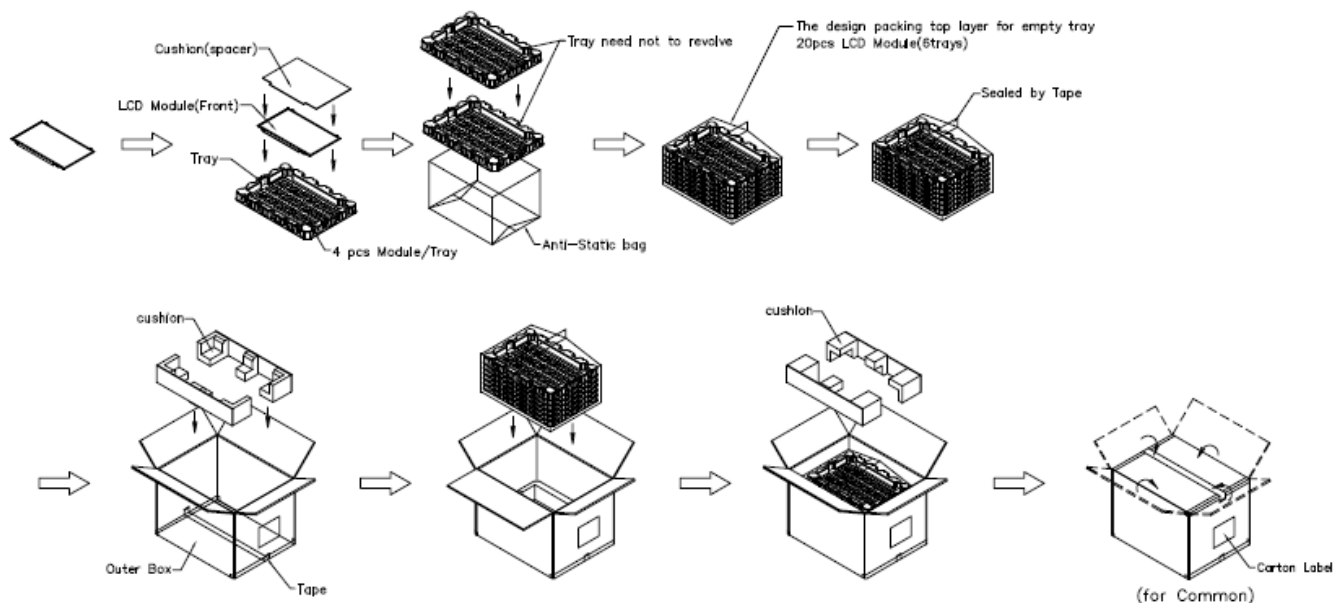
Figure. 7-1 Packing method

7.3 PALLET

Sea & Land Transportation

Air Transportation
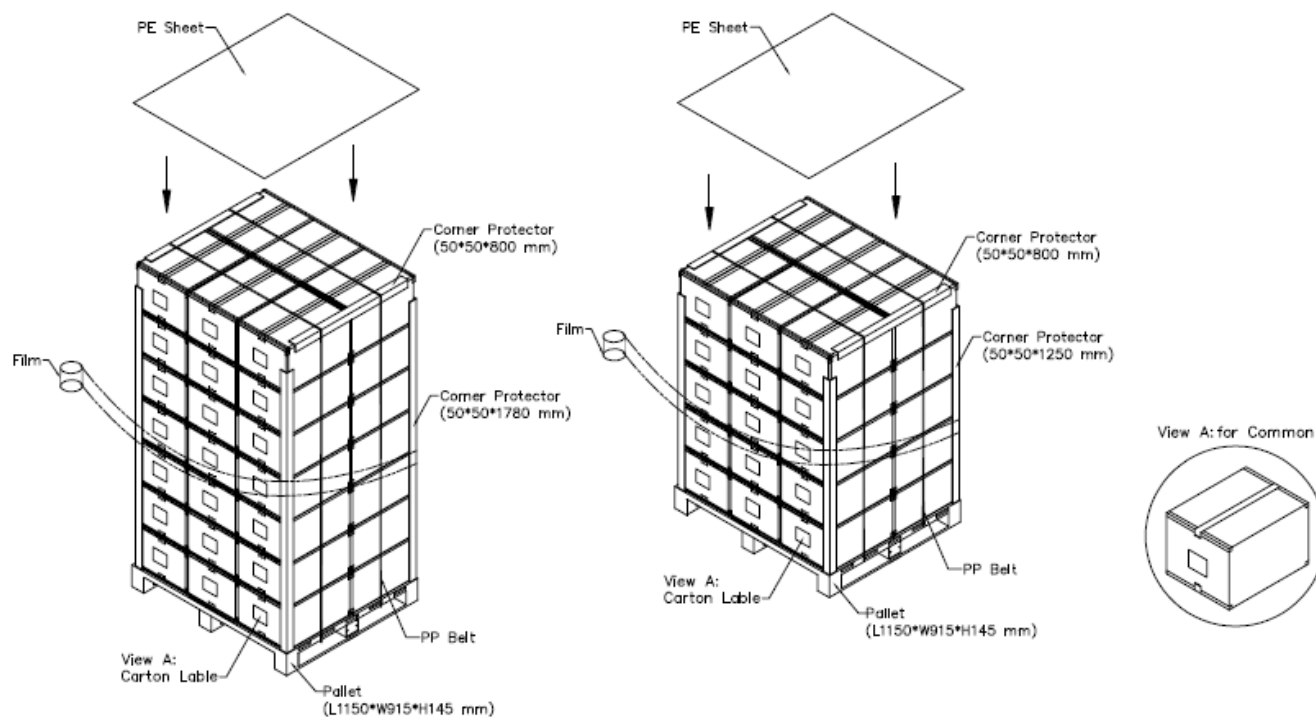
Figure. 7-2 Packing method

7.4 UN-PACKAGING METHOD
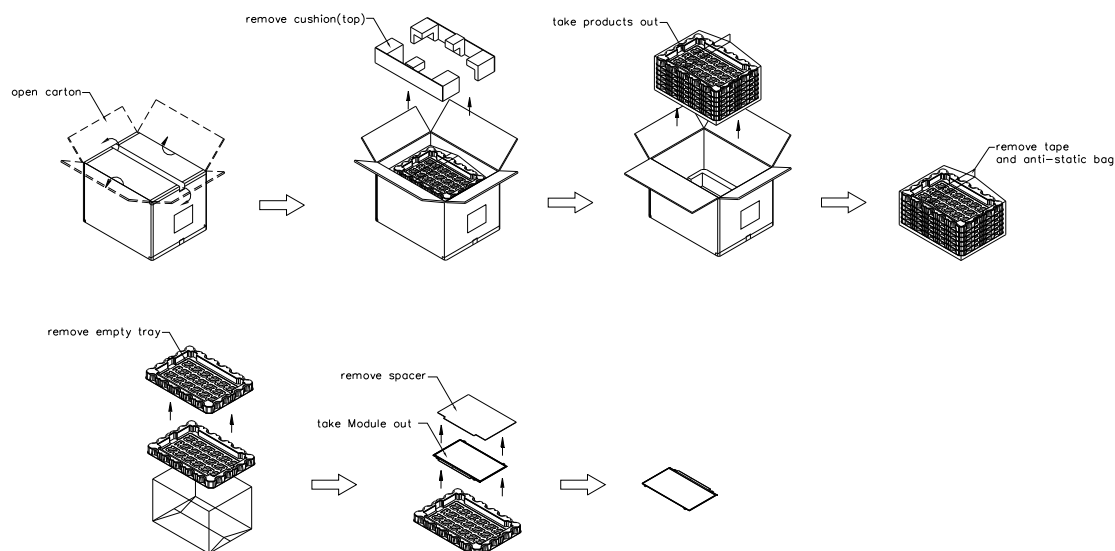
Figure. **7.3** un-packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the INXS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the

VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMN")	0D	00001101
9	9	EISA ID manufacturer name	AE	10101110
10	0A	ID product code (LSB)	99	10011001
11	0B	ID product code (MSB)	14	00010100
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	33	00110011
17	11	Year of manufacture (fixed year code)	17	00010111
18	12	EDID structure version ("1")	01	00000001
19	13	EDID revision ("4")	04	00000100
20	14	Video I/P definition ("Digital")	90	10010000
21	15	Active area horizontal ("30.94cm")	1F	00011111
22	16	Active area vertical ("17.4cm")	11	00010001
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB, Non-continous")	02	00000010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	7E	01111110
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	45	01000101
27	1B	Rx=0.575	93	10010011
28	1C	Ry=0.335	55	01010101
29	1D	Gx=0.327	53	01010011
30	1E	Gy=0.58	94	10010100
31	1F	Bx=0.157	28	00101000
32	20	By=0.137	23	00100011
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001

41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("76.42MHz")	DA	11011010
55	37	# 1 Pixel clock (hex LSB first)	1D	00011101
56	38	# 1 H active ("1366")	56	01010110
57	39	# 1 H blank ("226")	E2	11100010
58	3A	# 1 H active : H blank	50	01010000
59	3B	# 1 V active ("768")	00	00000000
60	3C	# 1 V blank ("32")	20	00100000
61	3D	# 1 V active : V blank	30	00110000
62	3E	# 1 H sync offset ("68")	44	01000100
63	3F	# 1 H sync pulse width ("45")	2D	00101101
64	40	# 1 V sync offset : V sync pulse width ("4 : 7")	47	01000111
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
66	42	# 1 H image size ("309 mm")	35	00110101
67	43	# 1 V image size ("174 mm")	AE	10101110
68	44	# 1 H image size : V image size	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
72	48	Detailed timing description # 2 Pixel clock ("50.95MHz")	E7	11100111
73	49	# 2 Pixel clock (hex LSB first)	13	00010011
74	4A	# 2 H active ("1366")	56	01010110
75	4B	# 2 H blank ("226")	E2	11100010
76	4C	# 2 H active : H blank	50	01010000
77	4D	# 2 V active ("768")	00	00000000
78	4E	# 2 V blank ("32")	20	00100000
79	4F	# 2 V active : V blank	30	00110000
80	50	# 2 H sync offset ("68")	44	01000100
81	51	# 2 H sync pulse width ("45")	2D	00101101
82	52	# 2 V sync offset : V sync pulse width ("4 : 7")	47	01000111
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
84	54	# 2 H image size ("309 mm")	35	00110101
85	55	# 2 V image size ("174 mm")	AE	10101110
86	56	# 2 H image size : V image size	10	00010000

87	57	# 2 H boarder ("0")	00	00000000
88	58	# 2 V boarder ("0")	00	00000000
89	59	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
90	5A	NA	00	00000000
91	5B	NA	00	00000000
92	5C	NA	00	00000000
93	5D	NA	00	00000000
94	5E	NA	00	00000000
95	5F	NA	00	00000000
96	60	NA	00	00000000
97	61	NA	00	00000000
98	62	NA	00	00000000
99	63	NA	00	00000000
100	64	NA	00	00000000
101	65	NA	00	00000000
102	66	NA	00	00000000
103	67	NA	00	00000000
104	68	NA	00	00000000
105	69	NA	00	00000000
106	6A	NA	00	00000000
107	6B	NA	00	00000000
108	6C	Detailed Timing Description #4	00	00000000
109	6D	Flags	00	00000000
110	6E	Reserved	00	00000000
111	6F	For Brightness Table and Power Consumption	02	00000010
112	70	Flags	00	00000000
113	71	PWM % [7:0] @ Step 0 = 5%	0C	00001100
114	72	PWM % [7:0] @ Step 5 = 26%	42	01000010
115	73	PWM % [7:0] @ Step 10 = 100%	FF	11111111
116	74	Nits [7:0] @ Step 0 = 11.84nits	0B	00001011
117	75	Nits [7:0] @ Step 5 = 60nits	3C	00111100
118	76	Nits [7:0] @ Step 10 = 220nits	6E	01101110
119	77	Panel Electronics Power @32x32 Chess Pattern =627mW	0F	00001111
120	78	Backlight Power @60 nits =584mW	0E	00001110
121	79	Backlight Power @Step 10 =2111mW	1A	00011010
122	7A	Nits @ 100% PWM Duty =226.42nit	71	01110001
123	7B	Flags	00	00000000
124	7C	Flags	00	00000000
125	7D	Flags	00	00000000
126	7E	Extension flag	00	00000000
127	7F	Checksum	AD	10101101

Appendix. OUTLINE DRAWING

Active Area

SEE DETAIL A

SEE DETAIL B

SEE DETAIL C

SEE DETAIL D

SYSTEM BEZEL OPENING NO MORE THAN 1.0MM
LARGER THAN ACTIVE AREA ON ALL 4 SIDE

320.4±0.5(OUTLINE)
312.7±0.3(CF POLARIZER)
309.399±0.100(ACTIVE AREA)
267.4±0.3

23.5±0.3
(2-20)

4-0.8±0.2

(1.5)(AA TO POLARIZER)
4.55±0.50(AA~Outline)
91.28±0.30
159.25±0.30
4.3±0.5(AA~Outline)

(1.5)(AA TO POLARIZER)

(6.45)(AA~Outline)
(1.8)(AA TO POLARIZER)

(1.8)(AA TO POLARIZER)
(8.85)(AA~Outline)

205.1±0.5
4-193.5±0.3
187.1±0.5(OUTLINE)
177.25±0.20(CF POLARIZER)
173.952±0.100(ACTIVE AREA)

(R2)
1.2±0.3
3.6 MAX

(2-29)
32.5±0.3
(50.2)
220(PCB LENGTH)
249.4±0.3

DETAIL A
SCALE 2:1
2-13
6.0±0.1
2-Φ2.4
2-6.5
3.2±0.2

DETAIL B
SCALE 2:1
3.5
6.0±0.1
2-0.5
2-R1.2
3.2±0.2

DETAIL C
SCALE 2:1
2-Φ2.4
2-6.5
3.2±0.2
2-13
6.0±0.1

DETAIL D
SCALE 2:1
2-0.5
2-R1.2
3.5
6.0±0.1
3.2±0.2

239.35(COF CENTER)
79.31(COF CENTER)
2-42.5
2-32.5
6.8
5.8
Tcon
6.45(TCON CENTER)
157.6(TCON CENTER)
PCBA LABEL

COF AND TCON LOCATIONS
SEE NOTES FOR EXPLANATION
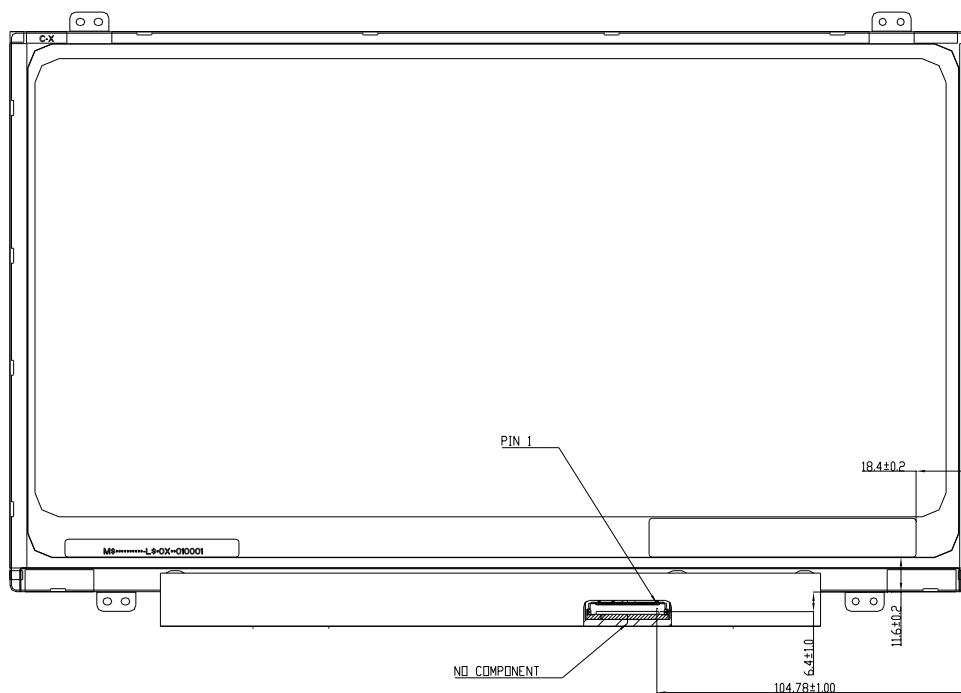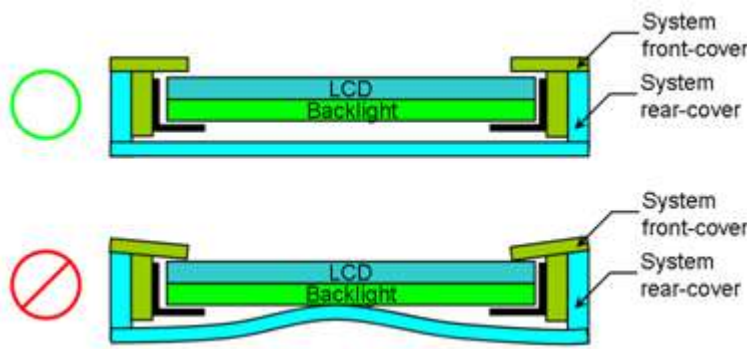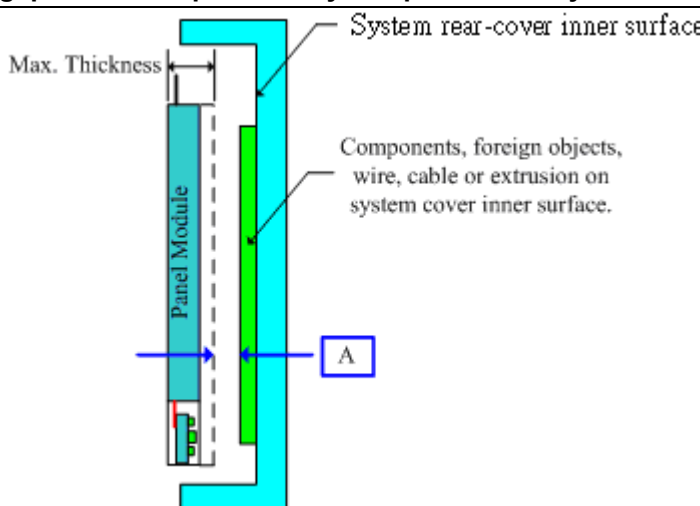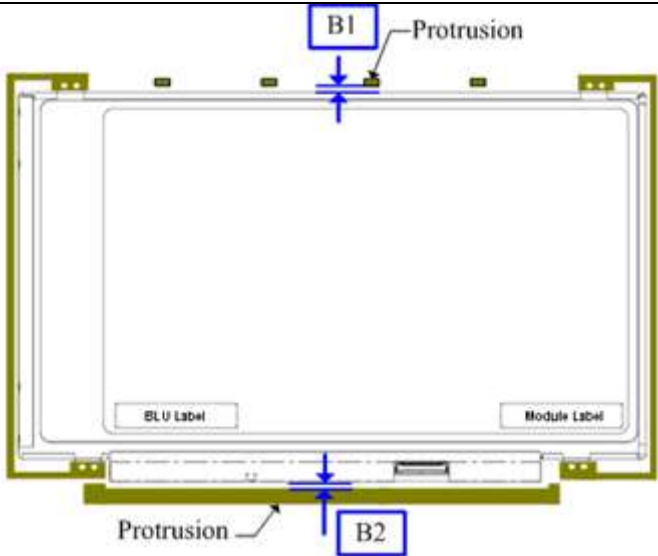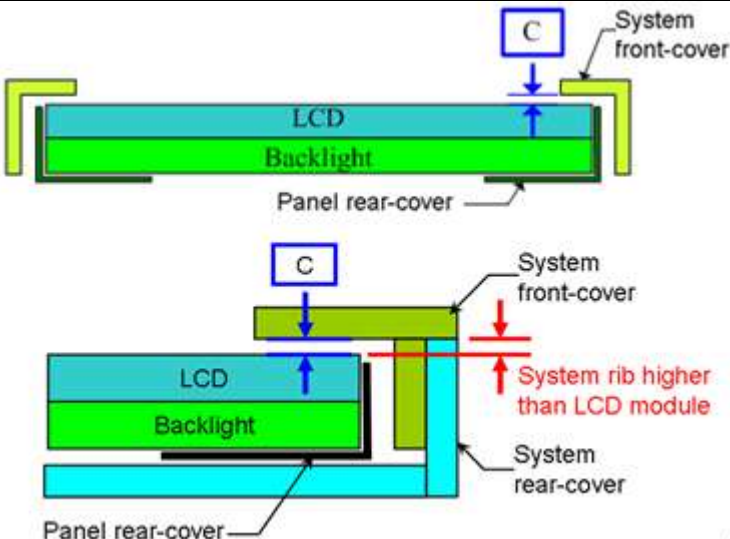
NOTES:
1. LCD MODULE INPUT CONNECTOR : I-PEX 20455-040E-12
2. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT,
   NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAN OR
   FOREIGN OBJECTS OVER COF, T-CON AND VR LOCATIONS.
3. LVDS CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
4. MODULE FLATNESS SPEC 0.5mm MAX.
5. "( )" MARKS THE REFERENCE DIMENSIONS.

Appendix. SYSTEM COVER DESIGN GUIDANCE   Ver.4
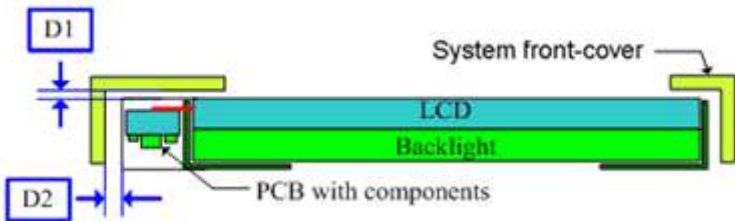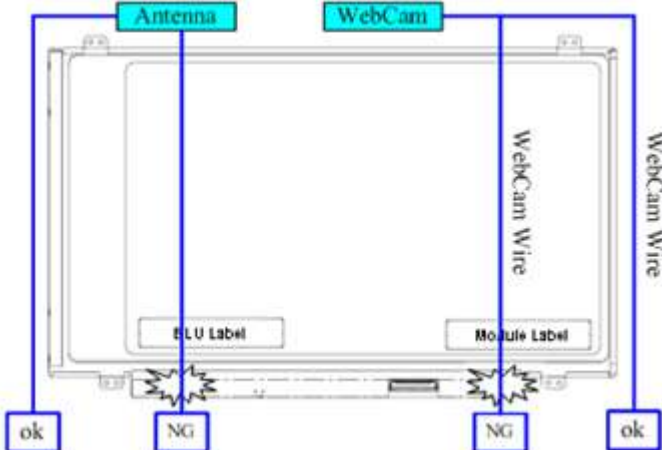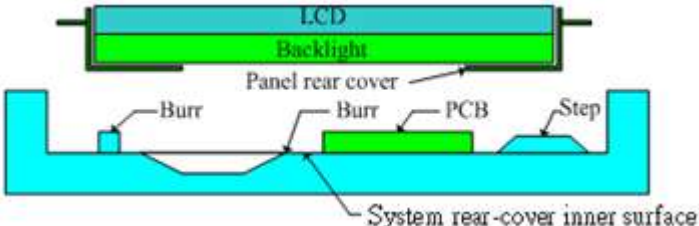
0.	Permanent deformation of system cover after reliability test
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1.	Design gap A between panel & any components on system rear-cover
Definition	Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Maximum flatness of panel and system rear-cover should be taken into account for gap design. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
2	Design gap B1 & B2 between panel & protrusions
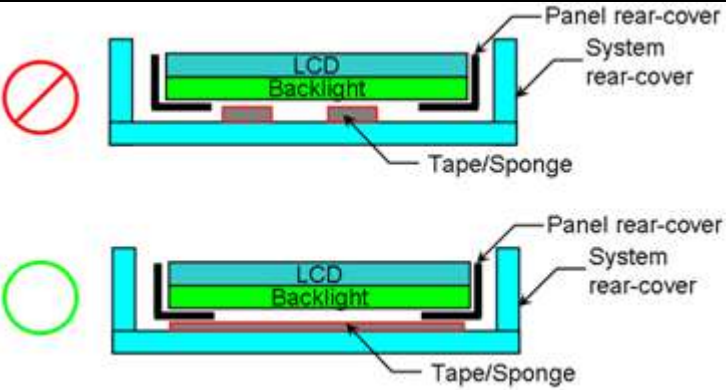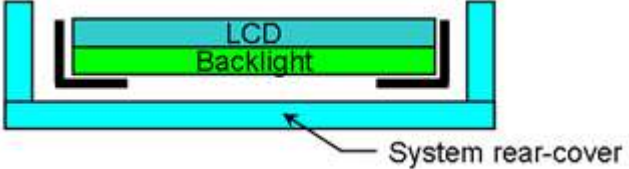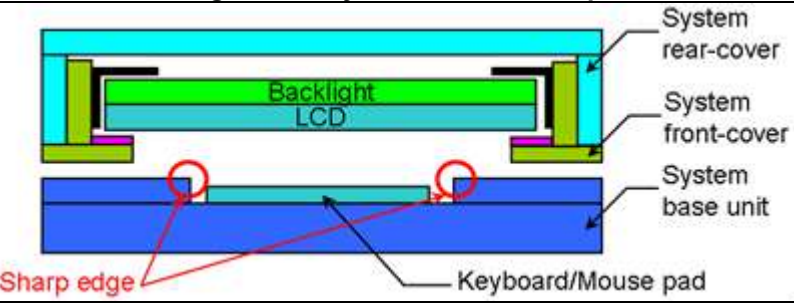
Definition	Gap between panel & protrusions is needed to prevent shock test failure. Because protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur. The gap should be large enough to absorb the maximum displacement during the test. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
3	**Design gap C between system front-cover & panel surface.**

Definition	Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
4	**Design gap D1 & D2 between system front-cover & PCB Assembly.**
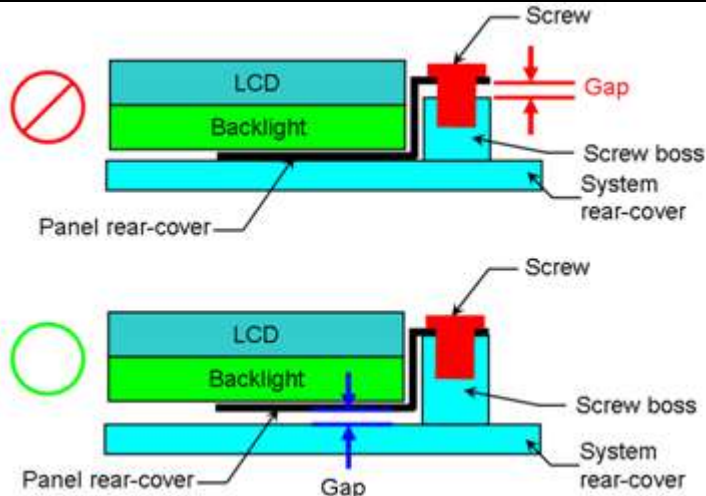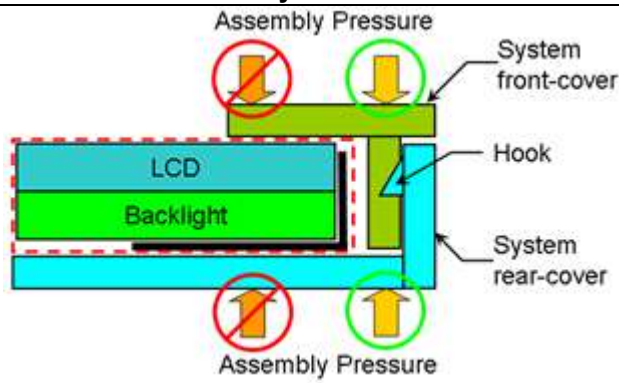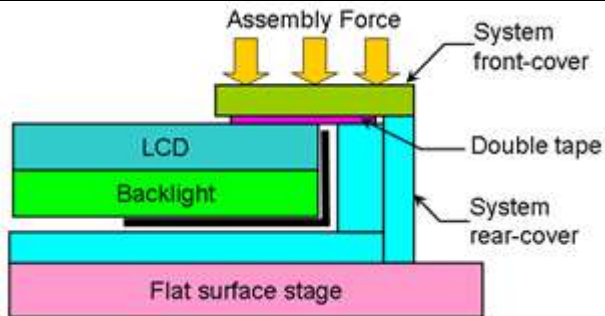
Definition	Same as point 2 and 3, but focus on PCBA side.
5	**Interference examination of antenna cable and WebCam wire**

Definition	Antenna cable or WebCam wire should not overlap with panel outline. Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
6	**System rear-cover inner surface examination**

Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
7	**Tape/sponge design on system inner surface**

Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.
8	**Material used for system rear-cover**

Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
9	**System base unit design near keyboard and mouse pad**

Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, sharp edge design in keyboard surface may damage panel during the test. We suggest to use slope edge design, or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.
10	**Screw boss height design**

Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
11	**Assembly SOP examination for system front-cover with Hook design**

Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
12	**Assembly SOP examination for system front-cover with Double tape design**

Definition	To prevent panel crack during system front-cover assembly process with double tape design, it is only allowed to give slight pressure (MAX 3 Kgf/50mm2) with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.
13	**System front-cover assembly reference with Double tape design**
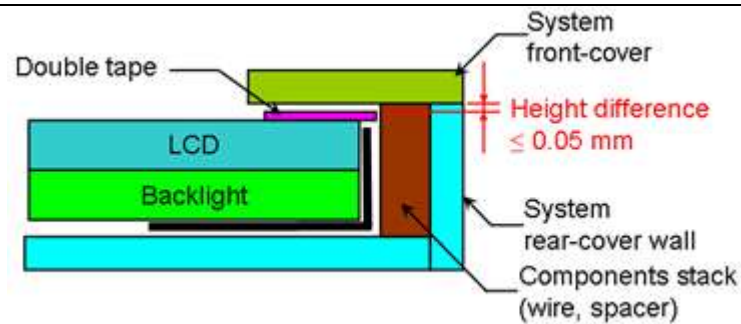
Definition	To prevent system front-cover peeling at double tape contact area, Height difference between system front-cover assembly reference such as wall or components stack (wire, spacer) and double tape top surface must be less than 0.05mm.
14	**Touch Application : TP and LCD Module Combination for White Line Prevention**
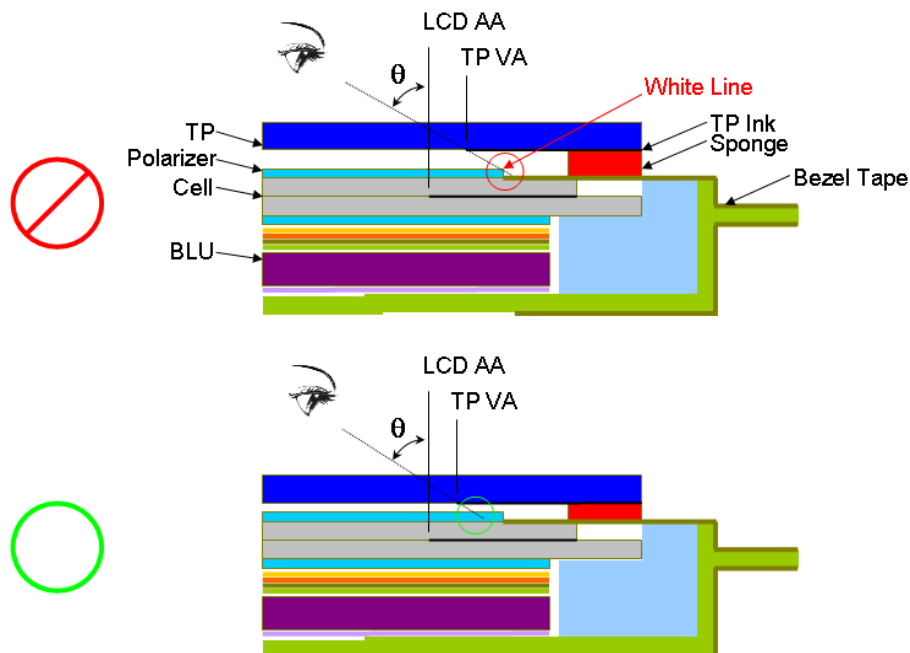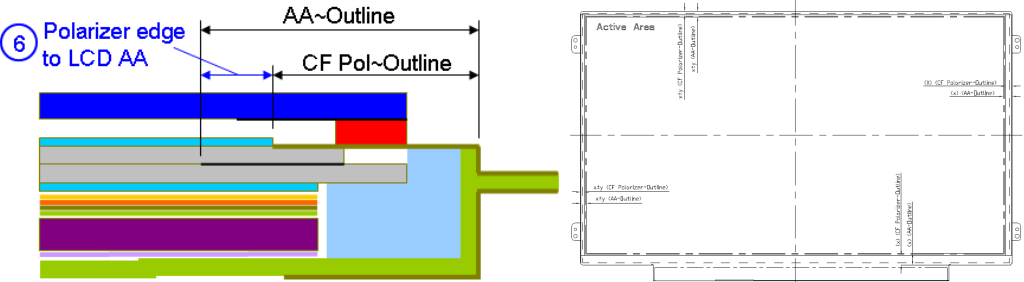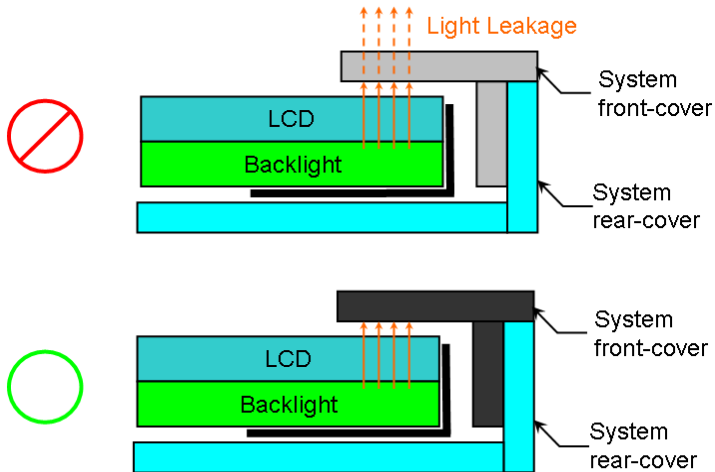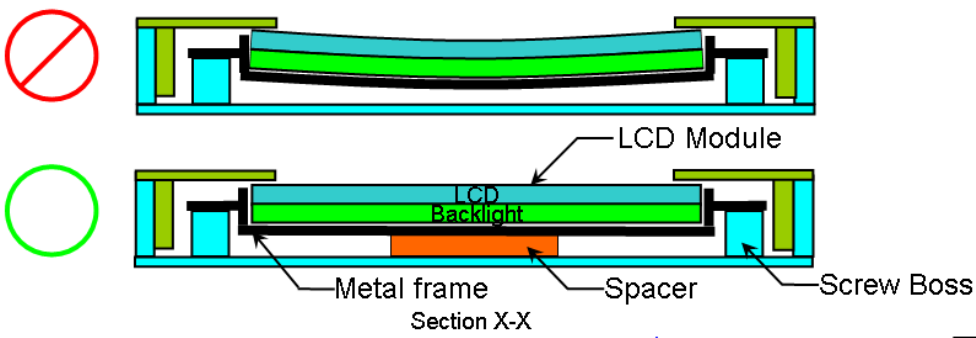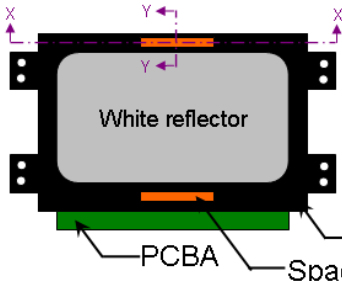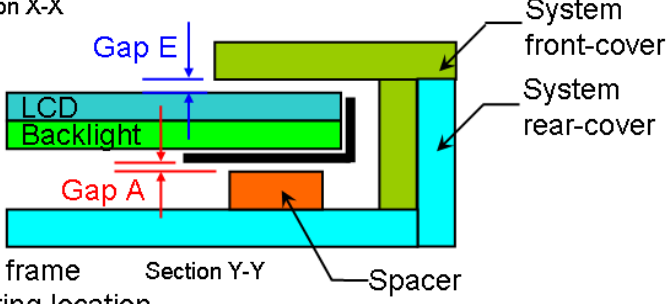
Parameter consideration for White Line Issue :

1	TP VA to LCD AA distance
2	TP Assembly tolerance
3	TP Ink Printing tolerance
4	Sponge thickness and tolerance
5	Inspection/Viewing Angle specification
6	Polarizer edge to LCD AA distance and tolerance

Polarizer edge to LCD AA distance can be derived by "AA~Outline" – "CF Pol~Outline" with respect to INX 2D Outline Drawing on each side.

Definition	For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear. Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module's Polarizer edge location and tolerance. This consideration must be taken at all four edges separately. The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area. Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing ("AA ~Outline" - "CF Pol~Outline"). Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer reference.
15	**Color of system front-cover material**

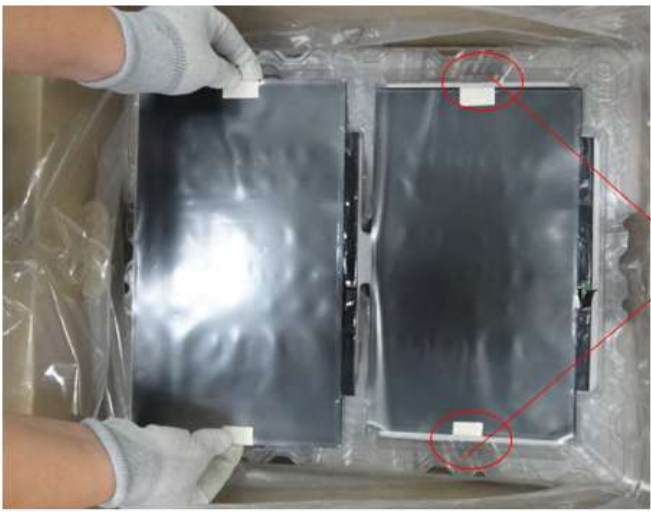| Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.
16	**Inspection spec of gap E between system front-cover to LCD module surface**

Definition	To maintain gap E (gap of system front-cover to LCD module) in its inspection spec, especially at location with maximum LCD deformation (center of LCD length), we recommend adding spacer with design gap A smaller or equal to gap E. The allowable spacer mating location is on module metal frame outside LCD Active-Area. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

Appendix. LCD MODULE HANDLING MANUAL

Purpose	· **This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure.** · **This manual provides guide in unpacking and handling steps.** · **Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.**
1.	**Unpacking**

Open carton   Remove EPE Cushion

Open plastic bag   Cut Adhesive Tape   Remove EPE Cushion

2.	**Panel Lifting**

Remove PET Cover → Remove PE Foam → Handle with care (see next page)

Finger Slot

Use slots at both sides for finger insertion. Handle panel upward with care.

3.	Do and Don't

Do :
- Handle with both hands.
- Handle panel at left and right edge.

Don't :
- Lifting with one hand.

- Handle at PCBA side.

Don't :
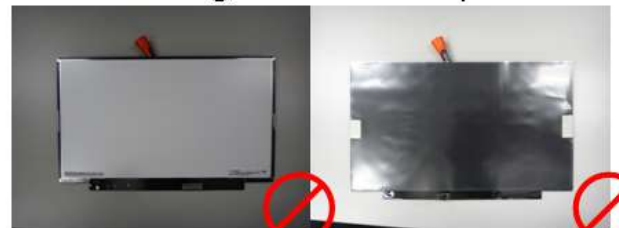- Stack panels.

- Press panel.

Don't :
- Put foreign stuff onto panel

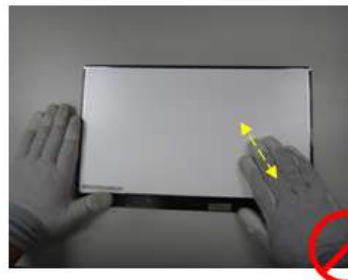- Put foreign stuff under panel

Don't :
- Paste any material unto white reflector sheet

Don't :
- Pull / Push white reflector sheet

Don't :
• Hold at panel corner.

Don't :
- Twist panel.

Do :
- Hold panel at top edge while inserting connector.

Don't :
- Press white reflector sheet while inserting connector.

Do :
- Remove panel protector film starts from side tape.

Don't :
- Remove panel protector film from film corner directly before side tape is removed.