# ITSV51X

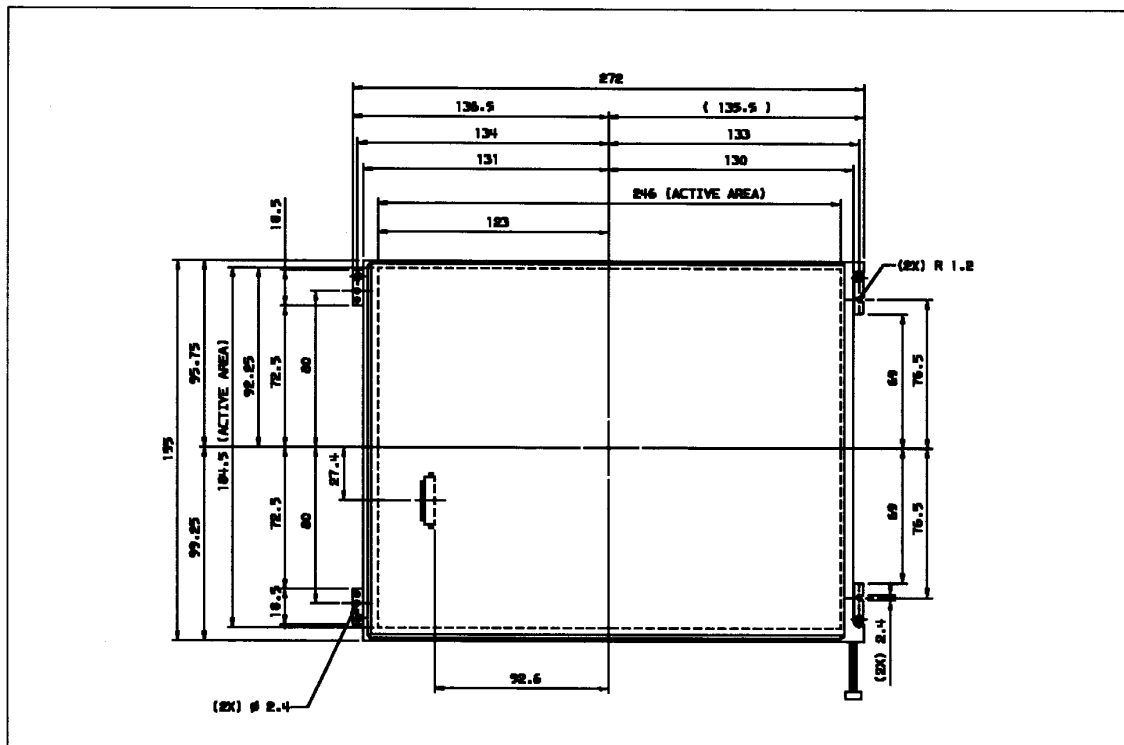## 12.1 inch  SVGA  Color TFT LCD Module

## Specification Summary

◆ **Screen Diagonal**                   30.8cm(12.1")

◆ **Active Area**                      246.0mm(H) x 184.5mm(V)

◆ **Pixel Format**                     800 x RGB x 600

◆ **Pixel Pitch**                      0.3075(per one triad)mm x 0.3075mm

◆ **Typical White Luminance**           70  cd/m²   Typ.

◆ **Power Consumption (VDD + VL)**      1.9W    Typ.

◆ **Weight**                          450 grams Typ. (w/o inverter)

◆ **Physical Size**                    272mm x 195mm x 7.5mm

◆ **Contrast Ratio**                   100 : 1 Typ.

◆ **Supported Colors**                 262k colors (6bit/color)



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                                                         Version 0.1

Preliminary

# ITSV51X
## 30.8cm(12.1 inch)SVGA(800x600) Color TFT LCD Module

ITSV51X is a TFT LCD color module to be designed to realize the largest screen on A4 size notebook style personal computer. In addition to its large screen,the characteristics of this module are light weight, slim/thin outline, low power consumption and high resolution of SVGA(800x600) capability.

## Features

- 30.8cm(12.1 inch) diagonal
- Native 262k colors (R/G/B 6bit each)
- SVGA 800 x 600 pixels
- Low Reflection (Black Matrix)
- Size :   272mm x 195mm x 7.5mm typ.
- Weight :   450 g typ.
- Power Consumption : 2.1 W typ.

## Applications

- Notebook PCs
- Monitors

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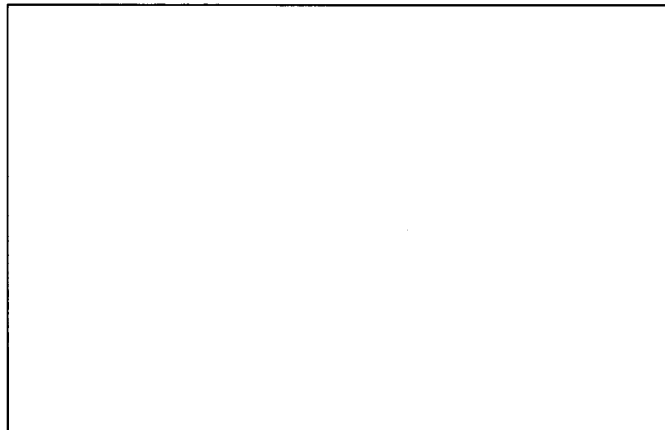
## Characteristics Summary

| | |
|---|---|
| Screen Diagonal | 30.8cm(12.1") |
| Active Area | 246.0mm(H) x 184.5mm(V) |
| Pixel Format | 800(x3) x 600 |
| Pixel Pitch | 0.3075(per one triad) x 0.3075 |
| Pixel Arrangement | R,G,B Vertical Stripe |
| Display Mode | Normally White |
| White Luminance | 70 cd/m$^2$ Typ. (CFL Discharge Current = 2.8 mA$_{RMS}$ ) |
| Contrast Ratio | 100 : 1 Typ. |
| Optical Rise Time/Fall Time | 35 msec. Typ. at 25 degC |
| Nominal Input Voltage VDD | +3.3V Typ. |
| Power Consumption (VDD line + Lamp input line) | 2.1W typ. |
| Weight | 450 grams typ. |
| Physical Size | 272mm x 195mm x 7.5mm typ. |
| Electrical Interface | Digital Video Signals(6-bit for each color R/G/B) Sync. Signal (x4) |
| Supported Colors | Native 262k colors |
| Temperature Range Operating Storage | +0 to +50 degC -20 to +60 degC |

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## Absolute Maximum Ratings

| Rating | Symbol | Value | Unit | Conditions |
|---|---|---|---|---|
| Supply Voltage | VDD | -0.3 to +3.9 | V | |
| | Vcfl | 1300 | Vrms | Lamp Ignition Voltage at 0 degC |
| Lamp Current | Icfl | 6.5 | mArms | Exclude inrush current |
| Input Voltage | VIN1 | -0.3 to Vdd+0.3 | V | |
| Shock | | 50 | G | 18ms |
| Vibration | | 1.5 | G | 10-200Hz |
| Storage Temperature | TST | -20 to + 60 | degC | At the glass surface |
| Operation Temprautre | TOP | 0 to +50 | degC | At the glass surface |
| Operation Humidity | | 8 to 95 | %RH | Max wet bulb temp. 29 degC No condensation |

## Block Diagram

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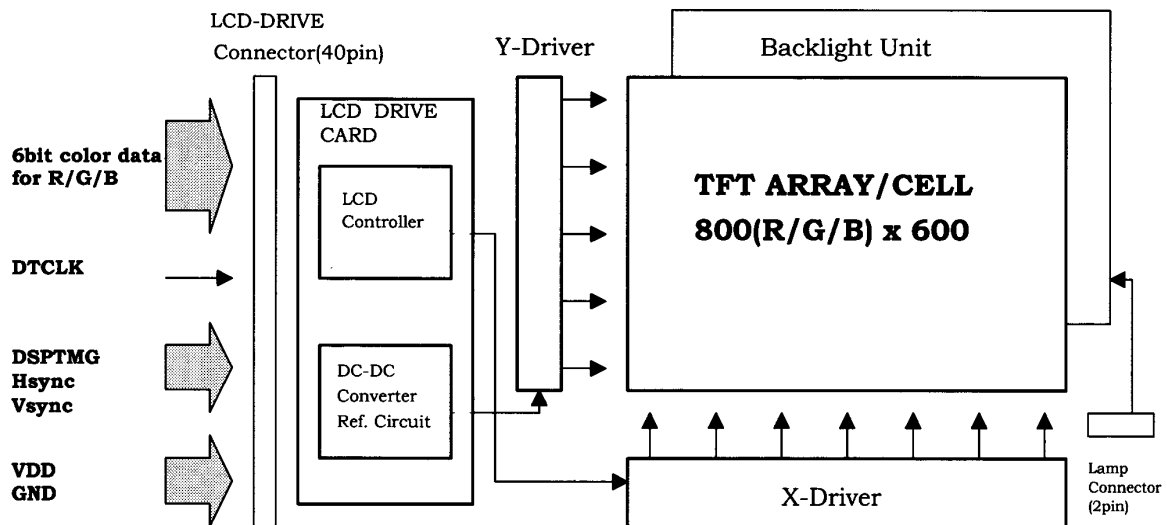
## Signal Interface

|  |  | Supplier Name | Supplier's Part Number |
|---|---|---|---|
| LCD Drive Connector | | JAE | IL-FHR-B40S-HF(for 0.5mm pitch FPC) |
| Corresponding Connector | | | 0.5mm pitch FPC |
| Pin No. | Signal Name | Description | |
| 15 | +RED5 | Red Data 5 (MSB) | |
| 14 | +RED4 | Red Data 4 | |
| 13 | +RED3 | Red Data 3 | |
| 11 | +RED2 | Red Data 2 | |
| 10 | +RED1 | Red Data 1 | |
| 9 | +RED0 | Red Data 0 (LSB) | |
| | | Red-Pixel-Data Each red pixel's data consists of these 6 bits pixel data | |
| 25 | +GREEN5 | Green Data 5 (MSB) | |
| 24 | +GREEN4 | Green Data 4 | |
| 23 | +GREEN3 | Green Data 3 | |
| 21 | +GREEN2 | Green Data 2 | |
| 20 | +GREEN1 | Green Data 1 | |
| 19 | +GREEN0 | Green Data 0 (LSB) | |
| | | Green-Pixel-Data Each green pixel's data consists of these 6 bits pixel data | |
| 35 | +BLUE5 | Blue Data 5 (MSB) | |
| 34 | +BLUE4 | Blue Data 4 | |
| 33 | +BLUE3 | Blue Data 3 | |
| 31 | +BLUE2 | Blue Data 2 | |
| 30 | +BLUE1 | Blue Data 1 | |
| 29 | +BLUE0 | Blue Data 0 (LSB) | |
| | | Blue-Pixel-Data Each blue pixel's data consists of these 6 bits pixel data | |

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| 2 | -DTCLK | Data Clock | The typical frequency is 40.00MHz.The signal is used to strobe the pixel data and +DSPTMG signals.All pixel data shall be valid at the falling edge when the +DSPTMG signal is high. |
|---|---|---|---|
| 37 | +DSPTMG | Display Timing | This signal strobed at the falling edge of -DTCLK.When the signal is high,the pixel data shall be valid to be displayed. |
| 5 | VSYNC | Vertical Sync | The signal is synchronized to -DTCLK. |
| 4 | HSYNC | Horizontal Sync | The signal is synchronized to -DTCLK. |
| 38,39 | VDD | +3.3V | |
| 1,3,6,7,8,12,16,17 18,22,26,27,28,32 36 | GND | Signal Ground | |
| 40 | | Reserved | No connection (Signal reserved for test) |

**Note:** Output signals from system shall be low or Hi-Z state when VDD is off.

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## Signal Interface for Lamp

|  |  | Supplier Name | Supplier's Part Number |
|---|---|---|---|
| Lamp Connector | | JST | BHR-03VS-1 |
| Pin No. | Signal Name | Description | |
| 1 | Lamp High | | |
| 3 | Lamp Low | | |

## Signal Specification

| R/G/B,DTCLK,DSPTMG,H/VSYNC signal specification | | | | |
|---|---|---|---|---|
| **Parameter** | **Condition** | **Min.** | **Max.** | **Unit** |
| Vih | High level input voltage | 2.0 | Vdd+0.3 | V |
| Vil | Low level input voltage | 0 | 0.8 | V |
| Iih | High level input current | — | 50 | uA |
| Iil | Low level input current | — | -50 | uA |

## Lamp Interface Specification

### 1) Absolute Maximum Rating

| **Parameter Name** | **Symbol** | **Value** | **Unit** | **Note** |
|---|---|---|---|---|
| CFL Discharge Current | $I_{CFL}$ | 6.5 Max | $[mA_{RMS}]$ | Exclude inrush current |
| CFL Inrush Current | $IR_{CFL}$ | 30 Max | $[mA_{0-P}]$ | T = 50 Max. [mSec] |

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2) Parameter Guideline for CFL Inverter

| Parameter Name | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| CFL Kick-off Voltage | $V_S$ | - | - | 900 | $[V_{RMS}]$ | $T_{amb}$=25 degC [4] |
| | | - | - | 1,300 | | $T_{amb}$= 0 degC [4] |
| CFL Discharge Current | $I_{CFL}$ | 2.0 [6] | - | 6.0 | $[mA_{RMS}]$ | Total operating range |
| | | - | 2.8 | - | | Screen 70 $[cd/m^2]$,25degC |
| CFL Discharge Voltage | $V_{CFL}$ | - | 500 | - | $[V_{RMS}]$ | Screen 70 $[cd/m^2]$, $T_{amb}$=25 degC |
| CFL Power Consumption | $P_{CFL}$ | - | 1.4 | - | [W] | Screen 70 $[cd/m^2]$, $T_{amb}$=25 degC |
| CFL Discharge Frequency | $F_{CFL}$ | 30 | 40 | 60 [6] | [kHz] | Reference [5] |

Note

*1  All of characteristics listed 2) are measured under the condition using the IBM Test inverter.

*2  It is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power happen.

*3  It is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4  Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until dischargement.

*5  CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6  Reducing CFL current increases CFL discharge voltage and generally increses CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current fromhigh-voltage output of the inverter.

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## Interface Timing

Basically ,interface timings should match the VESA  800 x 600 60Hz manufacturing guideline timing.

| Symbol | Signal Description | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{dck}$ | DTCLK frequency | 36.00 | 40.00 | 40.20 | MHz |
| $t_{ck}$ | DTCLK cycle time | 27.77 | 25.00 | 24.88 | nsec |
| $t_{wcl}$ | DTCLK low width | 5.00 | | | nsec |
| $t_{wch}$ | DTCLK high width | 5.00 | | | nsec |
| $t_{rck}$ | DTCLK rise time | | | 3.00 | nsec |
| $t_{fck}$ | DTCLK fall time | | | 3.00 | nsec |
| $t_{ds}$ | Data set up time | 5.00 | | | nsec |
| $t_{dh}$ | Data hold time | 5.00 | | | nsec |
| $t_{rdt}$ | DSPTMG rise time | 5.00 | | | nsec |
| $t_{fdt}$ | DSPTMG fall time | 5.00 | | | nsec |
| $t_{dts}$ | DSPTMG set up time | 5.00 | | | nsec |
| $t_{dth}$ | DSPTMG hold time | 5.00 | | | nsec |
| $t_{x}$ | X total time | 848 | 1056 | 1088 | $t_{ck}$ |
| $t_{acx}$ | X active time | | 800 | | $t_{ck}$ |
| $t_{bkx}$ | X blank time | 48 | 256 | 288 | $t_{ck}$ |
| $H_{sync}$ | H-sync frequency | 35.16 | 37.88 | 38.46 | kHz |
| $H_{w}$ | H-sync width | 16 | 128 | 152 | $t_{ck}$ |
| $t_{y}$ | Y total time | 611 | 628 | 1025 | $t_{x}$ |
| $t_{acy}$ | Y active time | | 600 | | $t_{x}$ |
| $V_{sync}$ | Frame rate | 56.25 | 60.00 | 61.00 | Hz |
| $V_{w}$ | V-sync width | 1 | 4 | 7 | $t_{x}$ |
| $V_{fp}$ | V-sync front porch | 1 | 1 | 415 | $t_{x}$ |
| $V_{bp}$ | V-sync back porch | 9 | 23 | 29 | $t_{x}$ |

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## Horizontal Timing



## Vertical Timing

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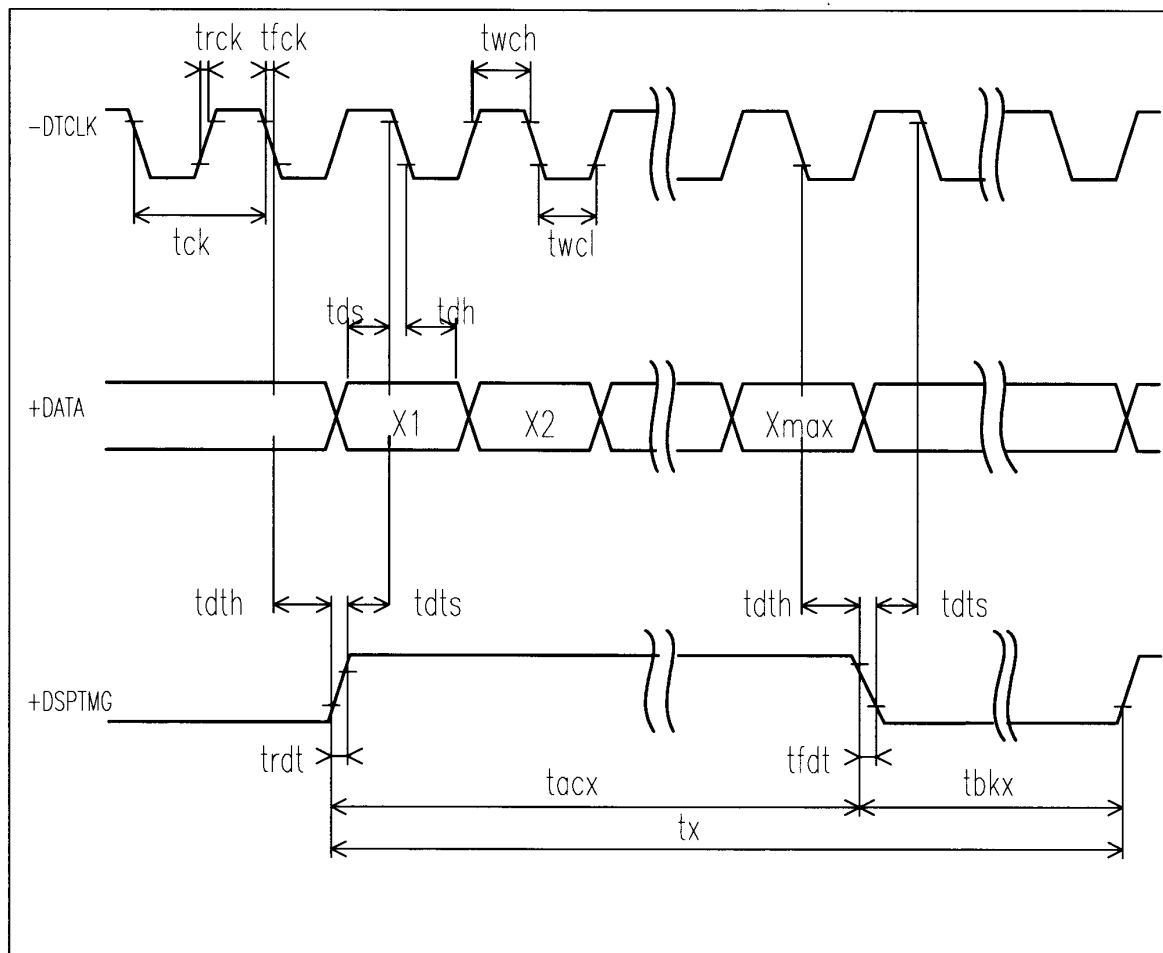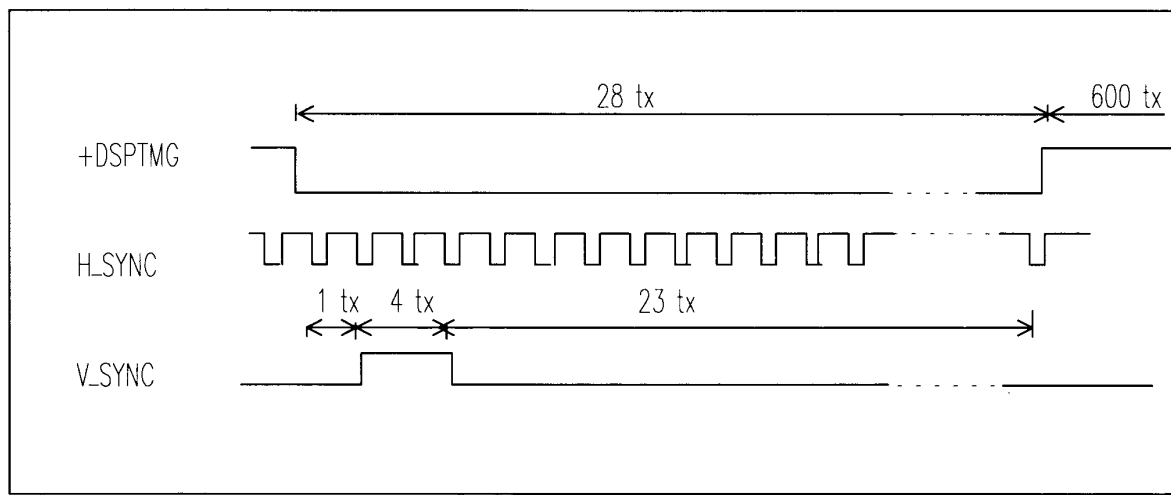
## Power Requirement

| SYMBOL | PARAMETER | Min. | Typ. | Max. | Unit | CONDITION |
|---|---|---|---|---|---|---|
| VDD | Logic/LCD Drive Voltage | +3.0 | +3.3 | +3.6 | V | Load Capacitance 40uF |
| PDD | VDD Power | | 0.7 | | W | VDD=+3.3V |
| PL | Lamp Power(w/o inverter) | | 1.4 | | W | |
| PDD+PL | Total Power(w/o inverter) | | 2.1 | | W | |
| VDDrp | Allowable Logic/LCD Drive Ripple Voltage | | | 100 | mVp-p | |
| VDDns | Allowable Logic/LCD Drive Ripple Noise | | | 100 | mVp-p | |

**Note:** This requirements shall be met with both 'All black pattern'.

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## Power ON/OFF sequence
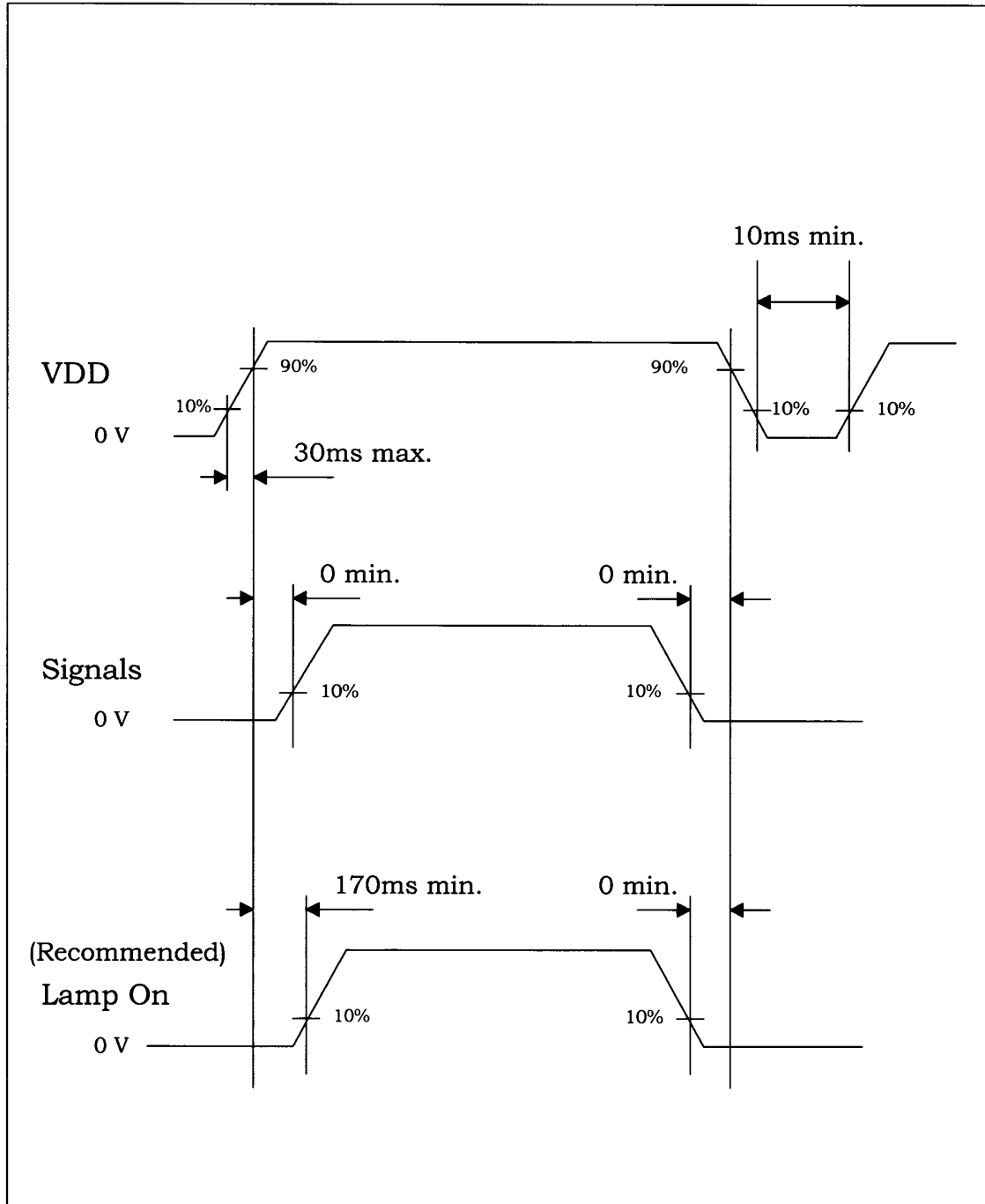
## Handling Precautions

1) Since front polarizer is easily damaged,pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately.Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled,wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or creak if dropped or bumped on hard surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.

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Reference Drawing without inverter



Dimensions shown in this Drawing are Reference Only.

They are subject to change without notifications.

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