Doc. Version	0.8
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Date	2007/10/23

Product Specifications

3.5" COLOR TFT-LCD MODULE

MODEL NAME: A035QN03 V1

< □ >Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2007/02/14		First draft.
0.1a	2007/03/01	5~6	Update the pin assignment
		22~23	Correct optical remark
		24	Correct reliability test items
		27	Update the application circuit
0.2	2007/03/26	28, 29	Add power on/ off and STB sequence
		8	Modify the typical DCLK to 24.54 MHz
0.3	2007/3/28	6	Correct LED reverse voltage from 2V to 5V.
		22	Updated response time and viewing angle
0.4	2007/04/16	6	Modify the absolute maximum rating table
		8	Modify the electrical characteristic table
		10~13	Modify the AC timing tables and diagrams
		14~18	Modify the register timing, tables, and description
		23	Change C14 to 10 uF
		26~27	Add recommend power on/ off settings
		28	Add notes for ESD protection
0.5	2007/05/21	6	Remove operation/storage temperature range
		7	Update LED limit curve
0.6	2007/07/10	9	Modify the electrical characteristics
		11	Modify the minimum value of V-blanking in UPS051
		13~15	Add CCIR/YUV input signal timing information
		17~21	Modify the SPI settings
		33~38	Add recommended register settings
0.7	2007/08/15	10	Add general input timing
		11, 12	Modify the timing specification table of UPS051
0.8	2007/10/23	24	Update response time spec

Contents:

A. General Description

A035QN03 V1 is an amorphous transmissive type Thin Film Transistor Liquid crystal Display (TFT-LCD). This model is composed of a TFT-LCD, a driver, an FPC (flexible printed circuit) and a backlight unit.

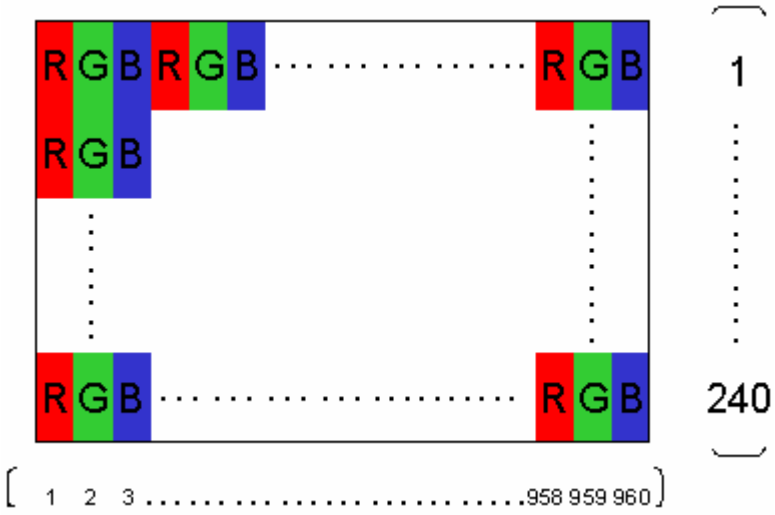
B. Features

- 3.5-inch display with QVGA resolution
- RGB stripe dot arrangement
- DC/DC integrated
- High brightness
- 3-wire register setting
- Digital serial 8-bit input
- Wide viewing angle
- 2-in-1 FPC for LCD signals and backlight LED power
- Green design

C. Physical Specifications

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	320 RGB (H)×240(V)	
2	Active Area	mm	70.08(H)×52.56(V)	
3	Screen Size	inch	3.5(Diagonal)	
4	Dot Pitch	mm	0.073(H)×0.219(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	16.7M Colors	
7	Overall Dimension	mm	76.9(H) × 63.9(V) × 2.92(T)	Note 2
8	Weight	g	29.5	
9	Panel surface treatment	--	Hard coating 3H	

Note 1: Below figure shows dot stripe arrangement.



Note 2: Not including FPC. Refer to the drawing next page for further information.

D. Electrical Specifications

1. Pin Assignment

Pin no.	Symbol	I/O	Description	Remarks
1	VCOM	I	VCOM	
2	VGL	C	Capacitor of charge pumping circuit	
3	VGH	C	Capacitor of charge pumping circuit	
4	C3P	C	Capacitor of charge pumping circuit	
5	C3M	C	Capacitor of charge pumping circuit	
6	LED_-	I	LED back light cathode	
7	LED_+	I	LED back light anode	
8	V_10	C	Capacitor of charge pumping circuit	
9	V_5	C	Capacitor of charge pumping circuit	
10	VINT2	C	Capacitor of charge pumping circuit	
11	C2P	C	Capacitor of charge pumping circuit	
12	C2M	C	Capacitor of charge pumping circuit	
13	VCAC	C	Capacitor of VCOMAC circuit	
14	FRP	O	Frame polarity	
15	VINT1	C	Capacitor of charge pumping circuit	
16	C1BP	C	Capacitor of charge pumping circuit	
17	C1AP	C	Capacitor of charge pumping circuit	
18	C1BM	C	Capacitor of charge pumping circuit	
19	C1AM	C	Capacitor of charge pumping circuit	
20	GND	G	Ground	
21	AVDD	PI	Analog power input, 3.0~3.6V is recommended.	
22	GMA_H	C	Stabilizing capacitor for analog power	
23	GND	G	Ground	
24	VCC	C	Digital power supply	

25	VIO	PI	Digital power input	
26	CS	I	Chip enable of serial interface	
27	SDA	IO	Serial data input and output of serial interface	
28	SCL	I	Clock of serial interface	
29	HSYNC	I	Horizontal synchronous signal	
30	VSYNC	I	Vertical synchronous signal	
31	DCLK	I	Dot clock	
32	DATA 7	I	Data of serial RGB input (MSB)	
33	DATA 6	I	Data of serial RGB input	
34	DATA 5	I	Data of serial RGB input	
35	DATA 4	I	Data of serial RGB input	
36	DATA 3	I	Data of serial RGB input	
37	DATA 2	I	Data of serial RGB input	
38	DATA 1	I	Data of serial RGB input	
39	DATA0	I	Data of serial RGB input (LSB)	
40	VCOM	I	VCOM	

I: Digital signal input, O: Digital signal output, IO: Digital inout pin, G: GND, PI: Power input

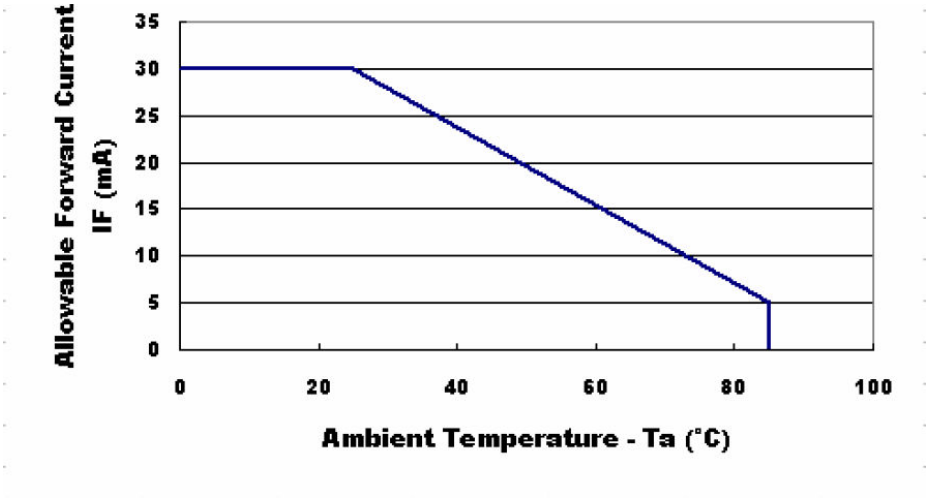
C: Power set capacitor connect pin.

2. Absolute Maximum Ratings

Items	Symbol	Values		Unit	Condition
		Min.	Max.		
Power Voltage	VIO	-0.5	7	V	
	AVDD	-0.5	7	V	
LED Reverse Voltage	Vr		5	V	One LED
LED Forward Current	If		30	mA	One LED, Note 2

Note 1.If the operating condition exceeds the absolute maximum ratings, the TFT-LCD module may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop.

Note 2. If LED current exceeds the limit curve, the lifetime will drop dramatically.



Note 3. 90% RH maximum humidity when temp. ≤60°C.

If temp. >60°C, the absolute humidity maximum shall be less than 90% RH.

3. Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

a. TFT- LCD Panel (GND=0V)

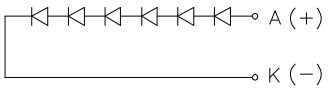
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Digital Power Supply	VIO	1.8	3.3	3.6	V	
Analog Power Supply	AVDD	3.0	3.3	3.6	V	
Input Signal Voltage	Vi	0		0.2 x VIO	V	
	VI	0.8 x VIO		VIO	V	
Frame Frequency	f_{Frame}		60		Hz	
Dot Data Clock	DCLK		24.54		MHz	
VCOM	VCOMDC	0.4	1.0	1.66	V	
	VCOMAC	3.6	4.2	5	V	
Power Stand-by Current	$ISTB_{AVDD}$		25	50	uA	AVDD=3.3V
Power Operating Current	I_{AVDD}		10	20	mA	VIO=3.3V

Note 1. Panel surface temperature should be kept less than content of section 3.2. “Absolute maximum ratings"

b. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Supply Current	I_L		25		mA	single serial
LED Supply Voltage	V_L		19.8		V	single serial
LED Life Time	L_L	10,000	---	---	Hr	Note 2, 3

Note 1: LED backlight is six LEDs serial type.



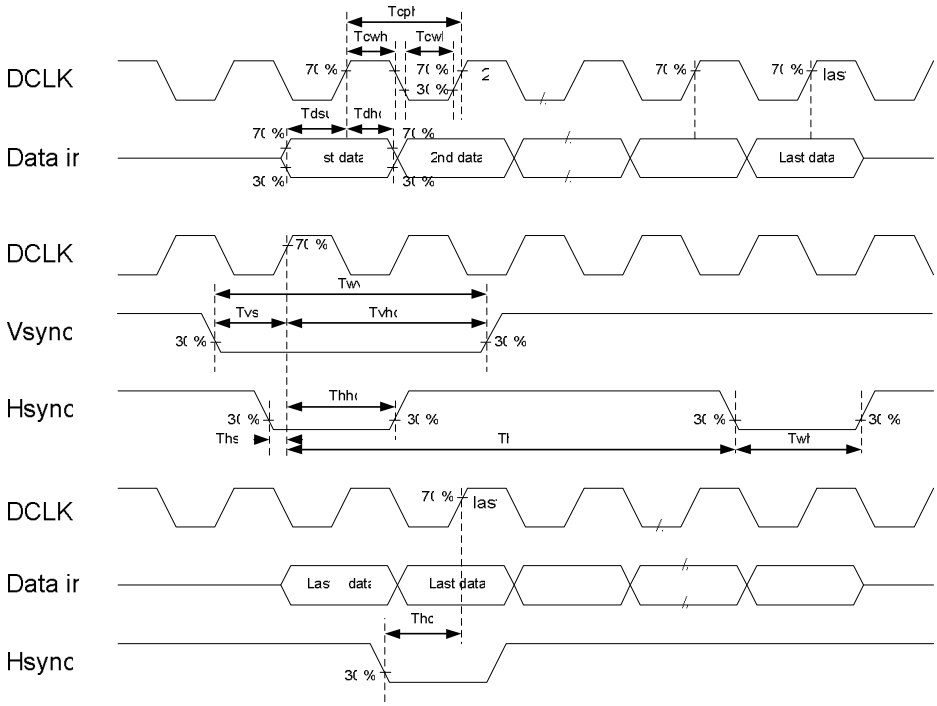
Note 2: The ”LED Supply Voltage” is defined by the number of LED at Ta=25°C, I_L=25mA. In the case of 6 pcs LED, V_L=3.3*6=19.8V

Note 3: The ”LED life time” is defined as the time for the module brightness to decrease to 50% of the initial value at Ta=25°C, I_L=20mA

Note 4: The LED lifetime could be decreased if operating $I_L$is larger than 25mA

4. AC Timing

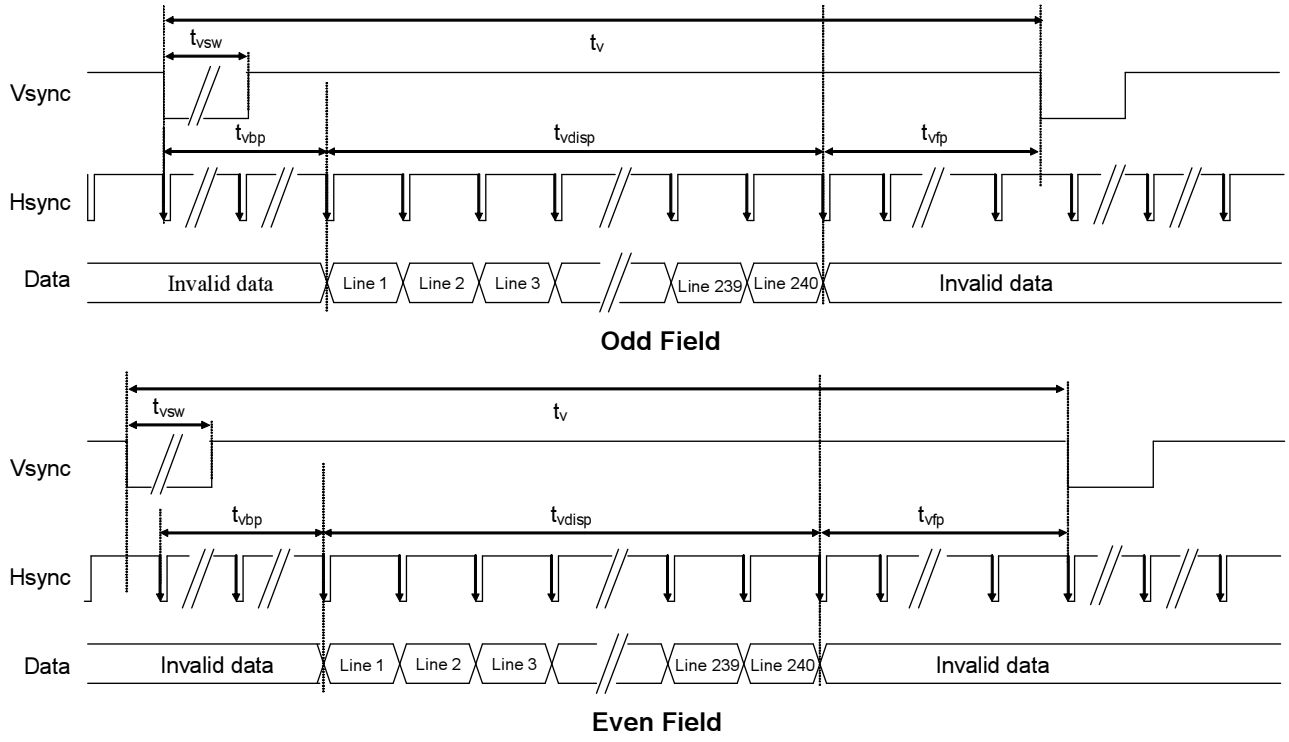
a. General input timing



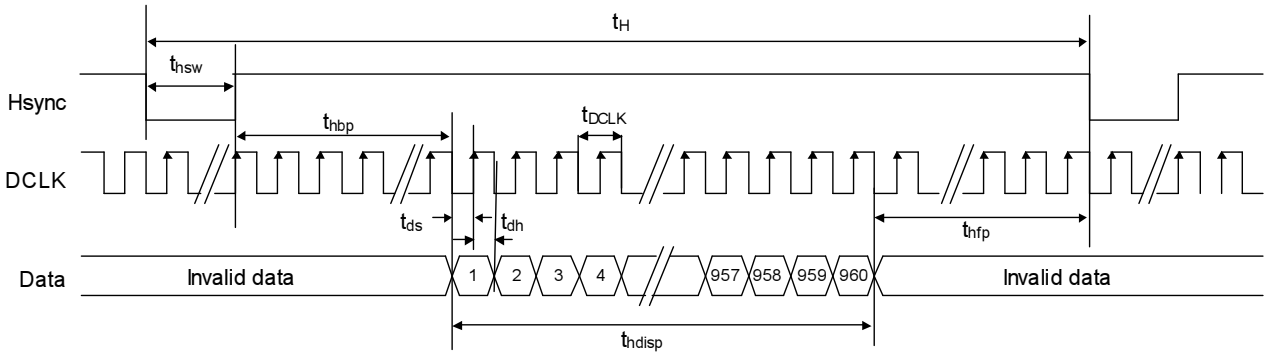
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK pulse duty	Tcw		40	50	60	%
Delay between Hsync and DCLK	Thc		-	-	1	DCLK
Hsync width	Twh		1	-	-	DCLK
Hsync period	Th		60	63.56	67	us
Hsync setup time	Thst		15	-	-	ns
Hsync hold time	Thhd		15	-	-	ns
Vsync width	Twv		1	-	-	Hsync
Vsync setup time	Tvst		15	-	-	ns
Vsync hold time	Tvhd		15	-	-	ns
Data set-up time	Tdsu	D0~D7 to DCLK	15	-	-	ns
Data hold time	Tdhd	D0~D7 to DCLK	15	-	-	ns

b. UPS051 compatible input timing

Vertical Timing



Horizontal Timing



Timing specification

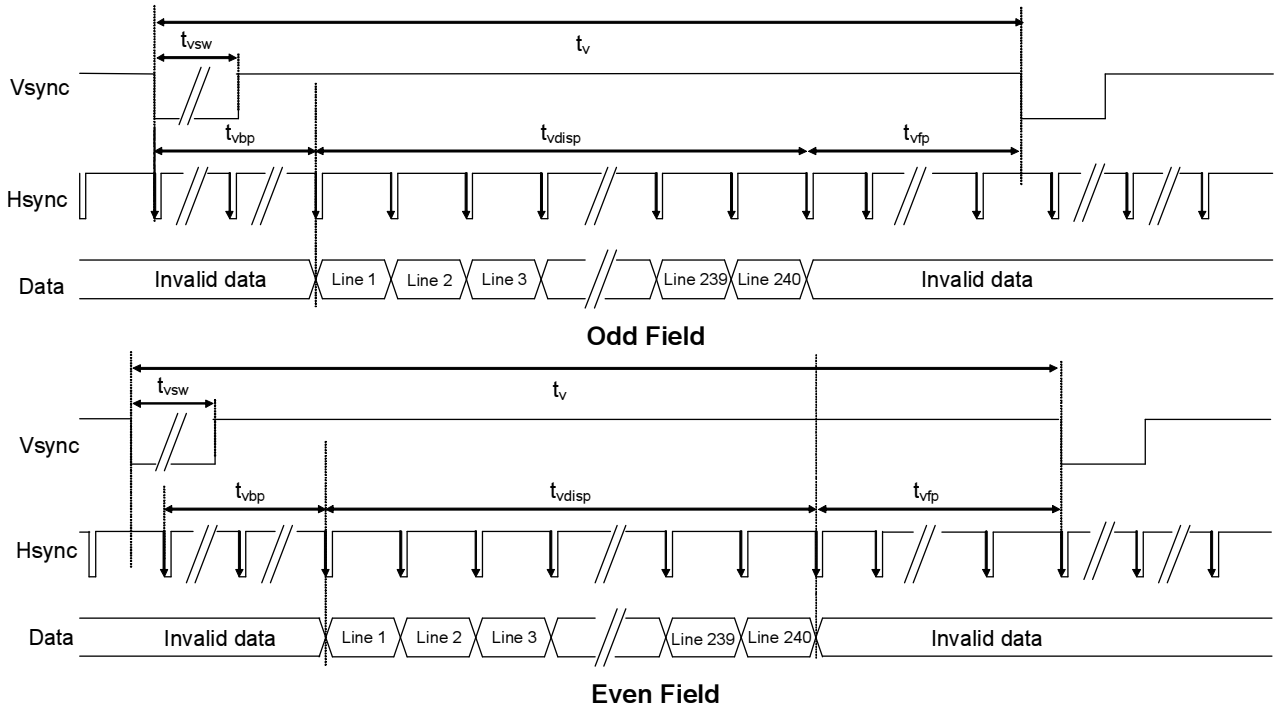
Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	13*	27	27.19	MHz	Note 1
Hsync	Period	t_H	1024	1716	1728	t_{DCLK}	
	Display period	t_{hdisp}	960			t_{DCLK}	
	Back porch	t_{hbp}	63	70	255	t_{DCLK}	

	Front porch		t_{hfp}	1	686	718	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	-	t_{DCLK}	
Vsync	Period	Odd	t_V	241	262.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	13	20	28	t_H	
		Even		13.5	20.5	28.5		
	Front porch	Odd	t_{vfp}	0	4.5	-	t_H	
		Even		0	5	-		
	Pulse width		t_{vsw}	1	1	-	t_H	

Note 1: **The minimum DCLK will lead the frame rate to be lower than 50Hz.**

c. UPS052 compatible input timing

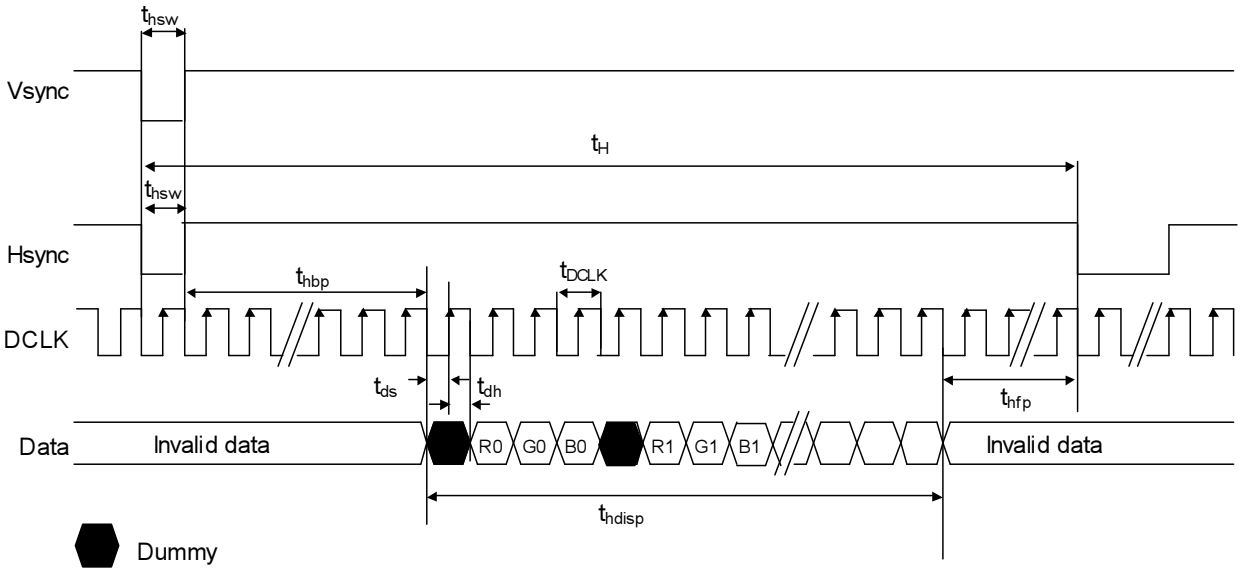
Vertical Timing



Odd Field

Even Field

Horizontal Timing



Timing specification

NTSC:

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	24.535	-	MHz	
Hsync	Period		t_H	-	1560	-	t_{DCLK}	
	Display period		t_{hdisp}		1280		t_{DCLK}	
	Back porch		t_{hbp}	-	241	-	t_{DCLK}	
	Front porch		t_{hfp}	0	28	-	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	-	t_{DCLK}	
Vsync	Period	Odd	t_V	-	262.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}		240		t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	21	-	t_H	
		Even		-	21.5	-		
	Pulse width		t_{vsw}	1	1	-	t_H	

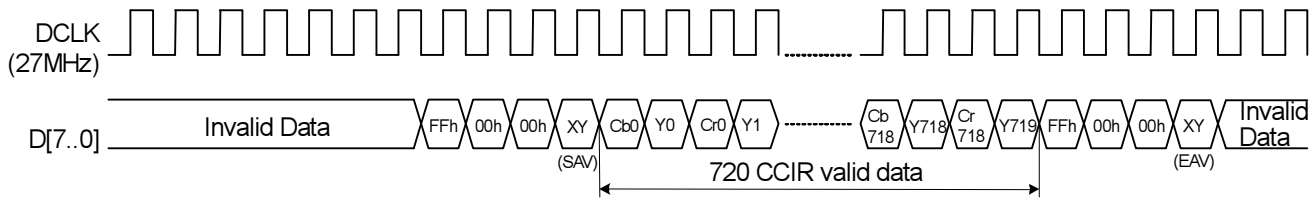
PAL:

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	-	24.375	-	MHz	
Hsync	Period	t_H	-	1560	-	t_{DCLK}	
	Display period	t_{hdisp}		1280		t_{DCLK}	
	Back porch	t_{hbp}	-	241	-	t_{DCLK}	

	Front porch		t_{hfp}	0	28	-	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	-	t_{DCLK}	
Vsync	Period	Odd	t_V	-	312.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}	288			t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	24	-	t_H	
		Even		-	24.5	-		
	Pulse width		t_{vsw}	1	1	-	t_H	

d. CCIR656

Timing format

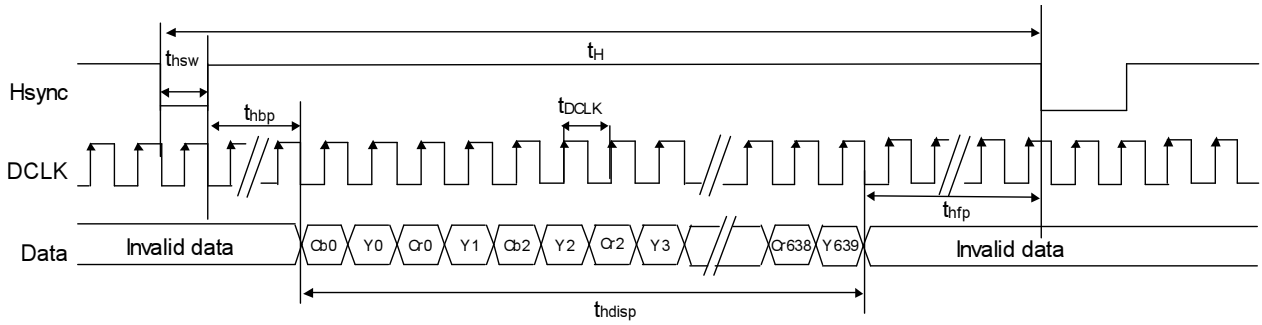


Timing specification

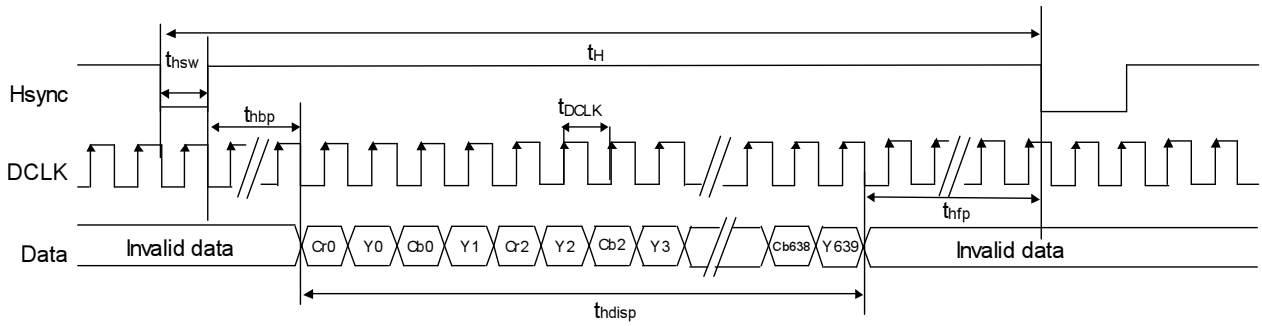
Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	27	-	MHz	
Hsync	Period		t_H	-	1716	-	t_{DCLK}	
	Display period		t_{hdisp}	1440			t_{DCLK}	
	Back porch		t_{hbp}	-	273	-	t_{DCLK}	
	Front porch		t_{hfp}	4	4	4	t_{DCLK}	
	Pulse width		t_{hsw}	1	-	-	t_{DCLK}	
Vsync	Period	Odd	t_V		262.5		t_H	
		Even						
	Display period	Odd	t_{vdisp}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	18	-	t_H	
		Even		-	17.5	-		
	Front porch	Odd	t_{vfp}	0	4.5	-	t_H	
		Even		0	5	-		
	Pulse width	Odd	t_{vsw}	1	-	-	t_{DCLK}	
		Even						

e. YUV640/YUV720

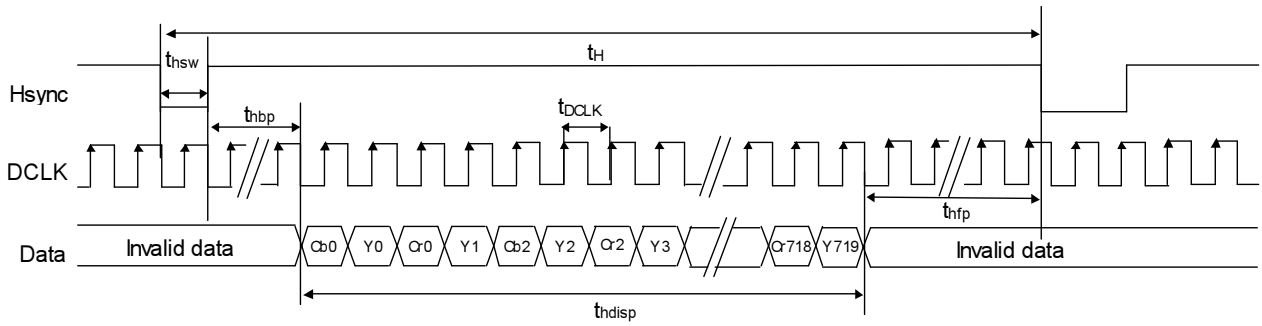
YUV640 mode A horizontal timing



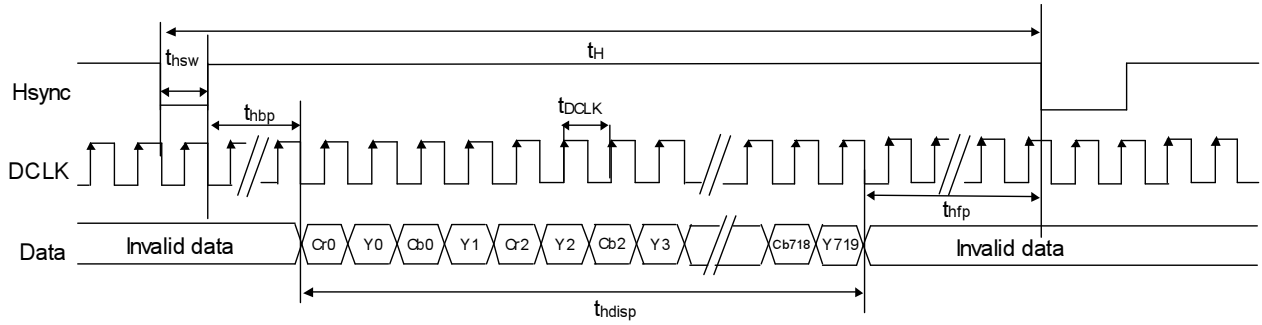
YUV640 mode B horizontal timing



YUV720 mode A horizontal timing



YUV720 mode B horizontal timing



Timing specification

YUV640 mode

NTSC:

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	24.535	-	MHz	
Hsync	Period		t_H	-	1560	-	t_{DCLK}	
	Display period		t_{hdisp}	1280			t_{DCLK}	
	Back porch		t_{hbp}	-	241	-	t_{DCLK}	
	Front porch		t_{hfp}	0	1	-	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	-	t_{DCLK}	
Vsync	Period	Odd	t_V	-	262.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	21	-	t_H	
		Even		-	21.5	-		

PAL:

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	24.375	-	MHz	
Hsync	Period		t_H	-	1560	-	t_{DCLK}	
	Display period		t_{hdisp}	1280			t_{DCLK}	
	Back porch		t_{hbp}	-	241	-	t_{DCLK}	
	Front porch		t_{hfp}	0	1	-	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	-	t_{DCLK}	
Vsync	Period	Odd	t_V	-	312.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}	288			t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	24	-	t_H	
		Even		-	24.5	-		

YUV 720 mode

NTSC:

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	27	-	MHz	
Hsync	Period		t_H	-	1716	-	t_{DCLK}	
	Display period		t_{hdisp}		1440		t_{DCLK}	
	Back porch		t_{hbp}	-	241	-	t_{DCLK}	
	Front porch		t_{hfp}	0	1	-	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	-	t_{DCLK}	
Vsync	Period	Odd	t_V	-	262.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}		240		t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	21	-	t_H	
		Even		-	21.5	-		

PAL:

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	27	-	MHz	
Hsync	Period		t_H	-	1728	-	t_{DCLK}	
	Display period		t_{hdisp}		1440		t_{DCLK}	
	Back porch		t_{hbp}	-	241	-	t_{DCLK}	
	Front porch		t_{hfp}	0	1	-	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	-	t_{DCLK}	
Vsync	Period	Odd	t_V	-	312.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}		288		t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	24	-	t_H	
		Even		-	24.5	-		

5. Command Register Map

a. Command Timing: Serial Peripheral Interface

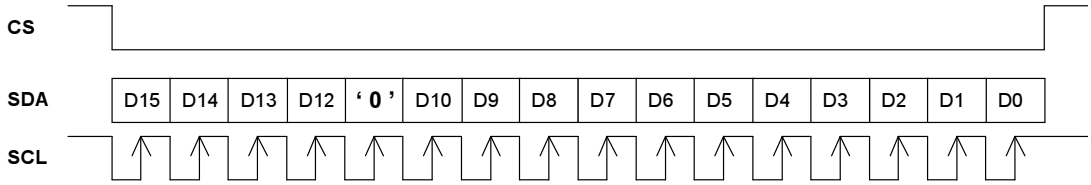
Configuration of serial data at SDA terminal

MSB LSB

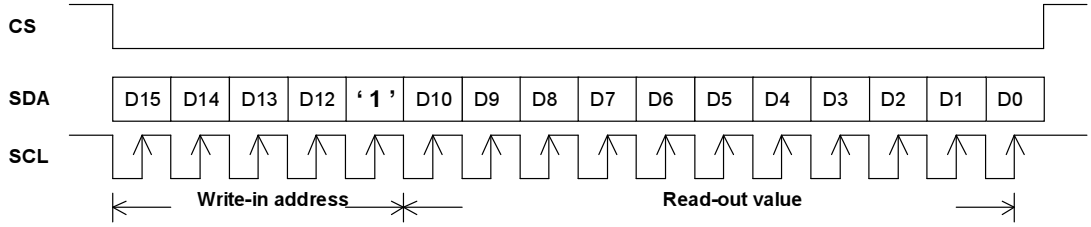
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register address				R/W	DATA										

Note: R/W = '0' ➔ Write mode R/W = '1' ➔ Read mode

Write mode waveform

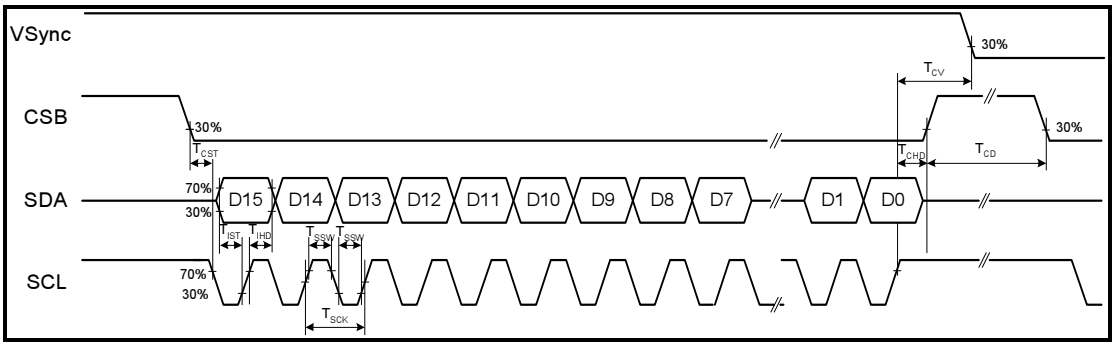


Read mode waveform

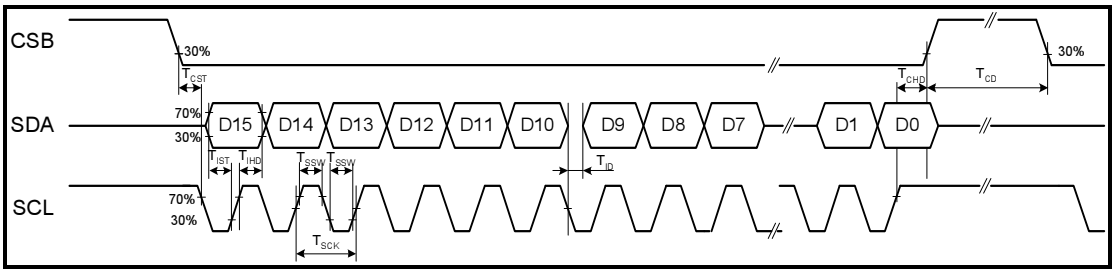


b. SPI timing diagram

AC serial interface write mode timings



AC serial interface read mode timings



c. Serial setting map

Reg N°	ADDRESS				CONTENT											
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

R0	0	0	0	0	R/W	-	-	*		*	U/D	SHL	GRB	STB	SHDB	SHCB
R1	0	0	0	1	R/W	-	-	-	-	*	PARAL	PALM	PAL	SEL		
R2	0	0	1	0	R/W	-	-	DDL_E	DDL							
R3	0	0	1	1	R/W	-	-	-	-	-	*		HDL			
R4	0	1	0	0	R/W	-	-	-	-	*	*			*	*	*
R5	0	1	0	1	R/W	-	-	-	-	-	-	-	CONTRAST			
R6	0	1	1	0	R/W	-	-	-	-	BRIGHTNESS						
R7	0	1	1	1	R/W	-	-	-	-	-	-	-	-	-	-	-
R8	1	0	0	0	R/W	-	-	-	-	-	-	-	VCOM_AC			
R9	1	0	0	1	R/W	-	-	-	-	VDCE	VCOM_DC					
R10	1	0	1	0	R/W	-	-	-	-	1	1	0	*		*	

Reg N°	ADDRESS				DEFAULT VALUES											
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	R/W	-	-	(00)		(0)	(1)	(1)	(1)	(1)	(0)	(1)
R1	0	0	0	1	R/W	-	-	-	-	(0)	(0)	(1)	(0)	(001)		
R2	0	0	1	0	R/W	-	-	(0)	(46h)							
R3	0	0	1	1	R/W	-	-	-	-	-	(01)		(7h)			
R4	0	1	0	0	R/W	-	-	-	-	(1)	(010)			(0)	(1)	(1)
R5	0	1	0	1	R/W	-	-	-	-	-	-	-	(8h)			
R6	0	1	1	0	R/W	-	-	-	-	(40h)						
R7	0	1	1	1	R/W	-	-	-	-	-	-	-	-	-	-	-
R8	1	0	0	0	R/W	-	-	-	-	-	-	-	(7h)			
R9	1	0	0	1	R/W	-	-	-	-	(1)	(2Dh)					
R10	1	0	1	0	R/W	-	-	-	-	(1)	(1)	(0)	(01)		(10)	

* Reserved

Note: Register R0/(D8,D7) must be (01)

d. SPI AC specification

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Serial clock period	Tsck	320	-	-	ns
Serial clock duty cycle	Tscw	40	50	60	%
Serial clock width low/high	Tssw	120	-	-	ns
Serial data setup time	Tist	120	-	-	ns
Serial data hold time	Tihd	120	-	-	ns
Serial data output delay	Tid	-	-	60	ns

CSB setup time	Tcst	120	-	-	ns
CSB data hold time	Tchd	120	-	-	ns
Chip select distinguish	Tcd	1	-	-	us
Delay between CSB and Vsync	Tcv	1	-	-	us

- Each serial command consists of 16 bits of data which is loaded one bit a time at the **rising edge** of serial clock SCL.
- Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
- The serial control block is operational after power on reset, but commands are established by the **Vsync** signal. If command is transferred multiple times for the same register, **the last command before the Vsync signal is valid.**
- If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
- If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data before the rising edge of CS pulse are valid data.
- Serial block operates with the SCL clock
- Serial data can be accepted in the power save mode.

e. Description of serial control data

R0: System settings

Address	Bit	Description		Default
0000	[5..0]	Bit5(U/D)	Vertical shift direction selection.	0_0011_1101b
		Bit4(SHL)	Horizontal shift direction selection.	
		Bit3(GRB)	Global reset.	
		Bit2(STB)	Standby mode setting.	
		Bit1(SHDB)	DC-DC converter shutdown setting.	
		Bit0(SHCB)	Charge Pump shutdown setting.	

Bit5	UD function
0	Flip vertically
1	**(default)**

Bit4	SHL function
0	Flip horizontally
1	**(default)**

Bit3	GRB function
0	The controller is reset, the charge pump and DCDC are off. Reset all registers to default value.
1	Normal operation. **(default)**

Bit2	STB function
0	T-CON, source driver and DC-DC converter are off. All outputs are High-Z.
1	Normal operation. **(default)**

Bit1	SHDB function
0	DC-DC converter is off. **(default)**
1	DC-DC converter is on. DC-DC controlled by STB and power on/off sequence.

Bit0	SHCB function
0	Charge Pump converter is off.
1	Charge Pump converter is on. **(default)** Charge Pump controls by STB and power on/off sequence.

R1: Timings settings

Address	**Bit**	**Description**		**Default**
0001	[4..0]	Bit4(PALM)	PAL 1/6, PAL1/6,8 selection.	001_0001b
		Bit3(PAL)	PAL/NTSC selection.	
		Bit2-0(SEL)	Input data format selection.	

Bit4	PALM function
0	Manual PAL/NTSC selection
1	Automatic PAL/NTSC detection **(default)**

Bit3	PAL function
0	NTSC Input format (240 active line). **(default)**
1	PAL Input format (288 active line).

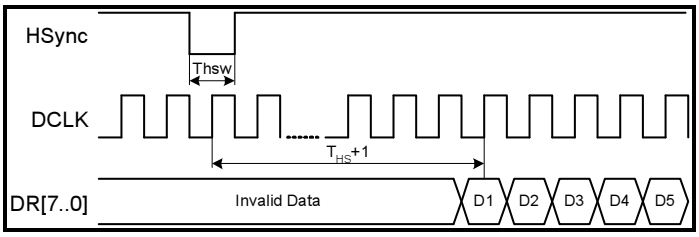
Bit2-0	SEL function
000	UPS051 path, special data format: DDX.

001	UPS052 320RGB 24.54MHz data format. **(default)**
010	UPS052 360RGB 27MHz data format.
011	YUV mode A 640Y 320CrCb 24.54MHz data format.
100	YUV mode A 720Y 360CrCb 27MHz data format.
101	YUV mode B 640Y 320CrCb 24.54MHz data format.
110	YUV mode B 720Y 360CrCb 27MHz data format.
111	CCIR 656 720Y 360CrCb 27MHz data format.

R2: Data delay settings

Address	Bit	Description		Default
0010	[8..0]	Bit8(DDL_E)	DDL setting selection.	0_0100_0110b
		Bit7-0(DDL)	Horizontal Data start delay selection.	

DDL_E	DDL	T_{HS}	Unit	Remark
X	00h	0	DCLK	UPS051
X	46h	70 (Default)	DCLK	
X	FFh	255	DCLK	
0	XXh	241(fixed)	DCLK	UPS051/YUV
1	00h~FFh	64~319	DCLK	
0	XXh	61(fixed)	DCLK	Parallel RGB
1	00h~FFh	0~255	DCLK	



R3: Vertical delay settings

Address	Bit	Description		Default
0011	[5..0]	Bit5-4(OEA)	Odd Even advance selection.	01_0111b
		Bit3-0(HDL)	Vertical delay selection.	

Bit5-4	OEA function (only in CCIR mode)
00	Display start @T_{VS} delay for Odd and Even field.

01	Display start @ T_{VS} delay for Odd field and @ T_{VS} +1 for Even field. **(default)**
1X	Display start @ T_{VS} +1 delay for Odd field and @ T_{VS} for Even field.

Bit3-0	HDL function
0000	TSTV=TVStyp - 7 Hsync period
0111	TSTV=TVStyp - 0 Hsync period. **(default)**
1111	TSTV=TVStyp + 8 Hsync period

R9: VCOM DC settings

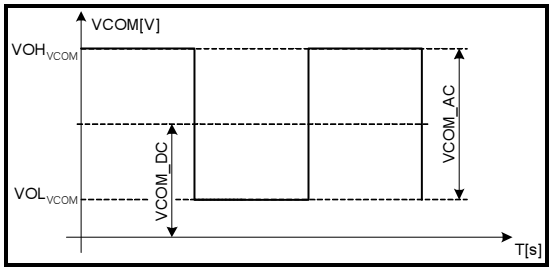
Address	Bit	Description		Default
1001	[6..0]	Bit6(VDCE)	VCOM DC Enable signal.	110_1101b
		Bit5-0(VCOM_DC)	VCOM DC level adjustment. Step 20mV/LSB.	

Bit6	VDCE function
0	VCOM DC function disables VCOM pin HighZ. VCOM_DC=VCOM_AC/2.
1	DC voltage of VCOM follows VCOM_DC settings.**(default)**

Bit5-0	VCOM DC level	
	MVA/Normal LC	Low Voltage LC
00h	1.4V	0.4V
2Dh	2.30V **(default)**	1.30V **(default)**
3Fh	2.66V	1.66V

VOL_{VCOM}= VCOM_DC-VCOM_AC/2

VOH_{VCOM}= VCOM_DC+VCOM_AC/2



E. Optical specifications (Note 1, 2)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	θ =0°	-	7	10	ms	Note 4
Fall	Tf		-	28	40	ms	
Contrast ratio	CR	At optimized viewing angle	200	300	-		Note 5, 6
Viewing Angle							
Top			35	50	-		
Bottom		CR≧10	40	55	-	deg.	Note 7
Left			45	60	-		
Right			45	60	-		
Brightness	Y_L	θ =0°	250	300	-	cd/m^2	Note 8
White Chromaticity	X	θ =0°	0.26	0.31	0.36		
	y	θ =0°	0.28	0.33	0.38		

Note 1 Ambient temperature = 25□.

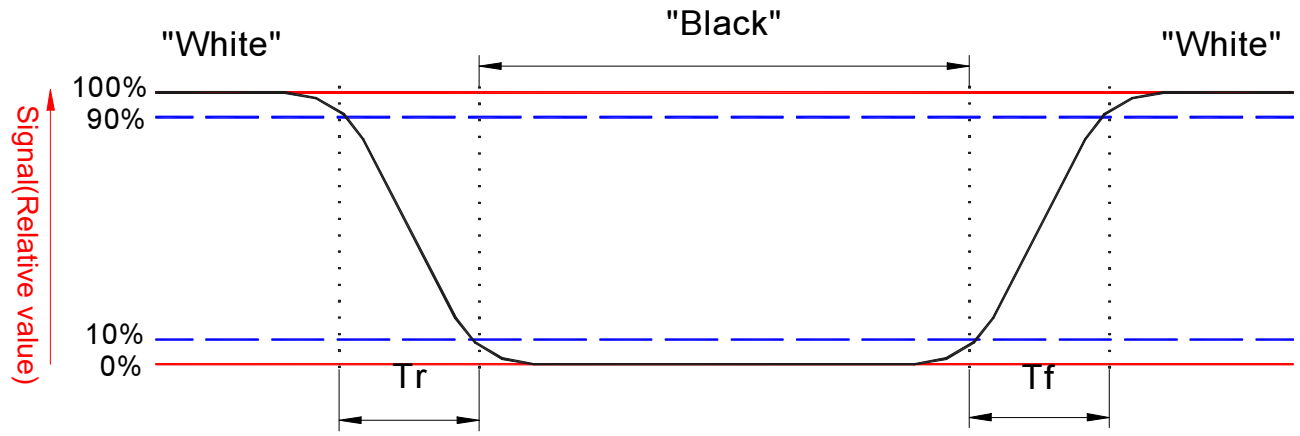
Note 2 Measured in the dark room

Note 3 Measured on the center area of panel with a field angle of 1° by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4 Definition of response time:

Output signals of photo detector are measured when the input signals are changed from “black” to “white” (falling time) and from “white” to “black” (rising time), respectively.

Response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to the figure as follows.



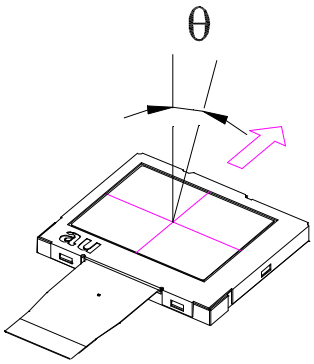
Note 5 Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6 White Vi = V_{i50} ⊣ 1.5V
Black Vi = V_{i50} ± 2.0V
“±” means that the analog input signal swings in phase with COM signal.
“⊣” means that the analog input signal swings out of phase with COM signal.
$V_{i50:}$ The analog input voltage when transmission is 50%
100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7 Definition of viewing angle:
Refer to the figure as follows.



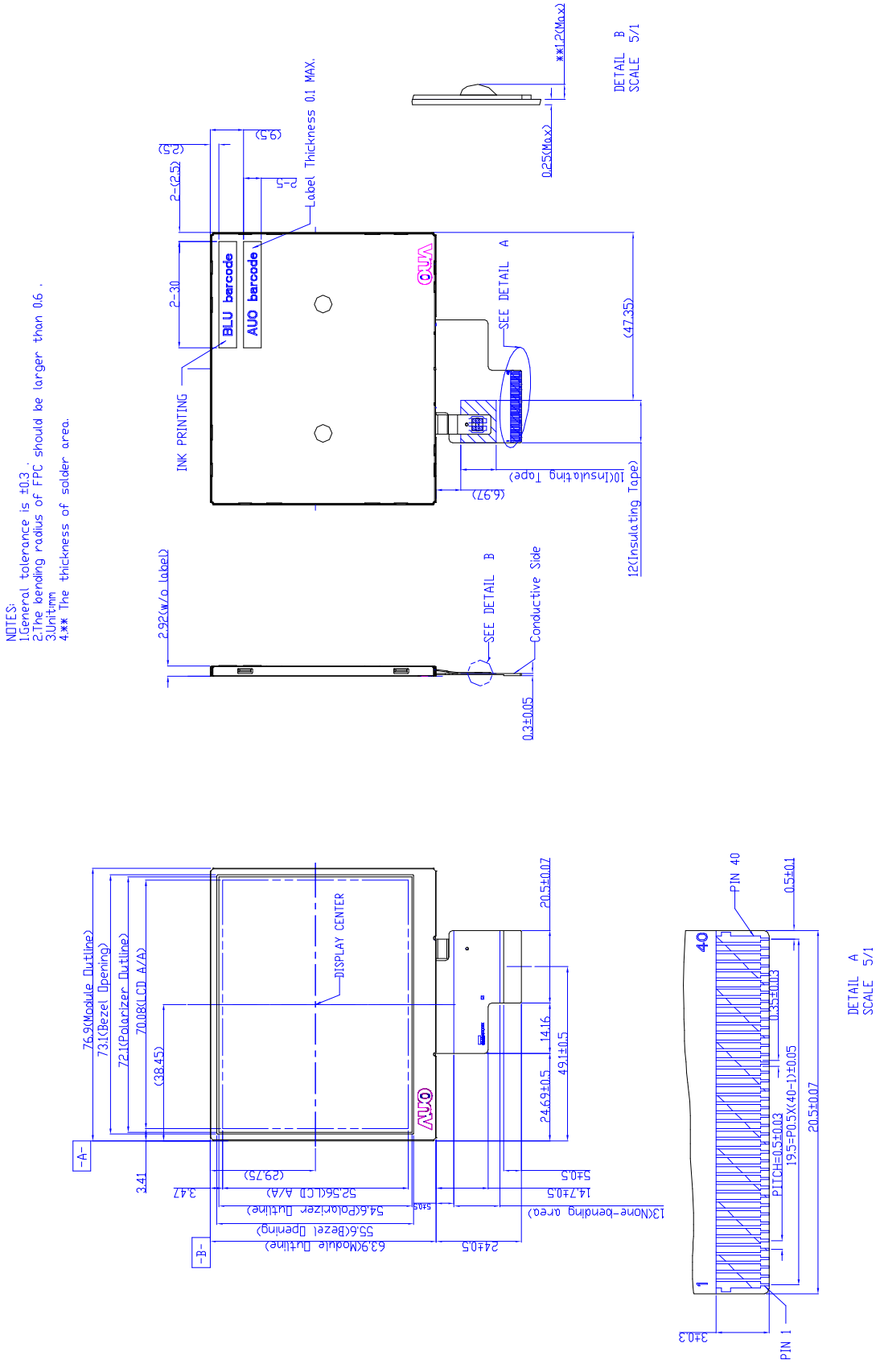
Note 8 Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

F. Reliability Test Items

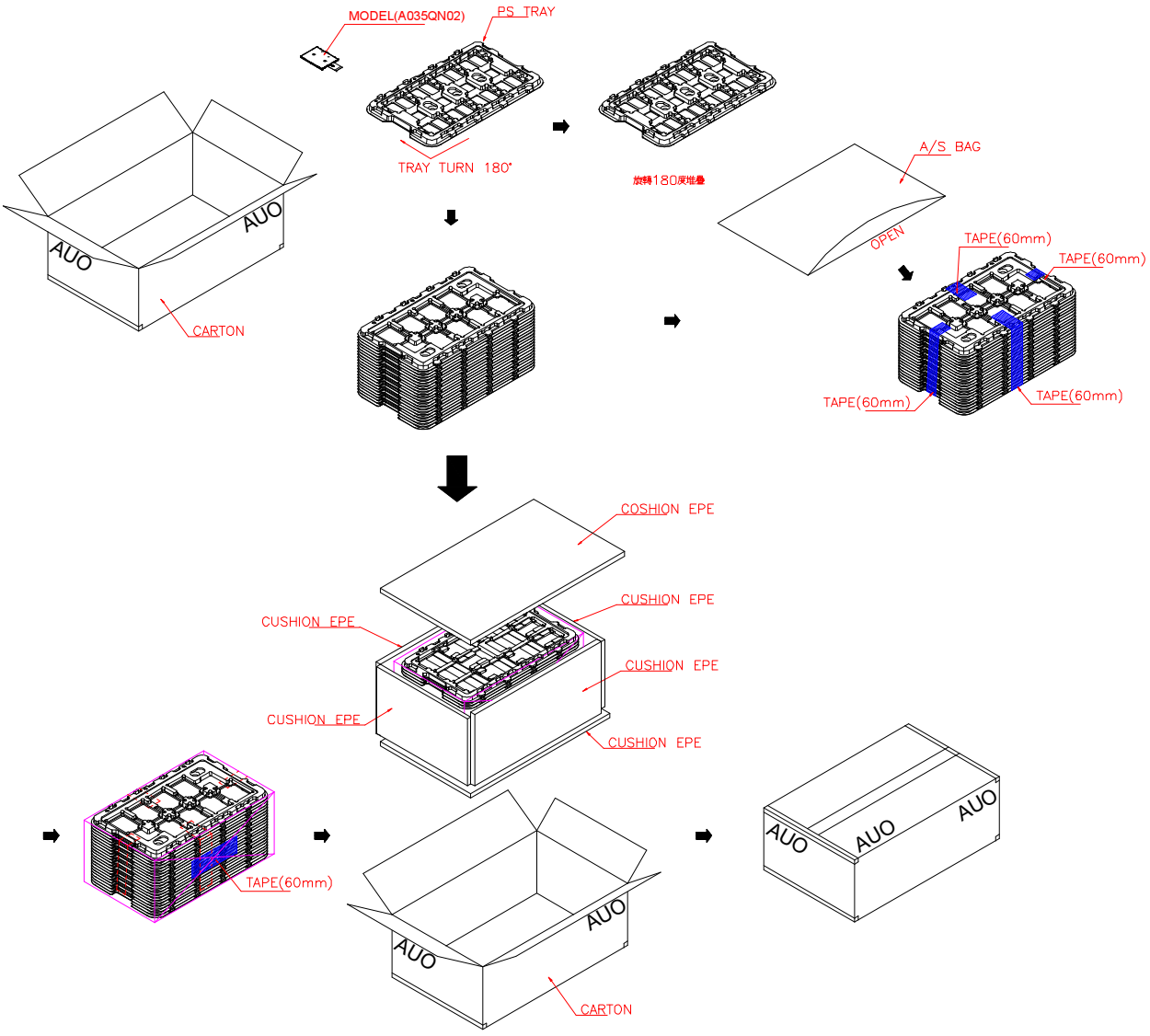
No.	Test items	Conditions	Remark
1	High temperature storage	Ta = 80□ 240Hrs	
2	Low temperature storage	Ta = -25□ 240Hrs	
3	High temperature operation	Ta = 60□ 240Hrs	
4	Low temperature operation	Ta = 0□ 240Hrs	
5	High temperature and high humidity	Ta = 60□. 90% RH 240Hrs	Operation
6	Heat shock	-25□~80□, 50 cycles, 2Hrs/cycle	Non-operation
7	Electrostatic discharge	± 200V,200pF (0Ω), once for each terminal	Non-operation
8	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz	IEC 68-34
9	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1: Ta: Ambient temperature.

G. Outline Dimension



H. Packing Form



MAX. CAPACITY:160 MODULES
MAX. WEIGHT: 12Kg
MEAS. 520mm*340mm*250mm

I. Application Note

1. Application circuit

The folowing drawing is the application circuit recommended.

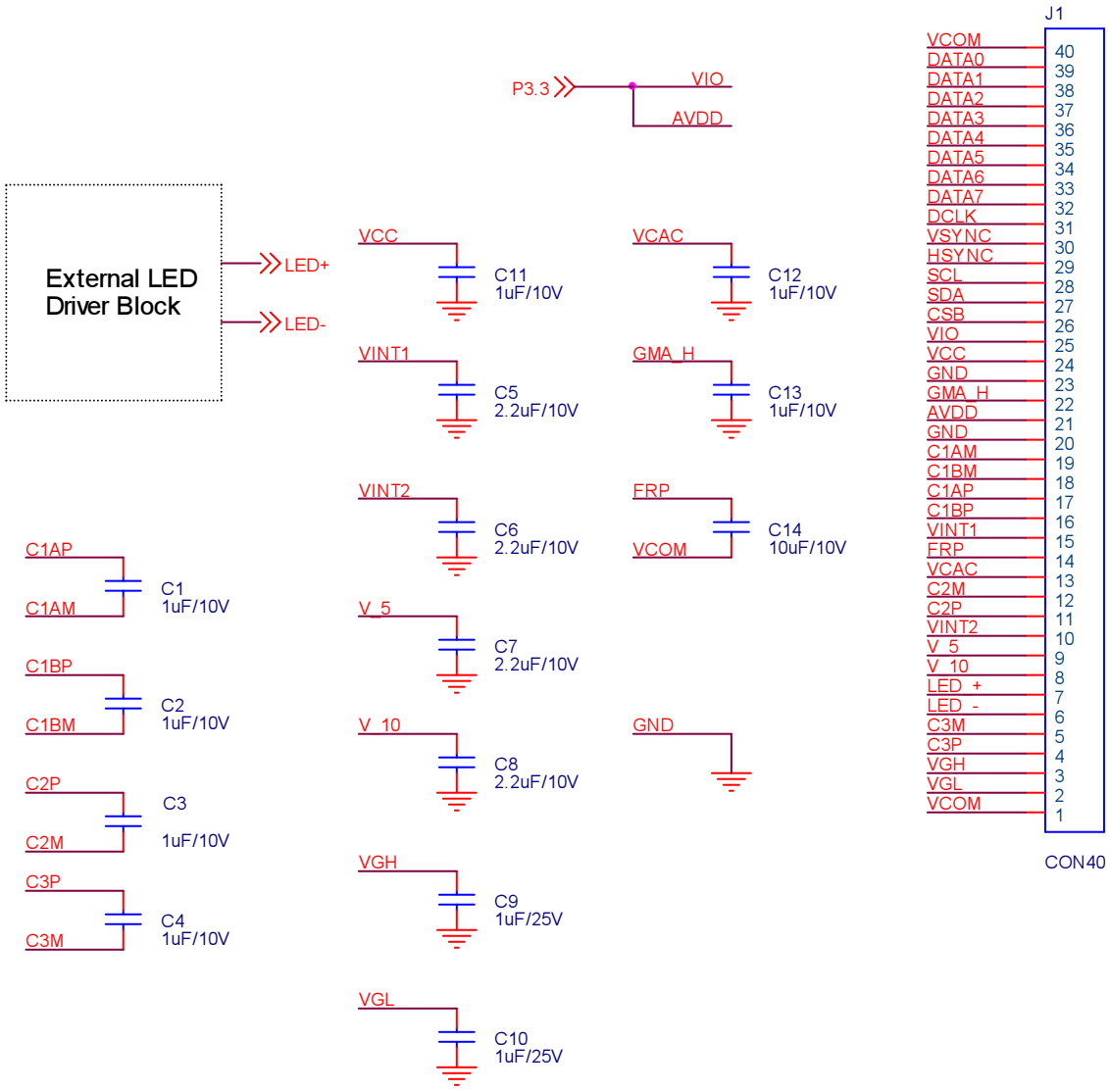
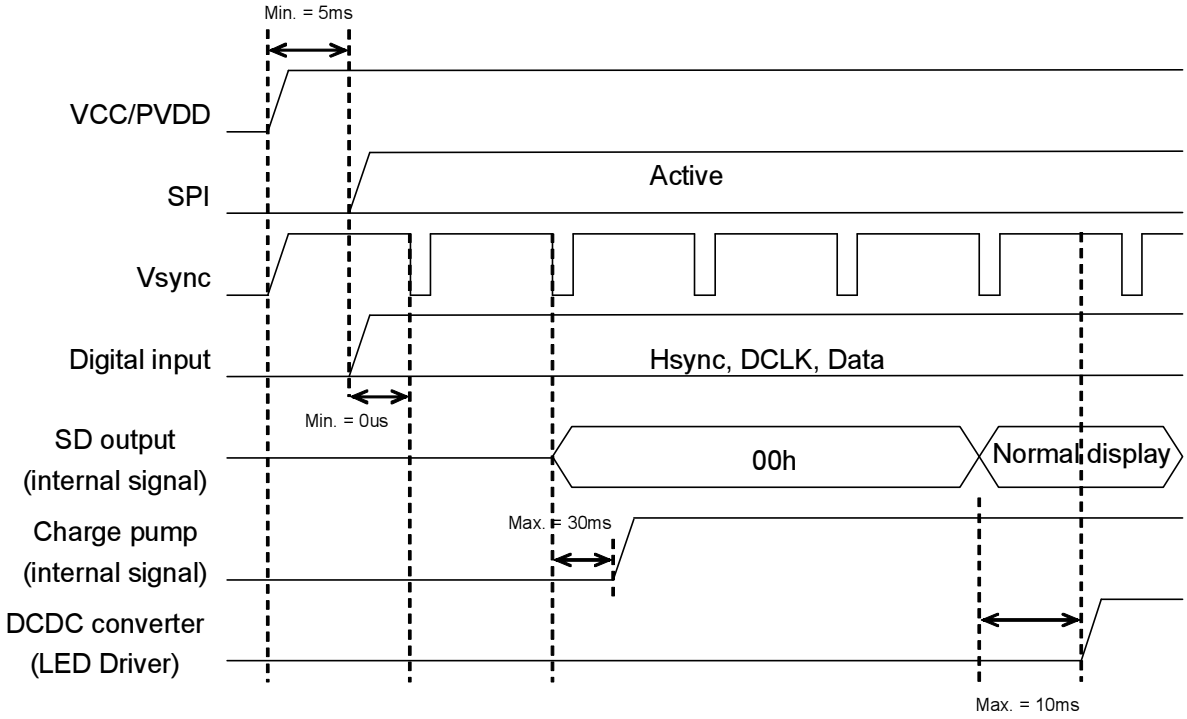


Table of Capacitors

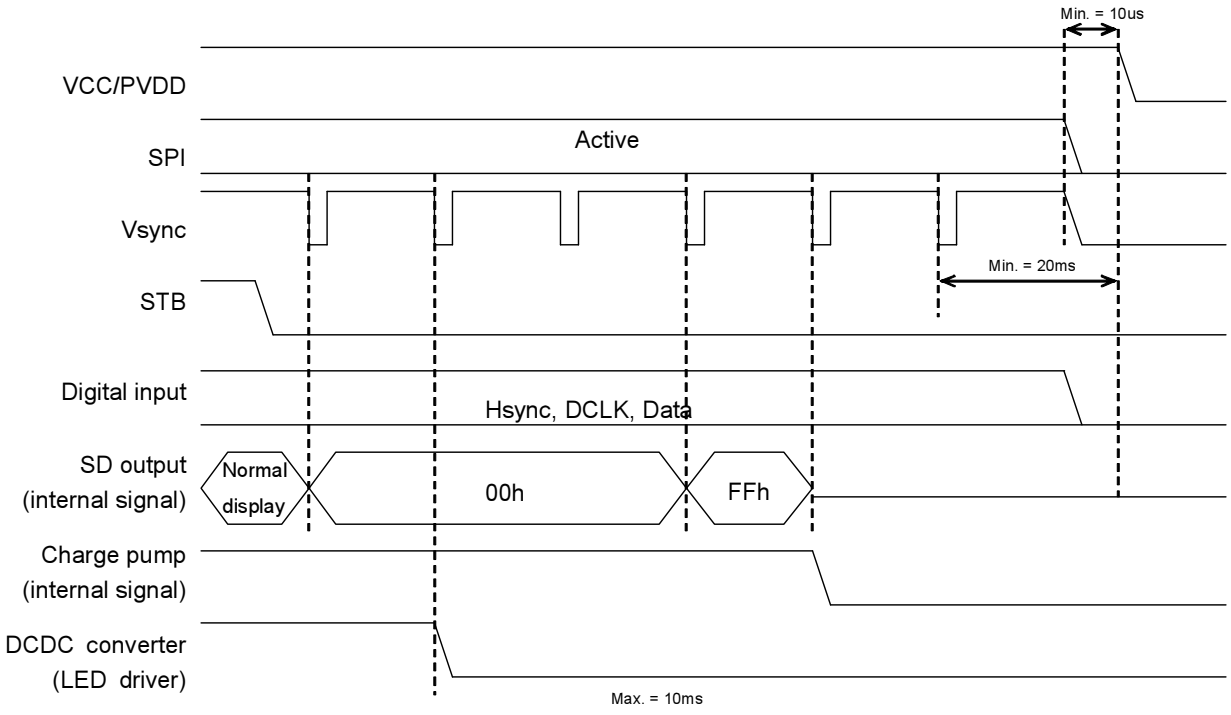
Item	Quantity	Reference	Part
1	7	C1,C2,C3,C4,C11,C12,C13	1uF/10V/X7R
2	4	C5,C6,C7,C8	2.2uF/10V/X7R
3	2	C9,C10	1uF/25V/X7R
4	1	C14	10uF/10V/X7R

2. Power on/ off sequence

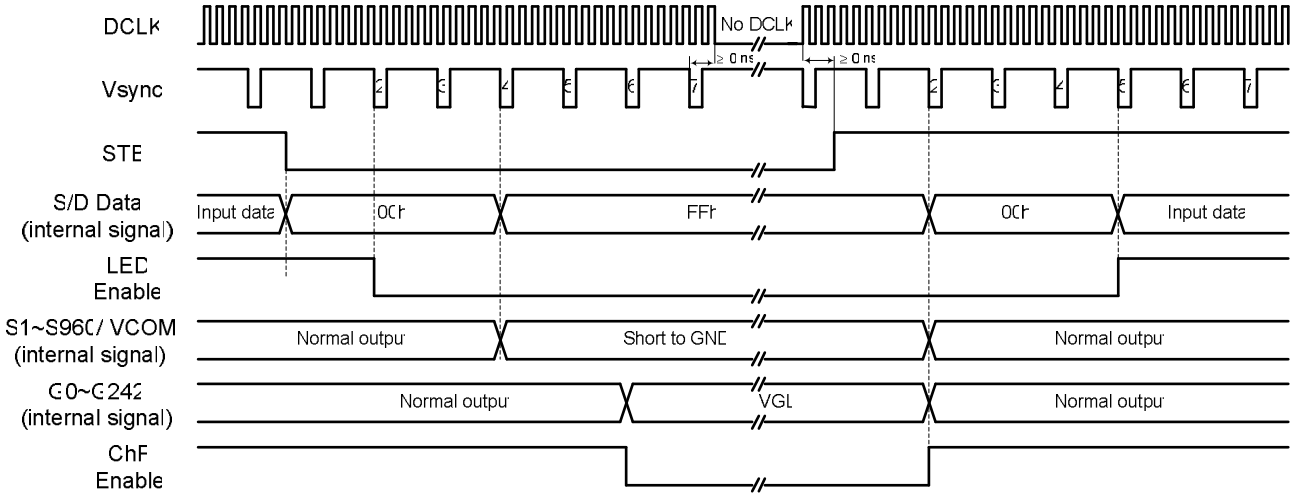
POWER ON



POWER OFF

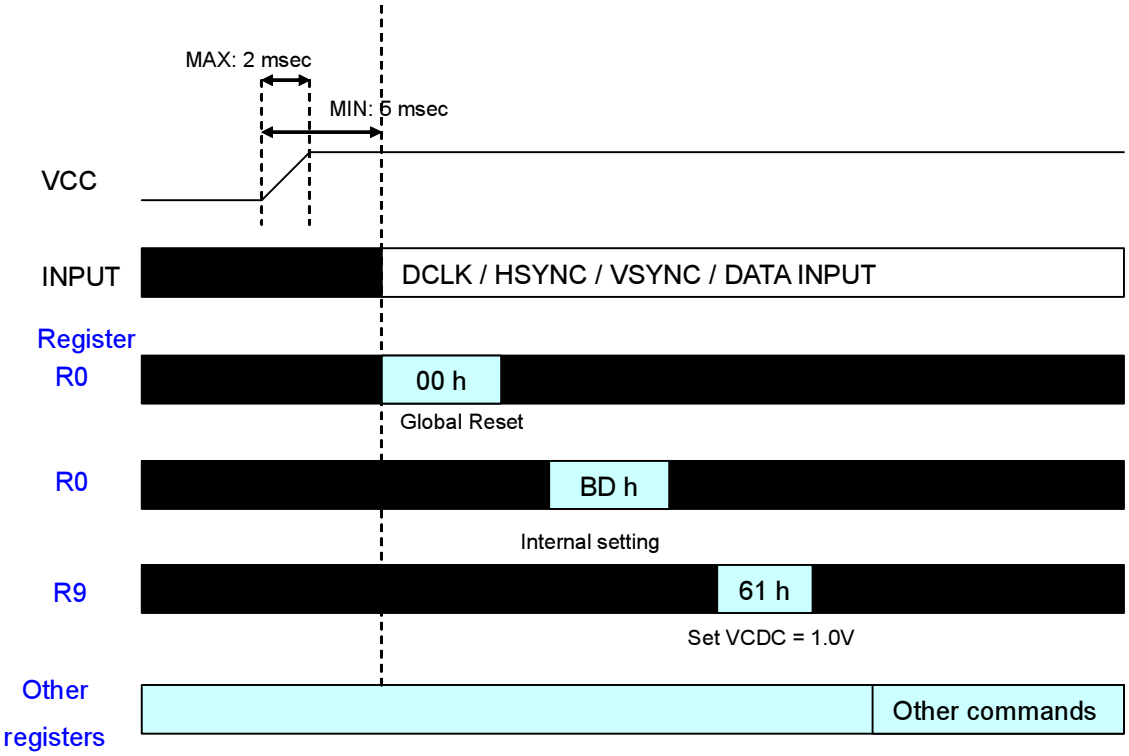


3. Standby timing

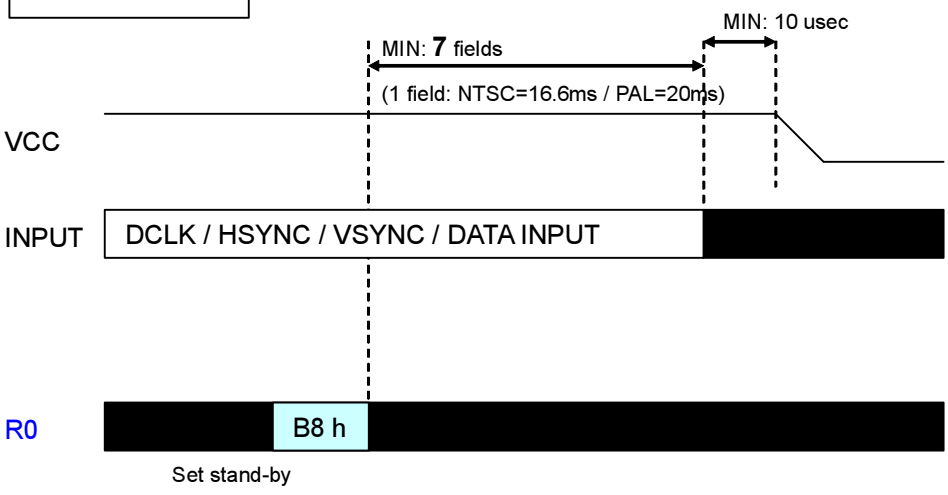


4. Recommand UPS052 320RGB (24.54MHz) Register Settings

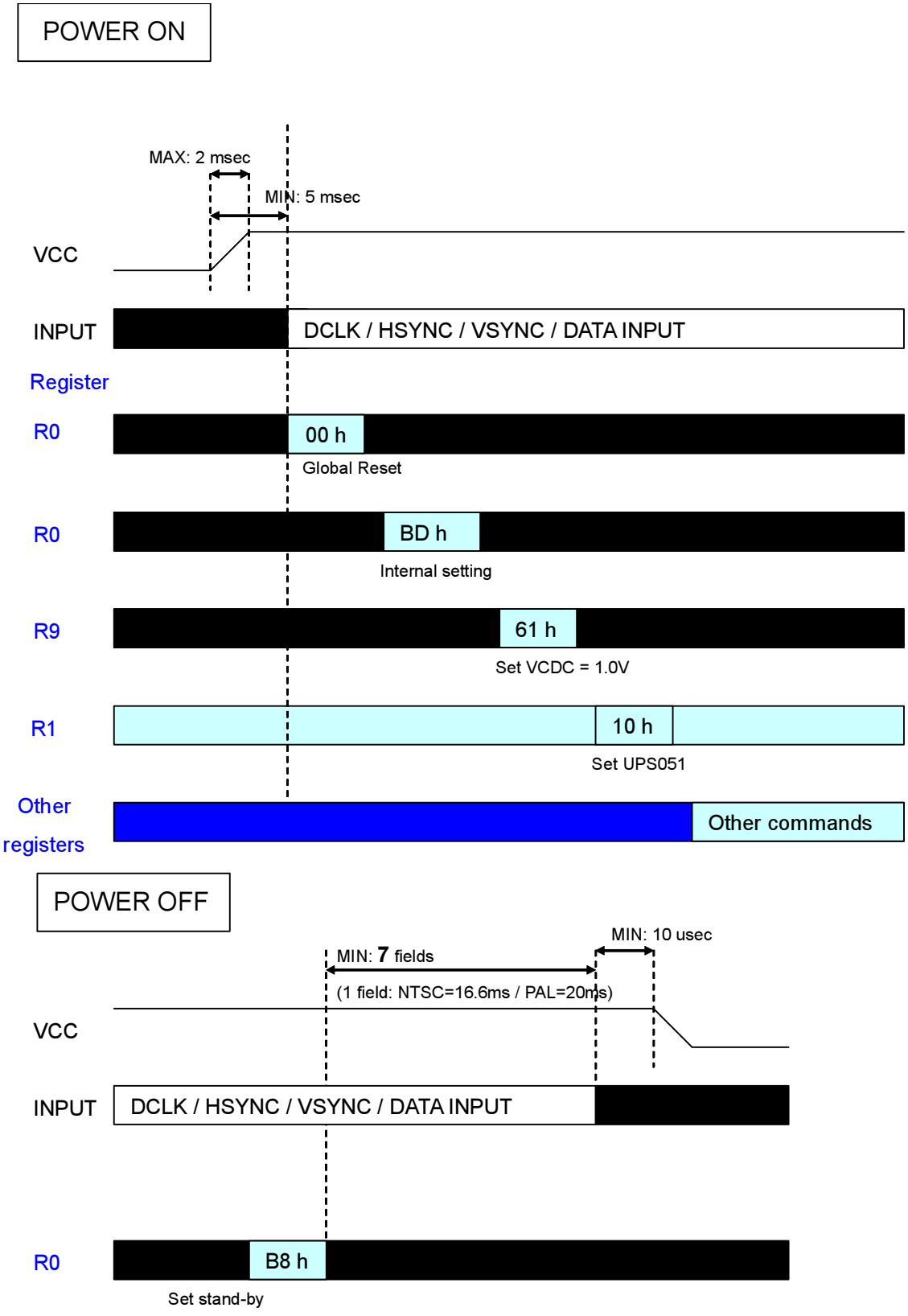
POWER ON



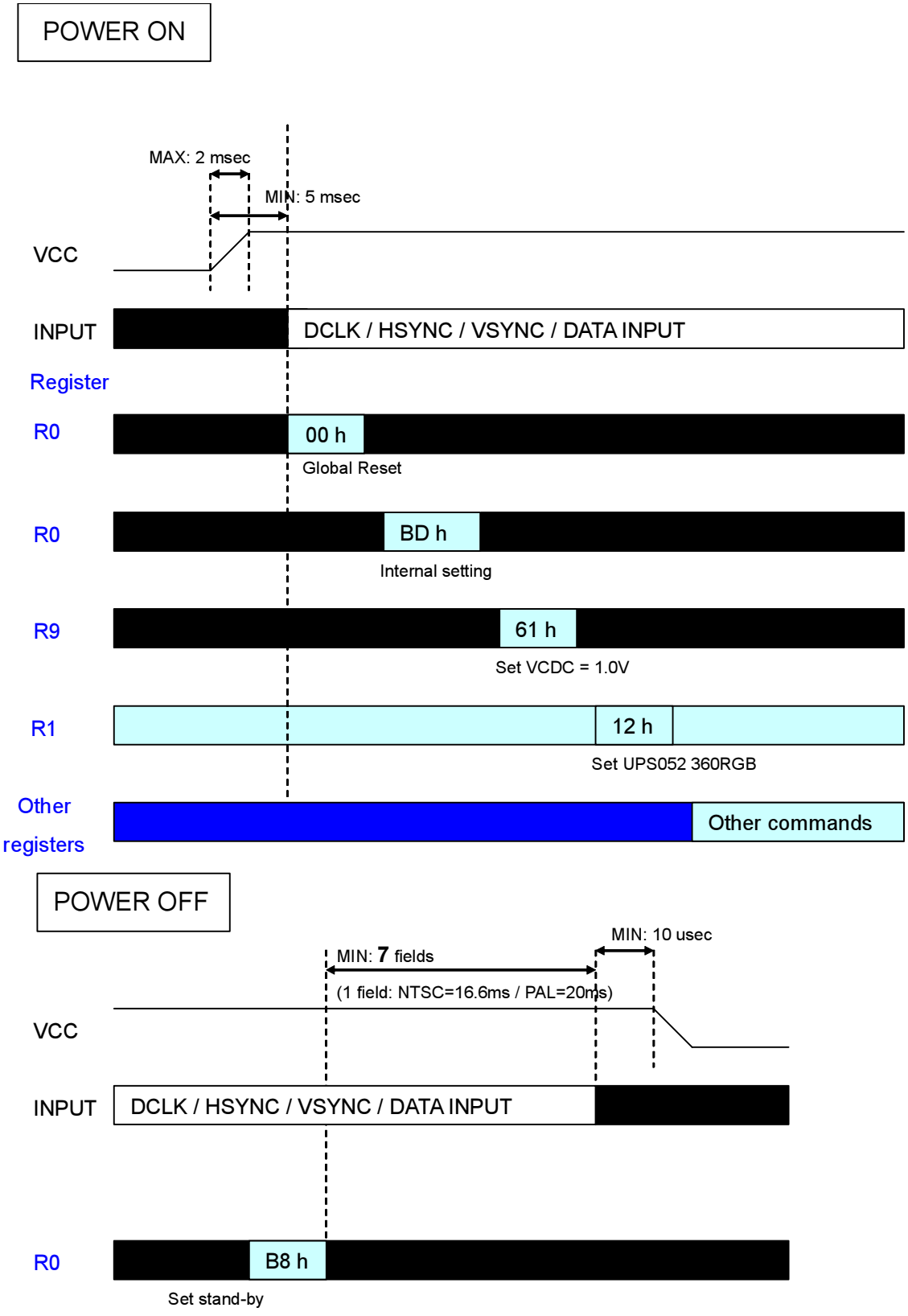
POWER OFF



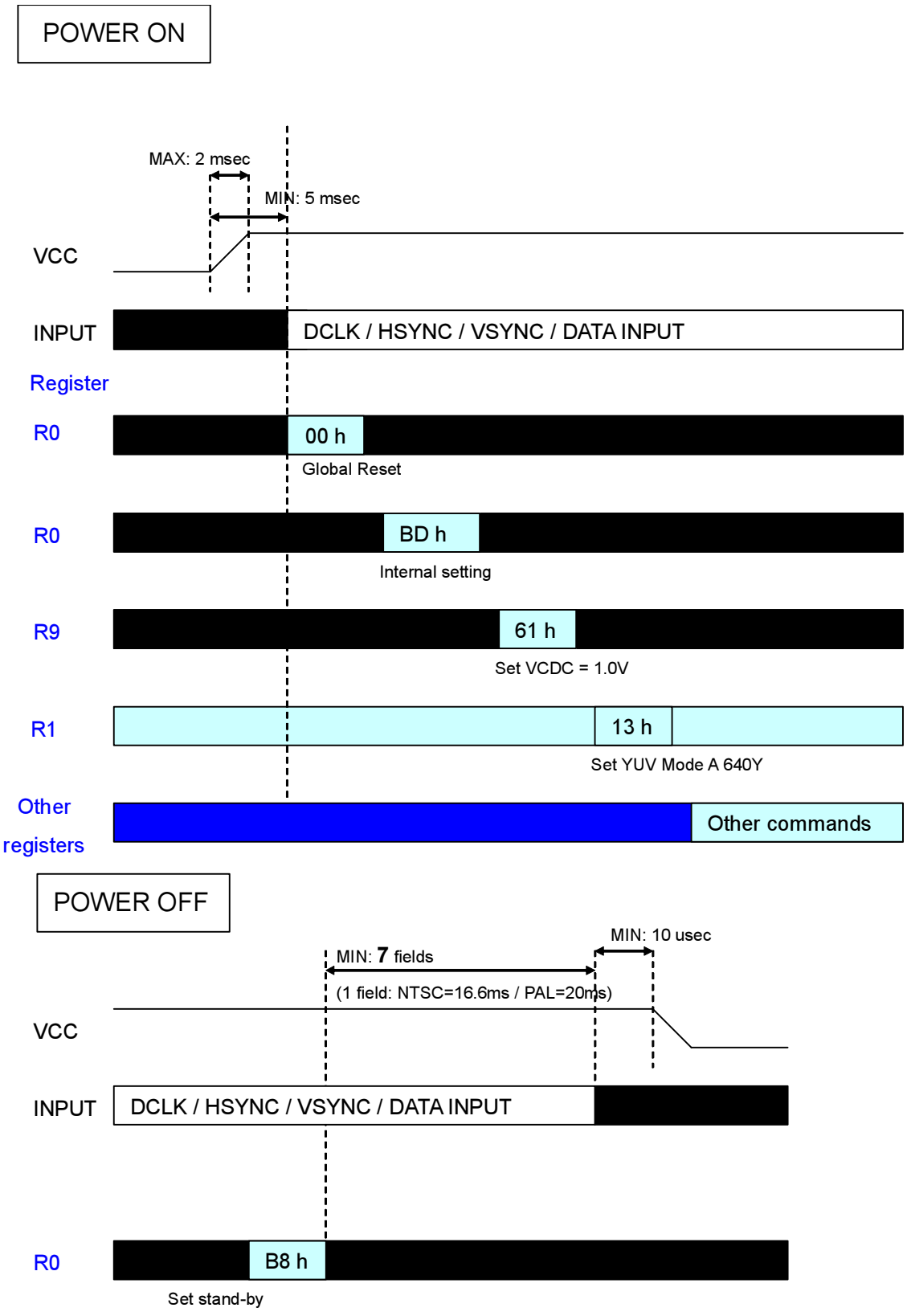
5. Recommand UPS051 Register Settings



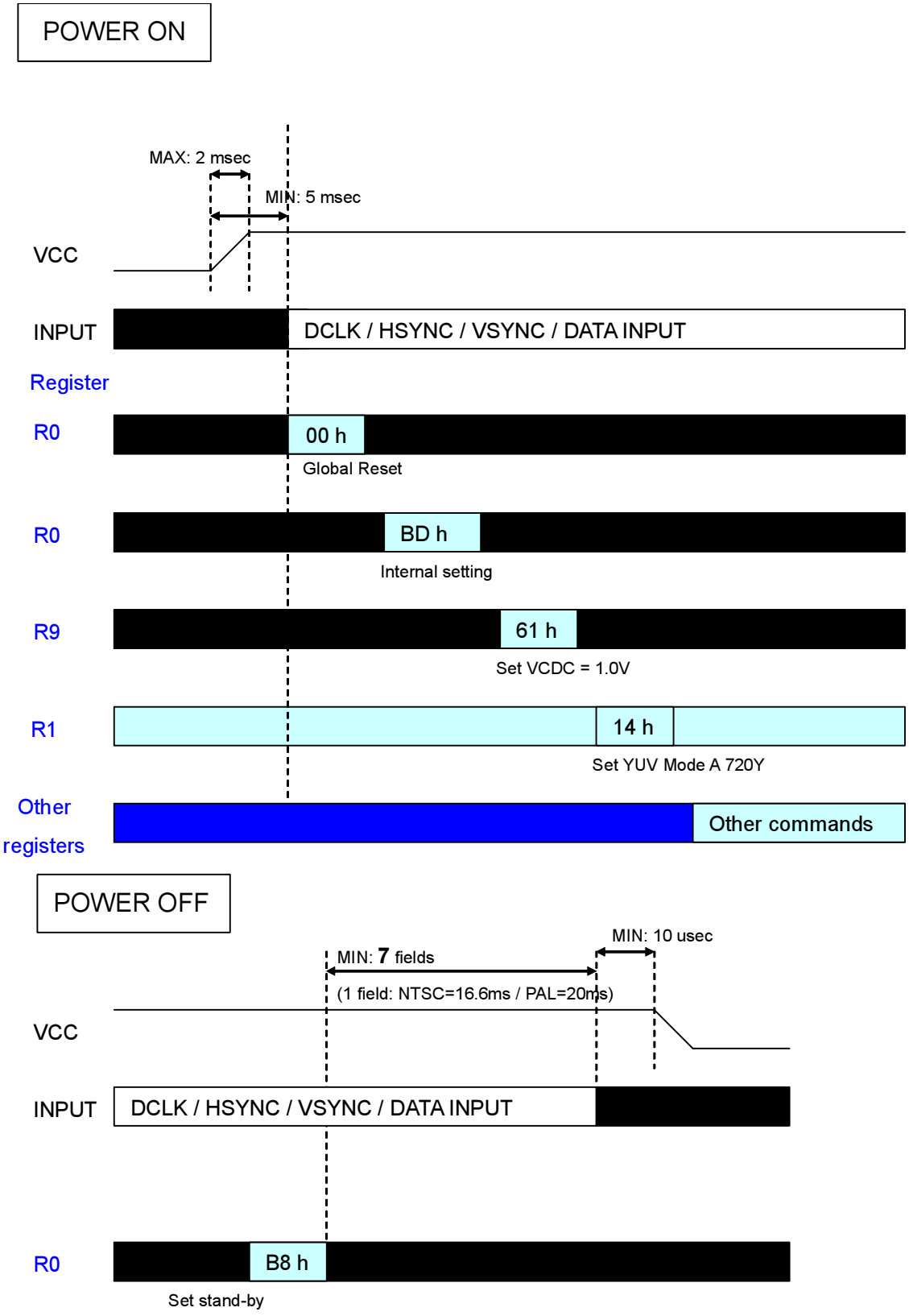
6. Recommand UPS052 360RGB (27MHz) Register Settings



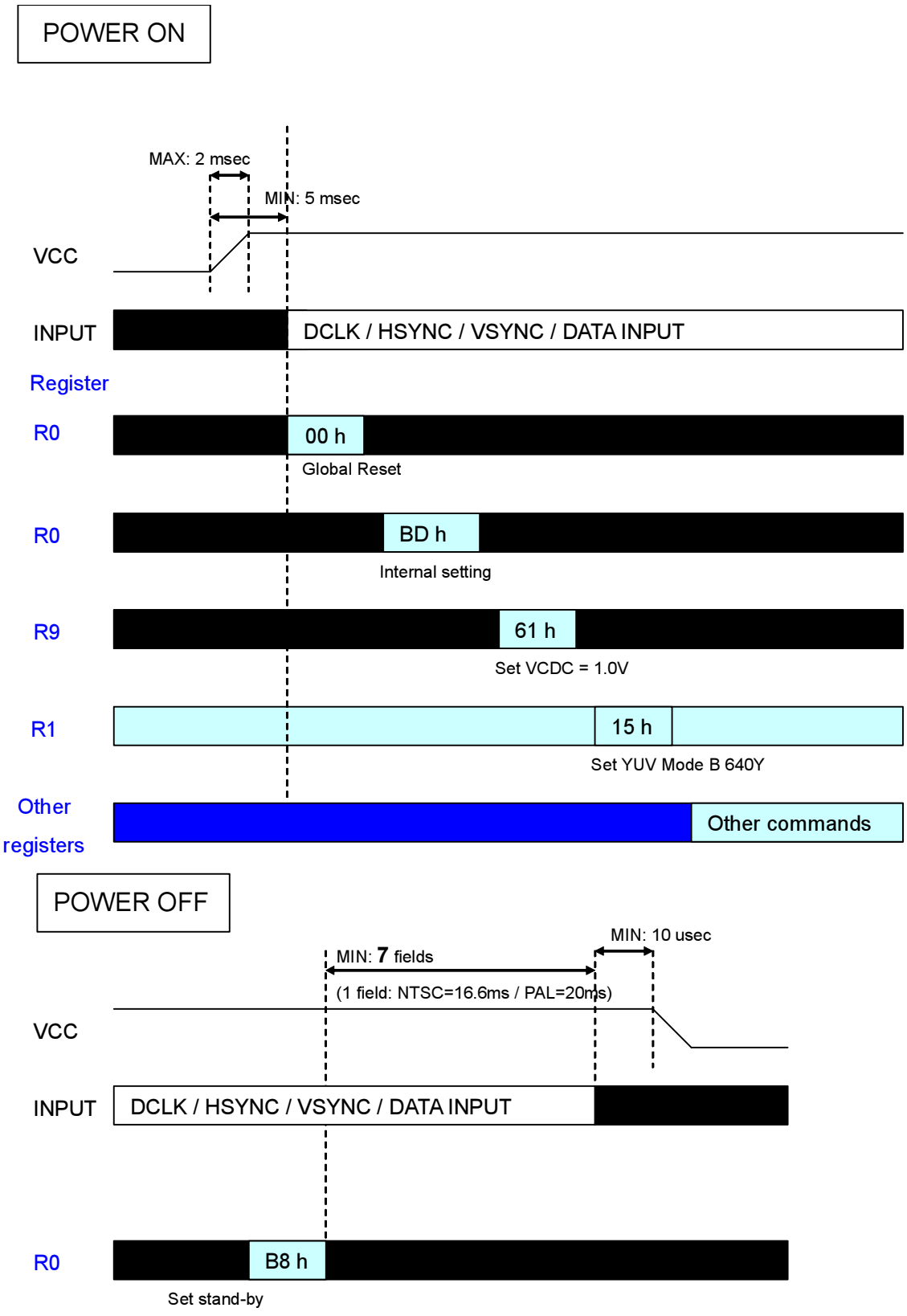
7. Recommand YUV Mode A 640Y 320CrCb (24.54MHz) Register Settings



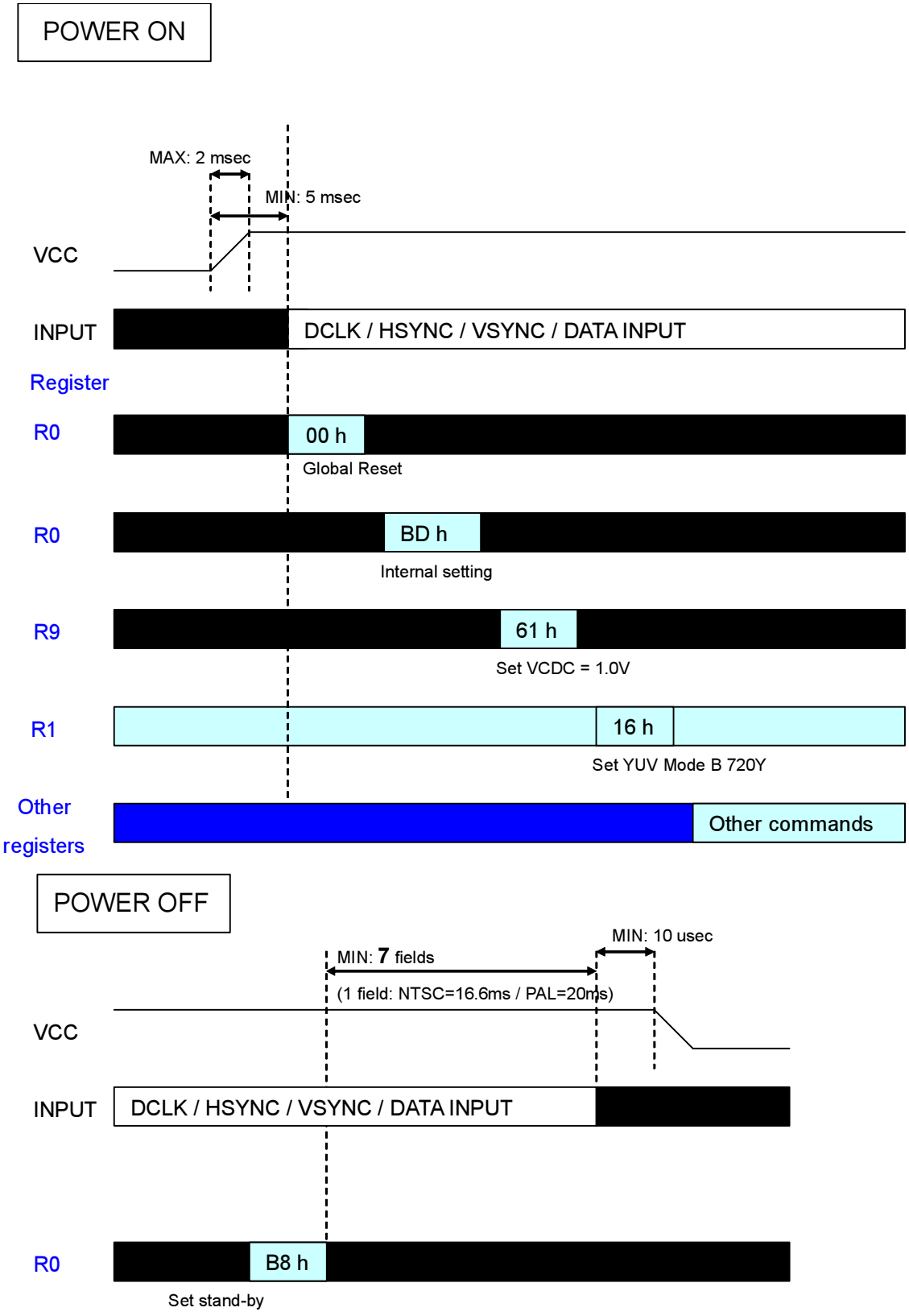
8. Recommand YUV Mode A 720Y 360CrCb (27MHz) Register Settings



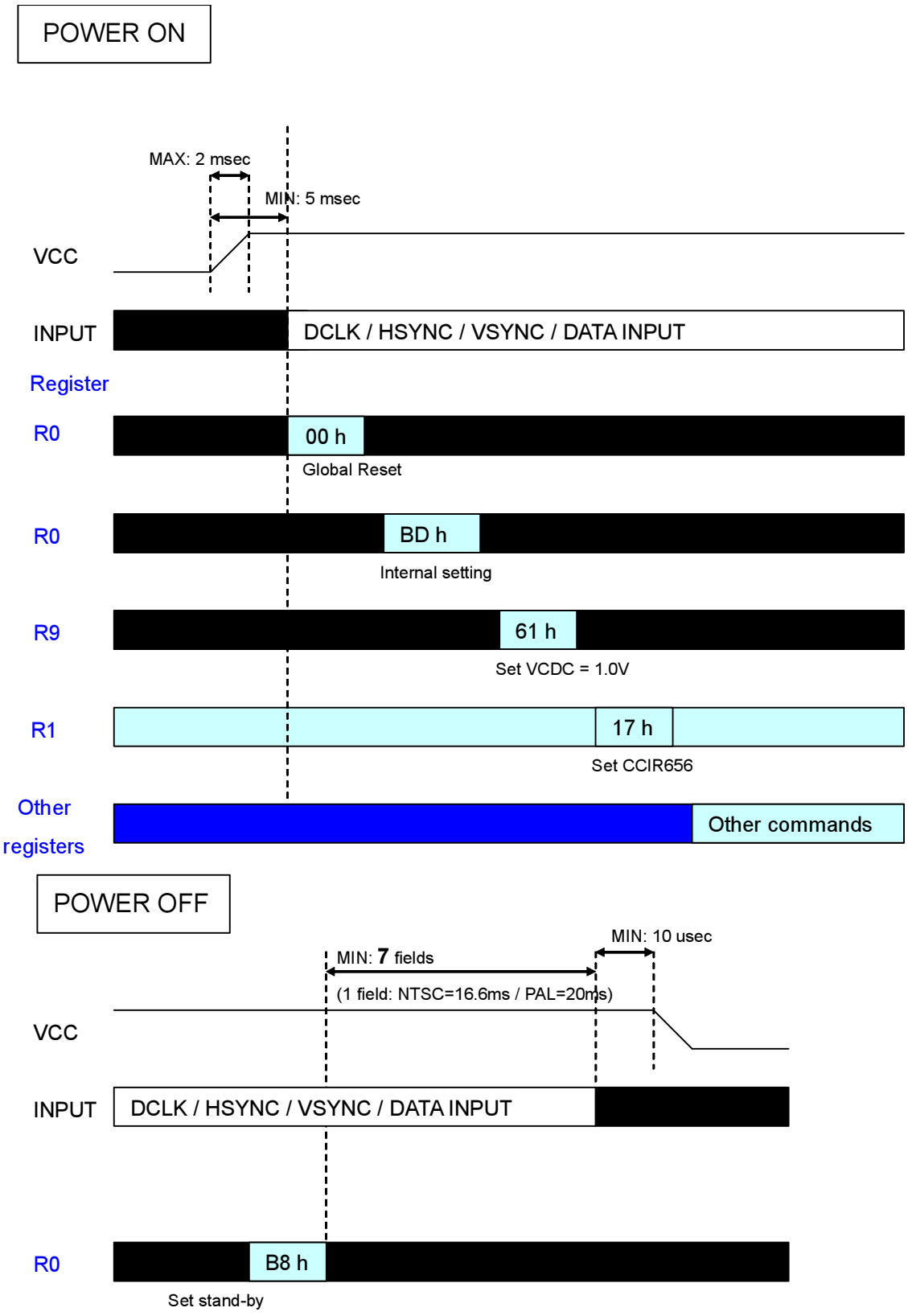
9. Recommand YUV Mode B 640Y 320CrCb (24.54MHz) Register Settings



10. Recommand YUV Mode B 720Y 360CrCb (27MHz) Register Settings



11. Recommand CCIR656 720Y 360CrCb (27MHz) Register Settings



12. Recommand ESD Protection

- In order to recover from register corruption cause from ESD, AUO suggests that registers should be set repeatedly.
- AUO suggests the bezel connects to system GND to enhance ESD protection ability.