CUSTOMER APPROVAL SHEET

Company Name	
MODEL	
CUSTOMER APPROVED	Title : Name :

- ☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.2)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.**
- ☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver.**
- ☐ **CUSTOMER REMARK :**

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Product Specification
3" COLOR TFT-LCD MODULE

Model Name： **A030FL01 V3**

<

Planned Lifetime:	From 2009/Mar To 2010/Dec
Phase-out Control:	From 20010/Jul To 2010/Dec
EOL Schedule:	2010/Dec

>

< >Preliminary Specification

< ◆ >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

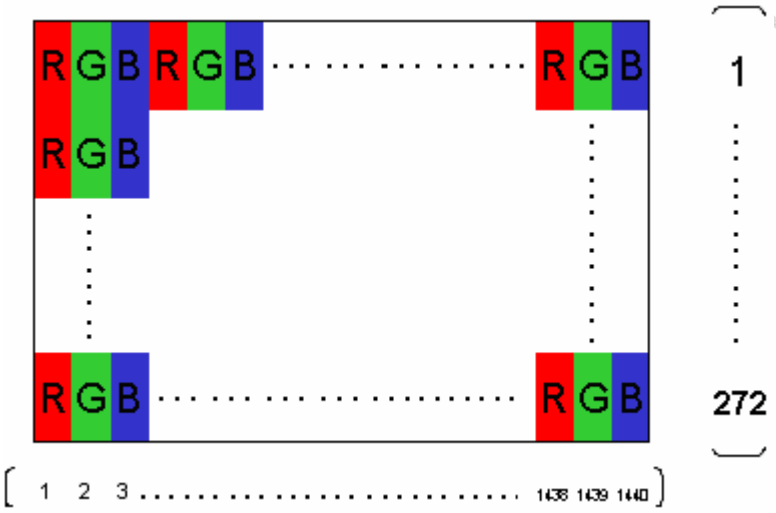
Version	Revise Date	Page	Content
0.0	2009/3/12	-	First Draft
0.1	2009/3/13	26	Update “C/R” spec.
0.2	2009/5/22	3	Add “operation & storage temperature spec”
		26	Add “NTSC spec”

Contents

A. General Information

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	480 RGB(H) × 272(V)	
2	Active Area	mm	65.52(H) × 37.128(V)	
3	Screen Size	inch	3.0” (Diagonal)	
4	Dot Pitch	mm	0.0455(H)x0.1365(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	16.7M Colors	Note 2
7	Overall Dimension	mm	76.02(H) × 43.7(V) × 2.26(T)	Note 3
8	Weight	g	TBD	
9	Display Mode	--	Normally Black	
10	Operation temperature	℃	0~60	
11	Storage temperature	℃	-25~70	

Note 1: Below figure shows dot stripe arrangement.



Note 2: The full color display depends on 8-bit data signal (pin9~34).

Note 3: Not include FPC. Refer F.outline dimension to get further information.

B. Electrical Specifications

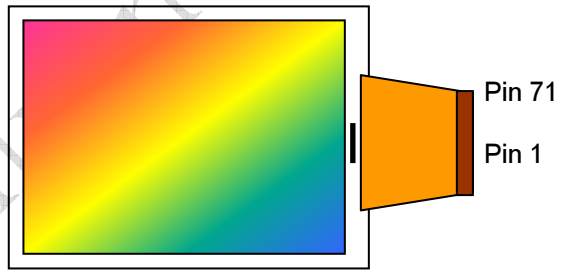
1. FPC Pin Assignment

Pin no	Symbol	Type	Description	Remark
1	VCOM	I	Common voltage	
2	FRP	O	Frame polarity	
3	VCOML	P	Power Setting Capacitor for VCOM	
4	VCOMH	P	Power Setting Capacitor for VCOM	
5	VGL	P	Power setting capacitor	
6	VGH	P	Power setting capacitor	
7	VLOUT2	P	Power setting capacitor	
8	V12	P	Connect capacitor for power circuit	
9	V11	P	Connect capacitor for power circuit	
10	V10	P	Connect capacitor for power circuit	
11	V9	P	Connect capacitor for power circuit	
12	V8	P	Connect capacitor for power circuit	
13	V7	P	Connect capacitor for power circuit	
14	VLOUT3	P	Power setting capacitor	
15	VCL	P	Power setting capacitor	
16	VDD3	P	Power setting capacitor	
17	V6	P	Connect capacitor for power circuit	
18	V5	P	Connect capacitor for power circuit	
19	V4	P	Connect capacitor for power circuit	
20	V3	P	Connect capacitor for power circuit	
21	V2	P	Connect capacitor for power circuit	
22	V1	P	Connect capacitor for power circuit	
23	VDD2	P	Power setting capacitor	
24	VDDA	P	Power setting capacitor	
25	GND	P	Ground	
26	GND	P	Ground	
27	VDD	P	Power supply for charge pump	

Pin no	Symbol	Type	Description	Remark
28	VDD	P	Power supply for charge pump	
29	VDDIO	P	Power supply for digital interface	
30	VDD_25V	P	Power setting capacitor	
31	R0	I	Red data (LSB)	
32	R1	I	Red data	
33	R2	I	Red data	
34	R3	I	Red data	
35	R4	I	Red data	
36	R5	I	Red data	
37	R6	I	Red data	
38	R7	I	Red data (MSB)	
39				N/A
40	G0	I	Green data (LSB)	
41	G1	I	Green data	
42	G2	I	Green data	
43	G3	I	Green data	
44	G4	I	Green data	
45	G5	I	Green data	
46	G6	I	Green data	
47	G7	I	Green data (MSB)	
48				N/A
49	B0	I	Blue data (LSB)	
50	B1	I	Blue data	
51	B2	I	Blue data	
52	B3	I	Blue data	
53	B4	I	Blue data	
54	B5	I	Blue data	
55	B6	I	Blue data	
56	B7	I	Blue data (MSB)	

Pin no	Symbol	Type	Description	Remark
57	GND	P	Ground	
58	DCLK	I	Pixel clock	
59	GRB	I	Global Reset	
60	HSYNC	I	Horizontal Sync Signal	
61	VSYNC	I	Vertical Sync Signal	
62	SCL	I	Serial command clock input	
63	SDA	I/O	Serial command data input	
64	CS	I	Serial command enable signal	
65	VLED+	P	LED anode	
66	VLED-	P	LED cathode	
67	DRV	O	VLED boost transistor driving signal	
68	VCOM	I	Common voltage	
69				N/A
70				N/A
71				N/A

Note 1: I: Input; O: Output; P: Power.Note: Definition of scanning direction, Refer to figure as below :



2. Electrical DC Characteristics

The following items are measured under stable condition and suggested application circuit.

2.1 TFT- LCD Typical Operation Condition

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply	VDD	3.1	3.3	3.5	V	
	VDDIO	1.65	3.3	3.5	V	
Vsync Frequency	f_V		60		Hz	
Hsync Frequency	f_H		17.16		kHz	
Main Frequency	f_{DCLK}		9.0	10.0	MHz	

Note 1: Above every operation range is based on stable operation from suggested application circuit 3.3.1.

Note 2: A built-in power-on reset circuit for VDD and VDDIO is provided within the integrated LCD driver IC. The LCD module is in default in power save mode, and a standby releasing is required after VDDIO power on through serial control interface. Please refer to the serial control interface for detail.

Note 3: The power supply of digital interface, VDDIO, is for the 1.8V digital interface requirement in the future. These digital signals are DCLK, HSYNC, VSYNC, R7~R0, G7~G0, B7~B0. If the digital interface is in the level of 3.3V, please short the power pin, VDD and VDDIO, to 3.3V. In other words, no matter the voltage level of VDDIO is 1.65V or 3.5V, the voltage level of VDD needs to be kept around 3.3V.

2.2 Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	I_L	---	20	22	mA	single seral
LED Voltage	V_L	---	12.8	---	V	single seral

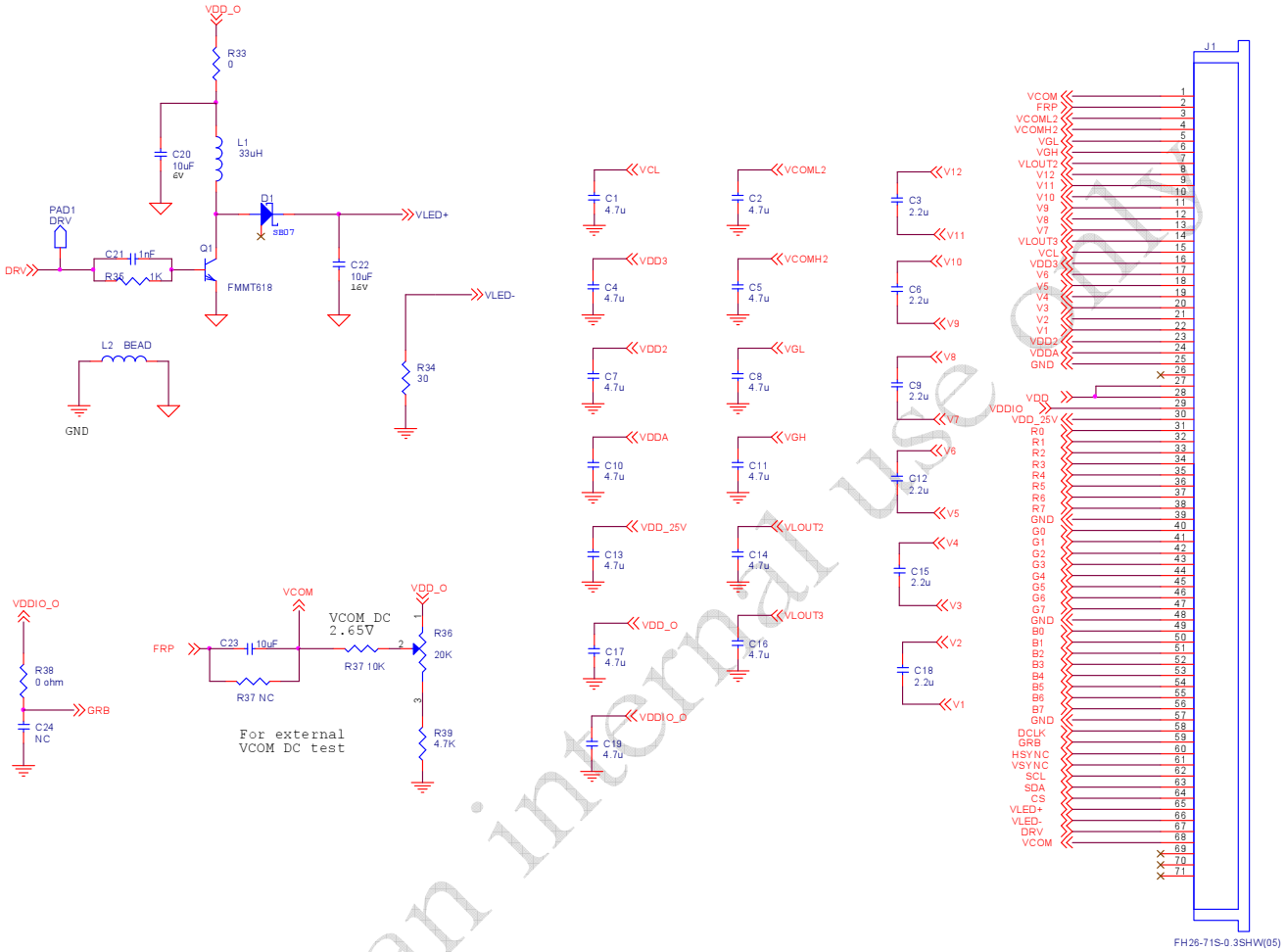
Note 2 :Define “LED Lifetime”: brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25℃ and LED current = 20mA.

Note 3: If it uses larger LED current I_L more than 20mA, it maybe decreases the LED lifetime.

2.3 Suggested Application Circuit

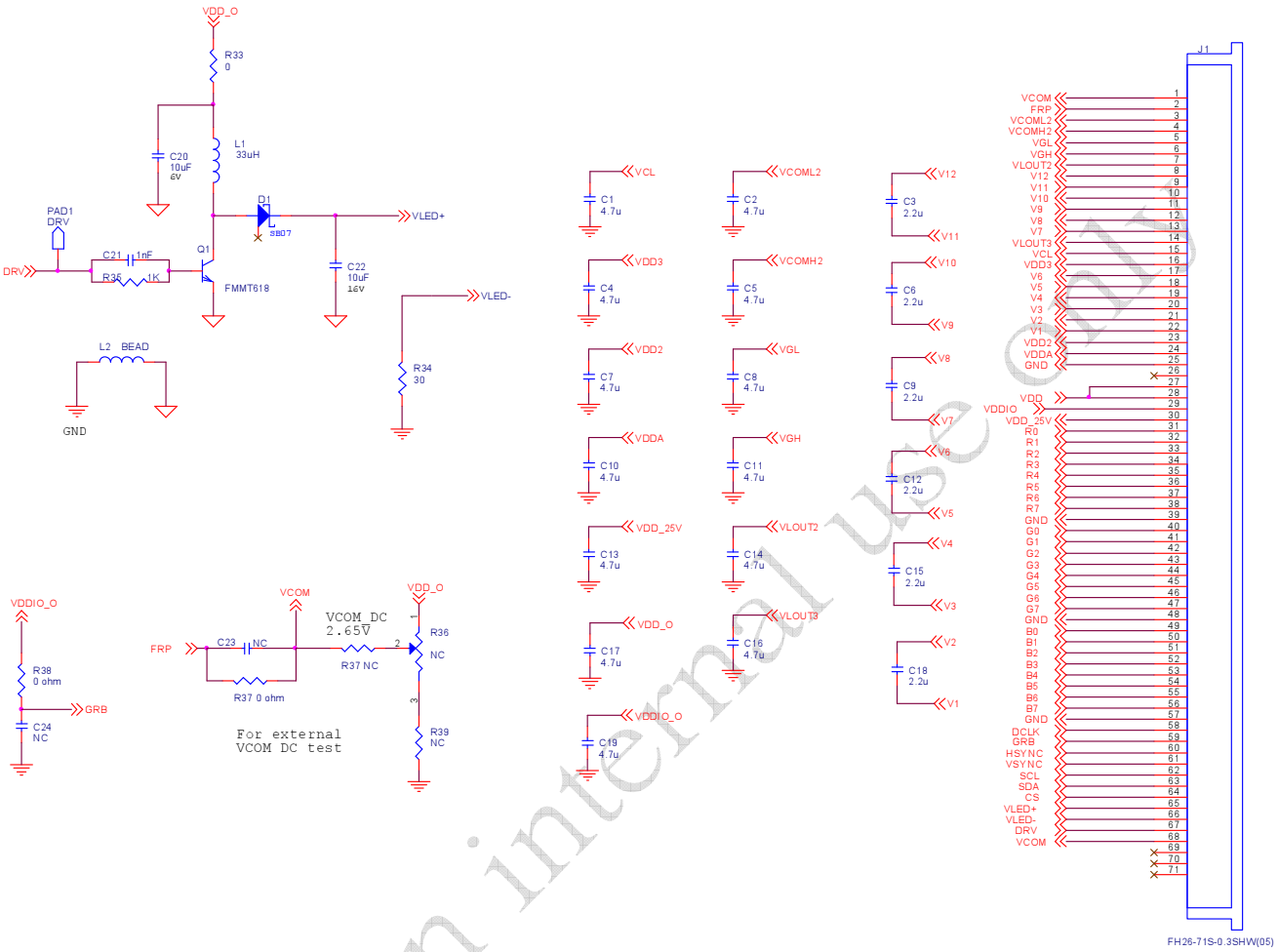
2.3.1 Suggested Application Circuit

(VCOM DC adjusted by variable resistance)



2.3.2 Suggested Application Circuit

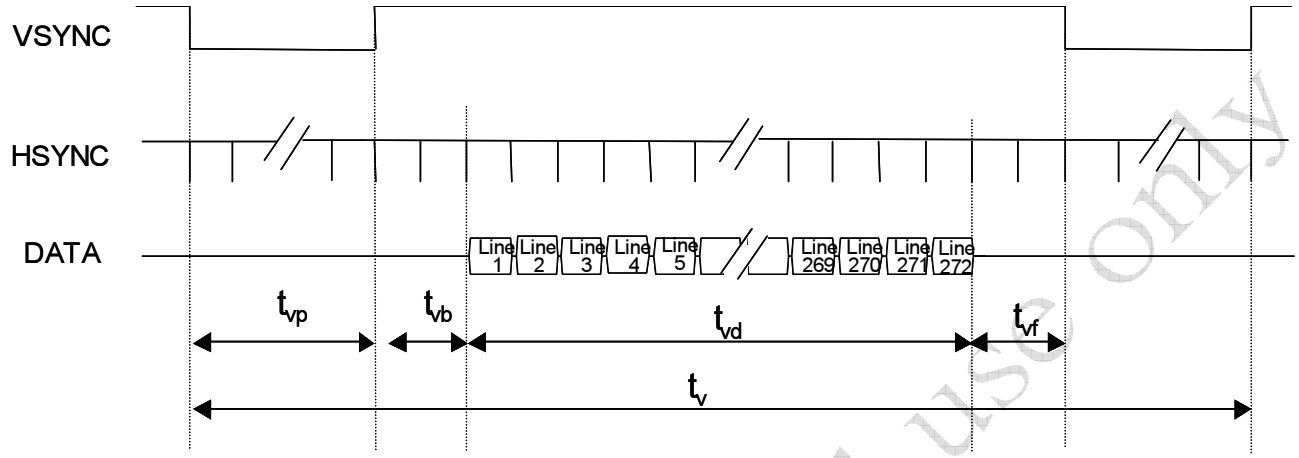
(VCOM DC adjusted by serial control interface)



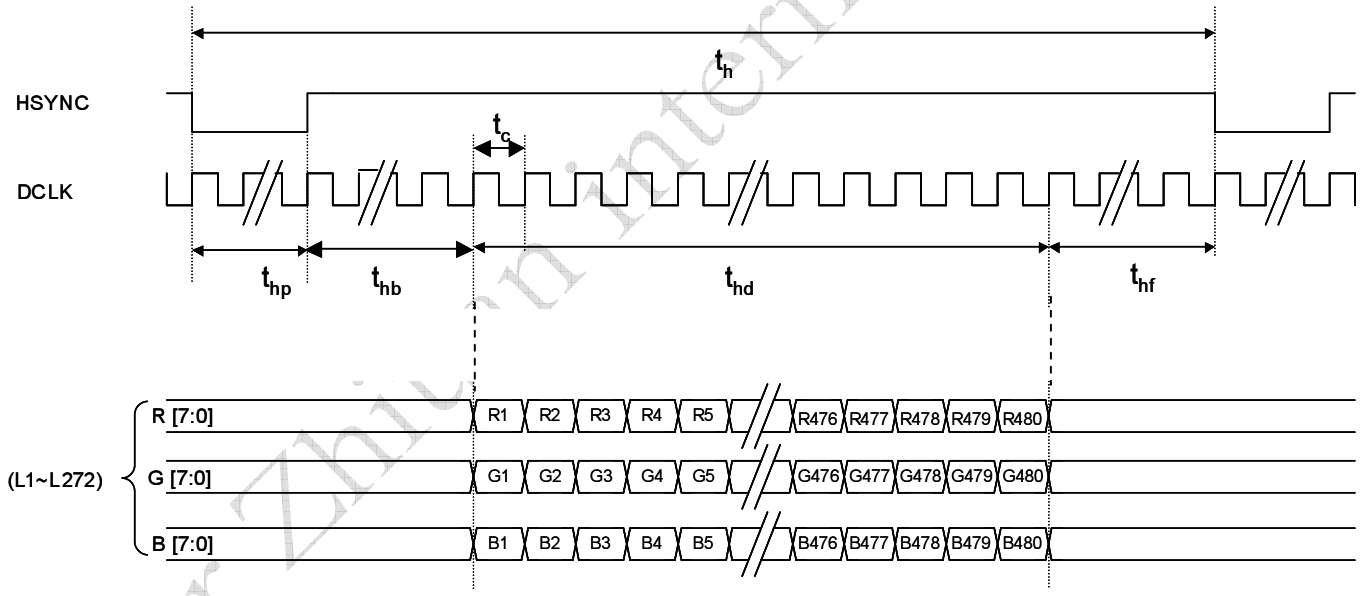
2.4 AC Timing

2.4.1 Timing Diagram

2.4.1.1 Vertical Timing of Input



2.4.1.2 Horizontal Timing of Input



2.4.2 Timing Condition

2.4.2.1. Timing Parameters

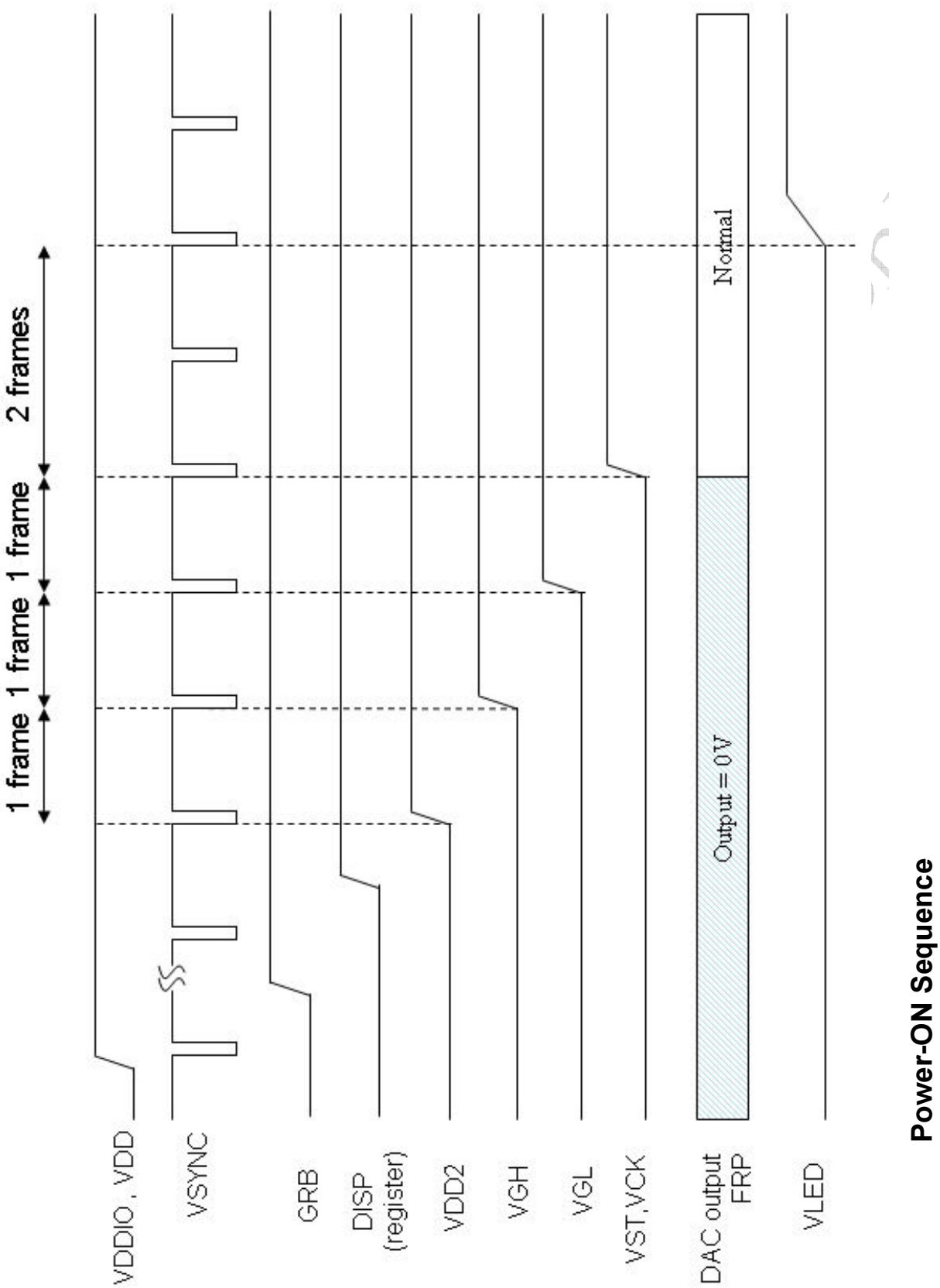
Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
Clock	Frequency	1/Tc	--	9.2	10	MHz	
	High Time	TCH	40	--	--	ns	
	Low Time	TCL	40	--	--	ns	
Data	Setup Time	TDS	10	--	--	ns	
	Hold Time	TDH	3	--	--	ns	
DE	Setup Time	TDES	10	--	--	ns	
	Hold Time	TDEH	3	--	--	ns	
Frame Frequency	Cycle	tv		16.7		ms	
1 Frame Scanning Time	Cycle	tv	--	288	--	H	
	Display Period	tvd	272			H	
	Front porch	tvf	2	4		H	
	Pulse width	tvp	1	10		H	
	Back porch	tvb	2	2		H	
1 Line Scanning Time	Cycle	th	494	533	545	DCLK	
	Display Period	thd	480			DCLK	
	Front porch	thf	2	8		DCLK	
	Pulse width	thp	1	41		DCLK	
	Back porch	thb	2	4		DCLK	

2.5 Power On/Off Sequence

The register DISP setting of standby mode disabling / enabling is used to control the build-in power on / off sequence.

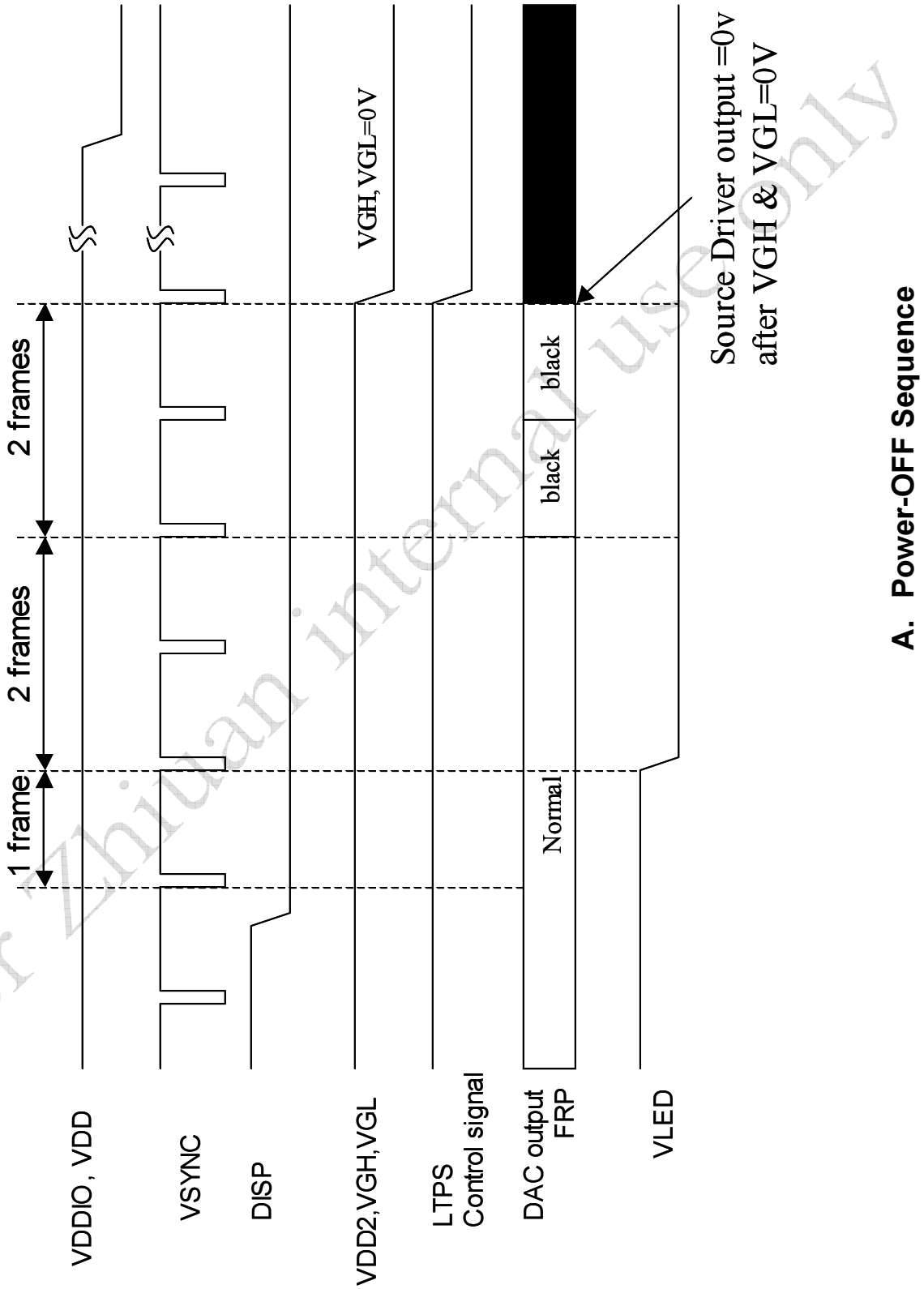
2.5.1 Power-On (Display ON; Standby Disabling)

The LCD driver is in default standby mode after VDD/VDDIO power-on, and set the register DISP to high to disable the standby mode is required for normal operation. When the standby mode is disabled, a build-in power on sequence is started. The driver IC analog power VDD2 is turned on first, and then the LCD positive and negative power supplies VGH/VGL are pumped, and followed by the LED power. Since we recommend using external LED driver, the backlight power should be provided at this time. Please refer to power on sequence for the detail timing.



Power-ON Sequence

3.5.2 Power-Off (Display Off; Standby Enabling)
When the register DISP is set to low to enable standby mode, a build-in power off sequence is started. Please also refer to the power off sequence for the detail timing.

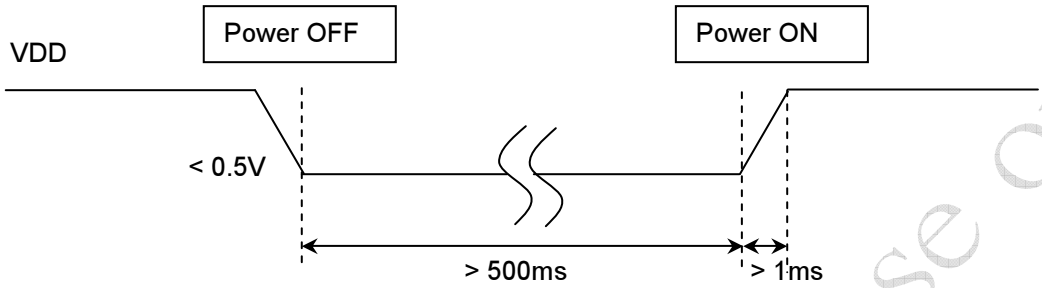


A. Power-OFF Sequence

2.5.3 Low-voltage Reset

Following figure suggests for low voltage reset function on power on sequence. When low voltage reset function enable, all the registers are loaded to default setting.

A. The rising time (10%-90%) of VDD nedds larger than 1ms.
B. After power off, VDD needs to be keep under 0.5V more than 500ms, then it can be power on again.



2.6 Serial Control Setting

2.6.1 Input timing specifications (refer to Fig. 1)

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Serial load input setup time	t_{s0}	50			ns	
Serial load input hold time	t_{h0}	50			ns	
Serial data input setup time	t_{s1}	50			ns	
Serial data input hold time	t_{h1}	50			ns	
SCL pulse width	t_{WL1}	50			ns	
	t_{WH1}	50			ns	
CS pulse width	t_{W2}	400			ns	

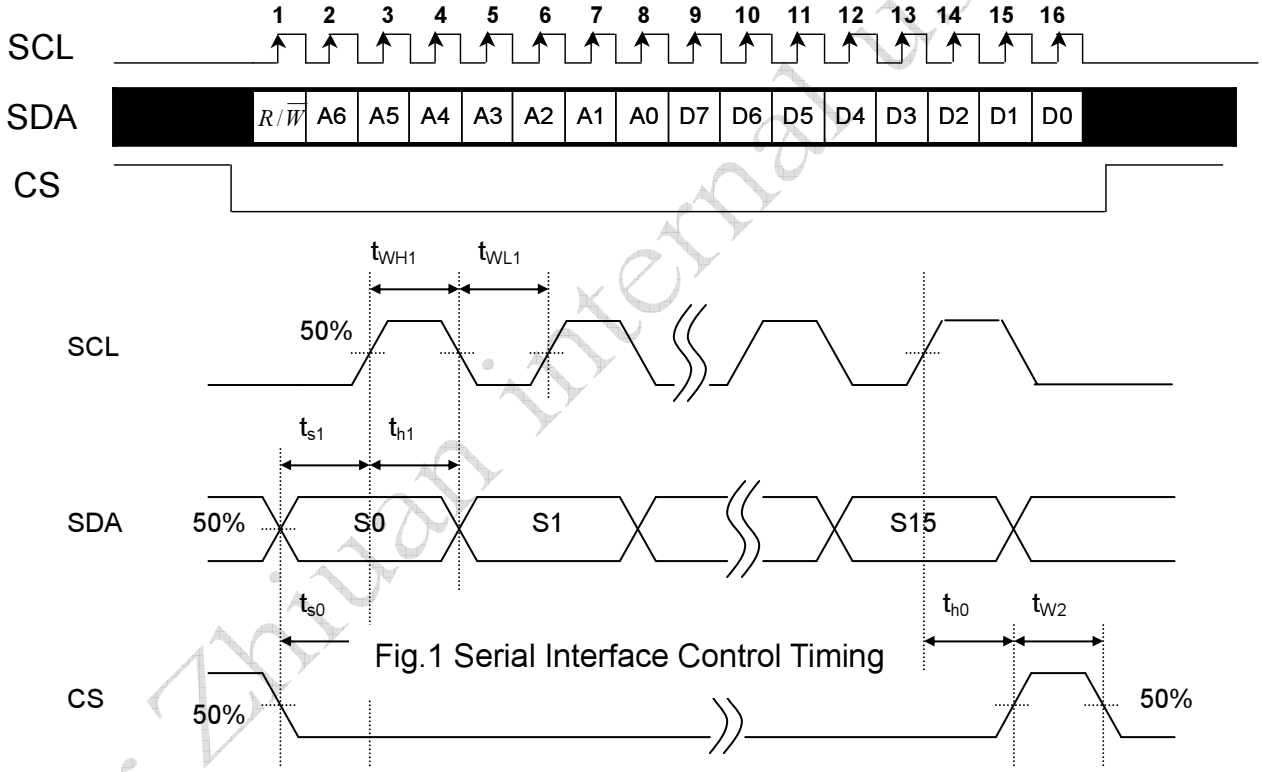


Fig.1 Serial Interface Control Timing

2.6.2 Serial setting table

No	Register Address								Register Data (Default Setting)							
	$R/\overline{W}$	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	X	VDIR(1)	HDIR(1)	0	VCOM_AC(0110)			
R1	0	0	0	0	0	0	0	1	0	VCOM_DC(40h)						
R2	0	0	0	0	0	0	1	0	CONTRAST(40h)							
R3	0	0	0	0	0	0	1	1	X	SUB-CONTRAST_R(40h)						
R4	0	0	0	0	0	1	0	0	X	SUB-CONTRAST_B(40h)						
R5	0	0	0	0	0	1	0	1	BRIGHTNESS(40h)							
R6	0	0	0	0	0	1	1	0	X	SUB-BRIGHTNESS_R(40h)						
R7	0	0	0	0	0	1	1	1	X	SUB-BRIGHTNESS_B(40h)						
R8	0	0	0	0	1	0	0	0	HSYNC BLANKING(2Bh)							
R9	0	0	0	0	1	0	0	1	Vdpol(1)	Hdpol(1)	VSYNC BLANKING(0Ch)					
R10	0	0	0	0	1	0	1	0	1	DCLKpol(1)	0	0	1	0	1	0
R11	0	0	0	0	1	0	1	1	LED_CURRENT(00)		BL_DRV(00)		DRV_FREQ(00)		PFM_DUTY(10)	
R12	0	0	0	0	1	1	0	0	LED_ON_CYCLE(0111)				LED_ON_RATIO(1111)			
R13	0	0	0	0	1	1	0	1	X	1	X	X	GRB(1)	1	SHDB1(0)	DISP(0)
R64	0	1	0	0	0	0	0	0	1	1	0 X		00		00	
R66	0	1	0	0	0	0	1	0	X	43h						
R68	0	1	0	0	0	1	0	0	X	28h						

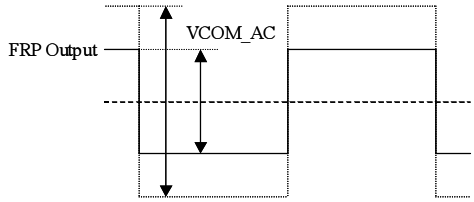
Note: X is “don’t care”. “ ” could be registered by customer.

Register R0

Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	00h	X	VDIR	HDIR	0	VCOM_AC			

VCOM_AC : Common voltage AC level selection (deviation ±0.1V)

VCOM_AC				Voltage (V)
D3	D2	D1	D0	
0	0	0	0	5.8
0	0	0	1	5.9
0	0	1	0	6.0
0	0	1	1	6.1
0	1	0	0	6.2
0	1	0	1	6.3
0	1	1	0	6.4 (Default)
0	1	1	1	6.5
1	0	0	0	6.6
1	0	0	1	6.7
1	0	1	0	6.8
1	0	1	1	6.9
1	1	X	X	7.0



Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	00h	X	VDIR	HDIR	0	VCOM_AC			

HDIR : Horizontal shift direction setting

HDIR	Description
0	Shift from right to left, ex : Last data = Y1←Y2…Y1439←Y1440 = First data
1	Shift from left to right, ex : First data = Y1→Y2…Y1439→Y1440 = Last data (Default)

VDIR : Vertical shift direction setting

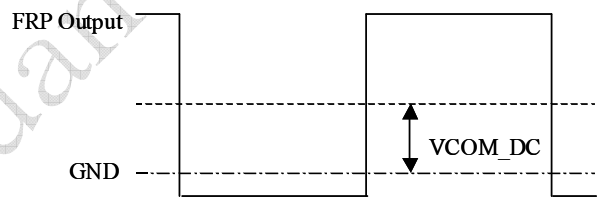
VDIR	Description
0	Shift from down to up, ex : Last line = L1←L2…L271←L272 = First line
1	Shift from up to down, ex : First line = L1→L2…L271→L272 = Last line (Default)

Register R1

Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R1	0	01h	0	VCOM_DC						

VCOM_DC : Common voltage DC level selection

VCOM_DC D6~D0	Voltage (V)
00h	2
:	:
40h	2.605 (Default)
:	:
7Fh	3.2



Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R2	0	02h	CONTRAST							

CONTRAST : RGB contrast level setting, the gain changes (1/64) / bit

CONTRAST D7~D0	Gain
00h	0
40h	1 (Default)
FFh	3.984

Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R3	0	03h	X	SUB-CONTRAST_R						

Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R4	0	04h	X	SUB-CONTRAST_B						

SUB-CONTRAST_RB : RB sub-contrast level setting, the gain changes (1/256) / bit

SUB-CONTRAST D6~D0	Gain
00h	0.75
40h	1 (Default)
7Fh	1.246

Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R5	0	05h	BRIGHTNESS							

BRIGHTNESS : RGB bright level setting, setting accuracy : 1 step / bit

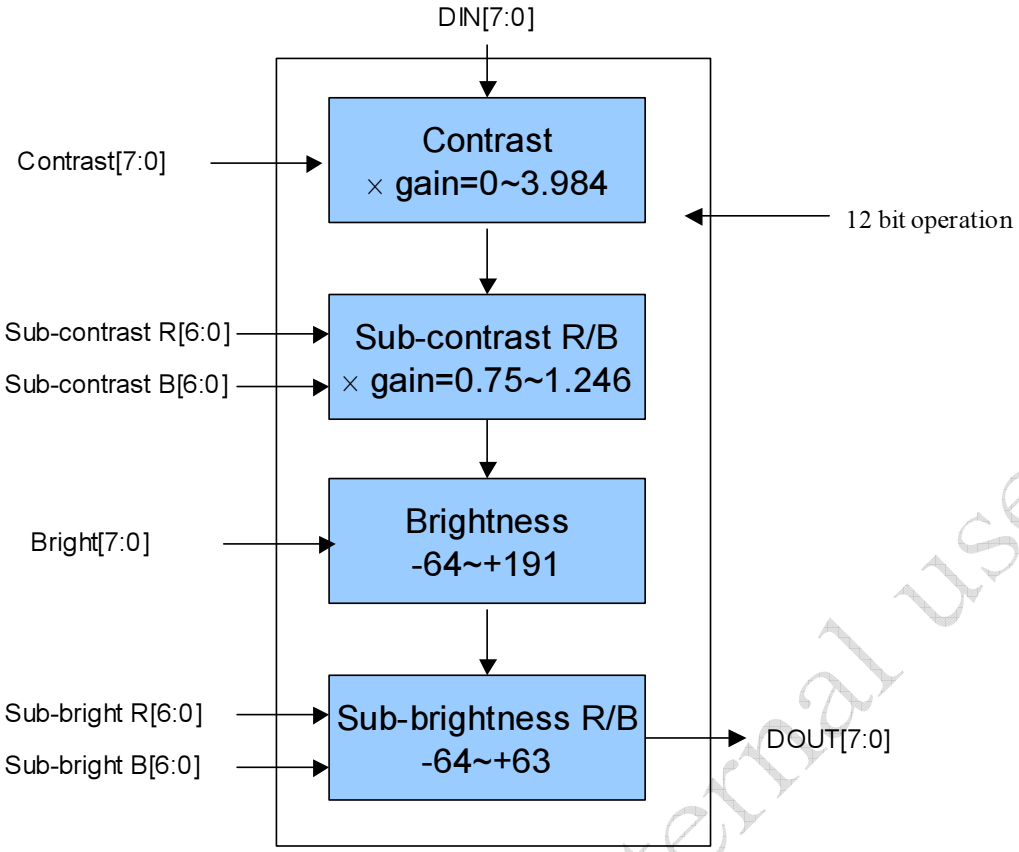
BRIGHTNESS D7~D0	Setting
00h	Dark (-64)
40h	Center (0) (Default)
FFh	Bright (+191)

Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R6	0	06h	X	SUB-BRIGHTNESS_R						

Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R7	0	07h	X	SUB-BRIGHTNESS_B						

SUB-BRIGHTNESS_RB : RB sub-brightness level setting, setting accuracy : 1 step / bit

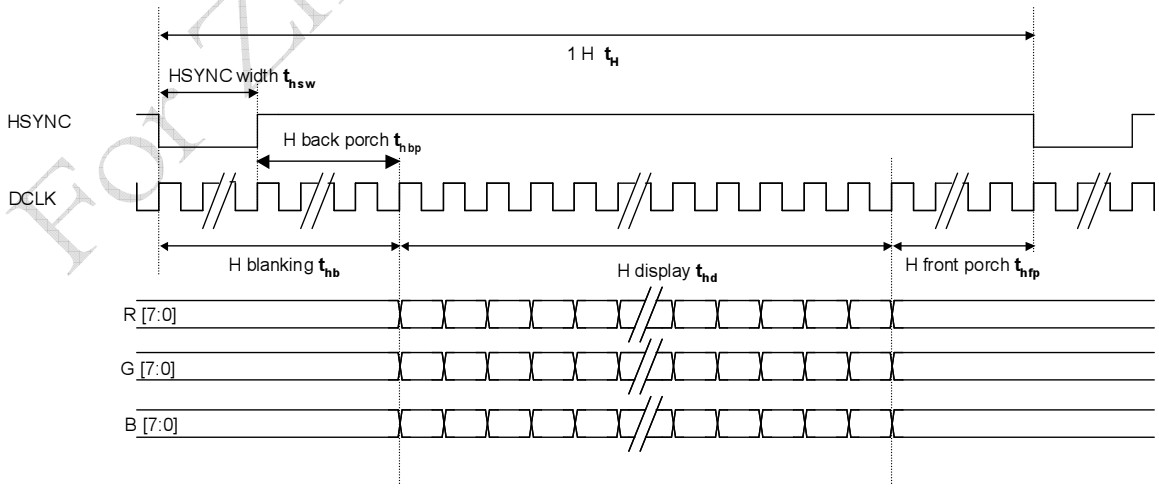
SUB-BRIGHTNESS D6~D0	Setting
00h	Dark (-64)
40h	Center (0) (Default)
7Fh	Bright (+63)



Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R8	0	08h	HSYNC BLANKING							

HSYNC BLANKING : Horizontal blanking setting

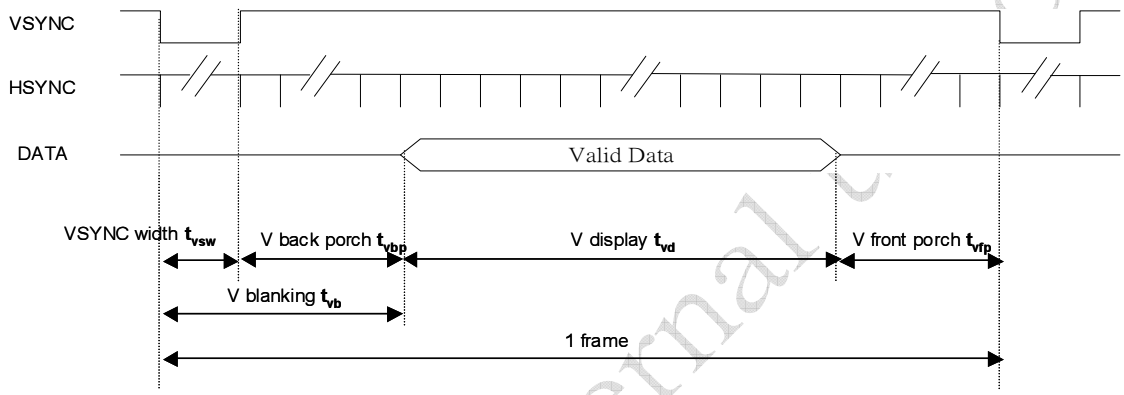
HSYNC BLANKING D7~D0	DCLK
00h	0
2Bh	43 (Default)
FFh	255



Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R9	0	09h	VDPOL	HDPOL	VSYNC BLANKING					

VSYNC BLANKING : Vertical blanking setting

VSYNC BLANKING	H
D5~D0	
00h	0
0Ch	12 (Default)
3Fh	63



Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R9	0	09h	VDPOL	HDPOL	VSYNC BLANKING					

HDPOL : HSYNC polarity selection

HDPOL	Function
0	Positive polarity
1	Negative polarity (Default)

VDPOL : VSYNC polarity selection

VDPOL	Function
0	Positive polarity
1	Negative polarity (Default)

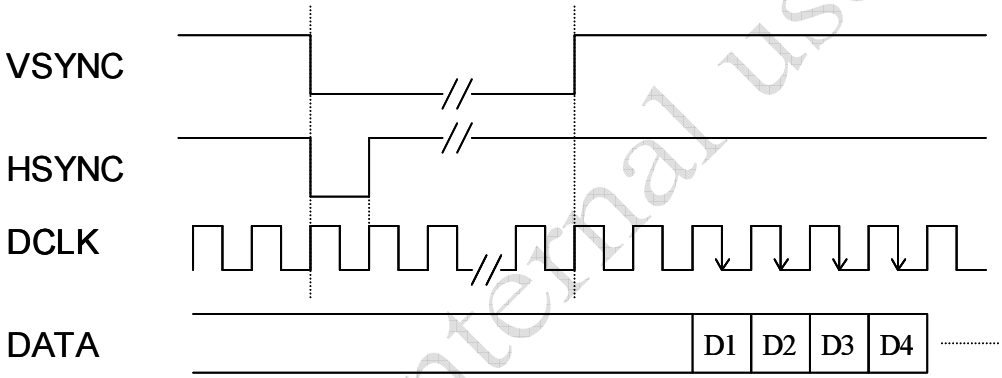
Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R10	0	0Ah	1	DCLKPOL	0	0	1	0	1	0

DCLKPOL : DCLK polarity selection

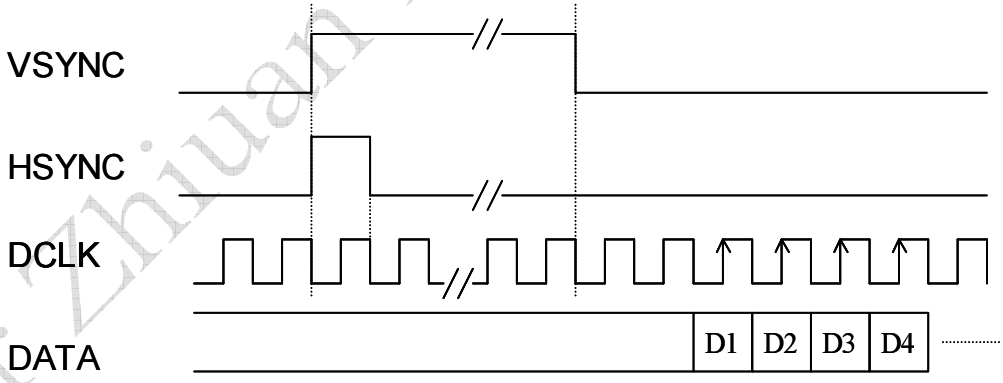
DCLKPOL	Description
0	**Positive polarity**
1	**Negative polarity (Default)**

When the command is sent to ASIC, it will be executed immediately.

• HDPOL=1, VDPOL=1, CLKPOL=1



• HDPOL=0, VDPOL=0, CLKPOL=0



Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R11	0	0Bh	LED_CURRENT		BL_DRV		DRV_FREQ		PFM_DUTY	

PFM_DUTY : PFM duty cycle selection for back light power converter

PFM_DUTY		PFM duty cycle	Note
D1	D0		
0	0	50 %	16/32
0	1	60 %	19/32
1	0	65 % (Default)	21/32
1	1	70 %	22/32

DRV_FREQ : DRV signal frequency setting

DRV_FREQ		Frequency
D3	D2	
0	0	DCLK / 32 (Default)
0	1	DCLK / 64
1	0	DCLK / 128
1	1	DCLK / 256

Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R11	0	0Bh	LED_CURRENT		BL_DRV		DRV_FREQ		PFM_DUTY	

BL_DRV : Backlight driving capability setting

BL_DRV		Capability
D5	D4	
0	0	Normal capability (Default)
0	1	4 times the Normal capability
1	0	8 times the Normal capability
1	1	12 times the Normal capability

LED_CURRENT : adjust LED current

LED_CURRENT		DC-DC Feedback Voltage
D7	D6	
0	0	0.6 V (default, 20mA)
0	1	0.75V (25mA)
1	0	0.45V (15mA)
1	1	0.3V (10mA)

Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R12	0	0Ch	LED_ON_CYCLE				LED_ON_RATIO			

LED_ON_CYCLE : Set the cycle of enable signal.

LED_ON_CYCLE				Value
D7	D6	D5	D4	
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8 (Default)
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

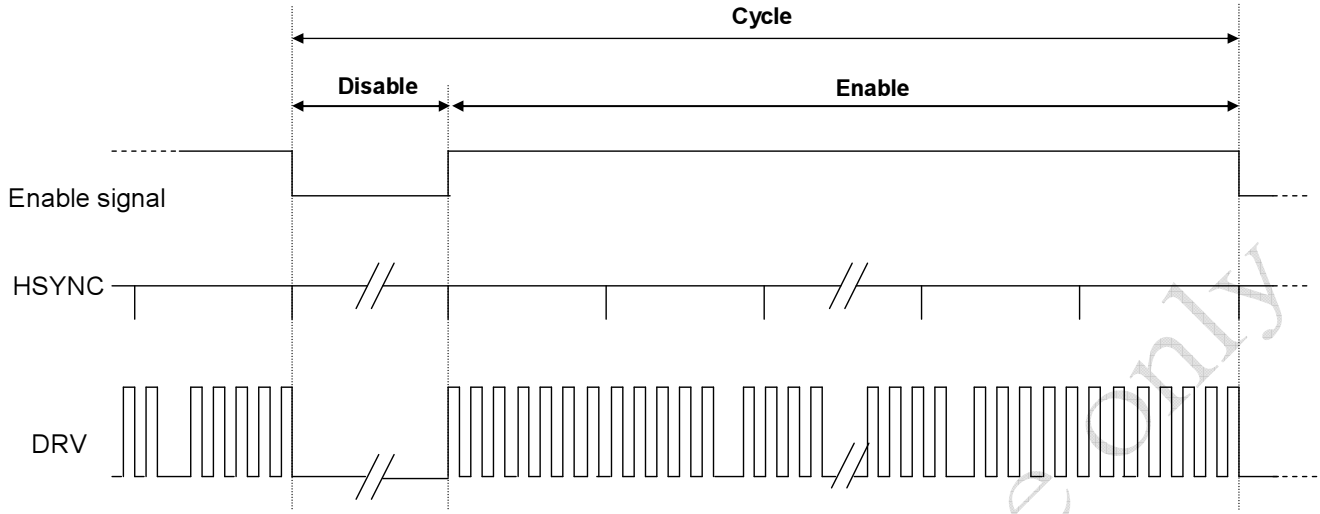
Need to keep the frequency of the enable signal more than 120Hz to prevent the backlight twinkle visible.
(Please refer to the example in the following page.)

Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R12	0	0Ch	LED_ON_CYCLE				LED_ON_RATIO			

LED_ON_RATIO : Set the active ratio of enable signal, and we can use it to decrease the brightness of the LEDs.

LED_ON_RATIO				Value
D3	D2	D1	D0	
0	0	0	0	1 / 16
0	0	0	1	2 / 16
0	0	1	0	3 / 16
0	0	1	1	4 / 16
0	1	0	0	5 / 16
0	1	0	1	6 / 16
0	1	1	0	7 / 16
0	1	1	1	8 / 16
1	0	0	0	9 / 16
1	0	0	1	10 / 16
1	0	1	0	11 / 16
1	0	1	1	12 / 16
1	1	0	0	13 / 16
1	1	0	1	14 / 16
1	1	1	0	15 / 16
1	1	1	1	16 / 16 (Default)

The advantage of this function is that it has 16–step to fine tune the brightness. If you would not like to decrease the brightness of the backlight, please set to “1111”.
(Please refer to the example in the following page.)



$16 * LED\_ON\_CYCLE = LED\_ON\_CYCLE * (LED\_ON\_RATIO * 16) + LED\_ON\_CYCLE * (16 - LED\_ON\_RATIO * 16)$

(Cycle) **(Enable)** **(Disable)** Unit : HSYNC

for example:
LED_ON_RATIO is **"1001"**, and LED_ON_CYCLE is **"0111"**, then:
Cycle = 16 * **8** = 128(HSYNC)
Enable = **8** * ((**10/16**) * 16) = 80(HSYNC)
Disable = **8** * (16-(**10/16**) * 16) = 48(HSYNC) ➔62.5% on

Register	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R13	0	0Dh	X	1	X	X	GRB	1	SHDB1	DISP

DISP : Standby (power saving) mode setting

DISP	Description
0	**Standby (Display OFF); timing control, DAC, and DC/DC converter are off, and register data should be kept (Default)**
1	**Normal operation (Display ON), with power on/off sequence**

Note : In standby mode, Source Driver output =0V, VGH =0V, VGL =0V, FRP =0V

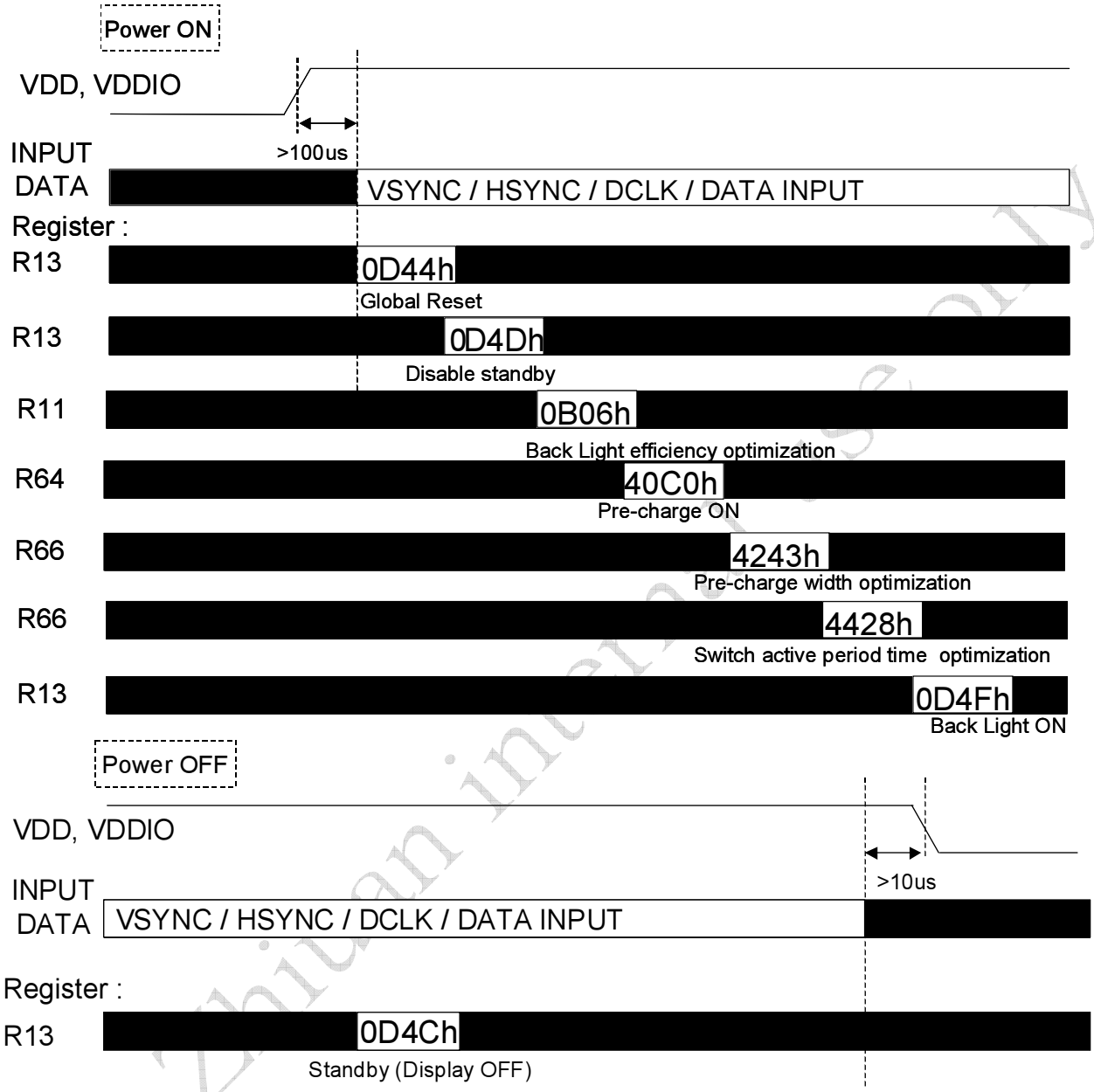
SHDB1 : Shut down for back light power converter

SHDB1	Description
0	**The back light power converter is off (Default)**
1	**The back light power converter is controlled by STB's power on/off sequence**

GRB : Register reset setting

GRB	Description
0	**Reset all registers to default value**
1	**Normal operation (Default)**

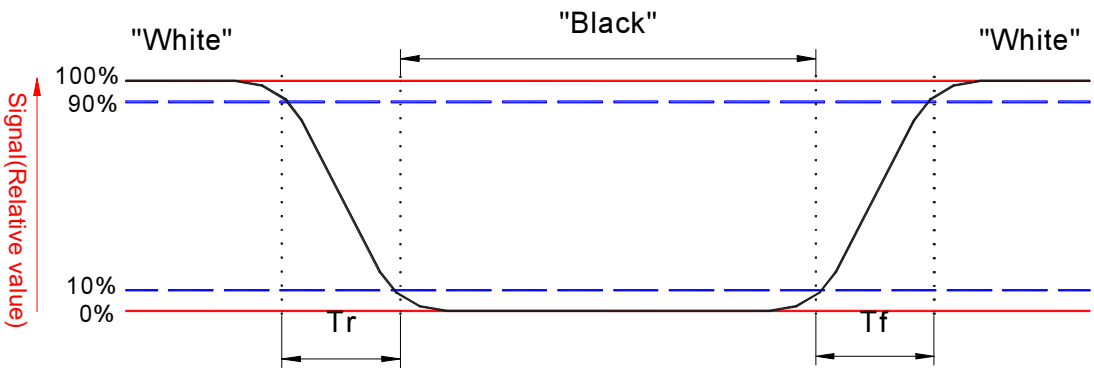
2.6.3 Suggested Serial Command Settings:



C. Optical Specification (Note1, Note 2 and Note 3)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall		 Tr Tf	θ =0°	 - -	 15 10	 25 20	 ms ms	Note 4
Contrast ratio		CR	At optimized viewing angle	400	500	-		Note 6, 7
Viewing Angle Top Bottom Left Right			CR≧10	 70 70 70 70	 80 80 80 80	 - - - 	 deg.	Note 8
Brightness		Y_L	θ =0°	300	350	-	cd/m^2	Note 9
NTSC				-	60	-	%	
Chromaticity	White	x	θ=0°	0.25	0.30	0.35		
		y	θ=0°	0.28	0.33	0.38		
	Red	x	θ=0°	0.56	0.61	0.66		
		y	θ=0°	0.27	0.32	0.37		
	Green	x	θ=0°	0.29	0.34	0.39		
		y	θ=0°	0.55	0.60	0.65		
	Blue	x	θ=0°	0.10	0.15	0.20		
		y	θ=0°	0.03	0.08	0.13		

Note 1. Ambient temperature =25℃.
Note 2. To be measured in the dark room.
Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-5A, after 10 minutes operation.
Note 4. Definition of response time:
The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.
The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White $Vi=V_{i50} \mp 1.5V$

Black $Vi=V_{i50} \pm 2.0V$

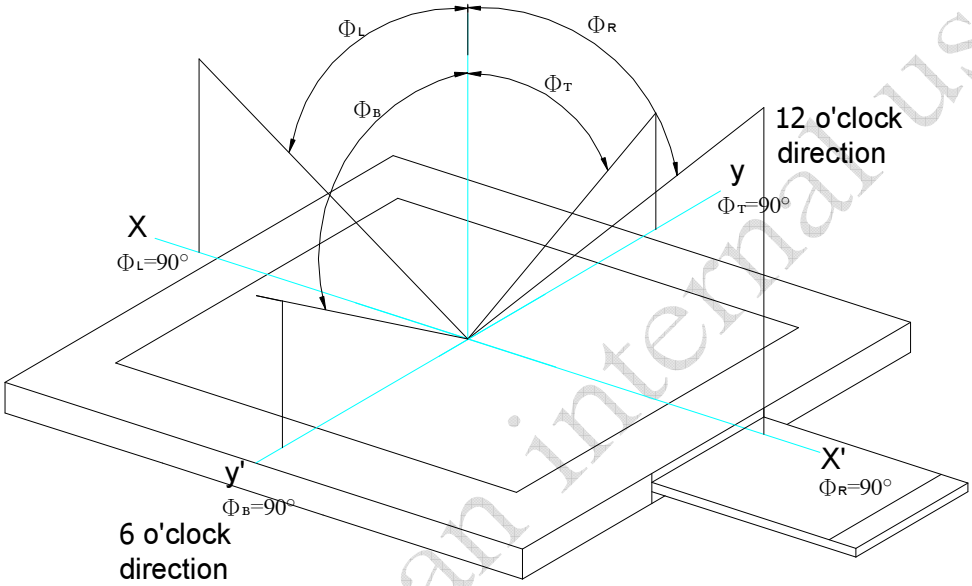
"±" Means that the analog input signal swings in phase with COM signal.

"∓" Means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

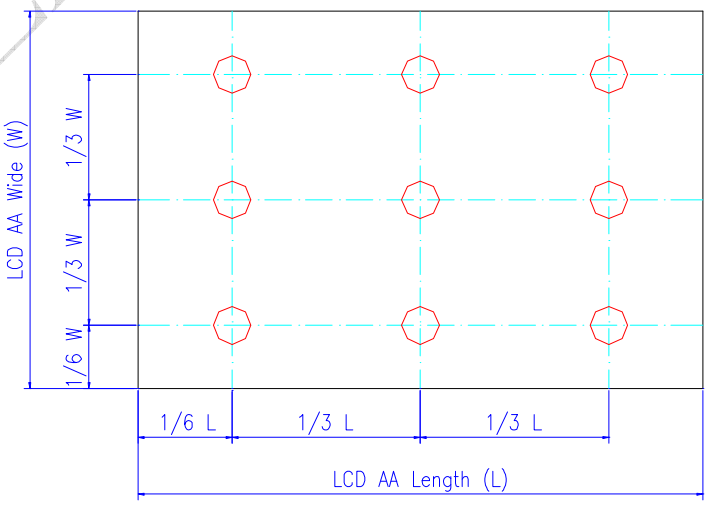
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle, Φ, Refer to figure as below.



Note 8. Measured at the center area of the panel in gray level 255

Note 9. Luminance Uniformity of these 9 points is defined as below:

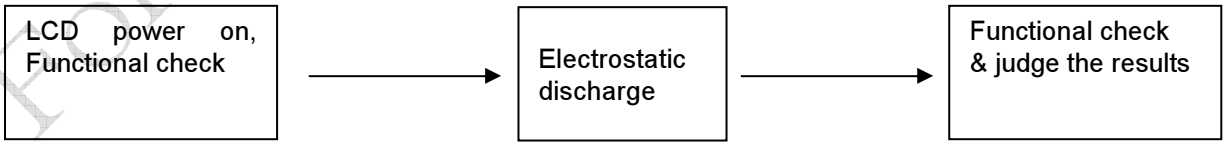


$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

D. Reliability Test Items

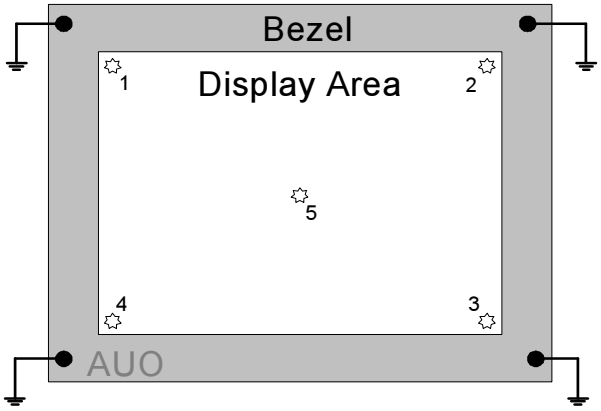
No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70□ 240Hrs	
2	Low Temperature Storage	Ta= -25□ 240Hrs	
3	High Ttemperature Operation	Tp= 60□ 240Hrs	
4	Low Temperature Operation	Ta= 0□ 240Hrs	
5	High Temperature & High Humidity	Tp= 60□. 90% RH 240Hrs	Operation
6	Heat Shock	-25□~80□, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	Note 2,3
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1. Ta: Ambient temperature.
Note 2. ESD Testing Flow as the below,



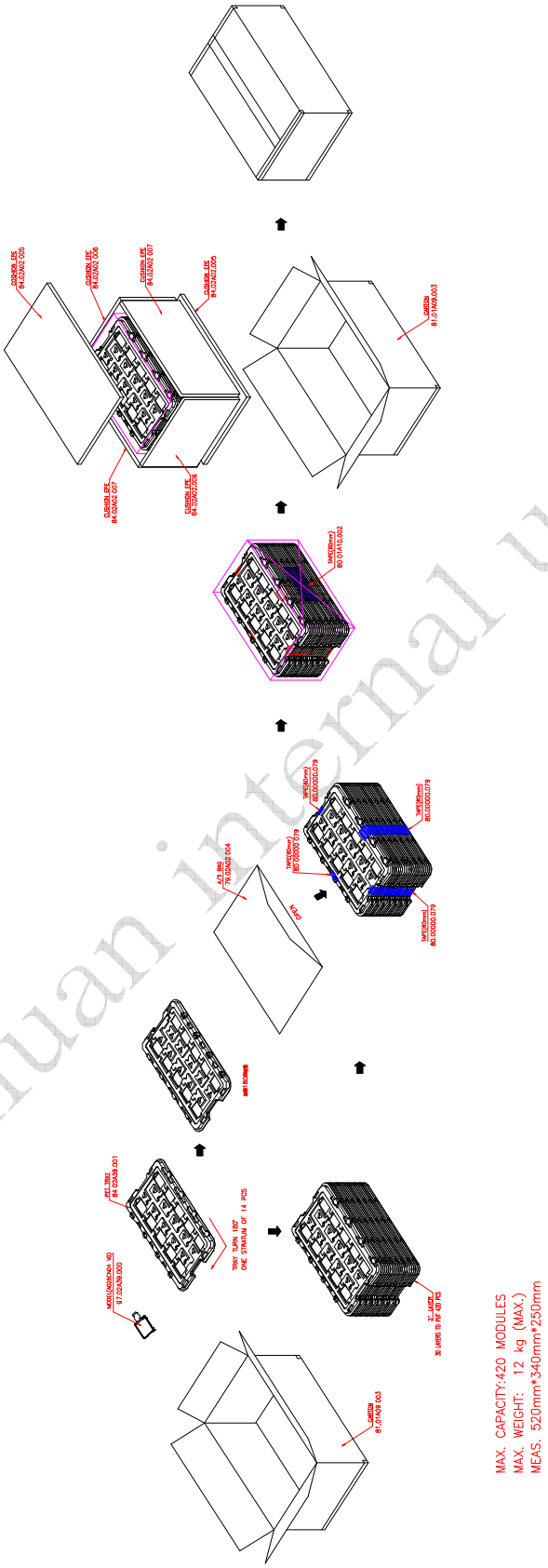
Note 3. ESD testing method.
1. Ambient: 24~26□, 56~65%RH
2. Instruments:NoisekenESS-2000,
3. Operation System: “CX40FL-B” and adapter “A030FL01 V3”
4. Test Mode: Operating mode, test pattern: colorbar+8Gray scale
5. Test Method:
   a. Contact Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
   b. Air Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point

6. Test point:



7. The metal casing is connected to power supply ground (0V) at four corners.
8. All register commands are repeating transfer.

E. Packing Form



F. Outline dimension