Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications
( ) Final Specifications

Module	**10.1”(10.07”) WXGA 16:10 Color TFT-LCD with LED Backlight design**
Model Name	B101EW05 V110 (HW: 0A)
Note ECOlor	***LED Backlight with driving circuit design*** ✓ ***Color Management (Virtual and Rich Color Solution)*** ✓ ***Dynamic Contrast Ratio (Power Saving Solution)***

Customer	**Date**
Checked & Approved by	**Date**
Note: This Specification is subject to change without notice.	

Approved by	**Date**
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Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2011/01/25	All	First Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breakdown.

2. General Description

B101EW05 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 WXGA, 1280(H) x800(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B101EW05 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	255.85 (10.07W")			
Active Area	[mm]	216.96(H) x 135.6(V)			
Pixels H x V		1280 x 3(RGB) x 800			
Pixel Pitch	[mm]	0.1695 X 0.1695			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (I_{LED}=21mA) **(Note: ILED is LED current)**	[cd/m^2]	350 typ. (5 points average) 297 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		1300 typ, 1000 min.			
Response Time	[ms]	25 typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.4 max. (Include Logic and BLU power)			
Weight	[Grams]	180max			
Physical Size **without bracket**	[mm]		Min.	Typ.	Max.
		Length	228.96	229.46	229.95
		Width	148.6	149.1	149.6
		Thickness	---	---	5.2
Electrical Interface		1 channel LVDS			

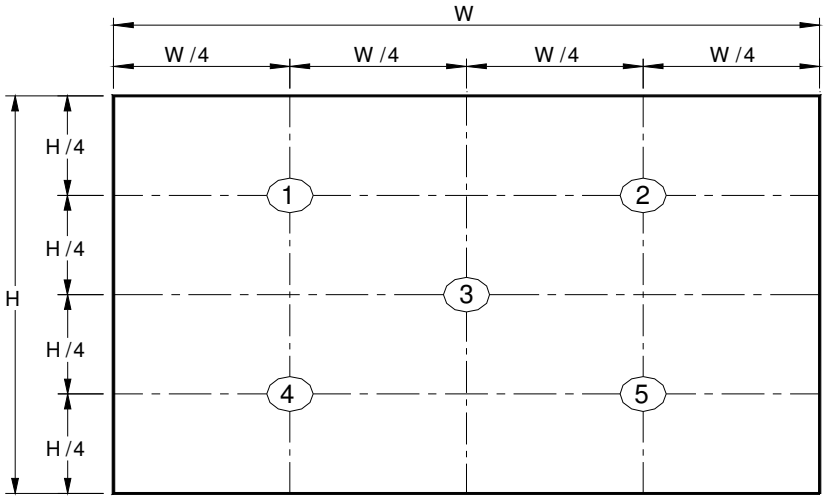
Glass Thickness	[mm]	0.3
Surface Treatment		Anti-Reflection≦1.5%, Hardness 3H
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

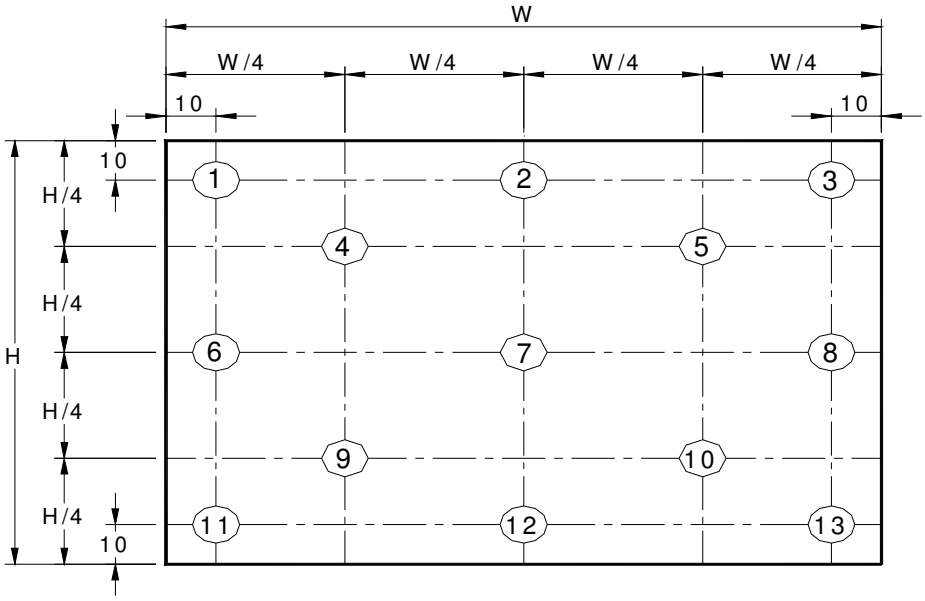
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=21mA			5 points average	297	350	---	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10	80	85	---	degree	4, 9
		θ_L	(Left)	80	85	---		
		ψ_H	Vertical (Upper) CR = 10	80	85	---		
		ψ_L	(Lower)	80	85	---		
Luminance Uniformity		δ_{5P}	5 Points	---	---	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	---	---	1.50		2, 3, 4
Contrast Ratio		CR		1000	1300	-		4, 6
Cross talk		%		---	---	4		4, 7
Response Time		T_{RT}	Rising + Falling	---	25	35	msec	4, 8
Color / Chromaticity Coordinates	Red	Rx	CIE 1931	0.549	0.579	0.609		4
		Ry		0.308	0.338	0.368		
	Green	Gx		0.295	0.325	0.355		
		Gy		0.530	0.560	0.590		
	Blue	Bx		0.132	0.152	0.182		
		By		0.095	0.125	0.155		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	45	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



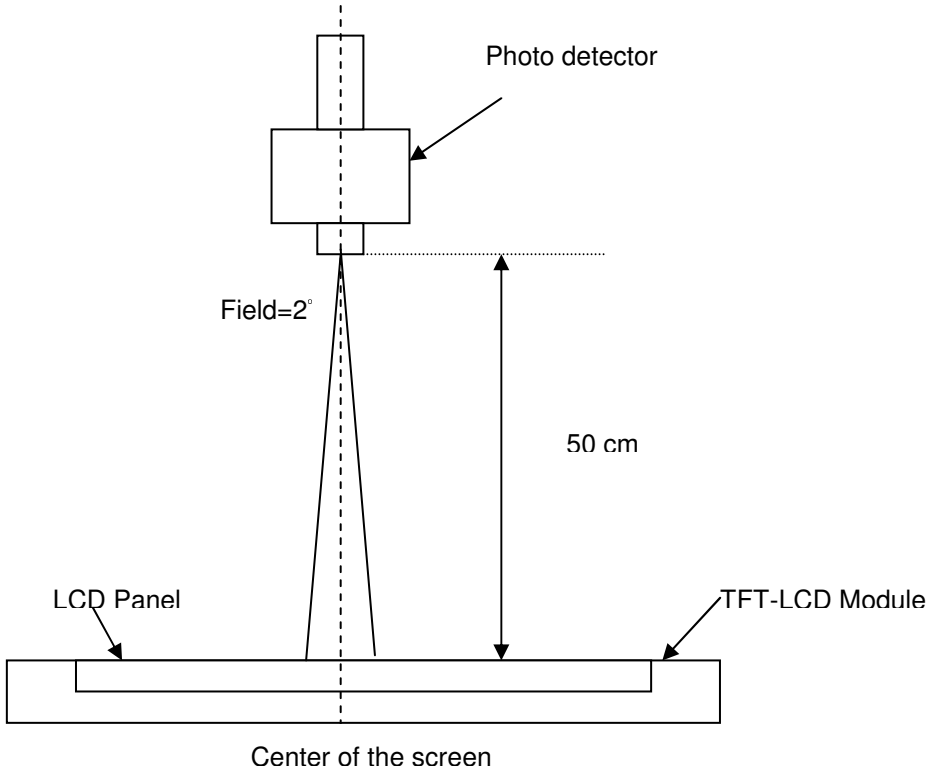
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

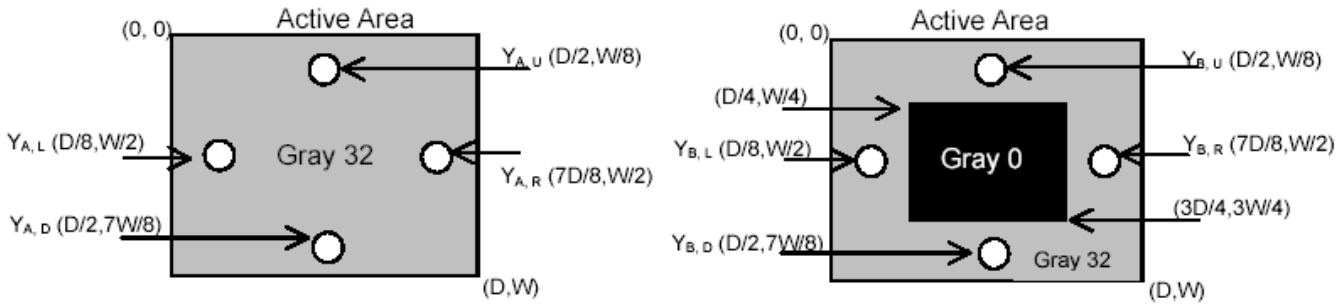
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

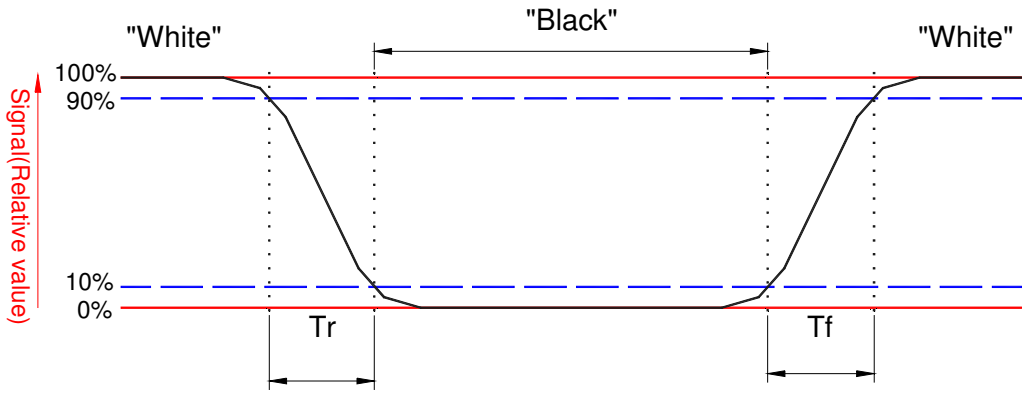
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



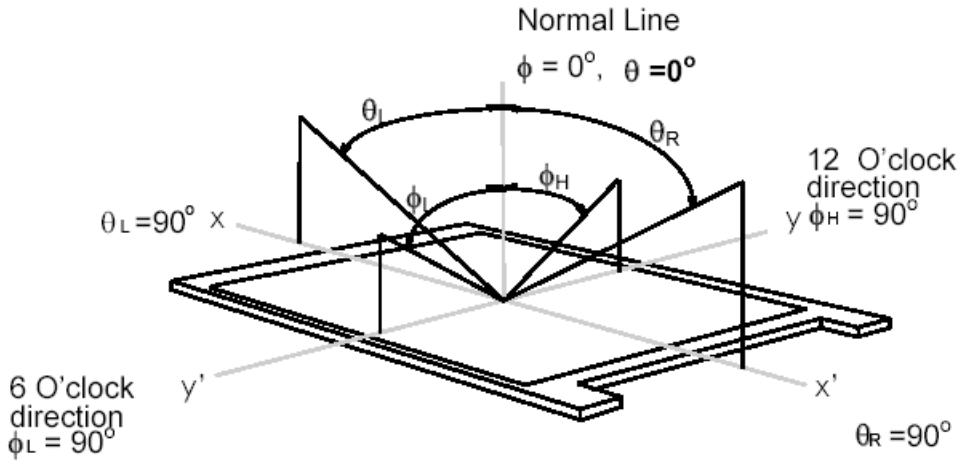
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



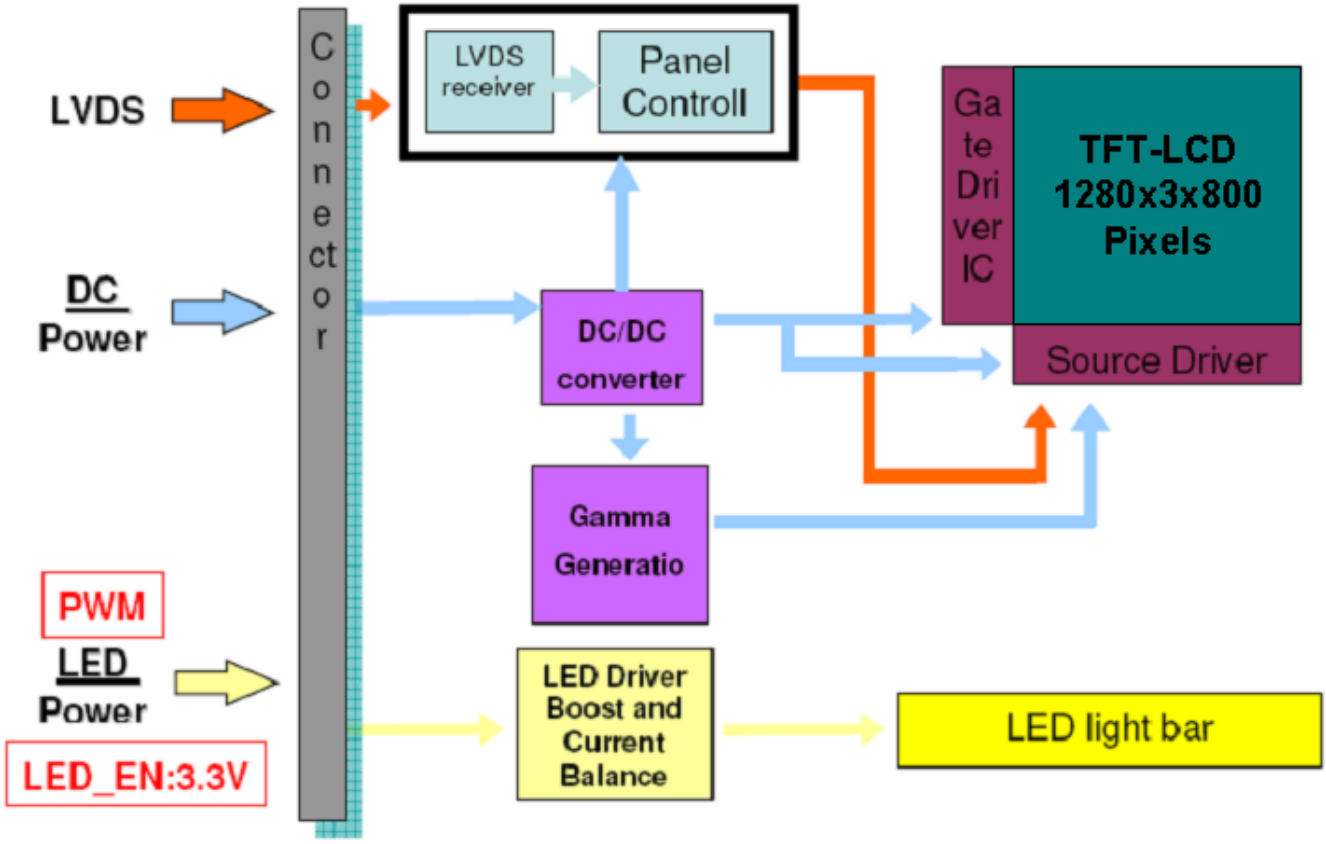
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 40 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

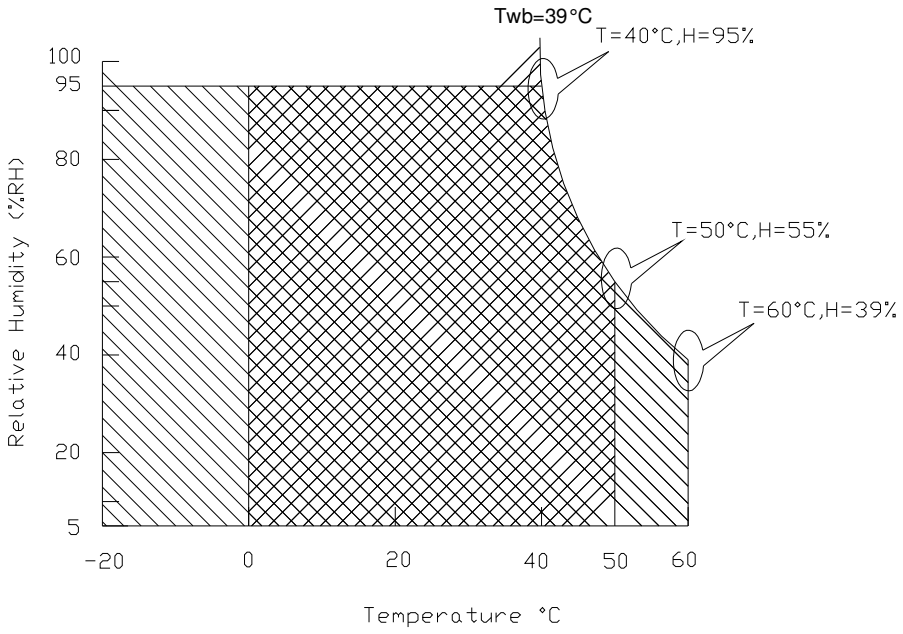
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

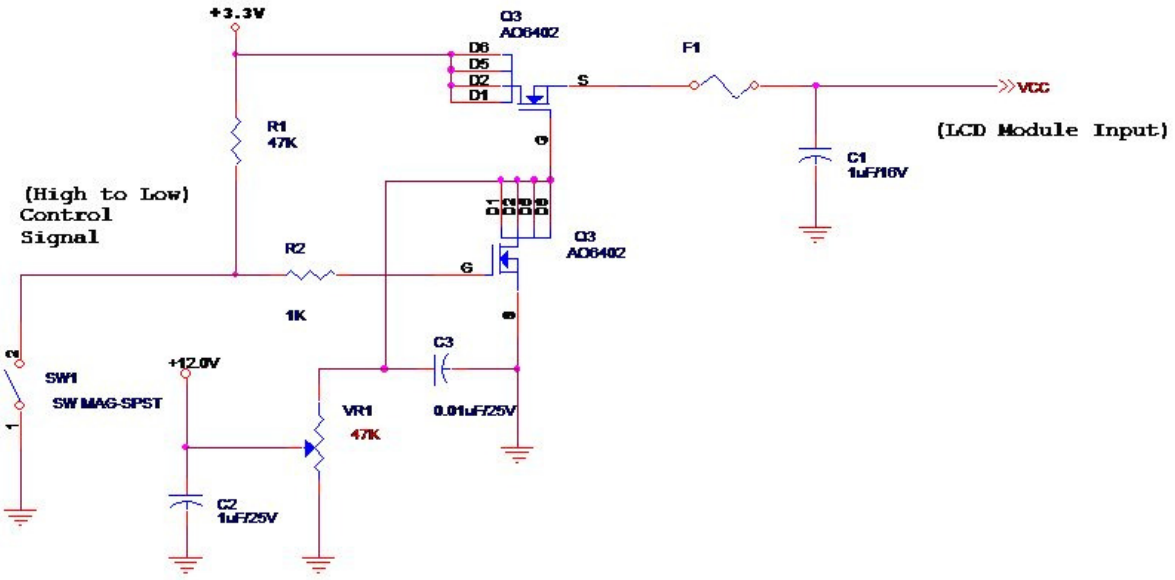
Input power specifications are as follows;

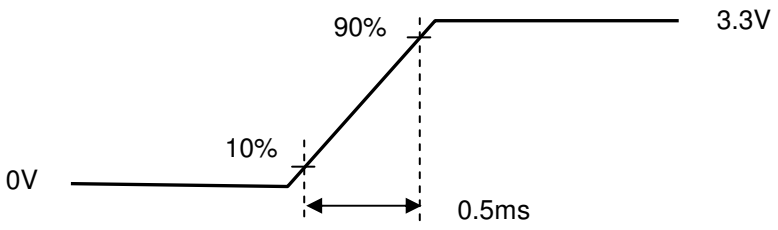
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	_	-	0.7	[Watt]	Note 1
IDD	IDD Current	_	_	212	[mA]	Note 1
IRush	Inrush Current	_	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2 : Measure Condition





Vin rising time

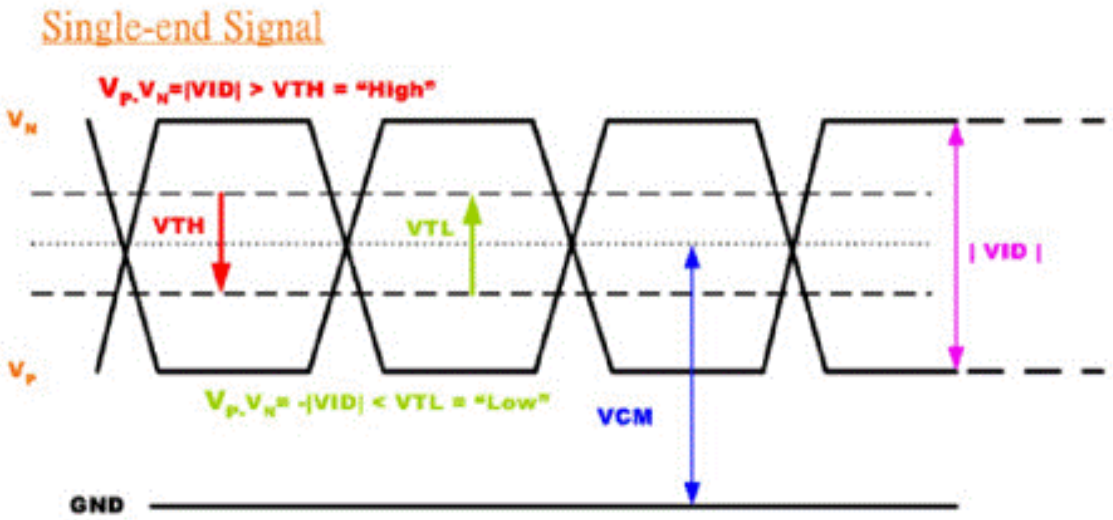
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{TH}	Differential Input High Threshold (Vcm=+1.2V)	---	100	[mV]
V_{TL}	Differential Input Low Threshold (Vcm=+1.2V)	-100	----	[mV]
$\|V_{ID}\|$	Differential Input Voltage	100	600	[mV]
V_{CM}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.1.3 Dynamic contrast ratio Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
Dynamic contrast ratio(DCR) Input High Level	DCR_EN	2.5	-	5.5	[Volt]	Define as Connector Interface (Ta=25℃)
Dynamic contrast ratio(DCR) Input Low Level		-	-	0.8	[Volt]	
DCR Mode Duty Index	Duty	70	-	100	%	Note 1
L0 Gray level	Power	-	0.7P	-	Watt	Note 2
L63 Gray level	Power	-	1P	-	Watt	

Note 1: The minimums dynamic contrast ratio is setting at darkness, and a maximum is setting at brightness.

Note 2: The power saving capability refer to original Backlight power consumption (P)

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.7	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=19mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

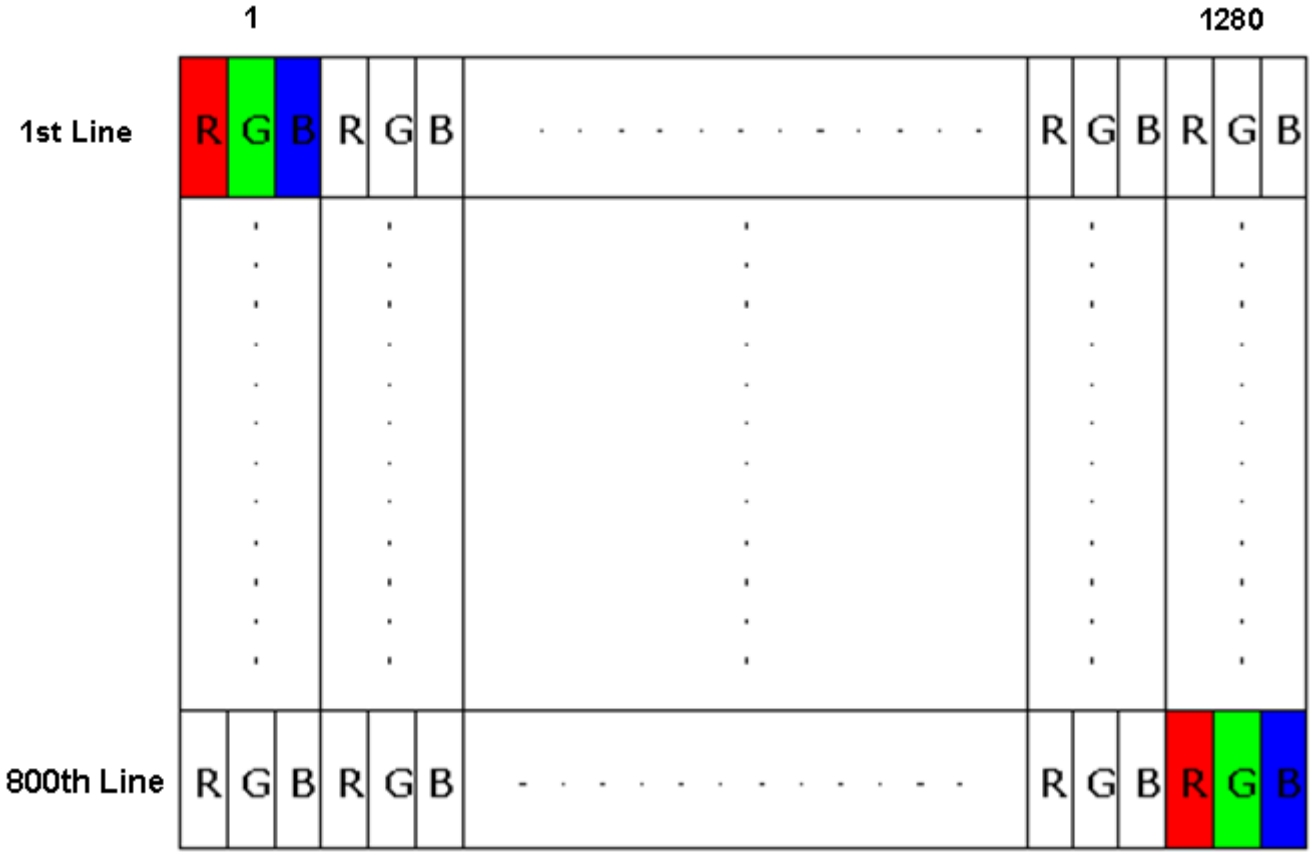
5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.5	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	200	-	20K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

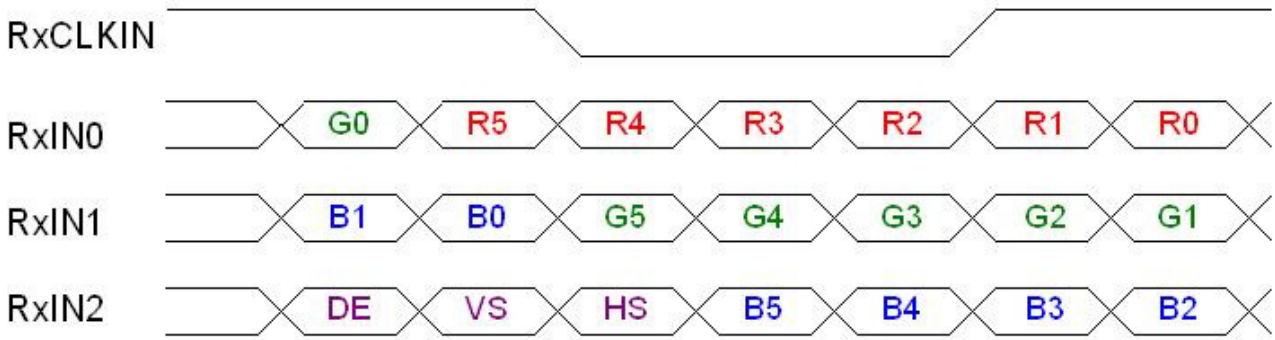
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 LVDS Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

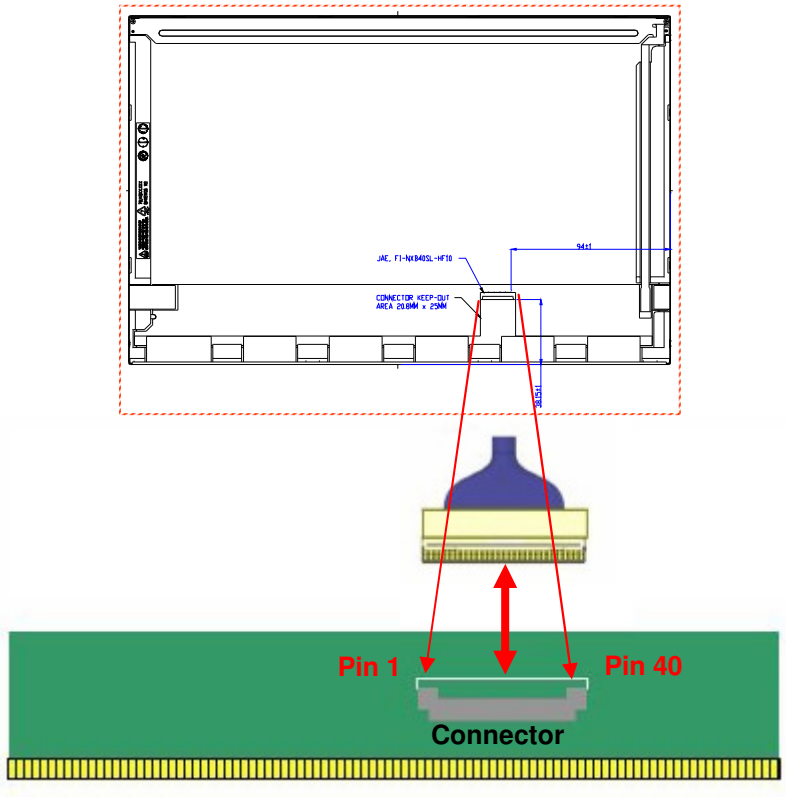
Connector Name / Designation	For Signal Connector
Manufacturer	JAE or Compatible
Type / Part Number	JAE HD1S040HA1 or Compatible
Mating Housing/Part Number	IPEX 20453-040T-11or Compatible

6.3.2 LVDS Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	NC	No Connection (Reserve)
2	AVDD	Power Supply +3.3V
3	AVDD	Power Supply +3.3V
4	VEDID	EDID +3.3V Power
5	NC	No Connection (Reserve)
6	CLK_EDID	EDID Clock Input
7	DAT_EDID	EDID Data Input
8	Rin0-	-LVDSdifferential data input(R0-R5,G0)
9	Rin0+	+LVDSdifferential data input(R0-R5,G0)
10	GND	Ground
11	Rin1-	-LVDSdifferential data input(G1-G5,B0-B1)
12	Rin1+	+LVDSdifferential data input(G1-G5,B0-B1)
13	GND	Ground
14	Rin2-	-LVDSdifferential data input(B2-B5,HS,VS,DE)
15	Rin2+	+LVDSdifferential data input(B2-B5,HS,VS,DE)
16	GND	Ground
17	ClkIN-	-LVDSdifferential clock input
18	ClkIN+	+LVDSdifferential clock input
19	GND	Ground–Shield
20	NC	No Connection (Reserve)
21	NC	No Connection (Reserve)
22	GND	Ground–Shield
23	NC	No Connection (Reserve)

24	NC	No Connection (Reserve)
25	GND	Ground–Shield
26	NC	No Connection (Reserve)
27	NC	No Connection (Reserve)
28	GND	Ground–Shield
29	NC	No Connection (Reserve)
30	NC	No Connection (Reserve)
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection (Reserve)
35	VPWM_EN	System PWM Logic Input Level
36	VLED_EN	LED enable input level
37	DCR_EN	DCR enable input level
38	VLED	LED Power Supply
39	VLED	LED Power Supply
40	VLED	LED Power Supply



Note1: Input signals shall be low or High-impedance state when VDD is off.

6.4 Touch Sensor Signal Description/ Pin Assignment

6.4.1 Touch Sensor Pin Assignment

Pin	Name	Comments	If Unused, Connect to
1	Vcc_5V	5V power	
2	SCL	Serial Interface Clock	Leave open
3	SDA	Serial Interface Data	Leave open
4	CHG	State change interrupt	Leave open
5	GND	Ground	
6	RESET	Reset low	Vcc_3V3, recommend connect to host system
7	DEBUG_DATA	Debug port data	Leave open
8	Enable	Low-Dropout Regulator Control	VCC_3.3 V

6.5 LVDS Interface Timing

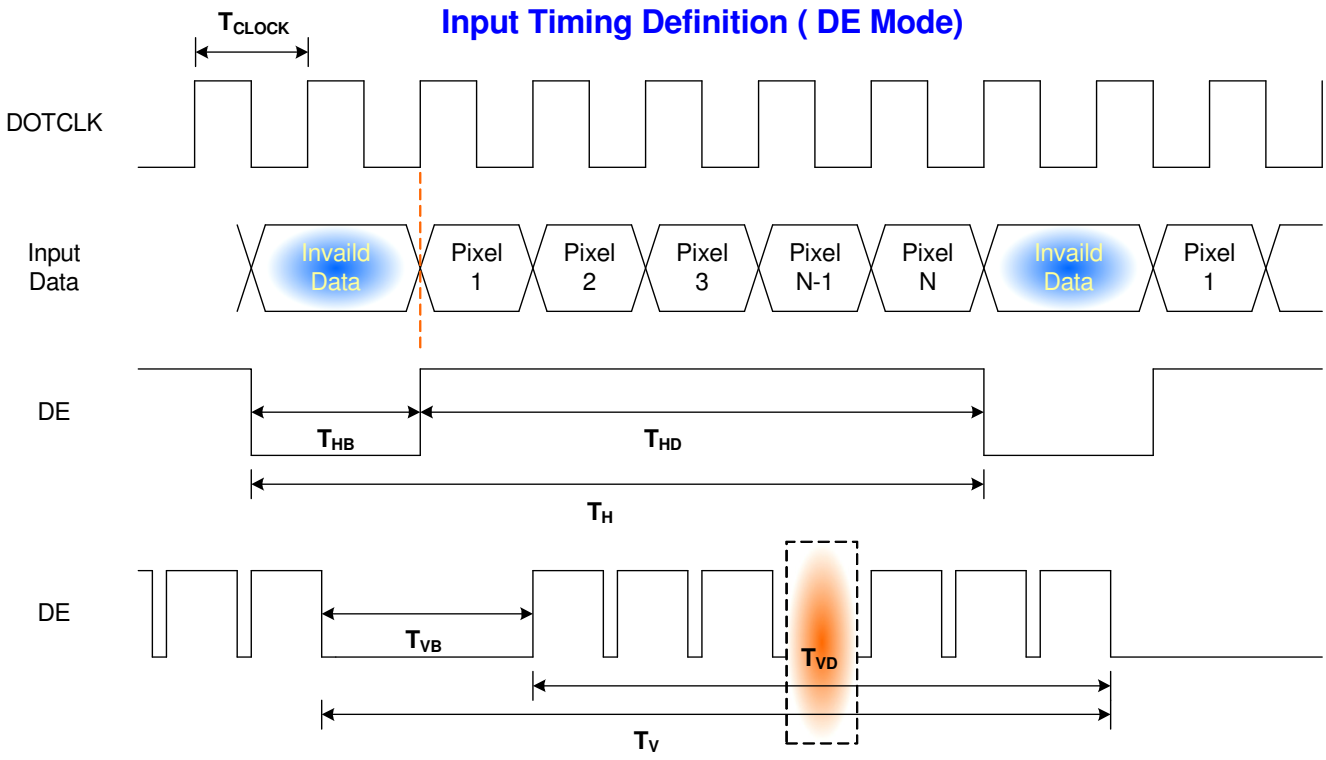
6.5.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T_{Clock}	64	68.93	85	MHz
Vertical Section	Period	T_V	808	816	1023	T_{Line}
	Active	T_{VD}	800			
	Blanking	T_{VB}	8	16	223	
Horizontal Section	Period	T_H	1310	1408	2047	T_{Clock}
	Active	T_{HD}	1280			
	Blanking	T_{HB}	40	168	767	

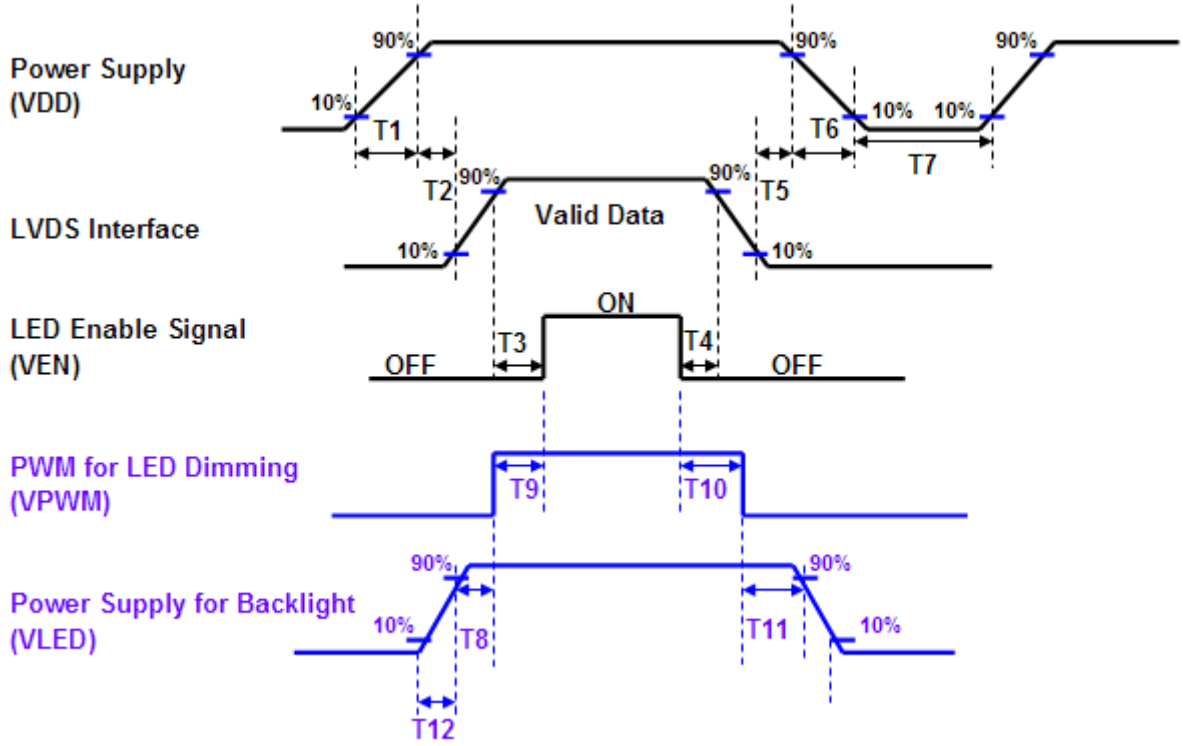
Note : DE mode only

6.5.2 Timing diagram



6.6 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Power Sequence Timing			
Parameter	Value		Units
	Min.	Max.	
T1	0.5	10	ms
T2	0	50	
T3	200	-	
T4	200	-	
T5	0	50	
T6	0	10	
T7	500	-	
T8	10	-	
T9	0	180	
T10	0	180	
T11	10	-	
T12	0.5	10	

7. Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

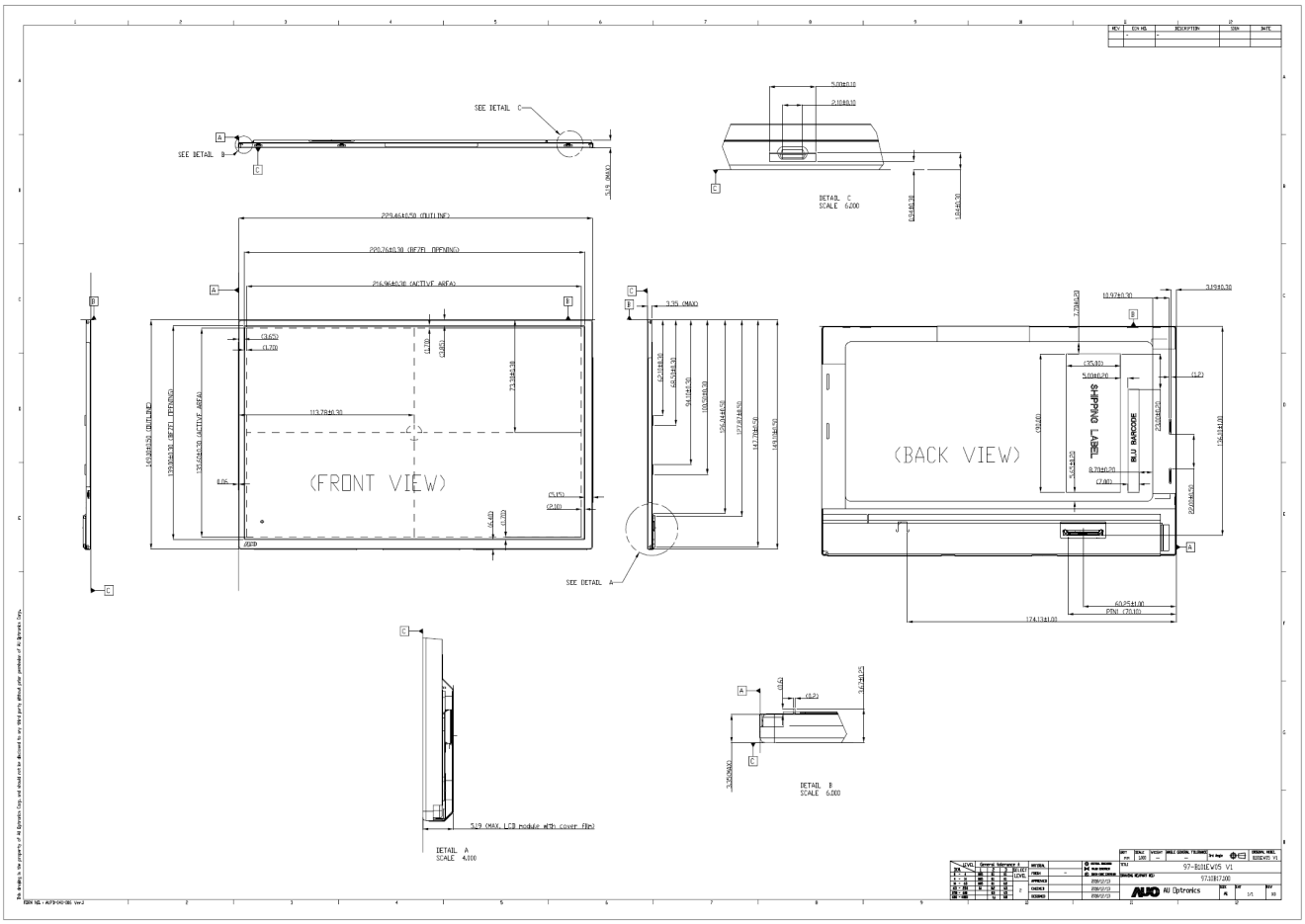
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension

8.1.1 Standard Front View &Rear View & Key components remark and remind

Prevention damage the IC, connector, Capacitor…., we recommend your design (Ex: cable, rib, hardness parts) far away those section those have remarked at this drawing.



Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

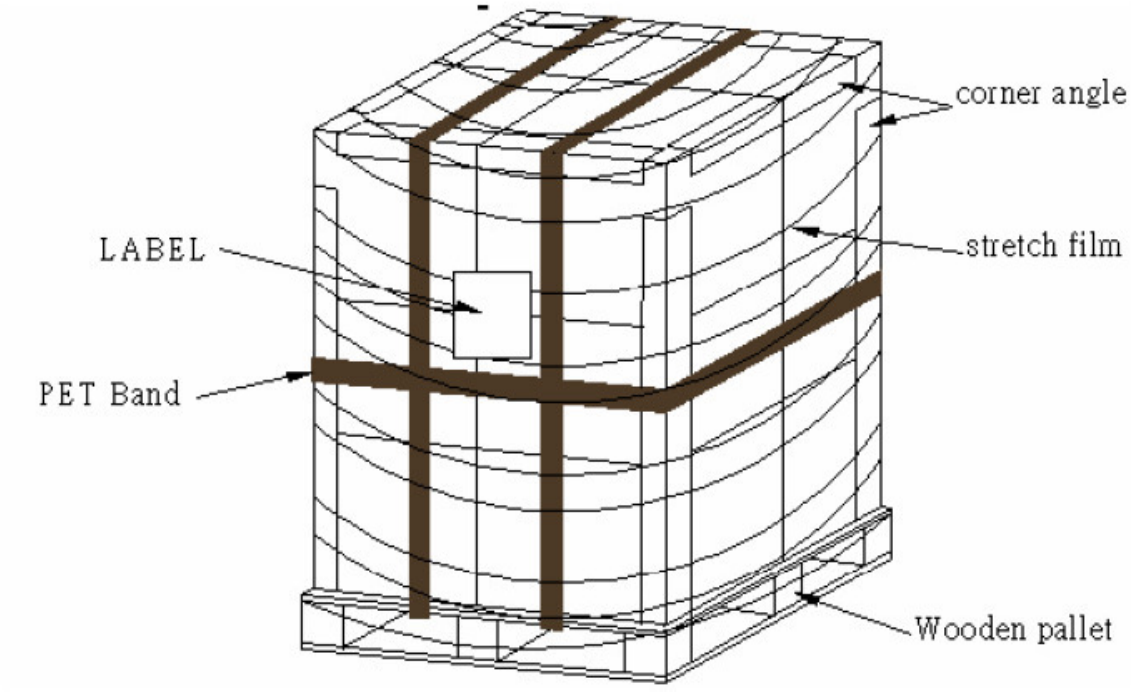
9. Shipping and Package

9.1 Shipping Label Format

9.2 Carton Package

The outside dimension of carton is (L)mm x (W)mm x (H)mm

9.3 Shipping Package of Palletizing Sequence



10. Appendix

10.1 EDID Description

B101EW05 V1 EDID Code

Address	FUNCTION	Value
HEX		HEX
00	Header	00
01		FF
02		FF
03		FF
04		FF
05		FF
06		FF
07		00
08	EISA Manuf. Code LSB	06
09	Compressed ASCII	AF
0A	Product Code	D4
0B	hex, LSB first	51
0C	32-bit ser #	00
0D		00
0E		00
0F		00
10	Week of manufacture	00
11	Year of manufacture	14
12	EDID Structure Ver.	01
13	EDID revision #	04
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	90
15	**Max H image size** *(rounded to cm)*	16
16	**Max V image size** *(rounded to cm)*	0E
17	**Display Gamma** *(=(gamma*100)-100)*	78
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02
19	Red/green low bits **(Lower 2:2:2:2 bits)**	CB
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	55
1B	Red x **(Upper 8 bits)**	94
1C	Red y/ highER 8 bits	57
1D	Green x	53
1E	Green y	8E
1F	Blue x	27
20	Blue y	23
21	White x	50
22	White y	54
23	Established timing 1	00

24	Established timing 2	00
25	Established timing 3	00
26	Standard timing #1	01
27		01
28	Standard timing #2	01
29		01
2A	Standard timing #3	01
2B		01
2C	Standard timing #4	01
2D		01
2E	Standard timing #5	01
2F		01
30	Standard timing #6	01
31		01
32	Standard timing #7	01
33		01
34	Standard timing #8	01
35		01
36	Pixel Clock/10000 LSB	D0
37	Pixel Clock/10000 USB	1B
38	Horz active **Lower 8bits**	00
39	Horz blanking **Lower 8bits**	B8
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	50
3B	Vertical Active **Lower 8bits**	20
3C	Vertical Blanking **Lower 8bits**	08
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30
3E	HorzSync. Offset	08
3F	HorzSync.Width	0A
40	VertSync.Offset : VertSync.Width	31
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00
42	Horizontal Image Size **Lower 8bits**	D8
43	Vertical Image Size **Lower 8bits**	87
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	00
45	Horizontal Border *(zero for internal LCD)*	00
46	Vertical Border *(zero for internal LCD)*	00
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18
48	Detailed timing/monitor	00
49	descriptor #2	00
4A		00
4B		0F
4C		00
4D		00
4E		00

4F		00
50		00
51		00
52		00
53		00
54		00
55		00
56		00
57		00
58		00
59		20
5A	Detailed timing/monitor	00
5B	descriptor #3	00
5C		00
5D		FE
5E		00
5F	Manufacture	41
60	Manufacture	55
61	Manufacture	4F
62		0A
63		20
64		20
65		20
66		20
67		20
68		20
69		20
6A		20
6B		20
6C	Detailed timing/monitor	00
6D	descriptor #4	00
6E		00
6F		FE
70		00
71	Manufacture P/N	42
72	Manufacture P/N	31
73	Manufacture P/N	30
74	Manufacture P/N	31
75	Manufacture P/N	45
76	Manufacture P/N	57
77	Manufacture P/N	30
78	Manufacture P/N	35
79	Manufacture P/N	20

7A	Manufacture P/N	56
7B	Manufacture P/N	31
7C		20
7D		0A
7E	Extension Flag	00
7F	Checksum	16