



Product Specification

AU OPTRONICS CORPORATION

B133EW01 V2

(V) Preliminary Specifications

() Final Specifications

Module	13.3" WXGA Color TFT-LCD
Model Name	B133EW01 V2

Customer	Date
_____	_____
Checked & Approved by	
_____	_____
Note: This Specification is subject to change without notice.	

Approved by	Date
_____	_____
Prepared by	
_____	_____
MDBU Marketing Division / AU Optronics corporation	



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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2006/4/23	All	First Edition for Customer		



1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
- 14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.



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2. General Description

B133EW01 V2 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter of backlight is not included.

B133EW01 V2 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	337.8 (13.3 W")
Active Area	[mm]	286.08 (H) x 178.8 (V)
Pixels H x V		1280x3(RGB) x 800
Pixel Pitch	[mm]	0.2235 x 0.2235
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (I _{CCFL} =6.0mA) Note: I _{CCFL} is lamp current	[cd/m ²]	250 typ. (5 points average) 210 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		400 typ
Optical Rise Time/Fall Time	[msec]	16 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption	[Watt]	4.8 max.(without inverter)
Weight	[Grams]	350 typ.
Physical Size	[mm]	299.5 max. (W) x 195.5 max. (H) x 5.5
Electrical Interface		1 channel LVDS
Surface Treatment		Glare, Hardness 3H, Reflectance ~4 %
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance



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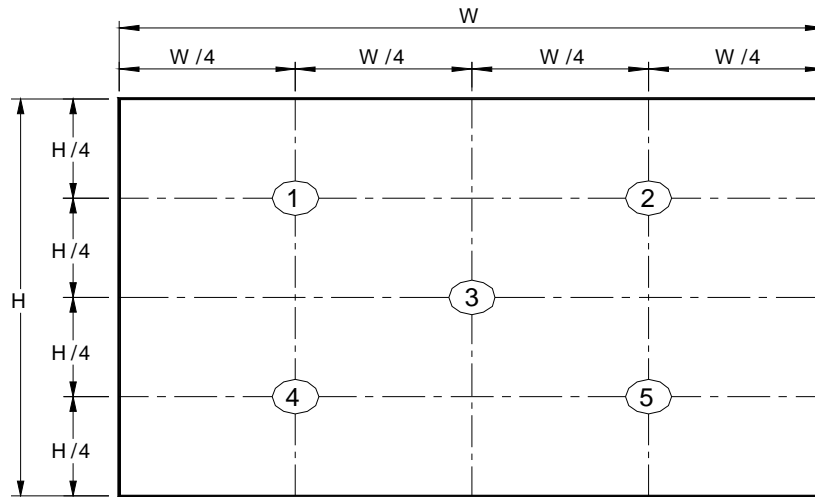
B133EW01 V2

2.2 Optical Characteristics

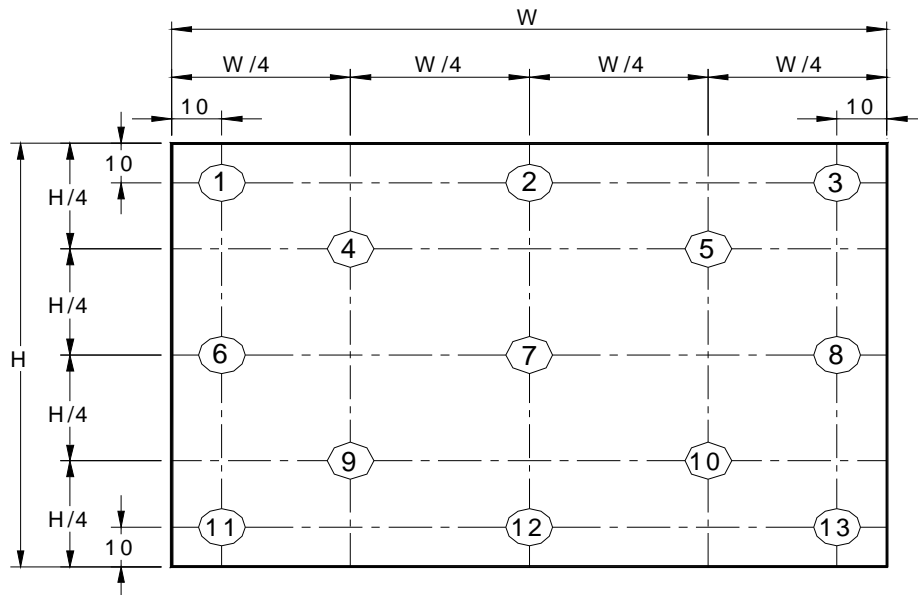
The optical characteristics are measured under stable conditions at 25°C (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance I _{CCFL} =6.0mA	[cd/m ²]	5 points average	210	250	-	1, 4, 5.
Viewing Angle	[degree]	Horizontal (Right)	40	45	-	8
	[degree]	CR = 10 (Left)	40	45	-	
	[degree]	Vertical (Upper)	10	25	-	
	[degree]	CR = 10 (Lower)	30	35	-	
Luminance Uniformity		5 Points			1.25	1
Luminance Uniformity		13 Points			1.50	2
CR: Contrast Ratio			300	400	-	6
Cross talk	%				4	7
Response Time	[msec]	Rising	-	4	8	8
	[msec]	Falling	-	12	17	
	[msec]	Rising + Falling		16	25	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.565	0.595	0.625	2,8
		Red y	0.315	0.345	0.375	
		Green x	0.29	0.32	0.35	
		Green y	0.525	0.555	0.585	
		Blue x	0.125	0.155	0.185	
		Blue y	0.115	0.145	0.175	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	

Note 1: 5 points position (Display area : 286.08 (H) x 178.8 (V)mm)



Note 2: 13 points position



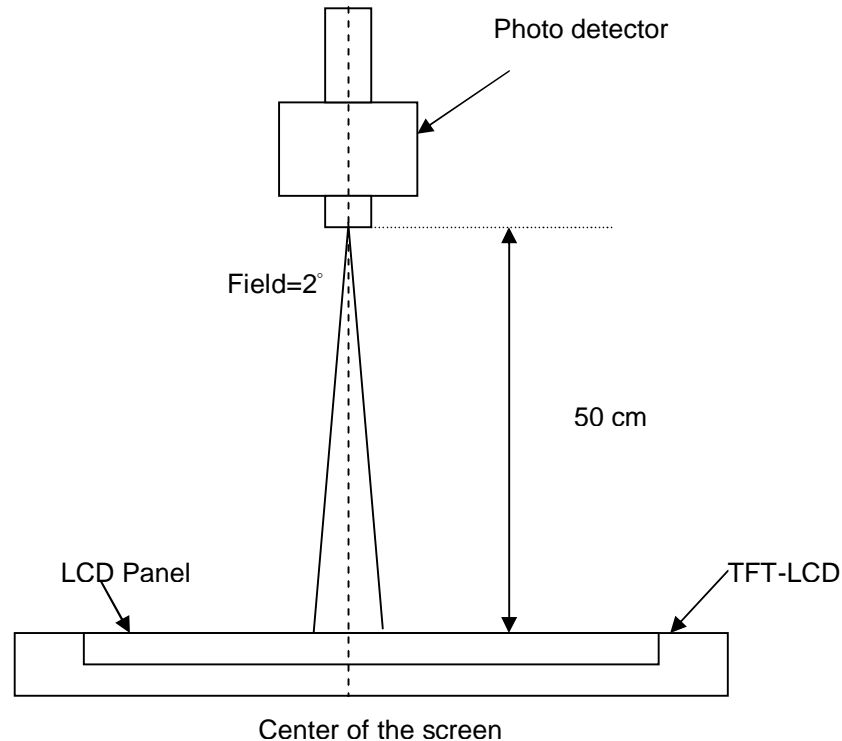
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

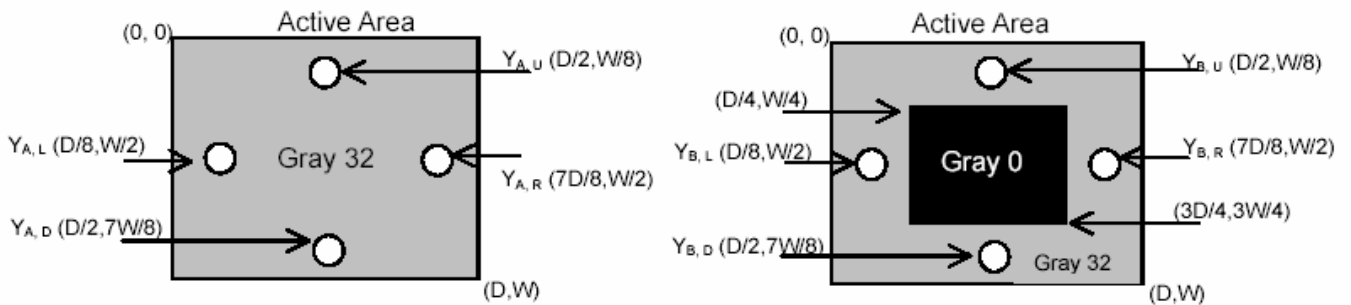
Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

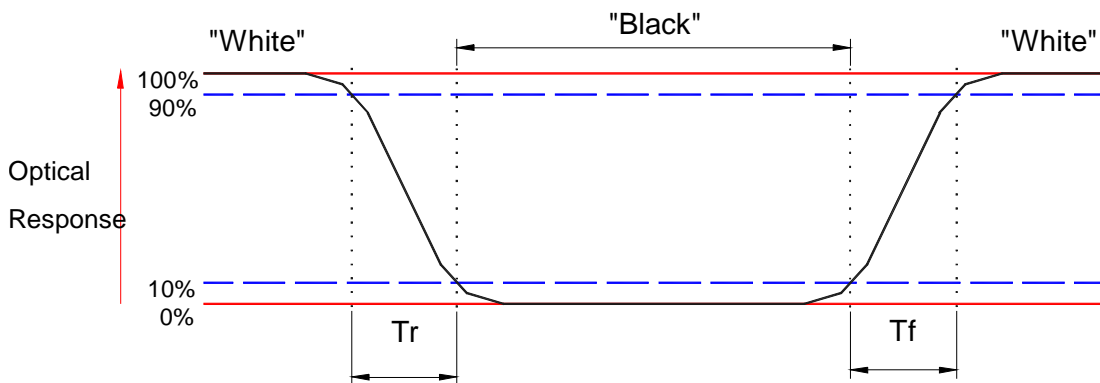
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



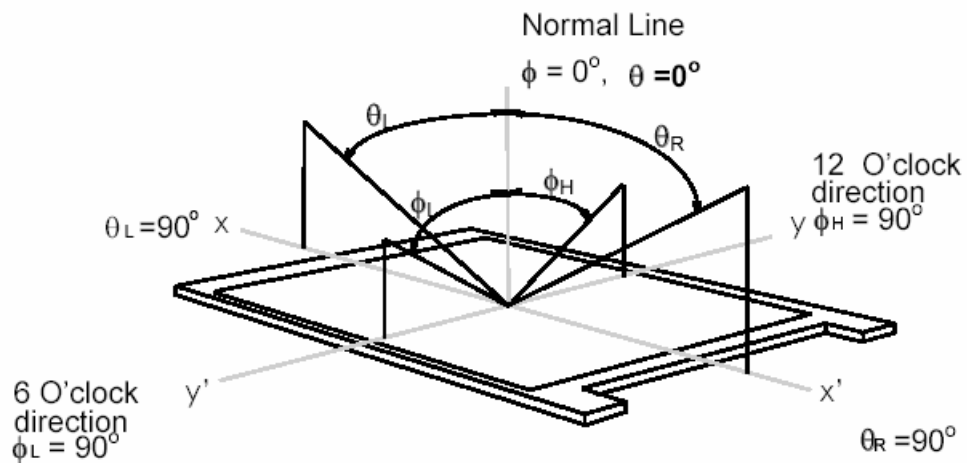
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



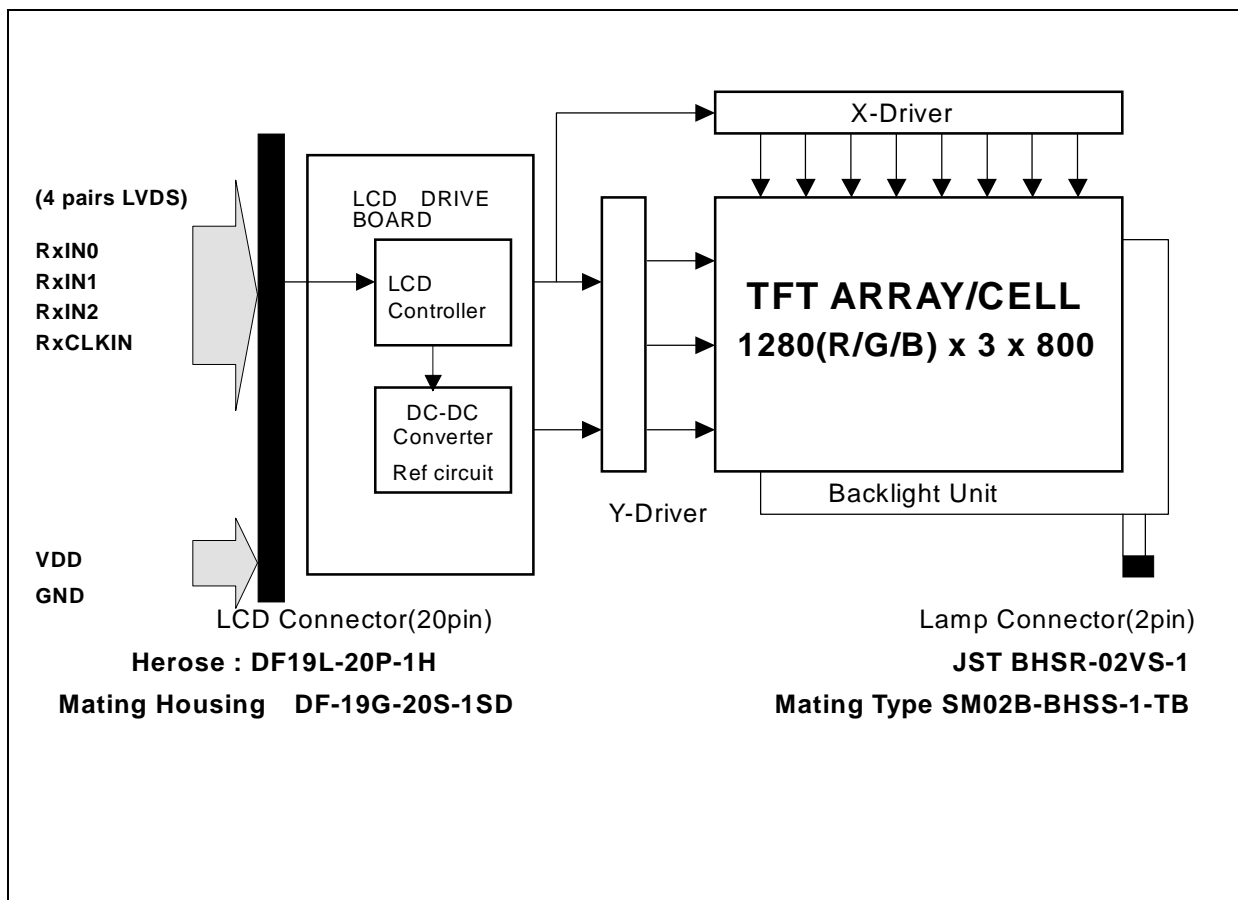
Note 8. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 13.3 inches wide Color TFT/LCD Module:





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4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	-	6.5	[mA] rms	Note 1,2

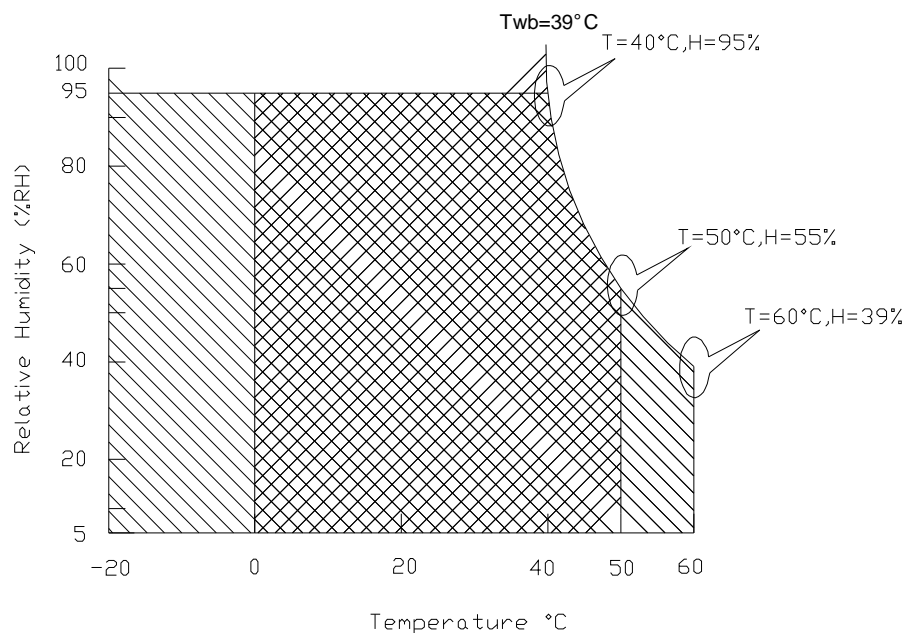
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range



Storage Range



5. Electrical characteristics

5.1 TFT LCD Module

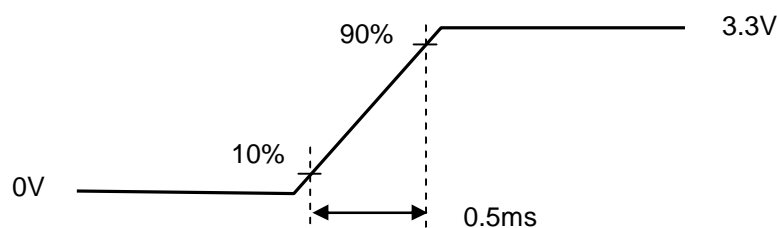
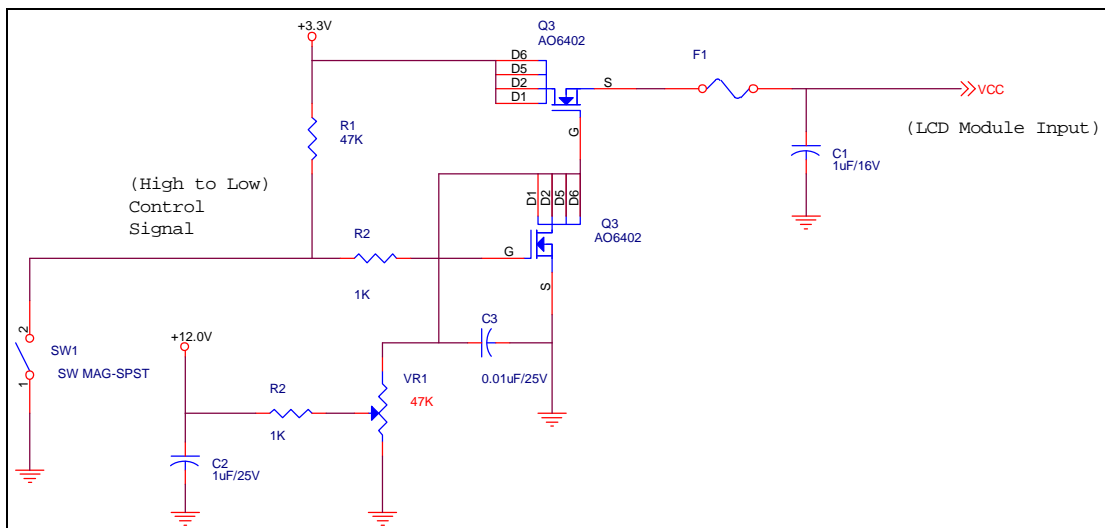
5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power			0.8	[Watt]	Note 1
IDD	IDD Current		200	2500	[mA]	Note 1
IRush	Inrush Current			1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Measure Condition



Vin rising time

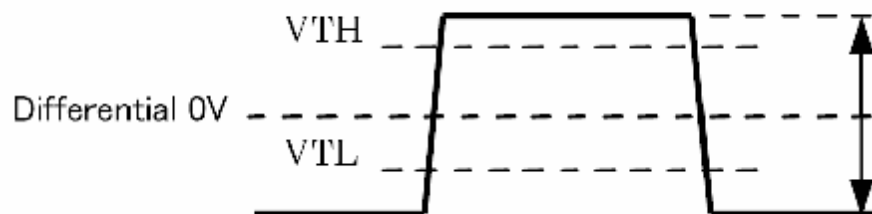
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold ($V_{cm}=+1.2V$)		100	[mV]
Vtl	Differential Input Low Threshold ($V_{cm}=+1.2V$)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.0	1.5	[V]

Note: LVDS Differential Voltage



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	210	250	-	[cd/m ²]	(Ta=25°C)
CCFL current(I _{CCFL})	2.0	6.0	7.0	[mA] rms	(Ta=25°C) Note 2
CCFL Frequency(F _{CCFL})	45	62	70	[KHz]	(Ta=25°C) Note 3,4
CCFL Ignition Voltage(V _s)	1315			[Volt] rms	(Ta= 0°C) Note 5
CCFL Ignition Voltage(V _s)	1095			[Volt] rms	(Ta= 25°C) Note 5
CCFL Voltage (Reference) (V _{CCFL})	608	640	672	[Volt] rms	(Ta=25°C) Note 6
CCFL Power consumption (P _{CCFL})	-	3.8	4.2	[Watt]	(Ta=25°C) Note 6

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully.

Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has "Duty Dimming", if ICCFL is less than 4mA.

Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,430 voltage. Lamp units need 1,400 voltage minimum for ignition.

Note 6: Calculator value for reference ($I_{CCFL} \times V_{CCFL} = P_{CCFL}$)

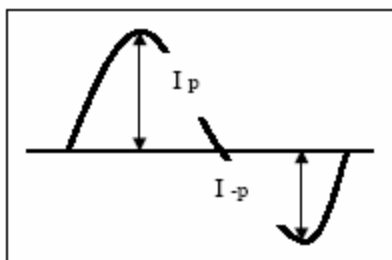
Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.

b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$.

* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$$\frac{|I_p - I_{-p}|}{I_{rms}} \times 100\%$$

* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{rms}$$



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6. Signal Characteristic

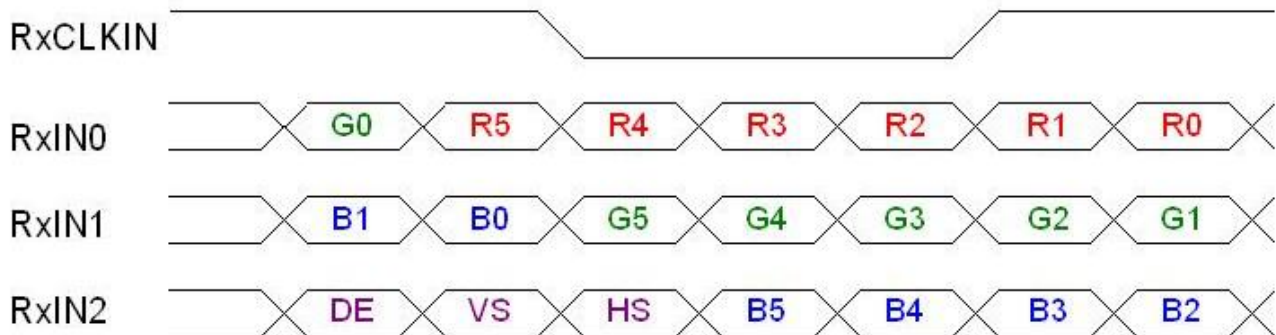
6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

	0			1													1278			1279		
1st Line	R	G	B	R	G	B	-										R	G	B	R	G	B

800th Line	R	G	B	R	G	B	-										R	G	B	R	G	B

6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The typical frequency is 68.9 MHZ.. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.



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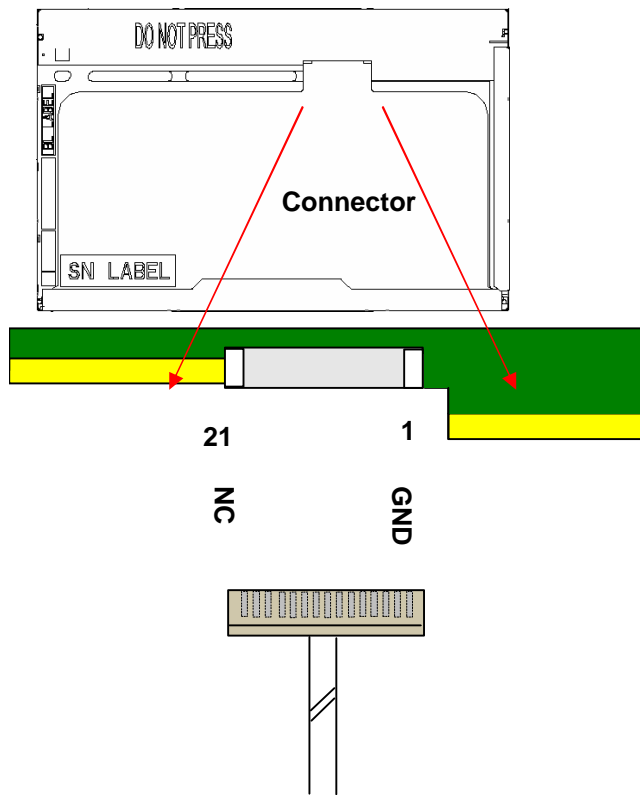
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6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

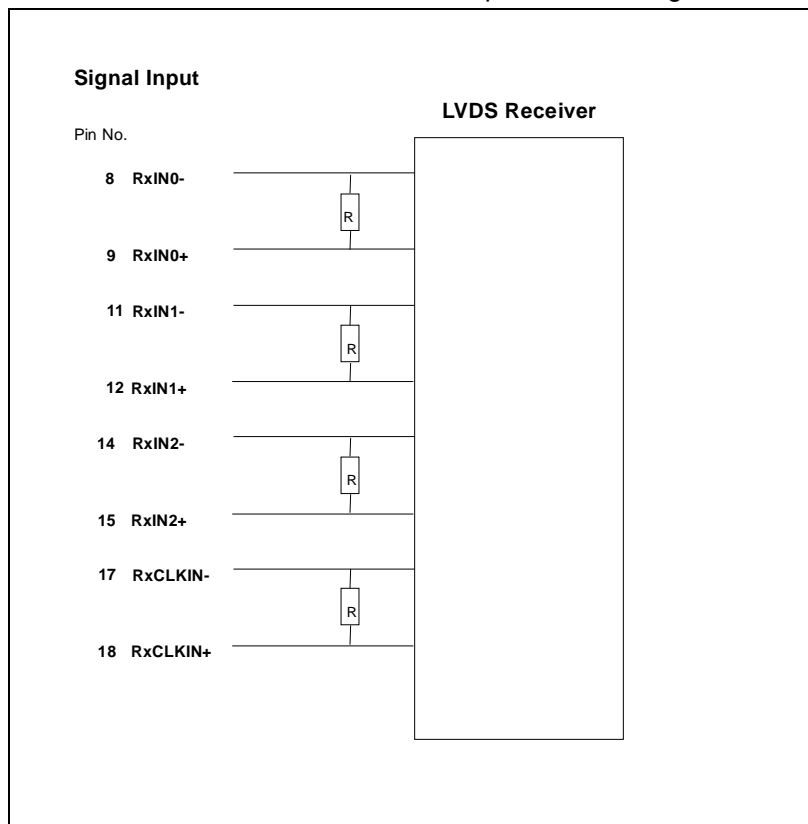
PIN#	Signal Name	Description
1	GND	Ground
2	VDD	+3.3V Power Supply
3	VDD	+3.3V Power Supply
4	V _{EDID}	+3.3V EDID Power
5	NC	No Connection (Reserve for AUO test)
6	CLK _{EDID}	EDID Clock Input
7	DATA _{EDID}	EDID Data Input
8	RxIN0-	LVDS differential data input(R0-R5, G0)
9	RxIN0+	LVDS differential data input(R0-R5, G0)
10	GND	Ground
11	RxIN1-	LVDS differential data input(G1-G5, B0-B1)
12	RxIN1+	LVDS differential data input(G1-G5, B0-B1)
13	GND	Ground
14	RxIN2-	LVDS differential data input(B2-B5, HS, VS, DE)
15	RxIN2+	LVDS differential data input(B2-B5, HS, VS, DE)
16	GND	Ground
17	RxCLKIN-	LVDS differential clock input
18	RxCLKIN+	LVDS differential clock input
19	GND	Ground
20	GND	Ground

Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.
internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

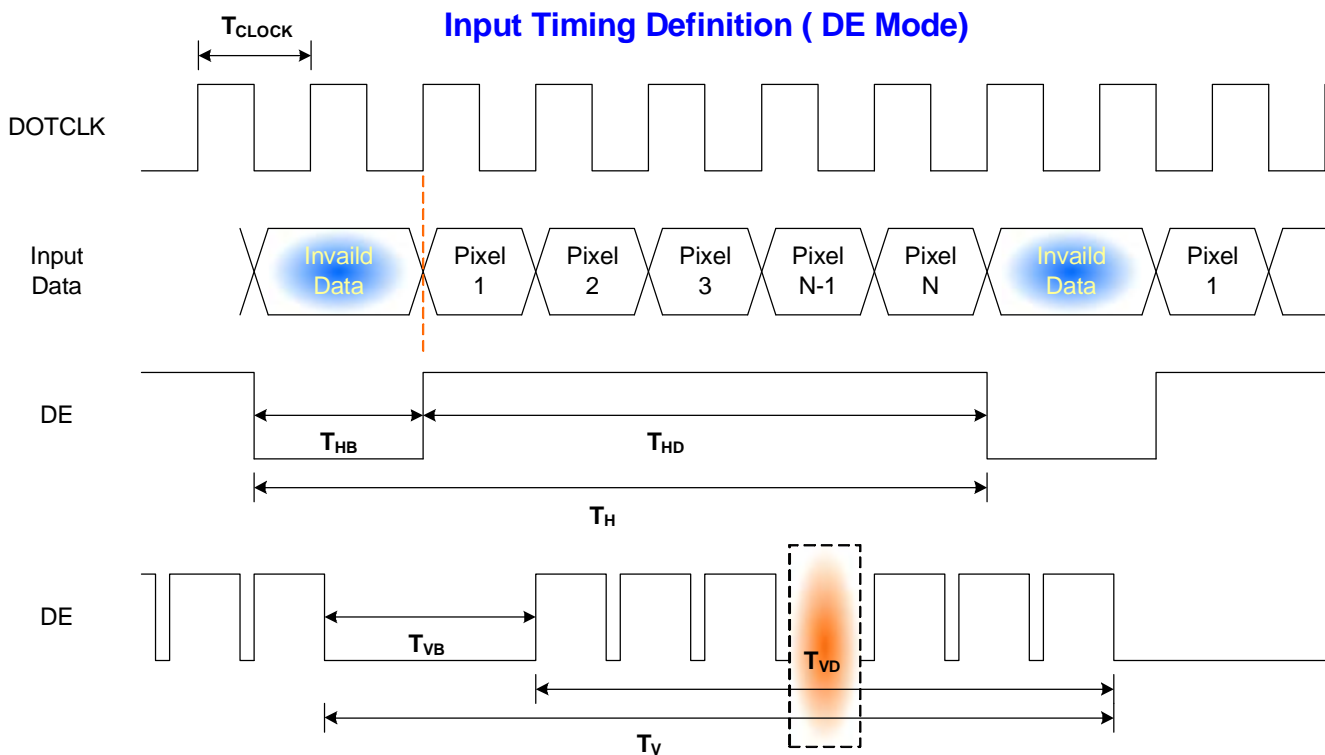
6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		$1/T_{\text{Clock}}$	50	68.9	80	MHz
Vertical Section	Period	T_V	803	816	832	T_{Line}
	Active	T_{VD}	-	800	-	
	Blanking	T_{VB}	3	16	32	
Horizontal Section	Period	T_H	1302	1408	1700	T_{Clock}
	Active	T_{HD}	-	1280	-	
	Blanking	T_{HB}	22	128	420	

Note : DE mode only

6.4.2 Timing diagram





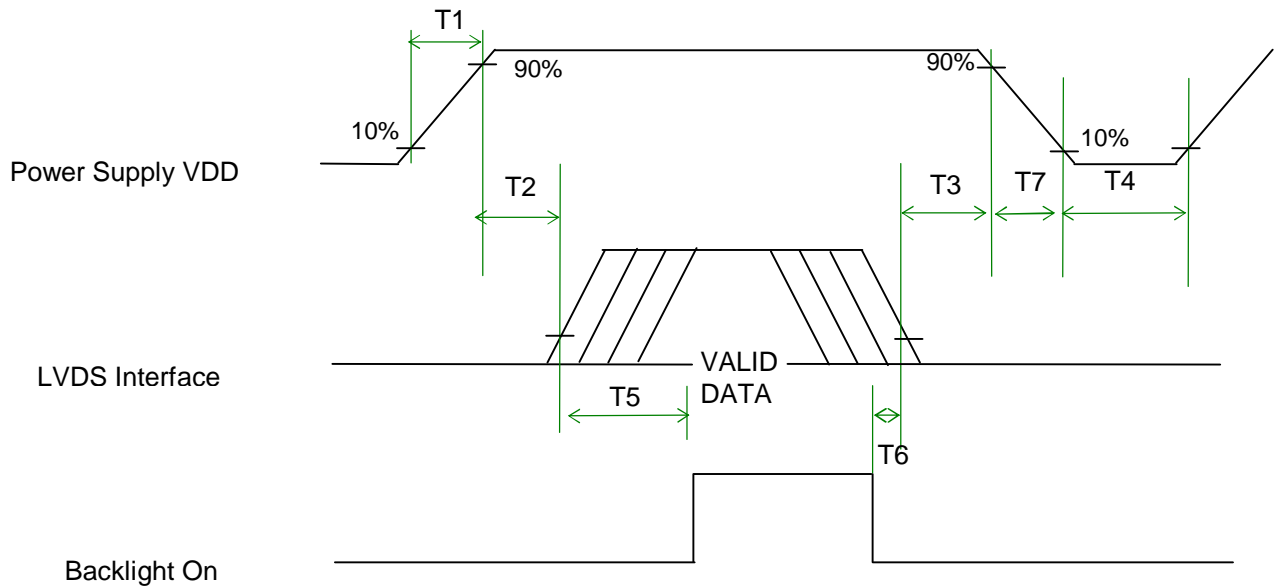
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6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)



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7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	Hirose or compatible
Type / Part Number	DF-19LA-20P-1H or compatible
Mating Housing/Part Number	DF19G-20S-1SD or compatible

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage



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8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- I Test method: Non-Operation
- I Acceleration: 1.5G , sine wave
- I Frequency: 10 - 500Hz Random
- I Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

- I Test method: Non-Operation
- I Acceleration: 200 G , Half sine wave
- I Active time: 2 ms
- I Pulse: X,Y,Z .one time for each side



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9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	40°C/90%,300Hr	
High Temperature Operation	60°C/Dry,300Hr	
Low Temperature Operation	0°C ,300Hr	
On/Off Test	25°C , ON/30 sec. OFF/30sec., 10,000 cycles)	
Hot Storage	60°C/35% RH ,250 hours	
Cold Storage	-20°C/50% RH ,250 hours	
Thermal Shock Test	-20°C/30 min ,60°C/30 min 100cycles	
Hot Start Test	50°C/1 Hr min. power on/off per 5 minutes, 5 times	
Cold Start Test	0°C/1 Hr min. power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	200G, 2ms, Half-sine wave	
Vibration Test (Non-Operating)	Sine-wave vibration, 1.5 G zero-to-peak, 10 to 500 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact : ±8KV/ operation Air : ±15KV / operation	Note 1
Room temperature Test	25°C , 2000hours, Operating with loop pattern	

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost
. Self-recoverable. No hardware failures.

Note2: CCFL Life time: 10,000 hours minimum under normal module usage.

Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

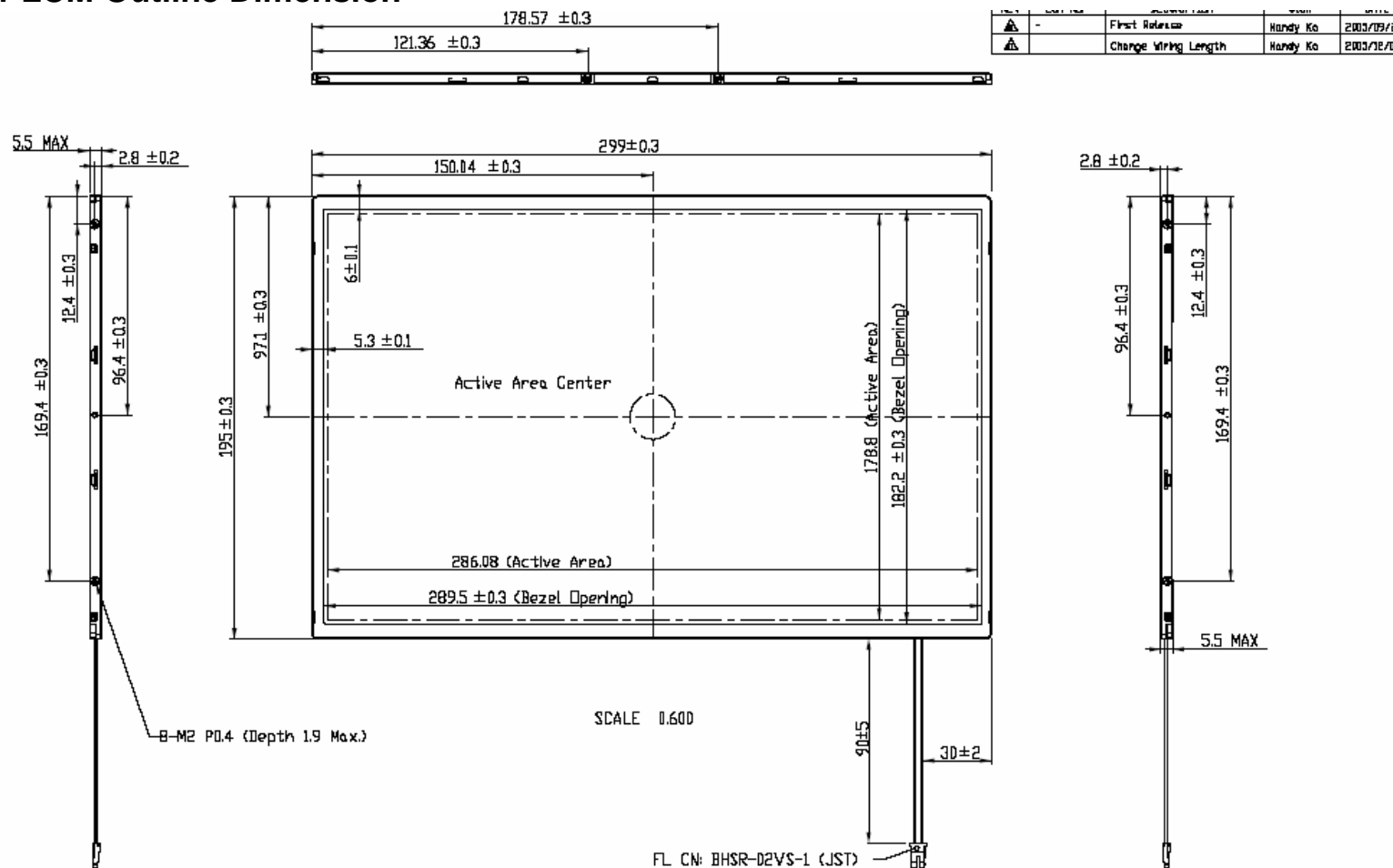
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10. Mechanical Characteristics

10.1 LCM Outline Dimension

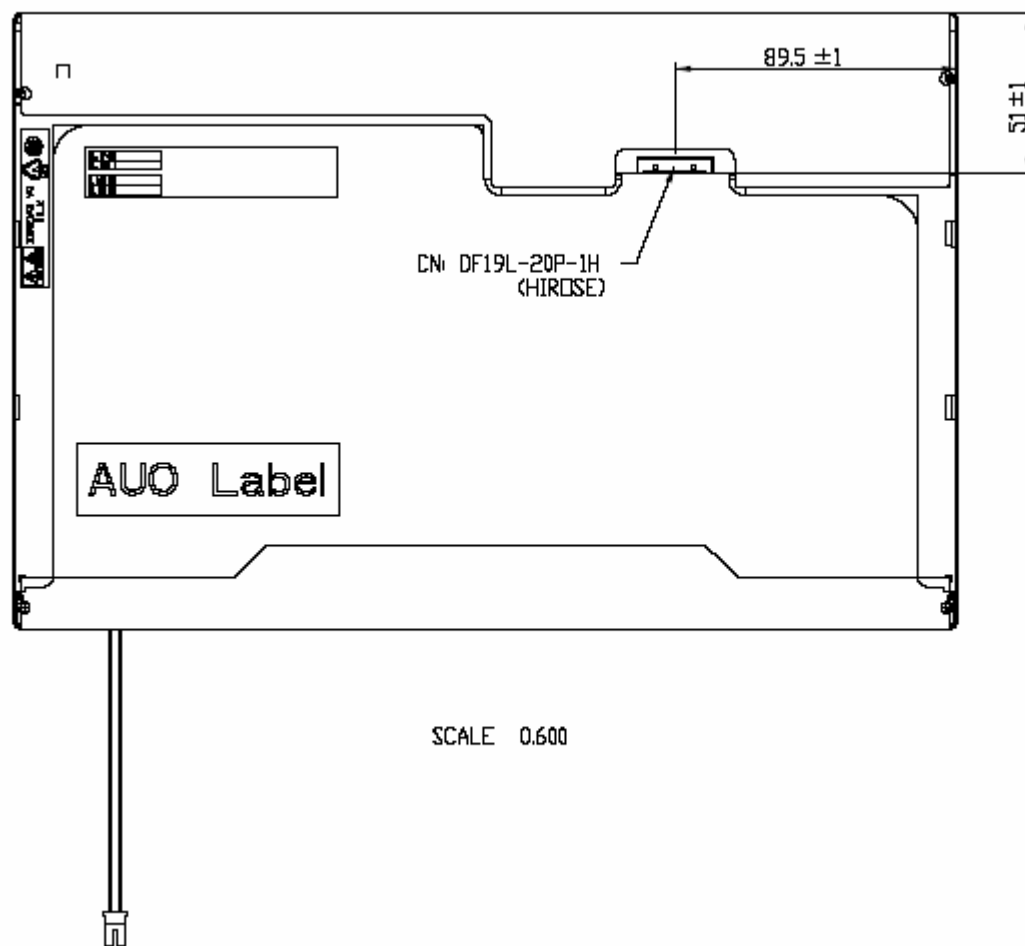




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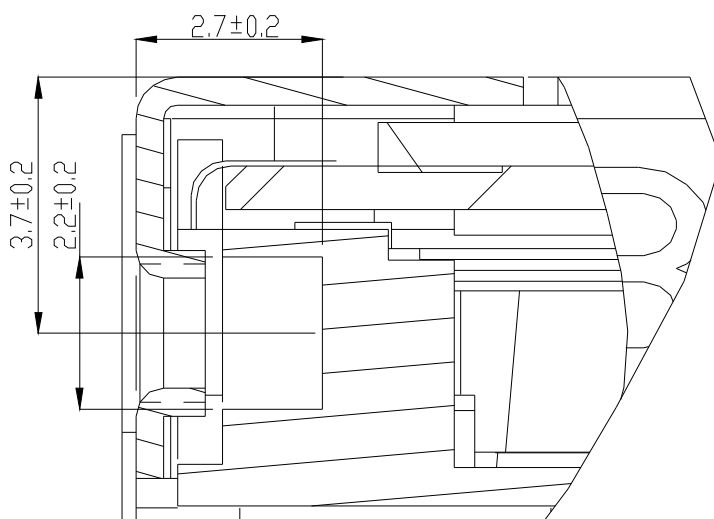


10.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface = 2.5 mm (See drawing)

Screw hole center location, from front surface = 2.8 ± 0.2 mm (See drawing)

Screw Torque: Maximum 2.1 kgf-cm





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11. Shipping and Package

11.1 Shipping Label Format

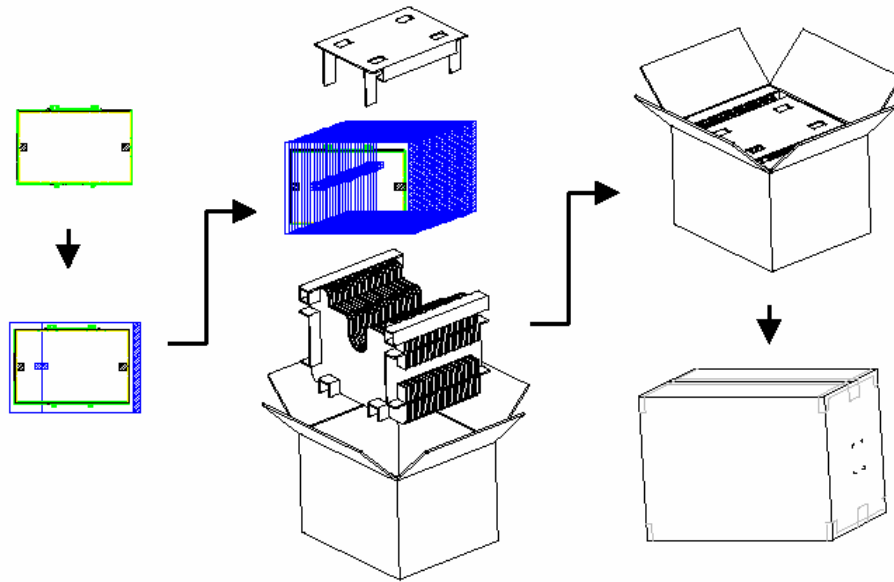
TBD

Note 1:

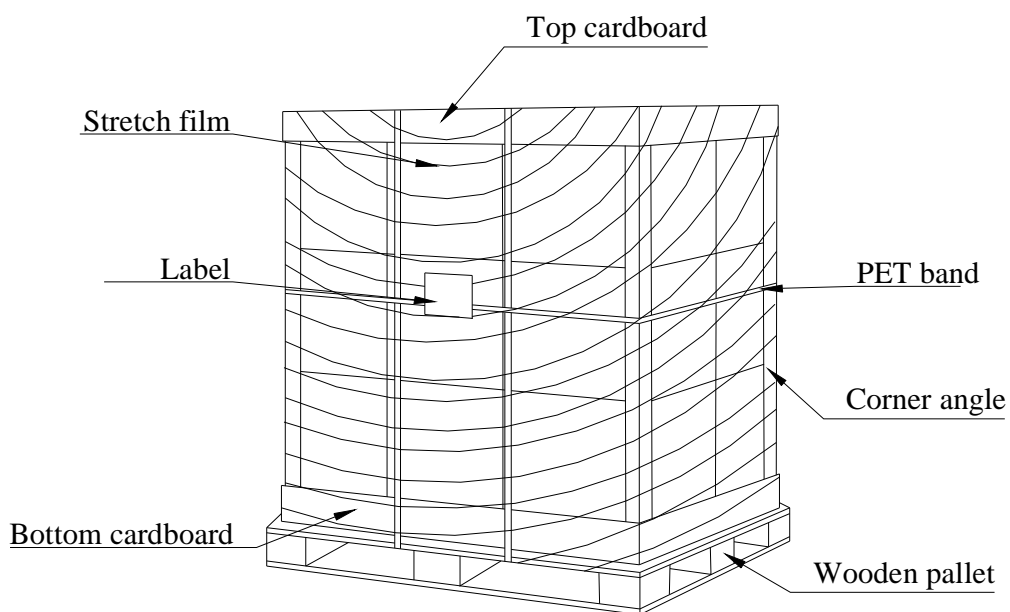
IC Combination	Control Code	H/W
TSB/NT (gate/source)	OAXXX	OA
NT/NT(gate/source)	1AXXX	1A

11.2. Carton package

The outside dimension of carton is **TBD**



11.3 Shipping package of palletizing





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12. Appendix: EDID description

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Address	Address	Field Name & Comments	Value	Value	Value
(Decimal)	(HEX)		(HEX)	(BIN)	(DEC)
0	0	Header	00	00000000	0
1	1		FF	11111111	255
2	2		FF	11111111	255
3	3		FF	11111111	255
4	4		FF	11111111	255
5	5		FF	11111111	255
6	6		FF	11111111	255
7	7		00	00000000	0
8	8	ASCII Data String:B133EW01	06	00000110	6
9	9	Compressed ASCII	AF	10101111	175
10	0A	Product Code = 24	24	00100100	36
11	0B	hex, LSB first = 12	12	00010010	18
12	0C	32-bit serial #	00	00000000	0
13	0D		00	00000000	0
14	0E		00	00000000	0
15	0F		00	00000000	0
16	10	Week 1	01	00000001	1
17	11	Year(2006-1990=16)	10	00010000	16
18	12	EDID Structure Ver # = 1	01	00000001	1
19	13	EDID revision # = 3	03	00000011	3
20	14	Digital Input	80	10000000	128
21	15	Max H image size = 29 Cm	1D	00011101	29
22	16	Max V image size = 18 Cm	12	00010010	18
23	17	Display Gamma = 2.2	78	01111000	120
24	18	no DPMS,Active off,RGB color	0A	00001010	10
25	19	Red/green low bits	50	01010000	80
26	1A	Blue/white low bits	C5	11000101	197
27	1B	Red x , Red x = 0.595	98	10011000	152
28	1C	Red y , Red y = 0.345	58	01011000	88
29	1D	Green x , Green x = 0.32	52	01010010	82



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30	1E	Green y , Green y = 0.555	8E	10001110	142
31	1F	Blue x , Blue x = 0.155	27	00100111	39
32	20	Blue y , Blue y = 0.145	25	00100101	37
33	21	White x , White x = 0.313	50	01010000	80
34	22	White y , White y = 0.329	54	01010100	84
35	23		00	00000000	0
36	24		00	00000000	0
37	25		00	00000000	0
38	26		01	00000001	1
39	27		01	00000001	1
40	28		01	00000001	1
41	29		01	00000001	1
42	2A		01	00000001	1
43	2B		01	00000001	1
44	2C		01	00000001	1
45	2D		01	00000001	1
46	2E		01	00000001	1
47	2F		01	00000001	1
48	30		01	00000001	1
49	31		01	00000001	1
50	32		01	00000001	1
51	33		01	00000001	1
52	34		01	00000001	1
53	35		01	00000001	1
54	36	Detailed timing/monitor	BC	10111100	188
55	37	1280x800 @60Hz : Pixel Clock =71 MHz	1B	00011011	27
56	38	Hor active=1280 pixels	00	00000000	0
57	39	Hor blanking=160 pixels	A0	10100000	160
58	3A		50	01010000	80
59	3B	Vertical active=800 lines	20	00100000	32
60	3C	Vertical blanking=23lines	17	00010111	23
61	3D		30	00110000	48
62	3E	H sync. Offset=48 pixels	30	00110000	48
63	3F	H sync. Width=32 pixels	20	00100000	32
64	40	V sync. Offset=3 lines	36	00110110	54



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65	41	V sync. Width=6 lines	00	00000000	0
66	42	H image size= 286.08 mm	1E	00011110	30
67	43	V image size = 178.8 mm	B3	10110011	179
68	44		10	00010000	16
69	45		00	00000000	0
70	46		00	00000000	0
71	47		18	00011000	24
72	48		00	00000000	0
73	49		00	00000000	0
74	4A		00	00000000	0
75	4B		0F	00001111	15
76	4C	Version	00	00000000	0
77	4D		00	00000000	0
78	4E		00	00000000	0
79	4F	Link Type (LVDS Link,MSB justified)	00	00000000	0
80	50	Pixel and link component format (6-bit panel interface)	00	00000000	0
81	51	Panel features (No inverter)	00	00000000	0
82	52		00	00000000	0
83	53		00	00000000	0
84	54		00	00000000	0
85	55		00	00000000	0
86	56		00	00000000	0
87	57		00	00000000	0
88	58		00	00000000	0
89	59		20	00100000	32
90	5A		00	00000000	0
91	5B		00	00000000	0
92	5C		00	00000000	0
93	5D		FE	11111110	254
94	5E		00	00000000	0
95	5F	A	41	01000001	65
96	60	U	55	01010101	85
97	61	O	4F	01001111	79
98	62		0A	00001010	10



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99	63		20	00100000	32
100	64		20	00100000	32
101	65		20	00100000	32
102	66		20	00100000	32
103	67		20	00100000	32
104	68		20	00100000	32
105	69		20	00100000	32
106	6A		20	00100000	32
107	6B		20	00100000	32
108	6C		00	00000000	0
109	6D		00	00000000	0
110	6E		00	00000000	0
111	6F		FE	11111110	254
112	70		00	00000000	0
113	71	B	42	01000010	66
114	72	1	31	00110001	49
115	73	3	33	00110011	51
116	74	1	33	00110011	51
117	75	E	45	01000101	69
118	76	W	57	01010111	87
119	77	0	30	00110000	48
120	78	1	31	00110001	49
121	79		20	00100000	32
122	7A	V	56	01010110	86
123	7B	2	32	00110010	50
124	7C		20	00100000	32
125	7D		0A	00001010	10
126	7E	Extension Flag = 00	00	00000000	0
127	7F	Checksum	61	01100001	97