



Product Specification

M270DAN01.0

AU OPTRONICS CORPORATION

() Preliminary Specification

(V) Final Specification

Module	27.0" Color TFT-LCD
Model Name	M270DAN01.0

Customer	Date
_____	_____
Approved by	
_____	_____
Note: This Specification is subject to change without notice.	

Approved by	Date
<u>Howard Lee</u>	_____
Prepared by	
<u>Shin Yu Lin</u>	<u>2013/4/16</u>
AU Optronics Corporation	



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Records of Revision

Version and Date	Page	Old description	New Description	Remark																																																																					
0.1 2012/09/20	All	First Version	N/A																																																																						
0.2 2012/09/20	6~7	1. The minimum of white luminance is 240nit 2. The typical of white luminance is 300nit 3. The module consumption is 31.26W 4. The Color / Chromaticity is TBD 5. The weight of module is TBD	1. The minumn of white luminance is 280 nit 2. The typical of white luminance is 350nit 3. The module consumption is 34.9W 4. The Color / Chromaticity is defined by Min/Tpy/Max 5. The weight of module is 2319g																																																																						
	12/ 28	-	Add second source of LVDS CNT1																																																																						
	13	LED forward Voltage variation maximum is 3.6V	LED forward Voltage variation maximum is 3.4V																																																																						
	15	-	Update power specifications <table><tr><th>Symbol</th><th>Description</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th><th>Conditions</th></tr><tr><td>VDD</td><td>Logic/LCD Drive Voltage</td><td>4.5</td><td>5.0</td><td>5.5</td><td>[Volt]</td><td>+/-10%</td></tr><tr><td rowspan="2">IDD1</td><td rowspan="2">Input Current</td><td>1.6</td><td>2.0</td><td></td><td>[A]</td><td>VDD= 5.0V, All White Pattern at 60 Hz</td></tr><tr><td>2.0</td><td>2.5</td><td></td><td>[A]</td><td>VDD= 5.0V, All White Pattern at 75 Hz</td></tr><tr><td rowspan="2">PDD1</td><td rowspan="2">VDD Power</td><td>8.0</td><td>10.0</td><td></td><td>[Watt]</td><td>VDD= 5.0V, All White Pattern at 60 Hz</td></tr><tr><td>10.0</td><td>12.5</td><td></td><td>[Watt]</td><td>VDD= 5.0V, All White Pattern at 75 Hz</td></tr><tr><td>IRush</td><td>Inrush Current</td><td></td><td></td><td>2.0</td><td>[A]</td><td>Note 1</td></tr><tr><td>VDDrip</td><td>Allowable Logic/LCD Drive Ripple Voltage</td><td></td><td></td><td>500</td><td>[mV] p-p</td><td>VDD= 5.0V, All White Pattern at 75 Hz</td></tr></table>	Symbol	Description	Min.	Typ.	Max.	Unit	Conditions	VDD	Logic/LCD Drive Voltage	4.5	5.0	5.5	[Volt]	+/-10%	IDD1	Input Current	1.6	2.0		[A]	VDD= 5.0V, All White Pattern at 60 Hz	2.0	2.5		[A]	VDD= 5.0V, All White Pattern at 75 Hz	PDD1	VDD Power	8.0	10.0		[Watt]	VDD= 5.0V, All White Pattern at 60 Hz	10.0	12.5		[Watt]	VDD= 5.0V, All White Pattern at 75 Hz	IRush	Inrush Current			2.0	[A]	Note 1	VDDrip	Allowable Logic/LCD Drive Ripple Voltage			500	[mV] p-p	VDD= 5.0V, All White Pattern at 75 Hz																		
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23/ 34	Old label position	Label position alteration																																																																							
33	-	Update mechanical drawing- add hook in gate IC side																																																																							
37	The weight of packing and shipment is TBD	To define weight of packing and shipment																																																																							
0.3 2013/01/6	27	1. The maker of module connector 2 is JAE. 2. The part no. of module connector 2 is FI-NXB40SLA-HF10	1. The maker of module connector 2 is STARCONN. 2. The part no. of module connector 2 is 115F40-R000RA-M3																																																																						
	22/38	Original pin assignment of module connector (CNT2)	New pin assignment of module connector (CNT2)																																																																						
	23/34	Original module back cover picture	New module back cover picture																																																																						
	26	The T6 of power ON/OFF sequence is 100 ms	The T6 of power ON/OFF sequence is 150 ms																																																																						



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0.4 2013/02/04	23/34	Original module back cover picture	New module back cover picture	
	28/33	Original module connector 1 information	New module connector 1 information	
0.5 2013/3/20	19~23 / 25	<ol style="list-style-type: none">1. The original relationship between LVDS 4 ports input signal is dual screen.2. The original naming of input signal are RFO_XX/ RBO_XX/ RFE_XX/ RBE_XX3. The original naming of signal pair are RFO/ RFE/ RBO/ RBE	<ol style="list-style-type: none">1. The new relationship between LVDS 4 ports input signal is single screen2. The new naming of input signal are RX_XX/ RX_XX3. The new naming of signal pair are port 1/ port 2/ port 3/ port 4	
	23/34	NA	Add shipping label mark line.	
0.6 2013/4/16	34	Original size and appearance of BS-ITO tape	New size and appearance of BS-ITO tape	

1 Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of LED light bar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Avoid touching COF position while doing mechanical design.
- 14) Avoid stressing front bezel position when doing mechanical design
- 15) While storing modules as spares for a long time, the following precautions are necessary:
 - Store modules in a dark place. Do not expose them to sunlight or fluorescent light.
 - Keep the temperature between 5°C and 35°C at normal humidity.

2 General Description

This specification applies to the 27 inch-QHD color a-Si TFT-LCD Module M270DAN01.0. The display supports the QHD - 2560(H) x 1440(V) screen format and 1.07B colors (RGB 8-bit +FRC data). The light source of this TFT-LCD module is W-LED. All input signals are 4-channel LVDS interface and this module doesn't contain a driver for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25°C condition:

Items	Unit	Specification
Screen Diagonal	[mm]	684.7 (27.0")
Active Area	[mm]	596.7 (H) x 335.6 (V)
Pixels H x V		2560(x3) x 1440
Pixel Pitch	[um]	233.1 (per one triad) ×233.1
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally Black
White Luminance (Center)	[cd/m2]	350 cd/m2 (Typ.)
Contrast Ratio		1000 (Typ.)
Optical Response Time	[msec]	12ms (Typ., G/G)
Nominal Input Voltage VDD	[Volt]	+ 5.0 V
Power Consumption (VDD line + LED line)	[Watt]	34.9 W (typ) VDD line : PDD (typ), All white pattern at 60Hz = 8.0W LED line : PBLU (typ) = 26.9 W
Weight	[g]	2319
Physical Size	[mm]	630.0 (W) x 368.2 (H) x 10.6(D) (Typ.)
Electrical Interface		4 channel LVDS
Support Color		1.07B colors (RGB 8-bit + FRC data)
Surface Treatment		Anti-Glare, 3H
Temperature Range Operating Storage (Shipping)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance
TCO Compliance		TCO 6.0 Compliance

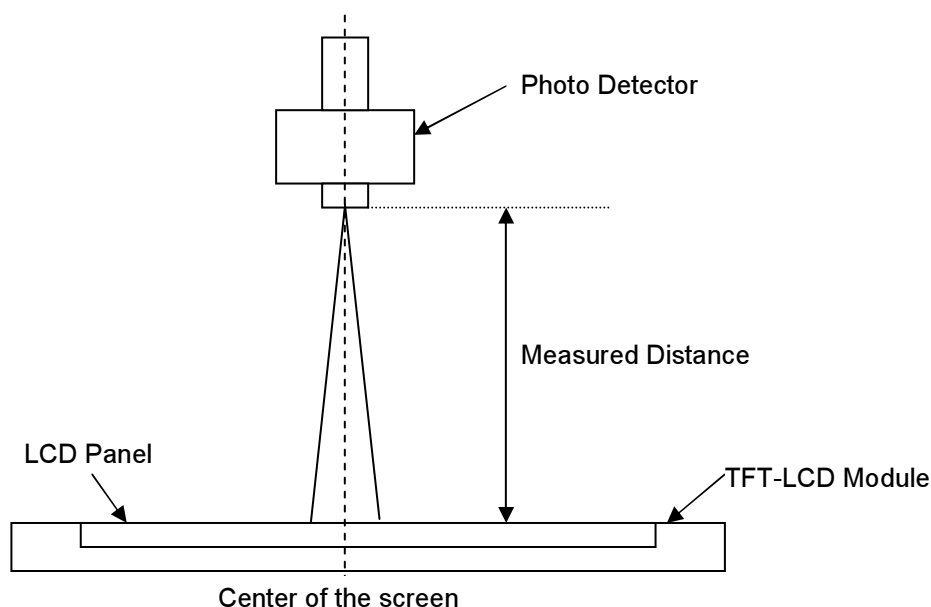
2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C:

Item	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing Angle	[degree]	Horizontal (Right)	75	89	-	2
		CR = 10 (Left)	75	89	-	
		Vertical (Up)	75	89	-	
		CR = 10 (Down)	75	89	-	
Contrast Ratio		Normal Direction	600	1000	-	3
Response Time	[msec]	Gray to Gray	-	12	-	4
Color / Chromaticity Coordinates (CIE)		Red x	0.630	0.660	0.690	5
		Red y	0.302	0.332	0.362	
		Green x	0.270	0.300	0.330	
		Green y	0.599	0.629	0.659	
		Blue x	0.117	0.147	0.177	
		Blue y	0.022	0.052	0.082	
Color Coordinates (CIE) White		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	
Central Luminance	[cd/m2]		280	350	-	6
Luminance Uniformity	[%]		75	80	-	7
Crosstalk (in 60Hz)	[%]				1.5	8
Flicker	dB				-20	9

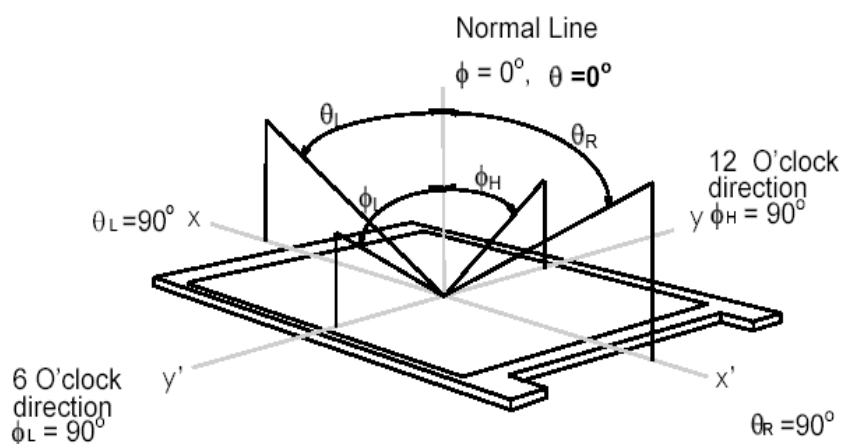
Note 1: Measurement Method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring (at surface 35°C). In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 2: Definition of Viewing Angle measured by ELDIM (EZContrast 88)

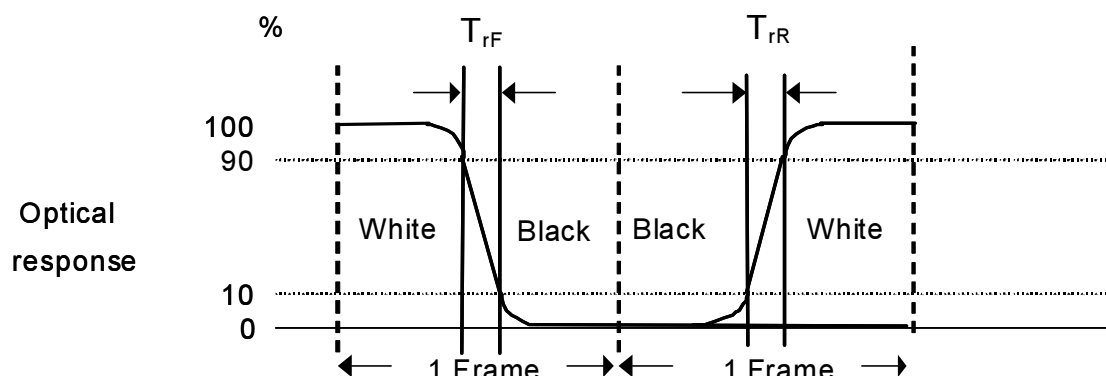
Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (ϕ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



Note 3: Contrast Ratio measured by TOPCON SR-3

Note 4: Definition of Response time measured by Westar TRD-100A

The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time, T_{rR}), and from “Full White” to “Full Black” (falling time, T_{rF}), respectively. The response time is interval between the 10% and 90% (1 frame at 60 Hz) of amplitudes.



The gray to gray response time is defined as the following table. The algorithm is $| \text{Gray Level A} - \text{Gray Level B} | \geq 256$.

Gray Level to Gray Level		Falling Time				
		G0	G255	G511	G767	G1023
Rising Time	G0					
	G255					
	G511					
	G767					
	G1023					

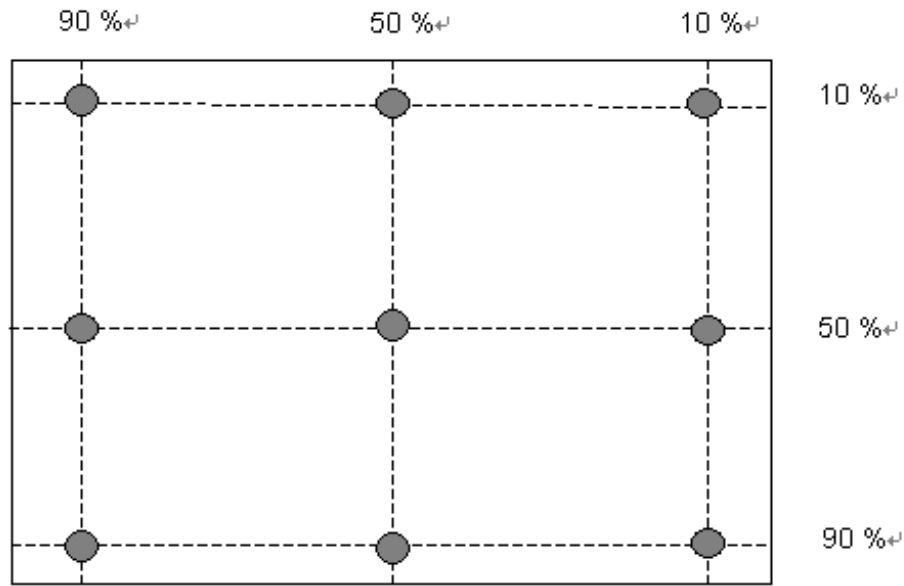
■ T_{GTG_typ} is the total average time at rising time and falling time of gray to gray.

■ T_{GTG_max} is the maximum time at rising time or falling time of gray to gray.

Note 5: Color Chromaticity and Coordinates (CIE) measured by TOPCON SR-3

Note 6: Central Luminance measured by TOPCON SR-3

Note 7: Luminance Uniformity of these 9 points defined as below and measured by TOPCON SR-3



$$\text{Uniformity} = \frac{\text{Minimum Luminance in 9 points (1 - 9)}}{\text{Maximum Luminance in 9 Points (1 - 9)}}$$

Note 8: Crosstalk defined as below and measured by TOPCON SR-3

$$\text{CT} = |Y_B - Y_A| / Y_A \times 100 (\%)$$

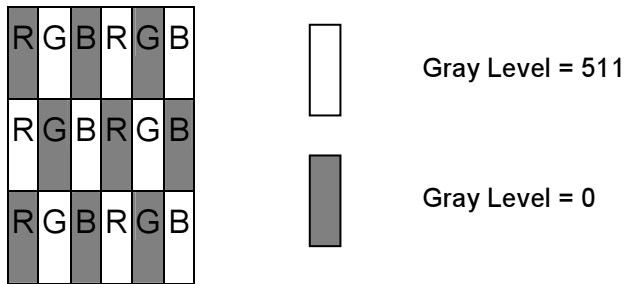
Where

Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

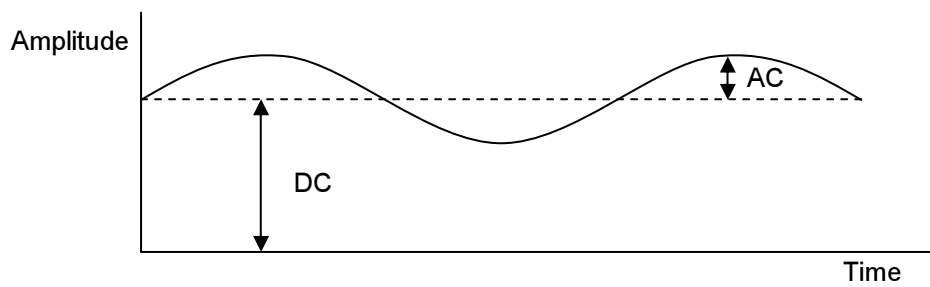
Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



Note 9: Test Pattern Sub-checker Pattern measured by TOPCON SR-3



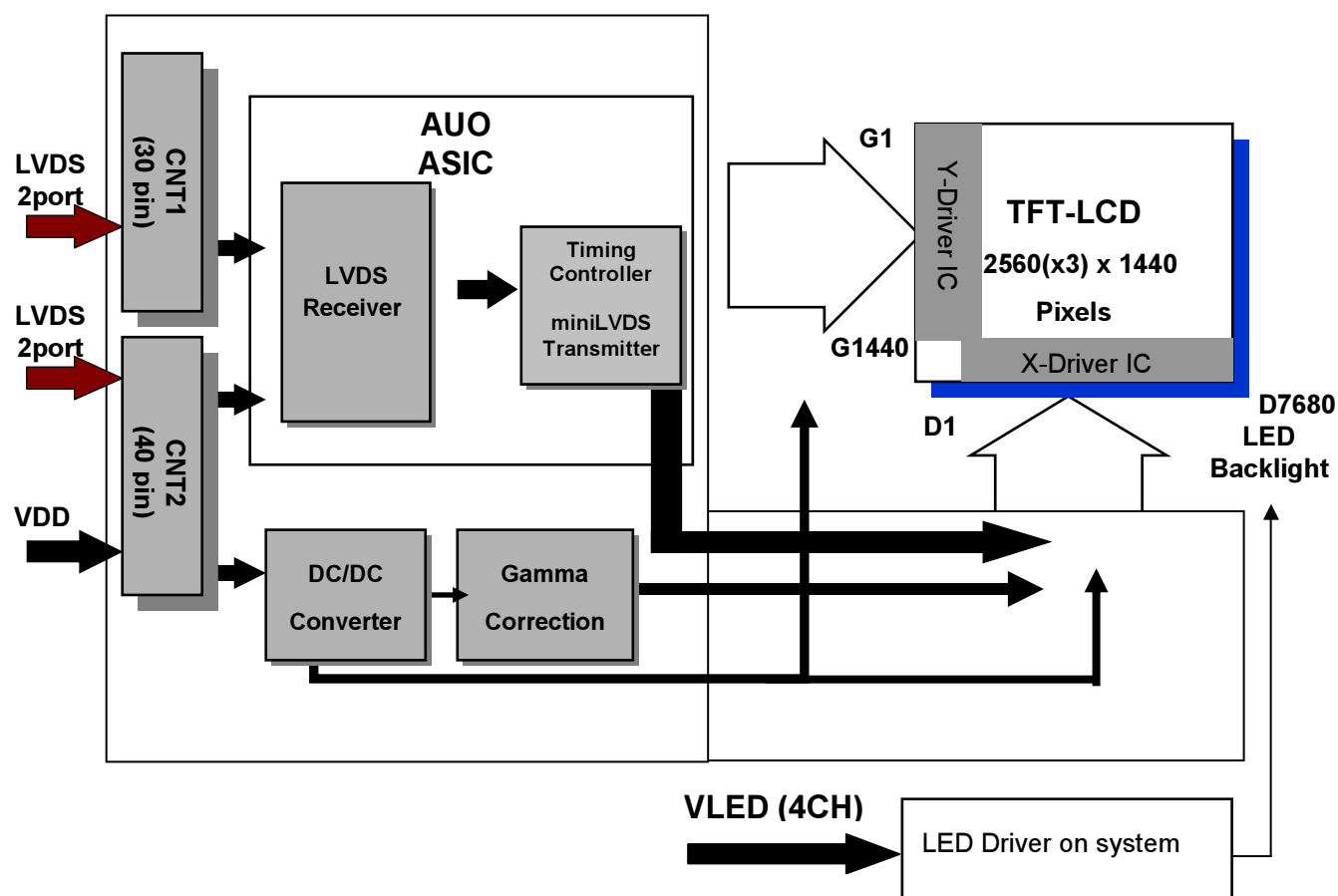
Method: Record dBV & DC value with TRD-100



$$\text{Flicker (dB)} = 20 \log \frac{\text{AC Level(at 30 Hz)}}{\text{DC Level}}$$

3 Functional Block Diagram

The following diagram shows the functional block of the 27.0 inch Color TFT-LCD Module:



4 Absolute Maximum Ratings

Absolute maximum ratings of the module are listed as follows:

4.1 TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	VDD	-0.3	6.0	[Volt]	Note 1, 2

4.2 Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
LED Forward Current	IRLED1	0	150	[mA]	Note 1,2,5 100% duty
	IRLED2				
	IRLED3				
	IRLED4				
LED Pulse Forward Current	IPLD1	-	300	[mA]	Note 1,2,5 10% duty @100Hz
	IPLD2				
	IPLD3				
	IPLD4				
LED forward Voltage variation (per string variation)	ΔV_f	-	3.4	[Volt]	Note 1,2

4.3 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Glass Surface Temperature (Operation)	TGS	0	+65	[°C]	Note3 Note4
Operation Humidity	HOP	5	90	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	
Storage Humidity	HST	5	90	[%RH]	

Note 1: With in Ta (25 °C)

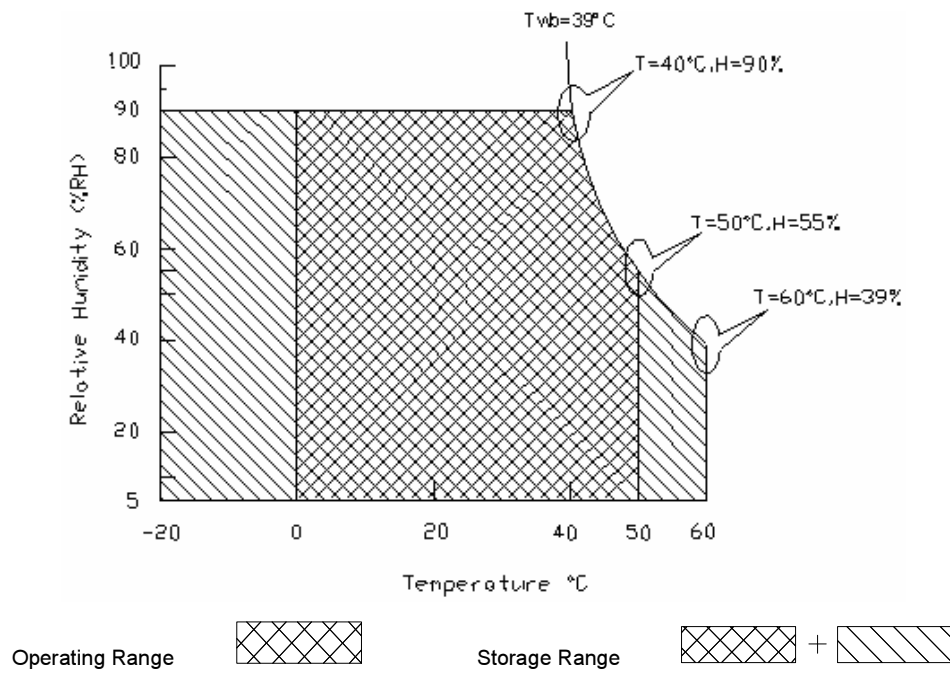
Note 2: Permanent damage to the device may occur if exceeding maximum values

Note 3: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max (Ta ≤ 39°C)
2. Max wet-bulb temperature at 39°C or less. (Ta ≤ 39°C)
3. No condensation

Note 4: Function Judged only

Note 5: IRLED1,2,3,4 and IPLD1,2,3,4 define as per strings LED current.



5 Electrical Characteristics

5.1 TFT LCD Module

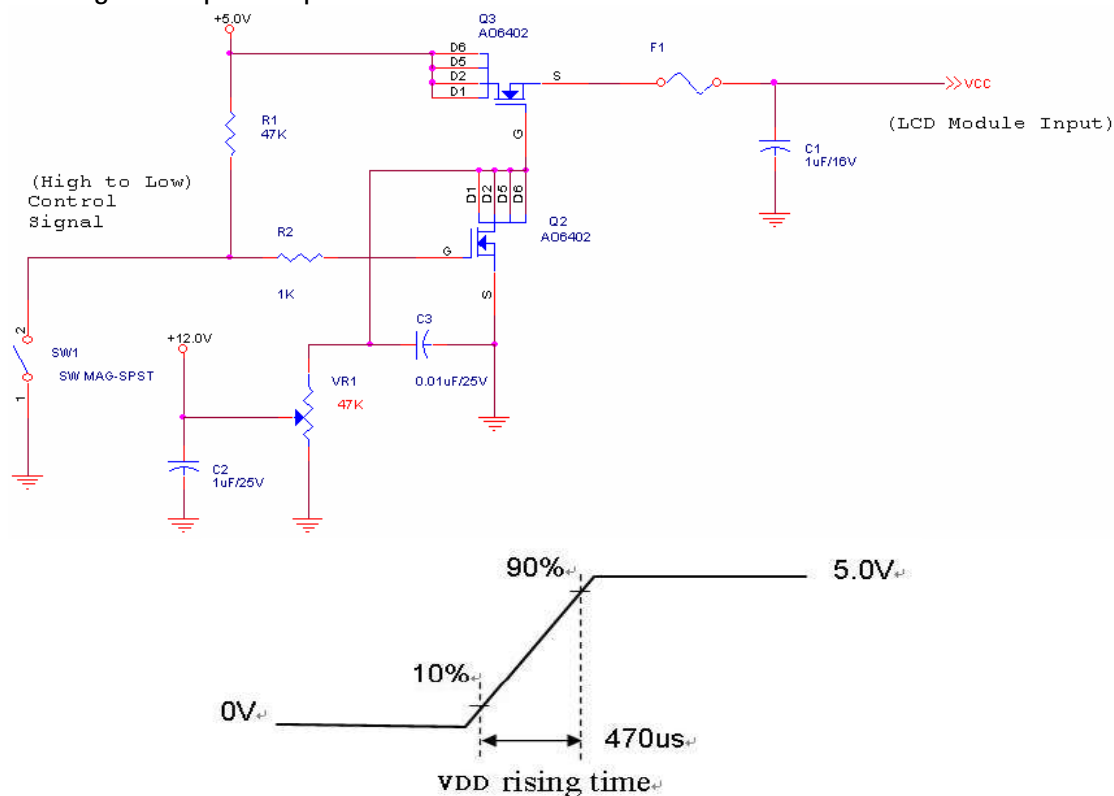
5.1.1 Power Specification

Input power specifications are listed as follows:

Symbol	Description	Min	Typ.	Max	Unit	Conditions
VDD	Logic/LCD Drive Voltage	4.5	5.0	5.5	[Volt]	+/-10%
IDD1	Input Current	-	1.6	2.0	[A]	VDD= 5.0V, All White Pattern at 60 Hz
		-	2.0	2.5	[A]	VDD= 5.0V, All White Pattern at 75 Hz
PDD1	VDD Power	-	8.0	10.0	[Watt]	VDD= 5.0V, All White Pattern at 60 Hz
		-	10.0	12.5	[Watt]	VDD= 5.0V, All White Pattern at 75 Hz
IRush	Inrush Current	-	-	2.0	[A]	Note 1
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	500	[mV] p-p	VDD= 5.0V, All White Pattern at 75 Hz

Note 1: Measurement Conditions:

The duration of rising time of power input is 470 us.



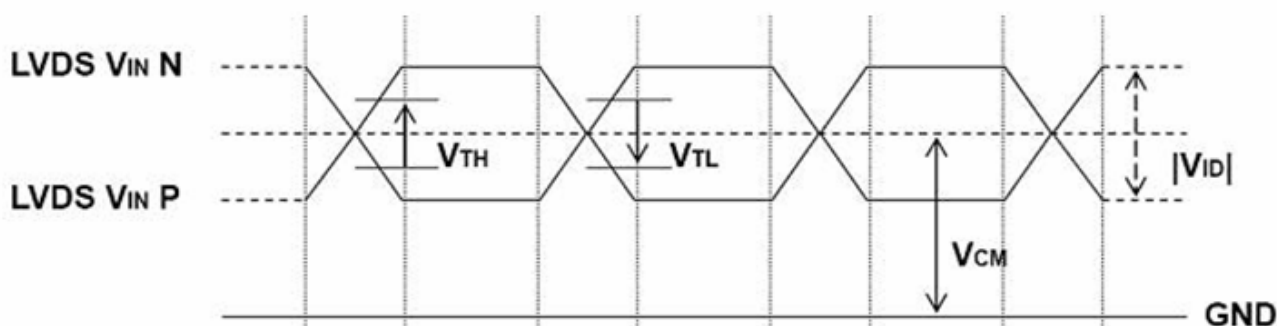
5.1.2 Signal Electrical Characteristics

(1) DC Characteristics of each signal are as following:

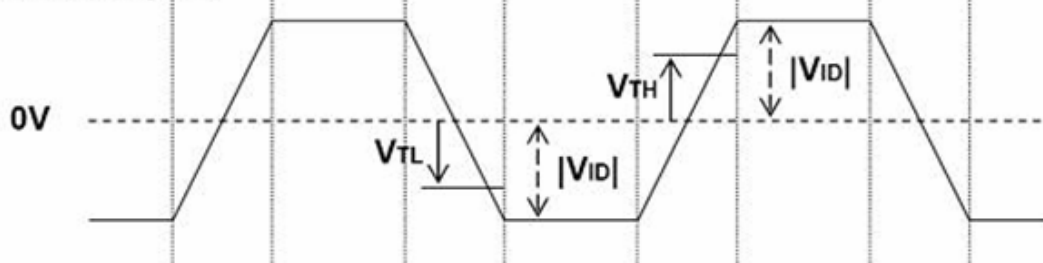
Symbol	Description	Min	Typ	Max	Units	Conditions
V_{TH}	Differential Input High Threshold	-	-	+100	[mV]	$V_{CM} = 1.2V$ Note 1
V_{TL}	Differential Input Low Threshold	-100	-	-	[mV]	$V_{CM} = 1.2V$ Note 1
$ V_{ID} $	Input Differential Voltage	100	-	600	[mV]	Note 1
V_{CM}	Differential Input Common Mode Voltage	+1.0	+1.2	+1.5	[V]	$V_{TH}-V_{TL} = 200mV$ (max) Note 1

Note 1: LVDS Signal Waveform

Single-End

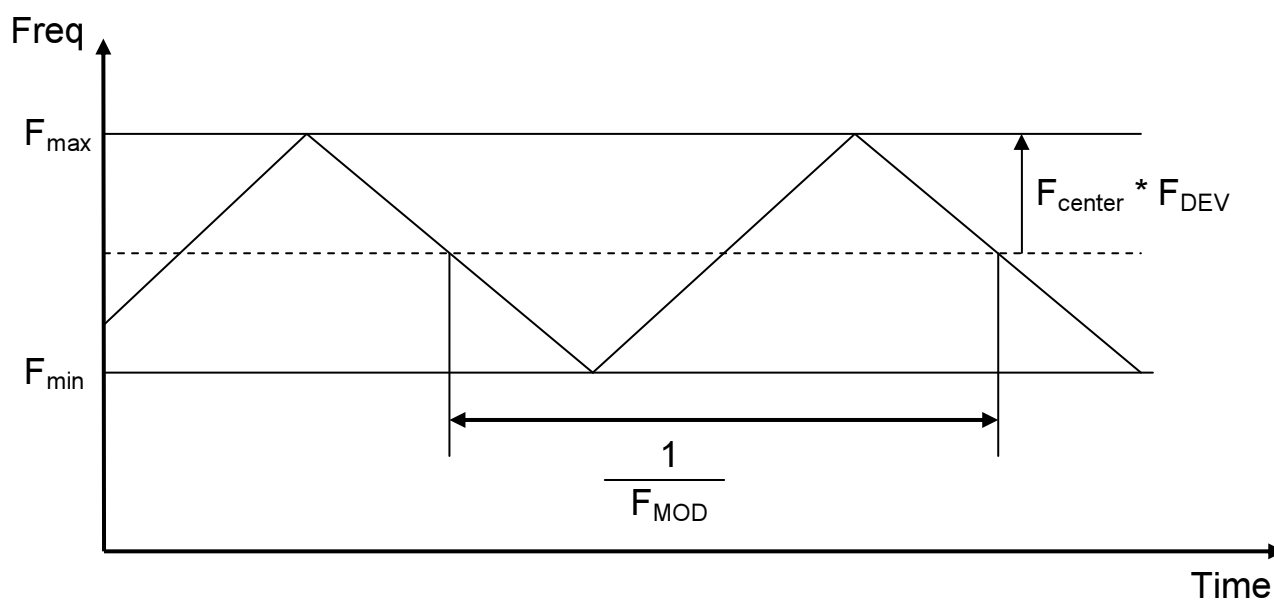


Differential Signal



(2) AC Characteristics

Symbol	Description	Min	Max	Units	Conditions
F_{DEV}	Maximum deviation of input clock frequency during SSC	-	± 3	%	
F_{MOD}	Maximum modulation frequency of input clock during SSC	-	200	KHz	



< Spread Spectrum >

5.2 Backlight Unit

Parameter guideline for LED driving is under stable conditions at 25 °C (Room Temperature):

Symbol	Description	Min.□	Typ.	Max.	Unit	Note
IRLED	LED Operation Current	-	120.0	130.0	[mA]	Note 1
VLB	Light Bar Operation Voltage (for reference)	50.0	56.1	61.2	[Volt]	Note 2
PBLU	BLU Power Consumption (for reference)	-	26.9	31.8	[Watt]	Note 3
LTLED	LED Life Time (Typical)	30,000	-	-	[Hour]	Note 4

Each module consists of 68 pcs LED (4 strings x 17 pcs / string)

Note 1: The specified current is 100% duty of LED chip input current, IRLED1,2,3,4 define as per strings LED current.

Note 2: The value showed is one string operation voltage.

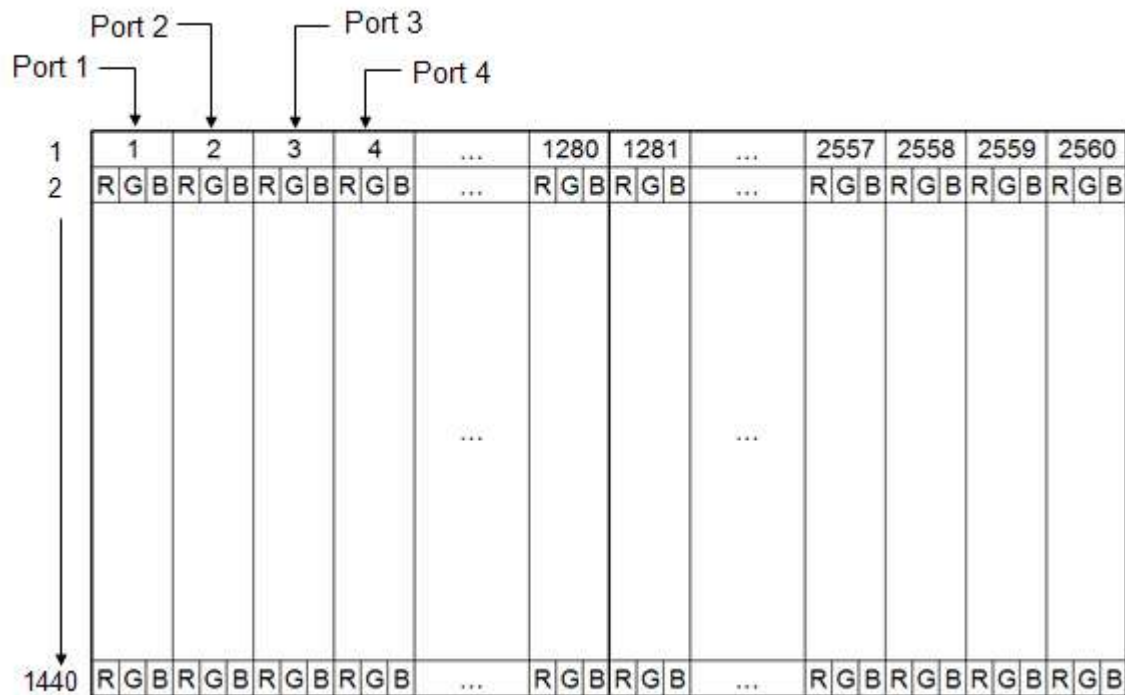
Note 3: $PBLU = VLB * (IRLED1 + IRLED2 + IRLED3 + IRLED4)$

Note 4: Definition of life time: Brightness becomes to 50% of its original value. The minimum life time of LED unit is on the condition of IRLED = 120mA and 25±2°C (Room Temperature).

6 Signal Characteristics

6.1 Pixel Format Definition

Following figure shows the relationship between the input signals and LCD pixel format.



Note 1: The module use 4port-LVDS interface.

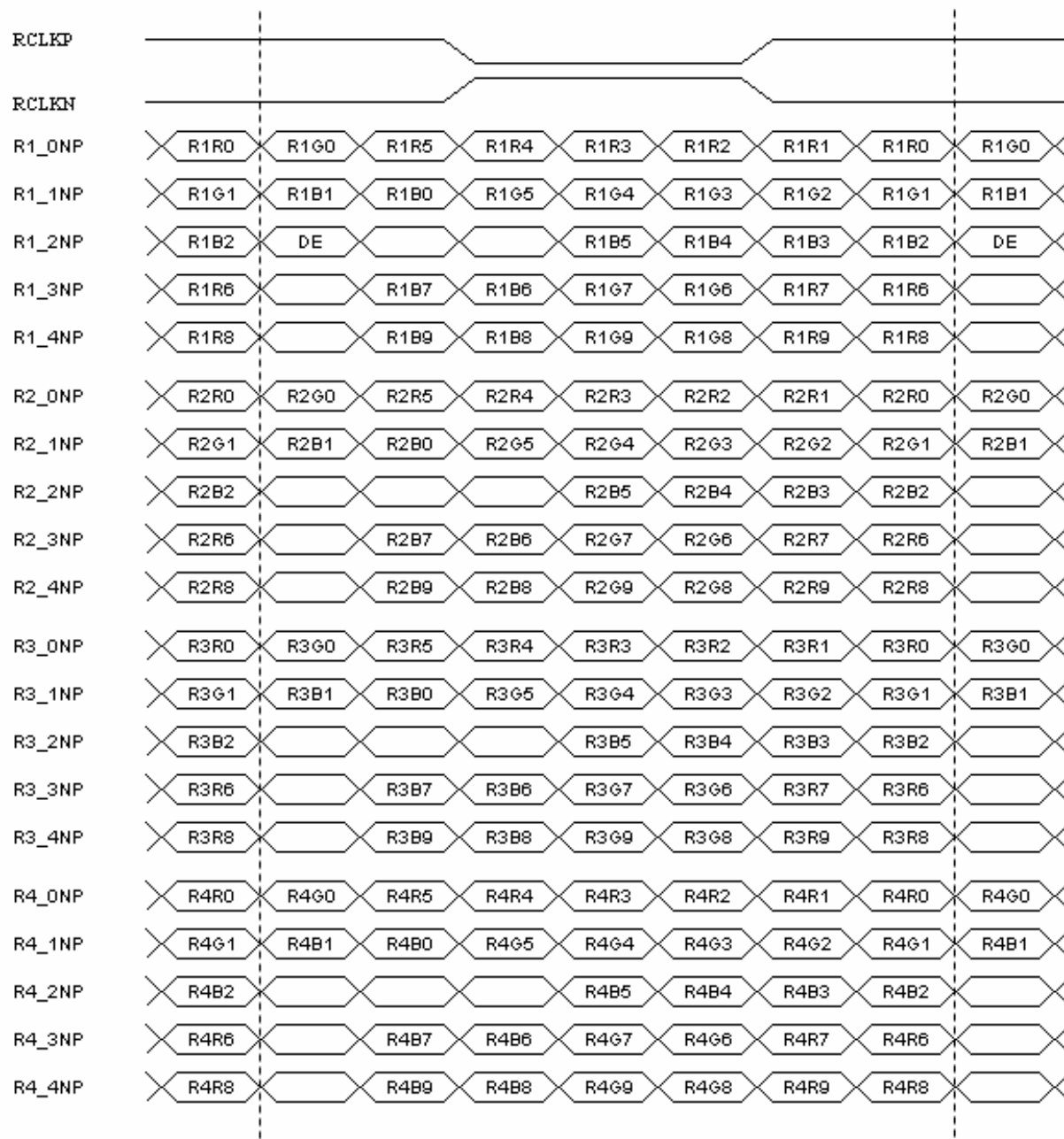
Port 1 : 1, 5.....→2557pixel

Port 2 : 2, 6.....→2558pixel

Port 3 : 3, 7.....→2559 pixel

Port 4 : 4, 8.....→2560 pixel

6.2 Input Data Format Definition



LVDS Data Mapping of NS Format for Quad Channel

6.3 Signal Description

The module using 30/40 pin 4port-LVDS interface. LVDS is a differential signal technology for LCD interface and high speed data transfer device.

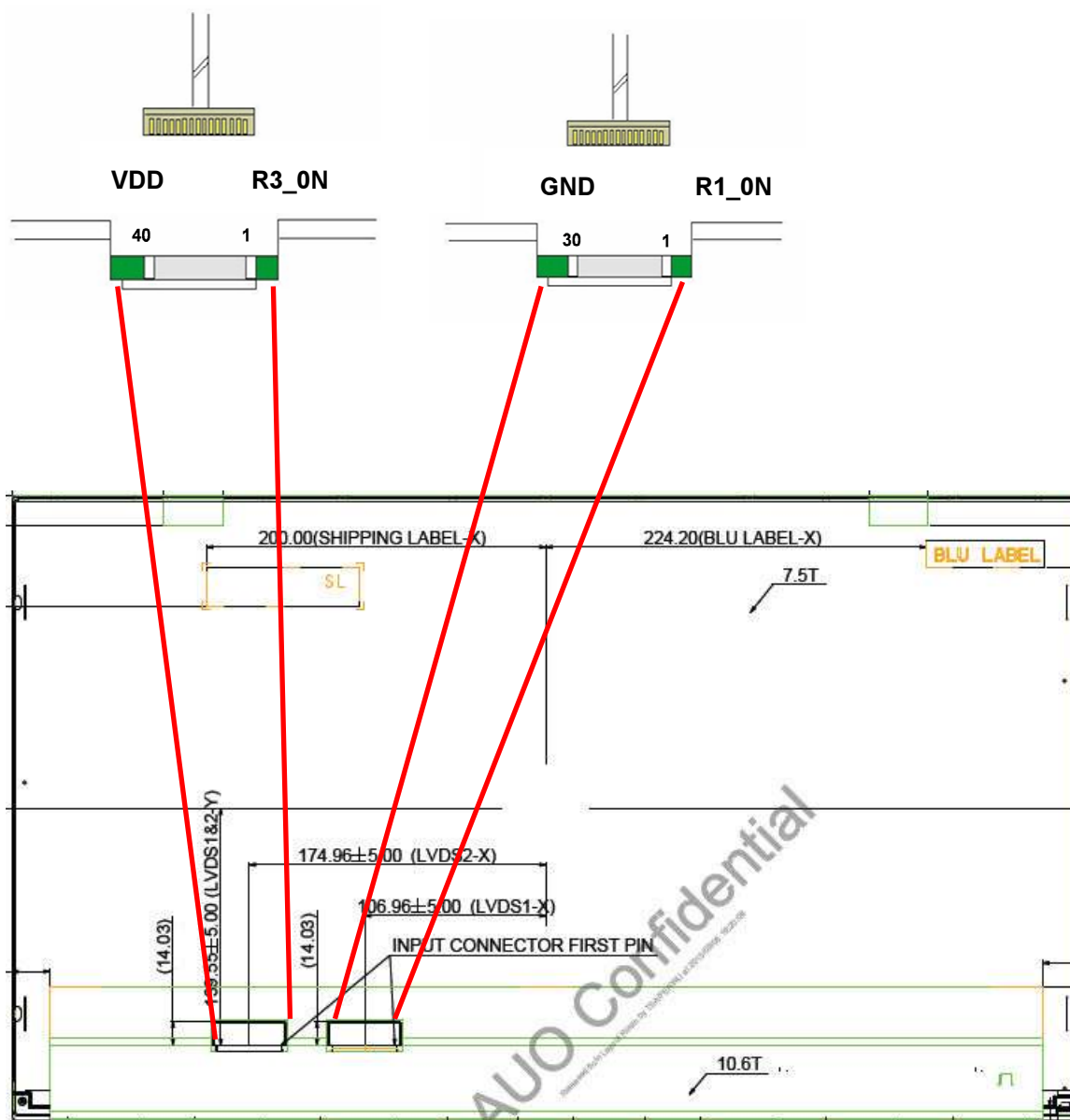
Module Connector - CNT1

PIN #	Signal Name	Description	Function
1	R1_0N	FIRST_ Negative LVDS differential data input	LVDS port 1
2	R1_0P	FIRST_ Positive LVDS differential data input	
3	R1_1N	FIRST_ Negative LVDS differential data input	
4	R1_1P	FIRST_ Positive LVDS differential data input	
5	R1_2N	FIRST_ Negative LVDS differential data input	
6	R1_2P	FIRST_ Positive LVDS differential data input	
7	GND	Power Ground	
8	R1_CLKN	FIRST_ Negative LVDS differential clock input	
9	R1_CLKP	FIRST_ Positive LVDS differential clock input	
10	GND	Power Ground	
11	R1_3N	FIRST_ Negative LVDS differential data input	
12	R1_3P	FIRST_ Positive LVDS differential data input	
13	R1_4N	FIRST_ Negative LVDS differential data input	
14	R1_4P	FIRST_ Positive LVDS differential data input	
15	GND	Power Ground	
16	R2_0N	SECOND_ Negative LVDS differential data input	LVDS port 2
17	R2_0P	SECOND_ Positive LVDS differential data input	
18	R2_1N	SECOND_ Negative LVDS differential data input	
19	R2_1P	SECOND_ Positive LVDS differential data input	
20	R2_2N	SECOND_ Negative LVDS differential data input	
21	R2_2P	SECOND_ Positive LVDS differential data input	
22	GND	Power Ground	
23	R2_CLKN	SECOND_ Negative LVDS differential clock input	
24	R2_CLKP	SECOND_ Positive LVDS differential clock input	
25	GND	Power Ground	
26	R2_3N	SECOND_ Negative LVDS differential data input	
27	R2_3P	SECOND_ Positive LVDS differential data input	
28	R2_4N	SECOND_ Negative LVDS differential data input	
29	R2_4P	SECOND_ Positive LVDS differential data input	
30	GND	Power Ground	



Module Connector - CNT2

PIN #	Signal Name	Description	Function
1	R3_0N	THIRD_ Negative LVDS differential data input	LVDS port 3
2	R3_0P	THIRD_ Positive LVDS differential data input	
3	R3_1N	THIRD_ Negative LVDS differential data input	
4	R3_1P	THIRD_ Positive LVDS differential data input	
5	R3_2N	THIRD_ Negative LVDS differential data input	
6	R3_2P	THIRD_ Positive LVDS differential data input	
7	GND	Power Ground	
8	R3_CLKN	THIRD_ Negative LVDS differential clock input	
9	R3_CLKP	THIRD_ Positive LVDS differential clock input	
10	GND	Power Ground	
11	R3_3N	THIRD_ Negative LVDS differential data input	
12	R3_3P	THIRD_ Positive LVDS differential data input	
13	R3_4N	THIRD_ Negative LVDS differential data input	
14	R3_4P	THIRD_ Positive LVDS differential data input	
15	GND	Power Ground	
16	R4_0N	FOURTH_ Negative LVDS differential data input	LVDS port 4
17	R4_0P	FOURTH_ Positive LVDS differential data input	
18	R4_1N	FOURTH_ Negative LVDS differential data input	
19	R4_1P	FOURTH_ Positive LVDS differential data input	
20	R4_2N	FOURTH_ Negative LVDS differential data input	
21	R4_2P	FOURTH_ Positive LVDS differential data input	
22	GND	Power Ground	
23	R4_CLKN	FOURTH_ Negative LVDS differential clock input	
24	R4_CLKP	FOURTH_ Positive LVDS differential clock input	
25	GND	Power Ground	
26	R4_3N	FOURTH_ Negative LVDS differential data input	
27	R4_3P	FOURTH_ Positive LVDS differential data input	
28	R4_4N	FOURTH_ Negative LVDS differential data input	
29	R4_4P	FOURTH_ Positive LVDS differential data input	
30	GND	Power Ground	
31	NC	No connection (for AUO test only. Do not connect)	NC
32	NC	No connection (for AUO test only. Do not connect)	
33	GND	Power Ground	Power
34	GND	Power Ground	
35	GND	Power Ground	
36	VDD	Power +5V	
37	VDD	Power +5V	
38	VDD	Power +5V	
39	VDD	Power +5V	
40	VDD	Power +5V	



Note 1: Input signals of port 1 to port 4 clocks shall be the same timing.

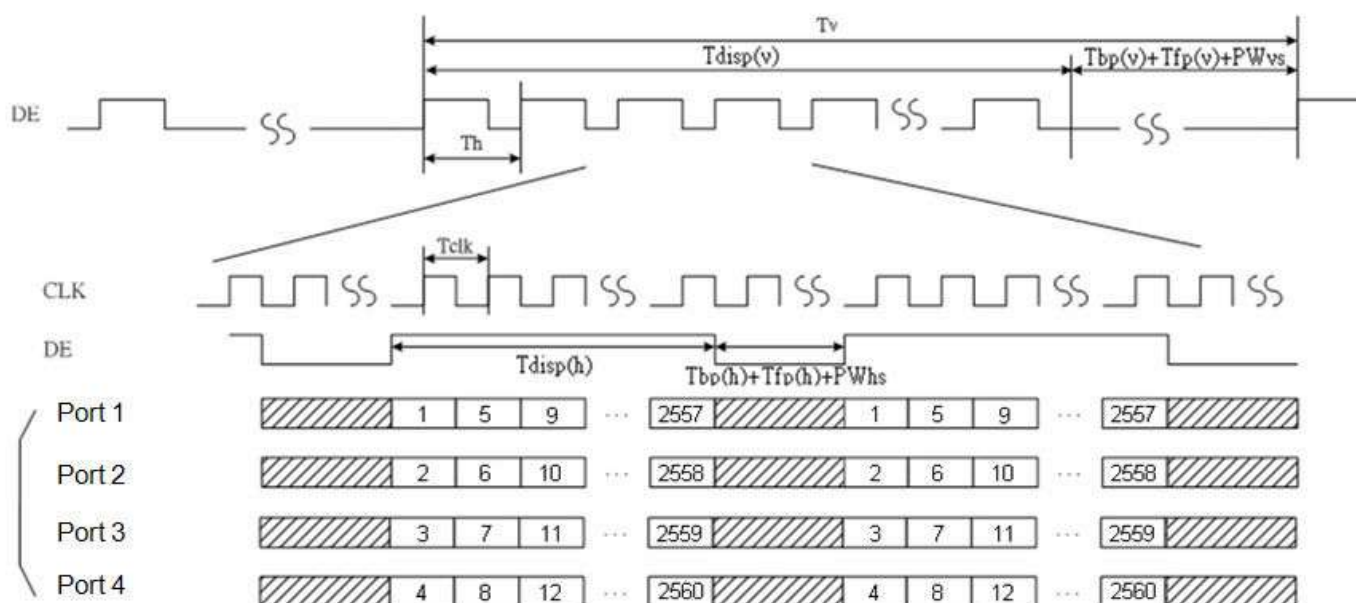
6.4 Timing Characteristics

The input signal timing specifications are shown as the following table

Signal	Item	Symbol	Min	Typ	Max	Unit
Vertical Section	Period	Tv	1479	1481	1483	Th
	Active	Tdisp(v)	1440	1440	1440	Th
	Blanking	Tbp(v)+Tfp(v)+PWvs	39	41	43	Th
Horizontal Section	Period	Th	676	680	684	Tclk
	Active	Tdisp(h)	640	640	640	Tclk
	Blanking	Tbp(h)+Tfp(h)+PWhs	36	40	44	Tclk
Clock	Period	Tclk	22.22	16.56	13.16	ns
	Frequency	Freq	45	60.4	76	MHz
Frame rate	Frame rate	F	50	60	75	Hz
Hsync Frequency	Hsync Frequency	HFreq	73.9	88.8	111.2	KHz

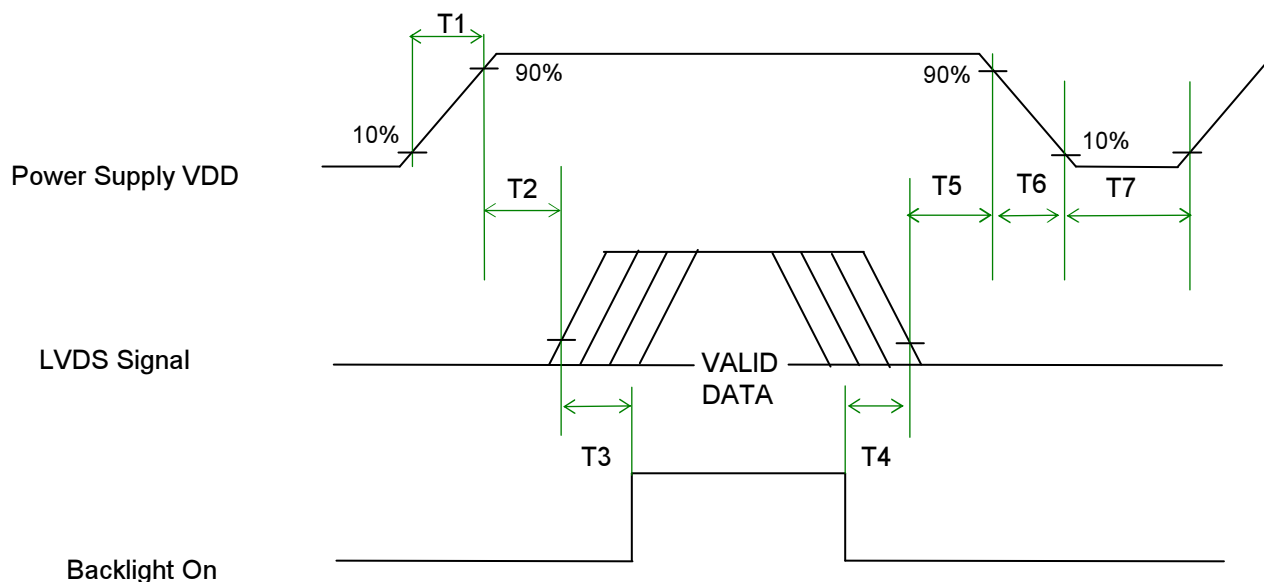
Note 1: DE mode only

6.5 Timing Diagram



6.6 Power ON/OFF Sequence

VDD power and lamp on/off sequence are as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state when VDD is off.



Power Sequence Timing

Parameter	Value			Unit
	Min.	Typ.	Max.	
T1	0.5	-	10	[ms]
T2	0	-	50	[ms]
T3	500	-	-	[ms]
T4	100	-	-	[ms]
T5	0	-	50	[ms] Note1,2
T6	5	-	150	[ms] Note1,2
T7	1000	-	-	[ms]

Note1 : Recommend setting T5 = 0ms to avoid electronic noise when VDD is off.

Note2 : During T5 and T6 period , please keep the level of input LVDS signals with Hi-Z state.

7 Connector and Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	Interface Connector / Interface Card
Manufacturer	CNT1: STM/ P-TOW/ STARCONN CNT2: STARCONN
Type Part Number	CNT1: STM_MSCKT2407P30HB P-TOW_AL230F-A0G1D-P STARCONN_093G30-02001A-M4 CNT2: STARCONN_115F40-R000RA-M3
Mating Housing Part Number	CNT1: JAE_FI-X30HL STM_PK2407P30V CNT2: FI-NX40HL

7.1.1 Pin Assignment

Module Connector - CNT1

Pin#	Signal Name	Pin#	Signal Name
1	R1_0N	2	R1_0P
3	R1_1N	4	R1_1P
5	R1_2N	6	R1_2P
7	GND	8	R1_CLKN
9	R1_CLKP	10	GND
11	R1_3N	12	R1_3P
13	R1_4N	14	R1_4P
15	GND	16	R2_0N
17	R2_0P	18	R2_1N
19	R2_1P	20	R2_2N
21	R2_2P	22	GND
23	R2_CLKN	24	R2_CLKP
25	GND	26	R2_3N
27	R2_3P	28	R2_4N
29	R2_4P	30	GND



Module Connector - CNT2

Pin#	Signal Name	Pin#	Signal Name
1	R3_0N	2	R3_0P
3	R3_1N	4	R3_1P
5	R3_2N	6	R3_2P
7	GND	8	R3_CLKN
9	R3_CLKP	10	GND
11	R3_3N	12	R3_3P
13	R3_4N	14	R3_4P
15	GND	16	R4_0N
17	R4_0P	18	R4_1N
19	R4_1P	20	R4_2N
21	R4_2P	22	GND
23	R4_CLKN	24	R4_CLKP
25	GND	26	R4_3N
27	R4_3P	28	R4_4N
29	R4_4P	30	GND
31	NC	32	NC
33	GND	34	GND
35	GND	36	VDD
37	VDD	38	VDD
39	VDD	40	VDD

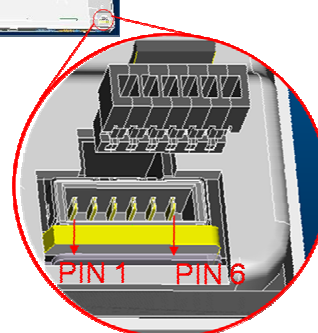
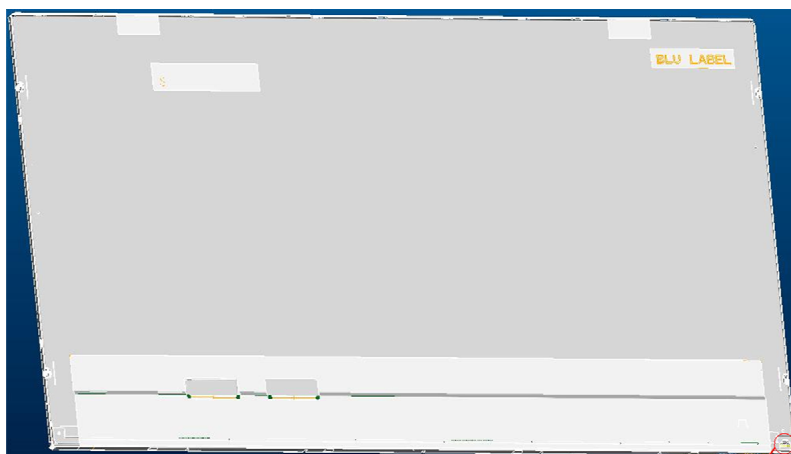
7.2 LED Connector on Backlight Unit

This connector is mounted on LED light bar.

Connector Name / Designation	Light Bar Connector
Manufacturer	E&T(ENTERY)
Type Part Number	3707K-S06N-21R
Mating Housing Part Number	H112K-P06N-13B (Locked Type)

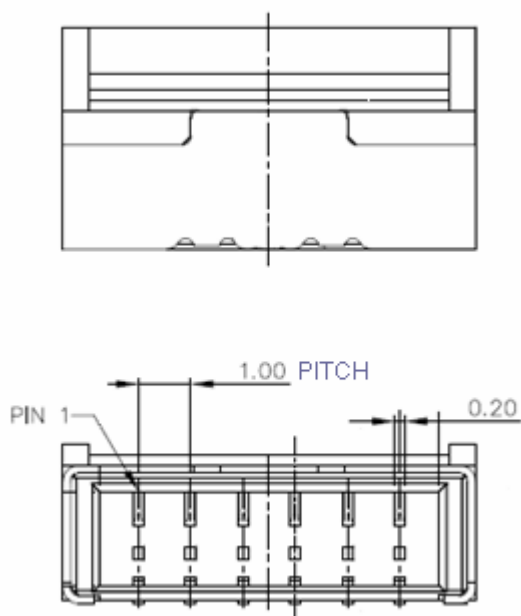
7.2.1 LED Pin assignment

Pin#	Signal Name
1	IRLED1 (current out)
2	IRLED2 (current out)
3	VLED (voltage in)
4	VLED (voltage in)
5	IRLED3 (current out)
6	IRLED4 (current out)

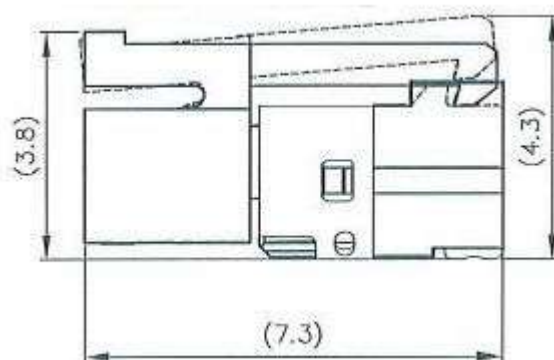
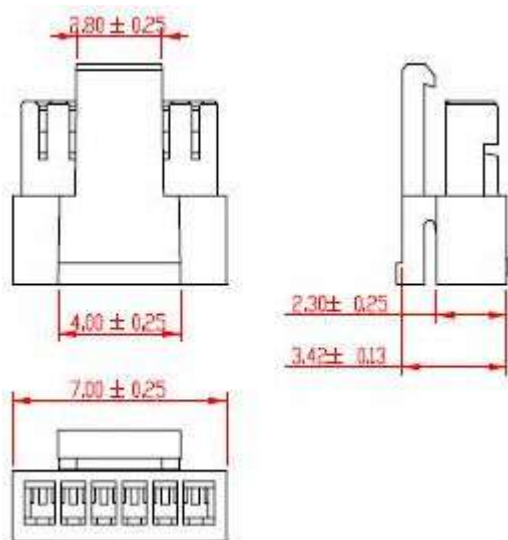


7.2.2 LED Connector Dimension

$H \times V \times D = 13.9 \times 3.00 \times 4.25$, Pitch = 1.0 (unit = mm)



7.2.3 LED Mating housing dimension



8 Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50°C, 80%RH, 300 hours	
High Temperature Operation (HTO)	Ta= 50°C, 50%RH, 300 hours	
Low Temperature Operation (LTO)	Ta= 0°C, 300 hours	
High Temperature Storage (HTS)	Ta= 60°C, 300 hours	
Low Temperature Storage (LTS)	Ta= -20°C, 300 hours	
Vibration Test (Non-operation)	Acceleration: 1.5 Grms Wave: Random Frequency: 10 - 200 Hz Duration: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: $\pm X$, $\pm Y$, $\pm Z$ (one time for each Axis)	
Drop Test	Height: 46 cm, package test	
Thermal Shock Test (TST)	-20°C/30min, 60°C/30min, 100 cycles	Note 1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: $\pm 8KV$, 150pF(330 Ω) 1sec, 15 points, 25 times/ point	Note 2
	Air Discharge: $\pm 15KV$, 150pF(330 Ω) 1sec 15 points, 25 times/ point	
Altitude Test	Operation: 18,000 ft Non-Operation: 40,000 ft	

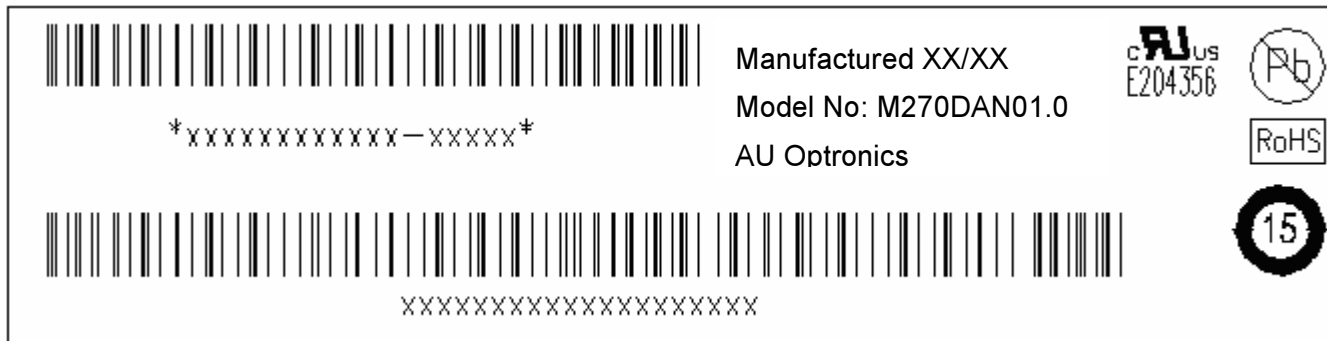
Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: EN61000-4-2, ESD class B: Certain performance degradation allowed:

- No data lost
- Self-recoverable
- No hardware failures

9 Shipping Label

The label on the panel is shown as below:



Note 1: For Pb Free products, AUO will add  for identification.

Note 2: For RoHS compatible products, AUO will add  for identification.

Note 3: For China RoHS compatible products, AUO will add  for identification.

Note 4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

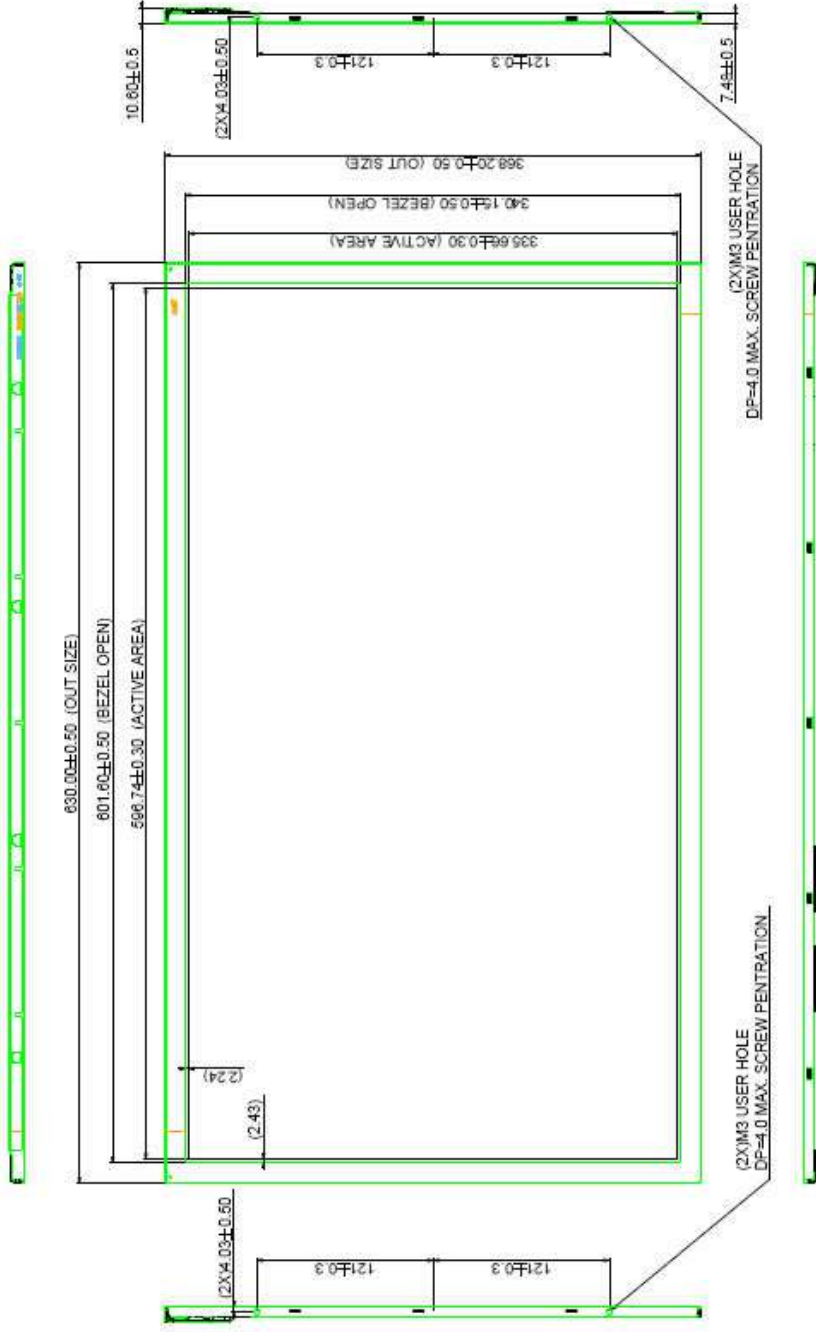


Product Specification

M270DAN01.0

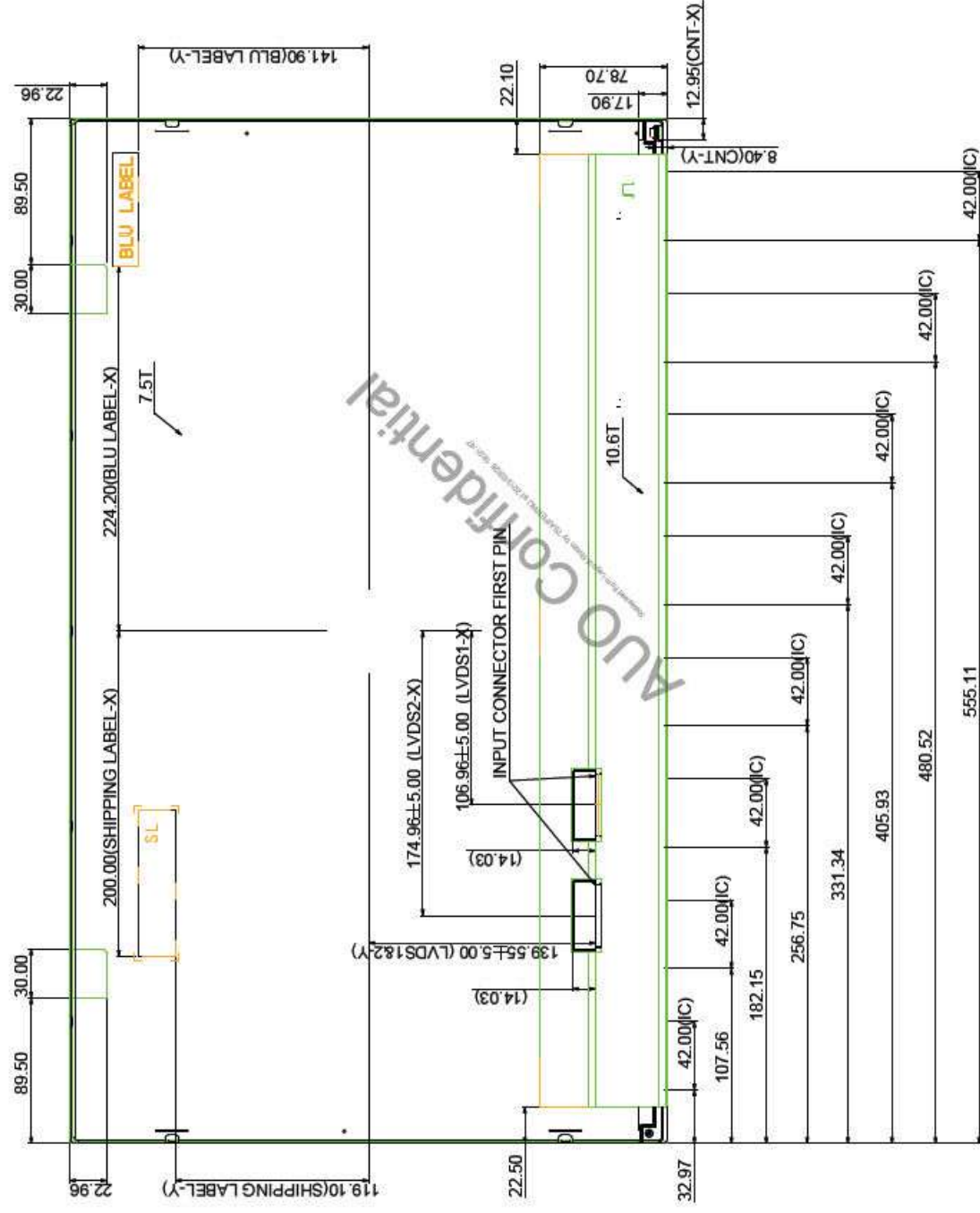
AU OPTRONICS CORPORATION

10 Mechanical Characteristics



- NOTE:
1. TOLERANCE WITHOUT NOTICED TO BE ± 0.5 MM.
 2. THE DIMENSION EXCLUDES DEFORMATION.
 3. BACKLIGHTED LIGHT-BAR.
 4. MODULE THICKNESS TO BE 11.1MM MAX.
 5. LVDS CONNECTOR 1 TO BE STM MSCKT2407P30HB.
 6. LVDS CONNECTOR 2 TO BE STARCONN 115F40-R000RA-M3.
 7. LIGHT-BAR CONNECTOR TO BE ENTRY 3707K-S08N-21R (6PIN).
 8. TORQUE OF M3 USER HOLE SHOULD BE WITHIN 3KGF-CM AND RE-SCREW 10 TIMES.

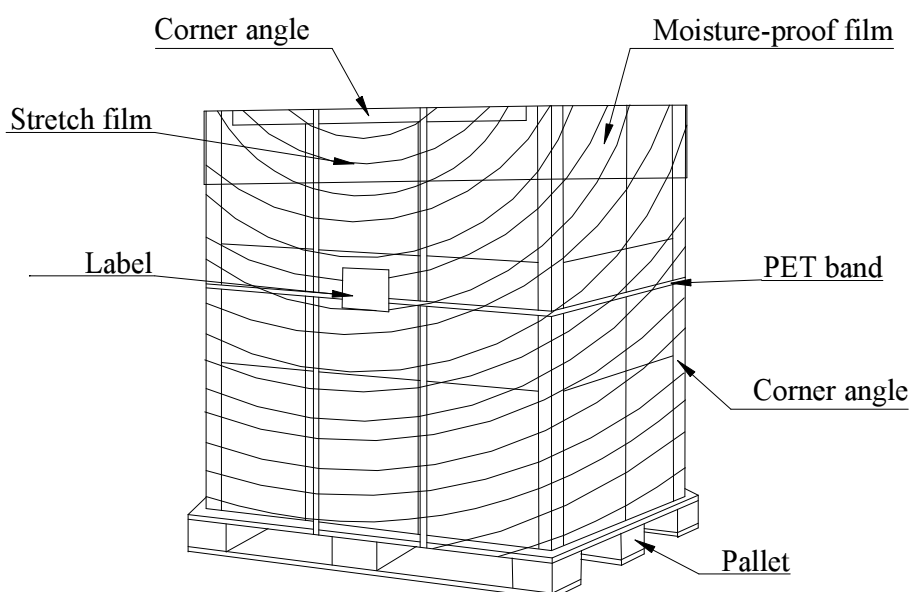
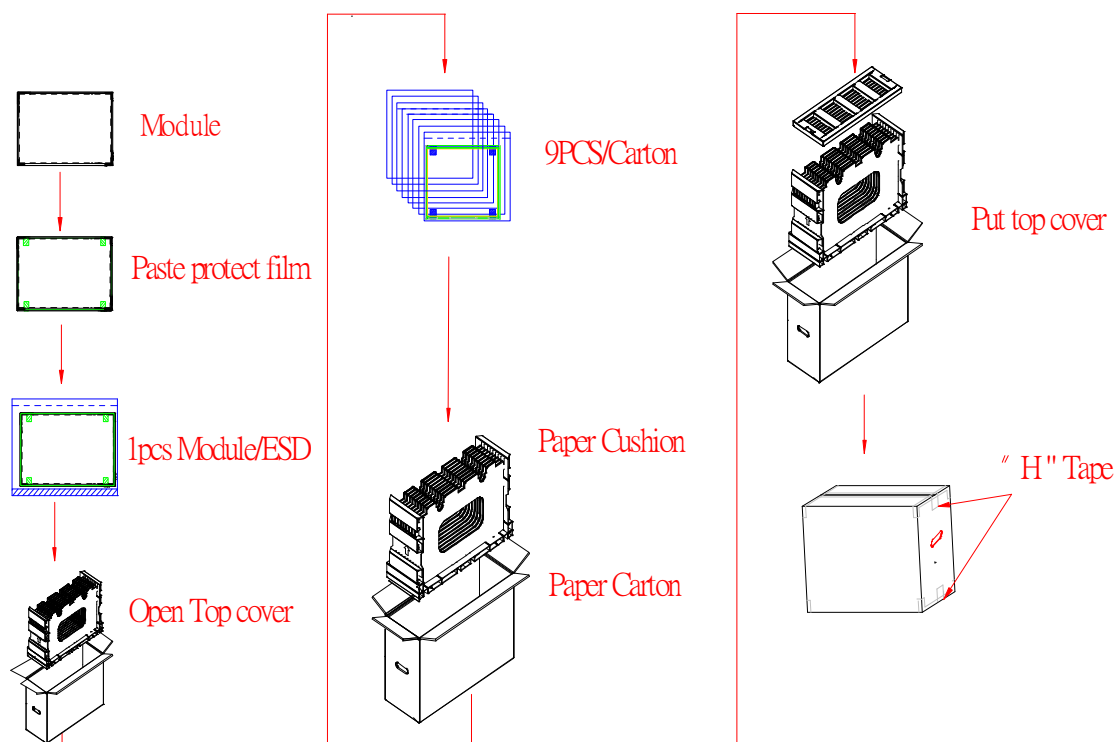
**Avoid stressing front bezel position
when doing mechanical design**



Avoid Touching IC Position When Doing Mechanical Design

11 Packing Specification

11.1 Packing Flow





11.2 Pallet and Shipment Information

	Item	Specification			Remark
		Q'ty	Dimension	Weight(kg)	
1	Panel	1	630.0(H)mm x 368.2(V)mm x 10.6(D)mm	2.319	<i>Note 1</i>
2	Cushion	1	-	4.41	
3	Box	1	720(L)mm x 264(W)mm x 460(H)mm	1.35	without Panel & cushion <i>Note 1</i>
4	Packing Box	9 pcs/Box	720(L)mm x 264(W)mm x 460(H)mm	26.424	with panel & cushion <i>Note 1</i>
5	Pallet	1	1070(L)mm x 740(W)mm x 138(H)mm	13.85	<i>Note 1</i>
6	Pallet after Packing	8 boxes/pallet	1070(L)mm x 740(W)mm x 1060(H)mm	225.24	<i>Note 1</i>

Note 1: Estimated value which is subject to change based on real measured data.