CUSTOMER APPROVAL SHEET

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MODEL	**H354VL02 V0**
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Doc. version :	0.0
Total pages :	30
Date :	2011/01/19

Product Specification

3.54" COLOR TFT-LCD MODULE

MODEL NAME: H354VL02 V0

< ◆ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2011/01/19		First Draft.

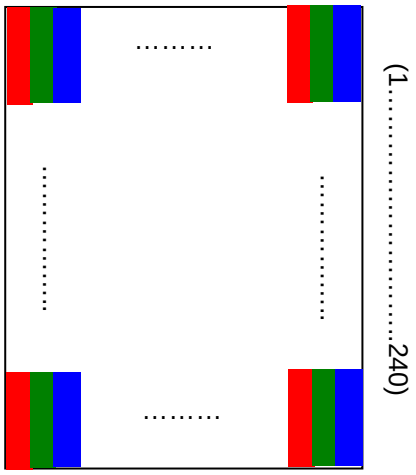
Contents

A. General Information

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	3.54(Diagonal)	
2	Display Resolution	dot	640RGB(H)×960(V)	
3	Overall Dimension	mm	54.22(H) × 82.73(V) × 1.59max(T)	Note 1
4	Active Area	mm	49.92(H)×74.88(V)	
5	Pixel Pitch	mm	0.026(H)×0.078(V)	
6	Color Configuration	--	R. G. B. Stripe	Note 2
7	Color Depth	--	16.7M Colors	
8	NTSC Ratio	%	50	
9	Display Mode	--	ECB Normally white	
10	Weight	g	11.05g	
11	Interface		MIPI I/F	
12	Viewing angle		CR>10:1 at 50 degree	

Note 1: Not include FPCs extrude stucture.

Note 2: Below figure shows dot stripe arrangement.



(1 2 3……718, 719, 720)

B. Electrical Specifications

1 Pin Assignment

Table 1. TFT LCD Panel Pin Assignment:

No.	Pin Name	I/O	Description	Remarks
1	1V8_DVDD	-	Power supply to interface pins.	
2	5V7_AVDDH	-	Power supply to the source driver pins and VCOM drive.	
3	GND	-	GND	
4	PIFA	I/O	Panel interface access	
5	MIPI_CKP	I	DSI CLK+ Line.	
6	STSTB	I	Set Rterm Measurement Mode. Active low. STSTB = 0: Rterm Measurement Mode STSTB = 1: Normal Operation	
7	MIPI_CKN	I	DSI CLK- Line.	
8	PWREN	O	The external power supply shut down output. 0: Disables the external power supply for AVDDH.	
9	GND	-	GND	
10	RESETB	I	Reset. Active Low.	
11	MIPI_D2P	I	DSI Data2+ Line.	
12	HIFA	I/O	Host interface access	
13	MIPI_D2N	I	DSI Data2- Line.	
14	GND	-	GND	
15	GND	-	GND	
16	MIPI_D0P	I/O	DSI Data0+ Line.	
17	NA	-	NA	
18	MIPI_D0N	I/O	DSI Data0- Line.	
19	NA	-	NA	
20	GND	-	GND	
21	GND	-	GND	

22	MIPI_D1P	I	DSI Data1+ Line.	
23	LED_BL_C	I	LED cathode	
24	MIPI_D1N	I	DSI Data1- Line.	
25	LED_BL_A	I	LED anode	
26	GND	-	GND	

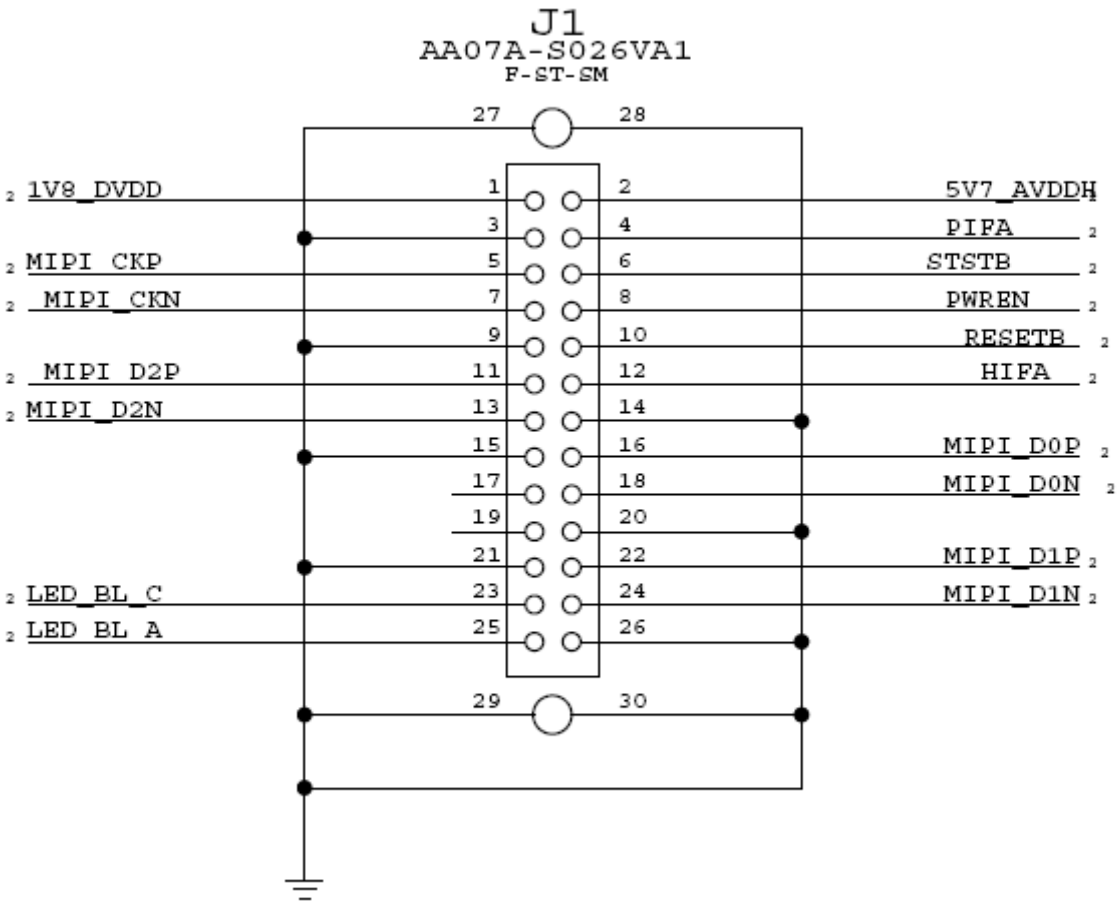


Figure 1 : Connector pin assignment

2 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings:

Item	Symbol	Ratings	Unit	Notes
Analog Supply Voltage	AVDDH	-0.3 ~ +6.4	V	
Analog Supply Current	I AVDDH	100	mA	3
Digital Logic I/O Voltage	DVDD	-0.3 ~ +2.5	V	
Digital Logic I/O Current	I DVDD	15	mA	3
Logic Input Voltage	V_{IN}	$-0.3<V_{IN}<V_{DVDD}+0.3$	V	1
LED Power Consumption	P_{LED}	110	mW	2
LED Current	I_{LED}	35	mA	2
Operating Temperature	TOP	-20 ~ +70	℃	
Storage Temperature	TSTG	-30 ~ +80	℃	

(1) Applies to RESETB, PIFA, HIFA, PWREN, STSTB

(2) Applies for each LED individually

(3) Inrush current maximum, not operating.

.

3 Electrical Characteristics

Table 3.Electrical Characteristics:

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Analog Supply Voltage	AVDDH	5.21	5.4	5.59	V	
Digital Logic I/O Voltage	DVDD	1.71	1.8	1.89	V	
LED Input Current	ILED			25	mA	
“H” Level Input Voltage	VIH	0.8DVDD	-	-	V	1,2
“L” Level Input Voltage	VIL	-	-	0.2DVDD	V	1,2
“H” Level Output Voltage	VOH	0.8DVDD	-	-	V	1,2
“L” Level Output Voltage	VOL	-	-	0.2DVDD	V	1,2
Driver Power Supply Stability				150	ms	5
Power, MIPI full refresh	PMIPI	-	-	110	mW	1
Power Consumption, Backlight	PB	-	-	372	mW	3
Power Consumption, Suspend	PS	-	-	60	uW	4

(1) The specified current and power consumption are under the conditions at AVDDH = 5.67V, DVDD = V_{EE} = 1.8V, T = 25℃, and f_v = 60 Hz

(2) Input mode of RESETB, PIFA, HIFA, PWREN, STSTB.

(3) LED Backlight assumptions: 3.1 V_f, 20 mA, 6 LED’s.

(4) DVDD present only, display off, reset asserted.

(5) Time from AVDDH and DVDD applied until driver power supplies are stable.

3.2 Color Input Data Reference

The brightness of each primary color(R,G,B) is based on 8-8-8 bit gray scale data respectively input for the color.The display outputs 24 bit color data. The higher the binary input,the brihhter the color. Table 4 below provides a reference for color versus data input.

Table4 Color Vs. Data

Colors & Gray Scale	Gray Scale Levels	Data Signal																							
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
Black	--	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Blue	--	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Green	--	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Cyan	--	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	--	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Ma-genta	--	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Yellow	--	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
White	--	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
⬆ Darker ⬆ ⬇ Brighter ⬇	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⬇	⬇																							
	GS253	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GS254	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Red	GS255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
⬆ Darker ⬆ ⬇ Brighter ⬇	GS1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GS2	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⬇	⬇																							
	GS253	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	GS254	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Green	GS255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
⬆ Darker ⬆ ⬇ Brighter ⬇	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	⬇	⬇																							
	GS253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
	GS254	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
Blue	GS255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

3.3.Block Diagram

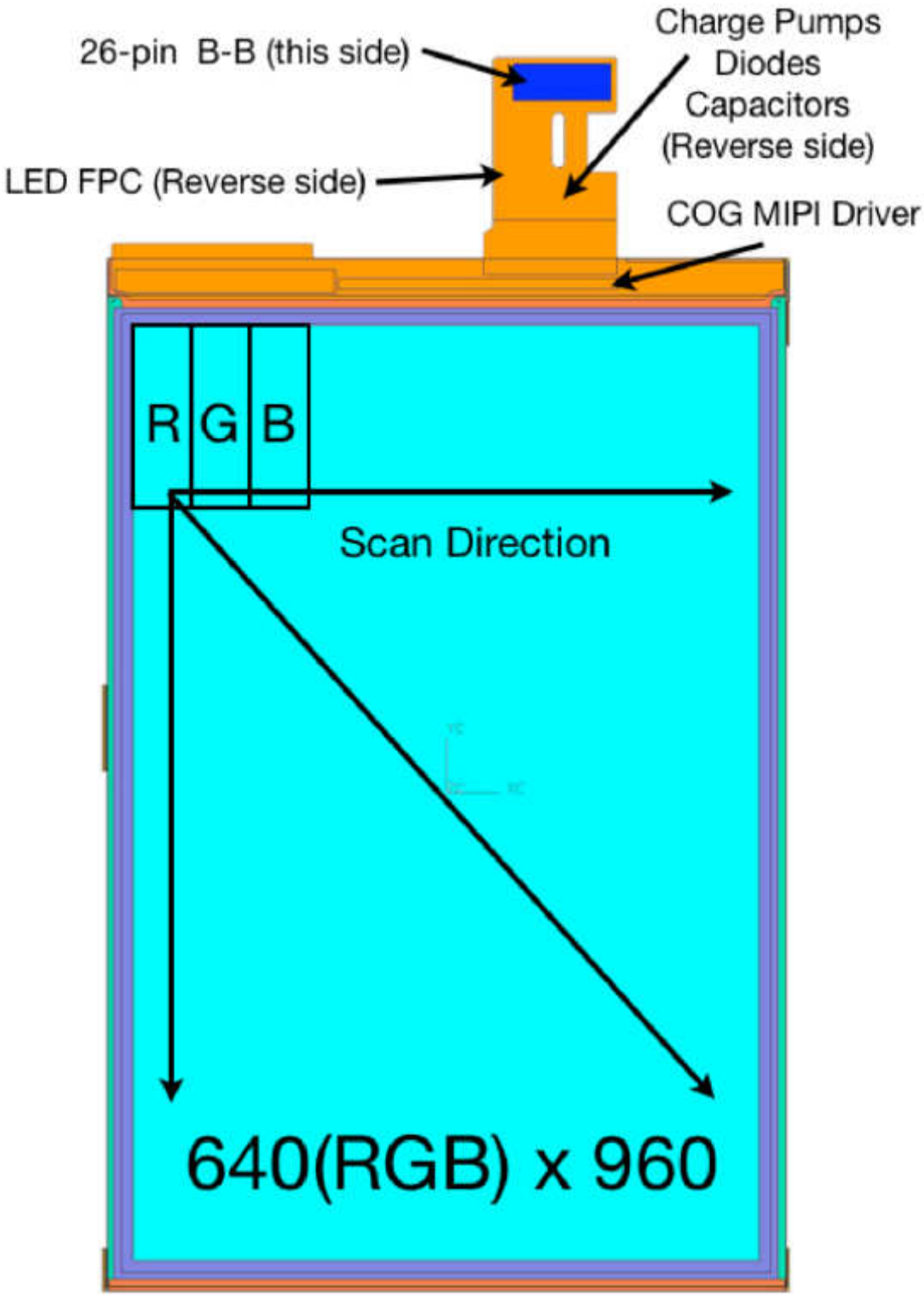


Figure 2 : Display Block Diagram

3.4 Timing Characteristics

The system input timing characteristics are provided in Table 3.5.1 and illustrated in Figure 3. The display must support up to 200MHz, and be tested up to 300MHz frequency to confirm the max MIPI functional interface frequency.

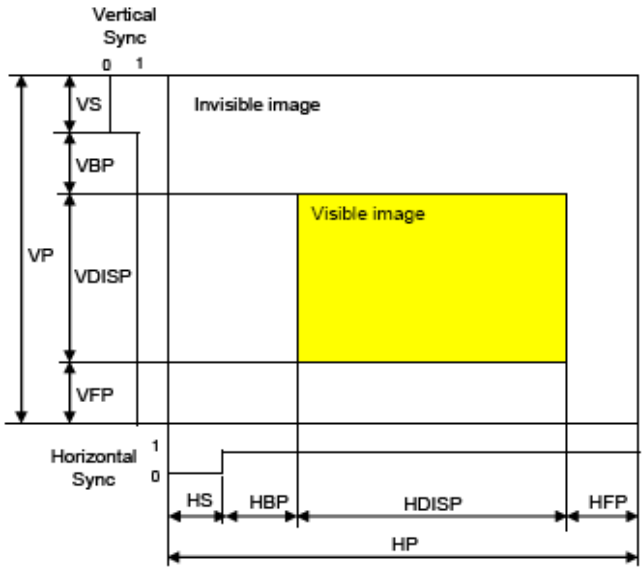


Figure 3 : timing

Table 5. Interface timing characteristics:

Item	Symbol	Timing	Unit	Notes
Vertical Cycle	VP	1000	Line	1
Vertical Low Pulse Width	VS	16	Line	1
Vertical Front Porch	VFP	12	Line	1
Vertical Back Porch	VBP	12	Line	1
Vertical Display Area	VDISP	960	Line	1
Horizontal Cycle	HP	684	clk	1
Horizontal Low Pulse Width	HS	16	clk	1, 2
Horizontal Front Porch	HFP	14	clk	1, 2
Horizontal Back Porch	HBP	14	clk	1, 2
Horizontal Display Area	HDISP	640	clk	1
Pixel Clock	fPLCK	N/A	MHz	1
		N/A	ns	1

4 Electrical Timing Characteristics

4.1. DSI Characteristics

Table 6. MIPI-DSI interface DC Specifications(See Figure 5):

Item		Symbol	Min.	Typ.	Max.	Units	Notes
LP_TX	Thevenin output low level	VOL	-50	-	50	mV	
	Thevenin output high level	VOH	1.1	1.2	1.3	V	
	Output impedance of LP transmitter	ZOLP	(110)	-	-	Ω	2
HS_RX	Different input high threshold	VIDTH	-	-	70	mV	
	Differential input low threshold	V_{IDTL}	-70	-	-	mV	
	Single-ended input low voltage	VILH	-40	-	-	mV	
	Single-ended input high voltage	V_{IHH}			460	mV	
	Common-mode voltage HS receive mode	V_{CM} RX(D	70	-	330	mV	1
	Differential input impedance	ZID		(90)	-	Ω	2
LP_RX	Logic 0 input voltage not in ULP	VIL	-50	-	550	mV	
	Logic 1 input voltage	VIH	880		1350	mV	
	I/O leakage curent	ILEA	-10		10	uA	
CD-RX	Logic 0 contention threshold	V_{ILCD}	-	-	200	mV	
	Logic 1 contention threshold	V_{IHCD}	450		-	mV	

Note:

1. VCMRX(DC) = (VDP+VDN)/2

2. Excluding COG Resistance (Contact Resistance and ITO Wiring Resistance). The value is tentative.

Table 7. HS-RX Clock and Data-Clock Specifications DVDD=DPHYVDD=1.71~1.89V:

Item	Symbol	Min.	Typ.	Max.	Units	Timing diagram	Notes
DSICLK Frequency	fDISCLK	50	-	250	MHz	-	
DSICLK Cycle time	tCLKP	4.0	-	20	ns	Figure 4	
DSI Data Transfer Rate	tDSIR	100	-	500	Mbps	-	
Data to Clock Setup Time	tSETUP	0.15	-	-	UI	Figure 4	
		0.3	-	-	ns		1
Clock to Data Hold Time	tHOLD	0.15	-	-	UI	Figure 4	
		0.3	-	-	Ns		1

Note:

1: @ 500 Mbps

0.15 x 1/(500 x 106) = 0.3 ns**

2.The characteristics in Table 7 are measured under the condition of the minmum differential input voltage 110mV becasure the minmum differential output voltage of HS transmitter is 140mV and insertion loss is -2dB(voltage ratio 0.794328)

Table 8. Global Operation Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit	diagram	Notes
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40 ns + 4*UI	-	85 ns + 6*UI	ns	Figure 6	
$T_{HS-PREPARE}$ + HS-ZERO	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145 ns + 10*UI	-	-	ns		
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	Max(n*8*UI,60 ns + n*4*UI)	-	-	ns		1,2
$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns		
T_{TA-GO}	Time to drive LP-00 after turnaround request	$4*T_{LPX}$					
$T_{TA-SURE}$	Time-out before new TX side starts driving	$1*T_{LPX}$		$2*T_{LPX}$			
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPX}$					

T_{LPX}	Length of any Low-Power state period	50	-	-	ns	Figure 6, 7, 8	4
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3		3/2			
$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated data lane has transitioned to LP mode	60 ns + 52*UI	-	-	UI	Figure 7	
$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8	-	-	UI		
$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38		95	ns		
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock.	300	-	-	ns		
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS ransmission burst	60			ns		
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state			105 ns + n*12*UI	ns		2

Notes:

1. If a > b then max(a, b) = a, otherwise max(a, b) = b

2. Where n = 1 for Forward-direction HS mode.

3. The R63303 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and delayed. But the R63303 can work without the remained process if tCLK-POST is more than 256 UI.

4. The R63303 uses the divided DSI clock from the Host processor for TX clock.

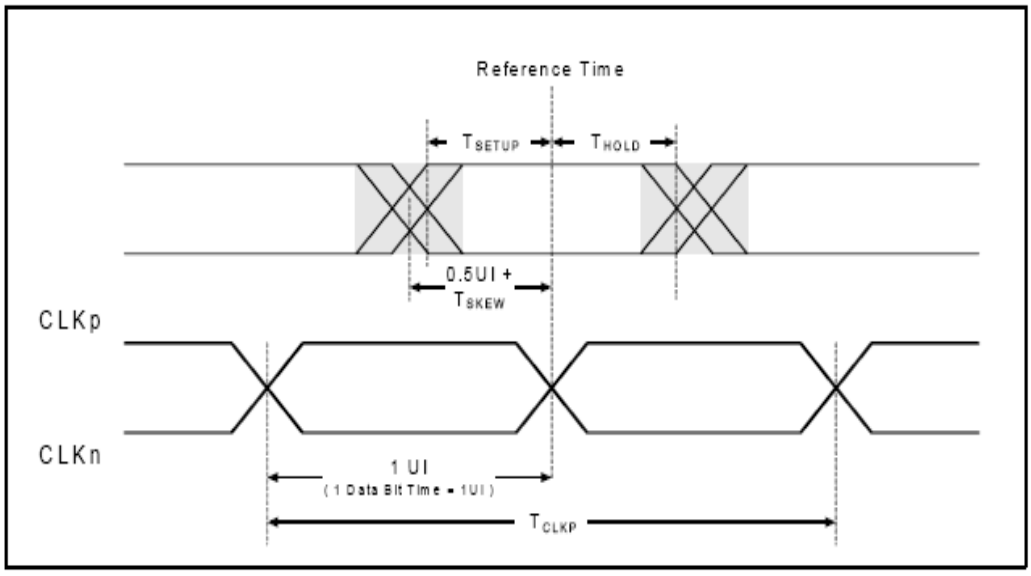


Figure 4. Data to Clock Timing Definitions

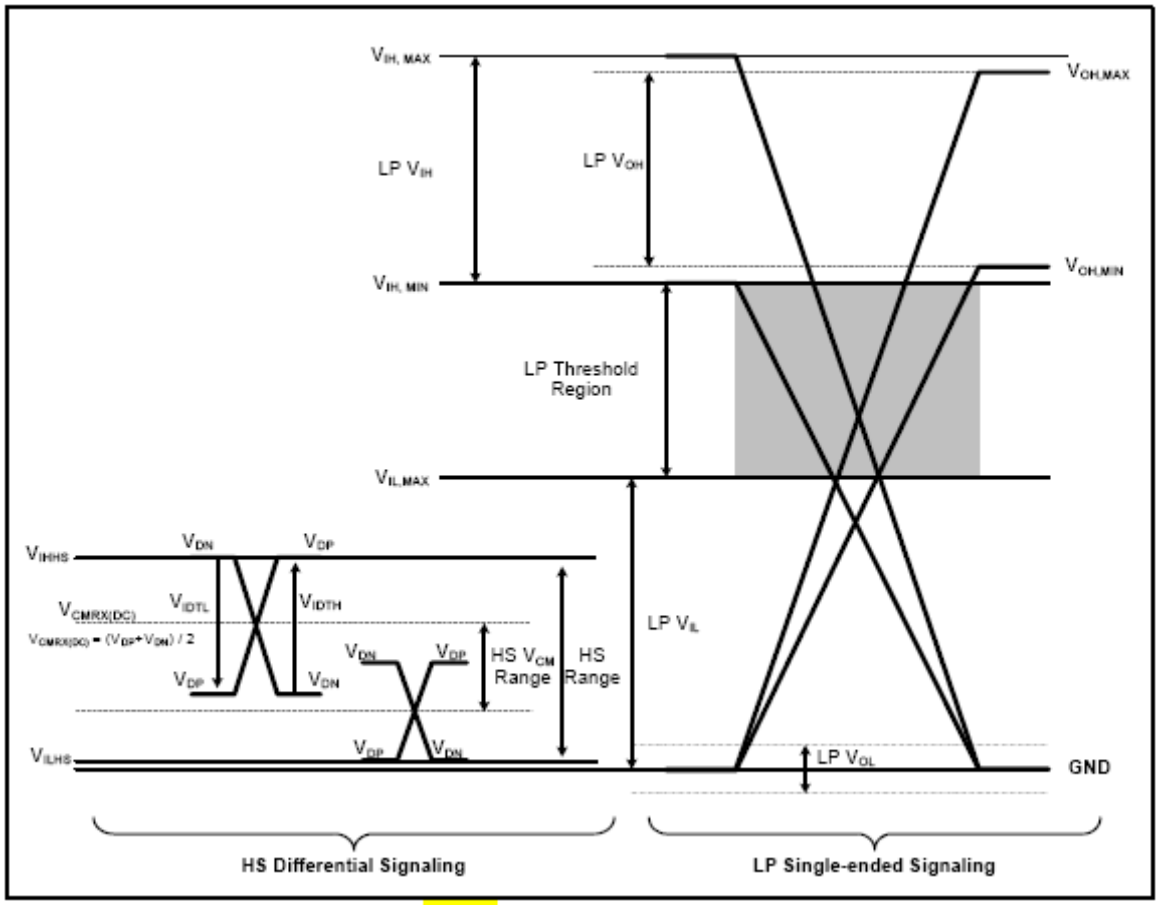


Figure 5. DPHY Signaling Levels

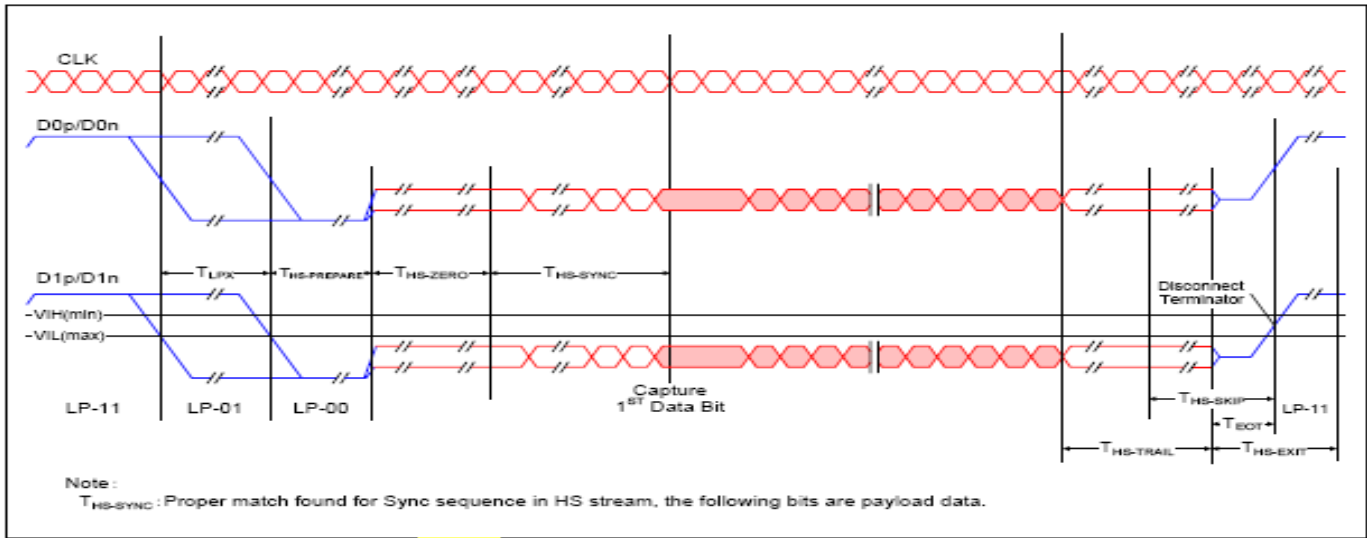


Figure 6. HS Data Transimission in Burats

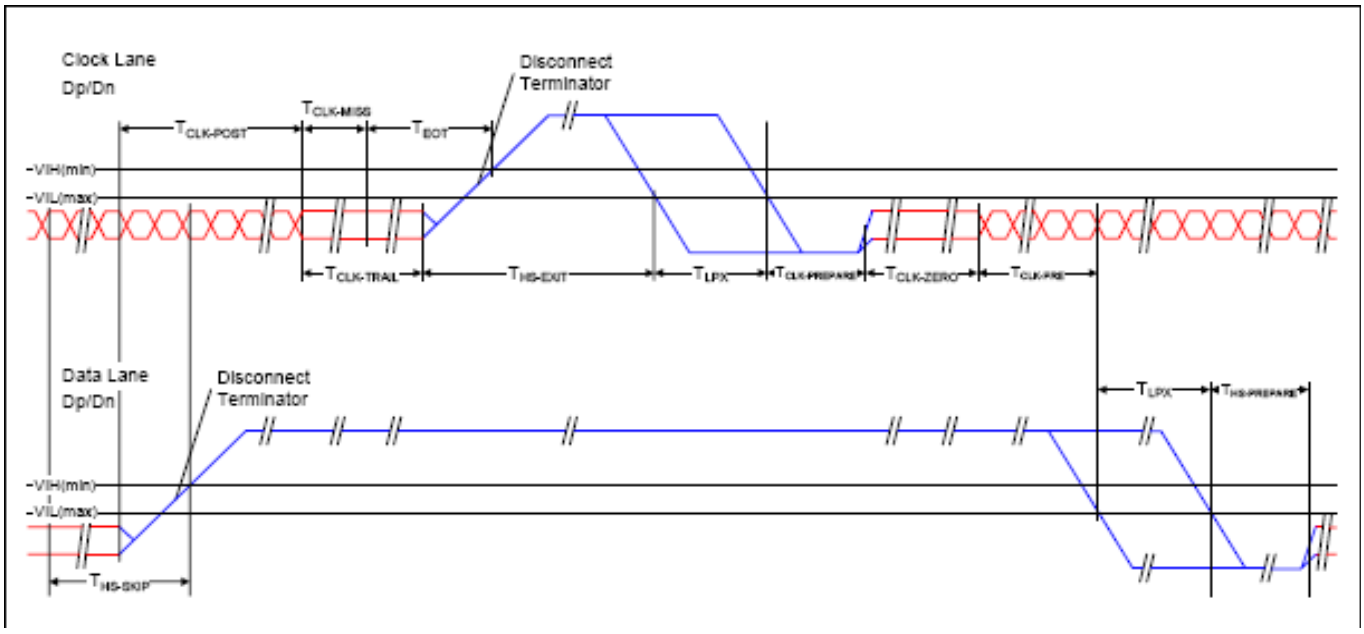


Figure 7. Switching the Clock Lane between Clock Transimission and LP mode

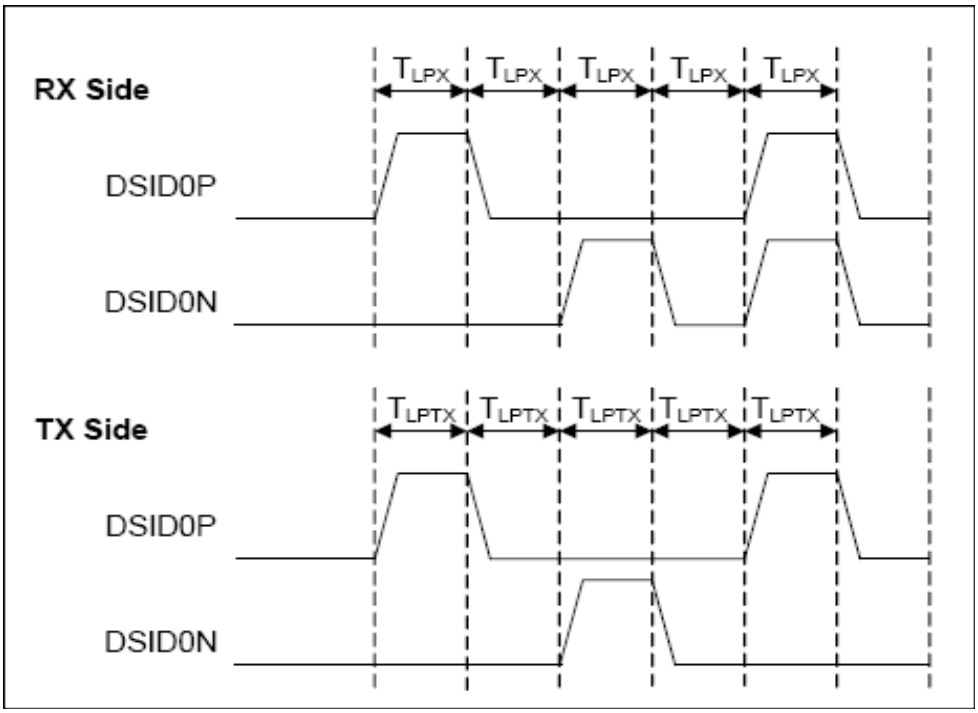


Figure 8. DSI LP mode

5 System Power On and Reset Sequences

5.1. Power On Sequence

The sequence for power On is shown in Figure 9.

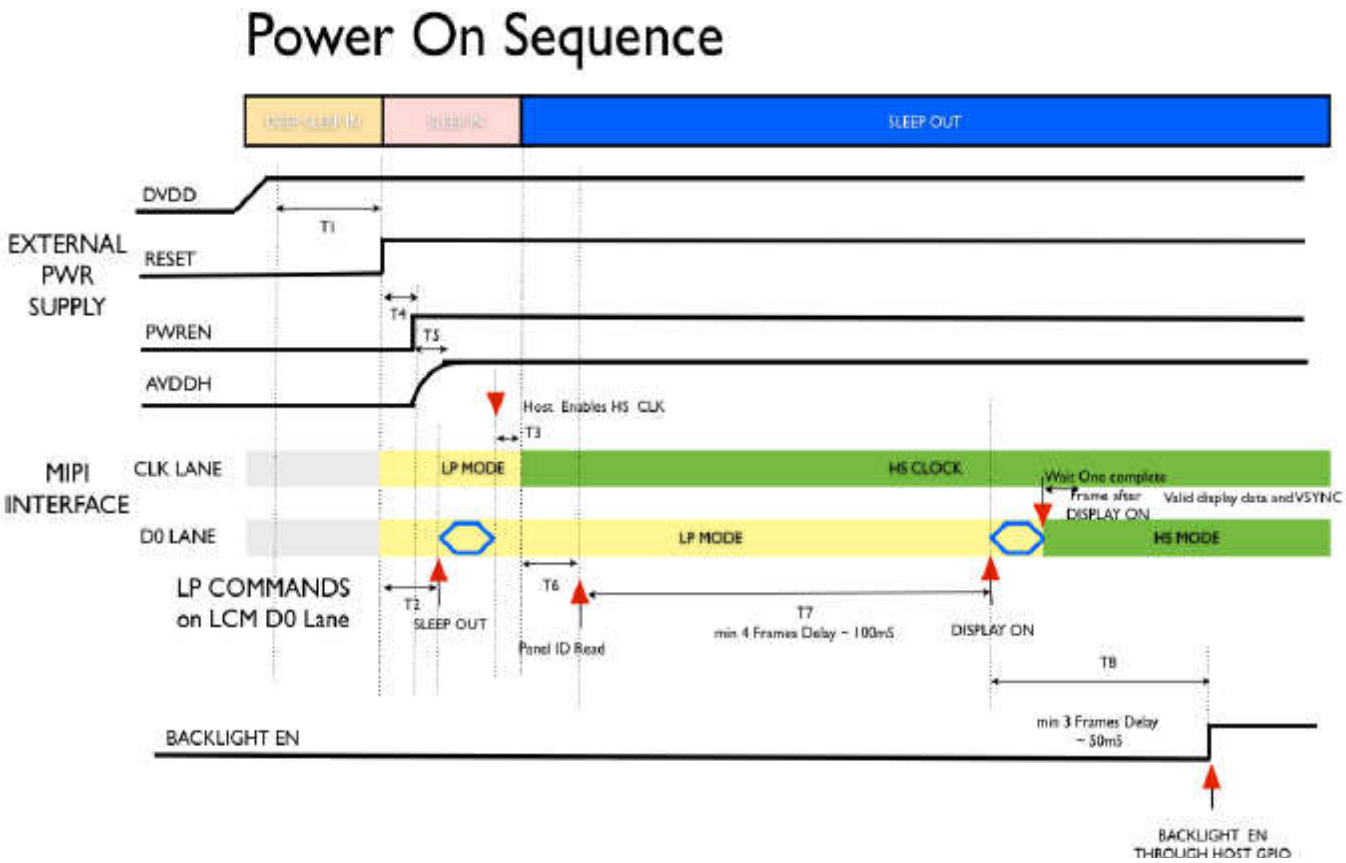


Figure 9. Power on Sequence

NOTE :

1.AVDDH voltage rail may not be completely discharged during the power on sequence due to residual voltage due to previous turn off . If AVDDH rail is not fully discharged in the off state, the driver and panel power on sequence is guaranteed as long as AVDDH ramps up to the specified value in max 3.5ms after PWREN becomes active (high).

2. This display has 4 control signals: RESETB, PWREN, PIFA, & HIFA. RESETB is an input signal with no PU / PD . PWREN, PIFA & HIFA are push pull output signals. The output signals states are specified as follows:

" Sleep in Mode and Ultra Low Power Mode : PWREN is low. PIFA and HIFA are Hi-Z.

" Normal Mode : PWREN is active (high). Our normal register settings are such that PIFA & HIFA are configured for low output

5.2. Power Off Sequence

The sequence for power On is shown in Figure 10.

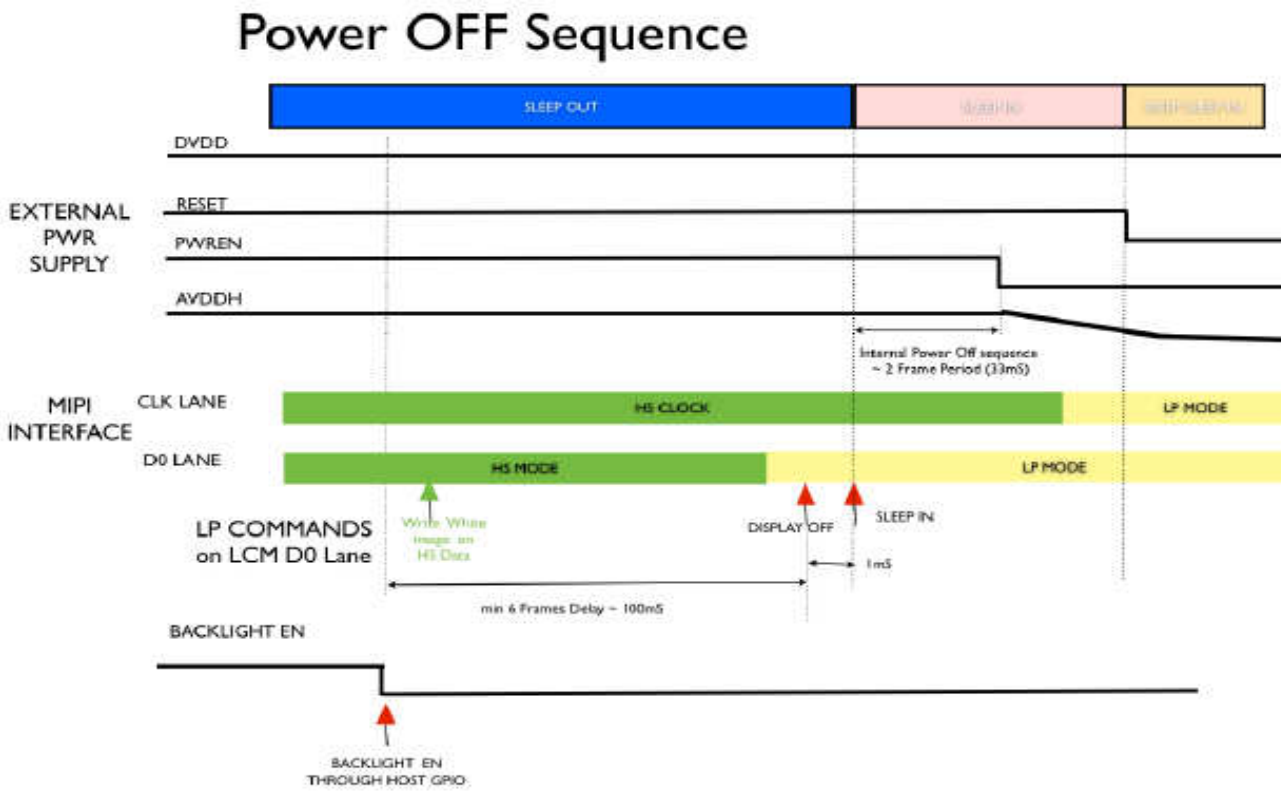


Figure 10. Power on Sequence

5.3 Software Flow & Register Settings

The display follow the basic software flowchart illustrated in Figure 10 and in following tables.

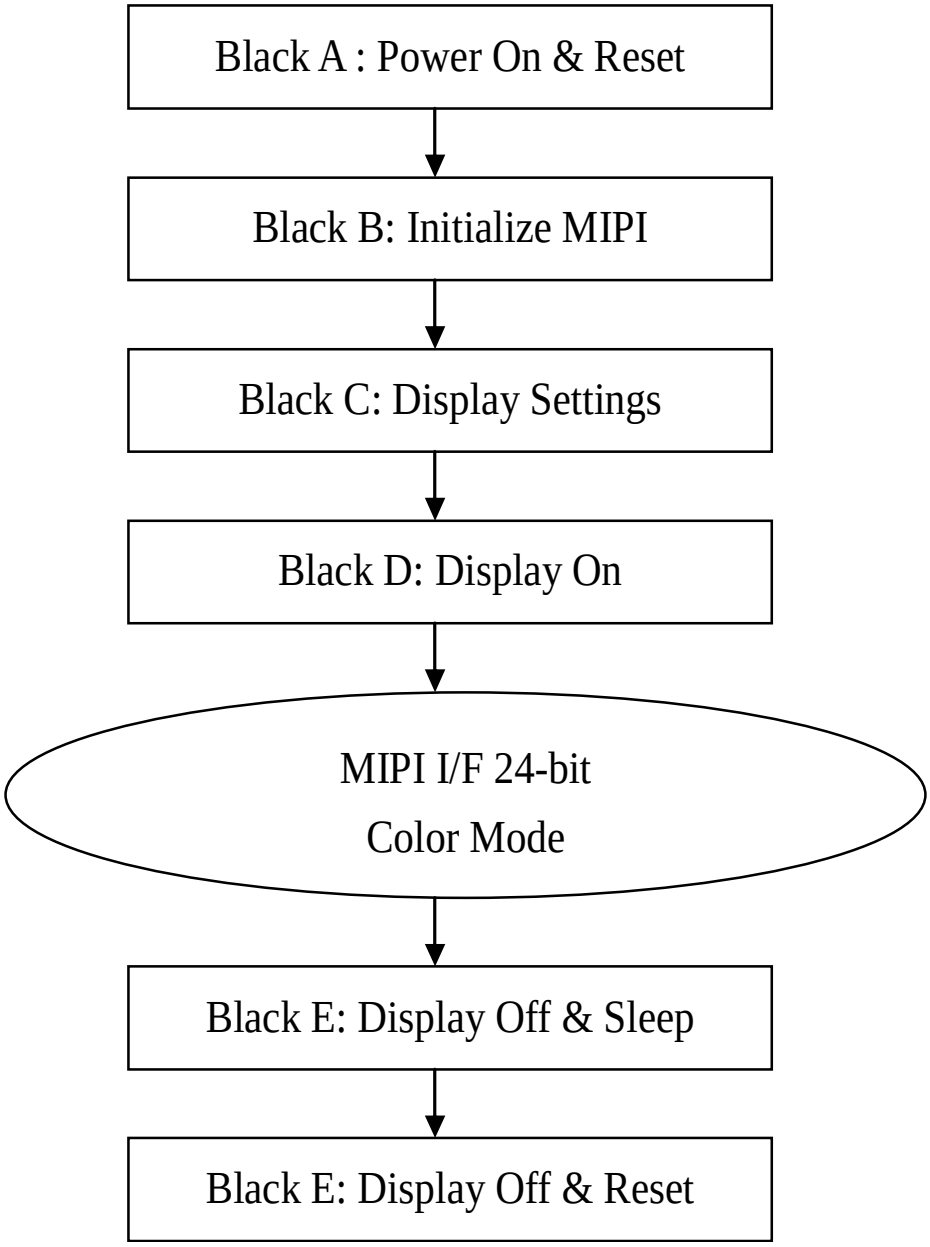


Figure 11. Software Flowchart

Table 9: Block A: Power on & Reset

Step	Operation
1	Apply DVDD
2	Toggle
3	LCM sends PWREN to logic high to enable AVDDH
4	AVDDH turns on

Table 9.1: Block B: Initialize MIPI

Step	Register/ Command	Parameter/Setting	Operation
1			Initialize System side MIPI block
2	0x00		Send MIPI NOP
3			Delay 6ms
4			Start MIPI Highspeed Clock

Table 9.2:Block C: Display Settings

Step	Register/ Command	Parameter/Setting	Operation
1	Optionally override EEPROM setting in supplier-specific electrical specification		

Table 9.3: Block D: Sleep out & Display On

Step	Register/ Command	Parameter/Setting	Operation
1			Delay 10ms
2	0x11		Sleep Out
3			Delay minimum 6 frames(100ms)
4	0x29		Display On
5			Delay minium 3 frames(50ms)
6			Backlight On

Table 9.4: Block E: Display Off & Sleep In

Step	Register/ Command	Parameter/Setting	Operation
1			Blacklight Off
2			Send White Image Data
3			Delay minimum 6 frames(100ms)
4	0x28		Display Off
5			Delay 1ms
6	0x10		Sleep In Command

Table 9.5: Block F: Power Off & Reset

Step	Register/ Command	Parameter/Setting	Operation
1	LCM turns off PWREN (logic low) to disable AVDDH		
2	Disable Host side MIPI I/F		
3	Reset low		

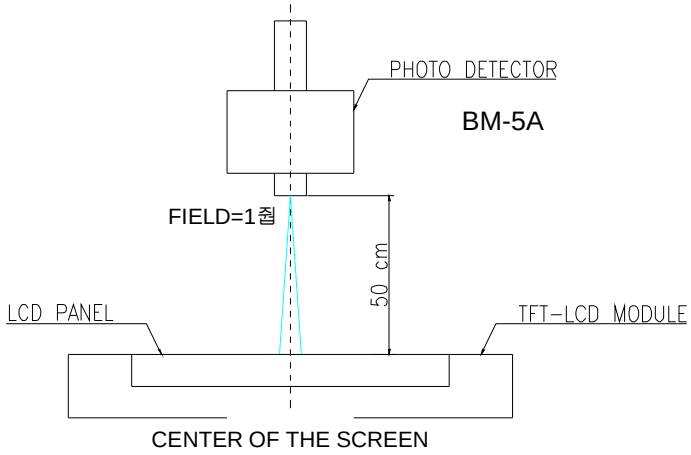
C. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall		 Tr Tf	θ=0°	 -- --	 6 20	 15 30	 ms ms	Note 3
Contrast ratio		CR	At optimized	100	150	--		Note 4
Viewing Angle	Top		CR□10	--	50	--	deg.	Note 5
	Bottom			--	50	--		
	Left			--	50	--		
	Right			--	50	--		
High gray level inversion	Top		CR≧10	--	50	--	deg.	Note 5
	Bottom			--	50	--		
	Left			--	50	--		
	Right			--	35	--		
Low gray level inversion	Top		CR≧10	--	50	--	deg.	Note 5
	Bottom			--	50	--		
	Left			--	50	--		
	Right			--	50	--		
Brightness		Bottom	θ=0°	450	500	--	cd/m^2	Note 6
NTSC		Left	θ=0°	--	50	--		
Chromaticity	White	X	θ=0°		0.309			
		Y	θ=0°		0.324			
	Red	X	θ=0°		0.610			
		Y	θ=0°		0.345			
	Green	X	θ=0°		0.320			
		Y	θ=0°		0.555			
	Blue	X	θ=0°		0.150			
		Y	θ=0°		0.120			
Uniformity		ΔY_L	%	--	80	--	%	Note 7

Note 1: Measured under Ambient temperature =25℃, and LED lightbar current I_L = 20mA in the dark room.

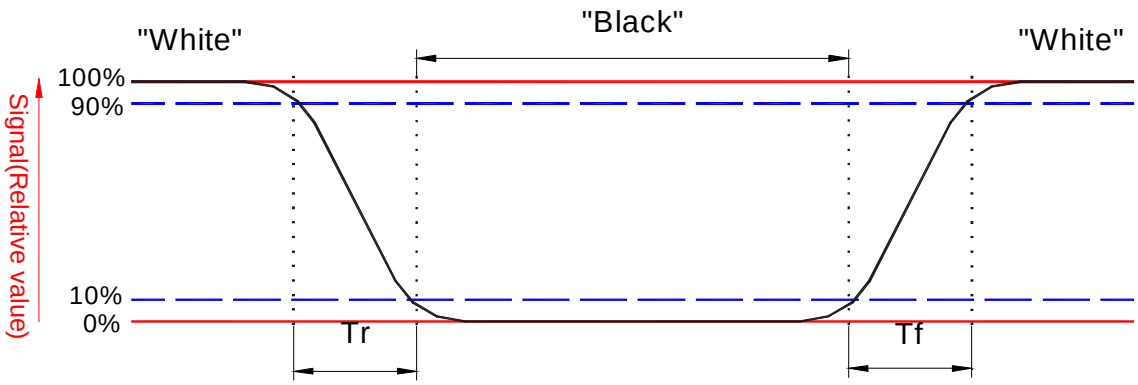
Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.



Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white” (falling time) and from “white” to “black” (rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

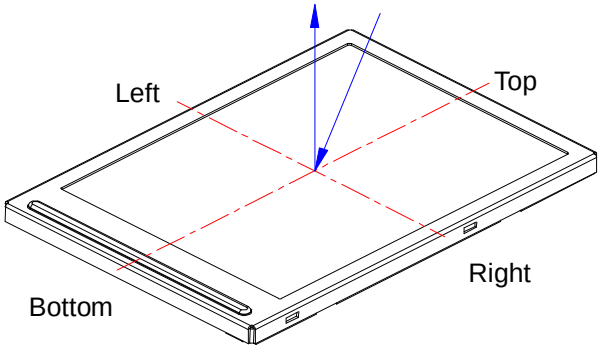


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

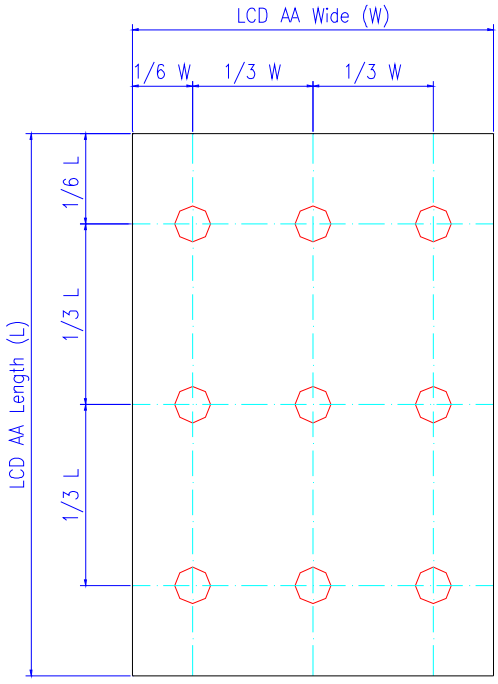
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

D. Reliability test items

1. Test items and conditions:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80℃ 500H	
2	Low temperature storage	Ta= -30℃ 500H	
3	High temperature operation	Ta= 70℃ 500H	
4	Low temperature operation	Ta= -20℃ 500H	
5	High temperature and high humidity	Ta= 50℃. 90% RH 240H	Operation
6	Heat shock	-30℃~80℃/50 cycles 1H/cycle	Non-operation
7	Electrostatic discharge	±HBM 2KV, once for each terminal in the non-operation mode.	Non-operation

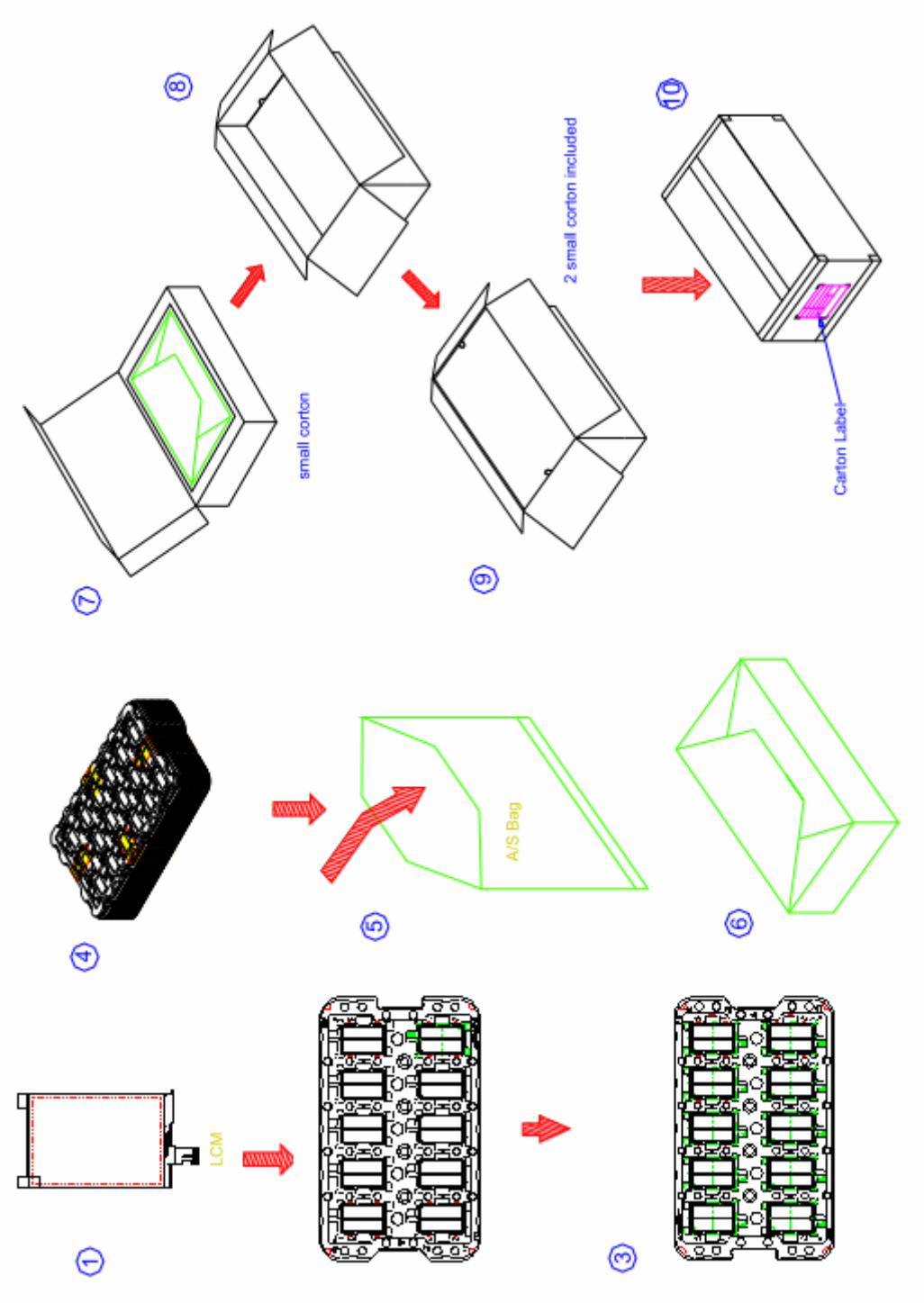
Note: After finishing the test, leave the samples under room temperature and normal humidity for 2 hours, and then this module should work normally.

2. Failure Judgment Criterion:

a. Neither abnormality nor significant visible deterioration should be found on display quality and appearance.

b. There should be no functional abnormalities on display quality.

E. Packing



F. Outline Dimension