Chunghwa Picture Tubes, Ltd.
Technical Specification

To : **STUDIO**

Date : 2008.08.05

CPT TFT-LCD

CLAA170EA07P Y

ACCEPTED BY：

APPROVED BY	CHECKED BY	PREPARED BY
KEVIN	LAWRENCE LAI	**TFT-LCD Product Planning Management General Division**

CHUNGHWA PICTUER TUBES, LTD.

1127 Hopin Rd., Padeh, Taoyuan, Taiwan 334, R.O.C.

TEL: +886-3-3675151 FAX: +886-3-377-3001

Doc.No:	CLAA170EA07P Y-STUDIO-2008/08/05	Issue Date:	2008/08/05

RECORD OF REVISIONS

Revision No.	Date	Page	Description
Ver:1	2008/08/05		First edition for customer-Lite-On /OBM

CONTENTS

1.OVERVIEW

CLAA170EA07P is 17.0" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs, control circuit and backlight. By applying 8 bit digital data, 1280×1024, 16.2M-color images are displayed on the 17.0" diagonal screen. Input power voltage is 5.0V for LCD driving.Inverter for backlight is not included in this module. General specification are summarized in the following table:

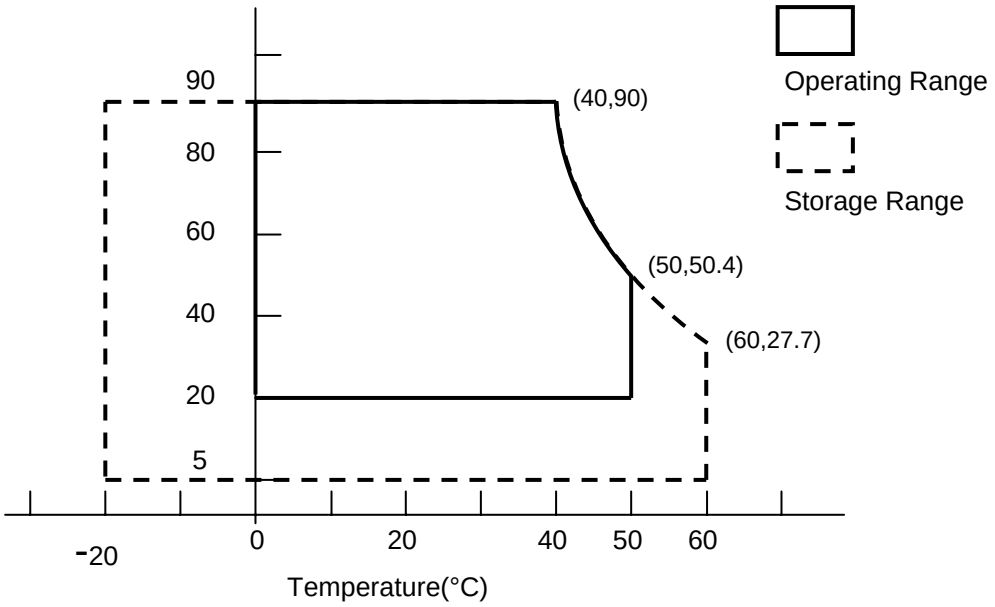
ITEM	SPECIFICATION
Display Area(mm)	337.920(H)x270.336(V) (17.0-inch diagonal)
Number of Pixels	1280(H)x1024(V)
Pixel Pitch(mm)	0.264(H)x0.264(V)
Color Pixel Arrangement	RGB vertical stripe
Display Mode	normally white, TN
Number of Colors	16.2M(6 Bit+FRC)
Brightness(cd/m^2)	300 cd/m^2(Typ.)(Center point, Lamp current=7.5 mA)
Viewing Angle	160 / 160(Typ.)
Surface Treatment	Anti-glare
Power consumption(W)	23.7 (Typ.)
Module Size(mm)	358.5(W)x296.5(H)x17.5(D)(max)
Module Weight(g)	2200(typ)
Backlight Unit	CCFL, 4 tables, edge-light(top*2/bottom*2)

2. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT	REMARK
Power Supply Voltage for LCD	VCC	0	6.5	V	--
Lamp Voltage	VL	590	832	Vrms	
Lamp Current	IL	3	8.0	mArms	*4), 7)
Lamp Frequency	FL	40	80	kHz	
static electricity	$VESD_t$	-200	200	V	5)
	$VESD_C$	-8000	8000	V	
Operation Temperature	T_{op}	0	50	℃	*1),2),3),6)
Storage Temperature	T_{stg}	-20	60	℃	*1),2),3)
Delayed Discharge Time	TD	--	1	Sec	*8)

[Note]

1) The relative temperature and humidity range are as below sketch, 90%RHMax.(Ta≦40℃).
2) The maximum wet bulb temperature ≦39℃(Ta＞40℃) and without dewing.
3) If you use the product in a environment which over the definition of temperature and humidity too long to effect the result of eye-atching.
4) The life time of the lamp is relate to the current of the lamp, so please accronding to the description of the "(b) backlight" on page 7.
5) Test Condition: IEC 1000-4-2
   VESDt: Contact discharge to input connector; $VESD_C$: Contact discharge to module
6) If you operate the product in normal temperature range, the center surface of panel should be under 60℃.
7) When lamp current is out of the absolute maximum range, the life will fall rapidly or shown unusual sign.
   IL min **2**mA only for test only, but we can't guarantee the lifetime and performance.
8) Delay lighting testing needs the volt above start volagte Vrms**.**Before the procedure tube needs typical lighting for 1 minute and stay in the temperature 25±2℃ for 24 hours and then testing in the same condition in dark room **.**



3. ELECTRICAL CHARACTERISTICS

(1)TFT-LCD

Ta=25℃

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	Remark
Power Supply Voltage for LCD		Vcc	4.5	5.0	5.5	V	*1)
Power Supply Current for LCD		Icc	-	700	950	mA	*2)
Permissive Input Ripple Voltage		VRP	-	-	100	mVp-p	Vcc=5.0V
Differential impedance		Zm	90	100	110	Ω	
Logic input voltage LVDS:IN+，IN-	Common Mode Voltag	VCM	1.125	1.25	1.375	V	
	Differential Input Voltage	|VID|	250	350	450	mV	
	Threshold Voltage(High)	VTH	-	-	100	mV	*3)
	Threshold Voltage(Low)	VTL	-100	-	-	mV	
LCD Inrush Current		Inrush			3	A	*4)
Power consumption		P		3.5	4.75	W	*2)

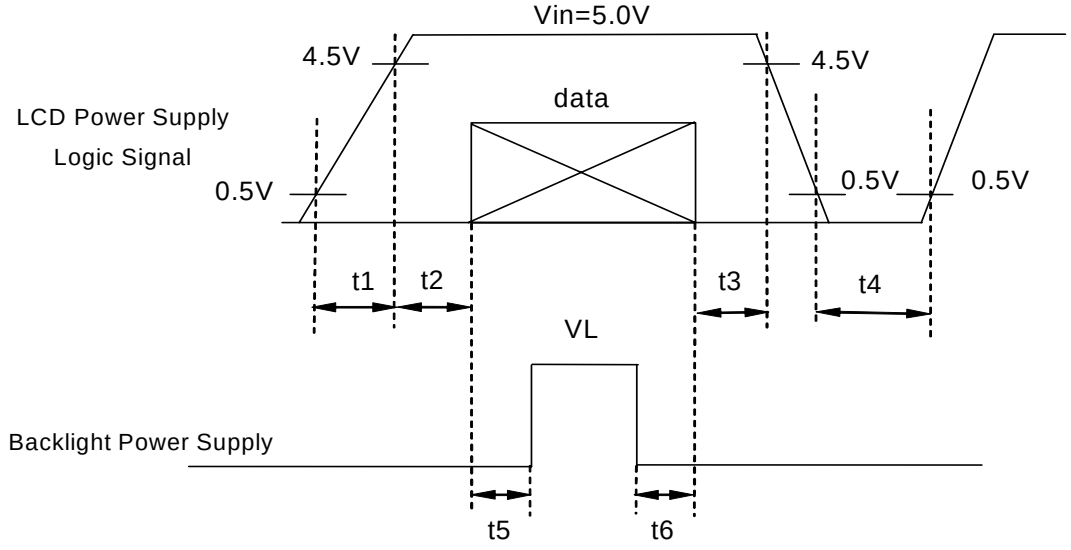
[Note]

1) VCC-turn-on conditions:

0.5ms≦t1≦10ms 1 sec≦t4

0＜t2≦20ms 200ms ≦t5

0＜t3≦50ms 200ms≦t6

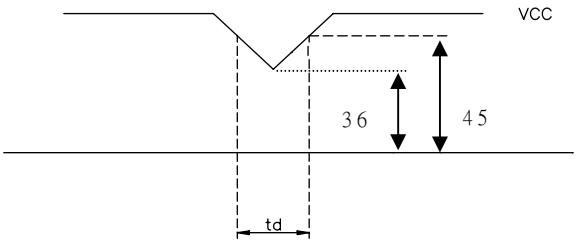


Data: RGB DATA, DCLK, DENA

VCC-dip conditions:

(1) When 3.6V≦Vcc(min)<4.5V: td≦10 ms

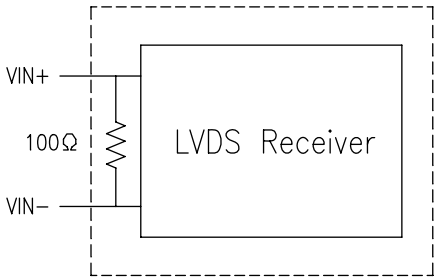
(2) When Vcc <3.6 V,VCC-dip conditions should also follow the VCC-turn-on conditions.

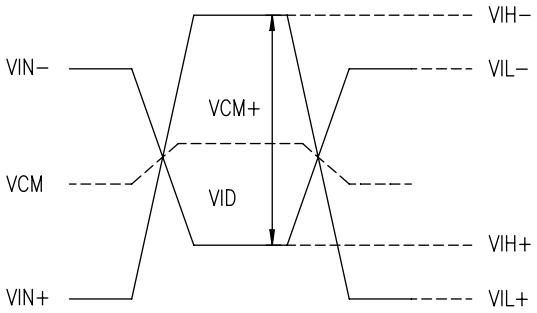


2) Typical current situation: 64 gray scale level,1280 line mode, VCC=5.0V, Fh=64Khz,Fv=60Hz,

Fclk=54 MHz.

3) LVDS Signal definition:

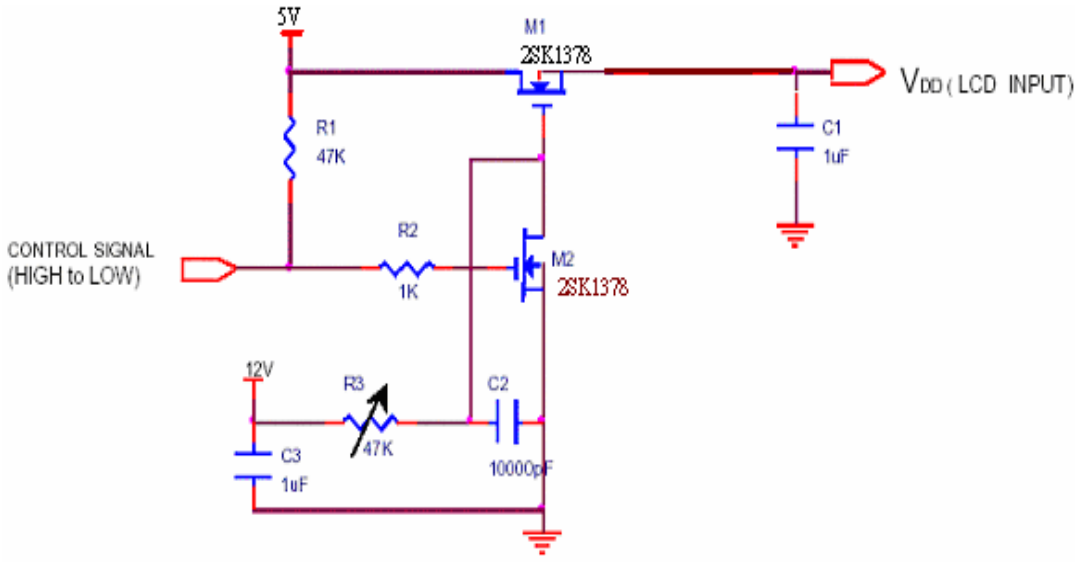


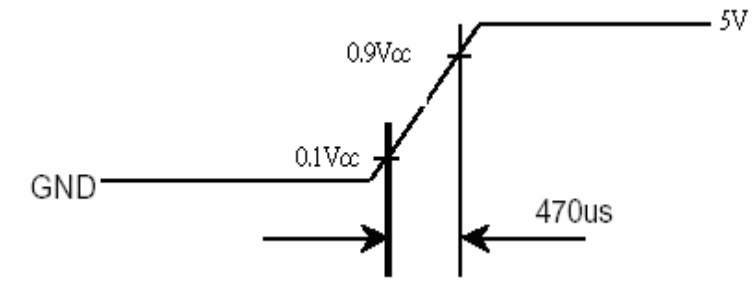


VID = VIN_+ – VIN- ,
△VCM = | VCM_+–VCM- | ,
△VID = | VID_+–VID- | ,
VID+ = | VIH_+–VIH- | ,
VID- = | VIL_+–VIL- | ,
VCM =(VIN_+ +VIN-)/2,
VCM+ =(VIH_+ +VIH-)/2,
VCM- =(VIL_+ +VIL-)/2,

VIN_+ = Positive differential DATA & CLK Input
VIN- = Negative differential DATA & CLK Input

4) Irush Measurement Condition





(2)Backlight

1. Electrical specification

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	REMARK
B/L Voltage	VL	572.4	636	699.6	Vrms	IL=7.5mA Ta=25℃
B/L Current	IL	7.0	7.5	8.0	mArms	*1)，Ta=25℃
B/L operating current	ILO	3.0	7.5	8.0	mArms	
B/L power comsuption	WL	--	20.2	22.2	W	*6)，IL=7.5mA Ta=25℃
Inverter Frequency	FI	45	50	65	kHz	*2)，Ta=25℃
Starting Lamp Voltage	VS	--	--	1600	Vrms	Ta=0℃
		--	--	1100	Vrms	*5)，Ta=25℃

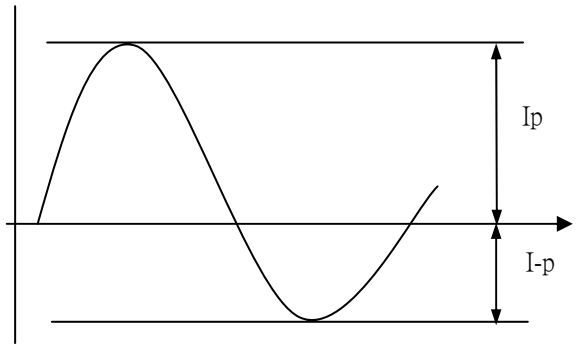
2.Lamp life time

ITEM	IL at 3.0 mA	IL at 7.0 mA	IL at 7.5 mA	IL at 8.0 mA	UNIT	REMARK
Lamp life Time	Min.50, 000	Min.40, 000	Min.40,000	--	hr	*3)，Continuous Operation,
Rated time (turn on/off)		Min.100,000	--	--	time	*4)

[Note] Measuring inverter Type：SAMPO DIVLCP0506D42

If the waveform of light up-driving is asymmetric, the distribution of mercury inside the lamp tube will become unequally or will deplete the Ar gas in it. Then it may cause the abnormal phenomenon of lighting-up. Therefore, designers have to try their best to forfill the conditions under the inverter designing-stage as below:

- The degrees of unbalance： ＜10%
- The ratio of wave height：＜√2 ±10%



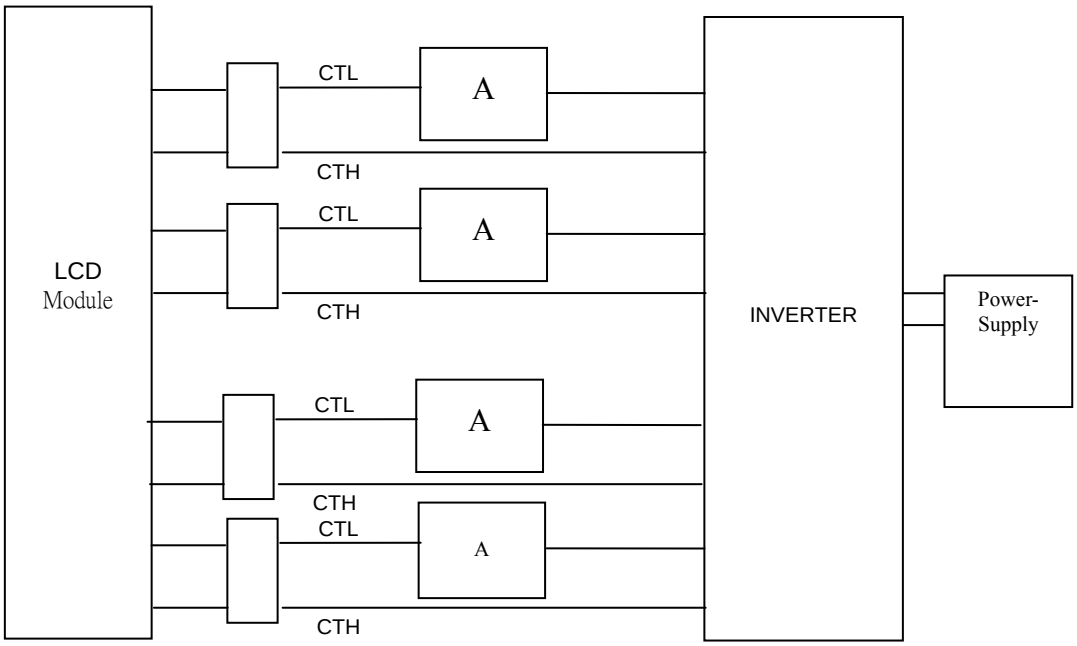
Ip：high side peak

I-p：low side peak

A：The degrees of unbalance = | Ip – I-p | / Irms ×100 (%)

B：The ratio of wave height = Ip (or I-p) / Irms

1) Lamp Current measurement method (The current meter is inserted in cold line)



2) a.Frequency in this range can mala the characterisitics of electric and optics maintain in +/- 10% except hue.
   b.If the lamp frequency can be maintain in 50~60KHz, the better charactristics of the electrical and the optical can be presented.
   c.If the operating frequency is 40~80 KHz, the life time and the reliability of the lamp will not be affect.
   d.Lamp frequency of inverter may produce interference with horizontal synchronous frequency,and this may cause horizontal beat on the display.Therefore, please adjust lamp frequency, and keep inverter as far from module as possible or use electronic shielding between inverter and module to avoid the interference.
3) Definition of the lamp life time： Luminance (L) under 50% of specification starting lamp voltage or starting lamp voltage is more than 130% of the initial value
4) The condition of Turn-on and Turn-off operation is as below:
   a. Lamp current is 7.5mA
   b. Frequency is 10 sec.(on)/10 sec.(off)
   c. Repeat it for 10 thousand times
   d. The result of eye-atching of the lamp hue is normal, and can switch the lamp.
   It should not have motion fail when starting lamp voltage is lower than 130% of the initial value
5) It is necessary to consider the maximal value when design inverter，in order to asure lighting**.**
6) the equation of power comsuption WL=IL x VL x 4。(IL=7.5mA，Ta=25℃)

4. INTERFACE PIN CONNECTION

(1) CN1 (Data Signal and Power Supply)

Used connector: FI-XB30SSRL-HF16 (JAE) or compatiable.

PIN NO.	SYMOBL	FUNCTION
1	RXO0-	minus signal of odd channel 0(LVDS)
2	RXO0+	plus signal of odd channel 0(LVDS)
3	RXO1-	minus signal of odd channel 1(LVDS)
4	RXO1+	plus signal of odd channel 1(LVDS)
5	RXO2-	minus signal of odd channel 2(LVDS)
6	RXO2+	plus signal of odd channel 2(LVDS)
7	GND	ground
8	RXOC-	minus signal of odd clock channel (LVDS)
9	RXOC+	plus signal of odd clock channel (LVDS)
10	RXO3-	minus signal of odd channel 3(LVDS)
11	RXO3+	plus signal of odd channel 3(LVDS)
12	RXE0-	minus signal of even channel 0(LVDS)
13	RXE0+	plus signal of even channel 0(LVDS)
14	GND	ground
15	RXE1-	minus signal of even channel 1(LVDS)
16	RXE1+	plus signal of even channel 1(LVDS)
17	GND	ground
18	RXE2-	minus signal of even channel 2(LVDS)
19	RXE2+	plus signal of even channel 2(LVDS)
20	RXEC-	minus signal of even clock channel (LVDS)
21	RXEC+	plus signal of even clock channel (LVDS)
22	RXE3-	minus signal of even channel 3(LVDS)
23	RXE3+	plus signal of even channel 3(LVDS)
24	GND	ground
25	NC	**NC**
26	NC	**NC**
27	NC	**NC**
28	VCC	Power supply input voltage(5.0 V)
29	VCC	Power supply input voltage(5.0 V)
30	VCC	Power supply input voltage(5.0 V)

(2) CN2,3,4,5 (BACKLIGHT)

Backlight-side connector: BHSR-02VS-1 (JST)

Inverter-side connector: SM02(4.0)B-BHS-1-TB (JST)

Pin No.	Symbol	Function
1	CTH	Power for CCFL
2	CTL	Power return for CCFL

5. INTERFACE TIMING

(1) Timing Specifications

ITEM			SYMBOL	MIN	TYP	MAX	UNIT
LCD Timing	DCLK	Frequency	f_{CLK}	45	54	70	MHz
		Period	t_{CLK}	14.3	18.5	22.2	ns
	DENA	Horizontal Active Time	t_{HA}	640	640	640	t_{CLK}
		Horizontal Blank Time	t_{HB}	112	204	390	t_{CLK}
		Horizontal Total Time	t_H	752	844	1030	t_{CLK}
		Vertical Active Time	t_{VA}	1024	1024	1024	t_H
		Vertical Blank Time	t_{VB}	22	42	76	t_H
		Vertical Total Time	t_V	1046	1066	1100	t_H
		Vertical Frame Rate	Fr	55	60	75	Hz

[Note]

1) DENA should always be positive polarity as shown in the timing specification.
2) CLK INshould appear during all blanking period,
3) Using LVDS IC

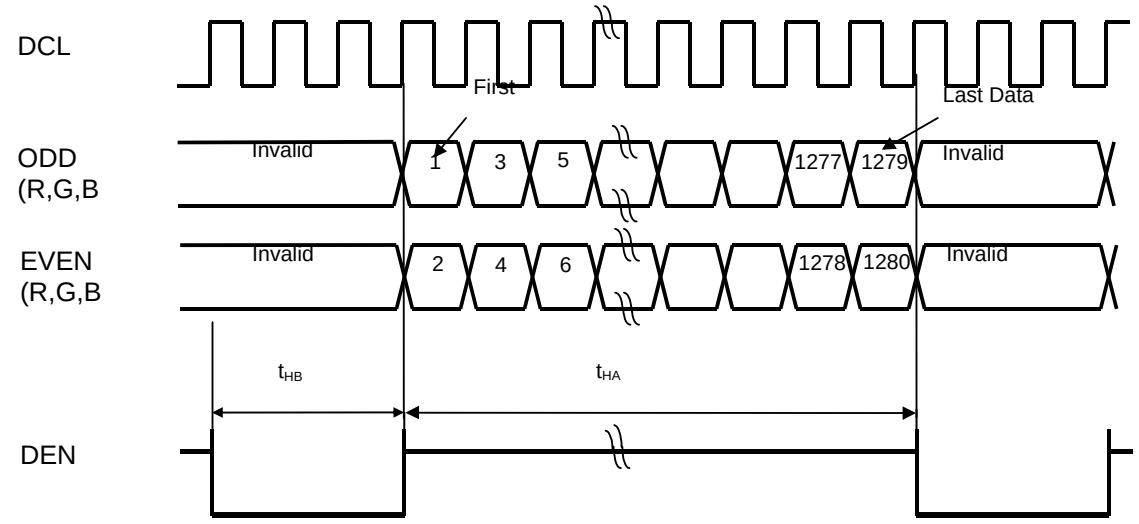
Receiver	Transmitter
DS90C384MTD(NS)	DS90C383MTD(NS)
SN75LVDS82(TI)	SN75LVDS83(TI)

4) Required signal assignment for flat link transmitter

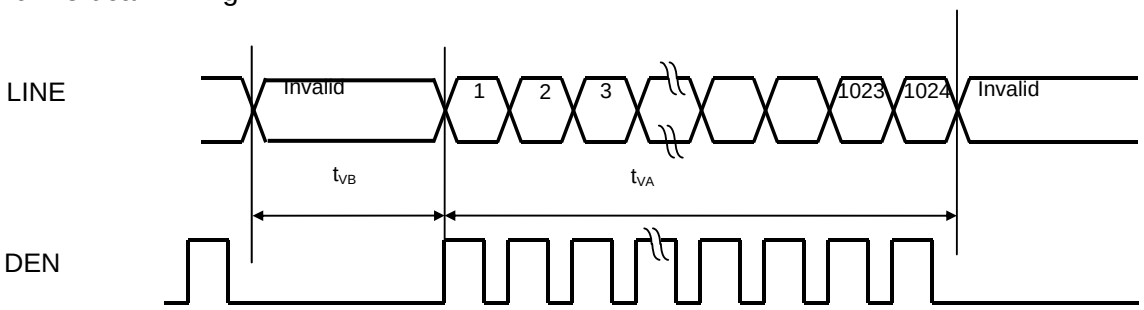
Pin No.	Pin Name	Require Signal	Pin No.	Pin Name	Require Signal
1	VCC	Power Supply for TTL Input	29	GND	Ground pin for TTL
2	D5	TTL Input (R7)	30	D26	TTL Input(DE)
3	D6	TTL Input (R5)	31	TxCLKIN	TTL Level clock Input
4	D7	TTL Input (G0)	32	PWR DWN	Power Down Input
5	GND	Ground pin for TTL	33	PLL GND	Ground pin for PLL
6	D8	TTL Input (G1)	34	PLL VCC	Power Supply for PLL
7	D9	TTL Input (G2)	35	PLL GND	Ground pin for PLL
8	D10	TTL Input (G6)	36	LVDS GND	Ground pin for LVDS
9	VCC	Power Supply for TTL Input	37	TxOUT3+	Positive LVDS differential data output 3
10	D11	TTL Input (G7)	38	TxOUT3-	Negative LVDS differential data output 3
11	D12	TTL Input (G3)	39	TxCLKOUT+	Positive LVDS differential clock output
12	D13	TTL Input (G4)	40	TxCLKOUT-	Negative LVDS differential clock output
13	GND	Ground pin for TTL	41	TxOUT2+	Positive LDVS differential data output 2
14	D14	TTL Input (G5)	42	TxOUT2-	Negative LVDS differential data output 2
15	D15	TTL Input (B0)	43	LVDS GND	Ground pin for LVDS
16	D16	TTL Input (B6)	44	LVDS VCC	Power Supply for LVDS
17	VCC	Power Supply for TTL Input	45	TxOUT1+	Positive LVDS differential data output 1
18	D17	TTL Input (B7)	46	TxOUT1-	Negative LVDS differential data output 1
19	D18	TTL Input (B1)	47	TxOUT0+	Positive LVDS differential data output 0
20	D19	TTL Input (B2)	48	TxOUT0-	Negative LVDS differential data output 0
21	GND	Ground pin for TTL	49	LVDS GND	Ground pin for TTL
22	D20	TTL Input (B3)	50	D27	TTL Input (R6)
23	D21	TTL Input (B4)	51	D0	TTL Input (R0)
24	D22	TTL Input (B5)	52	D1	TTL Input (R1)
25	D23	TTL Input (LVDS)	53	GND	Ground pin for TTL
26	VCC	Power Supply for TTL Input	54	D2	TTL Input (R2)
27	D24	TTL Input (HSYNC)	55	D3	TTL Input (R3)
28	D25	TTL Input (VSYNC)	56	D4	TTL Input (R4)

(2) Timing Chart

a. Horizontal Timing

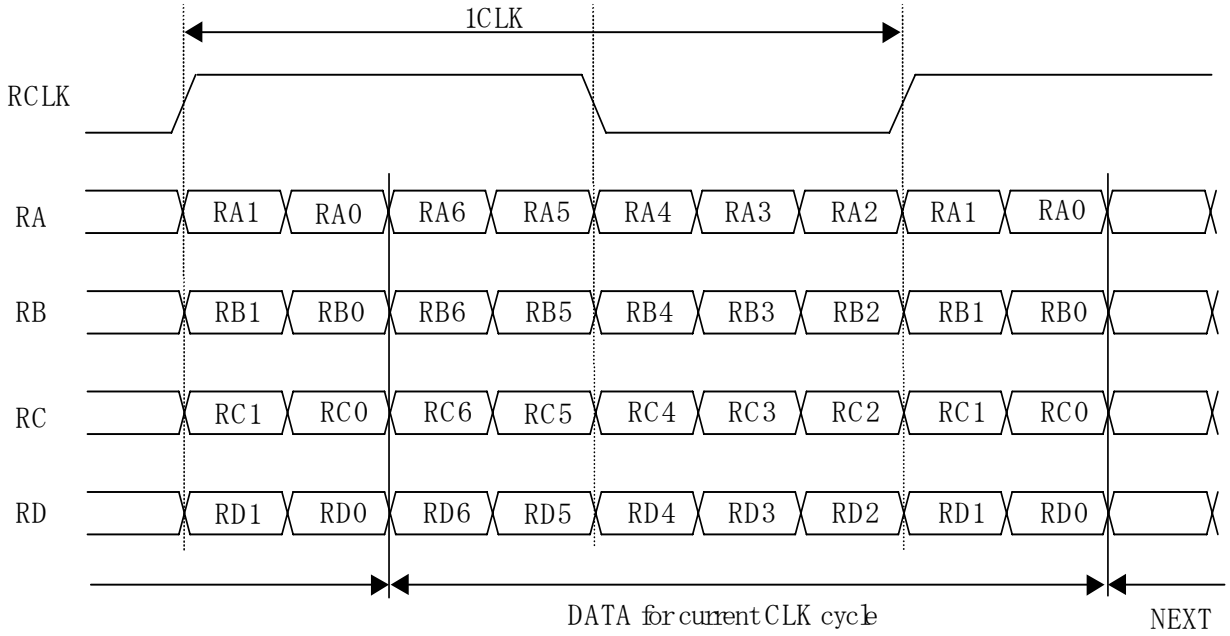


b. Vertical Timing



(3) LVDS DATA

(a) Timing Chart



(b) Data mapping

Cell	Input Pin *)	Data(6bit + FRC)
RA0	TxIN0	RI0
RA1	TxIN1	RI1
RA2	TxIN2	RI2
RA3	TxIN3	RI3
RA4	TxIN4	RI4
RA5	TxIN6	RI5
RA6	TxIN7	GI0
RB0	TxIN8	GI1
RB1	TxIN9	GI2
RB2	TxIN12	GI3
RB3	TxIN13	GI4
RB4	TxIN14	GI5
RB5	TxIN15	BI0
RB6	TxIN18	BI1
RC0	TxIN19	BI2
RC1	TxIN20	BI3
RC2	TxIN21	BI4
RC3	TxIN22	BI5
RC4	TxIN24	RSVD
RC5	TxIN25	RSVD
RC6	TxIN26	DENA
RD0	TxIN27	RI6
RD1	TxIN5	RI7
RD2	TxIN10	GI6
RD3	TxIN11	GI7
RD4	TxIN16	BI6
RD5	TxIN17	BI7
RD6	TxIN23	(RSVD)
Ref-RCLK	TxCLKIN	DCLKI

*)：DS90C383MTD

(4) Color Data Assignment

COLOR	INPUT DATA	R DATA								G DATA								B DATA							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENTA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	GREEN(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLUE(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

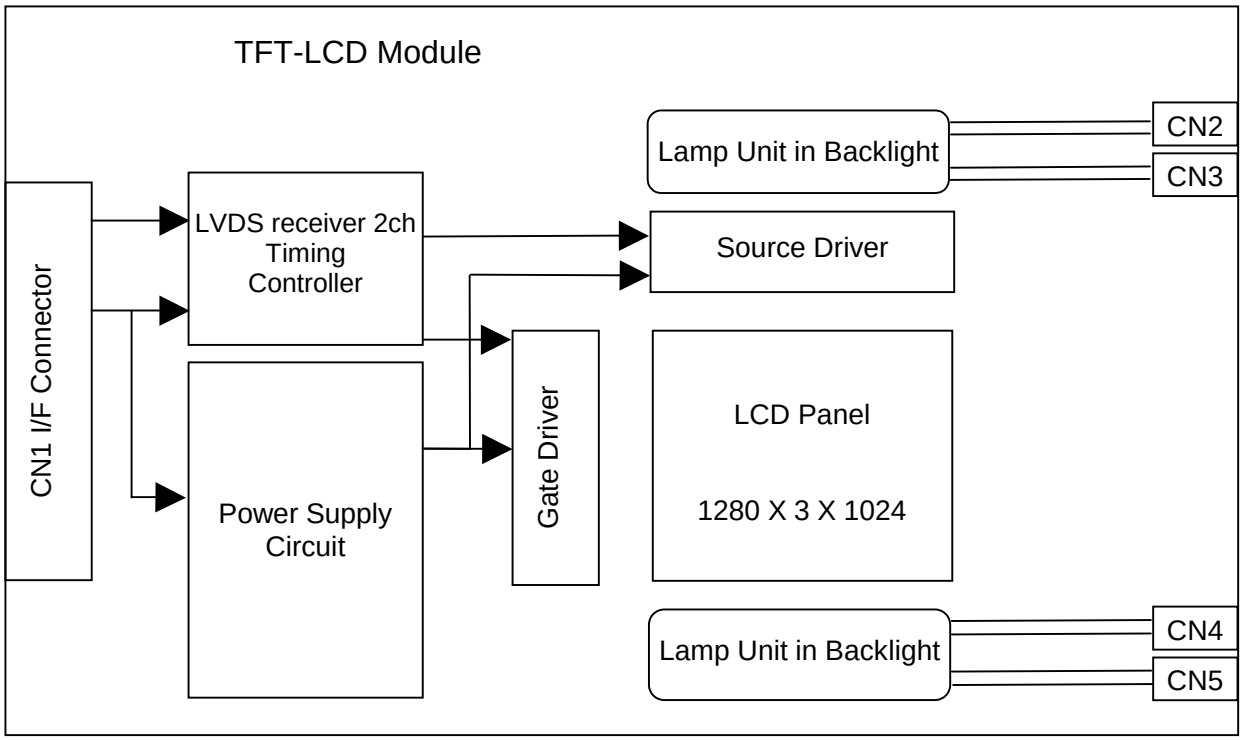
[Note]

1) Definition of gray scale: Color(n) : n indicates gray scale level.
   Higher n means brighter level.
2) Data:1-High,0-Low.
3) This assignment is applied to both odd and even data.

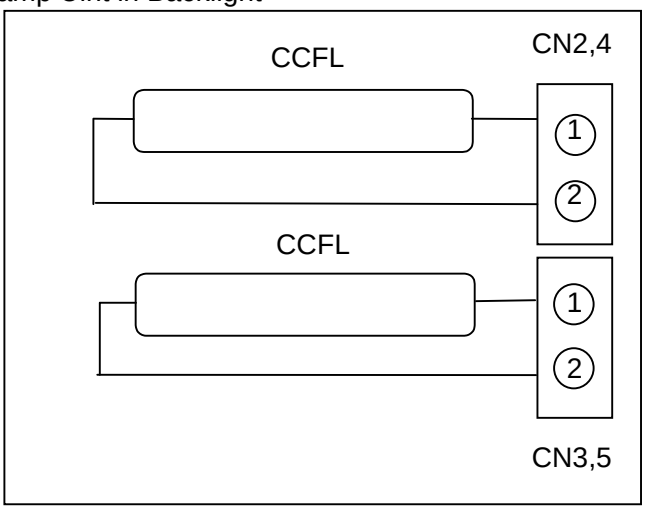
(5) Color Data Assignment

D(1,1)	D(2,1)	--	D(X,1)	--	D(1279,1)	D(1280,1)
D(1,2)	D(2,2)	--	D(X,2)	--	D(1279,2)	D(1280,2)
|	|	+	..	+	|	|
D(1,Y)	D(2,Y)	--	D(X,Y)	--	D(1279,Y)	D(1280,Y)
|	|	+	..	+	|	|
D(1,1023)	D(2, 1023)	--	D(X, 1023)	--	D(1279,1023)	D(1280,1023)
D(1,1024)	D(2, 1024)	--	D(X, 1024)	--	D(1279,1024)	D(1280,1024)

6. BLOCK DIAGRAM



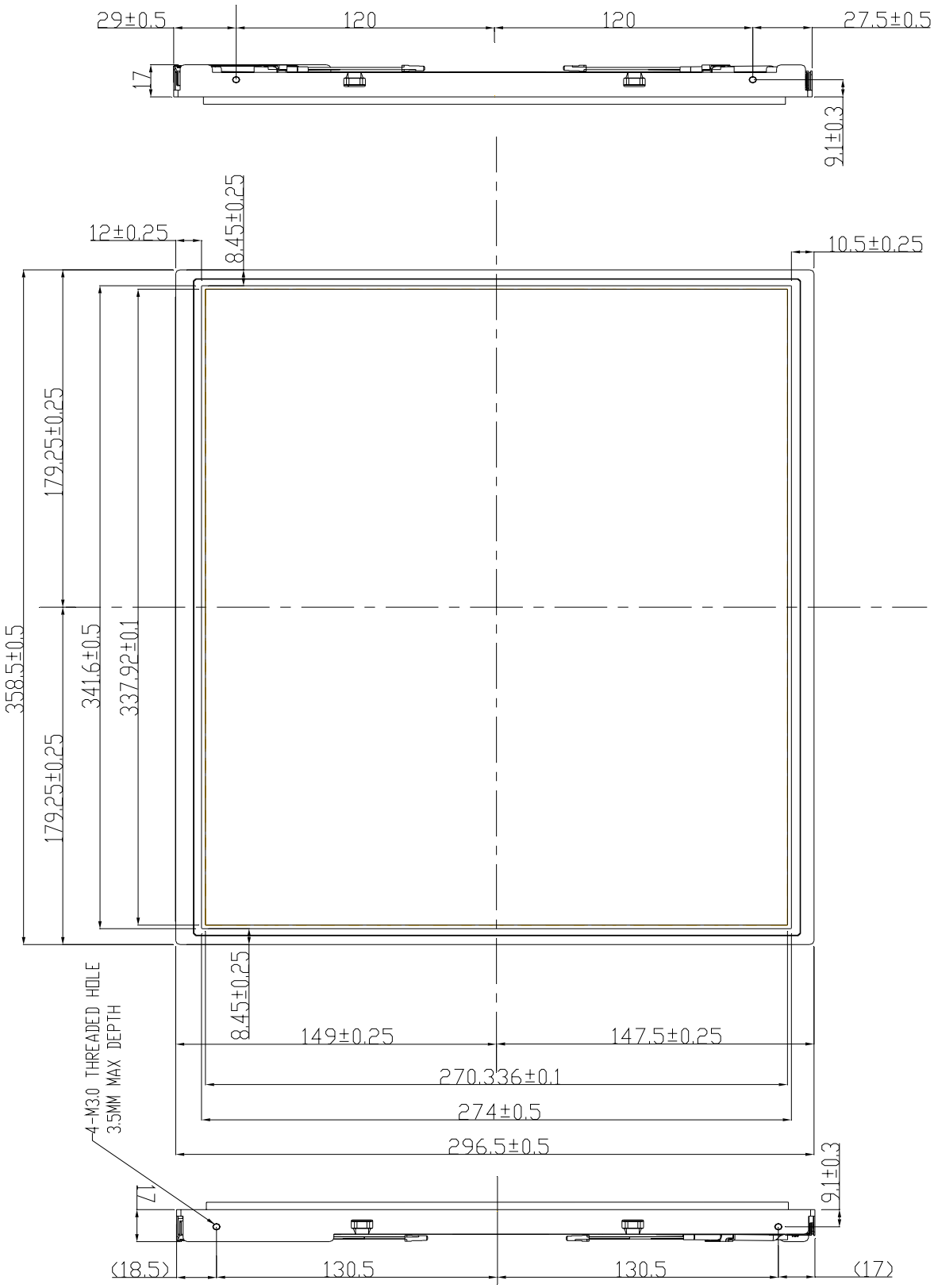
Lamp Uint in Backlight



7. MECHANICAL SPECIFICATION

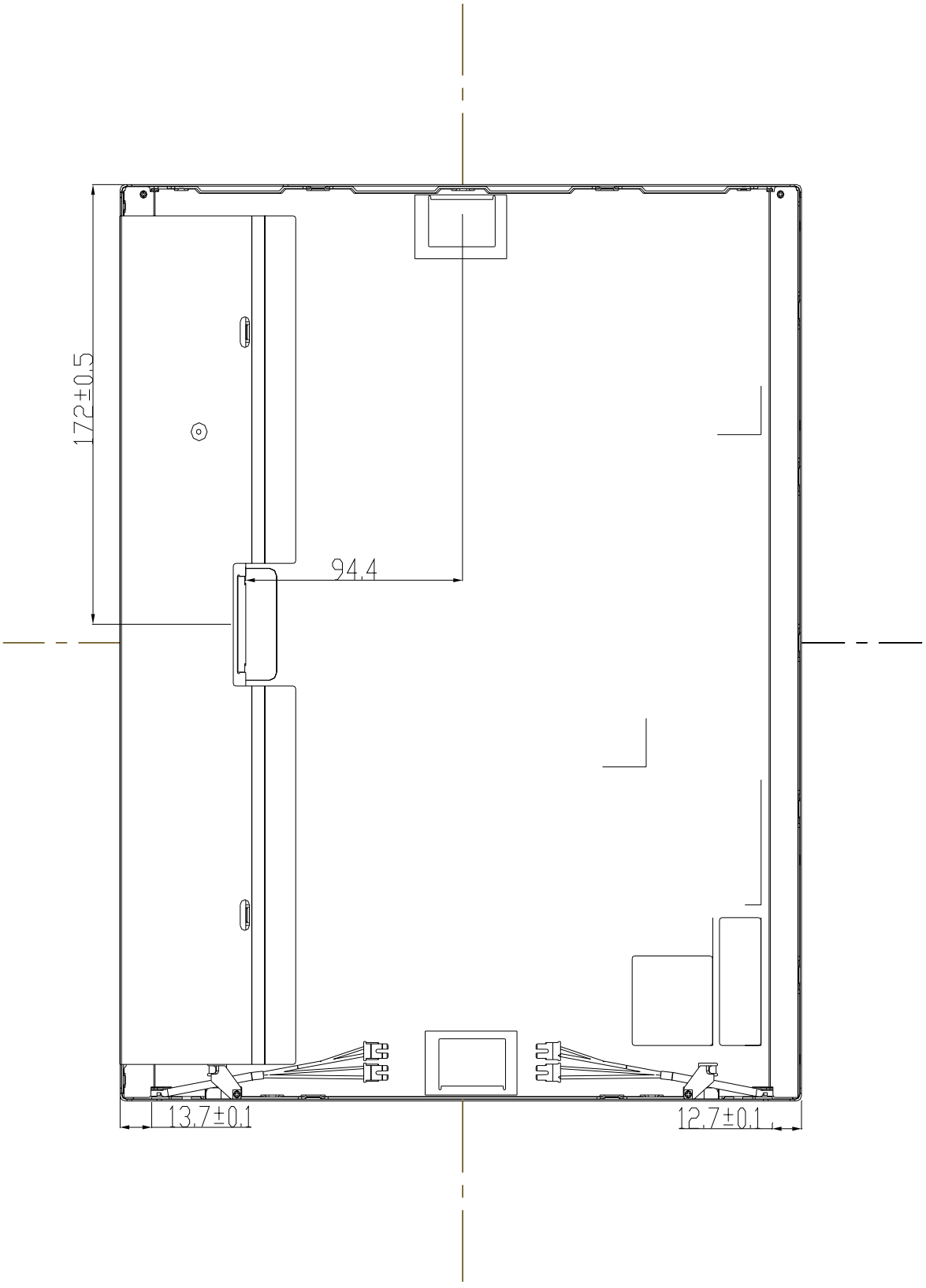
(1) Front side (Tolerance is ±0.5mm unless noted)

Unit: mm



(2) Rear side (Tolerance is ±0.5mm unless noted)

Unit: mm



8. OPTICAL CHARACTERISTICS

Ta=25℃，VCC=5.0V

ITEM		SYMBOL	CONDITION	min	typ	max	UNIT	REMARK
Contrast Ratio		CR	θ= ϕ= 0°	550	700	--	--	*1)
Luminance(CEN)		L	θ= ϕ= 0°	230	300	--	cd/m^2	*2)
9P Uniformity		ΔL	θ= ϕ= 0°	75	--	--	%	*2)
Response Time		Tr	θ= ϕ= 0°	--	1.5	4	ms	*4)
		Tf	θ= ϕ= 0°	--	3.5	6	ms	
Crosstalk		CT	θ= ϕ= 0°	0	--	1	%	*5)
Viewing Angle	Horizontal	ϕ	CR≧10	-70~70	-80~80	--	°	*3)
	Vertical	θ		-65~75	-75/85	--	°	
Color Coordinates	White	X Y	θ= ϕ= 0°	0.283 0.299	0.313 0.329	0.343 0.359	Color Coordinates	*2)
	Red	X Y		0.625 0.297	0.655 0.327	0.685 0.357		
	Green	X Y		0.243 0.587	0.273 0.617	0.303 0.647		
	Blue	X Y		0.114 0.049	0.144 0.079	0.174 0.109		
Gamut		CG	θ= ϕ= 0°	70	72	--	%	
Gamma		γ	VESA	2.0	2.2	2.4	--	*6)

[Note]

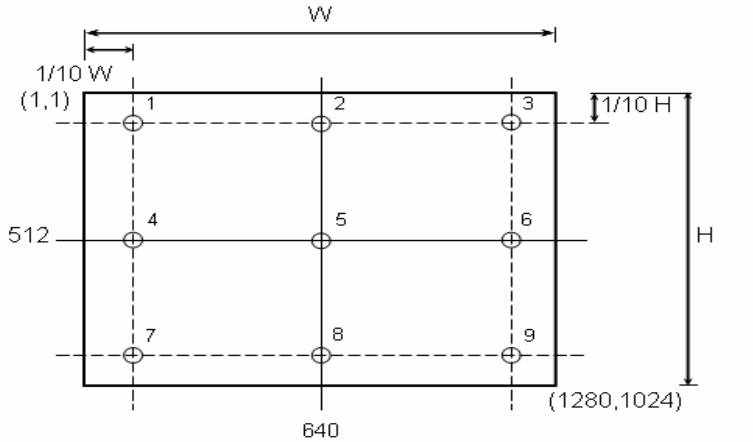
All optical specification condition:

(1) Equipment: BM-5A(TOPCON) under the dark room condition(2° view angle) after more than 30 minutes turning on the lamp

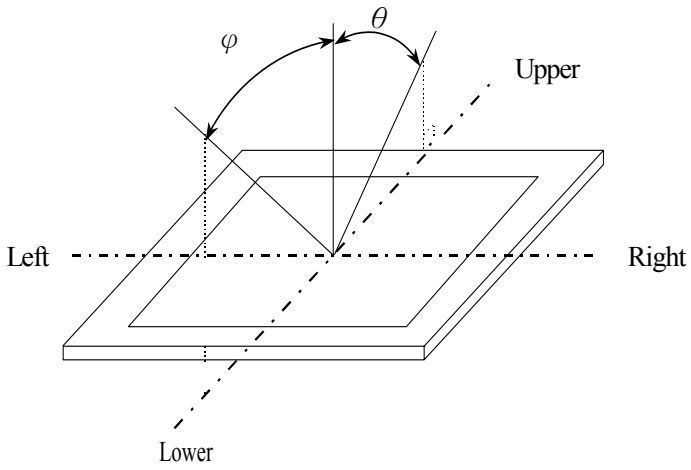
(2) Condition: IL=7.5 (each lamp)mA,
Inverter: SAMPO (DIVLCP0506D42), Frequency=50kHz.

*1) Defination of Contrast Ratio:
CR=ON (White) Luminance/OFF (Black) Luminance

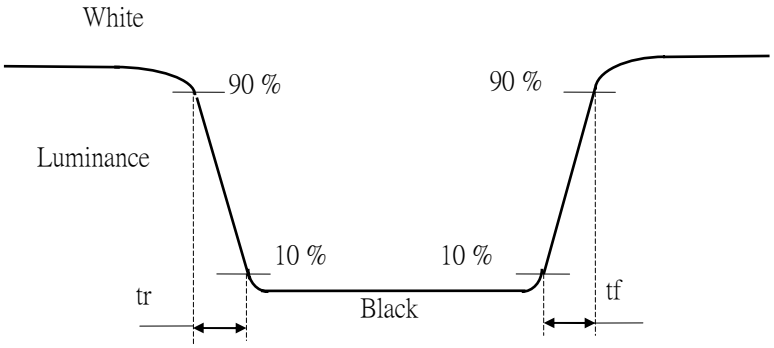
*2) Definition of Luminance and Luminance uniformity:
Center Luminance: measuring the luminance of the point no. 5
Average Luminance: measuring average luminance of points no.1-no.9
Uniformity: ΔL=[L(Min)/L(Max)]×100 %



*3) Definition of Viewing Angle(θ,ψ):



*4) Definition of Response Time:

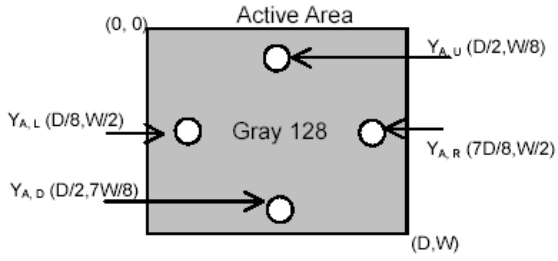


*5) Definition of crosstalk:

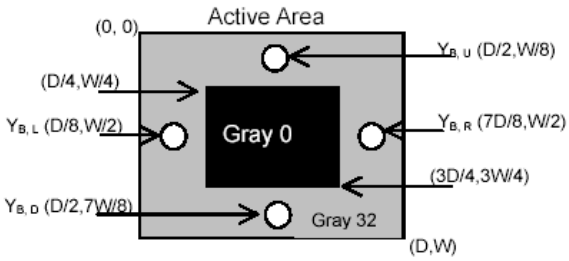
CT= | Y_B-Y_A | /Y_A X 100 (%)

Y_A : The luminance of measured position at pattern A

Y_B : The luminance of measured position at pattern B with Gray level 0

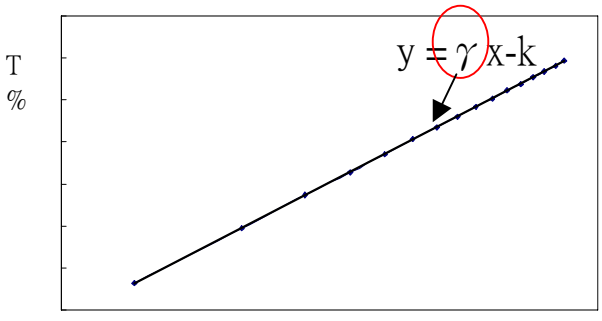


Pattern A



Pattern B

*6) Definition of Gamma (γ), follow VESA standard sampling every 16 gray level(0,16,32,…..224,240,255)



Gray level(LOG)

9.RELIABILITY TEST CONDITIONS

(1) Temperature and Humidity

TEST ITEMS	CONDITIONS
HIGH TEMPERATURE HIGH HUMIDITY OPERATION	50℃; 90%RH; 240h (No condensation)
HIGH TEMPERATURE HIGH HUMIDITY STORAGE	60℃; 90%RH;48h (No condensation)
HIGH TEMPERATURE OPERATION	50℃; 240h
HIGH TEMPERATURE STORAGE	60℃; 240h
LOW TEMPERATURE OPERATION	0℃; 240h
LOW TEMPERATURE STORAGE	-20℃; 240h
THERMAL SHOCK	BETWEEN -20℃(1hr)AND 60℃(1hr); 100 CYCLES

(2) Shock & Vibration

ITEMS	CONDITIONS
SHOCK (NON- OPERATION)	Shock level:1470m/s^2(150G) Waveform: half sinusoidal wave, 2ms Number of shocks: one shock input in each direction of three mutually perpendicular axes for a total of six shock inputs
VIBRATION (NON- OPERATION)	Vibration level: 9.8m/s^2(1.0G) zero to peak Waveform: sinusoidal Frequency range: 5 to 500 Hz Frequency sweep rate: 0.5 octave/min Duration: one sweep from 5 to 500Hz in each of three mutually perpendicular axis(each x,y,z axis: 1 hour, total 3 hours)

(3) ESD

POSITION	CONDITION(MDL turn off)
Connector	1. 200 pF，0 Ω，±250 V 2. contact mode for each pin
Moudle	1. 150 pF，330 Ω，±15K V 2. Air mode, test 25 times for each test point 3. Contact mode, 25 times for each test point

(4) Low Presure test

TEST ITEM	CONDITION
Low Presure test(storage)	260HPa (30000 ft.)；24 Hr

(5) Judgment standard

The judgment of the above test should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect. Partial transformation of the module parts should be ignored.

Fail: No display image, obvious non-uniformity, or line defects.

10. HANDLING PRECAUTIONS FOR TFT-LCD MODULE

Please pay attention to the followings in handling- TFT-LCD products;

(1) ASSEMBLY PRECAUTION

1) Please use the mounting hole on the module side in installing and do not beading or wrenching LCD in assembling. And please do not drop, bend or twist LCD module in handling.
2) Please design display housing in accordance with the following guide lines.
   a. Housing case must be destined carefully so as not to put stresses on LCD all sides and not to wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.
   b. Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. Approximately 1.0 mm of the clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.
   c. When some parts, such as, FPC cable and ferrite plate, are installed underneath the LCD module, still sufficient clearance is required, such as 0.5mm. This clearance is, especially, to be reconsidered when the additional parts are implemented for EMI countermeasure.
   d. Design the inverter location and connector position carefully so as not to give stress to lamp cable, or not to interface the LCD module by the lamp cable.
   e. Keep sufficient clearance between LCD module and the others parts, such as inverter and speaker so as not to interface the LCD module. Approximately 1.0mm of the clearance in the design is recommended.
3) Please do not push or scratch LCD panel surface with any-thing hard. And do not soil LCD panel surface by touching with bare hands. (Polarizer film, surface of LCD panel is easy to be flawed.)
4) Please do not press any parts on the rear side such as source TCP, gate TCP, control circuit board and FPCs during handling LCD module. If pressing rear part is unavoidable, handle the LCD module with care not to damage them.
5) Please wipe out LCD panel surface with absorbent cotton or soft cloth in case of it being soiled.
6) Please wipe out drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.
7) Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.
8) Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.
9) Please pay attention to handling lead wire of backlight so that it is not tugged in connecting wit inverter.

(2) OPERATING PRECAUTIONS

1) Please be sure to turn off the power supply before connecting and disconnecting signal input cable.
2) Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification.
3) Please consider that LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.
4) A condensation might happen on the surface and inside of LCD module in case of sudden charge of ambient temperature.
5) Please pay attention to displaying the same pattern for very long time. Image might stick on LCD. If then, time going on can make LCD work well.

6) Please obey the same caution descriptions as ones that need to pay attention to ordinary electronic parts.

(3) PRECAUTFONSWITHELECTROSTATICS

1) This LCD module use CMOS-IC on circuit board and TFT-LCD panel, and so it is easy to be affected by electrostatics. Please be careful with electrostatics by the way of your body connecting to the ground and so on.
2) Please remove protection film very slowly on the surface of LCD module to prevent from electrostatics occurrence.

(4) STORAGE PRECAUTIONS

1) When you store LCDs for a long time, it is recommended to keep the temperature between 0℃ ~40℃ without the exposure of sunlight and to keep the humidity less than 90%RH.
2) Please do not leave the LCDs in the environment of high humidity and high temperature such as 60℃ 90%RH.
3) Please do not leave the LCDs in the environment of low temperature; below -20℃.

(5) SAFETY PRECAUTIONS

1) When you waste LCDS, it is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
2) If any liquid leaks out of a damaged-glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

(6) OTHERS

1) A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight Land strong UV rays.
2) Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
3) For the. packaging box, please pay attention to the followings:
   a. Packaging box and inner case for LCD are designed to protect the LCDs from the damage or scratching during transportation. Please do not open except picking LCDs up from the box.
   b. Please do not pile them up more than 5 boxes. (They are not designed so.) And please do not turn over.
   c. Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
   d. Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)