( ) Preliminary Specifications
(v) Final Specifications

Module	**11.6”(11.58”) FHD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	B116HAN03.1(H/W: 0A)
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**
Checked & Approved by	**Date**

Approved by	**Date**
Kevin KH Shen	02/26/2012
Prepared by	
Erica YT Lin	02/26/2012

Note: This Specification is subject to change without notice.

MPBU Marketing Division
AU Optronics corporation

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2012/3/19	All	First Edition for Customer		
0.2 2012/4/02	5.26	First Edition for Customer	Update gerneral spec/ Connector part number/ 2D drawing	
0.3 2012/8/24	5	Update Support Color Update Max thickness Update Max Power Consumption		
	6	Update RGB color croodinates		
	6	Update view angle		
	11	Update Functional Block Diagram		
	13	Update Power Specification		
	14	Update Display port main link		
	15	Update LED characteristic		
	16	Update Backlight input signal characteristics		
	25	Update 2D drawing		
0.4 2012/12/19	5		Update Pixel Pitch	
1.0 2013/02/26		Final version release		
	5	I_{LED}=21mA	I_{LED}=23mA	
	12		Remove touch function	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B116HAN03.1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HDTV, 1920(H) x1080(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B116HAN03.1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	293.83 (11.6W")			
Active Area	[mm]	256.32(H) x 144.18(V)			
Pixels H x V		1920 x 3(RGB) x 1080			
Pixel Pitch	[mm]	0.1335 X 0.1335			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (I_{LED}=23mA) **(Note: ILED is LED current)**	[cd/m^2]	400 typ. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		800 typ			
Response Time	[ms]	25 typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4W max. (Include Logic and Blu power)			
Weight	[Grams]	170 max.(W/O digitizer)			
Physical Size (panel only) **without bracket**	[mm]		Min.	Typ.	Max.
		Length		270.37	
		Width		159.79	
		Thickness	---	---	4.9
Electrical Interface		2 lane eDP			
Glass Thickness	[mm]	0.25			
Surface Treatment(panel only)		Anti-Glare, Hardness 3H			

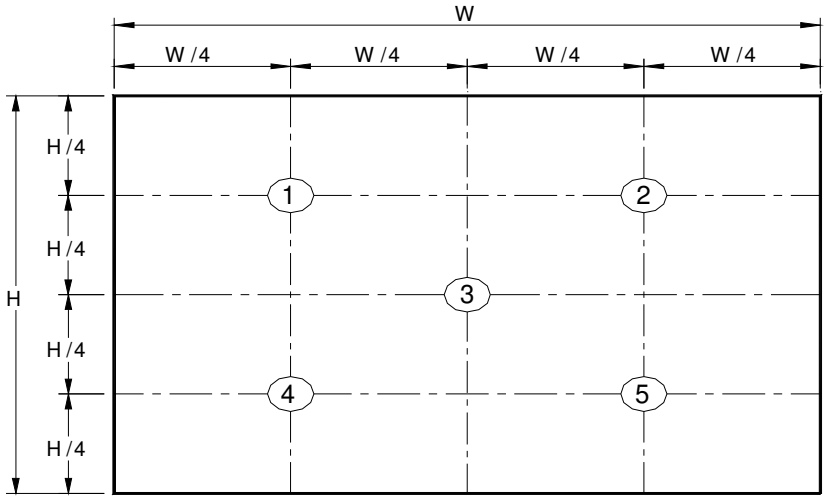
Support Color		RGB 8-bit
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

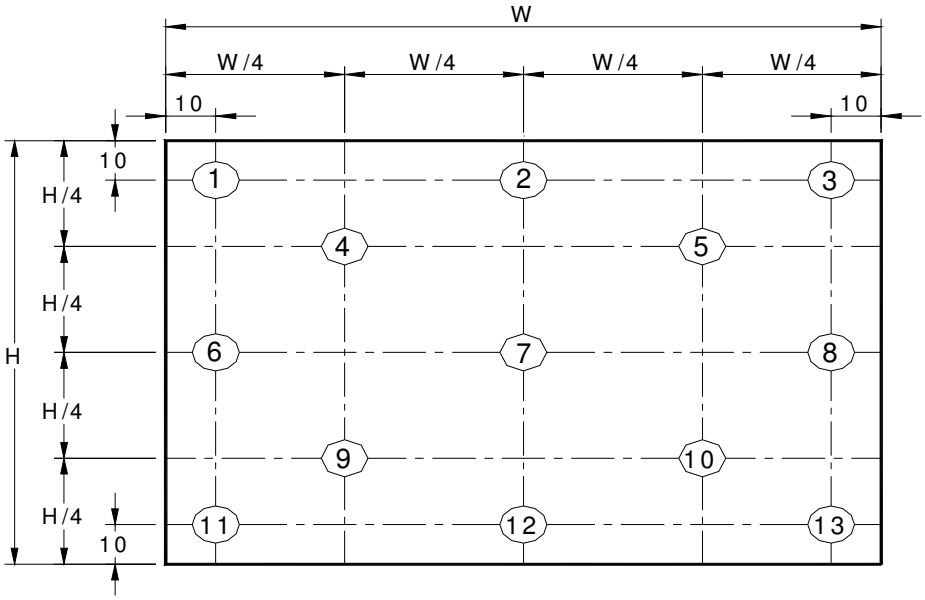
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=21mA			5 points average		400	---	cd/m²	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)		89 89	--- ---	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)		89 89	--- ---		
Luminance Uniformity		δ_{5P}	5 Points	---	---	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	---	---	1.5		2, 3, 4
Contrast Ratio		CR			800	-		4, 6
Cross talk		%		---	---	4		4, 7
Response Time		T_{RT}	Rising + Falling	---	30	45	msec	4, 8
Color / Chromaticity Coordinates	Red	Rx	CIE 1931	0.566	0.596	0.626		4
		Ry		0.316	0.346	0.376		
	Green	Gx		0.297	0.327	0.357		
		Gy		0.558	0.588	0.618		
	Blue	Bx		0.123	0.153	0.183		
		By		0.098	0.128	0.158		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	52	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

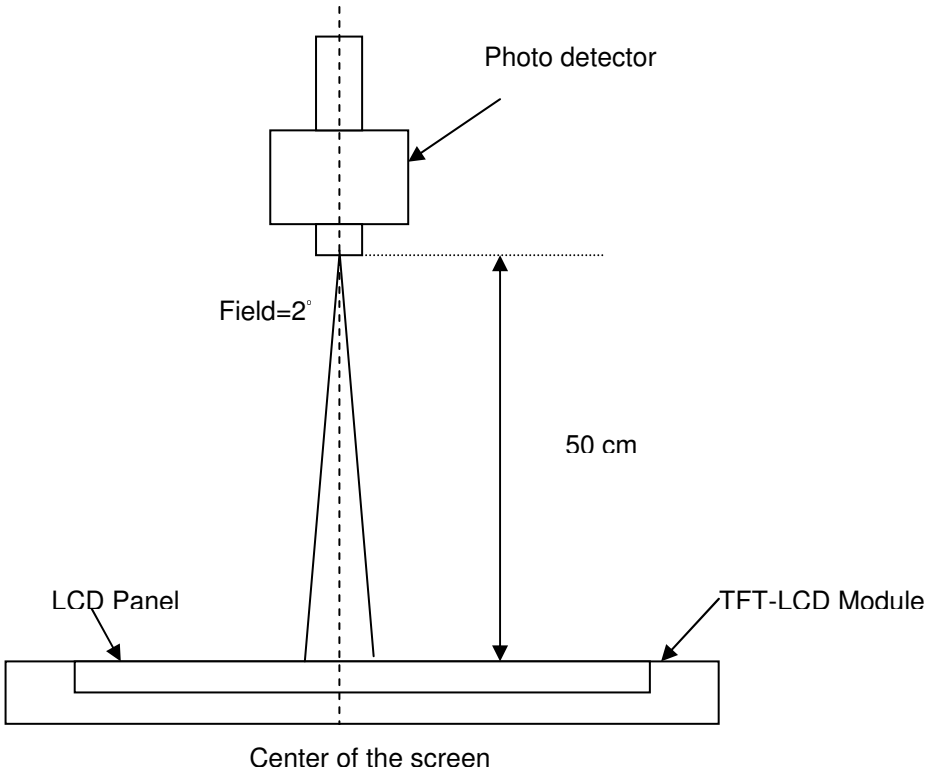
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

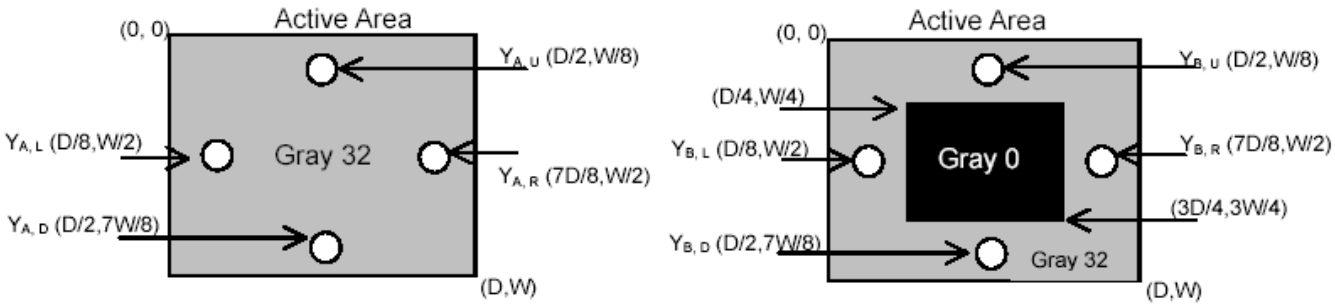
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

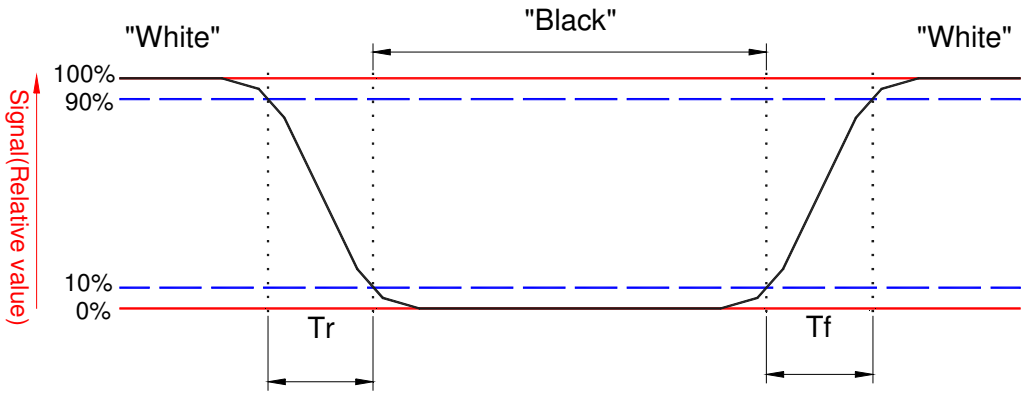
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



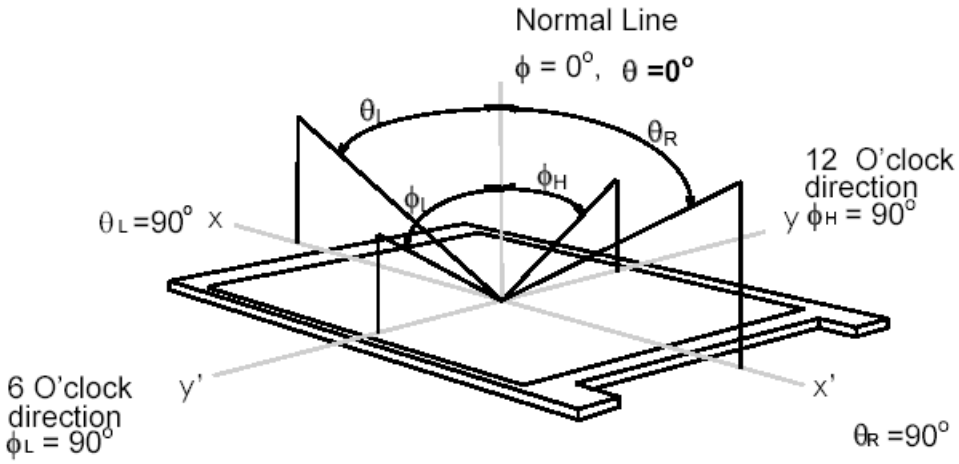
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



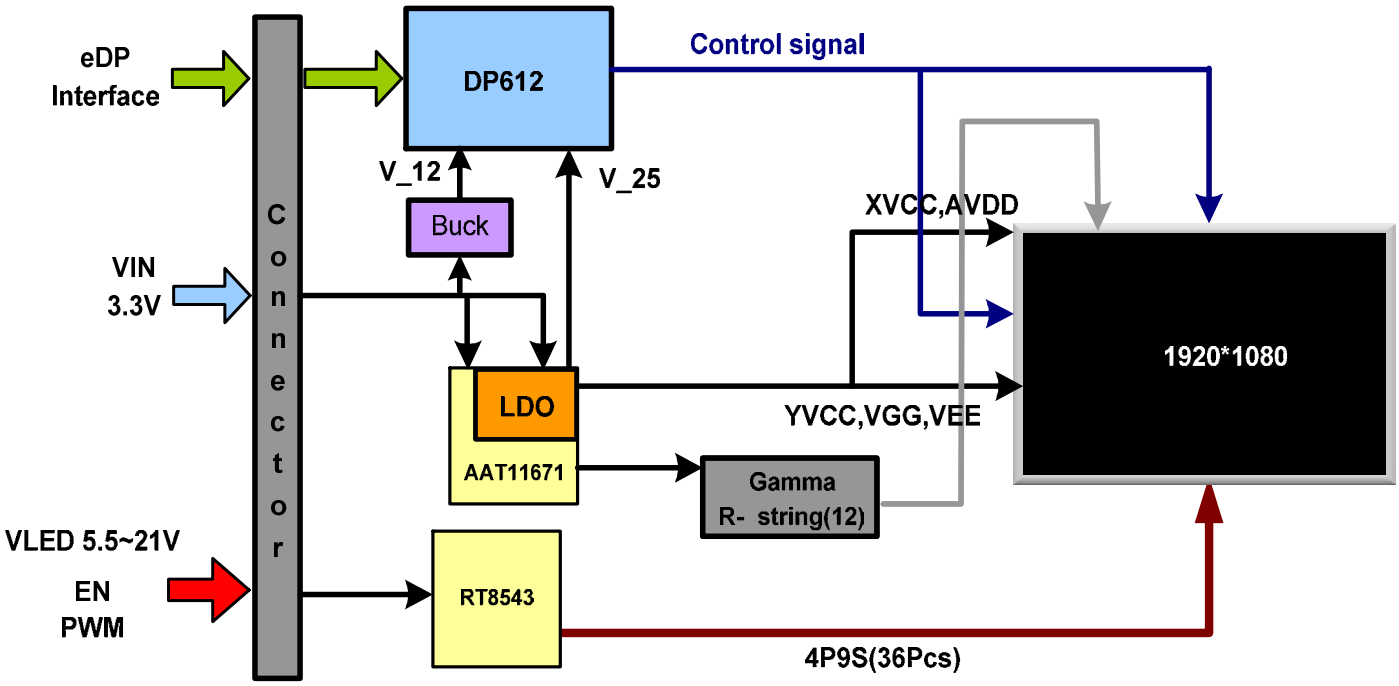
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 40 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

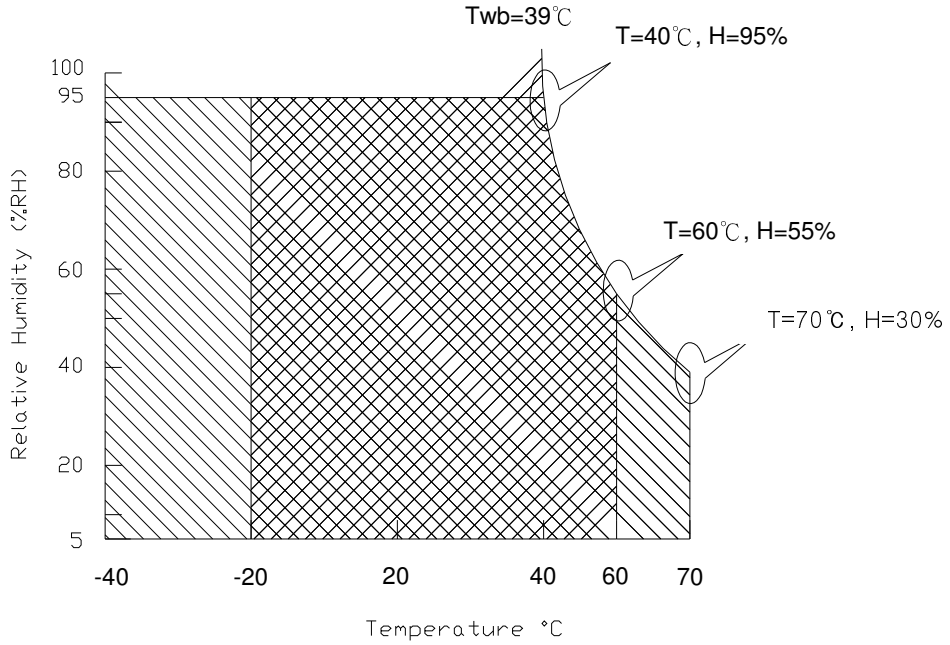
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

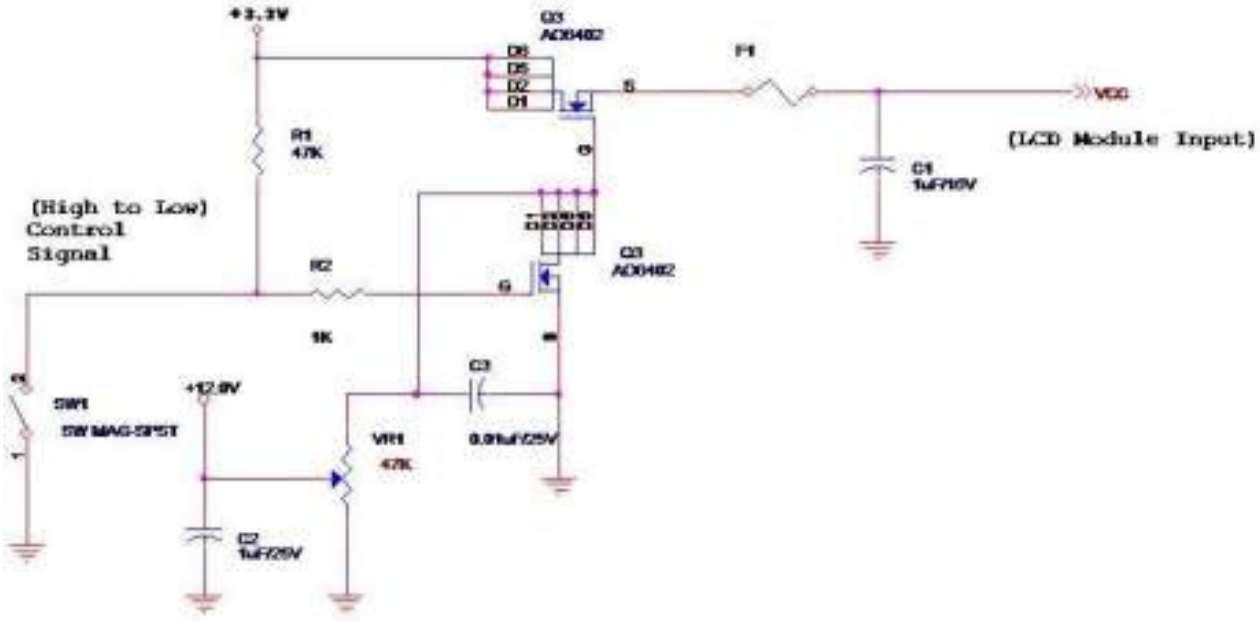
Input power specifications are as follows;

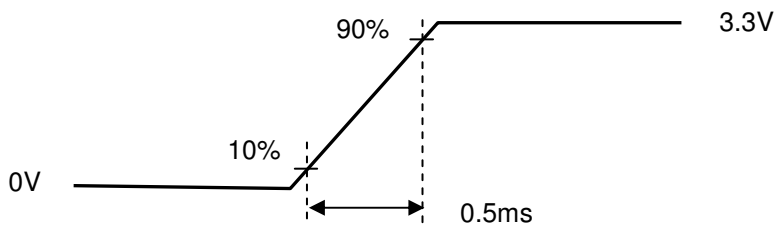
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1	[Watt]	Note 1
IDD	IDD Current	-	-	270	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2 : Measure Condition





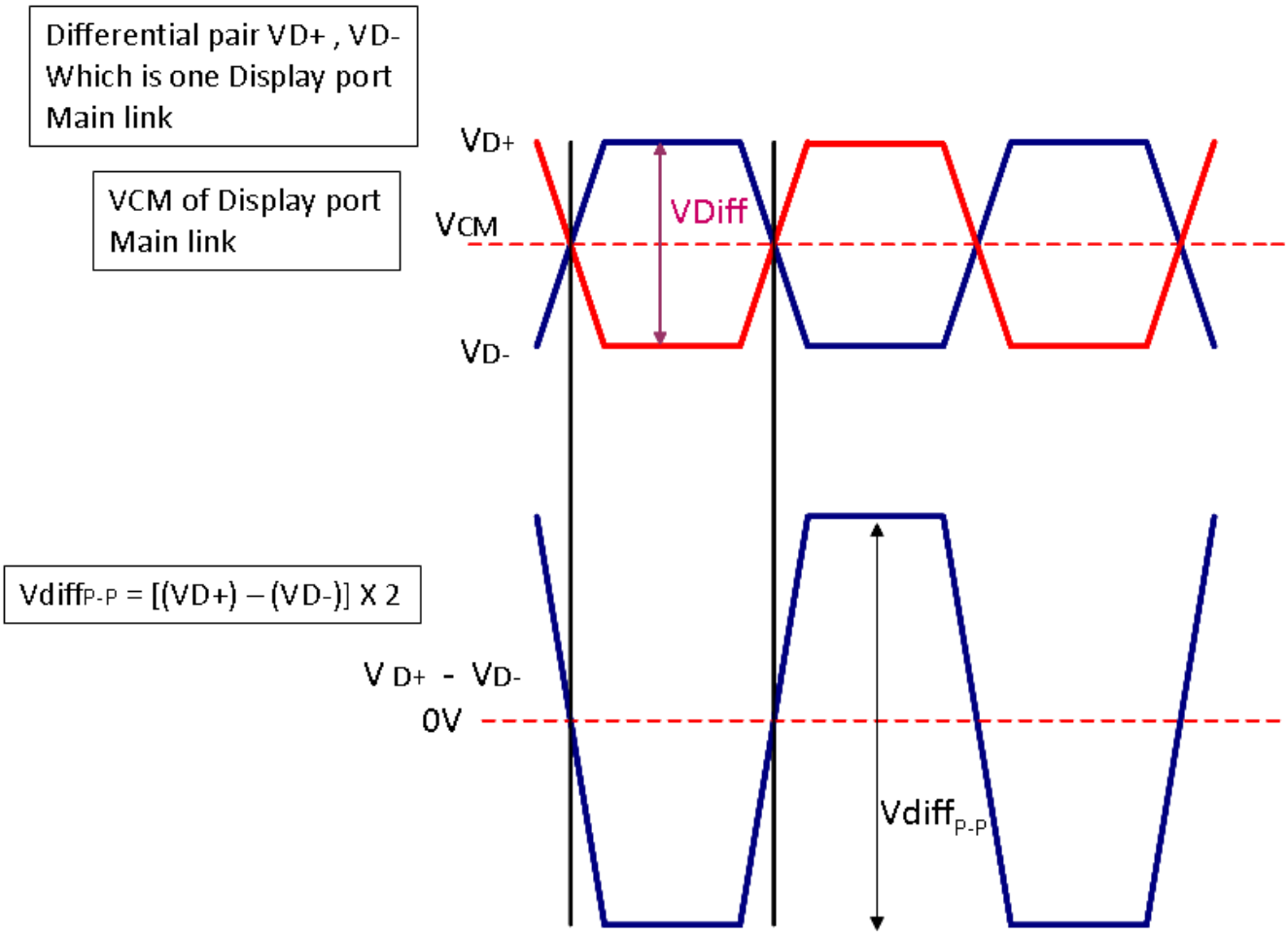
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

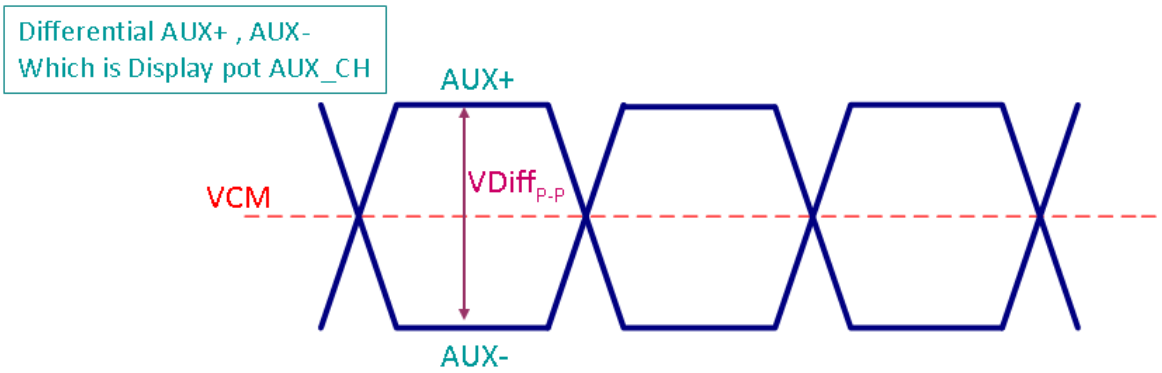
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	340		1320	mV

Follow as VESA display port standard V1.1a.

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Follow as VESA display port standard V1.1a.

Display Port V_{HPD} signal:

Display Port V_{HPD}					
		Min	Typ	Max	unit
V_{HPD}	HPD voltage	2.25		3.6	V

Follow as VESA display port standard V1.1a.

5.3 Backlight Unit

5.3.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	3.03	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25℃), Note 2 I_F=23 mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

Note 3: LED Forward Current 23 mA per string, total 92mA / LED Forward Voltage 27V typ / LED Array 4parallel * 9series

Note 4: LED driver IC Vender - Richtek

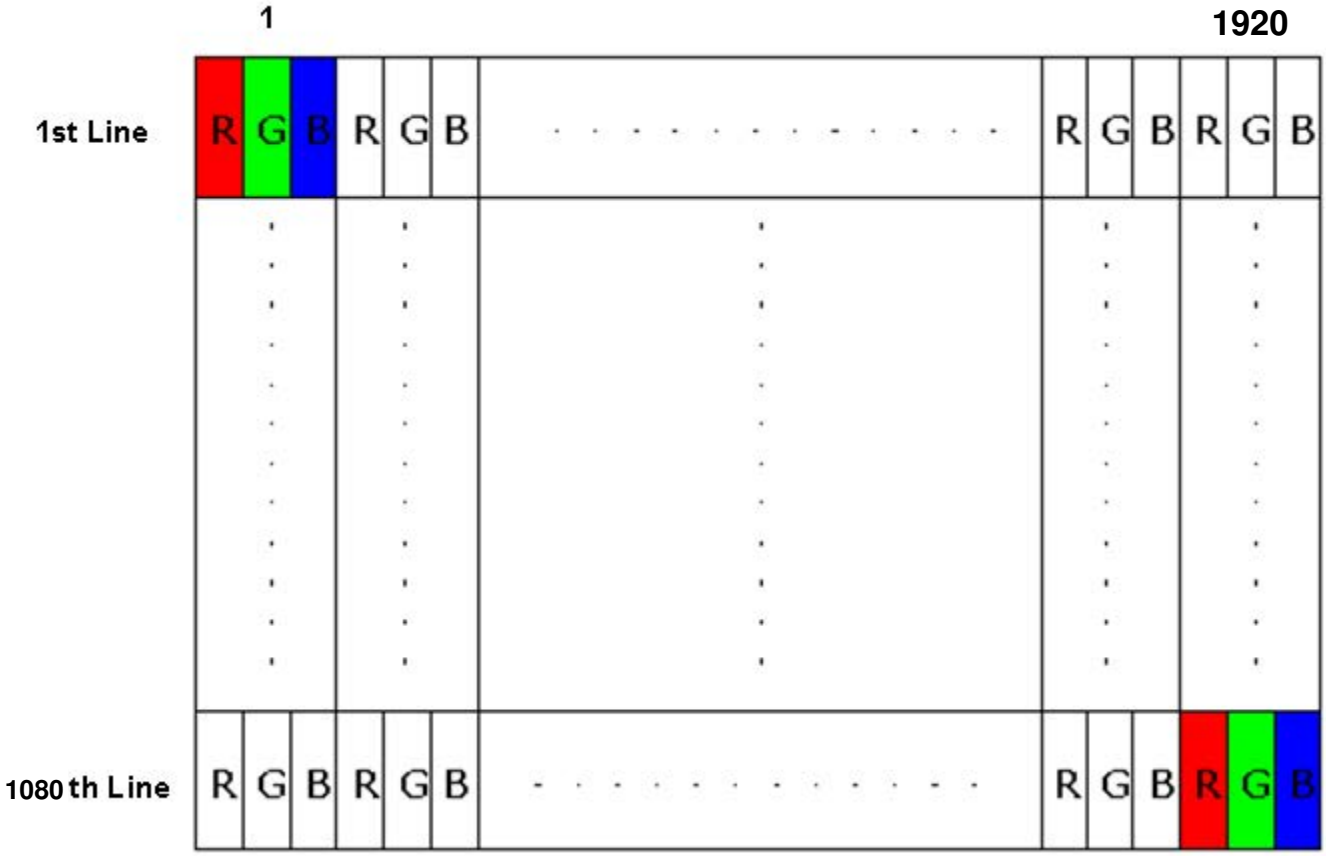
5.3.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.5	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
PWM Logic Input High Level	VPWM_EN	2.5	3.3	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	200	6K	15K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

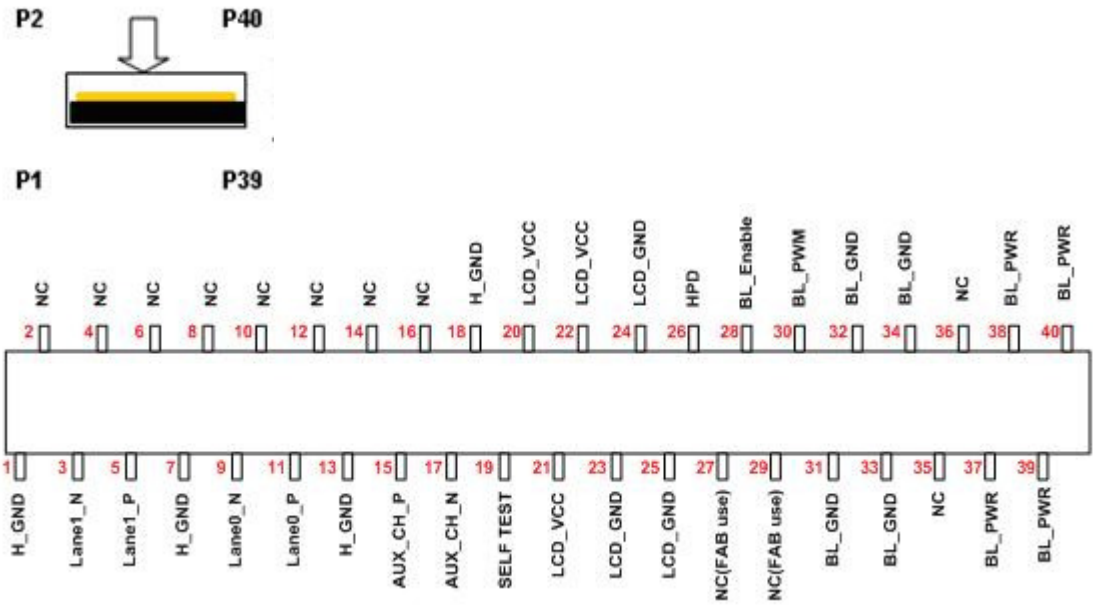
Connector Name / Designation	For Signal Connector
Manufacturer	DDK
Type / Part Number	FF12-40A-R12BN-D3
ting Housing/Part Number	FPC Cable

6.2.2 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
P1	H_GND	High Speed Ground
P2	NC	No Connect
P3	Lane1_N	Comp Signal Link Lane 1
P4	NC	No Connect
P5	Lane1_P	True Signal Link Lane 1
P6	NC	No Connect
P7	H_GND	High Speed Ground
P8	NC	No Connect
P9	Lane0_N	Comp Signal Link Lane 0
P10	NC	No Connect
P11	Lane0_P	True Signal Link Lane 0
P12	NC	No Connect
P13	H_GND	High Speed Ground
P14	NC	No Connect
P15	AUX_CH_P	True Signal Auxiliary Ch.
P16	NC	No Connect
P17	AUX_CH_N	Comp Signal Auxiliary Ch.
P18	H_GND	High Speed Ground
P19	LCD_Self_Test	LCD Panel Self Test Enable
P20	LCD_VCC	LCD logic and driver power

P21	LCD_VCC	LCD logic and driver power
P22	LCD_VCC	LCD logic and driver power
P23	LCD_GND	LCD_ground
P24	LCD_GND	LCD_ground
P25	LCD_GND	LCD_ground
P26	HPD	HPD signale pin
P27	NC	AUO FAB use EDID_DATA
P28	BL_Enable	LED driver IC enable
P29	NC	AUO FAB use EDID_CLK
P30	BL_PWM	LED driver IC PWM
P31	BL_GND	Backlight_ground
P32	BL_GND	Backlight_ground
P33	BL_GND	Backlight_ground
P34	BL_GND	Backlight_ground
P35	NC	No Connect
P36	NC	No Connect
P37	BL_PWR	Backlight power (5.5V~21V)
P38	BL_PWR	Backlight power (5.5V~21V)
P39	BL_PWR	Backlight power (5.5V~21V)
P40	BL_PWR	Backlight power (5.5V~21V)



6.4 Interface Timing

6.4.1 Timing Characteristics

Basically, interface timings should match the 1920 x 1080 /70.7 Hz manufacturing guide line timing.

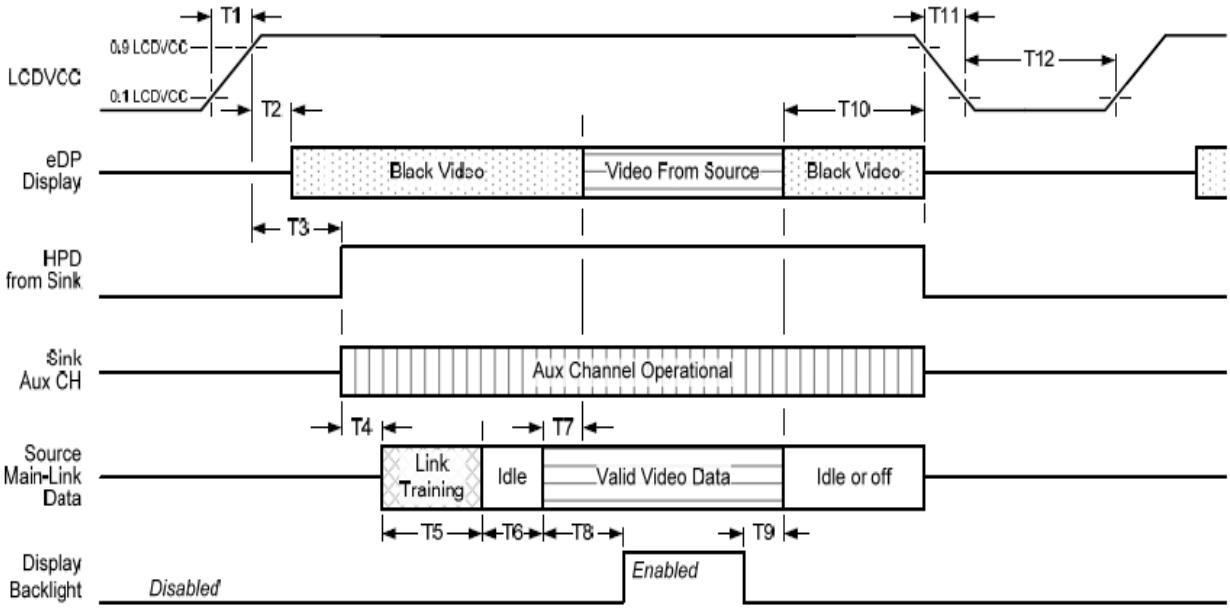
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	50	60	---	Hz
Clock frequency		1/ T_{Clock}		70.7		MHz
Vertical Section	Period	T_V	1084	1118	1380	T_{Line}
	Active	T_{VD}		1080		
	Blanking	T_{VB}	4	38	300	
Horizontal Section	Period	T_H	2000	2108	2320	T_{Clock}
	Active	T_{HD}		1920		
	Blanking	T_{HB}	80	188	400	

Note1 : The above is as optimized setting
Note2 : DE mode only
Note3 : The maximum clock frequency = [(1920 + B)*(1080+A)*60]/2 < 80MHz
Note4 : Clock frequency number is for reference, real setting value refer to EDID (Clock frequency 70.7 MHz)

6.5 Power On Sequence

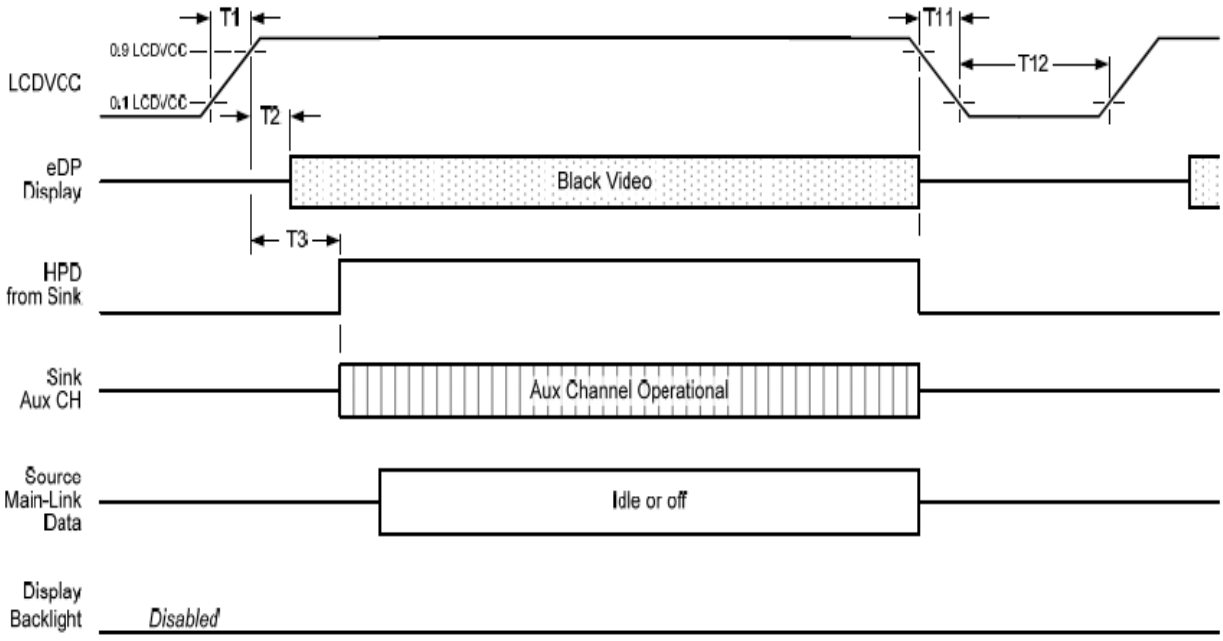
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note 1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the

source (at the end of T9).

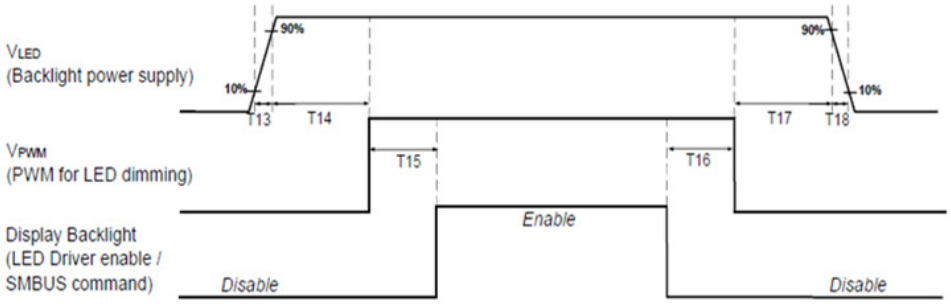
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

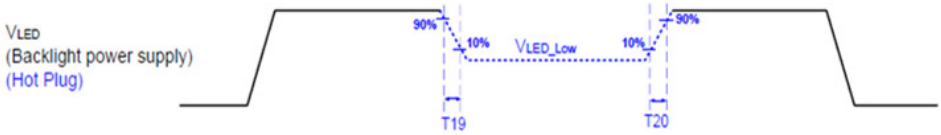
Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Note 4 : T8,T9,T10,T11 value are recommended, T8,T9,T10,T11 $\geqq$ 0 could be acceptable

Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

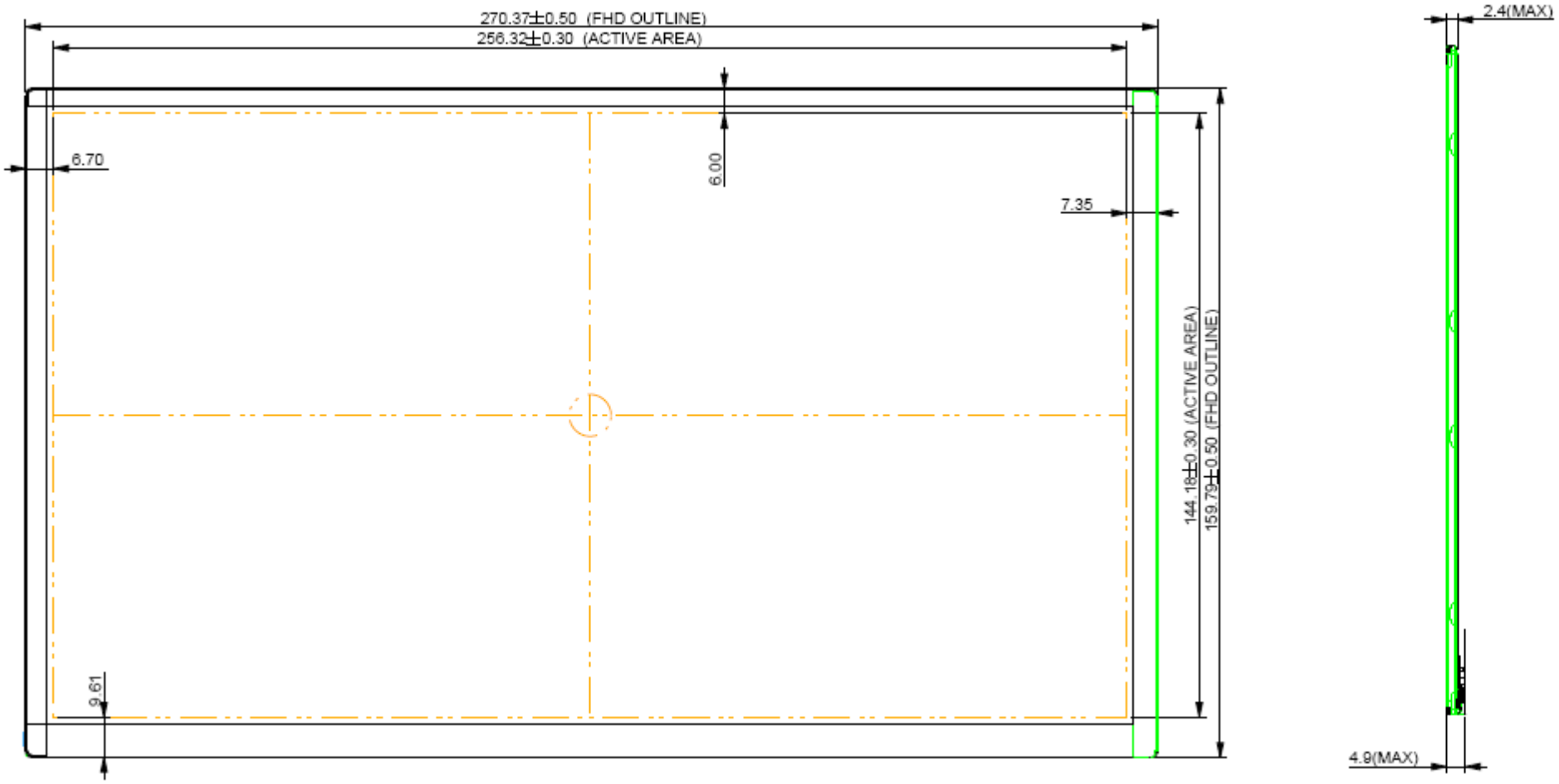
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 300h	
Low Temperature Storage	Ta= -20℃, 300h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

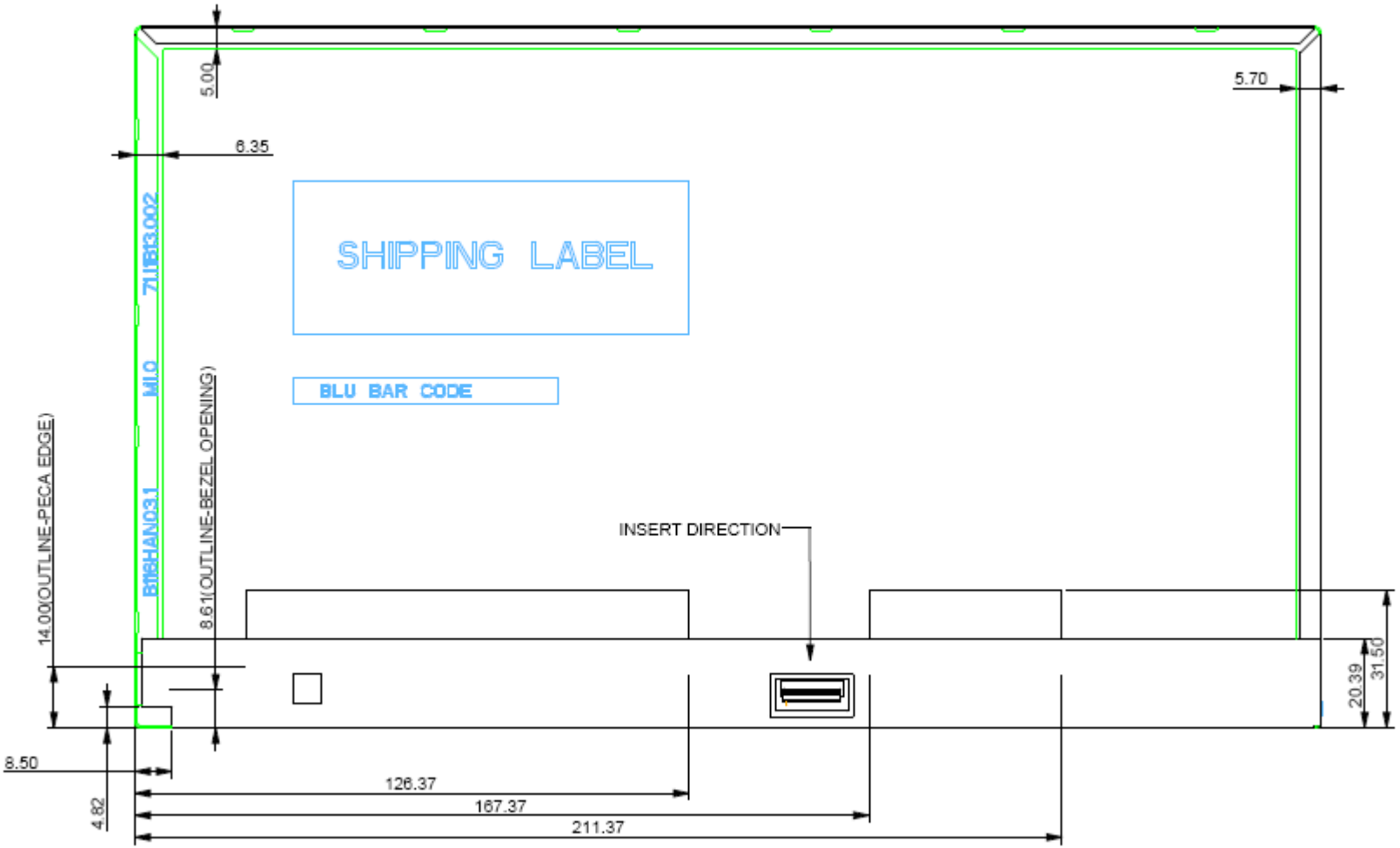
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1.1 Standard Front View



8.1.2 Standard Back View



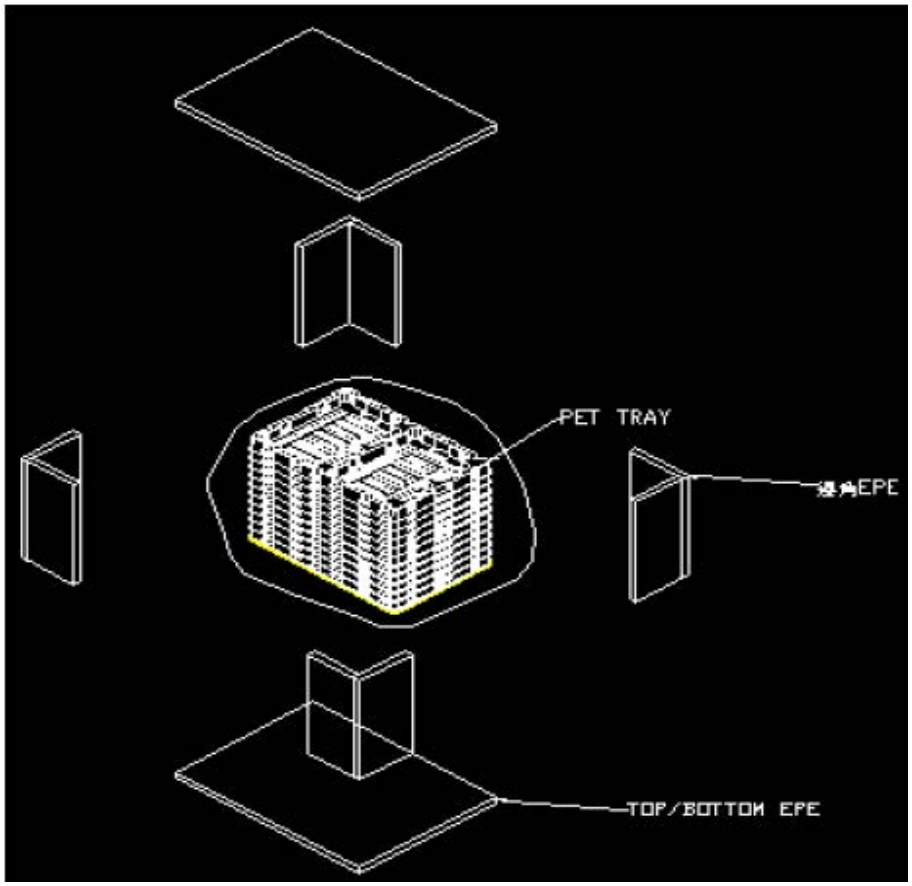
9. Shipping and Package

9.1 Shipping Label Format

Shipping label

Carton Label

9.2 Carton Package



9.3 Shipping Package of Palletizing Sequence