(V) Preliminary Specifications
( ) Final Specifications

Module	11.6"(11.57") HD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B116XTN01.0 (H/W:1A)
Note ( )	*LED Backlight with driving circuit design*

Customer	Date		Approved by	Date
Checked & Approved by	**Date**		**Prepared by**	**Date**
			Henry Chen	2013/12/20
Note: This Specification is subject to change without notice.			**NBBU Marketing Division** **AU Optronics corporation**	

Product Specification
AU OPTRONICS CORPORATION

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Record of Revision

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1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.

7) Do not open nor modify the Module Assembly.

8) Do not press the reflector sheet at the back of the module to any directions.

9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.

11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.

13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B116XTN01.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B116XTN01.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	293.8			
Active Area	[mm]	256.125 X 144.0			
Pixels H x V		1366x3(RGB) x 768			
Pixel Pitch	[mm]	0.1875X0.1875			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (I_{LED}=18mA) $(I_{LED}=18mA)$ **(Note: ILED is LED current)**	[cd/m²]	220 typ. (5 points average) 187 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		500 typ.			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	2.6 max**.** (Include Logic and BLU power)			
Weight	[Grams]	235 max.			
Physical Size **Include bracket**	[mm]		Min.	Typ.	Max.
		Length	277.5	278.0	278.5
		Width	167.5	168.0	168.5
		Thickness	-	-	3.6
Electrical Interface		1 Lane eDP			
Glass Thickness	[mm]	0.5			
Surface Treatment		Antei-Glare, Hardness 3H			
Support Color		262K colors (RGB 6-bit)			

| Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=18mA			5 points average	187	220	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	40 40	45 45	- -	degree	4, 9
		ϕ_H ϕ_L	Vertical (Upper) CR = 10 (Lower)	10 30	15 35	- -		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio		CR		-	500	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_r	Rising	-	3	-	msec	4, 8
		T_f	Falling	-	5	-		
		T_{RT}	Rising + Falling	-	8	16		
Color / Chromaticity Coodinates	**Red**	Rx	CIE 1931	TBD	TBD	TBD		4
		Ry		TBD	TBD	TBD		
	Green	Gx		TBD	TBD	TBD		
		Gy		TBD	TBD	TBD		
	Blue	Bx		TBD	TBD	TBD		
		By		TBD	TBD	TBD		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	45	-		

Note 1: 5 points position (Ref: Active area)
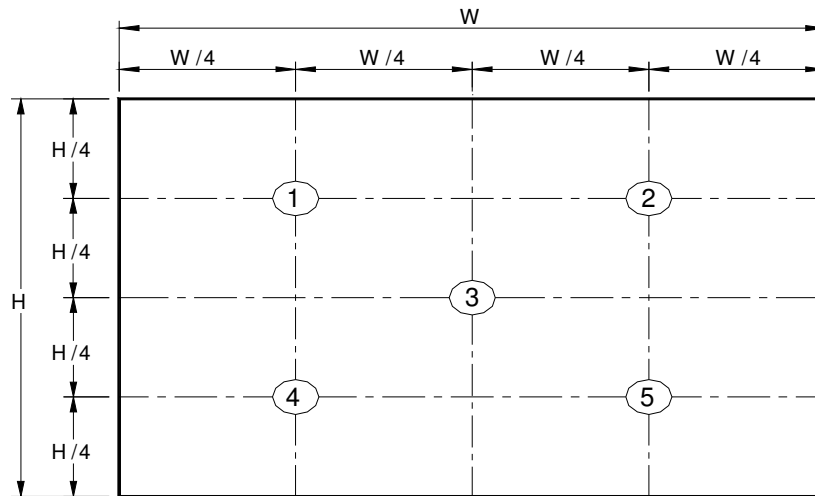
Note 2: 13 points position (Ref: Active area)
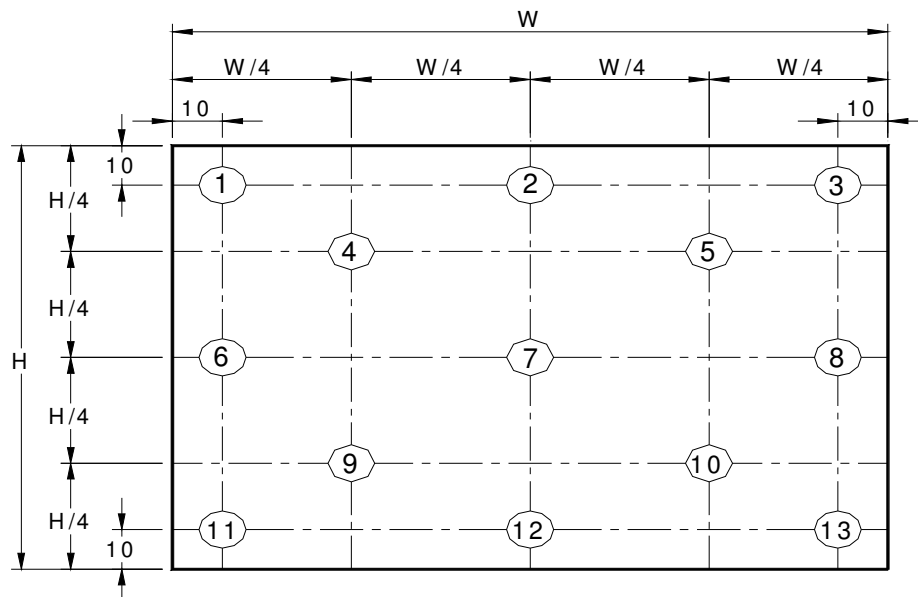
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.

Photo detector

Field=2°

50 cm

LCD Panel

TFT-LCD Module

Center of the screen
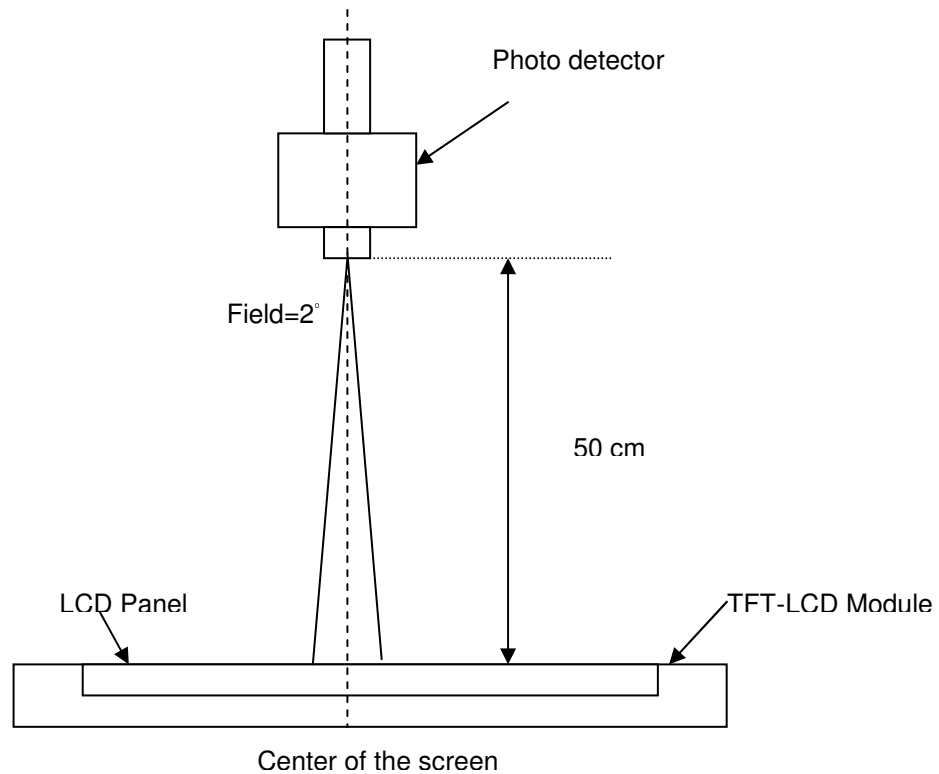
Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，$Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5$

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)

Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.
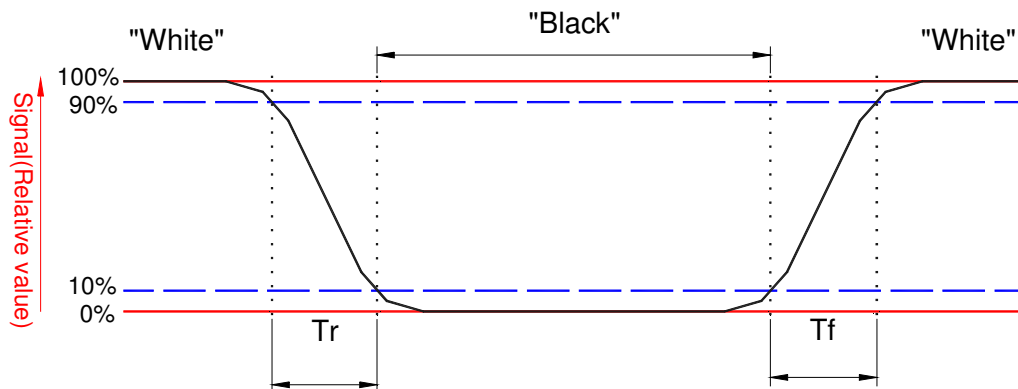
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio $\geqq 10$, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.

3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 30 Pin one lane eDP Module
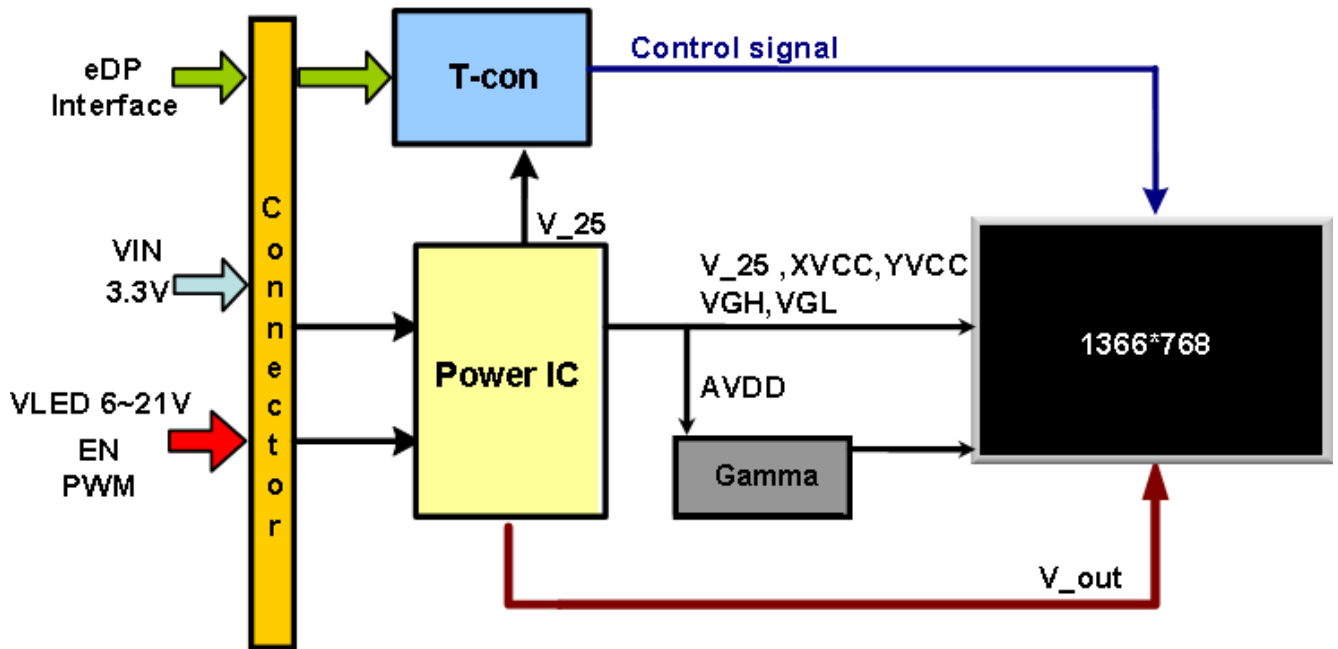
4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

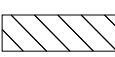| Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[^{o}C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[^{o}C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).
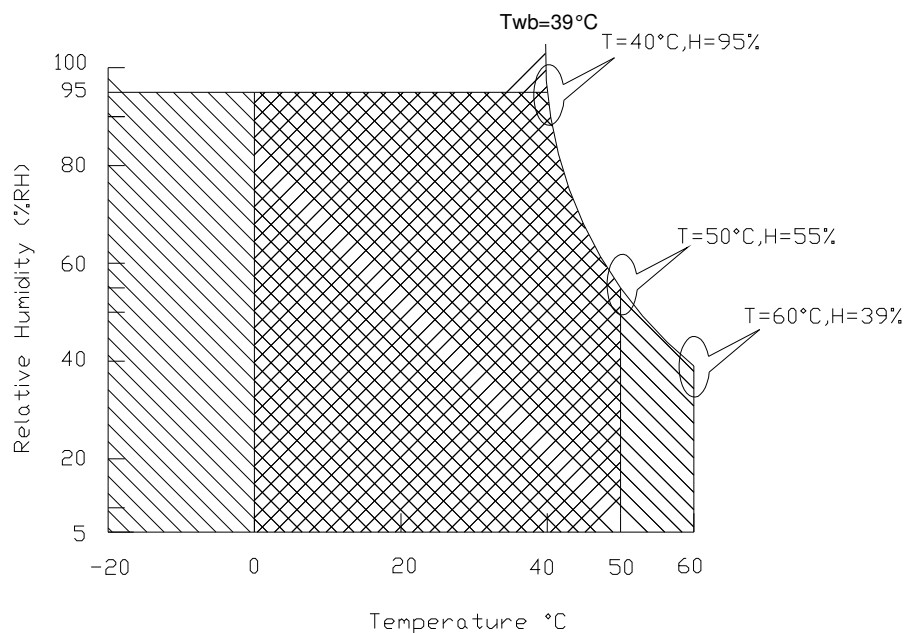
Operating Range   Storage Range

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.65	[Watt]	Note 1
IDD	IDD Current	-	-	180	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2：Measure Condition
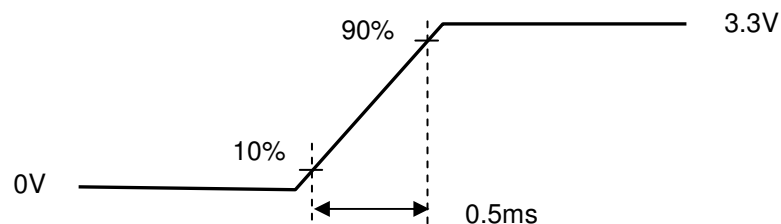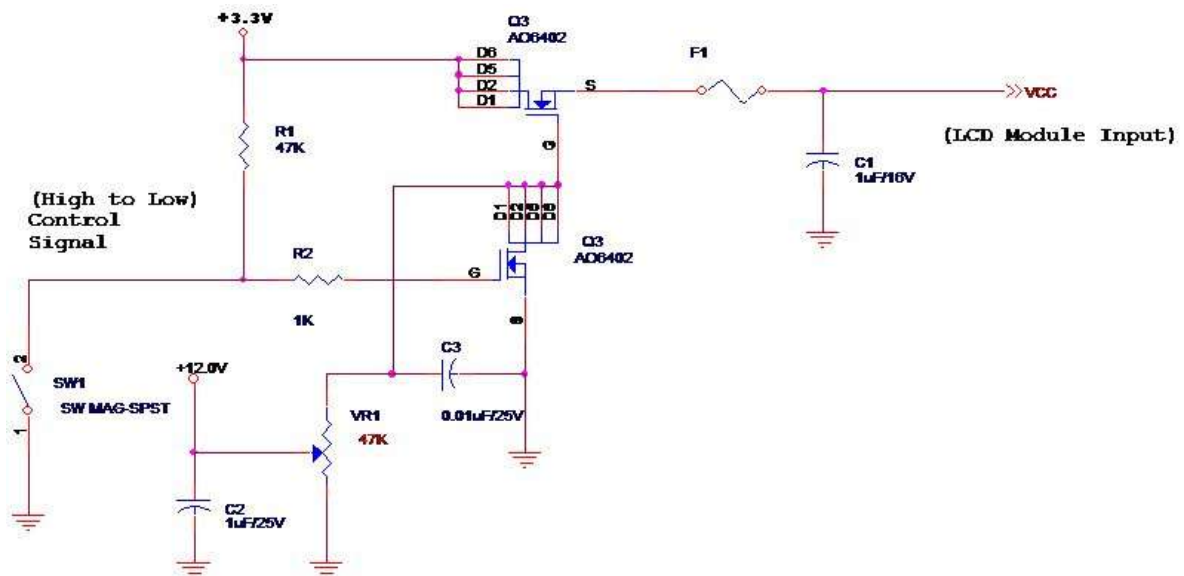
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Display Port main link signal:

Differential pair VD+ , VD- Which is one Display port Main link

VCM of Display port Main link

VD+

VCM

VDiff

VD-

$$Vdiff_{P-P} = [(VD+) - (VD-)] \times 2$$

V D+ - VD-

0V
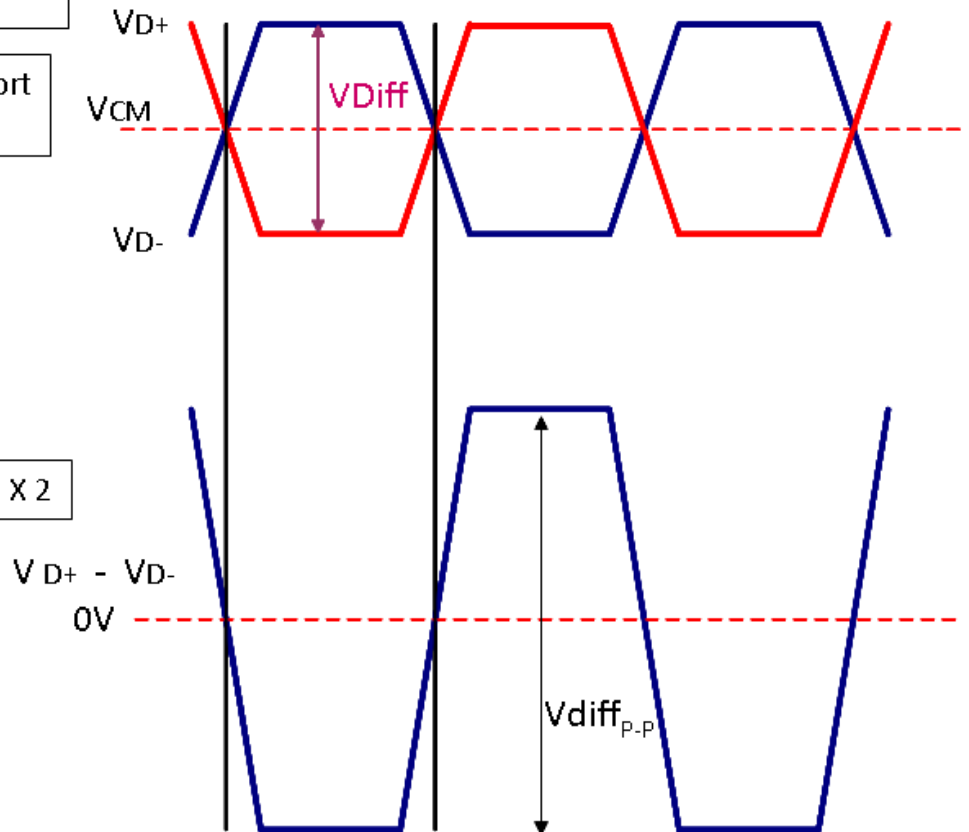
Vdiff$_{P-P}$

Display port main link				
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff$_{P-P}$	Peak-to-peak Voltage at a receiving Device	120		1320	mV

Follow as VESA display port standard V1.2

Display Port AUX_CH signal:

Differential AUX+ , AUX-
Which is Display pot AUX_CH

AUX+

VDiff$_{P-P}$

VCM

AUX-
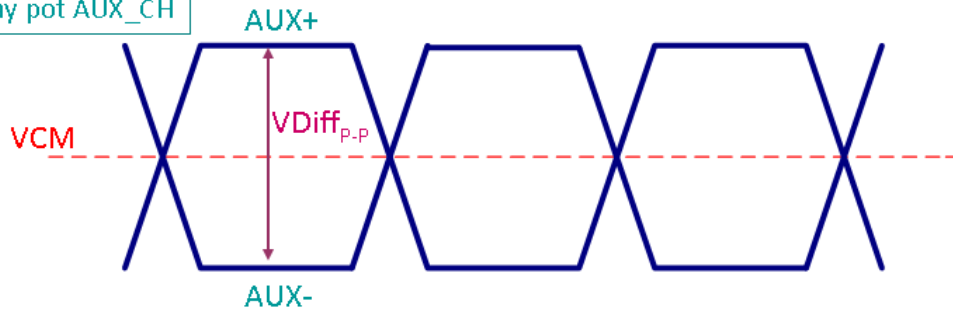
Display port AUX_CH		Min	Typ	Max	unit
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff$_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Follow as VESA display port standard V1.2

Display Port V$_{HPD}$ signal:

Display port V$_{HPD}$		Min	Typ	Max	unit
		Min	Typ	Max	unit
V$_{HPD}$	HPD Voltage	2		3.6	V

Follow as VESA display port standard V1.2

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	1.9	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.
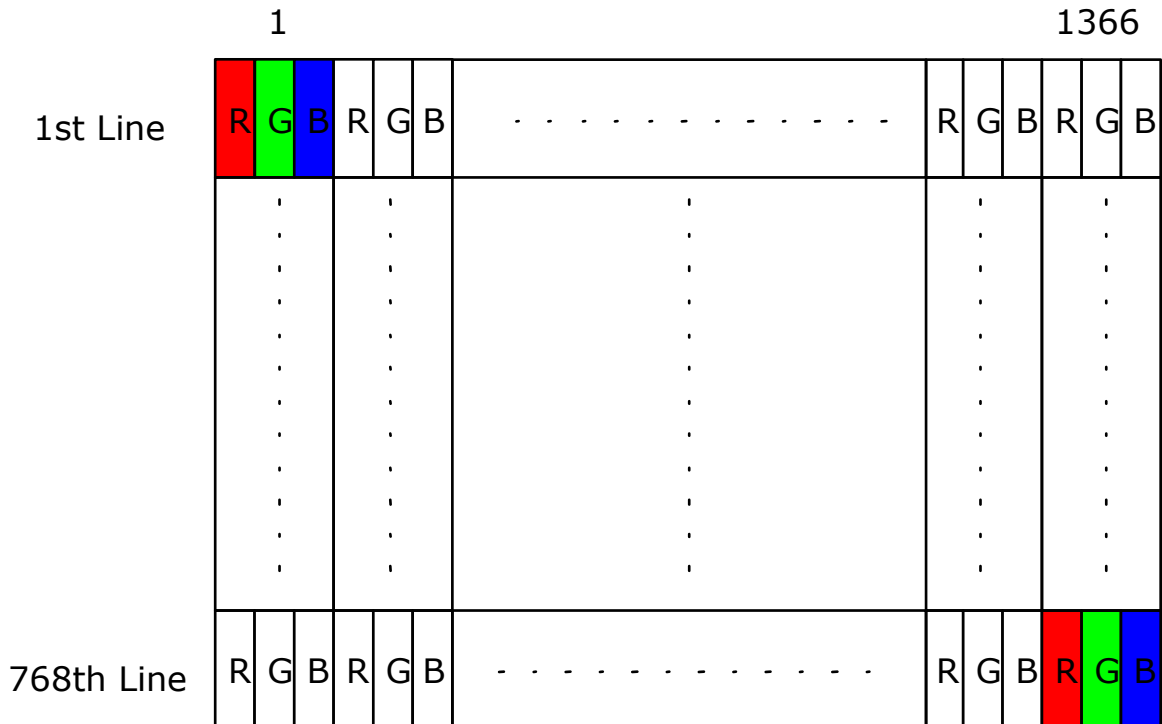
6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

| Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	20455-030E-12 or compatible
Mating Housing/Part Number	20453-030T-11

6.2.2 Pin Assignment

eDP is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	NC
2	H_GND	High Speed Ground
3	Lane1_N	Comp Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signale pin
18	BL_GND	Backlight ground
19	BL_GND	Backlight ground
20	BL_GND	Backlight ground
21	BL_GND	Backlight ground

22	BL_EN	Backlight On / Off
23	BL_PWM	System PWM signal Input
24	EDID_CLK	EDID_CLK
25	EDID_DATA	EDID_DATA
26	V_LED	Backlight power
27	V_LED	Backlight power
28	V_LED	Backlight power
29	V_LED	Backlight power
30	NC	No connect

Pin 30　　　**Pin 1**

VLED　　　NC

Connector
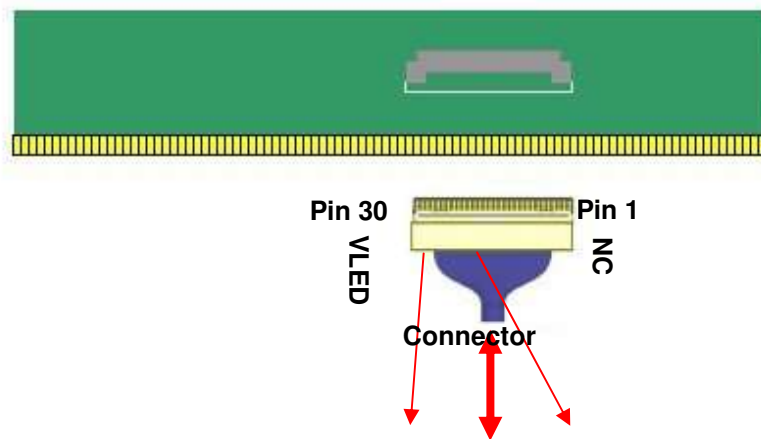
Note1: Input signals shall be low or High-impedance state when VDD is off.

6.3 Interface Timing

Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz   manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	**Hz**
Clock frequency		1/ T_{Clock}	-	69.3	-	**MHz**
Vertical Section	**Period**	T_V	778	793	1023	T_{Line}
	Active	T_{VD}		768		
	Blanking	T_{VB}	10	25	255	
Horizontal Section	**Period**	T_H	1446	1456	1700	T_{Clock}
	Active	T_{HD}		1366		
	Blanking	T_{HB}	80	90	334	

6.4 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.

Display Port panel power sequence:
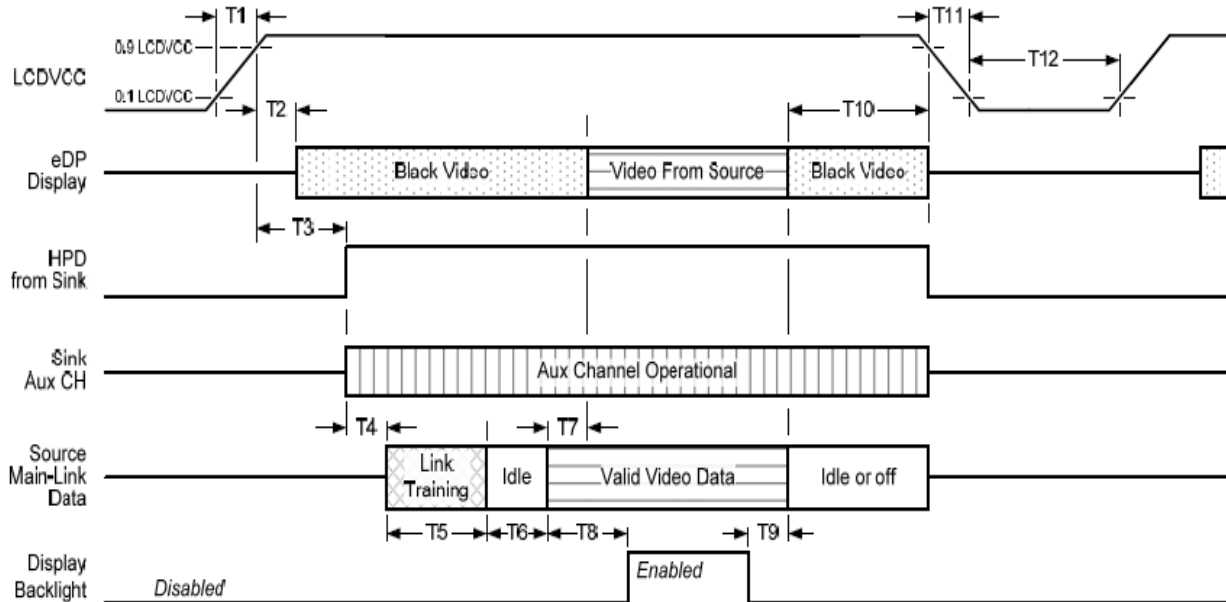
Display port interface power up/down sequence, normal system operation

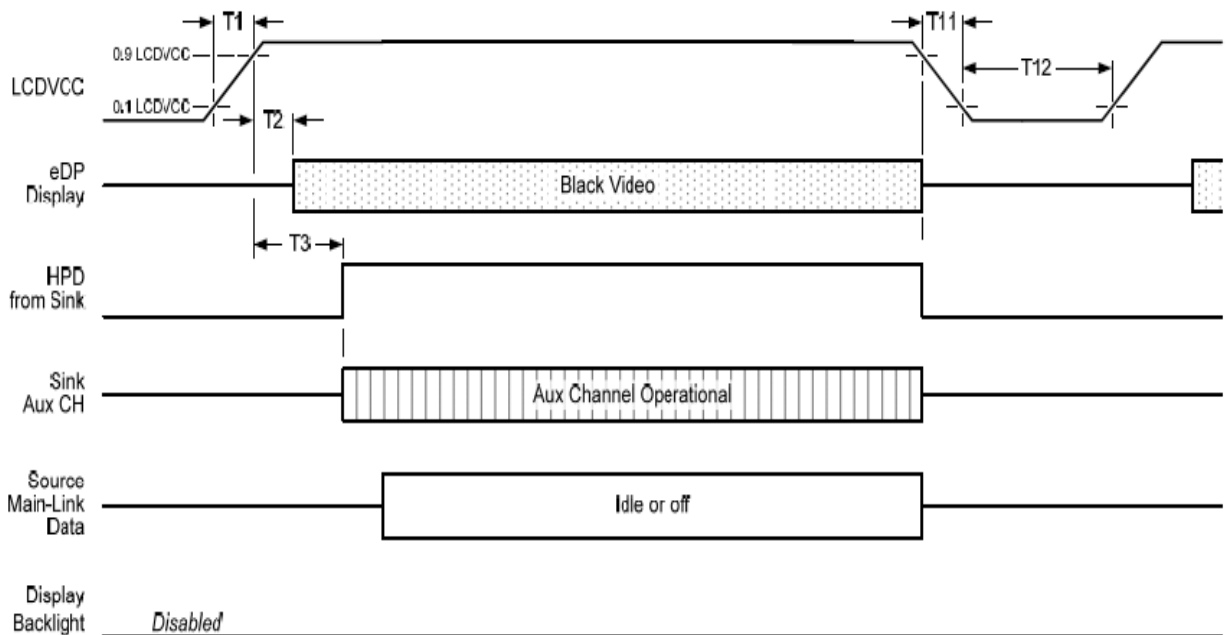**Display Port AUX_CH transaction only:**

Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note 1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:

	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT$_{PWM}$*

*T$_{PWM}$ = 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃ to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

. Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension

8.1.1 Standard Front View
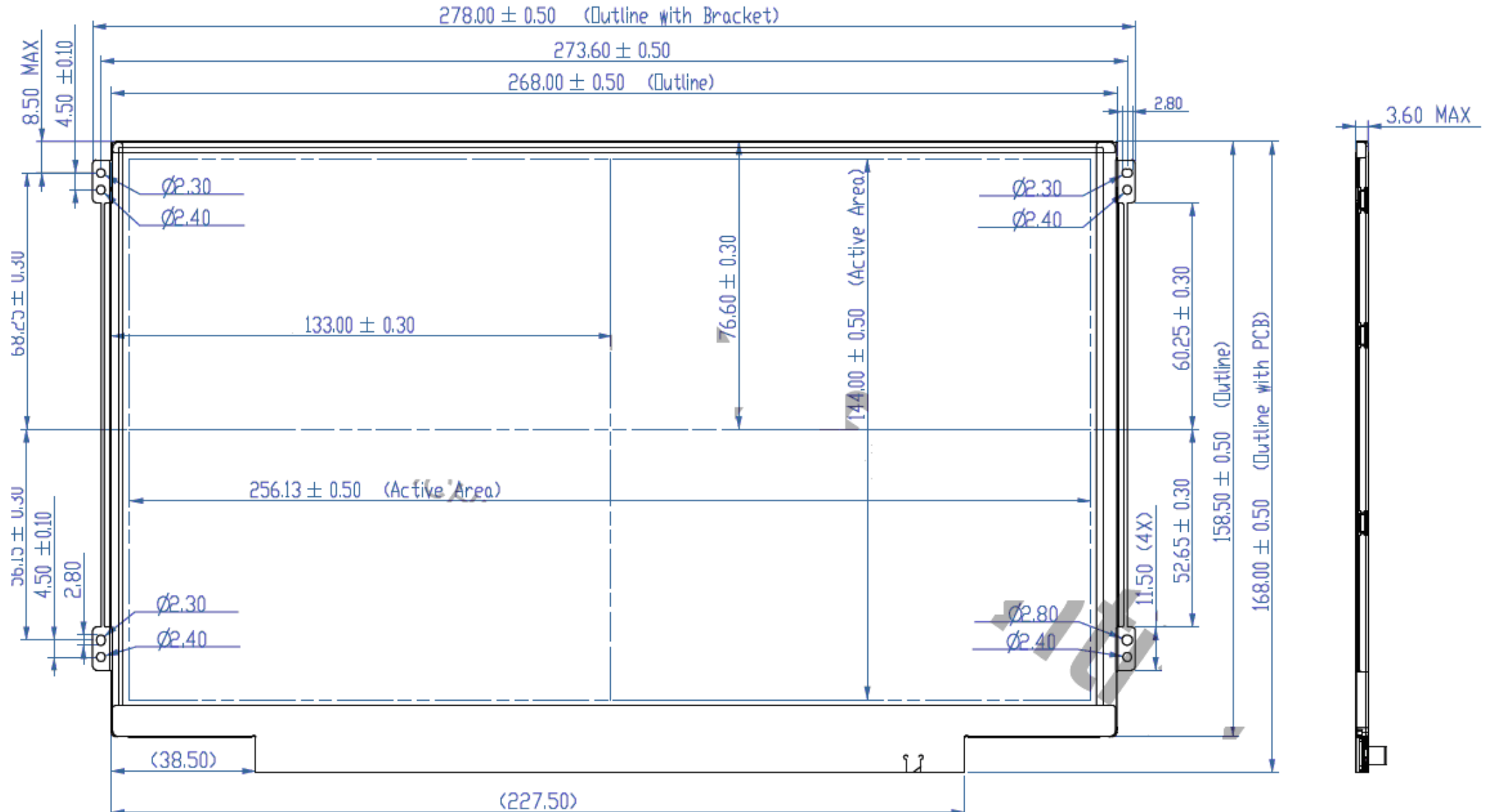
8.1.2 Standard Rear View & Key components remark and remind

Prevention damage the IC, connector, Capacitor…., we recommend your design (Ex: cable, rib, hardness parts) far away those section those have remarked at this drawing.
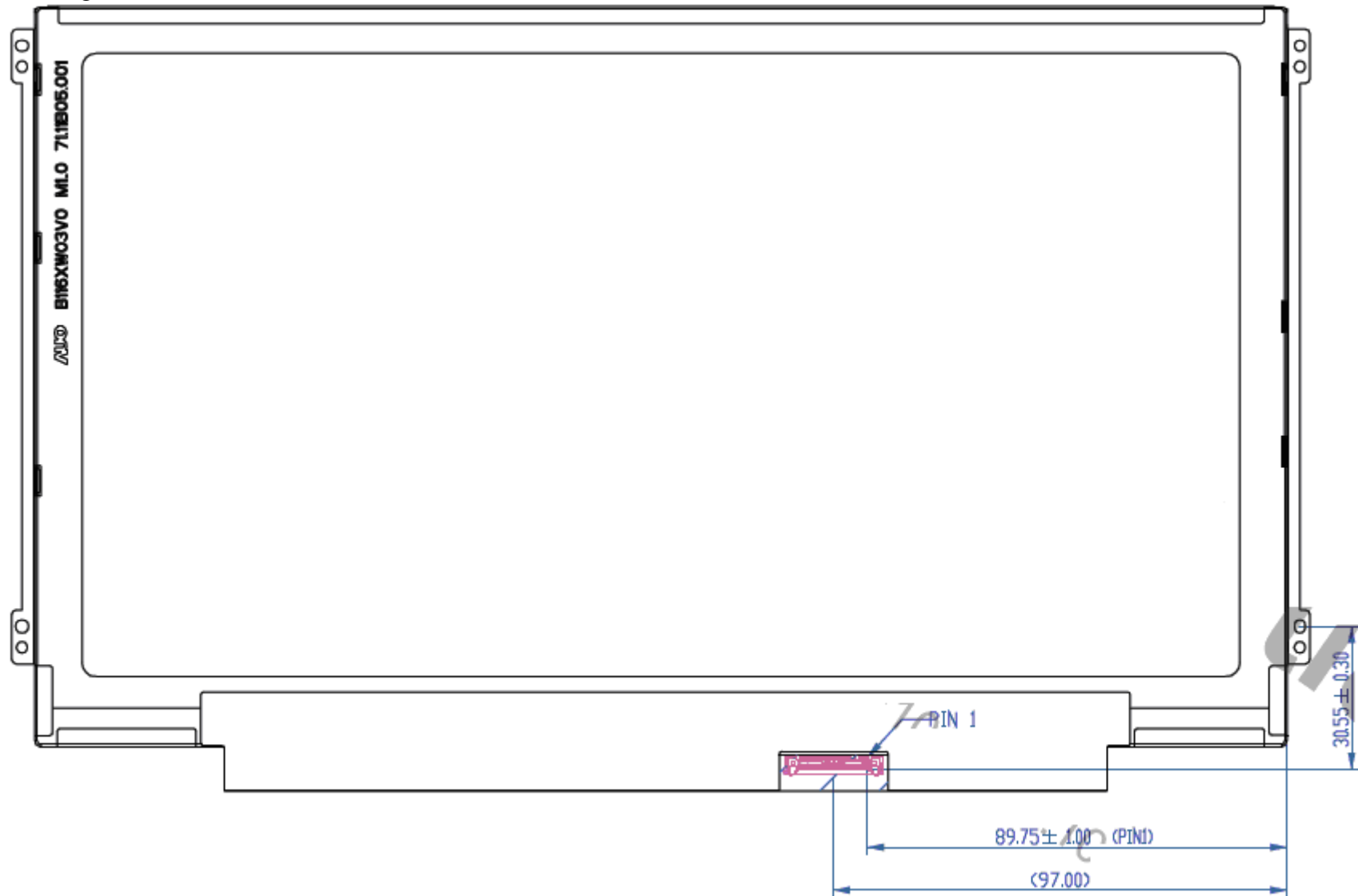
9. Shipping and Package

9.1 Shipping Label Format

Shipping Label

Manufactured 05/52
Model No: B116XTN01 V0
AU Optronics
Made in China (Z40)

H/W: 1A F/W:0

E204356

RoHS

* XXXXXXXXXXXX-XXXXXX

B116XTN01V0

Carton Label

AU Optronics   QTY：35   RoHS   Pb

B116XTN01 V0

PART NO：97.11B08.040-Z40

P/N 18201679

CARTON NO：

ZM100-0652300205

9.2 Carton Package

Outside the packing material contains

Carton：469mm*378mm*266mm, carton andcushion weight : 2590g
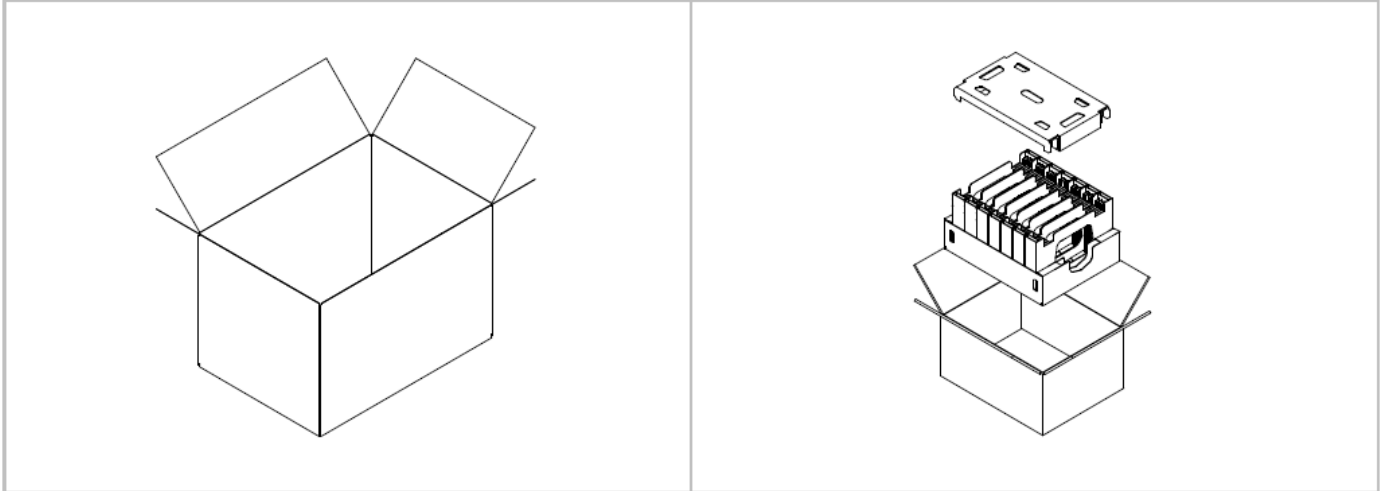
Pallet : 1140mm*980mm*138mm

Stretch film : 500mm (W)*300M (L)

Corner pillar : L type fiber board

PET band : 19mm (W)

Label : 105mm*75mm

One time put 1 PCS product into the side cushion slowly, until put 35 pcs.

9.3 Shipping Package of Palletizing Sequence

10. Appendix: EDID Description
B116XTN01 0 EDID Code

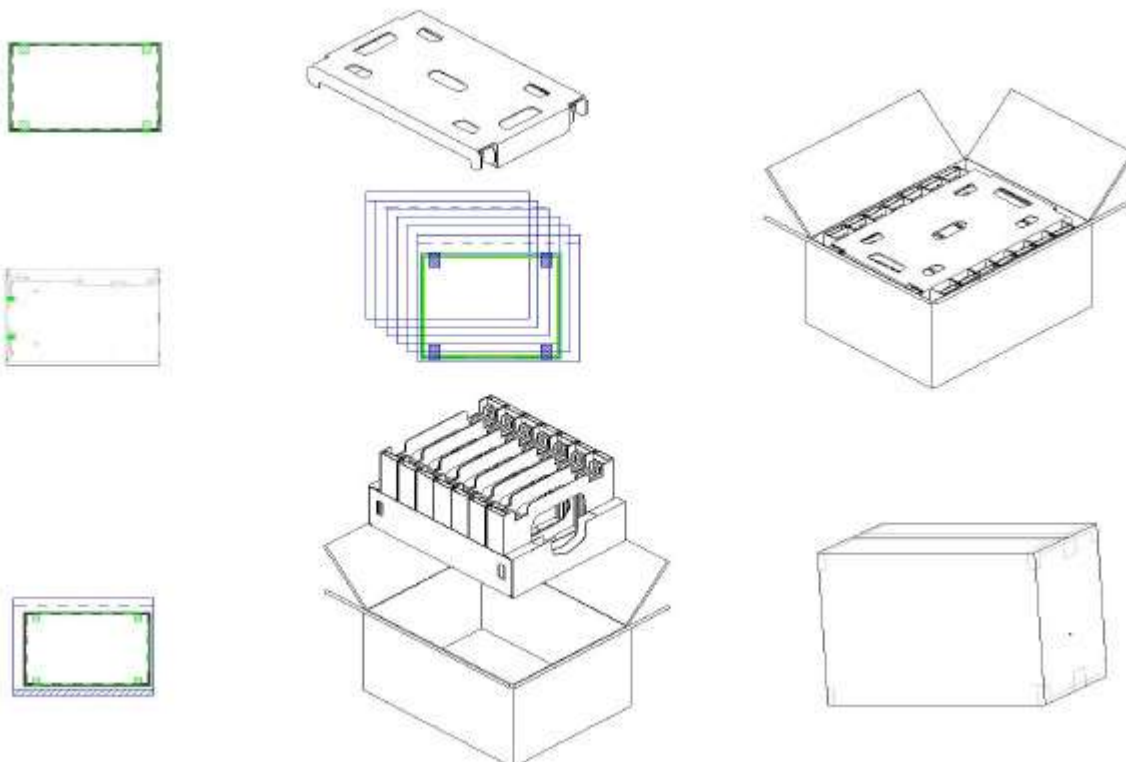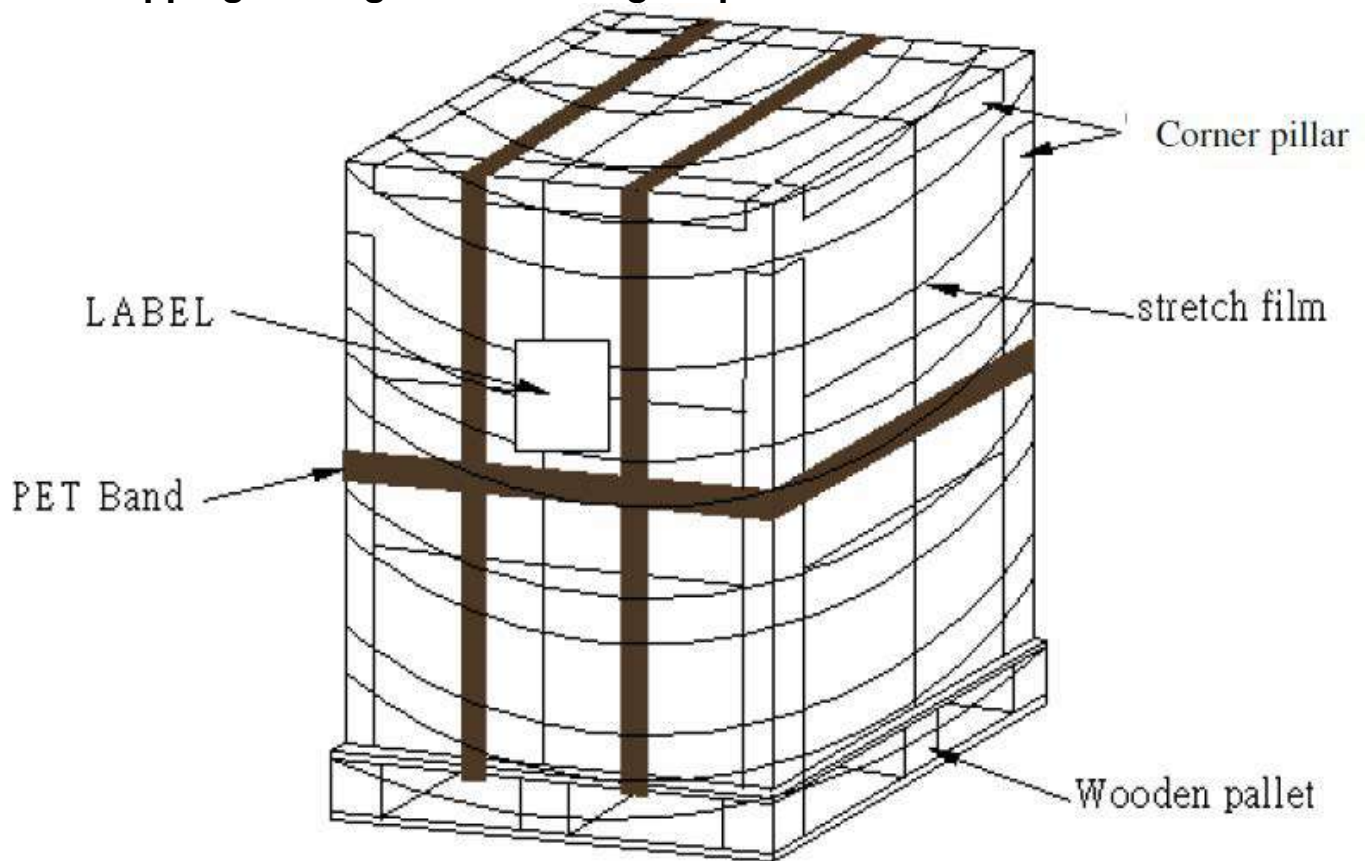| Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01	Header	FF	11111111	255	
02	Header	FF	11111111	255	
03	Header	FF	11111111	255	
04	Header	FF	11111111	255	
05	Header	FF	11111111	255	
06	Header	FF	11111111	255	
07	Header	00	00000000	0	
08	ID Manufacturer Name	30	00110000	48	
09		AE	10101110	174	
0A	ID Product Code	10	00010000	16	
0B		40	01000000	64	
0C	ID Serial Number (32-bit serial number)	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of Manufacture	01	00000001	1	
11	Year of Manufacture	15	00010101	21	
12	EDID Structure version	01	00000001	1	
13	EDID Revision	03	00000011	3	
14	Video Input Definition	80	10000000	128	
15	Max H Image Size(㎝)	1A	00011010	26	
16	Max V Image Size(㎝)	0E	00001110	14	
17	Display gamma (gamma x 100)-100	78	01111000	120	
18	Feature support(DPMS)	EA	11101010	234	
19	Red/Green Low Bits	99	10011001	153	
1A	Blue/White Low Bits	85	10000101	133	
1B	Red x	95	10010101	149	
1C	Red y	55	01010101	85	
1D	Green x	56	01010110	86	
1E	Green y	92	10010010	146	
1F	Blue x	28	00101000	40	
20	Blue y	22	00100010	34	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established Timing 1	00	00000000	0	
24	Established Timing 2	00	00000000	0	
25	Manufacturer's Timings	00	00000000	0	

26	Standard Timing Identification #1	01	00000001	1	
27		01	00000001	1	
28	Standard Timing Identification #2	01	00000001	1	
29		01	00000001	1	
2A	Standard Timing Identification #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard Timing Identification #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard Timing Identification #5	01	00000001	1	
2F		01	00000001	1	
30	Standard Timing Identification #6	01	00000001	1	
31		01	00000001	1	
32	Standard Timing Identification #7	01	00000001	1	
33		01	00000001	1	
34	Standard Timing Identification #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10,000 (LSB)	70	01110000	112	
37	Pixel Clock/10,000 (MSB) /	1C	00011100	28	
38	Horizontal Active	56	01010110	86	
39	Horizontal Blanking	A4	10100100	164	
3A	Horizontal Active : Horizontal Blanking	50	01010000	80	
3B	Vertical Active	00	00000000	0	
3C	Vertical Blanking	19	00011001	25	
3D	Vertical Active : Vertical Blanking	30	00110000	48	
3E	Horizontal Sync. Offset	28	00101000	40	
3F	Horizontal Sync Pulse Width	20	00100000	32	
40	Vertical Sync Offset : Sync Width	36	00110110	54	
41	Horizontal Vertical Sync Offset/Width upper 2bits	00	00000000	0	
42	Horizontal Image Size	00	00000000	0	
43	Vertical Image Size	90	10010000	144	
44	Horizontal & Vertical Image Size	10	00010000	16	
45	Horizontal Border	00	00000000	0	
46	Vertical Border	00	00000000	0	
47	Flags	18	00011000	24	
48	Pixel Clock/10,000 (LSB) (Slow Refresh rate)	44	01000100	68	48Hz
49	Pixel Clock/10,000 (MSB) / (Slow Refresh rate)	16	00010110	22	
4A	Horizontal Active	56	01010110	86	

4B	Horizontal Blanking	A0	10100000	160	
4C	Horizontal Active : Horizontal Blanking	50	01010000	80	
4D	Vertical Active	00	00000000	0	
4E	Vertical Blanking	0A	00001010	10	
4F	Vertical Active : Vertical Blanking	30	00110000	48	
50	Horizontal Sync. Offset	28	00101000	40	
51	Horizontal Sync Pulse Width	20	00100000	32	
52	Vertical Sync Offset : Sync Width	36	00110110	54	
53	Horizontal Vertical Sync Offset/Width upper 2bits = 0	00	00000000	0	
54	Horizontal Image Size	00	00000000	0	
55	Vertical Image Size	90	10010000	144	
56	Horizontal & Vertical Image Size	10	00010000	16	
57	Horizontal Border	00	00000000	0	
58	Vertical Border	00	00000000	0	
59	Flags	18	00011000	24	
5A	Flag	00	00000000	0	
5B	Flag	00	00000000	0	
5C	Flag	00	00000000	0	
5D	Data Type Tag	0F	00001111	15	
5E	Flag	00	00000000	0	
5F	(Horizontal active pixel /8)-31	8C	10001100	140	
60	Image Aspect Ratio	09	00001001	9	
61	Middle Refresh Rate	3C	00111100	60	
62	(Horizontal active pixel /8)-31	8C	10001100	140	
63	Image Aspect Ratio	09	00001001	9	
64	Low Refresh Rate	30	00110000	48	
65	Brightness(1/10nit)	16	00010110	22	
66	Feature flag	09	00001001	9	
67	Reserved	00	00000000	0	
68	LCD Supplier manufacture Code (3 character ID)	06	00000110	6	
69		AF	10101111	175	
6A	LCD Supplier Product code	31	00110001	49	
6B	LCD Supplier Product code	30	00110000	48	
6C	Flag	00	00000000	0	
6D	Flag	00	00000000	0	
6E	Flag	00	00000000	0	
6F	Data Type Tag	FE	11111110	254	
70	Flag	00	00000000	0	

71	Model Name	42	01000010	66	B
72	Model Name	31	00110001	49	1
73	Model Name	31	00110001	49	1
74	Model Name	36	00110110	54	6
75	Model Name	58	01011000	88	X
76	Model Name	54	01010100	84	T
77	Model Name	4E	01001110	78	N
78	Model Name	30	00110000	48	0
79	Model Name	31	00110001	49	1
7A	Model Name	2E	00101110	46	.
7B	Model Name	30	00110000	48	0
7C	Model Name	20	00100000	32	
7D	Model Name	0A	00001010	10	
7E	Extension flag	00	00000000	0	
7F	Checksum	CC	11001100	204	