Doc. Version	0.5
Total Page	28
Date	2007/08/02

Product Specification

3.5" COLOR TFT-LCD MODULE

MODEL NAME: A035QN03 V2

< □ >Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2007/03/16		First draft.
0.1	2007/04/03	12	Update the power-on sequence
		14~15	Update the SPI timing information
0.2	2007/04/18	9	Modify the absolute maximum rating table
		9	Modify the electrical characteristic table
		12~17	Modify the register timing, tables, and description
		25	Change C14 to 10 uF
		26	Add stand-by timing
		27	Add recommend power on/ off settings
		28	Add notes for ESD protection
0.3	2007/05/18	7	Swap VGH and VGL, and change pin12, 14, and 25 to GND
		8	Change pin71 from dummy to GRB
		9	Modify LED reverse voltage absolute maximum ratings
		25	Update the application circuit
0.4	2007/06/11	9	Add the current consumption of TFT LCD
		10	Add GRB timing into power-on sequence
0.5	2007/08/02	6	Update drawing

Contents:

A. General Description 4
B. Features 4
C. Physical Specifications 5
D. Outline Dimension 6
E. Electrical Specifications 7
1. Pin Assignment 7
2. Absolute Maximum Ratings 9
3. Electrical Characteristics 9
a. TFT- LCD Panel (GND=0V) 9
b. Backlight Driving Conditions 9
4. AC Timing 10
a. Power on/off sequence 10
b. Timing Condition 12
c. Timing Diagram 12
5. Command Register Map 13
a. Command Timing: Serial Peripheral Interface 13
b. SPI timing diagram 13
c. Serial setting map 14
d. SPI AC specification 15
e. Description of serial control data 15
F. Optical specifications (Note 1, 2) 19
G. Touch Screen Panel Specifications 21
1. FPC Pin Assignment 21
2. Electrical Characteristics 21
3. Mechanical Characteristics 21
4. Life test Condition 22
5. Attention 22
H. Reliability Test Items 24
I. Packing Form 25
J. Application Note 26
1. Application circuit 26
2. Standby timing 27
3. Recommand Parallel Interface Register Settings 28
4. Recommand ESD Protection 29

A. General Description

A035QN03 V2 is an amorphous transmissive type Thin Film Transistor Liquid crystal Display (TFT-LCD). This model is composed of a TFT-LCD, a driver, an FPC (flexible printed circuit), a backlight unit and a touch panel.

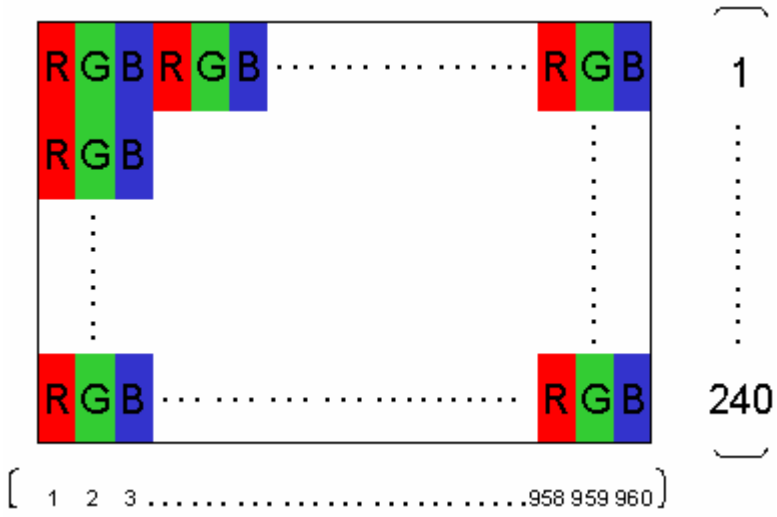
B. Features

- 3.5-inch display with touch panel
- QVGA resolution in RGB stripe dot arrangement
- DC/DC integrated
- 3-wire 16-bit register setting
- Interfaces: parallel RGB 24-bit
- Wide viewing angle
- Integrated touch screen panel (resistive type)
- 3-in-1 FPC for LCD signals, backlight LED power and touch panel
- Green design

C. Physical Specifications

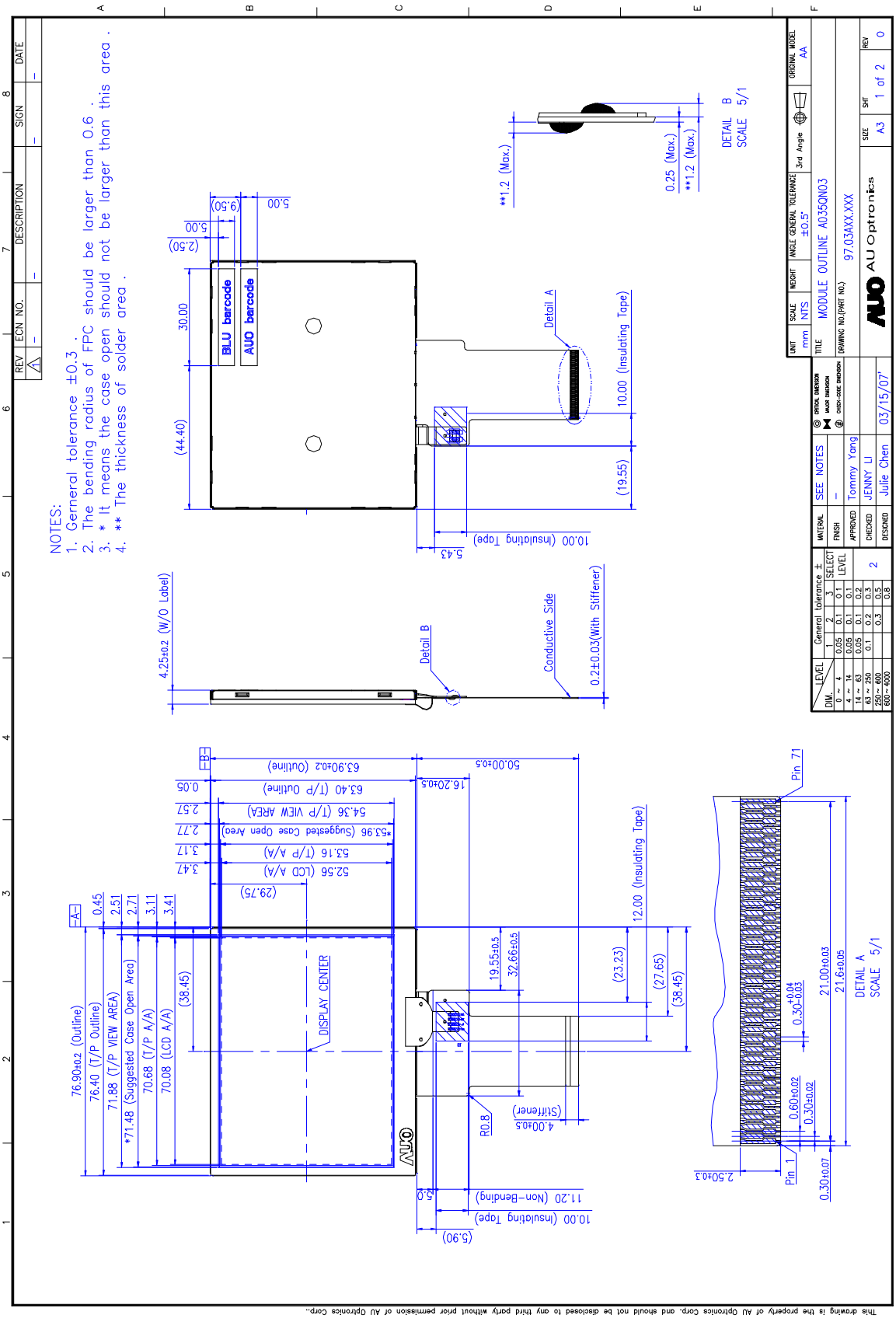
NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	320 RGB (H)×240(V)	
2	Active Area	mm	70.08(H)×52.56(V)	
3	Screen Size	inch	3.5(Diagonal)	
4	Dot Pitch	mm	0.073(H)×0.219(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	16.2M Colors	
7	Overall Dimension	mm	76.9(H) × 63.9(V) × 4.25(T)	Note 2
8	Weight	g	40	
9	Touch panel surface treatment	--	AG 10%	
10	Display Mode	--	Normally White	
11	Gray Level Inversion Direction		6 O'clock	

Note 1: Below figure shows dot stripe arrangement.



Note 2: Not including FPC. Refer to the drawing next page for further information.

D. Outline Dimension



E. Electrical Specifications

1. Pin Assignment

Connector type: HIROSE FH26-71S-0.3SHW
(71-pin, 0.3mm pitch, bottom contact)

No.	Pin Name	I/O	Description	Remarks
1	LED-	I	LED Cathode	
2	LED-	I	LED Cathode	
3	LED+	I	LED Anode	
4	LED+	I	LED Anode	
5	GND	G	Ground	
6	X1	I/O	X Right	
7	Y1	I/O	Y Bottom	
8	X2	I/O	X Left	
9	Y2	I/O	Y Top	
10	DUMMY		Not connected	
11	VGH	C	Capacitor of charge pumping circuit	
12	GND	G	Ground	
13	VGL	C	Capacitor of charge pumping circuit	
14	GND	G	Ground	
15	V_10	C	Capacitor of charge pumping circuit	
16	C3P	C	Capacitor of charge pumping circuit	
17	C3M	C	Capacitor of charge pumping circuit	
18	C2P	C	Capacitor of charge pumping circuit	
19	C2M	C	Capacitor of charge pumping circuit	
20	VCAC	C	Capacitor of VCOMAC circuit	
21	FRP	O	Frame polarity	
22	VCOM	I	VCOM	
23	C1BP	C	Capacitor of charge pumping circuit	
24	C1BM	C	Capacitor of charge pumping circuit	
25	GND	G	Ground	
26	V_5	C	Capacitor of charge pumping circuit	
27	PVDD	PI	Analog power input, 3.0~3.6V is recommended.	
28	PVDD	PI	Analog power input, 3.0~3.6V is recommended.	
29	C1AP	C	Capacitor of charge pumping circuit	
30	C1AM	C	Capacitor of charge pumping circuit	
31	VINT2	C	Capacitor of charge pumping circuit	
32	GND	G	Ground	
33	VINT1	C	Capacitor of charge pumping circuit	
34	DUMMY			

35	GMA_H	C	Stabilizing capacitor for analog power	
36	VCC	C	Digital power supply	
37	GND	G	Ground	
38	VIO	PI	Digital power input	
39	VIO	PI	Digital power input	
40	VSYNC	I	Vertical Synchronous Signal	
41	HSYNC	I	Horizontla Synchronous Signal	
42	DOTCLK	I	Data Clock	
43	DUMMY			
44	DATA23	I	Red Data (MSB)	
45	DATA22	I	Red Data	
46	DATA21	I	Red Data	
47	DATA20	I	Red Data	
48	DATA19	I	Red Data	
49	DATA18	I	Red Data	
50	DATA17	I	Red Data	
51	DATA16	I	Red Data (LSB)	
52	DATA15	I	Green Data (MSB)	
53	DATA14	I	Green Data	
54	DATA13	I	Green Data	
55	DATA12	I	Green Data	
56	DATA11	I	Green Data	
57	DATA10	I	Green Data	
58	DATA09	I	Green Data	
59	DATA08	I	Green Data (LSB)	
60	DATA07	I	Blue Data (MSB)	
61	DATA06	I	Blue Data	
62	DATA05	I	Blue Data	
63	DATA04	I	Blue Data	
64	DATA03	I	Blue Data	
65	DATA02	I	Blue Data	
66	DATA01	I	Blue Data	
67	DATA00	I	Blue Data (LSB)	
68	SCL	I	Clock of serial interface	
69	CS	I	Chip enable of serial interface	
70	SDA	IO	Serial data input and output of serial interface	
71	GRB	I	Global reset	

I: Digital signal input, O: Digital signal output, G: GND, P: Power input, C: Capacitor

2. Absolute Maximum Ratings

Items	Symbol	Values		Unit	Condition
		Min.	Max.		
Power Voltage	VIO	-0.5	7	V	
	PVDD	-0.5	7	V	
LED Reverse Voltage	Vr		5	V	One LED
LED Forward Current	If		30	mA	One LED

Note 1.If the operating condition exceeds the absolute maximum ratings, the TFT-LCD module may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop.

3. Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

a. TFT- LCD Panel (GND=0V)

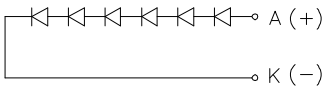
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Digital Power Supply	VIO	1.8	3.3	3.6	V	
Analog Power Supply	PVDD	3.0	3.3	3.6	V	
Input Signal Voltage	Vi	0		0.2 x VIO	V	
	VI	0.8 x VIO		VIO	V	
Frame Frequency	f_{Frame}		60		Hz	
Dot Data Clock	DCLK		6.134		MHz	
Power Stand-by Current	$ISTB_{PVDD}$		25	50	uA	PVDD=3.3V
Power Operating Current	I_{PVDD}		10	20	mA	VIO=3.3V

Note 1. Panel surface temperature should be kept less than content of “Absolute maximum ratings"

b. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Supply Current	I_L		20		mA	single serial
LED Supply Voltage	V_L		19.2		V	single serial
LED Life Time	L_L	10,000	---	---	Hr	Note 2, 3

Note 1: LED backlight is six LEDs serial type.



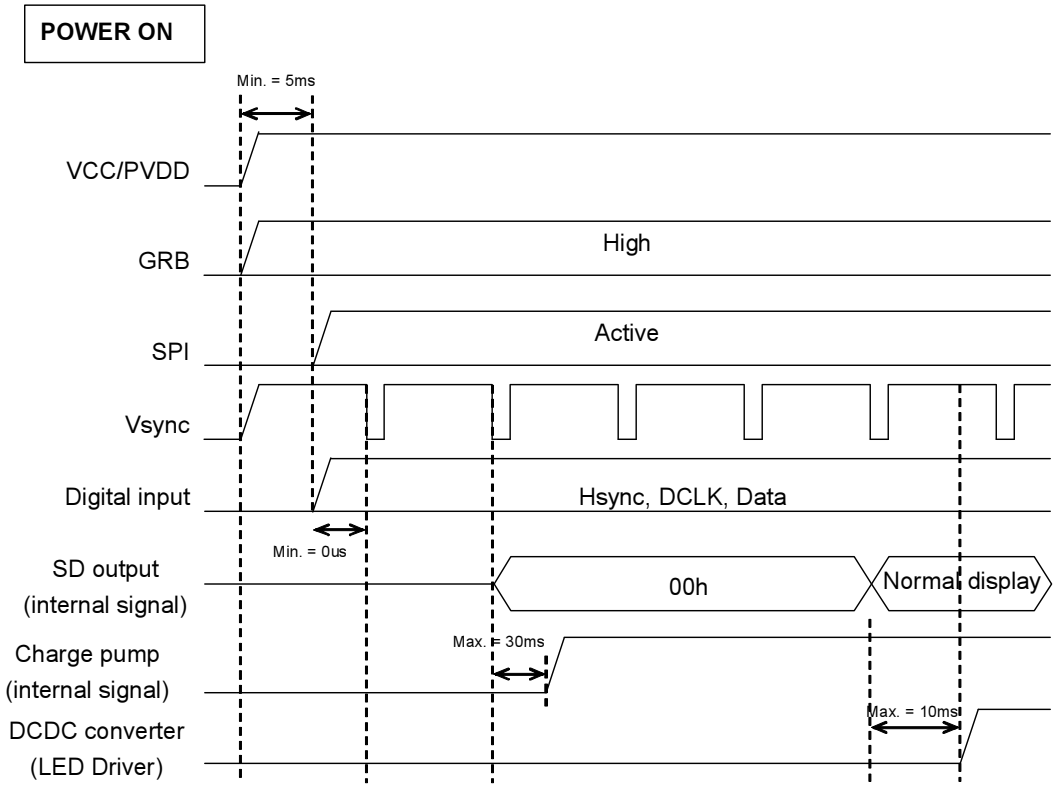
Note 2: The ”LED Supply Voltage” is defined by the number of LED at Ta=25°C, I_L=20mA. In the case of 6 pcs LED, V_L=3.2*6=19.2V

Note 3: The ”LED life time” is defined as the time for the module brightness to decrease to 50% of the initial value at Ta=25°C, I_L=20mA

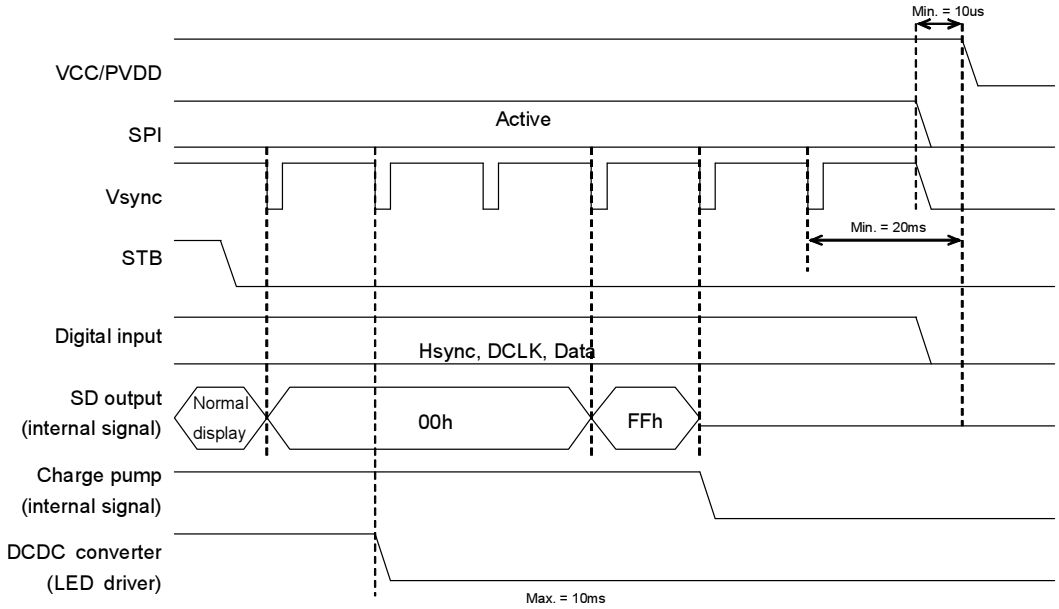
Note 4: The LED lifetime could be decreased if operating I_L is larger than 25mA

4. AC Timing

a. Power on/off sequence



POWER OFF

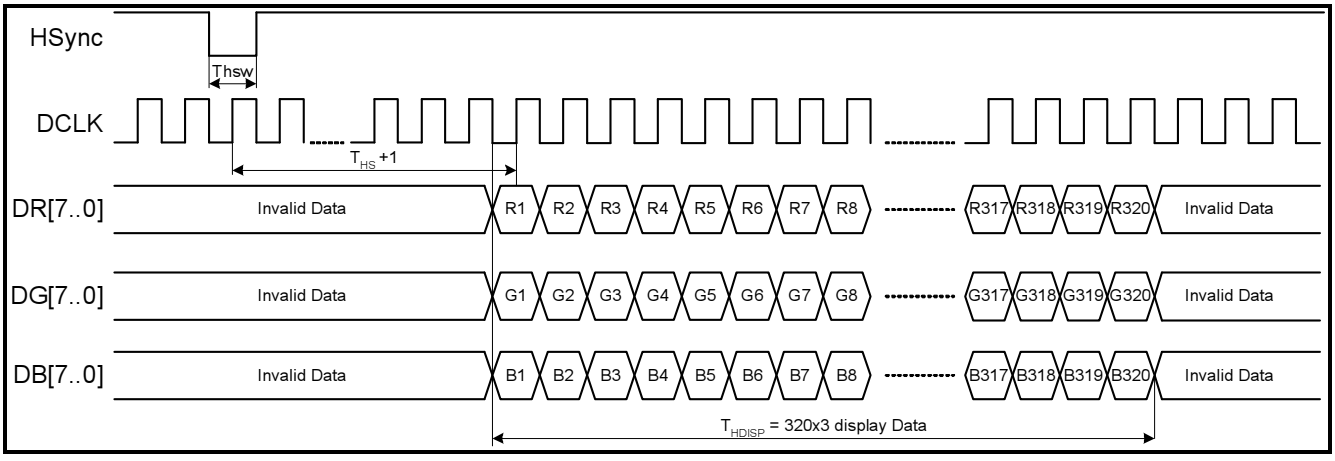


b. Timing Condition

PARAMETER		SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT
DCLK frequency		F_{CLK}			5	6.134	6.75	MHz
DCLK period		T_{CLK}			200	163	148	ns
Hsync	Period	T_H			-	390	-	T_{CLK}
	Display period	T_{HDISP}			320			T_{CLK}
	to 1st data input	T_{HS}	Function of DDL[7..0] settings		0	61	255	T_{CLK}
	Front porch	T_{HFP}			0	8	-	T_{CLK}
	Pulse Width	T_{HSW}			1	1	1	T_{CLK}
VSync	Period	T_V	NTSC		250	262.5	300	T_H
			PAL		290	312.5	350	
	Display period	T_{VDISP}	NTSC		240			T_H
			PAL 1/6		288			T_H
	Delay to 1st gate Output	T_{VS}	Function of HDL[3..0] settings	NTSC	14	21	29	T_H
				PAL	17	24	32	
	Front porch	T_{VFP}			0	9	-	TH
	Pulse Width	T_{VPW}			1	-	-	DCLK
DC converter osc. Frequency		Fosc	Fclk/32		-	383	-	kHz

Note: support interlaced and non interlaced timing

c. Timing Diagram



5. Command Register Map

a. Command Timing: Serial Peripheral Interface

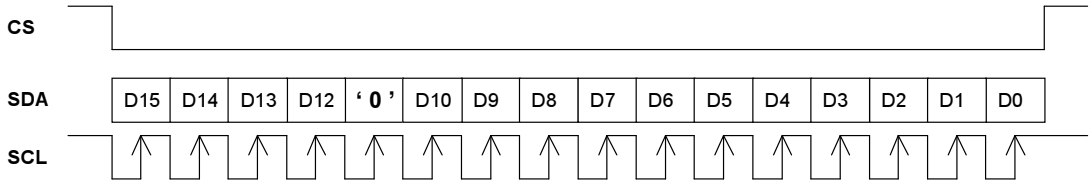
Configuration of serial data at SDA terminal

MSB LSB

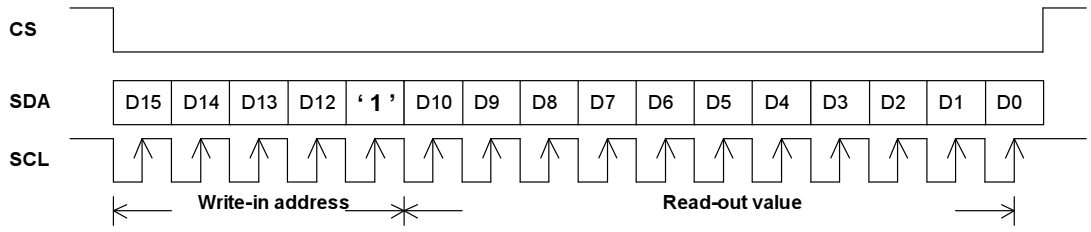
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register address				R/W	DATA										

Note: R/W = '0' ➔ Write mode R/W = '1' ➔ Read mode

Write mode waveform

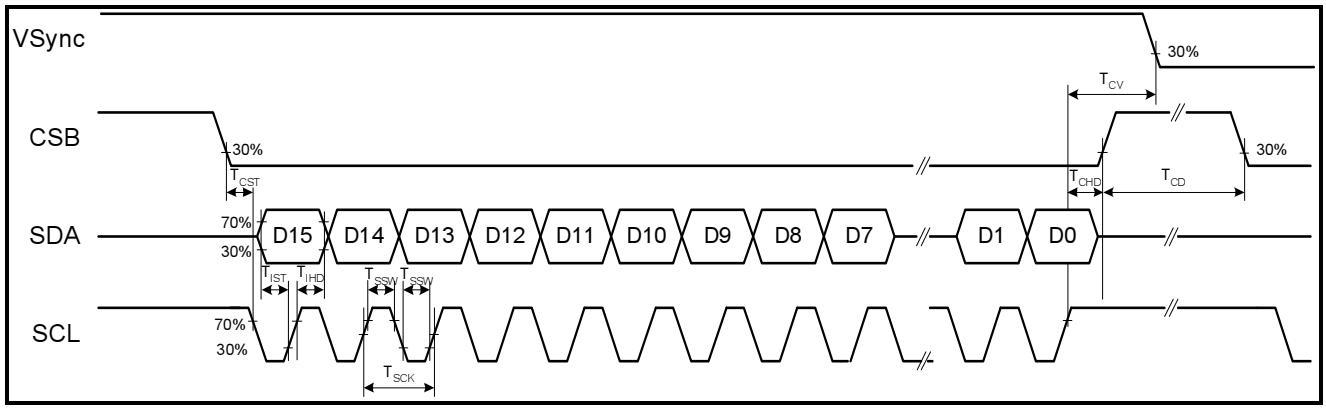


Read mode waveform

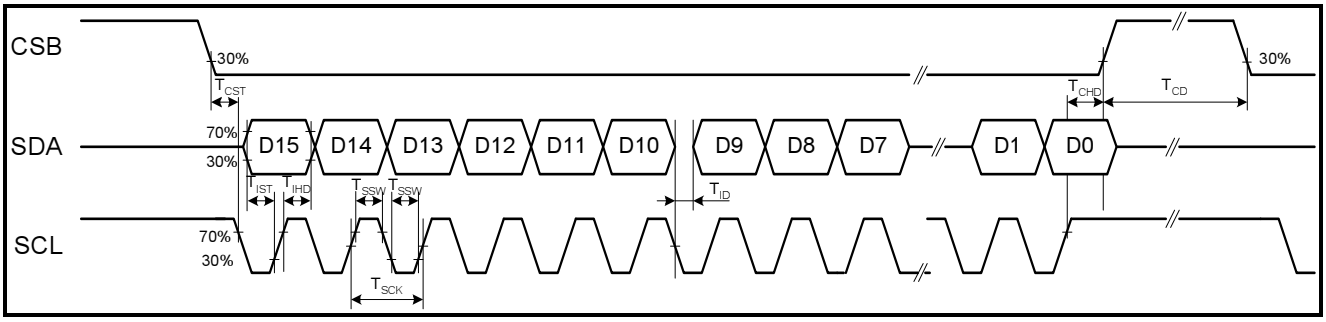


b. SPI timing diagram

AC serial interface write mode timings



AC serial interface read mode timings



c. Serial setting map

Reg N°	ADDRESS				CONTENT											
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	R/W	-	-	*		*	U/D	SHL	GRB	STB	SHDB	SHCB
R1	0	0	0	1	R/W	-	-	-	-	*	PARAL	PALM	PAL	SEL		
R2	0	0	1	0	R/W	-	-	DDL_E	DDL							
R3	0	0	1	1	R/W	-	-	-	-	-	*		HDL			
R4	0	1	0	0	R/W	-	-	-	-	*	*		D/S	DITH	AVGY	
R5	0	1	0	1	R/W	-	-	-	-	-	-	-	CONTRAST			
R6	0	1	1	0	R/W	-	-	-	-	BRIGHTNESS						
R7	0	1	1	1	R/W	-	-	-	-	-	-	-	-	-	-	-
R8	1	0	0	0	R/W	-	-	-	-	-	-	-	VCOM_AC			
R9	1	0	0	1	R/W	-	-	-	-	VDCE	VCOM_DC					
R10	1	0	1	0	R/W	-	-	-	-	1	1	0	DC_MAX_DUTY	DC_FB_LVL		

Reg N°	ADDRESS				DEFAULT VALUES											
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	R/W	-	-	(00)		(0)	(1)	(1)	(1)	(1)	(0)	(1)
R1	0	0	0	1	R/W	-	-	-	-	(0)	(0)	(1)	(0)	(001)		
R2	0	0	1	0	R/W	-	-	(0)	(46h)							
R3	0	0	1	1	R/W	-	-	-	-	-	(01)		(7h)			
R4	0	1	0	0	R/W	-	-	-	-	(1)	(010)		(0)	(1)	(1)	
R5	0	1	0	1	R/W	-	-	-	-	-	-	-	(8h)			
R6	0	1	1	0	R/W	-	-	-	-	(40h)						
R7	0	1	1	1	R/W	-	-	-	-	-	-	-	-	-	-	-
R8	1	0	0	0	R/W	-	-	-	-	-	-	-	(7h)			
R9	1	0	0	1	R/W	-	-	-	-	(1)	(2Dh)					
R10	1	0	1	0	R/W	-	-	-	-	(1)	(1)	(0)	(01)		(10)	

* Reserved

Note: Register R0/(D8,D7) must be (01)

d. SPI AC specification

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Serial clock period	Tsck	320	-	-	ns
Serial clock duty cycle	Tscw	40	50	60	%
Serial clock width low/high	Tssw	120	-	-	ns
Serial data setup time	Tist	120	-	-	ns
Serial data hold time	Tihd	120	-	-	ns
Serial data output delay	Tid	-	-	60	ns
CSB setup time	Tcst	120	-	-	ns
CSB data hold time	Tchd	120	-	-	ns
Chip select distinguish	Tcd	1	-	-	us
Delay between CSB and Vsync	Tcv	1	-	-	us

- Each serial command consists of 16 bits of data which is loaded one bit a time at the **rising edge** of serial clock SCL.
- Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
- The serial control block is operational after power on reset, but commands are established by the **Vsync** signal. If command is transferred multiple times for the same register, **the last command before the Vsync signal is valid.**
- If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
- If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data before the rising edge of CS pulse are valid data.
- Serial block operates with the SCL clock
- Serial data can be accepted in the power save mode.

e. Description of serial control data

R0: System settings

Address	Bit	Description		Default
0000	[5..0]	Bit5(U/D)	Vertical shift direction selection.	0_0011_1101b
		Bit4(SHL)	Horizontal shift direction selection.	
		Bit3(GRB)	Global reset.	
		Bit2(STB)	Standby mode setting.	

		Bit1(SHDB)	DC-DC converter shutdown setting.	
		Bit0(SHCB)	Charge Pump shutdown setting.	

Bit5	UD function
0	Flip vertically
1	**(default)**

Bit4	SHL function
0	Flip horizontally
1	**(default)**

Bit3	GRB function
0	The controller is reset, the charge pump and DCDC are off. Reset all registers to default value.
1	Normal operation. **(default)**

Bit2	STB function
0	T-CON, source driver and DC-DC converter are off. All outputs are High-Z.
1	Normal operation. **(default)**

Bit1	SHDB function
0	DC-DC converter is off. **(default)**
1	DC-DC converter is on. DC-DC controlled by STB and power on/off sequence.

Bit0	SHCB function
0	Charge Pump converter is off.
1	Charge Pump converter is on. **(default)** Charge Pump controls by STB and power on/off sequence.

R1: Timings settings

Address	**Bit**	**Description**		**Default**
0001	[5]	Bit5(PARAL)	Parallel mode selection.	001_0001b

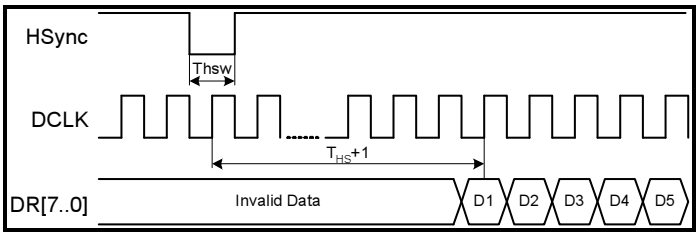
Bit5	PARAL function

0	Parallel mode disabled. Follow SEL function. Data input on DRx. **(default)**
1	Parallel mode enabled. Data input D0x to D2x.

R2: Data delay settings

Address	Bit	Description		Default
0010	[8..0]	Bit8(DDL_E)	DDL setting selection.	0_0100_0110b
		Bit7-0(DDL)	Horizontal Data start delay selection.	

DDL_E	DDL	T_{HS}	Unit	Remark
X	00h	0	DCLK	UPS051
X	46h	70 (Default)	DCLK	
X	FFh	255	DCLK	
0	XXh	241(fixed)	DCLK	UPS051/YUV
1	00h~FFh	64~319	DCLK	
0	XXh	61(fixed)	DCLK	Parallel RGB
1	00h~FFh	0~255	DCLK	



R3: Vertical delay settings

Address	Bit	Description		Default
0011	[5..0]	Bit5-4(OEA)	Odd Even advance selection.	01_0111b
		Bit3-0(HDL)	Vertical delay selection.	

Bit5-4	OEA function (only in CCIR mode)
00	Display start @T_{VS} delay for Odd and Even field.
01	Display start @ T_{VS} delay for Odd field and @ T_{VS} +1 for Even field. **(default)**
1X	Display start @ T_{VS} +1 delay for Odd field and @ T_{VS} for Even field.

Bit3-0	HDL function
0000	TSTV=TVStyp - 7 Hsync period

0111	TSTV=TVStyp - 0 Hsync period. **(default)**
1111	TSTV=TVStyp + 8 Hsync period

R9: VCOM DC settings

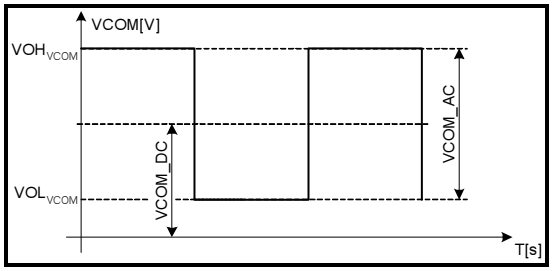
Address	Bit	Description		Default
1001	[6..0]	Bit6(VDCE)	VCOM DC Enable signal.	110_1101b
		Bit5-0(VCOM_DC)	VCOM DC level adjustment. Step 20mV/LSB.	

Bit6	VDCE function
0	VCOM DC function disables VCOM pin HighZ. VCOM_DC=VCOM_AC/2.
1	DC voltage of VCOM follows VCOM_DC settings.**(default)**

Bit5-0	VCOM DC level	
	MVA/Normal LC	Low Voltage LC
00h	1.4V	0.4V
2Dh	2.30V **(default)**	1.30V **(default)**
3Fh	2.66V	1.66V

VOL_{VCOM}= VCOM_DC-VCOM_AC/2

VOH_{VCOM}= VCOM_DC+VCOM_AC/2



VCOM AC DC level definition

F. Optical specifications (Note 1, 2)

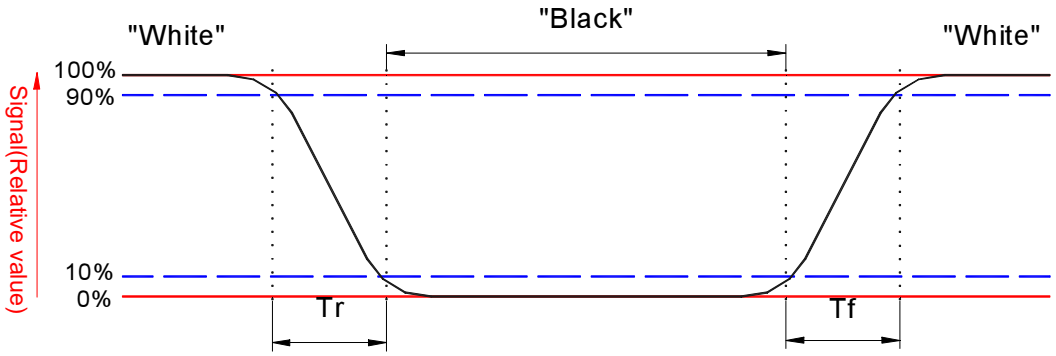
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	θ =0°	-	15	24	ms	Note 3
Fall	Tf		-	28	36	ms	
Contrast ratio	CR	At optimized viewing angle	150	300	-		Note 5, 6
Viewing Angle							
Top			35	50	-		
Bottom		CR≧10	40	55	-	deg.	Note 7, 8
Left			45	60	-		
Right			45	60	-		
Brightness	Y_L	θ =0°	280	330	-	cd/m^2	Note 9
NTSC				45		%	
White Chromaticity	X	θ =0°	0.26	0.31	0.36		
	y	θ =0°	0.28	0.33	0.38		

Note 1: Measurement should be performed in the dark room, optical ambient temperature =25°C, and backlight current I_L=20 mA

Note 2: To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.



Note 4. From liquid crystal characteristics, response time will become slower and the color of panel will become darker when ambient temperature is below 25℃.

$$\text{Contrastratio} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 5. Contrast ratio is calculated with the following formula.

Note 6. White Vi=Vi50 μ 1.5V

Black Vi=Vi50 ± 2.0V

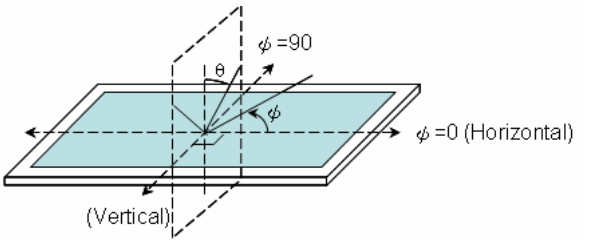
"±" means that the analog input signal swings in phase with COM signal.

"μ" means that the analog input signal swings out of phase with COM signal.

Vi50 :The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle: refer to figure as below.



Note 8. The viewing angles are measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 9. Brightness is measured at the center point of the display perpendicular to the surface.

G. Touch Screen Panel Specifications

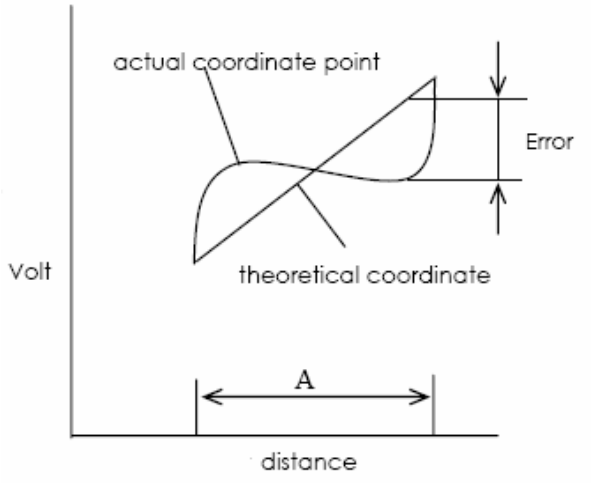
1. FPC Pin Assignment

Pin No.	Symbol
6	X1
7	Y1
8	X2
9	Y2

2. Electrical Characteristics

Item		Min.	Max.	Unit	Remark
Rate DC Voltage			7	V	
Resistance	X (Film)	350	950	Ω	At connector
	Y (Glass)	150	800		
Linearity		-1.5%	1.5%	--	Note 1, test by 250 gf
Chattering			10	ms	At connector pin
Insulation Resistance		10M		Ω	DC 25V

Note 1: Measurement condition of Linearity: difference between actual voltage & theoretical voltage is an error at any points. Linearity is the value max. error voltage divided by voltage difference on active area.



3. Mechanical Characteristics

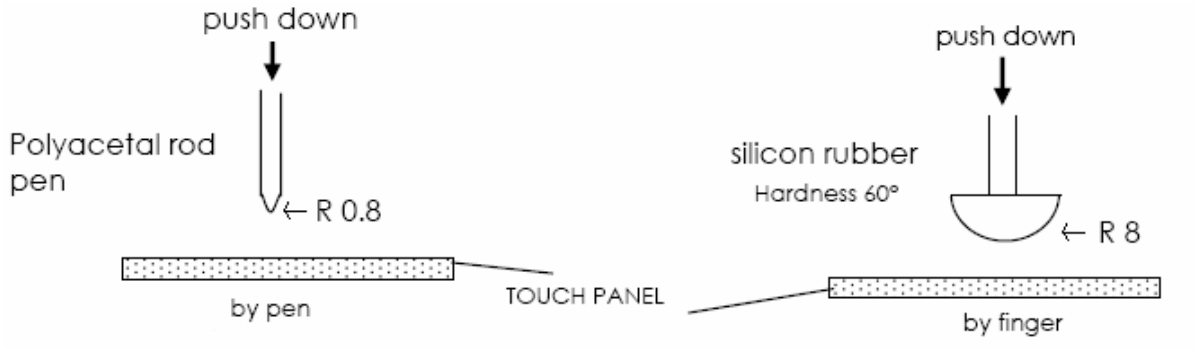
Item	Min.	Max.	Unit	Remark
Hardness of Surface	3	--	H	JIS K-5400
Operation Force (Pen or Finger)	--	50	gf	Note 1

Note 1: Within ”guaranteed active area”, but not on the edge and dot-spacer.

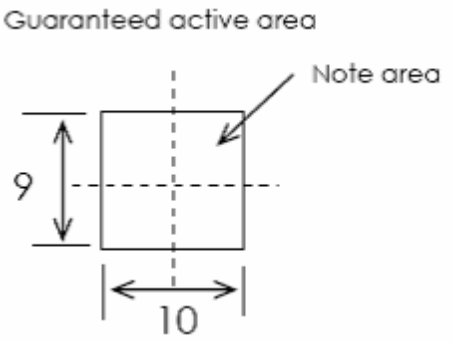
4. Life test Condition

Item	Min.	Max.	Unit	Remark
Notes Life	10^5	--	words	Note 1, 2
Input Life	10^6	--	times	Note 1, 3

Note 1: Measurement condition of Operation Force: Within "guaranteed active area". Resistance, Insulation resistance, and operation force should be under 5.2 & 5.3 condition. When user pushes down on the film, resistance between X & Y axis must be equal or lower than 2kΩ. Below is test figure.



Note 2: Notes Life test condition (by pen): Notes area for pen notes life test is 10×9 mm. Size of word is 7.5×6.75mm. Word is any A.B.C….. letter. Writing speed is 60mm/s. Center of each word is changed at random in notes area.



Note 3: Input Life test condition(by finger): By silicone rubber tapping at same point. Tapping Load is 200g, and tapping frequency is 5Hz.

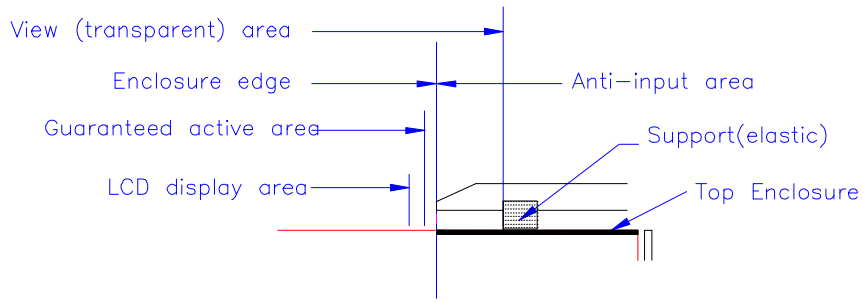
5. Attention

Please pay attention for below matters at mounting design of touch panel of LCD module.

1. Do not design enclosure pressing the view area to prevent from miss input.
2. Enclosure support must not touch with view area.
3. Use elastic or non-conductive material to enclosure touch panel.

4. Do not bond film of touch panel with enclosure.
5. The touch panel edge is conductive. Do not touch it with any conductive part after mounting.
6. If user wants to cleaning touch panel by air gun, pressure 2kg/cm2 below is suggested. Not to blow glass from FPC site to prevent FPC peeled off.
7. Do not put a heavy shock or stress on touch panel and film surface. Ex. Don't lift the panel by film face with vacuum.
8. Do not lift LCD module by FPC.
9. Please use dry cloth or soft cloth with neutral detergent (after wring dry) or one with ethanol at cleaning. Do not use any organic solvent, acid or alkali liquor.
10. Do not pile touch panel. Do not put heavy goods on touch panel.

Recommendation of the cushion area:



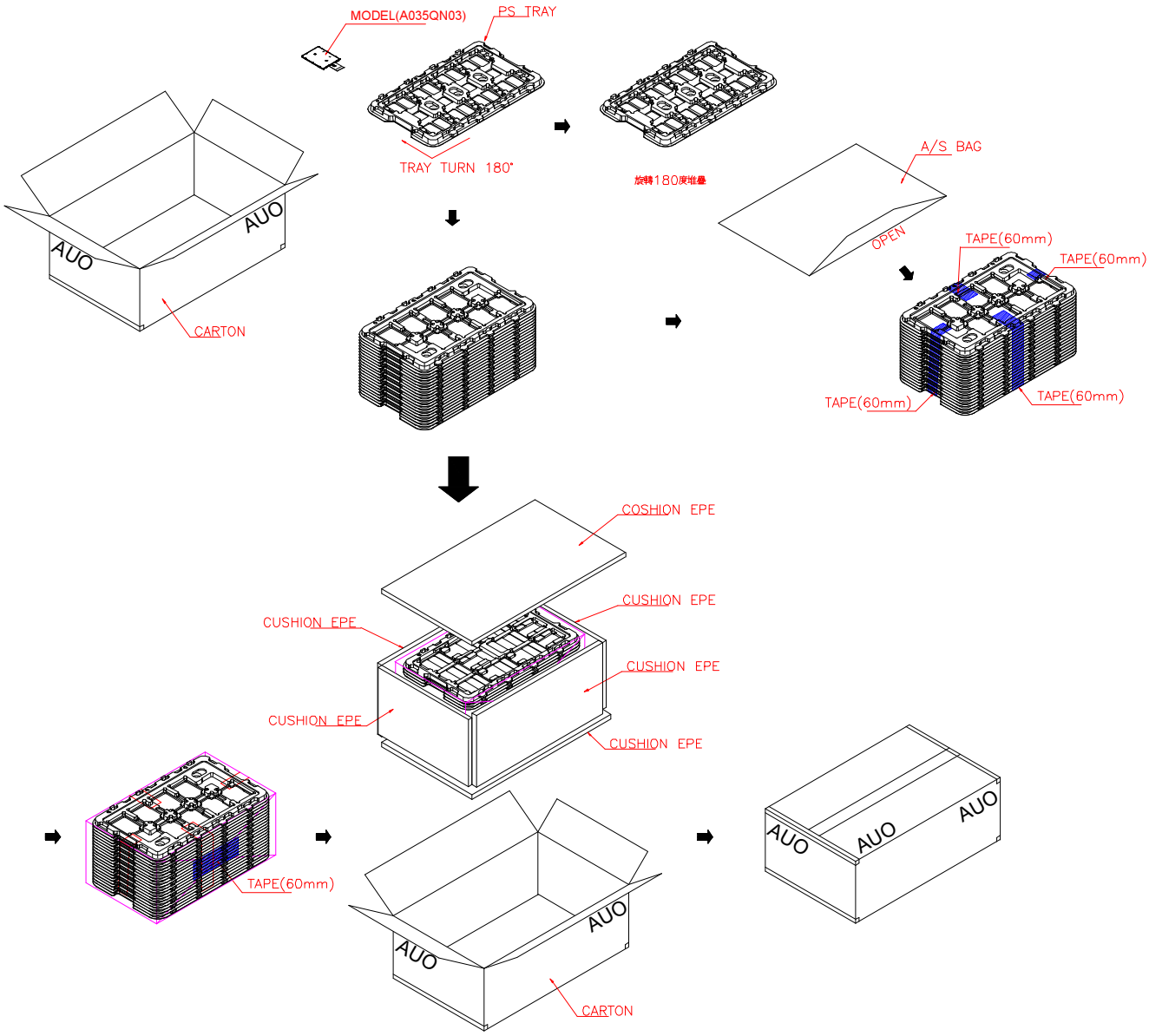
H. Reliability Test Items

No.	Test items	Conditions		Remark
1	High Temperature Storage	Ta= 70℃	240Hrs	
2	Low Temperature Storage	Ta= -30℃	240Hrs	
3	High Temperature Operation	Ta= 70℃	240Hrs	
4	Low Temperature Operation	Ta= -20℃	240Hrs	
5	High Temperature & High Humidity	Ta= 60℃. 90% RH	240Hrs	Operation
6	Heat Shock	-25℃~70℃, 50 cycle, 2Hrs/cycle		Non-operation
7	Electrostatic Discharge	±200V,200pF(0Ω), once for each terminal		Non-operation
8	Vibration (With Carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz		IEC 68-34
9	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces		
10	Touch Panel Impact Resistance	φ11mm(5g) steel ball Distance: 70cm Measured at the center of touch panel (Touch panel is supported around its four edges with 10mm thick and 10 mm wide PVC board)		

Note 1: Ta: Ambient temperature.

Note 2: In the standard condition, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

I. Packing Form



MAX. CAPACITY:160 MODULES
MAX. WEIGHT: 12Kg
MEAS. 520mm*340mm*250mm

J. Application Note

1. Application circuit

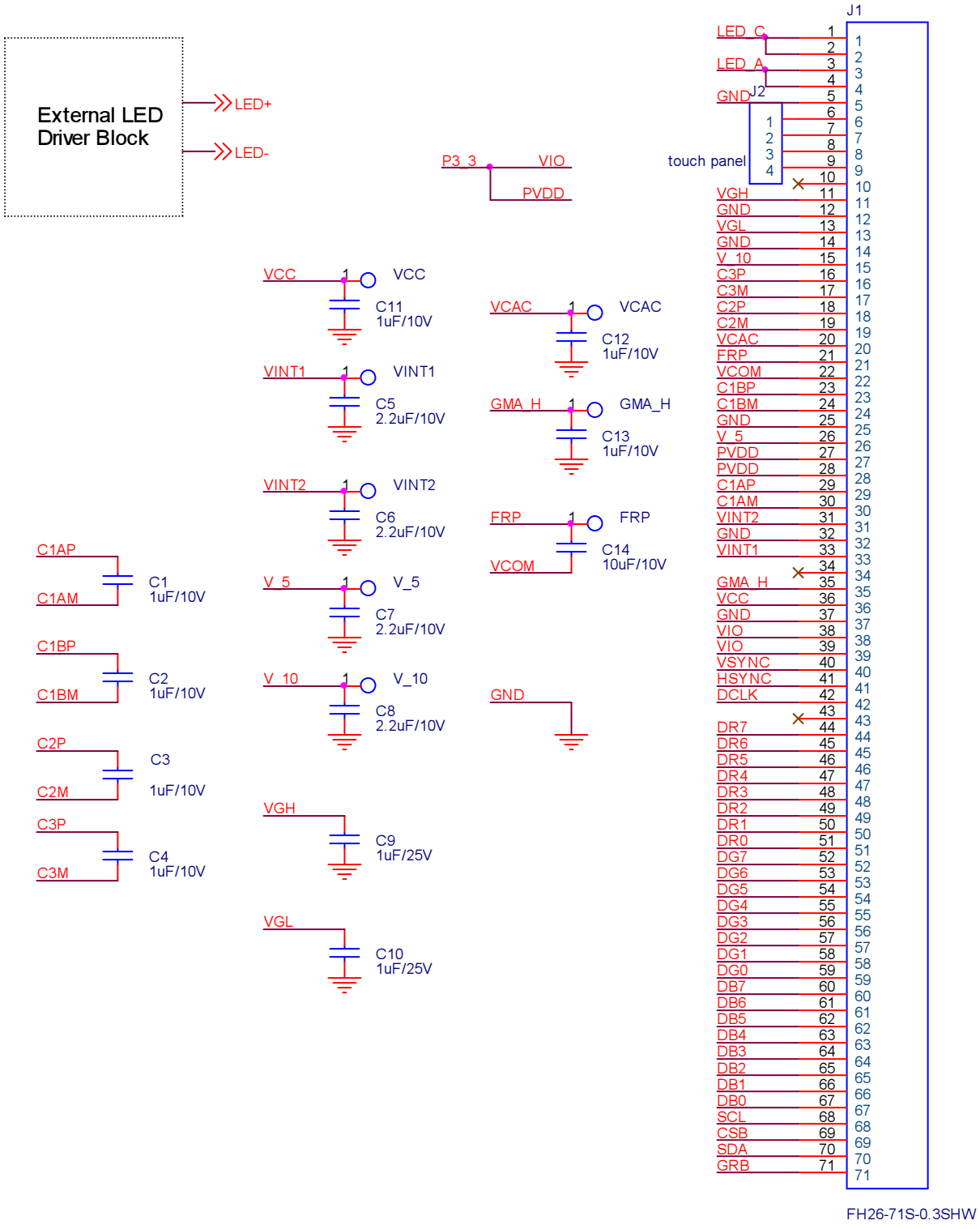


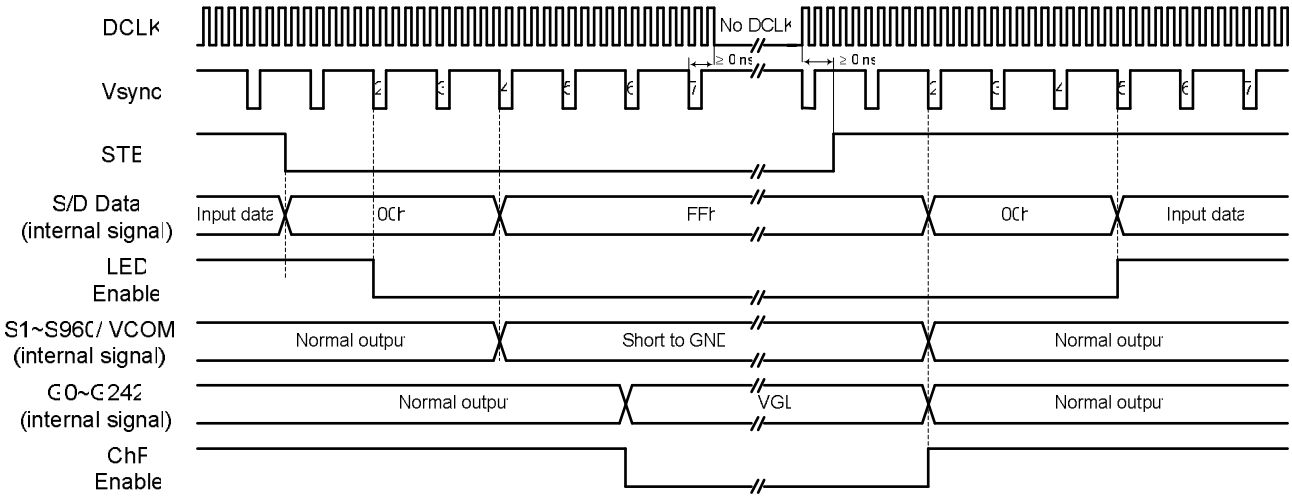
Table of Capacitors

Item	Quantity	Reference	Part
1	7	C1,C2,C3,C4,C11,C12,C13	1uF/10V/X7R

2†	4	C5,C6,C7,C8	1uF/10V/X7R
3	2	C9,C10	1uF/25V/X7R
4	1	C14	10uF/10V/X7R

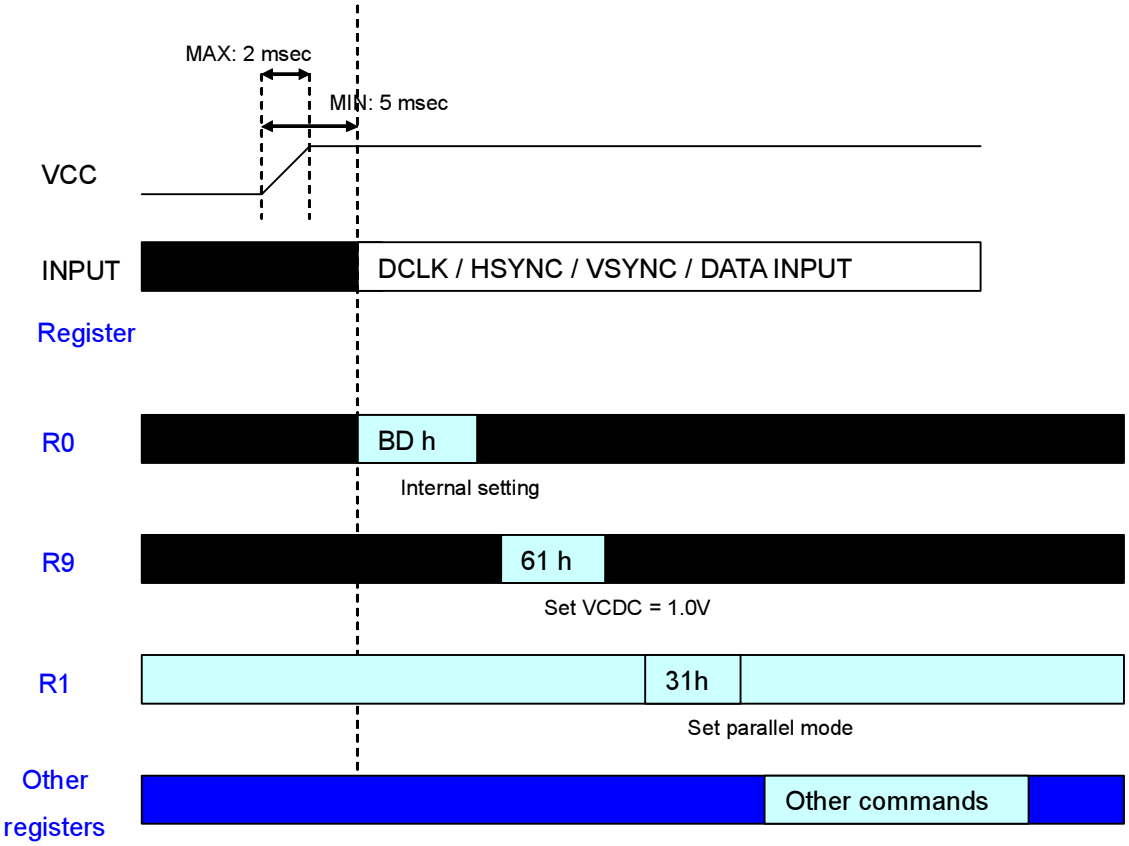
† 2.2uF is better.

2. Standby timing

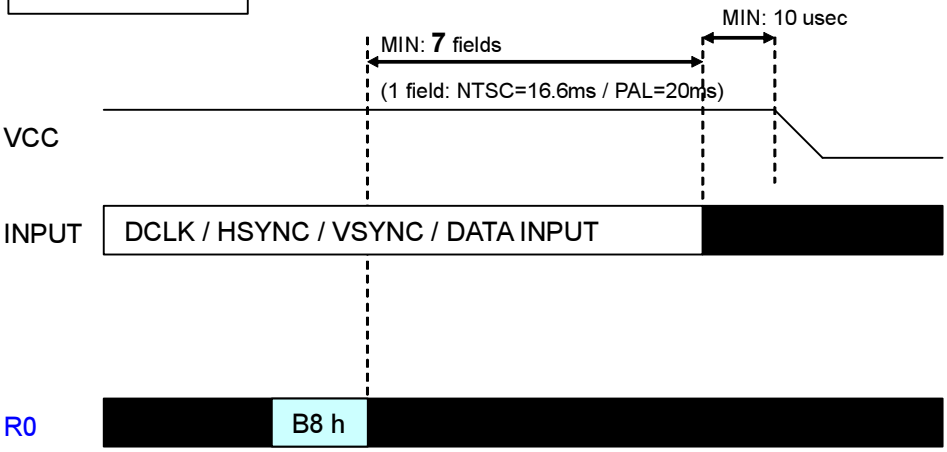


3. Recommand Parallel Interface Register Settings

POWER ON



POWER OFF



4. Recommand ESD Protection

- In order to recover from register corruption cause from ESD, AUO suggests that registers should be set repeatedly.
- AUO suggests the bezel connects to system GND to enhance ESD protection ability.