CUSTOMER APPROVAL SHEET

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MODEL	A025BN02 V5
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☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver. 0.4)**

AUO

Sales	PM	BU Head
	* 註明 Part No.:	

Doc. version : 0.4

Total pages：	52
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Product Specification

2.5″ COLOR TFT-LCD MODULE

MODEL NAME: A025BN02 V5

< ◆ > Preliminary Specification

< > Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	26/Mar/2007		First draft,
0.1	30/Apr/2007	40	Update module drawing.
0.2	30/Jul/2007	6	Update Electrical characteristics
		8	Modify Input timing format
		26	Modify Register description R4
0.3	20/Aug/2007	41	Update Module Drawing (Barcode size)
0.4	28/Aug/2007	41	Update Module Drawing (non-bending area)

Contents:

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution（dot）	640(W) × 240(H)	
2	Active area（mm）	49.92 x 37.44	
3	Screen size（inch）	2.5 (Diagonal)	
4	Dot pitch（mm）	0.078x0.156	
5	Color configuration	R G B delta	
6	Overall dimension（mm）	59.63(W) ×43.7(H) ×2.7(D)	Note 1
7	Weight（g）	13	
8	Panel surface treatment	Hard Coating (3H)	

Note 1: Refer to F. Outline Dimension

B. Electrical specifications

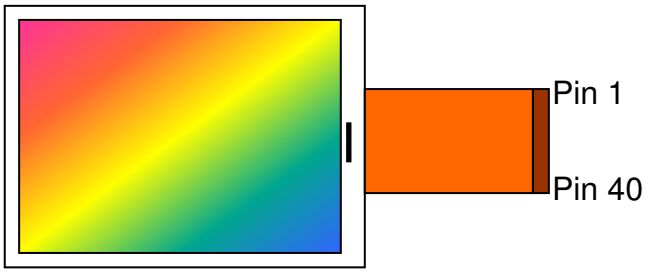
1. Pin assignment

Pin no	Symbol	I/O	Description	Remark
1	VCOM	I	Panel common voltage	
2	CS	I	Serial command enable	
3	SDA	I	Serial command data input	
4	SCL	I	Serial command clock input	
5	HSYNC	I	Horizontal sync input	
6	VSYNC	I	Vertical sync input	
7	DCLK	I	Data clock input	
8	D7	I	Data input; MSB	
9	D6	I	Data input	
10	D5	I	Data input	
11	D4	I	Data input	
12	D3	I	Data input	
13	D2	I	Data input	
14	D1	I	Data input	
15	D0	I	Data input; LSB	
16	GND	P	Ground for digital circuit	
17	VDD	P	System power	
18	VDDIO	P	Power supply for digital interface	1.8V~VDD
19	DVDD	C	Power setting capacitor connect pin	
20	V1	C	Power setting capacitor connect pin	
21	V2	C	Power setting capacitor connect pin	
22	V3	C	Power setting capacitor connect pin	
23	V4	C	Power setting capacitor connect pin	
24	VDD2	C	Power setting capacitor connect pin	
25	V5	C	Power setting capacitor connect pin	
26	V6	C	Power setting capacitor connect pin	
27	VDD3	C	Power setting capacitor connect pin	
28	VDD5	C	Power setting capacitor connect pin	
29	V7	C	Power setting capacitor connect pin	
30	V8	C	Power setting capacitor connect pin	
31	VGH	C	Power setting capacitor connect pin	
32	VGL	C	Power setting capacitor connect pin	

33	AGND	P	Ground for analog circuit	
34	FRP	O	Frame polarity output for VCOM	
35	COMDC	O	VCOM DC voltage output pin	
36	VCAC	C	Power setting capacitor for VCOM AC	
37	DRV	O	VLED boost transistor driving signal	
38	VLED	P	LED power anode	
39	FB	P	LED power cathode	
40	VCOM	I	Panel common voltage	

I：Input O：Output C：Capacitor P：Power

Note: Definition of scanning direction, Refer to figure as below：



2. Absolute maximum ratings

Item	Symbol	Min.	Max.	Unit	Remark
Digital Supply voltage	VDDIO	-0.5	5.0	V	
	DVDD	-0.5	5.0	V	
Supply voltage	VDD	-0.5	5.5	V	
Storage temperature	Tst	-25	80	□	
Operating temperature	Top	0	60	□	

3. Electrical characteristics

a. Typical operating conditions.(GND=AGND=0V)

(VDD=3.0~3.6V, VDDIO=1.8V~VDD, DVDD=1.8~2.2V, AGND=GND=0V, TA=25℃)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Charge pump supply voltage		VDD	3.0	3.3	3.6	V	--
Digital Interface Supply Voltage		VDDIO	1.8	-	VDD	V	--
Positive power supply		VGH	14.5	15	15.5	V	
Negative power supply		VGL	-10.5	-10	-9.5	V	
Input Voltage	Low Level	Vil	GND	-	0.2xVDDIO	V	Digital input pins
	High Level	Vih	0.8xVDDIO	-	GND	V	Digital input pins
Digital standby current		Idst1	-	3	8	uA	VDD=3.3V, DCLK is stopped.
		Idst2	-	15	25	uA	VDD=3.3V, DCLK input.
Digital operating current		Idop	-	2.5	3.5	mA	VDD=3.3V
Analog standby current		Iast	-	80	100	uA	VDD=3.3V
Analog operating current		Iaop	-	7.5	8.5	mA	VDD=3.3V,No loading
VCOM	VCAC	V_{CAC}	4.0	4.2	4.4	Vp-p	
	VCDC	V_{CDC}	-	0.3	-	V	

b. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	I_L	-	25		mA	
LED voltage	V_L	-	3.3	3.6	V	1 pcs LED
LED Life Time	L_L	-	7000	-	Hr	Note 1 and 2
Feedback voltage	V_{FB}	-	0.6	-	V	

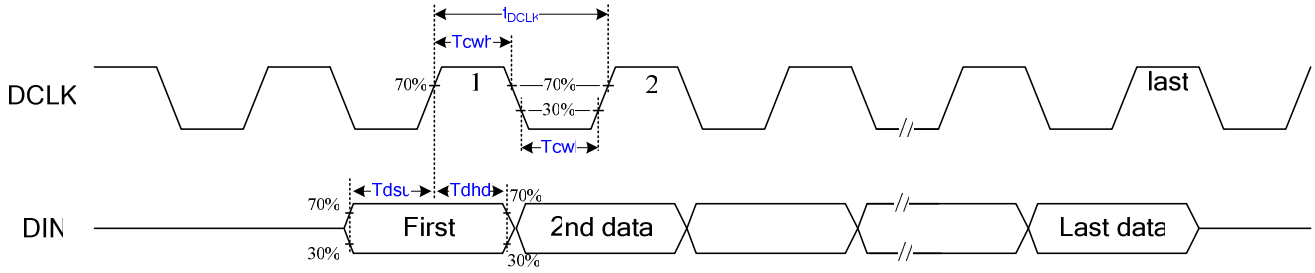
Note 1: Ta. = 25℃, I_L = 25mA

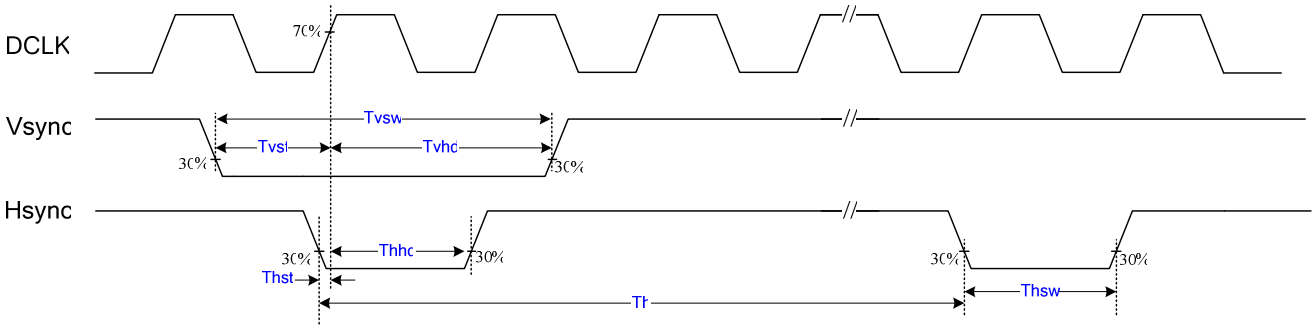
Note 2: Brightness to be decreased to 50% of the initial value

4. Input timing AC characteristic

(VDD=3.0 ~3.6V, VDDIO=1.8V~VDD, DVDD=1.8~2.2V, AGND=GND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK period time	t_{DCLK}	35	-	-	ns	
HSYNC period time	Th	60	63.56	67	us	
VSYNC setup time	Tvst	12	-	-	ns	
VSYNC hold time	Tvhd	12	-	-	ns	
HSYNC setup time	Thst	12	-	-	ns	
HSYNC hold time	Thhd	12	-	-	ns	
Data setup time	Tdst	12	-	-	ns	
Data hold time	Tdhd	12	-	-	ns	
HSYNC width	Thsw	1	1	96	t_{DCLK}	
VSYNC width	Tvsw	1 t_{DCLK}	1 t_{DCLK}	6Th		
DCLK duty cycle	Tcwh/Tcwl	40	50	60	%	





5. Input timing format

a. UPS051 timing conditions.(refer to Fig.1 Fig.2 Fig.3)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	11.29	13.5	13.59	MHz	
HSYNC	Period		t_H	768	858	864	t_{DCLK}	
	Display period		t_{hd}	640			t_{DCLK}	
	Back porch		t_{hbp}	20	30	121	t_{DCLK}	Note 1
	Front porch		t_{hfp}	103	188	-	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	t_{hbp} - 1	t_{DCLK}	
VSYNC	Period	Odd	t_V	241	262.5	-	t_H	
		Even						
	Display period	Odd	t_{vd}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	3	21	31	t_H	Note 2
		Even		3.5	21.5	31.5		
	Front porch	Odd	t_{vfp}	1	1.5	-	t_H	
		Even		1	1	-		
	Pulse width	Odd	t_{vsw}	1	1	-	t_{DCLK}	
		Even						
	1 frame			-	525	-		

(*): When t_H = 68us, t_V=245tH

Note1: t_{hbp} is programmable, please refer to HBLK setting.

Note2: t_{vbp} is programmable, please refer to VBLK setting.

Note3: UPS051 support interlacing input format

Note4: UPS051 support non-interlacing input format. Odd field only or even field only

Fig.1 UPS051 Input Horizontal Timing Chart

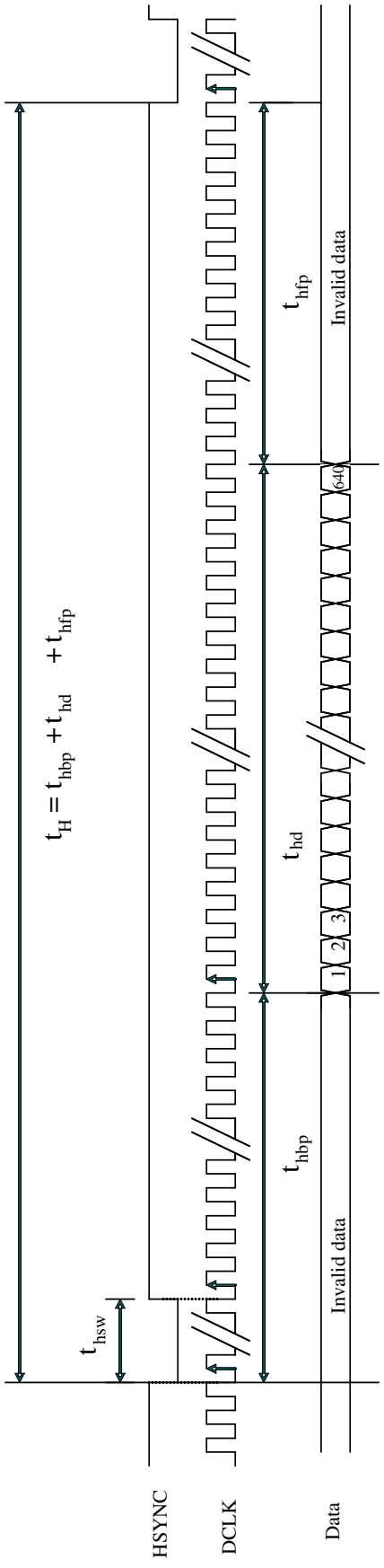


Fig.2 UPS051 Input Horizontal Data Sequence

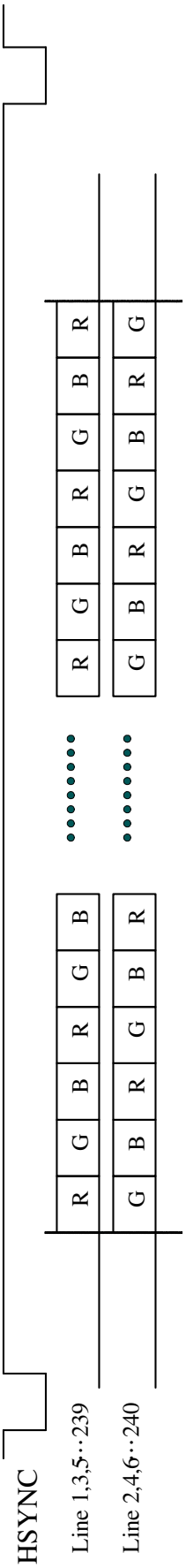
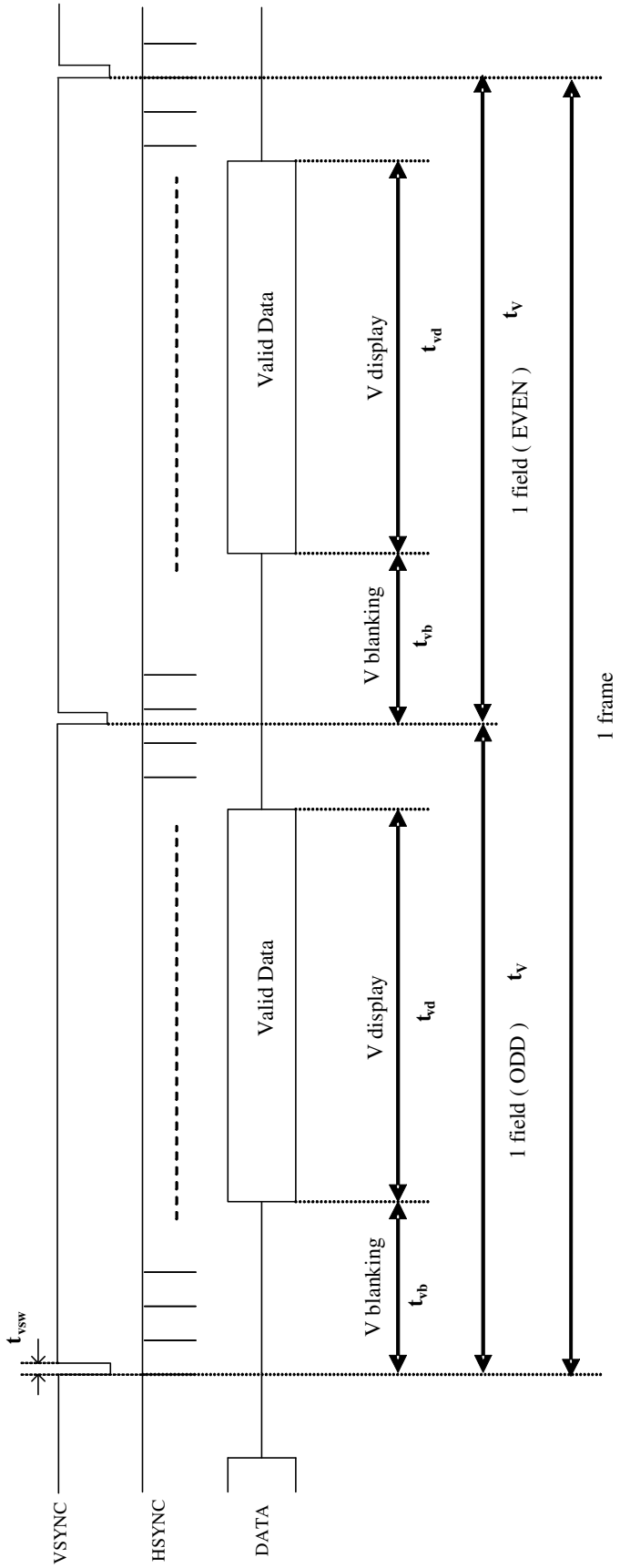


Fig.3 UPS051 Input Vertical Timing Chart



b.1 UPS052 (320 mode/NTSC/24.535MHz) timing specifications.(refer to Fig.4 Fig.5)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	24.535	-	MHz	
HSYNC	Period		t_H	-	1560	-	t_{DCLK}	
	Display period		t_{hdisp}	-	1280	-	t_{DCLK}	
	Back porch		t_{hbp}	-	241	-	t_{DCLK}	
	Front porch		t_{hfp}	-	-	-	t_{DCLK}	
	Pulse width		t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	Odd	t_V	-	262.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}	-	240	-	t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	21	-	t_H	
		Even		-	21.5	-		
	Front porch	Odd	t_{vfp}	-	1.5	-	t_H	
		Even		-	1	-		
	Pulse width	Odd	t_{vsw}	-	1	-	t_{DCLK}	
		Even						
	1 frame			-	525	-	t_H	

b.2 UPS052 (320 mode/PAL/24.535MHz) timing specifications(refer to Fig.4 Fig.5)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	24.375	-	MHz	
HSYNC	Period		t_H	-	1560	-	t_{DCLK}	
	Display period		t_{hdisp}	-	1280	-	t_{DCLK}	
	Back porch		t_{hbp}	-	241	-	t_{DCLK}	
	Front porch		t_{hfp}	-	-	-	t_{DCLK}	
	Pulse width		t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	Odd	t_V	-	312.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}	-	288	-	t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	24	-	t_H	
		Even		-	24.5	-		
	Front porch	Odd	t_{vfp}	-	0.5	-	t_H	
		Even		-	0	-		
	Pulse width	Odd	t_{vsw}	-	1	-	t_{DCLK}	
		Even						
	1 frame			-	625	-	t_H	

b.3 UPS052 (360 mode/NTSC/27MHz) timing specifications(refer to Fig.4 Fig.5)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	27	-	MHz	
HSYNC	Period		t_H	-	1716	-	t_{DCLK}	
	Display period		t_{hdisp}	-	1440	-	t_{DCLK}	
	Back porch		t_{hbp}	-	241	-	t_{DCLK}	
	Front porch		t_{hfp}	-	-	-	t_{DCLK}	
	Pulse width		t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	Odd	t_V	-	262.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}	-	240	-	t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	21	-	t_H	
		Even		-	21.5	-		
	Front porch	Odd	t_{vfp}	-	1.5	-	t_H	
		Even		-	1	-		
	Pulse width	Odd	t_{vsw}	-	1	-	t_{DCLK}	
		Even						
	1 frame			-	525	-	t_H	

b.4 UPS052 (360 mode/PAL/27MHz) timing specifications(refer to Fig.4 Fig.5)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	27	-	MHz	
HSYNC	Period		t_H	-	1728	-	t_{DCLK}	
	Display period		t_{hdisp}	-	1440	-	t_{DCLK}	
	Back porch		t_{hbp}	-	241	-	t_{DCLK}	
	Front porch		t_{hfp}	-	-	-	t_{DCLK}	
	Pulse width		t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	Odd	t_V	-	312.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}	-	288	-	t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	24	-	t_H	
		Even		-	24.5	-		
	Front porch	Odd	t_{vfp}	-	0.5	-	t_H	
		Even		-	0	-		
	Pulse width	Odd	t_{vsw}	-	1	-	t_{DCLK}	
		Even						
	1 frame			-	625	-	t_H	

Fig.4 UPS052 Input Horizontal Timing Chart

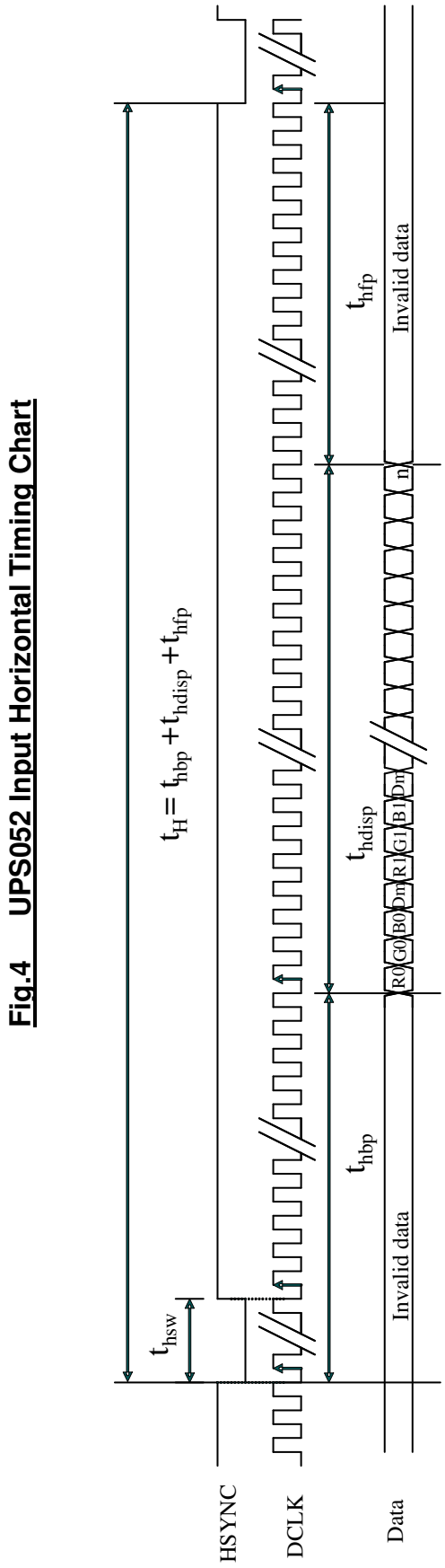
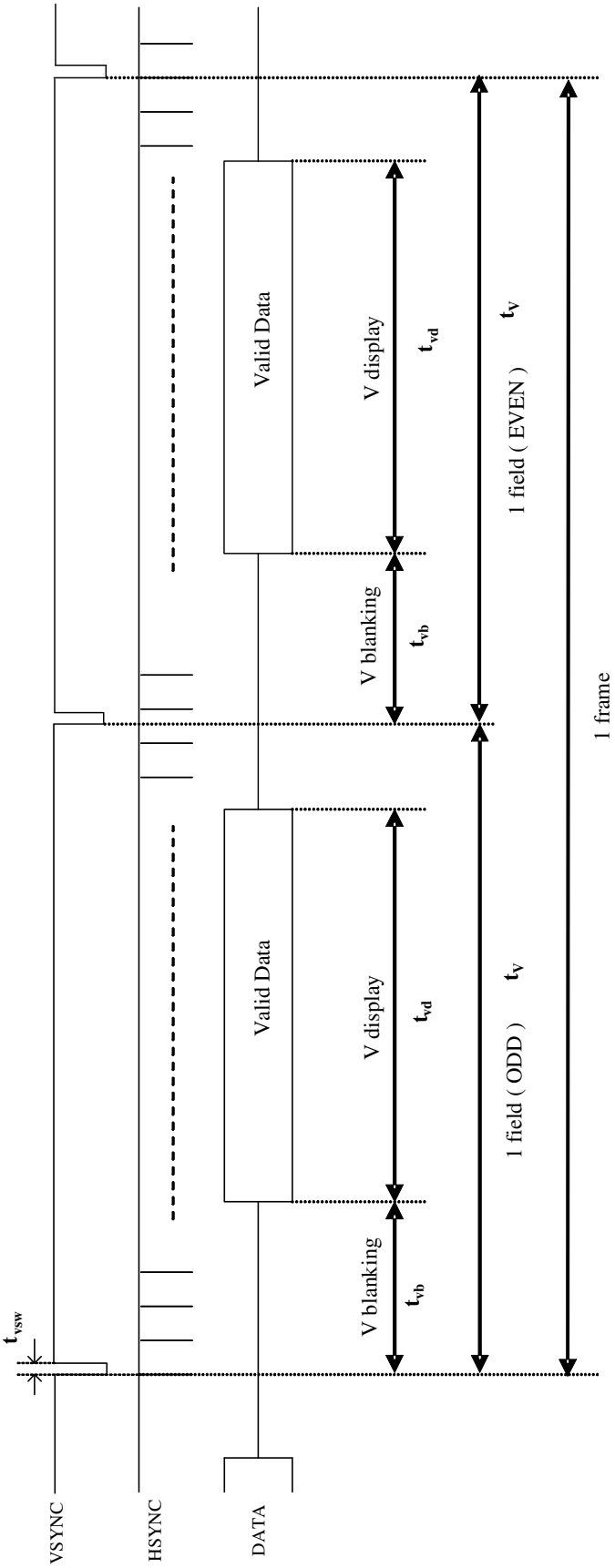


Fig.5 UPS052 Input Vertical Timing Chart



c. CCIR656 Timing

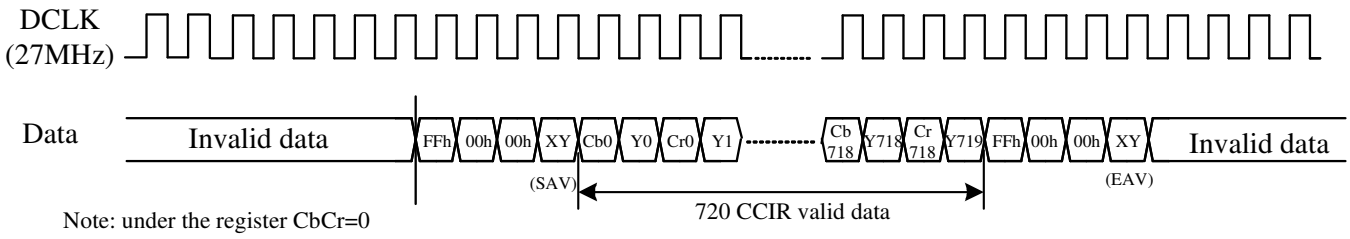


Fig.6 CCIR656 Data input format

c.1 CCIR656 decoding

- FF 00 00 < XY > signals are involved with HSYNC, VSYNC and Field
- <XY> encode following bits:

F=field select : F=0 for field 1, F=1 for field 2;

V=1 during vertical blanking

H=0 at SAV , H=1 at EAV ,

P3-P0=protection bits :

P3=V □ H P2=F □ H P1=F □ V P0=F □ V □ H □: represents the exclusive-OR function

- Control is provided through “End of Video” (EAV) and “Start of Video” (SAV) timing references.
- Horizontal blanking section consists of repeating pattern 80 10 80 10

XY							
D7(MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0(LSB)**
1	F	V	H	P3	P2	P1	P0

c.2 CCIR656 to RGB conversion

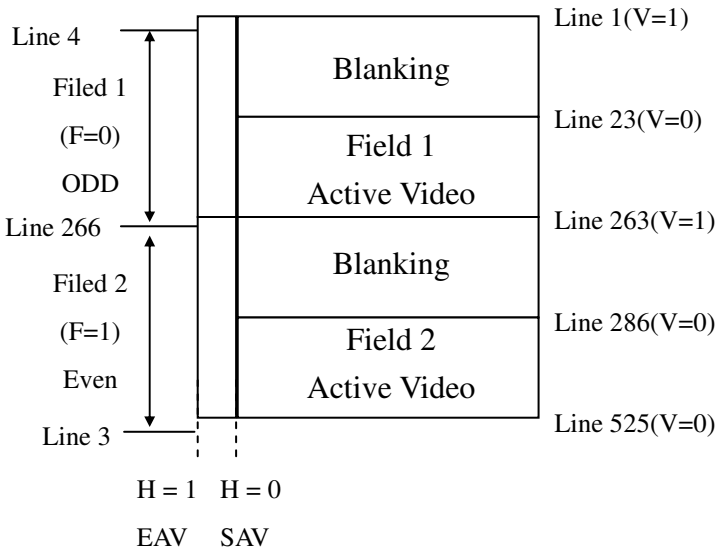
Rn=(Y2n+Y2n+1)/2 +1.371*(Cr2n-128)

Gn=(Y2n+Y2n+1)/2 -0.698(Cr2n-128)-0.336(Cb2n-128)

Bn=(Y2n+Y2n+1)/2 +1.732(Cb2n-128)

Where Y:16~235 Cr:16~240 Cb:16~240

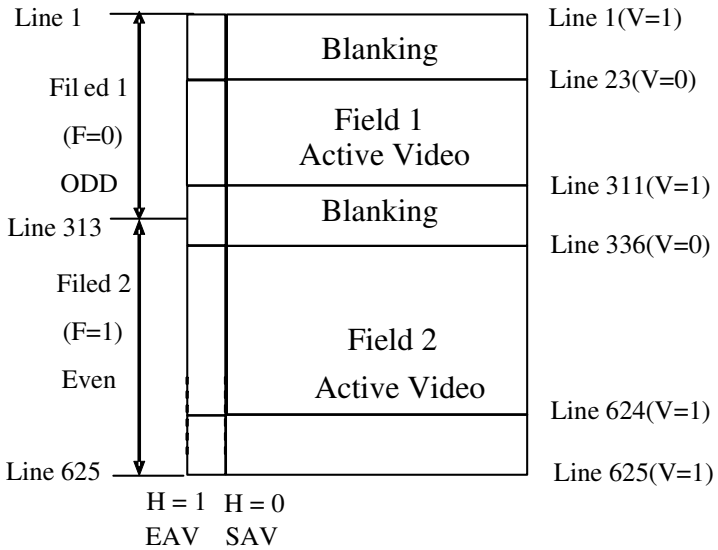
c.3 CCIR656 NTSC



Line Number	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	Even Field	EAV	Blanking
0	Odd Field	SAV	Active Video

c.4 CCIR656 PAL



Line Number	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
335-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	Even Field	EAV	Blanking
0	Odd Field	SAV	Active Video

d.1 YUV 720 mode/NTSC timing specifications(refer to Fig.7 Fig.9)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	27	-	MHz	
HSYNC	Period		t_H	-	1716	-	t_{DCLK}	
	Display period		t_{hdisp}	-	1440	-	t_{DCLK}	
	Back porch		t_{hbp}	-	240	-	t_{DCLK}	
	Front porch		t_{hfp}	-	-	-	t_{DCLK}	
	Pulse width		t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	Odd	t_V	-	262.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}	-	240	-	t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	21	-	t_H	
		Even		-	21.5	-		
	Front porch	Odd	t_{vfp}	-	1.5	-	t_H	
		Even		-	1	-		
	Pulse width	Odd	t_{vsw}	-	1	-	t_{DCLK}	
		Even						
	1 frame			-	525	-	t_H	

d.2 YUV 720 mode/PAL timing specifications(refer to Fig.7 Fig.9)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	27	-	MHz	
HSYNC	Period		t_H	-	1728	-	t_{DCLK}	
	Display period		t_{hdisp}	-	1440	-	t_{DCLK}	
	Back porch		t_{hbp}	-	240	-	t_{DCLK}	
	Front porch		t_{hfp}	-	-	-	t_{DCLK}	
	Pulse width		t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	Odd	t_V	-	312.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}	-	288	-	t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	24	-	t_H	
		Even		-	24.5	-		
	Front porch	Odd	t_{vfp}	-	0.5	-	t_H	
		Even		-	0	-		
	Pulse width	Odd	t_{vsw}	-	1	-	t_{DCLK}	
		Even						
	1 frame			-	625	-	t_H	

d.3 YUV 640 mode/NTSC timing specifications(refer to Fig.8 Fig.9)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	24.535	-	MHz	
HSYNC	Period		t_H	-	1560	-	t_{DCLK}	
	Display period		t_{hdisp}	-	1280	-	t_{DCLK}	
	Back porch		t_{hbp}	-	240	-	t_{DCLK}	
	Front porch		t_{hfp}	-	-	-	t_{DCLK}	
	Pulse width		t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	Odd	t_V	-	262.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}	-	240	-	t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	21	-	t_H	
		Even		-	21.5	-		
	Front porch	Odd	t_{vfp}	-	1.5	-	t_H	
		Even		-	1	-		
	Pulse width	Odd	t_{vsw}	-	1	-	t_{DCLK}	
		Even						
	1 frame			-	525	-	t_H	

d.4 YUV 640 mode/PAL timing specifications(refer to Fig.8 Fig.9)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	-	24.375	-	MHz	
HSYNC	Period		t_H	-	1560	-	t_{DCLK}	
	Display period		t_{hdisp}	-	1280	-	t_{DCLK}	
	Back porch		t_{hbp}	-	240	-	t_{DCLK}	
	Front porch		t_{hfp}	-	-	-	t_{DCLK}	
	Pulse width		t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	Odd	t_V	-	312.5	-	t_H	
		Even						
	Display period	Odd	t_{vdisp}	-	288	-	t_H	
		Even						
	Back porch	Odd	t_{vbp}	-	24	-	t_H	
		Even		-	24.5	-		
	Front porch	Odd	t_{vfp}	-	0.5	-	t_H	
		Even		-	0	-		
	Pulse width	Odd	t_{vsw}	-	1	-	t_{DCLK}	
		Even						
	1 frame			-	625	-	t_H	

Fig.7 YUV720 Input Horizontal Timing Chart

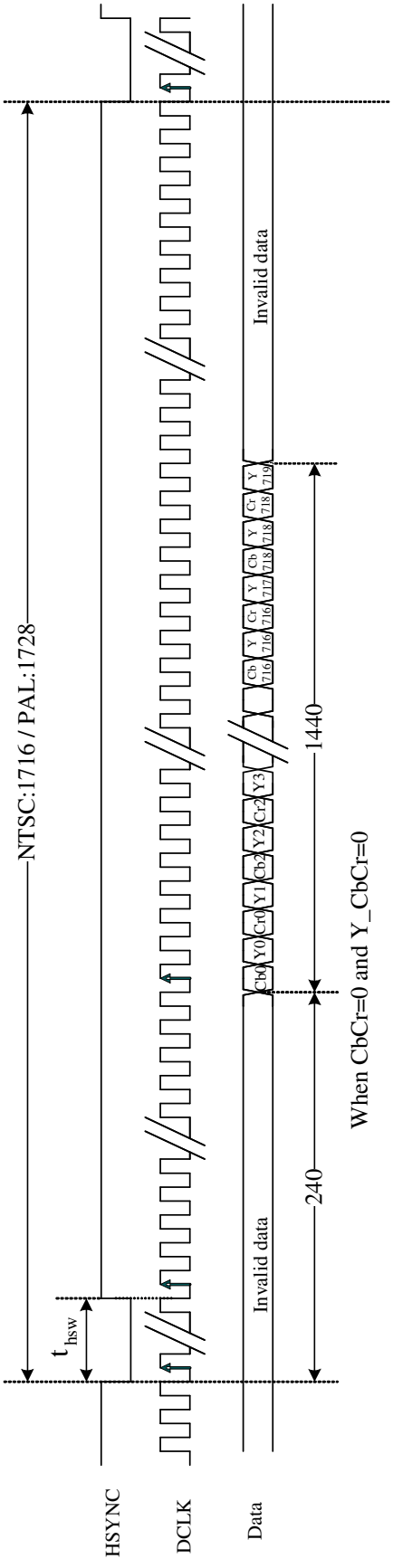


Fig.8 YUV640 Input Horizontal Timing Chart

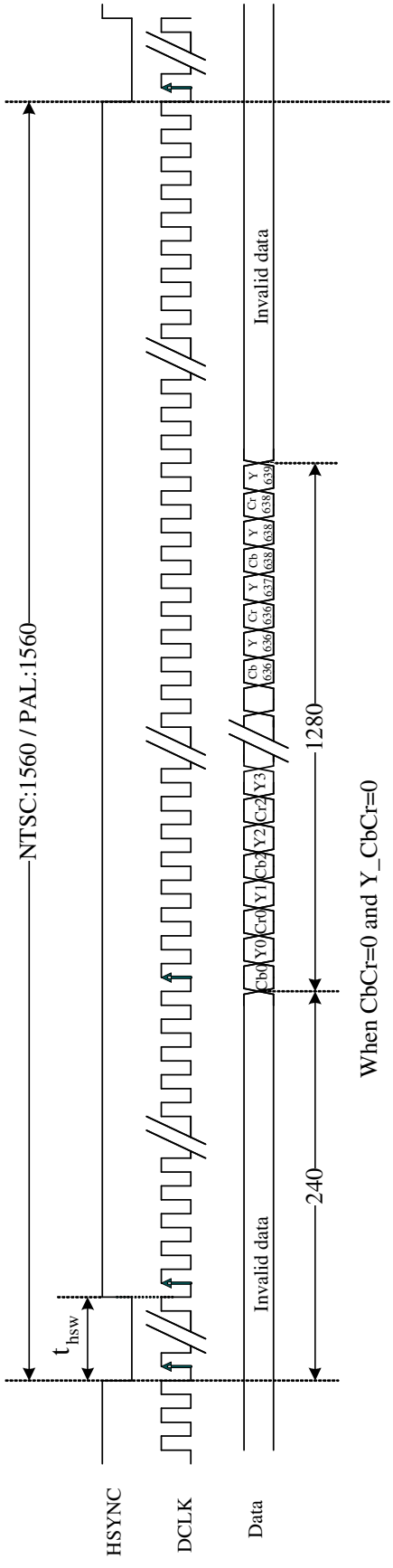
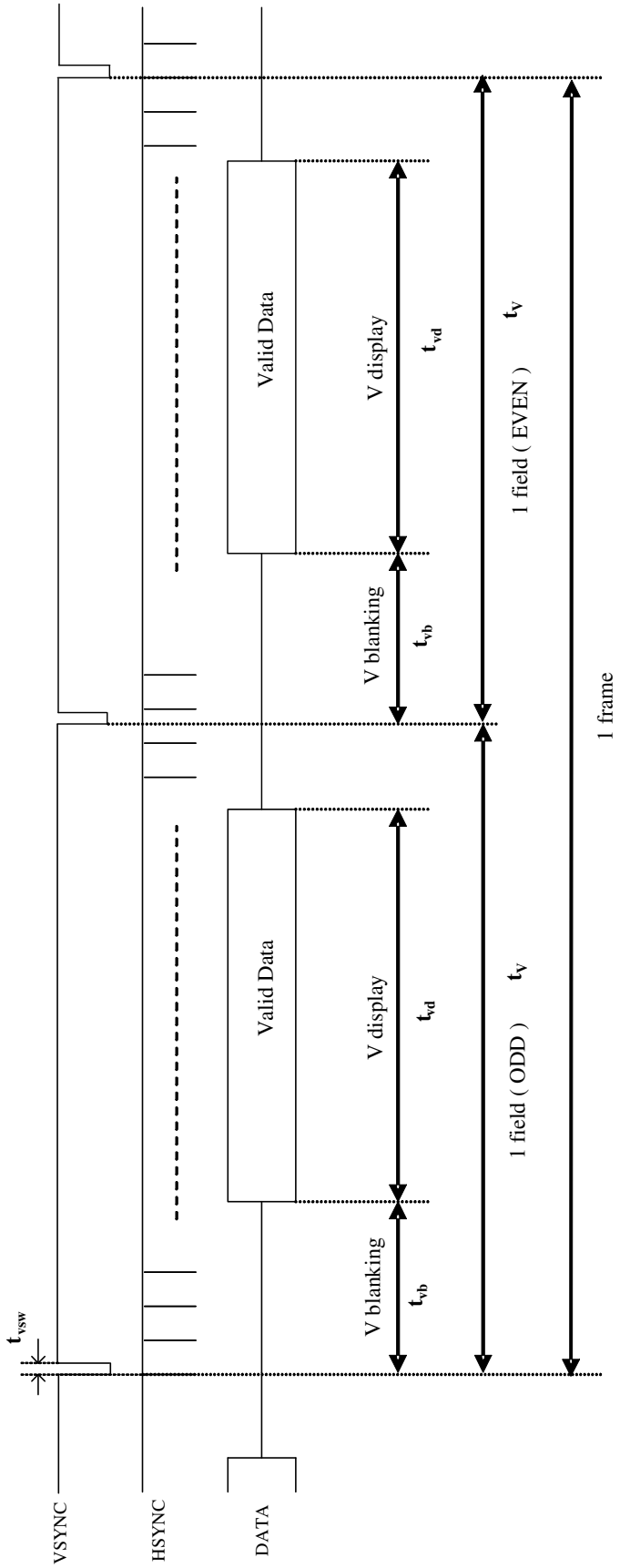
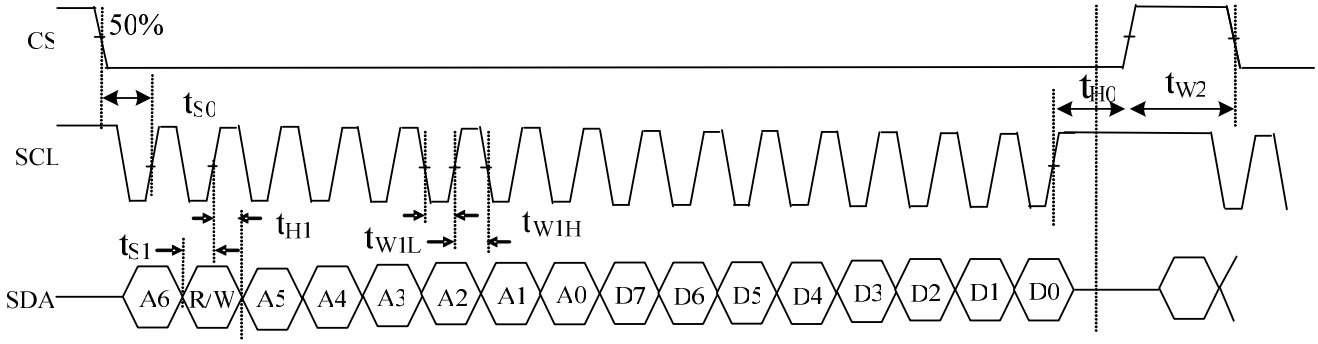


Fig.9 YUV Input Vertical Timing Chart

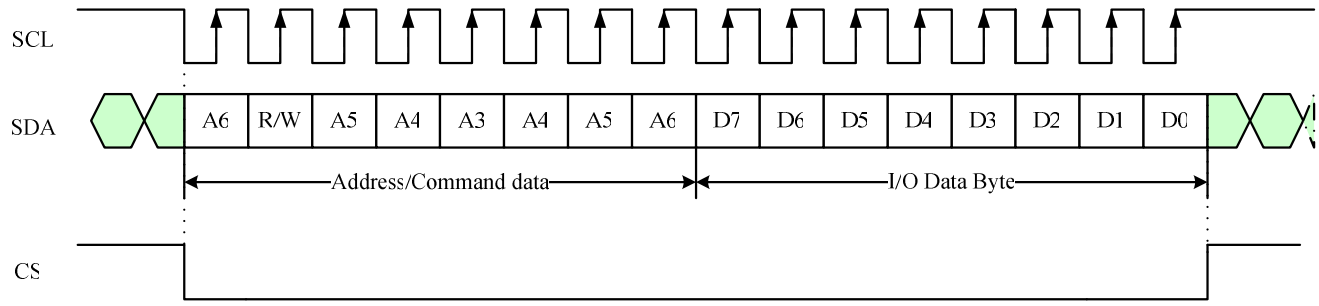


6. Serial interface AC characteristic



Item	Symbol	Min	Typical	Max	Unit
CS input setup Time	t_{S0}	50	-	-	ns
Serial data input setup Time	t_{S1}	50	-	--	ns
CS input hold Time	t_{H0}	50	-	-	ns
Serial data input hold Time	t_{H1}	50	-	-	ns
SCL pulse low width	t_{W1L}	50	-	-	ns
SCL pulse high width	t_{W1H}	50	-	-	ns
CS pulse high width	t_{W2}	400	-	-	ns

a. Serial control timing chart



1. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.
2. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
3. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.
4. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
5. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data before the rising edge of CS pulse are valid data.
6. Serial block operates with the SCL clock
7. Serial data can be accepted in the power save mode.

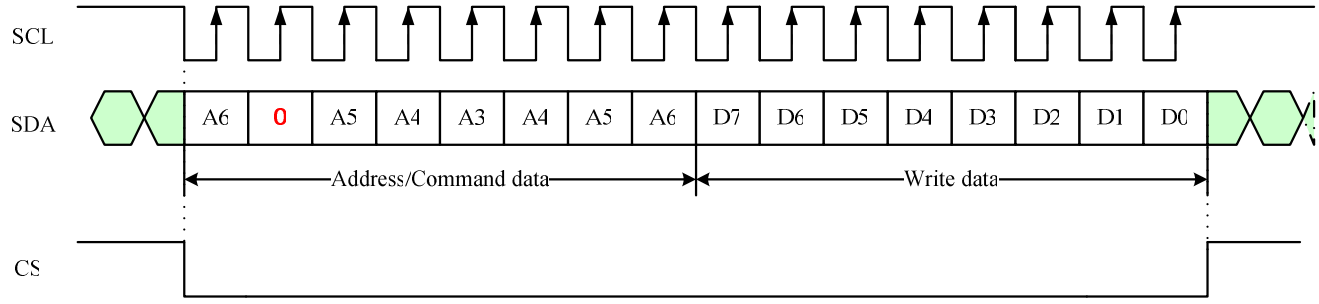
b. The configuration of serial data at SDA terminal is at below

MSB LSB

A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Address	R/W	Address						DATA							

R/W: Establishes the Read mode when set to ‘1’, and the Write mode when set to ‘0’.

Write Mode:



7. Register table

a. Register parameters

No.	Register address								MSB Register data LSB							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	Y_CbCr (0)	CCIR601 (0)	x	x	VCAC (0)	VCOM_AC (011)		
R1	0	0	0	0	0	0	0	1	VCDCE(1)	x	VCOM_DC(1Eh)					
R3	0	0	0	0	0	0	1	1	Brightness (40h)							
R4	0	0	0	0	0	1	0	0	Narrow (0)	YUV (0)	SEL (00)		NTSC/PAL (10)		VDIR (1)	HDIR (1)
R5	0	0	0	0	0	1	0	1	DRV_FREQ (0)	GRB (1)	x	PFM_DUTY (10)		SHDB2 (1)	SHDB1 (1)	STB (0)
R6	0	0	0	0	0	1	1	0	HBLK_EN (0)	LED_Current (00)	VBLK (15h)					
R7	0	0	0	0	0	1	1	1	HBLK(1Eh)							
R8	0	0	0	0	1	0	0	0	BL_DRV(00)		x	x	x	x	x	x
R12	0	0	0	0	1	1	0	0	PAIR(00)		x	CbCr(0)	x	Vdpol(1)	Hdpol(1)	DCLKpol(0)
R13	0	0	0	0	1	1	0	1	CONTRAST_B(40h)							
R14	0	0	0	0	1	1	0	1	x	SUB-CONTRAST_R(40h)						
R15	0	0	0	0	1	1	1	1	x	SUB-BRIGHTNESS_R(40h)						
R16	0	0	0	1	0	0	0	0	x	SUB-CONTRAST_B(40h)						
R17	0	0	0	1	0	0	0	1	x	SUB-BRIGHTNESS_B(40h)						
R21	0	0	0	1	0	1	0	1	LED_ON_CYCLE(0111)				LED_ON_RATIO(1111)			
R22	0	0	0	1	0	1	1	0	x	x	x	x	x	GAMMA2.2(1)	x	x
R23	0	0	0	1	0	1	1	1	x	GMA_V8(101)			x	GMA_V4(100)		
R24	0	0	0	1	1	0	0	0	x	GMA_V25(101)			x	GMA_V16(100)		
R25	0	0	0	1	1	0	0	1	x	GMA_V48(100)			x	GMA_V36(011)		
R26	0	0	0	1	1	0	1	0	x	GMA_V60(101)			x	GMA_V55(100)		

“X” => Please set to ‘0’.

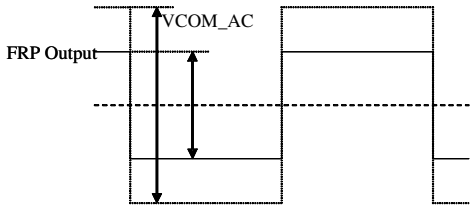
b. Register description

R0:

No.	Register address								MSB		Register data					LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	Y_CbCr(0)	CCIR601(0)	x	x	VCAC(0)	VCOM_AC(011)		

VCOM_AC: Common voltage AC level selection (deviation ±0.1V)

VCOM_AC			VCAC	Voltage(V)
D2	D1	D0	D3	
0	0	0	0	3.6
0	0	0	1	3.7
0	0	1	0	3.8
0	0	1	1	3.9
0	1	0	0	4.0
0	1	0	1	4.1
0	1	1	0	4.2(Default)
0	1	1	1	4.3
1	0	0	0	4.4
1	0	0	1	4.5
1	0	1	0	4.6
1	0	1	1	4.7
1	1	X	X	4.8



CCIR601: CCIR601 input timing selection

CCIR601	Function
0(Default)	Disable CCIR601 (Default)
1	Enable CCIR601. (please refer to the table of R4(SEL) for detail description)

Y_CbCr: Y & CbCr exchange position (only valid for 8-bit input YUV640 / YUV720)

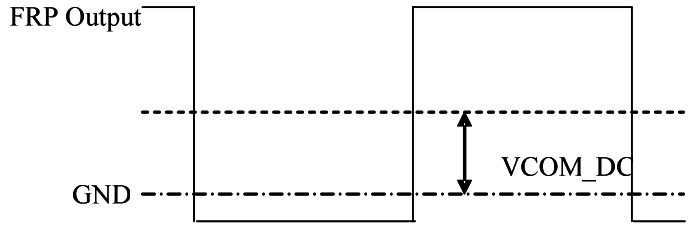
	CbCr(R12[4])='0'								CbCr(R12[4])='1'							
Y_CbCr='0' (Default)	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3	Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3
Y_CbCr='1'	Y0	Cb0	Y1	Cr0	Y2	Cb2	Y3	Cr2	Y0	Cr0	Y1	Cb0	Y2	Cr2	Y3	Cb2

R1:

No	Register address								MSB		Register data					LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R1	0	0	0	0	0	0	0	1	VCDC(1)	x	VCOM_DC(1Eh)					

VCOM_DC: Common voltage DC level selection (20mV/step)

VCOM_DC	VCOM DC level(V)
D5~D0	Low Voltage LC
00h	0.24
:	:
1Eh(Default)	0.84(Default)
:	:
3Fh	1.5



VCDCE: VCOM DC enable setting

VCDCE	Description
0	VCOM_DC function disable. The COMDC pin is Hi-Z.
1(Default)	VCOM_DC function enable. The COMDC pin voltage follows VCOM_DC setting.

R3:

No.	Register address								MSB		Register data					LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R3	0	0	0	0	0	0	1	1	Brightness(40h)							

BRIGHTNESS: RGB bright level setting, setting accuracy: 1 step / bit

D7 ~ D0	Brightness gain
00h	Dark(-64)
40h(Default)	Center (0) (Default)
FFh	Bright (+191)

R4:

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R4	0	0	0	0	0	1	0	0	Narrow(0)	YUV(0)	SEL(00)		NTSC/PAL(10)		VDIR(1)	HDIR(1)

HDIR: Horizontal shift direction setting

HDIR	Function
0	Shift from right to left, Last data = Y1←Y2…Y639←Y640 = First data
1(Default)	Shift from left to right, First data = Y1→Y2…Y639→Y640 = Last data (Default)

VDIR: Vertical shift direction setting

VDIR	Function
0	Shift from down to up, Last line = L1←L2…L239←L240 = First line U2D = 0, D2U = 1
1(Default)	Shift from up to down, First line = L1→L2…L239→L240 = Last line (Default) U2D = 1, D2U = 0

NTSC/PAL: NTSC or PAL input mode selection

NTSC/PAL		Mode
D3	D2	
0	0	PAL
0	1	NTSC
1	x	Auto detection (Default)

SEL: Input data timing format selection

CCIR601	YUV	SEL		INPUT TIMING FORMAT
		D5	D4	
0	0	0	0	UPS051(Default)
0	0	0	1	UPS052 320 × 240
0	0	1	x	UPS052 360 × 240
0	1	1	0	CCIR656
1	1	0	x	YUV 640(*)
1	1	1	0	YUV 720(*)

(*)Please refer to YUV640/YUV720 horizontal timing spec for detailed description.

YUV: YUV(CCIR656, YUV640, YUV720) or RGB input selection

YUV	Function
0(Default)	RGB input (Default)
1	CCIR656 / YUV640 / YUV720 input.

When this command is sent to ASIC,it will be executed immediately

Narrow: This setting is for WIDE scale panel to switch display mode between Normal display and Narrow display.

Narrow	Function
0(Default)	Normal display (Default)
1	Narrow Display

Narrow=0

Narrow=1

R5:

No	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R5	0	0	0	0	0	1	0	1	DRV_FREQ(0)	GRB(1)	x	PFM_DUTY(10)		SHDB2(1)	SHDB1(1)	STB(0)

STB: Standby (Power saving) mode setting

STB	Function
0(Default)	Standby; timing control, DAC, and DC/DC converter are off, and register data should be kept (Default)
1	Normal operation, with power on/off sequence

Note: In standby mode, Source Driver output =0V, VGH =0V, VGL =0V, FRP =0V.

SHDB1: Shut down for back light power converter

SHDB1	Function
0	The back light power converter is off
1(Default)	The back light power converter is controlled by STB's power on/off sequence (Default)

SHDB2: Shut down for VGH/VGL charge pump

SHDB2	Function
0	VGH/VGL charge pump is always off
1(Default)	VGH/VGL charge pump is controlled by STB's power on/off sequence (Default)

PFM_DUTY: PFM duty cycle selection for back light power converter

PFM_DUTY		Function	UPS051 (640)
D4	D3	PFM duty cycle	(dclk/dclk)
0	0	50%	16/32
0	1	60%	19/32
1	0	65%(Default)	21/32
1	1	70%	22/32

GRB: Register reset setting

GRB	Function
0	Reset all registers to default value
1(Default)	Normal operation (Default)

When this command is sent to ASIC,it will be executed immediately

DRV_FREQ: DRV signal frequency setting

DRV_FREQ	UPS051	UPS052
0(Default)	DCLK / 32	DCLK / 64
1	DCLK / 32 / 2	DCLK / 64 / 2

R6:

No	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R6	0	0	0	0	0	1	1	0	HBLK_EN(0)	LED_Current(00)		VBLK(15h)				

VBLK: Vertical blanking setting

UPS051 & UPS052 NTSC mode

D4 ~ D0	VBLK	Unit
00h	0	H
15h	21(Default)	
1Fh	31	

CCIR656 NTSC mode

D4 ~ D0	VBLK	Unit
00h	0	H
16h	22(Default)	
1Fh	31	

UPS052 CCIR656 PAL mode(Vertical blanking + 3)

D4 ~ D0	VBLK	Unit
00h	3	H
15h	24(Default)	
1Fh	34	

Note:

- In UPS051 & UPS052 NTSC, set the typical value VBLK=15h, actually V_blanking=VBLK lines (21 lines)
- In CCIR656 NTSC mode, set the typical value VBLK=16h , actually V_blanking = VBLK lines (22 lines)
- In UPS052 CCIR656 PAL mode, set the typical value VBLK=15h , actually V_blanking = VBLK+3 lines (24 lines)

LED_CURRENT: adjust LED current

DC-DC feedback voltage

D6	D5	Feedback Threshold voltage
0	0	0.6V(20mA)
0	1	0.75V(25mA)
1	0	0.45V(15mA)
1	1	0.3V(10mA)

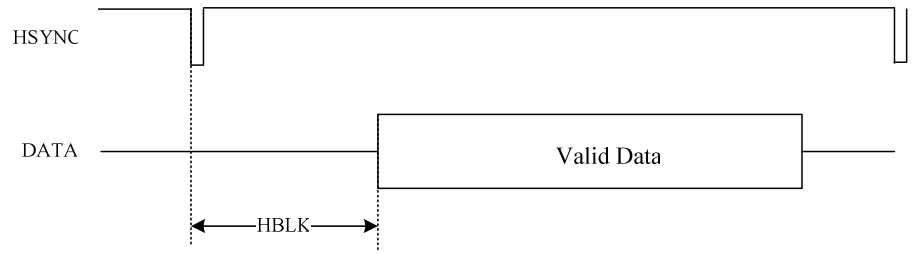
R6 & R7:

No	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R6	0	0	0	0	0	1	1	0	HBLK_EN(0)	LED_Current(00)		VBLK(15h)				
R7	0	0	0	0	0	1	1	1	HBLK(1Eh)							

HBLK_EN & HBLK: Horizontal blanking setting

HBLK_EN	HBLK(D7~D0)	HBLK	Unit	Remark
x	00h	0	DCLK(*)	UPS051
x	1Eh	30(Default)		
x	FFh	255		
x	x	241(Default)	DCLK(*)	UPS052
0	xxh	240(fixed)	DCLK(*)	YUV:8-bit input(ParaSeri=1)
1	00h ~ FFh	0 ~ 255	DCLK(*)	

*The frequency of DCLK is different under different input timing.



R8:

No.	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R8	0	0	0	0	1	0	0	0	BL_DRV(00)		x	x	x	x	x	x

BL_DRV: Backlight driving capability setting

D7	D6	BL_DRV capability
0	0	Normal capability(Default)
0	1	2 times the Normal capability
1	0	4 times the Normal capability
1	1	8 times the Normal capability

R12:

No.	Register address								MSB			Register data				LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R12	0	0	0	0	1	1	0	0	PAIR(00)		x	CbCr(0)	x	Vdpol(1)	Hdpol(1)	DCLKpol(0)

DCLKpol: DCLK polarity selection

DCLKpol	Function
0(Default)	Positive polarity (Default)
1	Negative polarity

HDpol: HSYNC polarity selection

HDpol	Function
0	Positive polarity
1(Default)	Negative polarity(Default)

VDpol: VSYNC polarity selection

VDpol	Function
0	Positive polarity
1(Default)	Negative polarity(Default)

CbCr: Cb & Cr exchange position, (Please refer to the table of R0(Y_CbCr) for detail description)

PAIR: Vertical start time setting for Odd/Even frame

UPS051 / UPS052 NTSC / UPS052 PAL(*)

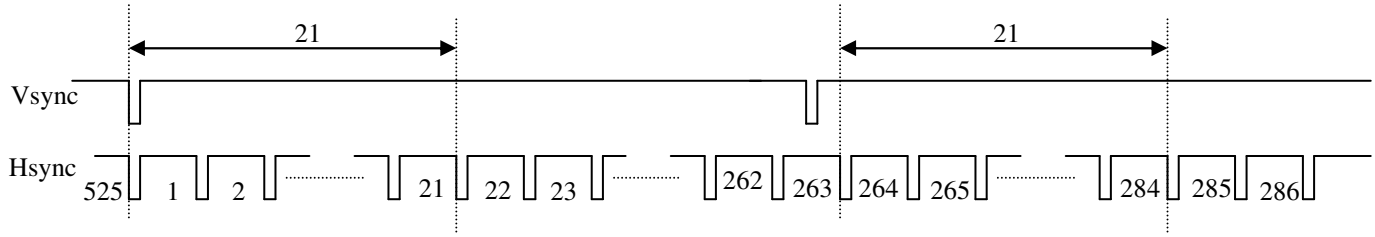
PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
x	0	21/21(Default)	H
x	1	21/20	

CCIR656/YUV640/YUV720 NTSC/PAL(**)

PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
0	0	22/22	H
0	1	22/23	
1	0	23/22	
1	1	23/23	

(*)The typical value of VBLK of UPS052 PAL(24 H) is different than UPS051/UPS052 NTSC(21H).

(**) The typical value of VBLK of CCIR656 PAL(24 H) is different than CCIR656 NTSC(22H).



	PAIR=0		PAIR=1	
Field \ Line	START	END	START	END
ODD	22	261	22	261
EVEN	285	524	284	523

This table is based on VBLK=21.

R13:

No.	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R13	0	0	0	0	1	1	0	1	CONTRAST_B(40h)							

CONTRAST_B: RGB contrast level setting, the gain changes (1/64) / bit

D7 ~ D0	Contrast gain
00h	0
40h(Default)	1(Default)
FFh	3.984

R14~R17:

No.	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R14	0	0	0	0	1	1	0	1	x	SUB-CONTRAST_R(40h)						
R16	0	0	0	1	0	0	0	0	X	SUB-CONTRAST_B(40h)						

SUB-CONTRAST: R/B sub-contrast level setting, the gain changes (1/256) / bit

D6 ~ D0	Brightness gain
00h	0.75
40h(Default)	1(Default)
7Fh	1.246

No.	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R15	0	0	0	0	1	1	1	1	X	SUB-BRIGHTNESS_R(40h)						
R17	0	0	0	1	0	0	0	1	X	SUB-BRIGHTNESS_B(40h)						

SUB-BRIGHTNESS: R/B sub-bright level setting, setting accuracy: 1 step / bit

D6 ~ D0	Brightness gain
00h	Dark(-64)
40h(Default)	Center(0)(Default)
7Fh	Bright(+63)

R21:

No.	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R21	0	0	0	1	0	1	0	1	LED_ON_CYCLE(0111)				LED_ON_RATIO(1111)			

LED_ON_RATIO: Set the active ratio of enable signal, and we can use it to adjust brightness of the LEDs.

LED_ON_RATIO				Value
D3	D2	D1	D0	
0	0	0	0	1/16
0	0	0	1	2/16
0	0	1	0	3/16
0	0	1	1	4/16
0	1	0	0	5/16
0	1	0	1	6/16
0	1	1	0	7/16
0	1	1	1	8/16
1	0	0	0	9/16
1	0	0	1	10/16
1	0	1	0	11/16
1	0	1	1	12/16
1	1	0	0	13/16
1	1	0	1	14/16
1	1	1	0	15/16
1	1	1	1	16/16(Default)

LED_ON_CYCLE : Set the cycle of enable signal , and we can use it to adjust brightness of the LEDs.

LED_ON_CYCLE				Value
D7	D6	D5	D4	
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8(Default)
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

R22:

No.	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R22	0	0	0	1	0	1	1	0	x	x	x	x	x	GAMMA2.2(1)	x	x

GAMMA2.2: Select auto or manual gamma setting

GAMMA2.2	Description
0	Manual set gamma by R23 ~ R26.
1(Default)	Auto set to gamma2.2 by LC type(Default).

R23 ~ R26:

No.	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R23	0	0	0	1	0	1	1	1	x	GMA_V8(x01)			x	GMA_V4(x01)		
R24	0	0	0	1	1	0	0	0	x	GMA_V25(x10)			x	GMA_V16(x10)		
R25	0	0	0	1	1	0	0	1	x	GMA_V48(x10)			x	GMA_V36(x10)		
R26	0	0	0	1	1	0	1	0	x	GMA_V60(x10)			x	GMA_V55(x10)		

		MSB			LSB
	Reg	x00	x01	x10	x11
VCOM=L	V0+	2.5			
	V4+	2.10	2.15	2.20	2.25
	V8+	1.85	1.95	2.00	2.05
	V16+	1.40	1.50	1.60	1.65
	V25+	1.10	1.20	1.30	1.35
	V36+	0.90	1.00	1.05	1.15
	V48+	0.65	0.75	0.80	0.85
	V55+	0.45	0.55	0.65	0.70
	V60+	0.30	0.35	0.45	0.5
	V63+	0.1			

		MSB			LSB
	Reg	x00	x01	x10	x11
VCOM=H	V0-	0.1			
	V4-	0.5	0.45	0.4	0.35
	V8-	0.75	0.65	0.6	0.55
	V16-	1.30	1.10	1.00	0.95
	V25-	1.50	1.40	1.30	1.25
	V36-	1.70	1.60	1.55	1.45
	V48-	1.95	1.85	1.80	1.75
	V55-	2.15	2.05	1.95	1.90
	V60-	2.3	2.25	2.15	2.10
	V63-	2.5			

C. Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time							
Rise	Tr	θ =0°	-	25	50	ms	Note 4
Fall	Tf		-	30	60	ms	
Contrast ratio	CR	At optimized viewing angle	150	300	-		Note 5,6
Viewing angle							
Top		CR≧10	10	15	-	deg.	Note 7
Bottom			30	35	-		
Left			40	45	-		
Right			40	45	-		
Brightness *	Y_L	θ =0°	200	250	-	cd/m^2	Note 8
White chromaticity	x	θ =0°	(0.26)	(0.31)	(0.36)		
	y	θ =0°	(0.28)	(0.33)	(0.38)		

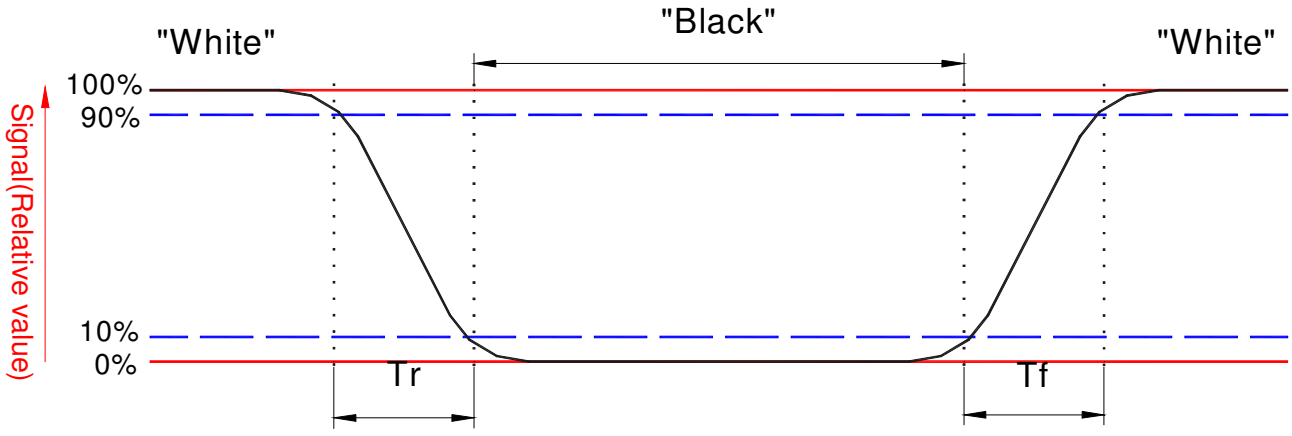
Note 1. Ambient temperature =25℃.

Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed



from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

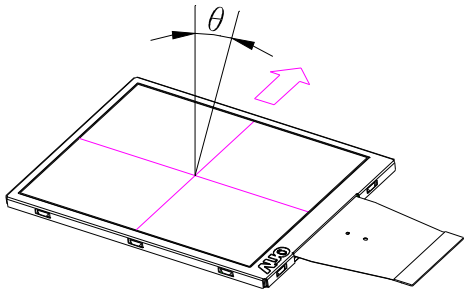
Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

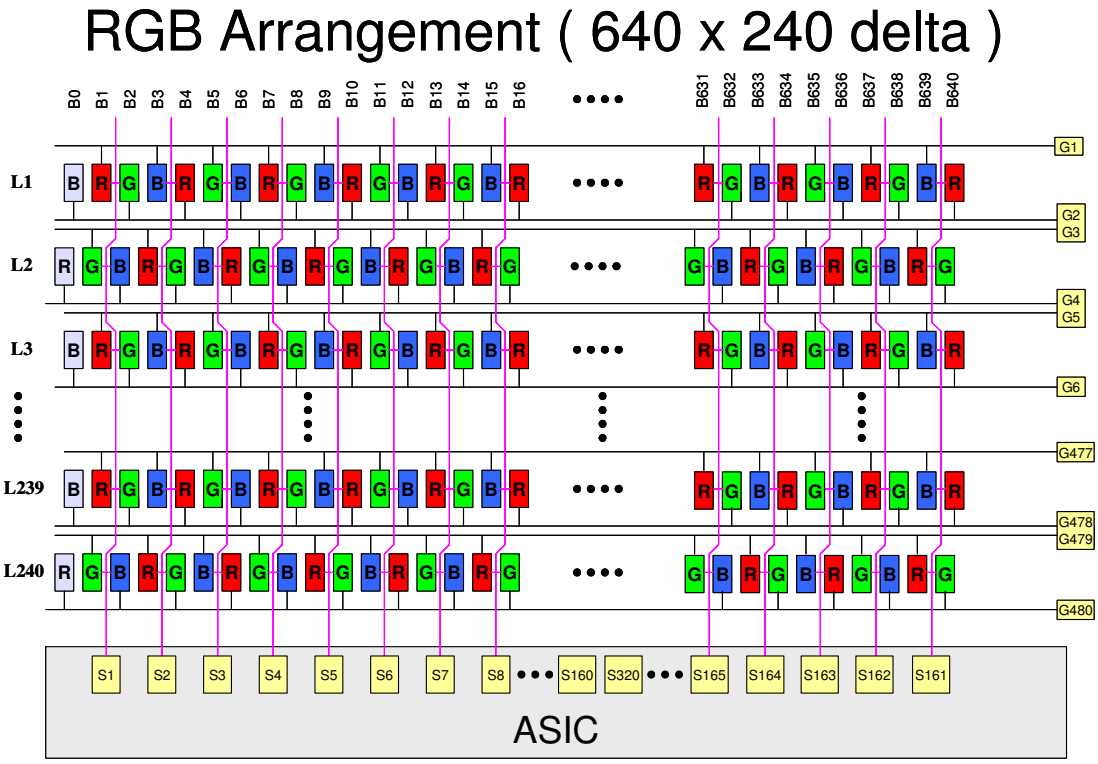
Note 6. White $Vi=V_{i50} \mp 1.5V$
Black $Vi=V_{i50} \pm 2.0V$
“±” Means that the analog input signal swings in phase with COM signal.
“∓” Means that the analog input signal swings out of phase with COM signal.
V_{i50} : The analog input voltage when transmission is 50%
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:
Refer to figure as below.



Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 9. Color Filter Arrangement

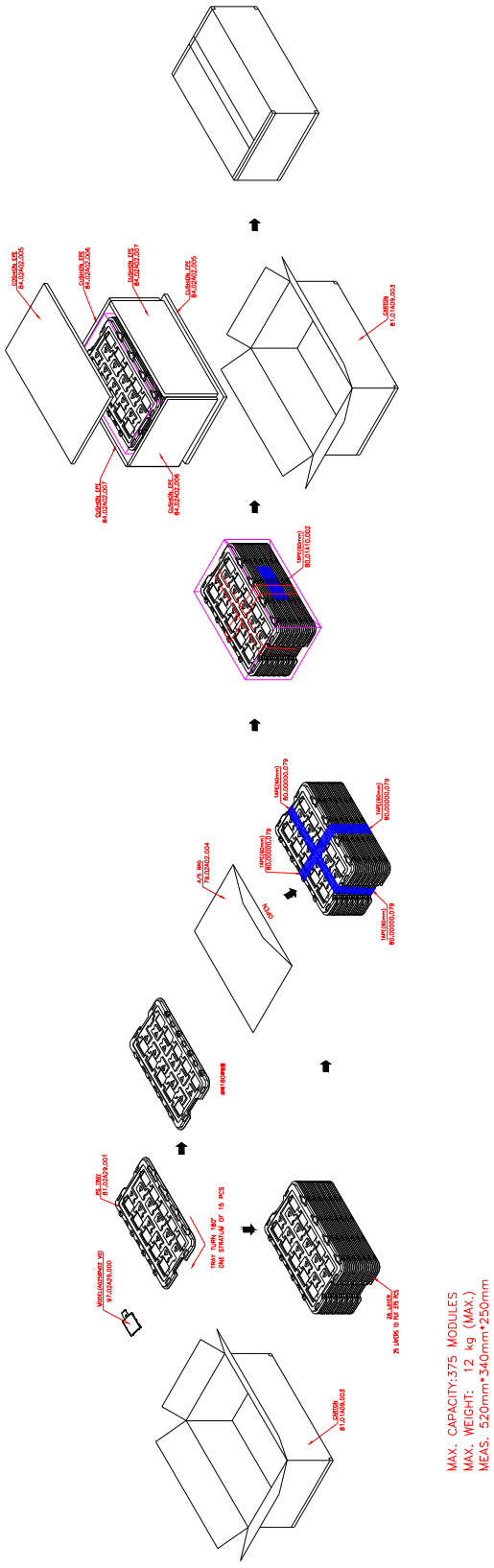


D. Reliability test items

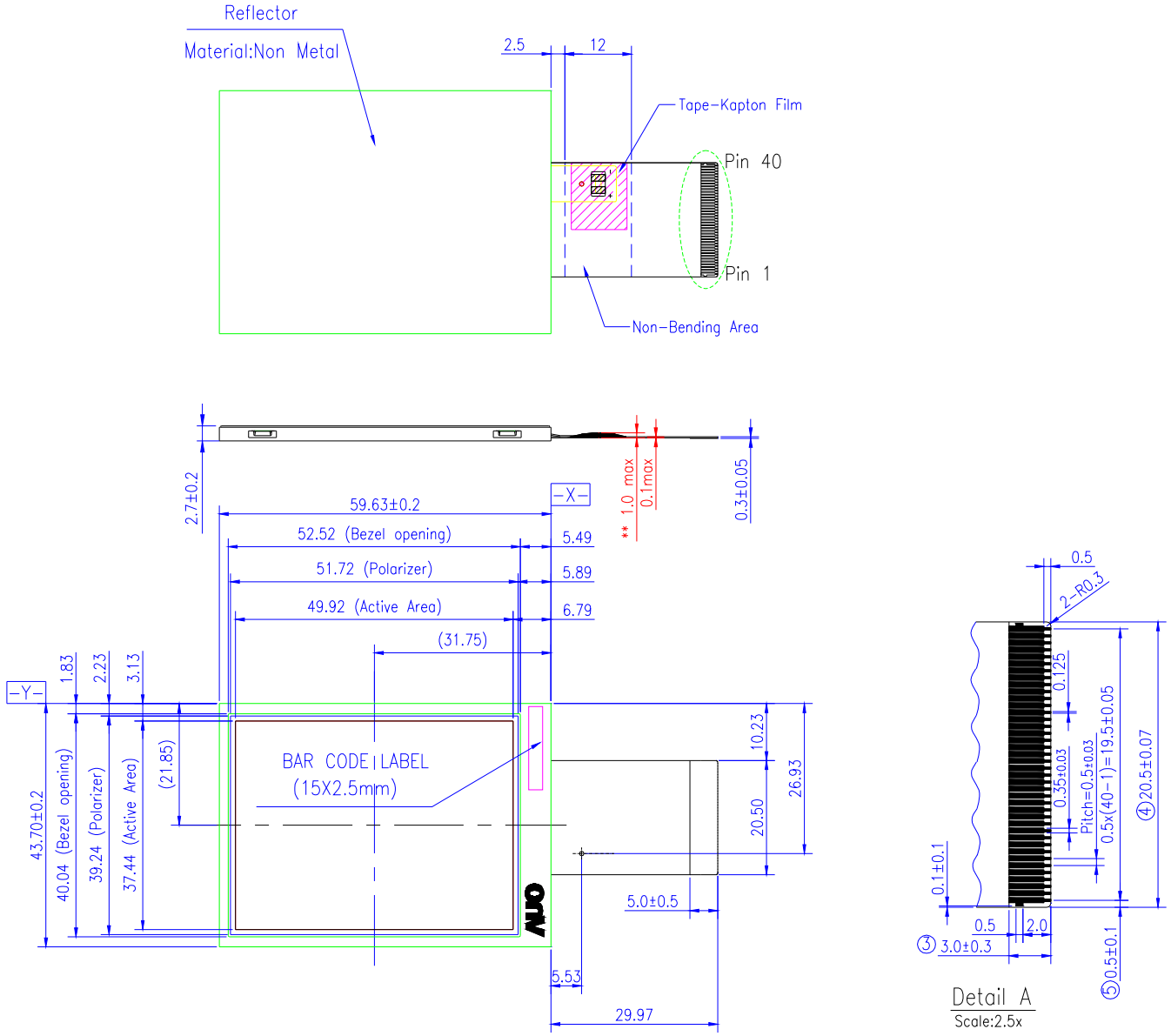
No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80℃ 240Hrs	
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
9	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note: Ta: Ambient temperature.

E. Packing form



F. Outline Dimension

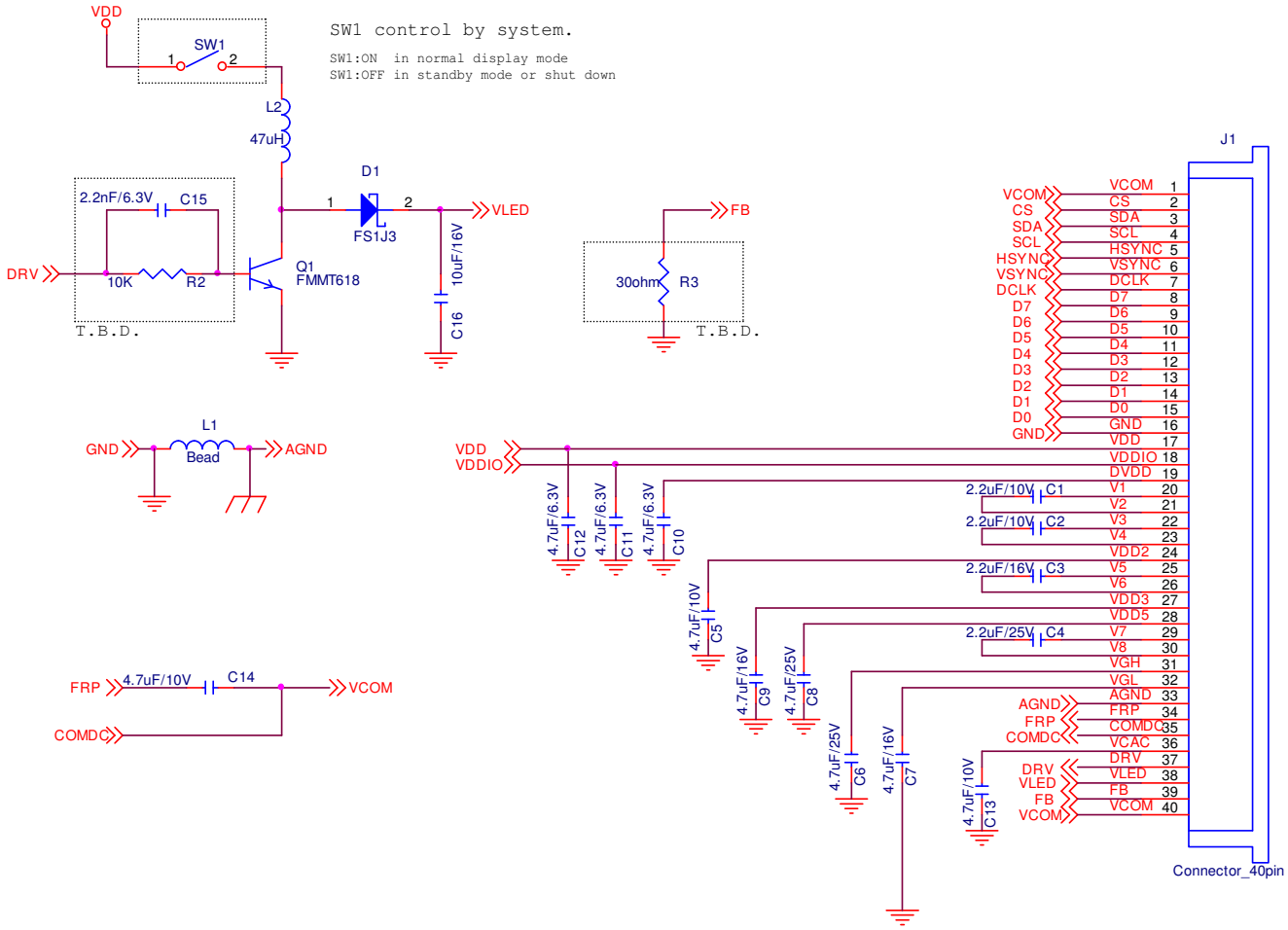


Notes:
1.General tolerance: ± 0.3
2.The bending radius of FPC should be larger than 0.6mm

G. Application note

1. Application circuit

1.1 With internal LED driver circuit

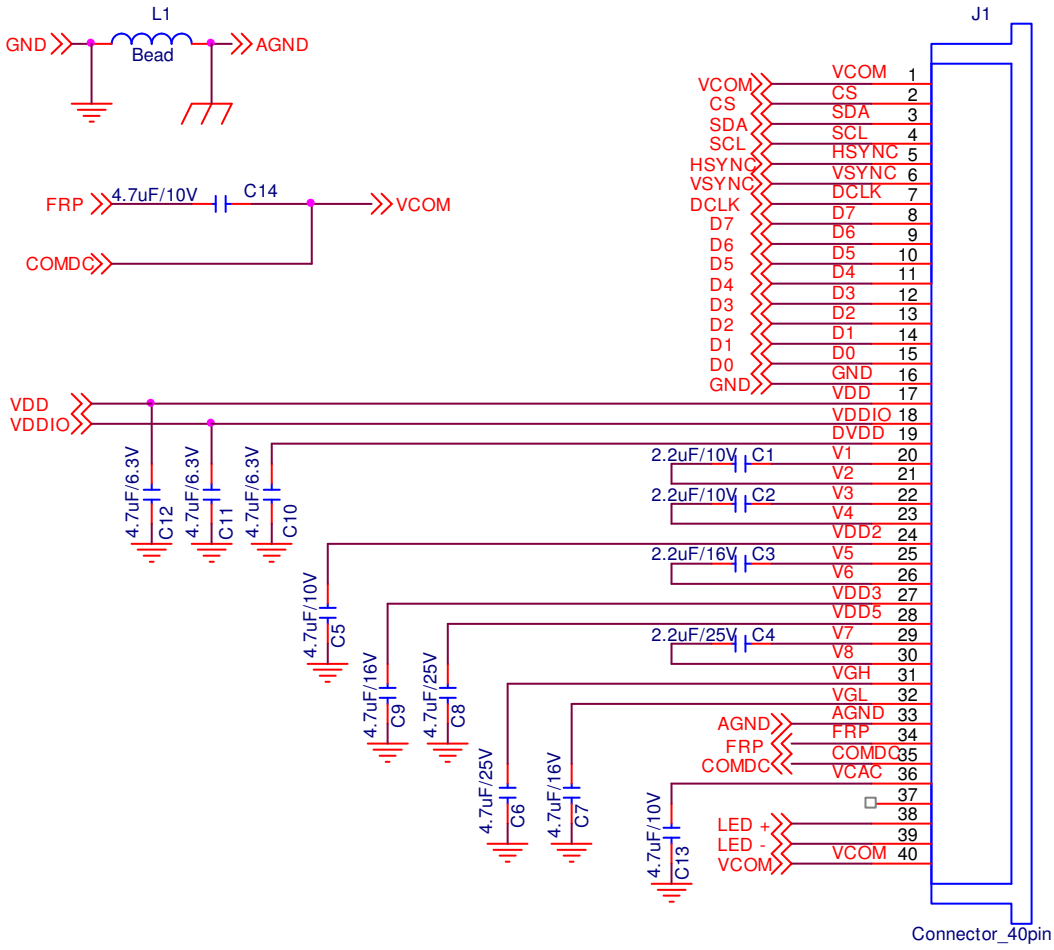


FigG.1 Application circuit with internal LED driver

Note1: Use internal LED driver must set R5[1](SHDB1)= ”1”.

Note2: IF use 3xLED, must set R5[7](DRV_FREQ)=”1” and R5[4:3](PFM_DUTY)=”11”

1.2 With external LED driver circuit



FigG.2 Application circuit with external LED driver

Note3: Use external LED driver must set R5[1](SHDB1)= ”0”.

2. Power on/off sequence

The register setting of standby mode disabling / enabling is used to control the build-in power on / off sequence.

2.1 Power on (Standby Disabling)

After VDD/VDDIO power on reset, VSYNC/HSYNC/DCLK/DATA can be input, and serial control interface is also operational. The LCD driver is in default standby mode after VDD/VDDIO power-on, and setting register STB to '1' to disable the standby mode is required for normal operation. When the standby mode is disabled, a build-in power on sequence is started. The LCD positive and negative power supplies VGH/VGL are pumped first, and followed by the LED power VLED. Please refer to FigG.3 for the detail timing of power on sequence.

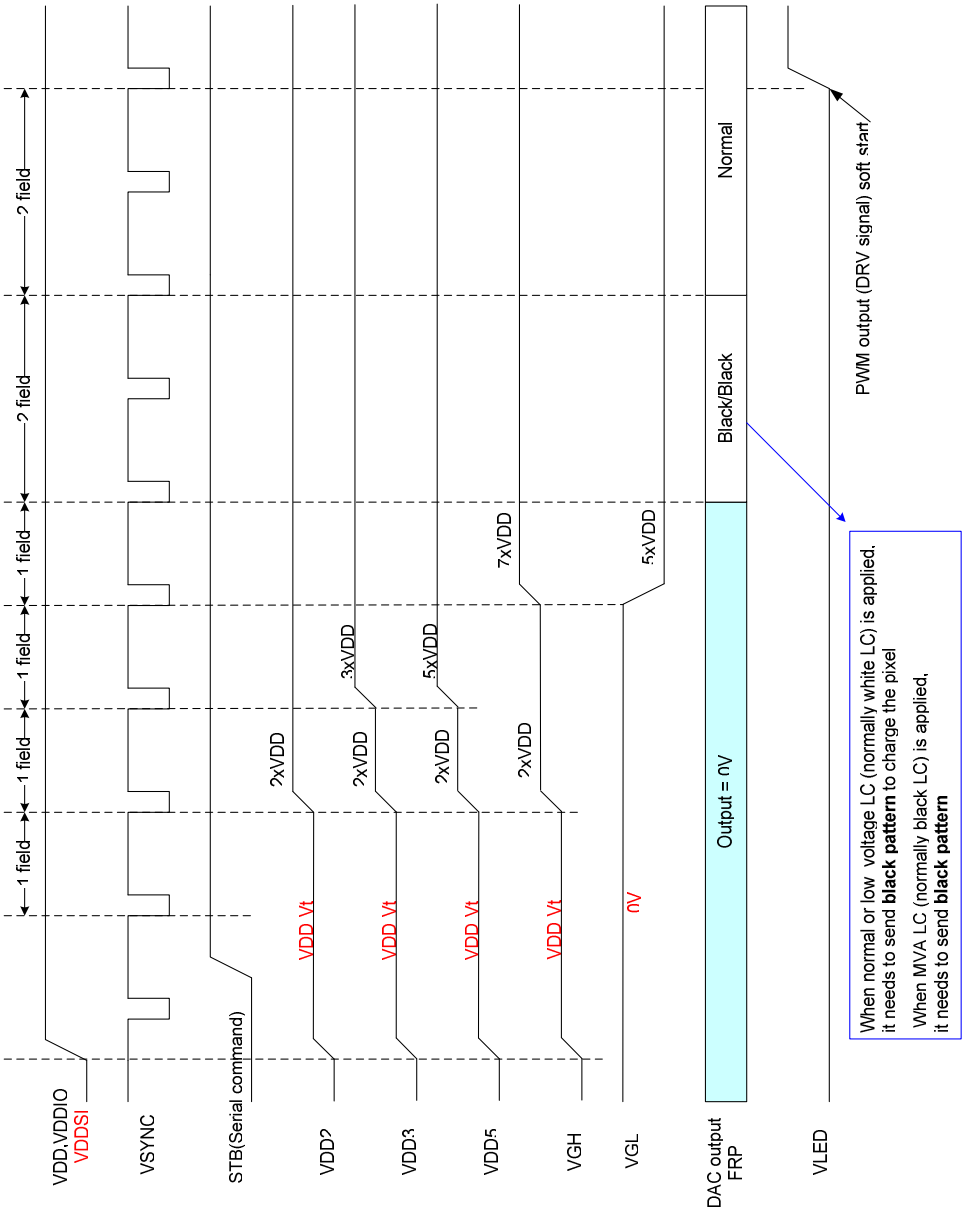


Fig.G.3 Power on sequence

2.2 Power off (Standby Enabling)

When the register STB is set to '0' to enable standby mode, a build-in power off sequence is started. Please refer to FigG.4 for the detail timing of power off sequence.

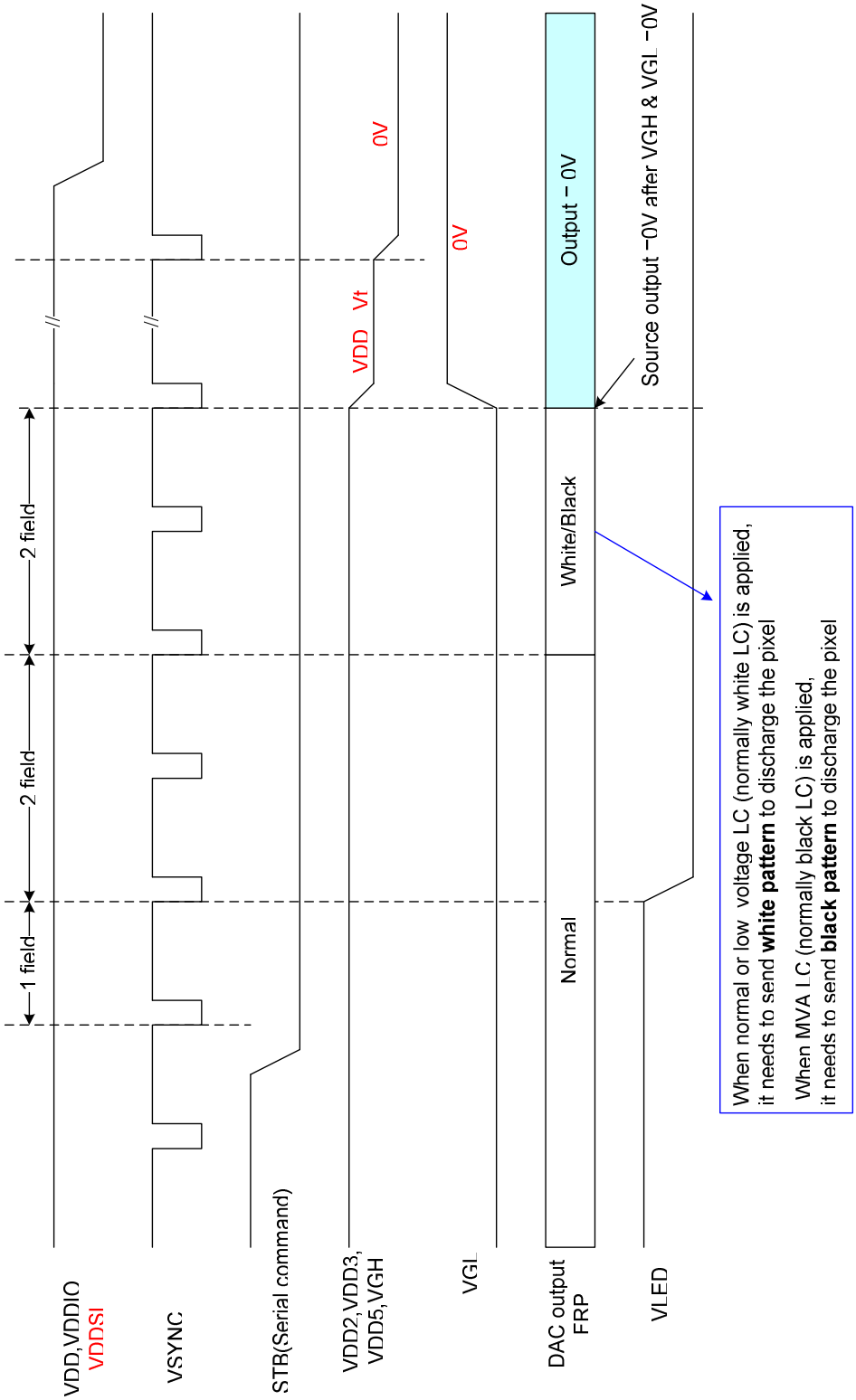
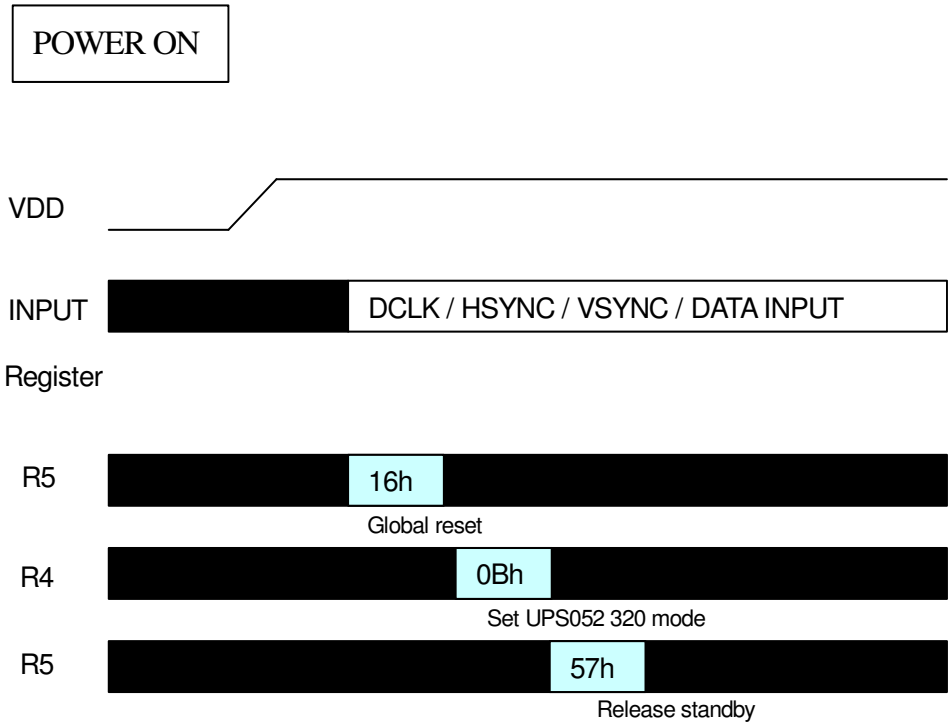
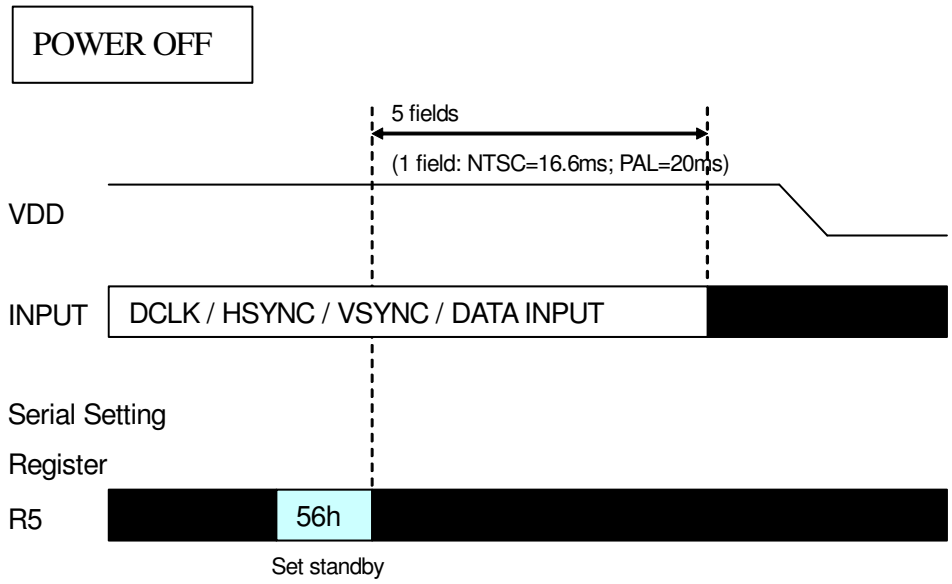


Fig.G.4 Power off sequence

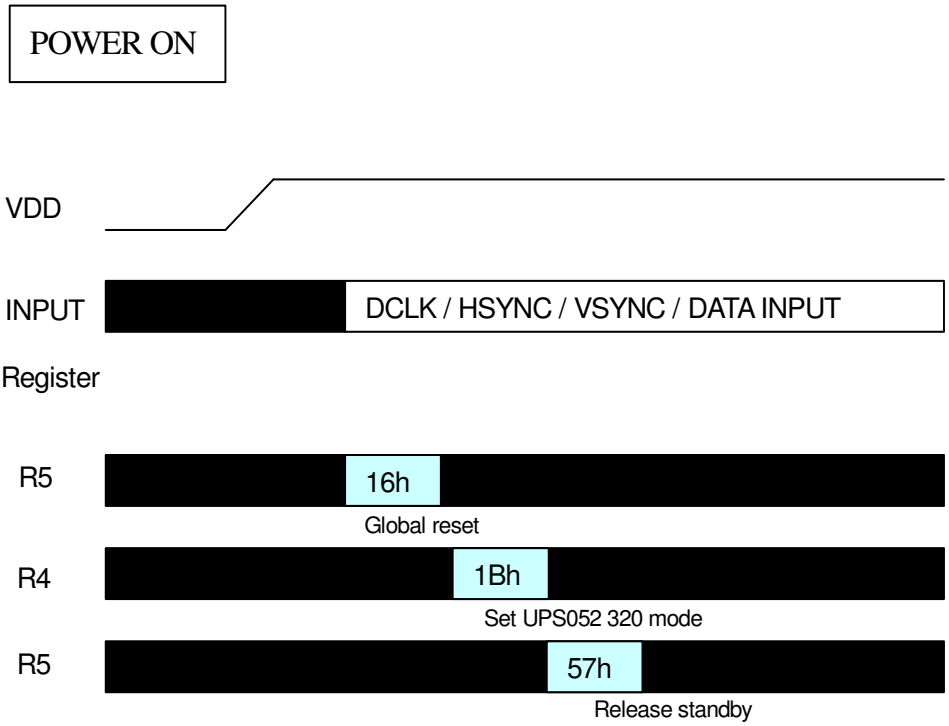
3. Recommended power on/off serial command settings

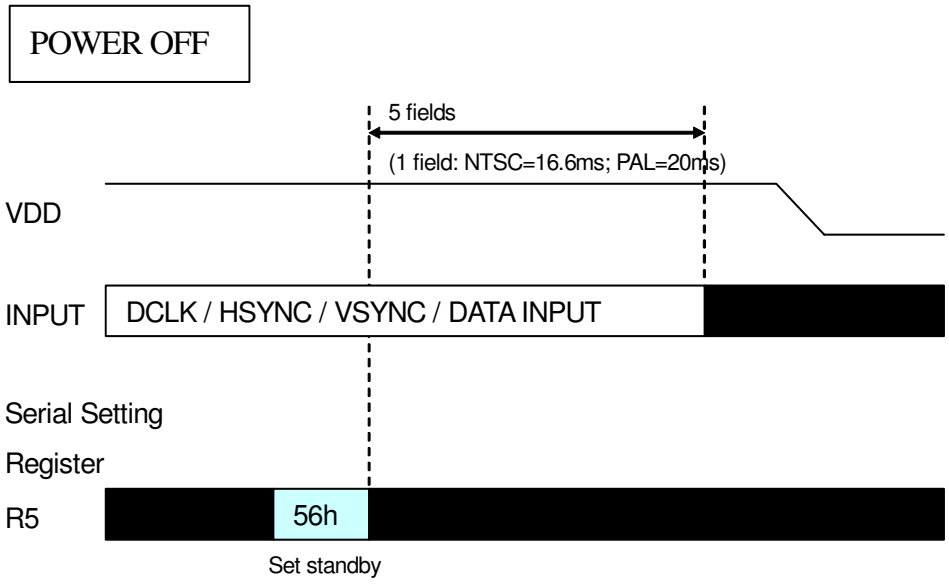
3.1 UPS051



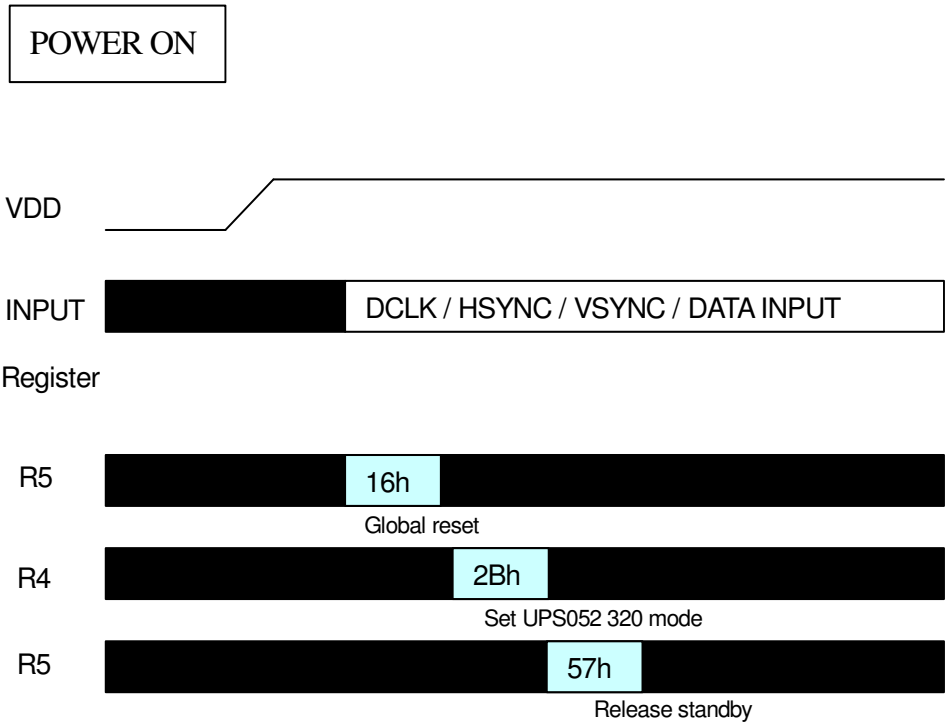


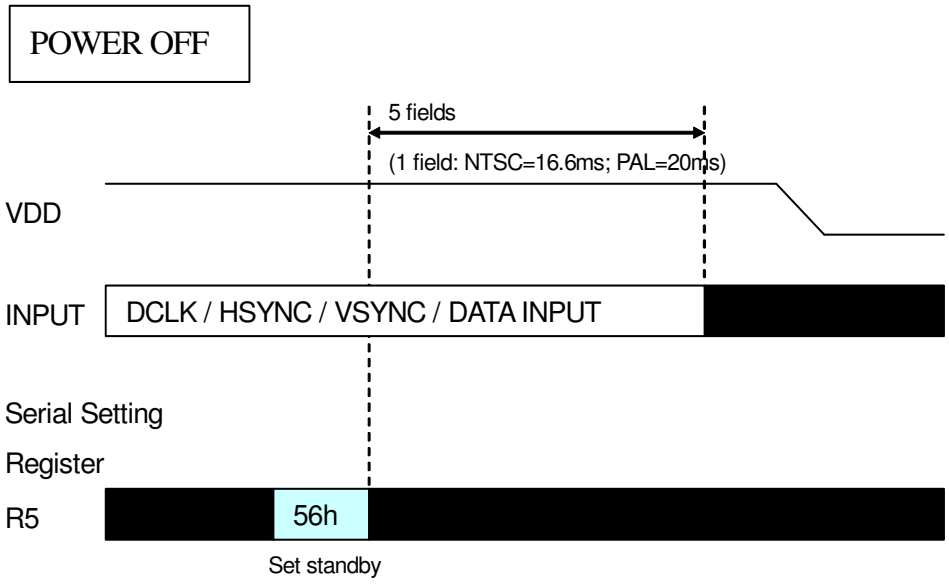
3.2 UPS052 320 mode



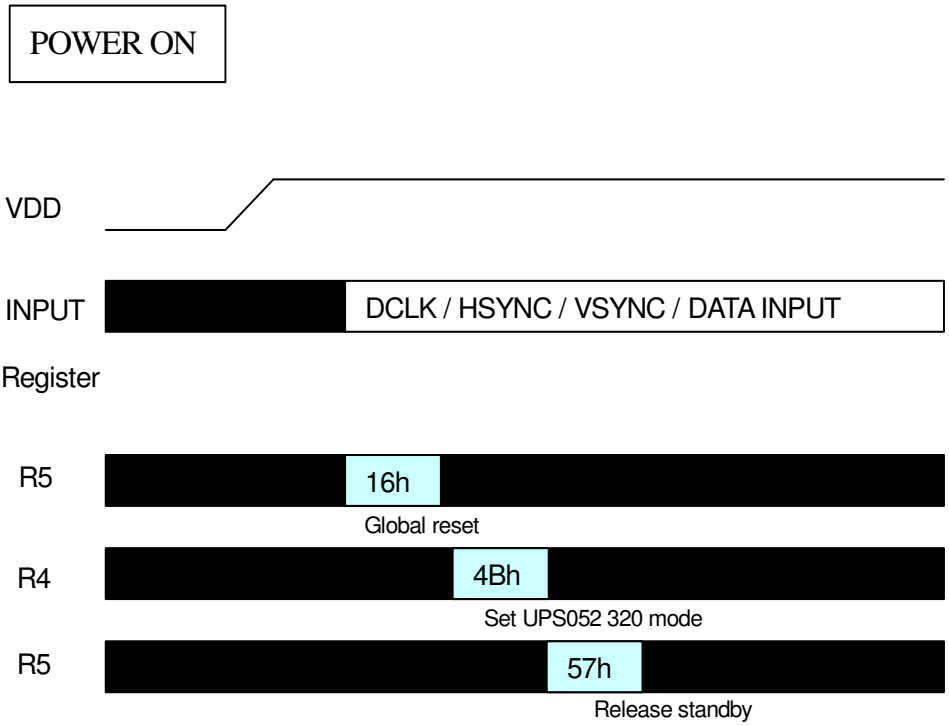


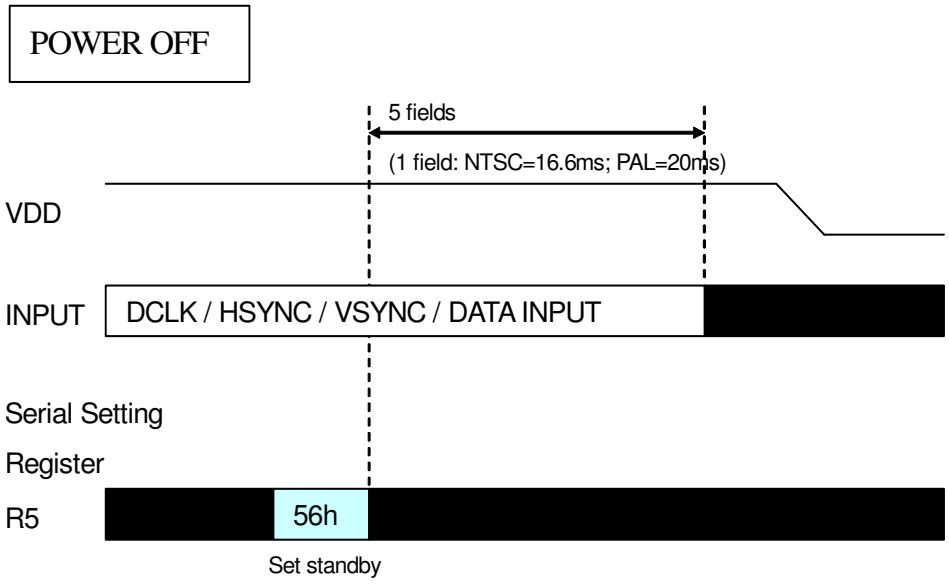
3.3 UPS052 360 mode



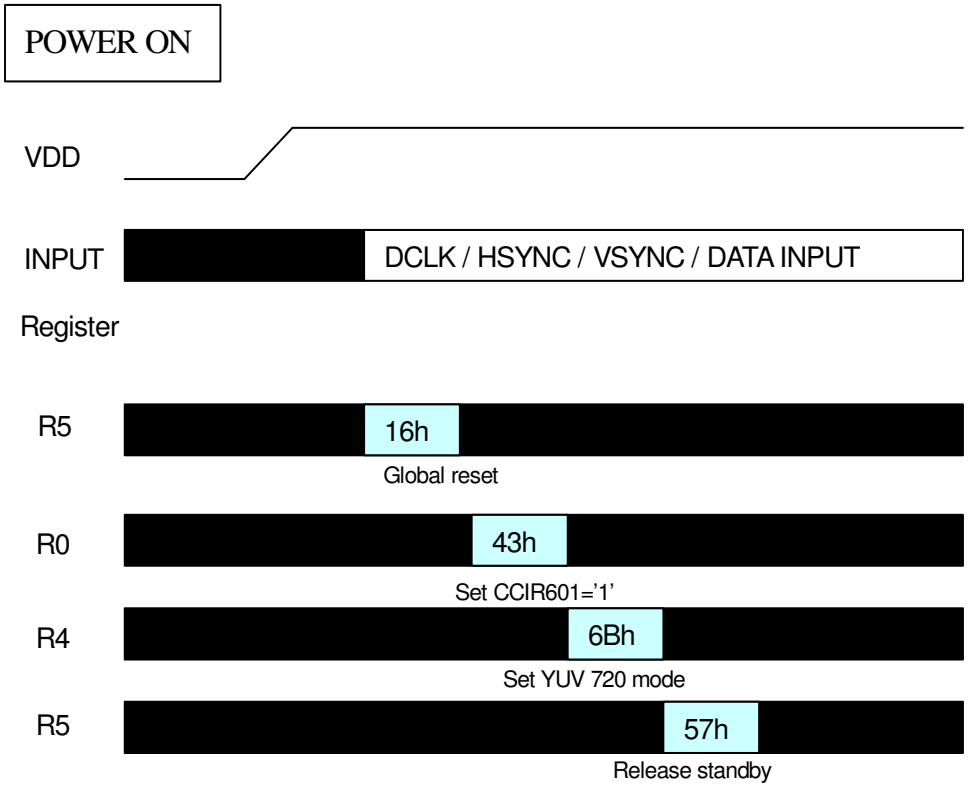


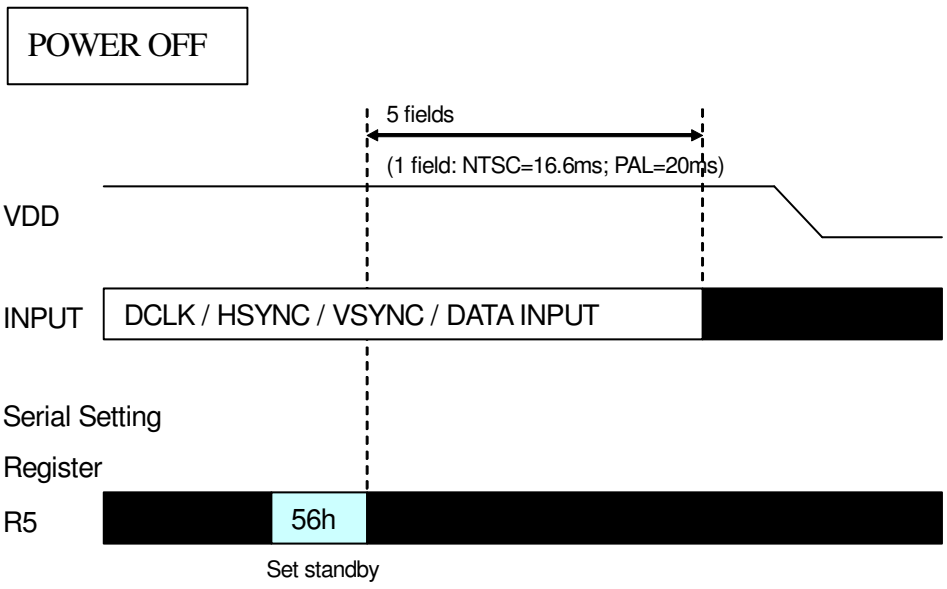
3.4 CCIR656 mode



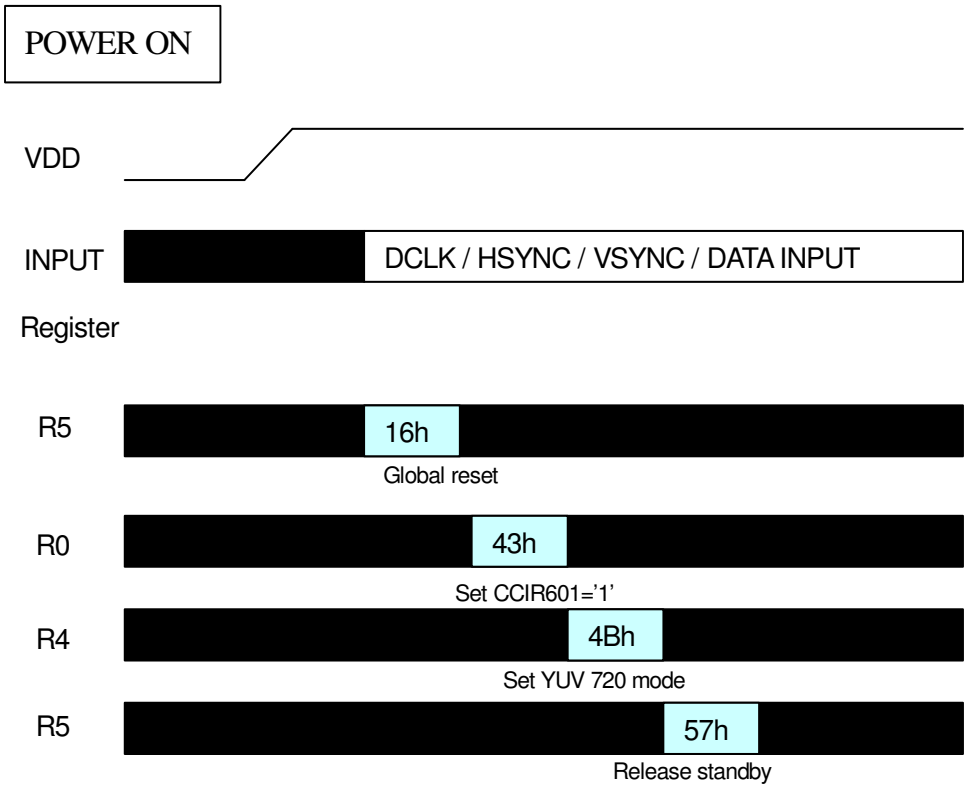


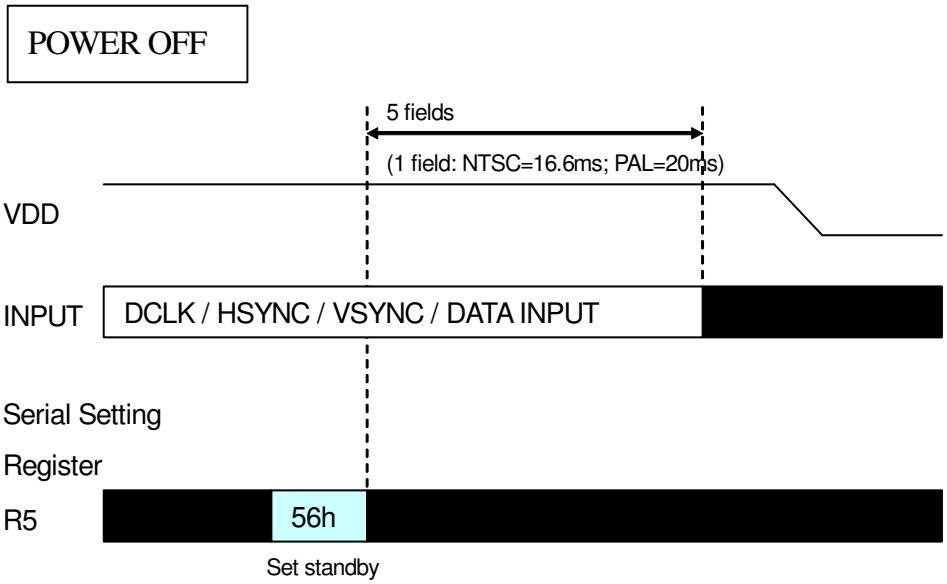
3.5 YUV 720 mode





3.6 YUV 640 mode





4. Power generation circuit

The black diagram of built-in power generation circuit for TFT-LCD supply power is shown as below: