CUSTOMER APPROVAL SHEET

Company Name	
MODEL	A080SN03 V2
CUSTOMER APPROVED	Title : Name :

- ☐ APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)
- ☐ APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.____)
- ☐ APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver.____)
- ☐ CUSTOMER REMARK :

AUO PM :

P/N : _____

Comment :

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Date :	2011/08/24

Product Specification

8" COLOR TFT-LCD MODULE

Model Name： **A080SN03 V2**

Planned Lifetime:	From 2010/May To 2012/Jun
Phase-out Control:	From 2012/Jan To 2012/Jun
EOL Schedule:	2012/Jun

< ◆ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2010/04/07	All	First Draft.
0.1	2010/5/12	P9	Add DC Charateristics
		P10	Modify Gamma Resistor R83 to 1.05Kohm
		P12~P17	Add Input timing remark for Max. value and PWCK setting.
		P23	Modify Application Circuit U4 to U3
0.2	2010/6/22	P10	Update Gamma voltage suggested circuit.
0.3	2011/5/25	P4	Update HPS TFT-LCD module 2D drawing
0.4	2011/8/24	P.0	Change the product lifetime and EOL schedule

Contents

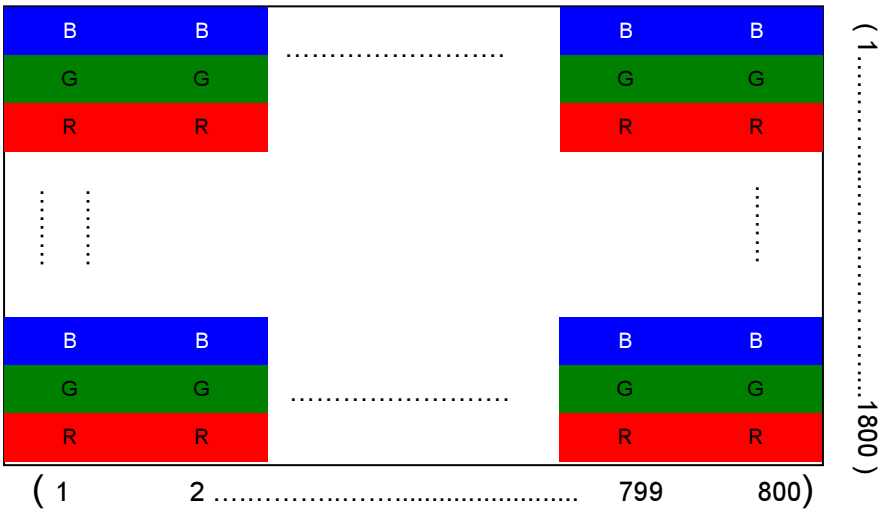
A. General Information

This product is for portable DVD and digital photo frame application.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	8(Diagonal)	
2	Display Resolution	dot	800(W)x600RGB(H)	
3	Overall Dimension	mm	170.1(W)x132.3(H)x1.43(D)	Note 1
4	Active Area	mm	162(W)x121.5(H)	
5	Pixel Pitch	mm	0.2025(W)x0.2025(H)	
6	Color Configuration	--	Tri-Gate	Note 2
7	Color Depth	--	16.2M Colors	Note 3
8	NTSC Ratio	%	50	
9	Display Mode	--	Normally White	
10	Panel surface Treatment	--	Anti-Glare, 3H	
11	Weight	g	68 ±10	
12	Panel Power Consumption	mW	189	Note 4
13	Backlight Power Consumption	W	xx	
14	Viewing direction		6 o'clock (gray inversion)	

Note 1: Not include blacklight cable and FPC. Refer next page to get further information.

Note 2: Below figure shows dot stripe arrangement.

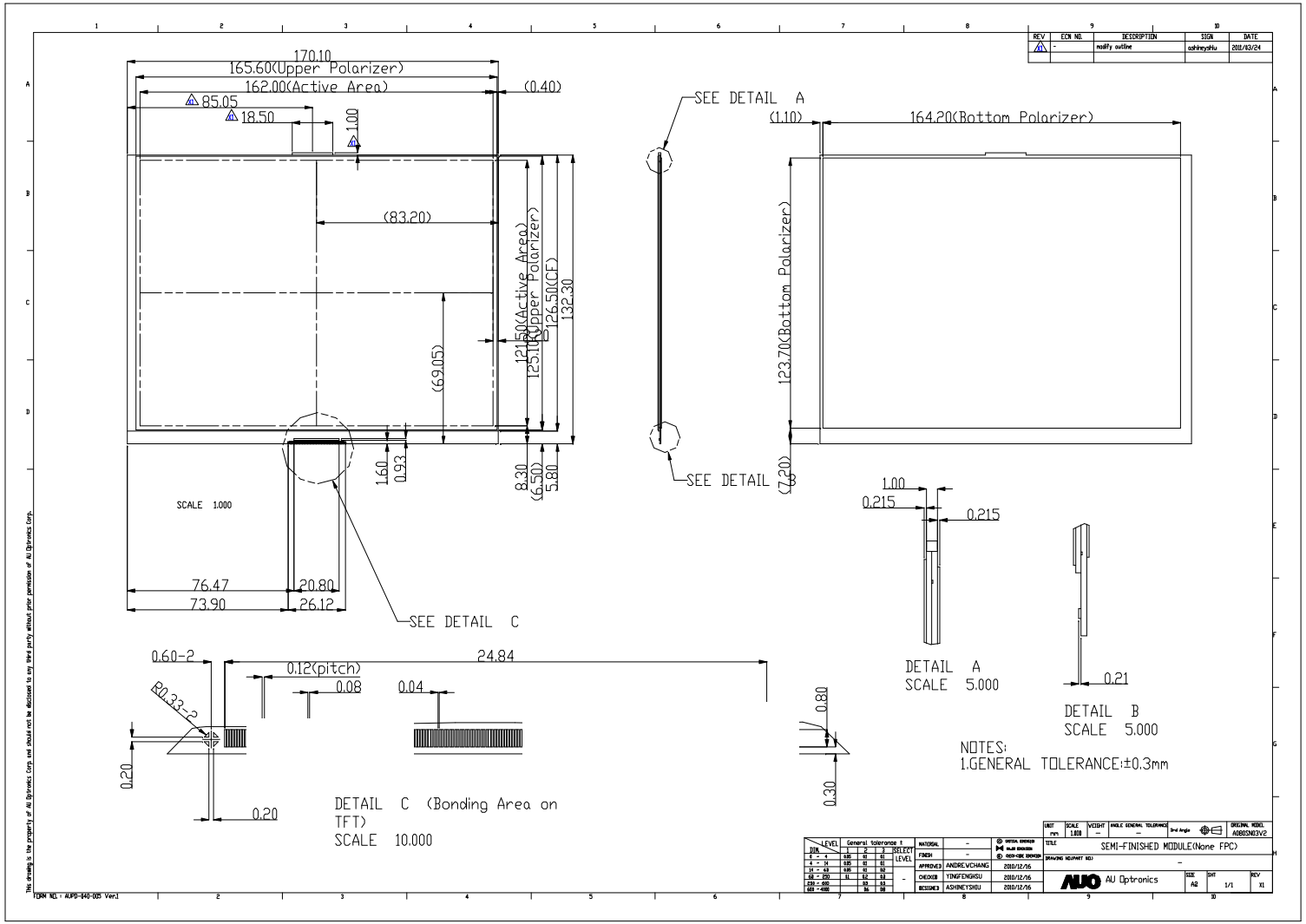


Note 3: The full color display depends on 24-bit data signal (pin 33~40, 42~49, 51~58).

Note 4: Please refer to Electrical Characteristics chapter.

B. Outline Dimension

1. TFT-LCD Module



C. Electrical Specifications

1. TFT LCD Panel Pin Assignment

Recommended connector : XF2M-6015-1AH

NO.	Symbol	I/O	Description	Remark
1	VCOM	I	Common electrode driving voltage	
2	VGL	P	Negative power supply voltage for Gate driver	
3	VGH	P	Positive power supply voltage for Gate driver	
4	VGH	P	Positive power supply voltage for Gate driver	
5	VDPA	P	Positive power supply voltage for analog power	
6	VDNA	P	Negative power supply voltage for analog power	
7	GND	P	Ground	
8	DRV_BLU	O	CABC PWM_SIGNAL output via an output buffer	
9	CABC_EN	I	CABC function enable	
10	U/D	I	Up/Down selection.	Note2
11	R/L	I	Left/Right selection	Note2
12	GRB	I	H/W global reset	Note1
13	V10	I	Gamma correction voltage reference	
14	V9	I	Gamma correction voltage reference	
15	V8	I	Gamma correction voltage reference	
16	V7	I	Gamma correction voltage reference	
17	V6	I	Gamma correction voltage reference	
18	V5	I	Gamma correction voltage reference	
19	V4	I	Gamma correction voltage reference	
20	V3	I	Gamma correction voltage reference	
21	V2	I	Gamma correction voltage reference	
22	V1	I	Gamma correction voltage reference	
23	VDDIO	P	Digital interface supply voltage of digital	
24	VDDIO	P	Digital interface supply voltage of digital	
25	CS	I	Chip select (Low active) of SPI	
26	SDA	I/O	Data input/output of SPI	
27	SCL	I	Clock input of SPI	
28	GND	P	Ground	
29	DCLK	I	Data clock input	
30	GND	P	Ground	
31	DE	I	Data enable Input (High active)	
32	GND	P	Ground	
33	DB7	I	Blue data Input (MSB)	
34	DB6	I	Blue data Input	

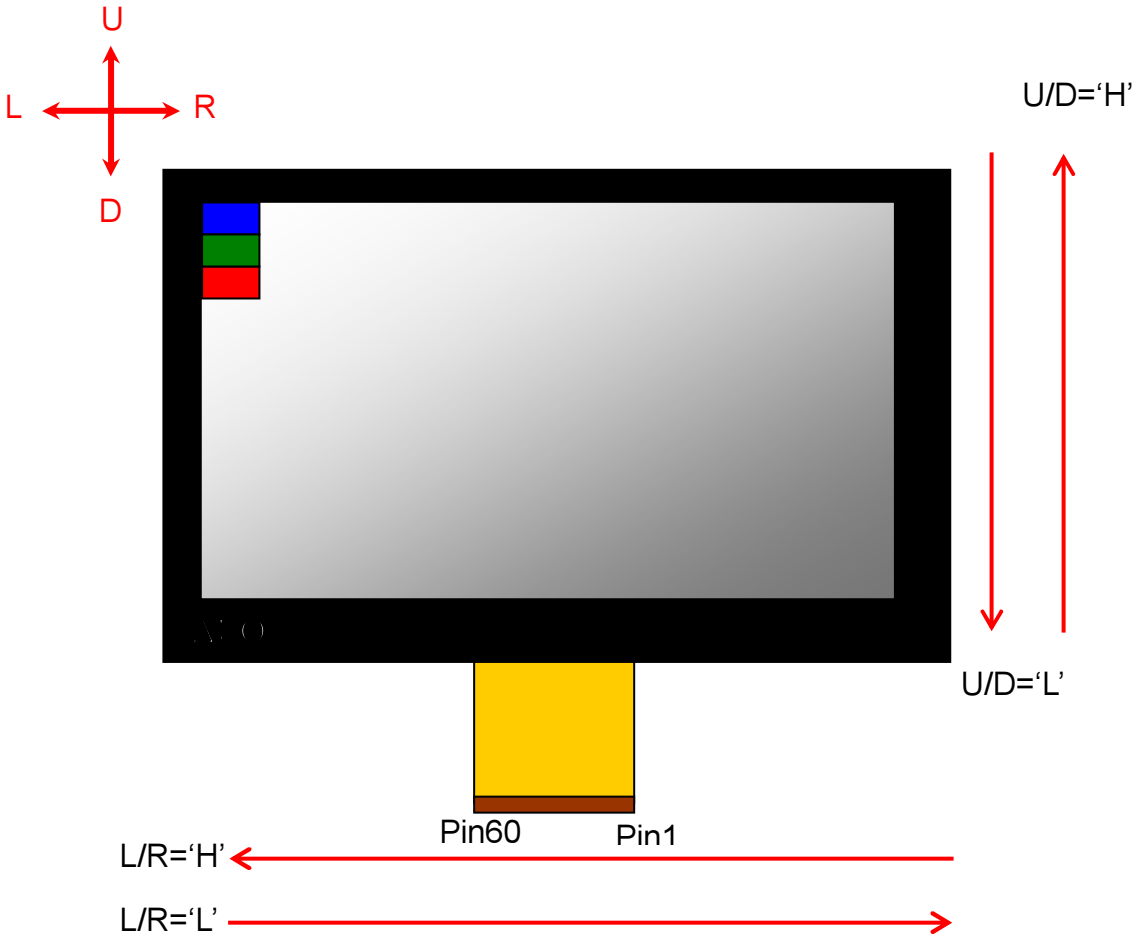
35	DB5	I	Blue data Input	
36	DB4	I	Blue data Input	
37	DB3	I	Blue data Input	
38	DB2	I	Blue data Input	
39	DB1	I	Blue data Input	
40	DB0	I	Blue data Input (LSB)	
41	GND	P	Ground	
42	DG7	I	Green data Input (MSB)	
43	DG6	I	Green data Input	
44	DG5	I	Green data Input	
45	DG4	I	Green data Input	
46	DG3	I	Green data Input	
47	DG2	I	Green data Input	
48	DG1	I	Green data Input	
49	DG0	I	Green data Input (LSB)	
50	GND	P	Ground	
51	DR7	I	Red data Input (MSB)	
52	DR6	I	Red data Input	
53	DR5	I	Red data Input	
54	DR4	I	Red data Input	
55	DR3	I	Red data Input	
56	DR2	I	Red data Input	
57	DR1	I	Red data Input	
58	DR0	I	Red data Input (LSB)	
59	GND	P	Ground	
60	VCOM	I	Common electrode driving voltage	

I: Input; P: Power

Note1: Global reset, normally pulled high. Suggest to connecting with an RC (R=10K ohm, C=1uF)reset circuit for stability. Normally pull high.

Note2:

U/D	Direction	**L/R**	Direction
H	D → U	H	R → L
L	U→ D	L	L → R



2. Backlight Pin Assignment

Recommended connector :

NO.	Symbol	I/O	Description	Remark
1	HI	I	Power supply for backlight unit (High voltage)	
2	GND	-	Ground for backlight unit	

3. Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power Voltage	VDDIO	GND=0	-0.5	5	V	
	VDPA	GND=0	-0.5	5.9	V	
	VDNA	GND=0	-5.9	0.5	V	
	VGH	GND=0	VDPA	--	V	
	VGL	GND=0	--	VDNA	V	
	VGH－VGL		-	32	V	

Input signal voltage	Vi	GND=0	-0.3	VDDIO+0.3	V	Note 1
	VCOM	GND=0	-3.5	0	V	
	V1~V5	GND=0	0	VDPA-0.2	V	
	V6~V10	GND=0	VDNA+0.2	0	V	
Operating temperature	Topa				℃	
Storage temperature	Tstg				℃	

Note 1: DE, Digital Data.

Note 2: Functional operation should be restricted under ambient temperature (25℃).

Note 3: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

4. Electrical DC Characteristics

a. DC Charateristics

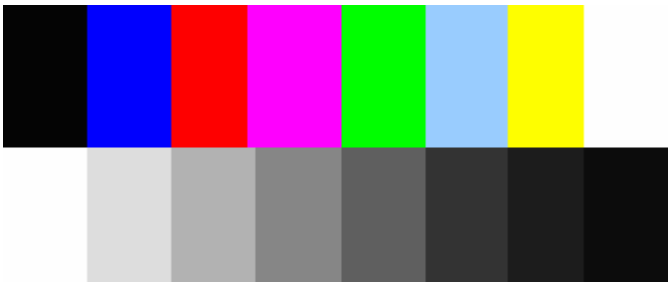
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDDIO	3	3.3	3.6	V	
		VDPA	4.5	5	5.5	V	
		VDNA	-5.5	-5	-4.5	V	
		VGH	12.6	14	15.4	V	
		VGL	-15.4	-14	-12.6	V	
VCOM		Vcdc	-1.6	-1.9	-2.2	V	
Input signal voltage	H Level	Vih	0.7xVDDIO	--	VDDIO	V	Note 1
	L Level	Vil	0	--	0.3xVDDIO	V	
Pull-up/down impedance		Rin	--	800k	--		
Input level of V1~V5		Vx	GND	--	VDPA-0.2	V	Note 2
Input level of V6~V10		Vx	VDNA+0.2	--	GND	V	Note 2

Note 1: DE, Digital Data
Note 2 : VDPA > V1 > V2 > V3 > V4 > V5 > V6 > V7 > V8 > V9 > V10 > VDNA

b. Current Consumption (AGND=GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input current for VDDIO	IVDDIO	VDDIO=3.3V	-	6.45	7	mA	Note 1
Input current forVDPA	IVDPA	VDPA=5V	-	5.58	12.9	mA	Note 1
Input current for VDNA	IVDNA	VDNA=-5V	-	-5.68	-13.4	mA	Note 1
Input current for VGH	IVGH	VGH=14V	-	3.96	5	mA	Note 1
Inpur current for VGL	IVGL	VGL=-14V	-	-4.04	-5	mA	Note 1
Input Leakage Current	Iin	Digital input pins	-	-	±1	uA	Note 2

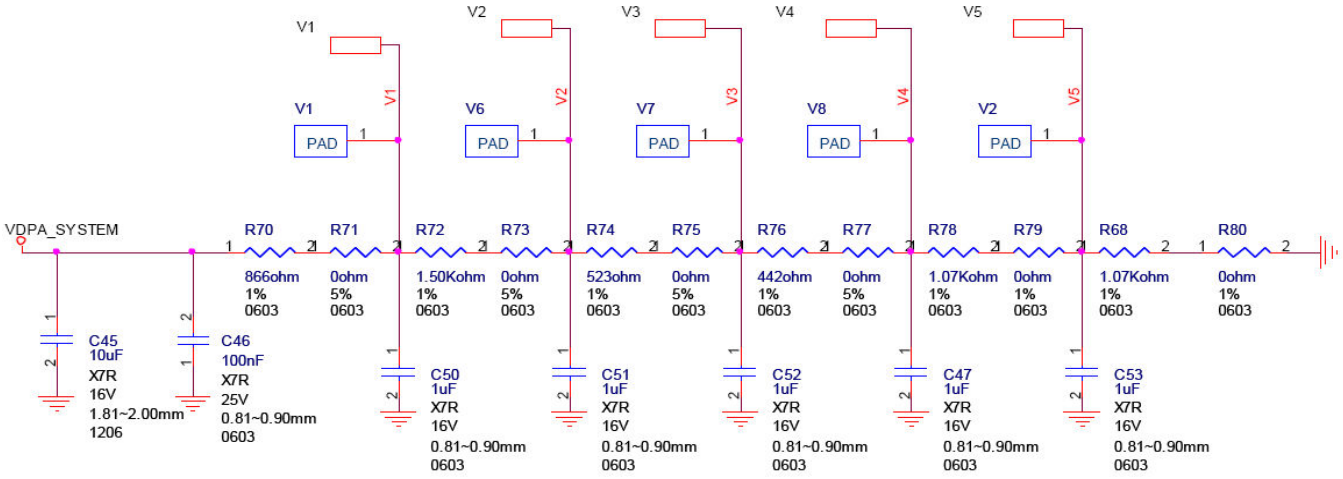
Note 1: The test pattern use the following pattern.



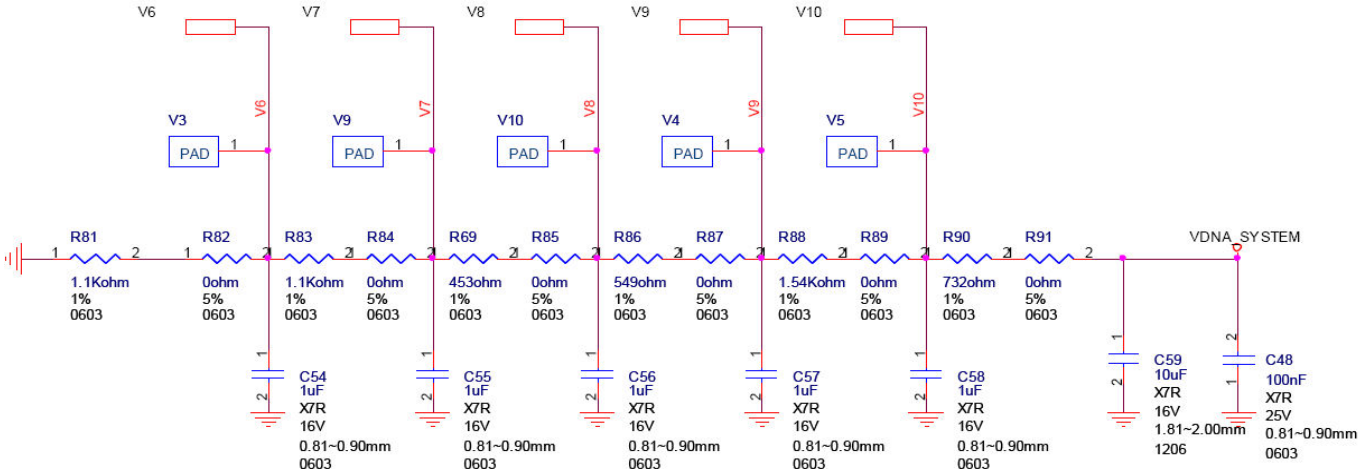
Note 2: except for pull-up, pull-down pins.

c. Gamma voltage suggested circuit is as follows

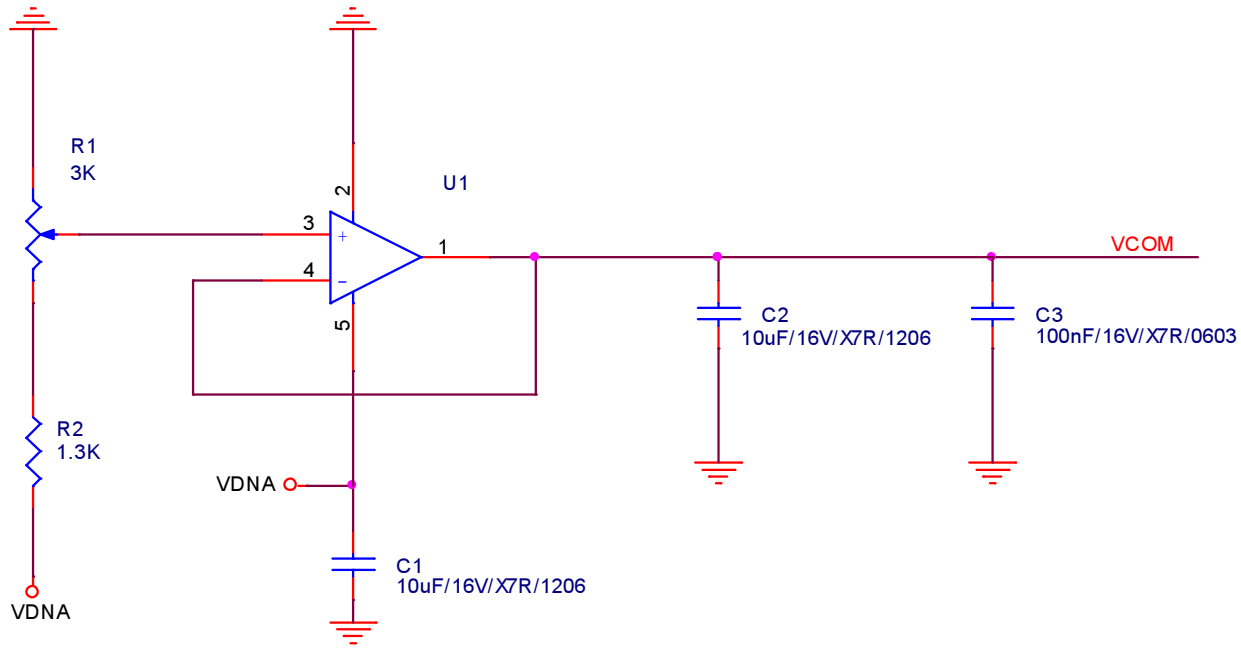
V1	4.277
V2	2.882
V3	2.396
V4	1.985
V5	0.994
V6	-0.998
V7	-1.995
V8	-2.409
V9	-2.908
V10	-4.305



Gamma & Vcom : Generate by VDNA_SYSTEM and VDPA_SYSTEM



d. Vcom buffer suggested circuit is as follows



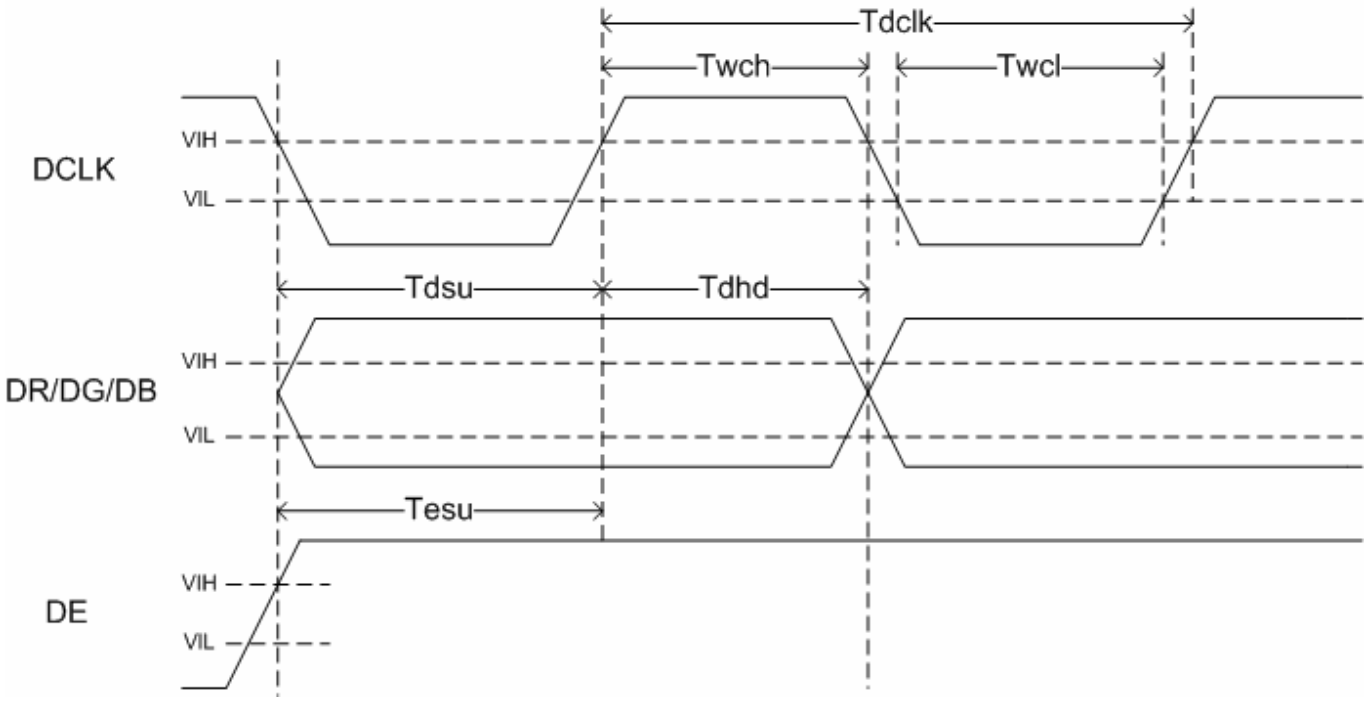
e. Backlight Driving Conditions

This is panel only product without BLU structure.

5. Electrical AC Characteristics

a. Signal AC Characteristics

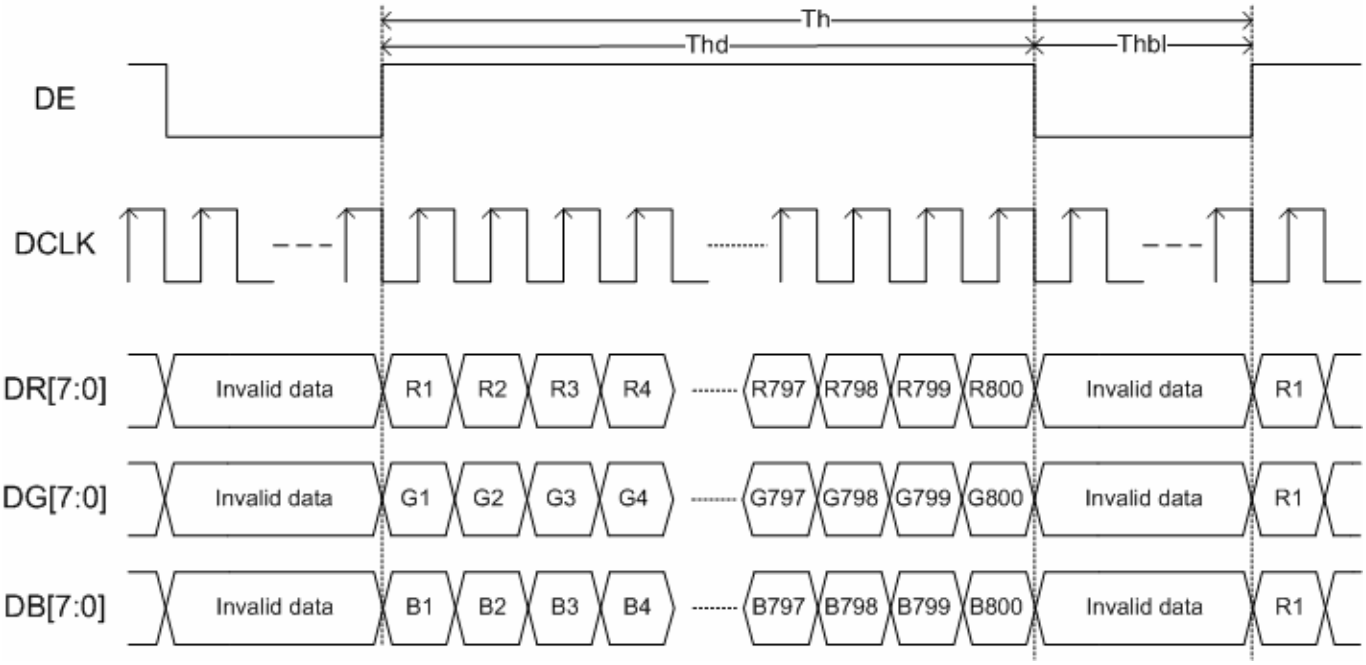
Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Clock High time	Twcl	8	--	--	ns	
Clock Low time	Twch	8	--	--	ns	
Data setup time	Tdsu	5	--	--	ns	
Data hold time	Tdhd	10	--	--	ns	
Data enable set-up time	Tesu	4	--	--	ns	



b. Input Timing Setting

Horizontal timing:

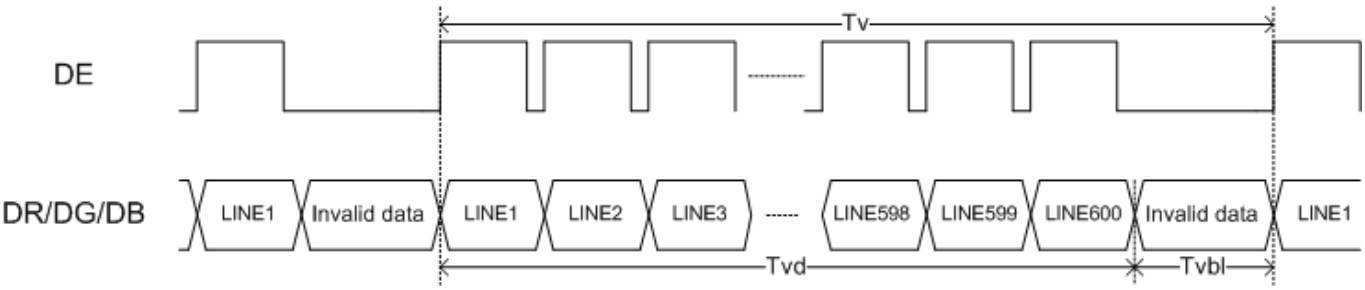
Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency	Fdclk	36.7	40	45.1	MHz	
DCLK period	Tdclk	22	25	27	ns	
Hsync period (= Thd + Thbl)	Th	986	1056	1183	DCLK	Note 1,2
Active Area	Thd	--	800	--	DCLK	
Horizontal blanking	Thbl	186	256	383	DCLK	



Horizontal input timing

Vertical timing:

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Vsync period (= Tvd + Tvbl)	Tv	620	628	635	Th	
Active lines	Tvd	--	600	--	Th	
Vertical blanking	Tvbl	20	28	35	Th	



Vertical timing

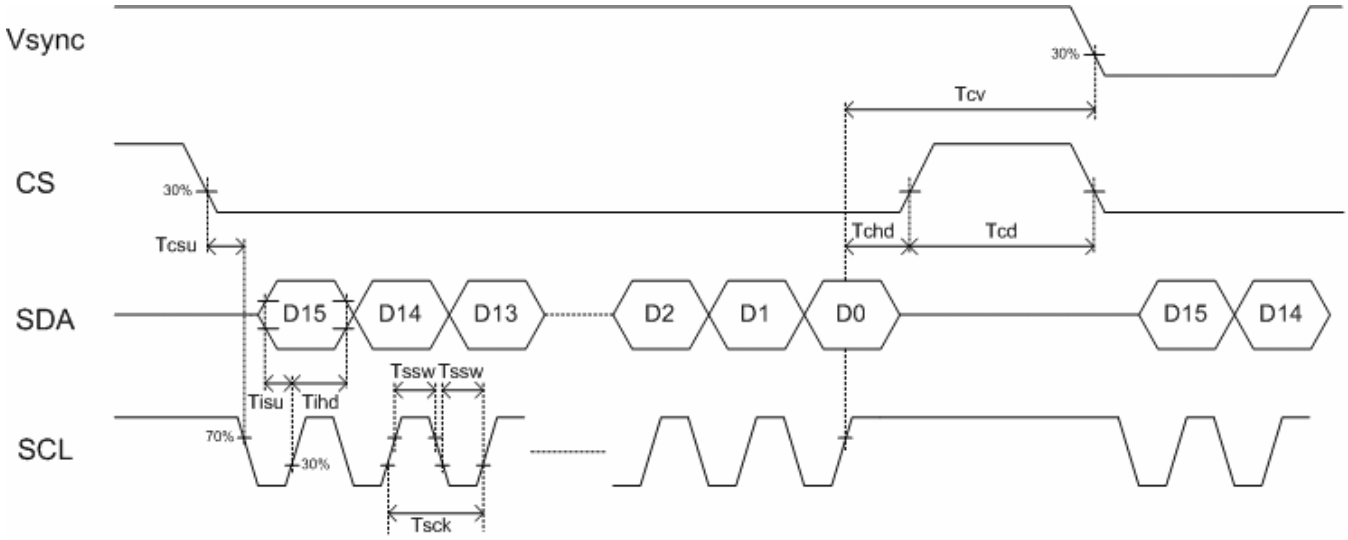
Note 1: If input timing operates with Min. to Typ. setting, the PWCK value use default value 1973 (Register R39=0000_0111, Register R40=1011_0101), and no need to change SPI register.

Note 2: If input timing operates with Typ. to Max. setting, the PWCK value must be set to 2025(Register R39=0000_0111, Register R40=1110_1001). Please reference the Serial interface setting table in Page.16 to set SPI Register R39 and R40 value.

6. Serial Interface Characteristics

a. Serial Control Interface AC Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Serial clock	Tsck	320	--	--	ns	
SCL pulse duty	Tscw	40%	50%	60%	Tsck	
Serial data setup time	Tisu	120	--	--	ns	
Serial data hold time	Tihd	120	--	--	ns	
Serial clock high/low	Tssw	120	--	--	ns	
CS setup time	Tcsu	120	--	--	ns	
CS hold time	Tchd	120	--	--	ns	
Delay from CS to VSYNC	Tcv	1	--	--	us	
Chip select distinguish	Tcd	1	--	--	us	



AC serial interface write mode timings

b. Register Bank

A totally 16-bit register includeing 7-bit address D[15:9], 1-bit Read bit D[8], and 8-bit data D[7:0] can be set via 3-wire serial peripheral interface. Beflow figure is for a detail description of the parameters.

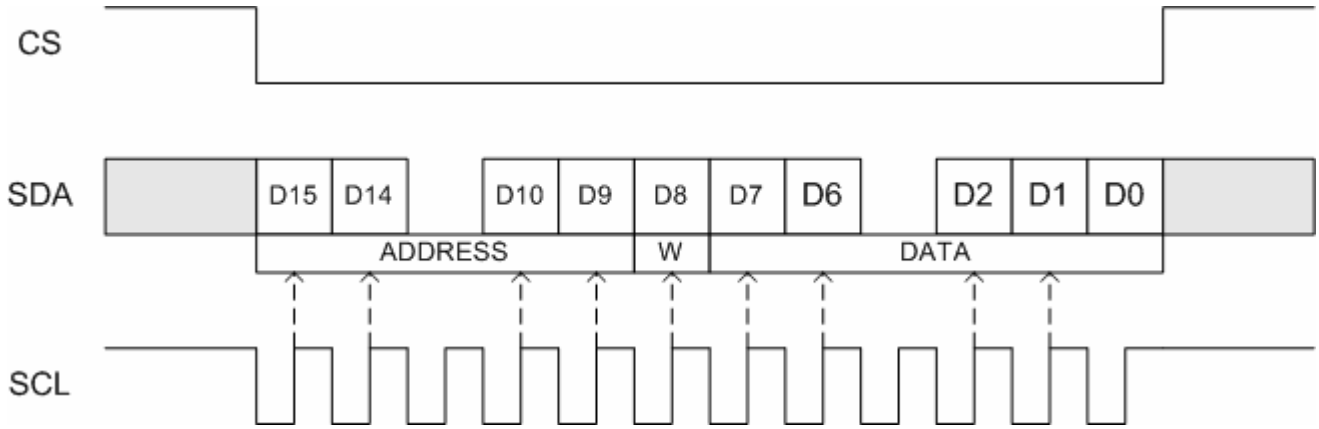


Figure. Serial interface read sequence

(1) Each serial command consists of 16bits of data which is loaded one bit a time at the rising edge of serial slock SCL.

(2) Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.

(3) The serial control block is operational after power on reset, but commands are established by the following rising edge of End Frame. If command is transferred multiple times for the same resgister, the last command before the following rising edge of the End Frame is valid, except for some special registers (ex. GRB, etc.).

(3) If less the 16 bits of SCL are input while CS is low, the transferred data is ignored. The read operation interrupt.

(4) If 16 bits or more of SCL are input while CS is low, the first 16 bits of transferred data in the duration of CS="L" are valid data.

(5) Serial block operates with the SCL clock

(6) Serial data can be accepted in the standy(power save) mode.

(7) It is suggested that DE, DCLK always exists in the same time.

(8) When GRB is activated through the serial interface, all register are cleared, except the GRB value.

(9) The register setting values are rewritten by the influence of static electricity, a noise, etc. to unsuitable value, incorrect operating may occur. It is suggested that the SPI interface will setup as frequently as possible.

c. Serial Interface Setting Table.

Reg	ADDRESS							R	DATA							
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	--	--	--	1 note 1	1 note 1	1 note 1	0	1
R1	0	0	0	0	0	0	1	0	0 note 1	0 note 1	--	--	00		00	
R39	0	1	0	0	1	1	1	0	--	--	--	--	PW_CK			
R40	0	1	0	1	0	0	0	0	PW_CK							

Note 1: The value of this bit could not be change. Otherwise the Panel will display abnormal.

d. Register Description

R0 setting

Address	Bit	Discription		Default
0000000	7 - 2	--	AUO internal use	000111
	1	STB	Standby mode setting	0
	0	GRB	S/W global reset	1

Bit 1	STB
0	Nomal operation **(default)**
1	Standby mode. Register data are kept.

Bit 0	GRB
0	S/W global reset. Reset all register to default value. H/W GRB has higher priority.
1	Normal operation. **(default)**

R1 Settings

Address	Bit	Discription		Default
0000001	7 - 4	--	AUO internal use	0000
	3 - 2	CHUD	Vertical scan direction setting	00
	1 - 0	CHLR	Horizontal scan direction setting	00

Bit 3 - 2	CHUD
0x	Accoring to H/W pin U/D setting. **(default)**
10	Vertical scan direction is from up to down.
11	Vertical scan direction is from down to up.

Bit 1 - 0	CHLR
0x	Accoring to H/W pin L/R setting. **(default)**
10	Horizontal scan direction is from left to right.
11	Horizontal scan direction is from right to left.

R39 setting

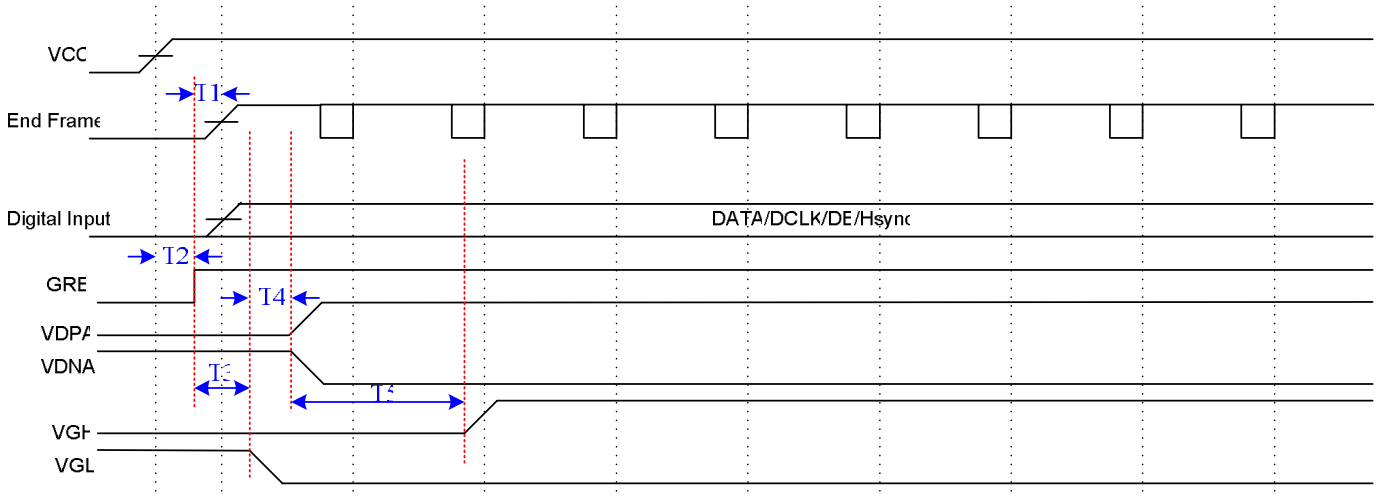
Address	Bit	Discription		Default
100111	3 - 0	--	AUO PW_CK default value	0111
	3 - 0	--	AUO PW_CK Max value	0111

R40 setting

Address	Bit	Discription		Default
101000	7 - 0	--	AUO PW_CK default value	1011_0101
	7 - 0	--	AUO PW_CK Max value	1110_1001

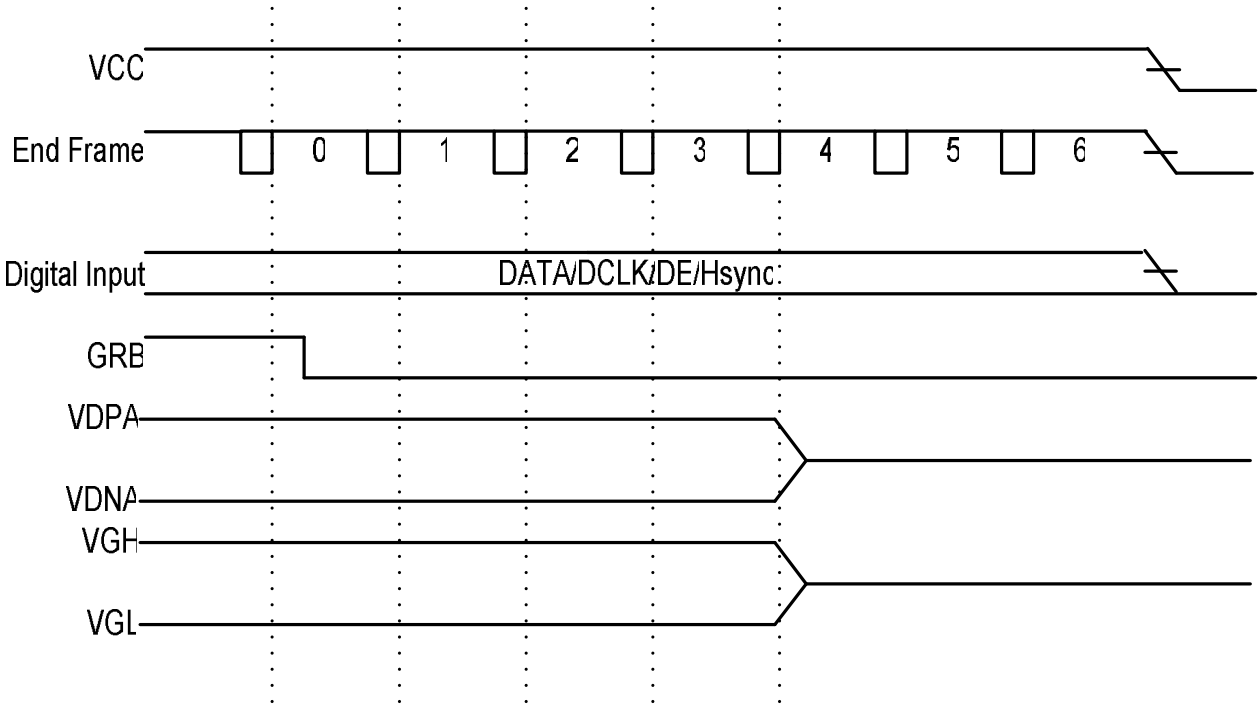
7. Power On/Off Characteristics

a. Recommended Power On Sequence



T1 > 0us; T2 ≧ 10us ; T3 ≧ 0us ; T4 > 0us ; T5 > 0us

b. Power Off Sequence



D. Optical Specification

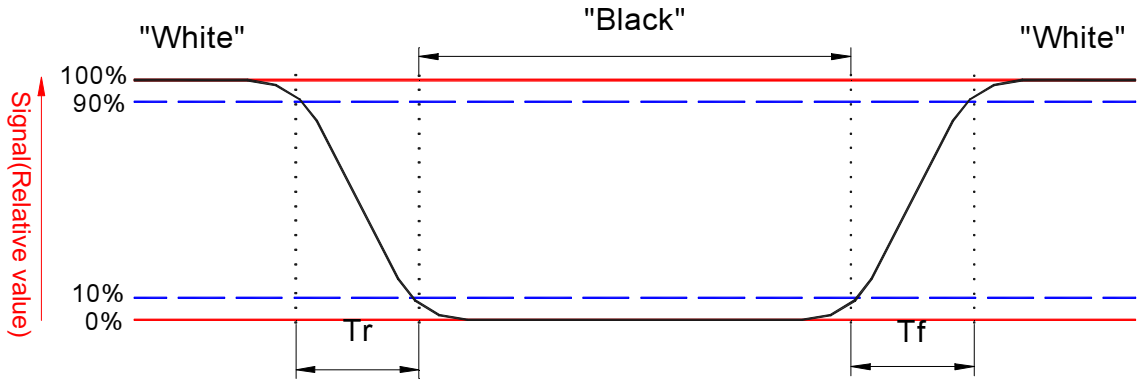
All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall		 Tr Tf	θ=0°	 -- --	 12 18	 24 36	 ms ms	Note 1
Contrast ratio		CR	At optimized viewing angle	400	500	--		Note 2
Viewing Angle	Top Bottom Left Right		CR≧10	40 50 60 60	60 65 70 70		deg.	Note 3
Transmission		Y_L	θ=0°	4.50	4.88	--	%	

Note 1: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

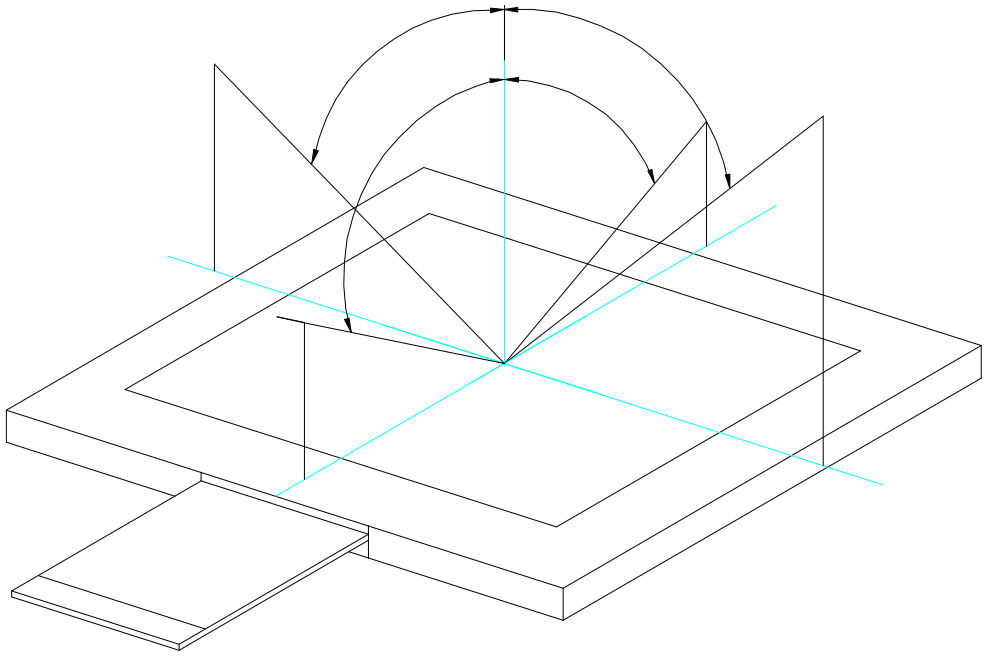


Note 2.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 3. Definition of viewing angle, θ, Refer to figure as below.



E. Reliability Test Items

No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70℃ 240Hrs	
2	Low Temperature Storage	Ta= -30℃ 240Hrs	
3	High Ttemperature Operation	Tp= 60℃ 240Hrs	
4	Low Temperature Operation	Ta= -10℃ 240Hrs	
5	High Temperature & High Humidity	Tp= 50℃. 80% RH 240Hrs	Operation
6	Heat Shock	-10℃~60℃, 100 cycle, 1Hrs/cycle	Non-operation
7	Vibration (With Carton)	Random vibration: 0.015G2/Hz from 5~200Hz	IEC 68-34
8	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1: Ta: Ambient Temperature. Tp: Panel Surface Temperature

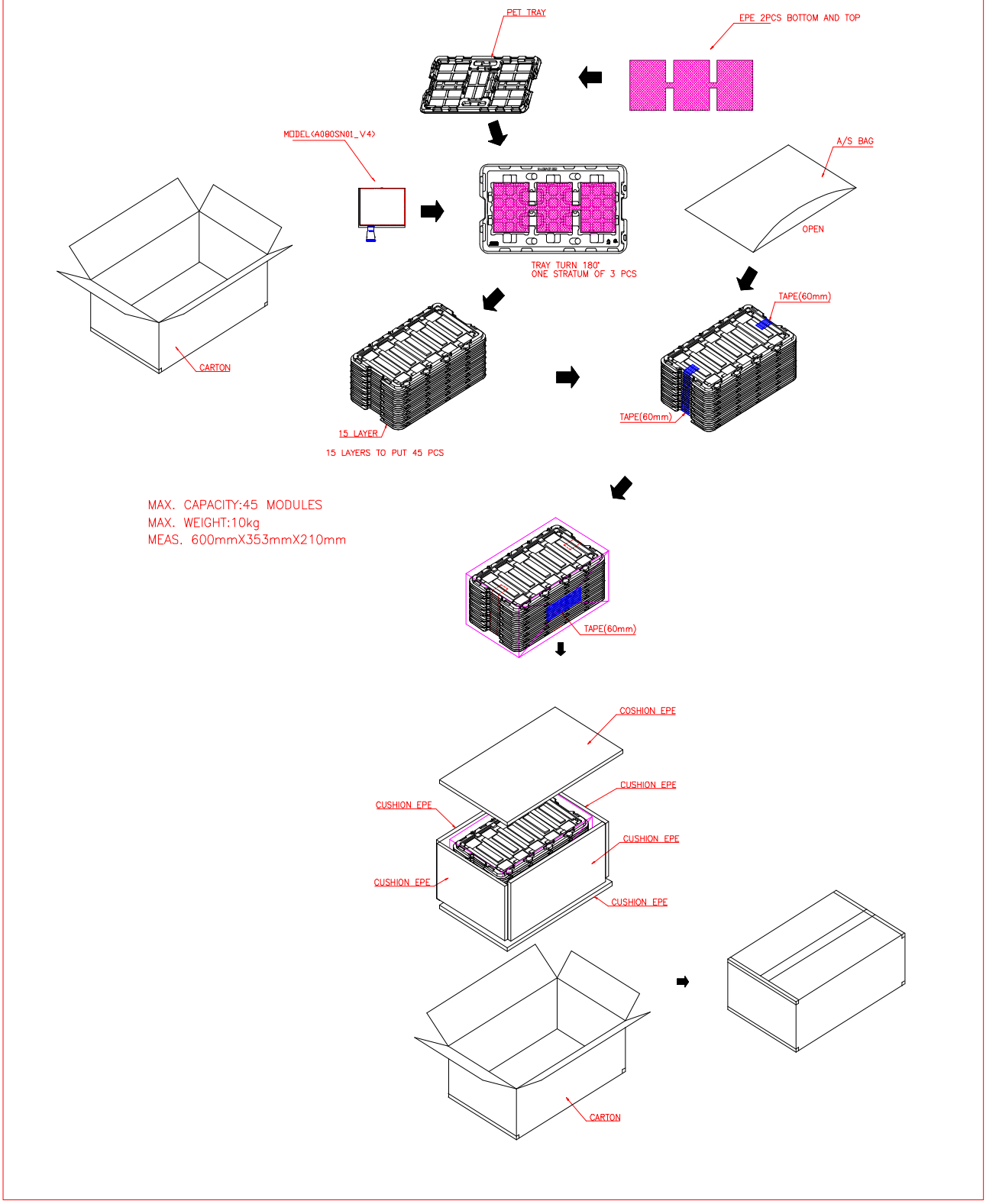
Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 3: All the cosmetic specification is judged before the reliability stress.

Note 4. In Reliability test, performance is confirmed after leave in room temperature

F. Packing and Marking

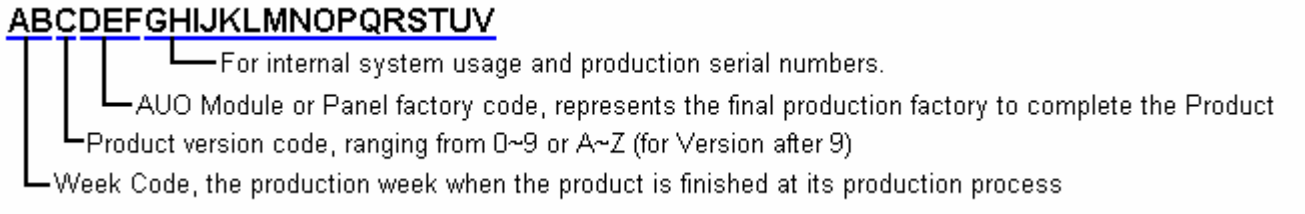
1. Packing Form



2. Module/Panel Label Information

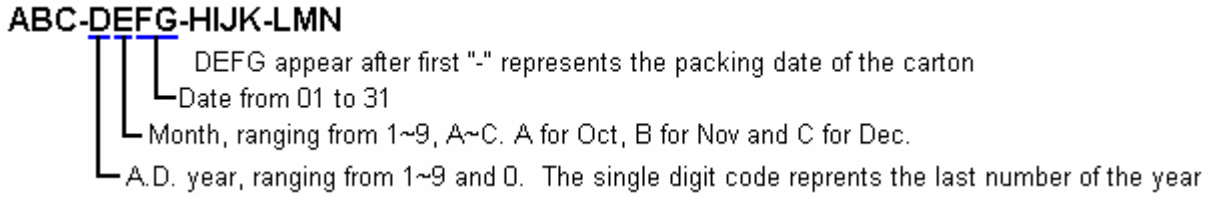
The module/panel (collectively called as the “Product”) will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for

detailed location and size of the label. The label is composed of a 22-digit serial number and printed with code 39/128 with the following definition:



3. Carton Label Information

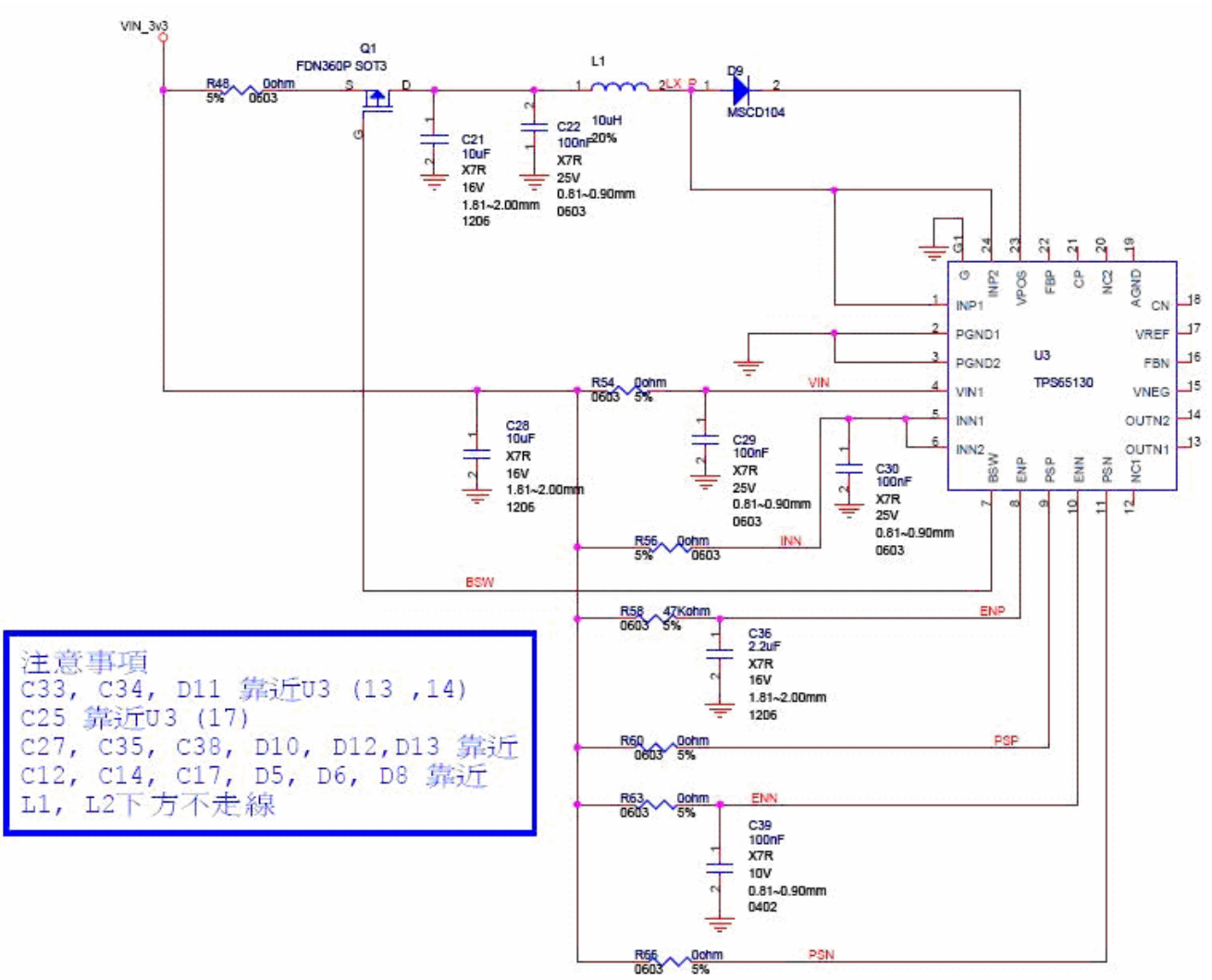
The packing carton will be attached with a carton label where packing Q'ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:

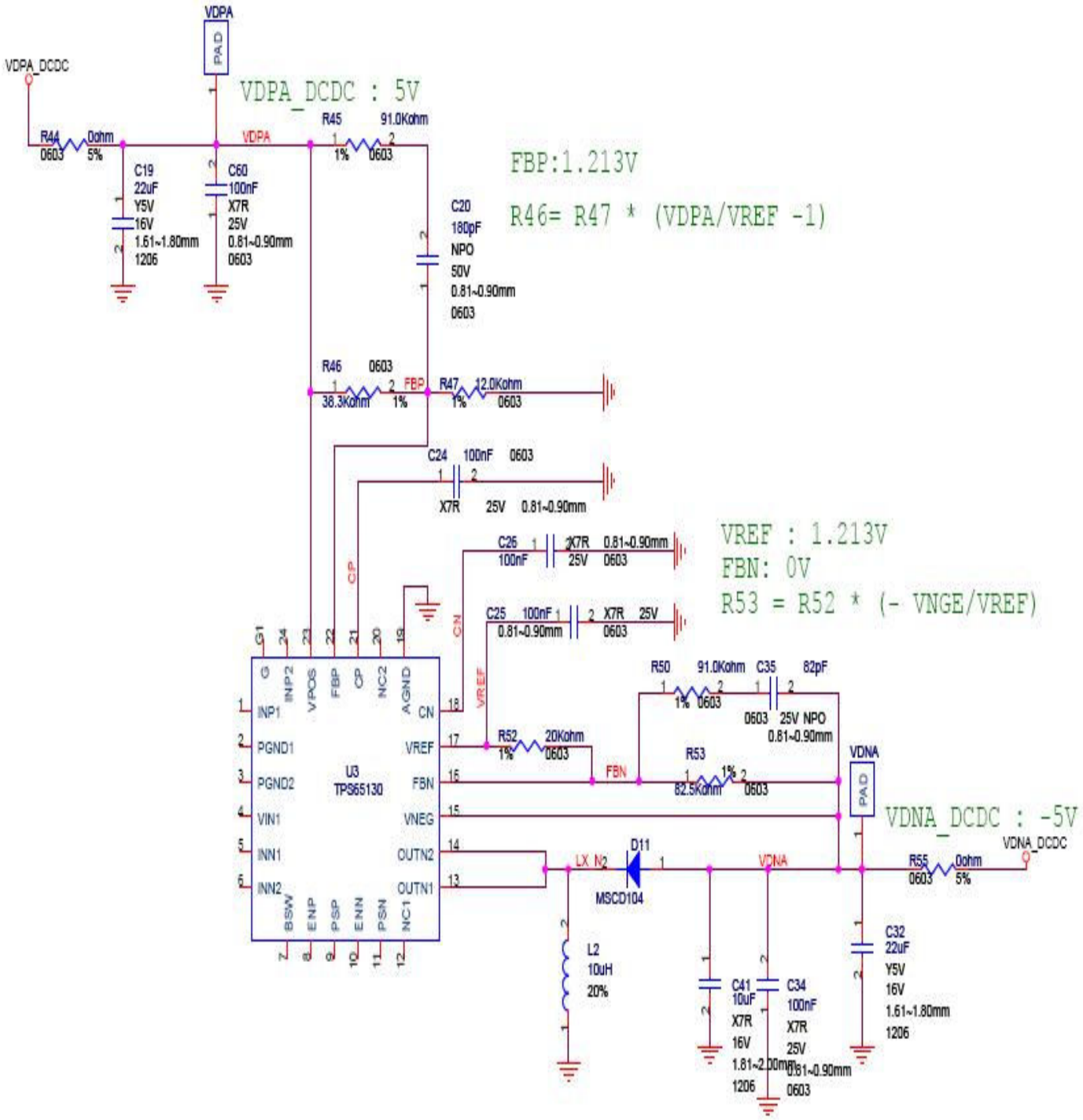


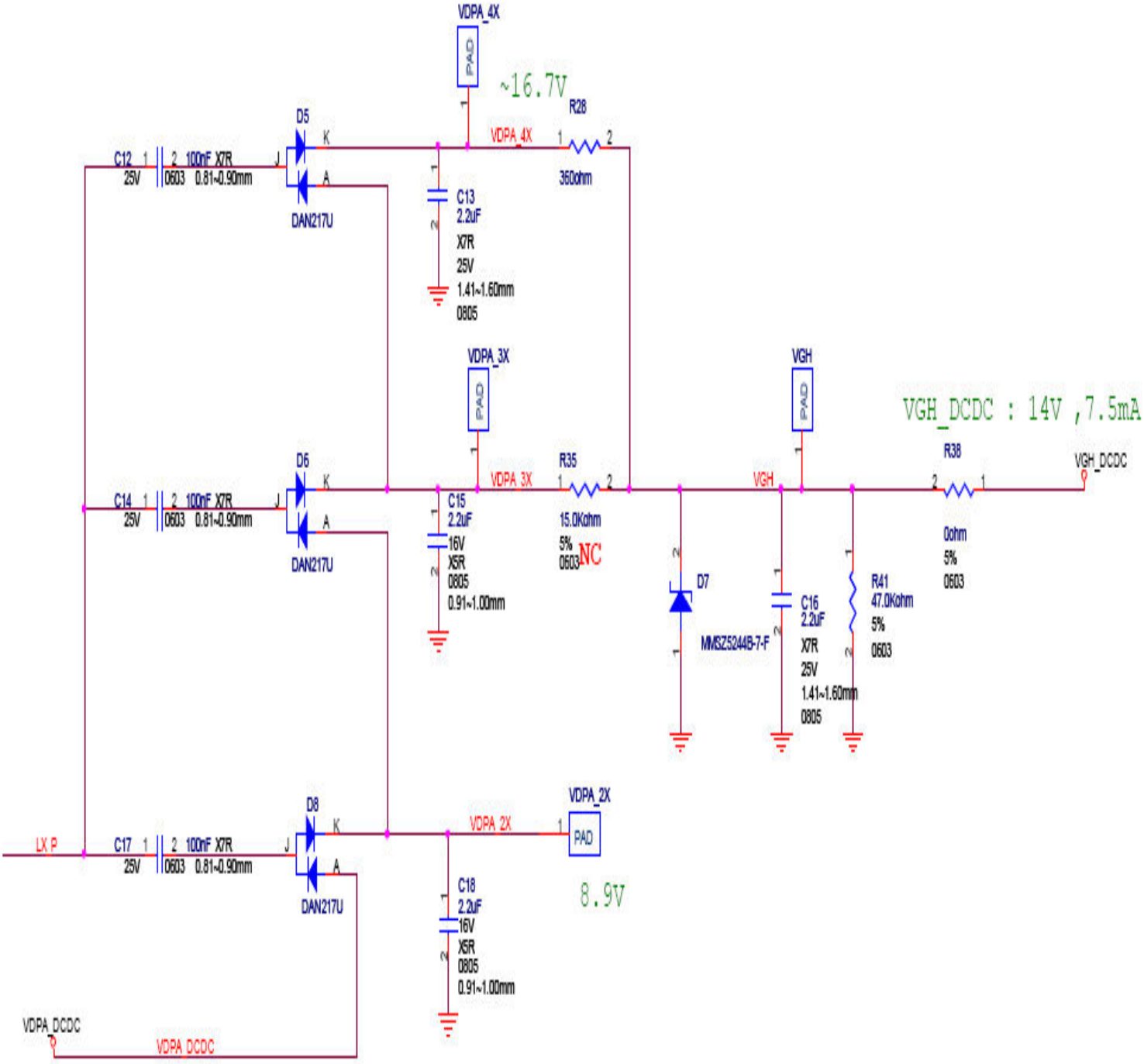
Refer to the drawing of packing format for the location and size of the carton label.

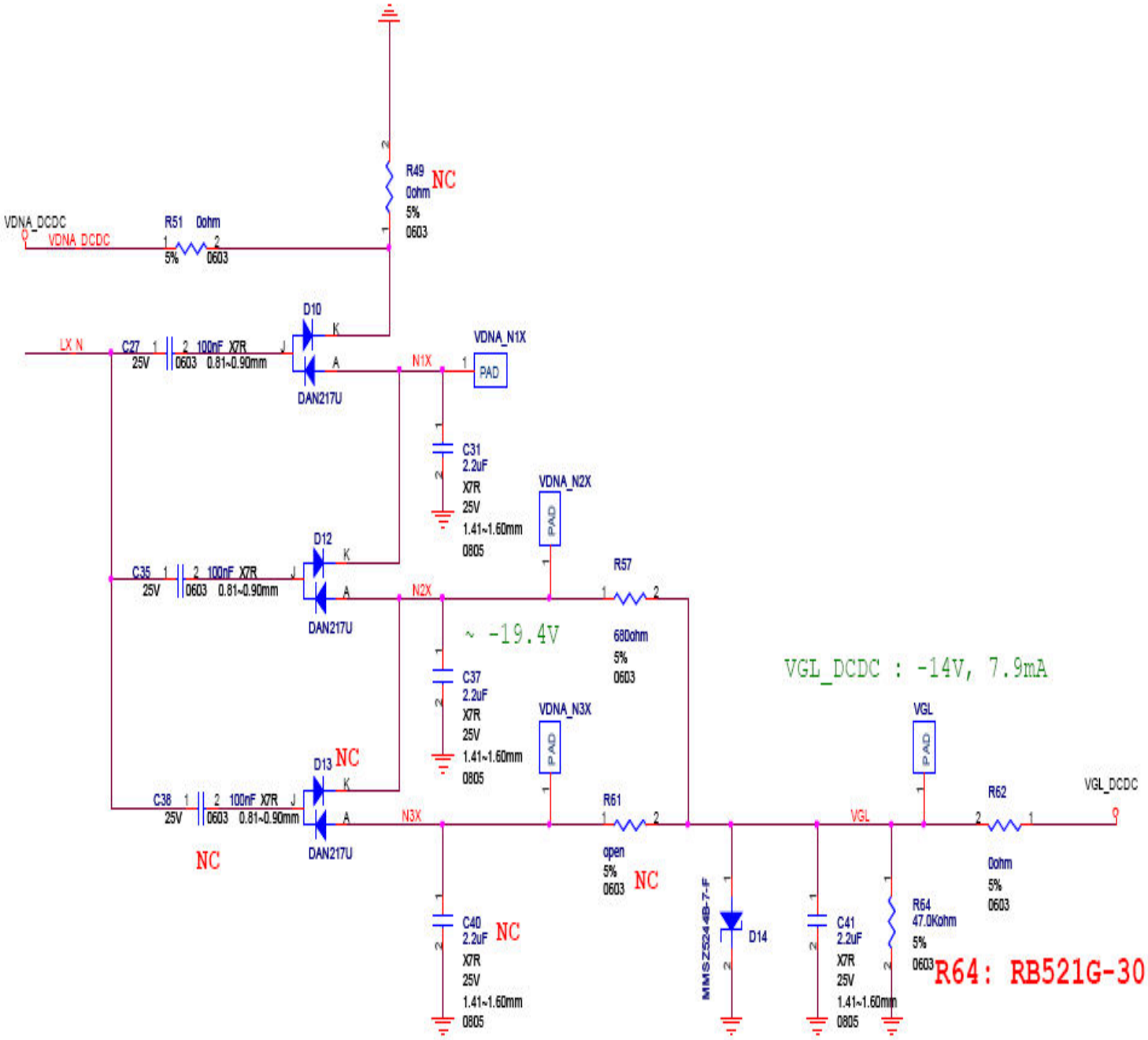
G. Application Note

1. Application Circuit

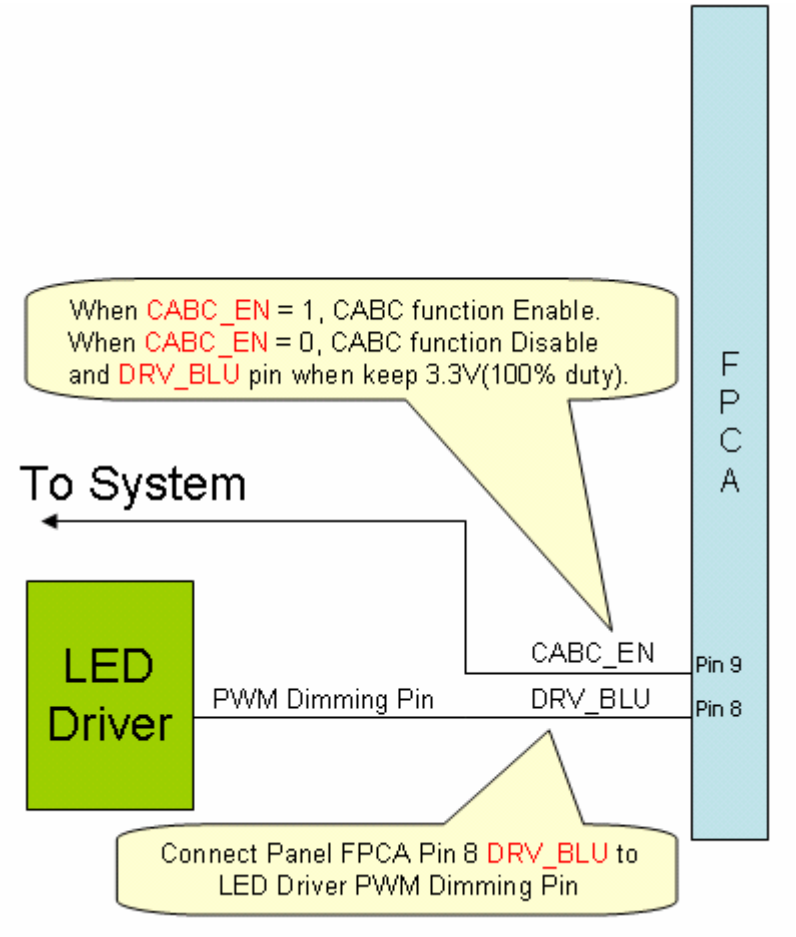








2. CABC Description



H. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.