(v) Preliminary Specifications
( ) Final Specifications

Module	**8”(8.0”) WUXGA 16:10 On-Cell TFT-LCD**
Model Name	B080UAB02.0 (H/W: 0A)
Note ( )	***LED Backlight without driving circuit design***

Customer	**Date**
Checked & Approved by	**Date**
Note: This Specification is subject to change without notice.	

Approved by	**Date**
Randolph	04/24/2019
Prepared by	
Claire Yu	04/24/2019
MPBU Marketing Division AU Optronics corporation	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2019/04/15	All	First Edition for Customer		
0.2 2019/04/22	23, 24	Modified Pin assignment		
	28,29	Modified 2D drawing		
0.3 2019/04/24	23,24	Modified pin assignment (pin 29)	Mark AUO NC	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B080UAB02.0 is a Liquid Crystal Display composed of a on-cell panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 , 1200(H) x1920(V) screen and 16.7M colors (RGB 8-bits data driver) without LED backlight driving circuit. All input signals are MIPI interface compatible.

B080UAB02.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	8”
Active Area	[mm]	107.64 (H) x 172.224(V)(LCD) 108.64(H) x 173.22(TP)
Pixels H x V		1200 x 3(RGB) x 1920
Pixel Pitch	[mm]	0.0879 X 0.0879
Pixel Format		R.G.B. Vertical Stripe
Display Mode		Normally Black
White Luminance (I_{LED}=19mA) **(Note: ILED is LED current)**	[cd/m^2]	Typ. 350nits / Min.298nits
Luminance Uniformity		70% min @13p
Contrast Ratio		900:1 typ
Response Time	[ms]	27 typ / 35 Max
Nominal Input Voltage VDD	[Volt]	+3.3 V typ
Power Consumption	[Watt]	Logic power: max. 0.4W@White with power IC BL power (w/o Effi.) : 1.46 max (6S4P) w/o efficiency ,Ityp. :19mA. TP power: 120mW @ normal operation mode.
Weight	[Grams]	max. 150g w/ CG
Electrical Interface		4 lane MIPI
Glass Thickness	[mm]	0.4(TFT),0.4(CF) ; 0.7(Coverlens, Sodalime)
Support Color		RGB 8-bit
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60

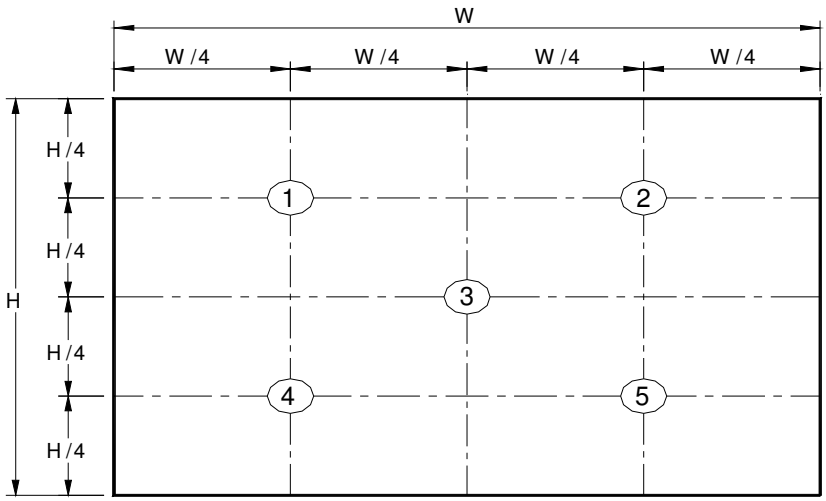
RoHS Compliance		RoHS Compliance			
Color of cover lens		TBD			
Type of Touch Sensor		On-cell			
Multi-Touch	Points	10			
Touch Report Rate	Hz	1 finger: @ 80Hz 2 fingers @ 80Hz			
Touch Input method		Finger			
Touch panel sensor IC		Parade TT41701-111BUI65			
Touch Sensor Channel		24 x38			
Touch Distance between 2 points	mm	H: ≦7mm V: ≦7mm D: ≦7mm			
Cover Lens Surface hardness	H	TBD			
Bonding Glue Thickness	um	200 typ,			
Total solution Dimension	[mm]		Min.	Typ.	Max.
		Length		193.28	
		Width		117.70	
		Thickness	---	3.27	

2.2 Optical Characteristics

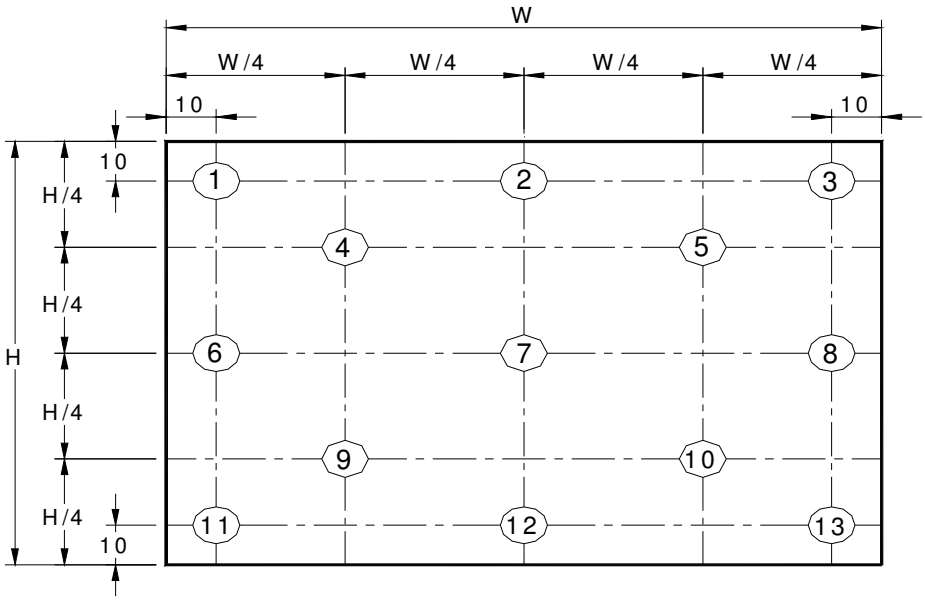
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=19mA			Central point	298	350	---	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10	75	80	---	degree	4, 9
		θ_L	(Left)	75	80	---		
		ψ_H	Vertical (Upper) CR = 10	75	80	---		
		ψ_L	(Lower)	75	80	---		
Luminance Uniformity		δ_{5P}	5 Points		---	---		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	70%	---	---		2, 3, 4
Contrast Ratio		CR		700	900	-		4, 6
Cross talk		%		---	---	1.2		4, 7
Response Time		T_{RT}	Rising + Falling	---	27	35	msec	4, 8
Color / Chromaticity Coordinates	Red	Rx	CIE1931	TBD	TBD	TBD		4
		Ry		TBD	TBD	TBD		
	Green	Gx		TBD	TBD	TBD		
		Gy		TBD	TBD	TBD		
	Blue	Bx		TBD	TBD	TBD		
		By		TBD	TBD	TBD		
	White	Wx		0.265	0.295	0.325		
		Wy		0.285	0.315	0.345		
NTSC		%		-	60	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



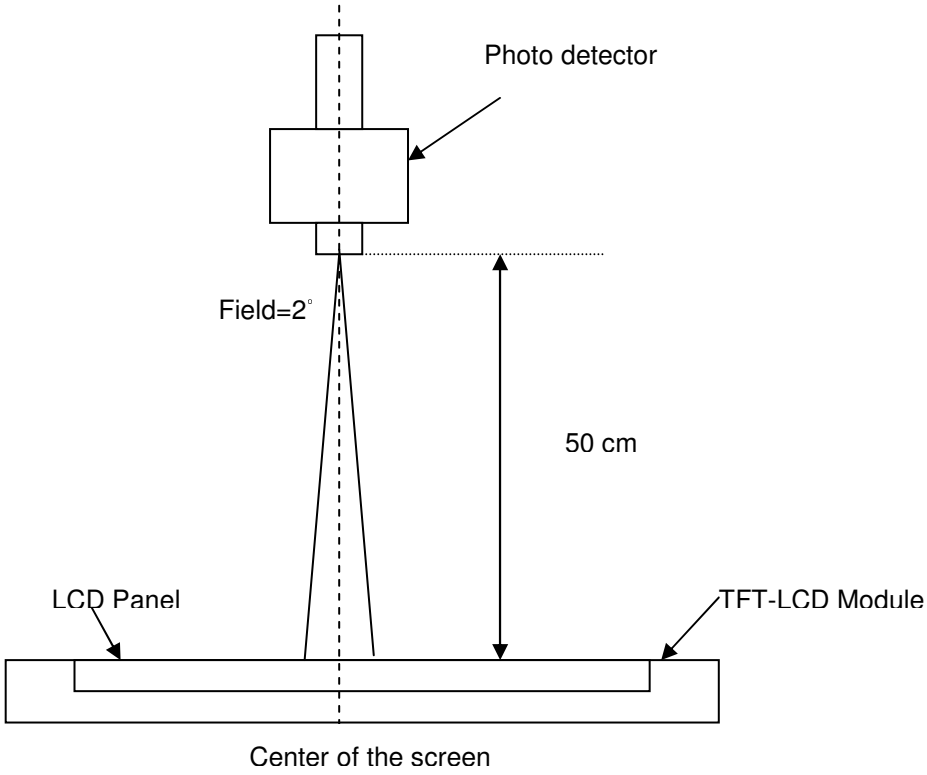
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

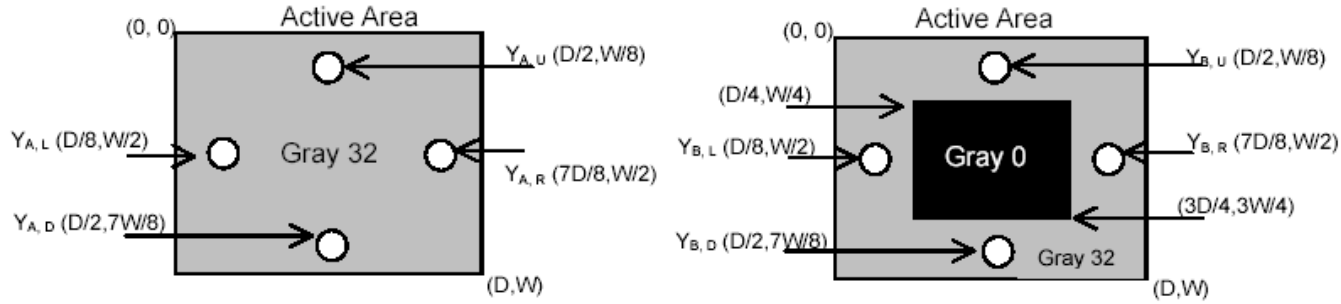
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

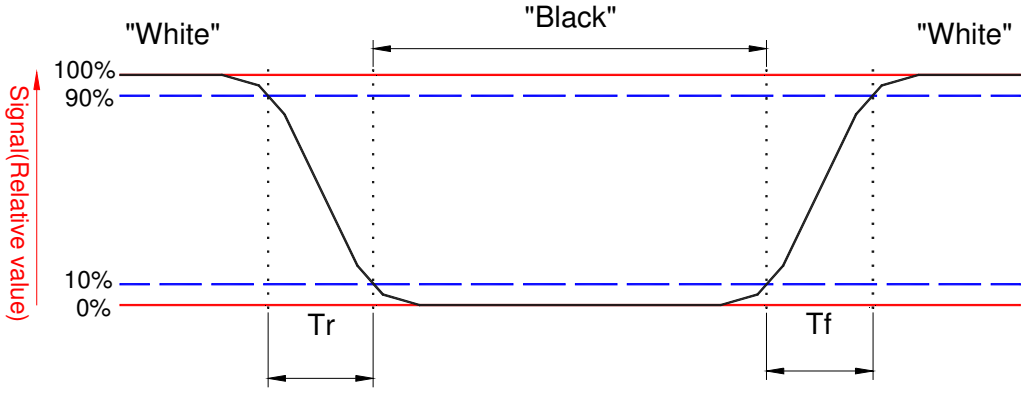
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



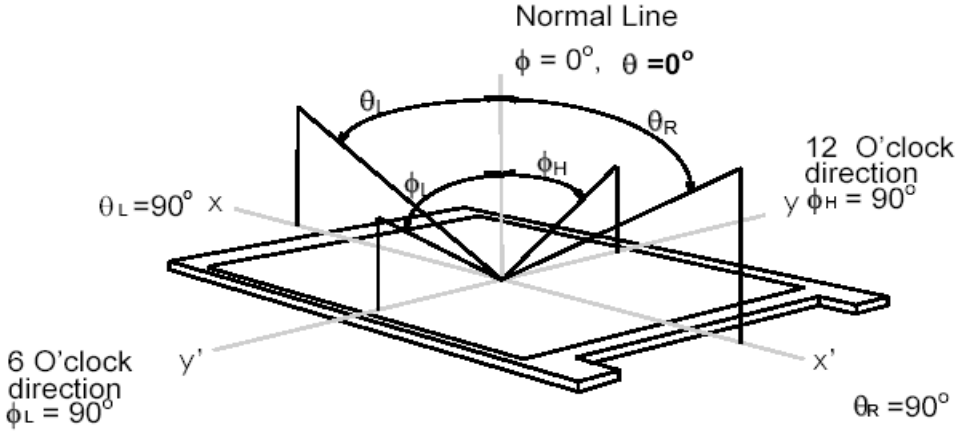
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



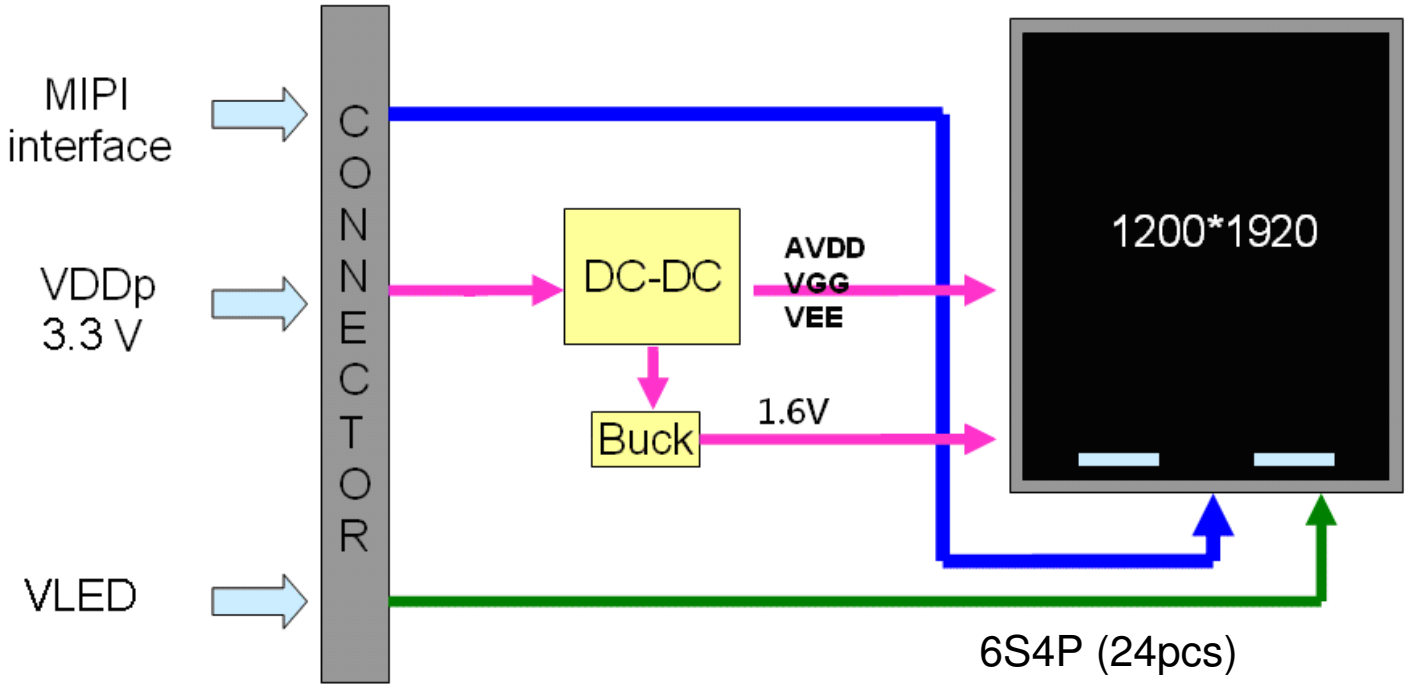
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 8 inches wide Color TFT/LCD 45 Pin four channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Touch Sensor

Item	Applicable Pins	Symbol	Condition	Rating	Unit
Voltage from VCC33 to DGND and AGND	AVDD	AVDD	Power	6	V
Voltage from any pin to DGND and AGND	I2C(SCL/SDA)	SCL/SDA	I2C	6	
Operating Temperature Range	-	T_A	-40	85	℃
Storage Temperature Range	-	T_{STR}	-55	150	

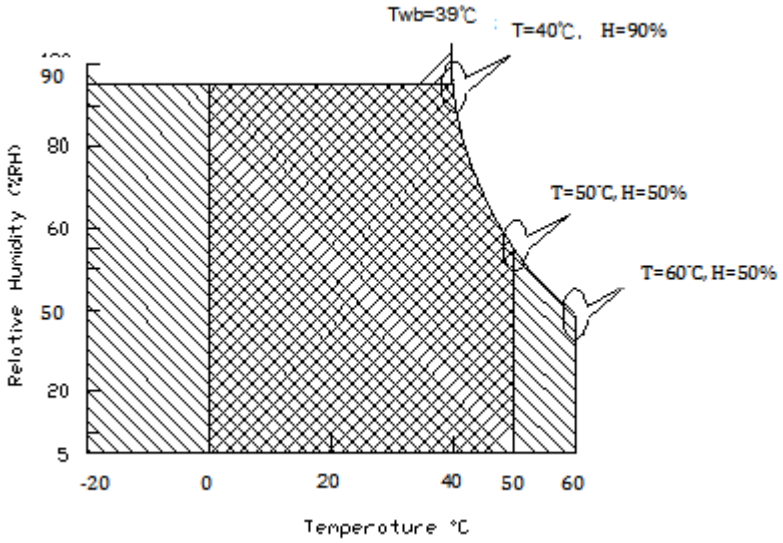
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

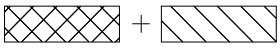
Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range 

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

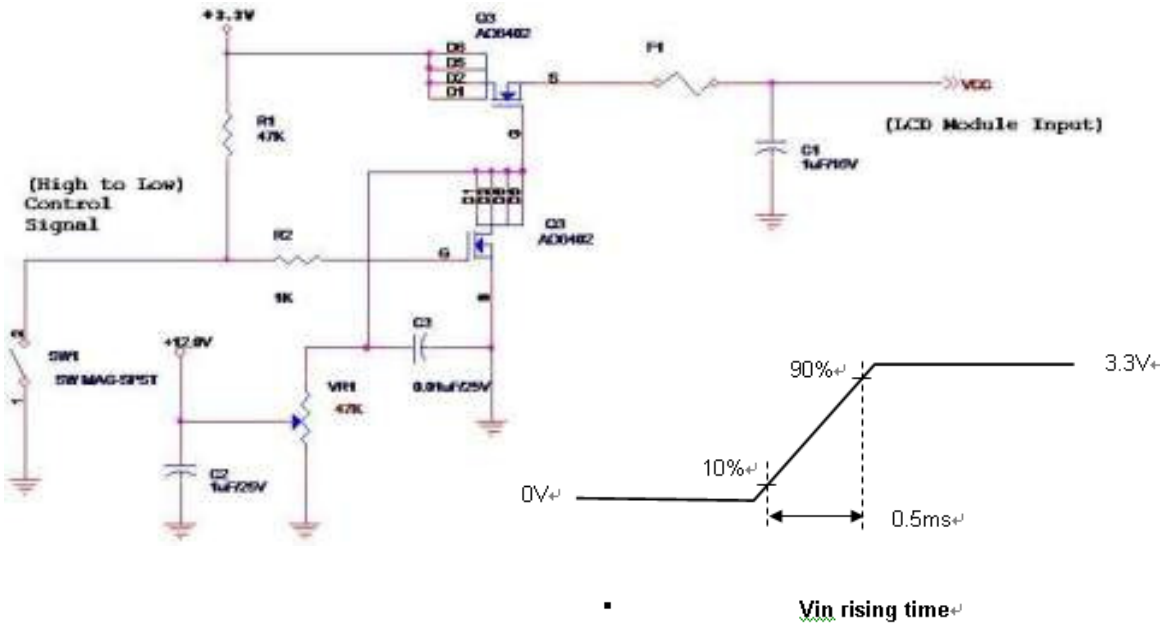
Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	_	-	0.45	[Watt]	Note 1
IDD	IDD Current	-	-	150	[mA]	Note 1
IRush	Inrush Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3}$ x I_{black})

Note 2：Measure Condition



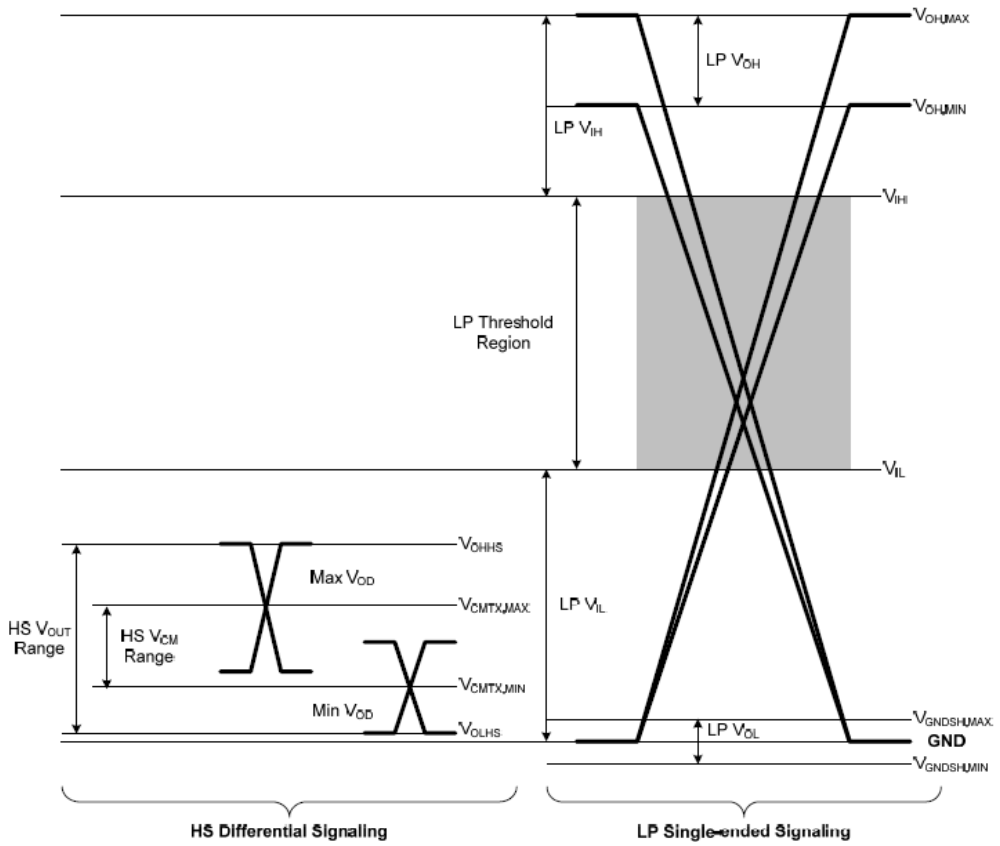
▪ Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

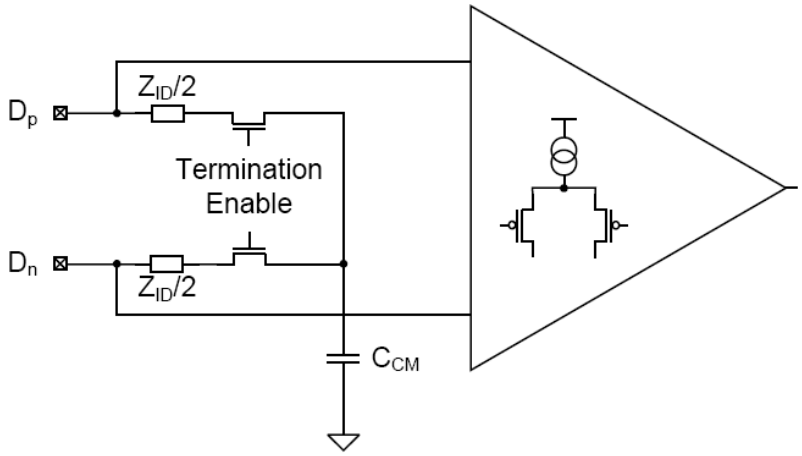
MIPI DC characteristics are as follows:

MIPI Receiver Differential Input (DC Characteristics)					
Symbol	Parameter	Min	Typ	Max	Unit
BR_{MIPI}	Input data bit rate	200	-	1000	Mbps
V_{CMRX}	Common-mode voltage(HS Rx mode)	155	-	330	mV
V_{IDTH}	Differential input high threshold (HS Rx mode)	-	-	70	mV
V_{IDTL}	Differential input low threshold (HS Rx mode)	-70	-	-	mV
$\lvert V_{IDM} \rvert$	Differential input voltage range (HS Rx mode)	70	-	500	mV
V_{IHHS}	Single-end input high voltage (HS Rx mode)	-	-	460	mV
V_{ILHS}	Single-end input low voltage (HS Rx mode)	-40	-	-	mV
Z_{ID}	Differential input impedance	80	100	125	Ω
V_{IHLP}	Logic 1 input voltage (LP Rx mode)	880			mV
V_{ILLP}	Logic 0 input voltage (LP Rx mode)			550	mV



MIPI Receiver Differential Input (AC Characteristics)						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz		-	-	100	mV
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz ~ 450MHz		-50	-	50	mV
C_{CM}	Common-mode termination		-	-	60	pF
UI_{INST}	UI instantaneous		1		12.5	ns

HS RX Scheme

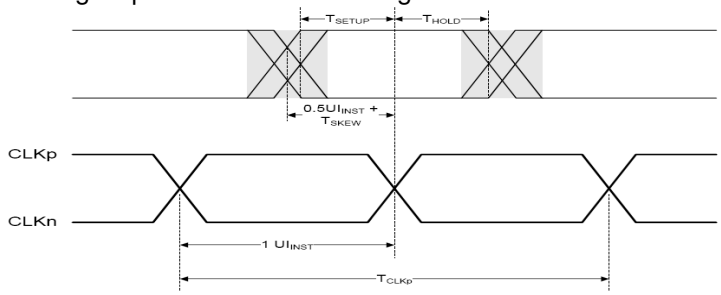


Symbol	Parameter	Min	Typ	Max	Unit	Notes
$T_{SKEW[TX]}$	Data to Clock Skew (mesured at transmitter)	-0.15		0.15	UI_{INST}	1
$T_{SETUP[RX]}$	Data to Clock Setup Time (receiver)	0.25			UI_{INST}	2
$T_{HOLD[RX]}$	Data to Clock Hold Time (receiver)	0.25			UI_{INST}	2

Note:

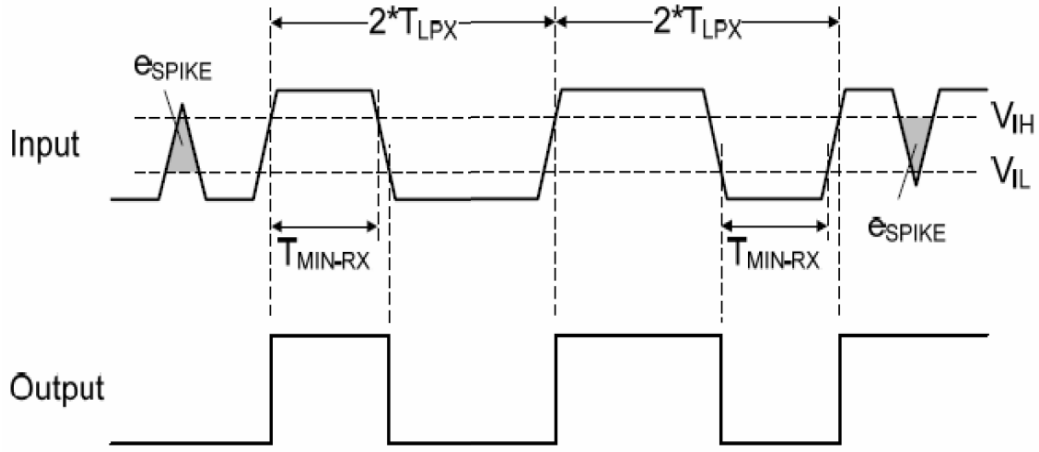
1. Total silicon and package delay budget of 0.25*UI_{INST}
2. Total setup and hold window for receiver of 0.5 *UI_{INST}

MIPI High-Speed Data-clock Timing

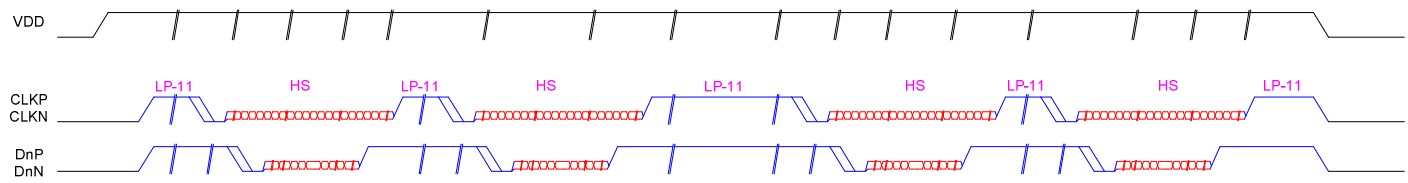


LP Receiver AC Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
e_{SPIKE}	Input pulse rejection		-	-	300	V · ps
T_{MIN-RX}	Minimum pulse width response		50	-	-	ns
V_{INT}	Peak interference amplitude		-	-	200	mV
f_{INT}	Interference frequency		450	-	-	MHz

Input Glitch Rejection of Low-Power Receivers



For MIPI data transmission from TX to TCON works properly in video mode, it is suggested that all of MIPI lanes status follow the scheme showed in below. When power is turned on, all lanes (include clock lane) are into LP-11 status first. When TX wants to start transmitting data to TCON, the clock lane is into HS and start toggling. Then data lanes are into HS and data are transmitted. After data transmissions are finished (ex. H-blanking, V-blanking), the data lanes are returned to LP-11, then clock lane, too. The transmission start from LP-11 and stop in LP-11 on all lanes (include clock lane) are the recommended proper operation sequence for MIPI video mode.



The timing definitions are listed in below,

Parameter	Description	Min	Typ	Max	Unit
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns

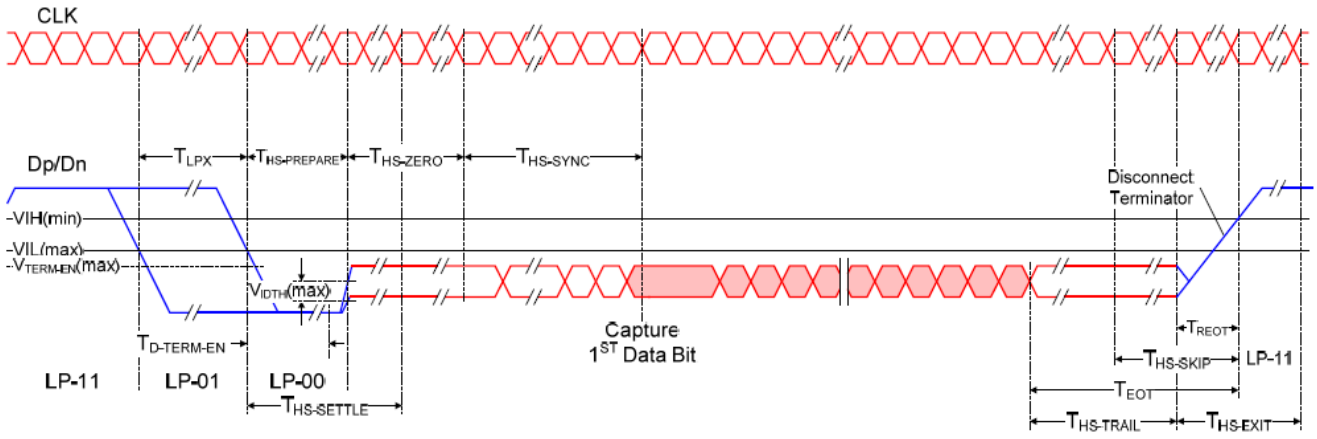
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60 ns + 52*UI			ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			35 ns + 4*UI	ns
TEOT	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.			105 ns + 12*UI	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100			ns
THS-SYNC	HS Sync-Sequence '00011101' period		8		UI
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns

THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE.	85 ns + 6*UI		145 ns + 10*UI	ns
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60 ns + 4*UI			ns
TLPX	Transmitted length of any Low-Power state period	50			ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	2/3		3/2	
TTA-GET	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*TLPX		ns
TTA-GO	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*TLPX		ns
TTA-SURE	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX		2*TLPX	ns

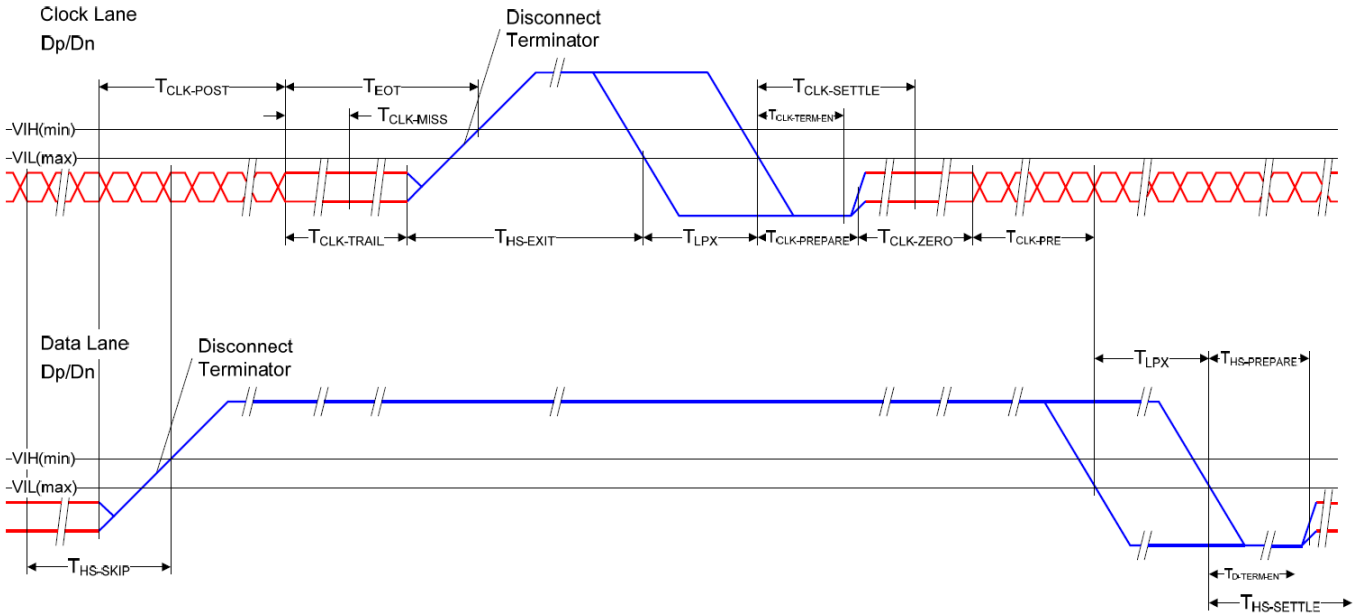
Note:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
3. The I-chip of AUO use is not support BTA (BTA define ignore).

High-Speed Data Transmission in Bursts



Switching the Clock Lane between Clock Transmission and Low-Power Mode



Turnaround Procedure

5.2 Touch Sensor Power Consumption

Parameter	Pins	Symbol	Condititon	Rated Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	**Power**	**VCC33**	**-**	3.0	3.3	4.7	**V**
Normal mode Current consumption @ Report rate 100Hz	**Power**	**I_{NORMAL}**	**VCC33=3.3V**	-	-	40	**mA**
Sleep mode Current consumption	**Power**	**I_{SLEEP}**	**VCC33=3.3V**	-	2	-	

5.3 Backlight Unit

5.3.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED			1.46	[Watt]	(Ta=25℃)
LED Life-Time	N/A	TBD			Hour	(Ta=25℃) Note1.
LED Forward Voltage	VF				[Volt]	(Ta=25℃)
LED Forward Voltage of every LED string	VF-string				[Volt]	(Ta=25℃) Note2.
LED Forward Current (1 series)	IF	-	19	-	[mA]	(Ta=25℃)

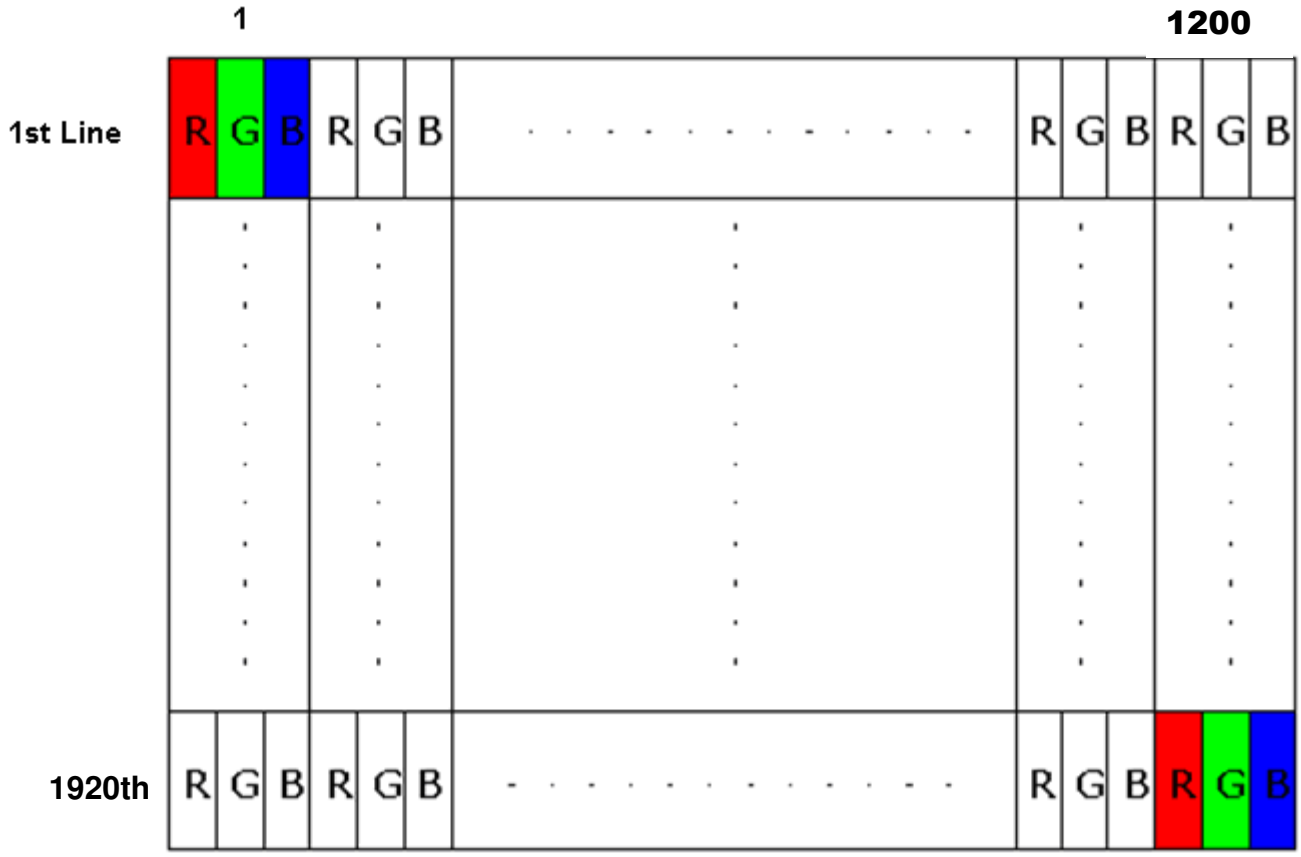
Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	I-PEX
Type / Part Number	20655-045E-01
Mating Housing/Part Number	FPC connector

6.2.2 Pin Assignment

MIPI lane is a differential signal technology for LCD interface and high speed data transfer device.

Pin assignment

Pin	Symbol	Description
1	LED+	Power for LED Anode
2	LED+	Power for LED Anode
3	NC	No connection
4	LED1-	Power for LED1 Cathode
5	LED2-	Power for LED2 Cathode
6	LED3-	Power for LED3 Cathode
7	LED4-	Power for LED4 Cathode
8	NC	No connection
9	GND	Ground
10	D0+	MIPI differential data0 input (Positive)
11	D0-	MIPI differential data0 input (Negative)
12	GND	Ground
13	D1+	MIPI differential data1 input (Positive)
14	D1-	MIPI differential data1 input (Negative)
15	GND	Ground
16	CLK+	MIPI differential clock input (Positive)
17	CLK-	MIPI differential clock input (Negative)
18	GND	Ground
19	D2+	MIPI differential data2 input (Positive)
20	D2-	MIPI differential data2 input (Negative)
21	GND	Ground
22	D3+	MIPI differential data3 input (Positive)
23	D3-	MIPI differential data3 input (Negative)
24	GND	Ground
25	NC	AUO Aging
26	ID0	System Hardware ID0 Select(Pull Low to GND with 10KΩ)
27	ID1	System Hardware ID1 Select(Pull Low to GND with 10KΩ)
28	RESX	AUO NC

29	VDDI	AUO NC (system: 1.8V input power)
30	OTP	Power supply pin for the OTP memory programming. –Panel vendor use
31	VDD	3.3V input power
32	VDD	3.3V input power
33	NC	AUO I2C (SCL)
34	NC	AUO NC (system: AVDD)
35	NC	AUO I2C (SDA)
36	NC	AUO NC (system: AVEE)
37	NC	NC
38	LEDPWM_OUT	AUO NC
39	GND	Ground
40	TP-VDD	3.3V input power
41	TP_SCL	Serial I2C clock signal
42	TP_SDA	Serial I2C data signal
43	TP_INT	Interrupt signal for TP
44	TP_RESX	AUO NC
45	GND	Ground

6.3 Touch Sensor Signal Description/ Pin Assignment

6.3.1 Touch Sensor Pin Assignment

Touch FPCA

TBD

6.4 Interface Timing

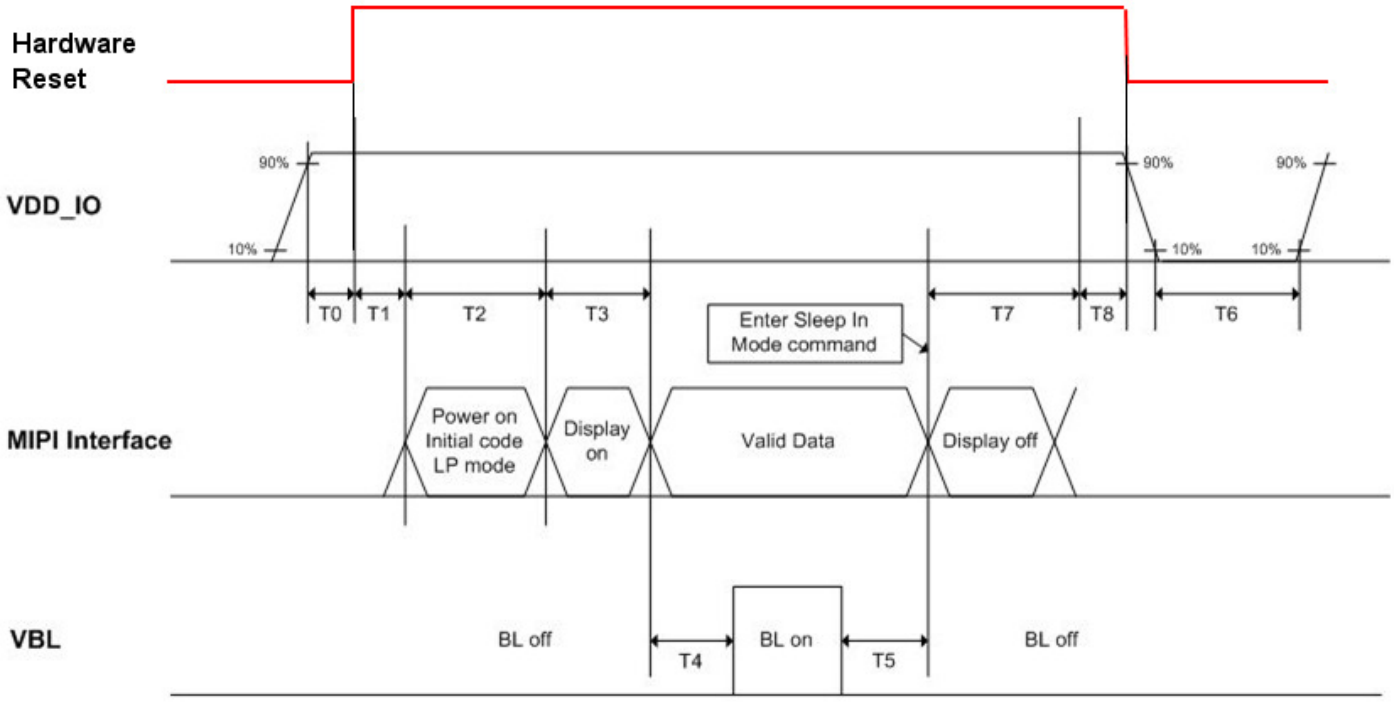
6.4.1 Timing Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---		60		Hz
MIPI data frequency		1/ T_{Clock}	893	999	1000	Mbps
Vertical Section	Period	T_V	1946	1981	1982	T_{Line}
	Active	T_{VD}	1920			
	Blanking	T_{VB}	10	25	25	
		T_{VF}	15	35	36	
		T_{VPW}	1	1	1	
Horizontal Section	Period	T_H	1275	1341	1342	T_{Clock}
	Active	T_{HD}	1200			
	Blanking	T_{HB}	32	60	60	
		T_{HF}	60	80	81	
		T_{HPW}	1	1	1	

6.5 Power On / Off Sequence

6.5.1 Power On/off sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.



	Min.	Typ.	Max.	Unit
T0 +T1	30	-		ms
T2	50	-		ms
T3	-	0	-	ms
T4	100	-	-	ms
T5	50	-	-	ms
T6	500	-	-	ms
T7	100	-	-	ms
T8	0	-	-	ms

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

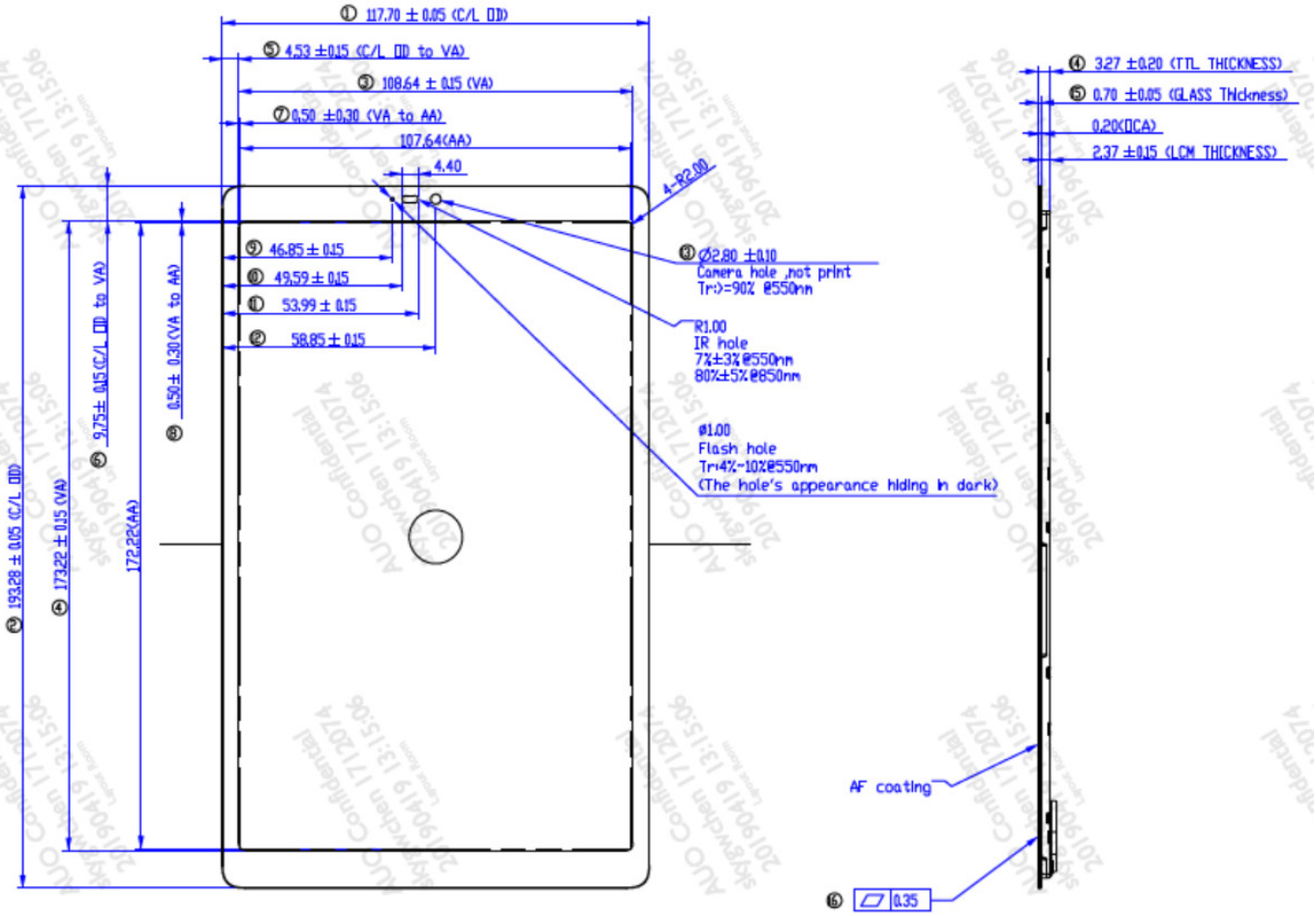
7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 60℃, 90%RH, 240h	
High Temperature Operation	Ta= 60℃, Dry, 240h	
Low Temperature Operation	Ta= -20℃, 240h	
High Temperature Storage	Ta= 80℃, 240h	
Low Temperature Storage	Ta= -40℃, 240h	
Thermal Shock Test	[(-40℃ 60min) → [(-40℃~60℃ 5min) → (60℃)60min)]/cycle, 30cycles->25℃120min.	
ESD	Class B (Air +/-15KV, Contact +/-8KV)	

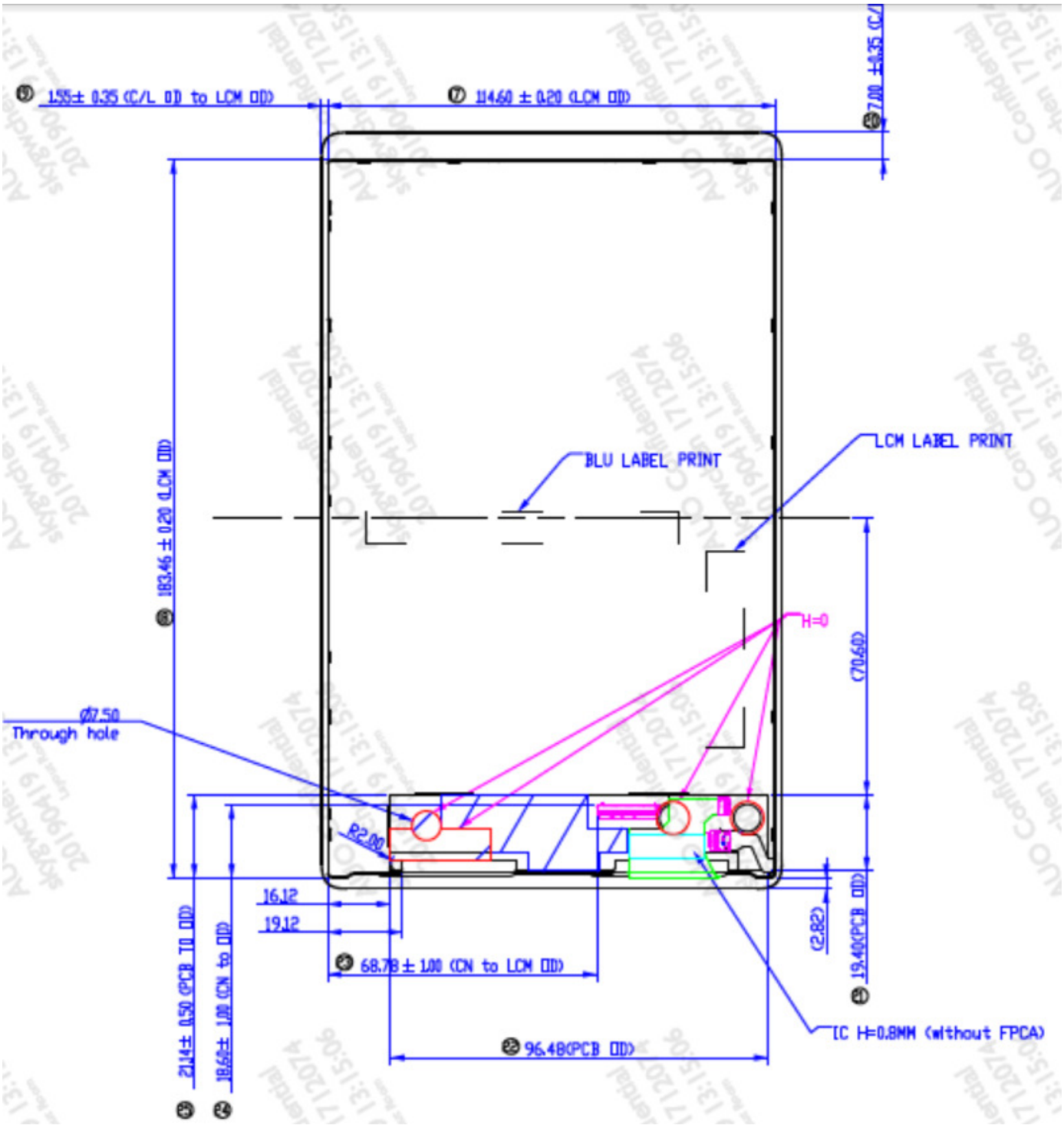
Note1: According to EN 61000-4-2 , ESD class B

8. Mechanical Characteristics

8.1.1 Standard Front View



8.1.2 Standard Back View



9. Shipping and Package

9.1 Shipping Label Format

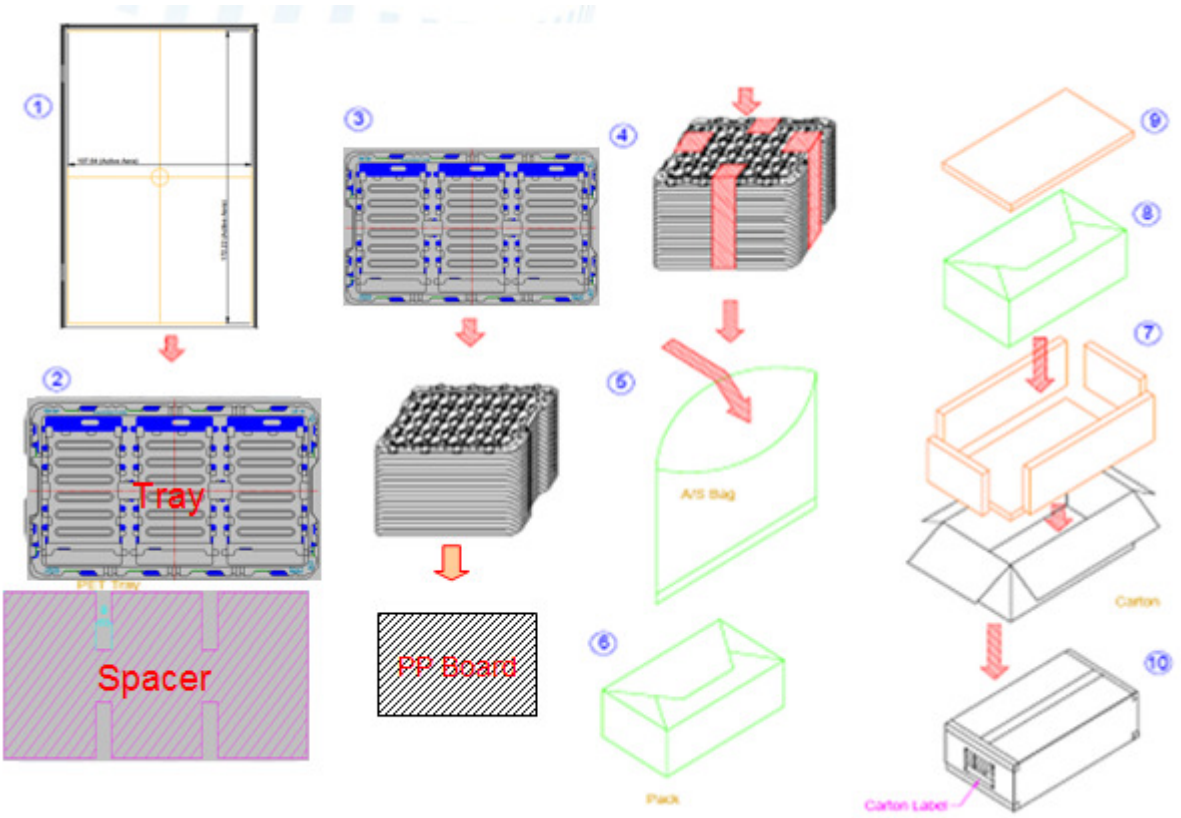
Shipping label

TBD

Carton Label

TBD

9.2 Carton Package



9.3 Shipping Package of Palletizing Sequence