AU OPTRONICS CORPORATION

Product Specification

17.0” WUXGA Color TFT-LCD Module

Model Name: B170UW02 V0 Rev 0.1

Approved by	Prepared by

MDBU Marketing Division / AU Optronics corporation

Customer	Checked & Approved by

Product Specification

17.0” WUXGA Color TFT-LCD Module
Model Name: B170UW02 V0
Rev 01

(V) Preliminary Specifications
( ) Final Specifications

Note: This Specification is subject to change without notice.

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
V1 2007/01/02	All	First Edition		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

2. General Description

B170UW02 V0 Rev A01 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WUXGA (1920(H) x 1200(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter of backlight is not included.

B170UW02 V0 Rev 01 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

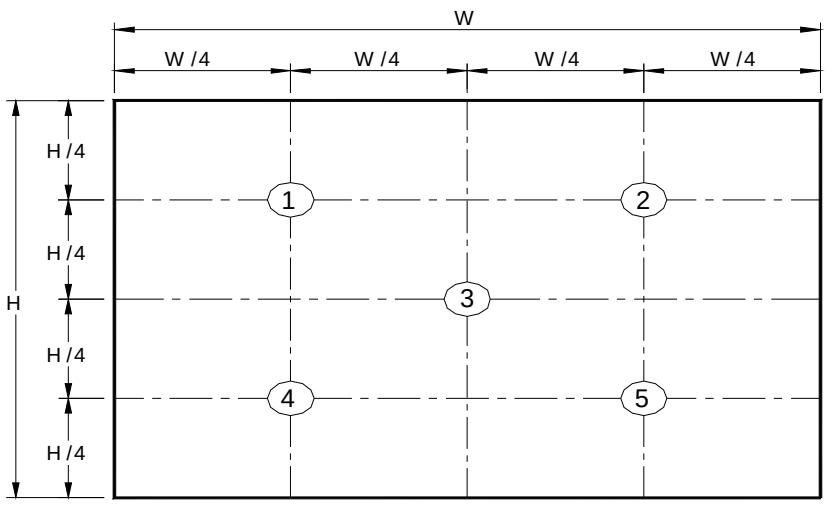
Items	Unit	Specifications
Screen Diagonal	[mm]	17.0”
Active Area	[mm]	367.20(H) x 229.50(V)
Pixels H x V		1920x3(RGB) x 1200
Pixel Pitch	[mm]	0..191(per one triad) x 0.191
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (ICCFL=6.5mA)	[cd/m^2]	400 typ. (5 points average) 350 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		600 typ.
Response time	[msec]	8 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Typical Power Consumption	[Watt]	3.0 W max. (without Inverter)
Weight	[Grams]	700 g max.
Physical Size	[mm]	382.7mm Max (W) 248.0mm Max (H) 7.0 mm Max (T)
Electrical Interface		6bit 2 channel LVDS
Surface Treatment		Anti-glare, Harness 4 H
Support Color		Native 262K colors (RGB 6-bit data driver)
Temperature Range Operating Storage (Non-Operating)	 [^{o}C] [^{o}C]	 0 to +50 -40 to +65
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

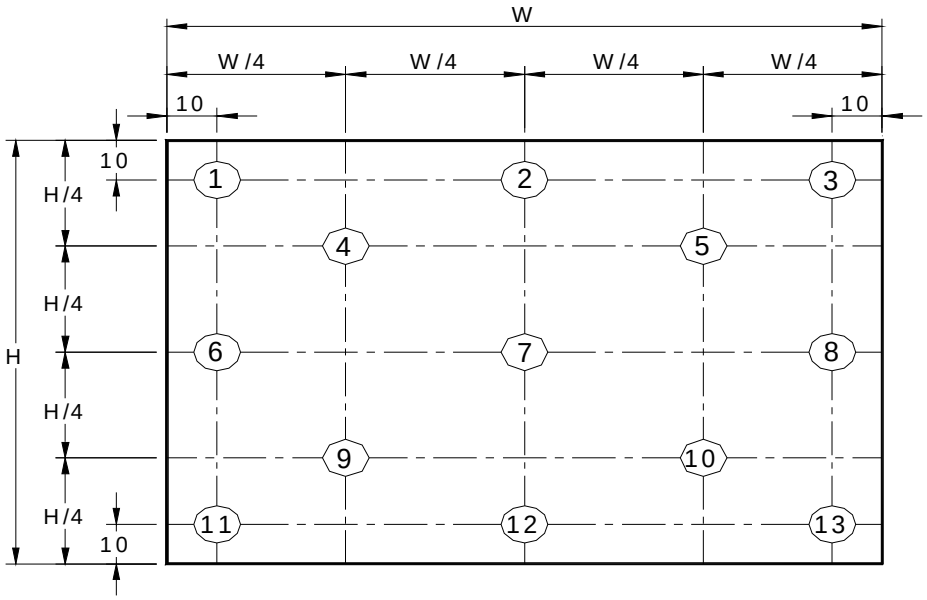
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
Luminance CCFL 6.5mA	[cd/m2]	5 points average	350	400	-	1,2,3
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	60 60	70 70	- -	2,7
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	40 50	60 60	- -	
Luminance Uniformity		5 Points			1.25	1
Luminance Uniformity		13 Points			2.0	
CR: Contrast Ratio			500	600	-	6
Cross talk	%				4	4
Response Time	[msec]	Rising	-	TBD		5
	[msec]	Falling	-	TBD		
	[msec]	Raising + Falling		8		
Color / Chromaticity Coordinates (CIE 1931)		Red x		TBD		2,7
		Red y		TBD		
		Green x		TBD		
		Green y		TBD		
		Blue x		TBD		
		Blue y		TBD		
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	

Note 1: 5 points position (Display area : 367.20(H) x 229.50(V)mm)



Note 2: 13 points position



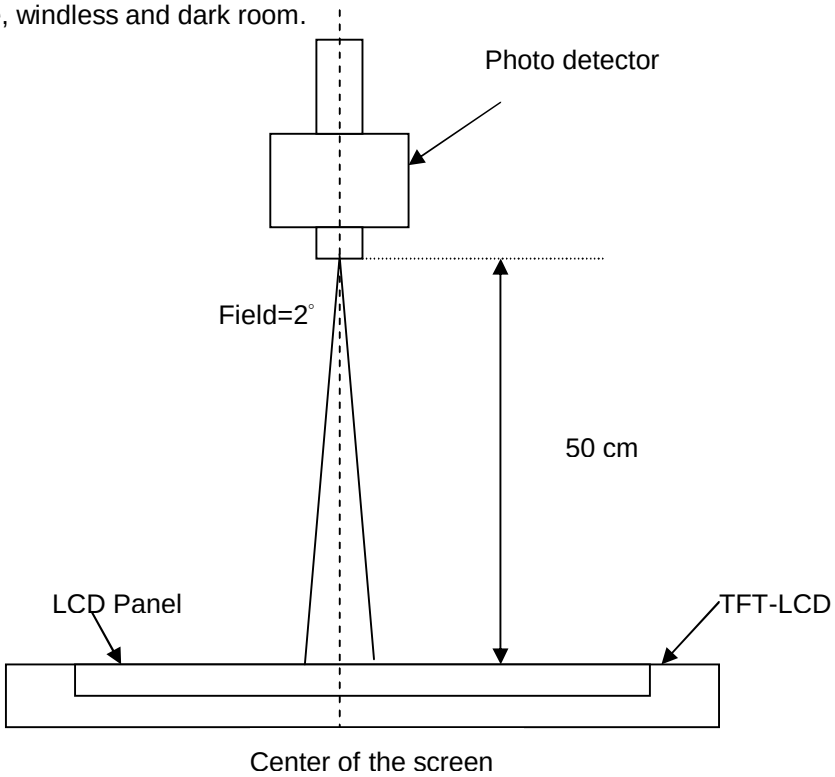
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



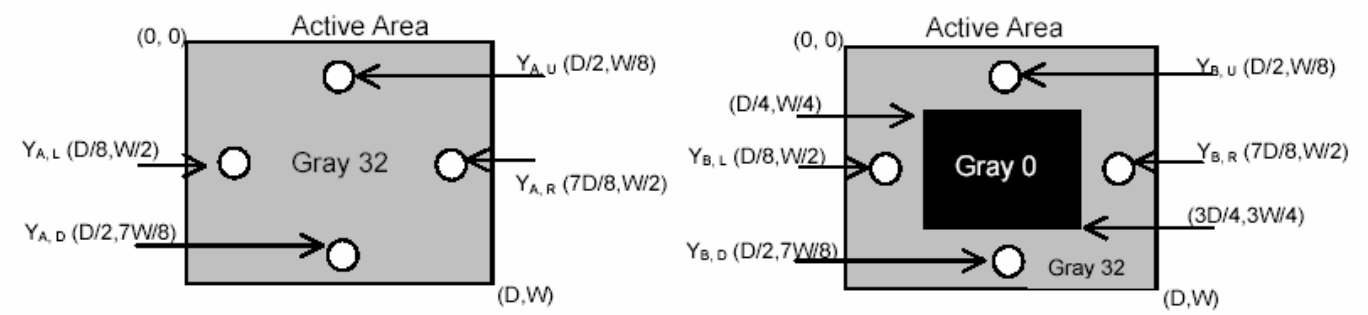
Note 5： Definition of Cross Talk (CT)

CT = | Y_B – Y_A | / Y_A × 100 (%)

Where

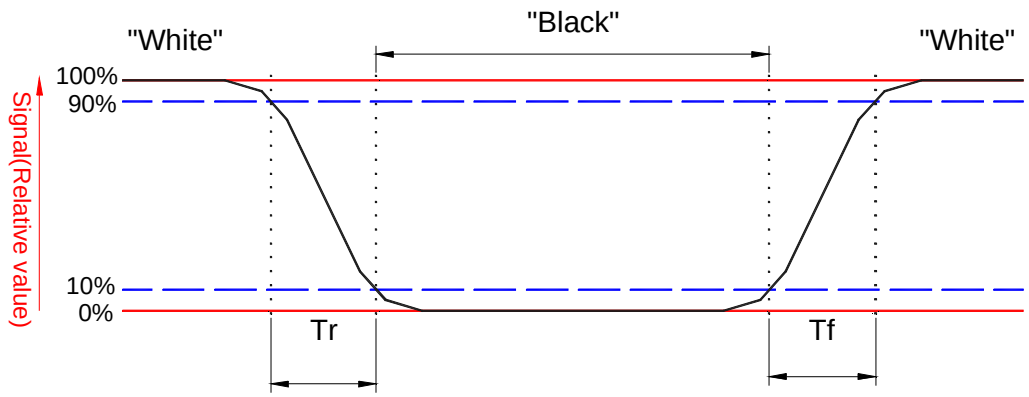
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



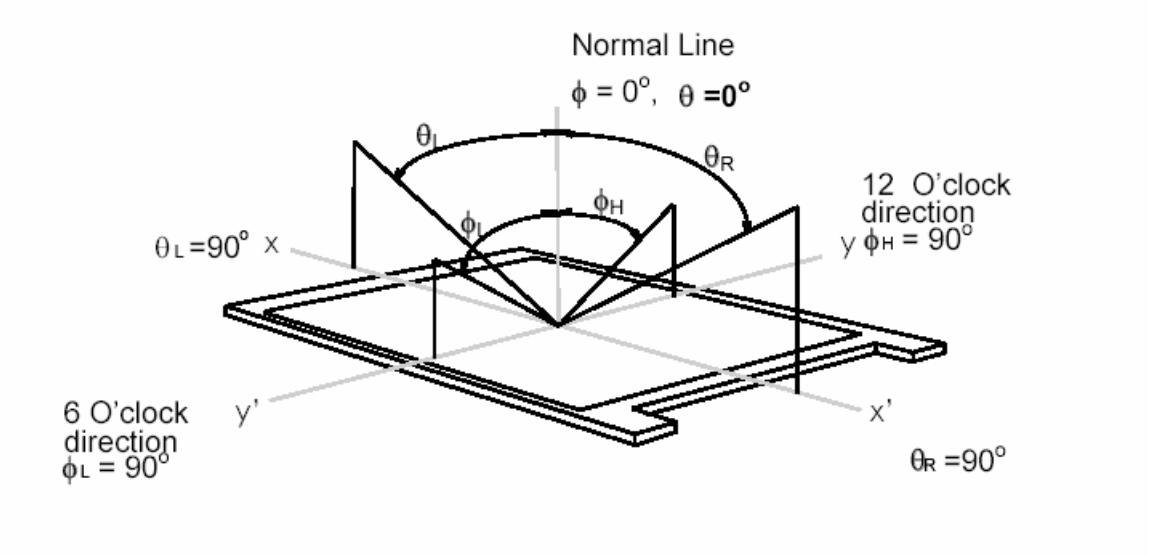
Note 6: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from“Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



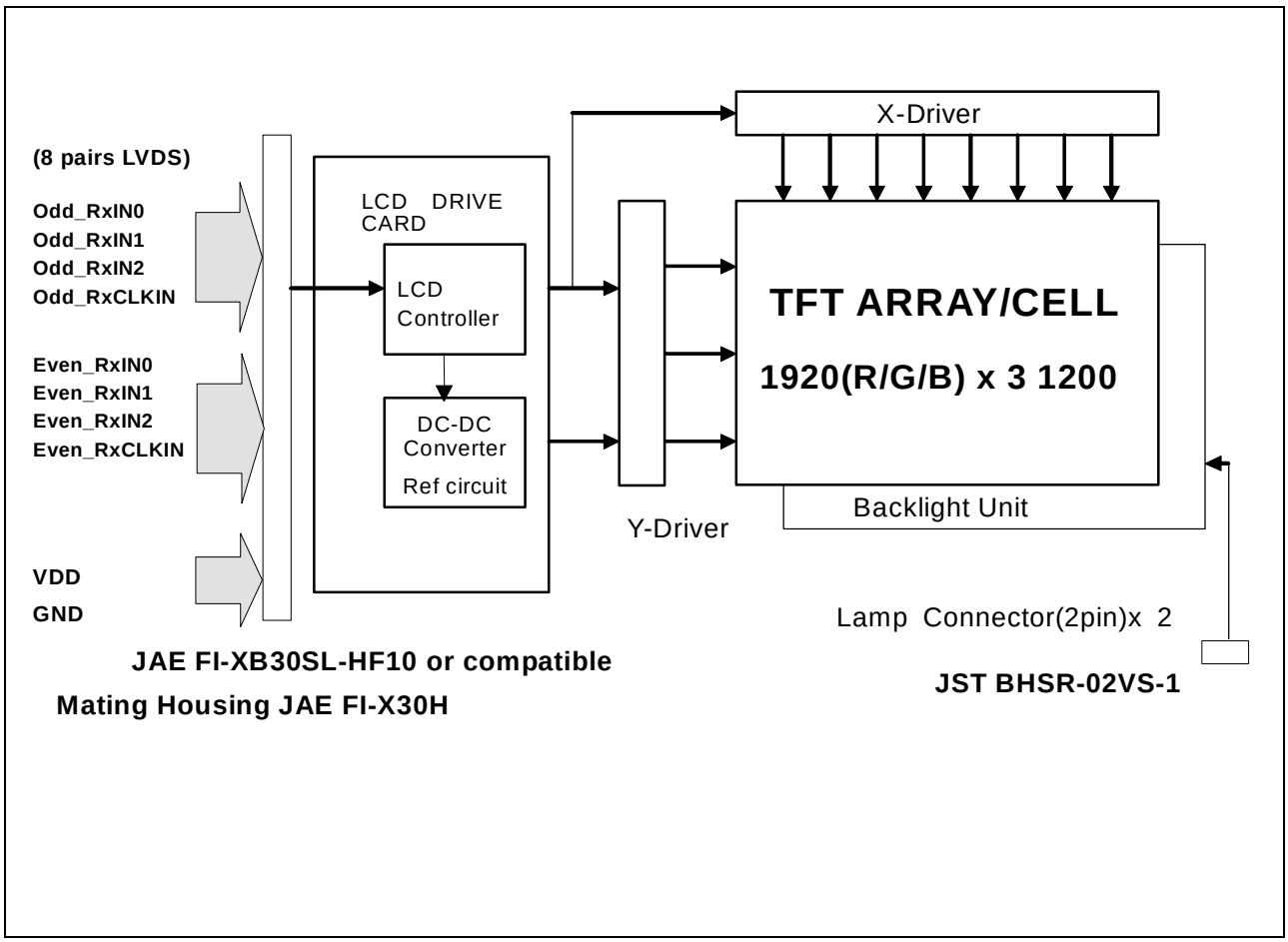
Note 7. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 17.0 inches wide Color TFT/LCD Module:



4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	-	6.5	[mA] rms	Note 1,2

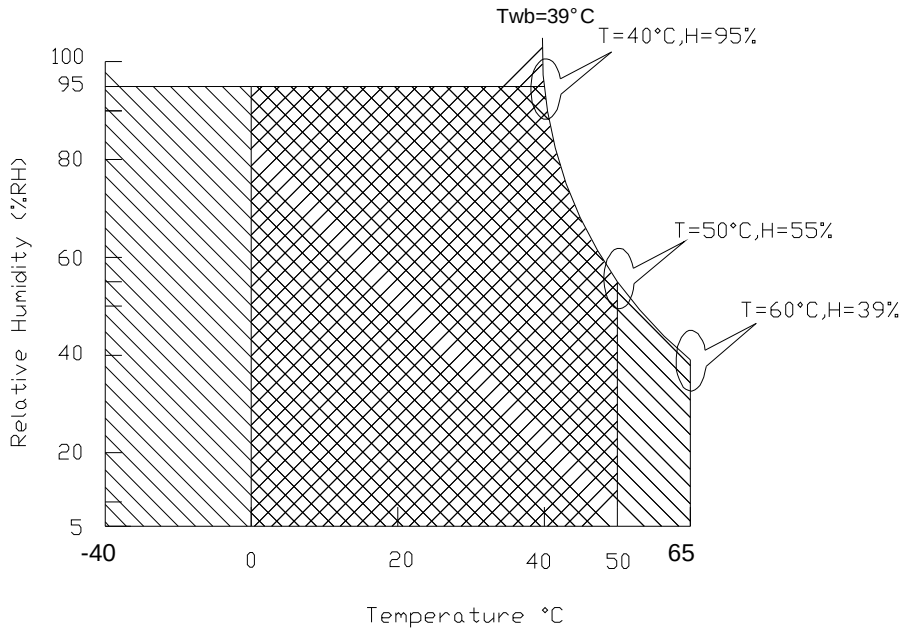
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: With in Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality perfermance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range Storage Range

5. Electrical characteristics

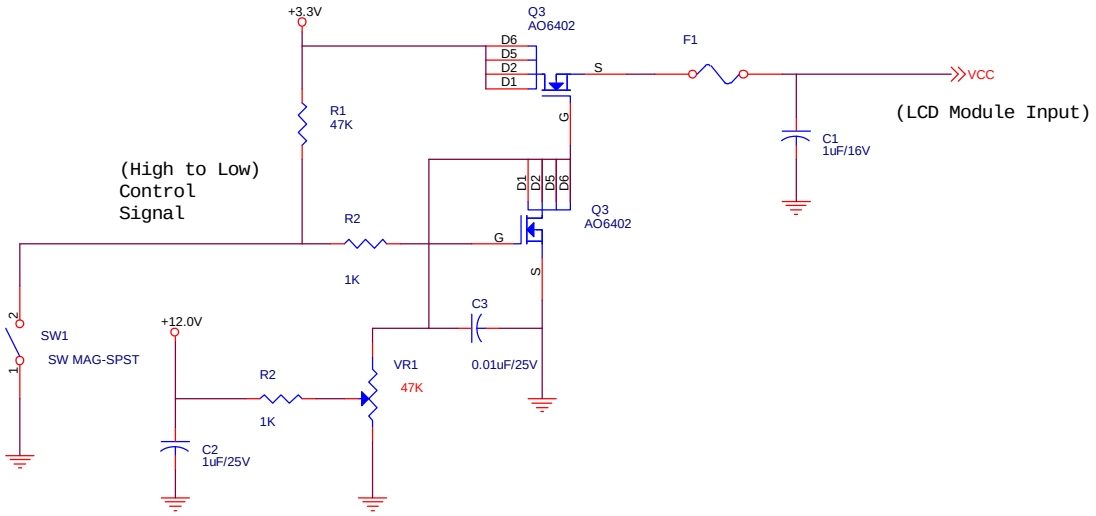
5.1 TFT LCD Module

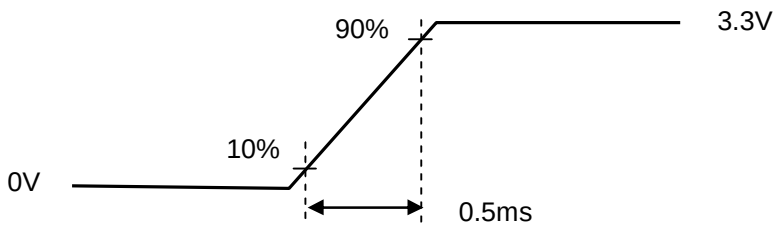
5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		2.5	3	[Watt	All White pattern
IDD	IDD Current		750		mA	Max:All Black Pattern
IRush	Inrush Current			TBD	mA	
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mV] p-p	

Note 1 : Measurement conditions:





Vin rising

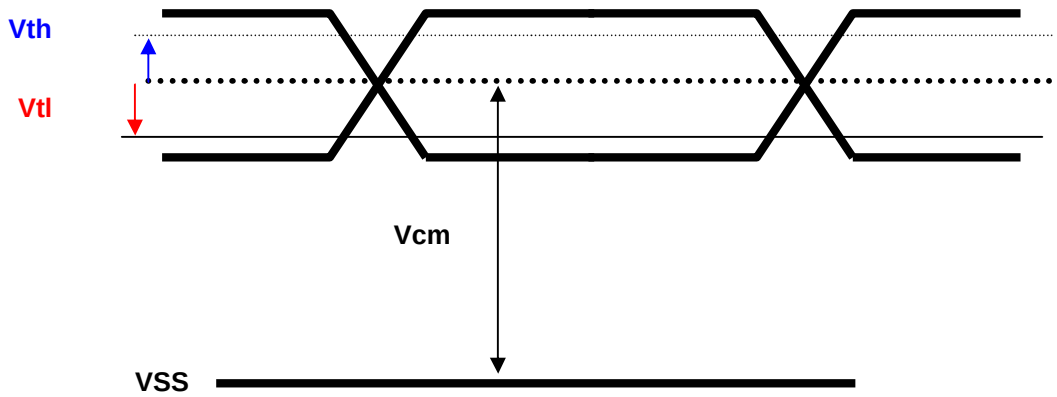
5.1.2 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

It is recommended to refer the specifications of **THC63LVDF84A(Thine Electronics Inc**.) in detail.Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	350	400	-	[cd/m^2]	(Ta=25℃)
CCFL current(ICCFL)	3.0	6.5	7.0	[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(FCCFL)	40	50	80	[KHz]	(Ta=25℃) Note 3,4
CCFL Ignition Voltage(Vs)		1360	1700	[Volt] rms	(Ta= 0℃) Note 5
CCFL Voltage (Reference) (VCCFL)	666	740	814	[Volt] rms	(Ta=25℃) Note 6
CCFL Power consumption (PCCFL)		4.81		[Watt]	(Ta=25℃) Note 6
CCFL Power consumption (2 lamp)	4	9.6	11.4	[Watt]	(Ta=25℃) Note 6
Set up Time			1	[Sec]	

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has “Duty Dimming”, if ICFL is less than 4mA.

Note 3: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

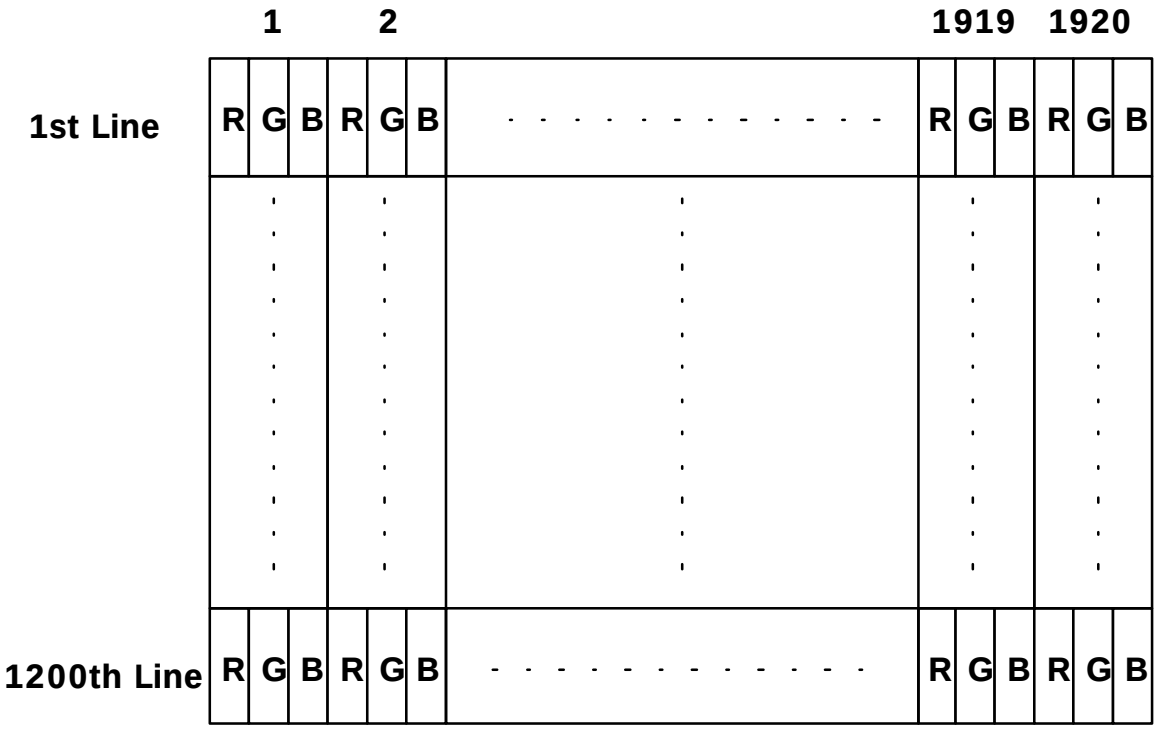
Note 5: CFL inverter should be able to give out a power that has a generating capacity of over 1,430 voltage. Lamp units need 1,400 voltage minimum for ignition.

Note 6: Calculator value for reference (ICCFL×VCCFL=PCCFL)

6. Signal Characteristic

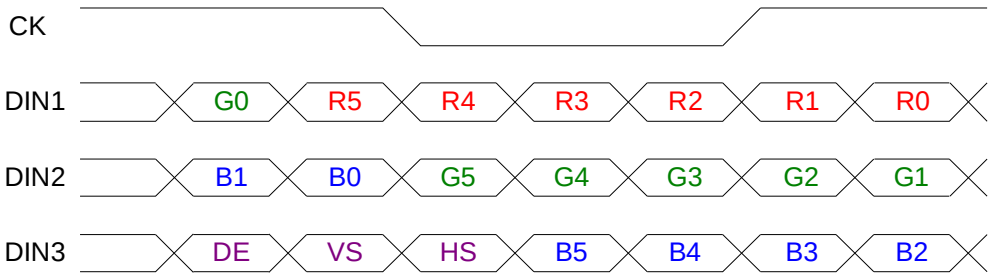
6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

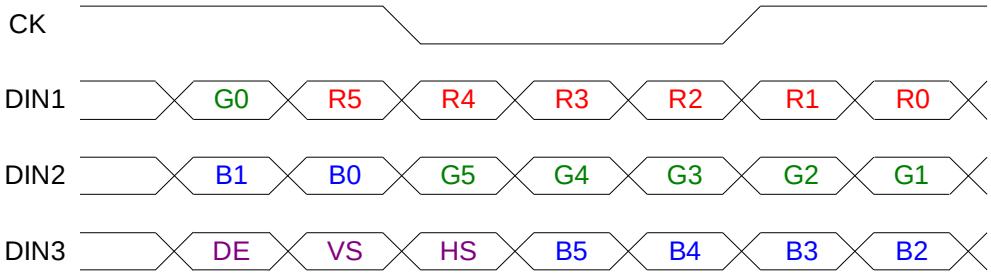


6.2 The input data format

ODD pair(1st pixel input)



Even pair(2nd pixel input)



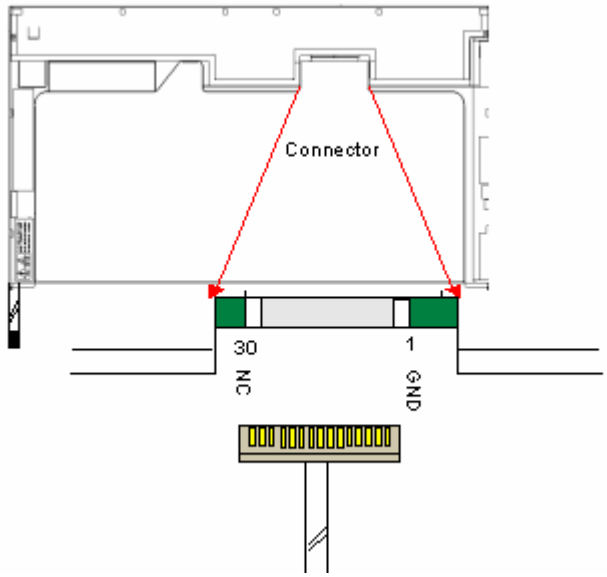
Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) **Red-pixel Data**	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) **Green-pixel Data**	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) **Blue-pixel Data**	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	**Data Clock**	The typical frequency is 48.2 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DE	**Display Timing**	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VS	**Vertical Sync**	The signal is synchronized to -DTCLK .
HS	**Horizontal Sync**	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

6.3 Signal Description

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Pin no	Symbol	Function	Etc.
1	GND	Ground	
2	VDD	Power supply ,3.3 V (typical)	
3	VDD	Power supply ,3.3 V (typical)	
4	V_{EDID}	DDC 3.3V power	
5	NC	No Connection (Reserved for AUO) test	
6	CLK_{EDID}	DDC Clock	
7	$Data_{EDID}$	DDC data	
8	Odd_RxIN0-	-LVDS differential data input	
9	Odd_RxIN0+	+LVDS differential data input	
10	GND	Ground	
11	Odd_RxIN1-	-LVDS differential data input	
12	Odd_RxIN1+	+LVDS differential data input	
13	GND	Ground	
14	Odd_RxIN2-	-LVDS differential data input	
15	Odd_RxIN2+	+LVDS differential data input	
16	GND	Ground	
17	Odd_RxCLKIN-	-LVDS differential clock input	
18	Odd_RxCLKIN+	+LVDS differential clock input	
19	GND	Ground	
20	Even_RxIN0-	-LVDS differential data input	
21	Even_RxIN0+	+LVDS differential data input	
22	GND	Ground	
23	Even_RxIN1-	-LVDS differential data input	
24	Even_RxIN1+	+LVDS differential data input	
25	GND	Ground	
26	Even_RxIN2-	-LVDS differential data input	
27	Even_RxIN2+	+LVDS differential data input	
28	GND	Ground	
29	Even_RxCLKIN-	-LVDS differential clock input	
30	Even_RxCLKIN+	+LVDS differential clock input	



Note1: Start from right side

Note2: Please follow VESA standard.
Note3: Input signals shall be low or High-impedance when VDD is off.
Internal circuit of LVDS inputs are as following.
The module uses a 100ohm resistor between positive and negative data lines of each receiver input

6.4 Interface Timing

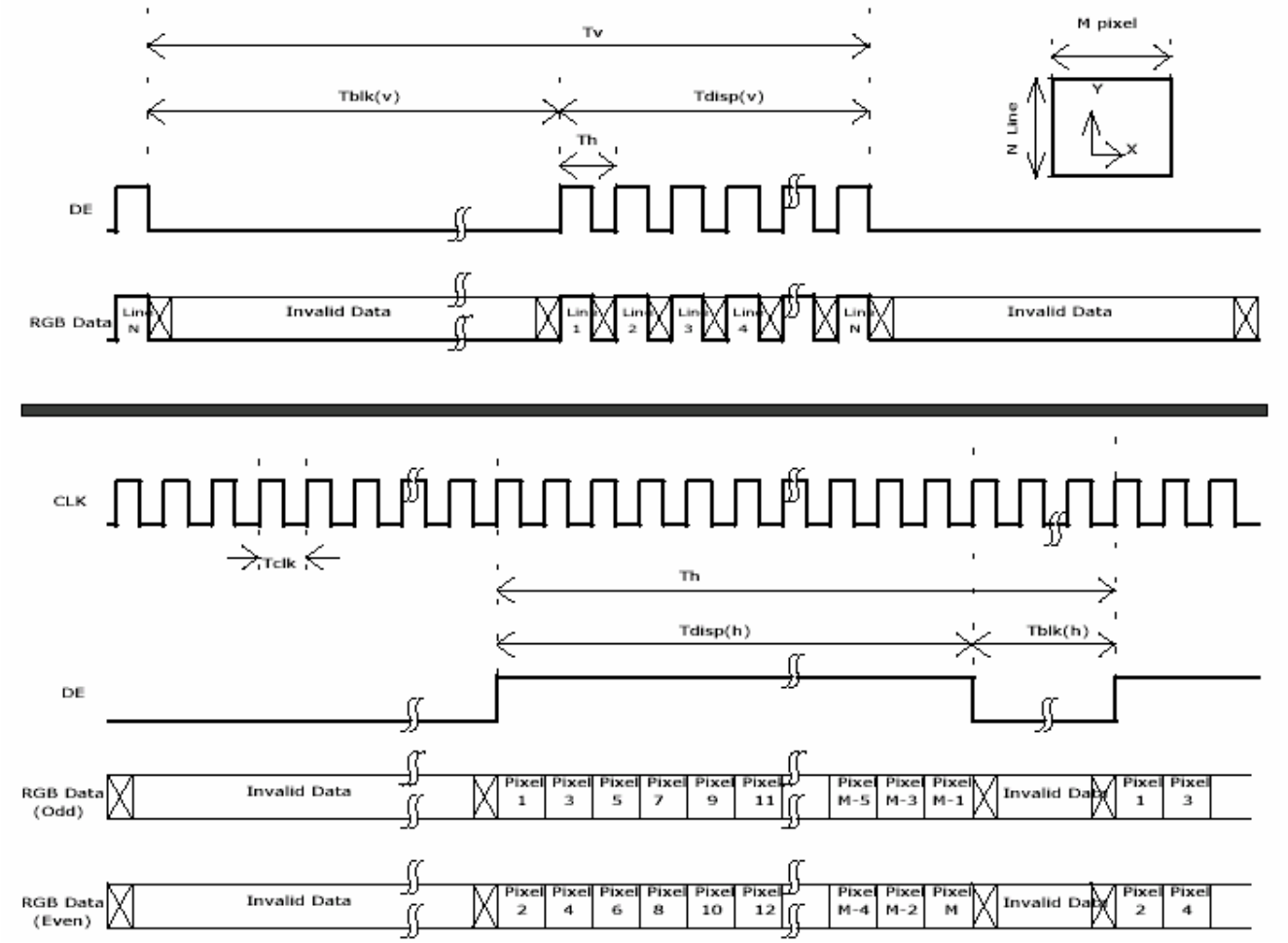
6.4.1 Timing Characteristics

Basically, interface timings should match the 1920x1200 manufacturing guide line timing.

Signal	Item	Symbol	Min	Typ	Max	Unit
Vertical section	Period	Tv	1208	1250	2048	Th
	Active	Tdisp(V)	1200	1200	1200	Th
	Blanking	Tblk(V)	8	50	848	Th
Horizontal Section	Period	Th	1000	1050	2048	Tclk
	Active	Tdisp(H)	960	960	960	Tclk
	Blanking	Tblk(H)	40	90	1088	Tclk
Clock	Period	Tclk	11.76	12.7		ns
	Frequency@60Hz	Freq		78.75	85	MHz

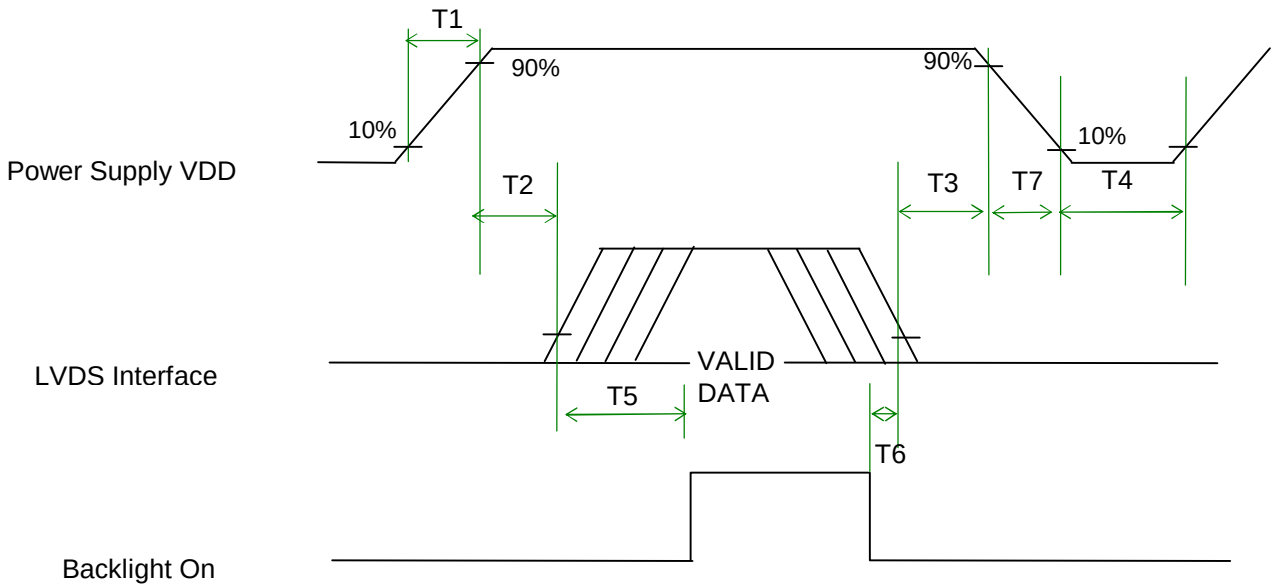
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SL-HF10 or compatible
Mating Housing/Part Number	FI-X30H
Mating Contact/Part Number	FI-XC3-1-15000

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage
3	Blue	Lamp High Voltage
4	Black	Lamp Low Voltage

8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 180 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

9. Reliability

Items	Required Conditions
Operating Life – High Temp.	Temp.= +50°C, Dynamic. 250 Hours, Humidity 20%
Operating Life – Low Temp.	Temp.= 0°C, Dynamic, 250 Hours, Humidity 20%
High Temp. Storage Life – Non-Operating	Temp.= +65°C, Non-Operating, 250 Hours, Humidity 20%
Low Temp. Storage Life – Non-Operating	Temp.= -40°C, Non-Operating, 250 Hours
High Temp & High Humidity Operating Life	Temp.=+40°C,Dynamic,Humidity 95%(Non-Condensing), 250 Hours
Shock – Non-Operating	180g, 2.0 ms, Half Sine Wave
Vibration – Non-Operating	Random vibration, 1.5 G zero-to-peak, 10 to 500 Hz, 30 mins in each of three mutually perpendicular axes
Temp. Cycle – Operating	0℃ to +40℃ ,Ramp< 20℃ /min, Duration at Temp. = 30 min, Test Cycles =160
Temp. Cycle – Non-Operating	-40°C to +65°C, Ramp ≤20°C/min, Duration at Temp. = 30min, Test Cycles = 50
ESD	Contact : ±8KV/ operation Air : ±15KV / operation
Room temperature Test	25℃, 2000hours, Operating with loop pattern

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

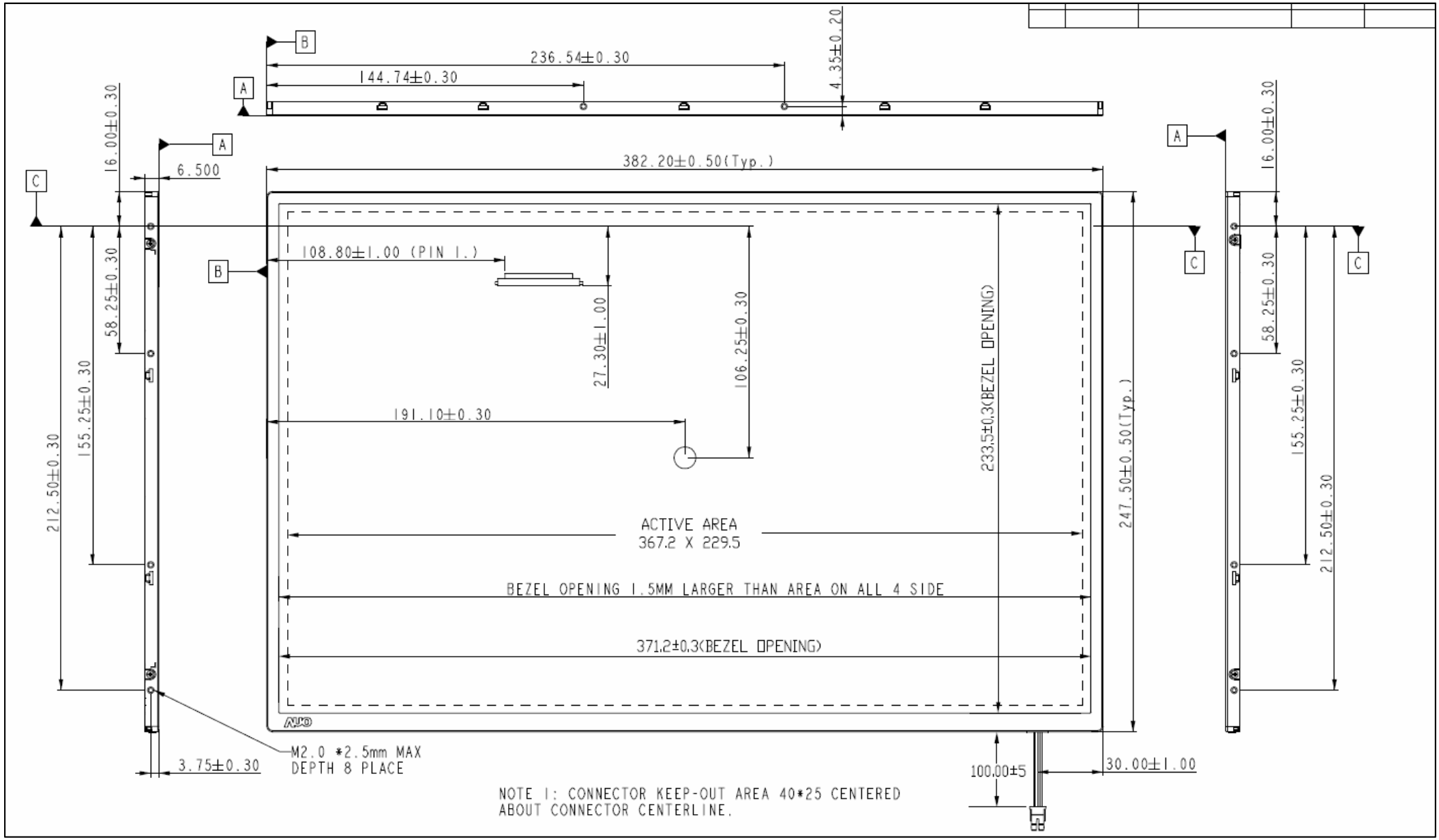
. Self-recoverable. No hardware failures.

Note2: CCFL Life time: 10,000 hours minimum under normal module usage.

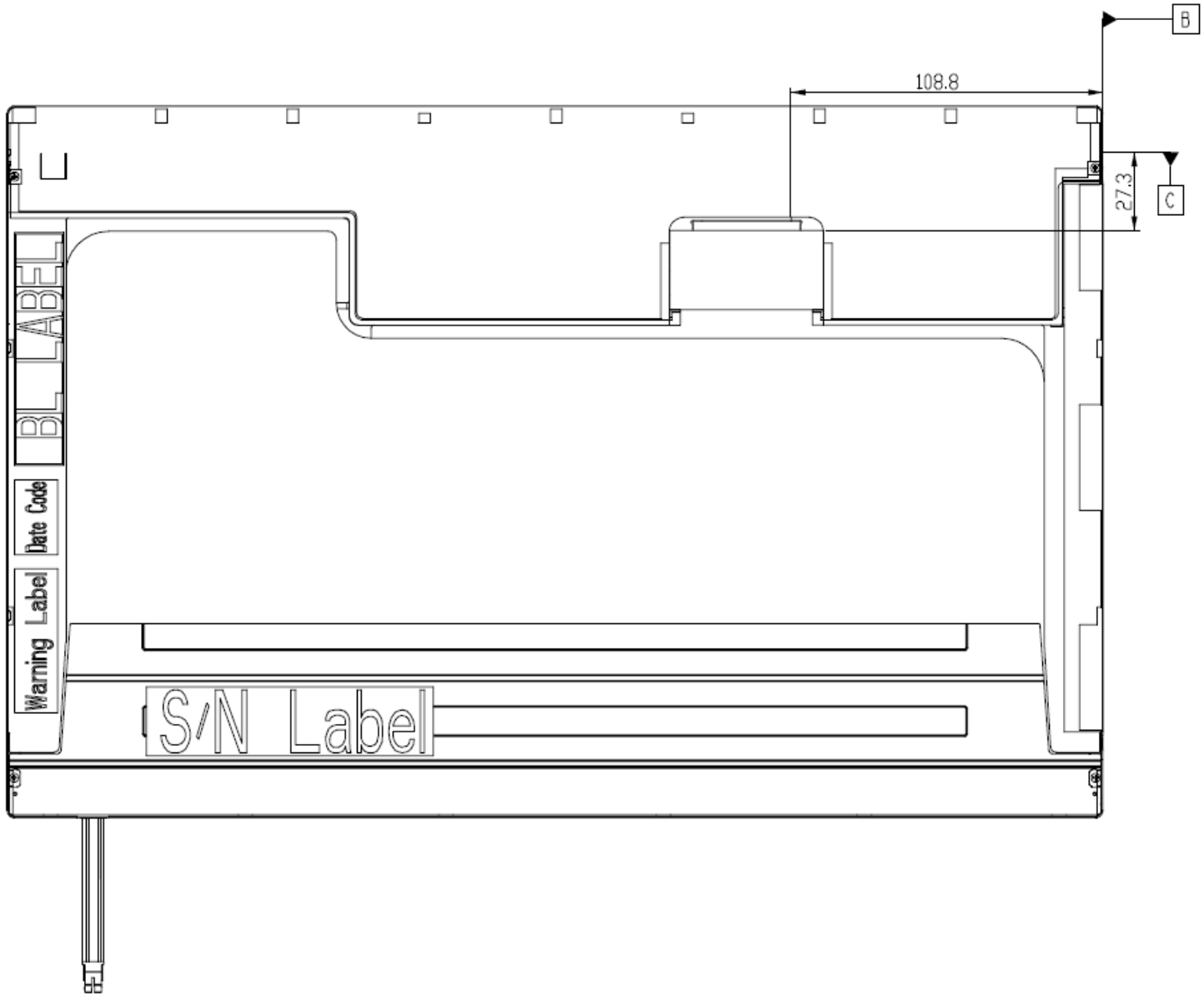
Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

10. Mechanical Characteristics

10.1 LCM Outline Dimension(Front View)



10.2 LCM Outline Dimension(Rear View)



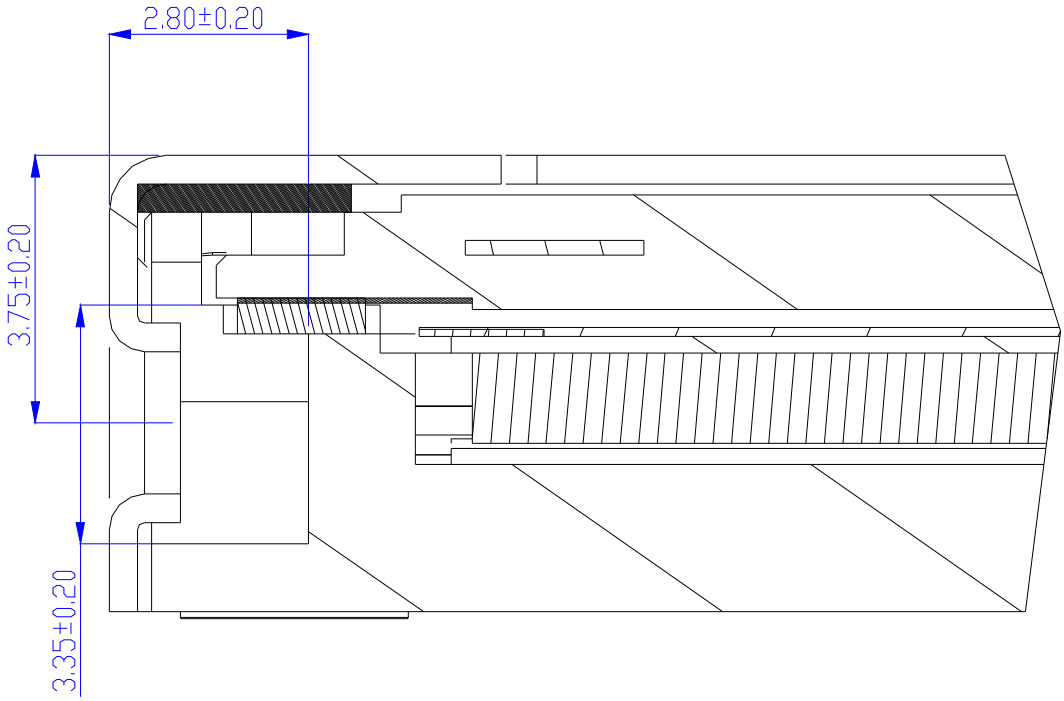
10.3 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface =2.6 mm (See drawing)

Screw hole center location, from front surface = 3.75 ± 0.2mm (See drawing)

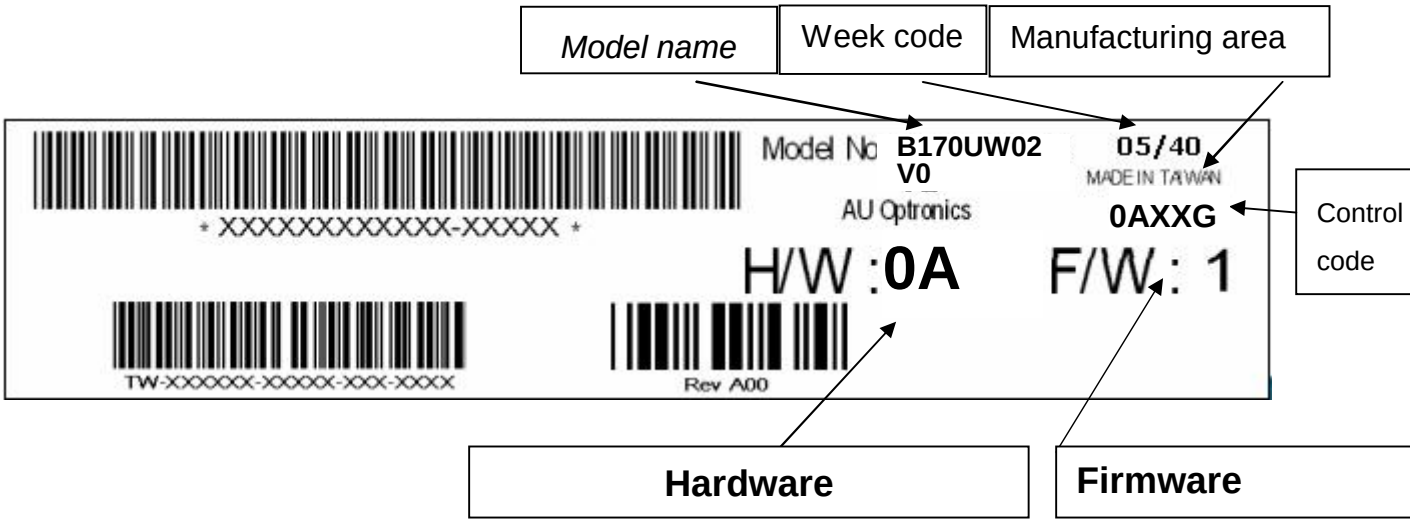
Screw maximum length = 2.3 mm (See drawing)

Screw Torque: Maximum2.5 kgzf-cm

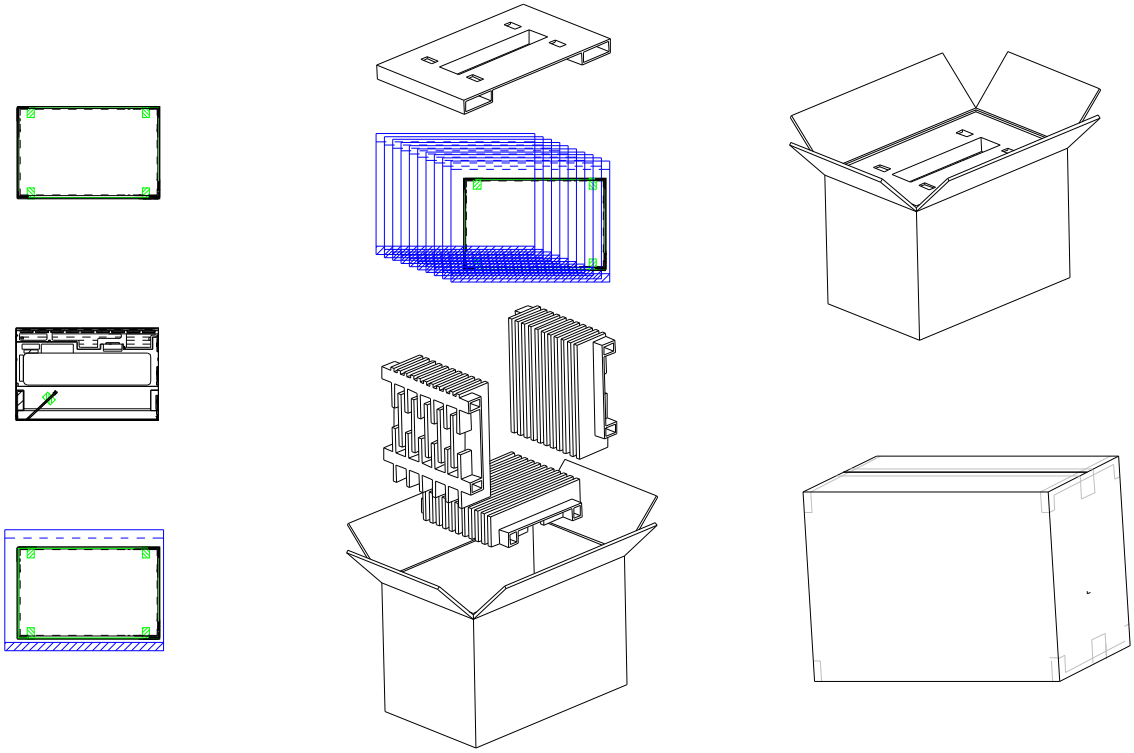


11. Shipping and Package

11.1 Shipping Label Format



11.2. Carton package



12. Appendix: EDID description

	B170UW02 V0 EDID Code				
Address	**FUNCTION**	**Value**	**Value**	**Value**	**Note**
HEX		**HEX**	**BIN**	**DEC**	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	88	10001000	136	
0B	hex, LSB first	20	00100000	32	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	01	00000001	1	
11	Year of manufacture	10	00010000	16	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	03	00000011	3	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	80	10000000	128	
15	**Max H image size** *(rounded to cm)*	25	00100101	37	
16	**Max V image size** *(rounded to cm)*	17	00010111	23	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	0A	00001010	10	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	07	00000111	7	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	E5	11100101	229	
1B	Red x **(Upper 8 bits)**	97	10010111	151	
1C	Red y/ highER 8 bits	57	01010111	87	
1D	Green x	4F	01001111	79	
1E	Green y	8C	10001100	140	
1F	Blue x	27	00100111	39	
20	Blue y	22	00100010	34	
21	White x	50	01010000	80	
22	White y	54	01010100	84	

23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	54	01010100	84	
37	Pixel Clock/10000 USB	3D	00111101	61	
38	Horz active **Lower 8bits**	80	10000000	128	
39	Horz blanking **Lower 8bits**	A0	10100000	160	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	70	01110000	112	
3B	Vertical Active **Lower 8bits**	B0	10110000	176	
3C	Vertical Blanking **Lower 8bits**	17	00010111	23	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40	01000000	64	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	36	00110110	54	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	6F	01101111	111	
43	Vertical Image Size **Lower 8bits**	E5	11100101	229	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	

4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	37	00110111	55	7
74	Manufacture P/N	30	00110000	48	0

75	Manufacture P/N	55	01010101	85	U
76	Manufacture P/N	57	01010111	87	W
77	Manufacture P/N	30	00110000	48	0
78	Manufacture P/N	32	00110010	50	2
79	Manufacture P/N	20	00100000	32	
7A	Manufacture P/N	56	01010110	86	V
7B	Manufacture P/N	30	00110000	48	0
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	88	10001000	136	
			SUM	6400	
			SUM to HEX	1900	