



# **SPECIFICATION FOR APPROVAL**

(	) Pre	liminary	Speci	fication
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Title

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BUYER	HP		SUPPLIER	LG Display Co., Ltd.
MODEL		1	*MODEL	LP173WF1

BUYER	HP
MODEL	

\*When you obtain standard approval, please use the above model name without suffix

TLB2

17.3" FHD TFT LCD

Suffix

	APPROVED BY	SIGNATURE
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	/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE				
H.S. Kim / S.Manager					
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Product Engineering Dept. LG Display Co., Ltd					



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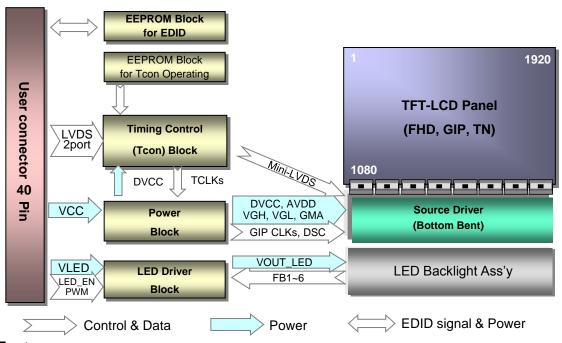
# **RECORD OF REVISIONS**

Revision No	Revision Date	Page	Description	EDID ver
0.0	Oct. 07. 2009	-	First Draft	-
0.1	Nov.09.2009	32-34	Updated EDID	0.0
0.2	Mar.02.2010	4	Update General Features	
		6	Update Electrical characteristics	
		14-15	Update Optical Specification	
		19	Update rear view Label	
		32-34	Update EDID	0.1
1.0	Mar.02.2010	-	Final Specification	1.0



#### 1. General Description

The LP173WF1 is a Color Active Matrix Liquid Crystal Display with an integral LED backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally white mode. This TFT-LCD has 17.3 inches diagonally measured active display area with FHD resolution (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into Red, Green and Blue subpixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors. The LP173WF1 has been designed to apply the interface method that enables low power, high speed, low EMI. The LP173WF1 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the subpixels, the LP173WF1 characteristics provide an excellent flat display for office automation products such as Notebook PC.



#### **General Features**

Active Screen Size	17.3 inches diagonal
Outline Dimension	398.1(H, Typ.) × 232.8(V, Typ.) × 6.0(D, Max.) mm
Pixel Pitch	0.1989 X 0.1989 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels RGB strip arrangement
Color Depth	6-bit, 262,144 colors
Luminance, White	300 cd/m <sup>2</sup> (Typ., @ I <sub>LED</sub> =22mA)
Power Consumption	Total 8.5W(Typ.) Logic : 2.0W (Typ.@ Mosaic), B/L : 6.5W (Typ.@ VLED 12V )
Weight	580g (Max.)
Display Operating Mode	Transmissive mode, normally white
Surface Treatment	Anti Glare treatment (3H) of the front Polarizer
RoHS Compliance	Yes
BFR/PVC/As Free	Yes for all



### 2. Absolute Maximum Ratings

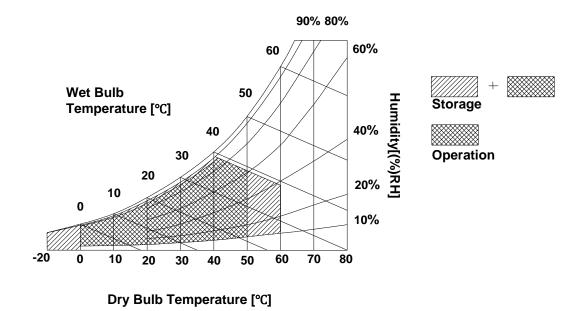
The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

**Table 1. ABSOLUTE MAXIMUM RATINGS** 

Parameter	Symbol	Val	ues	Units	Notes	
Farameter	Syllibol	Min	Max	Offics		
Power Input Voltage	VCC	-0.3	4.0	Vdc	at 25 ± 5°C	
Operating Temperature	Тор	0	50	°C	1	
Storage Temperature	Нѕт	-20	60	°C	1	
Operating Ambient Humidity	Нор	10	90	%RH	1	
Storage Humidity	Нѕт	10	90	%RH	1	

Note: 1. Temperature and relative humidity range are shown in the figure below.

Wet bulb temperature should be 39°C Max, and no condensation of water.





# 3. Electrical Specifications

### 3-1. Electrical Characteristics

The LP173WF1 requires two power inputs. The first logic is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second backlight is the input about LED BL.with LED Driver.

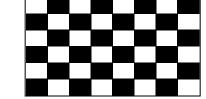
Table 2. ELECTRICAL CHARACTERISTICS

Danamatan.	Count of	Values				
Parameter	Symbol	Min	Тур	Max	Unit	Notes
LOGIC:						
Power Supply Input Voltage	Vcc	3.0	3.3	3.6	V	1
Power Supply Input Current	Icc	-	600	680	mA	2
Power Consumption	Pcc	-	1.98	2.24	W	2
Power Supply Inrush Current	ICC_P	-	770	900	mA	3
LVDS Impedance	ZLVDS	90	100	110	Ω	4
BACKLIGHT : ( with LED Driver)						
LED Power Input Voltage	VLED	7.0	12.0	21.0	V	5
LED Power Input Current	ILED	-	540	565	mA	6
LED Power Consumption	PLED	-	6.48	6.78	W	6
LED Power Inrush Current	ILED_P	-	450	550	mA	7
PWM Duty Ratio		5	-	100	%	8
PWM Jitter	-	0	-	0.2	%	9
PWM Impedance	Zpwm	20	40	60	kΩ	
PWM Frequency	FPWM	200	-	1000	Hz	10
PWM High Level Voltage	V <sub>PWM_H</sub>	3.0	-	5.3	V	
PWM Low Level Voltage	V <sub>PWM_L</sub>	0	-	0.3	V	
LED_EN Impedance	Zpwm	20	40	60	kΩ	
LED_EN High Voltage	VLED_EN_H	3.0	-	5.3	V	
LED_EN Low Voltage	VLED_EN_L	0	-	0.3	V	
Life Time		12,000	-	-	Hrs	11

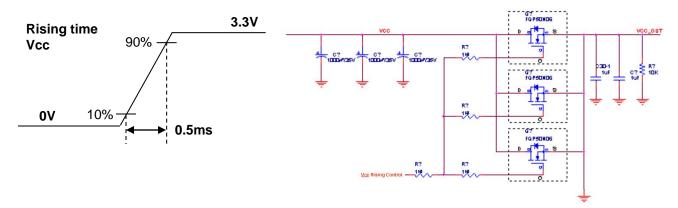


#### Note)

- 1. The measuring position is the connector of LCM and the test condition is under 25°C, fv = 60Hz, Black pattern.
- 2. The specified Icc current and power consumption are under the Vcc = 3.3V, 25°C, fv = 60Hz condition whereas Mosaic pattern is displayed and fv is the frame frequency.

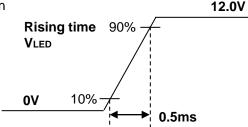


3. The below figures aire the measuring Vcc condition and the Vcc control block LGD used. The Vcc condition is same the minimum of T1 at Power on sequence.



- 4. This impedance value is needed to proper display and measured form LVDS Tx to the mating connector.
- 5. The measuring position is the connector of LCM and the test conditions are under 25°C.
- 6. The current and power consumption with LED Driver are under the VLED = 12.0V, 25°C, Dimming of Max luminance whereas White pattern is displayed and fv is the frame frequency.
- 7. The below figures are the measuring VLED condition and the VLED control block LGD used.

VLED control block is same with Vcc control block.



- The operation of LED Driver below minimum dimming ratio may cause flickering or reliability issue.
- 9. If Jitter of PWM is bigger than maximum. It may cause flickering.
- 10. This Spec. is not effective at 100% dimming ratio as an exception because it has DC level equivalent to 0Hz. In spite of acceptable range as defined, the PWM Frequency should be fixed and stable for more consistent brightness control at any specific level desired.
- 11. The life time is determined as the time at which brightness of LCD is 50% compare to that of minimum value specified in table 8. under general user condition.



## 3-2. Interface Connections

This LCD employs one interface connections, a 40 pin connector is used for the module electronics interface.

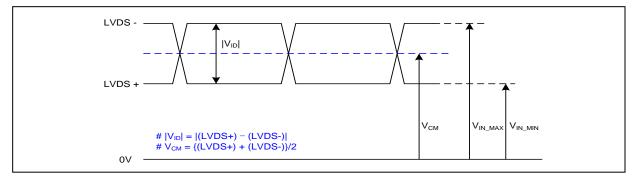
Table 3. MODULE CONNECTOR PIN CONFIGURATION (CN1)

1	Pin	Symbol	Description	Notes
2	1	NC	No Connection (Reserved)	[Interface Chip]
V EEDID   DDC 3.3V power   Sincluding LVDS Receiver.	2	VDD	Power Supply (3.3V typ.)	1. LCD :
5 NC No Connection (Reserved) 6 CLK EEDLD DDC clock / SMBus clock 7 DATA EEDLD DDC data / SMBus clock 8 Odd Rin0- 9 Odd Rin0- 1-VDS differential data input (R0-R5,G0) 9 Odd Rin0- 1-VDS differential data input (G1-G5,B0-B1) 10 GND Ground 11 Odd Rin1- 12 Odd Rin1- 14 Odd Rin1- 15 Odd Rin2- 16 GND Ground 17 Odd CliN1- 17 Odd CliN1- 18 Odd CliN1- 19 Odd CliN1- 19 Odd CliN1- 19 Odd CliN1- 10 Connectori 10 Odd Rin1- 11 Odd Rin1- 11 Odd Rin1- 11 Odd Rin1- 12 Odd Rin1- 14 Odd Rin1- 15 Odd Rin1- 16 GND Ground 17 Odd CliN1- 17 Odd CliN1- 18 Odd CliN1- 19 GND Ground 17 Odd CliN1- 18 Odd CliN1- 19 GND No Connection 20 Even Rin0- 10 LVDS differential data input (R0-R5,G0) 21 Even Rin0- 22 GND Ground 23 Even Rin1- 24 Even Rin1- 25 GND Ground 26 Even Rin1- 27 Even Rin2- 28 Even Rin1- 29 Even CliN1- 29 Even CliN1- 20 Even CliN1- 20 Even CliN1- 21 LVDS differential data input (B2-B5,HS,VS,DE) 21 Even Rin2- 22 Even Rin2- 23 Even Rin1- 24 Even Rin2- 25 GND Ground 26 Even Rin2- 27 Even Rin2- 28 Even Rin2- 29 Even CliN1- 20 Even CliN1- 20 Even CliN1- 21 ED power return 21 GND 22 Even CliN1- 23 Even CliN1- 24 ED power return 25 GND 26 Even CliN1- 27 Even CliN1- 28 GND 29 Even CliN1- 29 Even CliN1- 20 Even CliN1- 20 ED power return 21 GND 22 Even CliN1- 23 Even CliN1- 24 NC 25 GND 26 ED power return 27 GND 28 GND 29 Even CliN1- 29 Even CliN1- 20 ED power return 20 GND 21 ED power return 21 GND 22 ED power return 23 GND 24 ED power return 25 GND 26 ED power return 26 GND 27 NC 28 GND 28 EVEN Rin2- 29 EVEN CliN1- 20 ED Backlight Power (7V-21V) 29 EVEN CliN1- 20 ED Backlight Power (7V-21V) 20 ED Backlight Power (7V-21V) 20 ED Backlight Power (7V-21V) 21 ED Backlight Power (7V-21V) 21 EVEN END EVEN	3	VDD	Power Supply (3.3V typ.)	
CLK EEDID   DDC clock / SMBus clock   Pin to Pin compatible with LVDS	4	V EEDID	DDC 3.3V power	S
6 CLK EEDID DDC clock / SMBus clock 7 DATA EEDLD DDC data / SMBus data 8 Odd Rino- 9 Odd Rino- 1-VDS differential data input (R0-R5,G0) 9 Odd Rino- 1-VDS differential data input (R0-R5,G0) 10 GND Ground 11 Odd_Rin1- 1- LVDS differential data input (G1-G5,B0-B1) 12 Odd_Rin1+ 1- LVDS differential data input (G1-G5,B0-B1) 13 GND Ground 14 Odd_Rin2- 1- LVDS differential data input (B2-B5,HS,VS,DE) 15 Odd_Rin2- 1- LVDS differential data input (B2-B5,HS,VS,DE) 16 GND Ground 17 Odd_ClkiN- 17 Odd_ClkiN- 19 GND 20 Even Rin0- 20 Even Rin0- 21 Even Rin0+ 22 GND Ground 23 Even Rin1- 24 Even Rin1+ 25 LVDS differential data input (R0-R5,G0) 26 Even Rin1- 27 Even Rin1- 28 GND 30 Ground 31 GND 31 Ground 32 Even Rin1- 33 GND 34 NC 35 GND 36 Ground 36 Even ClkiN- 37 Even ClkiN- 4- LVDS differential data input (B2-B5,HS,VS,DE) 38 GND 39 Even ClkiN- 4- LVDS differential data input (B2-B5,HS,VS,DE) 39 Even ClkiN- 4- LVDS differential data input (B2-B5,HS,VS,DE) 30 Even ClkiN- 4- LVDS differential data input (B2-B5,HS,VS,DE) 31 GND 32 Even Rin2- 4- LVDS differential data input (B2-B5,HS,VS,DE) 33 GND 44 D 40 1 40 1 40 1 40 1 40 1 40 1 40 1 40 1	5	NC	No Connection (Reserved)	-
B		CLK EEDID	DDC clock / SMBus clock	•
9	7	DATA EEDLD	DDC data / SMBus data	* Pin to Pin compatible with LVDS
9	8	Odd_Rin0-	- LVDS differential data input (R0-R5,G0)	[Comparied]
10   GND   Ground   CVDS differential data input (G1-G5,B0-B1)   CVDS differential data input (G2-B5,HS,VS,DE)   CVDS differential data input (G2-G5,G0)   CVDS differential data input (G1-G5,G0)   CVDS differential data input (G1-G5,G0)   CVDS differential data input (G1-G5,G0-B1)   CVDS differential dock input   CVDS different	9	Odd_Rin0+		
11 Odd_Rin1+ LVDS differential data input (G1-G5,B0-B1) 12 Odd_Rin1+ LVDS differential data input (G1-G5,B0-B1) 13 GND Ground 14 Odd_Rin2+ LVDS differential data input (B2-B5,HS,VS,DE) 15 Odd_Rin2+ LVDS differential data input (B2-B5,HS,VS,DE) 16 GND Ground 17 Odd_CiklN- LVDS differential clock input 18 Odd_CiklN+ LVDS differential clock input 19 GND No Connection 20 Even Rin0- LVDS differential data input (R0-R5,G0) 21 Even Rin0+ LVDS differential data input (R0-R5,G0) 22 GND Ground 23 Even Rin1- LVDS differential data input (G1-G5,B0-B1) 24 Even Rin1+ LVDS differential data input (G1-G5,B0-B1) 25 GND 26 Even Rin2- LVDS differential data input (G1-G5,B0-B1) 27 Even Rin2+ LVDS differential data input (B2-B5,HS,VS,DE) 28 GND Ground 29 Even CiklN- LVDS differential clock input 30 Even CiklN- LVDS differential clock input 31 GND LED power return 32 GND LED power return 33 GND LED power return 34 NC No Connection (Reserved) 35 PWM PWM for luminance control 36 LED_EN LED Backlight Power (7V-21V) 39 VLED LED Backlight Power (7V-21V) 30 LED Backlight Power (7V-21V) 31 LED Backlight Power (7V-21V) 32 LED Backlight Power (7V-21V)	10	GND	Ground	
12	11	Odd_Rin1-	- LVDS differential data input (G1-G5,B0-B1)	
13	12			•
14	13	· · · · · · · · · · · · · · · · · · ·		
15 Odd_Rin2+ +LVDS differential data input (B2-B5,HS,VS,DE)  16 GND Ground  17 Odd_CikiNLVDS differential clock input  18 Odd_CikiN+ +LVDS differential clock input  19 GND No Connection  20 Even Rin0LVDS differential data input (R0-R5,G0)  21 Even Rin0+ +LVDS differential data input (R0-R5,G0)  22 GND Ground  23 Even Rin1- LVDS differential data input (R0-R5,G0)  24 Even Rin1+ +LVDS differential data input (G1-G5,B0-B1)  25 GND Ground  26 Even Rin2- LVDS differential data input (B2-B5,HS,VS,DE)  27 Even Rin2+ LVDS differential data input (B2-B5,HS,VS,DE)  28 GND Ground  29 Even CikiNLVDS differential clock input  30 Even CikiN+ +LVDS differential clock input  31 GND LED power return  32 GND LED power return  33 GND LED power return  34 NC No Connection (Reserved)  35 PWM PWM for luminance control  36 LED_EN LED Backlight Power (7V-21V)  39 VLED LED Backlight Power (7V-21V)  39 VLED LED Backlight Power (7V-21V)	14		- LVDS differential data input (B2-B5,HS,VS,DE)	
16    GND   Ground   17    Odd_ClklN-	15	Odd_Rin2+	· · · · · · · · · · · · · · · · · · ·	or equivalent
17 Odd_ClkiN LVDS differential clock input 18 Odd_ClkiN+ + LVDS differential clock input 19 GND No Connection 20 Even Rin0 LVDS differential data input (R0-R5,G0) 21 Even Rin0+ + LVDS differential data input (R0-R5,G0) 22 GND Ground 23 Even Rin1 LVDS differential data input (G1-G5,B0-B1) 24 Even Rin1+ + LVDS differential data input (G1-G5,B0-B1) 25 GND Ground 26 Even Rin2 LVDS differential data input (B2-B5,HS,VS,DE) 27 Even Rin2+ + LVDS differential data input (B2-B5,HS,VS,DE) 28 GND Ground 29 Even ClkiN LVDS differential clock input 30 Even ClkiN+ + LVDS differential clock input 31 GND LED power return 32 GND LED power return 33 GND LED power return 34 NC No Connection (Reserved) 35 PWM PWM for luminance control 36 LED_EN LED Backlight Power (7V-21V) 39 VLED LED Backlight Power (7V-21V) 39 VLED LED Backlight Power (7V-21V)	16	· · · · · · · · · · · · · · · · · · ·		
18 Odd_ClklN+ + LVDS differential clock input 19 GND No Connection 20 Even Rin0 LVDS differential data input (R0-R5,G0) 21 Even Rin0+ + LVDS differential data input (R0-R5,G0) 22 GND Ground 23 Even Rin1 LVDS differential data input (G1-G5,B0-B1) 24 Even Rin1+ + LVDS differential data input (G1-G5,B0-B1) 25 GND Ground 26 Even Rin2 LVDS differential data input (B2-B5,HS,VS,DE) 27 Even Rin2- + LVDS differential data input (B2-B5,HS,VS,DE) 28 GND Ground 29 Even ClklN+ + LVDS differential clock input 30 Even ClklN+ + LVDS differential clock input 31 GND LED power return 32 GND LED power return 33 GND LED power return 34 NC No Connection (Reserved) 35 PWM PWM for luminance control 36 LED_EN LED Backlight On/Off 37 NC No Connection (Reserved) 38 VLED LED Backlight Power (7V-21V) 39 VLED LED Backlight Power (7V-21V)	1 1		- LVDS differential clock input	[Connector pin arrangement]
19 GND No Connection 20 Even Rin0 LVDS differential data input (R0-R5,G0) 21 Even Rin0+ + LVDS differential data input (R0-R5,G0) 22 GND Ground 23 Even Rin1 LVDS differential data input (G1-G5,B0-B1) 24 Even Rin1+ + LVDS differential data input (G1-G5,B0-B1) 25 GND Ground 26 Even Rin2 LVDS differential data input (B2-B5,HS,VS,DE) 27 Even Rin2+ + LVDS differential data input (B2-B5,HS,VS,DE) 28 GND Ground 29 Even CikIN LVDS differential clock input 30 Even CikIN- + LVDS differential clock input 31 GND LED power return 32 GND LED power return 33 GND LED power return 34 NC No Connection (Reserved) 35 PWM PWM for luminance control 36 LED_EN LED Backlight On/Off 37 NC No Connection (Reserved) 38 VLED LED Backlight Power (7V-21V) 39 VLED LED Backlight Power (7V-21V)	1 }		<b> </b>	[
Even Rin0-   LVDS differential data input (R0-R5,G0)   21   Even Rin0+   LVDS differential data input (R0-R5,G0)   40   1   22   GND   Ground   23   Even Rin1-   LVDS differential data input (G1-G5,B0-B1)   24   Even Rin1+   LVDS differential data input (G1-G5,B0-B1)   25   GND   Ground   26   Even Rin2-   LVDS differential data input (B2-B5,HS,VS,DE)   27   Even Rin2+   LVDS differential data input (B2-B5,HS,VS,DE)   28   GND   Ground   29   Even ClkIN-   LVDS differential clock input   30   Even ClkIN+   LVDS differential clock input   31   GND   LED power return   32   GND   LED power return   33   GND   LED power return   34   NC   No Connection (Reserved)   35   PWM   PWM for luminance control   36   LED_EN   LED Backlight On/Off   37   NC   No Connection (Reserved)   No Connection (Reserved)   LED Backlight Power (7V-21V)   39   VLED   LED Backlight Power (7V-21V)   TED Backligh	1 )	<del></del>	<b> </b>	
21 Even Rin0+ + LVDS differential data input (R0-R5,G0) 22 GND Ground 23 Even Rin1 LVDS differential data input (G1-G5,B0-B1) 24 Even Rin1+ + LVDS differential data input (G1-G5,B0-B1) 25 GND Ground 26 Even Rin2 LVDS differential data input (B2-B5,HS,VS,DE) 27 Even Rin2+ + LVDS differential data input (B2-B5,HS,VS,DE) 28 GND Ground 29 Even ClkIN LVDS differential clock input 30 Even ClkIN+ + LVDS differential clock input 31 GND LED power return 32 GND LED power return 33 GND LED power return 34 NC No Connection (Reserved) 35 PWM PWM for luminance control 36 LED_EN LED Backlight On/Off 37 NC No Connection (Reserved) 38 VLED LED Backlight Power (7V-21V) 39 VLED LED Backlight Power (7V-21V)	1 )	Even Rin0-		
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24 Even Rin1+ + LVDS differential data input (G1-G5,B0-B1)  25 GND Ground  26 Even Rin2 LVDS differential data input (B2-B5,HS,VS,DE)  27 Even Rin2+ + LVDS differential data input (B2-B5,HS,VS,DE)  28 GND Ground  29 Even ClkIN LVDS differential clock input  30 Even ClkIN+ + LVDS differential clock input  31 GND LED power return  32 GND LED power return  33 GND LED power return  34 NC No Connection (Reserved)  35 PWM PWM for luminance control  36 LED_EN LED Backlight On/Off  37 NC No Connection (Reserved)  38 VLED LED Backlight Power (7V-21V)  39 VLED LED Backlight Power (7V-21V)	23	Even Rin1-	- LVDS differential data input (G1-G5,B0-B1)	
25 GND Ground 26 Even Rin2 LVDS differential data input (B2-B5,HS,VS,DE) 27 Even Rin2+ + LVDS differential data input (B2-B5,HS,VS,DE) 28 GND Ground 29 Even ClkIN LVDS differential clock input 30 Even ClkIN+ + LVDS differential clock input 31 GND LED power return 32 GND LED power return 33 GND LED power return 34 NC No Connection (Reserved) 35 PWM PWM for luminance control 36 LED_EN LED Backlight On/Off 37 NC No Connection (Reserved) 38 VLED LED Backlight Power (7V-21V) 39 VLED LED Backlight Power (7V-21V)	24	Even Rin1+		
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27 Even Rin2+ + LVDS differential data input (B2-B5,HS,VS,DE)  28 GND Ground  29 Even ClkIN LVDS differential clock input  30 Even ClkIN+ + LVDS differential clock input  31 GND LED power return  32 GND LED power return  33 GND LED power return  34 NC No Connection (Reserved)  35 PWM PWM for luminance control  36 LED_EN LED Backlight On/Off  37 NC No Connection (Reserved)  38 VLED LED Backlight Power (7V-21V)  LED Backlight Power (7V-21V)  LED Backlight Power (7V-21V)	1 )	Even Rin2-	- LVDS differential data input (B2-B5,HS,VS,DE)	
29 Even ClkIN LVDS differential clock input 30 Even ClkIN+ + LVDS differential clock input 31 GND LED power return 32 GND LED power return 33 GND LED power return 34 NC No Connection (Reserved) 35 PWM PWM for luminance control 36 LED_EN LED Backlight On/Off 37 NC No Connection (Reserved) 38 VLED LED Backlight Power (7V-21V) LED Backlight Power (7V-21V) LED Backlight Power (7V-21V)	27	Even Rin2+		
29 Even ClkIN LVDS differential clock input 30 Even ClkIN+ + LVDS differential clock input 31 GND LED power return 32 GND LED power return 33 GND LED power return 34 NC No Connection (Reserved) 35 PWM PWM for luminance control 36 LED_EN LED Backlight On/Off 37 NC No Connection (Reserved) 38 VLED LED Backlight Power (7V-21V) LED Backlight Power (7V-21V) LED Backlight Power (7V-21V)	28	GND	Ground	
30 Even ClkIN+ + LVDS differential clock input 31 GND LED power return 32 GND LED power return 33 GND LED power return 34 NC No Connection (Reserved) 35 PWM PWM for luminance control 36 LED_EN LED Backlight On/Off 37 NC No Connection (Reserved) 38 VLED LED Backlight Power (7V-21V) LED Backlight Power (7V-21V)	29	Even ClkIN-	- LVDS differential clock input	
31 GND LED power return 32 GND LED power return 33 GND LED power return 34 NC No Connection (Reserved) 35 PWM PWM for luminance control 36 LED_EN LED Backlight On/Off 37 NC No Connection (Reserved) 38 VLED LED Backlight Power (7V-21V) LED Backlight Power (7V-21V)	1 )	Even ClkIN+	<b> </b>	
32 GND LED power return  33 GND LED power return  34 NC No Connection (Reserved)  35 PWM PWM for luminance control  36 LED_EN LED Backlight On/Off  37 NC No Connection (Reserved)  38 VLED LED Backlight Power (7V-21V)  LED Backlight Power (7V-21V)		ĠŃĎ	LED power return	
33 GND LED power return  34 NC No Connection (Reserved)  35 PWM PWM for luminance control  36 LED_EN LED Backlight On/Off  37 NC No Connection (Reserved)  38 VLED LED Backlight Power (7V-21V)  LED Backlight Power (7V-21V)		ĞND		
34 NC No Connection (Reserved) 35 PWM PWM for luminance control 36 LED_EN LED Backlight On/Off 37 NC No Connection (Reserved) 38 VLED LED Backlight Power (7V-21V) LED Backlight Power (7V-21V)	1 1	ĠNĎ		
35 PWM PWM for luminance control 36 LED_EN LED Backlight On/Off 37 NC No Connection (Reserved) 38 VLED LED Backlight Power (7V-21V) 39 VLED LED Backlight Power (7V-21V)	1 )	NC		
36 LED_EN LED Backlight On/Off 37 NC No Connection (Reserved) 38 VLED LED Backlight Power (7V-21V) 39 VLED LED Backlight Power (7V-21V)	1 1		· · · · · · · · · · · · · · · · · · ·	
37 NC No Connection (Reserved) 38 VLED LED Backlight Power (7V-21V) 39 VLED LED Backlight Power (7V-21V)	1 1		<b> </b>	
38 VLED LED Backlight Power (7V-21V)  39 VLED LED Backlight Power (7V-21V)	1 1	· · · · · · · · · <del>· ·</del> · · · · · · ·	{ · · · · · · · · · · · · · · · · · · ·	
39 VLED LED Backlight Power (7V-21V)	1 1			
I FD Deal-Bak Dames (71/ 041/)	1 }		, ,	
'	40	VLED	LED Backlight Power (7V-21V)	



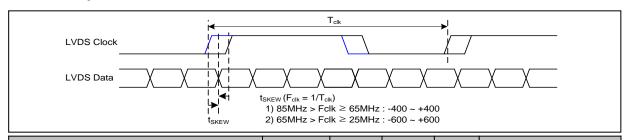
# 3-3. LVDS Signal Timing Specifications

# 3-3-1. DC Specification



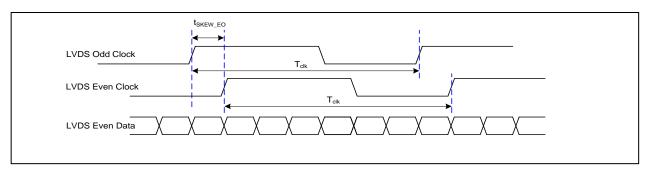
Description	Symb ol	Min	Max	Unit	Notes
LVDS Differential Voltage	V <sub>ID</sub>	100	600	mV	-
LVDS Common mode Voltage	V <sub>CM</sub>	0.6	1.8	V	-
LVDS Input Voltage Range	V <sub>IN</sub>	0.3	2.1	V	-

# 3-3-2. AC Specification

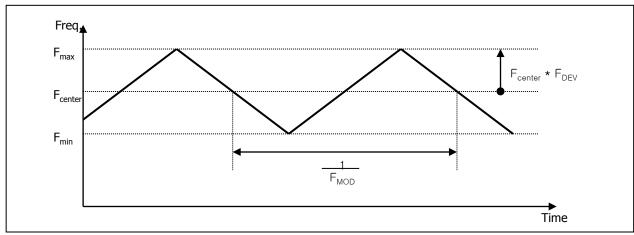


Description	Symbol	Min	Max	Unit	Notes
LVDS Clock to Data Skow Margin	t <sub>skew</sub>	- 400	+ 400	ps	85MHz > Fclk ≥ 65MHz
LVDS Clock to Data Skew Margin	t <sub>skew</sub>	- 600	+ 600	ps	65MHz > Fclk ≥ 25MHz
LVDS Clock to Clock Skew Margin (Even to Odd)	t <sub>SKEW_EO</sub>	- 1/7	+ 1/7	T <sub>clk</sub>	-
Maximum deviation of input clock frequency during SSC	F <sub>DEV</sub>	-	± 3	%	-
Maximum modulation frequency of input clock during SSC	F <sub>MOD</sub>	-	200	KHz	-





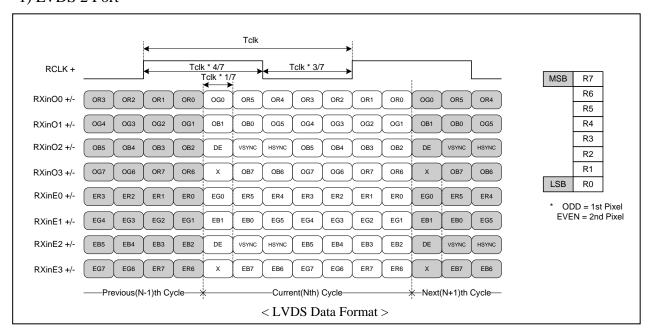
< Clock skew margin between channel >



< Spread Spectrum >

#### 3-3-3. Data Format

## 1) LVDS 2 Port





### 3-4. Signal Timing Specifications

This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of LVDS Tx/Rx for its proper operation.

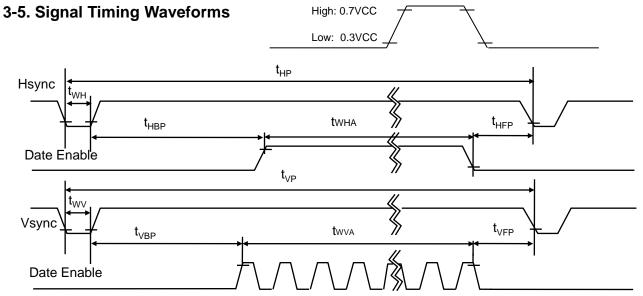
Table 5. TIMING TABLE

ITEM	Symbol		Min	Тур	Max	Unit	Note
DCLK	Frequency	f <sub>CLK</sub>	-	74.9	-	MHz	2port
	Period	t <sub>HP</sub>	1086	1138	1190		
Hsync	Width	t <sub>WH</sub>	32	48	56	tCLK	2port
	Width-Active	t <sub>WHA</sub>	960	960	960		
	Period	t <sub>VP</sub>	1093	1097	1101		
Vsync	Width	t <sub>WV</sub>	2	3	4	tHP	
	Width-Active	t <sub>WVA</sub>	1080	1080	1080		
	Horizontal back porch	t <sub>HBP</sub>	68	98	134	tCLK	Opert
Data	Horizontal front porch	t <sub>HFP</sub>	26	32	40	ICLN	2port
Enable	Vertical back porch	t <sub>VBP</sub>	10	12	14	tHP	
	Vertical front porch	t <sub>VFP</sub>	1	2	3	u IF	

#### Note)

1. In this documentation, all reliabilities are specified for timing specification based on refresh rate of 60Hz. However, LP173WF1 has a good actual performance even at lower refresh rate( eg. 40Hz or 50Hz) for power saving mode, whereas LP173WF1 is secured only for function under lower refresh rate. 60Hz at Normal mode, 50Hz ,40 Hz at Power save mode. Don't care Flicker level (power save mode).

Condition:  $V_{CC} = 3.3V$ 





# 3-6. Color Input Data Reference

The brightness of each primary color (red,green and blue) is based on the 6-bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 6. COLOR DATA REFERENCE

									Inp	out Co	olor D	ata							
	Color			RE	ΞD					GRE	EEN					BL	UE		
)	50101	MSE	3				LSB	-						MSE					LSB
		R 5	R 4	R 3	R 2	R 1	R 0	G 5	G 4	G 3	G 2	G 1	G 0	B 5	B 4	В3	B 2	B 1	B 0
	Black	0	0			0	0	0			0		0	0	0			0	0
	Red	1	1		1	. 1 	1	0	0	0	0		0	0	0		0	0	0
	Green	0	0				0	1	1	1		1	1	0	0			0	0
Basic	Blue	0	0	0		0	0	0	0	0	0		0	1	1	.1	1		1
Color	Cyan	0	0	0	0	0	0	1	1	1		. 1	1	1	1	.1	. 1		1
	Magenta	1	1	1	. 1	1		0	0	0	0	0	0	1	1	1	. 1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	RED (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
RED					 														
	RED (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
GREEN																			
	GREEN (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	BLUE (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
BLUE		ļ			••••• 			ļ			 						 		
	BLUE (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	 1	1	 1	 1	0
	BLUE (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	 1	1	1



#### 3-7. Power Sequence

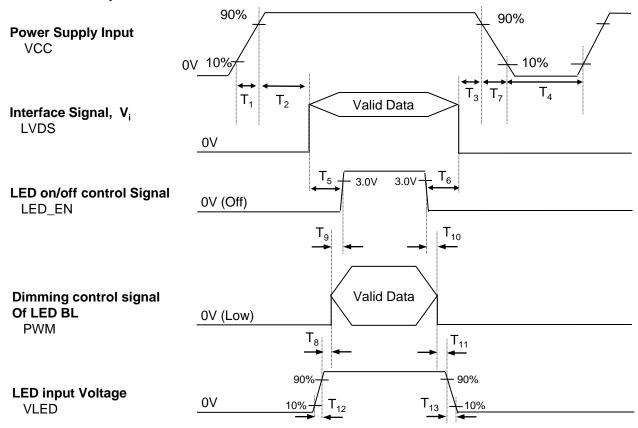


Table7. POWER SEQUENCE TABLE

Logic		Value		Lloito	LED		Value		Units
Parameter	Min.	Тур.	Max.	Units	Parameter	Min.	Тур.	Max.	Units
T <sub>1</sub>	0.5	-	10	ms	T <sub>8</sub>	10	-	-	ms
T <sub>2</sub>	0	ı	50	ms	T <sub>9</sub>	0	-	-	ms
T <sub>3</sub>	0	1	50	ms	T <sub>10</sub>	0	-	-	ms
T <sub>4</sub>	400	1	ı	ms	T <sub>11</sub>	10	-	-	ms
T <sub>5</sub>	200	1	ı	ms	T <sub>12</sub>	0.5	-	-	ms
T <sub>6</sub>	200	-	ı	ms	T <sub>13</sub>	0	-	5000	ms
T <sub>7</sub>	3	-	10	ms					

#### Note)

- 1. Do not insert the mating cable when system turn on.
- 2. Valid Data have to meet "3-3. LVDS Signal Timing Specifications"
- 3. LVDS, LED\_EN and PWM need to be on pull-down condition on invalid status.
- 4. LGD recommend the rising sequence of VLED after the Vcc and valid status of LVDS turn on.

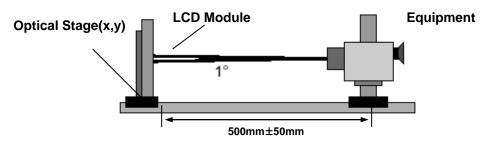


## 4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 20 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of  $\Phi$  and  $\Theta$  equal to  $0^{\circ}$ .

FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method



**Table 8. OPTICAL CHARACTERISTICS** 

Ta=25°C, VCC=3.3V,  $f_{V}$ =60Hz,  $f_{CLK}$ = 149.8MHz, ILED =22 mA

Parameter	Symbol		Values	1	Units	Notes
. a.a.meter	<b>G</b> y	Min	Тур	Max	00	
Contrast Ratio	CR	500	600	l <del>.</del>	<b>.</b>	1
Surface Luminance, white	L <sub>WH</sub>	255	300		cd/m <sup>2</sup>	2
Luminance Variation	δ <sub>WHITE</sub>	-	1.4	1.6		3
Response Time	Tr <sub>R +</sub> Tr <sub>D</sub>	-	8	16	ms	4
Color Coordinates						
RED	RX	0.610	0.640	0.670		
	RY	0.305	0.335	0.365		
GREEN	GX	0.290	0.320	0.350		
	GY	0.580	0.630	0.660	[	
BLUE	ВХ	0.120	0.150	0.180		
	BY	0.030	0.060	0.090	[	
WHITE	WX	0.283	0.313	0.343		
	WY	0.299	0.329	0.359	[	
Viewing Angle						5
x axis, right(Φ=0°)	Θr	60	-	-	degree	
x axis, left (Φ=180°)	Θl	60	-		degree	
y axis, up (Φ=90°)	Θu	50	-	-	degree	
y axis, down ( $\Phi$ =270°)	Θd	50	-	-	degree	
Gray Scale						6
Color Gamut	C/G	67	72	-	%	



#### Note)

1. Contrast Ratio(CR) is defined mathematically as

Surface Luminance with all white pixels

Contrast Ratio =

Surface Luminance with all black pixels

2. Surface luminance is the average of 5 point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 1.

$$L_{WH} = Average(L_1, L_2, \dots L_5)$$

3. The variation in surface luminance, The panel total variation ( $\delta_{WHITE}$ ) is determined by measuring L<sub>N</sub> at each test position 1 through 13 and then defined as followed numerical formula. For more information see FIG 2.

$$\delta_{\text{ WHITE}} = \frac{\text{Maximum}(\textbf{L}_{1}, \textbf{L}_{2}, \ \dots \ \textbf{L}_{13})}{\text{Minimum}(\textbf{L}_{1}, \textbf{L}_{2}, \ \dots \ \textbf{L}_{13})}$$

- Response time is the time required for the display to transition from white to black (rise time, Tr<sub>R</sub>) and from black to white(Decay Time, Tr<sub>D</sub>). For additional information see FIG 3.
- 5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.
- 6. Gray scale specification

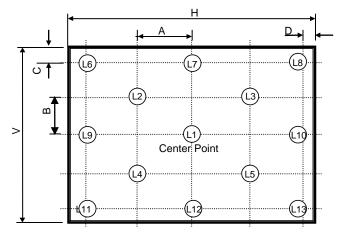
\* 
$$f_{V} = 60$$
Hz

Gray Level	Luminance [%] (Typ)
L0	0.11
L7	1.20
L15	5.23
L23	11.8
L31	20.6
L39	34.6
L47	53.3
L55	74.8
L63	100



#### FIG. 2 Luminance

<Measuring point for Average Luminance & measuring point for Luminance variation>



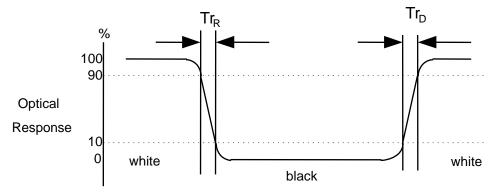
H,V: ACTIVE AREA

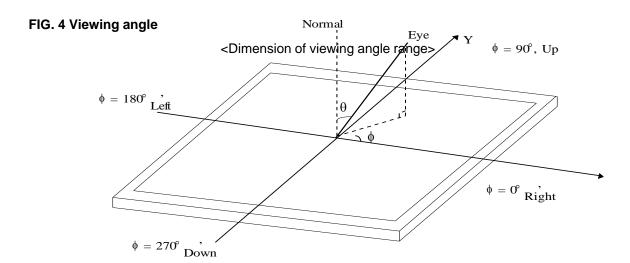
A: H/5 mm B: V/5 mm C: V/10 mm D: H/10 mm

POINTS: 13 POINTS

#### FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".







#### 5. Mechanical Characteristics

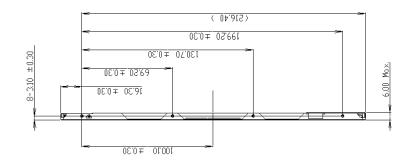
The contents provide general mechanical characteristics for the model LP173WF1. In addition the figures in the next page are detailed mechanical drawing of the LCD.

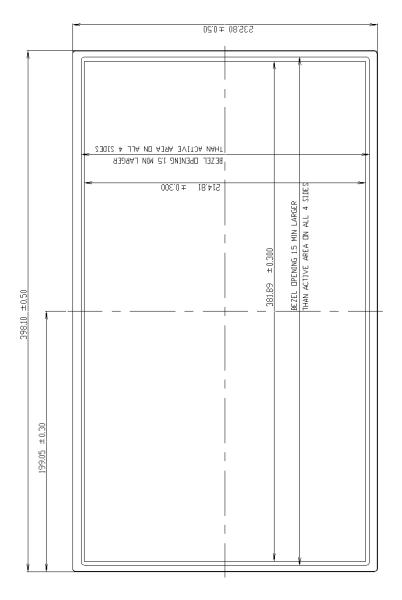
	Horizontal	398.1 ± 0.50mm			
Outline Dimension	Vertical	232.8 ± 0.50mm			
	Depth	6.0mm(Max.)			
Bezel Area	Horizontal	1.5mm Min.( Lager than Active Display Area )			
Dezei Alea	Vertical	1.5mm Min.( Lager than Active Display Area )			
Active Display Area	Horizontal	381.888mm			
Active Display Area	Vertical	214.812 mm			
Weight	580g (Max.)				
Surface Treatment	3H Anti-Glare treatment of the front Polarizer (Haze 44%)				



<FRONT VIEW>

Note) Unit:[mm], General tolerance: ± 0.5mm

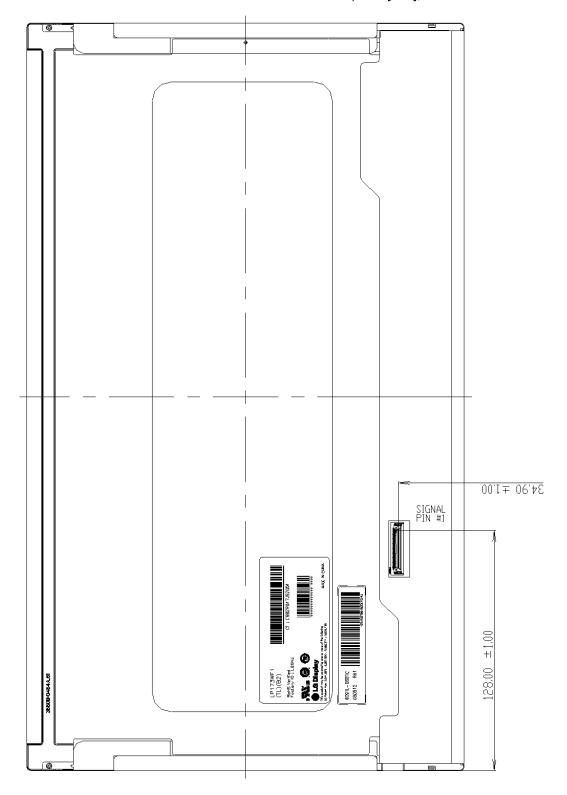






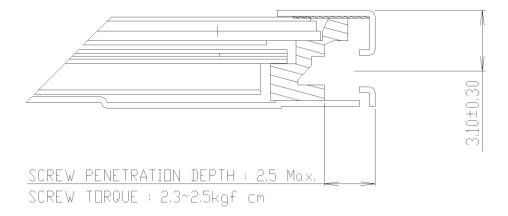
<REAR VIEW>

Note) Unit:[mm], General tolerance: ± 0.5mm



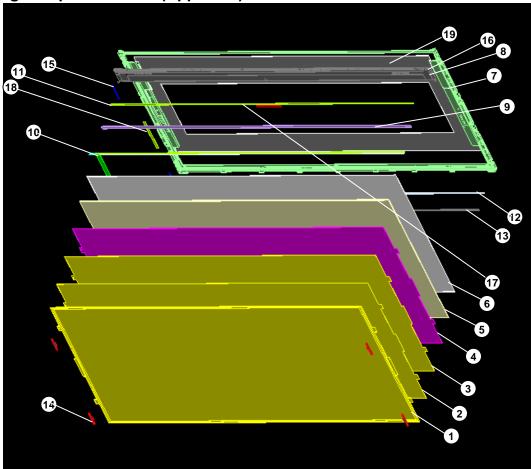


# [ DETAIL DESCRIPTION OF SIDE MOUNTING SCREW ]





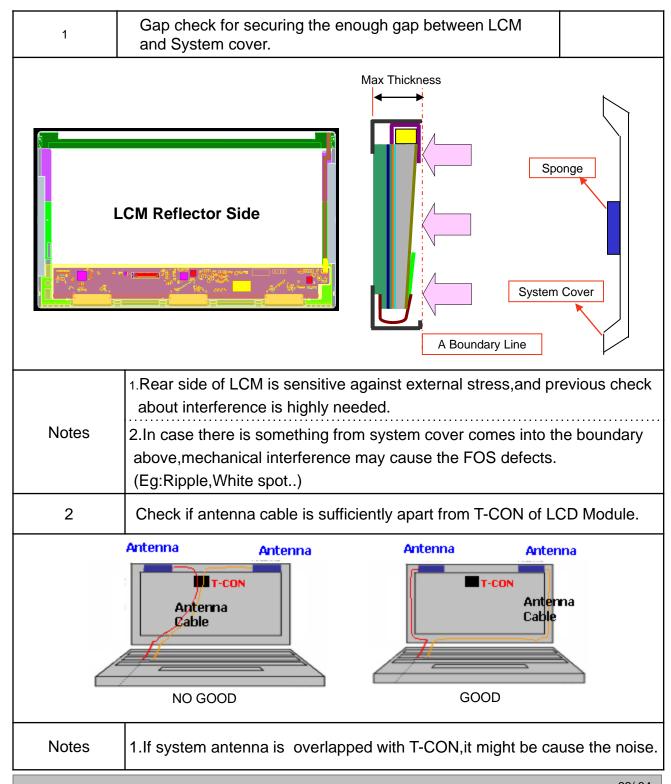
**Backlight Exploded View. (Appendix)** 



No	Part Name	No	Part Name
1	Diffuser Up Sheet	11	Cover Bottom Fixing Double Tape
2	Prism Up Sheet	12	LGP Fixing Double Tape
3	Prism Down Sheet	13	Reflective Single Tape
4	Diffuser Down Sheet	14	Sheet Fixing Pad (4pcs)
5	Light Guide Panel	15	Panel Fixing Pad (2pcs)
6	Reflector	16	Screw (2pcs)
7	Supporter Main	17	Reflector Fixing Tape
8	Cover Bottom	18	FPC Fixing Tape
9	LED Housing	19	AL Plate
10	LED Array		

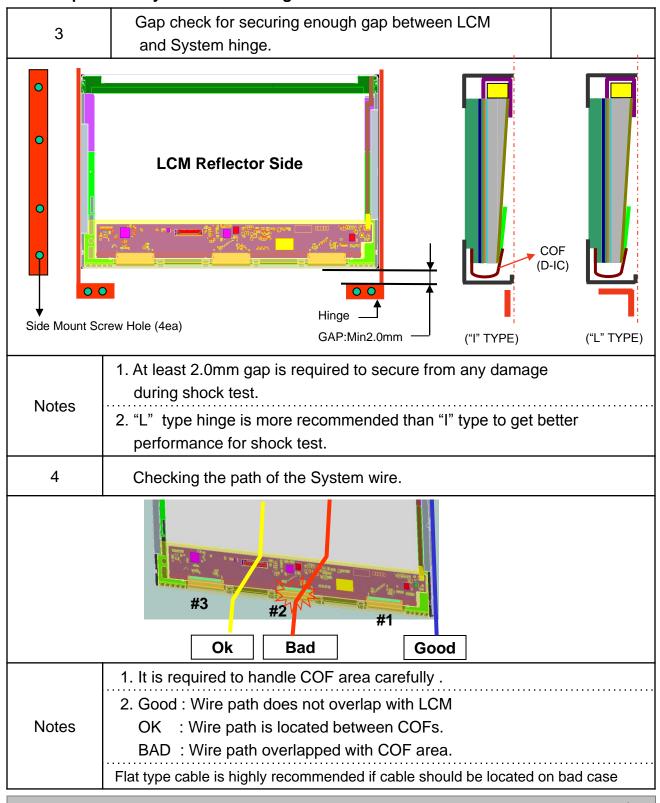


### LGD Proposal for system cover design.(Appendix)



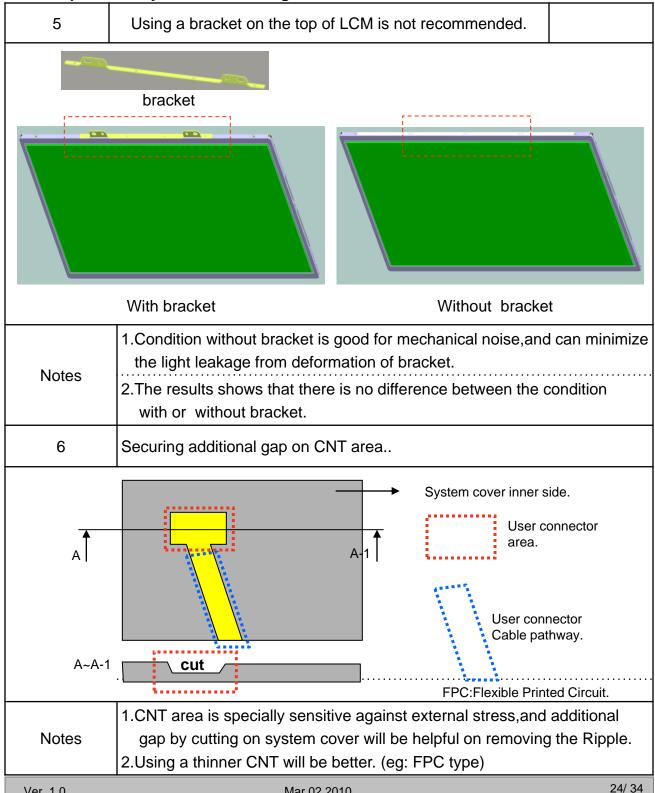


## LGD Proposal for system cover design.





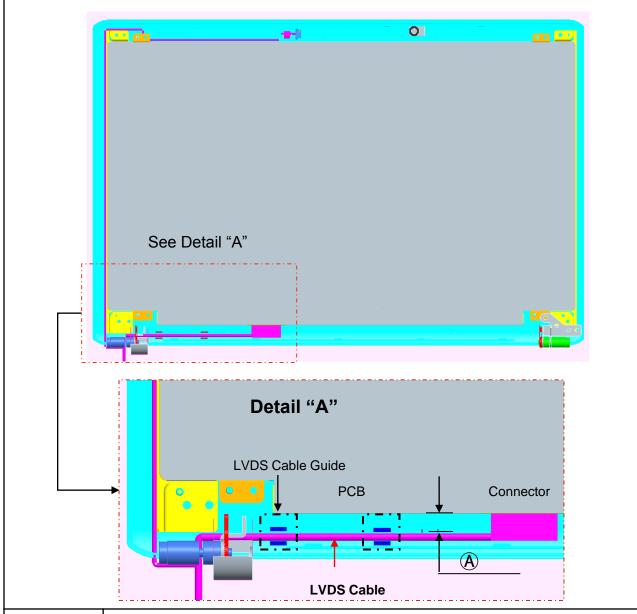
LGD Proposal for system cover design.





LGD Proposal for system cover design.

7 Checking the path of System LVDS Cable.



Notes

 At least 1.0mm gap (A) is required to secure from any damage by overlapping system cable and LCM (This overlap may cause a Abnormal Display after hinge test)

- 2."Flat" type of LVDS cable is more recommended than "Cylinderical" type .
- 3. Making LVDS Cable Guide will give better performance
- . (Refer to detail "A")



LGD Proposal for system cover design.

8 Securing additional gap between front cover & LCD at edge of front cover. "A": Overlap between Front Cover & Liquid Crystal area No Good Panel Size Front Bezel Open Size Front Cover Active Area **Liquid Crystal** Cell **Supporter Main Back Cover** Good Front Cover **Supporter Main Back Cover** Recess Depth(B): ?.?mm Resses Width(A): ?.?mm Recess Width(A): Up / Down /Left /Right ※ Recess Depth(®): Up / Down /Left /Right 1. Active area which is filled with Liquid Crystal is sensitive against external stress, so additional gap to make recess area on the edge of Notes front cover will be helpful to prevent mechanical Ripple. (Dimension of Recess depends on each model design)



# 6. Reliability

#### Environment test condition

No.	Test Item	Conditions					
1	High temperature storage test	Ta= 60°C, 240h					
2	Low temperature storage test	Ta= -20°C, 240h					
3	High temperature operation test	Ta= 50°C, 50%RH, 240h					
4	Low temperature operation test	Ta= 0°C, 240h					
5	Vibration test (non-operating)	Sine wave, 5 ~ 150Hz, 1.5G, 0.37oct/min 3 axis, 30min/axis					
6	Shock test (non-operating)	Half sine wave, 180G, 2ms one shock of each six faces(I.e. run 180G 2ms for all six faces)					
7	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr					



#### 7. International Standards

#### 7-1. Safety

- a) UL 60950-1, Second Edition, Underwriters Laboratories Inc.
   Information Technology Equipment Safety Part 1 : General Requirements.
- b) CAN/CSA C22.2 No.60950-1-07, Second Edition, Canadian Standards Association. Information Technology Equipment Safety Part 1: General Requirements.
- c) EN 60950-1:2006 + A11:2009, European Committee for Electrotechnical Standardization (CENELEC). Information Technology Equipment Safety Part 1 : General Requirements.
- d) IEC 60950-1:2005, Second Edition, The International Electrotechnical Commission (IEC). Information Technology Equipment Safety Part 1 : General Requirements.

#### 7-2. EMC

- a) ANSI C63.4 "American National Standard for Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electronic Equipment in the Range of 9 kHz to 40 GHz." American National Standards Institute (ANSI), 2003.
- b) CISPR 22 "Information technology equipment Radio disturbance characteristics Limit and methods of measurement." International Special Committee on Radio Interference (CISPR), 2005.
- c) CISPR 13 "Sound and television broadcast receivers and associated equipment Radio disturbance characteristics – Limits and method of measurement." International Special Committee on Radio Interference (CISPR), 2006.

#### 7-3. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003



# 8. Packing

## 8-1. Designation of Lot Mark

a) Lot Mark

А	В	С	D	Е	F	G	Н	I	J	К	L	М	
---	---	---	---	---	---	---	---	---	---	---	---	---	--

A,B,C : SIZE(INCH) D : YEAR

E: MONTH  $F \sim M$ : SERIAL NO.

#### Note

#### 1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

#### 2. MONTH

	Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
ſ	Mark	1	2	3	4	5	6	7	8	9	Α	В	С

#### b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module. This is subject to change without prior notice.

# 8-2. Packing Form

a) Package quantity in one box: 20pcs

b) Box Size :490X390X298



#### 9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

#### 9-1. MOUNTING PRECAUTIONS

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to t h e module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
  Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

#### 9-2. OPERATING PRECAUTIONS

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :  $V=\pm 200 mV$  (Over and under shoot voltage)
- (2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.



#### 9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

#### 9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

#### 9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

#### 9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

- (1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
  - Please carefully peel off the protection film without rubbing it against the polarizer.
- (3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
- (4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.



# APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 1/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
	0	00	Header	00	00000000
	1	01	Header	FF	111111111
	2	02	Header	FF	111111111
Header	3	03	Header	FF	11111111
Iea	4	FF	11111111		
F	5	05	Header	FF	11111111
	6	06	Header	FF	111111111
	7	07	Header	00	00000000
	8	08	EISA manufacture code ( 3 Character ID ) LGD	30	00110000
EDID	9	09	EISA manufacture code (Compressed ASC II)	E4	11100100
EI	10	0A	Panel Supplier Reserved - Product Code 0283h	83	10000011
	11	0B	( Hex. LSB first )	02	00000010
<b>z</b>	12	0C	LCD Module Serial No - Preferred but Optional ("0" If not used)	00	00000000
roduct Version	13	0D	LCD Module Serial No - Preferred but Optional ("0" If not used)	00	00000000
od,	14	0E	LCD Module Serial No - Preferred but Optional ("0" If not used)	00	00000000
Pr V	15	0F	LCD Module Serial No - Preferred but Optional ("0" If not used)	00	00000000
r/	16	10	Week of Manufacture 0 weeks	00	00000000
Vendor / Product Version	17	11	Year of Manufacture 2010years	14	00010100
Ver	18	12	EDID structure version #= 1	01	00000001
	19	13	EDID revision # = 3	03	00000011
s.	20	14	Video input Definition = Digital signal	90	10010000
ay zter	21	15	Max H image size (Rounded cm) = 38 cm	26	00100110
Display Parameters	22	16	Max V image size (Rounded cm) = 22 cm	16	00010110
Di	23	17	Display gamma = (gamma*100)-100 = Example:(2.2*100)-100=120 = 2.2 Gamma	78	01111000
$P_{\ell}$	24	18	Feature Support (no_DPMS, no_Active Off/Very Low Power, RGB color display, Timing BLK 1,no_GTF)	0A	00001010
Si	25	19	Red/Green Low Bits (RxRy/GxGy)	F1	11110001
Panel Color Coordinates	26	1A	Blue/White Low Bits (BxBy/WxWy)	95	10010101
din	27	1B	Red X $Rx = 0.64$	A3	10100011
or	28	1C	Red Y Ry = 0.335	55	01010101
$\mathcal{C}_{o}$	29	1D	Green X $Gx = 0.32$	52	01010010
or	30	1E	Green Y Gy =0.63	A1	10100001
Zol	31	1F	Blue X $Bx = 0.15$	26	00100110
el (	32	20	Blue Y By = $0.06$	0F	00001111
an	33	21	White X Wx =0.313	50	01010000
P	34	22	White Y Wy =0.329	54	01010100
d d	35	23	Established timing 1 (00h if not used)	00	00000000
Estabi ished Timin as	36	24	Established timing 2 (00h if not used)	00	00000000
rs Tr	37	25	Manufacturer's timings (00h if not used)	00	00000000
	38	26	Standard timing ID1 (01h if not used)	01	00000001
	39	27	Standard timing ID1 (01h if not used)	01	00000001
	40	28	Standard timing ID2 (01h if not used)	01	00000001
	41	29	Standard timing ID2 (01h if not used)	01	00000001
B	42	2A	Standard timing ID3 (01h if not used)	01	00000001
80	43	2B	Standard timing ID3 (01h if not used)	01	00000001
nin	44	2C	Standard timing ID4 (01h if not used)	01	00000001
Tin	45	2D	Standard timing ID4 (01h if not used)	01	00000001
<i>p.</i>	46	2E	Standard timing ID5 (01h if not used)	01	00000001
Standard Timing I	47	2F	Standard timing ID5 (01h if not used)	01	00000001
an	48	30	Standard timing ID6 (01h if not used)	01	00000001
St	49	31	Standard timing ID6 (01h if not used)	01	00000001
	50	32	Standard timing ID7 (01h if not used)	01	00000001
	51	33	Standard timing ID7 (01h if not used)	01	00000001
	52	34	Standard timing ID8 (01h if not used)	01	00000001
	53	35	Standard timing ID8 (01h if not used)	01	00000001



# APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 2/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
	54	36	Pixel Clock/10,000 (LSB) 149.8 MHz @ 60Hz	84	10000100
	55	37	Pixel Clock/10,000 (MSB)	3A	00111010
	56	38	Horizontal Active (lower 8 bits) 1920 Pixels	80	10000000
	57	39	Horizontal Blanking(Thp-HA) (lower 8 bits) 356 Pixels	64	01100100
	58	3A	Horizontal Active / Horizontal Blanking(Thp-HA) (upper 4:4bits)	71	01110001
1	59	3B	Vertical Avtive 1080 Lines	38	00111000
Timing Descriptor #1	60	3C	Vertical Blanking (Tvp-HA) (DE Blanking typ.for DE only panels) 17 Lines	11	00010001
)to	61	3D	Vertical Active : Vertical Blanking (Tvp-HA) (upper 4:4bits)	40	01000000
rip	62	3E	Horizontal Sync. Offset (Thfp) 64 Pixels	40	01000000
esc	63	3F	Horizontal Sync Pulse Width (HSPW) 96 Pixels	60	01100000
Ď	64	40	Vertical Sync Offset(Tvfp): Sync Width (VSPW) 2 Lines: 3 Lines	23	00100011
ing	65	41	Horizontal Vertical Sync Offset/Width (upper 2bits)	00	00000000
im	66	42	Horizontal Image Size (mm) 383 mm	7F	01111111
T	67	43	Vertical Image Size (mm) 215 mm	D7	11010111
	68	44	Horizontal Image Size / Vertical Image Size	10	00010000
	69	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
	70	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
			Non-Interlace, Normal display, no stereo, Digital Separate (Vsync_NEG, Hsync_NEG), DE only note: LSB is set to '1'		
	71	47	if panel is DE-timing only. H/V can be ignored.	19	00011001
	72	48	Flag	00	00000000
	73	49	Flag	00	00000000
	74	4A	Flag	00	00000000
	75	4B	Data Type Tag (Descriptor Defined by manufacturer)	00	00000000
	76	4C	Flag	00	00000000
#2	77	4D	Descriptor Defined by manufacturer	00	00000000
or	78	4E	Descriptor Defined by manufacturer	00	00000000
ipt	79	4F	Descriptor Defined by manufacturer	00	00000000
Timing Descriptor #2	80	50	Descriptor Defined by manufacturer	00	00000000
Des	81	51	Descriptor Defined by manufacturer	00	00000000
8 7	82	52	Descriptor Defined by manufacturer	00	00000000
nin	83	53	Descriptor Defined by manufacturer	00	00000000
Tün	84	54	Descriptor Defined by manufacturer	00	00000000
	85	55	Descriptor Defined by manufacturer	00	00000000
	86	56	Descriptor Defined by manufacturer	00	00000000
	87	57	Descriptor Defined by manufacturer	00	00000000
	88	58	Descriptor Defined by manufacturer	00	00000000
	89	59	Descriptor Defined by manufacturer	00	00000000
	90	5A	Flag	00	00000000
	91	5B	Flag	00	00000000
	92	5C	Flag	00	00000000
	93	5D	Data Type Tag ( ASCII String )	FE	11111110
	94	5E	Flag	00	00000000
#3	95	5F	ASCII String L	4C	01001100
)r +	96	60	ASCII String G	47	01000111
Timing Descriptor #3	97	61	ASCII String	20	00100000
cri	98	62	ASCII String D	44	01000100
Des	99	63	ASCII String i	69	01101001
8 1	100	64	ASCII String s	73	01110011
uin	101	65	ASCII String p	70	01110000
Tim	102	66	ASCII String 1	6C	01101100
`	103	67	ASCII String a	61	01100001
	104	68	ASCII String y	79	01111001
	105	69	Manufacturer P/N(If<13 char> 0Ah, then terminate with ASC II code 0Ah,set remaining char = 20h)	0A	00001010
	106	6A	Manufacturer P/N(If<13 char> 0Ah, then terminate with ASC II code 0Ah,set remaining char = 20h)	20	00100000
	107	6B	Manufacturer P/N(If<13 char> 0Ah, then terminate with ASC II code 0Ah,set remaining char = 20h)	20	00100000



# APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 3/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
	108	6C	Flag	00	00000000
	109	6D	Flag	00	00000000
	110	6E	Flag	00	00000000
	111	6F	Data Type Tag ( ASCII String )	FE	11111110
	112	70	Flag	00	00000000
#	113	71	ASCII String L	4C	01001100
Timing Descriptor #4	114	72	ASCII String P	50	01010000
ipt	115	73	ASCII String 1	31	00110001
scr	116	74	ASCII String 7	37	00110111
De	117	75	ASCII String 3	33	00110011
00	118	76	ASCII String W	57	01010111
ni	119	77	ASCII String F	46	01000110
Tü	120	78	ASCII String 1	31	00110001
	121	79	ASCII String -	2D	00101101
	122	7A	ASCII String T	54	01010100
	123	7B	ASCII String L	4C	01001100
	124	7C	ASCII String B	42	01000010
	125	7D	ASCII String 2	32	00110010
ksum	126	7E	Extension flag (# of optional 128 panel ID extension block to follow, Typ = 0)	00	00000000
Checksum	127	<b>7</b> F	Check Sum (The 1-byte sum of all 128 bytes in this panel ID block shall = 0)	BA	10111010