

CUSTOMER APPROVAL SHEET

C	ompany Name	
	MODEL	A061FW01 V0
	CUSTOMER	Title:
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	APPROVAL FOR SPECIF	FICATIONS ONLY (Spec. Ver) FICATIONS AND ES SAMPLE (Spec. Ver FICATIONS AND CS SAMPLE (Spec. Ver
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Product Specification

6.1" COLOR TFT-LCD MODULE

Model Name: A061FW01 V0

Planned Lifetime:From 2009/May To 2011/MayPhase-out Control:From 2010/Dec To 2011/MayEOL Schedule:2011/May

< ◆ >Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

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Record of Revision

Version	Revise Date	Page	Content
0.0	2009/04/14	All	First Draft.
0.1	2009/05/15	9	Update Optical specification
		11	Update Reliability test items
		13	Update drawing



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A. Physical specifications

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NO.	Item	Item Specification						
1	Display resolution(dot)	480RGB(W)x234(H)						
2	Active area(mm)	136.08(W)×71.955(H)						
3	Screen size(inch)	6.1(Diagonal)						
4	Dot pitch(mm)	0.0945(W)x 0.3075(H)						
5	Color configuration	R. G. B. stripe						
6	NTSC ratio	50%						
7	Overall dimension(mm)	149.0(W)×82.9(H)×5.1(D)	Note 1					
8	Weight (g)	113g±10%						
9	Surface treatment	AG(25%) with EWV film						
10	Backlight unit	LED						
11	Gray scale inversion direction	6 o'clock						

Note 1: Refer to Fig. 1



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B. Electrical specifications

1.Pin assignment

a. TFT-LCD panel driving section

Pin no	Symbol	I/O	Description	Remark
1	GND	-	Ground for logic circuit	
2	NC	-		
3	V_{GL}	ı	Negative power for scan driver	
4	STVD	I/O	Vertical start pulse	Note 1
5	UDC	I	UP/DOWN scan control input	Note 1,2
6	CKV	I	Shift clock input for scan driver	
7	OEV	I	Output enable input for scan driver	
8	NC	-		
9	NC	-		
10	STVU	I/O	Vertical start pulse	Note 1
11	V _{CC}	I	Supply voltage of logic control circuit for scan driver	Note 4
12	DV _{cc}	I	Supply voltage of logic control circuit for data driver	Note 4
13	V_{GH}	I	Positive power for scan driver	
14	NC	-		
15	VCOM	I	Common electrode driving signal	
16	STHR	I/O	Start pulse for horizontal scan line	Note 1
17	AV_{DD}	I	Supply voltage for analog circuit	
18	VR	I	Alternated video signal input(Red)	
19	VG	I	Alternated video signal input(Green)	
20	VB	I	Alternated video signal input(Blue)	
21	AGND	-	Ground for analog circuit	
22	CPH1	I	Sampling and shifting clock pulse for data driver	
23	CPH2	I	Sampling and shifting clock pulse for data driver	
24	CPH3	I	Sampling and shifting clock pulse for data driver	
25	GND	-	Ground for logic circuit	
26	MOD	I	Sequential sampling and simultaneous sampling setting	Note 3
27	LRC	I	LEFT/RIGHT scan control input	Note 1,2
28	OEH	I	Output enable input for data driver	
29	STHL	I/O	Start pulse for horizontal scan line	
30	GND	-	Ground for logic circuit	

Note 1: Selection of scanning mode (please refer to the following table)



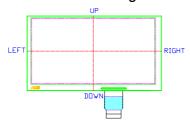
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Setting of scan control input			IN/OU ⁻ for star	T state t pulse		Scanning direction
UDC	LRC	STVD	STVU	STHR	STHL	
GND	V _{cc}	OUT	IN	OUT	IN	From up to down, and from left to right.
V _{CC}	GND	IN	OUT	IN	OUT	From down to up, and from right to left.
GND	GND	OUT	IN	IN	OUT	From up to down, and from right to left.
V _{CC}	V _{cc}	IN	OUT	OUT	IN	From down to up, and from left to right.

IN: Input; OUT: Output.

Note 2: Definition of scanning direction.

Refer to figure as below:



Note 3: MOD = H: Simultaneous sampling.

MOD = L: Sequential sampling.

Please set CPH2 and CPH3 to GND when MOD = H.

Note 4: Electrical characteristics of V_{CC} and DV_{CC} are the same.

b. Backlight driving section (Refer to Figure 1)

No.	Symbol	I/O	Description	Remark
1	HI		Power supply for backlight unit (High voltage)	
2	GND	-	Ground for backlight unit	

2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
	V _{CC}	GND=0	-0.3	7	V	
	AV_{DD}	AGND=0	-0.3	7	V	
Power voltage	V_{GH}	OND 0	-0.3	18	V	
	V_{GL}	GND=0	-15	0.3	V	
	$V_{GH} - V_{GL}$		-	33	V	
In a set of an all settle as	V_{i}		-0.3	AV _{DD} +0.3	V	Note 1
Input signal voltage	V_{l}		-0.3	V _{CC} +0.3	V	Note 2
	VCOM		-2.9	7.5	V	
LED	V_{F}	I _F = 120mA		25.2	V	
LED	I _F			120	mA	
Operation temperature	Topr	Ambient	-20	70	$^{\circ}\!\mathbb{C}$	
Storage temperature	Tstg	Ambient	-30	80	$^{\circ}\!\mathbb{C}$	

Note 1: VR, VG, VB.

Note 2: STHL, STHR, OEH, LRC, CPH1~CPH3, STVD, STVU, OEV, CKV, UDC, MOD.



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3. Electrical characteristics

a. Typical operating conditions (GND=AGND=0V, Note 3)

Item Symbol		Symbol	Min.	Тур.	Max.	Unit	Remark
		V _{cc}	3	3.3	5.5	V	Note4
		AV_{DD}	4.5	5	5.5	V	
Power	supply	V_{GH}	14.3	15	15.7	V	
		V_{GL}	-10.5	-10	-9.5	V	
	signal	V _{iA}	0.4	-	AV _{DD} -0.4	V	Note 1
•	itude	V_{iAC}	-	4	-	V	AC component
(VK,V	'G,VB)	V_{iDC}	-	AV _{DD} /2	-	V	DC component
V/C	OM	V_{CAC}	3.5	5.6	6.5	Vp-p	AC component
VCOM		V_{CDC}	1.38	1.58	1.78	V	DC component
Input	H Level	V _{IH}	0.8 V _{CC}	-	V _{cc}	V	Note 2
signal voltage	L Level	V_{IL}	0	1	0.2 V _{CC}	>	Note 2

Note 1: Refer to Fig.4- (a).

Note 2: STHL, STHR, OEH, LRC, CPH1, STVD, STVU, OEV, CKV, UDC, MOD.

Note 3: Be sure to apply GND, V_{CC} and V_{GL} to the LCD first, and then apply V_{GH} .

Note 4: If input signal amplitude is 3.3V, recommend value for Vcc is 3.3V

If input signal amplitude is 5V, recommend value for Vcc is 5V

b. Current consumption (GND=AGND=0V)

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit	Remark
Current	I_{GH}	V _{GH} =15V	-	0.5	1.0	mA	
for	I _{GL}	V _{GL} =-10V	-	0.5	1.0	mA	
driver	I _{cc}	DV _{CC} =5V	-	3.0	6.0	mA	Note 1
	I _{DD}	AV _{DD} =5V	-	12	30	mA	

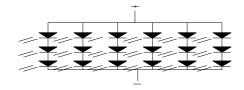
Note 1: I_{CC} is current consumption of DV_{CC} plus V_{CC}.

c. Backlight driving conditions (Self-heating type, Note1, Note3)

	Symb	Min.	Тур.	Max.	Unit	Remark
LED current	ΙL		120		mA	Note1
LED voltage	VL		9.6	10.5	V	Note1
LED Life Time	LL	10,000			Hrs	Note2

Note 1: Refer to below LED connection scheme

Note 2 : Under 25 $^{\circ}$ C, I_L = 120mA, continuous operation.





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4. AC Timing

a. Timing conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit.	Remark
Clock cycle time	t _{CPH}	100	103	107	ns	CPH1
CPH pulse duty	t _{cwh}	40	50	60	%	CPH1
CPH pulse delay	t _{C12} t _{C23} t _{C31}	30	t _{CPH} /3	t _{CPH} /2	ns	CPH1
STH setup time	t _{suh}	20	-	-	ns	STHR,STHL
STH hold time	t _{HDH}	20	-	-	ns	STHR,STHL
STH pulse width	t _{STH}		1		t _{CPH}	STHR,STHL
STH period	t _H	61.8	63.7	66.1	μ s	STHR,STHL
OEH pulse width	t _{oeh}	1	-	-	t _{CPH}	OEH (Note 1)
Sample and hold disable time	t _{DIS1}	1	-	-	t _{CPH}	Note 2
OEV pulse width	t _{OEV}	2.0	3.4	6.5	μ s	OEV
CKV pulse width	t _{CKV}	1.0	3.1	4.68	μ s	CKV
Clean enable time	t _{DIS2}	1.0	-	1 t _{OEV}	μ s	Note 3
Horizontal display start	t _{sh}		1		t _{CPH}	
Horizontal display timing range	t_{DH}	480		t _{CPH}		
STV setup time	t _{SUV}	400	-	-	ns	STVU, STVD
STV hold time	t _{HDV}	400	-	-	ns	STVU, STVD
STV pulse width	t _{STV}	-	-	1	t _H	STVU, STVD
Vertical display start	t _{SV}		3		t _H	
Vertical display timing range	t_{DV}		234	1	t _H	
VCOM rising time	t_{rCOM}		-	5	μ s	
VCOM falling time	t _{fCOM}		-	5	μ s	
VCOM delay time	t _{DCOM}	2	-	-	μ s	
TFT charging time	t_ch	55	-	-	μ s	
Output time delay	t _{del}	3	-	-	μ s	
Setup time of analog VR/VG/VB	t _{asu}	60	-	-	ns	
Hold time of analog VR/VG/VB	t _{ahd}	40	-	-	ns	
Frame rate		50	60	-	Hz	

Note 1: For all of the logic signals.

Note 2: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

Note 3: For Partial mode (4:3, side-black)

Note 4: Maximum time is one line period.

Note5: The maximum pulse width of OEH should refer to the minimum of t_{DIS1} and the hsync back porch.

Note 6: t_{dis1} is time difference between OEH and STHL

Note 7: t_{dis2} is time difference between OEV and CKV

Note 8: The unit is t_{CPH}



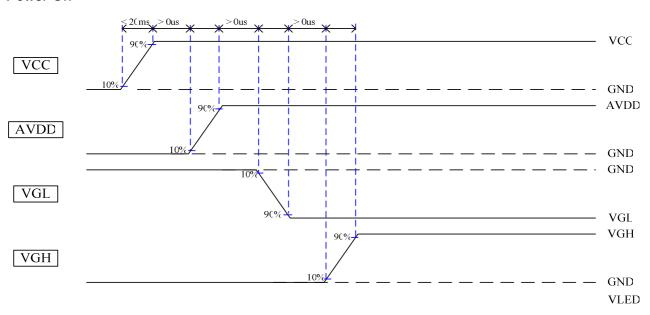
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b. Timing diagram

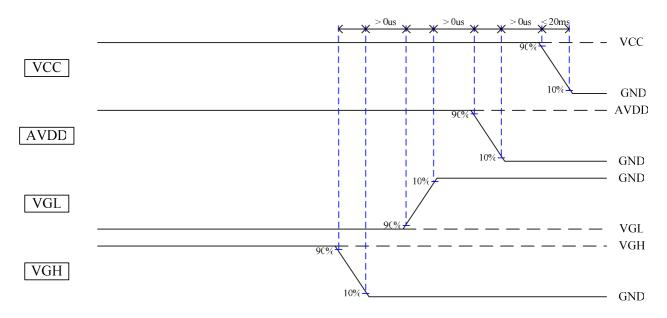
Please refer to the attached drawing, from Fig.2 to Fig.6.

5. Power On/Off Sequence (Only for reference)

Power On



Power Off





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C. Optical specification (Note1, Note2)

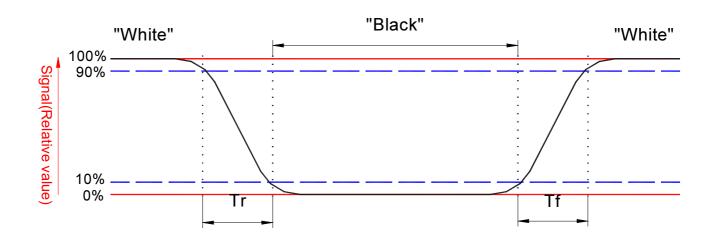
Item		Symbol	Condition	Min.	Тур.	Max.	Unit	Remark
Response time	Rise Fall	Tr Tf	<i>θ</i> =0°	-	15 20	50 60	ms ms	Note 3,5
Contrast ra	tio	CR	At optimized Viewing angle	350	500	-		Note 4, 5
Viewing angle	Top Bottom Left Right		CR≧10	35 55 55 55	45 65 65 65	- - -	deg.	Note 5, 6
Brightnes	S		I _L =120mA, 25°C	350	450		cd/m ²	
White chroma	aticity	X Y	$\theta = 0^{\circ}$ $\theta = 0^{\circ}$	0.26 0.29	0.31	0.36		Note 7

Note 1 : Ambient temperature =25 $^{\circ}$ C, and LED I_L = 120 mA.

Note 2 :To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-5, after 15 minutes operation.

Note 3. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (falling time) and from "white" to "black" (rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

Contrast ratio (CR)= Photo detector output when LCD is at "White" state

Photo detector output when LCD is at "Black" state



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Note 5. White $Vi=V_{i50} + 1.5V$

Black Vi= $V_{i50} \pm 2.0V$

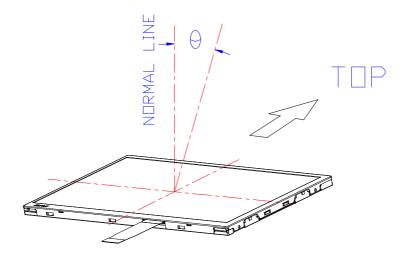
"±" means that the analog input signal swings in phase with V_{COM} signal.

" $\overline{+}$ " means that the analog input signal swings out of phase with V_{COM} signal.

 V_{i50} The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6. Definition of viewing angle, Refer to figure as below.



Note 7. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.



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D. Reliability test items(Note 3):

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80°C 240Hrs	Note1
2	Low temperature storage	Ta= -30℃ 240Hrs	
3	High temperature operation	Tp= 70°C 240Hrs	Note2
4	Low temperature operation	Ta= -20°C 240Hrs	
5	High temperature and high humidity	Tp= 50℃, 80% RH 240Hrs	Operation
6	Heat shock	-20°C ~70°C/50 cycles 2Hrs/cycle	Non-operation
7	Electrostatic discharge	$\pm 200 \text{V}, 200 \text{pF}(0\Omega)$, once for each termin	Non-operation
8	Vibration	Frequency range : $10\text{Hz} \sim 55\text{Hz}$ Stoke : 1.5mm Sweep : $10 \sim 55 \sim 10\text{Hz}$	JISC 7021
		2 hours for each direction of X,Y,Z (Total 6 Hours)	
9	Mechanical shock	100G, 6ms, ±X,±Y,±Z 3 times for each direction	JIS C7021, A-7 Condition C
10	Vibration (with carton)	Random vibration: 0.015G ² /Hz from 5~200Hz –6dB/octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	JIS Z0202

Note1: Ta: Ambient temperature.

Note2: Tp: Panel Surface Temperature

Note3: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

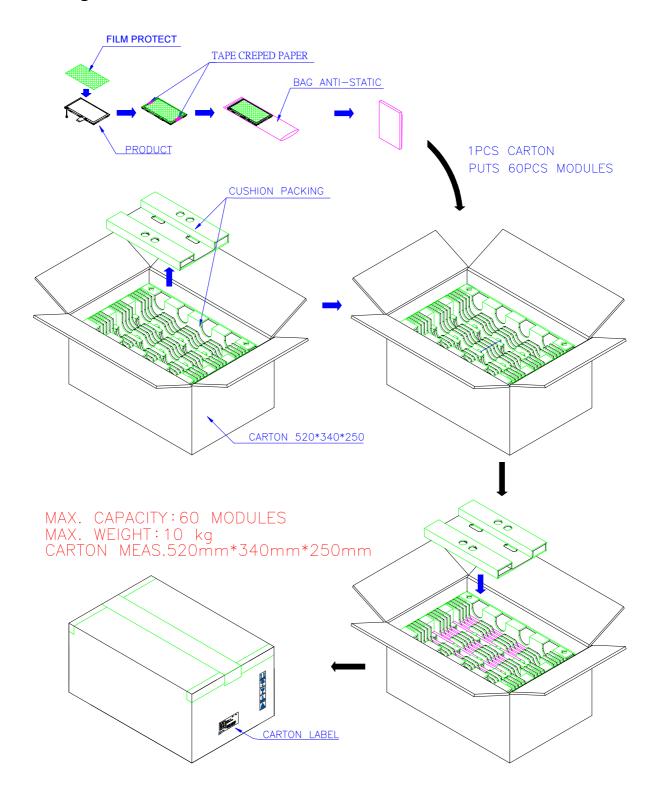


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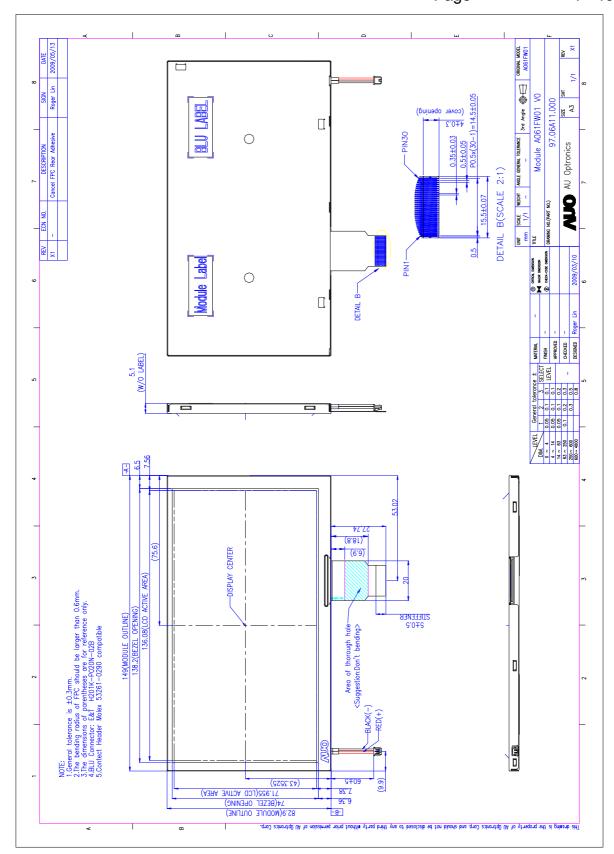
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E. Packing form





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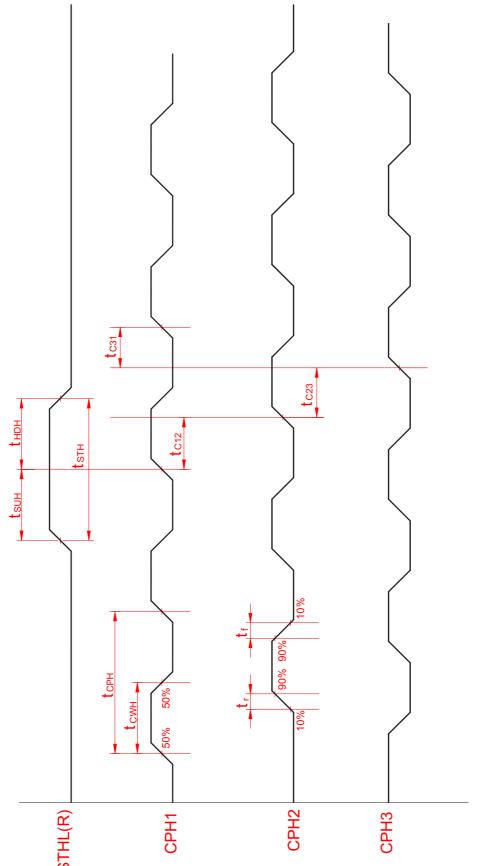
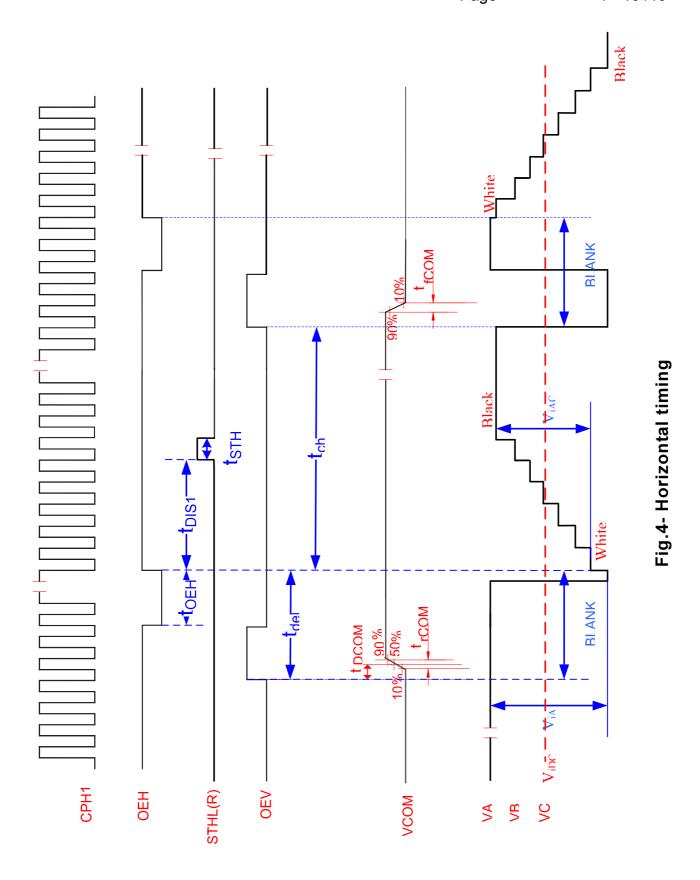


Fig.2 Sampling clock timing

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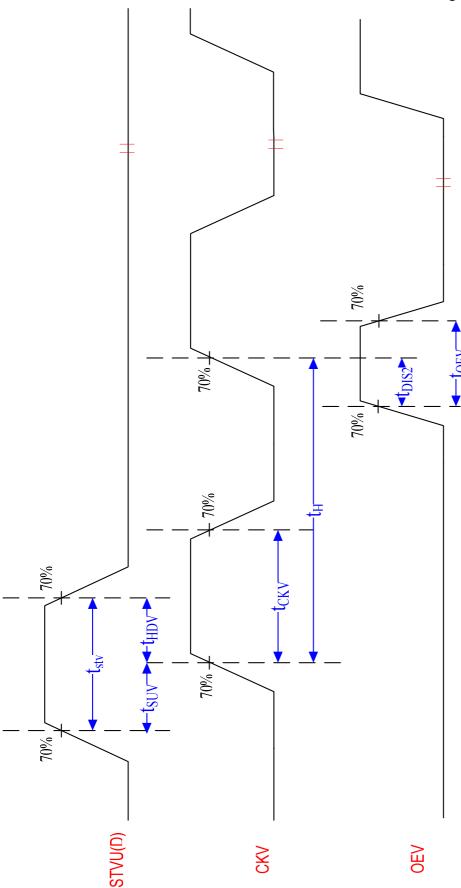


Fig.5- Vertical Shift Clock Timing



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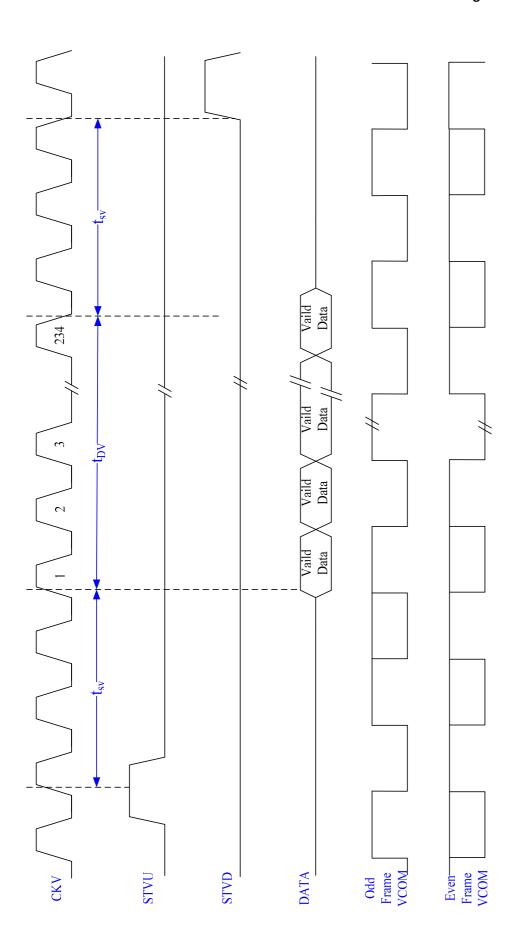


Fig.6 Vertical timing (From up to down)



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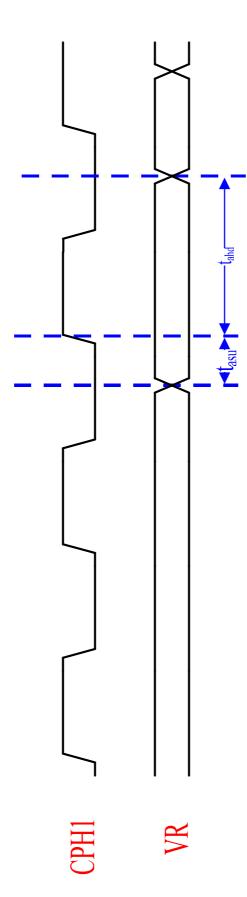


Fig.7 The setup and hold time definition between CPH1 and analog signal VR