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Product Specification

2.45″ COLOR TFT-LCD MODULE

MODEL NAME: A025CN02 V0

<◆>Preliminary Specification

< > Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0	11/Feb/2004		First draft.
0.1	4/May/2004	5-6 23-25	1) Point out optional V_{GH}, V_{GL} and LED backlight driving circuit in FPC pin assignment. 2) Provide suggested application circuit for private power supply of V_{GH}, V_{GL} and LED backlight driving
		7	Provide definition and suggestion of select pin in Note 4 and Note 5.

Contents:

Appendix:

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution(dot)	480(W) ×234(H)	
2	Active area(mm)	49.2(W)×38.142(H)	
3	Screen size(inch)	2.45(Diagonal)	
4	Dot pitch(mm)	0.1025(W)×0.163(H)	
5	Color configuration	R. G. B. delta	
6	Overall dimension(mm)	59.2(W) ×49.7(H) ×3.4(D)	Note 1
7	Weight(g)	21.0 (typ)	
8	Panel surface treatment	Anti-Glare	

Note 1: Refer to Fig. 2

B. Electrical specifications

1.Pin assignment

a. TFT-LCD panel driving section

Pin no	Symbol	I/O	Description	Remark
1	VSCL2	I	VCAC level Selection	Note 6
2	VSCL1	I	VCAC level Selection	Note 6
3	VSCL0	I	VCAC level Selection	Note 6
4	GND	P	Digital ground for gate	
5	VCC	PI	Digital Power for gate (+3.3V)	
6	VCAC	PS	VCOM level supply	
7	VGoff_H	PS	Negative power supply (High) for gate	
8	VCOM	SO	Frame polarity output for panel VCOM	
9	VGoff_L	PS	Negative power supply (Low) for gate	
10	C3M	C	Power setting capacitor connect pin	
11	C3P	C	Power setting capacitor connect pin	
12	VGH	PI	Positive power supply for gate (+15V)	Option Note 7
13	GND	-	Ground	
14	FB_G	FI	Main boost regulator feedback input. FB threshold is 0.6V	
15	GND	-	Ground	
16	DRV_G	O	Power transistor gate signal for the boost converter	
17	GLED1		LED module 1 Cathode	
18	VLED1	PI	LED module 1 Anode	Option Note 7
19			N/C	
20			N/C	
21	DRV_S	O	Power transistor gate signal for the boost converter	
22	FB_S	FI	Main boost regulator feedback input. FB threshold is 0.6V	
23	GND	P	Digital ground for source	
24	SHL	I	Selects left or right shift (Default=”H”)	Note 1
25	STB	I	Standby mode (Normal operation=”H”, Default setting)	Note 2
26	VCC	PI	Digital power supply for source (+3.3V)	

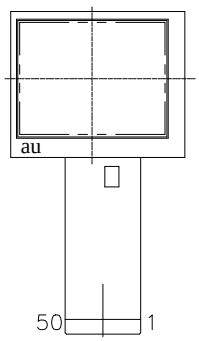
27	SHDB	I	Shutdown input (SHDB="L" DRV_S is off, Default="L")	Note 3
28	AVDD	PI	Analog power supply (+3.3V)	
29	AGND	P	Analog ground	
30	VSYNC	I	Vertical sync input (Negative polarity)	
31	HSYNC	I	Horizontal sync input (Negative polarity)	
32	GND	-	Ground	
33	DCLK	I	Clock Signal	
34	GND	-	Ground	
35	D07	I	Data input (MSB)	
36	D06	I	Data input	
37	D05	I	Data input	
38	D04	I	Data input	
39	D03	I	Data input	
40	D02	I	Data input	
41	D01	I	Data input	
42	D00	I	Data input (LSB)	
43	GND	-	Ground	
44	RSTB	I	Global reset pin (Default="H", Normal operation)	Note 5
45	SEL0	I	Data format selection (Default="L")	Note 4
46	SEL1	I	Data format selection (Default="L")	Note 4
47	SEL2	I	Data format selection (Default="L")	Note 4
48	U/D	I	Shift up or down control. (Default=H")	Note 1
49	Q1H	O	Data sequence control. Data sequence information	
50	VCOM_O	SI	VCOM Output	

I: Digital signal input, O: Digital signal output, P: GND, PI: Power input
C: Power setting capacitor connect pin, FI: Feedback input, PS: Power setting,
SO: VCOM signal output, SI: VCOM_O signal input,

Note 1: Selection of scanning mode

Mode	Setting of scan control input		Scanning direction
	U/D	SHL	
Normal mode	L	H	From up to down, and from left to right.
Reverse mode	H	L	From down to up, and from right to left.

Refer to figure as below:



Note 2: Stand by mode(STB). If STB high, it is normal operation. If it is low, it is standby function. Normally pulled high.

Note 3: Shutdown input (SHDB). Active low, DC-DC converter for White LED is off when SHDB is low, normally pulled low.

Note 4: Interface select pin. Suggest to pull Low for A025CN02 V0 Model.

Note 5: RSTB=”L”, the controller is reset.
RSTB=”H”, normal operation (RSTB should be connected to VCC). Default setting

SEL2	SEL1	SEL0	Data input format	Operating frequency
0	0	0	UPS051 path, special data format : DDX , 8-bits	9.7MHz (NTSC)
0	0	1	UPS051 path, special data format : DDX , 8-bits	9.7MHz (PAL1/6,8)
1	0	0	UPS052 path, normal data format : DIN , 8-bits	24.54MHz (NTSC)
1	0	1	UPS052 path, normal data format : DIN, 8-bits	24.54MHz (PAL1/6,8)

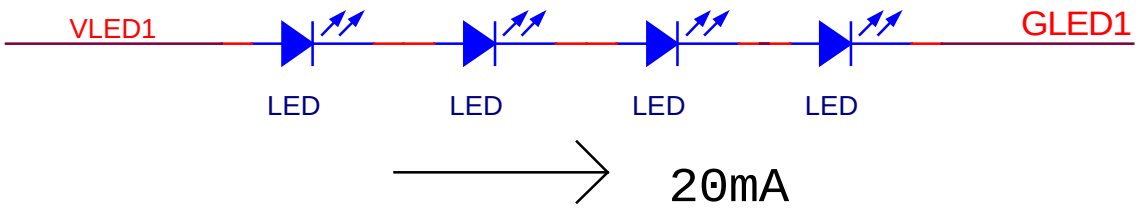
Note 6: Selection of VCAC level

VCSL2	VCSL1	VCSL0	Level (unit:V)
0	0	0	4.4
0	0	1	4.6
0	1	0	4.8
0	1	1	5.0
1	0	0	5.2
1	0	1	5.4
1	1	0	5.6(Default)
1	1	1	5.8

b. LED driving section

No.	Symbol	I/O	Description	Remark
Pin 17	GLED1	-	LED Cathode	
Pin 18	VLED1	-	LED Anode	

Refer to figure as below:



Note 7: A025CN02 V0 SIA (Smart Integration Advanced) solution provides internal PWM driving circuit (for V_{GH}, V_{GL} and LED backlight), application circuit as Fig10. Customer can use these internal driving circuit or provides private power supply as Fig 11~13.

2. Equivalent circuit of I/O

Pin no & Pin name	Schematics
21.DRV_S	TBD
22.FB_S 24.L/R 25.STB 27.SHDB	TBD

30.HSYNC 31.VSYNC 33.DCLK 35.D07 36.D06 37.D05 38.D04 39.D03 40.D02 41.D01 42.D00 44.RSTB 45.SEL0 46.SEL1 47.SEL2 48.U/D	

3. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V_{CC}	GND=0	-0.5	5	V	
	AV_{DD}	AV_{SS}=0	-0.5	7	V	
	V_{GH}	GND=0	13	17	V	
Operating temperature	Topa		0	60	℃	Ambient temperature
Storage temperature	Tstg		-25	80	℃	Ambient temperature

4. Electrical characteristics

a. Typical operating conditions (GND=AVss=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		V_{CC}	2.7	3.3	3.6	V	
		AV_{DD}	3.0	3.3	5	V	
		V_{GH}	14	15	16	V	
		VGoff_H	---	-10+VCAC	---	Vp-p	
		VGoff_L	---	-10	---	V	
VCOM		V_{CAC}	4.4		5.8	Vp-p	AC component, Note 1
		V_{CDC}		TBD		V	Note 2
Output Signal voltage	H Level	V_{OH}	Vcc-0.4			V	
	L Level	V_{OL}	GND		GND+0.4	V	
Input Signal voltage	H Level	V_{IH}	$0.8V_{CC}$	-	V_{CC}	V	
	L Level	V_{IL}	GND	-	$0.2V_{CC}$	V	
DRV output voltage		V_{DRV}	0		VCC	V	
DRV output		IDRV			10	mA	

Feedback voltage		V_{FB}	0.55	0.6	0.65	V	
Output current	H Level	IOH		10		uA	
	L Level	IOL		-10		uA	
Analog stand by current		Ist			200	uA	DCLK is stopped
FRP output current		H Level	I_{OHF}		20	mA	For Vcom circuits.
		L Level	I_{OLF}		20	mA	

Note 1: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.

Note 2: V_{CDC} could be adjusted so as to minimize vertical straight line, flicker and maximum contrast on each module.

b. Current consumption (GND=AVss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Current for driver	I_{GH}	V_{GH}=15V	---	---	1.5	mA	
	I_{CC}	V_{CC}=3.3V	---	3.0	3.5	mA	
	I_{DD}	AV_{DD}=3.3V	---	1.5	2	mA	CLK=9.7MHz

c. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current			20		mA	
LED voltage	V_L			16	V	
LED Life Time	L_L	10000			Hr	Note 1,2

Note 1 : Ta. = 25℃, I_L = 20mA

Note 2 : Brightness to be decreased to 50% of the initial value.

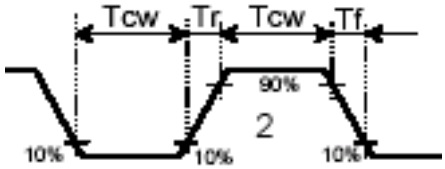
5. AC Timing

a. Timing conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK	Frequency	1/Tvc	-	9.7	-	MHz	
	Duty cycle	Tcw	40	50	60	%	
	Rising time	t_r	-		10	ns	
	Falling time	t_f	-		10	ns	
HSYNC	Period	TH	60	63.56	67	us	Note 2
				617		DCLK	
	Display period	THd		49.4		us	
	Pulse width	THp	5	44		DCLK	
	HSYNC-Clk timing	THc	20		Tvc-20	ns	
Hsync setup time		Thst	12			ns	
Hsync hold time		Thhd	12			ns	
Horizontal lines per field		t_V	256	262	268	t_H	
VSYNC	Period	TV		16.6		ms	Note 2
				262		t_H	

	Display period	TVd		14.83		ms	
	Pulse width	TVp	1			DCLK	
				3		TH	
Vsync setup time		Tvst	12			ns	
Vsync hold time		Tvhd	12			ns	
DATA D00~D07	DCLK-DATA timing	Tds	12	-	-	ns	
	DATA-CLK timing	Tdh	-	-	10	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	

Note 1 DCLK Tr and Tf is defined at 10%~90%. Refer to figure as below:



Note 2: Display position

A.. Horizontal display position

The display starts from the data of (105DCLK, THe=105DCLK) as shown in Fig 5.

(THe : From Hsync falling edge to 1st displayed data.)

B. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		18		TH	NTSC

b. Timing diagram

Please refer to the attached drawing, from Fig.5 to Fig.8.

6. Boost Converter

A025CN02 V0 main boost converter uses a boost PWM architecture to produce a positive regulated voltage, Please refer to the below figures to see the block diagram.

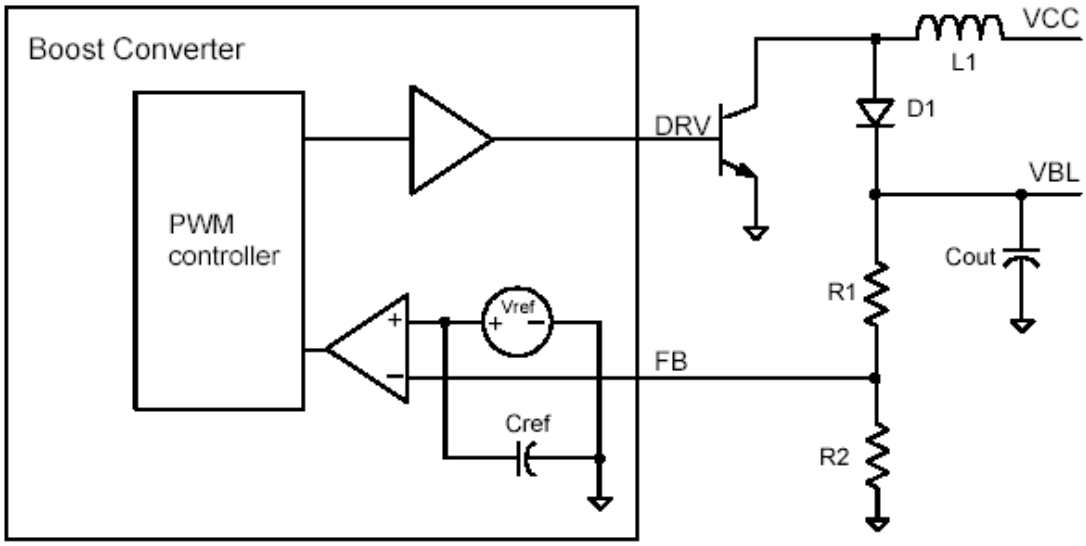


Fig 1 DC-DC converter block diagram

C. Optical specification (Note 1,Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time							
Rise	Tr	θ =0°	-	25	50	ms	Note 4
Fall	Tf		-	30	60	ms	
Contrast ratio	CR	At optimized viewing angle	100	150	-		Note 5,6
Viewing angle							
Top		CR≧10	10	-	-	deg.	Note 7
Bottom			30	-	-		
Left			45	-	-		
Right			45	-	-		
Brightness	Y_L	θ =0°	200	230	-	cd/m^2	Note 8
White chromaticity	X	θ =0°		TBD			
	y	θ =0°		TBD			

Note 1. Ambient temperature =25℃. And backlight current I_L=*20 mA*

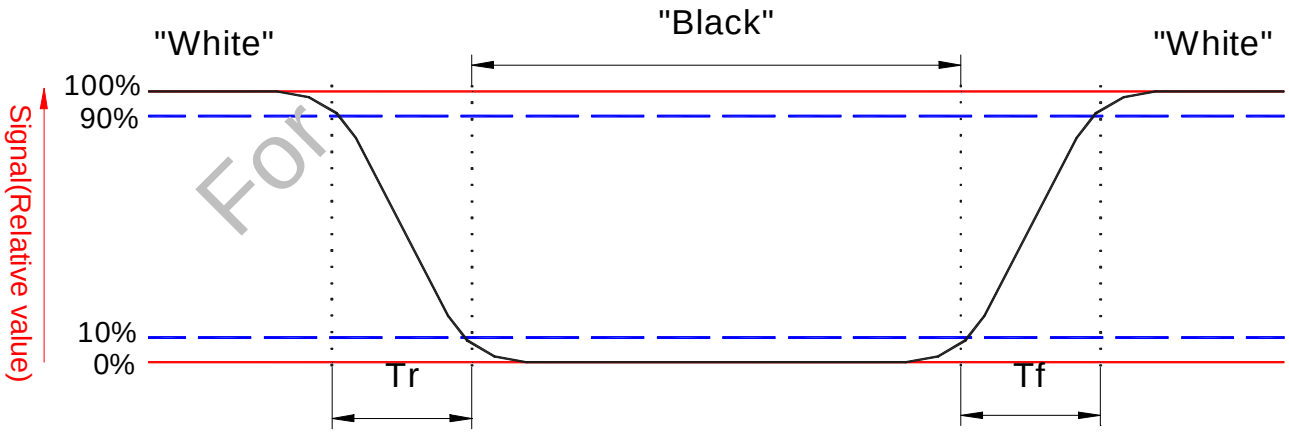
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

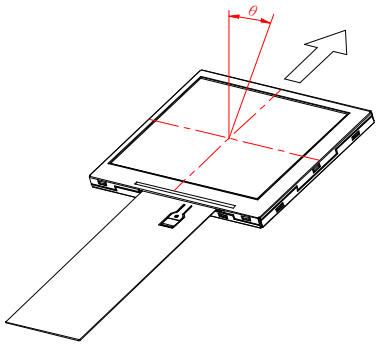
Note 6. White $Vi=V_{i50} \mp 1.5V$

Black $Vi=V_{i50} \pm 2.0V$

“±” Means that the analog input signal swings in phase with COM signal.

"$\overline{}$" Means that the analog input signal swings out of phase with COM signal.
V_{i50} : The analog input voltage when transmission is 50%
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:, refer to figure as below.



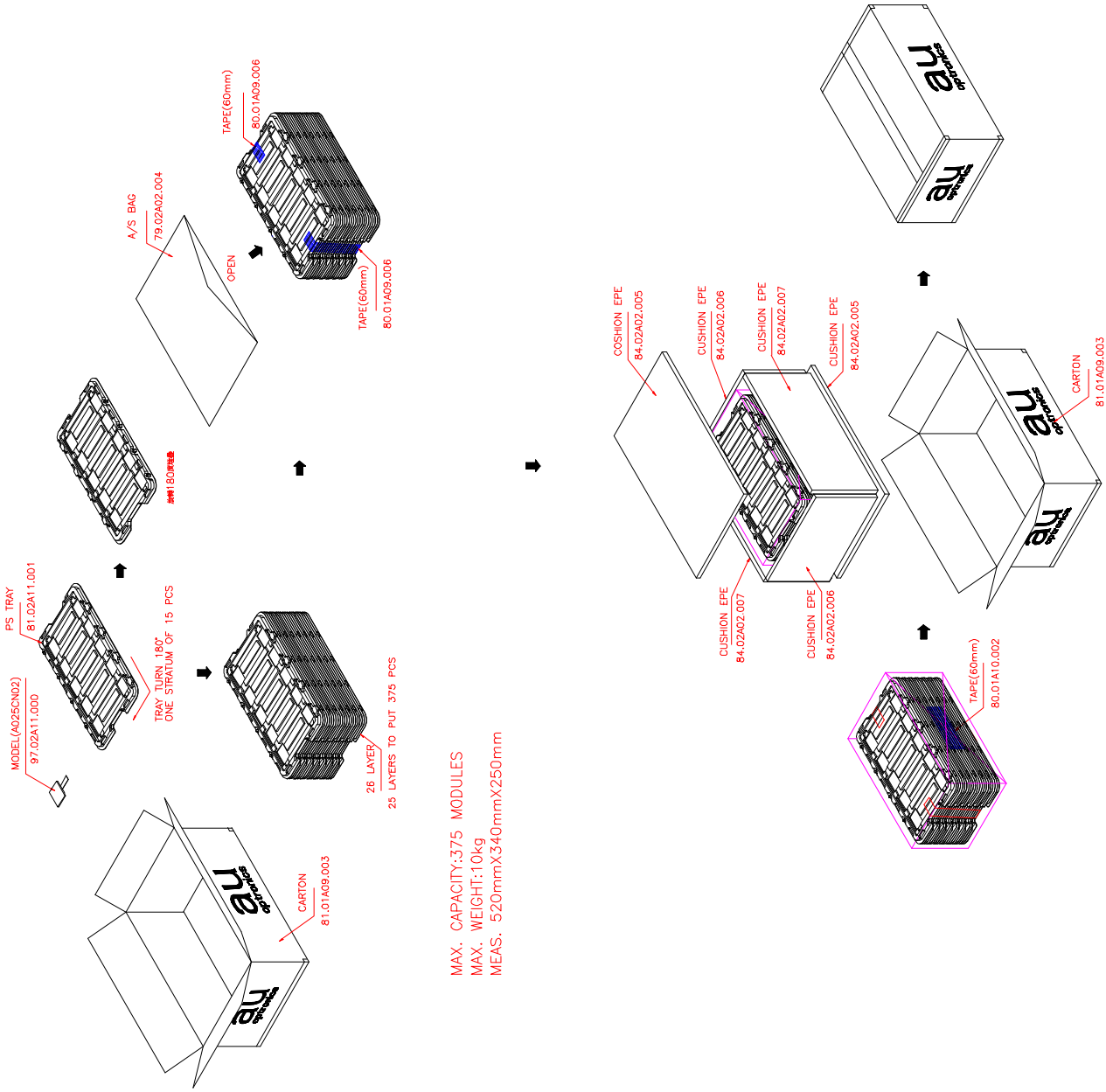
Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

D. Reliability test items:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80℃ 240Hrs	
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note: Ta: Ambient temperature.

E. Packing form



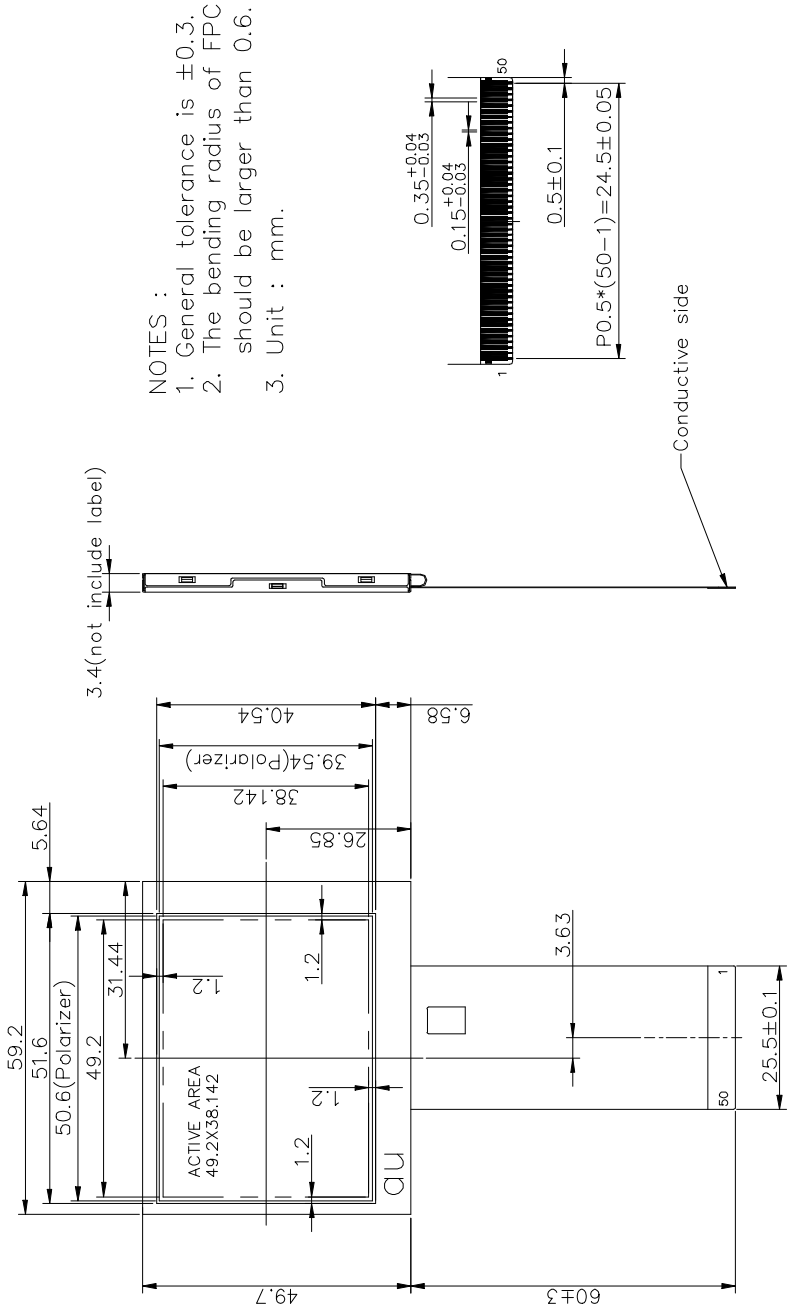


Fig. 4 outline dimension of TFT-LCD module

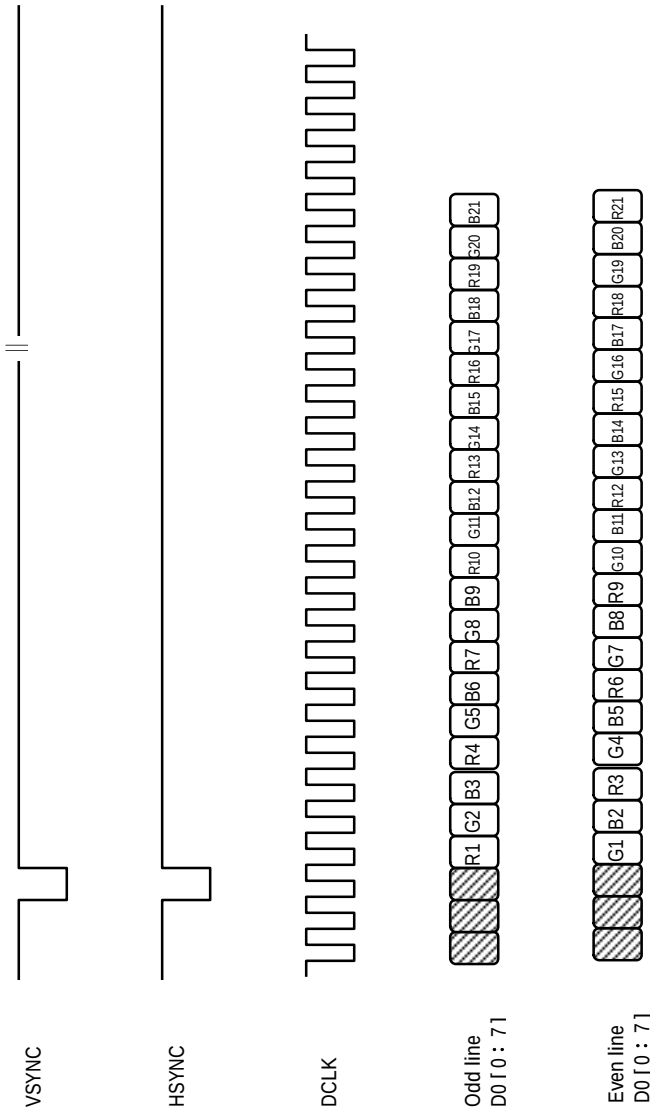


Fig. 5 Input signals timing relationship

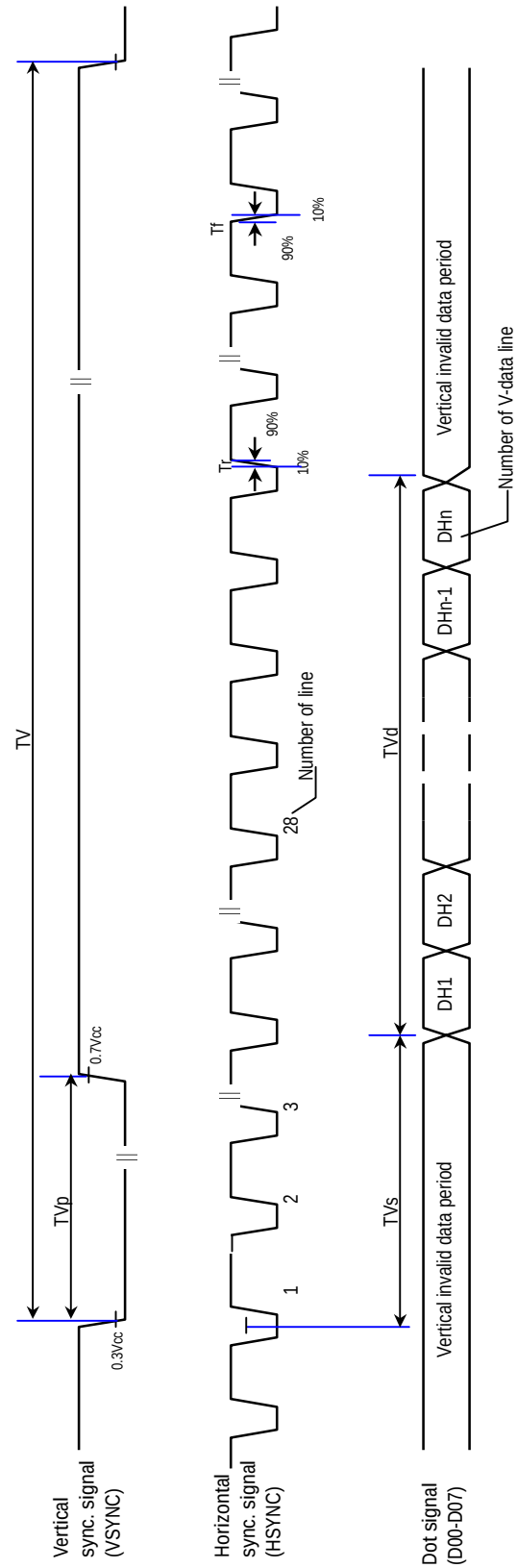


Fig. 6 Input Vertical Timing

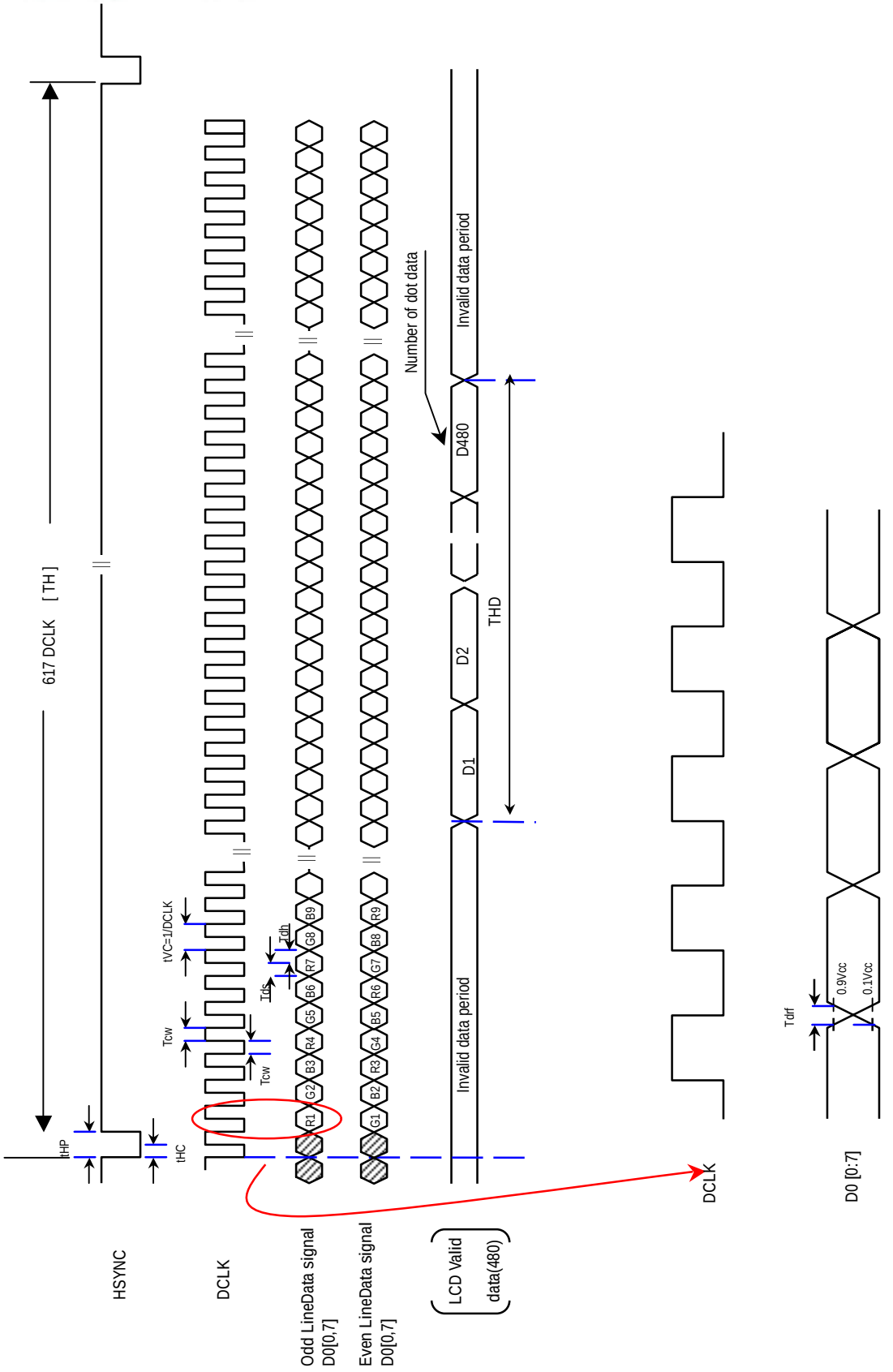


Fig. 7 Horizontal Input Timing

Fig. 8 Extraction of display data from memory to panel

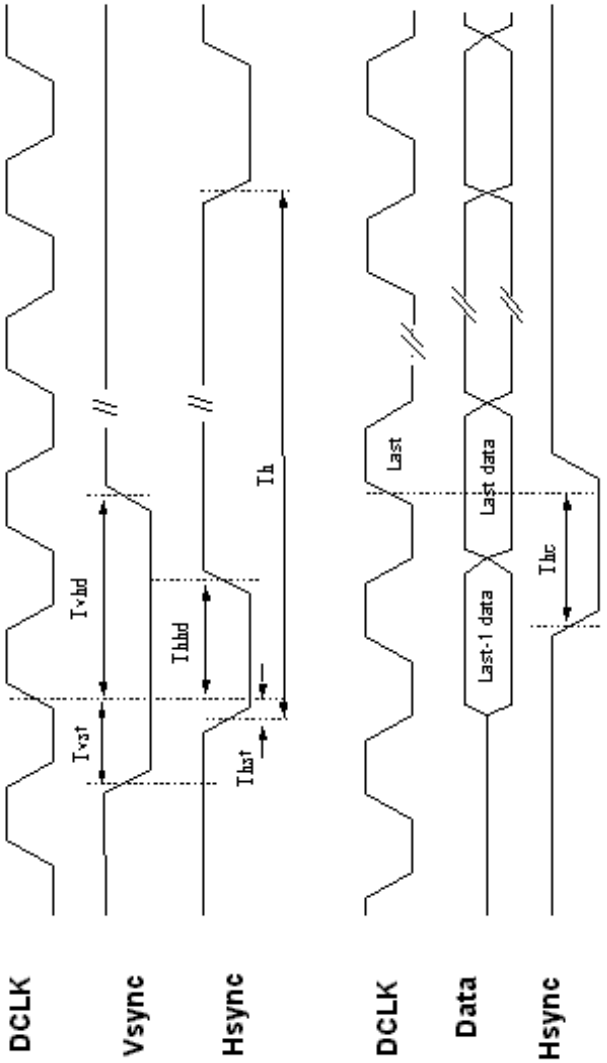
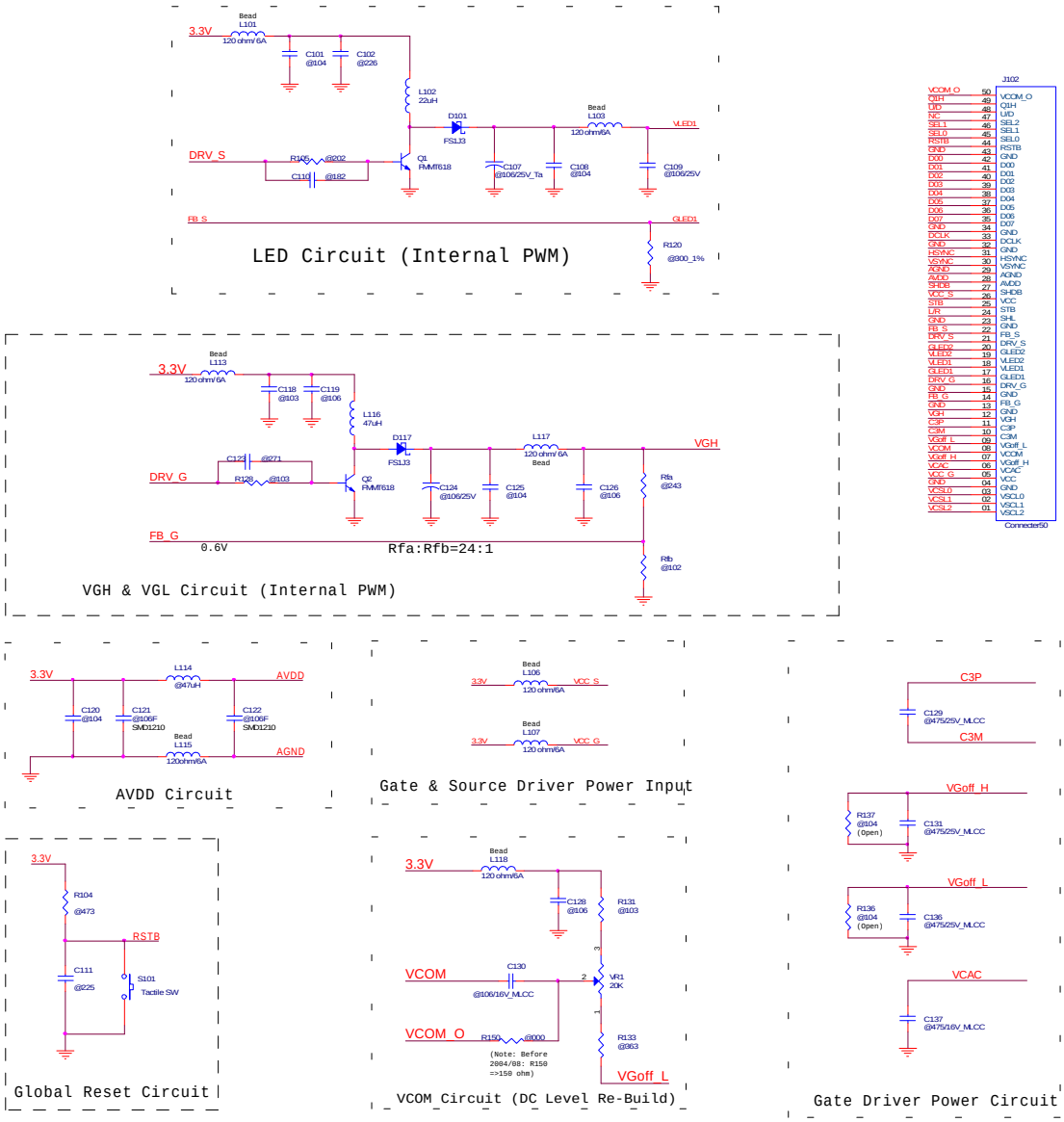
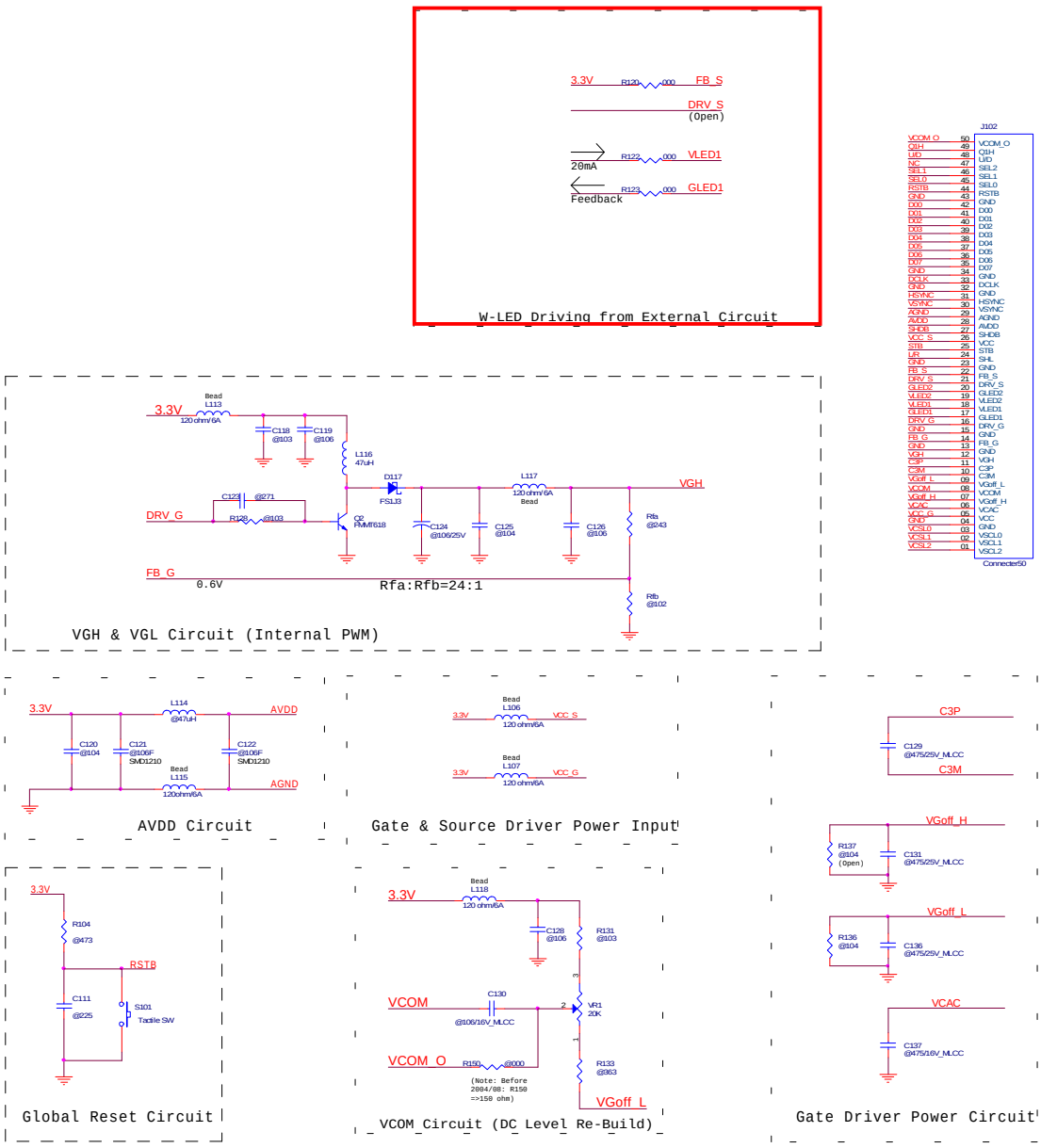


Fig. 9 Hsync, Vsync, Data, DCLk relationship



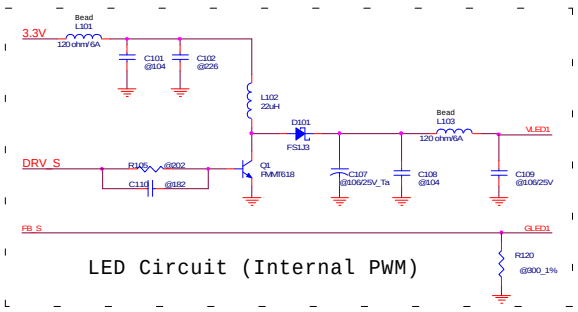
Note: Application circuit for using internal V_{GH} & V_{GL} , LED backlight driving function of drive IC

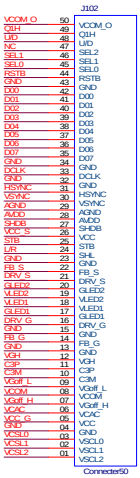
Fig. 10 Typical application circuit

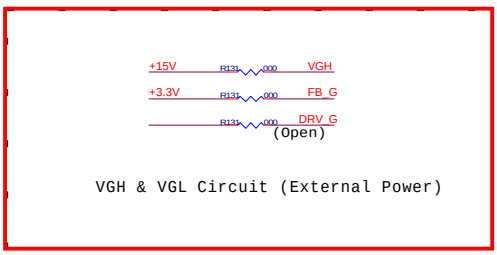


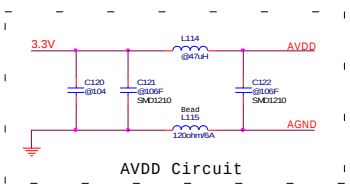
Note: Application circuit for only using internal V_{GH} & V_{GL} driving function of drive IC. Customer provides private LED driving circuit.

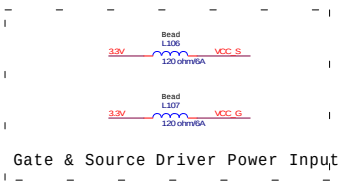
Fig. 11 Application circuit for LED driving circuit unused

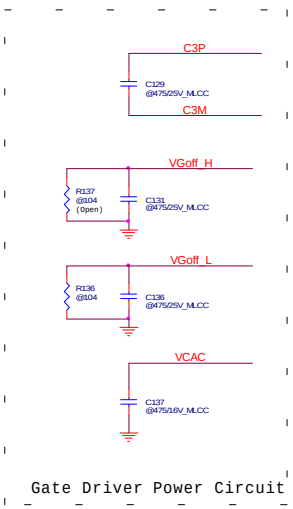


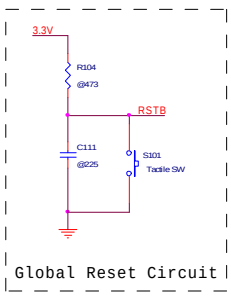


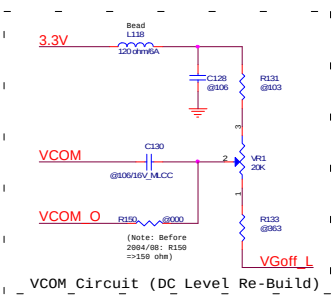






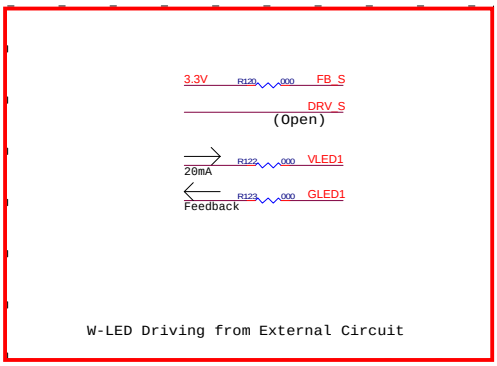


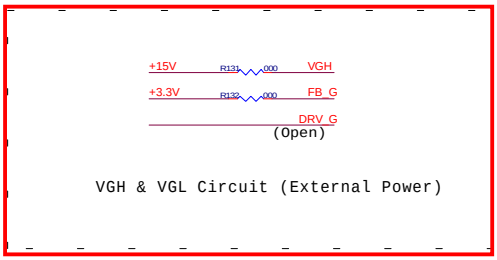


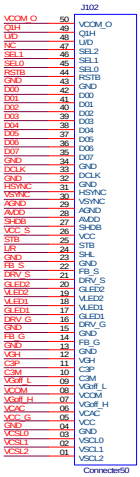


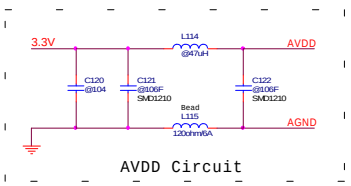
Note: Application circuit for only using internal LED driving function of drive IC. Customer provides private V_{GH} & V_{GL} driving circuit.

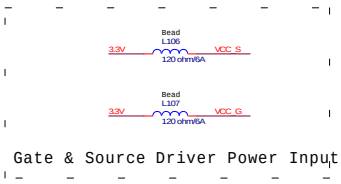
Fig. 12 Application circuit for V_{GH} & V_{GL} driving circuit unused

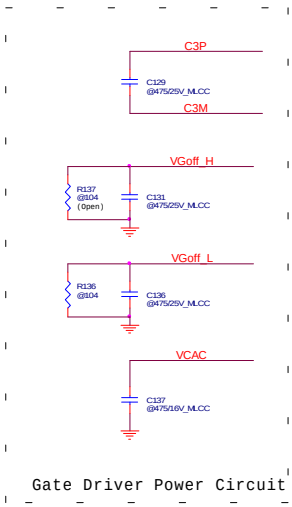


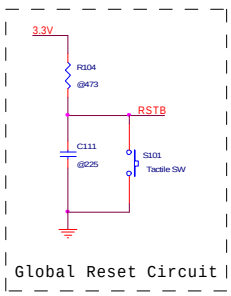


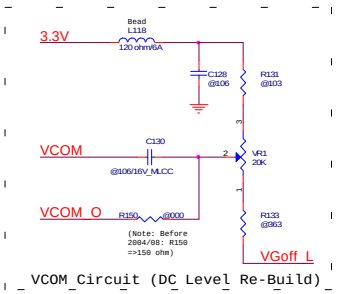












Note: Application circuit for that customer provides private both LED driving V_{GH} & V_{GL} driving circuit.

Fig. 13 Application circuit for both LED dirving and V_{GH} & V_{GL} driving circuit unused