



Product Specification

M238DTN01.0

AU OPTRONICS CORPORATION

(V) Preliminary Specification

() Final Specification

Module	23.8" Color TFT-LCD
Model Name	M238DTN01.0

<table><tr><td>Customer</td><td>Date</td></tr><tr><td>_____</td><td>_____</td></tr><tr><td>Approved by</td><td></td></tr><tr><td>_____</td><td>_____</td></tr></table>	Customer	Date	_____	_____	Approved by		_____	_____	<table><tr><td>Approved by</td><td>Date</td></tr><tr><td>_____</td><td><u>Aug. 05, 2015</u></td></tr><tr><td>Prepared by</td><td>Date</td></tr><tr><td>_____</td><td><u>Aug. 05, 2015</u></td></tr></table>	Approved by	Date	_____	<u>Aug. 05, 2015</u>	Prepared by	Date	_____	<u>Aug. 05, 2015</u>
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Note: This Specification is subject to change without notice.	AU Optronics corporation																



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Record of Revision

[illegible]

1 Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case a TFT-LCD Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lightbar edge. Otherwise the TFT-LCD Module may be damaged.
- 10) Insert or pull out the interface connector, be sure not to rotate nor tilt it of the TFT-LCD Module.
- 11) Do not twist nor bend the TFT -LCD Module even momentary. It should be taken into consideration that no bending/twisting forces are applied to the TFT-LCD Module from outside. Otherwise the TFT-LCD Module may be damaged.
- 12) Please avoid touching COF position while you are doing mechanical design.
- 13) When storing modules as spares for a long time, the following precaution is necessary:
Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5 and 35 at normal humidity.



2 General Description

This specification applies to the 23.8 inch wide Color a-Si TFT-LCD Module M238DTN01.0. The display supports the QHD - 2560(H) x 1440(V) screen format and 16.7M colors (RGB 8-bit data). The input interface is 8 port LVDS and this module doesn't contain an driver board for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	23.8"
Active Area	[mm]	526.85 (H) x 296.35 (V)
Pixels H x V	-	2560(x3) x 1440
Pixel Pitch	[um]	205.8 (per one triad) x205.8
Pixel Arrangement	-	R.G.B. Vertical Stripe
Display Mode	-	TN Mode, Normally White
White Luminance (Center)	[cd/m	
Contrast Ratio	-	1000 (Typ.)
Response Time	[msec]	5 (Typ., on/off)
Power Consumption (LCD Module + Backligh unit)		LCD module : PDD (Typ.)=6.5 W @ Black pattern,Fv=144Hz Backlight unit : P (Typ.) =14.9 @Is=80mA
Weight	[Grams]	
Outline Dimension	[mm]	543.0(H) x 317.4(V) x 11.9(D) Typ.
Electrical Interface	-	8 port LVDS
Support Color	-	16.7M colors (RGB 8-bits)
Surface Treatment	-	Anti-Glare, 3H
RoHS Compliance	-	RoHS Compliance
TCO Compliance	-	TCO 6.0 Compliance

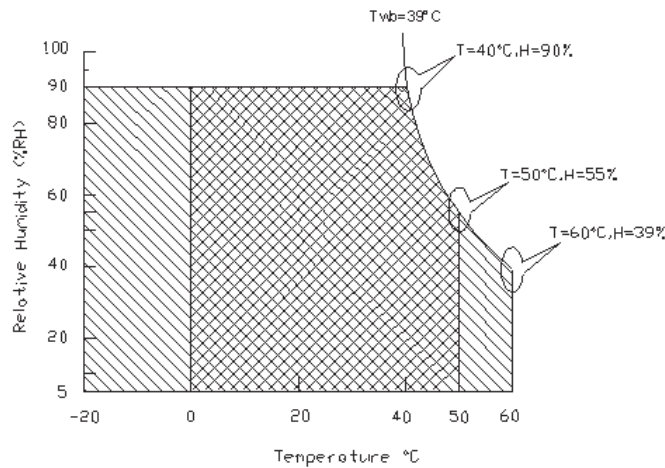
2.2 Absolute Maximum Rating of Environment

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	Note 2-1
TGS	Glass surface temperature (operation)	0	+65	[°C]	Note 2-1 Function judged only
HOP	Operation Humidity	5	90	[%RH]	Note 2-1
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-1: Temperature and relative humidity range are shown as the below figure.

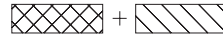
1. 90% RH Max ($T_a \leq 39^{\circ}\text{C}$)
2. Max wet-bulb temperature at 39°C or less. ($T_a \leq 39^{\circ}\text{C}$)
3. No condensation



Operating Range



Storage Range





2.3 Optical Characteristics

The optical characteristics are measured on the following test condition.

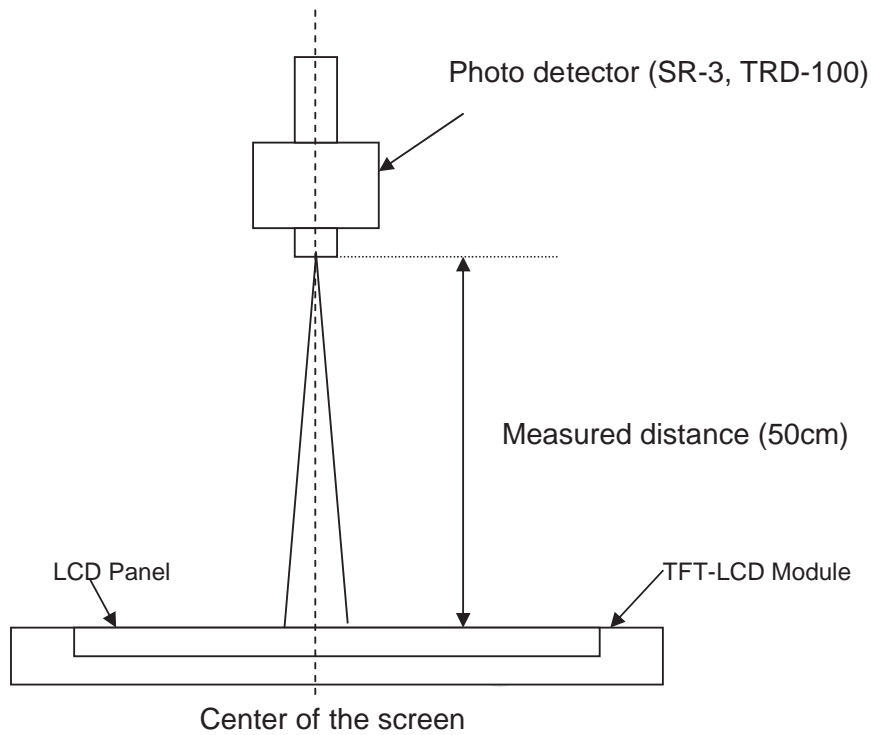
Test Condition:

1. Equipment setup: Please refer to **Note 2-2**.
2. Panel Lighting time: 30 minutes
3. VDD=12.0V, Fv=120Hz, **Is=80mA**, Ta=25°C

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
L _w	White Luminance (Center of screen)		300	350	-	[cd/m2]	Note 2-2 By SR-3
L _{uni}	Luminance Uniformity (9 points)		75	80	-	[%]	Note 2-3 By SR-3
CR	Contrast Ratio (Center of screen)		600	1000	-	-	Note 2-4 By SR-3
θ _R	Horizontal Viewing Angle (CR=10)	Right	75	85	-	[degree]	Note 2-5 By SR-3
θ _L		Left	75	85	-		
Φ _H	Vertical Viewing Angle (CR=10)	Up	70	80	-		
Φ _L		Down	70	80	-		
θ _R	Horizontal Viewing Angle (CR=5)	Right	75	88	-		
θ _L		Left	75	88	-		
Φ _H	Vertical Viewing Angle (CR=5)	Up	70	85	-		
Φ _L		Down	70	85	-		
T _R	Response Time	Rising Time	-	3.5	5.5	[msec]	Note 2-6 By TRD-100
T _F		Falling Time	-	1.5	2.5		
-		Rising + Falling	-	5	8		
R _x	Color Coordinates (CIE 1931)	Red x	TBD	TBD	TBD	-	By SR-3
R _y		Red y	TBD	TBD	TBD		
G _x		Green x	TBD	TBD	TBD		
G _y		Green y	TBD	TBD	TBD		
B _x		Blue x	TBD	TBD	TBD		
B _y		Blue y	TBD	TBD	TBD		
W _x		White x	0.283	0.313	0.343		
W _y		White y	0.299	0.329	0.359		
NTSC				72		[%]	By SR-3
CT Crosstalk			-	-	1.5	[%]	Note 2-7 By SR-3

F _{dB}	Flicker (Center of screen)	-	-	-20	[dB]	Note 2-8 By SR-3
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Note 2-2: Equipment setup :

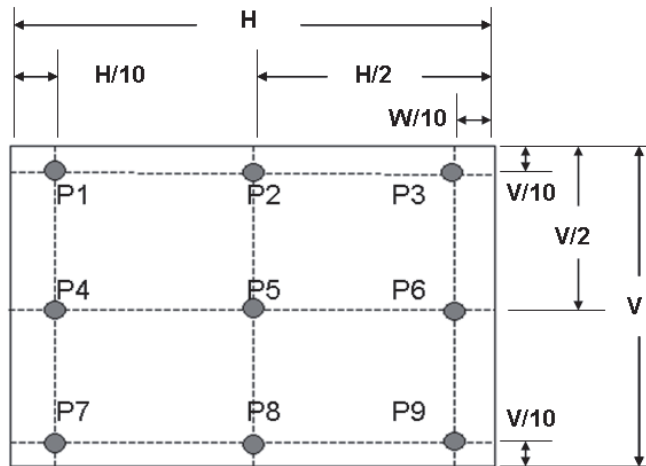


Note 2-3: Luminance Uniformity Measurement

Definition:

$$\text{Luminance Uniformity} = \frac{\text{Minimum Luminance of 9 Points (P1 ~ P9)}}{\text{Maximum Luminance of 9 Points (P1 ~ P9)}}$$

a. Test pattern: White Pattern



Note 2-4: Contrast Ratio Measurement

Definition:

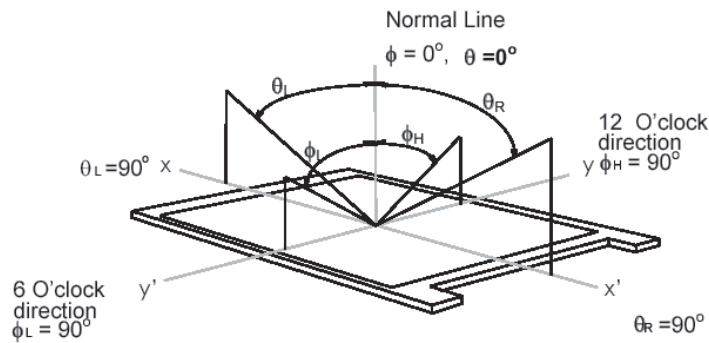
$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

- Measured position: Center of screen (P5) & perpendicular to the screen ($\theta = \Phi = 0^\circ$)

Note 2-5: Viewing angle measurement

Definition: The angle at which the contrast ratio is greater than 10 & 5 .

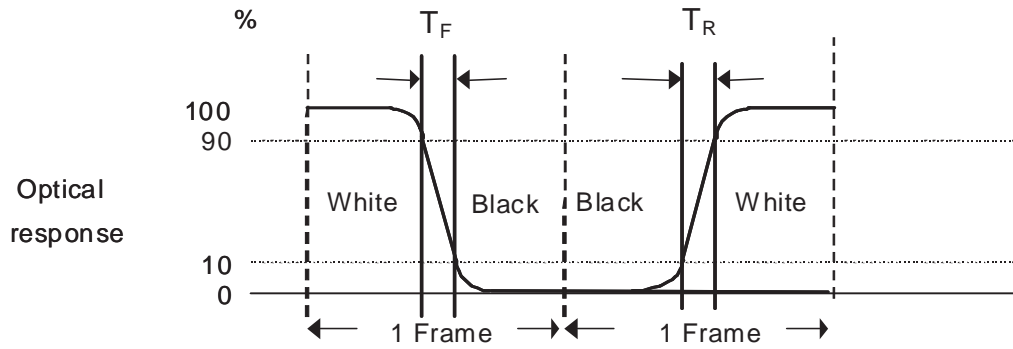
- Horizontal view angle: Divide to left & right (
- Vertical view angle: Divide to up & down (



Note 2-6: Response time measurement



The output signals of photo detector are measured when the input signals are changed from “Black” to “White” (rising time, T_R), and from “White” to “Black” (falling time, T_F), respectively. The response time is interval between the 10% and 90% of optical response. (*Black & White color definition: Please refer section 3.4.3*)



Note 2-7: Crosstalk measurement

Definition:

$$CT = \text{Max. } (CT_H, CT_V);$$

Where

a. Maximum Horizontal Crosstalk :

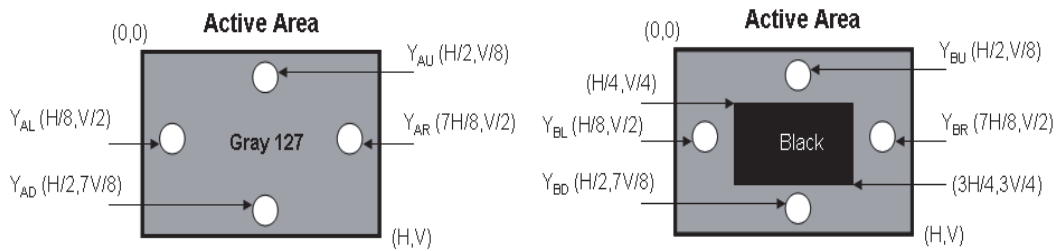
$$CT_H = \text{Max. } (|Y_{BL} - Y_{AL}| / Y_{AL} \times 100 \%, |Y_{BR} - Y_{AR}| / Y_{AR} \times 100 \%, |Y_{BU} - Y_{AU}| / Y_{AU} \times 100 \%, |Y_{BD} - Y_{AD}| / Y_{AD} \times 100 \%)$$

Maximum Vertical Crosstalk:

$$CT_V = \text{Max. } (|Y_{BU} - Y_{AU}| / Y_{AU} \times 100 \%, |Y_{BD} - Y_{AD}| / Y_{AD} \times 100 \%, |Y_{BL} - Y_{AL}| / Y_{AL} \times 100 \%, |Y_{BR} - Y_{AR}| / Y_{AR} \times 100 \%)$$

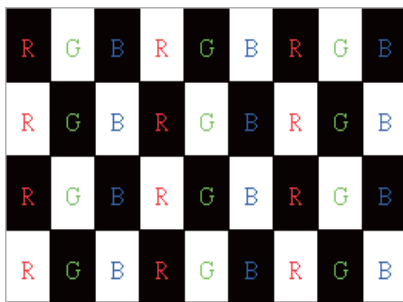
b. $Y_{AU}, Y_{AD}, Y_{AL}, Y_{AR}$ = Luminance of measured location without Black pattern

$Y_{BU}, Y_{BD}, Y_{BL}, Y_{BR}$ = Luminance of measured location with Black pattern



Note 2-8: Flicker measurement

a. Test pattern: It is listed as following.



Gray level = L0

Gray level = L127

b. Measured position: Center of screen (P5) & perpendicular to the screen ($\theta=\Phi=0^\circ$)

2.4 Mechanical Characteristics

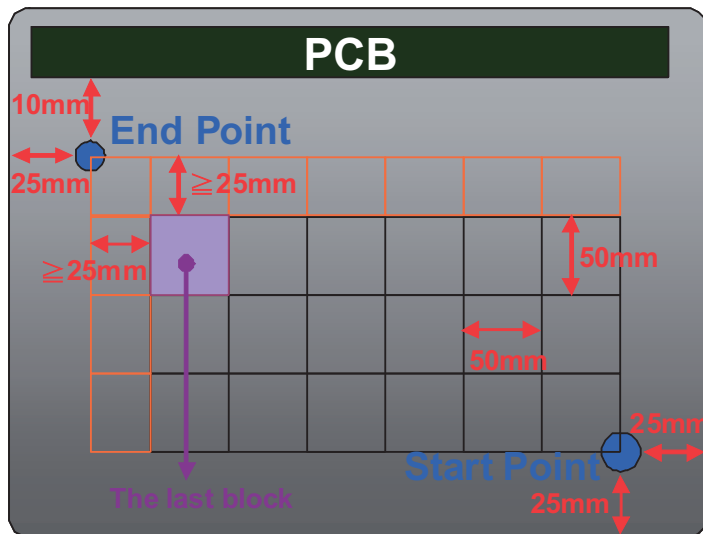
Symbol	Description	Min.	Max.	Unit	Remark
P_{bc}	Backside Compression	2.5	-	[Kgf]	<i>Note 2-9</i>

Note 2-9: Test Method:

The point is at a distance from right-downside 25mm x 25mm defined as the Start Point of Measure Points, and the point is at a distance 25mm from left-side & around 10mm from PCB defined as the End Point.

Align 50mm x 50mm block from Start Point on the Bezel Back, and the corners of each block are Measure Points.

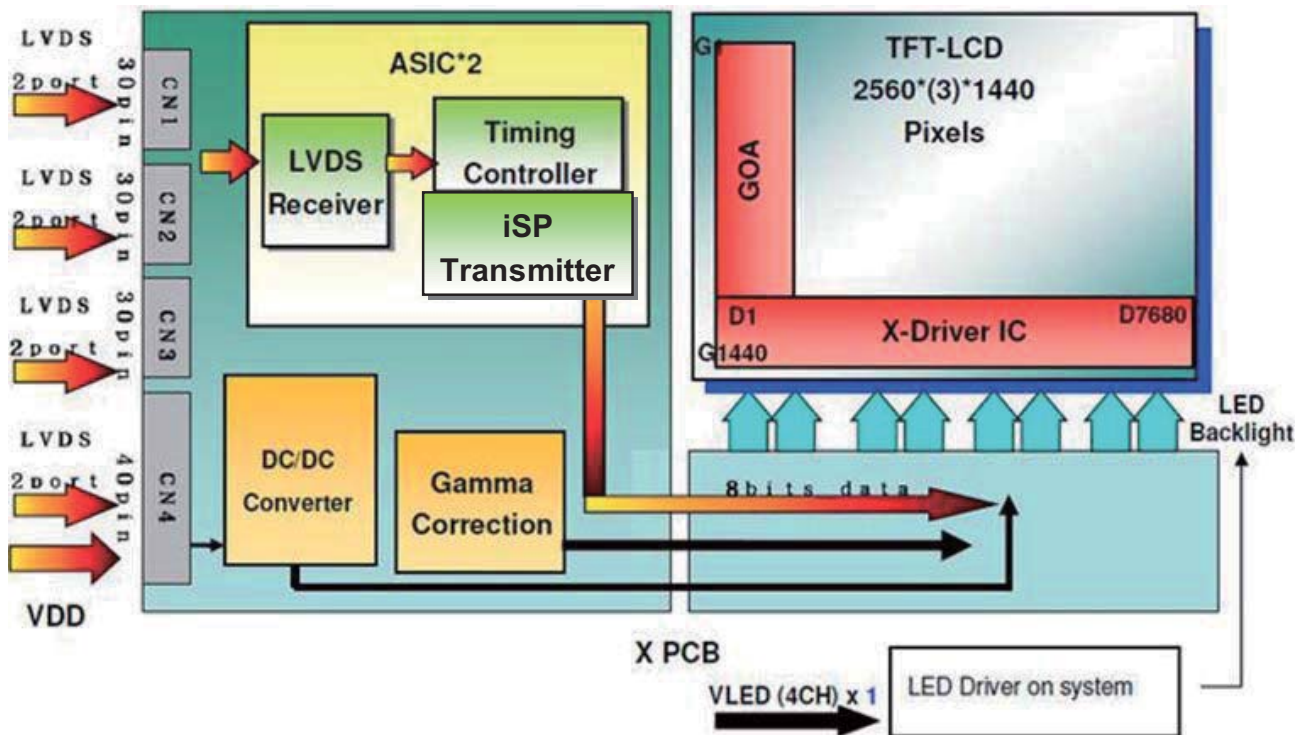
If the distance from the last block to each side of the End Point 25mm, add other blocks to make sure that most area of Bezel Back can be measured.



3 TFT-LCD Module

3.1 Block Diagram

The following shows the block diagram of the 23.8 inch Color TFT-LCD Module.





3.2 Interface Connection

3.2.1 Connector Type

TFT-LCD Connector (CNT1/2/3)	Manufacturer	STM	P-TWO
	Part Number	MSBKT2407P30HB	
TFT-LCD Connector (CNT4)	Manufacturer	Starconn	Fullconn
	Part Number	115F40-S000RA-M3	WF01-415-4032
Mating Connector (CNT1/2/3)	Manufacturer	STM or Compatible	
	Part Number	PK2407P30V or Compatible	
Mating Connector (CNT4)	Manufacturer	JAE or Compatible	
	Part Number	FI-NX40HL or Compatible	

3.2.2 Connector Pin Assignment

CN 1

PIN #	Symbol	Description	Remark
1	R1 0N	Negative LVDS differential data in Port1 data)	
2	R1 0P	Positive LVDS differential data in Port1 data)	
3	R1 1N	Negative LVDS differential data in Port1 data)	
4	R1 1P	Positive LVDS differential data in Port1 data)	
5	R1 2N	Negative LVDS differential data in Port1 data)	
6	R1 2P	Positive LVDS differential data input (Port1 data)	
7	GND	Ground	
8	R1 CLKN	Negative LVDS differential clock input (Port1 clock)	
9	R1 CLKP	Positive LVDS differential clock input (Port1 clock)	
10	GND	Ground	
11	R1 3N	Negative LVDS differential data input (Port1 data)	
12	R1 3P	Positive LVDS differential data input (Port1 data)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	GND	Ground	
16	R2 0N	Negative LVDS differential data input (Port2 data)	
17	R2 0P	Positive LVDS differential data input (Port2 data)	
18	R2 1N	Negative LVDS differential data input (Port2 data)	
19	R2 1P	Positive LVDS differential data input (Port2 data)	



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20	R2_2N	Negative LVDS differential data input (Port2 data)	
21	R2_2P	Positive LVDS differential data input (Port2 data)	
22	GND	Ground	
23	R2_CLKN	Negative LVDS differential clock input (Port2 clock)	
24	R2_CLKP	Positive LVDS differential clock input (Port2 clock)	
25	GND	Ground	
26	R2_3N	Negative LVDS differential data input (Port2 data)	
27	R2_3P	Positive LVDS differential data input (Port2 data)	
28	NC	No connection (for AUO test only. Do not connect)	
29	NC	No connection (for AUO test only. Do not connect)	
30	NC	No connection (for AUO test only. Do not connect)	

CN 2

PIN #	Symbol	Description	Remark
1	R3_0N	Negative LVDS differential data in Port3 data)	
2	R3_0P	Positive LVDS differential data in Port3 data)	
3	R3_1N	Negative LVDS differential data in ut (Port3 data)	
4	R3_1P	Positive LVDS differential data input (Port3 data)	
5	R3_2N	Negative LVDS differential data input (Port3 data)	
6	R3_2P	Positive LVDS differential data input (Port3 data)	
7	GND	Ground	
8	R3_CLKN	Negative LVDS differential clock input (Port3 clock)	
9	R3_CLKP	Positive LVDS differential clock input (Port3 clock)	
10	GND	Ground	
11	R3_3N	Ne ative LVDS differential data input (Port3 data)	
12	R3_3P	Positive LVDS differential data input (Port3 data)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	GND	Ground	
16	R4_0N	Negative LVDS differential data input (Port4 data)	
17	R4_0P	Positive LVDS differential data input (Port4 data)	
18	R4_1N	Negative LVDS differential data input (Port4 data)	
19	R4_1P	Positive LVDS differential data input (Port4 data)	
20	R4_2N	Negative LVDS differential data input (Port4 data)	
21	R4_2P	Positive LVDS differential data input (Port4 data)	
22	GND	Ground	
23	R4_CLKN	Negative LVDS differential clock input (Port4 clock)	
24	R4_CLKP	Positive LVDS differential clock input (Port4 clock)	



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25	GND	Ground	
26	R4 3N	Negative LVDS differential data input (Port4 data)	
27	R4 3P	Positive LVDS differential data input (Port4 data)	
28	NC	No connection (for AUO test only. Do not connect)	
29	NC	No connection (for AUO test only. Do not connect)	
30	IMS POL	Interlace Mode Selection Polarity (O)	

CN 3

PIN #	Symbol	Description	Remark
1	R5 0N	Negative LVDS differential data input (Port5 data)	
2	R5 0P	Positive LVDS differential data input (Port5 data)	
3	R5 1N	Negative LVDS differential data input (Port5 data)	
4	R5 1P	Positive LVDS differential data input (Port5 data)	
5	R5 2N	Negative LVDS differential data input (Port5 data)	
6	R5 2P	Positive LVDS differential data input (Port5 data)	
7	GND	Ground	
8	R5 CLKN	Negative LVDS differential clock input (Port5 clock)	
9	R5 CLKP	Positive LVDS differential clock input (Port5 clock)	
10	GND	Ground	
11	R5 3N	Negative LVDS differential data input (Port5 data)	
12	R5 3P	Positive LVDS differential data input (Port5 data)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	GND	Ground	
16	R6 0N	Negative LVDS differential data input (Port6 data)	
17	R6 0P	Positive LVDS differential data input (Port6 data)	
18	R6 1N	Negative LVDS differential data input (Port6 data)	
19	R6 1P	Positive LVDS differential data input (Port6 data)	
20	R6 2N	Negative LVDS differential data input (Port6 data)	
21	R6 2P	Positive LVDS differential data input (Port6 data)	
22	GND	Ground	
23	R6 CLKN	Negative LVDS differential clock input (Port6 clock)	
24	R6 CLKP	Positive LVDS differential clock input (Port6 clock)	
25	GND	Ground	
26	R6 3N	Negative LVDS differential data input (Port6 data)	
27	R6 3P	Positive LVDS differential data input (Port6 data)	
28	NC	No connection (for AUO test only. Do not connect)	
29	NC	No connection (for AUO test only. Do not connect)	
30	IMS	Interlace Mode Selection (I)	



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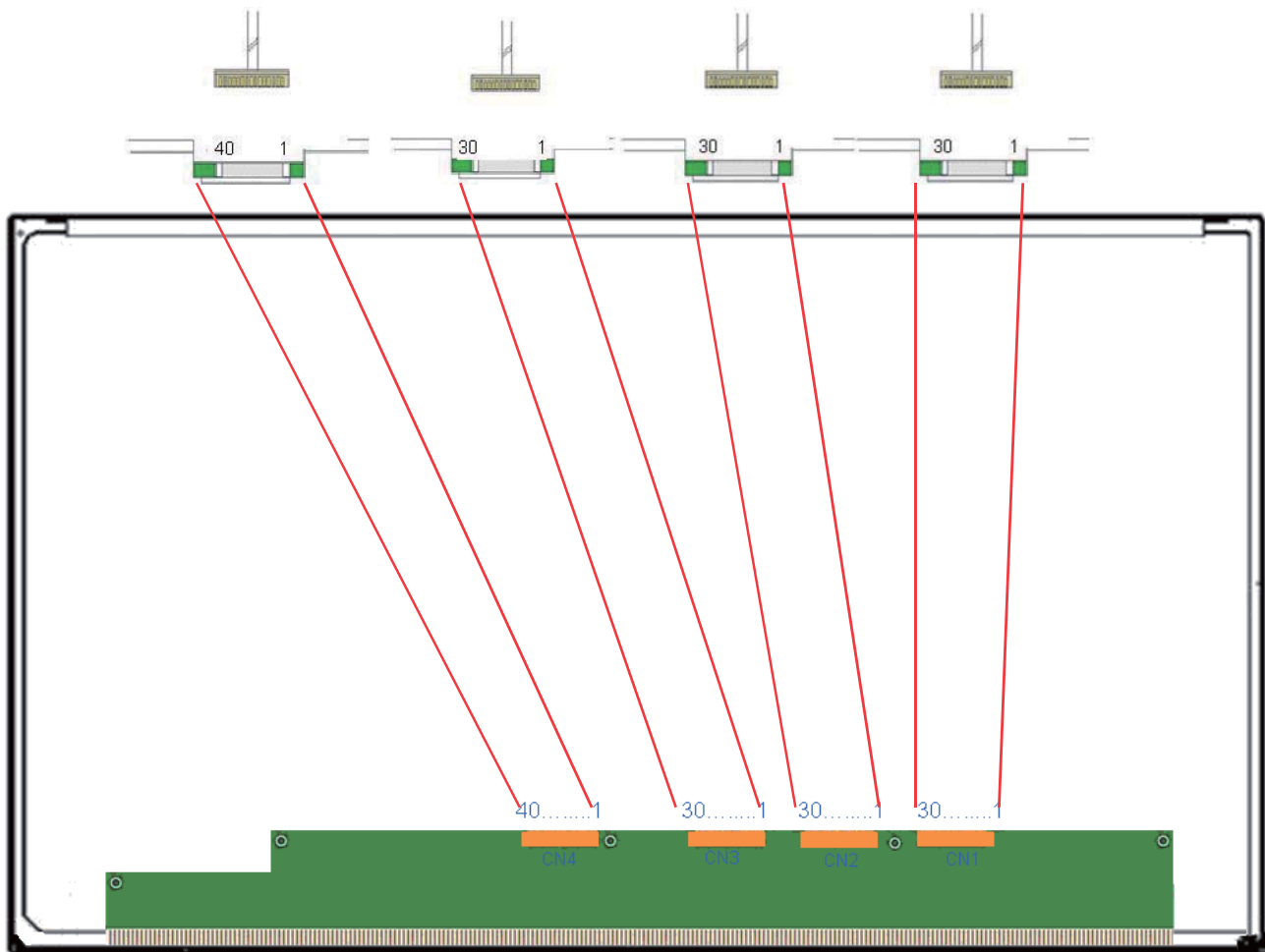
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CN 4

PIN #	Symbol	Description	Remark
1	R7_0N	Negative LVDS differential data input (Port7 data)	
2	R7_0P	Positive LVDS differential data input (Port7 data)	
3	R7_1N	Negative LVDS differential data input (Port7 data)	
4	R7_1P	Positive LVDS differential data input (Port7 data)	
5	R7_2N	Negative LVDS differential data input (Port7 data)	
6	R7_2P	Positive LVDS differential data input (Port7 data)	
7	GND	Ground	
8	R7_CLKN	Negative LVDS differential clock input (Port7 clock)	
9	R7_CLKP	Positive LVDS differential clock input (Port7 clock)	
10	GND	Ground	
11	R7_3N	Negative LVDS differential data input (Port7 data)	
12	R7_3P	Positive LVDS differential data input (Port7 data)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	GND	Ground	
16	R8_0N	Negative LVDS differential data input (Port8 data)	
17	R8_0P	Positive LVDS differential data input (Port8 data)	
18	R8_1N	Negative LVDS differential data input (Port8 data)	
19	R8_1P	Positive LVDS differential data input (Port8 data)	
20	R8_2N	Negative LVDS differential data input (Port8 data)	
21	R8_2P	Positive LVDS differential data input (Port8 data)	
22	GND	Ground	
23	R8_CLKN	Negative LVDS differential clock input (Port8 clock)	
24	R8_CLKP	Positive LVDS differential clock input (Port8 clock)	
25	GND	Ground	
26	R8_3N	Negative LVDS differential data input (Port8 data)	
27	R8_3P	Positive LVDS differential data input (Port8 data)	
28	NC	No connection (for AUO test only. Do not connect)	
29	NC	No connection (for AUO test only. Do not connect)	
30	NC	No connection (for AUO test only. Do not connect)	
31	NC	No connection (for AUO test only. Do not connect)	
32	NC	No connection (for AUO test only. Do not connect)	
33	NC	No connection (for AUO test only. Do not connect)	
34	GND	Ground	
35	GND	Ground	

36	NC	No connection (for AUO test only. Do not connect)	
37	VDD	Power Supply Input Voltage	
38	VDD	Power Supply Input Voltage	
39	VDD	Power Supply Input Voltage	
40	VDD	Power Supply Input Voltage	



3.3 Electrical Characteristics

3.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

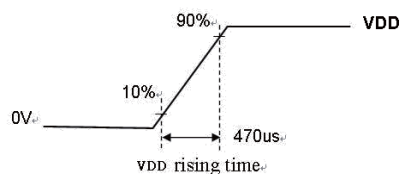
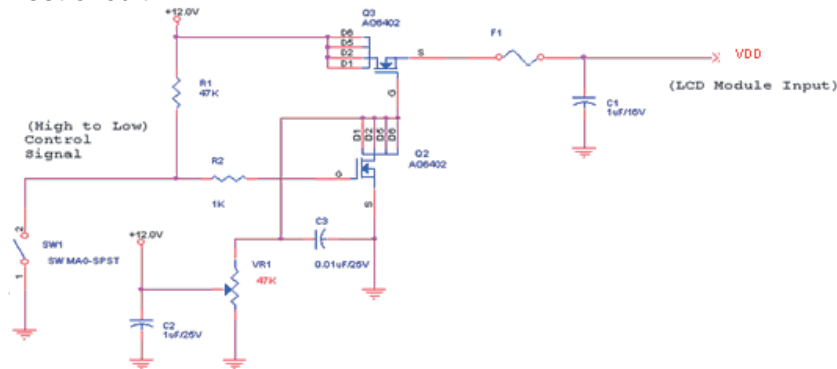
Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14	[Volt]	Ta=25°C

3.3.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power supply Input voltage	10.8	12.0	13.2	[Volt]	
IDD	Power supply Input Current (RMS)	-	TBD	TBD	[A]	VDD= 12 V, Black Pattern, Fv=120Hz
			TBD	TBD	[A]	VDD= 12 V, Black Pattern, Fv=145Hz
PDD	VDD Power Consumption	-	TBD	TBD	[Watt]	VDD= 12 V, Black Pattern, Fv=120Hz
			TBD	TBD	[Watt]	VDD= 12 V, Black Pattern, Fv=145Hz
IRush	Inrush Current	-	-	3.0	[A]	Note 3-1
VDDrp	Allowable VDD Ripple Voltage	-	-	500	[mV]	VDD= 12 V, Black Pattern, Fv=145Hz

Note 3-1: Inrush Current measurement:

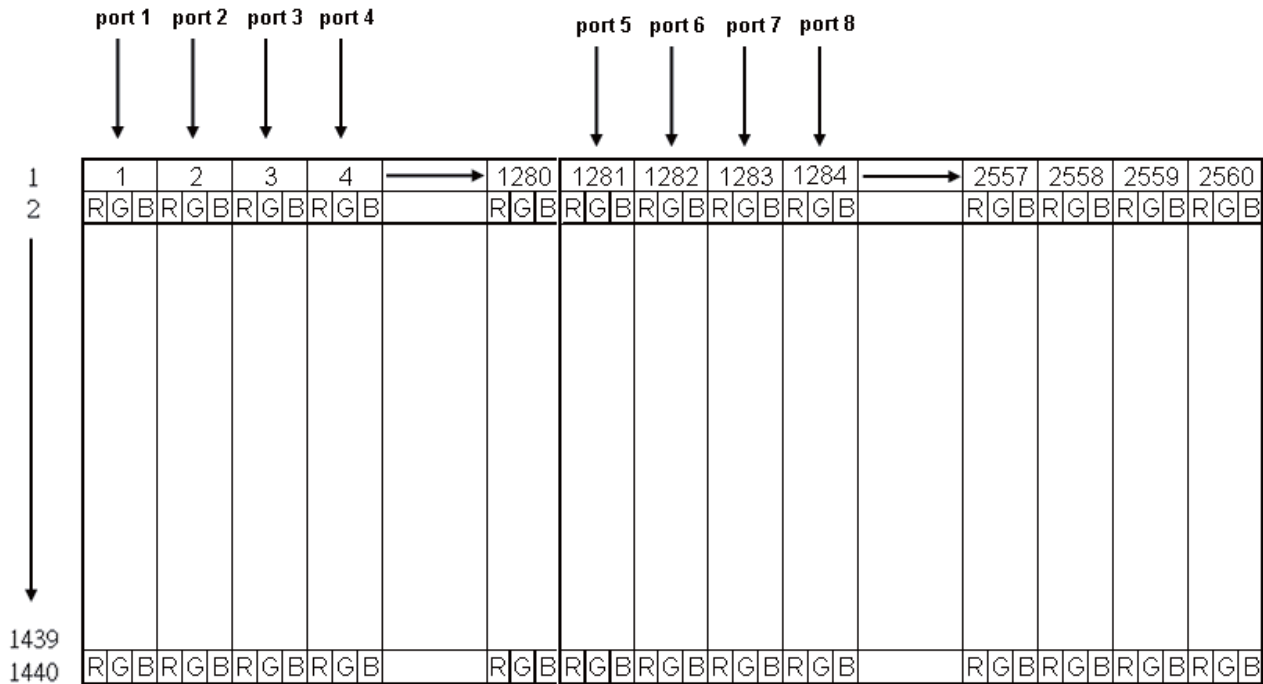
Test circuit:



The duration of VDD rising time: 470us.

3.4 Signal Characteristics

3.4.1 LCD Pixel Format



Note 3-2: The module use 8 port-LVDS interface.

Port 1 : $4N+1$ $N=0, \sim 319$ (1,5.. 1277pixel)

Port 2 : $4N+2$ $N=0, \sim 319$ (2,6.. 1278pixel)

Port 3 : $4N+3$ $N=0, \sim 319$ (3,7.. 1279pixel)

Port 4 : $4N+4$ $N=0, \sim 319$ (4,8.. 1280pixel)

Port 5 : $4N+1281$ $N=0, \sim 319$ (1281,1285.. 2557pixel)

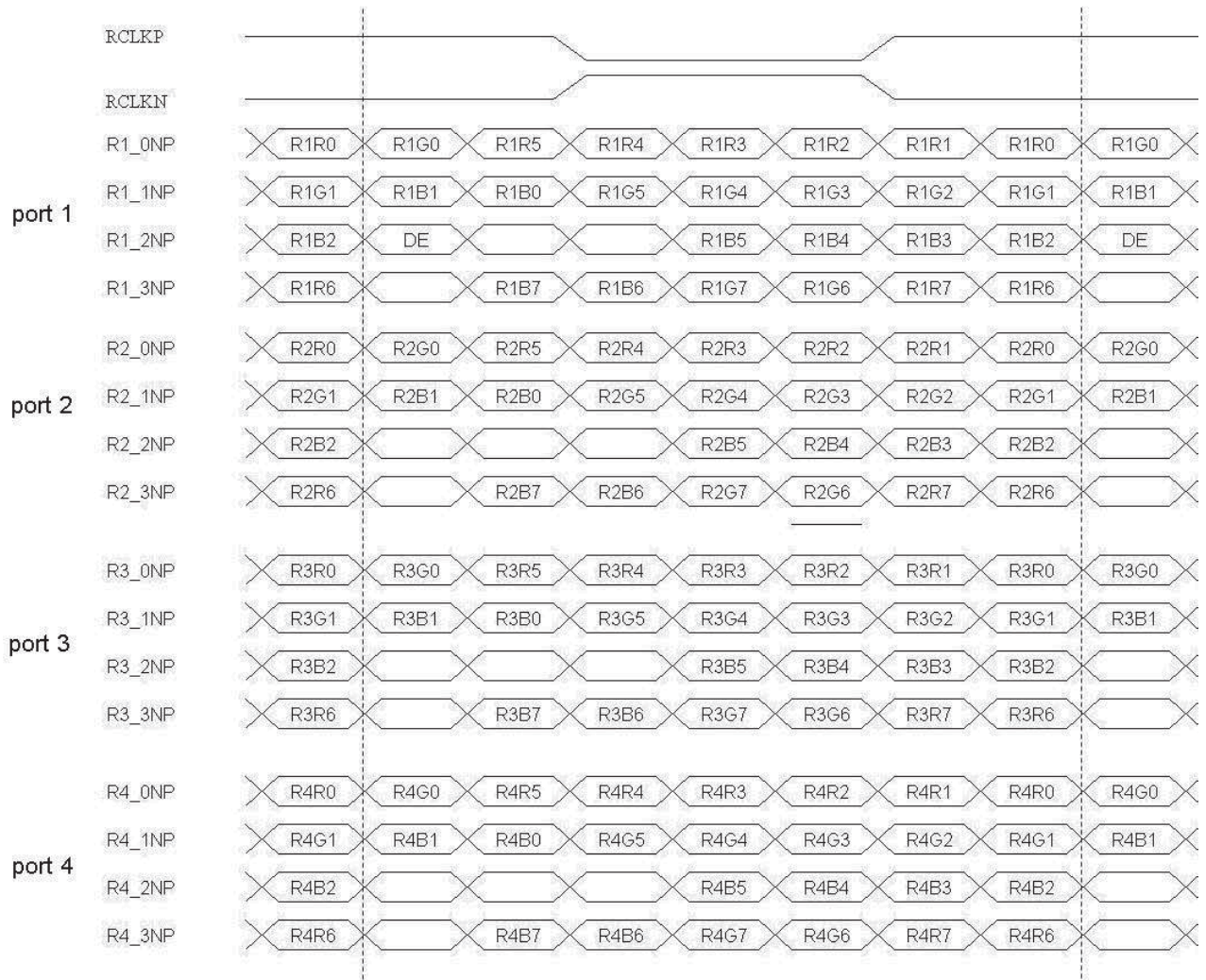
Port 6 : $4N+1282$ $N=0, \sim 319$ (1282,1286.. 2558pixel)

Port 7 : $4N+1283$ $N=0, \sim 319$ (1283,1287.. 2559pixel)

Port 8 : $4N+1284$ $N=0, \sim 319$ (1284,1288.. 2560pixel)



3.4.2 LVDS Data Format





Product Specification

M238DTN01.0

AU OPTRONICS CORPORATION

port 5	R5_0NP	R1281R0	R1281G0	R1281R5	R1281R4	R1281R3	R1281R2	R1281R1	R1281R0	R1281G0
	R5_1NP	R1281G1	R1281B1	R1281B0	R1281G5	R1281G4	R1281G3	R1281G2	R1281G1	R1281B1
	R5_2NP	R1281B2	DE			R1281B5	R1281B4	R1281B3	R1281B2	DE
	R5_3NP	R1281R6		R1281B7	R1281B6	R1281G7	R1281G6	R1281R7	R1281R6	
port 6	R6_0NP	R1282R0	R1282G0	R1282R5	R1282R4	R1282R3	R1282R2	R1282R1	R1282R0	R1282G0
	R6_1NP	R1282G1	R1282B1	R1282B0	R1282G5	R1282G4	R1282G3	R1282G2	R1282G1	R1282B1
	R6_2NP	R1282B2				R1282B5	R1282B4	R1282B3	R1282B2	
	R6_3NP	R1282R6		R1282B7	R1282B6	R1282G7	R1282G6	R1282R7	R1282R6	
port 7	R7_0NP	R1283R0	R1283G0	R1283R5	R1283R4	R1283R3	R1283R2	R1283R1	R1283R0	R1283G0
	R7_1NP	R1283G1	R1283B1	R1283B0	R1283G5	R1283G4	R1283G3	R1283G2	R1283G1	R1283B1
	R7_2NP	R1283B2				R1283B5	R1283B4	R1283B3	R1283B2	
	R7_3NP	R1283R6		R1283B7	R1283B6	R1283G7	R1283G6	R1283R7	R1283R6	
port 8	R8_0NP	R1284R0	R1284G0	R1284R5	R1284R4	R1284R3	R1284R2	R1284R1	R1284R0	R1284G0
	R8_1NP	R1284G1	R1284B1	R1284B0	R1284G5	R1284G4	R1284G3	R1284G2	R1284G1	R1284B1
	R8_2NP	R1284B2				R1284B5	R1284B4	R1284B3	R1284B2	
	R8_3NP	R1284R6		R1284B7	R1284B6	R1284G7	R1284G6	R1284R7	R1284R6	



3.4.3 Color versus Input Data

The following table is for color versus input data (8bit). The higher the gray level, the brighter the color.

Color	Gray Level	Color Input Data																								Remark
		RED data (MSB :R7, LSB :R0)								GREEN data (MSB :G7, LSB :G0)								BLUE data (MSB :B7, LSB :B0)								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1		
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0		
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1		



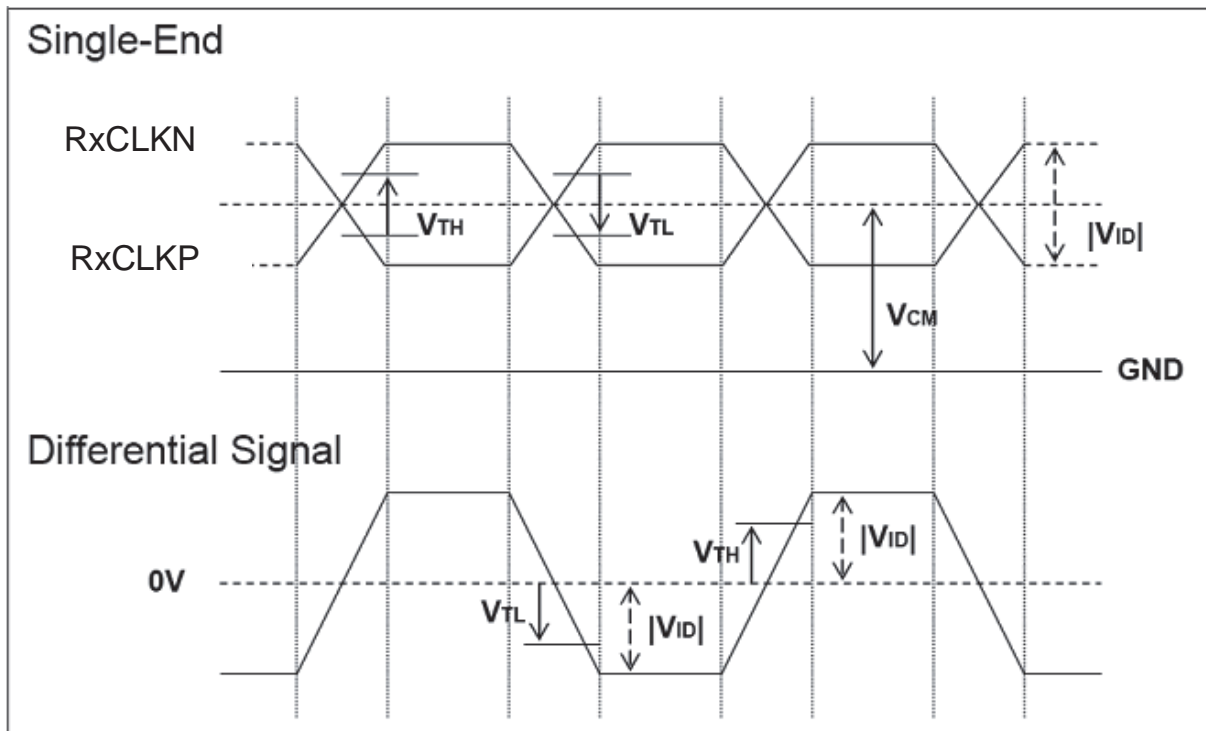
3.4.4 LVDS Specification

a. DC Characteristics:

Symbol	Description	Min	Typ	Max	Units	Condition
V_{TH}	LVDS Differential Input High Threshold	-	-	+100	[mV]	$V_{CM} = 1.2V$
V_{TL}	LVDS Differential Input Low Threshold	-100	-	-	[mV]	$V_{CM} = 1.2V$
$ V_{ID} $	LVDS Differential Input Voltage	100	-	600	[mV]	
V_{CM}	LVDS Common Mode Voltage	+1.0	+1.2	+1.5	[V]	$V_{TH} - V_{TL} = 200mV$

LVDS Signal Waveform:

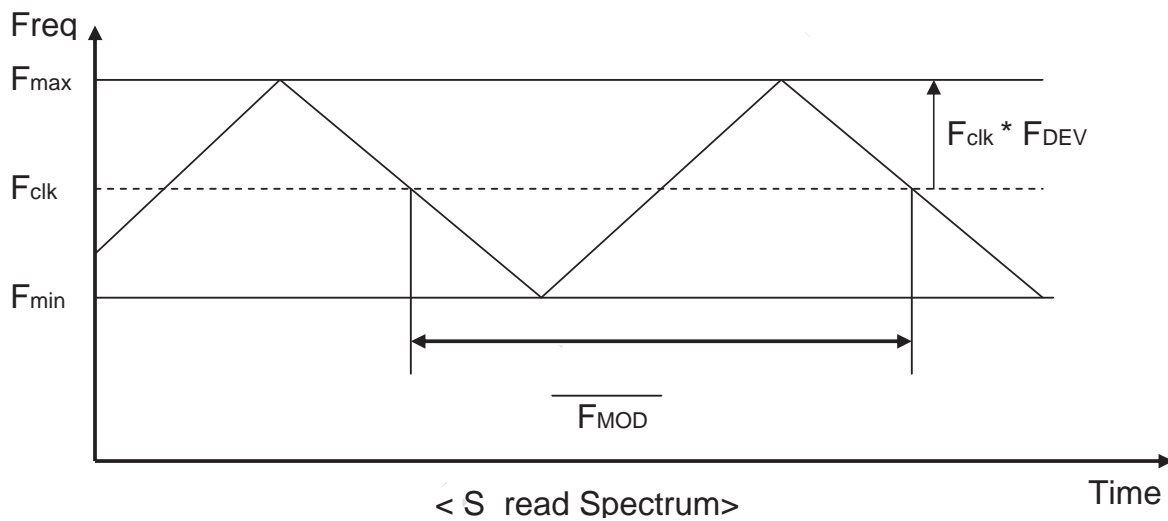
Use RxCLKN & RxCLKP as example.





b. AC Characteristics:

Symbol	Description	Min	Max	Unit	Remark
F_{DEV}	Maximum deviation of input clock frequency during Spread Spectrum	-	± 3	%	
F_{MOD}	Maximum modulation frequency of input clock during Spread Spectrum	-	100	KHz	



Fclk: LVDS Clock Frequency



3.4.5 Input Timing Specification

It only support DE mode, and the input timing are shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	1452	1481	8192	Th	
Tdisp (v)		Active	1440	1440	1440	Th	
Tblk (v)		Blanking	12	41	6752	Th	
Fv		Frequency	30	120	145	Hz	Note 3-3
Th	Horizontal Section	Period	359	360	1023	Tclk	
Tdisp (h)		Active	320	320	320	Tclk	
Tblk (h)		Blanking	39	40	703	Tclk	
Fh		Frequency	69.7	177.7	250.6	KHz	Note 3-4
Tclk	LVDS Clock	Period	11.1	15.6	39.9	ns	1/Fclk
Fclk		Frequency	25	64	90	MHz	Note 3-5

Note 3-3: The optimal Vertical Frequency is 119~145 Hz for best picture quality

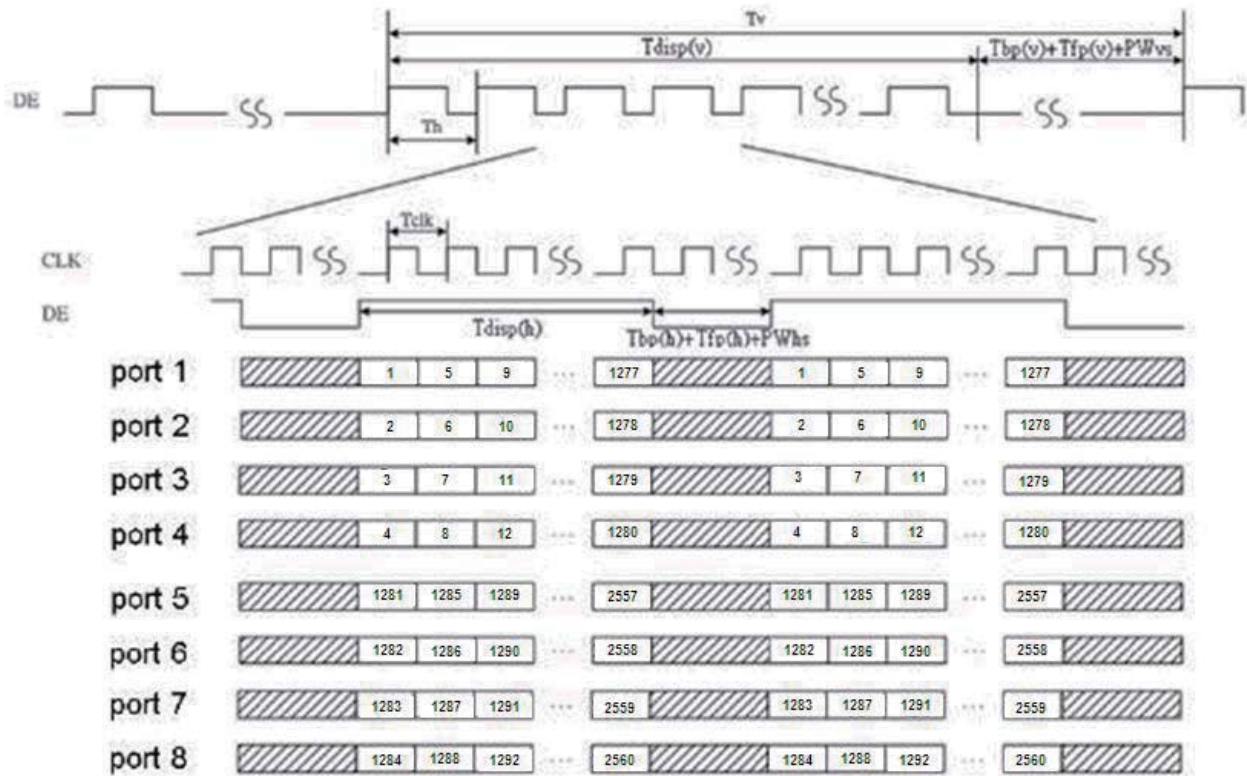
Note 3-4: The equation is listed as following. Please don't exceed the above recommended value.

$$\begin{aligned}Fh (\text{Min.}) &= Fclk (\text{Min.}) / Th (\text{Min.}); \\Fh (\text{Typ.}) &= Fclk (\text{Typ.}) / Th (\text{Typ.}); \\Fh (\text{Max.}) &= Fclk (\text{Max.}) / Th (\text{Min.});\end{aligned}$$

Note 3-5: The equation is listed as following. Please don't exceed the above recommended value.

$$\begin{aligned}Fclk (\text{Typ.}) &= Fv (\text{Typ.}) \times Th (\text{Typ.}) \times Tv (\text{Typ.}); \\Fclk (\text{Min.}) &< Fv \times Th \times Tv < Fclk (\text{Max.})\end{aligned}$$

3.4.6 Input Timing Diagram



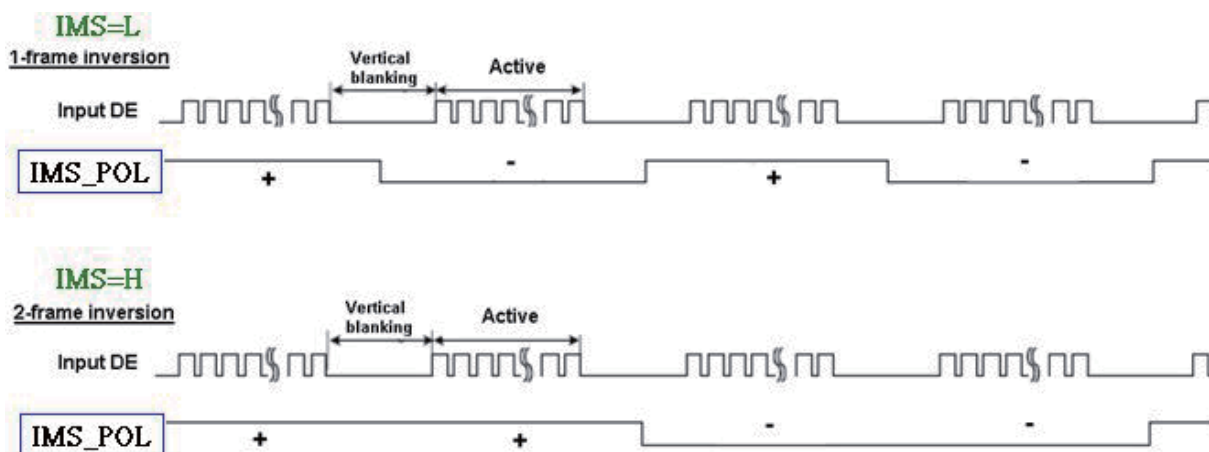
3.4.7 IMS Control

3.4.7.1. IMS control I/O Characteristics

Pin #	Symbol	I/O	Buffer	Description	Remark
CN2_pin 30	IMS_POL	O	4mA	Frame Inversion polarity Index IMS=L :1-frame inversion IMS=H :2-frame inversion	Note 3-6
CN3_pin 30	IMS	I	IPL*	Interlace mode selection control signal	

* IPL : internal pull low

Note 3-6



3.4.7.2. Absolute Maximum Rating

Symbol	Description	Min	Max	Unit	Remark
IMS	Interlace mode selection control signal	GND-0.3	5.0	[Volt]	Ta=25°C

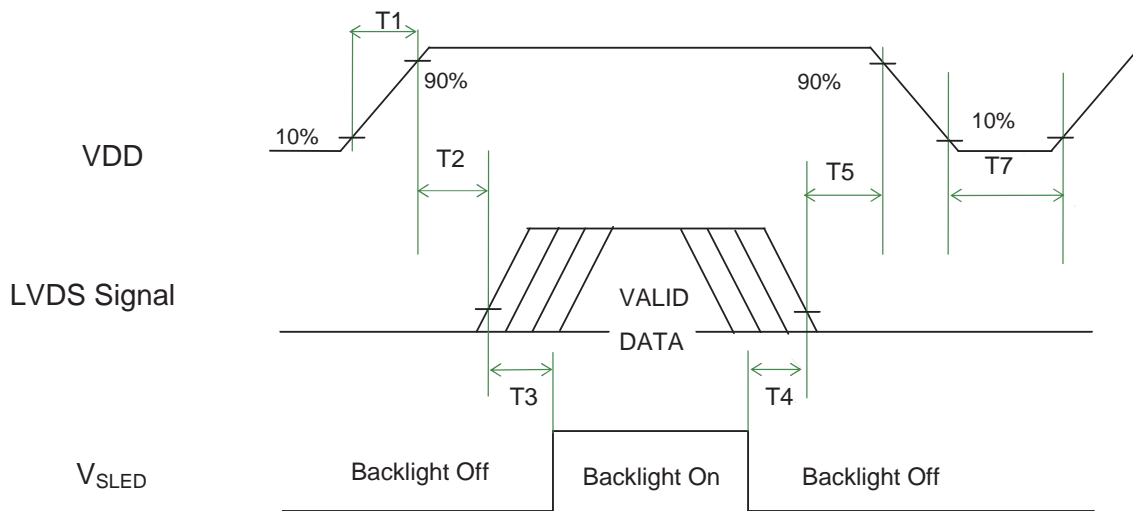


3.4.7.3. Recommended Operating Condition

Symbol	Parameter	Condition	Rating			Unit
			Min	Typ	Max	
V_{IH}	Input High Voltage	-	2.0	-	3.6	V
V_{IL}	Input Low Voltage	-	0	-	0.8	V
V_{OH}	Output High Voltage	$I_{OH} = 4mA$	2.4	-	3.4	V
V_{OL}	Output Low Voltage	$I_{OL} = -4mA$	0	-	0.4	V

3.5 Power ON/OFF Sequence

VDD power, LVDS signal and backlight on/off sequence are as following. LVDS signals from any system shall be Hi-Z state when VDD is off.



Power Sequence Timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	50	[ms]	
T3	500	-	-	[ms]	
T4	100	-	-	[ms]	
T5	0		50	[ms]	Note 3-7 Note 3-8
T7	1000	-	-	[ms]	

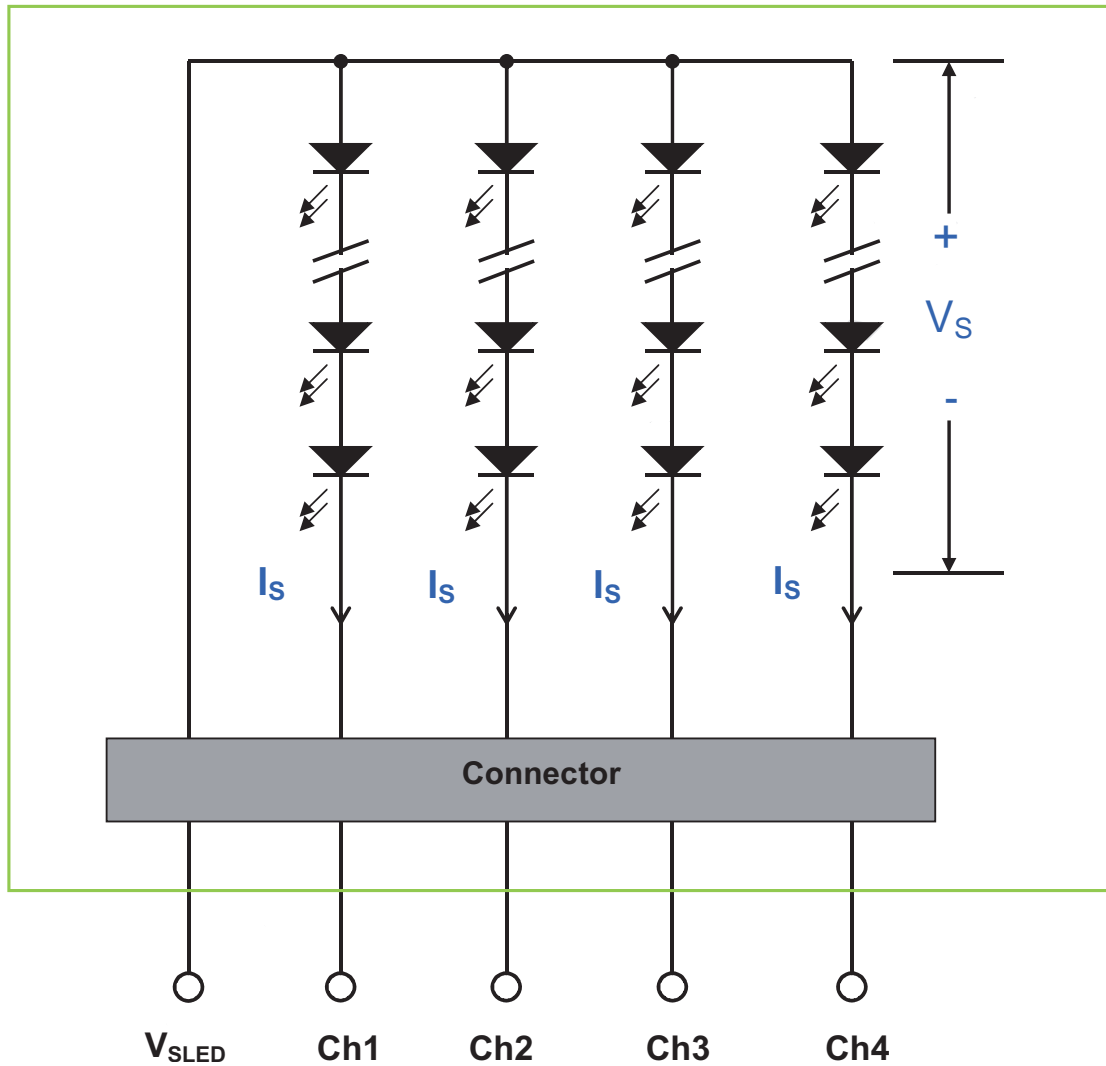
Note 3-7 : Recommend setting T5 = 0ms to avoid electronic noise when VDD is off.

Note 3-8 : During T5 period , please keep the level of input LVDS signals with Hi-Z state.

4 Backlight Unit

4.1 Block Diagram

The following shows the block diagram of the 23.8 inch Backlight Unit. And it includes 60 pcs LED in the LED light bar. (4 strings and 15 pcs LED of one string).



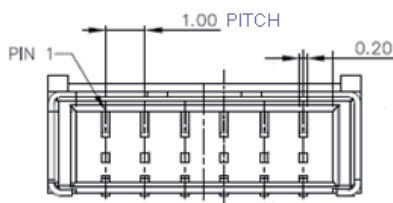
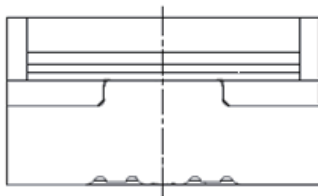
4.2 Interface Connection

4.2.1 Connector Type

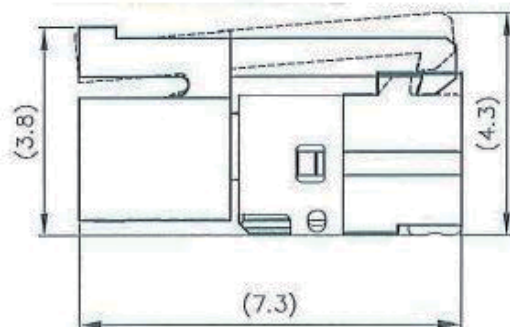
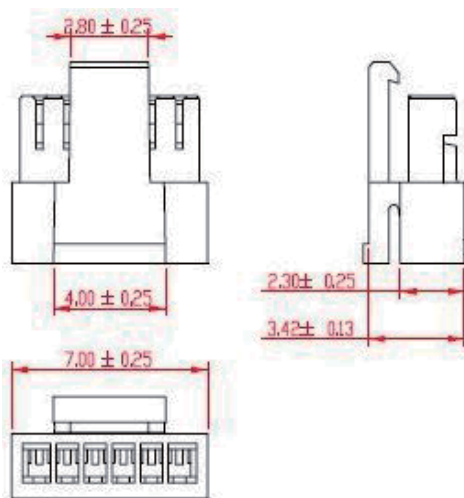
Backlight Connector	Manufacturer	ENTERY
	Part Number	3707K-S06N-21R
Mating Connector	Manufacturer	ENTERY or compatible
	Part Number	H112K-P06N-00B (Non-Locking type) H112K-P06N-03B (Locking type)

Backlight Connector dimension:

$H \times V \times D = 13.9 \times 3.00 \times 4.25$, Pitch = 1.0(unit = mm)

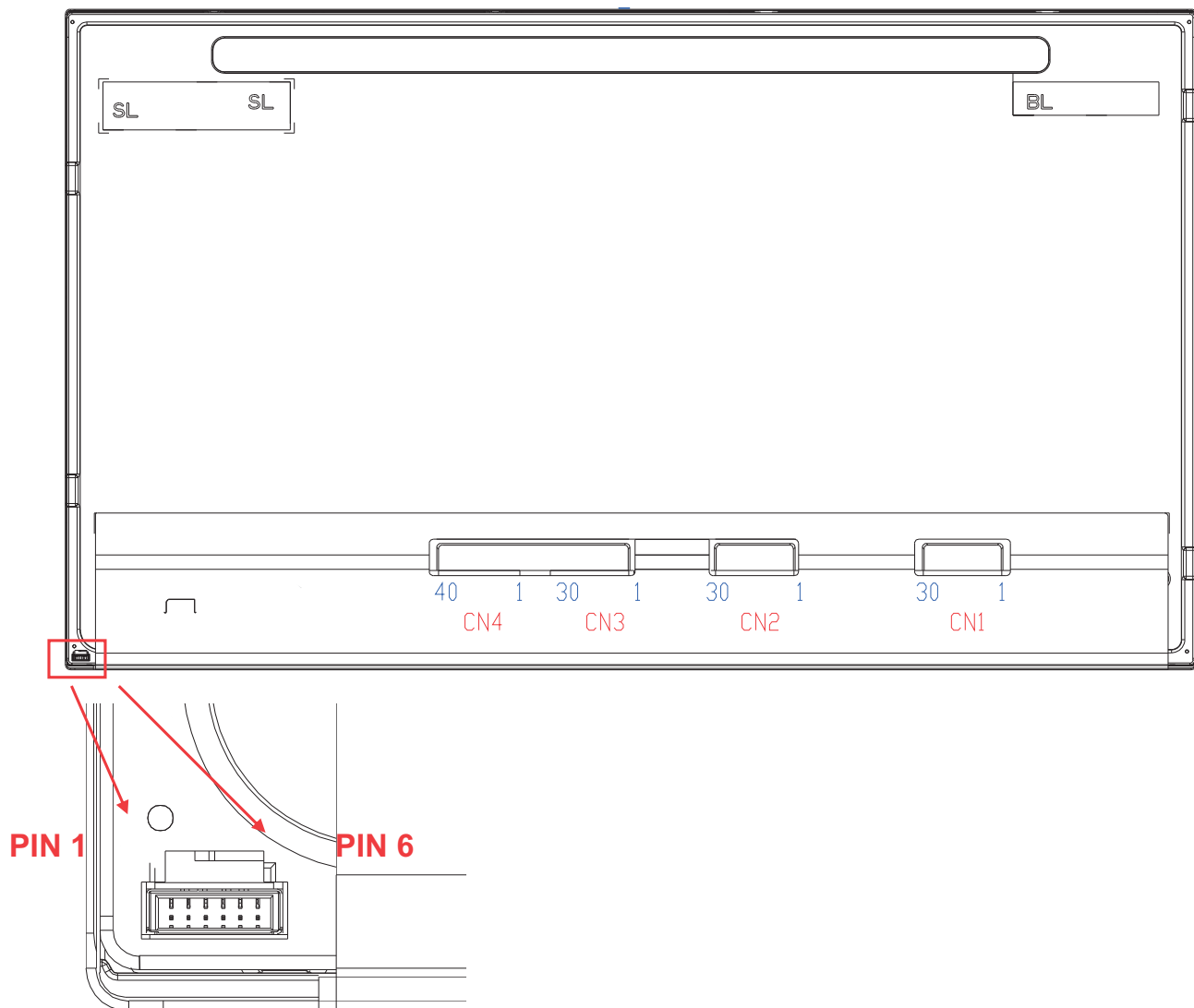


Mating Connector dimension:



4.2.2 Connector Pin Assignment

Pin#	Symbol	Description	Remark
1	Ch1	LED Current Feedback Terminal (Channel 1)	
2	Ch2	LED Current Feedback Terminal (Channel 2)	
3	V _{SLED}	LED Power Supply Voltage Input Terminal	
4	V _{SLED}	LED Power Supply Voltage Input Terminal	
5	Ch3	LED Current Feedback Terminal (Channel 3)	
6	Ch4	LED Current Feedback Terminal (Channel 4)	



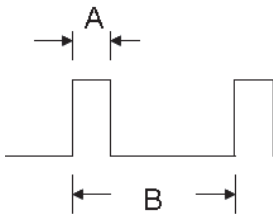
4.3 Electrical Characteristics

4.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

(Ta=25°C)

Symbol	Description	Min	Max	Unit	Remark
Is	LED String Current	0	150	[mA]	100% duty ratio
			210	[mA]	Duty ratio ≤ 10% Pulse time=10 ms



Duty ratio= (A / B) X 100% ; (A: Pulse time, B: Period)

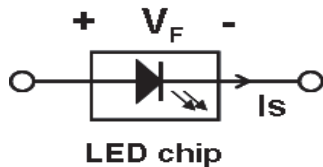
4.3.2 Recommended Operating Condition

(Ta=25°C)

Symbol	Description	Min.	Typ.	Max.	Unit	Remark
Is	LED String Current	-	80	88	[mA]	100% duty ratio of LED chip
Vs	LED String Voltage	43.5	46.5	49.5	[Volt]	Is=80mA @ 100% duty ratio; Note 4-1, Note 4-5
ΔVs	Maximum Vs Voltage Deviation of light bar	-	-	3	[Volt]	Is=80mA @ 100% duty ratio; Note 4-2
P _{BLU}	LED Light Bar Power Consumption	-	14.9	15.8	[Watt]	Note 4-3
LT _{LED}	LED Life Time	30,000	-	-	[Hour]	Note 4-4
OVP	Over Voltage Protection in system board	110% Vs max	-	-	[Volt]	Note 4-5

Note 4-1: $V_s (\text{Typ.}) = V_F (\text{Typ.}) \times \text{LED No. (one string)}$;

- V_F : LED chip forward voltage, $V_F (\text{Min.}) = 2.9\text{V}$, $V_F (\text{Typ.}) = 3.1\text{V}$, $V_F (\text{Max.}) = 3.3\text{V}$
- The same equation to calculate $V_s (\text{Min.})$ & $V_s (\text{Max.})$ for respective $V_F (\text{Min.})$ & $V_F (\text{Max.})$;



Note 4-2: $\Delta V_s (\text{Max.}) = \Delta V_F \times \text{LED No. (one string)}$;

- ΔV_F : LED chip forward voltage deviation; (0.2 V , each Bin of LED V_F)

Note 4-3: $P_{\text{BLU}} (\text{Typ.}) = V_s (\text{Typ.}) \times I_s (\text{Typ.}) \times 4$; (4 is total String No. of LED Light bar)

$$P_{\text{BLU}} (\text{Max.}) = V_s (\text{Max.}) \times I_s (\text{Typ.}) \times 4 ;$$

Note 4-4: Definition of life time:

- Brightness of LED becomes to 50% of its original value
- Test condition: $I_s = 80\text{mA}$ and 25°C (Room Temperature)

Note 4-5: Recommendation for LED driver power design:

Due to there are electrical property deviation in LED & monitor set system component after long time operation. AUO strongly recommend the design value of LED driver board OVP (over voltage protection) should be 10% higher than max. value of LED string voltage (V_s) at least.

Note 4-6: AUO strongly recommend "Analog Dimming" method for backlight brightness control for Wavy Noise Free. Otherwise, recommend that Dimming Control Signal (PWM Signal) should be synchronized with Frame Frequency.



5 Reliability Test

AUO reliability test items are listed as following table. (*Bare Panel only*)

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50°C , 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50°C , 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0°C , 300hours	
High Temperature Storage (HTS)	Ta= 60°C , 300hours	
Low Temperature Storage (LTS)	Ta= -20°C , 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 Grms Wave: Random Frequency: 10 - 200 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Thermal Shock Test (TST)	-20°C/30min, 60°C/30min, 100 cycles	Note 5-1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 15KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	Note 5-2
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:18,000 ft Non-Operation:40,000 ft	

Note 5-1: a. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C , and back again. Power is not applied during the test.
b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 5-2: EN61000-4-2, ESD class B: Certain performance degradation allowed
No data lost
Self-recoverable
No hardware failures.



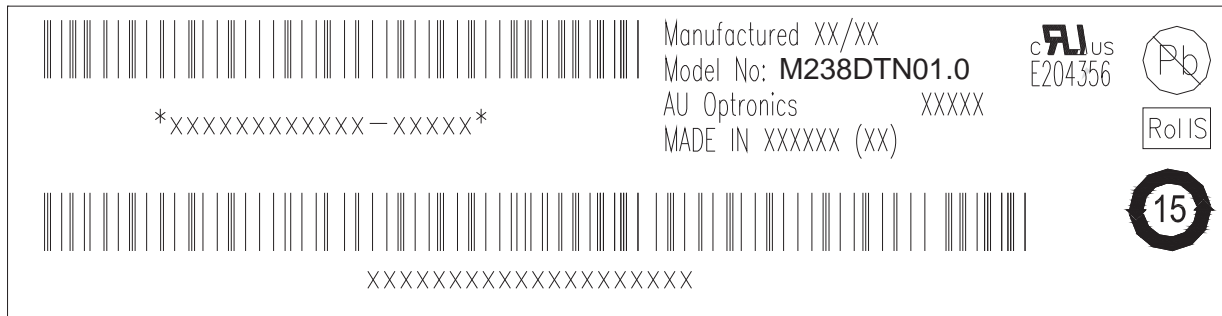
Product Specification

M238DTN01.0

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6 Shipping Label

The label is on the panel as shown below:



Note 6-1: For Pb Free products, AUO will add  for identification.

Note 6-2: For RoHS compatible products, AUO will add  for identification.

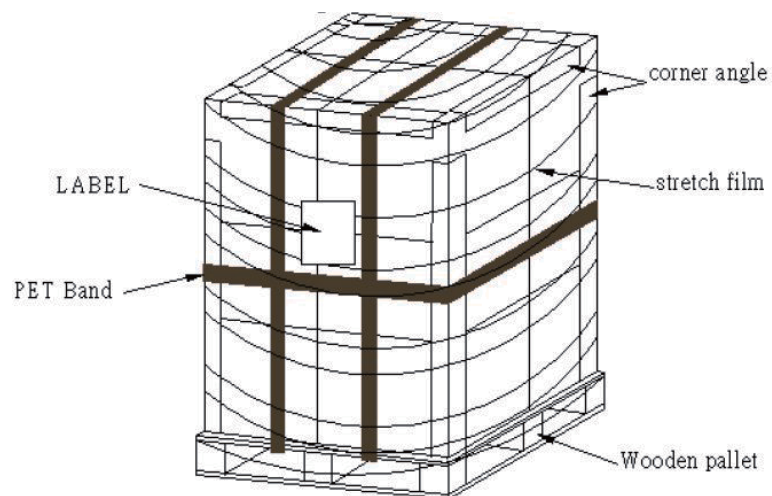
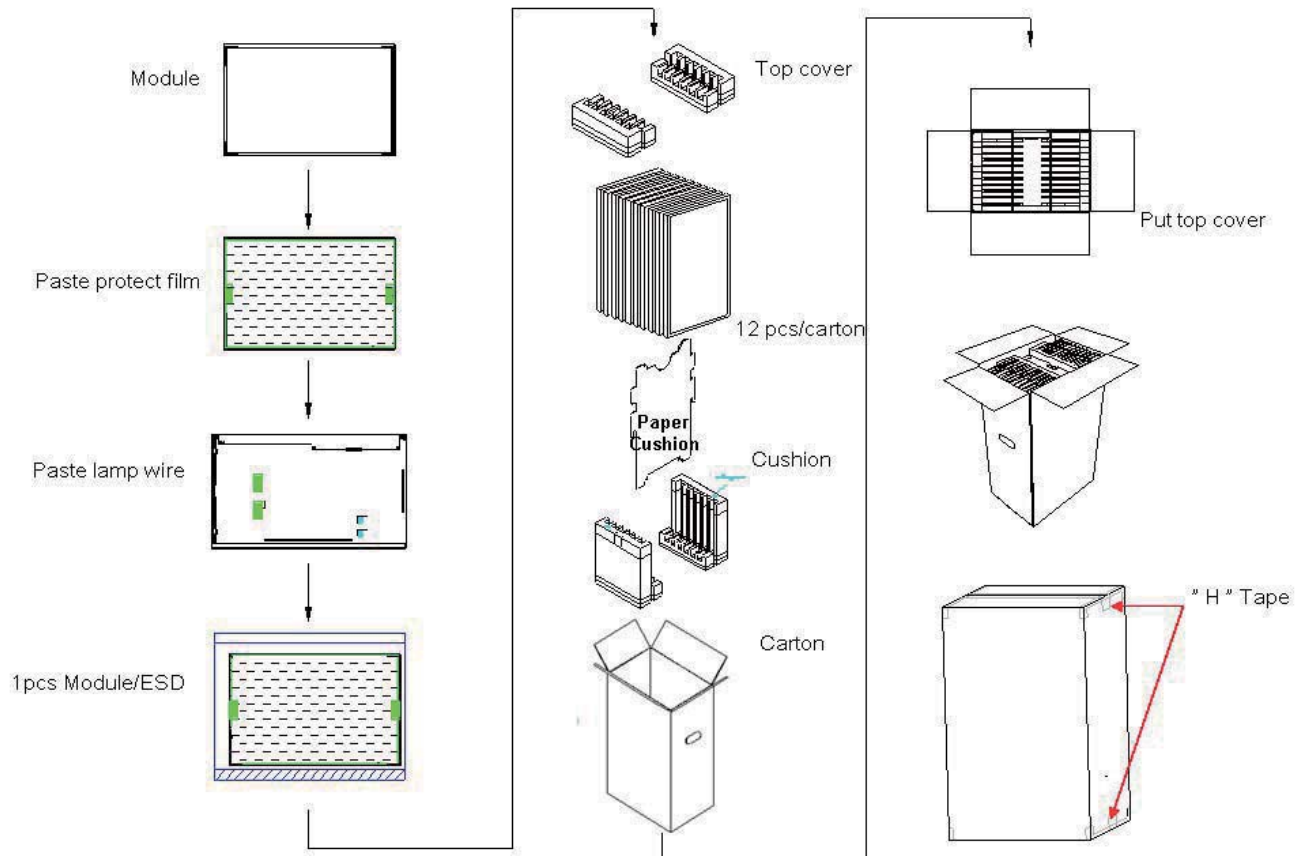
Note 6-3: For China RoHS compatible products, AUO will add  for identification.

Note 6-4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

[illegible]

8 Packing Specification

8.1 Packing Flow



8.2 Pallet and shipment information

Item	Specification			Remark
	Q'ty	Dimension	Weight (kg)	
Panel	1	543.0(H) x 317.4(V) x 11.9mm	2.32 (TBD)	
Cushion	1	-	0.435	
Box	1	395(L)mm x 284(W)mm x652(H)mm	1.56	without Panel & cushion
Packing Box	12 pcs/Box	395(L)mm x 284(W)mm x652(H)mm	TBD	with panel & cushion
Pallet	1	1150(L)mm x840(W)mm x 132(H)mm	12	
Pallet after Packing	16 boxes/pallet	395(L)mm x 284(W)mm x1436(H)mm	488.8(TBD)	