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## Product Functional Specification

15.2 inch Wide SXGA Color TFT LCD Module  
Model Name : B152EW01V2

(◆) Preliminary Specification  
( ) Final Specification

Note: This Specification is subject to change without notice.

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## **II Record of Revision**

Version and Date	Page	Old description	New Description	Remark
0.1. 2003/9/08	All	First Edition for Customer	All	

## 1.0 Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(2.11, IEC60950 or UL1950), or be applied exemption.
- 14) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit(2.4, IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

## 2.0 General Description

This specification applies to the 15.2 inch Color TFT/LCD Module B152EW01 V2

This module is designed for a display unit of notebook style personal computer.

The screen format is intended to support the Wide SXGA (1280(H) x 854(V)) screen and 262k colors (RGB 6-bits data driver).

All input signals are LVDS interface compatible.

This module does not contain an inverter card for backlight.

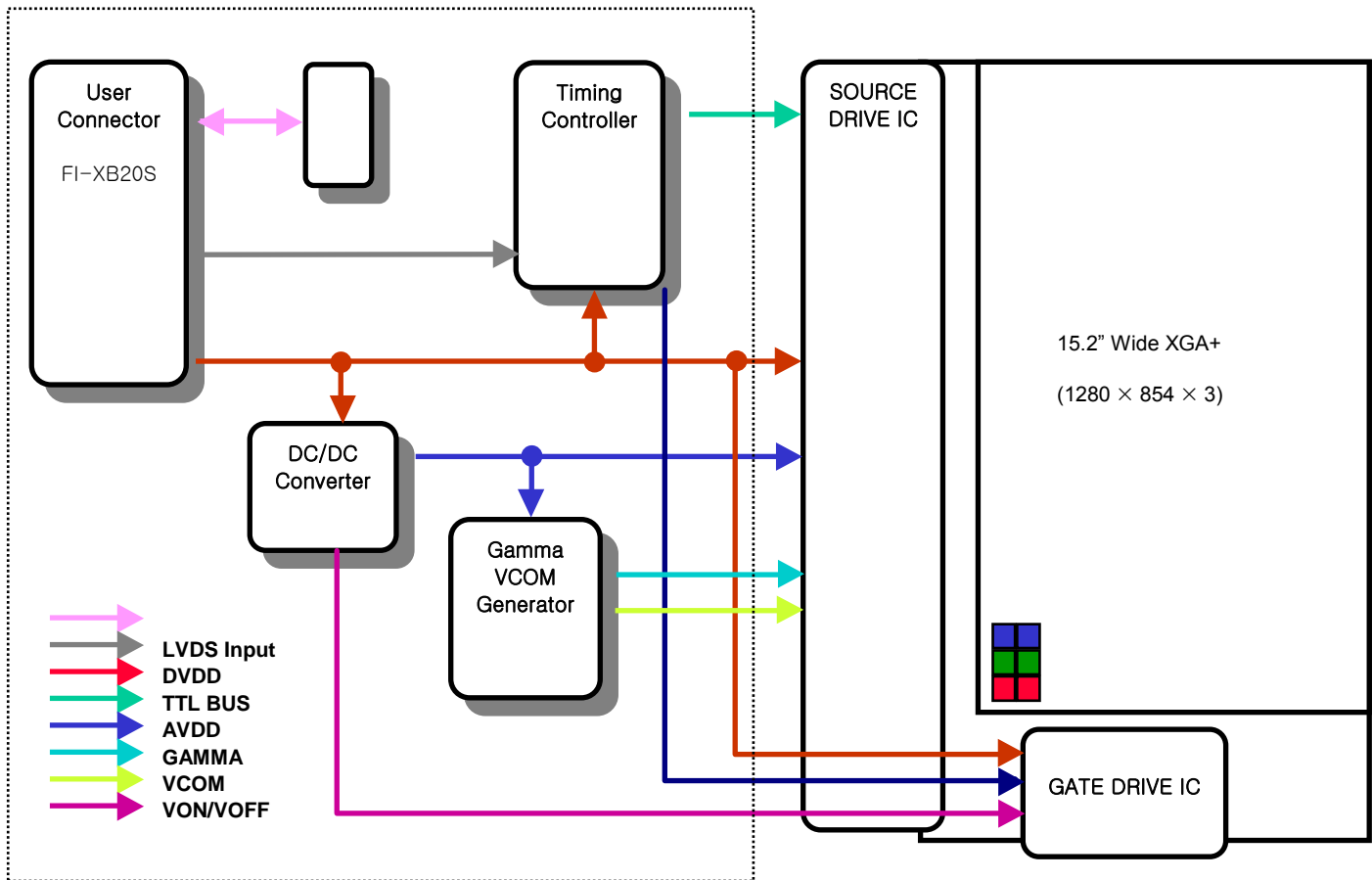
## 2.1 Display Characteristics

The following items are characteristics summary on the table under 25 °C condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	385.5(15.2")
Active Area	[mm]	320.7(H) x 213.9(V)
Pixels H x V		1280(x3) x 854
Pixel Pitch	[mm]	0.2505(per one triad) x 0.2505
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance(ICFL=5.0mA)	[cd/m <sup>2</sup> ]	150 Typ.(5 points average) @5mA
Contrast Ratio		300 : 1 Typ.
Optical Rise Time/Fall Time	[msec]	20/10 Typ.
Nominal Input Voltage VDD	[Volt]	+3.3 Typ.
Typical Power Consumption (VDD line + VCFL line)	[Watt]	6.2 (w/o Inverter, All black pattern)
Weight	[Grams]	535( Typ. (w/o Inverter)
Physical Size	[mm]	336.5(W) x 227.5(H) x 6.0(D) Max.
Electrical Interface		R/G/B Data, 3 Sync, Signals, Clock (4 pairs LVDS)
Support Color		Native 262K colors ( RGB 6-bit data driver )
Temperature Range		
Operating	[°C]	0 to +50
Storage (Shipping)	[°C]	-20 to +60

## 2.2 Functional Block Diagram

The following diagram shows the functional block of the 15.2 inches Color TFT/LCD Module:



### 3.0 Absolute Maximum Ratings

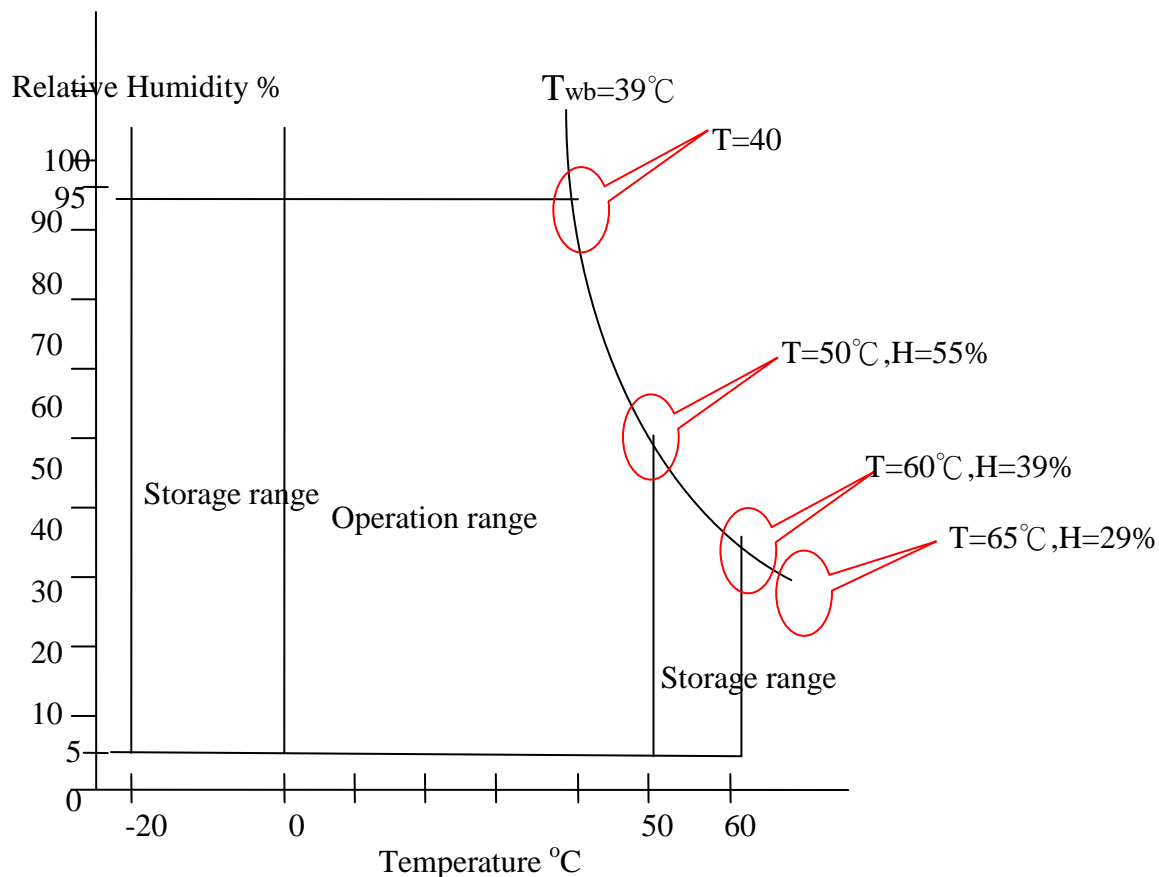
Absolute maximum ratings of the module is as following:

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	[Volt]	
Input Voltage of Signal	Vin	-0.3	VDD+0.3	[Volt]	
CCFL Current	ICFL	-	7	[mA] rms	
CCFL Ignition Voltage	Vs	-	1,400	Vrms	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	8	95	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	5	95	[%RH]	Note 2
Vibration			1.5 50-150	[G Hz]	
Shock			200 , 2	[G ms]	Half sine wave

Note 1 : Duration = 50msec

Note 2 : Maximum Wet-Bulb should be 39°C and No condensation.

#### Wet bulb temperature chart

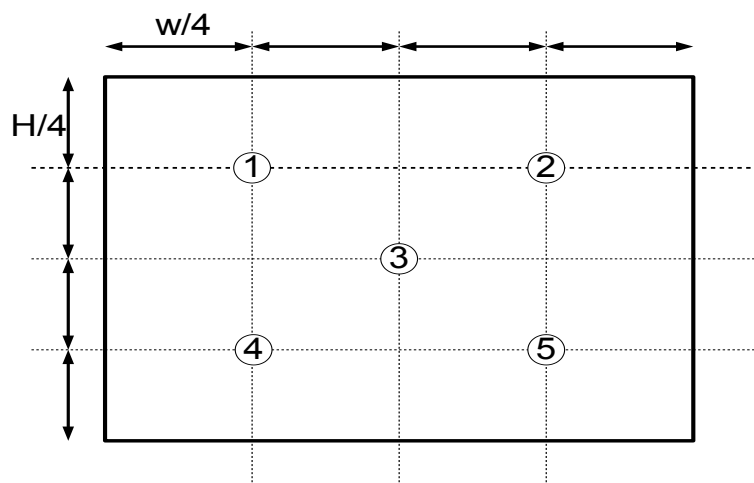


## 4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25°C condition:

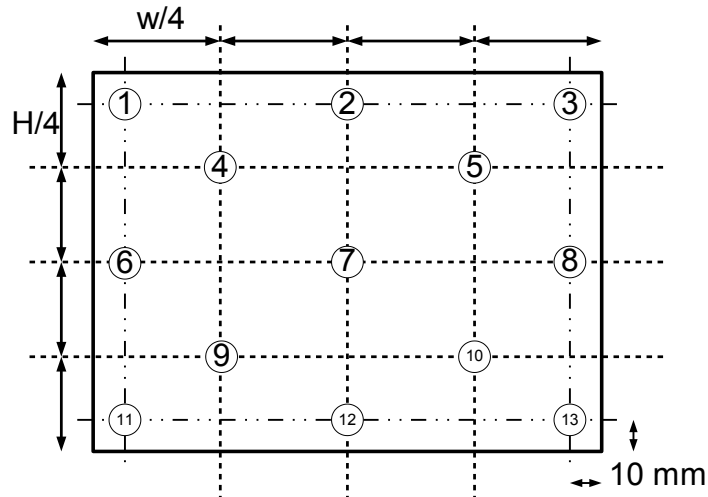
Item	Unit	Conditions	Min.	Typ.	Max.
Viewing Angle	[degree]	Horizontal (Right)	60	-	-
	[degree]	K = 10 (Left)	60	-	-
K: Contrast Ratio	[degree]	Vertical (Upper)	40	-	-
	[degree]	K = 10 (Lower)	50	-	-
Uniformity		5 Points			1.2
Uniformity		13 Points			1.6
Contrast ratio			200	300	-
Response Time	[msec]	Rising	-	20	-
	[msec]	Falling	-	10	-
Color / Chromaticity Coordinates (CIE)		Red x	0.570	0.600	0.630
		Red y	0.320	0.350	0.380
		Green x	0.280	0.310	0.340
		Green y	0.520	0.550	0.580
		Blue x	0.120	0.150	0.180
		Blue y	0.085	0.115	0.145
		White x	0.290	0.313	0.350
		White y	0.300	0.329	0.360
White Luminance CCFL 5.0mA	[cd/m <sup>2</sup> ]	5 points average	120	150	-

Note 1: 5 points position (Display area)





Note 2: 13 points position



## 5.0 Signal Interface

### 5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

<b>Connector Name / Designation</b>	For Signal Connector
<b>Manufacturer</b>	JAE
<b>Type / Part Number</b>	FI-XB20SR-HF11
<b>Mating Housing/Part Number</b>	FI-X20M
<b>Mating Contact/Part Number</b>	FI-C3-A1

<b>Connector Name / Designation</b>	For Lamp Connector
<b>Manufacturer</b>	JST
<b>Type / Part Number</b>	BHSR-02VS-1
<b>Mating Type / Part Number</b>	SM02B-BHSS-1-TB

### 5.2 Signal Pin

Pin#	Signal Name	Pin#	Signal Name
1	VDD	2	VDD
3	GND	4	GND
5	RxIN0-	6	RxIN0+
7	GND	8	RxIN1-
9	RxIN1+	10	GND
11	RxIN2-	12	RxIN2+
13	GND	14	RxCLKIN-
15	RxCLKIN+	16	GND
17	Reserved (NC)	18	Reserved (NC)
19	Reserved (NC)	20	Reserved (NC)

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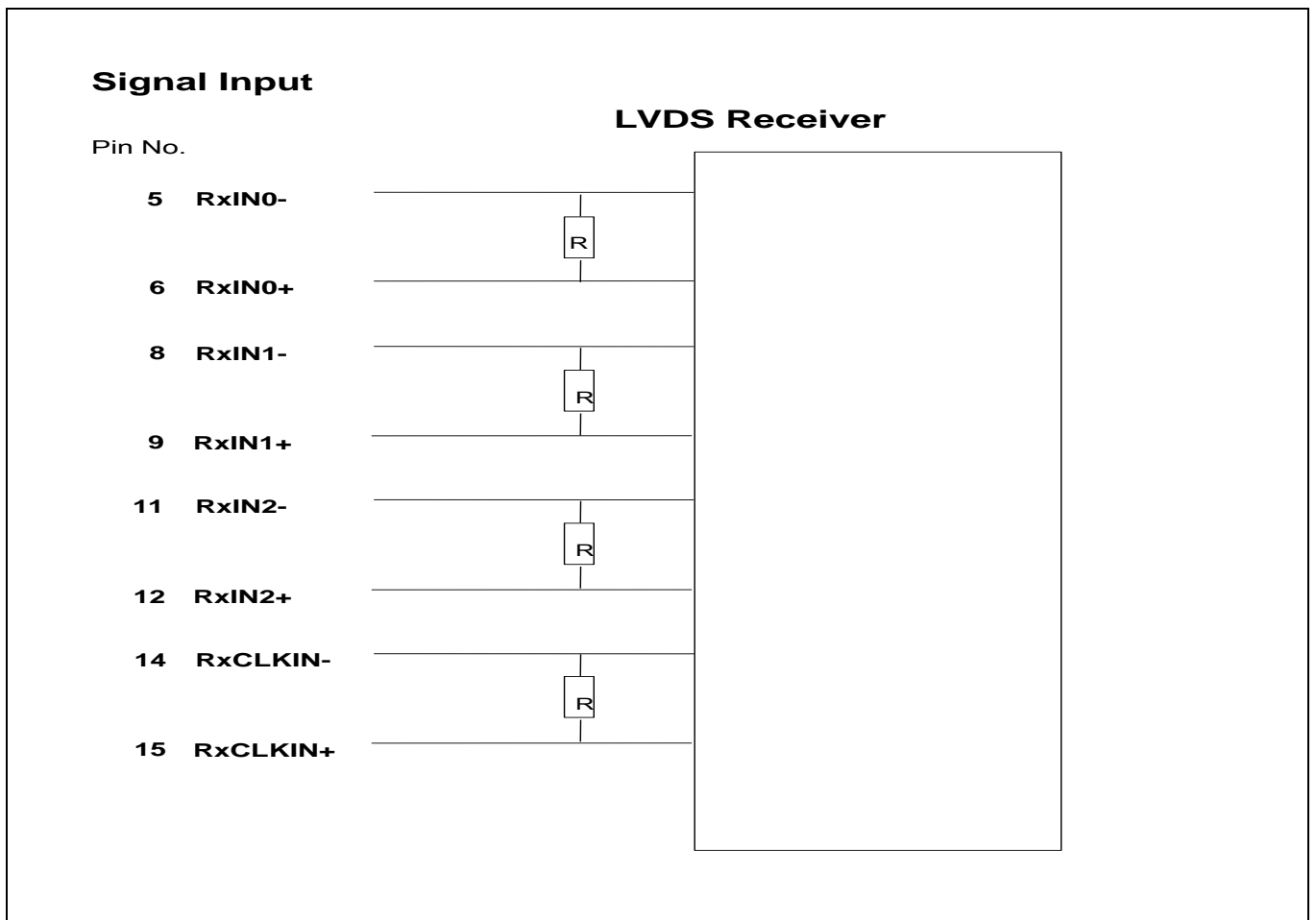
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### 5.3 Signal Description

The module using a LVDS receiver. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.

Signal Name	Description
RxIN0-, RxIN0+	LVDS differential data input(Red0-Red5, Green0)
RxIN1-, RxIN1+	LVDS differential data input(Green1-Green5, Blue0-Blue1)
RxIN2-, RxIN2+	LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DSPTMG)
RxCLKIN-, RxCLKIN0+	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

**Note:** Input signals shall be low or Hi-Z state when VDD is off.  
Internal circuit of LVDS inputs are as following.



The module uses a 100ohm resistor between positive and negative data lines of each receiver input

Signal Name	Description	
+RED5 +RED4 +RED3 +RED2 +RED1 +RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) <b>Red-pixel Data</b>	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) <b>Green-pixel Data</b>	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) <b>Blue-pixel Data</b>	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK	<b>Data Clock</b>	The typical frequency is 79.81 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	<b>Display Timing</b>	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	<b>Vertical Sync</b>	The signal is synchronized to -DTCLK .
HSYNC	<b>Horizontal Sync</b>	The signal is synchronized to -DTCLK .

**Note:** Output signals from any system shall be low or Hi-Z state when VDD is off.

## 5.4 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

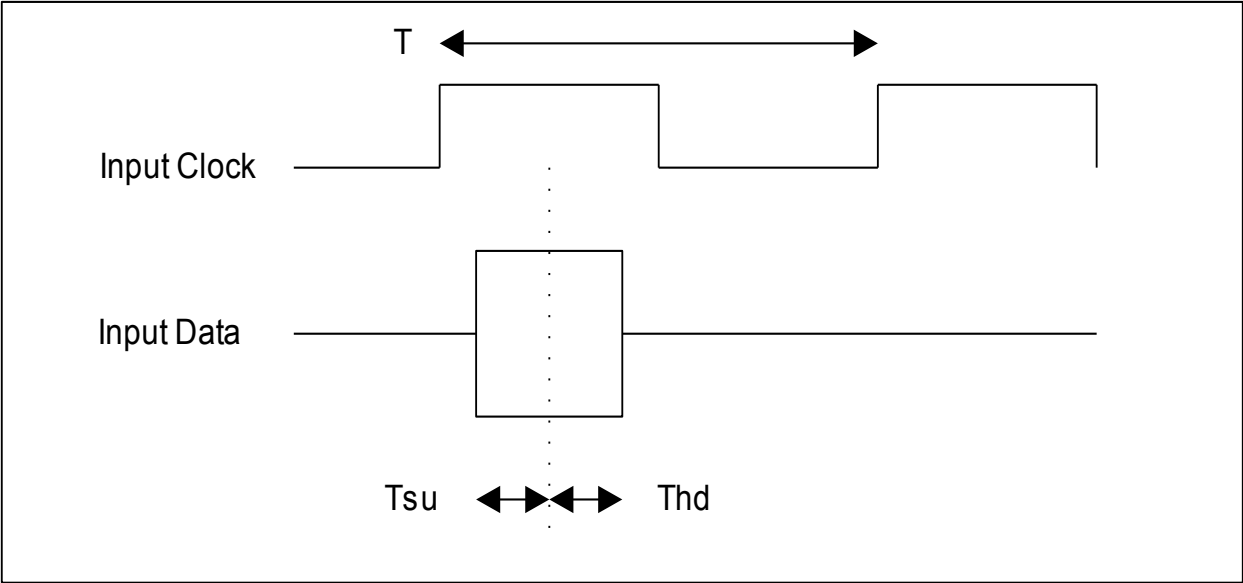
It is recommended to refer the specifications of SN75LVDS86DGG(Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Voltage(Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Voltage(Vcm=+1.2V)	-100		[mV]

LVDS Macro AC characteristics are as follows:

	Min.	Max.
Clock Frequency (T)	85MHz	TBD
Data Setup Time (Tsu)	600ps	
Data Hold Time (Thd)	600ps	



5.5 Signal for Lamp connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

## 6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



## 7.0 Parameter guide line for CFL Inverter

Parameter	Min	DP-1	Max	Units	Condition
White Luminance 5 points average	120	150	—	[cd/m <sup>2</sup> ]	(Ta=25°C)
CCFL current(ICFL)	2.0	6.0	6.5	[mA] rms	(Ta=25°C) <b>Note 2</b>
CCFL Frequency(FCFL)	40	60	65	[KHz]	(Ta=25°C) <b>Note 3</b>
CCFL Ignition Voltage(Vs)	1,500	—	—	[Volt] rms	(Ta= 0°C) <b>Note 4</b>
CCFL Voltage (Reference) (VCFL)	—	780	—	[Volt] rms	(Ta=25°C) <b>Note 5</b>
CCFL Power consumption (PCFL)	—	4.7	—	[Watt]	(Ta=25°C) <b>Note 5</b>

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**Note 1:** DP-1 is the recommended Design Points.

\*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

\*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

\*3 In designing an inverter, it is suggested to check safety circuit ver carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CCFL is damaged.

\*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

\*5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

\*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

**Note 2:** It should be employed the inverter which has "Duty Dimming", if ICCFL is less than 4mA.

**Note 3:** CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

**Note 4:** CCFL inverter should be able to give out a power that has a generating capacity of over 1,500 voltage at the ends of lamp. Lamp units need 1,500 voltage minimum for ignition.

\*1 Because there might be some voltage decade between inverter output and the ends of lamp. The output voltage of inverter transformer secondary side is suggested 1900Vrms as reference.

**Note 5:** Calculator value for reference ( $ICFL \times VCFL = PCFL$ )

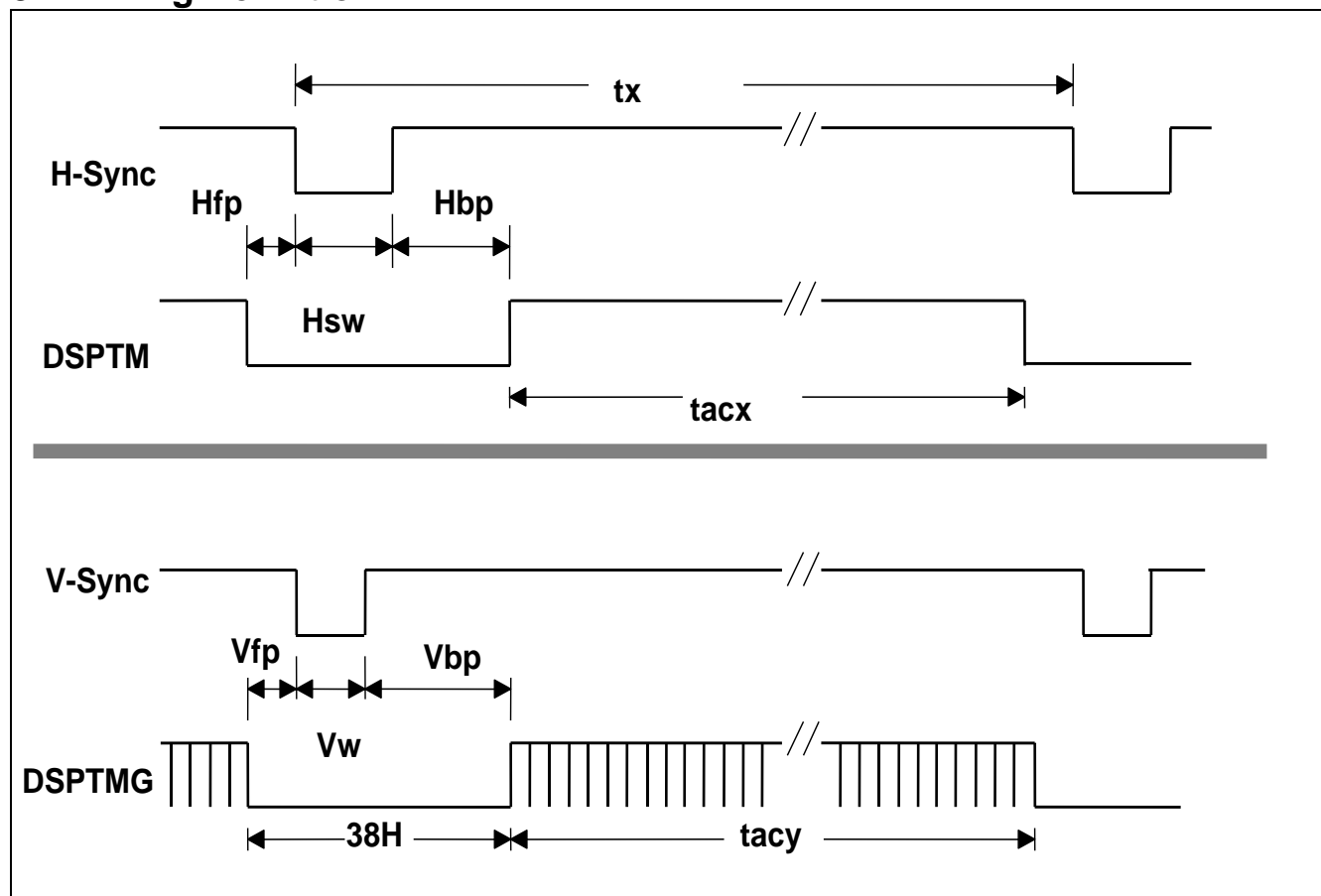
## 8.0 Interface Timings

Basically, interface timings should match the VESA 1280x854 /60Hz(VG901101) manufacturing guide line timing.

### 8.1 Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
fdck	DTCLK Frequency	78	80	85	[MHz]
tck	DTCLK cycle time		12.5		[nsec]
tx	X total time	1344	1536	4096	[tck]
tacx	X active time	1280	1280	1280	[tck]
tbkx	X blank time	64	256	2816	[tck]
Hsync	H frequency		51.96		[KHz]
Hsw	H-Sync width	2	112	3984	[tck]
Hbp	H back porch	2	128	3968	[tck]
Hfp	H front porch	2	16	4080	[tck]
ty	Y total time	861	866	2048	[tx]
tacy	Y active time	854	854	854	[tx]
Vsync	Frame rate	(55)	60	61	[Hz]
Vw	V-sync Width	2	3	2045	[tx]
Vfp	V-sync front porch	1	1	2047	[tx]
Vbp	V-sync back porch	4	8	2040	[tx]

## 8.2 Timing Definition



## 9.0 Power Consumption

Input power specifications are as follows;

Symbol	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.1	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		1.5		[Watt]	All Black Pattern
PDD Max	VDD Power max			1.98	[Watt]	Max Pattern <b>Note</b>
IDD	IDD Current		450		mA	All Black Pattern
IDD Max	IDD Current max			600	mA	Max Pattern <b>Note</b>
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mV] p-p	

**Note : VDD=3.3V**

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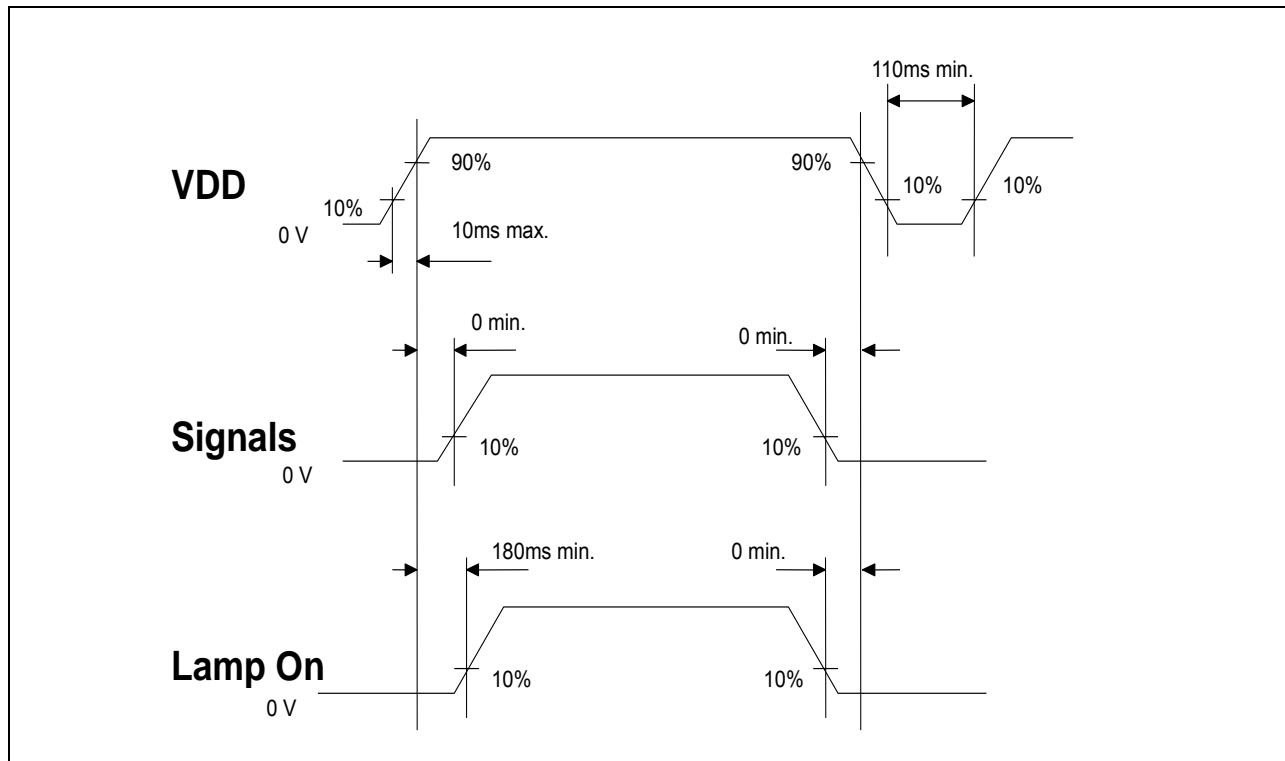
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## 10. Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



## 11.0 Safety Requirement

### 11.1 Safety

UL1950

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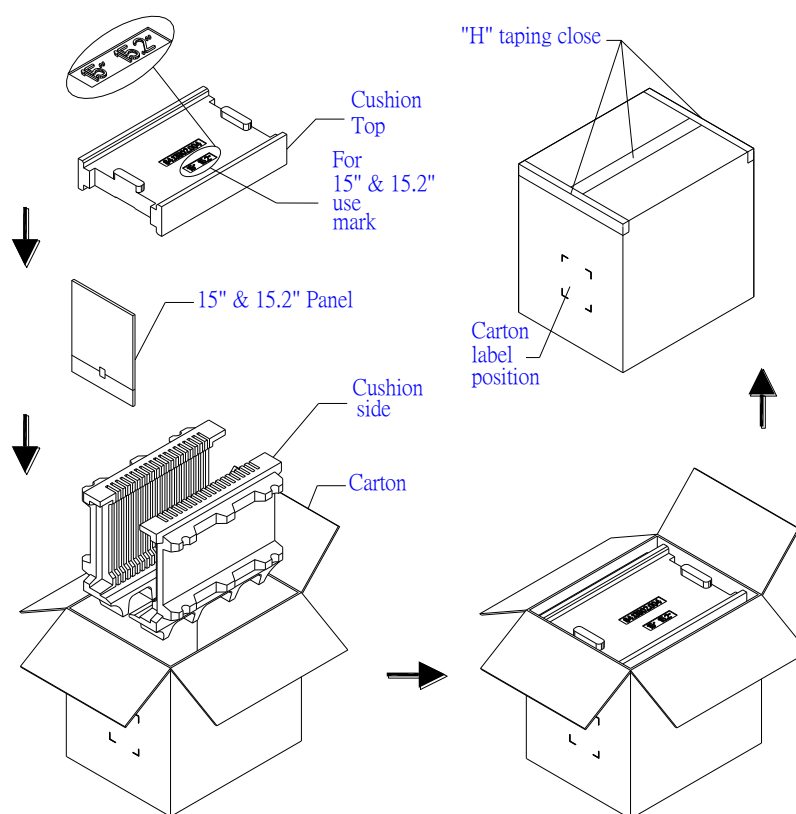
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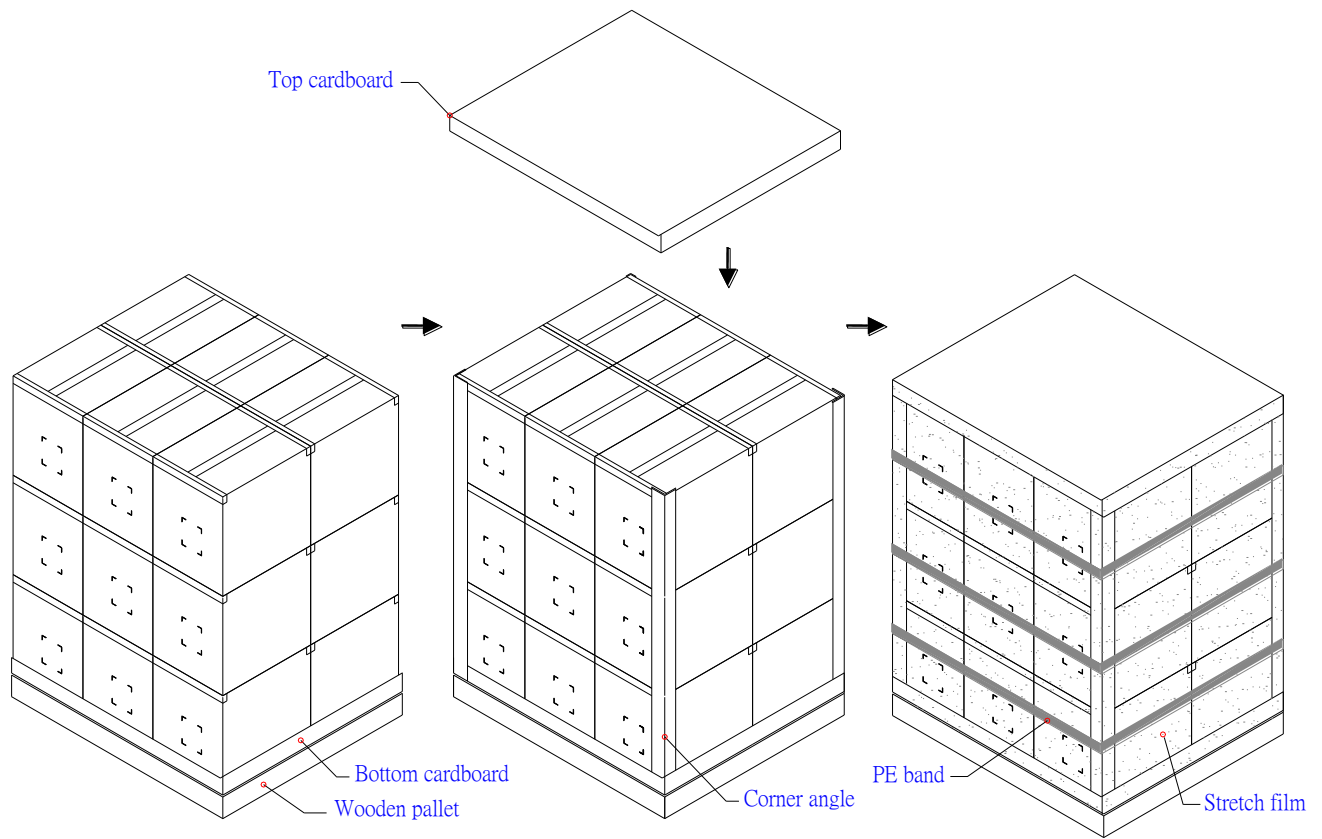


## 12. Carton package

The outside dimension of carton is 490 (L)mm x 390 (W)mm x 480 (H)mm



### 13. Shipping package of palletizing sequence



Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)

# 14.0 Mechanical Characteristics

