




Product Specification

AU OPTRONICS CORPORATION

() Preliminary Specifications

(✓) Final Specifications

Module	11.6"HD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B116XTT01.1 (H/W: 1A)
Note ()	<i>e-TP Display</i> (LCM:B116XTN02.3 +TP : I116FGT10.0 H/W:2A)

Customer	Date
_____	_____
Checked & Approved by	Date
_____	_____
Note: This Specification is subject to change without notice.	

Approved by	Date
<u>Terry Chien</u>	<u>2015/7/16</u>
Prepared by	Date
<u>Beniton Hung</u>	<u>2015/7/16</u>
NBBU Marketing Division AU Optronics corporation	

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Record of Revision

[illegible]

1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electronic breakdown.

2. General Description

B116XTT01.1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x 768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B116XTT01.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	293.8mm			
Active Area	[mm]	256.125 x 144.0			
Pixels H x V		1366 x 3 (RGB) x 768			
Pixel Pitch	[mm]	0.1875 x 0.1875			
Pixel Format		R.G.B Vertical stripe			
Display Mode		Normally White			
White Luminance (ILED= 25mA) (Note: ILED is LED current)	[cd/m ²]	200 typ. (5 points average) (Total Solution) 170 min. (5 points average) (Total Solution)			
Luminance Uniformity		1.6 max (13points)			
Contrast Ratio		500 typ.			
Response Time	[ms]	8 typ/16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.3 max. (Include Logic, TP and BLU power)			
Weight	[Grams]	280 max.			
Physical Size Include bracket (Panel only)	[mm]		Min.	Typ.	Max.
		Length	277.5	278.0	278.5
		Width	171.0	171.5	172.0
Thickness		Thickness	3.0 (Base panel) 5.03 (Total solution) 3.95 (Total Solution_Panel Side) 4.06 (Total Solution_PCBA Side)		
Physical Size Include bracket (Total Solution)	[mm]		Min.	Typ.	Max.
		Length	277.5	278.0	278.5
		Width	172.04	172.54	173.04
Electrical Interface		Display port			
Glass Thickness	[mm]	0.4			
Surface Treatment		Glare, hardness 7H			
Support Color		262K colors (RGB 6-bit)			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			



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2.1.1 General Touch Specification

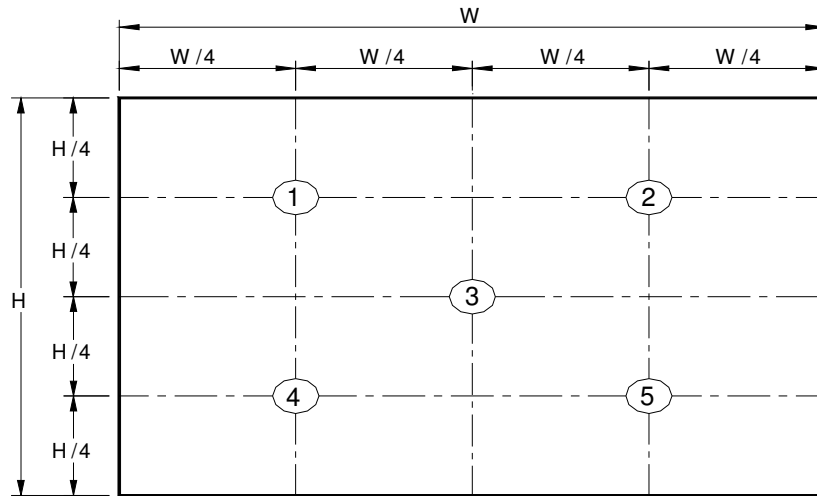
Items	Unit	Specifications
Type of Touch Sensor		Projective Capacitive (OGS)
Panel Size		11.6"
Outline Dimension	mm	265.2mm x 155.3mm
Total Thickness	mm	0.7 typ
Total Weight	g	85 max.
TP View Area	mm	257.32mm x 145.18mm
TP Active Area	mm	258.32mm x 146.18mm
Interface		I2C
Report Rate	Hz	100Hz@4contacts
Multi-Touch Point		10 points
Input method		Finger
Touch panel sensor IC		EKTH3912
Channel		52 x 30
Distance between 2 point	mm	10mm with 9mm-diameter contacts.
Surface hardness	H	7
TP F/W version		10.11

2.2 Optical Characteristics

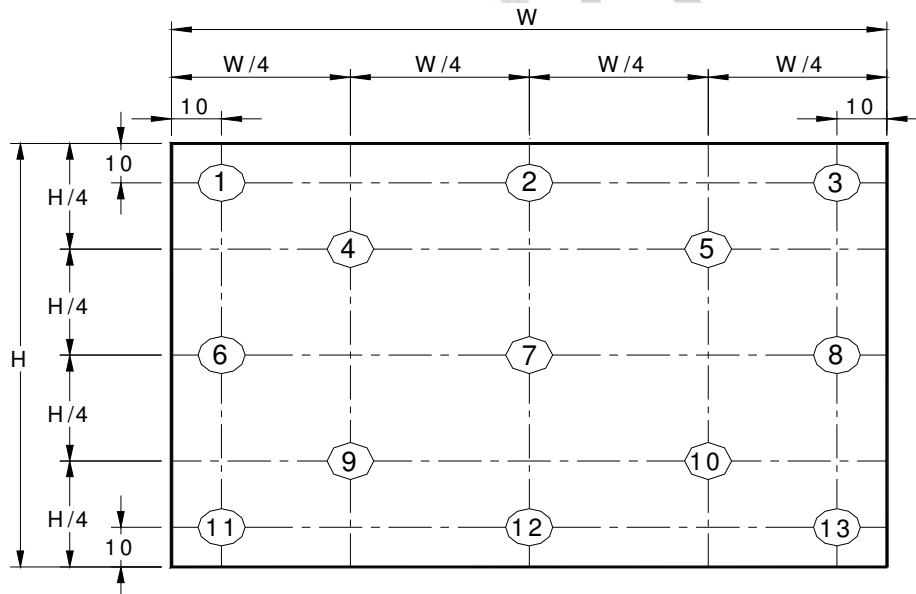
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=20mA		5 points average	170	200	-	cd/m ²	1, 4, 5.
Viewing Angle	θ_R	Horizontal (Right)	40	45	-	degree	4, 9
	θ_L	Horizontal (Left)	40	45	-		
	ψ_H	Vertical (Upper)	10	15	-		
	ψ_L	Vertical (Lower)	30	35	-		
Luminance Uniformity	δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio	CR		400	500	-		4, 6
Cross talk	%				4		4, 7
Response Time	T_{RT}	Rising + Falling	-	8	16		
Color / Chromaticity Coordinates	Red	R _x	0.550	0.580	0.610	CIE 1931	4
		R _y	0.305	0.335	0.365		
	Green	G _x	0.300	0.330	0.360		
		G _y	0.535	0.565	0.595		
	Blue	B _x	0.125	0.155	0.185		
		B _y	0.110	0.140	0.170		
	White	W _x	0.283	0.313	0.343		
		W _y	0.299	0.329	0.359		
	NTSC		-	45	-		

Note 1: 5 points' position (Ref: Active area)



Note 2: 13 points' position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

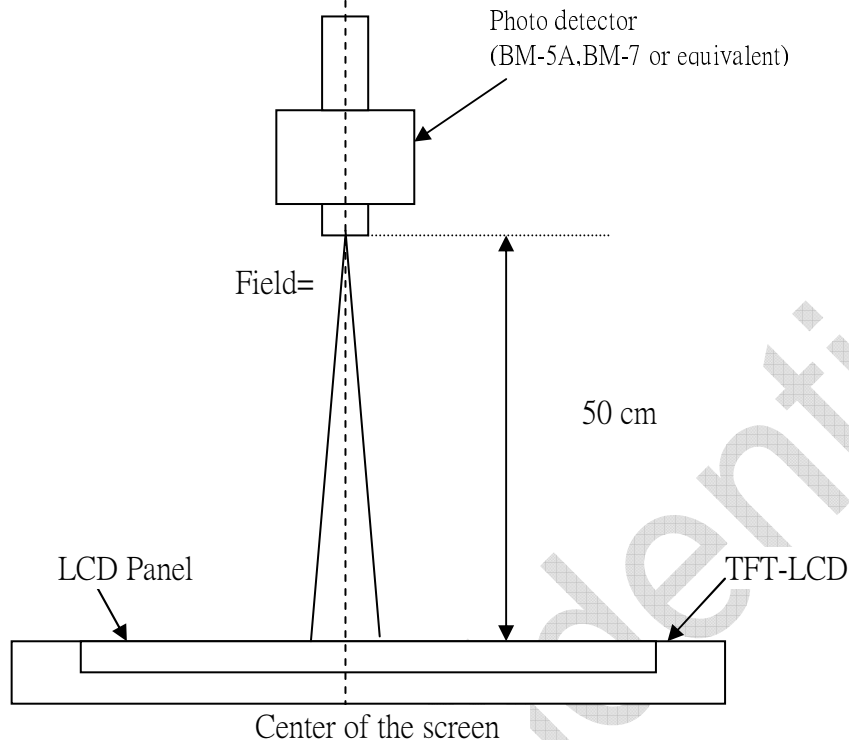
$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement

should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points · $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$
 $L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

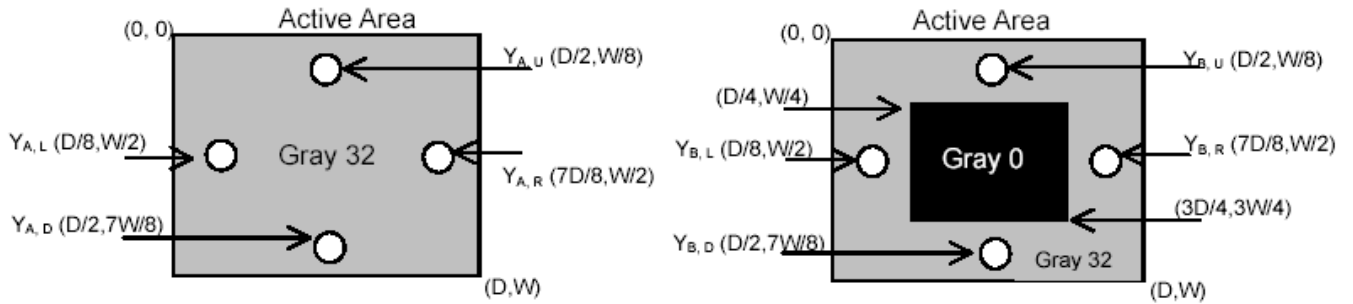
Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

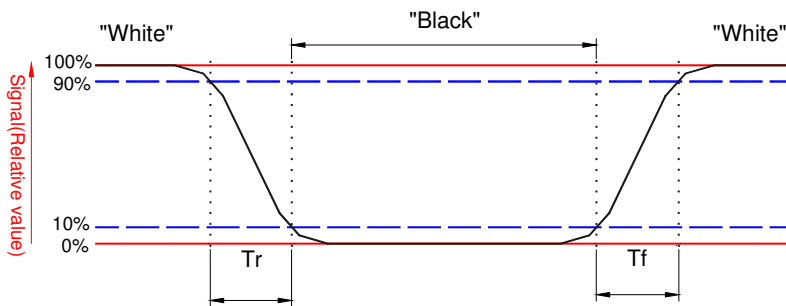
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



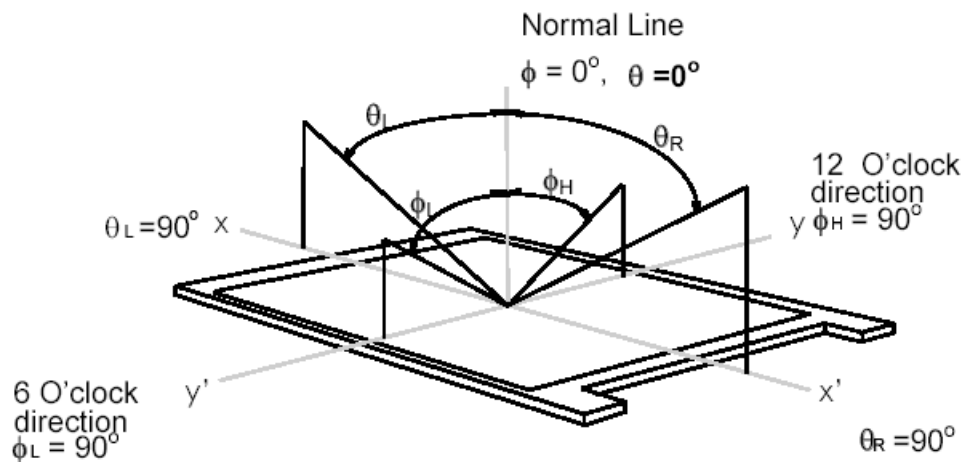
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



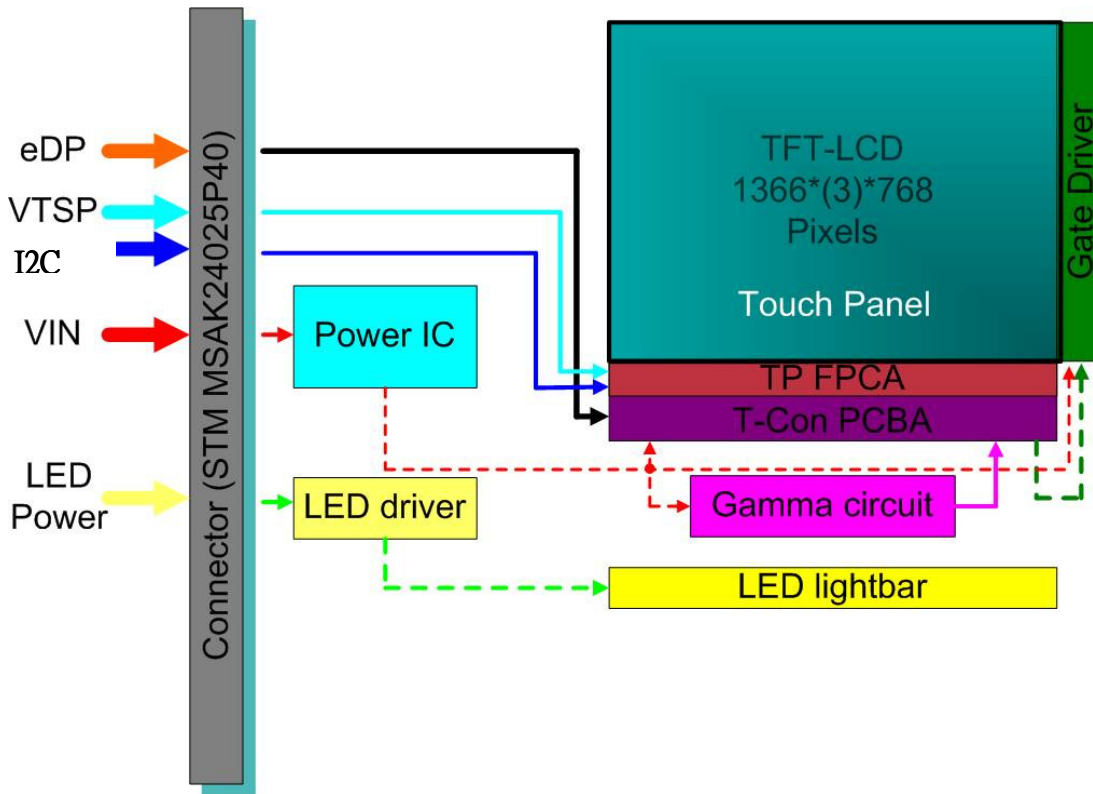
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 40 Pin (One CH/connector Module)



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

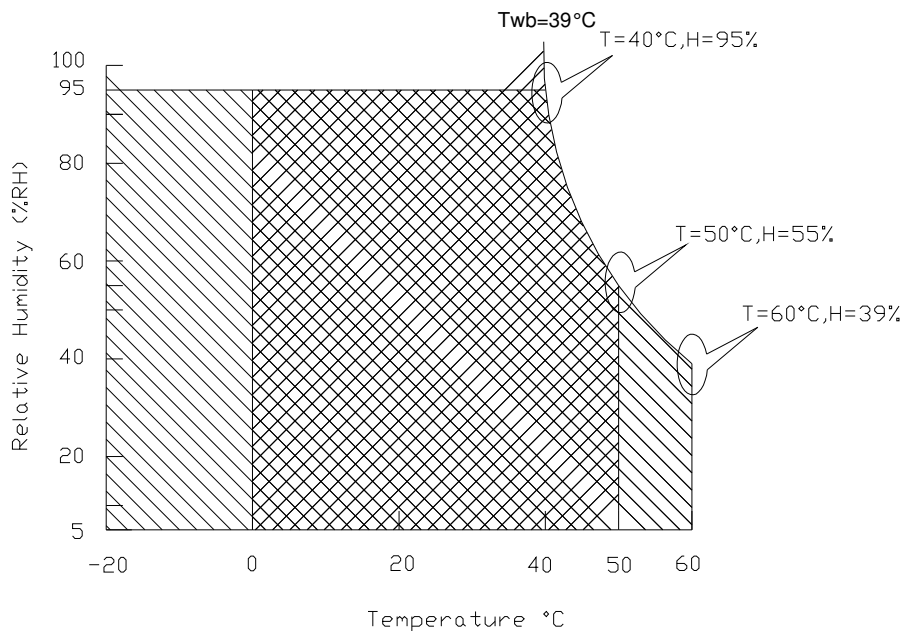
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

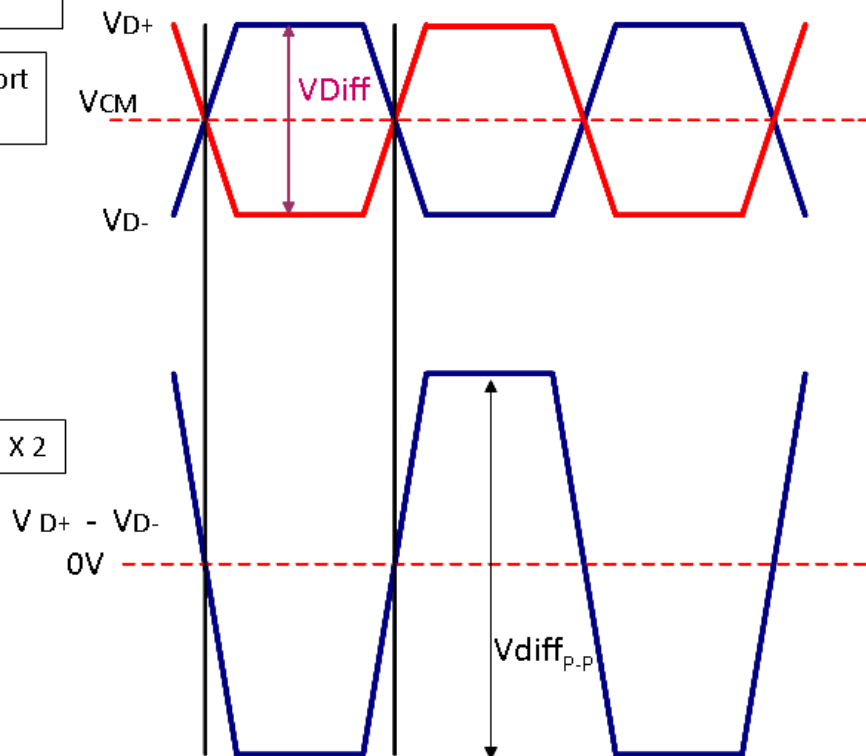
Signal electrical characteristics are as follows;

Display Port main link signal:

Differential pair VD+ , VD-
Which is one Display port
Main link

VCM of Display port
Main link

$$V_{diffP-P} = [(V_{D+}) - (V_{D-})] \times 2$$

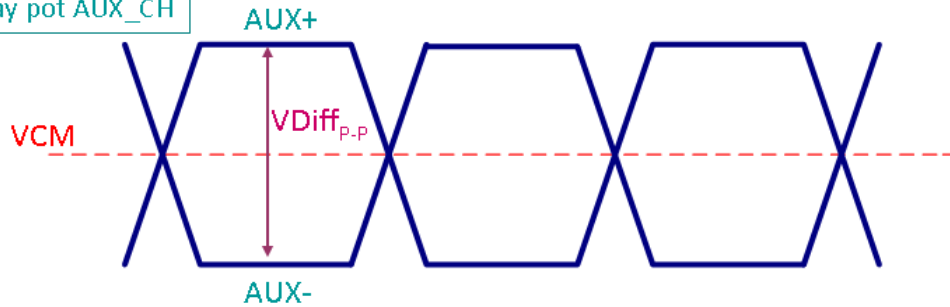


Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiffP-P	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Fallow as VESA display port standard V1.1a.

Display Port AUX_CH signal:

Differential AUX+ , AUX-
Which is Display port AUX_CH



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiffP-P	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Fallow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

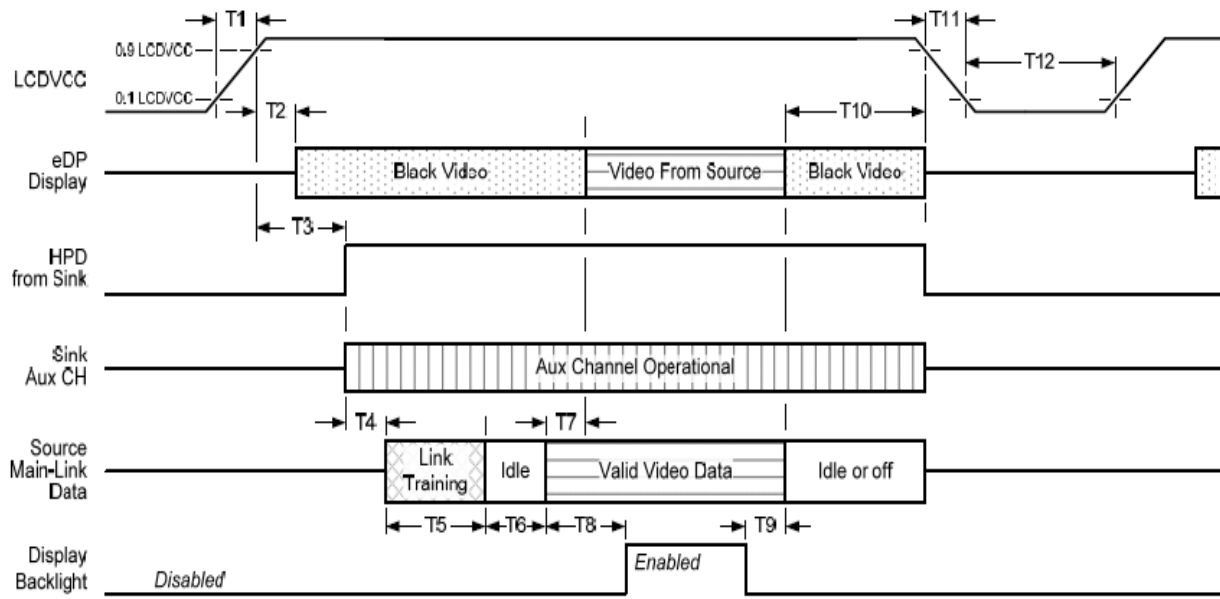
Fallow as VESA display port standard V1.1a.



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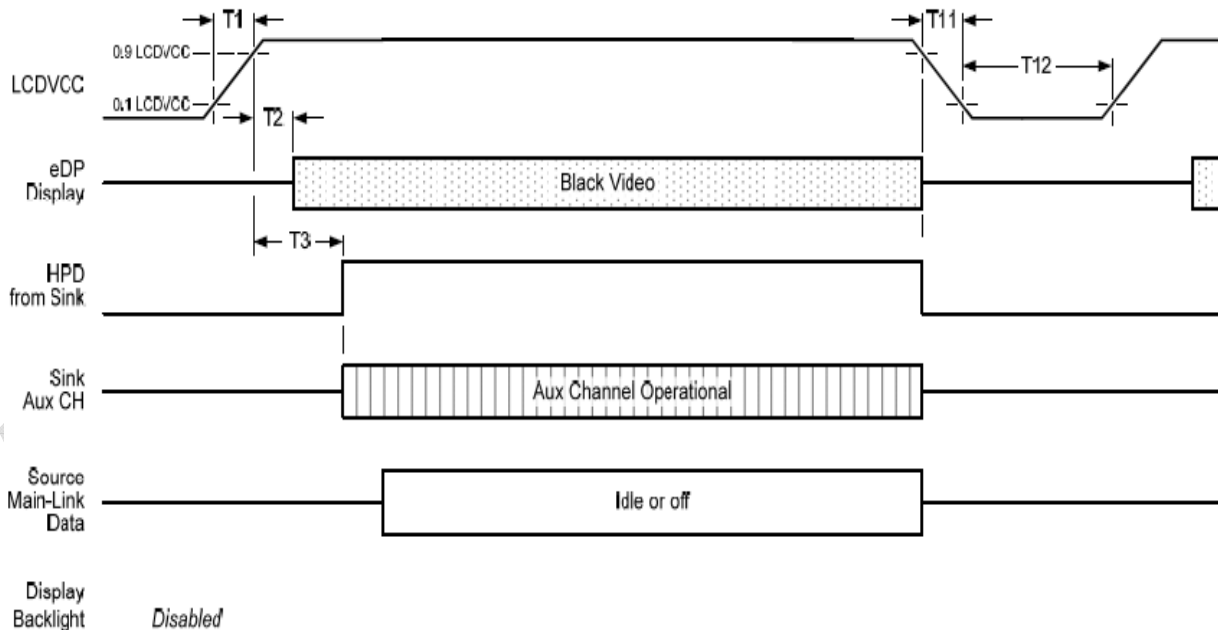
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Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only



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Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

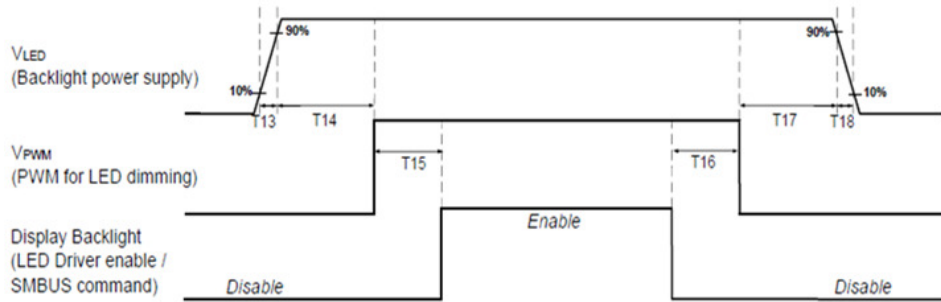
1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

- upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
- when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

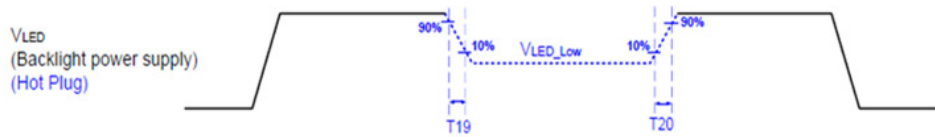
Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: $T19/T20 = 5 \times T_{PWM}^*$

* $T_{PWM} = 1/PWM \text{ Frequency}$



5.2 Touch Sensor

5.2 Touch Sensor Power Consumption

Items	Symbol	Specifications			Unit	Notes
		Min.	Typ.	Max.		
Touch Panel Power Supply	VDD	3.0	3.3	3.6	V	
The fully active state of the device.	Active		50		mW	
Selective Suspend State (5 seconds inactivity)	Idle		8.25		mW	

5.3 Backlight Unit

5.3.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	1.95	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 If=20 mA

Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.3.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6	12	21	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommended system pull up/down resistor no bigger than 10kohm.

6.1 Pixel Format Image

	1										1366											
1st Line	R	G	B	R	G	B										R	G	B	R	G	B
	⋮			⋮			⋮										⋮			⋮		
768th Line	R	G	B	R	G	B										R	G	B	R	G	B

6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or Compatible
Type / Part Number	I-PEX 20455-040E-12R or Compatible
Mating Housing/Part Number	I-PEX 20455-040T-12R or Compatible

6.2.2 Pin Assignment

Display Port is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	No connect
2	H_GND	High Speed Ground
3	NC	No connect
4	NC	No connect
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight ground
19	BL_GND	Backlight ground
20	BL_GND	Backlight ground
21	BL_GND	Backlight ground
22	BL_Enable	Backlight On / Off
23	BL_PWM_DIM	System PWM signal Input
24	NC	No connect
25	NC	No connect
26	NC	No connect
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	NC	No connect
31	TP_DN	
32	TP_DP	
33	GND	Ground-Shield
34	VTSP	Touch panel power supply (3.3V)
35	VTSP	Touch panel power supply (3.3V)
36	TP_EN	Touch function enable pin
37	TP_CLK	I2C CLK for Touch
38	TP_SDA	I2C Data for Touch
39	INT	Interrupt for Touch
40	RST	Reset for Touch

Note1 : start from right side

Note2 : Input signals shall be low or High-impedance state when VDD is off.

6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T _{Clock}	72.4	75	80	MHz
Vertical Section	Period	T _V	790	808	768+A	T _{Line}
	Active	T _{VD}	768			
	Blanking	T _{VB}	20	40	A	
Horizontal Section	Period	T _H	1526	1547	1366+B	T _{Clock}
	Active	T _{HD}	1366			
	Blanking	T _{HB}	160	181	B	

Note 1 : The above is as optimized setting

Note 2 : DE mode only

Note 3 : The maximum clock frequency = $(1366+B) \times (768+A) \times 60 < 80\text{MHz}$

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 35%RH, 300h	
Low Temperature Storage	Ta= -20°C, 50%RH, 250h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

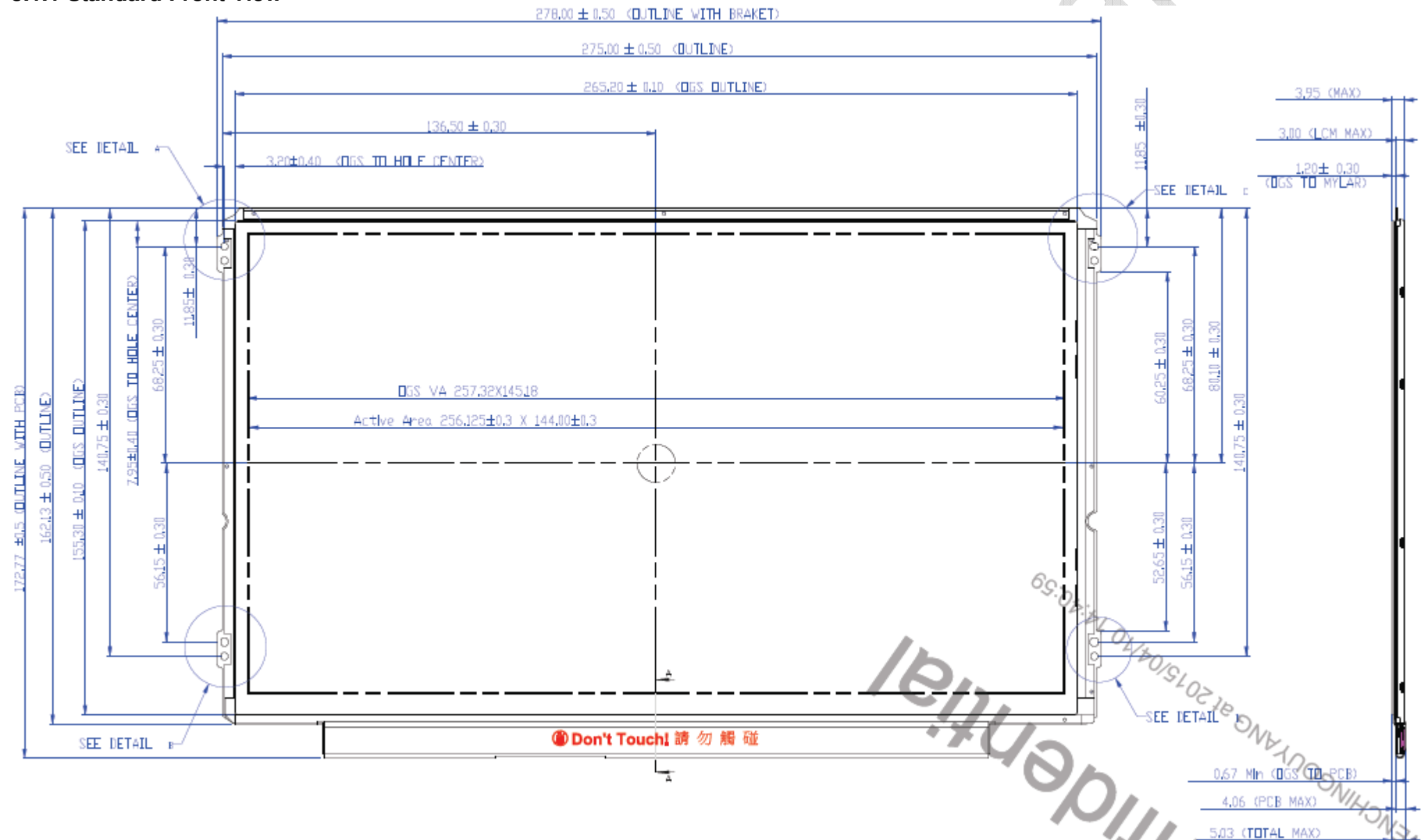
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed.
Self-recoverable.

No data lost, No hardware failures.

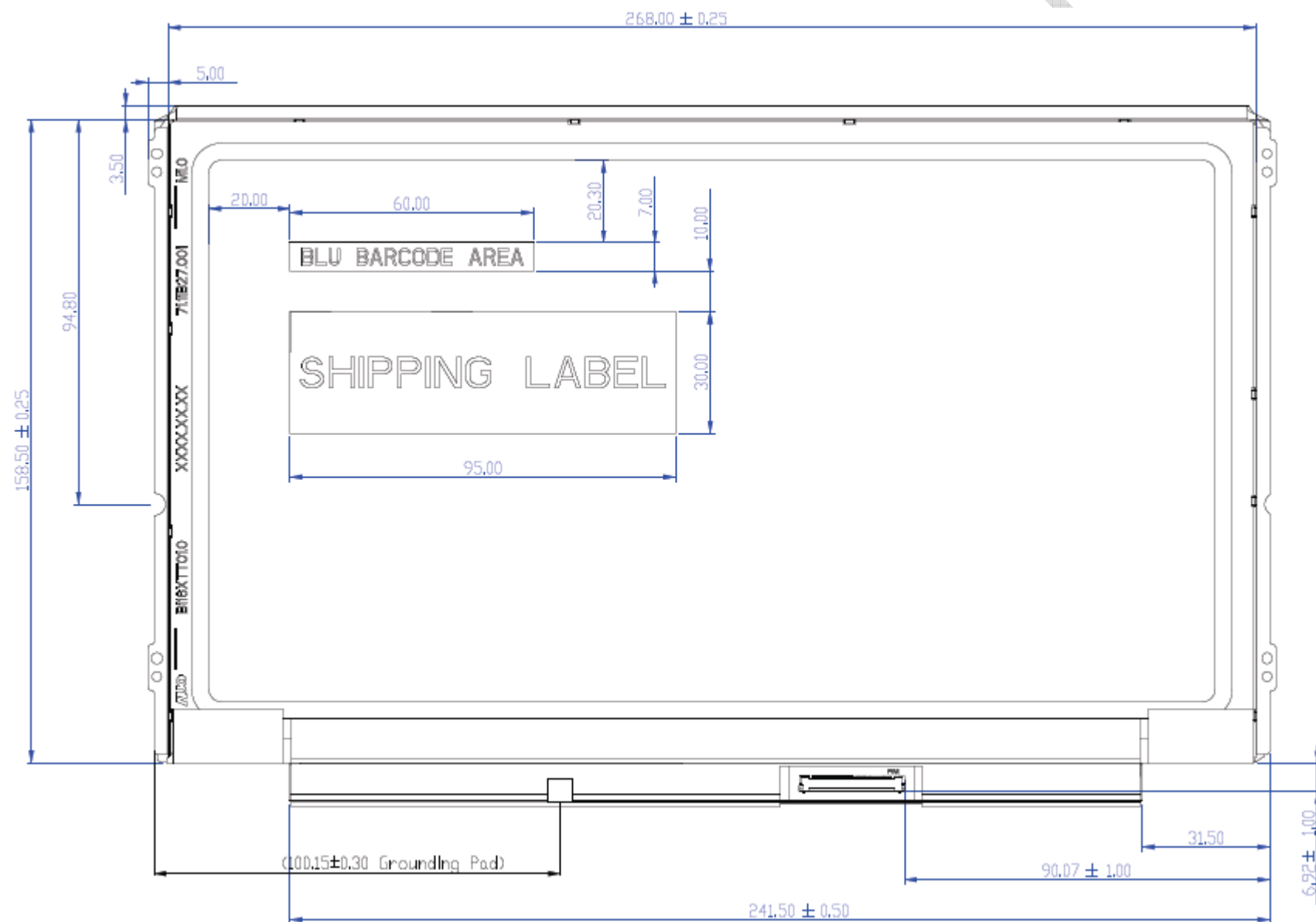
8. Mechanical Characteristics

8.1 LCM Outline Dimension

8.1.1 Standard Front View




8.1.2 Standard Rear View



9. Shipping and Package


9.1 Shipping Label Format


XXXXXXXXXXXX-XXXXXX



CN-OKY05P-72090
XXX-XXXX-A00
Made in China
DP/N OKY05P

Manufactured YY/MM
Model No: B116XTT01.1
AU Optronics
MADE IN CHINA (S01)
H/W: 1A F/W: 0

c  US
E204356





9.1 Carton Label Format

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QTY : 40



MODEL NO : B116XTT01.1

PART NO : 97.11B27.101

CUSTOMER NO :

CARTON NO :

Made in China


ZS0100-0652300205

PKGID (3S) 720907209054P000001 OKY05P 03



DP/N

OKY05P



Box Qty

40

Made In China



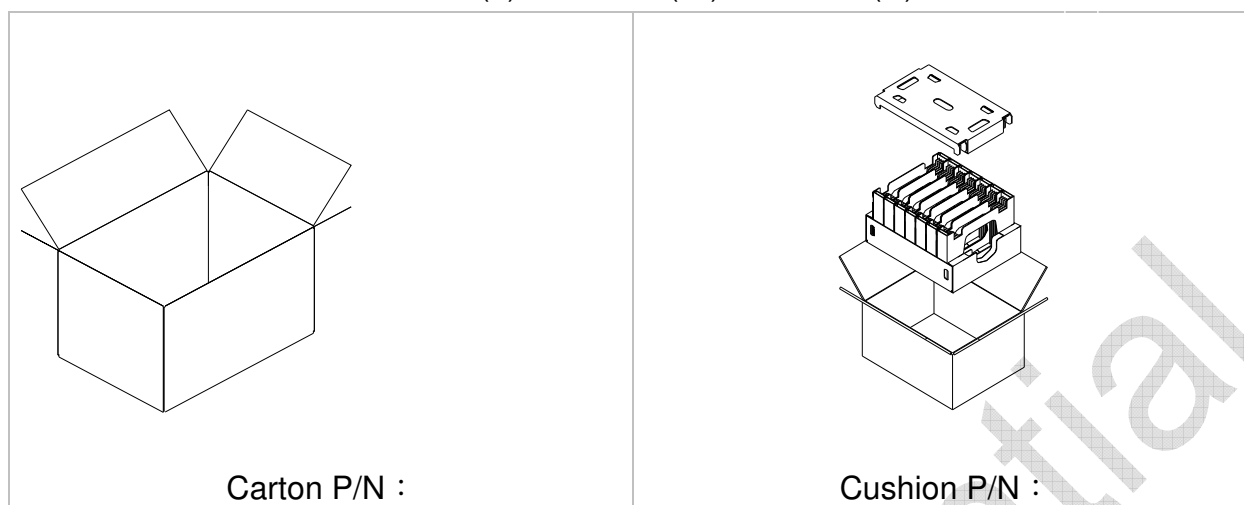

Rev. A00


Vendor ID | Loc ID
72090 | 72090


Mfg Id
72090

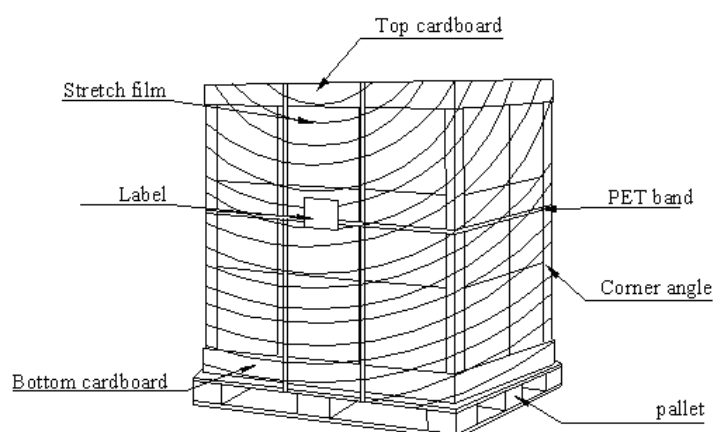
9.2 Carton Package

The outside dimension of carton is 460 (L)mm x 375 (W)mm x 268 (H)mm



- Pallet : **1140mm*890mm*138mm**
- Stretch film : **500mm (W)*300M (L)**

9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
0	Header	00	00000000	0	
1	Header	FF	11111111	255	
2	Header	FF	11111111	255	
3	Header	FF	11111111	255	
4	Header	FF	11111111	255	
5	Header	FF	11111111	255	
6	Header	FF	11111111	255	
7	Header	00	00000000	0	
8	EISA manufacture code = 3 Character ID	06	00000110	6	
9	EISA manufacture code (Compressed ASCII)	AF	10101111	175	
0A	Panel Supplier Reserved – Product Code	5C	01011100	92	
0B	Panel Supplier Reserved – Product Code	11	00010001	17	
0C	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0	
0D	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0	
0E	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0	
0F	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0	
10	Week of manufacture	24	00100100	36	
11	Year of manufacture	18	00011000	24	
12	EDID structure version # = 1	01	00000001	1	
13	EDID revision # = 4	04	00000100	4	
14	Video I/P definition	95	10010101	149	
15	Max H image size = ?? cm(Rounded to cm)	1A	00011010	26	
16	Max V image size = ?? cm(Rounded to cm)	0E	00001110	14	
17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78	01111000	120	
18	Feature support	02	00000010	2	
19	Red/Green Low bit (RxRy/GxGy)	6B	01101011	107	
1A	Blue/White Low bit (BxBY/WxWy)	F5	11110101	245	
1B	Red X Rx = 0.???	91	10010001	145	
1C	Red Y Ry = 0.???	55	01010101	85	
1D	Green X Rx = 0.???	54	01010100	84	
1E	Green Y Ry = 0.???	91	10010001	145	
1F	Blue X Rx = 0.???	27	00100111	39	
20	Blue Y Ry = 0.???	22	00100010	34	
21	White X Rx = 0.???	50	01010000	80	
22	White Y Ry = 0.???	54	01010100	84	
23	Established timings 1 (00h if not used)	00	00000000	0	
24	Established timings 2 (00h if not used)	00	00000000	0	
25	Manufacturer's timings (00h if not used)	00	00000000	0	
26	Standard timing ID1 (01h if not used)	01	00000001	1	
27	Standard timing ID1 (01h if not used)	01	00000001	1	
28	Standard timing ID2 (01h if not used)	01	00000001	1	

29	Standard timing ID2 (01h if not used)	01	00000001	1	
2A	Standard timing ID3 (01h if not used)	01	00000001	1	
2B	Standard timing ID3 (01h if not used)	01	00000001	1	
2C	Standard timing ID4 (01h if not used)	01	00000001	1	
2D	Standard timing ID4 (01h if not used)	01	00000001	1	
2E	Standard timing ID5 (01h if not used)	01	00000001	1	
2F	Standard timing ID5 (01h if not used)	01	00000001	1	
30	Standard timing ID6 (01h if not used)	01	00000001	1	
31	Standard timing ID6 (01h if not used)	01	00000001	1	
32	Standard timing ID7 (01h if not used)	01	00000001	1	
33	Standard timing ID7 (01h if not used)	01	00000001	1	
34	Standard timing ID8 (01h if not used)	01	00000001	1	
35	Standard timing ID8 (01h if not used)	01	00000001	1	
36	Pixel Clock/10,000 (LSB)	89	10001001	137	
37	Pixel Clock/10,000 (MSB)	1D	00011101	29	
38	Horizontal Active = ??? pixels (lower 8 bits)	56	01010110	86	
39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	D0	11010000	208	
3A	Horizontal Active/Horizontal blanking (Thbp) (upper 4:4 bits)	50	01010000	80	
3B	Vertical Active = ??? lines	00	00000000	0	
3C	Vertical Blanking (Tvbp) = ?? lines (DE Blanking typ. for DE only panels)	20	00100000	32	
3D	Vertical Active : Vertical Blanking (Tvbp) (upper 4:4 bits)	30	00110000	48	
3E	Horizontal Sync, Offset (Thfp) = ?? pixels	28	00101000	40	
3F	Horizontal Sync, Pulse Width = ??? pixels	20	00100000	32	
40	Vertical Sync, Offset (Tvfp) = ? lines Sync Width = ? lines	36	00110110	54	
41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0	
42	Horizontal Image Size = ??? mm	00	00000000	0	
43	Vertical image Size = ??? mm	90	10010000	144	
44	Horizontal Image Size / Vertical image size	10	00010000	16	
45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0	
46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0	
47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no stereo, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26	
48	Pixel Clock/10,000	89	10001001	137	

	(LSB)				
49	Pixel Clock/10,000 (MSB)	1D	00011101	29	
4A	Horizontal Active = xxxx pixels (lower 8 bits)	56	01010110	86	
4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	5A	01011010	90	
4C	Horizontal Active/Horizontal blanking (Thbp) (upper 4:4 bits)	52	01010010	82	
4D	Vertical Active = xxxx lines	00	00000000	0	
4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	20	00100000	32	
4F	Vertical Active : Vertical Blanking (Tvbp) (upper 4:4 bits)	30	00110000	48	
50	Horizontal Sync, Offset (Thfp) = xxxx pixels	28	00101000	40	
51	Horizontal Sync, Pulse Width = xxxx pixels	20	00100000	32	
52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	36	00110110	54	
53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0	
54	Horizontal Image Size =xxx mm	00	00000000	0	
55	Vertical image Size = xxx mm	90	10010000	144	
56	Horizontal Image Size / Vertical image size	10	00010000	16	
57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0	
58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0	
59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0]: See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26	
5A	Flag	00	00000000	0	
5B	Flag	00	00000000	0	
5C	Flag	00	00000000	0	
5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254	
5E	Flag	00	00000000	0	
5F	Dell P/N 1st Character	4B	01001011	75	
60	Dell P/N 2nd Character	59	01011001	89	
61	Dell P/N 3rd Character	30	00110000	48	
62	Dell P/N 4th Character	35	00110101	53	
63	Dell P/N 5th Character	50	01010000	80	
64	EDID Revision Bit[6:0] See charts below Bit[7] 0: X-rev, 1: A-rev	80	10000000	128	
65	Manufacturer P/N	42	01000010	66	
66	Manufacturer P/N	31	00110001	49	
67	Manufacturer P/N	31	00110001	49	

68	Manufacturer P/N	36	00110110	54	
69	Manufacturer P/N	58	01011000	88	
6A	Manufacturer P/N	54	01010100	84	
6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	54	01010100	84	
6C	Flag	00	00000000	0	
6D	Flag	00	00000000	0	
6E	Flag	00	00000000	0	
6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00	00000000	0	
70	Flag	00	00000000	0	
71	Color Management	00	00000000	0	
72	Panel Structure	41	01000001	65	
73	Frame Rate	22	00100010	34	
74	Light Controller Interface and Luminance	96	10010110	150	
75	Outdoor Features	01	00000001	1	
76	Multi-Media Features	11	00010001	17	
77	Multi-Media Features	00	00000000	0	
78	Special Features #1	00	00000000	0	
79	Special Features #2	0A	00001010	10	
7A	Special Features #3	01	00000001	1	
7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10	
7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32	
7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32	
7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0	
7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	5F	01011111	95	