# LCD MODULE

# SPECIFICATION

**Module Size:** 10.75 WQXGA

**Date:** 2019.07.26

**Version:** A

# Revision History

| Version | Revise Date | Page | Content | Prepared by |
|---|---|---|---|---|
| A | 2019-07-26 | All | New | Julin.huang |
| | | | | |
| | | | | |

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# 1 General Specification

## 1.1 Features

--TM type for main TFT-LCD panel
--One backlight with 4*9pcs white LEDs
-- MIPI 8 lanes
-- 2*39 Pin ZIF connector
--This product accords with RoHS and REACH environmental criterion.

## 1.2 Application

Display terminals for Tablet

## 1.3 General Specification

| No. | Item | Specification | Unit | Remark |
|---|---|---|---|---|
| 1 | Display Size | 10.75 | Inch | |
| 2 | ITO Technology Type | A-si | | |
| 3 | Liquid Crystal Alignment Method | IPS | | |
| 4 | Resolution | 1600*RGB*2560 | | |
| 5 | Display mode | Transmissive | | |
| 6 | Color Depth | 16.7M | | |
| 7 | Viewing Direction | All direction | | Note 1 |
| 8 | Contrast Ratio | 1000 min/1200typ | | |
| 9 | Luminance | 320/400 Typ | $cd/m^2$ | |
| 10 | Module Size | 150.62*242.652*1.90 | mm | Note 1 |
| 11 | COG step width | NA | mm | |
| 12 | Maximum Thickness | 2.05mmMax type=1.90±0.15 | mm | Note 1 |
| 13 | Panel Active Area | 144.72(W)*231.552(H) | mm | Note 1 |
| 14 | Pixel Size | 30.15*90.45 | um | |
| 15 | Pixel Pitch | 90.45*90.45 | um | |
| 16 | Pixel Aspect Ratio | 1:1 | | |
| 17 | Driver IC RAM Size | TBD | | |
| 18 | Driver IC | Ramless | | Panel e Ramless |
| 19 | Light Source | LED Backlight | | TBD |
| 20 | Interface | MIPI 8 lane@ 1Gbqs/ lane | | max |

| | | | | |
|---|---|---|---|---|
| 21 | Vcom type | DC Vcom | | |
| 22 | Driver Inversion type | Column Inversion & Zig-Zag | | |
| 23 | Operation Temperature | -10~+60 | degC | |
| 24 | Storage Temperature | -30~+70 | degC | |
| 25 | Weight | 120g Max | Gram | |
| 26 | Pixel Per inch | 281 | PPI | |
| 27 | Environmental Protection Requirement | RoHS & REACH must be executed | | |
| 28 | Connection method | LCD Conn:<br>39pin ZIF Connector*2<br>TP Conn:<br>8pin ZIF Connector | | |
| 29 | Color Enhancement | Hue and saturation can be adjusted separately.<br>The hue of flesh tone, red, green, blue can be adjusted separately.<br>Have a global saturation level.<br>The saturation of each color can be adjusted separately to be larger or smaller than original.<br>One color's saturation can only affect neighborhood color, but cannot affect far away color. | | For example,adjust flesh tone's saturation can affect orange to yellow,but can not affect green and blue . |
| 30 | Contrast Enhancement | Have the obvious global contrast enhancement effect, that is making bright part in the picture brighter, dark park in the picture darker. And the bright part can't be over-saturated, dark part can't be too dark to lose detail. can not cause contour, noisy, face abnormal problems. | | |
| 31 | CABC Function | Must keep full white picture to be max brightness.<br>Can reduce at least 5%~10% power on wechat, internet applications.<br>No flicker, gray ramp unsmooth, gray transition sudden change.<br>Data compensation must work correctly. Color hue can't be changed | | |

| | | | | |
|---|---|---|---|---|
| | | when turn on CABC. | | |
| 32 | Gamma Correction | After gamma, gray pattern transition should be smooth, no step, no luma or color temperature sudden change. | | |
| 33 | White balance adjustment | Can use this function to adjust the white balance(or color temperature) of each panel.independent of gamma. | | |
| 34 | Front Polarizer Type | Hard coating | 3H | |
| 35 | Panel gate scan direction reverse | Support | | |
| 36 | warpage | Front side warpage value is <0.5mm. Rear side warpage value is < 0.5mm). | | Note 2 Testing warpage data in first sample. If the warpage does not meet 0.3mm, according to 0.4mm control. |
| 37 | Diagonal Stripes&Morie | Invisible | | Note 3 |

## Connector specification (39pin ZIF)

| No. | Item | Specification | Unit |
|---|---|---|---|
| 1 | **Pin number** | **39Pin** | |
| 2 | **Pitch** | **0.3** | **mm** |
| 3 | **Outline** | **13.8*3.5*1.0 Max** | **mm** |
| 4 | **Current** | **0.3 AC/DC [AWG 40](per contact)** | **A** |
| 5 | **Voltage** | **100 AC** | **V** |
| 6 | **Contact Resistance** | **120 Max** | **mΩ** |
| 7 | **Dielectric Withstanding Voltage** | **250V AC (rms), 1min, No creeping discharge, flashover, nor insulator breakdown shall occur.** | |
| 8 | **Insulation Resistance** | **DC250V between the neighboring contacts. R≥500MΩ(intial)** | |
| 9 | **Durability** | **30 cycles at a speed 25±3mm/min. along the mating axis** | |
| 10 | **Voltage Standing Wave Ratio (Vswr)** | **0-6GHz，Vswr≤2** | |
| 11 | **Mating force** | **10 Max** | **N** |
| 12 | **Un-mating force** | **3 Min** | **N** |
| 13 | **Contact retention force** | **≥0.2 per Pin** | **N** |

## Connector specification (8pin ZIF)

| No. | Item | Specification | Unit |
|---|---|---|---|

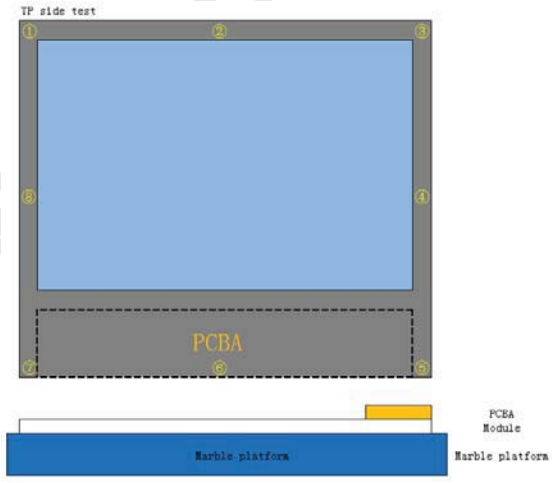
| | | | |
|---|---|---|---|
| 1 | Pin number | 8 Pin | |
| 2 | Pitch | 0.5 | mm |
| 3 | Outline | 6*3.2*1.1 Max | mm |
| 4 | Current | 0.3 AC/DC [AWG 40](per contact) | A |
| 5 | Voltage | 100 AC | V |
| 6 | Contact Resistance | 120 Max | mΩ |
| 7 | Dielectric Withstanding Voltage | 250V AC (rms), 1min, No creeping discharge, flashover, nor insulator breakdown shall occur. | |
| 8 | Insulation Resistance | DC250V between the neighboring contacts. R≥500MΩ(intial) | |
| 9 | Durability | 30 cycles at a speed 25±3mm/min. along the mating axis | |
| 10 | Voltage Standing Wave Ratio (Vswr) | 0-6GHz，Vswr≤2 | |
| 11 | Mating force | 10 Max | N |
| 12 | Un-mating force | 3 Min | N |
| 13 | Contact retention force | ≥0.2 per Pin | N |

Note 1:Please Refer to the mechanical drawing.

Warning: Some GOP panel cannot support gate bidirectional scanning, or even some gate bidirectional scanning GOP panel are abnormal working when the gate scanning direction set to be reversed.

Note 2: Warpage inspected by measuring system to analyze surface warpage and module thickness.

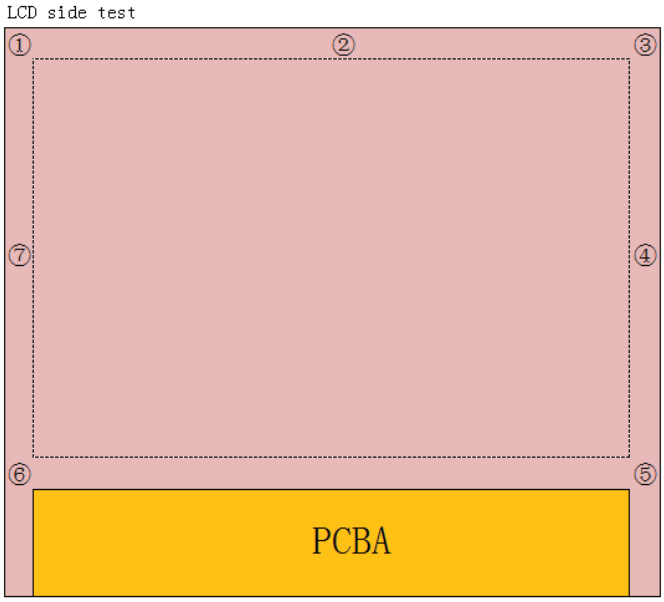
[1] Tp side test




- Remove protect film of TP side,put glass face down on the marble platform as shown in the figure.
- Smooth around bezel tape in order to prevent the bubble impact test.

- Test the warpage of TP side with feeler guage in order of 1,2,3,4,5,6,7,8.

[2] LCD side test





- Remove protect film of both side,put backlight face down on the marble platform as shown in the figure.
- Smooth around bezel tape in order to prevent the bubble impact test.
- Test the warpage of LCD side with feeler guage in order of 1,2,3,4,5,6,7.

Note 3: Viewing distance: 20cm to 25cm.

Viewing angle: $\theta_L$ <45° , $\theta_R$ <45° , $\psi_T$<45°, $\psi_B$<45° .

The viewing angle Refer to Note 9.

# 2 Pin Assignments

**LCD CN1**

| Pin No | Symbol | Description | Note |
|---|---|---|---|
| 1 | VSP | Positive gamma high voltage.(5.8V) | |
| 2 | VSP | Positive gamma high voltage.(5.8V) | |
| 3 | NC | NC | |
| 4 | NC | NC | |
| 5 | VSN | Negative gamma high voltage.(-5.8V) | |
| 6 | VSN | Negative gamma high voltage.(-5.8V) | |
| 7 | NC | NC | |
| 8 | NC | NC | |
| 9 | GND | Ground | |
| 10 | D0PA | MIPI Signal | |
| 11 | D0NA | MIPI Signal | |
| 12 | GND | Ground | |
| 13 | D1PA | MIPI Signal | |
| 14 | D1NA | MIPI Signal | |
| 15 | GND | Ground | |
| 16 | CLKPA | MIPI Signal | |
| 17 | CLKNA | MIPI Signal | |
| 18 | GND | Ground | |
| 19 | D2PA | MIPI Signal | |
| 20 | D2NA | MIPI Signal | |
| 21 | GND | Ground | |
| 22 | D3PA | MIPI Signal | |
| 23 | D3NA | MIPI Signal | |
| 24 | GND | Ground | |
| 25 | GND | Ground | |
| 26 | NC | NC | |
| 27 | LED6 | LED Current FB6 | 预留接口 |
| 28 | LED5 | LED Current FB5 | 预留接口 |

| | | | |
|---|---|---|---|
| 29 | LED4 | LED Current FB4 | |
| 30 | LED3 | LED Current FB3 | |
| 31 | LED2 | LED Current FB2 | |
| 32 | LED1 | LED Current FB1 | |
| 33 | NC | NC | |
| 34 | NC | NC | |
| 35 | VLED2 | LED Power | |
| 36 | VLED1 | LED Power | |
| 37 | NC | NC | |
| 38 | NC | NC | |
| 39 | GND | GND | |

LCD CN2

| Pin No | Symbol | Description | Note |
|---|---|---|---|
| 40 | NC | NC | |
| 41 | NC | NC | |
| 42 | GND | Ground | |
| 43 | ID0 | ID pin | GND |
| 44 | ID1 | ID pin | GND |
| 45 | LEDPWM | PWM OUT | |
| **46** | **NC** | **NC** | |
| 47 | IOVCC | Power supply for interface voltage and MIPI DSI-PHY (1.8V) | |
| 48 | IOVCC | Power supply for interface voltage and MIPI DSI-PHY (1.8V) | |
| 49 | RESET | Panel Reset | |
| 50 | GND | Ground | |
| 51 | D0PB | MIPI Signal | |
| 52 | D0NB | MIPI Signal | |
| 53 | GND | Ground | |
| 54 | D1PB | MIPI Signal | |
| 55 | D1NB | MIPI Signal | |
| 56 | GND | Ground | |
| 57 | CLKPB | MIPI Signal | |

| | | | |
|---|---|---|---|
| 58 | CLKNB | MIPI Signal | |
| 59 | GND | Ground | |
| 60 | D2PB | MIPI Signal | |
| 61 | D2NB | MIPI Signal | |
| 62 | GND | Ground | |
| 63 | D3PB | MIPI Signal | |
| 64 | D3NB | MIPI Signal | |
| 65 | GND | Ground | |
| 66 | NC | NC | |
| 67 | TP_AVDD | Power supply for touch analog circuit (3.3V) | |
| 68 | DVDD_IO | I/O Digital Power supply, TYP. 1.8V | |
| 69 | NC | NC | |
| 70 | TP_GND | Ground | |
| 71 | TP_RESET | Reset for touch | |
| 72 | TP_INT | State change interrupt for TSP | |
| 73 | I2C_SDA | SCL (I2C) for touch | |
| 74 | I2C_SCL | SCL (I2C) for touch | |
| 75 | GND | Ground | |
| 76 | GND | Ground | |
| 77 | NC | NC | |
| 78 | NC | NC | |

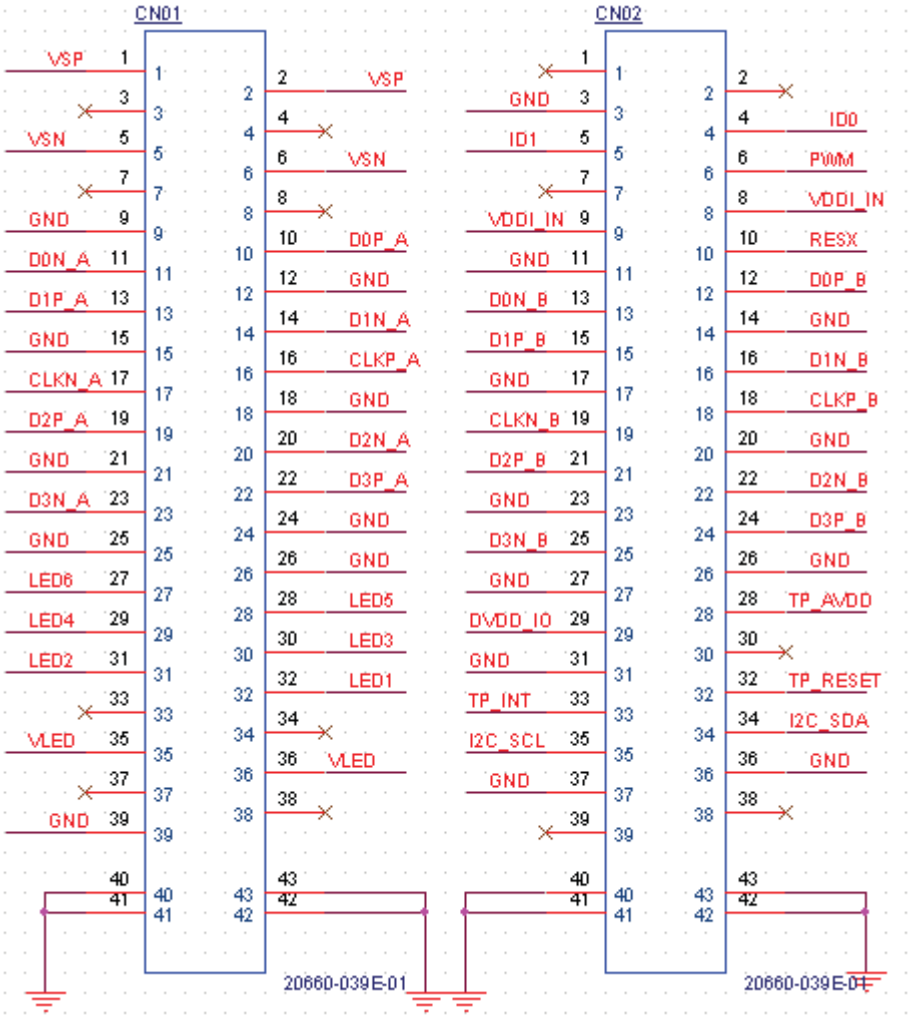
**TP CN**

| Pin No | Symbol | Description |
|---|---|---|
| 1 | TP_AVDD | Analog Power supply, TYP. 3.3V |
| 2 | DVDD_IO | I/O Digital Power supply, TYP. 1.8V |
| 3 | GND | Ground |
| 4 | TOUCH_RESET | Reset Pin，TYP 1.8V |
| 5 | TOUCH_INT | Interrupt Pin, TYP 1.8V |
| 6 | TP_SYNC | A:NC(Default)<br>B: TP_SYNC series 100 ohm resistor, Typ 1.8V |
| 7 | I2C_SDA | I2C SDA,TYP. 1.8V |

| | | |
|---|---|---|
| 8 | I2C_SCL | I2C CLK,TYP. 1.8V |

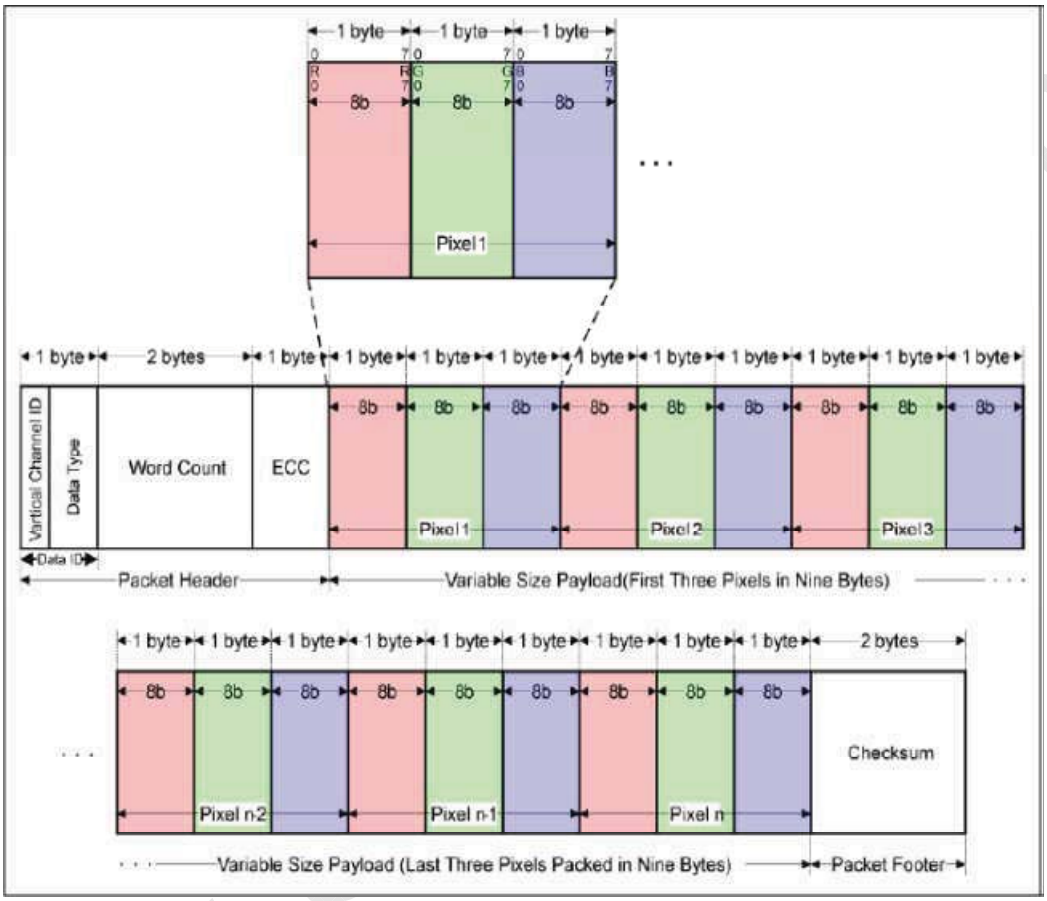
# 3 Schematic Circuit Diagram

## 3.1 MIPI Reference Circuit



# 4 Register & Pixel Data Format

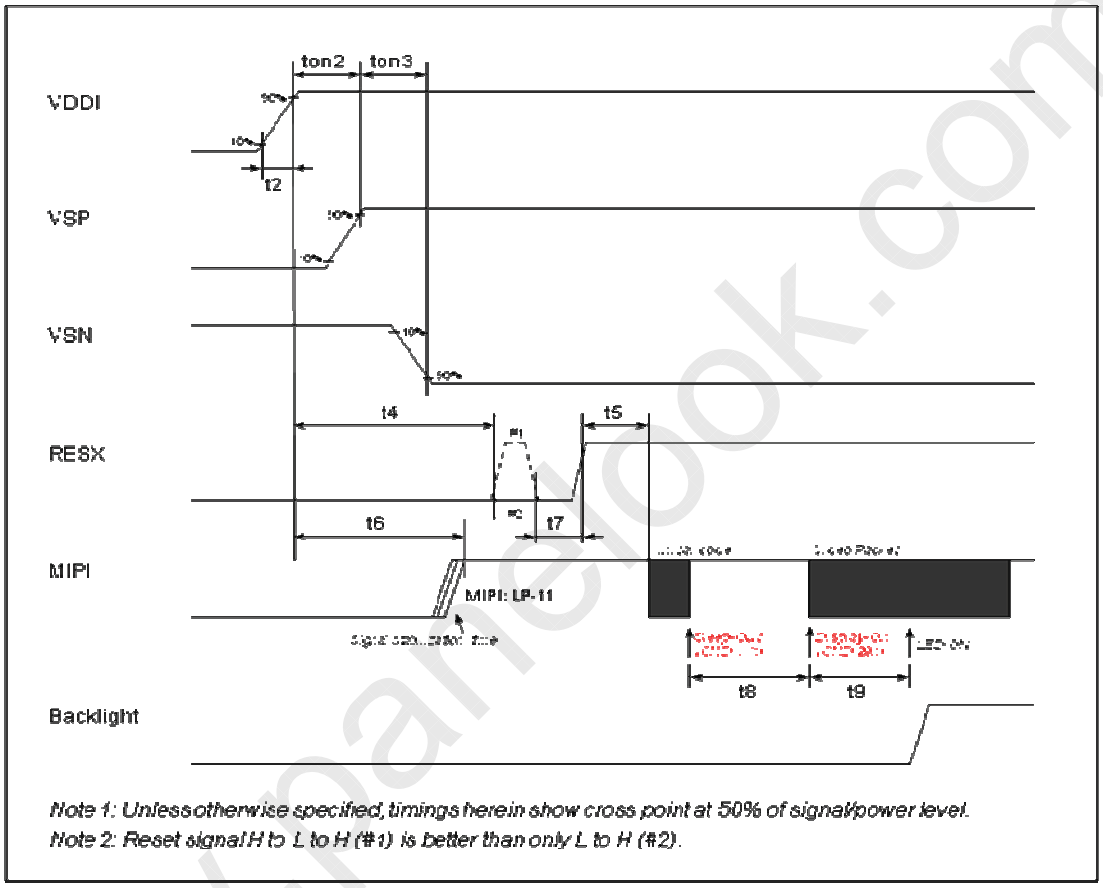
## 4.1 MIPI 24 bits RGB Data Format



# 5 Timing Characteristics

## 5.1 Power on/off Sequence

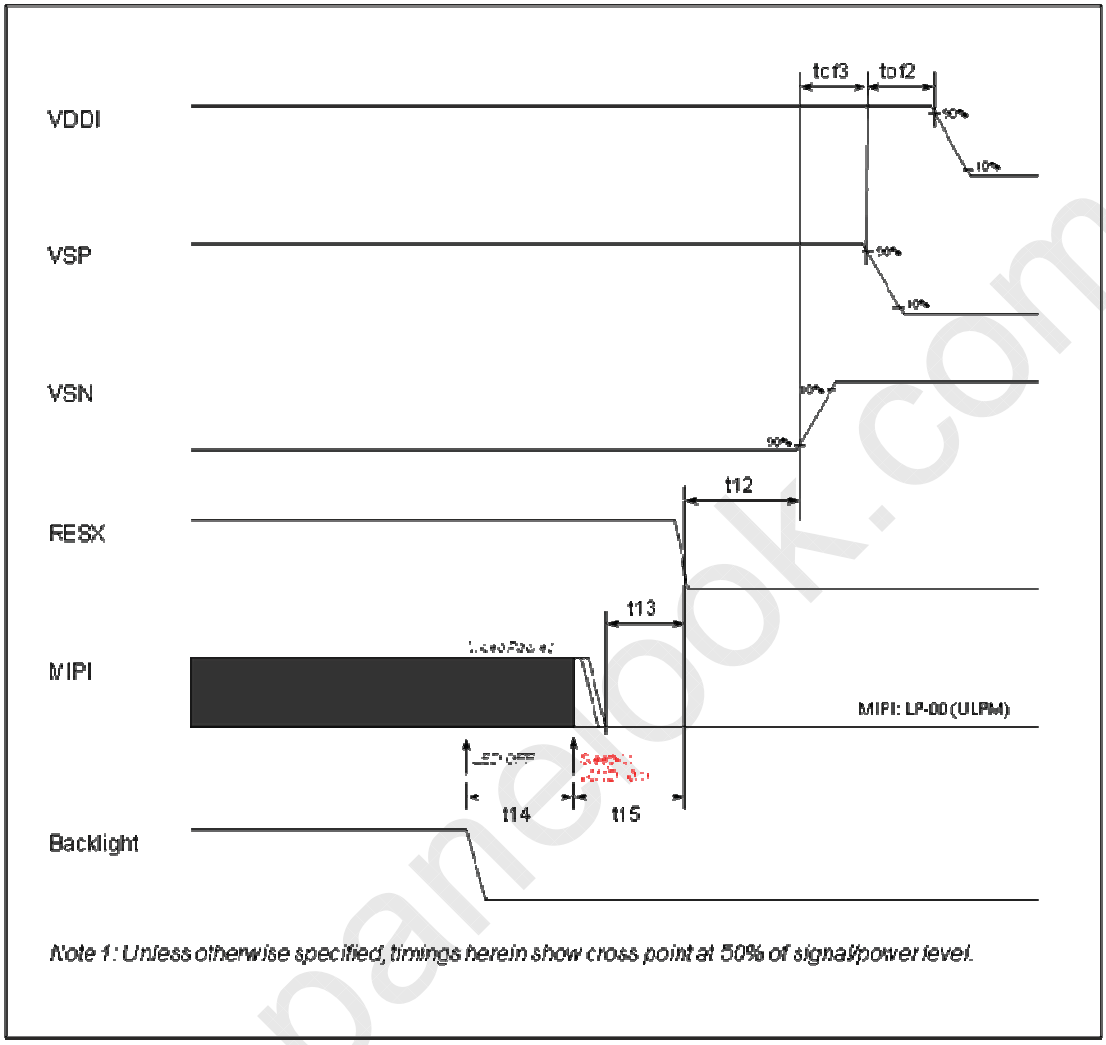
a) Power on sequence




*Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.*
*Note 2: Reset signal H to L to H (#1) is better than only L to H (#2).*

| Symbol | Value | | | Unit | Remark |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| ton2 | 0 | - | - | ms | |
| ton3 | 0 | - | - | ms | |
| t2 | - | - | 2 | ms | |
| t4 | 15 | - | - | ms | |
| t5 | 20 | - | - | ms | |
| t6 | 0 | - | t4 | ms | |
| t7 | 10 | - | - | μs | |
| t8 | 120 | - | - | ms | |
| t9 | 20 | - | - | ms | |

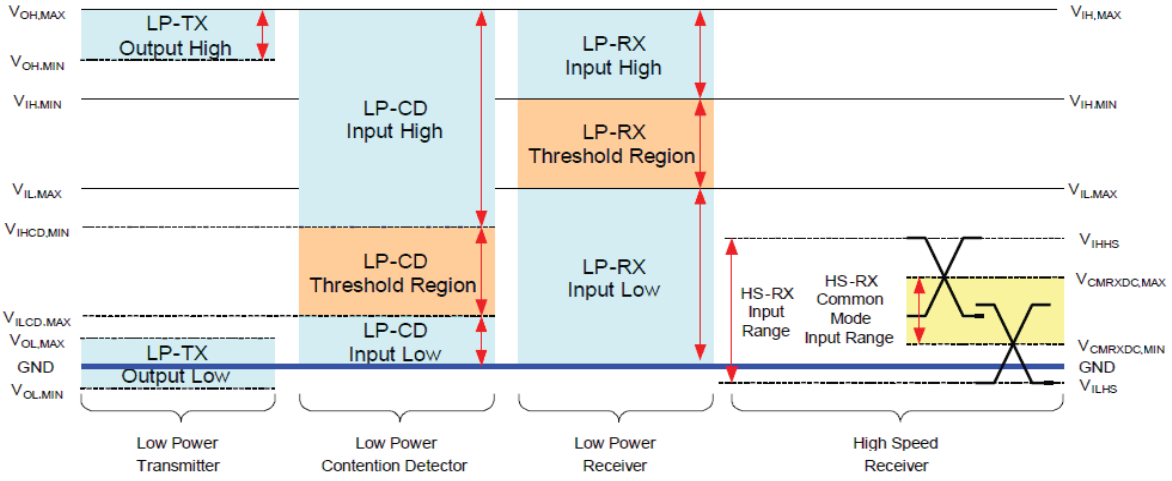
b) Power off sequence




*Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.*

| Symbol | Value | | | Unit | Remark |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| tof2 | 0 | - | - | ms | |
| tof3 | 0 | - | - | ms | |
| t12 | 0 | - | - | ms | |
| t13 | 0 | - | - | ms | |
| t14 | 0 | - | - | ms | |
| t15 | 100 | - | - | ms | |

## 5.2 MIPI Interface Characteristics




### 5.2.1 DC Electrical Characteristic

### 5.2.1.1. DC Characteristics for DSI LP Mode

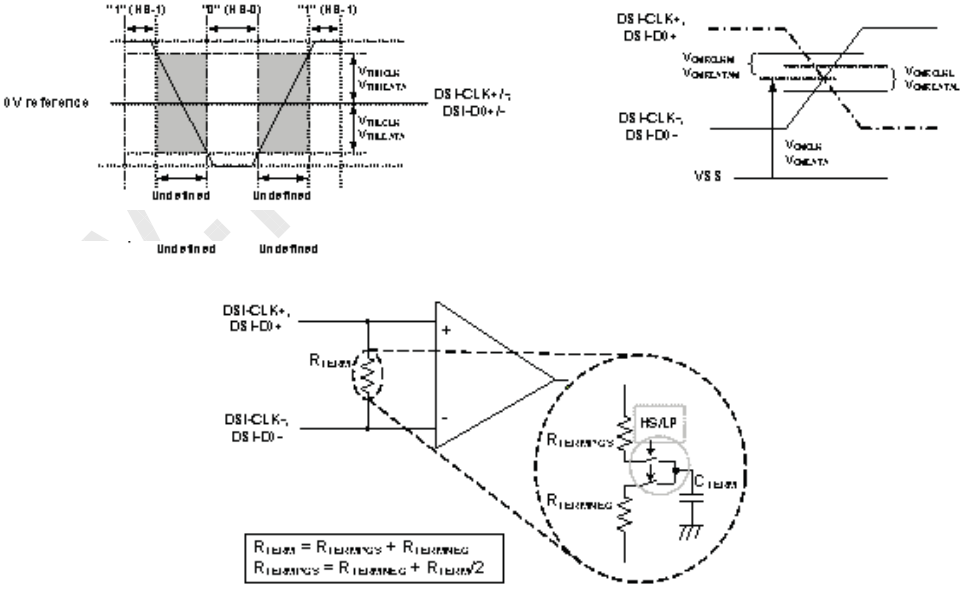
| Parameter | Symbol | Conditions | Specification | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Logic high level input voltage | $V_{IHLPCD}$ | LP-CD | 450 | - | 1350 | mV |
| Logic low level input voltage | $V_{ILLPCD}$ | LP-CD | 0 | - | 200 | mV |
| Logic high level input voltage | $V_{IHLPRX}$ | LP-RX (CLK, D0, D1) | 880 | - | 1350 | mV |
| Logic low level input voltage | $V_{ILLPRX}$ | LP-RX (CLK, D0, D1) | 0 | - | 550 | mV |
| Logic low level input voltage | $V_{ILLPRXULP}$ | LP-RX (CLK ULP mode) | 0 | - | 300 | mV |
| Logic high level output voltage | $V_{OHLPTX}$ | LP-TX (D0) | 1.1 | - | 1.3 | V |
| Logic low level output voltage | $V_{OLLPTX}$ | LP-TX (D0) | -50 | - | 50 | mV |
| Logic high level input current | $I_{IH}$ | LP-CD, LP-RX | - | - | 10 | μA |
| Logic low level input current | $I_{IL}$ | LP-CD, LP-RX | -10 | - | - | μA |
| Input pulse rejection | SGD | DSI-CLK+/-, DSI-Dn+/- (Note 3) | - | - | 300 | Vps |

*Note 1) VDDI=1.7~3.3V, VSP=5.3~5.9V, VSN=-5.3~-5.9V, GND=0V, Ta=-30 to 70 °C (to +85 °C no damage)*
*Note 2) DSI high speed is off.*
*Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.*

## 5.2.1.2. DC Characteristics for DSI HS Mode

| Parameter | Symbol | Conditions | Specification | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Input voltage common mode range | $V_{CMCLK}$ $V_{CMDATA}$ | DSI-CLK+/-, DSI-Dn+/- (Note2, 3) | 70 | - | 330 | mV |
| Input voltage common mode variation (≤ 450MHz) | $V_{CMRCLKL}$ $V_{CMRDATAL}$ | DSI-CLK+/-, DSI-Dn+/- (Note 4) | -50 | - | 50 | mV |
| Input voltage common mode variation (≥ 450MHz) | $V_{CMRCLKM}$ $V_{CMRDATAM}$ | DSI-CLK+/-, DSI-Dn+/- | - | - | 100 | mV |
| Low-level differential input voltage threshold | $V_{THLCLK}$ $V_{THLDATA}$ | DSI-CLK+/-, DSI-Dn+/- | -70 | - | - | mV |
| High-level differential input voltage threshold | $V_{THHCLK}$ $V_{THHDATA}$ | DSI-CLK+/-, DSI-Dn+/- | - | - | 70 | mV |
| Single-ended input low voltage | $V_{ILHS}$ | DSI-CLK+/-, DSI-Dn+/- (Note 3) | -40 | - | - | mV |
| Single-ended input high voltage | $V_{IHHS}$ | DSI-CLK+/-, DSI-Dn+/- (Note 3) | - | - | 460 | mV |
| Differential input termination resistor | $R_{TERM}$ | DSI-CLK+/-, DSI-Dn+/- | 80 | 100 | 125 | Ω |
| Single-ended threshold voltage for termination enable | $V_{TERM-EN}$ | DSI-CLK+/-, DSI-Dn+/- | - | - | 450 | mV |
| Termination capacitor | $C_{TERM}$ | DSI-CLK+/-, DSI-Dn+/- | - | - | 14 | pF |

*Note 1) VDDI=1.7~3.3V, VSP=5.3~5.9V, VSN=-5.3~-5.9V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)*
*Note 2) Includes 50mV (-50mV to 50mV) ground difference.*
*Note 3) Without $V_{CMRCLKM}$ / $V_{CMRDATAM}$ .*
*Note 4) Without 50mV (-50mV to 50mV) ground difference.*
*Note 5) Dn=D0, D1, D2 and D3.*




***Differential voltage range, termination resistor and Common mode voltage***

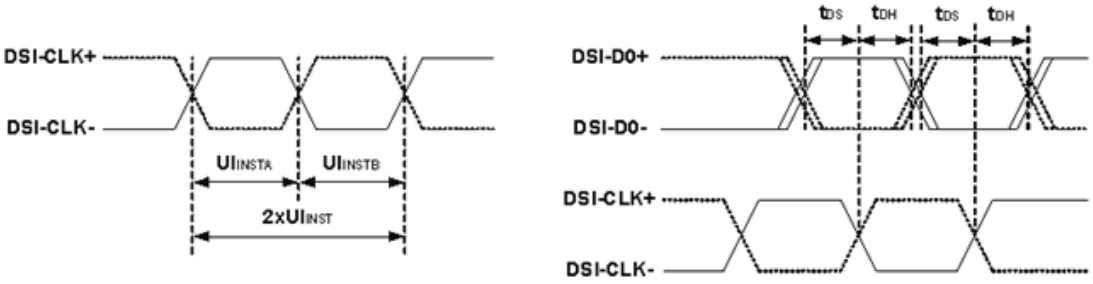
## 5.2.2. AC Electrical Characteristic

### 5.2.2.1. MIPI DSI Timing Characteristics

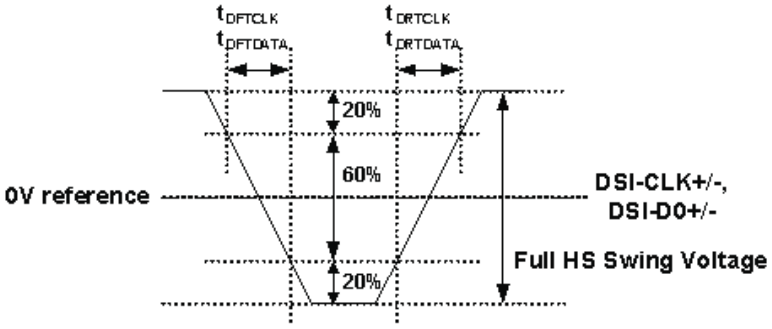
#### 5.2.2.1.1. High Speed Mode

| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit | Description |
|---|---|---|---|---|---|---|---|
| DSI-CLK+/- | $2xUI_{INST}$ | Double UI instantaneous | 2 | - | 5 | ns | 4 Lane (Note 2) |
| DSI-CLK+/- | $UI_{INSTA}$<br>$UI_{INSTB}$ | UI instantaneous halfs<br>($UI = UI_{INSTA} = UI_{INSTB}$) | 1 | - | 2.5 | ns | 4 Lane (Note 2) |
| DSI-Dn+/- | $t_{DS}$ | Data to clock setup time | 0.15xUI | - | - | ps | |
| DSI-Dn+/- | $t_{DH}$ | Data to clock hold time | 0.15xUI | - | - | ps | |
| DSI-CLK+/- | $t_{DRTCLK}$ | Differential rise time for clock | 150 | - | 0.3xUI | ps | |
| DSI-Dn+/- | $t_{DRTDATA}$ | Differential rise time for data | 150 | - | 0.3xUI | ps | |
| DSI-CLK+/- | $t_{DFTCLK}$ | Differential fall time for clock | 150 | - | 0.3xUI | ps | |
| DSI-Dn+/- | $t_{DFTDATA}$ | Differential fall time for data | 150 | - | 0.3xUI | ps | |

*Note 1) Dn = D0, D1, D2 and D3.*
*Note 2) Maximum total bit rate is 4Gbps for 24-bit data format, 3Gbps for 18-bit data format and 2.67Gbps for 16-bit data format in master-slave cascade application (4-lane x 2) which support to 1600RGBx 2560 resolution.*



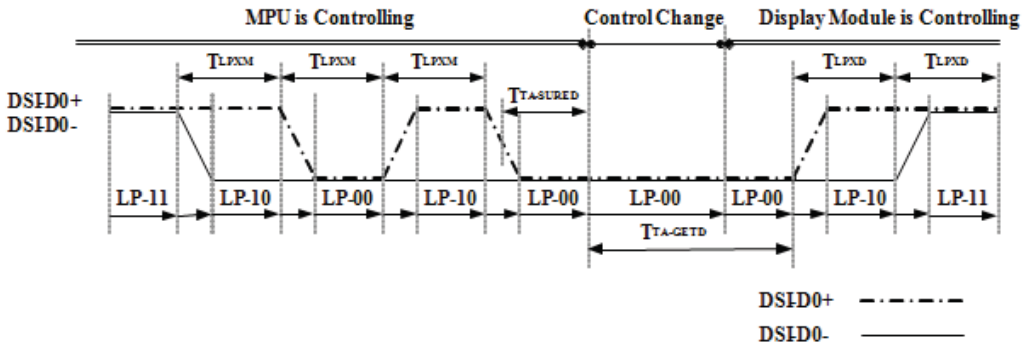

*DSI clock channel timing*



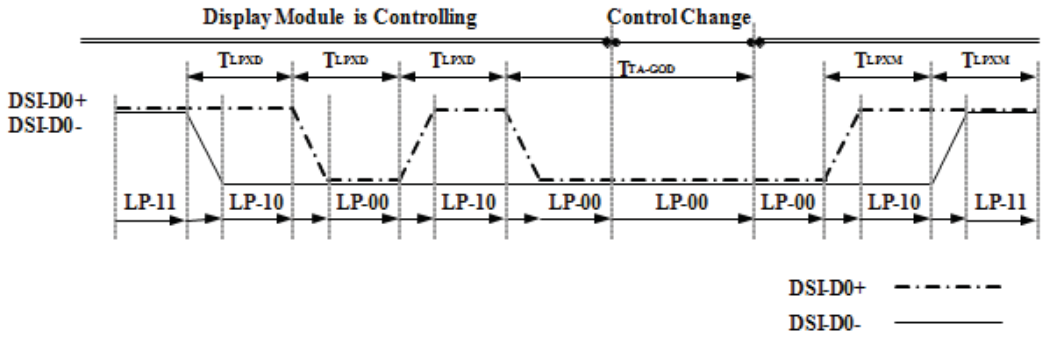

*Rising and fall time on clock and data channel*

## 5.2.2.1.2. Low Power Mode

| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit | Description |
|---|---|---|---|---|---|---|---|
| DSI-D0+/- | $T_{LPXM}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module | 50 | - | 75 | ns | Input |
| DSI-D0+/- | $T_{LPXD}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU | 50 | - | 75 | ns | Output |
| DSI-D0+/- | $T_{TA-SURED}$ | Time-out before the MPU start driving | $T_{LPXD}$ | - | $2xT_{LPXD}$ | ns | Output |
| DSI-D0+/- | $T_{TA-GETD}$ | Time to drive LP-00 by display module | $5xT_{LPXD}$ | - | - | ns | Input |
| DSI-D0+/- | $T_{TA-GOD}$ | Time to drive LP-00 after turnaround request - MPU | $4xT_{LPXD}$ | - | - | ns | Output |




*Bus Turnaround (BAT) from MPU to display module Timing*

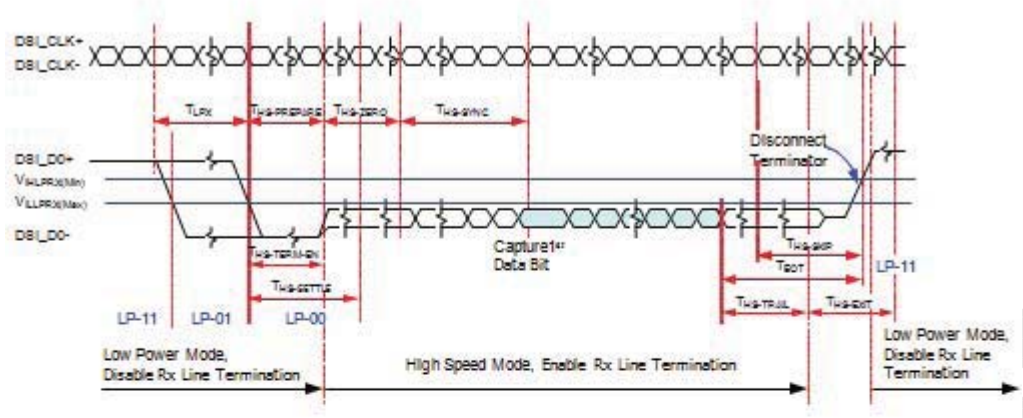



*Bus Turnaround (BAT) from display module to MPU Timing*

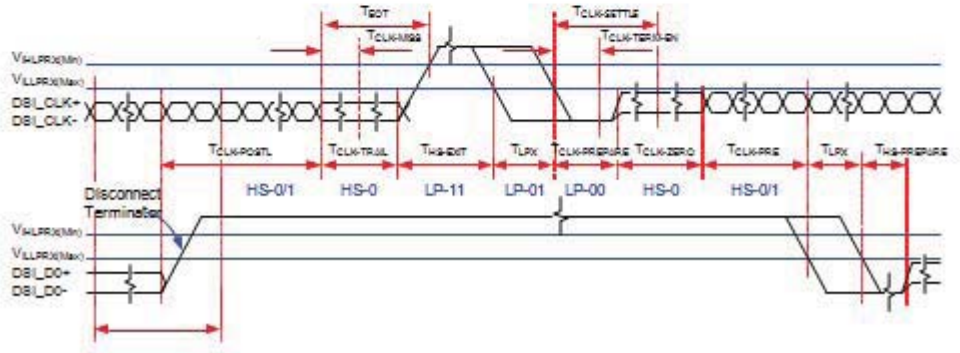
## 5.2.2.1.3. DSI Bursts

| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit | Description |
|---|---|---|---|---|---|---|---|
| Low Power Mode to High Speed Mode Timing | | | | | | | |
| DSI-Dn+/- | $T_{LPX}$ | Length of any low power state period | 50 | - | - | ns | Input |
| DSI-Dn+/- | $T_{HS-PREPARE}$ | Time to drive LP-00 to prepare for HS transmission | 40+4xUI | - | 85+6xUI | ns | Input |
| DSI-Dn+/- | $T_{HS-TERM-EN}$ | Time to enable data receiver line termination measured from when Dn crosses $V_{ILMAX}$ | - | - | 35+4xUI | ns | Input |
| High Speed Mode to Low Power Mode Timing | | | | | | | |
| DSI-Dn+/- | $T_{HS-SKIP}$ | Time-out at display module to ignore transition period of EoT | 40 | - | 55+4xUI | ns | Input |
| DSI-Dn+/- | $T_{HS-EXIT}$ | Time to drive LP-11 after HS burst | 100 | - | - | ns | Input |
| DSI-Dn+/- | $T_{HS-TRAIL}$ | Time to drive flipped differential state after last payload data bit of a HS transmission burst | 60+4xUI | - | - | ns | Input |
| High Speed Mode to/from Low Power Mode Timing | | | | | | | |
| DSI-CLK+/- | $T_{CLK-POS}$ | Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode | 60+52xUI | - | - | ns | Input |
| DSI-CLK+/- | $T_{CLK-TRAIL}$ | Time to drive HS differential state after last payload clock bit of a HS transmission burst | 60 | - | - | ns | Input |
| DSI-CLK+/- | $T_{HS-EXIT}$ | Time to drive LP-11 after HS burst | 100 | - | - | ns | Input |
| DSI-CLK+/- | $T_{CLK-PREPARE}$ | Time to drive LP-00 to prepare for HS transmission | 38 | - | 95 | ns | Input |
| DSI-CLK+/- | $T_{CLK-TERM-EN}$ | Time-out at clock lane display module to enable HS transmission | - | - | 38 | ns | Input |
| DSI-CLK+/- | $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | Minimum lead HS-0 drive period before starting clock | 300 | - | - | ns | Input |
| DSI-CLK+/- | $T_{CLK-PRE}$ | Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode | 8xUI | - | - | ns | Input |

*Note 1) Dn = D0, D1, D2 and D3.*
*Note 2) Two HS transmission can be sent with a break as short as $T_{HS-EXIT}$ from each other in continuous clock mode. In discontinuous mode, the break is longer which account $T_{CLK-POS}$, $T_{CLK-TRAIL}$ and $T_{HS-EXIT}$, before activity in clock and data lanes again.*

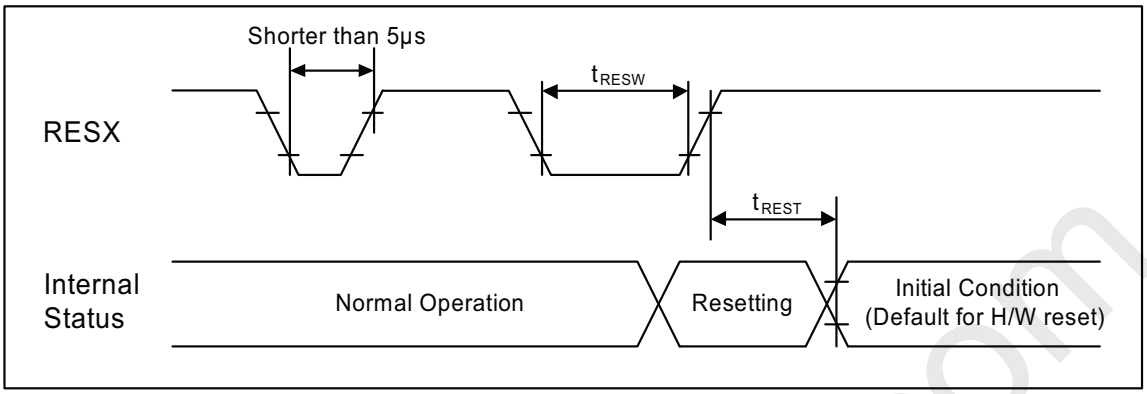



*Data lanes-Low Power Mode to/from High Speed Mode Timing*




*Clock lanes- High Speed Mode to/from Low Power Mode Timing*

## 5.2.2.2. Reset Input Timing

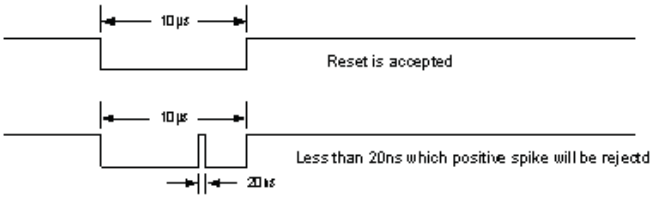



| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit | Description |
|---|---|---|---|---|---|---|---|
| RESX | $t_{RESW}$ | Reset "L" pulse width (Note 1) | 10 | - | - | µs | |
| | $t_{REST}$ | Reset complete time (Note 2) | - | - | 20 | ms | When reset applied during Sleep In Mode |
| | | | - | - | 120 | ms | When reset applied during Sleep Out Mode and Note 5 |

*Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.*

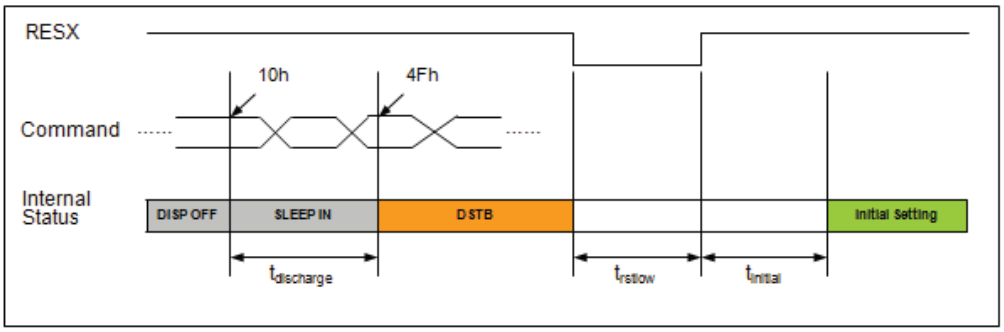
| *RESX Pulse* | *Action* |
|---|---|
| *Shorter than 5µs* | *Reset Rejected* |
| *Longer than 10µs* | *Reset* |
| *Between 5µs and 10µs* | *Reset Start* |

*Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.*
*Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time ($t_{REST}$) within 5ms after a rising edge of RESX.*
*Note 4) Spike Rejection also applies during a valid reset pulse as shown below:*




*Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.*

### 5.2.2.3. Deep Standby Mode Timing




(VDDI=1.7~3.3V, VSP=5.3~5.9V, VSN=-5.3~-5.9V, GND=0V, Ta=-30 to 70°C)

| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit | Description |
|---|---|---|---|---|---|---|---|
| RESX | $t_{discharge}$ | Sleep in into DSTB delay time | - | - | 100 | ms | |
| | $t_{rstlow}$ | Reset low pulse | 3 | - | - | ms | |
| | $t_{initial}$ | Reset high to initial setting delay time | - | - | 120 | ms | |

*Note 1) $t_{discharge}$ suggested delay time over 100ms.*
*Note 2) $t_{initial}$ suggested delay time over 120ms*

## 5.2.3. MIPI interface (Mobile Industry Processing Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode.

Note: The product only supports Video Mode operation.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display

module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or

other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems

that only operate in Video Mode may use a unidirectional data path.

### 5.2.3.1. MIPI Lane Configuration

| | MCU (Master) Display Module (Slave) |
|---|---|
| Clock Lane+/- | Unidirectional Lane<br>■ Clock Only<br>■ Escape Mode (ULPS Only) |
| Data Lane0+/- | Bi-directional Lane<br>■ Forward High-Speed<br>■ Bi-directional Escape Mode<br>■ Bi-directional LPDT |
| Data Lane1+/- | Unidirectional<br>■ Forward High speed |
| Data Lane2+/- | Unidirectional<br>■ Forward High speed |
| Data Lane3+/- | Unidirectional<br>■ Forward High speed |

The connection between host device and display module is as reference.

**Note: Usually, we suggest host can use non-continuous clock mode & burst mode to transmit the video stream to enhance ESD ability.**

# 6 Electrical Specifications

## 6.1 DC Characteristics Requirements

| Item | Symbol | Values | | | Unit | Remark |
|---|---|---|---|---|---|---|
| | | Min | Typ | max | | |
| I/O Supply Voltage | IOVCC | 1.7 | 1.8 | 1.9 | V | |
| Liquid crystal drive supply voltage | VSP | 5.6 | 5.8 | 6 | V | |
| Liquid crystal drive supply voltage | VSN | -6 | -5.8 | -5.6 | V | |
| Input High Voltage | $V_{IH}$ | 0.7x IOVCC | - | IOVCC | mV | MIPI HS |
| Input Low Voltage | $V_{IL}$ | 0 | - | 0.3x IOVCC | mV | MIPI HS |
| Output High Voltage | $V_{OH}$ | 0.8x IOVCC | - | IOVCC | V | MIPI LP |
| Output Low Voltage | $V_{OL}$ | 0 | - | 0.2x IOVCC | mV | MIPI LP |
| Frame Frequency | $f_{FRAME}$ | 55 | 60 | - | HZ | Video mode |
| Power Consumption | | - | - | 580 | mW | Note(1) |

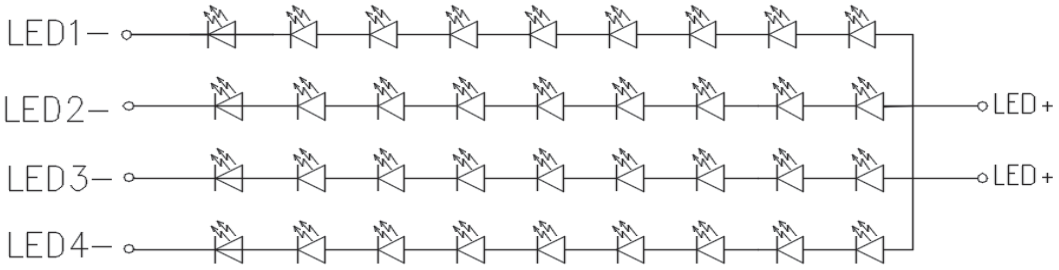
**Note (1) The specified power supply current is under the conditions at IOVCC =1.8 V, VSP=5.8V,VSN=-5.8V Ta = 25± 2˚ C, DC current and fv = 60 Hz, whereas a *white pattern* under 1600x2560 60Hz is displayed.**

## 6.2 Power Consumption of Backlight

Test Condition : $I_{LED}$=24mA LED 36PCS（4*9pcs）

Warning: LCM Brightness must match Optical Spec requirement when $I_{LED}$=24mA

Backlight Unit Schematic:




| Item | Symbol | Value | | | Unit | Remark |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Forward Voltage | $V_{BL}$ | 25.2 | 26.1 | 27.504 | V | Note 6 |
| Power Consumption | $P_{BL}$ | 2419.2 | 2505.6 | 2640 | mW | |
| LED Quantity | | 36 | | | pcs | |
| LED Rank | | Luminous Flux: | | | lm | LED requires Global patent |
| | | Chromaticity: | | | | |

Note 6 : When $I_{LED}$=24mA，the $V_{BL}$ must be in the range of above table specified.

The resistance between LED+ /LED- and LED soldering pad (including soldering resistance) must be less than 0.15ohm

The resistor between VLED+ and GND should be large than 1Mohm.

$P_{BL}$= $I_{LED}$x $V_{BL}$

# 7 Optical Specifications

**Test condition：IOVCC=1.8V VSP=+5.6V VSN=-5.6V ,Ta=25℃**

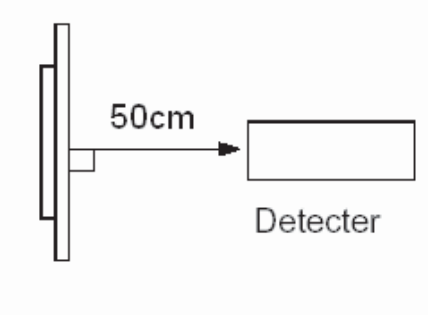
| Item | | Symbol | Condition | INX Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| luminance | | Bp | θ=0 Φ=0° | 320 | 400 | | cd/m$^2$ | Note 7 |
| Uniformity（24mA） | | △Bp | | 75 | 80 | | % | Note 8 |
| Viewing Angle | Left | $\theta_L$ | Cr≥10 | 75 | 80 | | deg | Note 9 |
| | Right | $\theta_R$ | | 75 | 80 | | | |
| | Top | $\psi_T$ | | 75 | 80 | | | |
| | Bottom | $\psi_B$ | | 75 | 80 | | | |
| Contrast Ratio | | Cr | θ=0°Φ=0° | 1200 | 1500 | | - | Note 10 |
| Response Time | | T | | | 25 | 30 | ms | Note 11 |
| Color Coordinate of CIE1931* | Red | x | θ=0°Φ=0° | 0.638 | 0.668 | 0.698 | | Note 12 |
| | | y | | 0.283 | 0.313 | 0.343 | | |
| | Green | x | | 0.247 | 0.277 | 0.307 | | |
| | | y | | 0.613 | 0.643 | 0.673 | | |
| | Blue | x | | 0.119 | 0.149 | 0.179 | | |
| | | y | | 0.031 | 0.061 | 0.091 | | |
| | White | x | | 0.265 | 0.295 | 0.325 | | |
| | | y | | 0.290 | 0.320 | 0.350 | | |
| NTSC Ratio | | NTSC | CIE1931 | 80 | 85 | - | % | Note 13 |
| Flicker | | amou | - | | | -30 | dB | Note 14 |
| Gamma | | - | - | 1.9 | 2.2 | 2.5 | | |

**Note 7: Luminance measurement**

- The test condition is at $I_{LED}$=24mA and measured on the surface of LCD module at 25℃.
- The data are measured after LEDs are lighted on for more than 5 minutes and LCM displays are fully white. The brightness is the average value of 13 measured spots. Measurement equipment CS2000 or similar equipments (Field of view:1deg,Distance:50cm)
- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.
- Measured value at the center point of LCD panel must be after more than 5 minutes while

backlight turning on.

- This is target spec, The provider must do the best to achieve the target.
- If the providers can't reach the target, the base line is the brightness of the center point must meet the brightness Requirement.



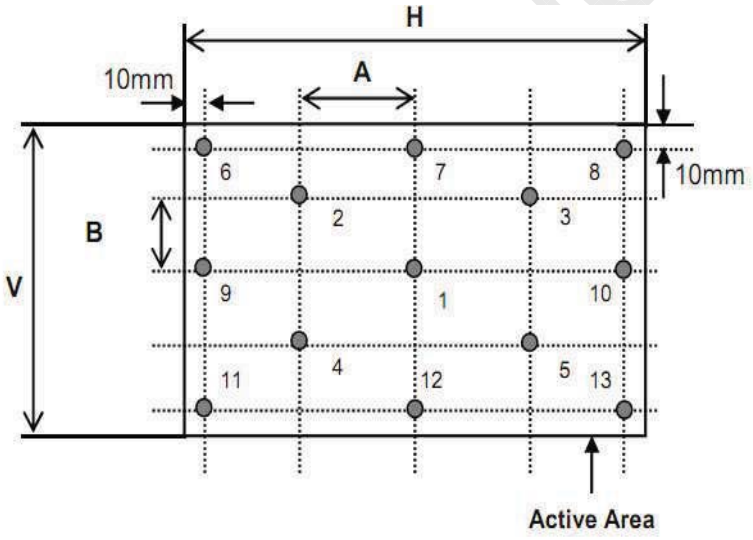

**Note 8: Uniformity**

- The test condition is at $I_{LED}$=24mA and measured on the surface of LCD module at 25℃.
- Measurement equipment: CS2000 or similar equipments.
- The luminance uniformity is calculated by using following formula:

△Bp = Bp (Min.) / Bp (Max.)×100 (%)

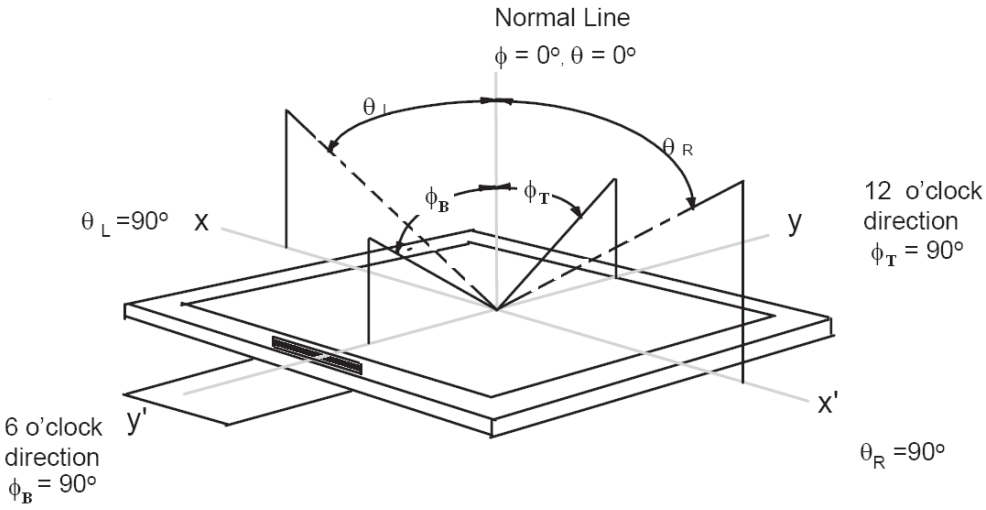
Bp (Max.) = Maximum brightness in 13 measured spots.

Bp (Min.) = Minimum brightness in 13 measured spots.




**Note 9: The definition of Viewing Angle**

Refer to the graph below marked by θ and Φ



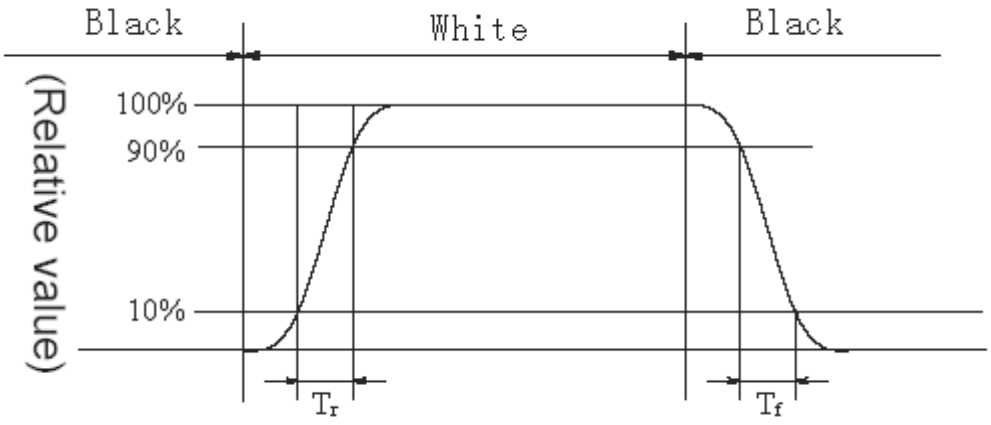

**Note 10: The definition of Contrast Ratio** (Test LCM using CA310 /CS2000 or similar equipments)

$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance When LCD is at "White" state}}{\text{Luminance When LCD is at "Black" state}}$$

(Contrast Ratio is measured in optimum common electrode voltage)

**Note 11: Definition of Response time.** (Test LCD using DMS501 or similar equipments)

The output signals of photo detector are measured when the input signals are changed from "black" to "white"(Voltage falling time) and from "white" to "black"(Voltage rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.




**Note 12: Color Coordinates of CIE 1931**

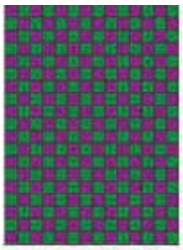
- The test condition is at $I_{LED}$=24mA and measured on the surface of LCD module at 25℃.
- Measurement equipment: CA210/CA310/CS2000 or similar equipments.
- The Color Coordinate (CIE 1931) measure the center of active area of the module.

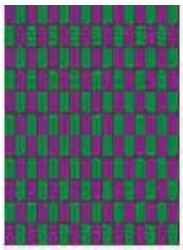
**Note 13: Definition of Color of CIE Coordinate and NTSC Ratio.**

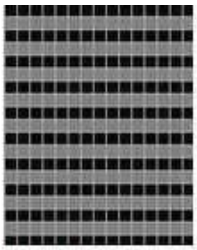
$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

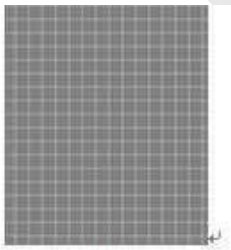
**Note 14: Flicker**

- Measurement equipment :CA-210 or similar equipments
- Measuring temperature: Ta=25℃.
- Test method: JEITA method
- Test pattern : Refer to below


1 Dot Inversion


2 Dot inversion


Line Inversion


Frame Inversion


1 Column Inversion

The point should be marked is, for line and frame inversion, the background of Flicker Test Pattern-"gray " are defined as middle gray scale .For example, RGB 24bit "gray" defined as below:

| R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

For Dot inversion, the RGB data for first pixel is (127, 0, 127), the RGB data for the second pixel is (0, 127, 0).

- Frame Frequency Requirement before test： The LCD must be tuned to more than 65HZ before measurement .
- Measurement Point: the center of display active area
- Conversion of Flicker ratio:

  Flicker[dB] = 10xlog[Px/P0]

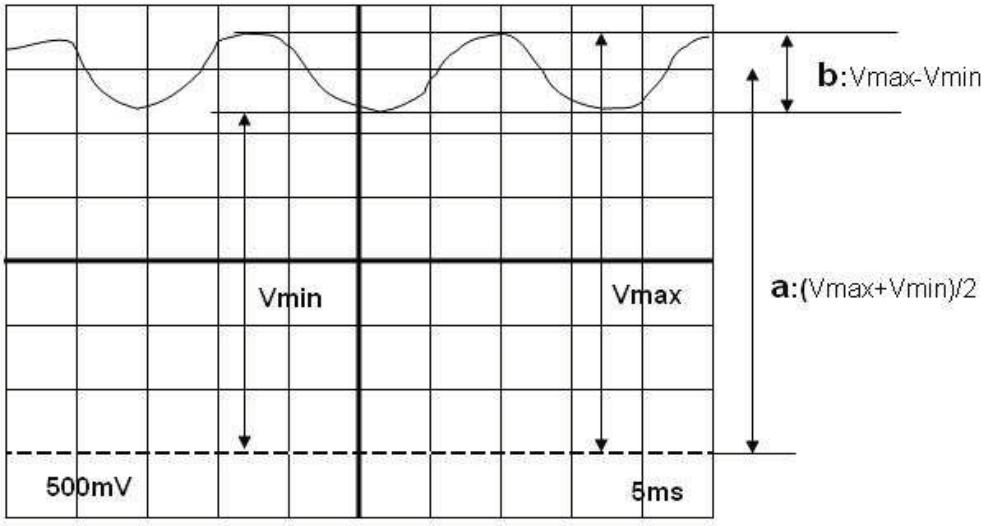
  Where

  Px: Maximum power spectrum of AC component after passing through integrator

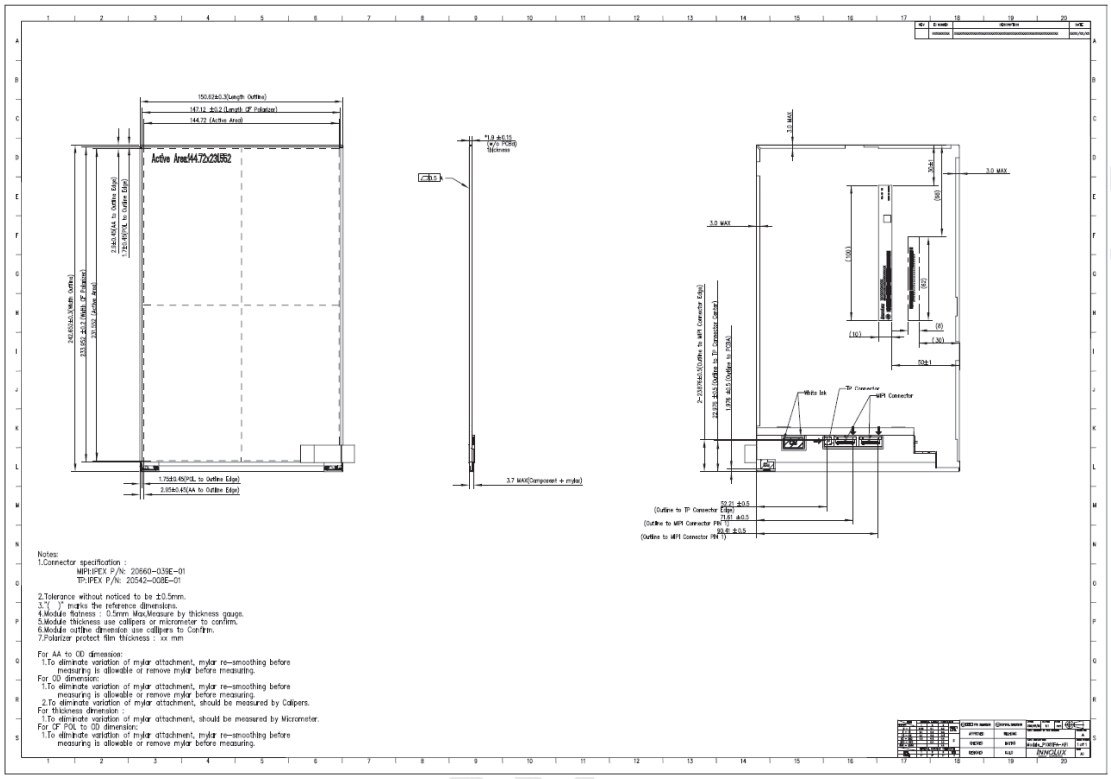
  P0:Power spectrum of DC component after passing through integrator

  AC component=b (Refer to below diagram )

  DC component=a (Refer to below diagram)



# 8 Mechanical Drawing




module_for_spec_p1
08sfa-af1_VerA_1907

# 9 Reliability Requirement

| Test item | Test condition | No. of failures /No. of examinations |
|---|---|---|
| High Temperature Storage Test | 60ºC, 240 hours | 0/3 |
| Low Temperature Storage Test | -20ºC, 240 hours | 0/3 |
| Thermal Shock Storage Test | -20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle | 0/3 |
| High Temperature Operation Test | 60ºC, 240 hours | 0/3 |
| Low Temperature Operation Test | -10ºC, 240 hours | 0/3 |
| High Temperature & High Humidity Storage Test | 50ºC, RH 90%, 240hours | 0/3 |

Note (1) criteria : Normal display image with no mura and extra line defect.

(should be checked with 6% ND filter and within 45° viewing angle from vertical)

Note (2) Evaluation should be tested after storage at room temperature for more than two hour