




# Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications

( v ) Final Specifications

Module	17.3"(17.25") FHD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B173HTN01.0 (H/W:0A)
Note (  )	<b>LED Backlight with driving circuit design</b>

Customer	Date
Checked & Approved by	Date
Note: This Specification is subject to change without notice.	

Approved by	Date
<u>Wen Hwa</u>	<u>3/3/2015</u>
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# Product Specification

AU OPTRONICS CORPORATION

## Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2013/10/23	All	First Edition for Customer		
0.2 2014/2/17		Update Label & EDID		

## 1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



## 2. General Description

B173HTN01.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the FHD 16:9 1920(H) x 1080(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B173HTN01.0 is designed for a display unit of notebook style personal computer and industrial machine.

### 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

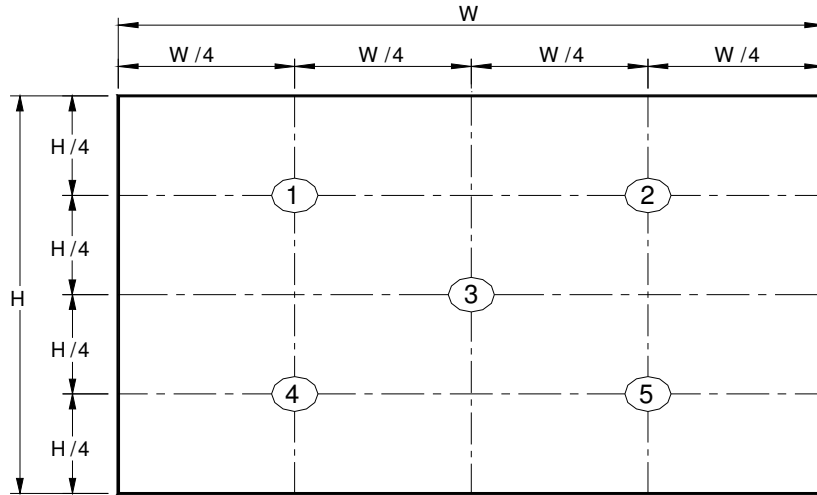
Items	Unit	Specifications			
Screen Diagonal	[mm]	17.3W"(17.25)			
Active Area	[mm]	381.888 X 214.812			
Pixels H x V		1920x3(RGB) x1080			
Pixel Pitch	[mm]	0.1989X0.1989			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (ILED=26mA) (Note: ILED is LED current)	[cd/m <sup>2</sup> ]	300 typ. (5 points average) 255 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		600 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	9.0 max. (Include Logic and Blu power)			
Weight	[Grams]	590 max.			
Physical Size Include bracket	[mm]		Min.	Typ.	Max.
		Length	397.6	398.1	398.6
		Width	232.3	232.8	233.3
		Thickness	---	---	6.0
Electrical Interface		eDP 1.2			
Glass Thickness	[mm]	0.5			
Surface Treatment		Glare,Hardness 3H, Reflection 4.3%			
Support Color		262K colors ( RGB 6-bit )			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

## 2.2 Optical Characteristics

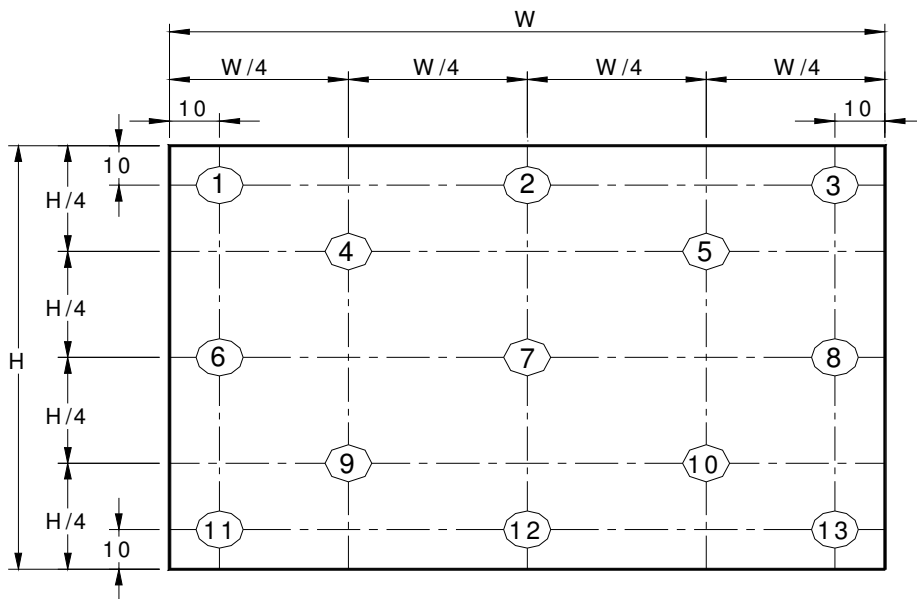
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note				
White Luminance ILED=26mA			5 points average	255	300	---	cd/m <sup>2</sup>	1, 4, 5.				
Viewing Angle		$\theta_R$ $\theta_L$	Horizontal (Right) CR = 10 (Left)	60	70	---	degree	4, 9				
				60	70	---						
		$\psi_H$ $\psi_L$	Vertical (Upper) CR = 10 (Lower)	50	60	---						
				50	60	---						
Luminance Uniformity		$\delta_{5P}$	5 Points	---	---	1.25		1, 3, 4				
Luminance Uniformity		$\delta_{13P}$	13 Points	---	---	1.60		2, 3, 4				
Contrast Ratio		CR		300	400	---		4, 6				
Cross talk		%		---	---	4		4, 7				
Response Time		T <sub>RT</sub>	Rising + Falling	---	8	16	msec	4, 8				
Color / Chromaticity Coordinates	Red	R <sub>x</sub>	CIE 1931	0.611	0.641	0.671	---	4				
		R <sub>y</sub>		0.315	0.345	0.375						
	Green	G <sub>x</sub>		0.294	0.324	0.354						
		G <sub>y</sub>		0.591	0.621	0.651						
	Blue	B <sub>x</sub>		0.121	0.151	0.181						
		B <sub>y</sub>		0.027	0.057	0.087						
	White	W <sub>x</sub>		0.283	0.312	0.342						
		W <sub>y</sub>		0.299	0.329	0.359						
	NTSC			%		---			72	---		

**Note 1:** 5 points position (Ref: Active area)



**Note 2:** 13 points position (Ref: Active area)



**Note 3:** The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

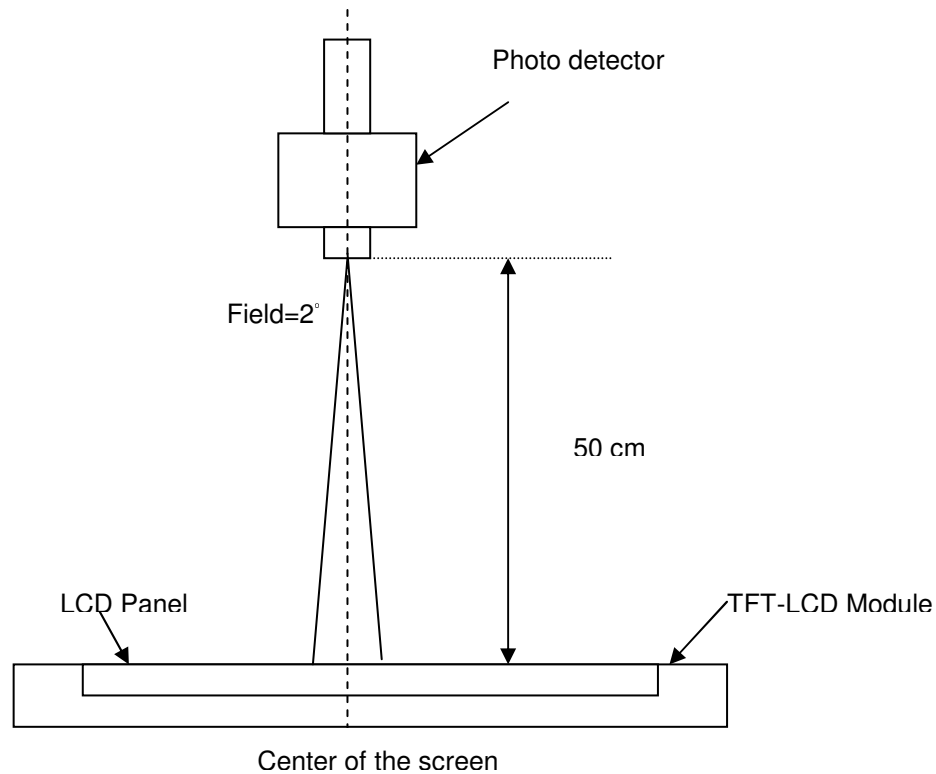
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

**Note 4:** Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for

for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



**Note 5 :** Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 63 at 5 points ,  $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$  is corresponding to the luminance of the point X at Figure in Note (1).

**Note 6 :** Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

**Note 7 :** Definition of Cross Talk (CT)

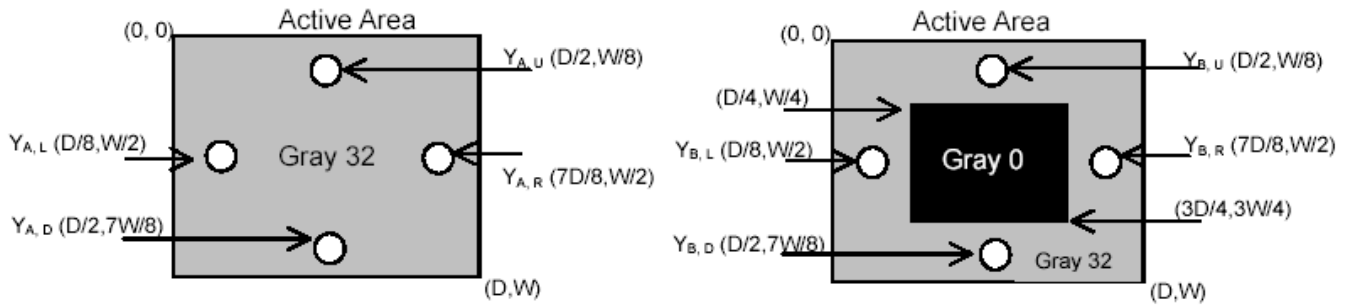
$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

$Y_A$  = Luminance of measured location without gray level 0 pattern ( $\text{cd/m}^2$ )

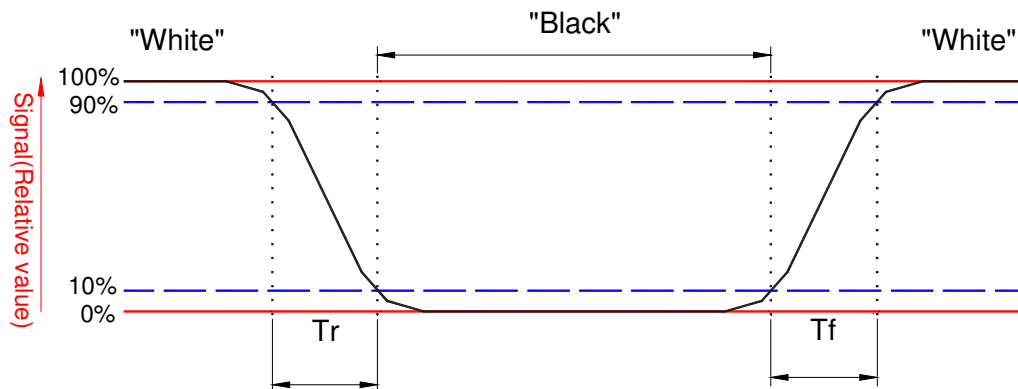
$Y_B$  = Luminance of measured location with gray level 0 pattern ( $\text{cd/m}^2$ )





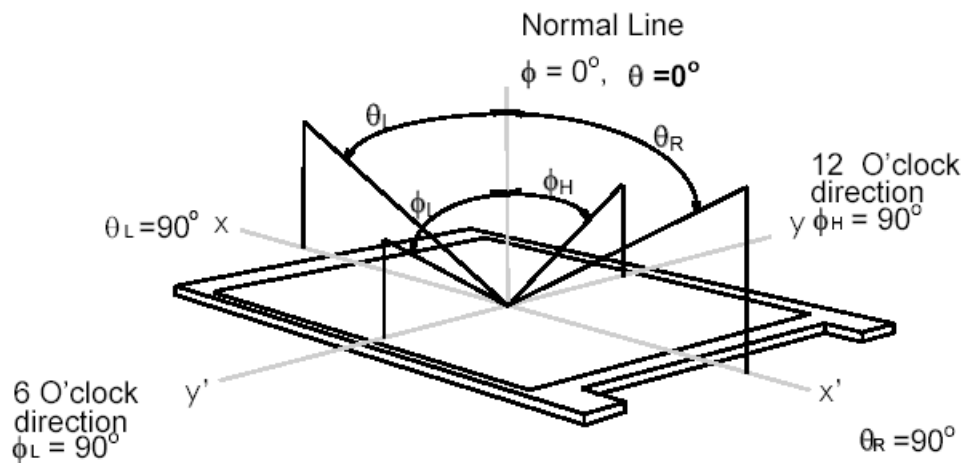
**Note 8:** Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



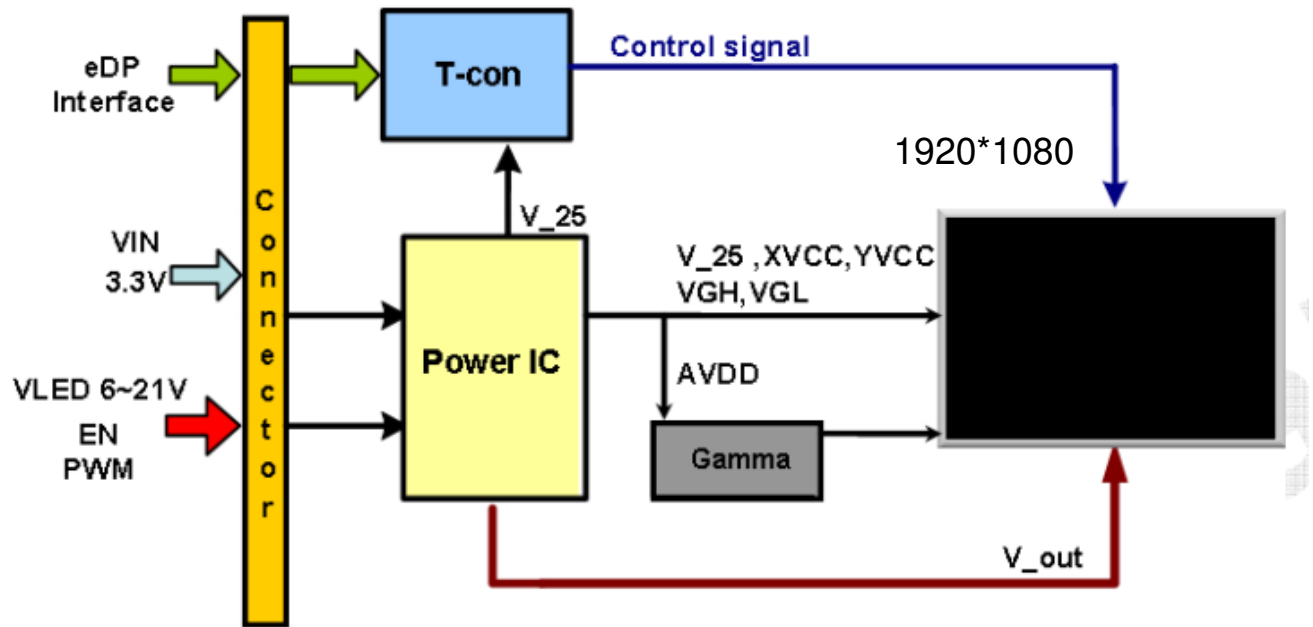
## Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a  $180^\circ$  horizontal and  $180^\circ$  vertical range (off-normal viewing angles). The  $180^\circ$  viewing angle range is broken down as follows;  $90^\circ$  ( $\theta$ ) horizontal left and right and  $90^\circ$  ( $\phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



## 3. Functional Block Diagram

The following diagram shows the functional block of the 17.3 inches wide Color TFT/LCD 30 Pin two channel Module



## 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

### 4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

### 4.2 Absolute Ratings of Environment

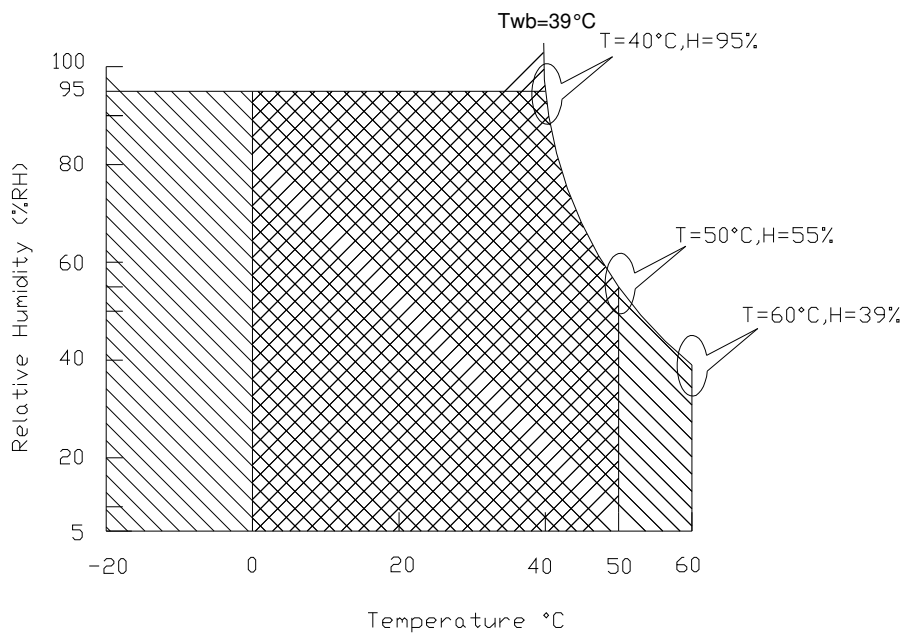
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C )

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

## 5. Electrical Characteristics

### 5.1 TFT LCD Module

#### 5.1.1 Power Specification

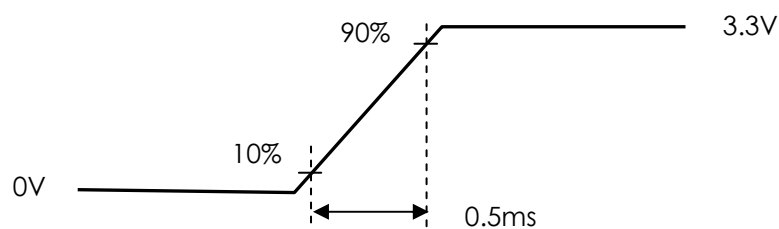
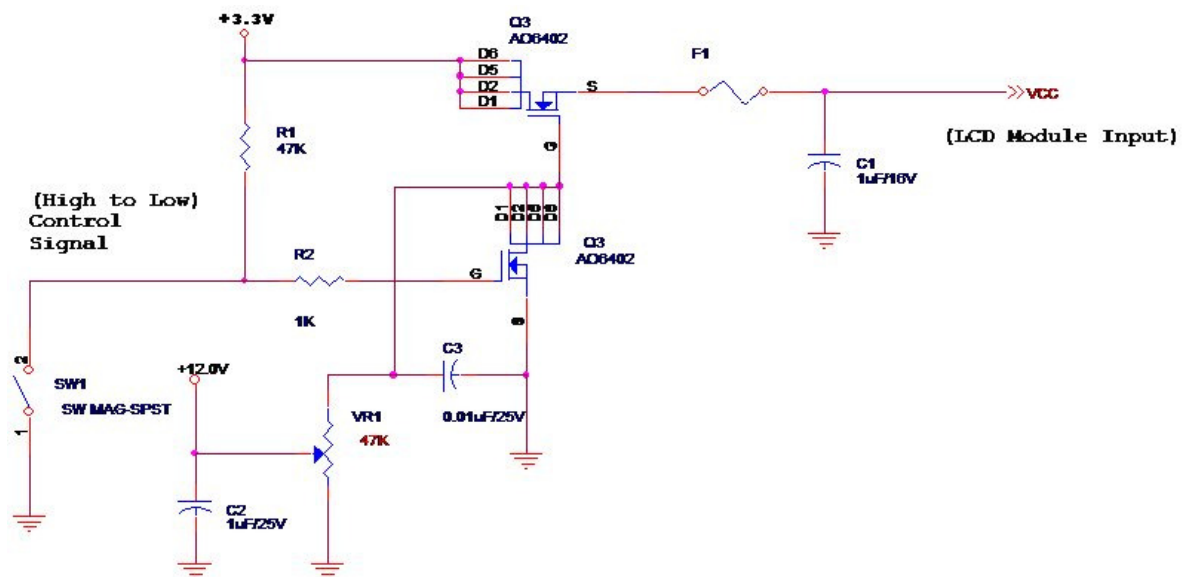
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	2	[Watt]	Note 1
IDD	IDD Current	-	350	606	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ( $P_{max}=V_{3.3} \times I_{black}$ )

Note 2 : Measure Condition



Vin rising time

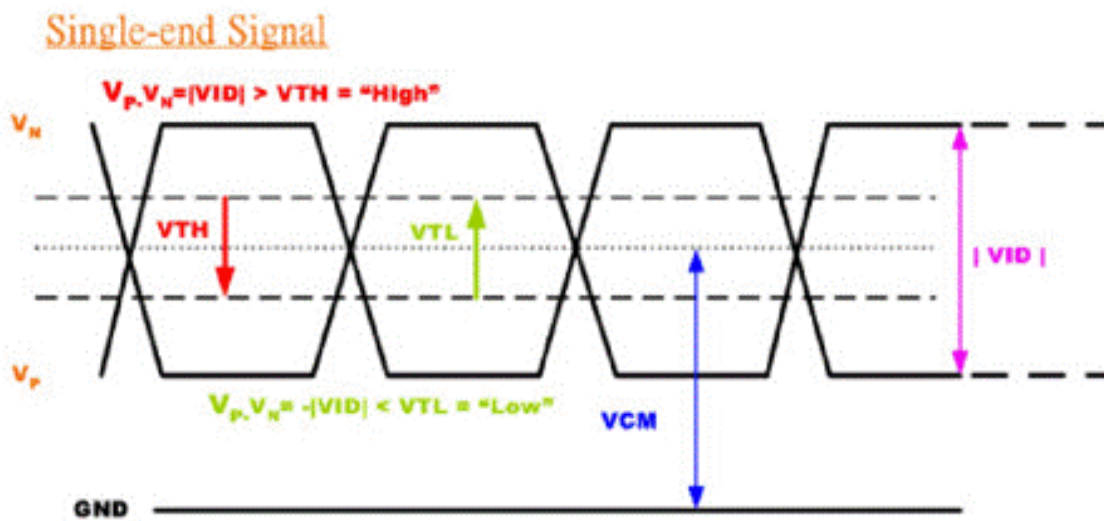
## 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
$V_{th}$	Differential Input High Threshold ( $V_{cm}=+1.2V$ )	---	100	[mV]
$V_{tl}$	Differential Input Low Threshold ( $V_{cm}=+1.2V$ )	-100	---	[mV]
$V_{ID}$	Differential Input Voltage	100	600	[mV]
$V_{cm}$	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: eDP Signal Waveform



## 5.2 Backlight Unit

### 5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	7	[Watt]	(Ta=25°C), Note 1. Vin=12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 IF=20 Ma

**Note 1:** Calculator value for reference  $P_{LED} = V_F$  (Normal Distribution) \*  $I_F$  (Normal Distribution) / Efficiency

**Note 2:** The LED life-time define as the estimated time to 50% degradation of initial luminous.

### 5.2.2 Backlight input signal characteristics

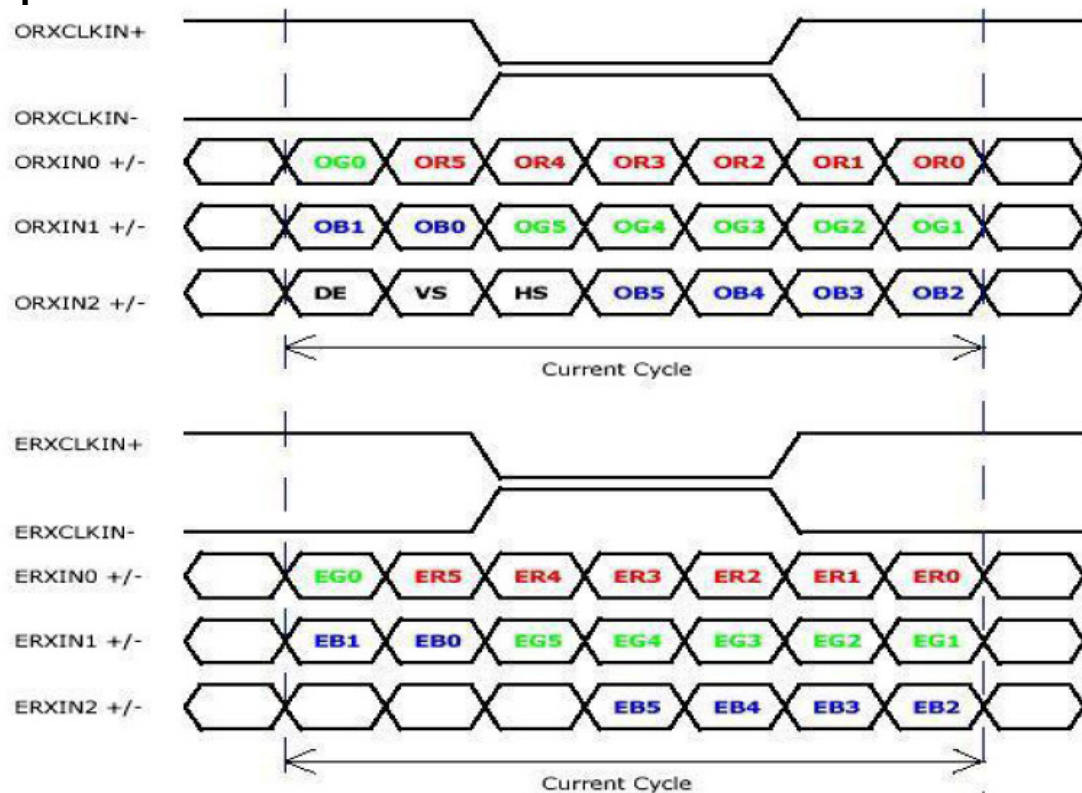
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

**Note 1 :** Recommend system pull up/down resistor no bigger than 10kohm





## 6.2 The Input Data Format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN.
HS	Horizontal Sync	The signal is synchronized to RxCLKIN.

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

## 6.3 Integration Interface Requirement

### 6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	I-PEX or Compatible
Type / Part Number	I-PEX 20455-030-E12 or Compatible
Mating Housing/Part Number	I-PEX 20455-030-E12 or Compatible

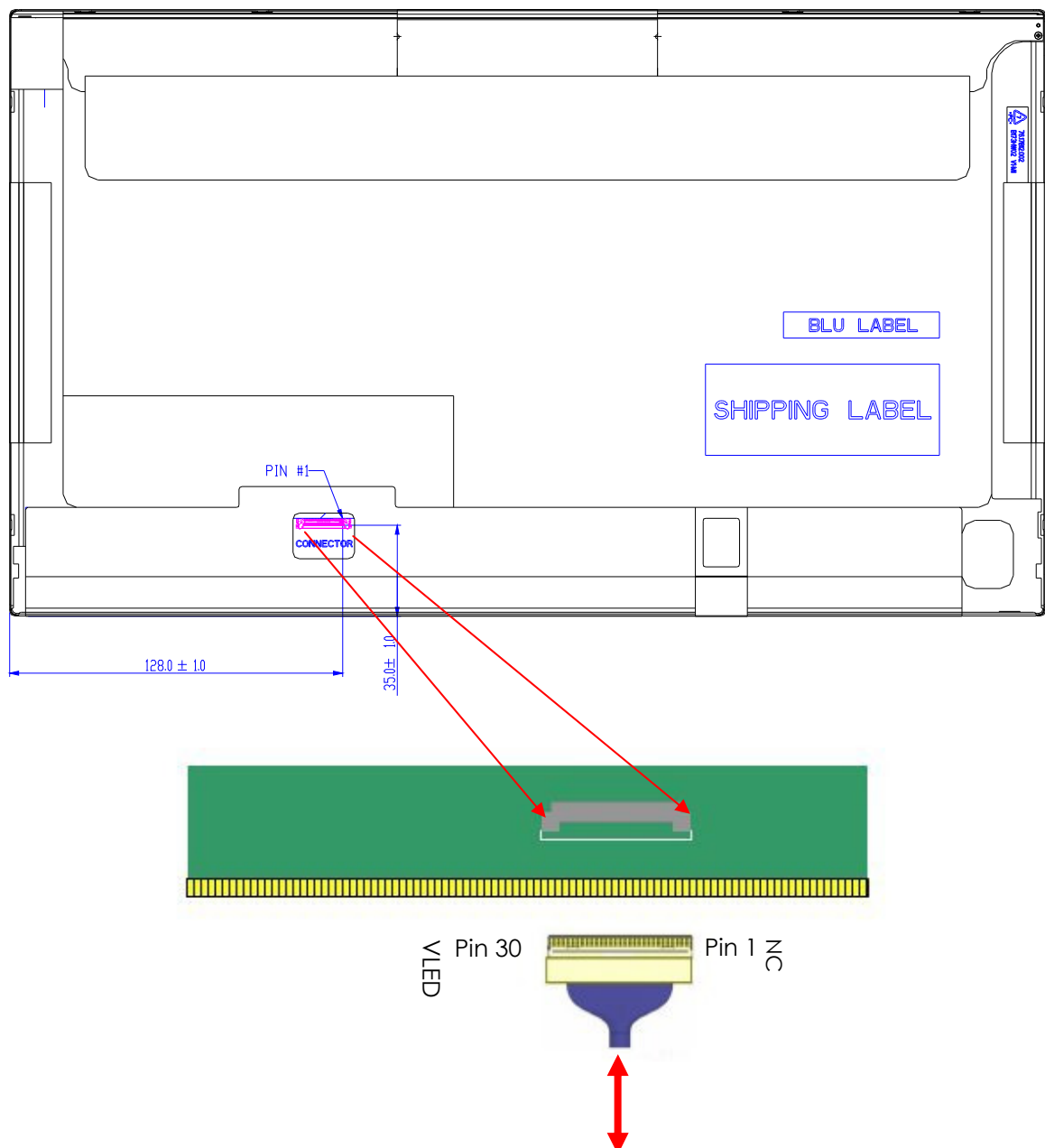
### 6.3.2 Pin Assignment

eDP S is a differential signal technology for LCD interface and high speed data transfer device.

item	Symbol	Function
1	NC	No Connect
2	H_GND	High Speed Ground
3	Lane1_N	Comp Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	NC	Reverse for AUO TEST only
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off

23	BL PWM DIM	System PWM signal Input
24	NC	Reverse for AUO TEST only
25	NC	Reverse for AUO TEST only
26	BL_PWR	Backlight power (6V~21V)
27	BL_PWR	Backlight power (6V~21V)
28	BL_PWR	Backlight power (6V~21V)
29	BL_PWR	Backlight power (6V~21V)
30	NC	No Connect

Note1: Input signals shall be low or High-impedance state when VDD is off.



Note1: Input signals shall be low or High-impedance state when VDD is off.

## 6.4 Interface Timing

### 6.4.1 Timing Characteristics

Basically, interface timings should match the 1920X1080 / 60Hz manufacturing guide line timing.

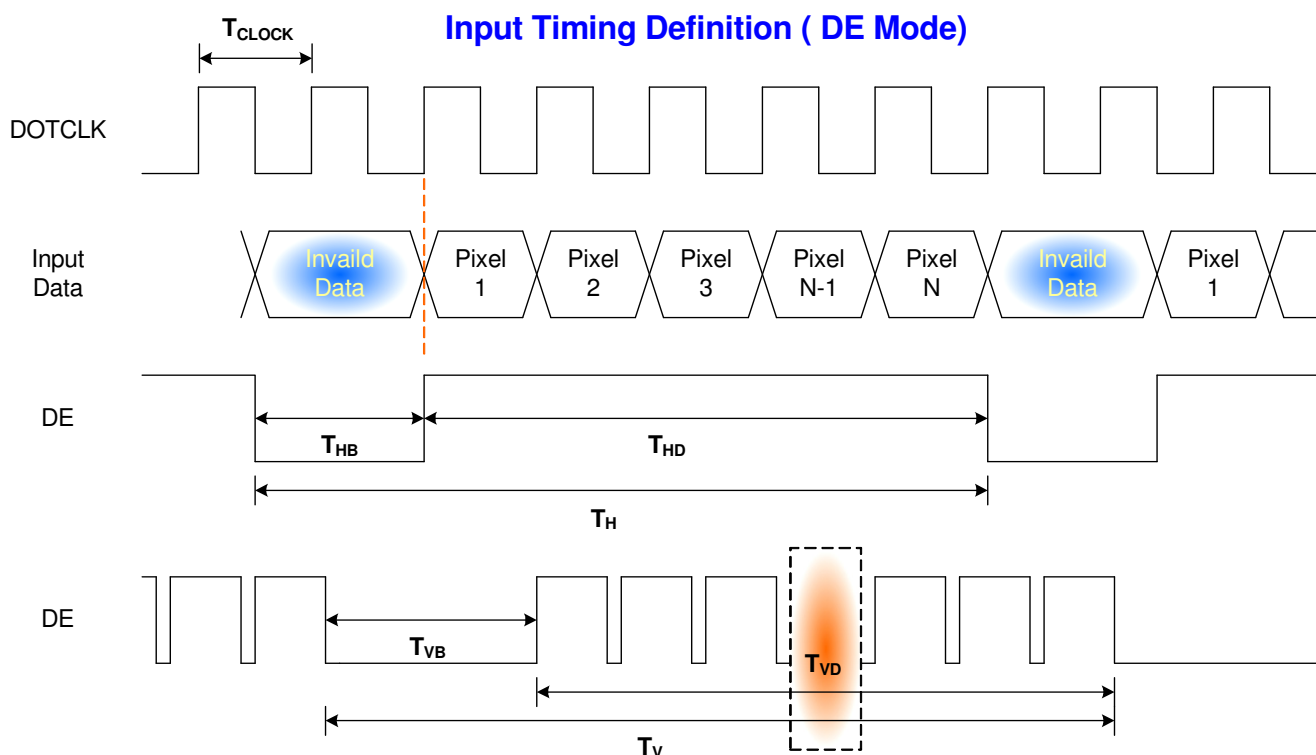
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-		60	-	Hz
Clock frequency		1/ T <sub>Clock</sub>	66.6	70	80	MHz
Vertical Section	Period	T <sub>V</sub>	1100	1088	1080+A	T <sub>Line</sub>
	Active	T <sub>VD</sub>	1080			
	Blanking	T <sub>VB</sub>	20	30	A	
Horizontal Section	Period	T <sub>H</sub>	1010	1072	960+B	T <sub>Clock</sub>
	Active	T <sub>HD</sub>	960			
	Blanking	T <sub>HB</sub>	50	112	B	

**Note 1 :** The above is as optimized setting

**Note 2 :** DE mode only

**Note 3 :** The maximum clock frequency =  $(960+B) \times (1080+A) \times 60 < 330\text{MHz}$

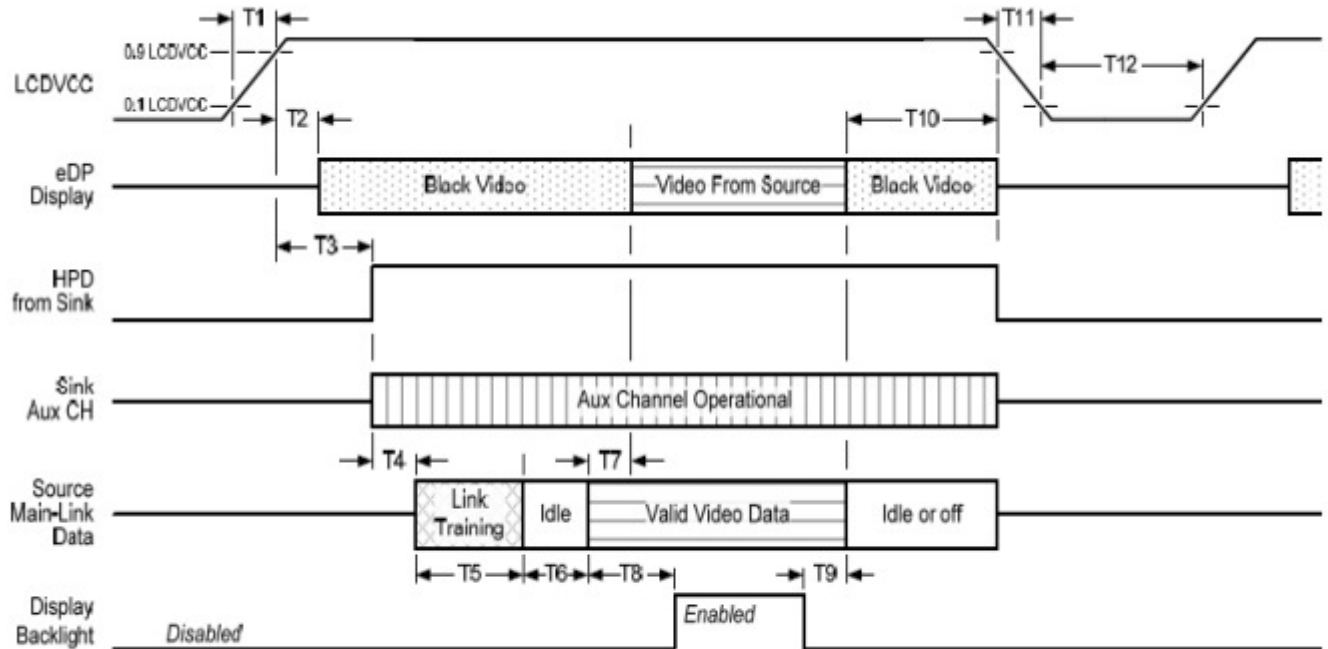
### 6.4.2 Timing diagram



## 6.5 Power ON/OFF Sequence

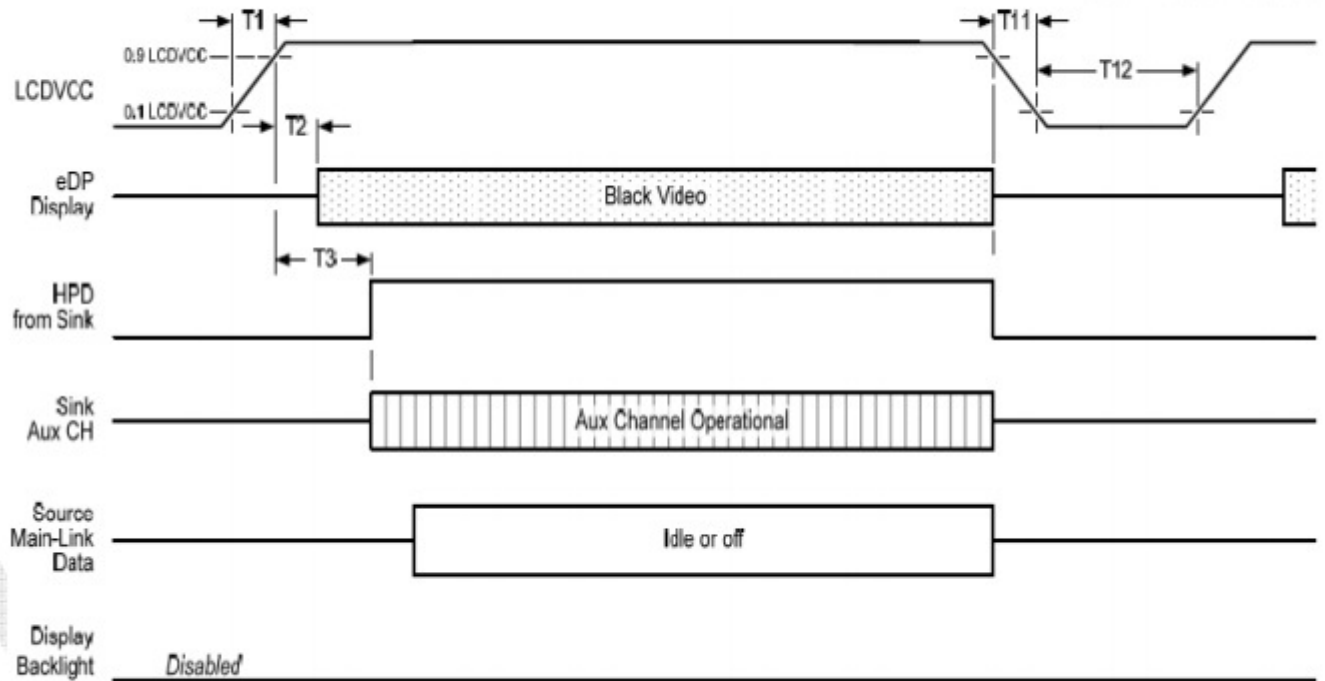
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

### Display Port panel power sequence:



### Display port interface power up/down sequence, normal system operation

## Display Port AUX\_CH transaction only:



Display port interface power up/down sequence, AUX\_CH transaction only



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Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	150ms			



## 7. Panel Reliability Test

### 7.1 Vibration Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

### 7.2 Shock Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

### 7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃ , 90%RH, 300h	
High Temperature Operation	Ta= 50℃ , Dry, 300h	
Low Temperature Operation	Ta= 0℃ , 300h	
High Temperature Storage	Ta= 60℃ , 35%RH, 300h	
Low Temperature Storage	Ta= -20℃ , 50%RH, 250h	
Thermal Shock Test	Ta=-20℃ to 60℃ , Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

**Note1:** According to EN 61000-4-2 , ESD class B: Some performance degradation allowed.  
Self-recoverable.

No data lost, No hardware failures.

**Remark:** MTBF (Excluding the LED): 30,000 hours with a confidence level 90%



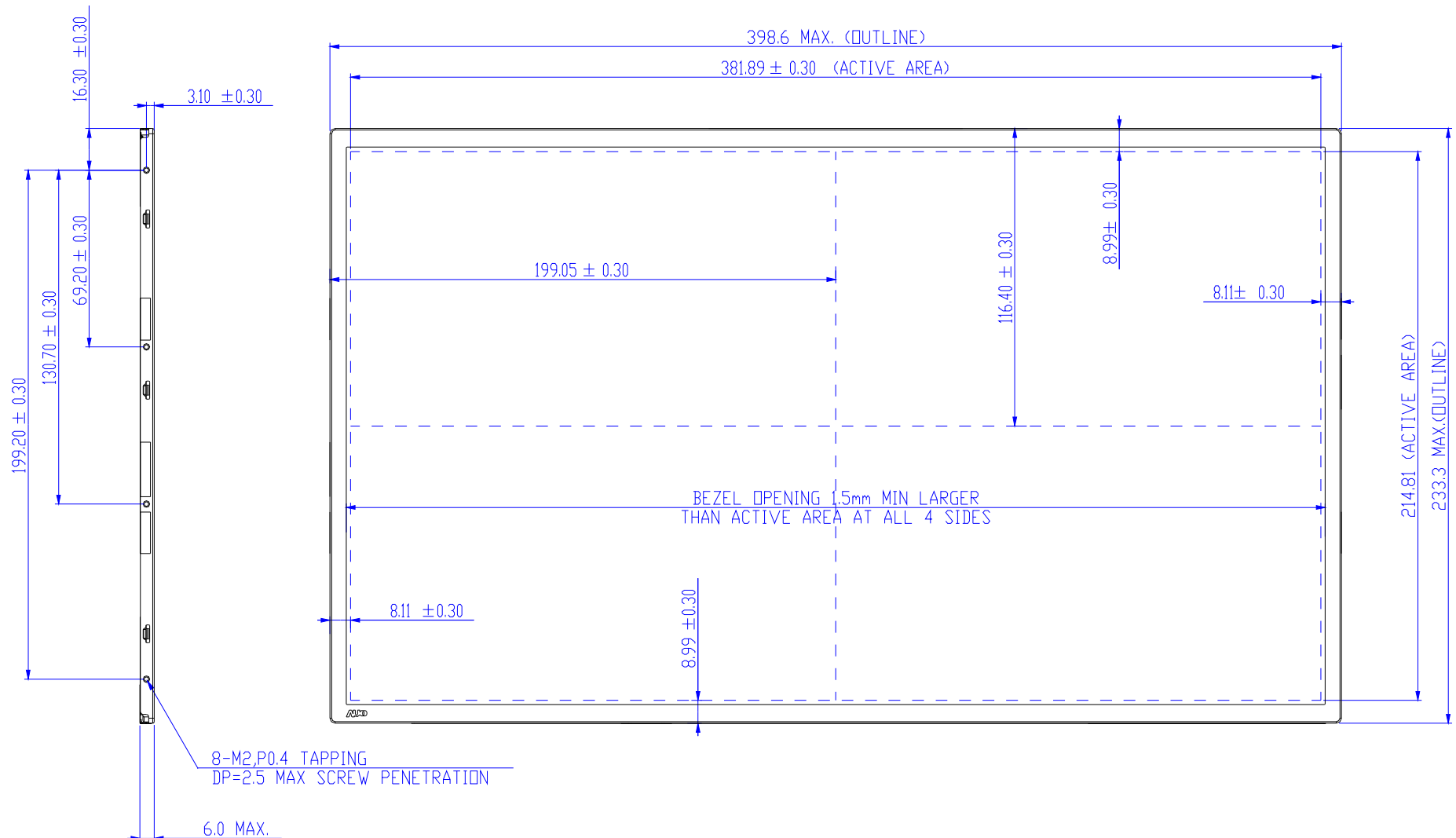


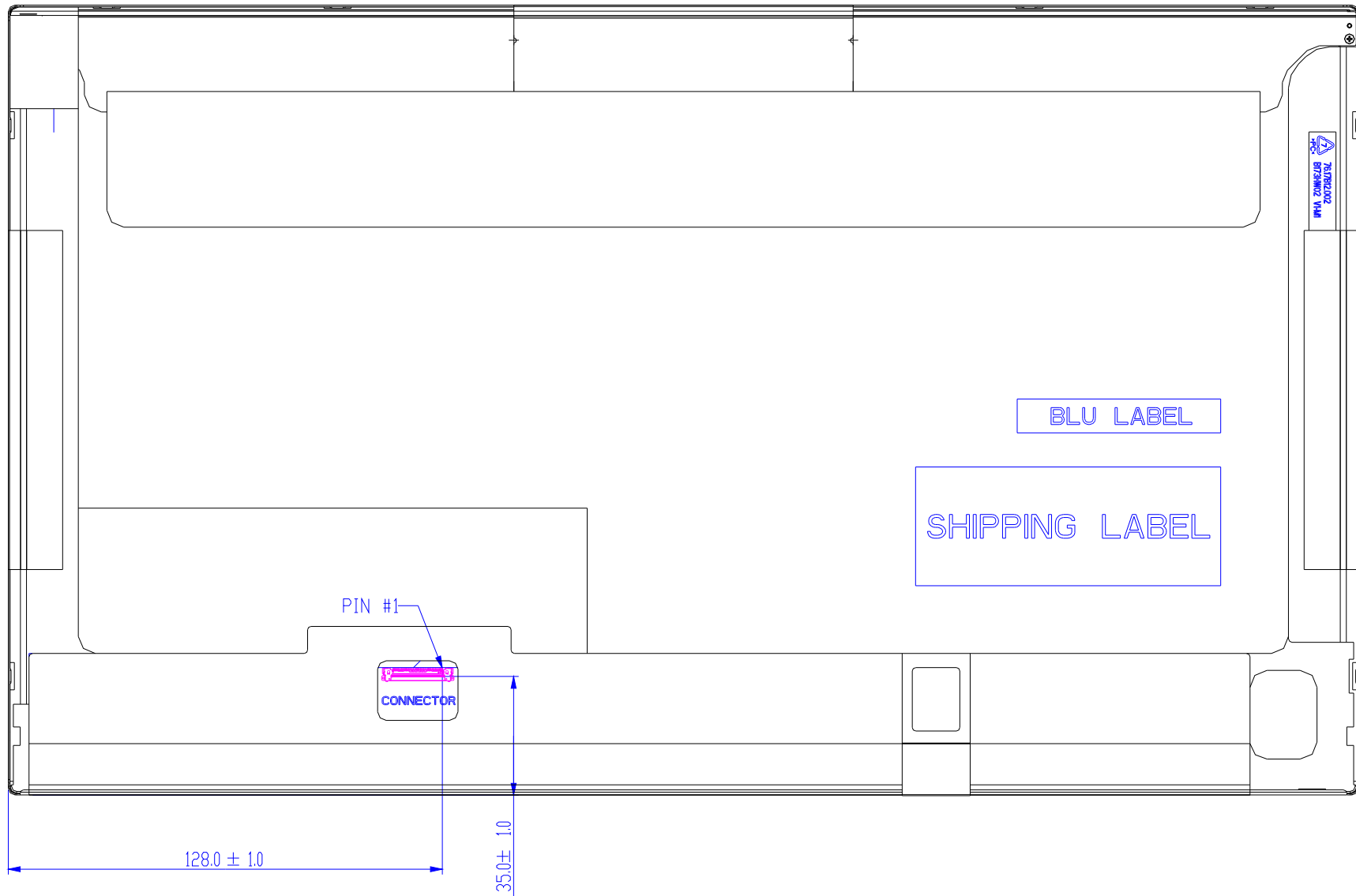
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## 8. Mechanical Characteristics

### 8.1 LCM Outline Dimension





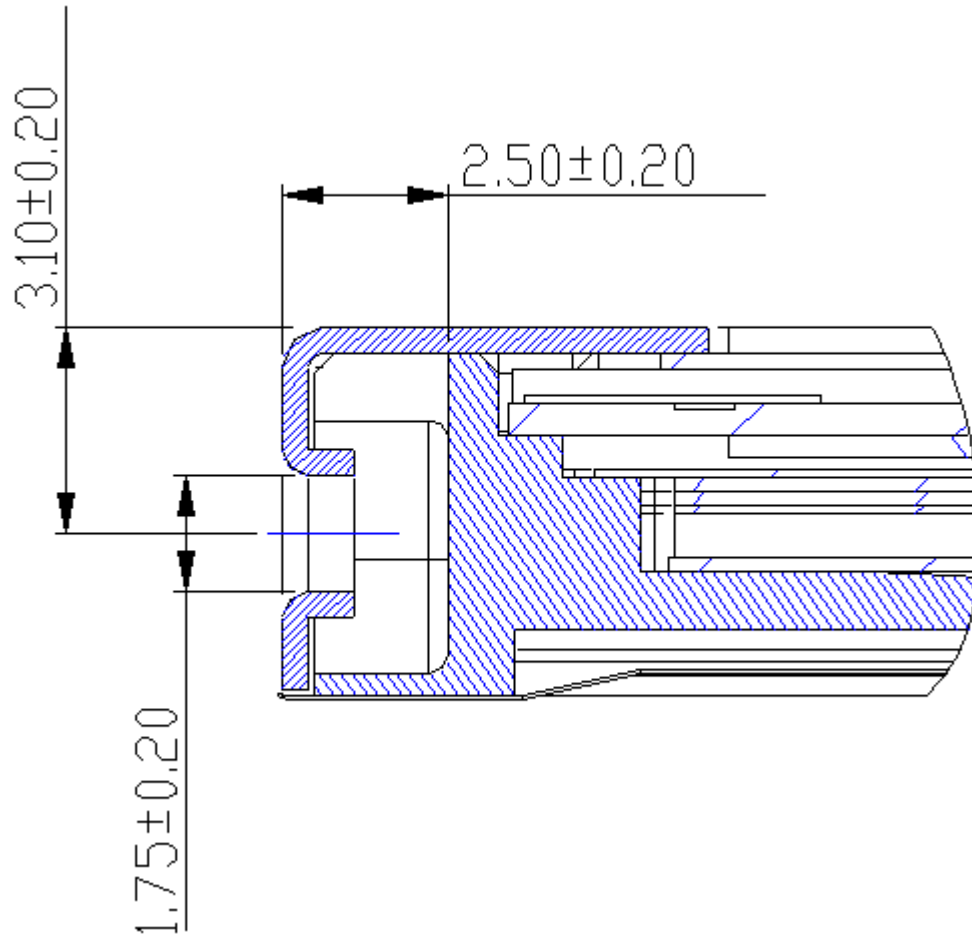
Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

## 8.2 Screw Hole Depth and Center Position

Maximum Screw penetration from side surface is 2.3 mm

The center of screw hole center location is  $3.1 \pm 0.2\text{mm}$  from front surface

Screw Torque: Maximum 2.5 kgf-cm





## 9. Shipping and Package

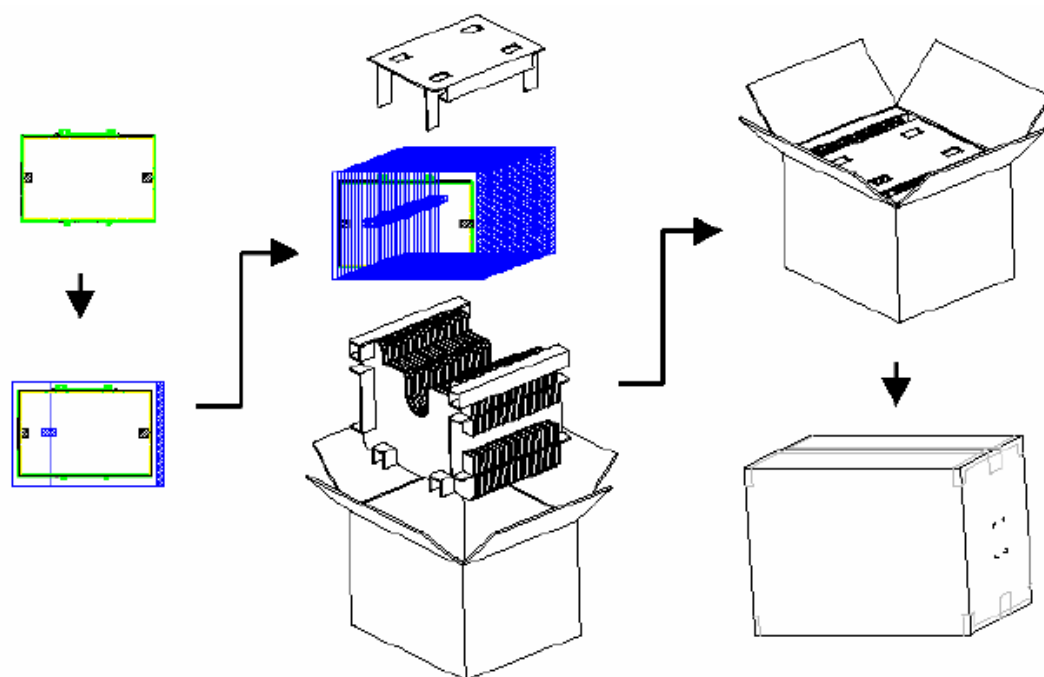
### 9.1 Shipping Label Format

#### 9.1.1. Panel shipping label

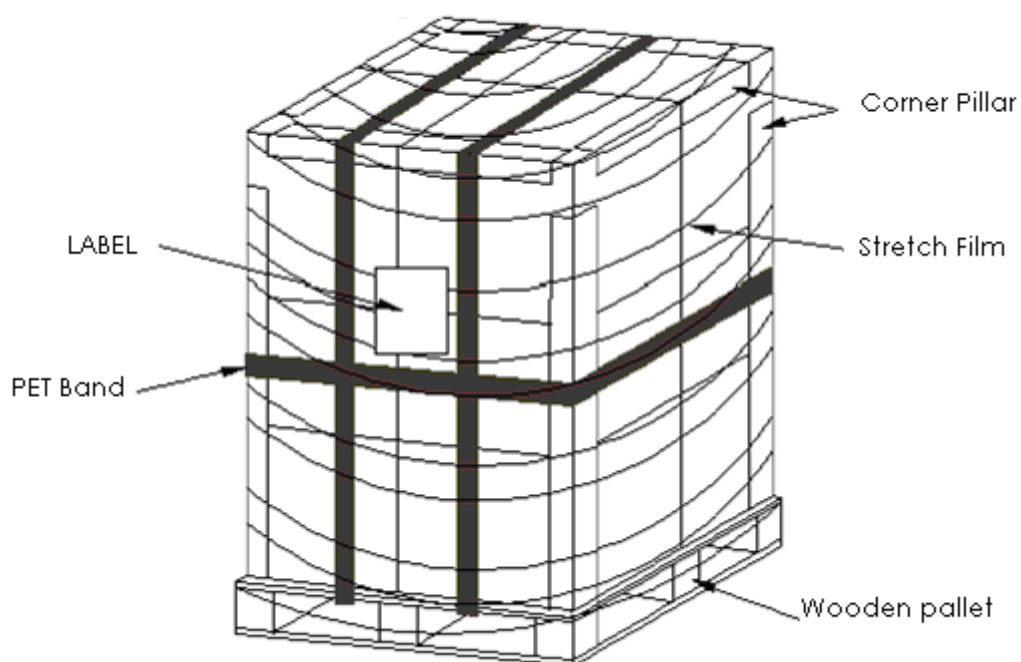
#### 9.1.2. Carton label

## 9.2

### Carton Package



## 9.3 Shipping Package of Palletizing Sequence





## 10. Appendix: EDID Description