LCD MODULE

SPECIFICATION

Module Size：**12.02"2160x1440**

Spec Part No.：

Date：**2015-09-21**

Version：A

Revision History

Version	Revise Date	Page	Content	Prepared by
A	2015-9-21	All	First Release	Zheng Yi

Table of Contents

1 General Specification

1.1 Features

-- Thin and light weight

-- Display 16.7M colors

-- EDP1.3　Interface

-- High luminance and contrast ratio, low power consumption and wide viewing angle

1.2 Application

Display module for Portable Terminal

1.3 General Specification

No.	Item		Specification	STD	Unit	Remark
1	Display Size		→	12.2	Inch	
2	TFT Technology Type		→	a-Si		
3	Liquid Crystal Alignment Method		IPS	IPS or equivalence		
4	Resolution		→	2160*RGB*1440		
5	Display mode		Normal Black	Transmissive		
6	Color Depth		→	16.7M（RGB 24bit）		
7	Viewing Direction		→	Full Viewing Angle Min75/Typ80@CR>10		
8	Contrast Ratio		→	800 min/1000 typ		
9	Luminance		→	380 min/450 typ	cd/m^2	9point average
10	Module Size	LCM	→	262.42 (W)*179.55(H)*Max2.25 (T)	mm	Note 1 CPK>1.33
11	Maximum Thickness		→	Panel：0.2(Typ)/0.2(Typ) Module: Max4.25 (w PCBA)	mm	Note 1
12	Panel Active Area		→	254.016(W)*169.344(H)	mm	Note 1
13	Pixel Size		→	0.0392(W)*0. 1176(H)	mm	
14	Pixel Pitch		→	0.1176(W)×0.1176(H)	mm	
15	Pixel Aspect Ratio		→	1:1	mm	

16	Driver IC	TC2016	TBD		6EA
17	Light Source	→	RG LED Backlight		
18	Interface	→	eDP1.3		
19	Vcom type	→	DC Vcom		
20	Driver Inversion type	Column Inversionon	Column Inversionon /Z Inversion		
21	Operation Temperature	→	-10~+60	degC	
22	Storage Temperature	→	-20~+70	degC	
23	Weight	165	168	Gram	
24	Pixel Per inch	216	216	PPI	
25	Pixel Aperture Ratio	TBD	TBD	%	
26	Environmental Protection Requirement	RoHS	RoHS & REACH must be executed		
27	Connection method	ZIF 40Pins	ZIF 40Pins		
28	PSR(RAM Size)	Need	Need		
29	Color Enhancement	→	Need		Note 4
30	CABC Function	→	Need		
31	E-EDID	Implementing an EDID 1.3 or later data structure	Implementing an EDID 1.3 or later data structure		
32	Dynamic Contrast	Need	Need		
33	Gamma Correction	Need	Need		
34	Polarizer Type	Hard coat treating Glare	Hard coat treating Glare	3H	
35	Panel gate scan direction reverse	Support	TBD		
36	warpage	front side value < 0.4mm rear side value < 0.4mm.	front side value < 0.4mm rear side value < 0.4mm.		Note 2, And refer to 1st lot;
37	Diagonal Stripes&Morie	Invisible	Invisible		Note 3

Note 1:Please Refer to the mechanical drawing.

Note 2: Warpage inspected by measuring system to analyze surface warpage and module thickness.

[1] Tp side test

TP side test

PCBA

PCBA
Module

Marble platform
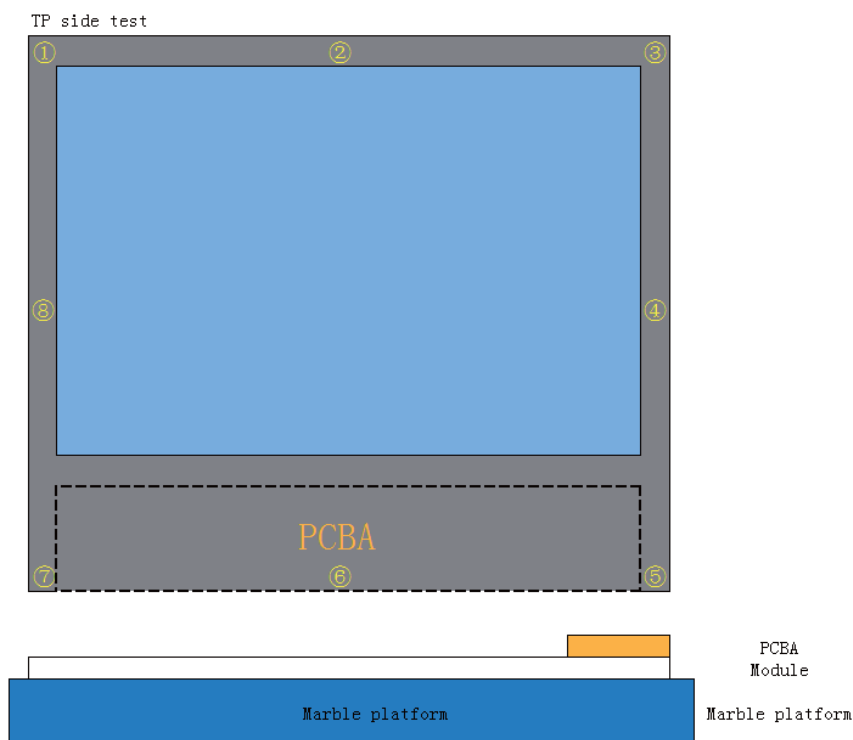
Marble platform

- Remove protect film of TP side,put glass face down on the marble platform as shown in the figure.
- Smooth around bezel tape in order to prevent the bubble impact test.
- Test the warpage of TP side with feeler guage in order of 1,2,3,4,5,6,7,8.

[2] LCD side test
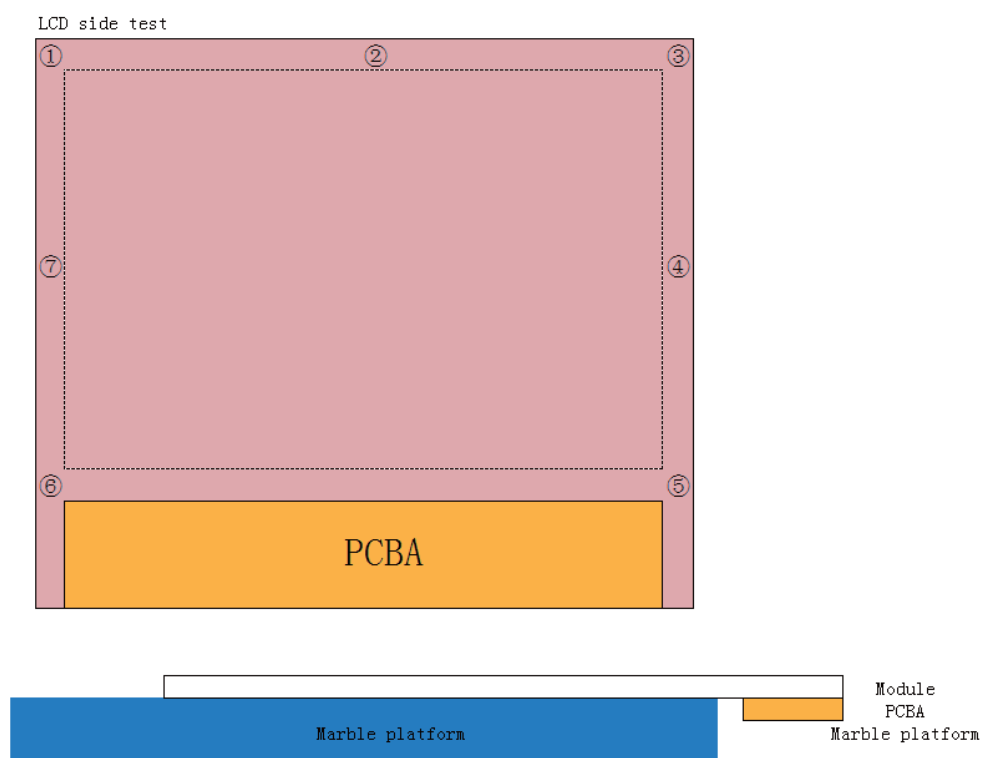
- Remove protect film of both side,put backlight face down on the marble platform as shown in the figure.
- Smooth around bezel tape in order to prevent the bubble impact test.
- Test the warpage of LCD side with feeler guage in order of 1,2,3,4,5,6,7.

Note 3: Viewing distance: 20cm to 25cm.

Viewing angle: $\theta_L < 45°$, $\theta_R < 45°$, $\psi_T < 45°$, $\psi_B < 45°$.

The viewing angle Refer to Note 9.

Note 4: The detail test method can refer to the template of HUAWEI Display Validation test report.

2 Pin Assignments

2.1 Display Interface

Pin No.	Symbol	Voltage	Description	I/O
1	VCCS	3.3V	LCD logic and driver power	P
2	VCCS	3.3V	LCD logic and driver power	P
3	VCCS	3.3V	LCD logic and driver power	P
4	HSYNC	3.3V	Horizontal SYNC signal	O

5	ID	3.3V/0V	ID Pin	-
6	BIST	NA	BIST enable	I
7	GND		Ground	P
8	AUX_CH_N	500mV(min)	Complement Signal Auxiliary Channel	I/O
9	AUX_CH_P	1000mV (max)	True Signal Auxiliary Channel	I/O
10	GND		Ground	P
11	Lane0_N	100mV(min)	Complement Signal Link Lane 0	I
12	Lane0_P	1320mV (max)	True Signal Link Lane 0	I
13	GND		Ground	P
14	Lane1_N	100mV(min)	Complement Signal Link Lane 1	I
15	Lane1_P	1320mV (max)	True Signal Link Lane 1	I
16	GND		Ground	P
17	Lane2_N	100mV(min)	Complement Signal Link Lane 2	I
18	Lane2_P	1320mV (max)	True Signal Link Lane 2	I
19	GND		Ground	P
20	Lane3_N	100mV(min)	Complement Signal Link Lane 3	I
21	Lane3_P	1320mV (max)	True Signal Link Lane 3	I
22	GND		Ground	P
23	HPD	3.3V	HPD signal pin	I/O
24	GND		Ground	P
25	WPN	NA	I2C Write Protection	I
26	SCL	NA	I2C CLK	I
27	SDA	NA	I2C SDA	I/O
28	DBC_EN	3.3V/0V	Pull High Enable, Pull Low Disable	I
29	BL_PWM_IN	3.3V	System PWM signal input for dimming	I
30	BL_PWM_OUT	3.3V	Bypass PWMI or TCON output PWM for BL control	O
31	LED_1		Power for LED1 Cathode	P
32	LED_2		Power for LED2 Cathode	P
33	LED_3		Power for LED3 Cathode	P

34	LED_4		Power for LED4 Cathode	P
35	LED_5		Power for LED5 Cathode	P
36	LED_6		Power for LED6 Cathode	P
37	NC		Reserved for LCD manufacturer's use	-
38	BL_VCCS	29V	Power for LED Anode	P
39	BL_VCCS	29V	Power for LED Anode	P
40	BL_VCCS	29V	Power for LED Anode	P

3 Module data for customer

3.1 Mechanical Drawing

Drawing Attachment:(The drawing file will be sent by Huawei Additionally)

12inch 2160*3(RGB)*1440

179.55 ± 0.20 (Outline)
172.244 ± 0.20 (CF Pol)
169.344 ± 0.10 (Active Area)

(7.50 AA to Outline)
(1.90 AA to CF Pol)

2.70 ± 0.30 (AA to Outline)
1.00 ± 0.20 (AA to CF Pol)

(5.50 AA to Outline)
(1.15 AA to CF Pol)

(132.508)

262.42 ± 0.25 (Outline)
256.316 ± 0.20 (CF Pol)
254.016 ± 0.10 (Active Area)

Active Area Center

(87.372)

2.90 ± 0.30 (AA to Outline)
1.15 ± 0.20 (AA to CF Pol)

SECTION A-A

64.25 (Max)

2.25 Max

2.30 Max

0.05 (Punch)

168.20 ± 0.50 (Connector to Outline)

14.00　Max (PCBA to Outline)

(2X) 5.21 ± 0.30

7.91 ± 0.30

30.40 ± 0.30

125.47 ± 0.30

23.41 ± 0.50 (Outline to Connector Pin)

(248.00 PCBA)

Active Area Center

BLU ID Printing Area

Module ID Printing Area

(12.00 PCBA)

(6.51) PCBA to Outline)

NO	Document No.	Type	Format	Attachment file
1	TV120WTM-NH0 LCM Outline	2D	CAD	lcm_assy_12inch .dwg
2	TV120WTM-NH0_HW_MDL	3D	Stp	lcm_assy_12inch _asm.stp

Double-Click the "Attachment Icon" above for opening attachment file.

3.2 Code of module

NO	Document No.	Type	Attachment file
1	TV120WTM-NH0 Initial Code For HUAWEI	initialization	工作表 在 TV120WTM-NH0-1RA0

Double-Click the "Attachment Icon" above for opening attachment file.

Remark：initialization code must include the code for GAMMA 2.2 in the Power Supply condition for the module。

3.3 Electrical circuit

NO	Document No.	Type	Attachment file
1	TV120WTM-NH0 PCB Schematic	principium	12inch HW_Final_0921.PDF
2	TV120WTM-NH0 PCB Gerber	layout	Gerber for 12inch_Final_0918
3	TV120WTM-NH0 Circuit Design Checklist	checklist	确认后更新

Double-Click the "Attachment Icon" above for opening attachment file.

4 Schematic Circuit Diagram

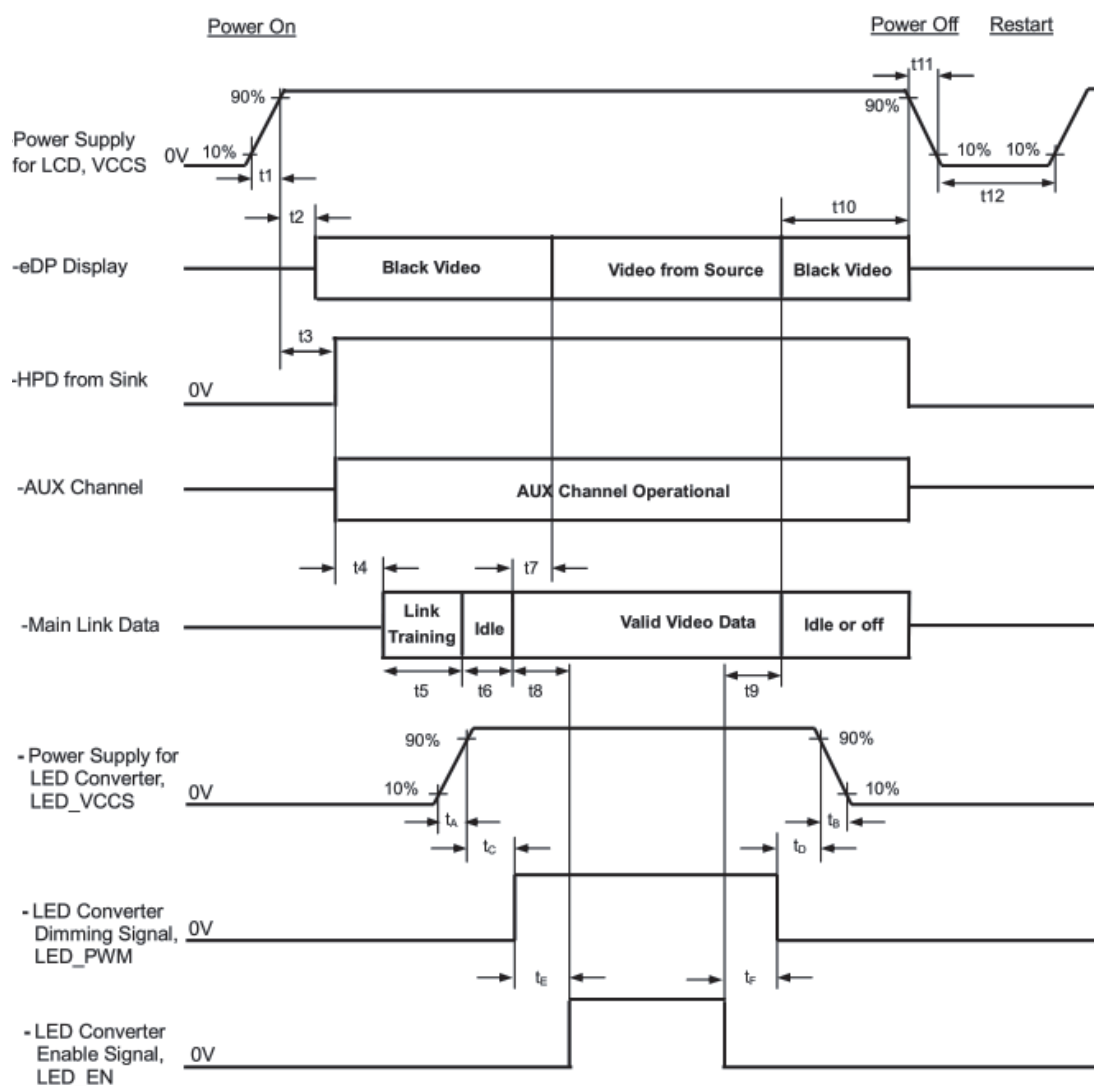## 4.1 Display Edp1.3 Reference Circuit
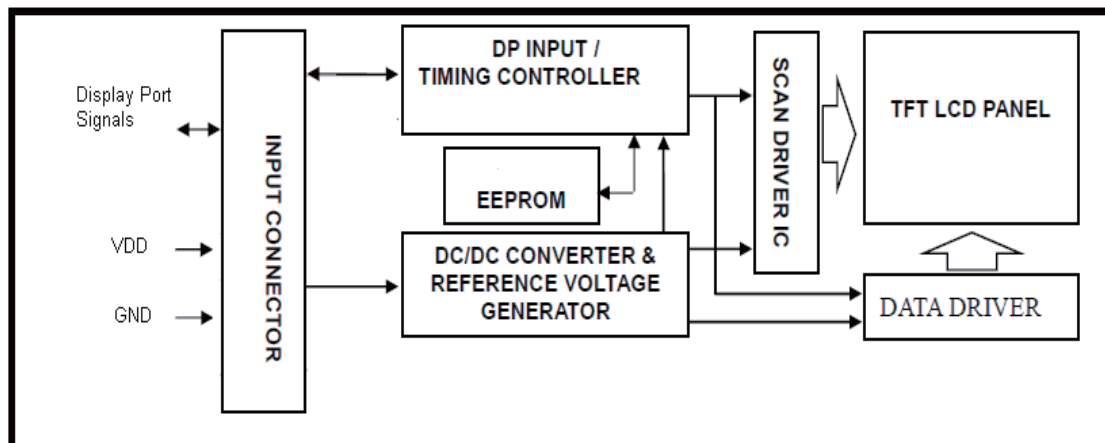
5 Register & Pixel Data Format

5.1 eDP1.3 Data Format

24bpp RGB to a 4-Lane Main Link Mapping

Lane 0	Lane 1	Lane 2	Lane 3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-7:0	B5-7:0	B6-7:0	B7-7:0
R8-7:0	R9-7:0	R10-7:0	R11-7:0
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-7:0	B9-7:0	B10-7:0	B11-7:0

6 Timing Characteristics

6.1 Power on/off Sequence

Timing Specifications:

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	-	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	-	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	-	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	-	-	ms	Source must assure display video is stable
t9	Delay from backlight off to end of valid video data	Source	-	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below)
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-
t12	VCCS Power off time	Source	500	-	ms	-
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t_B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-

6.2 EDP1.3 Input Signal Characteristics

Support for Panel Self Refresh (PSR)

7 Electrical Specifications

7.1 LCD Typical Operation Conditions

Item		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	
Ripple Voltage		V$_{RP}$	-	(50)	-	mV	
LED PWM OUT	High Level	VOH	3.0	3.3	3.6	V	
	Low Level	VOL	-	-	0.495	V	
Frame frequency		fFrame	-	60	-	HZ	
Hot plug Detect		HPD	-	3.3	-	V	

7.2 Power Consumption of TFT Panel

Power Supply: Frame Frequency: VDDframe>=60HZ @ 25degC456

Display Mode	Item	Symbol	Value		Unit	Remark
			Typ	Max		
Display White	Current of VDD	IVDD	330	350	mA	以后续实测数据为准
Display Black	Current of VDD	IVDD	TBD	TBD	mA	
Standby Mode	Current of VDD	IVDD	-	TBD	mA	

7.3 Power Consumption of Backlight

Test Condition: I_{LED}=21mA   LED 54PCS

Warning: LCM Brightness must match Optical Spec requirement when I_{LED}=21mA

Backlight Unit Schematic:

Item	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Forward Voltage	V_{BL}		TBD	28.8	V	Note 5
Power Consumption	P_{BL}		TBD	3650	mW	
LED Quantity		54			pcs	
LED Rank		Luminous Flux: TBD			lm	
		Chromaticity:TBD				

Note 5 : When I_{LED}=21mA，the V_{BL} must be in the range of above table specified.

The FPC wire resistance between LED+ and LED- must be less than 0.15ohm

$P_{BL}= I_{LED}× V_{BL}$

Note 6 : The overall Power consumption of Backlight and Panel is less than 4600mW.

8 Optical Specifications

Test condition：VDD=3.3V , I_{LED}=21mA, Ta=25℃

Item		Symbol	Condition	Value			Unit	Note
				Min	Typ	Max		
luminance		Bp	θ=0°	380	450	--	cd/m^2	Note 7
Uniformity		△Bp	Φ=0°	75	80	--	%	Note 8
Color Uniformity		△u'△ v'-A		--	--	0.015		Note 26
		△u'△ v'-B		--	--	TBD		Sign the limit sample shall prevail.
		△E*ab		--	--	NA		
Viewing Angle	Left	$θ_L$	Cr≥10	75	80	--	deg	Note 9
	Right	$θ_R$		75	80	--		
	Top	$ψ_T$		75	80	--		
	Bottom	$ψ_B$		75	80	--		
Contrast Ratio		Cr	θ=0°	800	1000	--	-	Note 10
Response		$T_{r+}T_f$	Φ=0°	--	25	35	m	Note 11

						s	
Time						s	
	Tgray		-	45	55	ms	
Color Coordinate of CIE1931	Red	x	Typ-0.03	0.673	Typ+0.03	-	Note 12
		y	Typ-0.03	0.326	Typ+0.03		
	Green	x	Typ-0.03	0.265	Typ+0.03		
		y	Typ-0.03	0.634	Typ+0.03		
	Blue	x	Typ-0.03	0.149	Typ+0.03		
		y	Typ-0.03	0.058	Typ+0.03		
	White	x	0.272	0.302	0.332		
		y	0.284	0.314	0.344		
NTSC Ratio	NTSC	CIE1931	--	85	--	%	Note 13
Color Temperature	CT		-	7500	-		
Flicker	amount	-	-	-	-30	dB	Note 14
Gamma		-	1.9	2.2	2.5		Note 15
Crosstalk	△CT	-	-	1.10	1.20		Note 16
Transmittance @w/o APF	Tm		TBD		--	%	
Reflectance	Rf	@550nm	--		TBD	%	Note 17
Polarization Direction of Front Polarizer	PdF			TBD		deg	Note 18
Polarization Direction of Rear Polarizer	PdR			TBD		deg	
Luminance decrease ratio		θL=30°	---	---	75	%	Note 19
		θR=30°	---	---	75	%	
		ψT=30°	---	---	75	%	
		ψB=30°	---	---	75	%	
Contrast decrease ratio		θL=30°	---	---	75	%	Note 20
		θR=30°	---	---	75	%	
		ψT=30°	---	---	75	%	
		ψB=30°	---	---	75	%	
Color shift		θL=30°	---	---	3	JNCD	Note 21
		θR=30°	---	---	3	JNCD	
		ψT=30°	---	---	3	JNCD	
		ψB=30°	---	---	3	JNCD	
Gray inversion angle		ψ=0°		NA		deg	Note 22
Sunglass Readability			NA				
Afterimage				3		Minute	Note 23
CABC Test							Note 24
Hot spot	△Bp	θ=0° Φ=0°	75	80		%	Note25

|		θ=0° Φ=0°	80	85		%	Every near 9 points Note25

Note7:Luminance measurement

The test condition is at I_{LED}=21mA and measured on the surface of LCD module at 25℃

- The data are measured after LEDs are lighted on for more than 5 minutes and LCM displays are fully white. The brightness is the average value of 9 measured spots. Measurement equipment CS2000 or similar equipments(Field of view:1deg,Distance:50cm)

- Measuring surroundings: Dark room.

- Measuring temperature: Ta=25℃.

- Adjust operating voltage to get optimum contrast at the center of the display.

- Measured value at the center point of LCD panel must be after more than 5 minutes while backlight turning on.
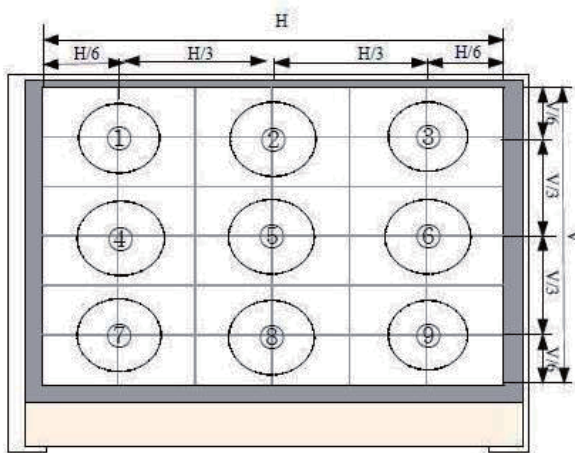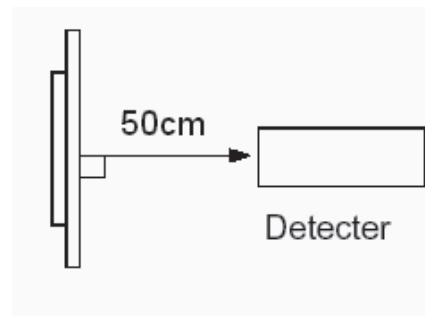
Note8:Uniformity

- The test condition is at I_{LED}=20mA and measured on the surface of LCD module at 25℃.
- Measurement equipment:CS2000 or similar equipments
- The luminance uniformity is calculated by using following formula:

- $\triangle Bp = Bp$ (Min.) / Bp (Max.)$\times 100$ (%)
- Bp (Max.) = Maximum brightness in 13 measured spots
- Bp (Min.) = Minimum brightness in 13 measured spots.
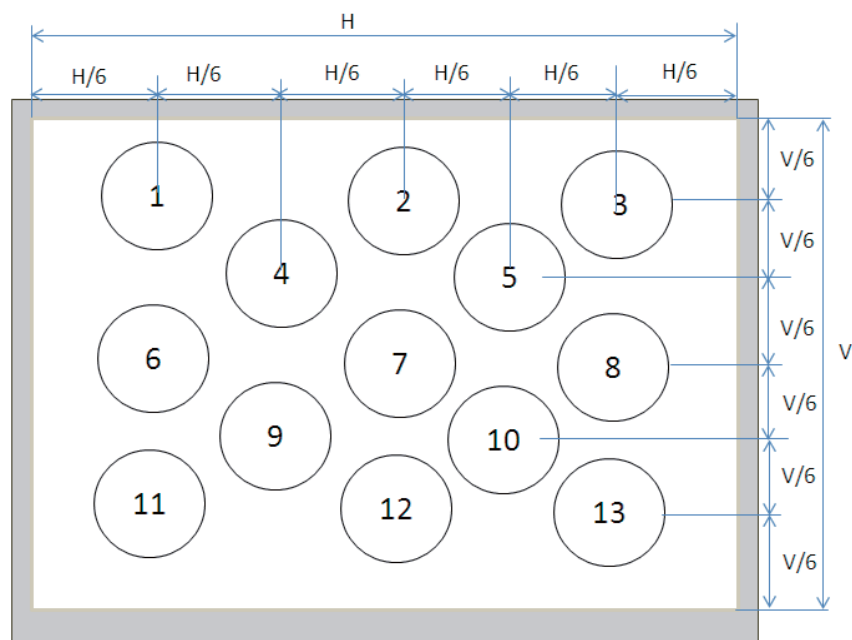
Note 9:**The definition of Viewing Angle**

Refer to the graph below marked by
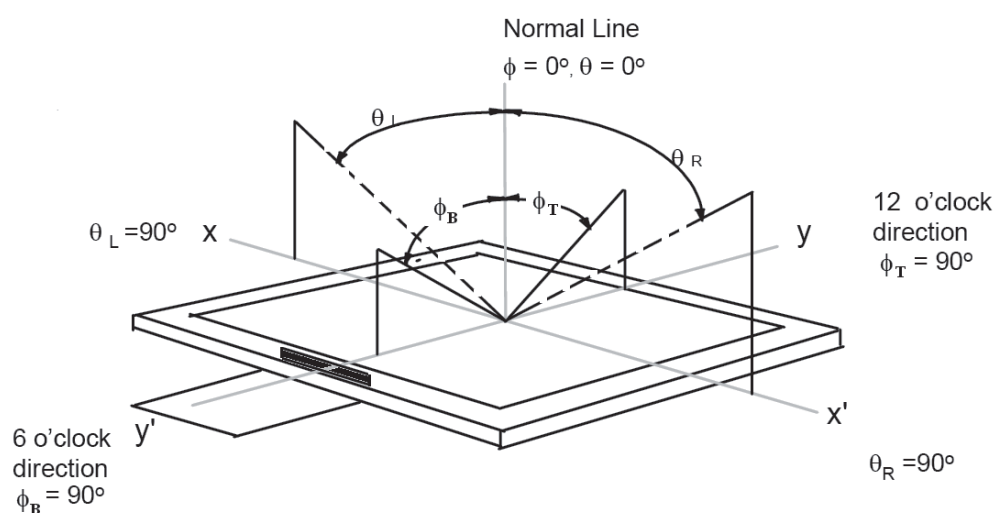
Note10:**ThedefinitionofContrastRatio** (Test LCM using CS2000 or similar equipments):

$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance When LCD is at "White" state}}{\text{Luminance When LCD is at "Black" state}}$$

(Contrast Ratio is measured in optimum common electrode voltage)

Note11:**DefinitionofResponse time.**(Test LCD using DMS501 or similar equipments):

Theoutputsignalsofphotodetectoraremeasuredwhentheinputsignalsarechanged from "black"to"white"(Voltagefallingtime)andfrom"white"to"black"(Voltage rising time), respectively .The response time is defined as the time interval between the 10% and 90% of amplitudes . Refer to figures below.
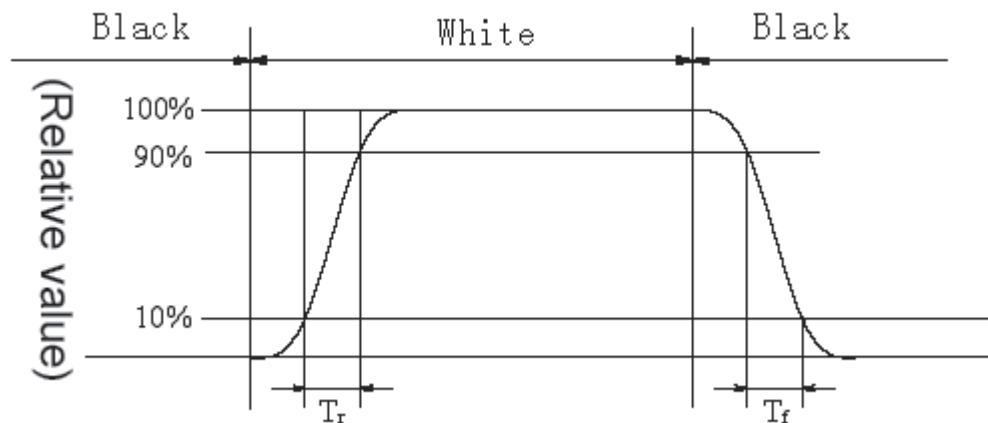
Response time of gray to gray:

- Measurement equipment: DMS501 or similar equipments.
- Test method: we define 8 grays L0-L7,the grays of L0-L7 were defined as:0,36,73, 109, 146, 182, 219, 255. Theoutputsignalsofphotodetectoraremeasuredwhentheinputsignalsarechanged from "Lx" to "Ly", x, y= [0, 7]. The response time is defined as the time interval between the 10% and 90% of amplitudes. The result of the test can be noted as below:

	L0	L1	L2	L3	L4	L5	L6	L7
L0	■							
L1		■						
L2			■					
L3				■				
L4					■			
L5						■		
L6							■	
L7								■

Note 12: Color Coordinates of CIE 1931

- The test condition is at I$_{LED}$=20mA and measured on the surface of LCD module at 25℃.
- Measurement equipment:CS2000 or similar equipments
- The Color Coordinate (CIE 1931) is the measurement of the center of the display shown in below figure.

Note 13: Definition of Color of CIE Coordinate and NTSC Ratio.

$$S = \frac{area \ of \ RGB \ triangle}{area \ of \ NTSC \ triangle} \times 100\%$$
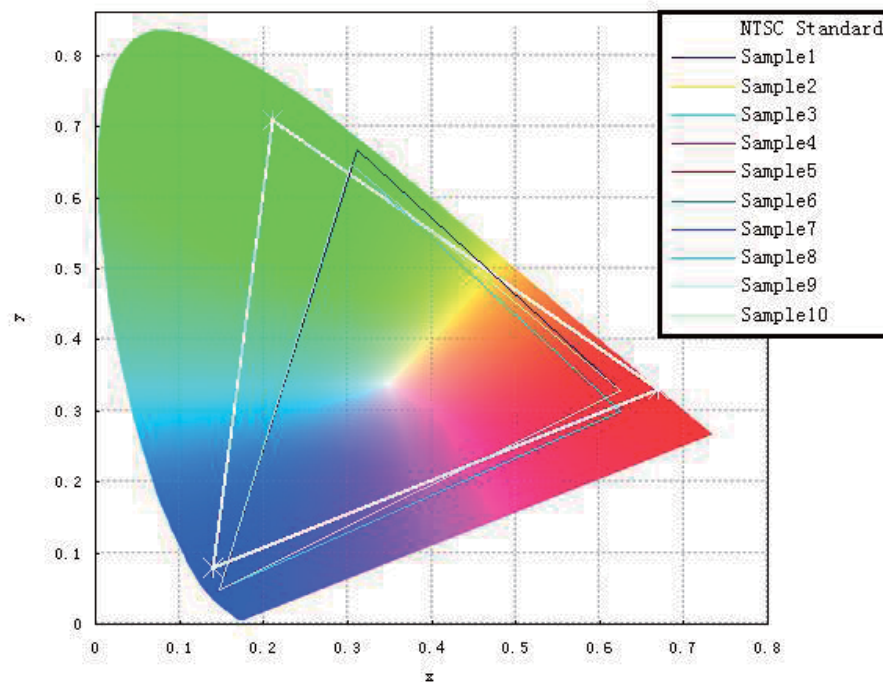
Note 14: **Flicker**

- Measurement equipment :CA-210 or similar equipments
- Measuring temperature: Ta=25℃.
- Test method: JEITA method
- Test pattern : Refer to below(Test Pattern should be full-fill of display screen)
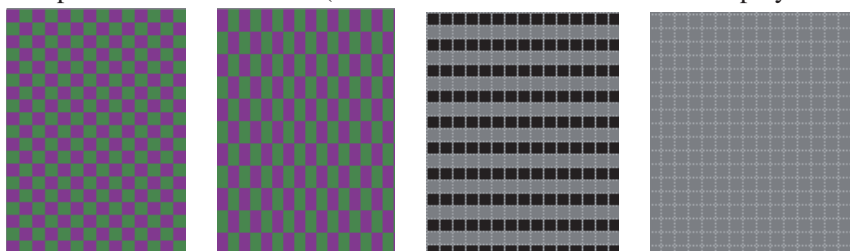
1 Dot Inversion,   2 Dot Inversion ,   Line Inversion ,   Frame Inversion

The point should be marked is, for line and frame inversion, the background of Flicker

Test Pattern-"gray " are defined as middle gray scale .For example, RGB 24bit "gray" defined as below:

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

For Dot inversion, the RGB data for first pixel is (127, 0, 127), the RGB data for the second pixel is (0, 127, 0).

- Frame Frequency Requirement before test： The LCD must be tuned to more than 65HZ before measurement.

- Measurement Point: the center of display active area

- Conversion of Flicker ratio:

  Flicker [dB] = 10 x log[Px/P0]

  Where

  Px: Maximum power spectrum of AC component after passing through integrator

  P0: Power spectrum of DC component after passing through integrator

  AC component=b (Refer to below diagram)

  DC component=a (Refer to below diagram)
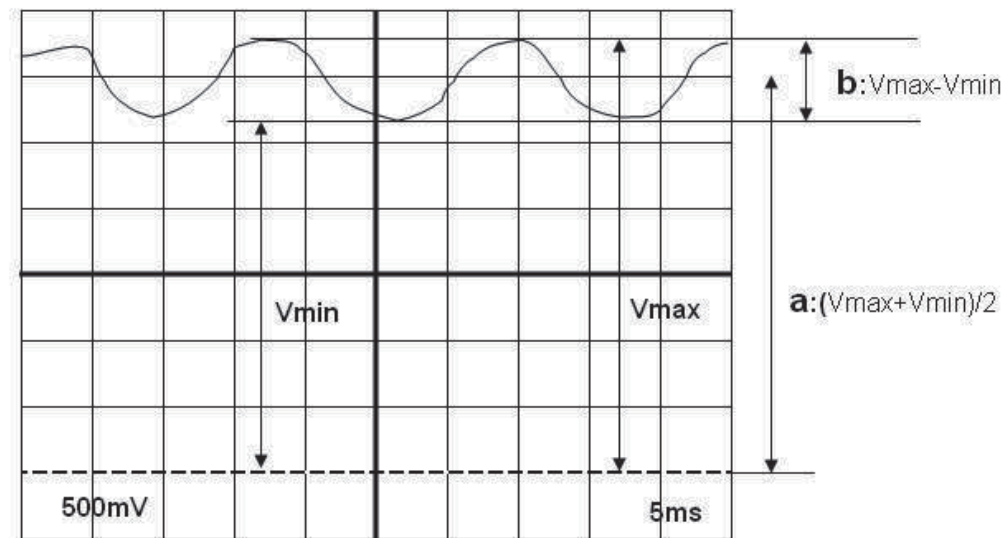
Note 15: gamma curve control

- For gamma curve control, HUAWEI's request as below:

- 1,the whole curve's tolerance must control within +/-0.3, HUAWEI will test the gray scale below:
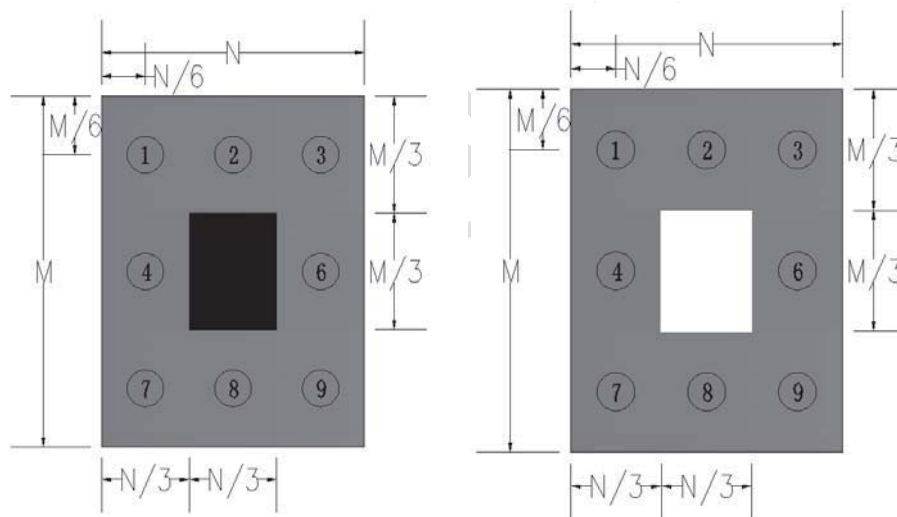
  0, 8, 16, 25, 33, 41, 49, 58, 66, 74, 82, 90, 99, 107, 115, 123, 132, 140, 148, 156, 165, 173, 181, 189, 197,206, 214, 222, 230, 239, 247, 255

Note 16:**Crosstalk**

- There should be no visible cross-talk in normal direction of the display when the two "Cross-talk Test Patterns" below are loaded.

- Measurement equipment:CS2000 or similar equipments

- The point should be marked is, the background of Cross-talk Test Pattern-"gray " are defined as middle gray scale . For example, RGB 24bit "gray" defined as below:
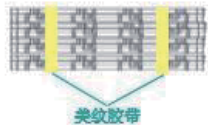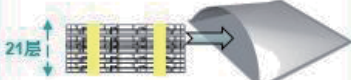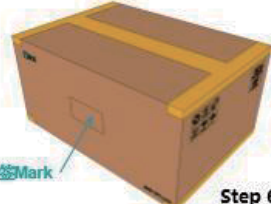
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

- $\triangle Bpn = Bpn \text{ (gray)} / Bpn \text{ (white)}$

  Which n means the dot No. In the Cross-talk Test Pattern ;

  Bpn (gray) means the brightness of the No.n spots in Cross-talk Test Pattern;

  Bpn (white) means the brightness of the No.n spots in Full white Test Pattern;

- $\triangle Bp \text{ (Max.)}$ = Maximum value in $\triangle Bp1 \sim \triangle Bp9$, except the No. 5 spot.

- $\triangle Bp \text{ (Min.)}$ = Minimum value in $\triangle Bp1 \sim \triangle Bp9$, except the No.5 spot.

- $\triangle CT = \triangle Bp \text{ (Max.)}/\triangle Bp\text{(Min.)}$.

- $\triangle CT$ must be less than 1.10

Cross-talk Test Pattern

9 Packing Method

9.1 Packing order

- **Box Dimension: 545mm(W) x 380mm(D) x 252mm(H)**
- **Package Quantity in one Box: 40pcs**

10   Reliability Requirement

NO	Document No.	Type	Attachment file
1	-	mechanism	Attachment
2	-	environment	
3	-	electric	
4	-	ROSH	Attachment

Double-Click the "Attachment Icon" above for opening attachment file.

10.1 General Reliability Requirement

Test item	Test condition	No. of failures /No. of examinations
Low temperature storage test	Ta= -10°C, 240h, Recovery Time 2 Hrs.	0/10
High temperature storage test	Ta= 60°C, 240h, Recovery Time 2 Hrs.	0/10
Low temperature operation test	Ta= 0°C, 240h, Recovery Time 2 Hrs.	0/10
High temperature operation test	Ta= 50°C, 240h, Recovery Time 2 Hrs.	0/10
High temperature & High humidity operation test	Ta= 50°C, 80%RH, 240h, Recovery Time 2 Hrs.	0/10
Thermal Shock	(-10°C 30min) → (60°C 30min)]/cycle, 100cycles, Transfer time less than 5 Mins. Recovery Time 2 Hrs.	0/10

Note: Vendors and Huawei should reach an agreement on items marked in red before quotation.