



TO : China general

DATE : Oct, 11, 2011

SAMSUNG TFT-LCD

MODEL NO.: LTN140AT21-W

NOTE: Extension code [- Wxx]

→ LTN140AT21-Wxx

Surface type [Anti-Glare]

Any modification of Spec is not allowed without SEC's permission

Application engineering part, Mobile Division Samsung Electronics Co., Ltd.

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REVISION HISTORY

Approval

Date	Revision No.	Page	Summary
Oct. 11. 2011	A00	All	The approval specification of 14.0" SMS HD was issued first.

GENERAL DESCRIPTION

DESCRIPTION

LTN140AT21 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as switching devices.

This model is composed of a TFT LCD panel, a driver circuit and a backlight unit.

The resolution of a 14.0" contains 1366 x 768 pixels and can display up to 262,144 colors.

6 O'clock direction is the optimum viewing angle.

FEATURES

- · High contrast ratio
- HD(1366 x 768 pixels) resolution
- Fast Response
- LED Back Light with embedded LED Driver
- DE (Data enable) only mode
- 3.3V LVDS Interface
- Onboard EEDID chip

APPLICATIONS

- Notebook PC
- If the usage of this product is not for PC application, but for others, please contact SEC

GENERAL INFORMATION

Item	Specification		Note
Display area	309.399 (H) x 173.952 (V) (14.0"diagonal)	mm	
Driver element	a-Si TFT active matrix		
Display colors	Display colors 262,144		
Number of pixel	1366 * 768	pixel	16:9
Pixel arrangement	RGB vertical stripe		
Pixel pitch	0.2265(H) x 0.2265(V)	mm	
Display Mode	Normally white		
Surface treatment	Haze 25%, Hardness 3H		A/G

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Mechanical Information

	Item	Min.	Тур.	Max.	Unit	Note
	Horizontal (H)	323.0	323.5	324.0	mm	
Module size	Vertical (V)	191.4	191.9	192.4	mm	
3126	Depth (D)	-	-	4.0	mm	PCB Area
	Weight	-	-	355	g	

Note (1) Measurement condition of outline dimension

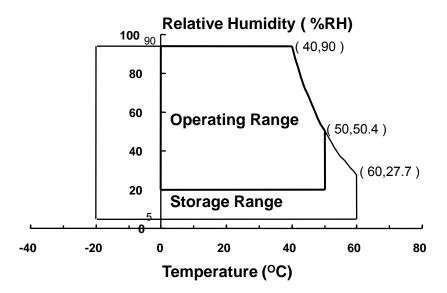
. Equipment : Bernier Calipers . Push Force : 500g ·f (minimum)

1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENTAL ABSOLUTE RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Storage temperate	TSTG	-20	60	°C	(1)
Operating temperate (Temperature of glass surface)	TOPR	0	50	°C	(1)
Shock (non-operating)	Snop	-	240	G	(2),(4)
Vibration (non-operating)	Vnop	-	2.41	G	(3),(4)

Note (1) Temperature and relative humidity range are shown in the figure below. 95 % RH Max. (40 $^{\circ}$ C \geq Ta) Maximum wet - bulb temperature at 39 $^{\circ}$ C or less. (Ta > 40 $^{\circ}$ C) No condensation



- (2) 2ms, half sine wave, one time for $\pm X$, $\pm Y$, $\pm Z$.
- (3) 5 500 Hz, random vibration, 30min for X, Y, Z.
- (4) At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard and rigid enough so that the Module would not be twisted or bent by the fixture.

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1.2 ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

 $V_{DD} = 3.3V, V_{SS} = GND = 0V$

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V _{DD}	V _{DD} - 0.3	V _{DD} + 0.3	V	(1)
Logic Input Voltage	Vin	V _{DD} - 0.3	V _{DD} + 0.3	V	(1)

Note (1) Within Ta (25 \pm 2 °C)

(2) BACK-LIGHT UNIT

Ta = 25 ± 2 °C

Item	Symbol	Min.	Тур.	Max.	Unit	Note
LED Current	I L	-	22	-	mArm s	(1)
LED Voltage	VL	-	3.2	-	V	(1)

Note 1) Permanent damage to the device may occur if maximum values are exceeded Functional operation should be restricted to the conditions described under normal operating conditions.

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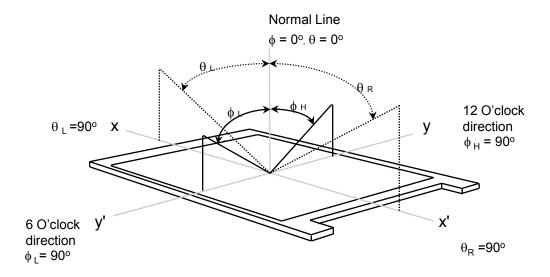
2. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (5). Measuring equipment: TOPCON SR-3

		* T	$a = 25 \pm 2$ °C	C, V _{DD} =3.3	3V, fv= 60)Hz, fdclk=	: 70.7MHz, II	= 100% duty	
ltem		Symbol	Condition	Min.	Тур.	Max	Unit	Note	
Contrast I (5 Poil		CR		300	-	-	-	(1), (2), (5)	
Response Tir (Rising + F		Тят		-	16	25	msec	(1), (3)	
Average Lun of White (5		YL,AVE	Normal	200	220	-	cd/m ²	IF=100% duty (1), (4)	
	Ded	Rx	Viewing		0.565				
	Red	Ry	Angle φ = 0		0.350				
	0	Gx	θ = 0		0.340				
Color	Green	Gy		Тур-	0.565	Тур			
Chromaticity (CIE)	Dlue	Вх		0.03	0.155	+0.03	-		
	Blue	By					0.120		
	White	Wx			0.313			SR-3	
	vvriite	WY			0.329				
	Hor	θι		40	-	-			
Viewing	Hor.	θн	CR ≥ 10	40	-	-	Degrees		
Angle	Ver.	фн	At center	15	-	-			
		фь		30	-	-			
Color Ga	ımut	CG		-	45	-	%		
13 Poir White Var		δι		-	-	2.0	-	(6)	

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Note 1) Definition of Viewing Angle : Viewing angle range ($10 \le C/R$)

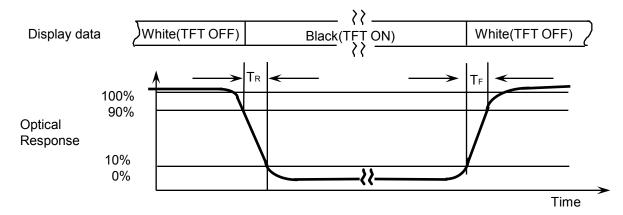


Note 2) Definition of Contrast Ratio (CR): Ratio of gray max (Gmax) ,gray min (Gmin) at 5 points(4, 5, 7, 9, 10)

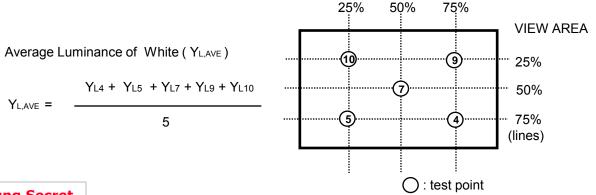
$$CR = \frac{CR(4) + CR(5) + CR(7) + CR(9) + CR(10)}{5}$$

Points : (4), (5), (7), (9), (10) at the figure of Note (6).

Note 3) Definition of Response time:



Note 4) Definition of Average Luminance of White: measure the luminance of white at 5 points.

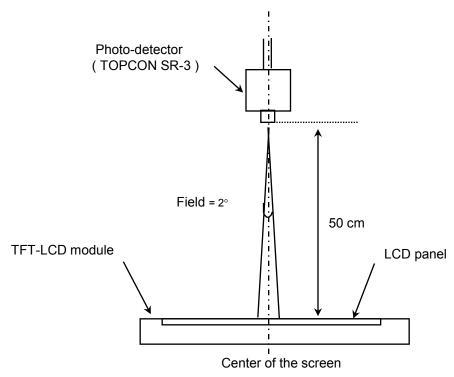


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Note 5) After stabilizing and leaving the panel alone at a given temperature for 30 min , the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. 30 min after lighting the backlight. This should be measured in the center of screen.

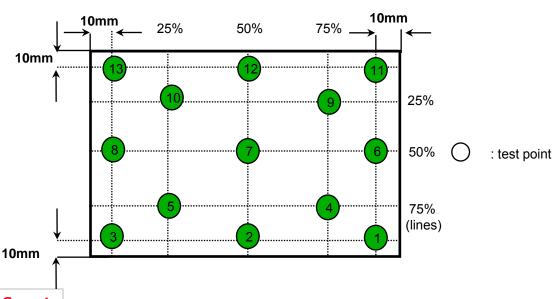
IF current: 22mA

Environment condition : Ta = 25 ± 2 °C



[Optical characteristics measurement setup]

Note 6) Definition of 13 points white variation (δ L), CR variation (CVER) [1 ~ 13] δ L = $\frac{\text{Maximum luminance of 13 points}}{\text{Minimum luminance of 13 points}}$



3. ELECTRICAL CHARACTERISTICS

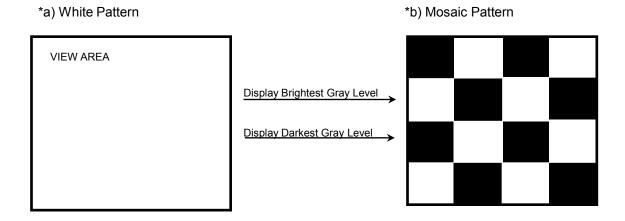
3.1 TFT LCD MODULE

Ta= 25 ± 2 °C

Item		Symbol	Min.	Тур.	Max.	Unit	Note
Voltage of Power	Supply	V _{DD}	3.0	3.3	3.6	>	
Differential Input	High	VIH	-	-	+100	mV	V _{CM} = +1.2V
Voltage for LVDS Receiver Threshold	Low	VIL	-100	-	-	mV	
Vsync Freque	ncy	fv	-	60	-	Hz	
Main Frequer	псу	fdclk	67.39	70.7	105.84	MHz	-
Rush Currer	nt	Irush	1	-	1.5	Α	(4)
	White		-	200	-	mA	
Current of Power Supply	I Mosaic I		-	200	250	mA	*a),b),c)
	V.stripe		-	300	350	mA	

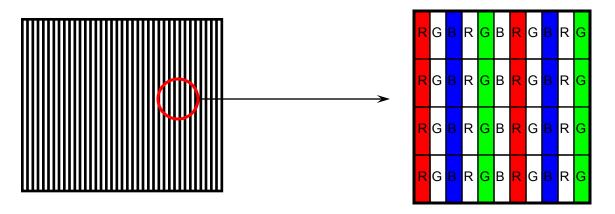
Note (1) Display data pins and timing signal pins should be connected.(GND = 0V)

- (2) $f_V = 60$ Hz, $f_{DCLK} = 70.7$ MHZ, $V_{DD} = 3.3$ V, DC Current.
- (3) Power dissipation pattern

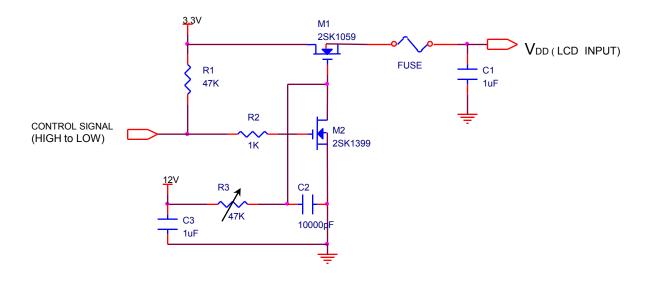


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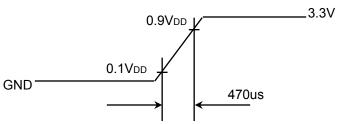
*c) 1dot Vertical stripe pattern



4) Rush current measurement condition



V_{DD} rising time is 470us



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3.2 LED Driver

- On board LED Driver (Intersil)

Ta= 25 \pm 2 °C

Item-	Symbol	Min.	Тур.	Max.	Unit	Note
Input Voltage	Vin	7	12	20	V	-
Input Current	I	ı	250	1	mA	-
Dower Consumption	Р	-	0.7	1	W	@ 60nit
Power Consumption	P	ı	3.0	3.5	W	@ Max
EN control level	ON	2.0	-	-	V	
EN CONTrol level	OFF	-	-	0.8	V	
PWM control level	ON	2.0	-	-	V	
Pyvivi control level	OFF	-	-	0.8	V	
PWM Control Duty	D	5	-	100	%	PWM freq: 200Hz~10KHz
Ratio	D	10	-	100		PWM freq: 1KHz~10KHz
External PWM Dimming Control Frequency (BLIM)	Fвым	0.2	1	10	kHz	
Operating Life Time	Hr	10,000	-	-	Hour	

Note (1) Life time (Hr) of LEDs can be defined as the time in which it continues to operate under the condition Ta= 25 ± 2 °C and IF = 22 mArms until one of the following event occurs. When the brightness becomes 50% or lower than the original.

3.3 BACK-LIGHT UNIT

Ta= 25 \pm 2 °C

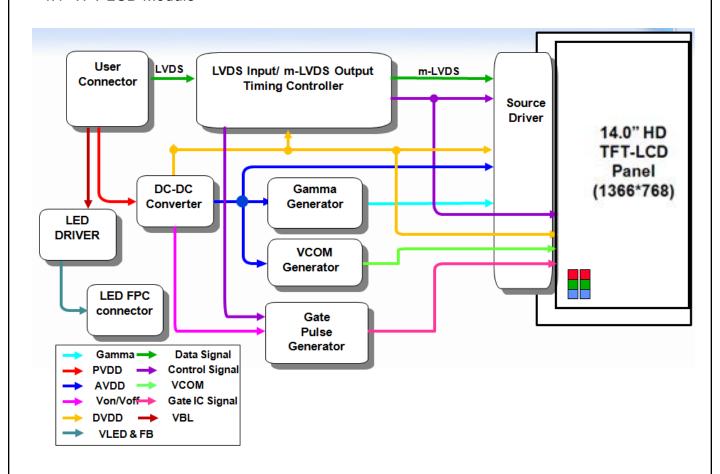
ltem	Symbol	Min.	Тур.	Max.	Unit	Note
LED Forward Current	IF	-	22	-	mA	
LED Forward Voltage	VF	3.0	3.2	3.4	V	
LED Array Voltage	VP	ı	25.6	-	V	VF X 8 LEDs

	unc		

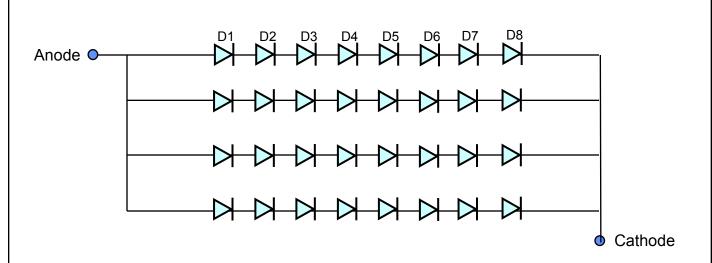
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4. BLOCK DIAGRAM

4.1 TFT LCD Module



4.2 LED placement structure



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5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power (LVDS, Connector: Molex 104062's or equivalent)

1 NC No Connection (Reserved for supplier)	No.	Symbol	Function	Polarity	Remarks
AVDD Power Supply 3.3V (typical)	1	NC	No Connection (Reserved for supplier)		
DVDD DDC 3.3V power	2	AVDD	Power Supply 3.3V (typical)		
5 NC No Connection 6 SCL DDC Clock 7 SDA DDC data 8 RINO- -LVDS differential data input (R0-R5, G0) Negative 9 RINO+ +LVDS differential data input (R0-R5, G0) Positive 10 GND Ground RIN1- -LVDS differential data input (G1-G5, B0-B1) Negative 12 RIN1+ +LVDS differential data input (G1-G5, B0-B1) Positive 13 GND Ground Ground 14 RIN2- -LVDS differential data input (B2-B5, HS, VS, DE) Negative 15 RIN2+ +LVDS differential data input (B2-B5, HS, VS, DE) Positive 16 GND Ground Ground 17 CLK- -LVDS differential clock input Negative 18 CLK+ +LVDS differential clock input Positive 19 GND Ground Ground 20 NC No connection No connection 21 NC No connection No connection	3	AVDD	Power Supply 3.3V (typical)		
6 SCL DDC Clock 7 SDA DDC data 8 RINO- -LVDS differential data input (R0-R5, G0) Negative 9 RINO+ +LVDS differential data input (R0-R5, G0) Positive 10 GND Ground RIN1- -LVDS differential data input (G1-G5, B0-B1) Negative 12 RIN1+ +LVDS differential data input (G1-G5, B0-B1) Positive 13 GND Ground Ground 14 RIN2- -LVDS differential data input (B2-B5, HS, VS, DE) Negative 15 RIN2+ +LVDS differential data input (B2-B5, HS, VS, DE) Positive 16 GND Ground Ground 17 CLK- -LVDS differential clock input Negative 18 CLK+ +LVDS differential clock input Positive 19 GND Ground Ground 20 NC No connection No connection 21 NC No connection No connection 24 NC No connection <t< td=""><td>4</td><td>DVDD</td><td>DDC 3.3V power</td><td></td><td></td></t<>	4	DVDD	DDC 3.3V power		
7 SDA DDC data 8 RINO- -LVDS differential data input (R0-R5, G0) Negative 9 RINO+ +LVDS differential data input (R0-R5, G0) Positive 10 GND Ground RIN1- -LVDS differential data input (G1-G5, B0-B1) Negative 11 RIN1+ +LVDS differential data input (G1-G5, B0-B1) Positive 13 GND Ground Ground 14 RIN2- -LVDS differential data input (B2-B5, HS, VS, DE) Negative 15 RIN2+ +LVDS differential data input (B2-B5, HS, VS, DE) Positive 16 GND Ground Ground 17 CLK- -LVDS differential clock input Negative 18 CLK+ +LVDS differential clock input Positive 19 GND Ground Ground 20 NC No connection No connection 21 NC No connection No connection 24 NC No connection No connection 27 NC	5	NC	No Connection		
8 RINO- -LVDS differential data input (R0-R5, G0) Negative 9 RINO+ +LVDS differential data input (R0-R5, G0) Positive 10 GND Ground Gond 11 RIN1- -LVDS differential data input (G1-G5, B0-B1) Negative 12 RIN1+ +LVDS differential data input (G1-G5, B0-B1) Positive 13 GND Ground Ground 14 RIN2- -LVDS differential data input (B2-B5, HS, VS, DE) Negative 15 RIN2+ +LVDS differential data input (B2-B5, HS, VS, DE) Positive 16 GND Ground Ground 17 CLK- -LVDS differential clock input Negative 18 CLK+ +LVDS differential clock input Positive 19 GND Ground Ground 20 NC No connection No connection 21 NC No connection No connection 24 NC No connection No connection 25 GND Ground	6	SCL	DDC Clock		
9 RIN0+ +LVDS differential data input (R0-R5, G0) Positive 10 GND Ground 11 RIN1LVDS differential data input (G1-G5, B0-B1) Negative 12 RIN1+ +LVDS differential data input (G1-G5, B0-B1) Positive 13 GND Ground 14 RIN2LVDS differential data input (B2-B5, HS, VS, DE) Negative 15 RIN2+ +LVDS differential data input (B2-B5, HS, VS, DE) Positive 16 GND Ground 17 CLKLVDS differential clock input Negative 18 CLK+ +LVDS differential clock input Positive 19 GND Ground 20 NC No connection 21 NC No connection 22 GND Ground 23 NC No connection 24 NC No connection 25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No Connect	7	SDA	DDC data		
10 GND Ground 11 RIN1LVDS differential data input (G1-G5, B0-B1) Negative 12 RIN1+ +LVDS differential data input (G1-G5, B0-B1) Positive 13 GND Ground 14 RIN2LVDS differential data input (B2-B5, HS, VS, DE) Negative 15 RIN2+ +LVDS differential data input (B2-B5, HS, VS, DE) Positive 16 GND Ground 17 CLKLVDS differential clock input Negative 18 CLK+ +LVDS differential clock input Positive 19 GND Ground 20 NC No connection 21 NC No connection 22 GND Ground 23 NC No connection 24 NC No connection 25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No connection	8	RIN0-	-LVDS differential data input (R0-R5, G0)	Negative	
11 RIN1LVDS differential data input (G1-G5, B0-B1) Negative 12 RIN1+ +LVDS differential data input (G1-G5, B0-B1) Positive 13 GND Ground 14 RIN2LVDS differential data input (B2-B5, HS, VS, DE) Negative 15 RIN2+ +LVDS differential data input (B2-B5, HS, VS, DE) Positive 16 GND Ground 17 CLKLVDS differential clock input Negative 18 CLK+ +LVDS differential clock input Positive 19 GND Ground 20 NC No connection 21 NC No connection 22 GND Ground 23 NC No connection 24 NC No connection 25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No connection	9	RIN0+	+LVDS differential data input (R0-R5, G0)	Positive	
12 RIN1+ +LVDS differential data input (G1-G5, B0-B1) Positive 13 GND Ground 14 RIN2LVDS differential data input (B2-B5, HS, VS, DE) Negative 15 RIN2+ +LVDS differential data input (B2-B5, HS, VS, DE) Positive 16 GND Ground 17 CLKLVDS differential clock input Negative 18 CLK+ +LVDS differential clock input Positive 19 GND Ground 20 NC No connection 21 NC No connection 22 GND Ground 23 NC No connection 24 NC No connection 25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No Connection	10	GND	Ground		
13 GND Ground 14 RIN2LVDS differential data input (B2-B5, HS, VS, DE) Negative 15 RIN2+ +LVDS differential data input (B2-B5, HS, VS, DE) Positive 16 GND Ground 17 CLKLVDS differential clock input Negative 18 CLK+ +LVDS differential clock input Positive 19 GND Ground 20 NC No connection 21 NC No connection 22 GND Ground 23 NC No connection 24 NC No connection 25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No Connection	11	RIN1-	-LVDS differential data input (G1-G5, B0-B1)	Negative	
14 RIN2LVDS differential data input (B2-B5, HS, VS, DE) Negative 15 RIN2+ +LVDS differential data input (B2-B5, HS, VS, DE) Positive 16 GND Ground 17 CLKLVDS differential clock input Negative 18 CLK+ +LVDS differential clock input Positive 19 GND Ground 20 NC No connection 21 NC No connection 22 GND Ground 23 NC No connection 24 NC No connection 25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No Connection	12	RIN1+	+LVDS differential data input (G1-G5, B0-B1)	Positive	
15 RIN2+ +LVDS differential data input (B2-B5, HS, VS, DE) 16 GND Ground 17 CLKLVDS differential clock input Negative 18 CLK+ +LVDS differential clock input Positive 19 GND Ground 20 NC No connection 21 NC No connection 22 GND Ground 23 NC No connection 24 NC No connection 25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No Connect	13	GND	Ground		
16 GND Ground 17 CLK- -LVDS differential clock input Negative 18 CLK+ +LVDS differential clock input Positive 19 GND Ground Ground 20 NC No connection No connection 21 NC No connection No connection 23 NC No connection No connection 24 NC No connection No connection 25 GND Ground Ground 26 NC No connection No connection 27 NC No connection No connection 28 GND Ground Ground 29 NC No Connect No Connect	14	RIN2-	-LVDS differential data input (B2-B5, HS, VS, DE)	Negative	
17 CLK- -LVDS differential clock input Negative 18 CLK+ +LVDS differential clock input Positive 19 GND Ground Ground 20 NC No connection No connection 21 NC No connection No connection 22 GND Ground Ground 24 NC No connection No connection 25 GND Ground Ground 26 NC No connection No connection 28 GND Ground Ground 29 NC No Connect No Connect	15	RIN2+	+LVDS differential data input (B2-B5, HS, VS, DE)	Positive	
18 CLK+ +LVDS differential clock input Positive 19 GND Ground Ground 20 NC No connection No connection 21 NC No connection No connection 22 GND Ground Ground 23 NC No connection No connection 24 NC No connection No connection 25 GND Ground Ground 27 NC No connection 28 GND Ground 29 NC No Connect	16	GND	Ground		
19 GND Ground 20 NC No connection 21 NC No connection 22 GND Ground 23 NC No connection 24 NC No connection 25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No Connect	17	CLK-	-LVDS differential clock input	Negative	
20 NC No connection 21 NC No connection 22 GND Ground 23 NC No connection 24 NC No connection 25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No Connect	18	CLK+	+LVDS differential clock input	Positive	
21 NC No connection 22 GND Ground 23 NC No connection 24 NC No connection 25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No Connect	19	GND	Ground		
22 GND Ground 23 NC No connection 24 NC No connection 25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No Connect	20	NC	No connection		
23 NC No connection 24 NC No connection 25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No Connect	21	NC	No connection		
24 NC No connection 25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No Connect	22	GND	Ground		
25 GND Ground 26 NC No connection 27 NC No connection 28 GND Ground 29 NC No Connect	23	NC	No connection		
26NCNo connection27NCNo connection28GNDGround29NCNo Connect	24	NC	No connection		
27NCNo connection28GNDGround29NCNo Connect	25	GND	Ground		
28 GND Ground 29 NC No Connect	26	NC	No connection		
29 NC No Connect	27	NC	No connection		
	28	GND	Ground		
30 NC No Connect	29	NC	No Connect		
	30	NC	No Connect		

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No.	Symbol	Function	Polarity	Remarks
31	VSSLED	Ground – LED		
32	VSSLED	Ground – LED		
33	VSSLED	Ground – LED		
34	NC	No Connect		
35	PWM	System PWM Signal Input (+3.3V Swing)		
36	LED_EN	LED enable pin (+3.3V Input)		
37	NC	No Connect		
38	VDDLED	LED power		
39	VDDLED	LED power		
40	VDDLED	LED power		

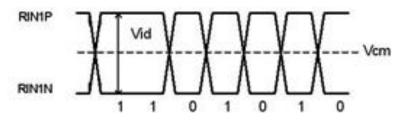
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5.2 LVDS Interface

5.2.1 LVDS DC Input

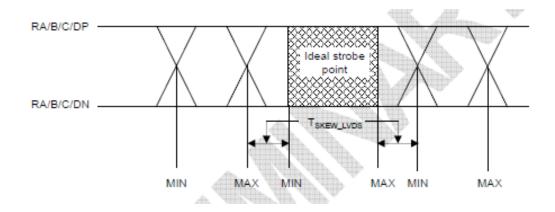
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
LVDS Differential Voltage	VID	200	ı	600	mV	
Input Common Mode Voltage	V_{CM}	0.4	1.2	1.7	V	



5.2.1 LVDS AC Input

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
LVDS input Clock Frequency		F _{CLK_LVDS}	30		100	Mhz	
LVDS RX skew Right margin	100MHz		I	-	270	ps	(1),(2)
	50MHz	T _{RSRM} -	1	_	700	ps	(1),(2)
LVDS RX skew Left margin	100MHz		-270	_	1	ps	(1),(2)
	50MHz		-700	-	ı	ps	(1),(2)
Maximum deviation of LVDS input clock during SSCG		F _{CLK_DEV}	I	_	± 3	%	(3)
Modulating frequency of LVDS input clock during SSCG		F _{CLK_MOD}	30	_	300	KHz	(3)

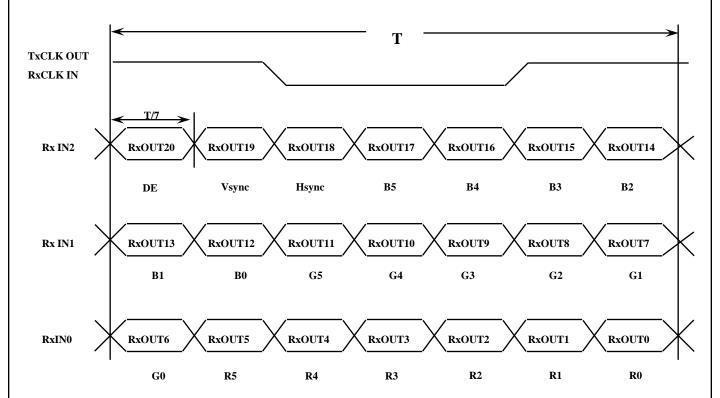
Note (1): LVDS Receiver Skew (Strobe) Margin



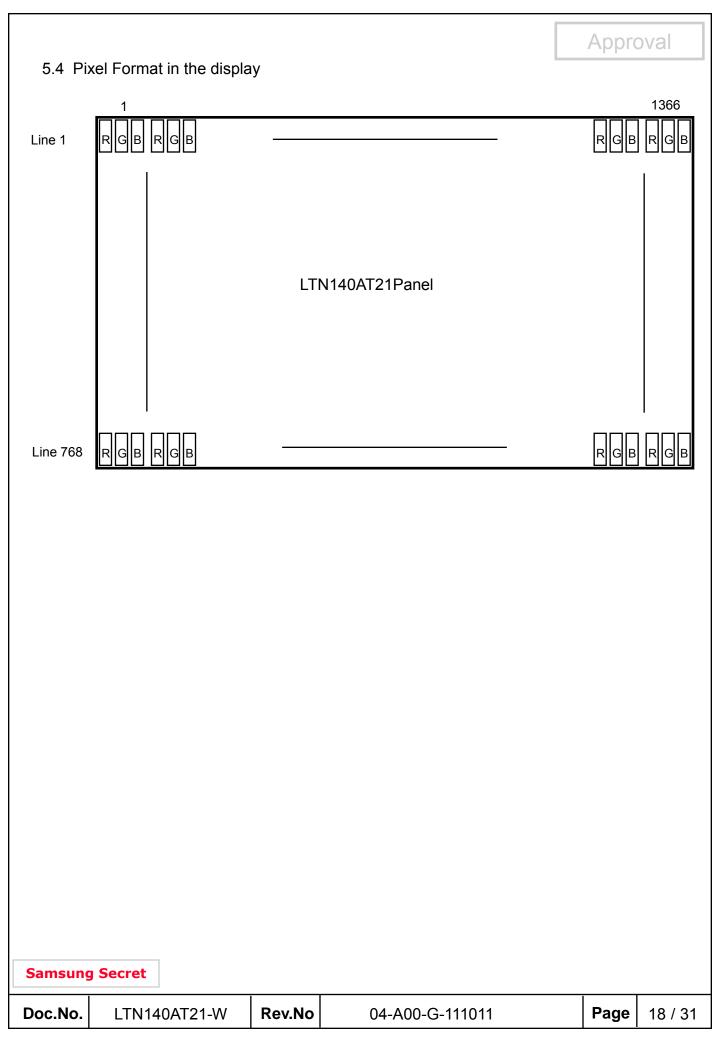
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5.3 Timing Diagrams of LVDS For Transmission

LVDS Receiver : Integrated T-con



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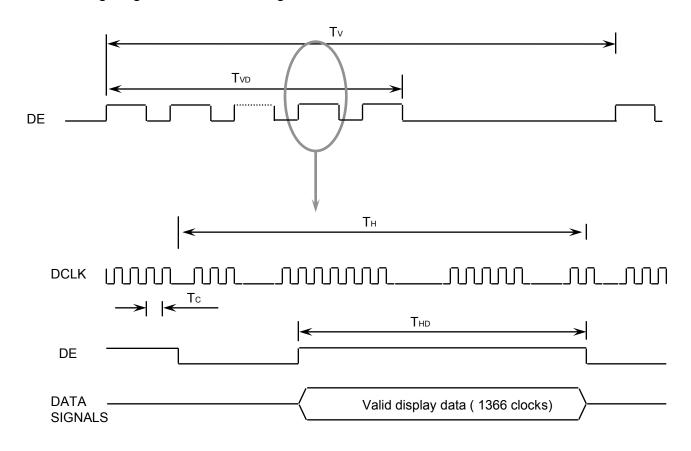


6. INTERFACE TIMING

6.1 Timing Parameters

Signal	Item	Symbol	Min.	Тур.	Max.	Unit	Note
Frame Frequency	Cycle	TV	780	790	980	Lines	
Vertical Active Display Term	Display Period	TVD	1	768	1	Lines	
One Line Scanning Time	Cycle	TH	1440	1526	1800	Clocks	
Horizontal Active Display Term	Display Period	THD	-	1366	-	Clocks	

6.2 Timing diagrams of interface signal

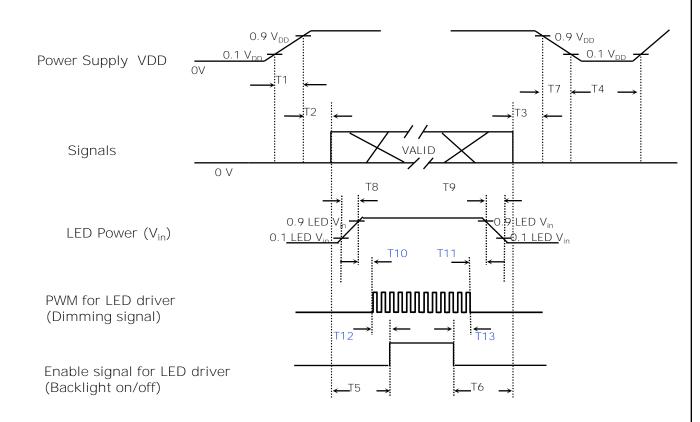


S	a	m	S	ur	ng	S	e	cr	et	t
					_					

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6.3 Power ON/OFF Sequence

: To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Timing (ms)	Remarks
0.5 < T1≤10	V _{DD} rising time from 10% to 90%
0 <t2 <b="">≤50</t2>	Delay from V _{DD} to valid data at power ON
0 <t3 <b="">≤50</t3>	Delay from valid data OFF to V _{DD} OFF at power Off
500 ≤T4	V _{DD} OFF time for Windows restart
300 ≤T5	Delay from valid data to B/L enable at power ON
200 ≤T6	Delay from valid data off to B/L disable at power Off
0 <t7 <b="">≤10</t7>	V _{DD} falling time from 90% to 10%
0.5 < T8≤10	LED V _{in} rising time from 10% to 90%
0.5 < T9≤10	LED V _{in} falling time from 90% to 10%
0 ≤T10	Delay from LED driver Vin rising time 90% to PWM ON
0≤T11	Delay from PWM Off to LED driver Vin falling time 10%, Must Keep rule
0≤T12	Delay from PWM ON to B/L Enable ON, Must Keep rule
0 ≤T13	Delay from B/L Enable Off to PWM Off

Power Sequence & Timing Parameters

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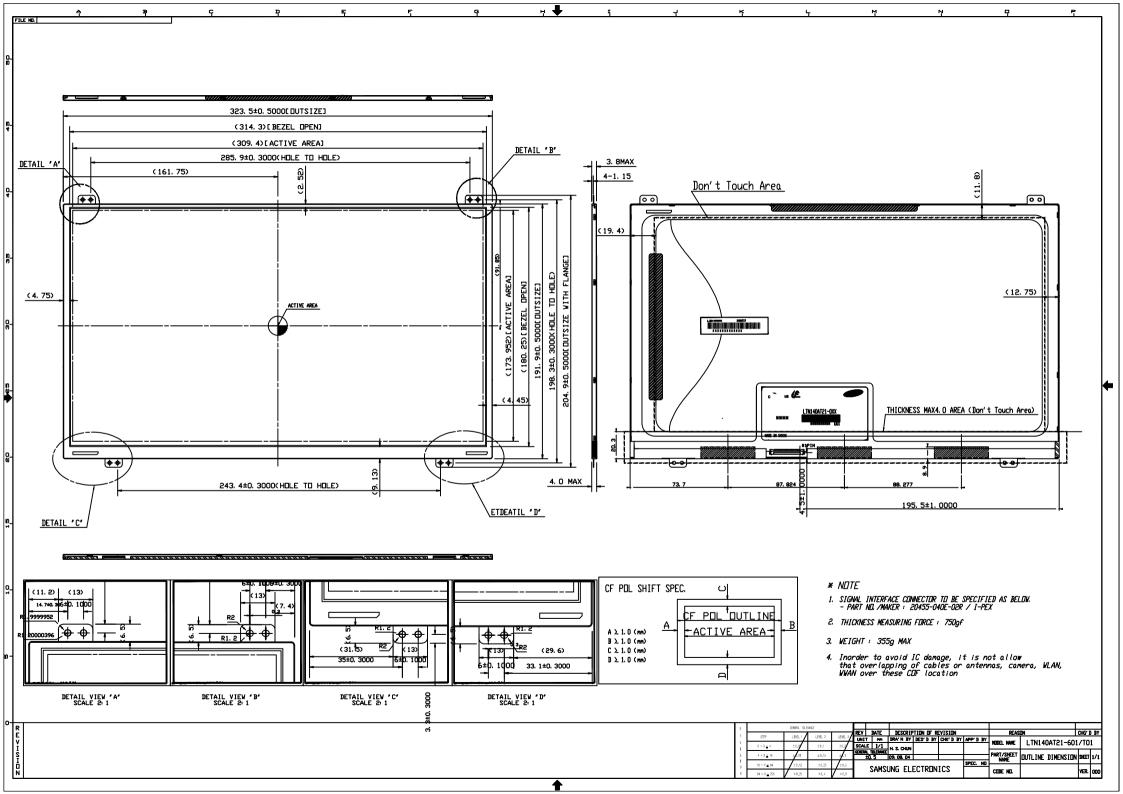
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6.3 Power ON/OFF Sequence

NOTE.

- (1) The supply voltage of the external system for the module input should be the same as the definition of VDD.
- (2) Apply the lamp voltage within the LCD operation range. When the back-light turns on before the LCD operation or the LCD turns off before the back-light turns off, the display may momentarily become white.
- (3) In case of VDD = off level, please keep the level of input signals on the low or keep a high impedance.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

7. Mechai	nical Outline Dimens	sion		Appro	oval
Refer to	the next page				
Samsung	Secret				
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- 1. CARTON(Internal Package)
 - (1) Packing Form
 Corrugated fiberboard box and corrupad form as shock absorber
 - (2) Packing Method



Note 1)Total Weight: Approximately 15.4 kg 2) Acceptance number of piling: 36 sets 3) Carton size: 373(W) × 410(D) × 239(H)

(3)Packing Material

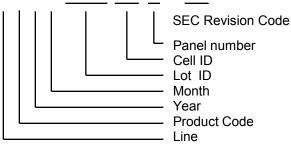
No	Part name	Quantity
1	Static electric protective sack	36
2	Trap (inner Box)	9
3	Rib	10
4	Carton	1 set

9. MARKINGS & OTHERS

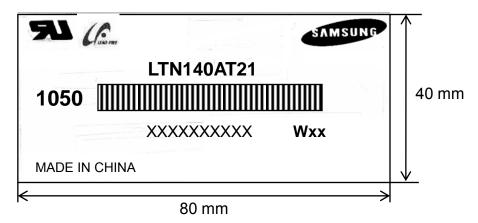
A nameplate bearing followed by is affixed to a shipped product at the specified location on each product.

(1)Parts number: LTN140AT21

(2)Revision code: 3 letters



(5) Nameplate Indication



Parts name : LTN140AT21
Lot number : XXXXXXXXXX

Inspected work week : 1050(2010 year, 50nd week)

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High voltage caution label



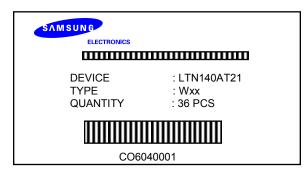
HIGH VOLTAGE CAUTION

RISK OF ELECTRIC SHOCK DISCONNECT THE ELECTRIC POWER BEFORE SERVICE THIS COVER CONTAINS
FLUORESCENT LAMP.
PLEASE FOLLOW LOCAL
ORDINANCES OR
REGULATIONS FOR ITS DISPOSAL

10mm High voltage caution

70mm

(6) Packing small box attach



10. GENERAL PRECAUTIONS

1. Handling

- (a) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist and bend the modules.
- (b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and CCFT back-light.
- (c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.
- (d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.
- (e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (f) The desirable cleaners are water, IPA (Isoprophyl Alcohol) or Hexane.

 Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
- (h) Protect the module from static, it may cause damage to the C-MOS Gate Array IC.
- (i) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (j) Do not disassemble the module.
- (k) Do not pull or fold the lamp wire.
- (I) Do not adjust the variable resistor which is located on the back side.
- (m) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (n) Pins of I/F connector shall not be touched directly with bare hands.

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2. STORAGE

- (a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 5 to 40 °C and relative humidity of less than 70%.
- (b) Do not store the TFT-LCD module under the direct sunlight.
- (c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during storage.
- (d) Storage period is recommended not to exceed 1 year.

3. OPERATION

- (a) Do not connect, disconnect the module in the "Power On" condition.
- (b) Power supply should always be turned on/off by following item 6.3 "Power on/off sequence ".
- (c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (d) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, SEC is not to be held reliable for the defective operations. It is strongly recommended to contact SEC to find out fitness for a particular purpose.

4 OTHERS

- (a) Ultra-violet ray filter is necessary for outdoor operation.
- (b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.
- (c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.
- (d) If the module displays the same pattern continuously for a long period of time, it can be the situation when the image "sticks" to the screen.
- (e) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

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Approval

Address		Value			ASCII	
	FUNCTION	***************************************	BIN	DEC	or	Notes
(HEX)		HEX			Data	
00		00	00000000	0		
01		FF	11111111	255		
02		FF	11111111	255		
03	Header	FF	11111111	255		EDID Header
04	rieadei	FF	11111111	255		LDID Headel
05		FF	11111111	255		
06		FF	11111111	255		
07		00	00000000	0		
08		4C	01001100	76	S	3 character ID
_	ID Manufacturer Name				E	
09		A3	10100011	163	С	"SEC"
0A	ID Product Code	49	01001001	73	[1]	
0B	.2	36	00110110	54	[6]	
0C		00	00000000	0		
0D	32-bit serial no.	00	00000000	0		
0E		00	00000000	0		
0F		00	00000000	0		
10	Week of manufacture	00	00000000	0		
11	Year of manufacture	15	00010101	21	2011	2011
12	EDID Structure Ver.	01	00000001	1	1	EDID Ver. 1.0
13	EDID revision #	03	00000011	3	3	EDID Rev. 3
14	Video input definition	80	10000000	128		
15	Max H image size	1F	00011111	31	31	31 cm(approx)
16	Max V image size	11	00010001	17	17	17 cm(approx)
17	Display Gamma	78	01111000	120	2.2	Gamma 2.2
18	Feature support	0A	00001010	10		
19	Red/green low bits	E3	11100011	227		10000111
1A	Blue/white low bits	F5	11110101	245		11111110
1B	Red x/ high bits	90	10010000	144	0.565	Red x 0.615=
						1001010010
1C	Red y	59	01011001	89	0.350	Red y 0.325=
						0101011100
1D	Green x	57	01010111	87	0.340	Green x 0.300=
						0100111101
1E	Green y	90	10010000	144	0.565	Green y 0.570=
		_				1000110011
1F	Blue x	27	00100111	39	0.155	Blue x 0.145=
		_			0.100	001001111
20	Blue y	1E	00011110	30	0.120	Blue y 0.080=
					0.010	001001111
21	White x	50	01010000	80	0.313	White x 0.313= 0101000001
					0.000	
22	White y	54	01010100	84	0.329	White y 0.329= 0101010001
	Established timing 4	- 00	00000000			0101010001
23	Established timing 1 Established timing 2	00	00000000	0		
24	Ÿ	00	00000000			
25	Established timing 3	00	00000000	0	<u> </u>	
26	Standard timing #1	01	00000001	1		not used
27 28		01	00000001 00000001	1		
28	Standard timing #2	01	00000001	1		not used
	1	U 01	00000001	1		

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2A	Standard timing #2	01	00000001	1		notuced
2B	Standard timing #3	01	00000001	1		not used
2C	Standard timing #4	01	00000001	1		not used
2D	Standard tilling #4	01	00000001	1		Hot useu
2E	Standard timing #5	01	00000001	1		not used
2F	Standard timing #5	01	00000001	1		not used
30	Standard timing #6	01	00000001	1		notuced
31	Standard timing #6	01	00000001	1		not used
32	Standard timing #7	01	00000001	1		not used
33	Standard tilling #7	01	00000001	1		not used
34	Standard timing #8	01	00000001	1		not used
35	Standard timing #6	01	00000001	1		Hot used
36		9E	10011110	158	70.7	Main alore 70 44 MHz
37		1B	00011011	27		Main clock= 70.44 MHz
38	•	56	01010110	86	1366	Hor active=1366 pixels
39	•	78	01111000	120	120	Hor blanking=160 pixels
3A	•	50	01010000	80	120	4bit : 4bit
3B		00	00000000	0	768	Vertcal active=768 lines
3C	•	18	00011000	24	24	Vertical blanking=22 lines
3D	•	30	00110000	48	27	4bit : 4bit
3E		30	00110000	48	48	
3F	Detailed timing/monitor	20	00100000	32	32	H sync. Width=32 pixels
	descriptor #1				2	V sync. Offset=2 lines
40		25	00100101	37	5	V sync. Width=5 lines
41		00	00000000	0		2bit : 2bit :2bit :2bit
42		35	00110101	53	309	H image size= 309 mm(approx)
43		AE	10101110	174	174	V image size = 173 mm(approx)
44		10	00010000	16		
45		00	00000000	0		No Horizontal Border
46		00	00000000	0		No Vertical Border
47		19	00011001	25		
48		00	00000000	0		
49		00	00000000	0		
4A		00	00000000	0		Manufacturer Specified (Timing)
4B		0F	00001111	15		5,
4C		00	00000000	0		
						Value=HCDWm:= / 2
4D	-	00	00000000	0		Value=HSPWmin / 2
4E	Detailed timing/manita-	00	00000000	0		Value=HSPWmax / 2
4F 50	Detailed timing/monitor	00	00000000	0	-	Value=Thbpmin /2 Value=Thbpmax /2
50	descriptor #2	00	00000000	0		Value=Inopmax/2 Value=VSPWmin /2
52	1	00	00000000	0		Value=VSPWmin/2 Value=VSPWmax/2
53	1	00	00000000	0		Value=Tvbpmin / 2
54		00	00000000	0		Value=Tvbpmax/2
55		1E	00011110	30		Thpmin=value*2 + HA pixelclks
56	1	B4	10110100	180		Thpmin-value 2 + HA pixelciks Thpmax=value*2 + HA pixelciks
57	1	02	00000010	2		Typmin=value*2 + VA lines
58	1	74	01110100	116		Tvpmax=value*2 + VAlines
59	1	00	00000000	0		Module revision
Jä		00	00000000			Wodule levision

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5A		00	00000000	0		
5B		00	00000000	0		
5C		00	00000000	0		ASCII Data String Tag
5D		FE	11111110	254		
5E		00	00000000	0		
5F		53	01010011	83	[S]	
60		41	01000001	65	[A]	
61	Detailed timing/monitor	4D	01001101	77	[M]	
62	descriptor #3	53	01010011	83	[S]	
63	·	55	01010101	85	[U]	
64		4E	01001110	78	[N]	
65		47	01000111	71	[G]	
66		0A	00001010	10	[^]	
67		20	00100000	32	[]	
68		20	00100000	32	[]	
69		20	00100000	32	[]	
6A		20	00100000	32	[]	
6B		20	00100000	32	[]	
6C		00	00000000	0		
6D		00	00000000	0		
6E		00	00000000	0		Monitor Name Tag (ASCII)
6F		FE	11111110	254		
70		00	00000000	0		
71		4C	01001100	76	[L]	
72		54	01010100	84	[T]	
73	Detailed timing/monitor	4E	01001110	78	[N]	
74	descriptor #4	31	00110001	49	[1]	
75		34	00110100	52	[4]	
76		30	00110000	48	[0]	
77		41	01000001	65	[A]	
78		54	01010100	84	[T]	
79		32	00110010	50	[2]	
7A		31	00110001	49	[1]	
7B		30	00110000	48	[0]	
7C		0A	00001010	10	[*]	
7D		20	00100000	32	[*]	
7E	Extension Flag	00	00000000	0		
7F	Checksum	1C	00011100	28		

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