




Product Specification

AU OPTRONICS CORPORATION

() Preliminary Specifications

(V) Final Specifications

Module	10.1”(10.1”) WXGA 16:10 Color TFT-LCD with LED Backlight design
Model Name	B101EVN05 (H/W: 3A ; DP/N: 0MGHVW)
Note 	<i>LED Backlight with driving circuit design</i> ✓ <i>Color Management (Virtual and Rich Color Solution)</i> ✓ <i>Dynamic Contrast Ratio (Power Saving Solution)</i>

Customer

Date

Checked &
Approved by

Date

Note: This Specification is subject to change
without notice.

Approved by

Date

Ivan Wu

2/6/2012

Prepared by

Jay SC Lin

2/6/2012

NBBU Marketing Division
AU Optronics corporation



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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2012/02/06	All	First Edition for Customer		



1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



2. General Description

B101EW05 V4 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 WXGA, 1280(H) x800(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. In terms of technology side, the module utilizes Amorphous-Silicon process (A-Si) and features with Multi-Domain Vertical Alignment (MVA). All input signals are LVDS interface compatible.

B101EW05 V4 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	255.85 (10.1W")			
Active Area	[mm]	216.96(H) x 135.6(V)			
Pixels H x V		1280 x 3(RGB) x 800			
Pixel Pitch	[mm]	0.1695 X 0.1695			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (ILED=22mA) (Note: ILED is LED current)	[cd/m ²]	Base panel level: 400 typ. (5 points average) 340 min. (5 points average) Total solution level 340 typ (5 points average) 290 min (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		1300 typ, 1000 min.			
Response Time	[ms]	25 typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.2 max. (Logic 0.7W and Blu power 3.1W, TP 0.4W)			
Weight	[Grams]	180 max.(Panel only)			
		336 max (total solution)			
Physical Size (panel only) without bracket	[mm]		Min.	Typ.	Max.
		Length	229.16	229.66	230.16
		Width	148.9	149.4	149.9
		Thickness	---	---	5.6
		Thickness	---	---	7.4
Electrical Interface		1 channel LVDS			



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Glass Thickness	[mm]	0.3
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

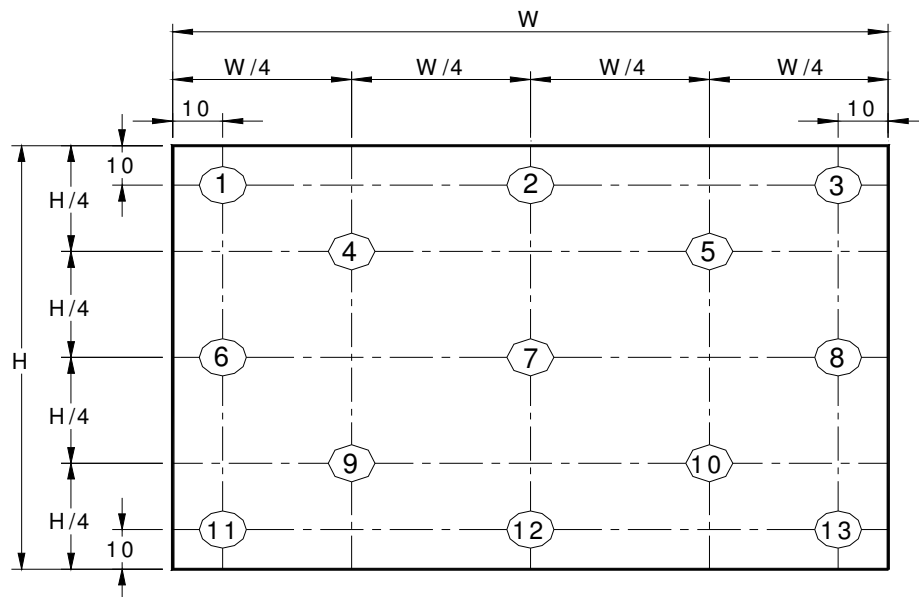
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I _{LED} =22mA		5 points average	290	340	---	cd/m²	1, 4, 5.
Viewing Angle	θ_R	Horizontal (Right) CR = 10 (Left)	80	85	---	degree	4, 9
	θ_L		80	85	---		
	ψ_H	Vertical (Upper) CR = 10 (Lower)	80	85	---		
	ψ_L		80	85	---		
Luminance Uniformity	δ_{5P}	5 Points	---	---	1.25		1, 3, 4
Luminance Uniformity	δ_{13P}	13 Points	---	---	1.50		2, 3, 4
Contrast Ratio	CR		1000	1300	-		4, 6
Cross talk	%		---	---	4		4, 7
Response Time	T_{RT}	Rising + Falling	---	25	35	msec	4, 8
Color / Chromaticity Coordinates	Red	R_x	0.549	0.579	0.609		4
		R_y	0.308	0.338	0.368		
	Green	G_x	0.295	0.325	0.355		
		G_y	0.530	0.560	0.590		
	Blue	B_x	0.132	0.152	0.182		
		B_y	0.095	0.125	0.155		
	White	W_x	0.283	0.313	0.343		
		W_y	0.299	0.329	0.359		
	NTSC	%	-	45	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

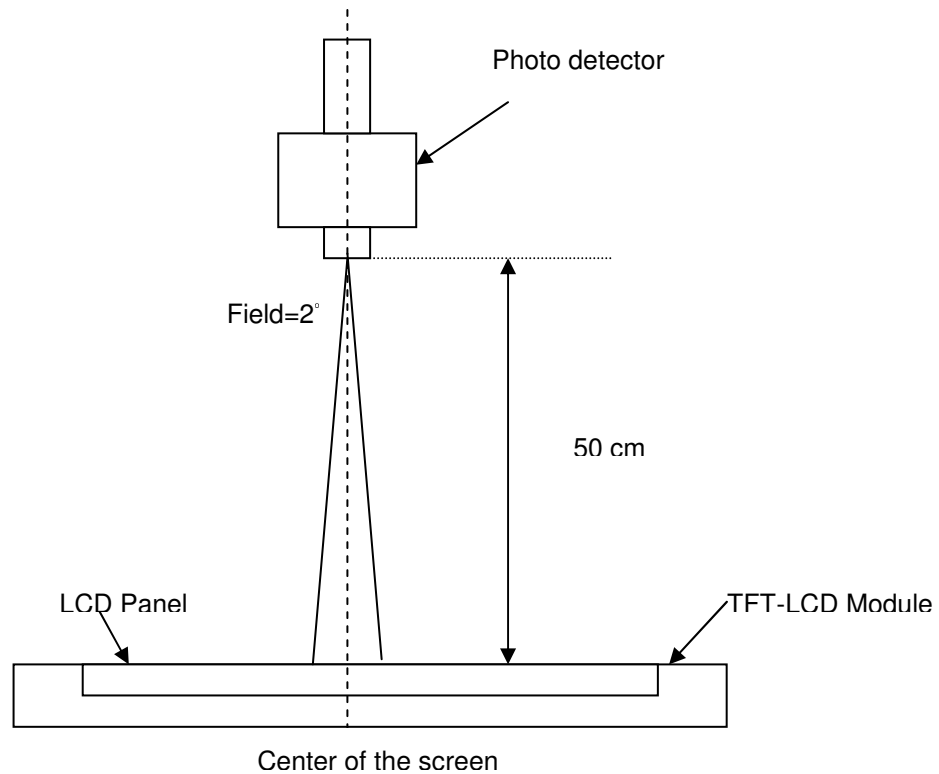
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



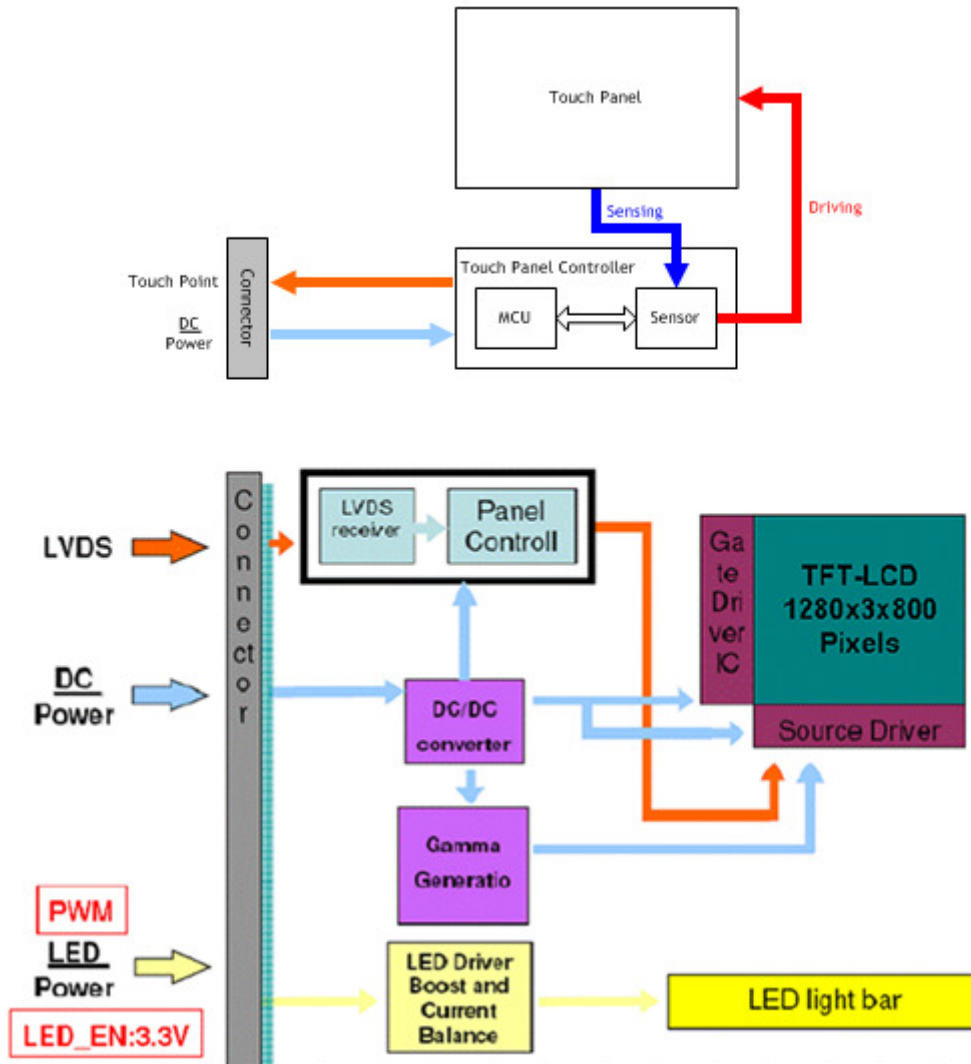
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (ϕ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 40 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

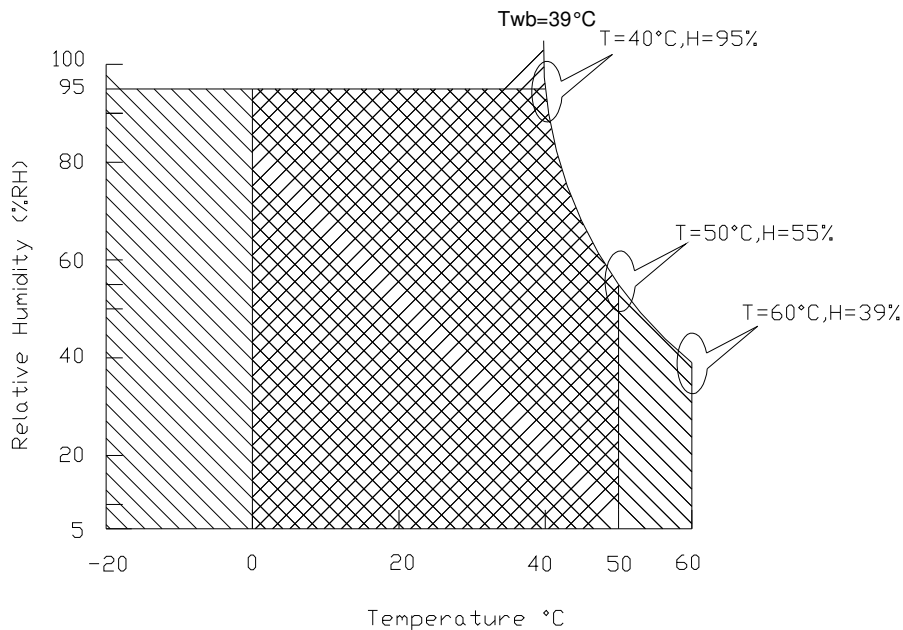
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

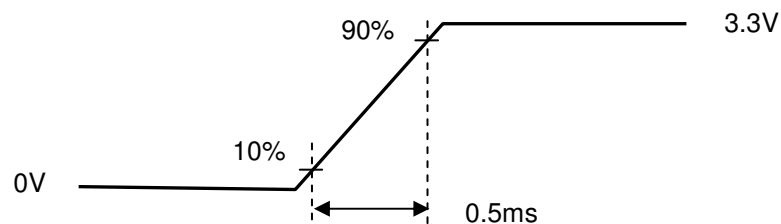
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.7	[Watt]	Note 1
IDD	IDD Current	-	-	212	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2 : Measure Condition



Vin rising time

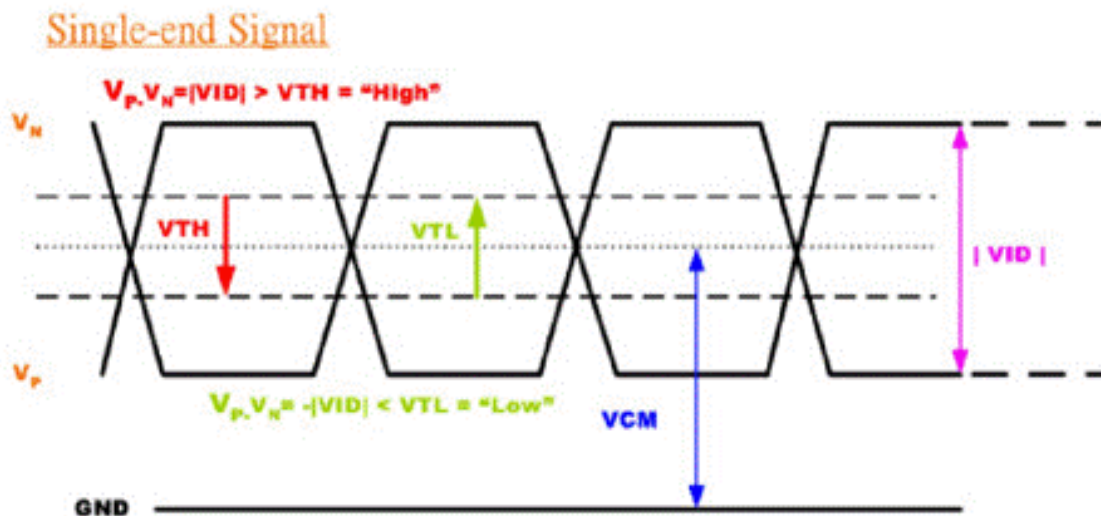
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{TH}	Differential Input High Threshold ($V_{cm}=+1.2V$)	---	100	[mV]
V_{TL}	Differential Input Low Threshold ($V_{cm}=+1.2V$)	-100	----	[mV]
$ V_{ID} $	Differential Input Voltage	100	600	[mV]
V_{CM}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	3.1	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 If=19mA

Note 1: Calculator value for reference $P_{LED} = V_F \text{ (Normal Distribution)} * I_F \text{ (Normal Distribution)} / \text{Efficiency}$

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

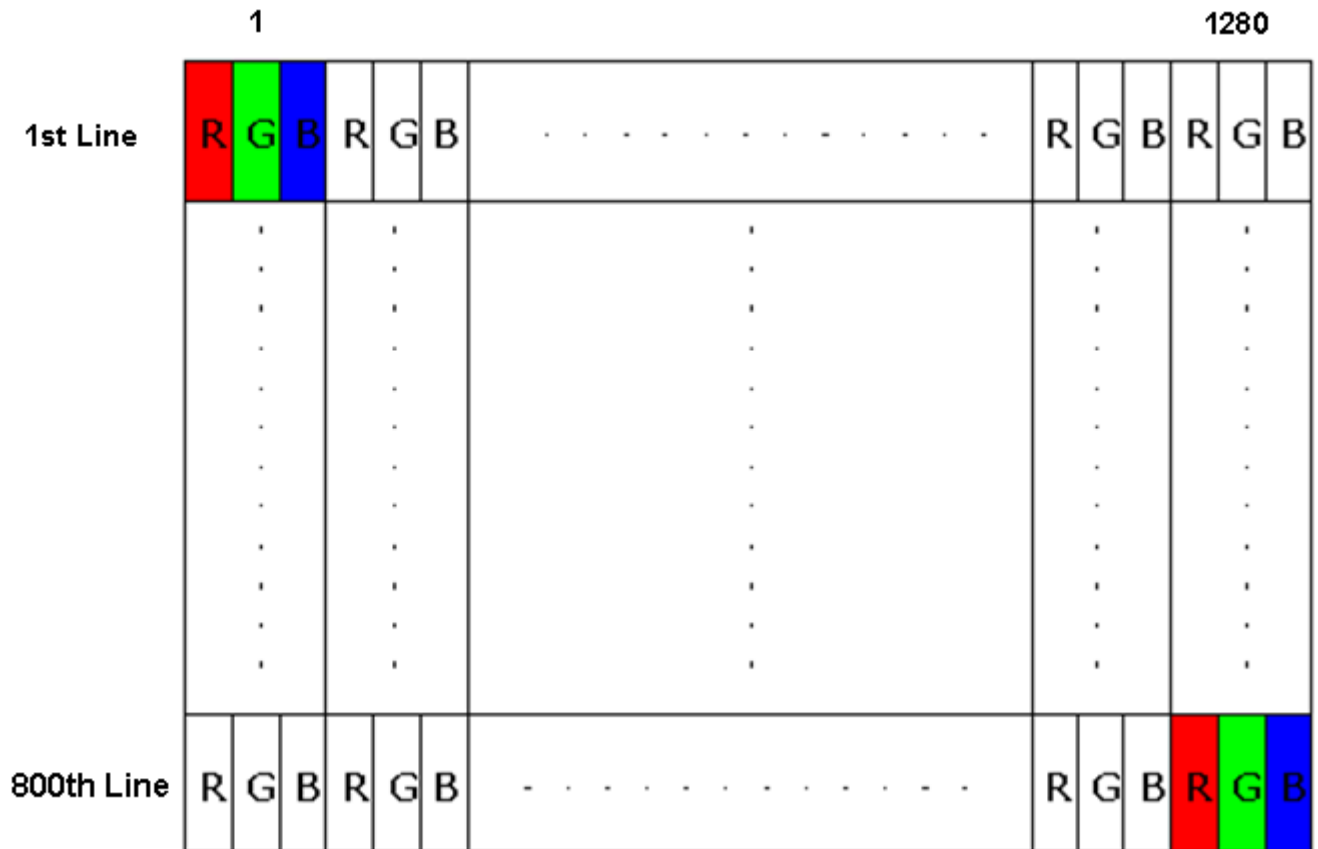
5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.5	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	200	-	20K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 LVDS Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or Compatible
Type / Part Number	JAE HD1S040HA1 or Compatible
Mating Housing/Part Number	IPEX 20453-040T-11or Compatible

6.3.2 LVDS Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	NC	No Connection (Reserve)
2	AVDD	Power Supply +3.3V
3	AVDD	Power Supply +3.3V
4	VEDID	EDID +3.3V Power
5	Aging	BIST Mode
6	CLK_EDID	EDID Clock Input
7	DAT_EDID	EDID Data Input
8	Rin0-	-LVDSdifferential data input(R0-R5,G0)
9	Rin0+	+LVDSdifferential data input(R0-R5,G0)
10	GND	Ground
11	Rin1-	-LVDSdifferential data input(G1-G5,B0-B1)
12	Rin1+	+LVDSdifferential data input(G1-G5,B0-B1)
13	GND	Ground
14	Rin2-	-LVDSdifferential data input(B2-B5,HS,VS,DE)
15	Rin2+	+LVDSdifferential data input(B2-B5,HS,VS,DE)
16	GND	Ground
17	ClkIN-	-LVDSdifferential clock input
18	ClkIN+	+LVDSdifferential clock input
19	GND	Ground–Shield
20	NC	No Connection (Reserve)
21	NC	No Connection (Reserve)
22	GND	Ground–Shield
23	NC	No Connection (Reserve)



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24	NC	No Connection (Reserve)
25	GND	Ground–Shield
26	NC	No Connection (Reserve)
27	NC	No Connection (Reserve)
28	GND	Ground–Shield
29	NC	No Connection (Reserve)
30	NC	No Connection (Reserve)
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection (Reserve)
35	VPWM_EN	System PWM Logic Input Level
36	VLED_EN	LED enable input level
37	DCR_EN	No Connection (Reserve)
38	VLED	LED Power Supply
39	VLED	LED Power Supply
40	VLED	LED Power Supply

6.4 LVDS Interface Timing

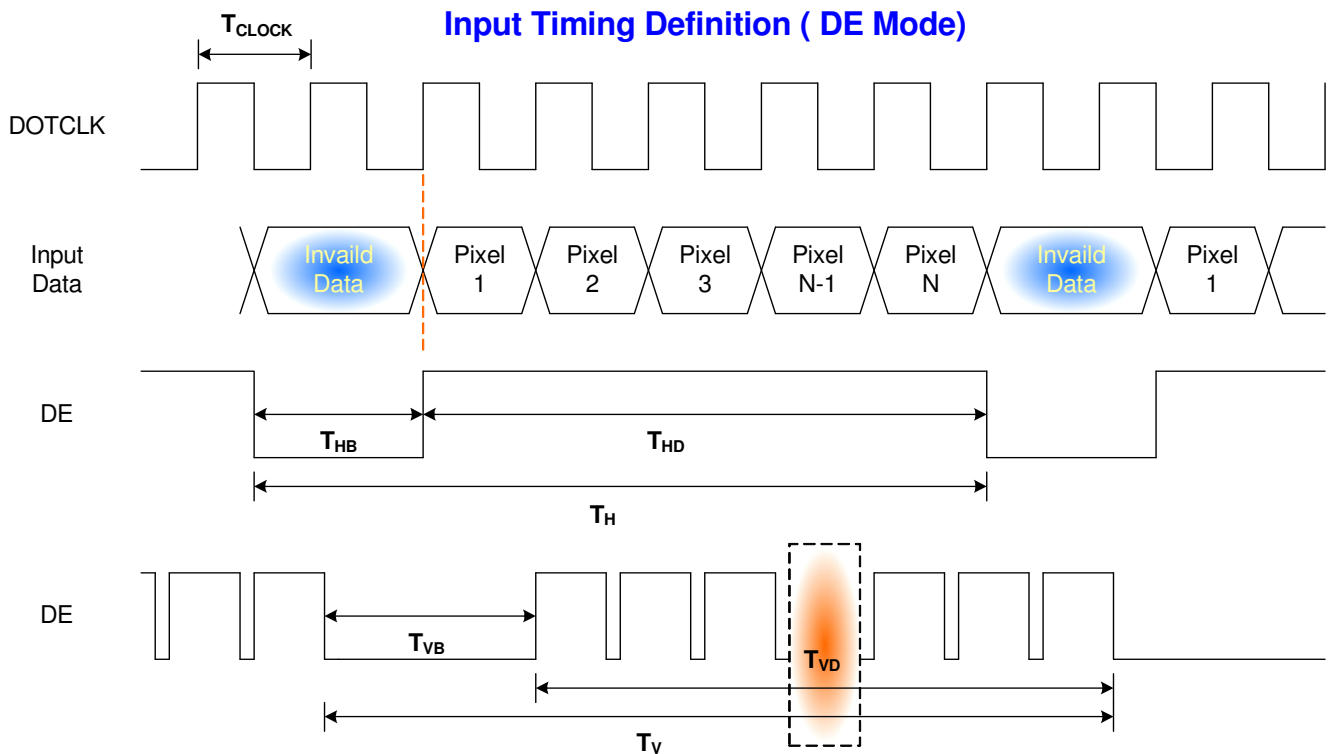
6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T _{Clock}	64	68.93	85	MHz
Vertical Section	Period	T _V	808	816	1023	T _{Line}
	Active	T _{VD}	800			
	Blanking	T _{VB}	8	16	223	
Horizontal Section	Period	T _H	1310	1408	2047	T _{Clock}
	Active	T _{HD}	1280			
	Blanking	T _{HB}	40	168	767	

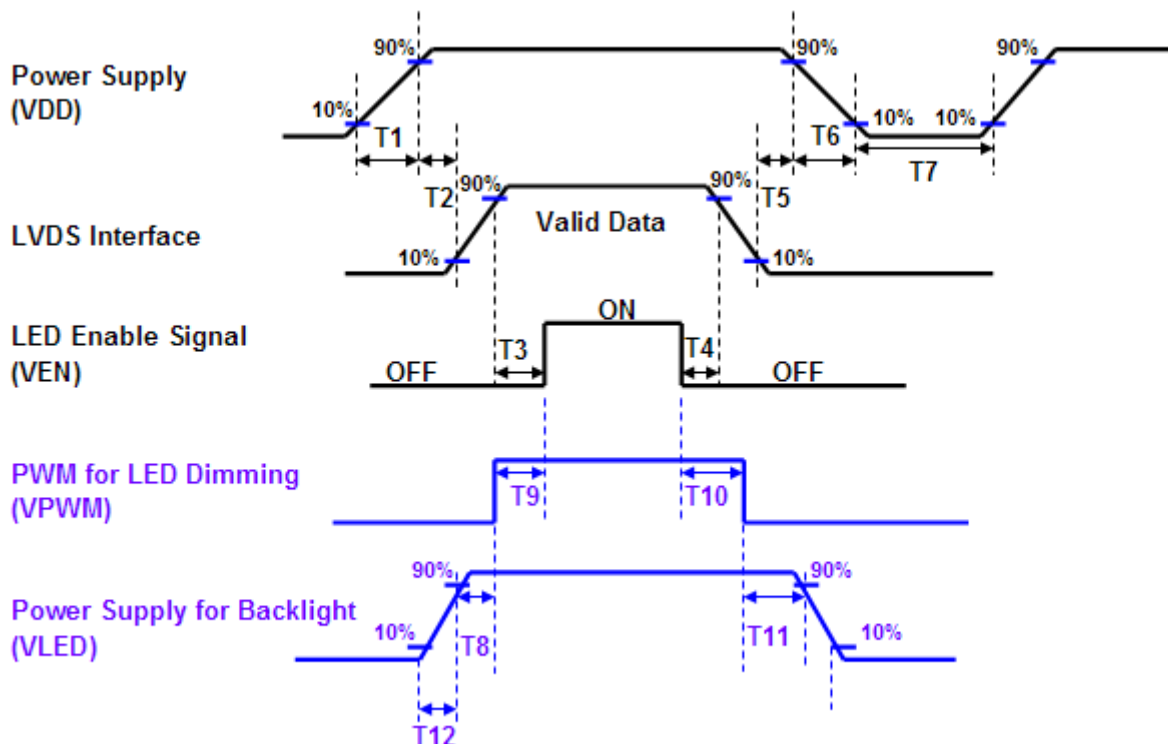
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Power Sequence Timing			
Parameter	Value		Units
	Min.	Max.	
T1	0.5	10	ms
T2	0	50	
T3	200	-	
T4	200	-	
T5	0	50	
T6	0	10	
T7	500	-	
T8	10	-	
T9	0	180	
T10	0	180	
T11	10	-	
T12	0.5	10	

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

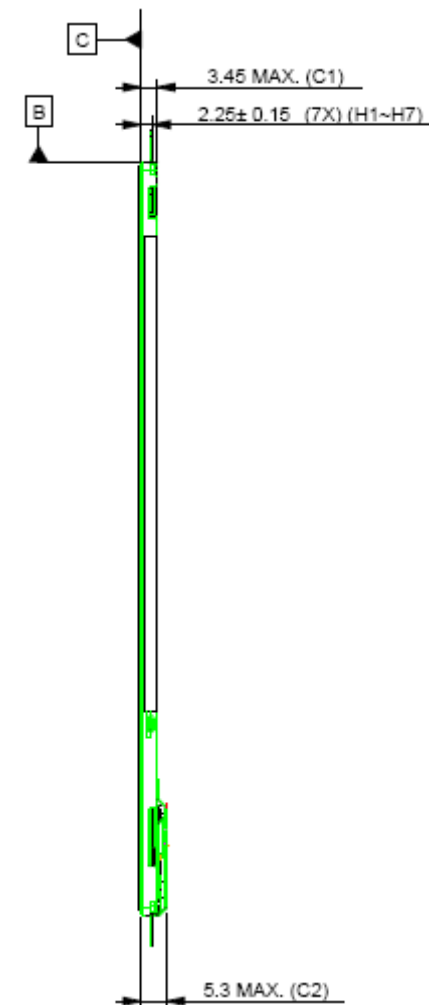
7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 35%RH, 300h	
Low Temperature Storage	Ta= -40°C, 50%RH, 250h	
Thermal Shock Test	Ta=-40°C to 65°C, Duration at 20 min, 50 cycles	

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

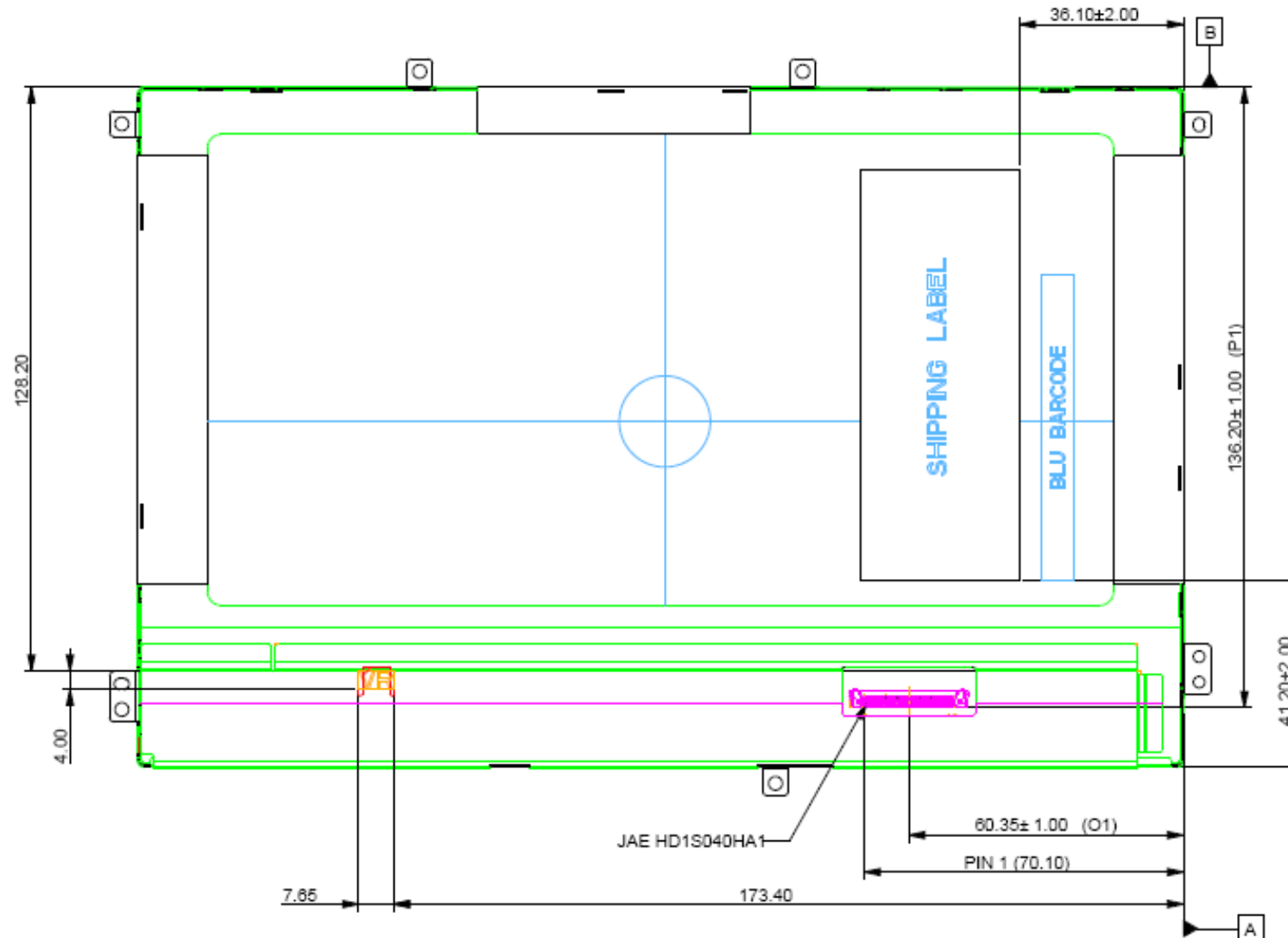
The above test criteria are for panel alone; regarding to the system RA test please refer to “**MPG/SVDC LCD Display and Touch Panel Solution Cosmetic and Quality Specification v03**” document.

8.1.1 Standard Front View



8.1.2 Standard Rear View & Key components remark and remind

Prevention damage the IC, connector, Capacitor...., we recommend your design remarked at this drawing.










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9. Shipping and Package

9.1 Shipping Label Format

Shipping label

 XXXXXXXXXXXX-XXXXX	Manufactured YY/WW Model No: B101EVN05.0 AU Optronics MADE IN CHINA (S01) H/W: 3A F/W:0	C  US E204356	  
---	--	---	---

Carton label

AU Optronics	QTY : 40		
MODEL NO :B101EVN05.0			
PART NO : 97.10B34.013			
CUSTOMER NO :			
CARTON NO :			
Made in China	*ZM100-0652300205*		



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10. Appendix

10.1 EDID Description

Byte	Field Name and Comments	Value	Value	Value
(hex)		(hex)	(binary)	(DEC)
0	Header	00	00000000	0
1	Header	FF	11111111	255
2	Header	FF	11111111	255
3	Header	FF	11111111	255
4	Header	FF	11111111	255
5	Header	FF	11111111	255
6	Header	FF	11111111	255
7	Header	00	00000000	0
8	EISA manufacture code = 3 Character ID	06	00000110	6
9	EISA manufacture code (Compressed ASCII)	AF	10101111	175
0A	Panel Supplier Reserved – Product Code	D4	11010100	212
0B	Panel Supplier Reserved – Product Code	54	01010100	84
0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
10	Week of manufacture	00	00000000	0
11	Year of manufacture	15	00010101	21
12	EDID structure version # = 1	01	00000001	1
13	EDID revision # = 4	04	00000100	4
14	Video I/P definition	90	10010000	144
15	Max H image size = ?? cm(Rounded to cm)	16	00010110	22
16	Max V image size = ?? cm(Rounded to cm)	0E	00001110	14
17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78	01111000	120
18	Feature support	02	00000010	2
19	Red/Green Low bit (RxRy/GxGy)	65	01100101	101
1A	Blue/White Low bit (BxBY/WxWy)	05	00000101	5
1B	Red X Rx = 0.???	94	10010100	148
1C	Red Y Ry = 0.???	56	01010110	86
1D	Green X Rx = 0.???	53	01010011	83
1E	Green Y Ry = 0.???	8F	10001111	143
1F	Blue X Rx = 0.???	27	00100111	39
20	Blue Y Ry = 0.???	20	00100000	32
21	White X Rx = 0.???	50	01010000	80
22	White Y Ry = 0.???	54	01010100	84
23	Established timings 1 (00h if not used)	00	00000000	0
24	Established timings 2 (00h if not used)	00	00000000	0
25	Manufacturer's timings (00h if not used)	00	00000000	0
26	Standard timing ID1 (01h if not used)	01	00000001	1
27	Standard timing ID1 (01h if not used)	01	00000001	1
28	Standard timing ID2 (01h if not used)	01	00000001	1
29	Standard timing ID2 (01h if not used)	01	00000001	1



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2A	Standard timing ID3 (01h if not used)	01	00000001	1
2B	Standard timing ID3 (01h if not used)	01	00000001	1
2C	Standard timing ID4 (01h if not used)	01	00000001	1
2D	Standard timing ID4 (01h if not used)	01	00000001	1
2E	Standard timing ID5 (01h if not used)	01	00000001	1
2F	Standard timing ID5 (01h if not used)	01	00000001	1
30	Standard timing ID6 (01h if not used)	01	00000001	1
31	Standard timing ID6 (01h if not used)	01	00000001	1
32	Standard timing ID7 (01h if not used)	01	00000001	1
33	Standard timing ID7 (01h if not used)	01	00000001	1
34	Standard timing ID8 (01h if not used)	01	00000001	1
35	Standard timing ID8 (01h if not used)	01	00000001	1
36	Pixel Clock/10,000 (LSB)	D0	11010000	208
37	Pixel Clock/10,000 (MSB)	1B	00011011	27
38	Horizontal Active = ??? pixels (lower 8 bits)	00	00000000	0
39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	B8	10111000	184
3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000	80
3B	Vertical Active = ??? lines	20	00100000	32
3C	Vertical Blanking (Tvbp) = ?? lines (DE Blanking typ. for DE only panels)	08	00001000	8
3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48
3E	Horizontal Sync, Offset (Thfp) = ?? pixels	08	00001000	8
3F	Horizontal Sync, Pulse Width = ??? pixels	0A	00001010	10
40	Vertical Sync, Offset (Tvfp) = ? lines Sync Width = ? lines	31	00110001	49
41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
42	Horizontal Image Size = ??? mm	D8	11011000	216
43	Vertical image Size = ??? mm	87	10000111	135
44	Horizontal Image Size / Vertical image size	00	00000000	0
45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26
48	Pixel Clock/10,000 (LSB)	D0	11010000	208
49	Pixel Clock/10,000 (MSB)	1B	00011011	27
4A	Horizontal Active = xxxx pixels (lower 8 bits)	00	00000000	0
4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	B8	10111000	184
4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000	80
4D	Vertical Active = xxxx lines	20	00100000	32
4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	08	00001000	8
4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48
50	Horizontal Sync, Offset (Thfp) = xxxx pixels	08	00001000	8
51	Horizontal Sync, Pulse Width = xxxx pixels	0A	00001010	10
52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	31	00110001	49
53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0



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54	Horizontal Image Size =xxx mm	D8	11011000	216
55	Vertical image Size = xxx mm	87	10000111	135
56	Horizontal Image Size / Vertical image size	00	00000000	0
57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26
5A	Flag	00	00000000	0
5B	Flag	00	00000000	0
5C	Flag	00	00000000	0
5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254
5E	Flag	00	00000000	0
5F	Dell P/N 1 st Character	4D	01001101	77
60	Dell P/N 2 nd Character	47	01000111	71
61	Dell P/N 3 rd Character	48	01001000	72
62	Dell P/N 4 th Character	56	01010110	86
63	Dell P/N 5 th Character	57	01010111	87
64	EDID Revision Bit[6:0] See charts below Bit[7] 0: X-rev, 1: A-rev	0A	00001010	10
65	Manufacturer P/N	42	01000010	66
66	Manufacturer P/N	31	00110001	49
67	Manufacturer P/N	30	00110000	48
68	Manufacturer P/N	31	00110001	49
69	Manufacturer P/N	45	01000101	69
6A	Manufacturer P/N	57	01010111	87
6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	35	00110101	53
6C	Flag	00	00000000	0
6D	Flag	00	00000000	0
6E	Flag	00	00000000	0
6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00	00000000	0
70	Flag	00	00000000	0
71	Color Management	00	00000000	0
72	Panel Structure	41	01000001	65
73	Frame Rate	02	00000010	2
74	Light Controller Interface and Luminance	A8	10101000	168
75	Outdoor Features	01	00000001	1
76	Multi-Media Features	00	00000000	0
77	Multi-Media Features	00	00000000	0
78	Special Features #1	00	00000000	0
79	Special Features #2	01	00000001	1
7A	Special Features #3	01	00000001	1
7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10
7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32



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7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0
7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	34	00110100	52

	6656
Sum	1A00