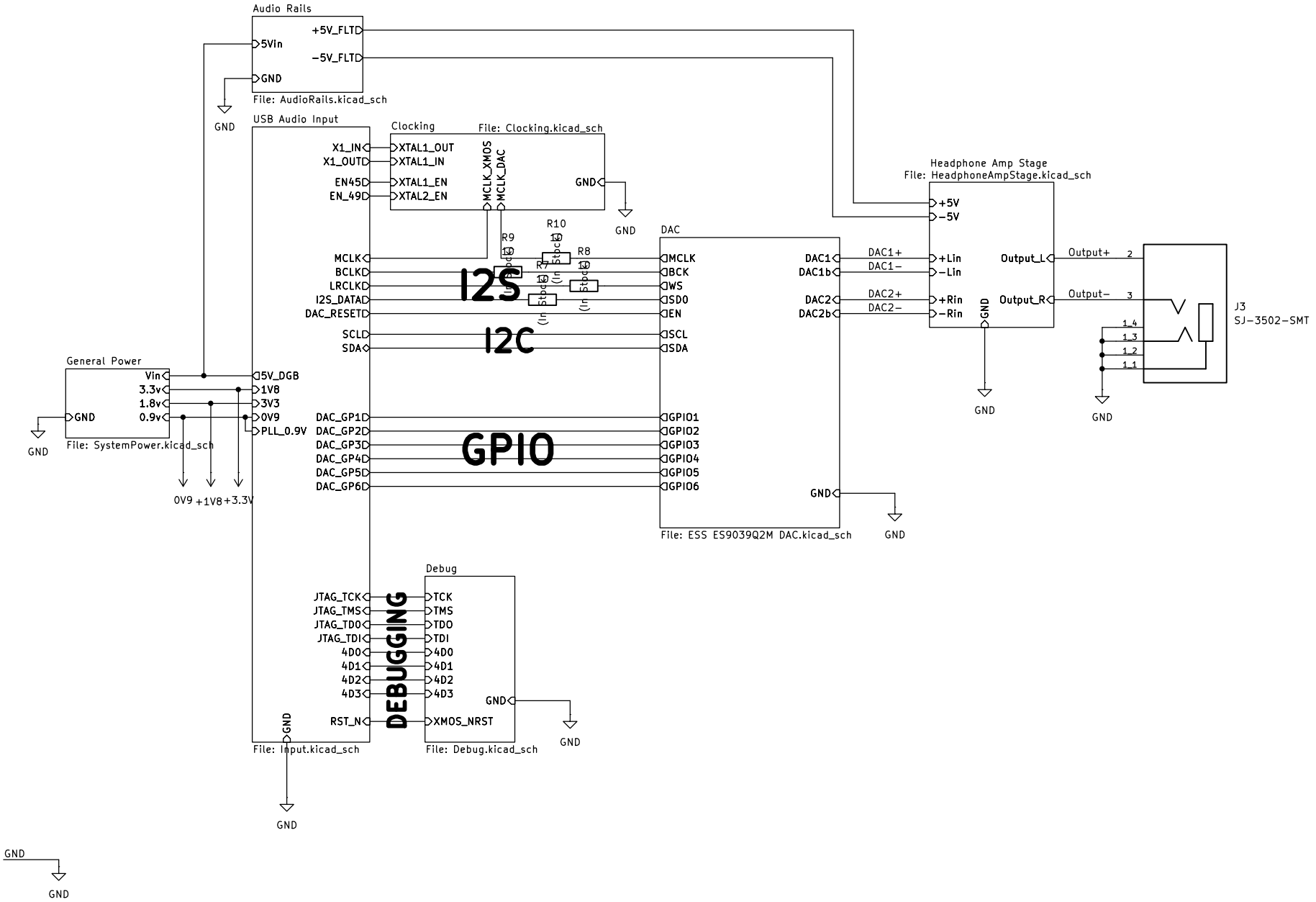
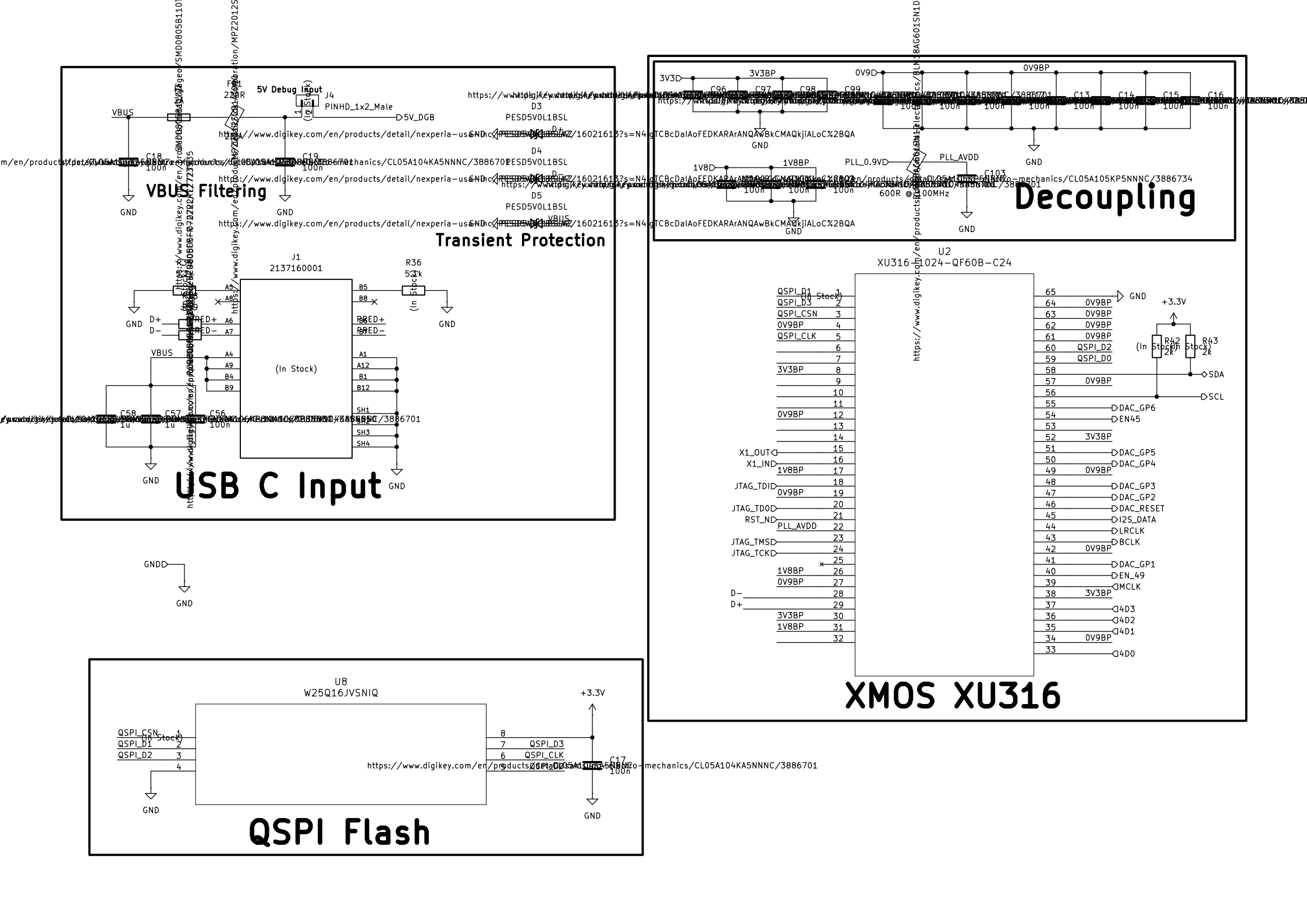
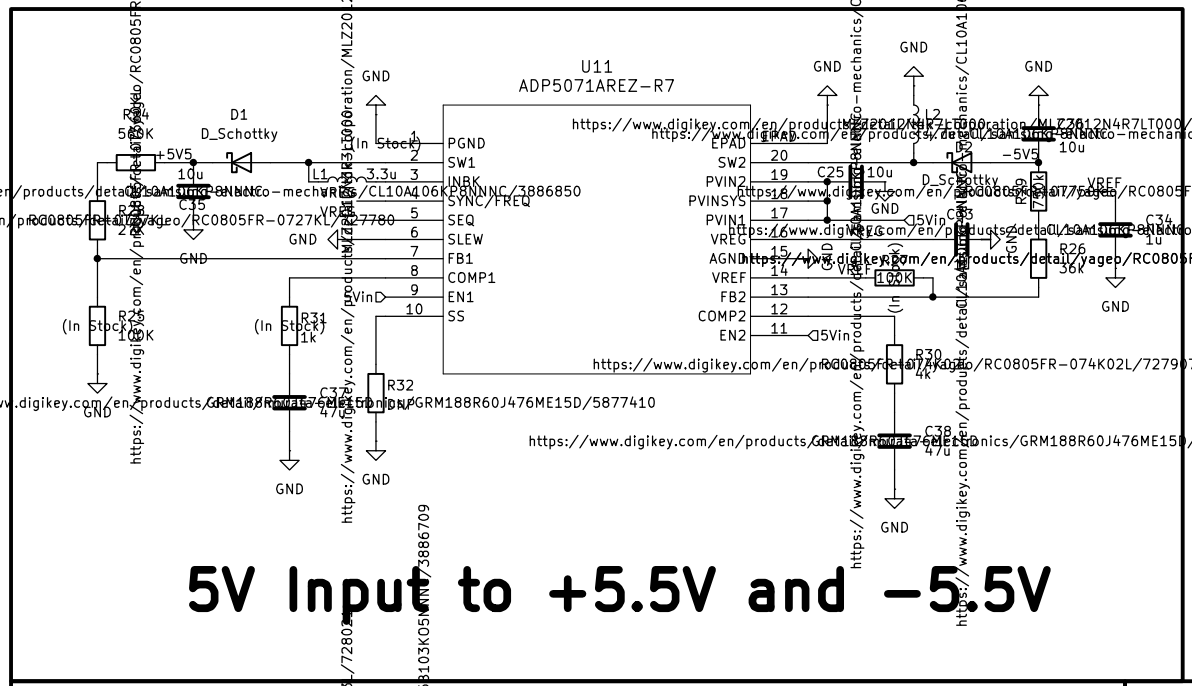
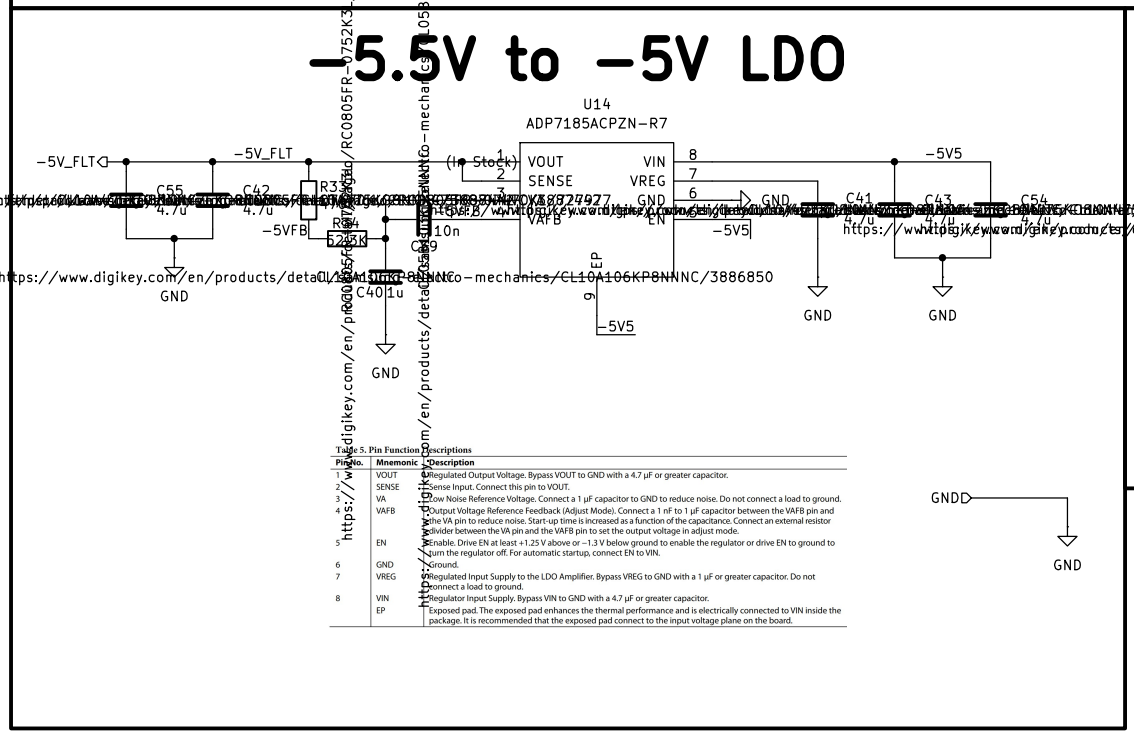

Audio Rails
+5V_FLT
5Vin
−5V_FLT
GND
File: AudioRails.kicad_sch
GND
USB Audio Input
Clocking
File: Clocking.kicad_sch
X1_IN
X1_OUT
EN45
EN_49
XTAL1_OUT
XTAL1_IN
XTAL1_EN
XTAL2_EN
MCLK_XMOS
MCLK_DAC
GND
GND
R9
R10
R8
R7
MCLK
BCLK
LRCLK
I2S_DATA
DAC_RESET
I2S
SCL
SDA
I2C
DAC
MCLK
BCK
WS
SDO
EN
SCL
SDA
DAC1
DAC1b
DAC2
DAC2b
DAC1+
DAC1−
DAC2+
DAC2−
Headphone Amp Stage
File: HeadphoneAmpStage.kicad_sch
+5V
−5V
+Lin
−Lin
+Rin
−Rin
GND
Output_L
Output_R
Output+
Output−
2
3
J3
SJ−3502−SMT
1_4
1_3
1_2
1_1
GND
GND
General Power
Vin
3.3v
1.8v
0.9v
GND
5V_DGB
1V8
3V3
0V9
PLL_0.9V
File: SystemPower.kicad_sch
GND
0V9
+1V8
+3.3V
DAC_GP1
DAC_GP2
DAC_GP3
DAC_GP4
DAC_GP5
DAC_GP6
GPIO
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GND
File: ESS ES9039Q2M DAC.kicad_sch
GND
Debug
JTAG_TCK
JTAG_TMS
JTAG_TDO
JTAG_TDI
4D0
4D1
4D2
4D3
RST_N
DEBUGGING
TCK
TMS
TDO
TDI
4D0
4D1
4D2
4D3
GND
XMOS_NRST
GND
File: Debug.kicad_sch
GND
File: Input.kicad_sch
GND
GND
GND
GND



VBUS Filtering
Transient Protection
USB C Input
Decoupling
XMOS XU316
QSPI Flash
5V Debug Input
J4
PINHD_1x2_Male
5V_DGB
VBUS
GND
J1
2137160001
(In Stock)
R36
5.1k
D3
PESD5V0L1BSL
D4
PESD5V0L1BSL
D5
PESD5V0L1BSL
3V3
3V3BP
0V9
0V9BP
1V8
1V8BP
PLL_0.9V
PLL_AVDD
600R @ 100MHz
U2
XU316-1024-QF60B-C24
QSPI_D1
QSPI_D3
QSPI_CSN
QSPI_CLK
QSPI_D2
QSPI_D0
X1_OUT
X1_IN
JTAG_TDI
JTAG_TDO
RST_N
JTAG_TMS
JTAG_TCK
DAC_GP6
EN45
DAC_GP5
DAC_GP4
DAC_GP3
DAC_GP2
DAC_RESET
I2S_DATA
LRCLK
BCLK
DAC_GP1
EN_49
MCLK
4D3
4D2
4D1
4D0
SDA
SCL
+3.3V
R42
R43
U8
W25Q16JVSNIQ
QSPI_CSN
QSPI_D1
QSPI_D2
QSPI_D3
QSPI_CLK
C17
100n



5V Input to +5.5V and −5.5V



−5.5V to −5V LDO

Pin No.	Mnemonic	Description
1	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 4.7 µF or greater capacitor.
2	SENSE	Sense Input. Connect this pin to VOUT.
3	VA	Low Noise Reference Voltage. Connect a 1 µF capacitor to GND to reduce noise. Do not connect a load to ground.
4	VAFB	Output Voltage Reference Feedback (Adjust Mode). Connect a 1 nF to 1 µF capacitor between the VAFB pin and the VA pin to reduce noise. Start-up time is increased as a function of the capacitance. Connect an external resistor divider between the VA pin and the VAFB pin to set the output voltage in adjust mode.
5	EN	Enable. Drive EN at least +1.25 V above or −1.3 V below ground to enable the regulator or drive EN to ground to turn the regulator off. For automatic startup, connect EN to VIN.
6	GND	Ground.
7	VREG	Regulated Input Supply to the LDO Amplifier. Bypass VREG to GND with a 1 µF or greater capacitor. Do not connect a load to ground.
8	VIN	Regulator Input Supply. Bypass VIN to GND with a 4.7 µF or greater capacitor.
EP		Exposed pad. The exposed pad enhances the thermal performance and is electrically connected to VIN inside the package. It is recommended that the exposed pad connect to the input voltage plane on the board.

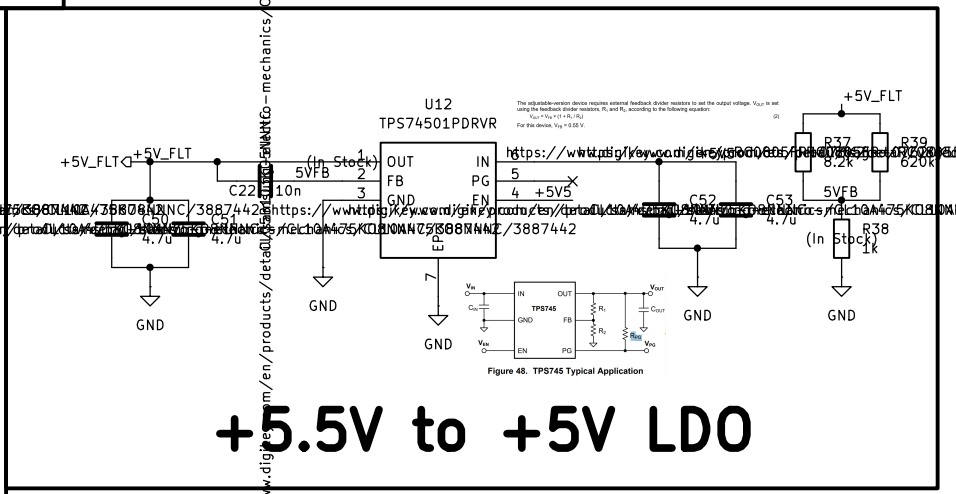
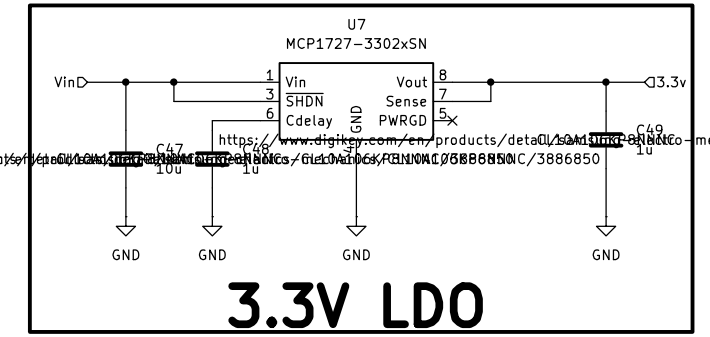
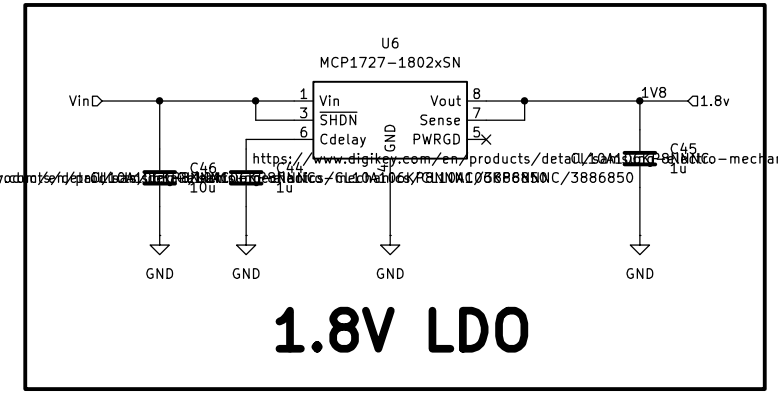
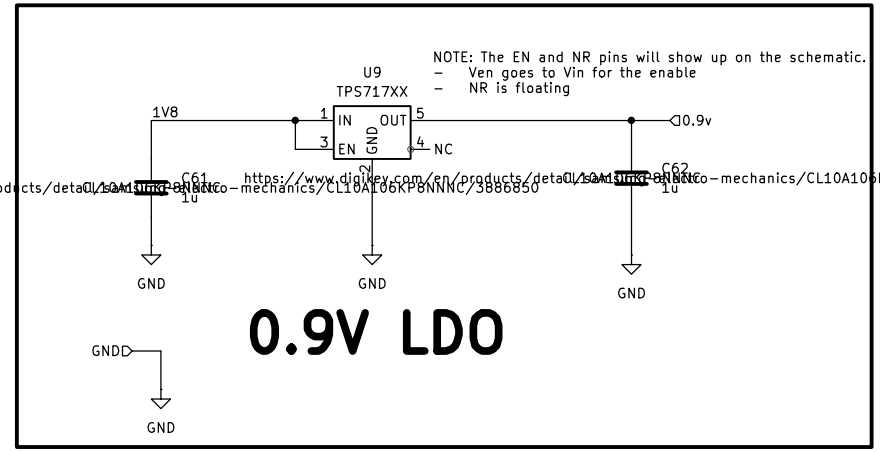


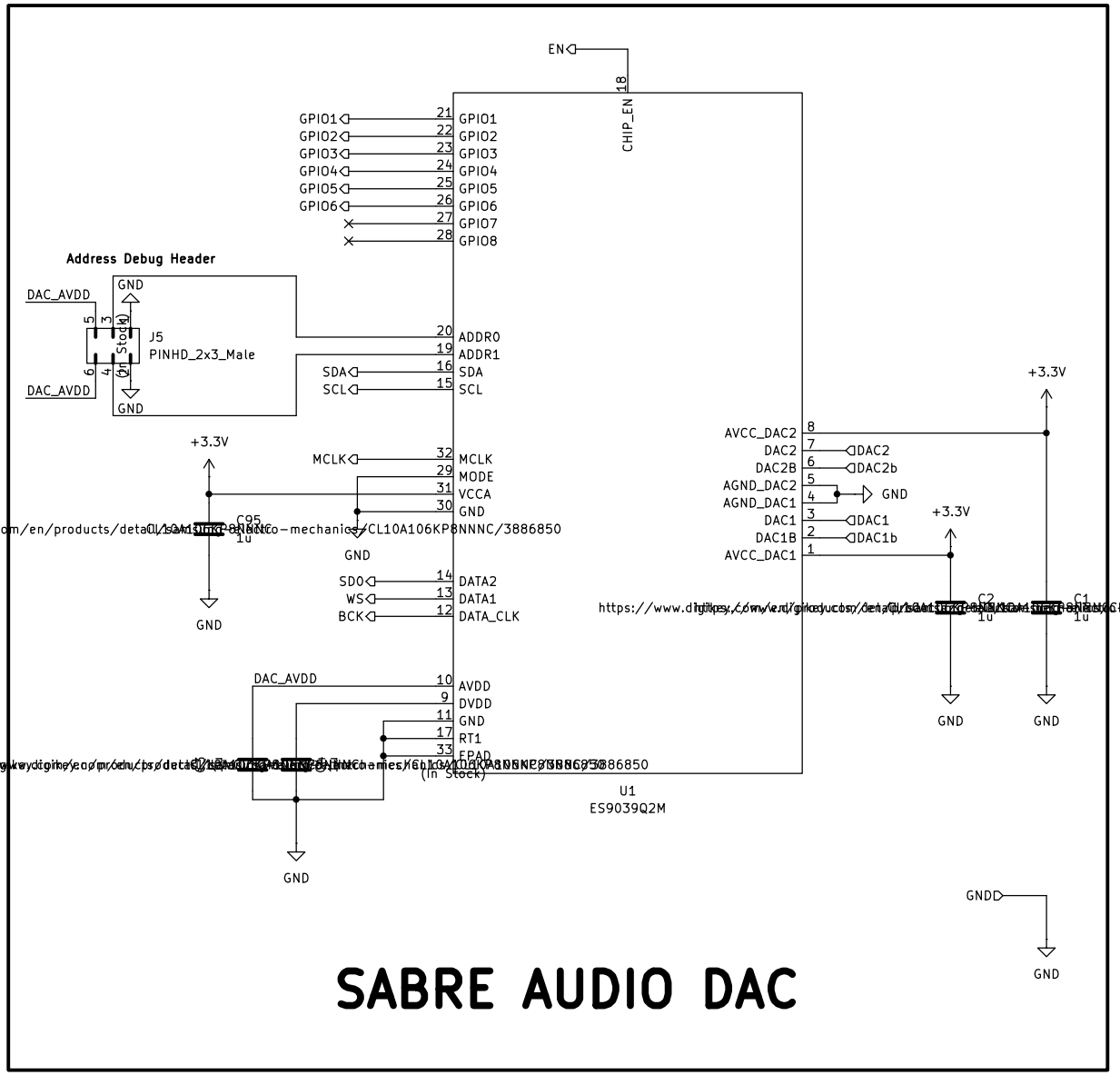
Figure 48. TPS745 Typical Application

+5.5V to +5V LDO


U7
MCP1727-3302xSN
Vin
1
Vin
3
SHDN
6
Cdelay
GND
2
EP
Vout
8
Sense
7
PWRGD
5
3.3v
C47
10u
C48
1u
C49
1u
GND
GND
GND
GND
3.3V LDO


U6
MCP1727-1802xSN
Vin
1
Vin
3
SHDN
6
Cdelay
GND
2
EP
Vout
8
Sense
7
PWRGD
5
1V8
1.8v
C46
10u
C44
1u
C45
1u
GND
GND
GND
GND
1.8V LDO


NOTE: The EN and NR pins will show up on the schematic.
– Ven goes to Vin for the enable
– NR is floating
U9
TPS717XX
1V8
1
IN
3
EN
GND
2
OUT
5
NC
4
0.9v
C61
1u
C62
1u
GND
GND
GND
GND
0.9V LDO



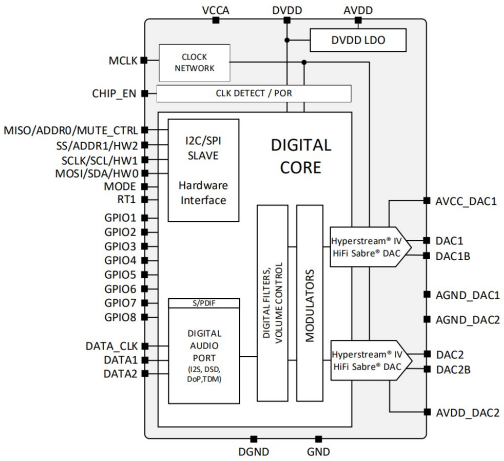


Figure 1 - ES9039Q2M Block Diagram

Software (SW) mode

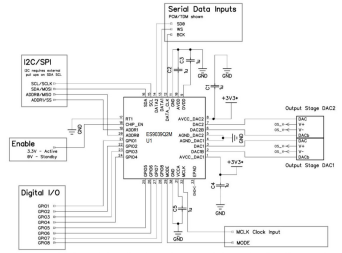
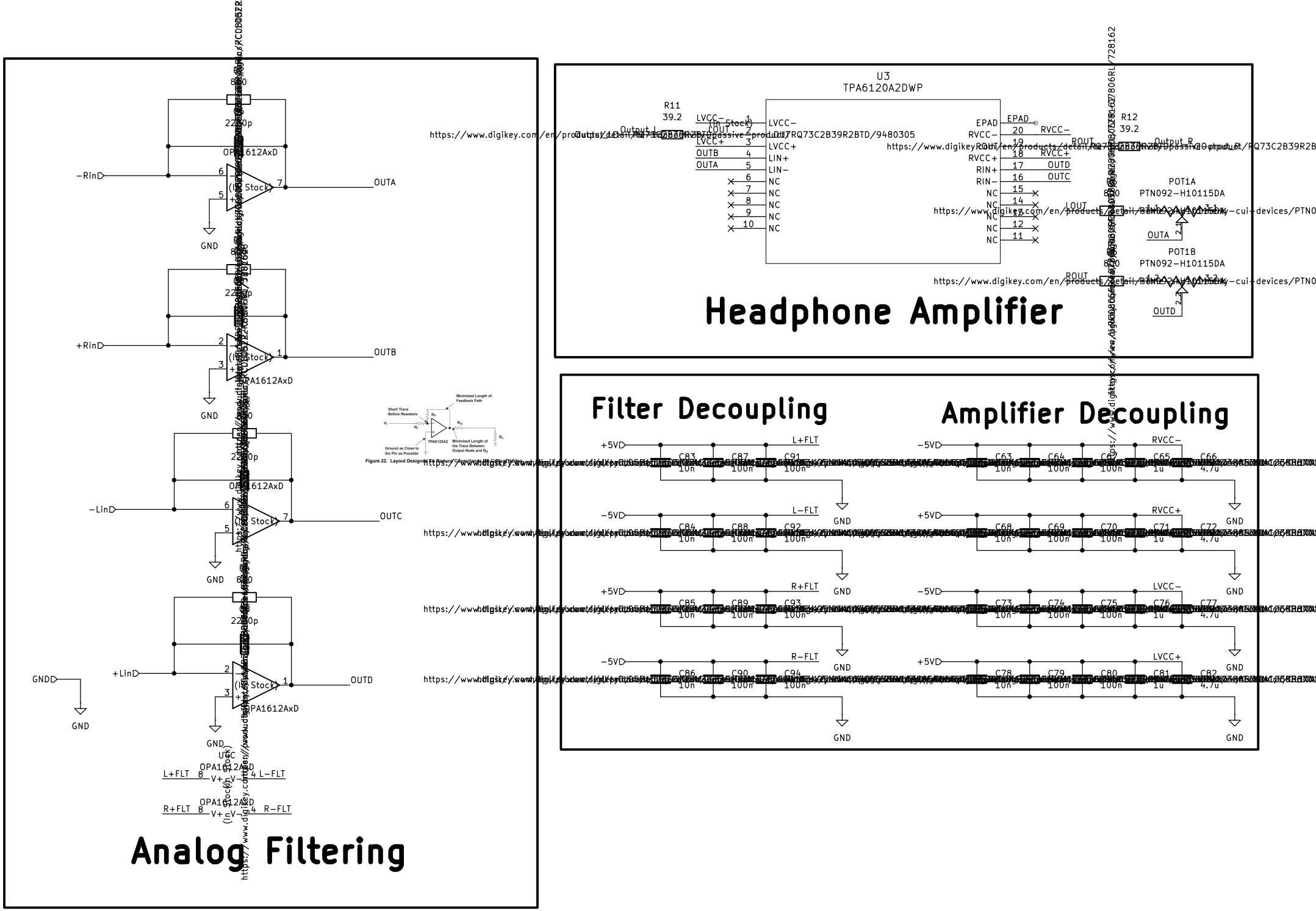


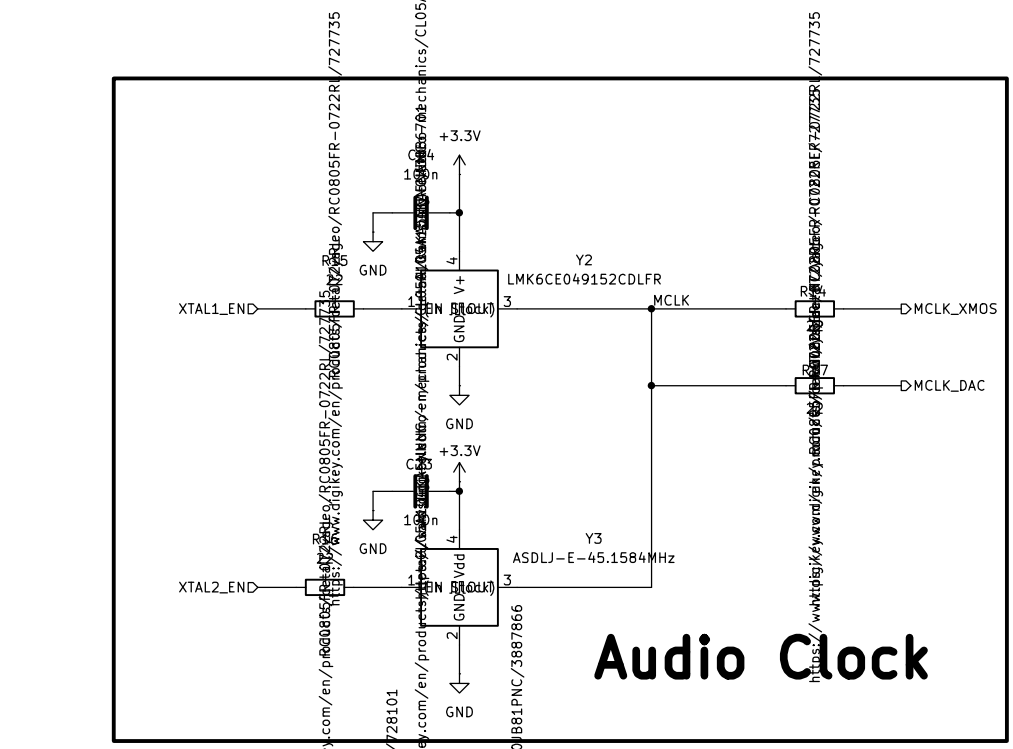
Figure 22 – Software mode reference schematic for ES9039Q2M

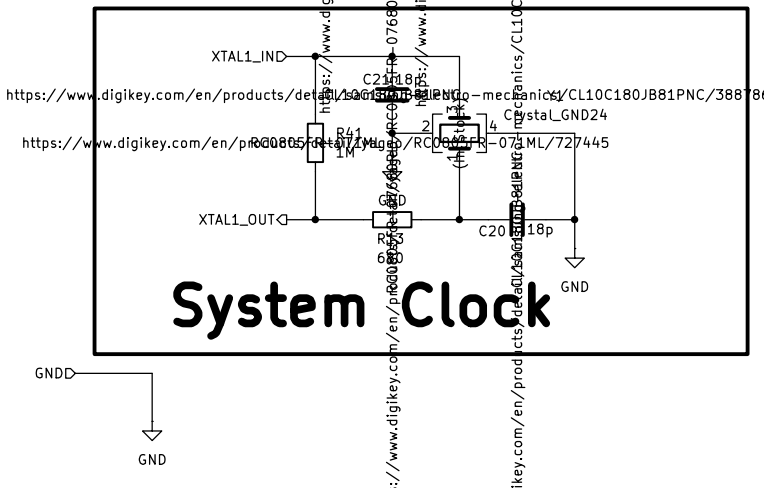
GPIO Pin Descriptions

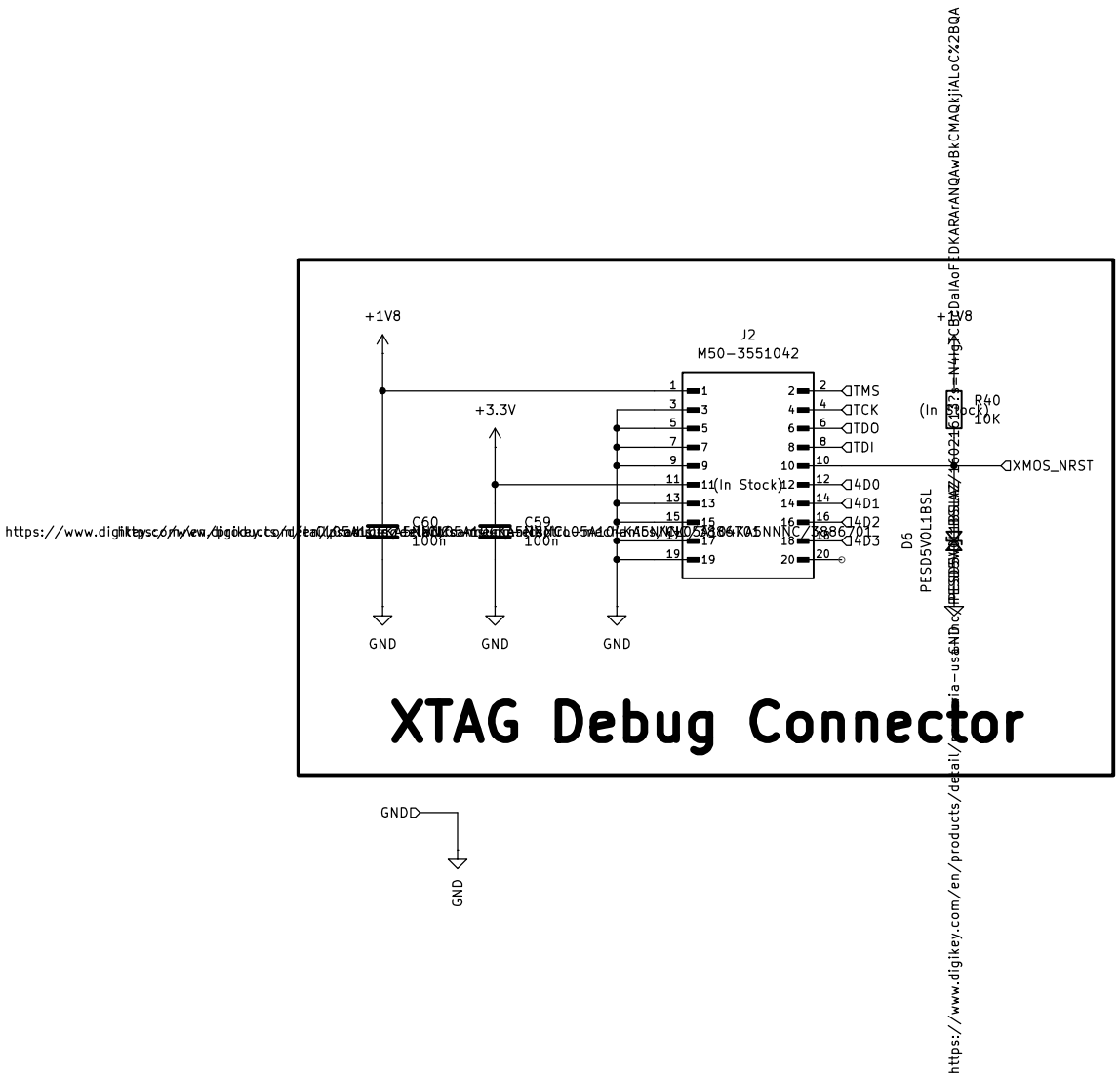
GPIOx	Hardware Mode	Software mode
GPIO1	Automute status.	Regular GPIO.
GPIO2	Lock Status	Regular GPIO.
GPIO3	No hardware mode connection	GPIO3 is connected to the Reg92[0] *TDM_DAISY_CHAIN* logic. When *TDM_DAISY_CHAIN* = 1'b1, GPIO3 can ONLY be used as an output for daisy chain delayed data line. If TDM_DAISY_CHAIN = 1'b0, GPIO3 can then be used as a GPIO.
GPIO4	S/PDIF input pin, requires HW modes 16-18.	Regular GPIO.
GPIO5	DoP input enable, requires HW modes 0-23, 28-31	Regular GPIO.
GPIO6	FIR filter selection, 1'b0: Filter 0, Minimum phase (register default), 1'b1: Filter 2, Linear phase fast roll-off. Requires HW modes 0-23, 28-31.	Regular GPIO.
GPIO7	Connect to Ground*	Regular GPIO.
GPIO8	CAL_RES (calibration resistor)	CAL_RES, disable to use as regular GPIO.

Note*: In Hardware mode GPIO7 needs to be connected to Ground.


Analog Filtering
Headphone Amplifier
Filter Decoupling
Amplifier Decoupling
U3
TPA6120A2DWP
R11
39.2
R12
39.2
POT1A
PTN092-H10115DA
POT1B
PTN092-H10115DA
OPA1612AxD
−Rin
+Rin
−Lin
+Lin
OUTA
OUTB
OUTC
OUTD
GND
L+FLT
L−FLT
R+FLT
R−FLT
+5V
−5V
RVCC−
RVCC+
LVCC−
LVCC+
LOUT
ROUT
EPAD
LIN+
LIN−
RIN+
RIN−
NC
Figure 22. Layout Designed to Reduce Capacitance on Critical Nodes


Audio Clock
+3.3V
GND
Y2
LMK6CE049152CDLFR
XTAL1_END
MCLK
MCLK_XMOS
MCLK_DAC
Y3
ASDLJ-E-45.1584MHz
XTAL2_END


System Clock
XTAL1_IN
XTAL1_OUT
C21 18p
C20 18p
R41
1M
Crystal_GND24
GND
GNDD



+1V8
J2
M50-3551042
+3.3V
TMS
TCK
TDO
TDI
(In Stock)
4D0
4D1
4D2
4D3
R40
10K
XMOS_NRST
C60
100n
C59
100n
D6
PESD5V0L1BSL
GND
GND
GND
XTAG Debug Connector
GND
GND