Lab2: BCD转换二进制电路的设计与实现

**实验介绍**

本实验通过使用ISE软件进行BCD转二进制的模块设计。

**实验目标**

学习8位BCD码转换二进制的转换电路实现。

**实验步骤**

1. 编写8位BCD码转换二进制模块的verilog代码。
2. 将8位BCD转换二进制的verilog代码作为顶层文件生成project。
3. 仿真验证、综合、下载到实验板（详细过程可参考Lab0），实现可以在8个发光二极管输出二进制结果的电路。

**实验原理**

1. 将开关分成两组，表示8位BCD，十位SW[7:4]，个位SW[3:0]；
2. 采用8个发光二极管LD[7:0]作为转换后二进制的输出。

**参考UCF文件**

# Pin assignment for LEDs

NET "LD<7>" LOC = "G1" ; # Bank = 3, Signal name = LD7

NET "LD<6>" LOC = "P4" ; # Bank = 2, Signal name = LD6

NET "LD<5>" LOC = "N4" ; # Bank = 2, Signal name = LD5

NET "LD<4>" LOC = "N5" ; # Bank = 2, Signal name = LD4

NET "LD<3>" LOC = "P6" ; # Bank = 2, Signal name = LD3

NET "LD<2>" LOC = "P7" ; # Bank = 3, Signal name = LD2

NET "LD<1>" LOC = "M11" ; # Bank = 2, Signal name = LD1

NET "LD<0>" LOC = "M5" ; # Bank = 2, Signal name = LD0

# Pin assignment for SWs

NET "SW<7>" LOC = "N3"; # Bank = 2, Signal name = SW7

NET "SW<6>" LOC = "E2"; # Bank = 3, Signal name = SW6

NET "SW<5>" LOC = "F3"; # Bank = 3, Signal name = SW5

NET "SW<4>" LOC = "G3"; # Bank = 3, Signal name = SW4

NET "SW<3>" LOC = "B4"; # Bank = 3, Signal name = SW3

NET "SW<2>" LOC = "K3"; # Bank = 3, Signal name = SW2

NET "SW<1>" LOC = "L3"; # Bank = 3, Signal name = SW1

NET "SW<0>" LOC = "P11"; # Bank = 2, Signal name = SW0