

Universidade Estadual de Campinas

FACULDADE DE ENGENHARIA MECÂNICA

ES670 - Projeto de Sistemas Embarcados

Relatório - Projeto Prático (Parte 1)

Requisitos de Teclado, LEDs e Display de Sete Segmentos

Nome: RA
Daniel Dello Russo Oliveira 101918
Davi Rodrigues 116581

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1 Objetivo

O objetivo do projeto é, de maneira incremental, implementar no target os requisitos apresentados no roteiro[1] inicialmente desenvolvendo o modelo e depois implementando cada requisito. Estes requisitos são referentes à configuração e implementação de entradas de teclado, acionamento de LEDs, display de sete segmentos, protocolo de comunicação, display LCD, medição de velocidade de rotação, PWM, ADC e Controlador.

2 Modelagem

Detectamos logo no início do projeto um defeito estrutural no código fornecido quando lidando com GPIO, o identificador da porta e o número do pino utilizado eram referenciados em diversos locais diferentes do código, dificultando de maneira agravante mudanças na configuração de hardware. Para resolver isso, inicialmente pensamos em utilizar o arquivo fsl_gpio_hal.h da biblioteca da FRDM-Kl25Z, como isso não nos foi permitido e calcular as posições na memória de cada registrador seria reimplementar a biblioteca, escolhemos por criar macros que geram o mesmo estilo de código utilizado no exemplo fornecido, utilizando o operador do pré processador de concatenação ##. Porém, esse operador apresenta algumas particularidades, por exemplo macros que o utilizam no seu corpo não tem seus argumentos expandidos [4], para circular essa dificuldade criamos uma outra macro que funciona como uma wrapper para essa

Utilizando o Rational Rhapsody Modeler e tomando como base os requisitos propostos mostrados na figura 1, complementamos o modelo inicial[2] (requisitos de teclado e LEDs) adicionando um bloco ao modelo referente aos displays de sete segmentos (REQ1C), conforme mostrado na figura 2. Adicionamos também alguns blocos auxiliares relacionados ao gerenciamento de pinos GPIO, e a interrupções periódicas, que foram utilizados para nossa implementação

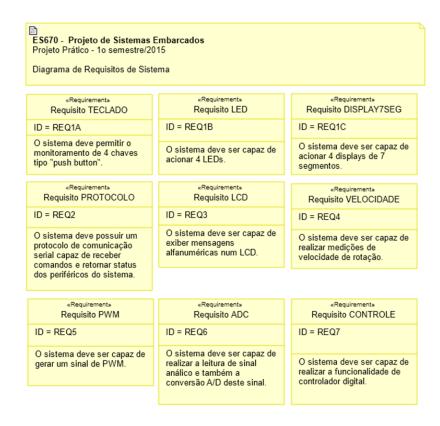


Figura 1: Diagrama de requisitos

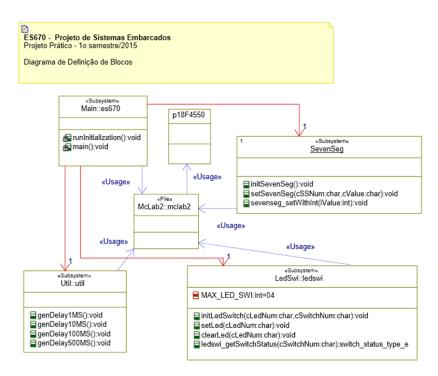


Figura 2: Diagrama de definição de blocos

O bloco SevenSeg possui três operações: inicialização, definição de saída (recebendo qual dos displays será usado e qual valor deve ser exibido) e definição de saída com inteiro (recebendo apenas o valor inteiro a ser exibido no conjunto de quatro displays).

3 Diagramas Esquemáticos

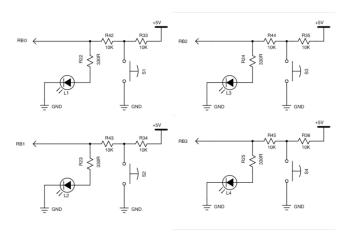


Figura 3: Esquema teclado e LEDs

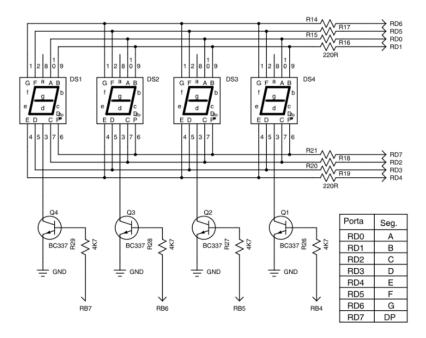


Figura 4: Esquema sete segmentos

Como pode ser visto na figura 4, é necessário fazer um gerenciamento das portas RB4-7 e RD0-7 para que sejam mostrados os valores desejados nos displays de

sete segmentos. Para isso, é preciso alternar qual RB está ativo fazendo a mudança nos RD0-7 para que cada display esteja mostrando um valor diferente. É importante lembrar que a frequência dessa alternância seja escolhida de modo que o olho humano não perceba que os displays estão ligando e desligando.

4 Matriz de Rastreabilidade

A matriz de rastreabilidade apresentada na tabela 1 relaciona cada um dos requisitos com a sua implementação.

Tabela 1: Matriz de Rastreabilidade

ID do Requisito	Implementação
REQ1A	ledswi.c
	- void ledswi_initLedSwitch(char cLedNum, char cSwitchNum)
	- switch_status_type_e ledswi_getSwitchStatus(char cSwitchNum)
REQ1B	ledswi.c
	- void ledswi_initLedSwitch(char cLedNum, char cSwitchNum)
	- void ledswi_setLed(char cLedNum)
	- void ledswi_clearLed(char cLedNum)
REQ1C	sevenSeg.c
	<pre>- void sevenseg_init(void)</pre>
	- void sevenseg_set(char cSSNum, sevenseg_value_e eValue)
	void sevenseg_setWithInt (int iValue)

5 Notas

Os maiores problemas identificados foram a dificuldade de conseguir conectar a placa com o computador e alguns mal contatos relacionados aos botões e do próprio PIC. Além disso, houve alguns conflitos com a IDE, pois muitas funcionalidades poderiam ter sido implementadas, já que a função de autocompletar é bem comum em IDE's e o duplo clique poderia selecionar a palavra em vez de colocar um breakpoint.

6 Referências

- [1] Roteiro de Laboratório Semanas 04 e 05 (disponibilizado para os alunos)
- [2] Projeto do Modelo Inicial do Sistema (disponibilizado para os alunos)

- [3] Código Fonte Inicial em Linguagem C (disponibilizado para os alunos)
- [4] The C Preprocessor (Concatenation) https://gcc.gnu.org/onlinedocs/cpp/Concatenation.html#Concatenation

7 Apêndice

Listagem dos códigos fonte:

7.1 ../Sources/LedSwi/ledswi'hal.h

```
/* File name:
                         ledswi_hal.h
  /* File description: Header file containing the function/
     methods
                         prototypes of ledswi.c
                         dloubach
  /* Author name:
  /* Creation date:
                         09jan2015
  /* Revision date:
                         13\,\mathrm{abr}2016
  #ifndef SOURCES_LEDSWI_LEDSWI_HAL_H_
11 #define SOURCES_LEDSWI_LEDSWI_HAL_H_
13 #define MAX_LED_SWI
                               04
15 typedef enum
```

```
SWITCH_OFF,
      SWITCH_ON
switch_status_type_e;
   * As the hardware board was designed with LEDs/Switches
     sharing
  * the same pins, this method configures how many LEDS
     and switches
   * will be available for the application
* @param cLedNum num of LEDs
   * @param cSwitchNum num of Switches (cLedNum +
     cSwitchNum <= MAX_LED_SWI)
  */
27
  void ledswi_initLedSwitch(char cLedNum, char cSwitchNum);
   * set the led ON
* @param cLedNum which LED {1..4}
   */
void ledswi_setLed(char cLedNum);
37
  * set the led OFF
   * @param cLedNum which LED {1..4}
  void ledswi_clearLed(char cLedNum);
43
   * return the switch status
* @param cSwitchNum which switch
   * @return If the switch is ON or OFF
```

7.2 .../Sources/LedSwi/ledswi'hal.c

```
/* File name:
                        ledswi_hal.c
 /* File description: This file has a couple of useful
     functions to */
                        control LEDs and Switches from
     peripheral board */
5 /* Author name:
                        dloubach
  /* Creation date:
                        20jan2015
7 /* Revision date:
                      13\,\mathrm{abr}2016
 #include "ledswi_hal.h"
11 #include "KL25Z/es670_peripheral_board.h"
13 #define USING_OPENSDA_DEBUG
   * As the hardware board was designed with LEDs/Switches
     sharing
```

```
the same pins, this method configures how many LEDS
     and switches
     will be available for the application
  * @param cLedNum num of LEDs
   * @param cSwitchNum num of Switches (cLedNum +
     cSwitchNum <= MAX_LED_SWI)
21
  void ledswi_initLedSwitch(char cLedNum, char cSwitchNum)
23 {
      /* un-gate port clock*/
      SIM\_SCGC5 = SIM\_SCGC5\_PORTA(CGC\_CLOCK\_ENABLED);
      /* set pin as gpio */
  #ifndef USING_OPENSDA_DEBUG
      PORTA_PCR1 = PORT_PCR_MUX(LS1_ALT);
      PORTA\_PCR2 = PORT\_PCR\_MUX(LS2\_ALT);
31 #endif
      PORTA_PCR4 = PORT_PCR_MUX(LS3_ALT);
      PORTA_PCR5 = PORT_PCR_MUX(LS4_ALT);
33
35
      /* check if the number to configured is according to
      hardware dev kit */
      if ((cLedNum + cSwitchNum) <= MAX_LED_SWI)
39
          /* max number of peripherals to configure is ok,
     carry on */
          switch (cSwitchNum)
41
43
                   /* no switches in system configuration */
                  /* all leds */
                  GPIOA\_PDDR \mid = GPIO\_PDDR\_PDD(
     LS1_DIR_OUTPUT | LS2_DIR_OUTPUT | LS3_DIR_OUTPUT |
     LS4_DIR_OUTPUT);
                  break;
^{47}
```

```
case 1:
49
                   /* just 1 switch */
                   GPIOA_PDDR |= GPIO_PDDR_PDD(
51
     LS2_DIR_OUTPUT | LS3_DIR_OUTPUT | LS4_DIR_OUTPUT);
                   GPIOA_PDDR &= ~GPIO_PDDR_PDD(
     LS1_DIR_INPUT);
                   break;
53
               case 2:
55
                   /* just 2 switches */
                   GPIOA\_PDDR \mid = GPIO\_PDDR\_PDD(
57
     LS3_DIR_OUTPUT | LS4_DIR_OUTPUT);
                   GPIOA_PDDR &= ~GPIO_PDDR_PDD(
     LS1_DIR_INPUT | LS2_DIR_INPUT);
                   break;
59
               case 3:
61
                   /* 3 switches */
                   GPIOA_PDDR |= GPIO_PDDR_PDD(
63
     LS4_DIR_OUTPUT);
                   GPIOA_PDDR &= ~GPIO_PDDR_PDD(
     LS1_DIR_INPUT | LS2_DIR_INPUT | LS3_DIR_INPUT);
                   break;
65
               case 4:
67
                   /* 4 switches */
                   GPIOA_PDDR &= ~GPIO_PDDR_PDD(
69
     LS1_DIR_INPUT | LS2_DIR_INPUT | LS3_DIR_INPUT |
     LS4_DIR_INPUT);
                   break;
          } /* switch(cSwitchNum) */
      } /* if ((cLedNum + cSwitchNum) <= MAX_LED_SWI) */
73
75 }
```

```
77
79
    * set the led ON
   * @param cLedNum which LED {1..4}
  void ledswi_setLed(char cLedNum)
       /* sanity check */
85
       if (cLedNum <= MAX_LED_SWI)</pre>
           switch (cLedNum)
89
                case 1:
                    GPIOA\_PSOR = GPIO\_PSOR\_PTSO( (0x01U <<
91
      LS1_PIN));
                    break;
93
                    GPIOA\_PSOR = GPIO\_PSOR\_PTSO( (0x01U <<
      LS2\_PIN));
                    break;
95
                case 3:
                    GPIOA\_PSOR = GPIO\_PSOR\_PTSO( (0x01U <<
97
      LS3_PIN));
                    break;
                case 4:
99
                    GPIOA\_PSOR = GPIO\_PSOR\_PTSO( (0x01U <<
      LS4-PIN));
                    break;
101
           } /* switch(cLedNum) */
       } /* if (cLedNum <= MAX_LED_SWI) */
105 }
107
```

```
109
    * set the led OFF
   * @param cLedNum which LED {1..4}
void ledswi_clearLed(char cLedNum)
       /* sanity check */
115
       if (cLedNum <= MAX_LED_SWI)
117
            switch (cLedNum)
119
                 case 1:
                     GPIOA.PCOR = GPIO.PCOR.PTCO( (0x01U <<
121
      LS1_PIN));
                     break;
                 case 2:
                     GPIOA\_PCOR = GPIO\_PCOR\_PTCO( (0x01U <<
      LS2\_PIN));
                     break;
125
                 case 3:
                     GPIOA\_PCOR = GPIO\_PCOR\_PTCO( (0x01U <<
127
      LS3_PIN) );
                     break;
                 case 4:
129
                     \label{eq:GPIOA_PCOR} \text{GPIOA_PCOR\_PTCO}(\ \ (0\,\text{x}01\text{U}\ <<
      LS4_PIN) );
                     break;
131
            } /* switch(cLedNum) */
133
       } /* if (cLedNum <= MAX_LED_SWI) */
135 }
137
139 /**
```

```
* return the switch status
   * @param cSwitchNum which switch
   * @return If the switch is ON or OFF
   */
143
   switch_status_type_e ledswi_getSwitchStatus(char
      cSwitchNum)
145 {
       switch_status_type_e sstReturn = SWITCH_OFF;
147
       /* sanity check */
       if (cSwitchNum <= MAX_LED_SWI)</pre>
149
           switch (cSwitchNum)
151
                case 1:
153
                    if (SWITCH_ON == ((GPIOA_PDIR &
      LS1_DIR_INPUT) >> LS1_PIN) )
                        sstReturn = SWITCH_ON;
155
                    break;
157
                case 2:
                    if (SWITCH_ON == ((GPIOA_PDIR &
159
      LS2\_DIR\_INPUT) >> LS2\_PIN)
                        sstReturn = SWITCH_ON;
                    break:
161
                case 3:
163
                    if(SWITCH\_ON == ((GPIOA\_PDIR \&
      LS3\_DIR\_INPUT) >> LS3\_PIN)
                        sstReturn = SWITCH_ON;
165
                    break;
167
                case 4:
                    if (SWITCH_ON == ((GPIOA_PDIR &
169
      LS4_DIR_INPUT) >> LS4_PIN) )
                        sstReturn = SWITCH_ON;
```

```
break;

} /* switch(cSwitchNum) */

} /* if(cSwitchNum <= MAX_LED_SWI) */

/* return the result */
return(sstReturn);

}</pre>
```

7.3 ../Sources/Mcg/mcg hal.h

7.4 ../Sources/Mcg/mcg'hal.c

```
2 /* File name:
                       mgc_hal.c
 /* File description: Multipurpose clk generator hardware
     abstraction */
                       layer. Enables the clock
     configuration
                 */
                       Modes of Operation
                       FLL Engaged Internal (FEI)
    DEFAULT
                       FLL Engaged External (FEE)
                 */
                       FLL Bypassed Internal (FBI)
                 */
                       FLL Bypassed External (FBE)
                 */
```

```
PLL Engaged External (PEE)
                   */
                         PLL Bypassed External (PBE)
                   */
                         Bypassed Low Power Internal (BLPI)
                   */
                         Bypassed Low Power External (BLPE)
                   */
                         Stop
                   */
                   */
                         For clock definitions, check the
      chapter
                         5.4 Clock definitions from
                         KL25 Sub-Family Reference Manual
                   */
  /* Author name:
                         dloubach
/* Creation date:
                         21\,\mathrm{out}\,2015
  /* Revision date:
                         13 a br 2016
24 /*
       */
26 #include "mcg_hal.h"
28 /* systems include */
  #include "fsl_smc_hal.h"
30 #include "fsl_port_hal.h"
 #include "fsl_clock_manager.h"
```

```
/* EXTAL0 PTA18 */
34 #define EXTALO_PORT
                                         PORTA
  #define EXTALO_PIN
                                         18U
36 #define EXTALO_PINMUX
                                         kPortPinDisabled
38 /* XTALO PTA19 */
  #define XTAL0_PORT
                                         PORTA
40 #define XTALO_PIN
                                         19U
  #define XTAL0_PINMUX
                                         kPortPinDisabled
  /* OSCO configuration */
44 #define OSC0_INSTANCE
                                         0U
  #define OSC0_XTAL_FREQ
                                         8000000U /* 08 MHz*/
46 #define OSC0_SC2P_ENABLE_CONFIG
                                         false
  #define OSC0_SC4P_ENABLE_CONFIG
                                         false
48 #define OSC0_SC8P_ENABLE_CONFIG
                                         false
  #define OSC0_SC16P_ENABLE_CONFIG
                                         false
50 #define MCG_HGO0
                                         kOscGainLow
  #define MCG_RANGEO
                                         kOscRangeVeryHigh
<sub>52</sub> #define MCG_EREFS0
                                         kOscSrcOsc
54 /* RTC external clock configuration. */
  #define RTC_XTAL_FREQ
56 #define RTC_SC2P_ENABLE_CONFIG
                                         false
  #define RTC_SC4P_ENABLE_CONFIG
                                         false
58 #define RTC_SC8P_ENABLE_CONFIG
                                         false
  #define RTC_SC16P_ENABLE_CONFIG
                                         false
60 #define RTC_OSC_ENABLE_CONFIG
                                         false
  #define RTC_CLK_OUTPUT_ENABLE_CONFIG false
  /* RTC_CLKIN PTC1 */
64 #define RTC_CLKIN_PORT
                                         PORTC
  #define RTC_CLKIN_PIN
                                         1U
66 #define RTC_CLKIN_PINMUX
                                         kPortMuxAsGpio
```

```
#define CLOCK_VLPR
                                        1U /* very low power
      run mode */
70 #define CLOCK_RUN
                                         2U /* run mode */
#ifndef CLOCK_INIT_CONFIG
  #define CLOCK_INIT_CONFIG CLOCK_RUN
74 #endif
  /* Configuration for enter VLPR mode, Core clock = 4MHz
78 const clock_manager_user_config_t
     g_defaultClockConfigVlpr =
      .mcgConfig =
80
          . mcg\_mode
                               = kMcgModeBLPI,
                                                      // Work
      in BLPI mode
          .irclkEnable
                               = true,
     MCGIRCLK enable
          .irclkEnableInStop = false,
84
     MCGIRCLK disable in STOP mode
          .ircs
                               = kMcgIrcFast,
     Select IRC4M
                               = 0U,
          . fcrdiv
86
     FCRDIV is 0
          .frdiv
                   = 0U,
88
                   = kMcgDcoRangeSelLow,
          .drs
                                                      // Low
     frequency range
          . dmx32
                   = kMcgDmx32Default,
                                                      // DCO
     has a default range of 25\%
          .pll0EnableInFllMode = false,
                                                      // PLL0
      disable
```

```
// PLL0
           . pll0EnableInStop
                               = false,
       disalbe in STOP mode
           .prdiv0
                               = 0U,
94
           .vdiv0
                               = 0U,
       },
96
       . simConfig =
98
           .pllFllSel = kClockPllFllSelFll,
      PLLFLLSEL select FLL
           . er32kSrc = kClockEr32kSrcLpo,
100
      ERCLK32K selection, use LPO
           .outdiv1
                      = 0U,
           .outdiv4
                      = 4U,
102
       .oscerConfig =
104
           .enable
                          = true,
106
      OSCERCLK enable
           .enableInStop = false,
      OSCERCLK disable in STOP mode
      }
108
  };
110
   /* Configuration for enter RUN mode, Core clock = 40 MHz
      */
   * 24.5.1.1 Initializing the MCG
   * KL25 Sub-Family Reference Manual, Rev. 3, September
      2012
   * Refer also to
   * Table 24-18. MCG modes of operation
118
   * On L-series devices the MCGFLLCLK frequency is limited
       to 48 MHz max
```

```
* The DCO is limited to the two lowest range settings (
     MCG_C4[DRST_DRS] must be set to either 0b00 or 0b01).
   * FEE (FLL engaged external)
122
   * fext / FLL_R must be in the range of 31.25 kHz to
     39.0625 \text{ kHz}
* FLL_R is the reference divider selected by the C1
     FRDIV] bits
   * F is the FLL factor selected by C4[DRST_DRS] and C4[
     DMX32 bits
126
   * (fext / FLL_R) * F = (8 MHz / 256) * 1280 = 40 MHz
128
   * */
const clock_manager_user_config_t g_defaultClockConfigRun
      /* — multipurpose clock generator
132
      configurations ----**
      .mcgConfig =
134
          .\,\mathrm{mcg\_mode}
                      = kMcgModeFEE, // Work
      in FEE mode
136
                       ----- MCGIRCCLK settings
          .irclkEnable
                              = true,
138
     MCGIRCLK enable
          .irclkEnableInStop = false,
     MCGIRCLK disable in STOP mode
          .ircs
                              = kMcgIrcSlow,
140
      Select IRC 32kHz
          . fcrdiv
                              = 0U,
     FCRDIV is 0
142
```

```
——— MCG FLL settings
           . fr div = 0b011,
144
      Divide Factor is 256 (EXT OSC 8 MHz / 256 = 31.250 \text{ kHz}
      )
                                                      // The
      resulting frequency must be in the range 31.25 kHz to
      39.0625~\mathrm{kHz}
           .drs
                    = kMcgDcoRangeSelMid,
146
      frequency range
           .\,\mathrm{dmx}32
                    = kMcgDmx32Default,
                                                      // DCO
      has a default range of 25\%
148
                           ----- MCG PLL settings
           .pll0EnableInFllMode = false,
                                                      // PLL0
150
      disable
           .pll0EnableInStop = false,
                                                      // PLL0
      disabLe in STOP mode
           .prdiv0
                              = 0x0U,
152
           .vdiv0
                              = 0x0U,
      },
154
      /* _____ system integration module
      configurations -----**
      . simConfig =
156
           .pllFllSel = kClockPllFllSelFll,
158
      PLLFLLSEL select PLL
           .er32kSrc = kClockEr32kSrcLpo,
      ERCLK32K selection, use LPO
           . outdiv1 = 0U,
                                                      // core/
160
      system clock, as well as the bus/flash clocks.
                                                     // bus
           . outdiv4 = 1U,
      and flash clock and is in addition to the System clock
       divide ratio
      },
162
```

```
/* ---- system oscillator output
      configurations
       .oscerConfig =
164
           .enable
                          = true,
166
      OSCERCLK enable
           .enableInStop = false,
      OSCERCLK disable in STOP mode
       }
168
   };
170
    * Oscillator configuration
   void mcg_initOsc0(void)
176
       /* OSC0 configuration */
       osc\_user\_config\_t \ osc0Config =
178
           .freq
                                  = OSC0\_XTAL\_FREQ,
180
           . hgo
                                  = MCG_HGO0,
           . range
                                  = MCG_RANGE0,
182
           .erefs
                                  = MCG_EREFS0,
                                  = \ {\rm OSC0\_SC2P\_ENABLE\_CONFIG}\,,
           .enable Capacitor 2p
184
           .enableCapacitor4p
                                  = OSC0\_SC4P\_ENABLE\_CONFIG,
           .enableCapacitor8p
                                  = OSC0\_SC8P\_ENABLE\_CONFIG,
186
           .enableCapacitor16p = OSC0_SC16P_ENABLE_CONFIG,
       };
188
       /* oscillator initialization */
190
       CLOCK_SYS_OscInit(OSC0_INSTANCE, &osc0Config);
192 }
```

```
196
    * Function to initialize RTC external clock base on
      board configuration
   */
198
  void mcg_initRtcOsc(void)
200 {
  #if RTC_XTAL_FREQ
      // If RTC_CLKIN is connected, need to set pin mux.
      Another way for
      // RTC clock is set RTC_OSC_ENABLE_CONFIG to use OSC0
204
      , please check
      // reference manual for details
      PORT_HAL_SetMuxMode(RTC_CLKIN_PORT, RTC_CLKIN_PIN,
206
      RTC_CLKIN_PINMUX);
  #endif
208
  #if ((OSC0_XTAL_FREQ != 32768U) && (RTC_OSC_ENABLE_CONFIG
      ))
#error Set RTC_OSC_ENABLE_CONFIG will override OSC0
      configuration and OSC0 must be 32k.
  #endif
212
       rtc_osc_user_config_t rtcOscConfig =
214
           .freq
                                 = RTC\_XTAL\_FREQ,
           .enable Capacitor 2p
                                 = RTC_SC2P_ENABLE_CONFIG,
216
           .enableCapacitor4p
                                 = RTC_SC4P_ENABLE_CONFIG,
           .enableCapacitor8p
                                 = RTC_SC8P_ENABLE_CONFIG,
218
           .enableCapacitor16p
                                = RTC\_SC16P\_ENABLE\_CONFIG,
           .enableOsc
                                 = RTC_OSC_ENABLE_CONFIG,
220
       };
222
       /* OSC RTC initialization */
      CLOCK_SYS_RtcOscInit(0U, &rtcOscConfig);
```

```
226
228
   * System clock configuration
   */
   void mcg_initSystemClock(void)
232
      /* Set system clock configuration. */
234
      \# \mathtt{if} \ (\mathtt{CLOCK\_INIT\_CONFIG} = \mathtt{CLOCK\_VLPR})
           CLOCK_SYS_SetConfiguration(&
236
      g_defaultClockConfigVlpr);
      #else
           CLOCK_SYS_SetConfiguration(&
238
      g_defaultClockConfigRun);
      #endif
240 }
242
      *************
   /* Method name: mcg_clockInit
246 /* Method description: main board clk configuration */
   /* Input params:
                      n/a
248 /* Output params:
  void mcg_clockInit(void)
      /* enable clock for PORTs */
252
      CLOCK_SYS_EnablePortClock(PORTA_IDX);
      CLOCK_SYS_EnablePortClock(PORTC_IDX);
254
      CLOCK_SYS_EnablePortClock(PORTE_IDX);
256
      /* set allowed power mode to allow all */
      SMC_HAL_SetProtection(SMC, kAllowPowerModeAll);
```

```
/* configure OSC0 pin mux */
260
      PORT_HAL_SetMuxMode(EXTAL0_PORT, EXTAL0_PIN,
      EXTALO_PINMUX);
      PORT_HAL_SetMuxMode(XTAL0_PORT, XTAL0_PIN,
262
      XTAL0_PINMUX);
       /* setup OSC0 */
264
       mcg_initOsc0();
266
       /* setup OSC RTC */
       mcg_initRtcOsc();
268
       /* setup system clock */
270
       mcg_initSystemClock();
272 }
```

7.5 ../Sources/PIT/pit hal.h

```
#ifndef SOURCES_PIT_PIT_HAL_H_
#define SOURCES_PIT_PIT_HAL_H_
14 /**
   * Enables Periodic Interruption Timer module.
* (With the stop on debug flag set to on)
  */
void pit_enable(void);
20 /**
   * Start interruptions for given timer, unchained mode.
  * Timer interruptions are masked.
  * @param usTimer_numb The number for the desired timer
   * @param uiTimer_period The number of bus_clock cycles
     between interrupts
  * @param fpInterrupt_handler Timer interrupt handler
      routine address pointer
   */
void pit_start_timer_interrupt (unsigned short
     usTimer_numb, unsigned int uiTimer_period, void (*
     fpInterrupt_handler)(void));
   * Stop interruptions for given timer, unchained mode.
   * @param usTimer_numb The number for the desired timer
     (0,1)
34 */
  void pit_stop_timer_interrupt(unsigned short usTimer_numb
     );
```

```
/**

* Mark interruption as handled for the given timer, this should be called by timer

* interruption handlers once they are finished.

*

* @param usTimer_numb The number for the desired timer (0,1)

*/

void pit_mark_interrupt_handled(unsigned short usTimer_numb);

/**

* Pit interruption handler. Checks what timer caused the interruption and call the

* correct timer interruption handler.

*/

void PIT_IRQHandler(void);

#endif /* SOURCES_PIT_PIT_HAL_H_ */
```

7.6 ../Sources/PIT/pit'hal.c

```
/* Creation date:
                        10\,\mathrm{abr}2016
  /* Revision date:
                        13 abr 2016
10 // Careful when handling PIT DOC! Bit endianness is
     inverted in relation to GPIO doc
12 #include "pit_hal.h"
  #include "KL25Z/es670_peripheral_board.h"
  #define PIT_IRQ_NUMBER PIT_IRQn
16
  *Default timer interruption handler. Does nothing.
   */
20 static void _nop_handler(void){
    PIT_TFLG0 \mid = PIT_TFLG_TIF(0x1u);
    PIT_TFLG1 = PIT_TFLG_TIF(0x1u);
  }
  static void (*fpTimer0Handler)(void) = &_nop_handler;
static void (*fpTimer1Handler)(void) = &_nop_handler;
   * Pit interruption handler. Checks what timer caused the
       interruption and call the
   * correct timer interruption handler.
32 void PIT_IRQHandler(void){
    if (PIT_TFLG0) {
      (*fpTimer0Handler)();
34
    }
    if (PIT_TFLG1) {
```

```
(*fpTimer1Handler)();
40
  * Enables Periodic Interruption Timer module.
   * (With the stop on debug flag set to on)
  */
  void pit_enable(void){
    SIM_SCGC6 |= SIM_SCGC6_PIT_MASK;
    PIT\_MCR \&= PIT\_MCR\_MDIS(0x1u);
    //Freeze in debug mode
    PIT\_MCR \mid = PIT\_MCR\_FRZ(0x1u);
    NVIC_ClearPendingIRQ(PIT_IRQ_NUMBER);
      NVIC\_EnableIRQ\left(PIT\_IRQ\_NUMBER\right);
52 }
   * Start interruptions for given timer, unchained mode.
   * Timer interruptions are masked.
  * @param usTimer_numb The number for the desired timer
   * @param_uiTimer_period The number of bus_clock_cycles
     between interrupts
  * @param fpInterrupt_handler
                                     Timer interrupt handler
      routine address pointer
void pit_start_timer_interrupt (unsigned short
     usTimer_numb, unsigned int uiTimer_period, void (*
     fpInterrupt_handler)(void)){
    if (!usTimer_numb) {
      timer0Handler = fpInterrupt_handler;
64
      PIT_LDVAL0 = PIT_LDVAL_TSV(uiTimer_period);
      PIT_TCTRL0 &= ~PIT_TCTRL_CHN(0x1u); /*Disable chain
      mode*/
```

```
PIT\_TCTRL0 \mid = PIT\_TCTRL\_TIE(0x1u);
                                               /*Enable
     interrupts for timer 0*/
      PIT\_TCTRL0 \mid = PIT\_TCTRL\_TEN(0x1u);
                                               /*Enable timer
     0*/
    }else{
      timer1Handler = fpInterrupt_handler;
70
      PIT_LDVAL1 = PIT_LDVAL_TSV(uiTimer_period);
      PIT_TCTRL1 &= ~PIT_TCTRL_CHN(0x1u);
                                               /*Disable chain
72
      mode*/
      PIT\_TCTRL1 \mid = PIT\_TCTRL\_TIE(0x1u);
                                               /*Enable
     interrupts for timer 1*/
      PIT\_TCTRL1 = PIT\_TCTRL\_TEN(0x1u);
                                             /*Enable timer
     1*/
    }
76 }
   * Stop interruptions for given timer, unchained mode.
   * @param usTimer_numb The number for the desired timer
      (0,1)
  */
82
  void pit_stop_timer_interrupt(unsigned short usTimer_numb
    if (!usTimer_numb) {
84
      PIT_TCTRL0 &= ~PIT_TCTRL_TIE(0x1u);
      PIT_TCTRL0 &= "PIT_TCTRL_TEN(0x1u);
86
    }else{
      PIT_TCTRL1 &= ~PIT_TCTRL_TIE(0x1u);
88
      PIT_TCTRL1 &= ^{\sim}PIT_TCTRL_TEN(0x1u);
90
92
  * Mark interruption as handled for the given timer, this
       should be called by timer
```

7.7 ../Sources/SevenSeg/sevenseg'hal.h

```
11 #ifndef SOURCES_SEVEN_SEGMENT_HAL_H_
  #define SOURCES_SEVEN_SEGMENT_HAL_H_
  #include "KL25Z/es670_peripheral_board.h"
  #define MAX.SEGMENT_NUMBER 8
#define MAX_DISP_NUMBER 4
19
  typedef enum
21 {
      SEG\_A = SEGA\_PIN,
      SEG_B = SEGB_PIN,
23
      SEG_C = SEGC_PIN,
      SEG_D = SEGD_PIN,
25
      SEG_E = SEGE_{PIN},
      SEG_F = SEGF_PIN,
27
      SEG\_G = SEGG\_PIN,
      SEG_DP = SEGDP_PIN,
29
    SEG\_END = -1
| seven_segment_seg_type_e;
33 typedef enum
      DISP_1 =
                 SEG_DISP1_PIN,
    DISP_2 =
               SEG_DISP2_PIN,
    DISP_{-3} =
               SEG_DISP3_PIN,
37
    DISP_{-4} =
               SEG_DISP4_PIN,
39 } seven_segment_disp_type_e;
  * Initialize the seven segment display
  void sevenseg_init(void);
45
```

```
* Sets only the selected segments as high. Setting the
     others as low
   * @param epDet_segments = Array with the segments that
     should be set as on (Last element should be SEGEND)
  void sevenseg_setSegs(seven_segment_seg_type_e*
     epSet_segments);
51
  /**
  * Shows the value written in the segment pins to the
   * given display after clearing the others
  * @param eDisplay the display to initialize.
   */
void sevenseg_setDisp(seven_segment_disp_type_e eDisplay)
59 /**
   * Shows the passed value in hexadecimal format in the
     seven segment display.
* @param uiHex the value to be printed
   */
oid sevenseg_printHex(unsigned int uiHex);
65 /**
   * Shows the passed value in decimal format in the seven
     segment display.
* @param uiDec the value to be printed
   */
op void sevenseg_printDec(unsigned int uiDec);
71 /**
   * Converts the less significative decimal digit of the
     argument into it's seven
* segment display configuration
```

```
* @param usDec the value to be converted (-1 if none
     should be displayed)
  * @param epRet address for results (should be a
     allocated array of minimal 9 elements)
  * @return epRet
79 seven_segment_seg_type_e* sevenseg_dec2segArray(unsigned
     short usDec, seven_segment_seg_type_e* epRet);
81 /**
   * Converts the less significative hexadecimal digit of
     the argument into it's seven
  * segment display configuration
  * @param usHex the value to be converted (-1 if none
     should be displayed)
  * @param epRet address for results (should be a
     allocated array of minimal 9 elements)
  * @return epRet
   */
sel seven_segment_seg_type_e* sevenseg_hex2segArray(unsigned
     short usHex, seven_segment_seg_type_e* epRet);
91 #endif /* SOURCES_SEVEN_SEGMENT_HAL_H_ */
```

7.8 ../Sources/SevenSeg/sevenseg'hal.c

```
for handling SEVEN SEGMENT DISPLAY
                         from the peripheral board
                        ddello
     Author name:
     Creation date:
                        18mar2016
  /* Revision date:
                        13 abr 2016
#include "GPIO/gpio_hal.h"
 #include "sevenseg_hal.h"
#include "math.h"
  #include "KL25Z/es670_peripheral_board.h"
#include "PIT/pit_hal.h"
| #define SEV_SEG_SEGMENT_MASK GPIO_HIGH << SEGA_PIN |
     GPIO_HIGH << SEGB_PIN | GPIO_HIGH << SEGC_PIN |
     GPIO_HIGH << SEGD_PIN | GPIO_HIGH << SEGE_PIN |
     GPIO_HIGH << SEGF_PIN | GPIO_HIGH << SEGG_PIN |
     GPIO_HIGH << SEGDP_PIN
 #define SEV_SEG_DISP_MASK GPIO_HIGH << SEG_DISP1_PIN |
     {\rm GPIO\_HIGH} << {\rm SEG\_DISP2\_PIN} \ | \ {\rm GPIO\_HIGH} <<
     SEG_DISP3_PIN | GPIO_HIGH << SEG_DISP4_PIN
  static unsigned short usIsHex = 0;
static unsigned int uiPrintVal = -1;
23 /**
   * Interrupt handler for updating in display
     configuration
25 | */
```

```
void _sevenseg_interrupt_handler(void){
    static seven_segment_disp_type_e epDisplays[] = {DISP_1
      , DISP_2, DISP_3, DISP_4;
    static seven_segment_seg_type_e epSeg_array[9];
    static unsigned short usCur_disp = 0;
    if (usIsHex) {
      sevenseg_hex2segArray(uiPrintVal/pow(16,usCur_disp),
31
     epSeg_array);
    }else{
      sevenseg_dec2segArray(uiPrintVal/pow(10,usCur_disp),
33
     epSeg_array);
    sevenseg_setSegs(epSeg_array);
35
    sevenseg_setDisp(epDisplays[usCur_disp]);
    usCur_disp = (usCur_disp+1)\%4;
    pit_mark_interrupt_handled(SEV_SEG_PIT_TIMER_NUMB);
39 }
  * Initialize the seven segment display
  void sevenseg_init(void){
    GPIO_UNGATE_PORT(SEV_SEG_PORT_ID);
    // Init the Seven Segment segment control pins as
47
     OUTPUT
    GPIO_INIT_PIN(SEV_SEG_PORT_ID, SEGA_PIN, GPIO_OUTPUT);
    GPIO_INIT_PIN(SEV_SEG_PORT_ID, SEGB_PIN, GPIO_OUTPUT);
49
    GPIO_INIT_PIN(SEV_SEG_PORT_ID, SEGC_PIN, GPIO_OUTPUT);
    {\tt GPIO\_INIT\_PIN} ({\tt SEV\_SEG\_PORT\_ID}\,,\,\,{\tt SEGD\_PIN}\,,\,\,{\tt GPIO\_OUTPUT})\,;
51
    GPIO_INIT_PIN(SEV_SEG_PORT_ID, SEGE_PIN, GPIO_OUTPUT);
    GPIO_INIT_PIN(SEV_SEG_PORT_ID, SEGF_PIN, GPIO_OUTPUT);
    GPIO_INIT_PIN(SEV_SEG_PORT_ID, SEGG_PIN, GPIO_OUTPUT);
    GPIO_INIT_PIN(SEV_SEG_PORT_ID, SEGDP_PIN, GPIO_OUTPUT);
    // Init the Seven Segment segment display pins as
     OUTPUT
```

```
GPIO_INIT_PIN(SEV_SEG_PORT_ID, SEG_DISP1_PIN,
     GPIO_OUTPUT);
    GPIO_INIT_PIN(SEV_SEG_PORT_ID, SEG_DISP2_PIN,
     GPIO_OUTPUT);
    GPIO_INIT_PIN(SEV_SEG_PORT_ID, SEG_DISP3_PIN,
     GPIO_OUTPUT);
    GPIO_INIT_PIN(SEV_SEG_PORT_ID, SEG_DISP4_PIN,
     GPIO_OUTPUT);
61
    //Init pit interrupts
    pit_enable();
    //Init timer 0
    pit_start_timer_interrupt (SEV_SEG_PIT_TIMER_NUMB,
     SEVEN_SEG_PIT_PERIOD, & sevenseg_interrupt_handler);
67
   * Sets only the selected segments as high. Setting the
     others as low
* @param epDet_segments = Array with the segments that
     should be set as on (Last element should be SEG_END)
void sevenseg_setSegs(seven_segment_seg_type_e*
     epSet_segments){
    //Clear all segments.
   GPIO-WRITE_MASK(SEV_SEG_PORT_ID, SEV_SEG_SEGMENT_MASK,
75
     GPIOLOW);
    //Set the selected segments to high
    for(unsigned short usCounter = 0; epSet_segments[
     usCounter | != SEG_END; usCounter++){
      GPIO_WRITE_PIN(SEV_SEG_PORT_ID, epSet_segments[
     usCounter], GPIO_HIGH);
79
```

```
* Shows the value written in the segment pins to the
   * given display after clearing the others
* @param eDisplay the display to initialize.
   */
87 void sevenseg_setDisp(seven_segment_disp_type_e eDisplay)
    //Clear all displays
    GPIO-WRITE_MASK(SEV_SEG_PORT_ID, SEV_SEG_DISP_MASK,
     GPIOLOW);
    //Activate the selected display
    GPIO_WRITE_PIN(SEV_SEG_PORT_ID, eDisplay, GPIO_HIGH);
93
   * Shows the passed value in hexadecimal format in the
      seven segment display.
   * @param uiHex the value to be printed
  void sevenseg_printHex(unsigned int uiHex){
    usIsHex = 1;
    uiPrintVal = uiHex;
101 }
   * Shows the passed value in decimal format in the seven
      segment display.
  * @param uiDec the value to be printed
105
void sevenseg_printDec(unsigned int uiDec){
    usIsHex = 0;
    uiPrintVal = uiDec;
111
```

```
* Converts the less significative decimal digit of the
      argument into it's seven
   * segment display configuration
   * @param usDec the value to be converted (-1 if none
      should be displayed)
   * @param epRet address for results (should be a
      allocated array of minimal 9 elements)
117
   * @return epRet
   */
119
  seven_segment_seg_type_e* sevenseg_dec2segArray(unsigned
      short usDec, seven_segment_seg_type_e* epRet){
     if(usDec < 0)
121
      epRet[0] = SEG\_END;
       return epRet;
123
    }
    epRet[0] = SEG_A;
125
    epRet[1] = SEG_B;
    epRet[2] = SEG_C;
127
    epRet[3] = SEGD;
    epRet[4] = SEG_E;
129
    epRet[5] = SEG_F;
    epRet[6] = SEG_G;
131
    epRet[7] = SEG\_END;
    switch (usDec%10){
133
     case 0:
      //{SEG_A,SEG_B,SEG_C,SEG_D,SEG_G,SEG_E,SEG_F,SEG_END
135
      epRet[7] = SEG\_END;
      break;
137
     case 1:
      //{SEG_B,SEG_C,SEG_END};
      epRet[0] = SEG_B;
      epRet[1] = SEG_C;
141
      epRet[2] = SEG\_END;
      break;
143
```

```
case 2:
       //{SEG_A, SEG_B, SEG_G, SEG_D, SEG_E, SEG_END};
145
       epRet[2] = SEG_G;
       epRet[5] = SEG\_END;
147
       break;
     case 3:
149
       //{SEG_A,SEG_B,SEG_C,SEG_D,SEG_G,SEG_END}
       epRet[4] = SEG_G;
151
       epRet[5] = SEG\_END;
       break;
153
     case 4:
       //\{SEG\_G, SEG\_B, SEG\_C, SEG\_F, SEG\_END\}
155
       epRet[0] = SEG_G;
       epRet[3] = SEG_F;
157
       epRet[4] = SEG\_END;
       break;
159
     case 5:
       //{SEG_A,SEG_G,SEG_C,SEG_D,SEG_F,SEG_END}
161
       epRet[1] = SEG_G;
       epRet[4] = SEG_F;
163
       epRet[5] = SEG\_END;
       break;
165
     case 6:
       //{SEG_A,SEG_G,SEG_C,SEG_D,SEG_E,SEG_F,SEG_END}
167
       epRet[1] = SEG_G;
       epRet[6] = SEG\_END;
169
       break;
     case 7:
171
       //{SEG_A, SEG_B, SEG_C, SEG_END}
       epRet[3] = SEG\_END;
173
       break;
     case 8:
       //\{SEG\_A, SEG\_B, SEG\_C, SEG\_D, SEG\_E, SEG\_F, SEG\_G, SEG\_END\}
177
       break;
     case 9:
       //SEG_A, SEG_B, SEG_C, SEG_F, SEG_G, SEG_END}
179
```

```
epRet[3] = SEG_F;
       epRet[4] = SEG_G;
181
       epRet[5] = SEG\_END;
       break;
183
    return epRet;
185
187
   * Converts the less significative hexadecimal digit of
189
      the argument into it's seven
   * segment display configuration
   * @param usHex the value to be converted (-1) if none
      should be displayed)
   * @param epRet address for results (should be a
      allocated array of minimal 9 elements)
193
   * @return epRet
195
  seven_segment_seg_type_e* sevenseg_hex2segArray(unsigned
      short usHex, seven_segment_seg_type_e* epRet){
     if(usHex < 0)
197
       epRet[0] = SEG\_END;
       return epRet;
199
    epRet[0] = SEG_A;
    epRet[1] = SEG_B;
    epRet[2] = SEG_C;
203
    epRet[3] = SEG_D;
    epRet[4] = SEG_E;
205
    epRet[5] = SEG_F;
    epRet[6] = SEG_G;
207
    epRet[7] = SEG\_END;
    switch (usHex%16){
209
       case 0:
       case 1:
211
```

```
case 2:
       case 3:
213
       case 4:
       case 5:
215
       case 6:
       case 7:
217
       case 8:
       case 9:
219
         return sevenseg_dec2segArray(usHex%16, epRet);
         break;
221
       case 10: //A
         //\{SEG\_A, SEG\_B, SEG\_C, SEG\_G, SEG\_E, SEG\_F, SEG\_END\}
223
         epRet[3] = SEG_G;
         epRet[6] = SEG\_END;
225
         break;
       case 11: //B (b)
227
         //{SEG_G,SEG_F,SEG_C,SEG_D,SEG_E,SEG_END}
         epRet[0] = SEG_G;
229
         epRet[1] = SEG_F;
         epRet[5] = SEG\_END;
231
         break;
       case 12: //C
233
         //{SEG_A,SEG_E,SEG_F,SEG_D,SEG_END}
         epRet[1] = SEG_E;
235
         epRet[2] = SEG_F;
         epRet[4] = SEG\_END;
237
         break;
       case 13: //D (d)
239
         //{SEG_G,SEG_B,SEG_C,SEG_D,SEG_E,SEG_END}
         epRet[0] = SEG_G;
241
         epRet[5] = SEG\_END;
         break;
       case 14: //E
         //{SEG_A,SEG_G,SEG_F,SEG_D,SEG_E,SEG_END}
245
         epRet[1] = SEG_G;
         epRet[2] = SEG_F;
^{247}
```

```
epRet[5] = SEG\_END;
          break;
249
        case 15: //F
          //\{SEG\_A, SEG\_E, SEG\_F, SEG\_G, SEG\_END\}
251
          epRet[1] = SEG_E;
          epRet[2] = SEG_F;
253
          epRet[3] = SEG_G;
          epRet[4] = SEG\_END;
255
          break;
257
     return epRet;
259 }
```

7.9 ../Sources/GPIO/gpio hal.h

```
| #include "KL25Z/es670_peripheral_board.h"
/* GPIO input / output */
 #define GPIO_INPUT
                                       0x00U
17 #define GPIO_OUTPUT
                                       0x01U
19 #define GPIO_MUX_ALT
                                       0x01u
#define GPIO_HIGH
  #define GPIOLOW
                       0
23
  * Ungates the clock for a gpio port
   * @param PORT_ID the GPIO port id(A,B)
  */
  #define GPIO_UNGATE_PORT(PORT_ID) \
   _GPIO_UNGATE_PORT(PORT_ID)
31 //Wrapper macro above is needed for argument expansion
     when using concatenation
 #define _GPIO_UNGATE_PORT(PORT_ID) \
    /* un-gate port clock*/\
      SIM\_SCGC5 = SIM\_SCGC5\_PORT \#\# PORT\_ID (
     CGC_CLOCK_ENABLED)
35
  * inits a pin as GPIO in the given direction
   * @param PORT_ID the GPIO port id(A,B)
  * @param PIN_NUM pin number in port
   * @param DIR pin direction (GPIO_HIGH, GPIO_LOW)
  */
 #define GPIO_INIT_PIN(PORT_ID, PIN_NUM, DIR)\
      _GPIO_INIT_PIN(PORT_ID, PIN_NUM, DIR)
```

```
45 //Wrapper macro above is needed for argument expansion
     when using concatenation
  #define _GPIO_INIT_PIN(PORT_ID, PIN_NUM, DIR)\
      /* set pin as gpio */
      PORT ## PORT_ID ## _PCR ## PIN_NUM = PORT_PCR_MUX(
     GPIO_MUX_ALT);\
      /* Set pin direction */\
49
      if(DIR = GPIO\_OUTPUT) \{ \setminus \}
        GPIO ## PORT_ID ## _PDDR \mid= GPIO_PDDR_PDD(0x01 <<
     PIN_NUM);
      }else{\
        GPIO ## PORT_ID ## _PDDR &= ~GPIO_PDDR_PDD(0x01 <<
     PIN_NUM);\
   * Writes a pin with the given value
  * @param PORT_ID the GPIO port id(A,B)
   * @oaram PIN_NUM pin number in port
  * @param VAL pin value (GPIO_HIGH, GPIO_LOW)
   */
63 #define GPIO_WRITE_PIN(PORT_ID, PIN_NUM, VAL)
      _GPIO_WRITE_PIN(PORT_ID, PIN_NUM, VAL)
  //Wrapper macro above is needed for argument expansion
     when using concatenation
67 #define _GPIO_WRITE_PIN(PORT_ID, PIN_NUM, VAL)\
    if(VAL = GPIO_HIGH) \{ \setminus \}
      GPIO ## PORT_ID ## _PSOR = GPIO_PSOR_PTSO( (0x01U <<
     PIN_NUM));\
    } else {\
      GPIO ## PORT_ID ## _PCOR = GPIO_PCOR_PTCO( (0x01U <<
     PIN_NUM));\
    }
73
```

```
* Writes the given value to the pins given in the MASK
   * @param PORT_ID the GPIO port id(A,B)
* @param MASK 31 bit Mask with 1 in the bits
      corresponding to the pins of interest.
   * @param VAL pins value (GPIO_HIGH, GPIO_LOW)
79
  #define GPIO_WRITE_MASK(PORT_ID, MASK, VAL)\
      _GPIO_WRITE_MASK(PORT_ID, MASK, VAL)
83 #define _GPIO_WRITE_MASK(PORT_ID, MASK, VAL) \
    if(VAL = GPIO\_HIGH) \{ \setminus \}
      GPIO ## PORT_ID ## _PSOR = GPIO_PSOR_PTSO(MASK);\
85
    } else {\
      GPIO ## PORT_ID ## _PCOR = GPIO_PCOR_PTCO(MASK);\
89
91
   * Reads the status of a GPIO PIN
   * @param PORT_ID the GPIO port id(A,B)
   * @param PIN_NUM pin number in port
   * @param VAL pin value (GPIO_HIGH, GPIO_LOW)
97 #define GPIO_READ_PIN(PORT_ID, PIN_NUM)\
      _GPIO_READ_PIN(PORT_ID, PIN_NUM)
  //Wrapper macro above is needed for argument expansion
      when using concatenation
| #define GPIO_READ_PIN(PORT_ID, PIN_NUM)
      ((GPIO \#\# PORD\_ID \#\# \_PDIR \& (0x01u << PIN\_NUM)) >>
     PIN_NUM) )
103
  #endif /* SOURCES_GPIO_GPIO_HAL_H_ */
```

7.10 .../Sources/Main/es670.c

```
#include "fsl_device_registers.h"
2 #include "KL25Z/es670_peripheral_board.h"
  #include "LedSwi/ledswi_hal.h"
4 #include "Mcg/mcg_hal.h"
  #include "Buzzer/buzzer_hal.h"
6 #include "SevenSeg/sevenseg_hal.h"
  #include "PIT/pit_hal.h"
s #include "Util/util.h"
  int main(void)
12 {
    mcg_clockInit();
    buzzer_init();
14
    ledswi_initLedSwitch(3,1);
    sevenseg_init();
16
    sevenseg_printHex(0xABCDu);
    unsigned short usPrintHex = 1;
    unsigned short usLedOn = 1;
    while (1) {
20
      if (ledswi_getSwitchStatus(3) == SWITCH_ON) {
        usPrintHex = !usPrintHex;
22
        usLedOn = !usLedOn;
        if (usPrintHex) {
24
           sevenseg_printHex(0xABCDu);
        } else {
26
           sevenseg_printDec(0xABCDu);
        }
28
        if (usLedOn) {
           ledswi_setLed(4);
        } else {
           ledswi_clearLed(4);
32
      }
34
```

```
/* Never leave main */
return 0;
```

7.11 ../Sources/Buzzer/buzzer'hal.c

```
2 /* File name:
                        buzzer_hal.c
  /* File description: File dedicated to the hardware
     abstraction layer*/
                        related buzzer from the peripheral
     board
  /* Author name:
                        dloubach
  /* Creation date:
                        12jan2016
  /* Revision date:
                      13\,\mathrm{abr}2016
#include "GPIO/gpio_hal.h"
  #include "buzzer_hal.h"
#include "KL25Z/es670_peripheral_board.h"
 #include "PIT/pit_hal.h"
14
  * Initialize the buzzer device
void buzzer_init(void)
   GPIO_UNGATE_PORT(BUZZER_PORT_ID);
```

```
GPIO_INIT_PIN(BUZZER_PORT_ID, BUZZER_PIN, GPIO_OUTPUT);
    pit_enable();
22
24
26
   * Clear the buzzer
  void buzzer_clearBuzz(void)
      {\tt GPIO\_WRITE\_PIN}({\tt BUZZER\_PORT\_ID},\ {\tt BUZZER\_PIN},\ {\tt GPIO\_LOW})\,;
34
36
   * Set the buzzer
  void buzzer_setBuzz(void)
    GPIO_WRITE_PIN(BUZZER_PORT_ID, BUZZER_PIN, GPIO_HIGH);
44
   * Handler for buzzer interruptions
48 void _buzzer_interrupt_handler(void){
    buzzer_setBuzz();
    buzzer_clearBuzz();
    pit_mark_interrupt_handled(BUZZER_PIT_TIMER_NUMB);
52 }
   * Starts the buzzer with the specified period
56
```

7.12 ../Sources/Buzzer/buzzer'hal.h

```
11 #ifndef SOURCES_BUZZER_HAL_H_
  #define SOURCES_BUZZER_HAL_H_
  /**
  * Initialize the buzzer device
void buzzer_init(void);
19
  * Clear the buzzer
void buzzer_clearBuzz(void);
25
  * Set the buzzer
   */
void buzzer_setBuzz(void);
   * Starts the buzzer with the specified period
   * @param uiPeriod The period of the buzzer signal, in
     clock cycles (40MHz)
  void buzzer_initPeriodic(unsigned int uiPeriod);
  * Stops any periodic buzzer signal
   */
void buzzer_stopPeriodic(void);
```

```
#endif /* SOURCES_BUZZER_HAL_H_ */
```

7.13 ../Sources/KL25Z/es670'peripheral'board.h

```
es 670\_peripheral\_board.h
  /* File name:
  /* File description: Header file containing the
     peripherals mapping */
                         of the peripheral board for the
     ES670 hardware*/
  /* Author name:
                        dloubach
  /* Creation date:
                        16out2015
  /* Revision date:
                        25\,\mathrm{fev}\,2016
10 #ifndef SOURCES_ES670_PERIPHERAL_BOARD_H_
  #define SOURCES_ES670_PERIPHERAL_BOARD_H_
  /* system includes */
14 #include <MKL25Z4.h>
                      General uC definitions
18 /* Clock gate control */
 #define CGC_CLOCK_DISABLED
                                        0x00U
```

```
20 #define CGC_CLOCK_ENABLED
                                      0x01U
22 /* GPIO DIRECTION
 #define GPIO_OUTPUT
                              0x01U
  /* Workaround for PORTID macro expansion to stop at
     port level*/
26 typedef int A;
  typedef int B;
28 typedef int C;
  typedef int D;
30 typedef int E;
                    END OF General uC definitions
                     BUZZER Definitions
36 #define BUZZER_PORT_BASE_PNT
                                      PORTD
                        /* peripheral port base pointer */
 #define BUZZER_GPIO_BASE_PNT
                        /* peripheral gpio base pointer */
38 #define BUZZER_PORT_ID
                                D
                  /* peripheral port identifier */
40 #define BUZZER_PIT_TIMER_NUMB
42 #define BUZZER_PIN
                                       1
                       /* buzzer pin */
  #define BUZZER_DIR
                                       kGpioDigitalOutput
44 #define BUZZER_ALT
                                       0x01u
                     END OF BUZZER definitions
```

```
LED and SWITCH Definitions
  #define LS_PORT_BASE_PNT
                                      PORTA
                         /* peripheral port base pointer */
50 #define LS_PORT_ID
                        /* peripheral port identifier*/
  #define LS_GPIO_BASE_PNT
                         /* peripheral gpio base pointer */
  /* THIS PIN CONFLICTS WITH PTA1 USED AS UARTO_RX IN THE
     OPENSDA SERIAL DEBUG PORT */
#define LS1_PIN
                                       1U
                         /* led/switch #1 pin */
  #define LS1_DIR_OUTPUT
                                       (GPIO_OUTPUT <<
     LS1_PIN)
56 #define LS1_DIR_INPUT
                                       (GPIO_OUTPUT <<
     LS1_PIN)
 #define LS1_ALT
                                       0x01u
                         /* GPIO alternative */
  /* THIS PIN CONFLICTS WITH PTA2 USED AS UARTO_TX IN THE
     OPENSDA SERIAL DEBUG PORT */
60 #define LS2_PIN
                                       2U
                         /* led/switch #2 pin */
 #define LS2_DIR_OUTPUT
                                       (GPIO_OUTPUT <<
     LS2_PIN)
62 #define LS2_DIR_INPUT
                                       (GPIO_OUTPUT <<
     LS2_PIN)
 #define LS2_ALT
                                       LS1\_ALT
                                       4U
  #define LS3_PIN
                         /* led/switch #3 pin */
66 #define LS3_DIR_OUTPUT
                                       (GPIO\_OUTPUT <<
     LS3_PIN)
 #define LS3_DIR_INPUT
                                       (GPIO_OUTPUT <<
     LS3_PIN)
```

```
68 #define LS3_ALT
                                         LS1\_ALT
70 #define LS4_PIN
                                         5U
                          /* led/switch #4 pin */
  #define LS4_DIR_OUTPUT
                                         (GPIO_OUTPUT <<
     LS4_PIN)
<sub>72</sub> #define LS4_DIR_INPUT
                                         (GPIO_OUTPUT <<
     LS4_PIN)
  #define LS4_ALT
                                         LS1_ALT
74
                      END OF LED and SWITCH definitions
                      SEVEN SEGMENT DISPLAY Definitions
78 #define SEV_SEG_PORT_BASE_PNT
                                        PORTC
                         /* peripheral port base pointer */
  #define SEV_SEG_PORT_ID
                         /* peripheral port identifier*/
80 #define SEV_SEG_GPIO_BASE_PNT
                                       PTC
                         /* peripheral gpio base pointer */
82 #define SEV_SEG_PIT_TIMER_NUMB
      /* timer number for seven seg PIT */
  #define SEVEN_SEG_PIT_PERIOD
                                     0x0001E847
       /*125000 \text{ cycles} = 3.125 \text{ms} (40 \text{MHz}) */
  #define SEGA_PIN
                                          0
                          /* Segment A*/
86 #define SEGA_DIR_OUTPUT
                                          (GPIO_OUTPUT <<
     SEGA_PIN)
  #define SEGA_ALT
                                          0x01u
                           /* GPIO alternative */
  #define SEGB_PIN
                                          1
```

```
90 #define SEGB_DIR_OUTPUT
                                         (GPIO_OUTPUT <<
      SEGB_PIN)
  #define SEGB_ALT
                                         SEGA_ALT
  #define SEGC_PIN
94 #define SEGC_DIR_OUTPUT
                                         (GPIO_OUTPUT <<
      SEGC_PIN)
  #define SEGC_ALT
                                         SEGA_ALT
  #define SEGD_PIN
98 #define SEGD_DIR_OUTPUT
                                         (GPIO_OUTPUT <<
      SEGD_PIN)
  #define SEGD_ALT
                                         SEGA_ALT
100
  #define SEGE_PIN
102 #define SEGE_DIR_OUTPUT
                                         (GPIO_OUTPUT <<
      SEGE_PIN)
  #define SEGE_ALT
                                         SEGA_ALT
104
  #define SEGF_PIN
#define SEGF_DIR_OUTPUT
                                         (GPIO_OUTPUT <<
      SEGF_PIN)
  #define SEGF_ALT
                                         SEGA_ALT
108
  #define SEGG_PIN
110 #define SEGG_DIR_OUTPUT
                                         (GPIO_OUTPUT <<
      SEGG_PIN)
  #define SEGG_ALT
                                         SEGA_ALT
112
  #define SEGDP_PIN
#define SEGDP_DIR_OUTPUT
                                          (GPIO_OUTPUT <<
      SEGDP_PIN)
  #define SEGDP_ALT
                                          SEGA_ALT
116
  #define SEG_DISP1_PIN
                                          13
```

```
#define SEG_DISP1_DIR_OUTPUT
                                           (GPIO_OUTPUT <<
      SEG_DISP1_PIN)
  #define SEG_DISP1_ALT
                                           SEGA_ALT
120
  #define SEG_DISP2_PIN
                                           12
| #define SEG_DISP2_DIR_OUTPUT
                                           (GPIO_OUTPUT <<
      SEG_DISP2_PIN)
  #define SEG_DISP2_ALT
                                           SEGA\_ALT
124
  #define SEG_DISP3_PIN
                                           11
#define SEG_DISP3_DIR_OUTPUT
                                           (GPIO_OUTPUT <<
      SEG_DISP3_PIN)
  #define SEG_DISP3_ALT
                                           SEGA_ALT
128
  #define SEG_DISP4_PIN
                                           10
130 #define SEG_DISP4_DIR_OUTPUT
                                           (GPIO_OUTPUT <<
      SEG_DISP4_PIN)
  #define SEG_DISP4_ALT
                                           SEGA_ALT
132
                      END of SEVEN SEGMENT DISPLAY
      Definitions
134
_{136}|\#endif\ /*\ SOURCES\_ES670\_PERIPHERAL\_BOARD\_H\_\ */
```

7.14 ../Sources/Util/util.h

```
Those delays were tested under the
      following:
                         core clock @ 40MHz
                         bus clock @ 20MHz
  /* Author name:
                         dloubach
  /* Creation date:
                         09 \mathrm{jan} 2015
10 /* Revision date:
                        13\,\mathrm{abr}2016
  #ifndef UTIL_H
4 #define UTIL_H
   * generates ~ 088 micro sec
  void util_genDelay088us(void);
20
   * generates ~ 250 micro sec
  */
  void util_genDelay250us(void);
26
  /* generates ~ 1 mili sec
  void util_genDelay1ms(void);
32
```

```
/**
    * generates ~ 10 mili sec

*/
void util_genDelay10ms(void);

*#endif /* UTIL_H */
```

7.15 ../Sources/Util/util.c

```
#include "util.h"
   * generates ~ 088 micro sec
void util_genDelay088us(void)
      char i;
22
      for (i=0; i<120; i++)
24
           __asm("NOP");
          __asm("NOP");
26
          __asm("NOP");
          __asm("NOP");
28
          __asm("NOP");
           __asm("NOP");
30
          _asm("NOP");
          __asm("NOP");
32
           __asm("NOP");
          __asm("NOP");
          __asm("NOP");
           __asm("NOP");
36
          _asm("NOP");
          __asm("NOP");
38
          __asm("NOP");
40
   * generates ~
                    250 micro sec
```

```
*/
  void util_genDelay250us(void)
      char i;
50
      for (i=0; i<120; i++)
           _asm("NOP");
           __asm("NOP");
54
           __asm("NOP");
           __asm("NOP");
56
           __asm("NOP");
           __asm("NOP");
           __asm("NOP");
           __asm("NOP");
60
           __asm("NOP");
           __asm("NOP");
62
      }
      util_genDelay088us();
      util_genDelay088us();
66 }
68
     generates ~
                    1 mili sec
  void util_genDelay1ms(void)
74 {
      util_genDelay250us();
      util_genDelay250us();
76
      util_genDelay250us();
      util_genDelay250us();
78
```

```
* generates ~
                    10 mili sec
  void util_genDelay10ms(void)
86 {
      util_genDelay1ms();
      util_genDelay1ms();
      util_genDelay1ms();
      util_genDelay1ms();
90
      util_genDelay1ms();
      util_genDelay1ms();
92
      util_genDelay1ms();
      util_genDelay1ms();
94
      util_genDelay1ms();
      util_genDelay1ms();
96
```