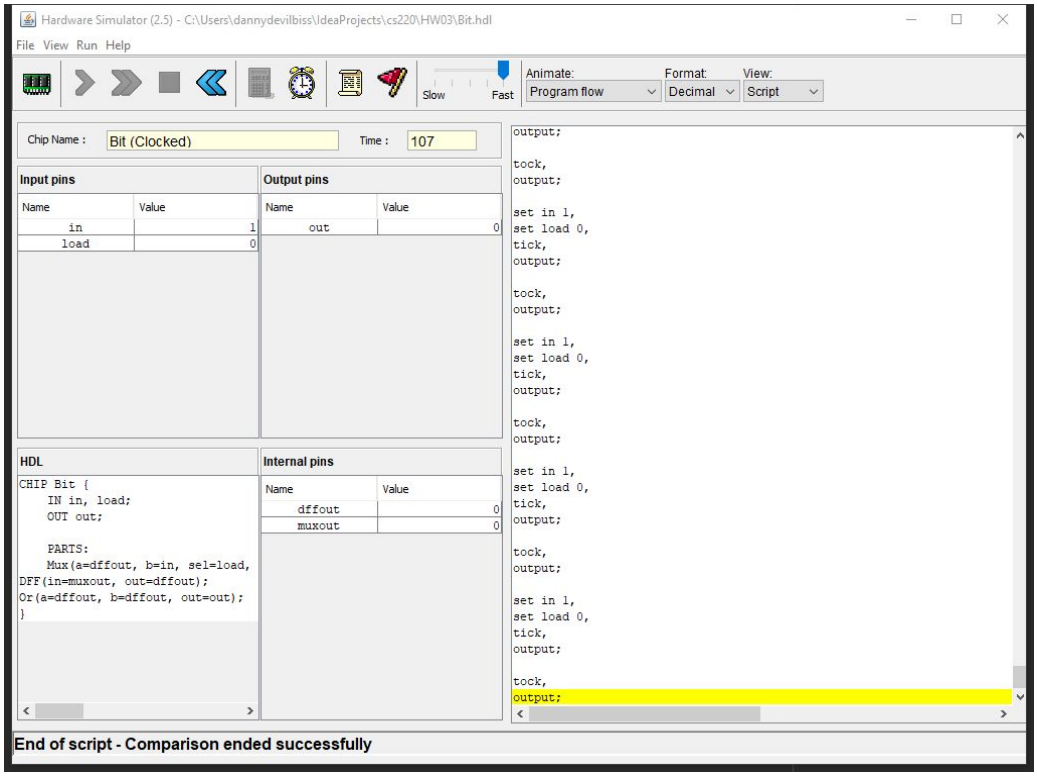
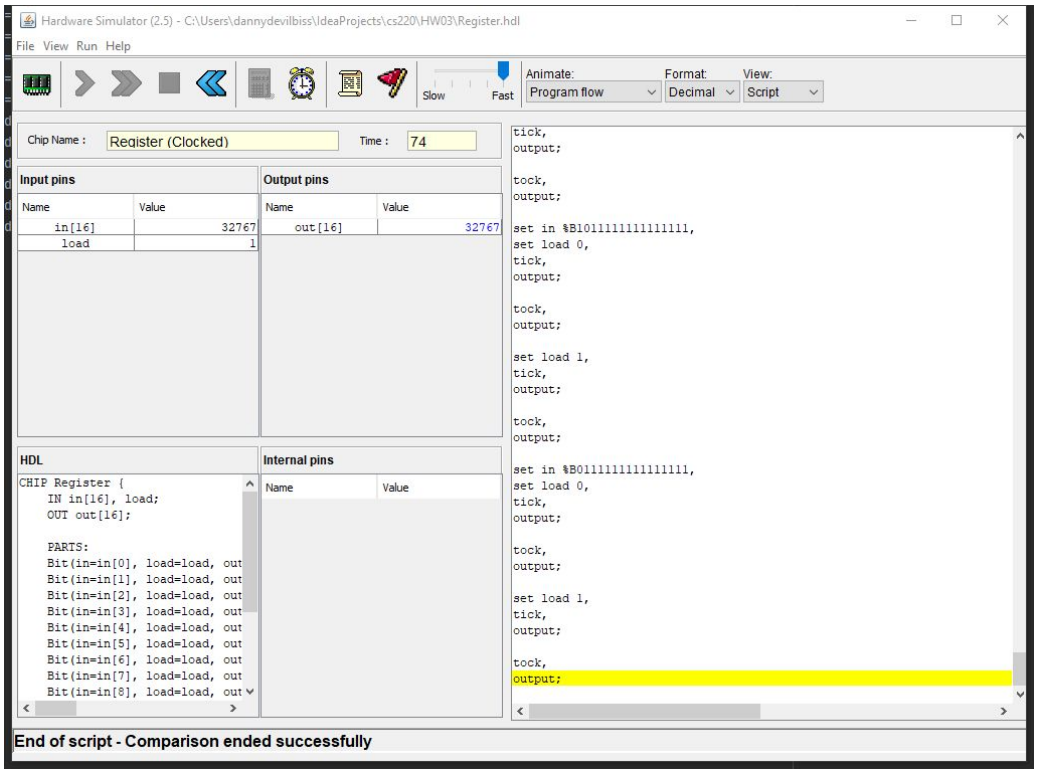
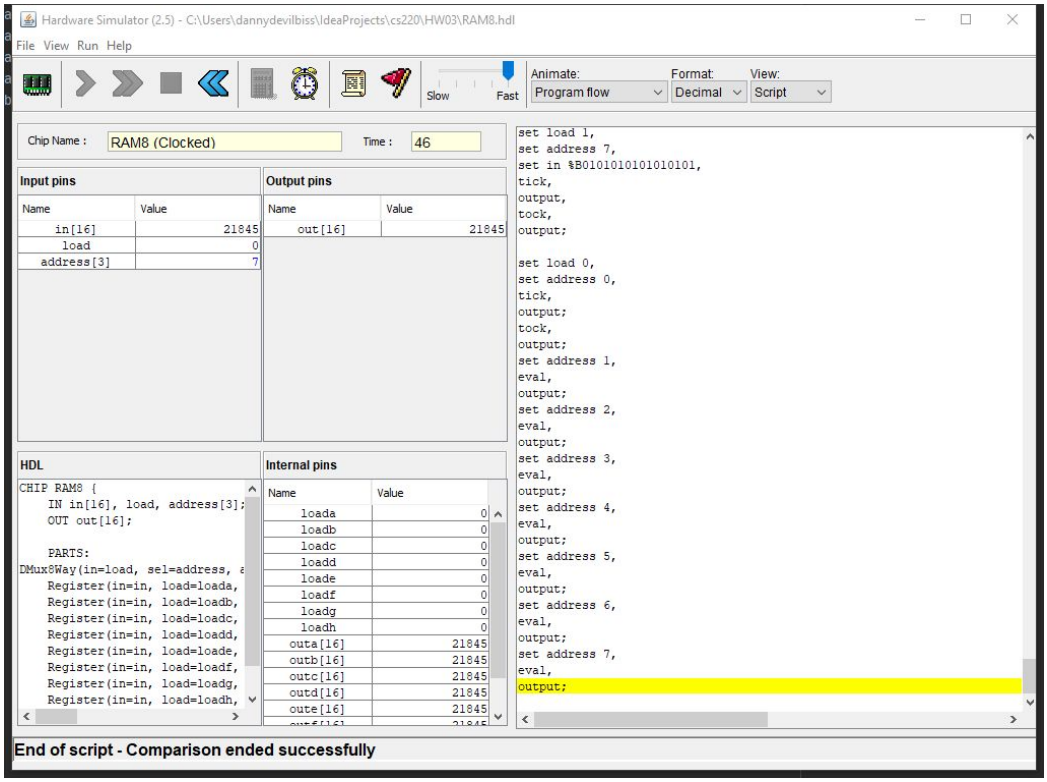
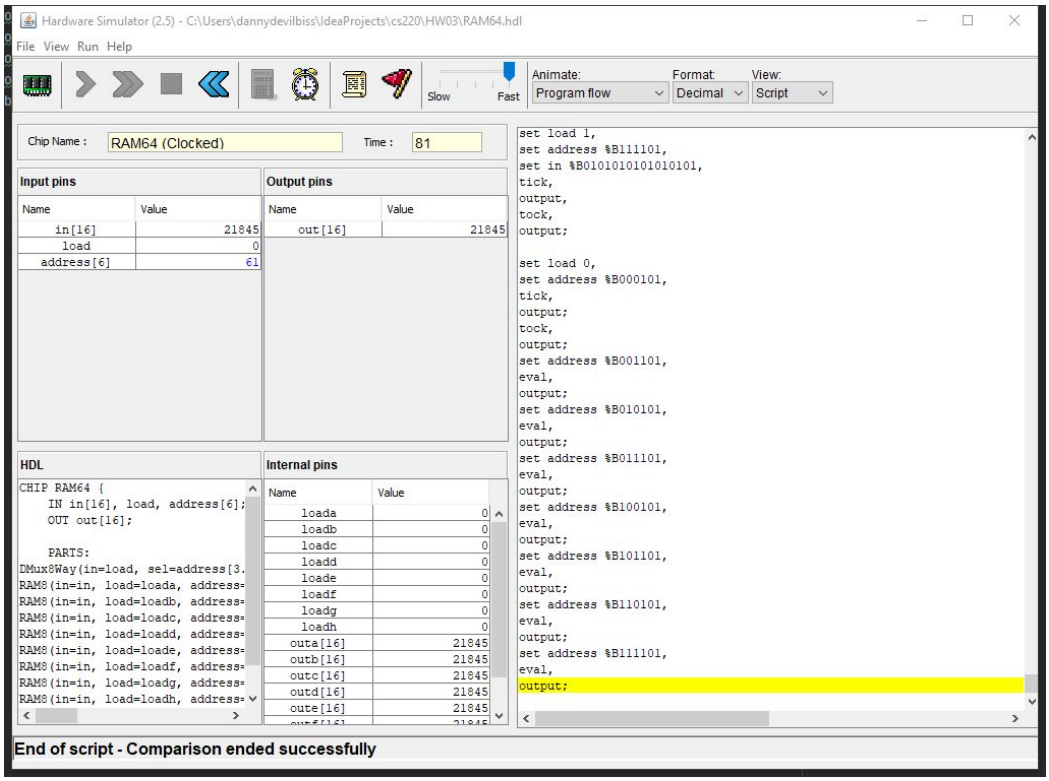
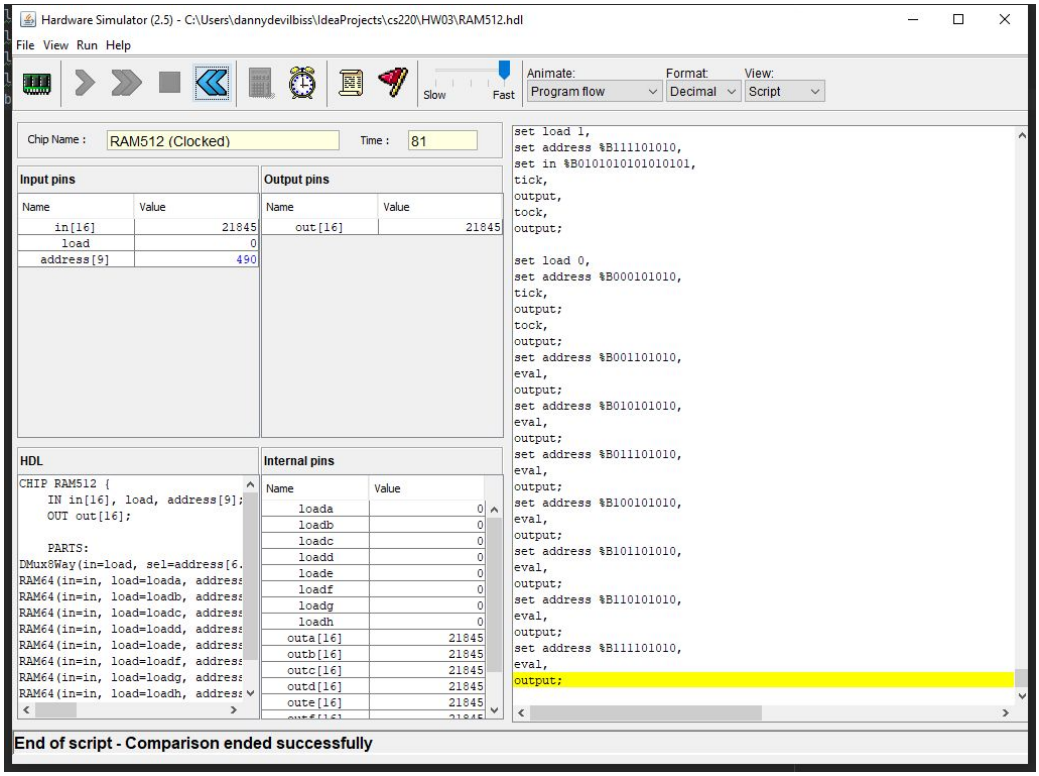
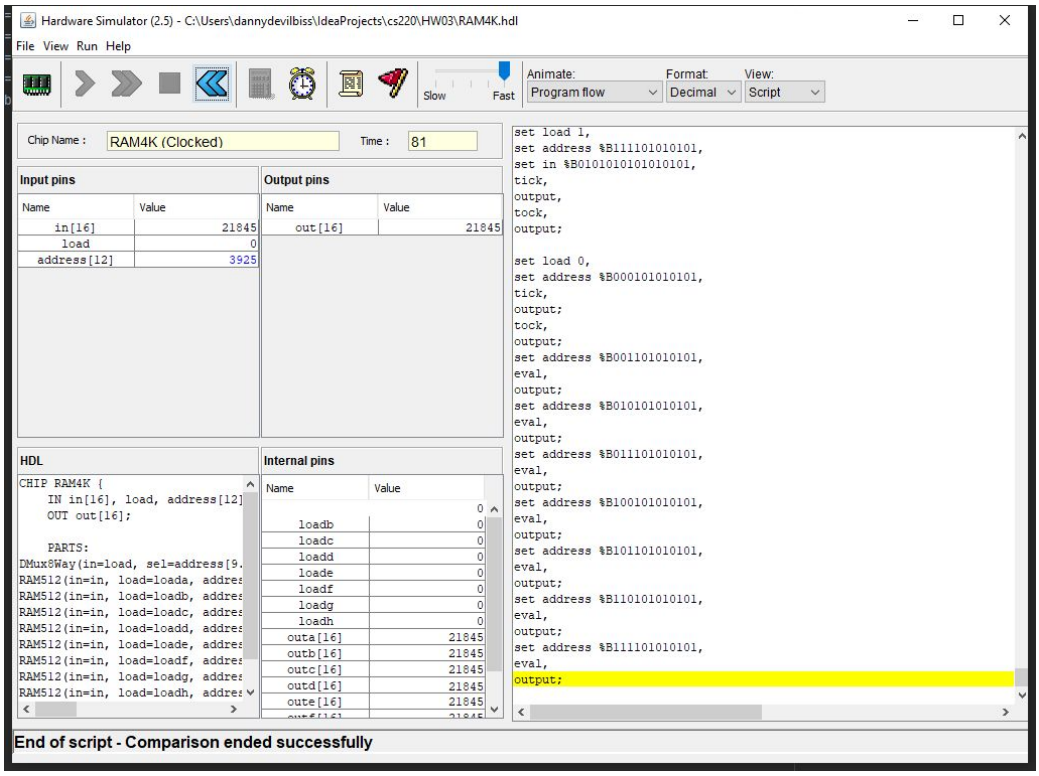

Hardware Simulator (2.5) - C:\Users\dannydevilbiss\IdeaProjects\cs220\HW03\Bit.hdl
File View Run Help
Slow
Fast
Animate:
Program flow
Format:
Decimal
View:
Script
Chip Name :
Bit (Clocked)
Time :
107
Input pins
Name
Value
in
1
load
0
Output pins
Name
Value
out
0
HDL
CHIP Bit {
IN in, load;
OUT out;
PARTS:
Mux(a=dffout, b=in, sel=load,
DFF(in=muxout, out=dffout);
Or(a=dffout, b=dffout, out=out);
}
Internal pins
Name
Value
dffout
0
muxout
0
output;
tock,
output;
set in 1,
set load 0,
tick,
output;
tock,
output;
set in 1,
set load 0,
tick,
output;
tock,
output;
set in 1,
set load 0,
tick,
output;
tock,
output;
set in 1,
set load 0,
tick,
output;
tock,
output;
End of script - Comparison ended successfully

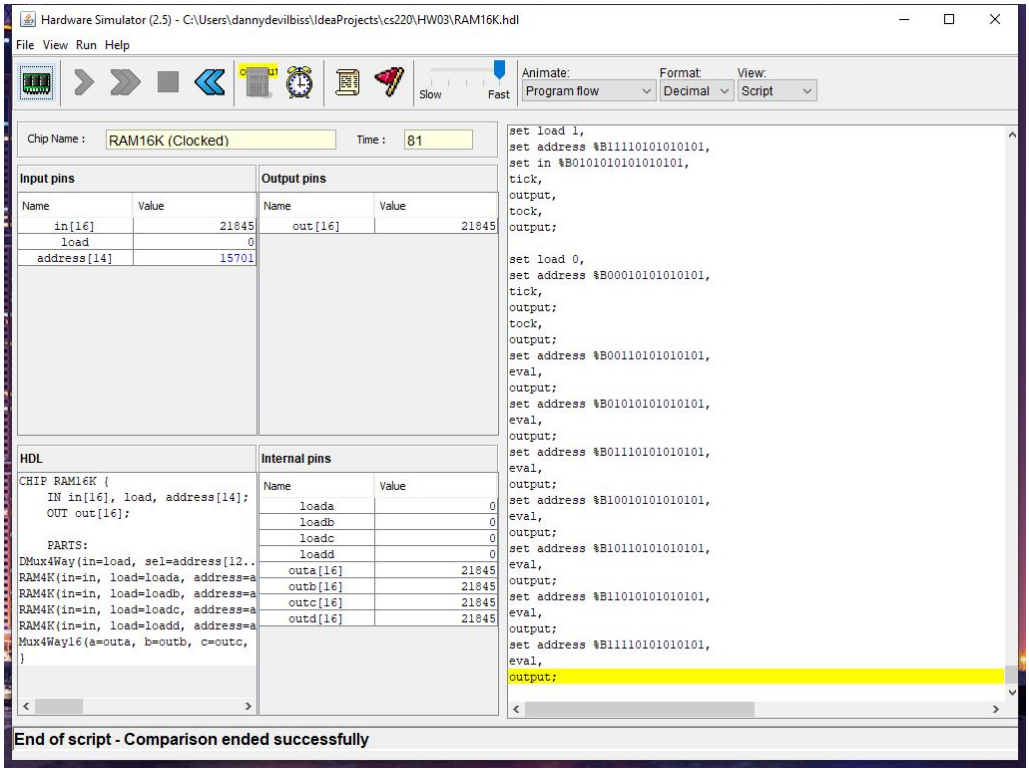

Hardware Simulator (2.5) - C:\Users\dannydevilbiss\IdeaProjects\cs220\HW03\Register.hdl
File View Run Help
Slow
Fast
Animate:
Program flow
Format:
Decimal
View:
Script
Chip Name :
Register (Clocked)
Time :
74
Input pins
Name
Value
in[16]
32767
load
1
Output pins
Name
Value
out[16]
32767
HDL
CHIP Register {
IN in[16], load;
OUT out[16];
PARTS:
Bit(in=in[0], load=load, out
Bit(in=in[1], load=load, out
Bit(in=in[2], load=load, out
Bit(in=in[3], load=load, out
Bit(in=in[4], load=load, out
Bit(in=in[5], load=load, out
Bit(in=in[6], load=load, out
Bit(in=in[7], load=load, out
Bit(in=in[8], load=load, out
Internal pins
Name
Value
tick,
output;
tock,
output;
set in %B1011111111111111,
set load 0,
tick,
output;
tock,
output;
set load 1,
tick,
output;
tock,
output;
set in %B0111111111111111,
set load 0,
tick,
output;
tock,
output;
set load 1,
tick,
output;
tock,
output;
End of script - Comparison ended successfully

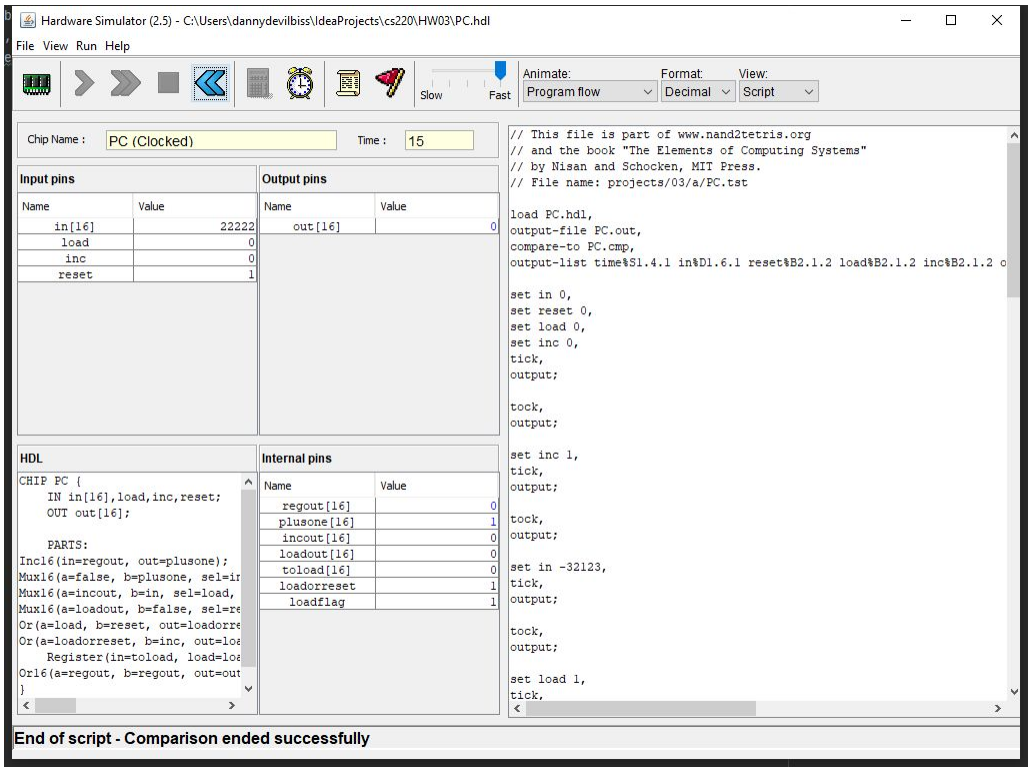

Hardware Simulator (2.5) - C:\Users\dannydevilbiss\IdeaProjects\cs220\HW03\RAM8.hdl
File View Run Help
Slow
Fast
Animate:
Program flow
Format:
Decimal
View:
Script
Chip Name :
RAM8 (Clocked)
Time :
46
Input pins
Name
Value
in[16]
21845
load
0
address[3]
7
Output pins
Name
Value
out[16]
21845
HDL
CHIP RAM8 {
IN in[16], load, address[3];
OUT out[16];
PARTS:
DMux8Way(in=load, sel=address,
Register(in=in, load=loada,
Register(in=in, load=loadb,
Register(in=in, load=loadc,
Register(in=in, load=loadd,
Register(in=in, load=loade,
Register(in=in, load=loadf,
Register(in=in, load=loadg,
Register(in=in, load=loadh,
Internal pins
Name
Value
loada
0
loadb
0
loadc
0
loadd
0
loade
0
loadf
0
loadg
0
loadh
0
outa[16]
21845
outb[16]
21845
outc[16]
21845
outd[16]
21845
oute[16]
21845
set load 1,
set address 7,
set in %B0101010101010101,
tick,
output,
tock,
output;
set load 0,
set address 0,
tick,
output;
tock,
output;
set address 1,
eval,
output;
set address 2,
eval,
output;
set address 3,
eval,
output;
set address 4,
eval,
output;
set address 5,
eval,
output;
set address 6,
eval,
output;
set address 7,
eval,
output;
End of script - Comparison ended successfully


Hardware Simulator (2.5) - C:\Users\dannydevilbiss\IdeaProjects\cs220\HW03\RAM64.hdl
File View Run Help
Slow
Fast
Animate:
Program flow
Format:
Decimal
View:
Script
Chip Name :
RAM64 (Clocked)
Time :
81
Input pins
Name
Value
in[16]
21845
load
0
address[6]
61
Output pins
Name
Value
out[16]
21845
HDL
CHIP RAM64 {
IN in[16], load, address[6];
OUT out[16];
PARTS:
DMux8Way(in=load, sel=address[3.
RAM8(in=in, load=loada, address=
RAM8(in=in, load=loadb, address=
RAM8(in=in, load=loadc, address=
RAM8(in=in, load=loadd, address=
RAM8(in=in, load=loade, address=
RAM8(in=in, load=loadf, address=
RAM8(in=in, load=loadg, address=
RAM8(in=in, load=loadh, address=
Internal pins
Name
Value
loada
0
loadb
0
loadc
0
loadd
0
loade
0
loadf
0
loadg
0
loadh
0
outa[16]
21845
outb[16]
21845
outc[16]
21845
outd[16]
21845
oute[16]
21845
set load 1,
set address %B111101,
set in %B0101010101010101,
tick,
output,
tock,
output;
set load 0,
set address %B000101,
tick,
output;
tock,
output;
set address %B001101,
eval,
output;
set address %B010101,
eval,
output;
set address %B011101,
eval,
output;
set address %B100101,
eval,
output;
set address %B101101,
eval,
output;
set address %B110101,
eval,
output;
set address %B111101,
eval,
output;
End of script - Comparison ended successfully


Hardware Simulator (2.5) - C:\Users\dannydevilbiss\IdeaProjects\cs220\HW03\RAM512.hdl
File View Run Help
Slow
Fast
Animate:
Program flow
Format:
Decimal
View:
Script
Chip Name :
RAM512 (Clocked)
Time :
81
Input pins
Name
Value
in[16]
21845
load
0
address[9]
490
Output pins
Name
Value
out[16]
21845
HDL
CHIP RAM512 {
IN in[16], load, address[9];
OUT out[16];
PARTS:
DMux8Way(in=load, sel=address[6.
RAM64(in=in, load=loada, address
RAM64(in=in, load=loadb, address
RAM64(in=in, load=loadc, address
RAM64(in=in, load=loadd, address
RAM64(in=in, load=loade, address
RAM64(in=in, load=loadf, address
RAM64(in=in, load=loadg, address
RAM64(in=in, load=loadh, address
Internal pins
Name
Value
loada
0
loadb
0
loadc
0
loadd
0
loade
0
loadf
0
loadg
0
loadh
0
outa[16]
21845
outb[16]
21845
outc[16]
21845
outd[16]
21845
oute[16]
21845
set load 1,
set address %B111101010,
set in %B0101010101010101,
tick,
output,
tock,
output;
set load 0,
set address %B000101010,
tick,
output;
tock,
output;
set address %B001101010,
eval,
output;
set address %B010101010,
eval,
output;
set address %B011101010,
eval,
output;
set address %B100101010,
eval,
output;
set address %B101101010,
eval,
output;
set address %B110101010,
eval,
output;
set address %B111101010,
eval,
output;
End of script - Comparison ended successfully


Hardware Simulator (2.5) - C:\Users\dannydevilbiss\IdeaProjects\cs220\HW03\RAM4K.hdl
File View Run Help
Slow
Fast
Animate:
Program flow
Format:
Decimal
View:
Script
Chip Name :
RAM4K (Clocked)
Time :
81
Input pins
Name
Value
in[16]
21845
load
0
address[12]
3925
Output pins
Name
Value
out[16]
21845
HDL
CHIP RAM4K {
IN in[16], load, address[12];
OUT out[16];
PARTS:
DMux8Way(in=load, sel=address[9.
RAM512(in=in, load=loada, addres
RAM512(in=in, load=loadb, addres
RAM512(in=in, load=loadc, addres
RAM512(in=in, load=loadd, addres
RAM512(in=in, load=loade, addres
RAM512(in=in, load=loadf, addres
RAM512(in=in, load=loadg, addres
RAM512(in=in, load=loadh, addres
Internal pins
Name
Value
0
loadb
0
loadc
0
loadd
0
loade
0
loadf
0
loadg
0
loadh
0
outa[16]
21845
outb[16]
21845
outc[16]
21845
outd[16]
21845
oute[16]
21845
set load 1,
set address %B111101010101,
set in %B0101010101010101,
tick,
output,
tock,
output;
set load 0,
set address %B000101010101,
tick,
output;
tock,
output;
set address %B001101010101,
eval,
output;
set address %B010101010101,
eval,
output;
set address %B011101010101,
eval,
output;
set address %B100101010101,
eval,
output;
set address %B101101010101,
eval,
output;
set address %B110101010101,
eval,
output;
set address %B111101010101,
eval,
output;
End of script - Comparison ended successfully


Hardware Simulator (2.5) - C:\Users\dannydevilbiss\IdeaProjects\cs220\HW03\RAM16K.hdl
File View Run Help
Animate: Program flow
Format: Decimal
View: Script
Slow
Fast
Chip Name : RAM16K (Clocked)
Time : 81
Input pins
Name Value
in[16] 21845
load 0
address[14] 15701
Output pins
Name Value
out[16] 21845
HDL
CHIP RAM16K {
IN in[16], load, address[14];
OUT out[16];
PARTS:
DMux4Way(in=load, sel=address[12..
RAM4K(in=in, load=loada, address=a
RAM4K(in=in, load=loadb, address=a
RAM4K(in=in, load=loadc, address=a
RAM4K(in=in, load=loadd, address=a
Mux4Way16(a=outa, b=outb, c=outc,
}
Internal pins
Name Value
loada 0
loadb 0
loadc 0
loadd 0
outa[16] 21845
outb[16] 21845
outc[16] 21845
outd[16] 21845
set load 1,
set address %B11110101010101,
set in %B0101010101010101,
tick,
output,
tock,
output;
set load 0,
set address %B00010101010101,
tick,
output;
tock,
output;
set address %B00110101010101,
eval,
output;
set address %B01010101010101,
eval,
output;
set address %B01110101010101,
eval,
output;
set address %B10010101010101,
eval,
output;
set address %B10110101010101,
eval,
output;
set address %B11010101010101,
eval,
output;
set address %B11110101010101,
eval,
output;
End of script - Comparison ended successfully


Hardware Simulator (2.5) - C:\Users\dannydevilbiss\IdeaProjects\cs220\HW03\PC.hdl
File View Run Help
Animate: Program flow
Format: Decimal
View: Script
Slow
Fast
Chip Name : PC (Clocked)
Time : 15
Input pins
Name Value
in[16] 22222
load 0
inc 0
reset 1
Output pins
Name Value
out[16] 0
HDL
CHIP PC {
IN in[16],load,inc,reset;
OUT out[16];
PARTS:
Inc16(in=regout, out=plusone);
Mux16(a=false, b=plusone, sel=in
Mux16(a=incout, b=in, sel=load,
Mux16(a=loadout, b=false, sel=re
Or(a=load, b=reset, out=loadorre
Or(a=loadorreset, b=inc, out=loa
Register(in=toload, load=loa
Or16(a=regout, b=regout, out=out
}
Internal pins
Name Value
regout[16] 0
plusone[16] 1
incout[16] 0
loadout[16] 0
toload[16] 0
loadorreset 1
loadflag 1
// This file is part of www.nand2tetris.org
// and the book "The Elements of Computing Systems"
// by Nisan and Schocken, MIT Press.
// File name: projects/03/a/PC.tst
load PC.hdl,
output-file PC.out,
compare-to PC.cmp,
output-list time%S1.4.1 in%D1.6.1 reset%B2.1.2 load%B2.1.2 inc%B2.1.2 o
set in 0,
set reset 0,
set load 0,
set inc 0,
tick,
output;
tock,
output;
set inc 1,
tick,
output;
tock,
output;
set in -32123,
tick,
output;
tock,
output;
set load 1,
tick,
End of script - Comparison ended successfully