CSE 234 Logic Circuits and Digital Design

Lab 5 – Advanced Traffic Light Controller

Lab Session (Exact Duration: 90min):

This is the same assignment as the previous lab but this time you will design the datapath with the counter and comparators to fully design the traffic light controller. For that purpose, you will use a counter and comparators to generate **p3s, p7s** and **p37s** signals. Also use the **resetT** signal in your datapath to clear timer (counter) content. Combine your datapath with the control unit you designed in the previous lab to have a complete digital design.

a. Use the schematic of the previous lab as your controller.
b. Design datapath including counter and comparators.
c. Design your resultant circuit using Logisim.
d. Simulate your resultant circuit to be sure it works flawless.

Rules:

DO NOT USE ANALYZE CIRCUIT PROPERTY OF LOGISIM.

Demo Session:

During demo, explain and simulate each step of your design. Do not forget you only have at most 4 minutes for that. Also you will answer any questions asked by the TA.