Di Wu

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EDUCATION

- **University of Science and Technology of China [🌐]** — Hefei, China
  B.S. in Applied Physics — Sep. 2021 - July 2025
  GPA: 3.91/4.30

- **University of Toronto[🌐]** — Toronto, Canada
  Ph.D. in Computer Science, supervised by Prof. Qizhen Zhang — Sep. 2025 - Dec. 2030 (expected)

  ○ **Relevant Coursework :**

Computer Architecture H	*93/100*	Computer Organization	*96/100*
Computer Programming A	*95/100*	Computational Method	*95/100*
Computer Network	*87/100*	Operation System	*85/100*
Linear Algebra	*100/100*	Artificial Intelligence Foundation	*93/100*
Probability Theory & Math. Statistics	*96/100*	Mathematical Analysis	*93/100*

  ○ **Honors & Rewards**

National Encouragement Scholarship	Oct. 2023
Third Prize in "Challenge Cup" National Extracurricular Acad. & Tech. Works Competition	Aug. 2024
Talented Class Scholarship	Oct. 2024
Outstanding Student Scholarship (First Prize) (1/48)	Oct. 2024

RESEARCH EXPERIENCE

- **Chair, the System and Networking Group, NUS** — July 2024 - Jan. 2025

  Supervisor: Prof. Bingsheng He and Prof. Yao Chen

  Project I: *Content Addressable Memory on FPGA*

  ○ Conducted analysis of FPGA-based CAM, enhancing the theoretical foundation for this DSA design.
  ○ Proposed a configurable DSP-based CAM architecture with high-performance and multi-query support.
  ○ Implemented an extensible CAM kernel with a hybrid HLS and RTL architecture on FPGA, now publicly available on GitHub.
  ○ Submitted a research paper detailing the design to DAC'25.

- **Research Assistant, Institute of ASIC, USTC** — June 2023 - June 2024

  Supervisor: Prof. Lei Zhao

  Project I: *Test and analysis of a SerDes prototype chip based on 180 nm CMOS process*
  ○ Designed an efficient testing scheme tailored to the chip's specific structure and key testing metrics.
  ○ Investigated chip configurations and built test code using Verilog HDL.
  ○ Utilized FPGA to test the relevant index shortness, providing data to enhance the feed-through design.

  Project II: *Simulation of the chip wiring S parameters*
  ○ Built the simulation models for chip wiring based on the encapsulated drawings.
  ○ Determined the S parameters to accommodate the shape material wiring, providing important information for the post-simulation circuit analysis.

- **Research Assistant, Institute of "Subtle Discernment", USTC** — Jan. 2023 - May 2023

  Supervisor: Prof. Jie Zeng

  Project I: *The effect of surface modification on electrocatalytic ammonia synthesis*
  ○ Analyzed catalyst surface modifications and their effects on ammonia synthesis performance.
  ○ Examined the impact and mechanisms of surface modification, completing key technical metrics for pub.

PUBLICATIONS
C=CONFERENCE, J=JOURNAL, O=ORAL PRESENTATION, S=IN SUBMISSION, T=THESIS

[C.1] Yao Chen, Feng Yu, **Di Wu**, Weng-Fai Wong and Bingsheng He. "**Configurable DSP-Based CAM Architecture for Data-Intensive Applications on FPGAs**," in *2025 62th Design Automation Conference (DAC)*. ⌗

[O.1] Jiacheng Guo, Jiajun Qin, Lei Zhao, **Wu Di**, Xinyu Bin, "**A 4×6.25-Gbs Serial Link Transmitter Core in 0.18-μm CMOS for high-speed front-end ASICs**," in *2024 24th IEEE Real Time Conference*.

[J.1] Yuheng Wu, Xiangdong Kong, Yechao Su, Jiankang Zhao, Yiling Ma, Tongzheng Ji, **Di Wu**, Junyang Meng, Yan Liu, Zhigang Geng, Jie Zeng, "**Thiol Ligand-Modified Au for Highly Efficient Electroreduction of Nitrate to Ammonia**," in *Precis. Chem. 2024, 2, 3, 112–119*.

SKILLS & INTERESTS

- **Programming Languages:** C/C++, Verilog/System Verilog, Python, LaTeX
- **Developer Tools:** Vivado, Vitis
- **Technologies/Frameworks:** Linux, Git, HLS, CUDA, Pytorch
- **Interests:** Students Chorus Member, Badminton