Di Wu

Email: wd3271391891@mail.ustc.edu.cn Tel: (86) 19359106198
Address: 96 Jinzhai Road – Baohe District, Anhui, P. R. China
Personal Web: home.ustc.edu.cn/~wd3271391891

Education

University of Science and Technology of China, Hefei, China September 2021 - Present
Bachelor of Science in Physics (expected in July 2025)
GPA (overall): **3.95/4.3**; **GPA** (major): **4.00/4.3**; **Ranking**: **2/47**
Core courses: Computer Programming A(95/100), Computational Method(95/100), Linear Algebra B1(100/100), Fast Electronics(93/100), Digital Circuits Experiment H(93/100), Probability Theory and Mathematical Statistics(96/100), Mathematical Analysis B(93/100), Electronic Circuits(93/100), Digital Circuits(92/100), Computer Network(87/100)

Outstanding Student Scholarship (First Prize) (1/38) November 2022
National Encouragement Scholarship October 2023

Research Experiences

Chair, Institute of ASIC, USTC
Supervisor: Prof. **Lei Zhao**
Project I: ***Test and analysis of a SerDes prototype chip based on 180 nm CMOS process*** June 2023 - Present

- Designed an efficient test scheme based the specific structure of the chip and essential test index.
- Investigated the configuration of each part of the chip and built test code by Verilog HDL.
- Used FPGA to test the relevant index shortness, provided information for the improvement of the feed-through design.

Project II: ***Simulation of the chip wiring S parameters*** November 2023 - Present

- Built the simulation models for chip wiring based on the encapsulated drawings.
- Found the S parameters of the specific shape material wiring, which could provide important information for the circuit post simulation.

Research Assistant, Institute of "Subtle Discernment", USTC
Supervisor: Prof. **Jie Zeng**
Project I: ***The effect of surface modification on electrocatalytic ammonia synthesis*** January 2023 - May 2023

- Investigated the structure of the modified surface of the catalyst and the performance of the ammonia synthesis.
- Explored the impact and mechanism of surface modification and finished the technical index of the paper.

Publication

- Jiacheng Guo; Jiajun Qin; Lei Zhao; **Di Wu**; Xinyu Bin. A 4×6.25-Gbs Serial Link Transmitter Core in 0.18-μm CMOS for high-speed front-end ASICs. Accepted by IEEE RT2024.
- Wu, Yuheng; Kong, Xiangdong; Su,Yechao; Zhao, Jiankang; Ma,Yiling; Ji,Tongzheng; **Wu, Di**; Meng, junyang; Liu, Yan; Geng, zhigang; Zeng, jie. Thiol Ligand-modified Au for Highly Efficient Electroreduction of Nitrate to Ammonia. Submitted to PC in ACS.

Leadership & Activities

USTC Students Chorus | member September 2022 - Present

- Took part in the choral concert.

Skills

Languages: Verilog/System Verilog, Python, C/C++, Latex, Matlab
Developer Tools: VS Code
Technologies/Frameworks: Linux, GitHub, Gitlab, Vivado