

Eldo Device Equations Manual

Software Version 6.3_1

Release 2004.1



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About this Manual

Introduction

This document is the *Eldo Device Equations Manual* to be used in conjunction with the Eldo software version v6.3_1.

Associated Documentation

Other documents and manuals that are referenced in this manual, and that you may need to refer to are:

- [Eldo User's Manual](#)

Manual Organization

Each chapter in this manual deals with a different topic as follows:

- [Chapter 1](#) describes the Diode Model Equations
- [Chapter 2](#) describes the Bipolar Junction Transistor Level 1 Model Equations
- [Chapter 3](#) describes the Mextram Bipolar Model 503 Equations
- [Chapter 4](#) describes the Bipolar Junction Transistor Level 5 Model Equations
- [Chapter 5](#) describes the VBIC Model Equations
- [Chapter 6](#) describes the HICUM Model Equations
- [Chapter 7](#) describes the Mextram Bipolar Model 504 Equations

- [**Chapter 8**](#) describes the Philips Modela Model
- [**Chapter 9**](#) describes the JFET and MESFET Model Equations
- [**Chapter 10**](#) describes the MOS Model Common Equations
- [**Chapter 11**](#) describes the MOS Levels 1, 2, and 3 Model Equations
- [**Chapter 12**](#) describes the MOS Levels 4, 5, and 6 Model Equations
- [**Chapter 13**](#) describes the Berkeley BSIM1 Model Equations
- [**Chapter 14**](#) describes the Berkeley BSIM2 Model Equations
- [**Chapter 15**](#) describes the EKV MOS Model Equations
- [**Chapter 16**](#) describes the MISNAN Model Equations
- [**Chapter 17**](#) describes the Berkeley BSIM3v2 Model Equations
- [**Chapter 18**](#) describes the Berkeley BSIM3v3 Model Equations
- [**Chapter 19**](#) describes the Berkeley BSIMSOI Model Equations
- [**Chapter 20**](#) describes the Berkeley BSIMSOI v2.x Model Equations
- [**Chapter 21**](#) describes the Philips MOS Model 9 (MM9) Equations
- [**Chapter 22**](#) describes the Berkeley BSIM4 Model Equations
- [**Chapter 23**](#) describes the TFT Polysilicon Model
- [**Chapter 24**](#) describes the Philips MOS Model 11 Equations
- [**Chapter 25**](#) describes the TFT Amorphous-Si Model
- [**Chapter 26**](#) describes the HiSIM Model
- [**Chapter 27**](#) describes the Surface-Potential-Based Compact (SP) Model
- [**Chapter 28**](#) describes the HVMOS Model

Table of Contents

About this Manual.....	iii
Introduction.....	iii
Associated Documentation	iii
Manual Organization	iii
 Chapter 1	
Diode Model Equations.....	1-1
Overview.....	1-1
Equivalent Circuit Schematics.....	1-2
Level 1 Equations	1-3
Level 1 Scaling.....	1-3
Level 1 Current Calculations	1-6
Level 1 Capacitance Calculations	1-6
Level 1 Temperature Effects	1-8
Level 1 Model Parameters	1-11
Level 2 Equations	1-13
Level 2 Scaling.....	1-13
Level 2 Current Calculations	1-14
Level 2 Capacitance Calculations	1-15
Level 2 Temperature Effects	1-16
Level 2 Model Parameters	1-17
Level 3 Equations	1-18
Level 3 Scaling.....	1-18
Level 3 DC calculation.....	1-18
Level 3 Capacitance calculation.....	1-19
Level 3 Model Parameters	1-19
Level 8 Equations	1-19
Level 8 Introduction.....	1-19
Level 8 Current Equations (DIOLEV \neq 9).....	1-20
Level 8 Current Equations (DIOLEV=9).....	1-21
Level 8 Capacitance Equations (DIOLEV \neq 9)	1-23
Level 8 Capacitance Equations (DIOLEV=9)	1-24
Level 8 Temperature Effects	1-25
Level 8 Parameters	1-29

Table of Contents (cont.)

Noise Equations for All Levels.....	1-31
Level 9 (Philips Diode Level 500).....	1-31
Level 9 (Philips Diode Level 500) Modeled Effects	1-31
Level 9 (Philips Diode Level 500) Equivalent Circuits	1-32
Level 9 (Philips Diode Level 500) Equations	1-33
Level 9 (Philips Diode Level 500) Parameters	1-40
Level 21	1-41
Level 21 Scaling.....	1-41
Level 21 Temperature Effects	1-45
Level 21 Current Calculations	1-49
Level 21 Capacitance Calculations	1-52
Level 21 Parameters.....	1-53
Chapter 2	
BJT Level 1 Equations	2-1
Overview.....	2-1
Definitions and Conventions	2-1
Current convention and displays	2-1
Structure conventions.....	2-1
NPN and PNP convention	2-2
Internal variables	2-2
Equivalent Circuit Schematics.....	2-3
For DC and TRANSIENT analysis.....	2-3
For AC and NOISE analysis	2-4
Scaling	2-5
DC Current Calculations.....	2-6
Collector and base currents	2-6
Substrate current.....	2-7
Quasi-saturation effects.....	2-7
Series resistance	2-8
Capacitance Calculations.....	2-9
Base-emitter capacitance.....	2-9
Base-collector capacitance	2-9
Substrate capacitance	2-10
Temperature Related Equations.....	2-11

Table of Contents (cont.)

General definitions	2-11
Saturation current, beta, IKF, IKR and IRB equations	2-12
Resistance related temperature equations	2-14
Capacitance related temperature equations	2-14
Other temperature equations	2-17
Noise	2-18
Model Parameters	2-19
Chapter 3	
Mextram Equations.....	3-1
Introduction.....	3-1
Survey of Modeled Effects	3-1
Equivalent Circuits and Equations.....	3-3
Model Constants	3-5
Temperature Effects.....	3-5
Conversions to Kelvin.....	3-5
Thermal voltage	3-5
Resistances	3-6
Depletion capacitance	3-6
Base charge	3-6
Current gain.....	3-7
Currents and voltages	3-8
Transit times.....	3-8
Avalanche parameter.....	3-9
Parameter Dependent Constants	3-9
Static Current Equations	3-9
Ideal forward and reverse current	3-9
The main current I_N	3-9
Forward base currents	3-10
Reverse base currents	3-10
Weak avalanche current	3-11
Series resistances.....	3-13
Variable base resistance	3-13
Variable collector resistance	3-14
Charge Equations.....	3-15

Table of Contents (cont.)

Emitter depletion charge Q_{TE}	3-15
Intrinsic collector depletion charge QTC_1	3-16
Collector transit time in quasi-saturation	3-16
Extrinsic collector depletion charges Q_{TEX} and XQ_{TEX}	3-17
Depletion charge Q_{TS}	3-18
Stored base charges Q_{BE} and Q_{BC}	3-19
Neutral and emitter charge	3-19
Stored epilayer charge.....	3-20
Extrinsic Charges.....	3-20
Extended Modeling.....	3-21
Currents	3-21
Charges.....	3-22
Distributed High Frequency Effects in the Intrinsic Base	3-22
Noise Model.....	3-23
Thermal noise.....	3-24
Collector current shot noise	3-24
Forward base current shot noise and $1/f$ noise	3-24
Emitter-base sidewall current shot noise and $1/f$ noise	3-24
Reverse base current shot noise and $1/f$ noise	3-25
Extrinsic current shot noise and $1/f$ noise	3-25
Model Parameters	3-25
References.....	3-27
Chapter 4	
BJT Level 5 Equations	4-1
Overview.....	4-1
Definitions and Conventions	4-1
Current convention and displays	4-1
Structure conventions.....	4-1
NPN and PNP convention	4-2
Internal variables	4-2
Equivalent Circuit Schematics.....	4-3
For DC and TRANSIENT analysis.....	4-3
For AC and NOISE analysis	4-5
Scaling	4-7

Table of Contents (cont.)

DC Current Calculations.....	4-8
Collector and base currents	4-8
Substrate current.....	4-9
Quasi-saturation effects.....	4-9
Series resistance	4-10
Capacitance Calculations	4-11
Base-emitter capacitance.....	4-11
Base-collector capacitance	4-11
Substrate capacitance	4-12
Temperature Related Equations.....	4-14
General definitions	4-14
Saturation current, beta, IKF, IKR and IRB equations	4-14
Resistance related temperature equations	4-16
Capacitance related temperature equations	4-16
Quasi-saturation temperatures.....	4-19
Other temperature equations	4-20
Noise	4-20
Model Parameters	4-21
 Chapter 5	
VBIC Equations.....	5-1
Introduction.....	5-1
VBIC versions	5-1
VBIC v1.2 updates	5-2
Typical Structures used for VBIC Modeling.....	5-3
VBIC Equivalent Network	5-4
VBIC Model Formulation.....	5-8
Parameter Extraction	5-26
Relationship between SGP and VBIC Parameters	5-28
VBIC DC Modeling.....	5-30
Electrothermal Examples.....	5-32
High Frequency Modeling	5-33
Parameter List for v1.2	5-38
Parameter List for v1.1.5	5-42
Parameter aliases	5-44

Table of Contents (cont.)

References.....	5-45
Chapter 6	
HICUM Equations	6-1
Introduction.....	6-1
Version selection	6-3
Equivalent Circuit.....	6-3
Quasi-Static Transfer Current.....	6-5
Basic formulation	6-5
Extension to the 2D (3D) case and influence of internal base resistance	6-6
Emitter periphery injection	6-7
Heterojunction bipolar transistors (HBTs).....	6-7
High current densities	6-9
Final transfer current model formulation	6-10
Minority Charge, Transit Times, and Diffusion Capacitances	6-12
Base-emitter voltage controlled minority charge	6-13
Low-current densities.....	6-15
Medium and high current densities	6-18
Base-collector voltage controlled minority charge	6-24
Depletion Charges and Capacitances.....	6-24
Base-emitter junction	6-25
Internal base-collector junction.....	6-27
External base-collector junction.....	6-32
Collector-substrate junction	6-34
Static Base Current Components	6-34
Internal Base Resistance	6-36
External (Parasitic) Bias Independent Capacitances	6-39
External Series Resistances	6-41
External base resistance	6-41
External collector resistance	6-42
Emitter resistance	6-44
Non-Quasi-Static Effects	6-45
Vertical direction.....	6-45
Lateral direction	6-47
Breakdown	6-47

Table of Contents (cont.)

Collector-Base Breakdown	6-47
Emitter-base breakdown.....	6-50
Substrate Network	6-53
Parasitic Substrate Transistor	6-54
Small-signal Equivalent Circuit.....	6-56
Noise Model.....	6-62
Temperature Dependence	6-63
Transfer current.....	6-64
Base currents and current gain	6-65
Transit time and minority charge	6-66
Depletion charges and capacitances.....	6-68
Series resistances.....	6-70
Breakdown	6-71
Self-heating.....	6-72
Lateral Scaling	6-73
Transfer current.....	6-73
Base current components	6-74
Minority charge and transit times	6-74
Low current densities	6-74
Critical current (density)	6-75
High current densities	6-77
Depletion charges and capacitances.....	6-80
Series resistances.....	6-81
Breakdown	6-82
Parasitic substrate transistor.....	6-82
Self-heating	6-82
Model Parameter List for HICUM	6-83
References.....	6-88
 Chapter 7	
Mextram 504 Equations.....	7-1
Introduction.....	7-1
Model Parameters	7-2

Table of Contents (cont.)

Chapter 8

Modella Equations.....	8-1
Introduction.....	8-1
Modeled Effects.....	8-1
Equivalent Circuit.....	8-3
Documentation.....	8-4
Model Parameters	8-5
Example of a Modella Model Card	8-8
DC Operating Point Output	8-9
References.....	8-10

Chapter 9

JFET & MESFET Equations	9-1
Introduction.....	9-1
Equivalent Circuit Schematics.....	9-1
Circuit Topology (TOM3).....	9-2
Gate Current I_G	9-3
Internal Variables.....	9-5
Scaling	9-5
Drain resistance.....	9-5
Source resistance	9-5
Gate resistance	9-6
Static Current Equations	9-6
Gate to drain current.....	9-6
Gate to source current	9-7
Leakage currents—Level 9, Update=3 (TOM3)	9-8
Drain-Source Current Equations.....	9-9
IDS current—Level 1	9-9
IDS current—Level 2.....	9-10
IDS current—Level 3	9-10
IDS current—Level 6 (Curtice)	9-10
Transient effect.....	9-11
IDS current—Level 7 (Shichman & Hodge)	9-11
Transient effect.....	9-11

Table of Contents (cont.)

IDS current—Level 8 (Statz)	9-11
IDS current—Level 9, Update=1 (TriQuint)	9-12
IDS current—Level 9, Update=2 (TOM2).....	9-12
IDS current—Level 9, Update=3 (TOM3).....	9-12
Capacitance Equations.....	9-13
Levels 1, 2, 3, 6, 7 calculations	9-13
Levels 8 and 9 calculations	9-14
Capacitance and charge calculations—Level9, Update=3 (TOM3)	9-15
Temperature Effects.....	9-18
If MODLEV=1	9-18
Levels 2, 3, 7, 8, 9 Update=1 only	9-20
Level 9, Update=2 only.....	9-20
Level 9, Update=3 only.....	9-20
Noise	9-21
Thermal noise.....	9-21
Channel noise.....	9-21
JFET Parameters	9-22
Model Parameters for LEVEL= 1, 2 and 3	9-22
MESFET Parameters	9-24
Model Parameters for LEVEL= 6, 7 and 8	9-24
Model Parameters for LEVEL=9, UPDATE=1, 2 and 3	9-26
TOM3 Subcircuit	9-29
GD subckt (GDMOD=1).....	9-29
AC/DC subckt (GDMOD=0)	9-30
Chapter 10	
Common Equations.....	10-1
Overview.....	10-1
Common Model Parameters.....	10-1
Equivalent Circuits for MOS Transistors	10-2
Scaling Rules	10-5
Access Resistance Equations.....	10-6
Related model parameters	10-6
Related device parameters.....	10-7
Related options.....	10-7

Table of Contents (cont.)

Equations	10-8
Area Computation	10-11
Related model parameters	10-12
Related device parameters	10-12
Related options	10-13
OPTION XA	10-14
Equations	10-14
Diode Current Computation (DIOLEV \neq 9)	10-21
Related model parameters	10-21
Related device parameters	10-22
Related options	10-22
Initialization	10-22
Equations	10-23
Diode Current Equations (DIOLEV=9)	10-24
Related model parameters	10-24
Junction Capacitances/Charges (DIOLEV \neq 9)	10-27
Related model parameters	10-27
Related device parameters	10-28
Related options	10-28
Initialization	10-28
Equations	10-30
Equations used with DCAPLEV=4	10-31
Compatibility between ALEV & DCAPLEV	10-32
Capacitance Model (DIOLEV=9)	10-33
Temperature Effects	10-34
Related model parameters	10-34
General definitions	10-35
Access resistance related temperature equations	10-35
Saturation current equations (DIOLEV \neq 9)	10-36
Capacitance related temperature equations (DIOLEV \neq 9)	10-37
Surface potential temperature equations (Levels 1, 2, 3 & 16)	10-39
Threshold voltage temperature equations (Levels 1, 2, 3 & 16)	10-41
Mobility temperature equations (Levels 1, 2, 3 & 16)	10-41
Temperature Update (DIOLEV=9)	10-42
.OPTION ACM	10-43

Table of Contents (cont.)

OPTACM Model Parameter	10-45
Noise Models in MOSFETs.....	10-46
Flicker Noise Models	10-47
Thermal Noise Models	10-47
Chapter 11	
MOS Level 1, 2, 3 Equations	11-1
Berkeley Spice Model General Threshold Voltage Equations	11-1
Calculation of GAMMA, PHI and VTO	11-1
MOSFET Level 1 Equations	11-2
Threshold voltage V_{th}	11-2
Saturation voltage V_{dsat}	11-3
I_{ds} current equations	11-3
MOSFET Level 2 Equations	11-3
Threshold voltage V_{th}	11-3
Level 2 Precise compatibility	11-7
MOSFET Level 3 Equations	11-9
Threshold voltage V_{th}	11-9
Mobility reduction.....	11-11
Channel length modulation	11-11
Saturation voltage V_{dsat}	11-12
I_{ds} current equations	11-12
Linear & saturation region	11-13
Modified Eldo Level=3 (Level=13)	11-13
MOSFET Gate Capacitances Equations	11-14
Definitions.....	11-14
Spice Meyer gate capacitances—CAPLEV=0	11-14
Modified Meyer gate capacitances—CAPLEV=1	11-15
Parameterized modified Meyer capacitances—CAPLEV=2	11-18
Charge Equations.....	11-21
Charge equations for Level 2	11-21
Charge equations for Level 3	11-23
Berkeley Spice Model Parameters	11-24
Model parameters.....	11-24
Model parameters with Precise option	11-25

Table of Contents (cont.)

Chapter 12

MOS Level 4, 5, 6 Equations	12-1
Introduction.....	12-1
Equations Common to Levels 4, 5 and 6.....	12-2
Effective length and width calculations	12-2
Initialization	12-2
Temperature dependence (Common to levels 4, 5 and 6).....	12-2
Level 4	12-3
Threshold voltage.....	12-3
Saturation voltage.....	12-4
Ids current calculation.....	12-4
Subthreshold current	12-5
Level 5	12-5
Threshold voltage.....	12-5
Early voltage	12-5
Saturation voltage.....	12-5
Ids current calculations	12-6
Level 6	12-6
Threshold voltage.....	12-6
Saturation voltage.....	12-7
Ids current calculations	12-7
Subthreshold current	12-8
Model Parameters	12-9

Chapter 13

BSIM1 Equations	13-1
Introduction.....	13-1
Useful Internal Parameters	13-1
Effective channel length and width.....	13-1
Geometrically related parameters	13-2
Voltage dependent parameters ($param_v$)	13-3
Static Current Equations	13-3
Threshold voltage.....	13-3
Drain saturation voltage	13-3

Table of Contents (cont.)

Drain Current in the Linear region.....	13-4
Drain Current in the Saturation region.....	13-4
Subthreshold current	13-5
Charge Equations.....	13-6
Definitions.....	13-6
Charge calculations	13-7
Temperature Effects.....	13-9
Model Parameters	13-9
 Chapter 14	
BSIM2 Equations	14-1
Introduction.....	14-1
Useful Internal Parameters	14-2
Effective channel length and width.....	14-2
Geometrically related parameters	14-2
Voltage dependent parameters ($param_v$)	14-3
Static Current Equations	14-4
Threshold voltage.....	14-4
Drain saturation voltage	14-5
Drain Current in the Linear region.....	14-5
Drain Current in the Saturation region.....	14-5
Drain Current in the Weak inversion region	14-5
Drain Current in the Transition region.....	14-6
Charge Equations.....	14-6
Definitions.....	14-6
Charge calculations	14-7
Temperature Effects.....	14-8
Model Parameters	14-8
 Chapter 15	
EKV MOSFET Equations	15-1
Introduction.....	15-1
Model evolution since v2.3	15-2
Compatibility between v2.3, v2.5 and v2.6	15-4

Table of Contents (cont.)

Static Intrinsic Model Equations	15-6
EKV model equations version 2.6	15-7
EKV model equations Version 2.5.....	15-15
EKV model equations Version 2.3.....	15-16
Quasi-Static Model Equations	15-17
Dynamic model for the intrinsic node charges (v2.5 and v2.6 only)	15-17
Intrinsic capacitances (for versions EKV v2.5 and v2.6 only)	15-18
Intrinsic capacitances for version=2.3.....	15-19
Overlap capacitances (for all versions)	15-21
Total capacitances (for all versions)	15-21
Non-Quasi-Static (NQS) Model Equations	15-21
NQS model equations for versions>2.3	15-21
NQS model equations for version=2.3	15-22
Intrinsic Noise Model Equations	15-23
Thermal noise.....	15-23
Flicker noise	15-24
Temperature Effects.....	15-24
Intrinsic parameters temperature update	15-24
Operating Point Information	15-25
Estimation and Limits of Intrinsic Model Parameters	15-25
Model Parameters	15-27
References.....	15-31
Chapter 16	
MISNAN Equations	16-1
Introduction.....	16-1
Model Inputs	16-2
Flatband Voltage.....	16-3
Normalized Voltage Variables	16-4
Basic Device Quantities.....	16-5
Short- and Narrow-Channel Effects	16-5
Short-channel effect	16-5
Narrow-channel effect.....	16-6
Effective flatband voltage	16-7
Boundary Surface Potential	16-7

Table of Contents (cont.)

Boundary Charge Densities	16-9
Drain Current	16-9
Mobility Model	16-10
Saturation Condition	16-11
Saturation Region Model	16-12
Function M_1	16-13
Function M_2	16-16
Model in Deep Subthreshold	16-16
Stored Charges	16-18
Intrinsic long-channel MOSFET	16-18
Intrinsic MOSFET with short-channel effects	16-20
Deep subthreshold operation	16-21
Representation of MOS capacitor behavior in the vicinity of flatband	16-22
Extrinsic stored charges	16-23
Junction Diodes	16-24
Conductances and Capacitances	16-27
Extrinsic Series Resistances	16-29
Noise Model.....	16-29
Equivalence: Model Parameter Symbols & Names.....	16-29
Model Parameters	16-31
References.....	16-34
 Chapter 17	
BSIM3v2 Equations	17-1
Introduction.....	17-1
Useful Internal Parameters	17-2
Initialization	17-2
Effective channel length and width.....	17-3
Static Current Equations	17-3
Threshold voltage.....	17-3
Poly gate depletion effect.....	17-4
Mobility	17-4
Drain saturation voltage	17-5
DC current calculation	17-6
Linear region	17-7

Table of Contents (cont.)

Saturation region	17-7
Subthreshold region	17-9
Transition region	17-10
Charge Equations.....	17-11
Definitions.....	17-11
Charge calculations	17-11
Temperature Effects.....	17-13
Model Parameters	17-14
Note about parameters.....	17-17
Chapter 18	
BSIM3v3 Equations	18-1
Introduction.....	18-1
BSIM3v3.2.4 enhancements	18-2
BSIM3v3.2.3 enhancements	18-3
BSIM3v3.2 enhancements	18-3
Backward compatibility of BSIM3v3.2 with BSIM3v3.1	18-4
Additional Features.....	18-6
BSIM4 Gate Current inside BSIM3v3	18-6
BSIM4 Gate-Induced Drain Leakage Current inside BSIM3v3	18-6
BSIM3SOI DTOXCV Parameter inside BSIM3v3	18-7
Compatibility option for negative Rds values.....	18-7
Useful Internal Parameters	18-8
Initialization	18-8
Effective channel length and width.....	18-10
Static Current Equations	18-11
Threshold voltage.....	18-11
Poly gate depletion effect.....	18-12
Subthreshold model.....	18-12
Mobility calculation	18-13
Drain saturation voltage	18-14
Effective Vds.....	18-15
Drain current expression	18-15
Substrate current.....	18-17
Charge Equations.....	18-18

Table of Contents (cont.)

Definitions.....	18-18
Intrinsic charge model.....	18-19
Overlap charge calculation.....	18-32
Junction capacitances/charge model (DCAPLEV=4).....	18-34
Initialization	18-34
Equations.....	18-35
Temperature updating	18-35
Diode IV model.....	18-36
Modeling the S/B Diode.....	18-36
Modeling the D/B Diode	18-38
Non-Quasi-Static (NQS) Model Equations	18-39
Temperature Effects.....	18-41
Noise Model.....	18-42
General	18-42
BSIM3v3 Noise Models.....	18-43
Thermal Noise.....	18-43
Flicker Noise Model.....	18-44
Model Parameters	18-47
Notes about Parameters.....	18-54
BSIM3v3 Binning Parameters	18-55
BINUNIT Parameter Selector	18-57
Model Parameters Range Checking.....	18-58
Printing and Plotting BSIM3v3 Output States.....	18-60
 Chapter 19	
BSIM3SOI Equations	19-1
Introduction.....	19-1
I-V Model	19-3
V_{bs0} —Body potential at full depletion and strong inversion conditions	19-3
V_{thfd} —Threshold voltage at fully depleted condition ($V_{bs} = V_{bs0}$).....	19-3
$V_{bs0eff}/V_{bs0teff}$ —Effective V_{bs0}/V_{bs0t} for all V_{gs}	19-4
V_{bsdio}	19-4
V_{bseff} —Equivalent V_{bs} bias for MOS IV calculation	19-5
Threshold Voltage	19-6
Poly depletion effect	19-7

Table of Contents (cont.)

Effective V _{gst} for all region (with Polysilicon Depletion Effect)	19-7
Effective Bulk Charge Factor.....	19-8
Mobility and Saturation Velocity.....	19-9
Drain Saturation Voltage.....	19-9
V _{dseff}	19-10
Drain current expression	19-10
Drain/Source Resistance	19-11
Impact Ionization Current	19-12
Gate-Induced-Drain-Leakage (GIDL)	19-12
Body contact current	19-13
Diode and BJT currents.....	19-13
Total body current	19-15
Temperature effects.....	19-15
C-V Model	19-17
Dimension Dependence	19-17
Charge Conservation.....	19-17
Front Gate Body Charge	19-17
Inversion Charge	19-21
Overlap Capacitance	19-23
Extrinsic Charges	19-25
Helper Charge	19-25
Printing/Plotting States	19-25
.OP Printout	19-27
Parameter List.....	19-28
Chapter 20	
BSIM3SOI v2.x and v3.x Equations	20-1
Introduction.....	20-1
Version Selection	20-1
SOIMOD selection.....	20-2
TNODEOUT keyword	20-2
BSIM3SOI features	20-3
BSIM3SOIv2.x	20-5
BSIMPDv2.x	20-5
BSIMPD I-V Model	20-7

Table of Contents (cont.)

BSIMPD C-V Model.....	20-21
BSIMPD Noise Models.....	20-32
BSIMPDv2.x Parameter List	20-35
BSIMFDv2.x.....	20-43
BSIMFD I-V Model.....	20-44
BSIMFD C-V Model.....	20-56
BSIMFD Noise Models.....	20-63
BSIMFD v2.1 Parameter List	20-66
BSIMDDv2.1	20-72
BSIMDD I-V Model	20-72
BSIMDD C-V Model.....	20-85
BSIMDD Noise Models.....	20-91
BSIMDDv2.1 Parameter List.....	20-94
BSIM3SOIv3.x	20-101
BSIM3SOIv3.1.1.....	20-101
BSIM3SOIv3.1.....	20-102
BSIM3SOIv3.0.....	20-102
BSIMSOIv3.x Model Equations	20-103
BSIMSOIv3.x Parameter List	20-106
Enhanced Binned Parameters for BSIM3SOIv3.1	20-108
Printing/Plotting BSIM3SOI v2.x and v3.x States	20-109
.OP Print out.....	20-112
References.....	20-112
 Chapter 21	
MOS Model 9 Equations.....	21-1
Introduction.....	21-1
Changes between MOS level 903 and MOS level 902	21-2
Version selection	21-2
Preprocessing and Clipping	21-2
Effective channel length and width.....	21-2
Calculation of the threshold voltage parameters	21-3
Calculation of the channel-current parameters	21-4
Calculation of drain-feedback parameters	21-5
Calculation of subthreshold parameters	21-5

Table of Contents (cont.)

Calculation of weak avalanche parameters	21-5
Calculation of charge parameters.....	21-6
Calculation of Noise parameters	21-6
Clipping.....	21-6
Extended Equations	21-10
Useful functions	21-10
Constant definitions	21-10
Extended current equations	21-10
Extended charge equations.....	21-13
Extended noise equations	21-14
Temperature Effects.....	21-17
.OP Printout	21-17
Model Parameters	21-18
Chapter 22	
BSIM4 Equations	22-1
Introduction.....	22-1
BSIM4.1.0 enhancements	22-2
BSIM4.2.0 enhancements	22-3
BSIM4.2.1 enhancements	22-3
BSIM4.3.0 enhancements	22-4
Use of Juncap diode (DIOLEV=9.0) with BSIM4.....	22-5
Version selection	22-6
Documentation	22-6
BSIM4 Parameters.....	22-7
Printing or Plotting a State from the BSIM4 States Structure	22-24
Chapter 23	
TFT Polysilicon Model.....	23-1
Introduction.....	23-1
Model Structure	23-3
Effective Dimensions Calculation	23-3
DC Current Equations.....	23-4
Total Drain Current	23-4

Table of Contents (cont.)

Subthreshold Current	23-4
Above Threshold Current.....	23-5
Kink Effect	23-6
Subthreshold Leakage Current.....	23-6
Threshold Voltage	23-8
Temperature Dependence.....	23-8
Access Resistance Calculation	23-9
Frequency Dispersion.....	23-10
Capacitance Equations	23-11
Model Parameters	23-14
Parasitic Parameters (Access Resistance and Overlap Capacitance Parameters)	23-16
Printing and Plotting Output States.....	23-17
References.....	23-18
 Chapter 24	
MOS Model 11 Equations.....	24-1
Introduction.....	24-1
MOS Model 11 Level 1101 Equations	24-2
MM 11 (1101) Model Parameters.....	24-4
DC operating points	24-13
MOS Model 11 Level 1100 Equations	24-17
MM 11 (1100) Model Parameters.....	24-17
DC operating points	24-23
 Chapter 25	
TFT Amorphous-Si Model	25-1
Introduction.....	25-1
Model Structure	25-2
DC Current Equations.....	25-3
Drain Current	25-3
Temperature Dependence.....	25-5
Capacitance	25-5
Access Resistance Calculation	25-6

Table of Contents (cont.)

Overlap Capacitance Calculation	25-7
Model Parameters	25-8
Parasitic Parameters (Access Resistance and Overlap Capacitance Parameters)	25-9
Printing and Plotting Output States.....	25-10

Chapter 26

HiSIM Model	26-1
Introduction.....	26-1
Version selection	26-2
Documentation	26-3
Model Parameters	26-3
Printing and Plotting Output States.....	26-7

Chapter 27

Surface-Potential-Based Compact MOSFET Model	27-1
Introduction.....	27-1
Part I—Core Model	27-2
General Comments.....	27-2
Structure of the Core Model (Order of Computations)	27-3
Bias-Independent Variables	27-4
Additional Notations	27-5
Lateral Gradient Factor	27-6
Surface Potential ϕ_{ss} (at the Source End of the Channel) and Related Variables ..	27-8
Effective Drain-Source Voltage	27-11
Surface Potential ϕ_{ss} (at the Drain End of the Channel) and Related Variables	27-12
Mid-Point Surface Potential ϕ_m and Related Variables	27-13
Quantum-Mechanical Corrections	27-15
Polysilicon Depletion	27-17
Drain Current Computation.....	27-18
Intrinsic Charges	27-20
Examples (Simulation Results)	27-21

Table of Contents (cont.)

Part II—Extrinsic Model	27-24
General Comments.....	27-24
Bias-Independent Variables	27-24
Additional Notations	27-25
Streamlined Surface Potential Approximation.....	27-25
Extrinsic Charge Model	27-27
Gate Current Model.....	27-29
Substrate Current Model	27-31
Total Terminal Currents	27-32
Noise	27-32
References.....	27-35
Simple Model of the Lateral Gradient Factor.....	27-37
Analytical Approximation for the Surface Potential	27-39
Evaluation of $\phi = \phi_{sd} - \phi_{ss}$ for $x_g < x_{g23}$	27-41
Core Model Local Parameters	27-42
Core Model Global Parameters	27-43
Scaling Equations	27-44
Ranges of SP Parameters	27-47
Temperature dependence (-55 to 150)	27-51
Extrinsic Model Parameters.....	27-53
Printing/Plotting SP States.....	27-55
 Chapter 28	
BTA HVMOS Model	28-1
Introduction.....	28-1
HVMOS License.....	28-1
BTA HVMOS v2.0	28-2
Model Parameters	28-3
 Trademark Information	
 End-User License Agreement	

Table of Contents (cont.)

Chapter 1

Diode Model Equations

1.0 Overview

The DC characteristics of the diode level 1 model are mainly determined by the parameters ***IS*** and ***N***. Non-idealities are included through ***RS*** (series resistance). Reverse breakdown is modeled by an exponential increase in the reverse diode current through parameters ***BV*** and ***IBV***. High injection are introduced through ***IK*** and ***IKR***. Charge storage effects are modeled by a diffusion capacitance through the parameter ***TT*** and depletion capacitance through ***CJO*, *MJ*, *VJ*, *FC***. In the Level 1 model, sidewall effects are added though ***ISW*, *CJSW*, *MJSW***. For the Shottky diode model, ***KMS*** may be used.

Level 2 is an improved model from the static characteristics point. They are mainly determined by the parameters ***IS*** and ***N***. Non-idealities are included through ***RS*** (series resistance). A recombination current is included through ***ISR***, ***NR*** parameters. The reverse behavior is improved through the use of ***IBV*, *IBVL*, *NBV*, *NBVL*** and ***BV*** parameters. The high injection is introduced through ***IKF***. The temperature model is improved through the addition of temperature coefficients on ***IKF*, *BV*** and ***RS***.

Level 3 selects the Fowler-Nordheim model. Such a typical diode is formed as a Metal-Insulator-Semiconductor or Semiconductor-Insulator-Semiconductor layer structure. This model may be used to describe tunneling current that flows through insulators like in EEPROM device, air-gap switch. This model may be geometrically based.

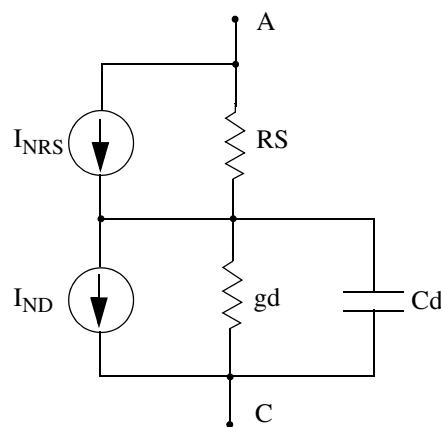
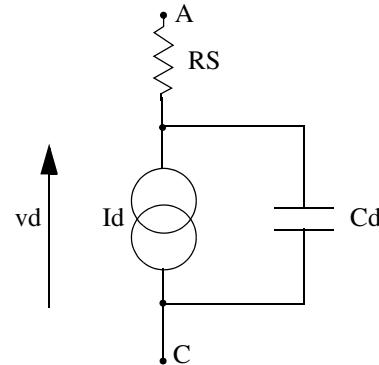
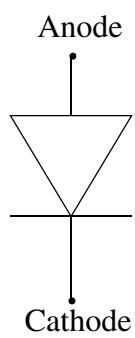
Level 8 selects the JUNMOS model, which is the replica of the bulk-source/drain parasitic diode model included in the common MOS structure. This model may be used to define the bulk diode as an external component or to define new elements such as the substrate diode with similar behaviors.

The Philips Diode Level 500 model (Eldo Level 9) provides a detailed description of the diode currents in forward and reverse biased Si-diodes. It is meant to be used for DC, transient and AC analysis.

Level 21 is a combination of the Level 9 current equations and Level 1 capacitance model with a mix in the temperature dependencies of both models.

2.0 Equivalent Circuit Schematics

The symbol and equivalents circuits for the diode are shown below.



The AC conductance, gd is defined as $gd = \frac{\partial Id}{\partial vd}$

Figure 1-1. Equivalent circuits for diode

3.0 Level 1 Equations

3.1 Level 1 Scaling

The level 1 model is a geometrical model, it is possible to scale different model parameters through the use of the following parameters: ***AREA***, ***PERI***, ***SCALM***, ***SCALE***, ***SHRINK*** and ***M***.

The selector ***SCALEV*** selects the scaling equations used.

- If ***SCALEV*=1**

$$AREA_{eff} = AREA \cdot M$$

$$PERI_{eff} = PERI \cdot M$$

$$ISW_{eff} = PERI \cdot ISW$$

$$IS_{eff} = AREA \cdot IS$$

$$ISAT_{eff} = IS_{eff} + ISW_{eff}$$

$$CJSW_{eff} = CJSW \cdot PERI$$

$$CJO_{eff} = CJO \cdot AREA$$

$$IK_{eff} = IK \cdot AREA$$

$$IKR_{eff} = IKR \cdot AREA$$

$$IBV_{eff} = IBV \cdot AREA$$

$$RS_{eff} = RS / AREA$$

- If ***SCALEV*=2 or 3**

If ***L*** and ***W*** are given as element parameters and model parameters, the element parameters override the model parameters. If they are not given as element parameters and are given as model parameters the model parameters are used.

For ***L*** and ***W*** as element parameters:

$$Leff = L \cdot SCALE \cdot SHRINK + XWeff$$

$$Weff = W \cdot SCALE \cdot SHRINK + XWeff$$

If L and W used are model parameters:

$$Leff = L \cdot SCALM \cdot SHRINK + XWeff$$

$$Weff = W \cdot SCALM \cdot SHRINK + XWeff$$

If L and W are given then $AREA$ and $PERI$ are calculated via L and W :

$$AREA_{eff} = Weff \cdot Leff \cdot M$$

$$PERI_{eff} = (2 \cdot Weff + 2 \cdot Leff) \cdot M$$

Else if W and L are not given and $AREA$ and $PERI$ are specified they are used according to the following priority, if $AREA$ and $PERI$ are given as model parameters and element parameters, the element parameters overrides the model parameters, but if they are not given as element parameters the model parameters are used.

If $AREA$ and $PERI$ are element parameters:

$$AREA_{eff} = AREA \cdot M \cdot SCALE^2 \cdot SHRINK^2$$

$$PERI_{eff} = PERI \cdot SCALE \cdot M \cdot SHRINK$$

If $AREA$ and $PERI$ are model parameters:

$$AREA_{eff} = AREA \cdot M \cdot SCALM^2 \cdot SHRINK^2$$

$$PERI_{eff} = PERI \cdot SCALM \cdot M \cdot SHRINK$$

- If $SCALEV=2$

Parameters are scaled using $AREA(AREA_{eff})$, $PERI(PERI_{eff})$.

$$ISW_{eff} = PERI \cdot ISW$$

$$IS_{eff} = AREA \cdot IS$$

$$ISAT_{eff} = IS_{eff} + ISW_{eff}$$

$$CJSW_{eff} = CJSW \cdot PERI$$

$$CJO_{eff} = CJO \cdot AREA$$

$$RS_{eff} = RS / AREA$$

- If **SCALEV**=3

Parameters are scaled using **AREA**($AREA_{eff}$), **PERI**($PERI_{eff}$), **SCALE** or **SCALM** and **SHRINK** as follows:

$$ISW_{eff} = PERI \cdot (ISW / SCALM)$$

$$IS_{eff} = AREA \cdot (IS / SCALM^2)$$

$$ISAT_{eff} = IS_{eff} + ISW_{eff}$$

$$CJSW_{eff} = (CJSW / SCALM) \cdot PERI$$

$$CJO_{eff} = (CJO / SCALM^2) \cdot AREA$$

$$IK_{eff} = IK \cdot AREA$$

$$IKR_{eff} = IKR \cdot AREA$$

$$IBV_{eff} = IBV \cdot (AREA / SCALM^2)$$

$$RS_{eff} = (RS / SCALM^2) / (AREA)$$

The polysilicon and metal capacitor dimensions are determined by multiplying each by **SCALE** or by **SCALM** if specified as model parameters. These parameters are scaled if specified, regardless to **SCALEV**.

$$LM_{eff} = LM \cdot SCALE \cdot SHRINK$$

$$WM_{eff} = WM \cdot SCALE \cdot SHRINK$$

$$LP_{eff} = LP \cdot SCALE \cdot SHRINK$$

$$WP_{eff} = WP \cdot SCALE \cdot SHRINK$$

$$XP_{eff} = XP \cdot SCALM$$

$$XM_{eff} = XM \cdot SCALM$$

3.2 Level 1 Current Calculations

The total diode current \mathbf{Id} is expressed as: $Id = Kfwd \cdot Ifwd + Krev \cdot Irev$

The forward current $Ifwd$ is determined as: $Ifwd = ISAT_{eff} \cdot \left(\exp \frac{vd}{N \cdot Vt} - 1 \right)$

The forward Knee current coefficient $Kfwd$ is defined to introduce non-ideal effects in the forward current. It acts as a limitation of the positive exponential current increase. Therefore, if IK or vd are negative, $Kfwd = 1$.

$$\text{Otherwise } Kfwd = \left(1 + \sqrt{\frac{Ifwd}{IK}} \right)^{-1}$$

The reverse current $Irev$ is determined as $Irev = -IBV_{eff} \cdot \exp \frac{vd + BV}{N \cdot Vt}$

The Reverse Knee current coefficient $Krev$ is defined to introduce non-ideal effects in the reverse current. It acts as a limitation of the negative exponential current increase. Therefore, if vd is positive or IKR negative, $Krev = 1$.

$$\text{Otherwise } Krev = 1 + \left(\sqrt{\frac{-Irev}{IKR}} \right)^{-1}$$

3.3 Level 1 Capacitance Calculations

In the Diode level 1 model, the total diode capacitance is given as the sum of the diffusion and depletion diode capacitances, the last one is described by a junction bottom (area dependence) and a junction periphery (perimeter dependence) as:

$$Cd = CDEPa + CDEPp + CDIFF + CMETAL + CPOLY$$

Depletion capacitance

DCAP is the selector for the capacitance model.

The following equations are for the case of **DCAP = 1 or 2**; for the case of **DCAP=2**, put **FC = FCS = 0** in the equations.

Bottom and sidewall depletion capacitances are similar in expressions. In the case of the shottky diode style, the parameter **KMS** models the effect of a different behavior of the depletion capacitance.

The P-N junction depletion bottom capacitance **CDEPa** is modeled through **FC**, **CJO**, **VJ**, **MJ** and **KMS**.

$$\text{If } vd < FC \cdot VJ - KMS \text{ then } CDEPa = CJO_{eff} \cdot \left(1 - \frac{vd + KMS}{VJ}\right)^{-MJ}$$

$$\text{else } CDEPa = \frac{CJO_{eff}}{(1 - FC)^{1 + MJ}} \cdot \left(1 - FC \cdot (1 + MJ) + \frac{MJ \cdot (vd + KMS)}{VJ}\right)$$

The P-N junction depletion sidewall capacitance **CDEPp** is modeled using **FC**, **CJSW**, **VJ**, **MJSW** and **KMS**.

$$\text{If } vd < FC \cdot VJ - KMS \text{ then } CDEPp = CJSW_{eff} \cdot \left(1 - \frac{vd + KMS}{VJ}\right)^{-MJSW}$$

else

$$CDEPp = \frac{CJSW_{eff}}{(1 - FC)^{1 + MJSW}} \cdot \left(1 - FC \cdot (1 + MJSW) + \frac{MJSW \cdot (vd + KMS)}{VJ}\right)$$

Diffusion capacitance

The diffusion capacitance **CDIFF** is defined as $CDIFF = TT \cdot \frac{\partial Id}{\partial vd} = TT \cdot gd$

Metal and Polysilicon capacitance

The metal and polysilicon capacitance are determined as follows:

$$C_{metal} = \left(\frac{\epsilon_{ox}}{XOI} \right) \cdot (WP_{eff} + XP_{eff}) \cdot (LP_{eff} + XP_{eff}) \cdot M$$

$$C_{poly} = \left(\frac{\epsilon_{ox}}{XOM} \right) \cdot (WM_{eff} + XM_{eff}) \cdot (LM_{eff} + XM_{eff}) \cdot M$$

3.4 Level 1 Temperature Effects

General definitions

The operating temperature T is defined as $T = Temp + 273.15$.

The reference temperature T_{nom} is defined as $T_{nom} = TNOM + 273.15$

$$Vt(T) = k_B \cdot \frac{T}{q} \quad \delta T = T - T_{nom}$$

The effective Energy Gap of P-N junction is defined as:

If $TLEV=0$ or 1

$$EG_{eff}(T) = 1.16 - 7.02 \cdot 10^{-4} \cdot \frac{T^2}{T + 1108}$$

$$fact = \frac{EG}{Vt(T_{nom})} - \frac{EG}{Vt(T)} + XTI \cdot \ln \frac{T}{T_{nom}}$$

else ($TLEV=2$)

$$EG_{eff}(T) = EG - GAP1 \cdot \frac{T^2}{T + GAP2}$$

$$fact = \frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + XTI \cdot \ln \frac{T}{T_{nom}}$$

Breakdown voltage equations

If $TLEV=0$ $BV(T) = BV - TCV \cdot \delta T$

else ($TLEV=1$ or 2) $BV(T) = BV \cdot (1 - TCV \cdot \delta T)$

Saturation current equations

The temperature dependence of the saturation currents are determined as:

$$IS(T) = IS \cdot \exp\left(\frac{fact}{N}\right) \quad ISW(T) = ISW \cdot \exp\left(\frac{fact}{N}\right)$$

Transit Time temperature equations

$$TT(T) = TT \cdot (1 + TTT1 \cdot \delta T + TTT2 \cdot \delta T^2)$$

Grading coefficient temperature equations

$$MJ(T) = MJ \cdot (1 + TM1 \cdot \delta T + TM2 \cdot \delta T^2)$$

Resistance temperature equations

$$RS(T) = RS \cdot (1 + TRS \cdot \delta T)$$

Capacitance and contact potential related temperature equations

If $TLEVc=0$

$$VJ(T) = VJ \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right)$$

$$PHP(T) = PHP \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right)$$

$$CJO(T) = CJO \cdot \left(1 + MJ \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta T - \frac{VJ(T)}{VJ} \right) \right)$$

$$CJSW(T) = CJSW \cdot \left(1 + MJSW \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta T - \frac{PHP(T)}{PHP} \right) \right)$$

If **TLEV=1**

$$\begin{aligned} VJ(T) &= VJ - TPB \cdot \delta T \\ PHP(T) &= PHP - TPHP \cdot \delta T \\ CJO(T) &= CJO \cdot (1 + CTA \cdot \delta T) \\ CJSW(T) &= CJSW \cdot (1 + CTP \cdot \delta T) \end{aligned}$$

If **TLEV=2**

$$\begin{aligned} VJ(T) &= VJ - TPB \cdot \delta T \\ PHP(T) &= PHP - TPHP \cdot \delta T \\ CJO(T) &= CJO \cdot \left(\frac{VJ}{VJ(T)} \right)^{MJ} \\ CJSW(T) &= CJSW \cdot \left(\frac{PHP}{PHP(T)} \right)^{MJSW} \end{aligned}$$

If **TLEV=3**

$$\begin{aligned} VJ(T) &= VJ + dpbdt \cdot \delta T \\ PHP(T) &= PHP + dphpdt \cdot \delta T \\ CJO(T) &= CJO \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\delta T}{VJ} \right) \\ CJSW(T) &= CJSW \cdot \left(1 - 0.5 \cdot dphpdt \cdot \frac{\delta T}{PHP} \right) \end{aligned}$$

where for **TLEV=0** or **1**,

$$\begin{aligned} dpbdt &= \frac{EGnom + 3 \cdot vtnom + (1.16 - EGnom) \cdot \left(2 - \frac{Tnom}{Tnom + 1108} \right) - VJ}{Tnom} \\ dphpdt &= \frac{EGnom + 3 \cdot vtnom + (1.16 - EGnom) \cdot \left(2 - \frac{Tnom}{Tnom + 1108} \right) - PHP}{Tnom} \end{aligned}$$

and $TLEV=2$

$$dpbdt = \frac{EGnom + 3 \cdot vtnom + (EG - EGnom) \cdot \left(2 - \frac{Tnom}{Tnom + \mathbf{GAP2}}\right) - VJ}{Tnom}$$

$$dphpdt = \frac{EGnom + 3 \cdot vtnom + (EG - EGnom) \cdot \left(2 - \frac{Tnom}{Tnom + \mathbf{GAP2}}\right) - PHP}{Tnom}$$

3.5 Level 1 Model Parameters

Nr.	Name	Description	Default	Units	SCALE effect
1	LEVEL	Model index	1		
Scaling Model Parameters					
2	SCALEV	Scaling equation selector	2		
3	AREA	Junction area	1		
4	PERI	Junction periphery	0		
5	L	Length of diode		m	
6	W	Width of diode		m	
7	SCALM	Model parameter scaling factor	1		
8	SHRINK	Shrink factor	1		
DC Related Model Parameters					
9	IS (ISA,JS)	Saturation current	1.0×10^{-14}	^a Am ⁻²	S ²
10	ISW (JSW,ISP)	Sidewall saturation current	0	^a Am ⁻¹	S
11	N (NF)	Emission coefficient	1		
12	BV (VAR,VB)	Reverse breakdown voltage	∞	V	
13	IBV	Current at breakdown voltage	1.0×10^{-3}	^a Am ⁻²	S ²
14	IK* (IKF,JBF)	Forward knee current	0	^a Am ⁻²	S ²
15	IKR* (JBR)	Reverse knee current	0	^a Am ⁻²	S ²
Capacitance Related Model Parameters					
16	DCAP	Capacitance equation selector	1		
17	CJO (CJ0,CJ,CJA)	Zero-bias junction capacitance	0	^a Fm ⁻²	S ²
18	M (MJ,EXA)	Grading coefficient	0.5		
19	CJSW (CJP)	Bulk sidewall capacitance	0	^a Fm ⁻¹	S
20	MJSW (EXP)	Bulk sidewall grading coefficient	0.33		

Nr.	Name	Description	Default	Units	SCALE effect
21	FC	Coefficient for forward bias depletion capacitance formula	0.5		
22	FCS	Coefficient for forward bias depletion periphery capacitance formula	FC		
23	KMS*	Metal-semiconductor charge storage parameter	0		
24	TT (TF)	Transit time	0	s	
25	VJ (PB,PHI)	Junction potential	1	V	
26	PHP	Periphery junction potential	PB	V	
Metal and Polysilicon Capacitor Parameters					
27	LM	Length of metal capacitor	0	m	
28	LP	Length of polysilicon capacitor	0	m	
29	WM	Width of metal capacitor	0	m	
30	WP	Width of polysilicon capacitor	0	m	
31	XM	Accounts for masking and etching effects	0	m	
32	XOI	Thickness of the poly to bulk oxide	1.0×10^3	Å	
33	XOM	Thickness of the metal to bulk oxide	1.0×10^3	Å	
34	XP	Accounts for masking and etching effects	0	m	
Parasitic Resistance Related Model Parameters					
35	RS (RB)	Ohmic resistance	0	$\text{a}\Omega \text{ m}^2$	s^{-2}
Noise Related Model Parameters					
36	AF	Flicker noise exponent	1		
37	KF	Flicker noise coefficient	0		
Temperature Related Model Parameters					
38	EG	Activation energy	1.11	eV	
39	TNOM (TREF)	Nominal temperature	27	°C	
40	TMOD	Model temperature	TNOM	°C	
41	TLEV	Temperature equation selector	0		
42	TLEVc	Temperature equation selector for junction capacitor and potential	0		
43	CTA	Temperature coefficient for area junction capacitance (TLEVc =1)	0	$^\circ\text{K}^{-1}$	
44	CTP	Temperature coefficient for periphery junction capacitance (TLEVc =1)	0	$^\circ\text{K}^{-1}$	
45	GAP1	First bandgap correction factor	7.02×10^{-4}	$\text{eV}^\circ\text{K}^{-1}$	
46	GAP2	Second bandgap correction factor	1108	°K	

Nr.	Name	Description	Default	Units	SCALE effect
47	TCV	Breakdown voltage temperature coefficient	0	$^{\circ}\text{K}^{-1}$	
48	TM1	Temperature coefficient (Linear) for MJ	0	$^{\circ}\text{K}^{-1}$	
49	TM2	Temperature coefficient (Quadratic) for MJ	0	$^{\circ}\text{K}^{-2}$	
50	TPB (TVJ)	Temperature coefficient for PB	0	$\text{V}^{\circ}\text{K}^{-1}$	
51	TPHP	Temperature coefficient for PHP	0	$\text{V}^{\circ}\text{K}^{-1}$	
52	TRS	Resistance temperature coefficient	0	$^{\circ}\text{K}^{-1}$	
53	TTT1	Temperature coefficient (Linear) for TT	0	$^{\circ}\text{K}^{-1}$	
54	TTT2	Temperature coefficient (Quadratic) for TT	0	$^{\circ}\text{K}^{-2}$	
55	XTI (PT)	Saturation current temperature exponent	3		

a. The units of the marked parameters has changed as they are updated with geometry.

Note, the SCALE option is only in effect if AREA an PERI are element parameters. If AREA and PERI are model parameters then SCALM is in effect.

*. Parameters marked with a * after their name provide compatibility with the PRECISE diode model.

4.0 Level 2 Equations

4.1 Level 2 Scaling

Although Level 2 model is a non-geometrical model, it is possible to scale different model parameters through the usage of **AREA** and **M** element parameters. The relations are the following:

$$IS_{eff} = IS \cdot AREA \cdot M \quad ISR_{eff} = ISR \cdot AREA \cdot M$$

$$IBV_{eff} = IBV \cdot AREA \cdot M \quad IBVL_{eff} = IBVL \cdot AREA \cdot M$$

$$CJO_{eff} = CJO \cdot AREA \cdot M \quad RS_{eff} = \frac{RS}{AREA \cdot M}$$

The **SCALE** option affects the diode parameters in the following way: the effective area is first computed (equation below) then the above diode parameters values are updated with the value $AREA_{eff}$.

$$AREA_{eff} = AREA \cdot SCALE^2$$

The **SHRINK** option has exactly the same effect as the **SCALE** option:

$$AREA_{eff} = AREA \cdot SHRINK^2$$

In general, if both **SCALE** and **SHRINK** options are specified:

$$AREA_{eff} = AREA \cdot SHRINK^2 \cdot SCALE^2$$

$AREA_{eff}$ is then used to update all geometry dependent parameters listed above.

4.2 Level 2 Current Calculations

The total diode current ***Id*** is expressed as: $Id = Kfwd \cdot Ifwd + Irev$

The total forward current ***Ifwd*** is determined as: $Ifwd = Inrm + Kgen \cdot Irec$

The forward current ***Inrm*** is determined as: $Inrm = IS_{eff} \cdot \left(\exp \frac{vd}{N \cdot Vt} - 1 \right)$

The forward recombination current ***Irec*** is determined as:

$$Irec = ISR_{eff} \cdot \left(\exp \frac{vd}{NR \cdot Vt} - 1 \right)$$

The generation factor ***Kgen*** is determined as: $Kgen = \left(\left(1 - \frac{vd}{VJ} \right)^2 + 0.005 \right)^{MJ/2}$

The Forward Knee current Coefficient ***Kfwd*** is defined to introduce non-ideal effects in the forward current. It acts as a limitation of the positive exponential current increase.

So if IK or vd are negative, $Kfwd = 1$, otherwise:

$$Kfwd = \left(1 + \frac{Ifwd}{IK \cdot AREA \cdot M}\right)^{-1/2}$$

The reverse current $Irev$ is determined as the sum of 2 basic reverse currents $Irev = Irevh + Irevl$, which are determined as:

$$Irevl = -IBVL_{eff} \cdot \left(\exp \frac{-(vd + BV)}{NBVL \cdot Vt} - 1 \right)$$

$$Irevh = -IBV_{eff} \cdot \left(\exp \frac{-(vd + BV)}{NBV \cdot Vt} - 1 \right)$$

4.3 Level 2 Capacitance Calculations

In the Diode level 2 model, the total diode capacitance is given as the sum of the diffusion and depletion diode capacitances as: $Cd = CDEP + CDIFF$.

The P-N junction depletion capacitance $CDEP$ is modeled using FC , CJO , VJ , MJ .

If $vd < FC \cdot VJ$ then $CDEP = CJO_{eff} \cdot \left(1 - \frac{vd}{VJ}\right)^{-MJ}$

else $CDEP = \frac{CJO_{eff}}{(1 - FC)^{1 + MJ}} \cdot \left(1 - FC \cdot (1 + MJ) + \frac{MJ \cdot vd}{VJ}\right)$

The diffusion capacitance $CDIFF$ is defined as:

$$CDIFF = TT \cdot \frac{\partial Id}{\partial vd} = TT \cdot gd$$

4.4 Level 2 Temperature Effects

General definitions

The operating temperature T is defined as $T = t$ (Celsius) + 273.15

The reference temperature T_{nom} is defined as $T_{nom} = TNOM + 273.15$

$$Vt(T) = k_B \cdot \frac{T}{q} \quad \delta T = T - T_{nom}$$

The effective Energy Gap of P-N junction is defined as:

$$EG_{eff}(T) = 1.16 - 7.02 \cdot 10^{-4} \cdot \frac{T^2}{T + 1108}$$

$$fact = \frac{EG}{Vt(T_{nom})} - \frac{EG}{Vt(T)} + XTI \cdot \ln \frac{T}{T_{nom}}$$

Saturation current equations

The temperature dependence of the saturation currents are determined as:

$$IS(T) = IS \cdot \exp\left(\frac{fact}{N}\right) \quad ISR(T) = ISR \cdot \exp\left(\frac{fact}{N}\right)$$

Capacitance related temperature equations

$$VJ(T) = VJ \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right)$$

$$CJO(T) = CJO \cdot \left(1 + MJ \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta T - \frac{VJ(T)}{VJ} \right) \right)$$

Other temperature equations

$$IKF(T) = IKF \cdot (1 + TIKF \cdot \delta T)$$

$$BV(T) = BV \cdot (1 + TBV1 \cdot \delta T + TBV2 \cdot \delta T^2)$$

$$RS(T) = RS \cdot (1 + TRS1 \cdot \delta T + TRS2 \cdot \delta T^2)$$

4.5 Level 2 Model Parameters

Nr.	Name	Description	Default	Units	SCALE effect
1	LEVEL	Model index	1		
DC Related Model Parameters					
2	IS	Saturation current	1.0×10^{-14}	^a Am ⁻²	S ²
3	ISR	Recombination current parameter	0	^a Am ⁻²	S ²
4	NR	Emission coefficient for ISR	2		
5	N (NF)	Emission coefficient	1		
6	BV	Reverse breakdown 'knee' voltage		V	
7	IBV	Reverse breakdown 'knee' current	1.0×10^{-3}	^a Am ⁻²	S ²
8	IBVL	Low-level reverse breakdown current	0	^a Am ⁻²	S ²
9	NBV	Reverse breakdown ideality factor	1		
10	NBVL	Low-level reverse breakdown ideality factor	1		
11	IKF	High-injection 'knee' current		A	
Capacitance Related Model Parameters					
12	CJO (CJ0)	Zero-bias junction capacitance	0	^a Fm ⁻²	S ²
13	M	Grading coefficient	0.5		
14	EG	Activation energy	1.11	eV	
15	FC	Coefficient for forward bias depletion capacitance formula	0.5		
16	TT	Transit time	0	s	
17	VJ	Junction potential	1	V	
Parasitic Resistance Related Model Parameters					
18	RS	Ohmic resistance	0	^a Ω m ²	S ⁻²
Noise Related Model Parameters					
19	AF	Flicker noise exponent	1		
20	KF	Flicker noise coefficient	0		
Temperature Related Model Parameters					
21	TRS1	RS temperature coefficient (linear)	0	°C ⁻¹	
22	TRS2	RS temperature coefficient (quadratic)	0	°C ⁻²	
23	TNOM	Nominal temperature	27	°C	
24	TMOD	Model temperature	TNOM	°C	
25	XTI	Saturation current temperature exponent	3		
26	TBV1	BV temperature coefficient (linear)	0	°C ⁻¹	

Nr.	Name	Description	Default	Units	SCALE effect
27	TBV2	BV temperature coefficient (quadratic)	0	$^{\circ}\text{C}^{-2}$	
28	TIKF	IKF temperature coefficient (linear)	0	$^{\circ}\text{C}^{-1}$	

a. The units of the marked parameters has changed as they are updated with geometry.

5.0 Level 3 Equations

5.1 Level 3 Scaling

If \mathbf{Le} and \mathbf{We} element parameters, and \mathbf{Wm} , \mathbf{Lm} and \mathbf{XW} model parameters, are not defined then $AREA_{eff} = AREA \cdot M$, where $AREA$ is expressed in m^2 .

Otherwise, if \mathbf{Le} is undefined, $L_{eff} = Lm \cdot SCALM + XW \cdot SCALM$

else: $L_{eff} = Le \cdot SCALE + XW \cdot SCALM$

If \mathbf{We} is undefined, $W_{eff} = Wm \cdot SCALM + XW \cdot SCALM$

else: $W_{eff} = We \cdot SCALE + XW \cdot SCALM$

Finally, $AREA_{eff} = AREA \cdot M \cdot L_{eff} \cdot W_{eff}$

5.2 Level 3 DC calculation

When vd is positive (forward bias)

$$Id = AREA_{eff} \cdot JF \cdot \left(\frac{vd}{TOX} \right)^2 \cdot \exp \frac{-EF \cdot TOX}{vd}$$

Otherwise (vd negative) $Id = AREA_{eff} \cdot JR \cdot \left(\frac{vd}{TOX} \right)^2 \cdot \exp \frac{ER \cdot TOX}{vd}$

5.3 Level 3 Capacitance calculation

The dynamic behavior is modeled by a constant capacitance Cd as:

$$Cd = AREA_{eff} \cdot \frac{\epsilon_0}{TOX}$$

5.4 Level 3 Model Parameters

Nr.	Name	Description	Default	Units
1	LEVEL	Model index	1	
2	EF	Forward critical electric field	1.0×10^{-8}	V cm ⁻¹
3	ER	Reverse critical electric field	EF	V cm ⁻¹
4	JF	Forward Fowler-Nordheim current coefficient	1.0×10^{-10}	AV ⁻²
5	JR	Reverse Fowler-Nordheim current coefficient	JF	AV ⁻²
6	TOX	Thickness of oxide layer	100	Å
7	L	Length of diode	0	m
8	W	Width of diode	0	m
9	xw	Width and length reduction size	0	m

6.0 Level 8 Equations

6.1 Level 8 Introduction

To simplify the understanding of the equations when comparing the diode schematic to the MOS bulk schematic, the definitions have to be set in the following equations:

$$vbx = vd \quad Ibx = Id \quad Cbx = Cd$$

Related device parameters

- M : Number of parallel transistors

Related options

In the **.OPTION** command the following parameters may be set:

- ***scalm***: sets the size multiplier for the model parameters in Mosfet models.
Default value is 1.

Level 8 Scaling

$$\begin{aligned} JS_{scal} &= \frac{JS}{scalm \cdot scalm} & JSW_{scal} &= \frac{JSW}{scalm} \\ CJ_{scal} &= \frac{CJ}{scalm \cdot scalm} & CJSW_{scal} &= \frac{CJSW}{scalm} \\ CJGATE_{scal} &= \frac{CJGATE}{scalm} \end{aligned}$$

6.2 Level 8 Current Equations (DIOLEV ≠ 9)

If $Val = M \cdot (JS_{scal} \cdot AREA + JSW_{scal} \cdot PERI) > 0$ then $Isatbx = Val$
otherwise $Isatbx = M \cdot IS$

The diode current, ***Ibx***, is expressed as follows:

If $vbx > 0$ (forward mode): $Ibx = Isatbx \cdot \left(\exp \frac{vbx}{N \cdot Vt} - 1 \right)$

otherwise (reverse mode)

- **DIOLEV = 1**: $Ibx = Isatbx \cdot \frac{vbx}{N \cdot Vt}$
- **DIOLEV = 2**:

If $VNDS \leq vbx \leq 0$ then $Ibx = Isatbx \cdot vbx$

else $Ibx = Isatbx \cdot \left(VNDS + \frac{vbx - VNDS}{NDS} \right)$

- **DIOLEV = 3:**

$$\text{If } V_{NDS} \leq vbx \leq 0 \text{ then } Ib_x = Isatbx \cdot \frac{vbx}{N \cdot Vt}$$

$$\text{else } Ib_x = \frac{Isatbx}{N \cdot Vt} \cdot \left(V_{NDS} + \frac{vbx - V_{NDS}}{NDS} \right)$$

- **DIOLEV = 4:**

$$\text{If } vbx > -10 \cdot N \cdot Vt \text{ then } Ib_x = Isatbx$$

$$\text{else } Ib_x = Isatbx \cdot \left(\exp \frac{vbx}{N \cdot Vt} - 1 \right)$$

6.3 Level 8 Current Equations (DIOLEV=9)

This selector is used to implement the JUNCAP junction diode model.

The bottom diffusion current, I_{DB} , is expressed as:

$$I_{DB} = I_{SDB} \cdot \left(\exp \left(\frac{vbx}{NBJ \cdot \phi_{TD}} \right) - 1 \right)$$

The bottom generation current, I_{GB} , is expressed as:

$$I_{GB} = \begin{cases} I_{SGB} \cdot \left(\frac{V_{DB} - vbx}{V_{DB}} \right)^{PB} \cdot \left(\exp \left(\frac{vbx}{NBJ \cdot \phi_{TD}} \right) - 1 \right), & vbx \leq 0.0 \\ I_{SGB} \cdot \left(\frac{V_{AB}}{vbx + V_{AB}} \right)^2 \cdot \left(1 - \exp \left(\frac{-vbx}{NBJ \cdot \phi_{TD}} \right) \right), & vbx > 0.0 \end{cases}$$

$$\text{where } V_{AB} = \frac{2 \cdot V_{DB}}{PB}$$

The locos-edge diffusion current, I_{DS} , is expressed as:

$$I_{DS} = I_{SDS} \cdot \left(\exp\left(\frac{vbx}{NSJ \cdot \phi_{TD}}\right) - 1 \right)$$

The locos-edge generation current, I_{GS} , is expressed as:

$$I_{GS} = \begin{cases} I_{SGS} \cdot \left(\frac{V_{DS} - vbx}{V_{DS}} \right)^{PS} \cdot \left(\exp\left(\frac{vbx}{NSJ \cdot \phi_{TD}}\right) - 1 \right), & vbx \leq 0.0 \\ I_{SGS} \cdot \left(\frac{V_{AS}}{vbx + V_{AS}} \right)^2 \cdot \left(1 - \exp\left(\frac{-vbx}{NSJ \cdot \phi_{TD}}\right) \right), & vbx > 0.0 \end{cases}$$

$$\text{where } V_{AS} = \frac{2 \cdot V_{DS}}{PS}$$

The gate-edge diffusion current, I_{DG} , is expressed as:

$$I_{DG} = I_{SDG} \cdot \left(\exp\left(\frac{vbx}{NGJ \cdot \phi_{TD}}\right) - 1 \right)$$

The gate-edge generation current, I_{GG} , is expressed as:

$$I_{GG} = \begin{cases} I_{SGG} \cdot \left(\frac{V_{DG} - vbx}{V_{DG}} \right)^{PG} \cdot \left(\exp\left(\frac{vbx}{NGJ \cdot \phi_{TD}}\right) - 1 \right), & vbx \leq 0.0 \\ I_{SGG} \cdot \left(\frac{V_{AG}}{vbx + V_{AG}} \right)^2 \cdot \left(1 - \exp\left(\frac{-vbx}{NGJ \cdot \phi_{TD}}\right) \right), & vbx > 0.0 \end{cases}$$

$$\text{where } V_{AB} = \frac{2 \cdot V_{DG}}{PG}$$

The total junction current Ibx can be expressed as:

$$Ibx = AREA \cdot (I_{DB} + I_{GB}) + PERI \cdot (I_{DS} + I_{GS}) + PGATE \cdot (I_{DG} + I_{GG})$$

6.4 Level 8 Capacitance Equations (DIOLEV≠9)

Charge storage is modeled by three constant capacitors, \mathbf{CGSO} , \mathbf{CGDO} and \mathbf{CGBO} . Capacitances taken into account are the non-linear thin-oxide capacitance distributed among the gate, source, drain and bulk regions, and the non-linear depletion-layer capacitances for both substrate junctions divided into bottom and periphery, which vary as the \mathbf{MJ} and \mathbf{MJSW} power of junction voltage respectively, and are determined by the parameters \mathbf{CBD} , \mathbf{CBS} , \mathbf{CJ} , \mathbf{CJSW} , \mathbf{MJ} , \mathbf{MJSW} and \mathbf{PB} . The model is the piecewise linear voltage dependent capacitance model proposed by Meyer.

Initialization

If $\mathbf{CJ} > 0$ then: $Cjax = M \cdot AREA \cdot CJ_{scal}$ else: $Cjax = 0$

If $\mathbf{CJSW} > 0$ then: $Cjpx = M \cdot PERI \cdot CJSW_{scal}$ else: $Cjpx = 0$

If $\mathbf{CJGATE} > 0$ then: $Cjpx = Cjpx + M \cdot PGATE \cdot CJGATE_{scal}$

Equations

The total capacitance \mathbf{Cbx} is expressed as the sum of bottomwall, sidewall depletion capacitances and diffusion capacitance.

$$Cbx = Cbx_{bottom} + Cbx_{sidewall} + Cbx_{diff}$$

The bottomwall capacitance \mathbf{Cbx}_{bottom} is expressed as:

- for $vbx \leq FC \cdot PB$ then $Cbx_{bottom} = Cjax \cdot \left(1 - \frac{vbx}{PB}\right)^{-MJ}$
- else $Cbx_{bottom} = \frac{Cjax}{(1 - FC)^{1+MJ}} \cdot \left(1 - FC \cdot (1 + MJ) + \frac{MJ \cdot vbx}{PB}\right)$

The sidewall depletion capacitance $\mathbf{Cbx}_{sidewall}$ is expressed as:

- for $vbx \leq FC \cdot PBSW$ then $Cbx_{sidewall} = Cjpx \cdot \left(1 - \frac{vbx}{PBSW}\right)^{-MJSW}$

else:

$$Cbx_{sidewall} = \frac{Cjpx}{(1 - FC)^{1 + MJSW}} \cdot \left(1 - FC \cdot (1 + MJSW) + \frac{MJSW \cdot vbx}{PBSW} \right)$$

The diffusion capacitance Cbx_{diff} is expressed as:

- for $TT > 0$ then $Cbx_{diff} = TT \cdot \frac{\partial Ibx}{\partial vbx}$ else: $Cbx_{diff} = 0$

6.5 Level 8 Capacitance Equations (DIOLEV=9)

The total capacitance Cbx can be described by the sum of three elementary capacitances which represent the bottom, locos-edge and gate-edge contributions:

$$Cbx = AREA \cdot C_{JBV} + PERI \cdot C_{JSV} + PGATE \cdot C_{JGV}$$

In order to prevent an unlimited increase of the voltage derivative of the elementary capacitor, it is split into two parts: the original power function and an additional quadratic function. At the cross-over point between these regions, indicated by V_{LB} , the following parameters are defined:

$$F_{CB} = 1 - \left(\frac{1 + PB}{3} \right)^{\frac{1}{PB}} \quad V_{LB} = F_{CB} \cdot V_{DB} \quad C_{LB} = C_{JB}(1 - F_{CB})^{-PB}$$

The capacitance C_{JBV} of the bottom area is calculated as:

$$C_{JBV} = \begin{cases} C_{JB} \cdot \left(1 - \frac{vbx}{V_{DB}} \right)^{-PB}, & vbx < V_{LB} \\ C_{LB} + \frac{C_{LB} \cdot PB \cdot (vbx - V_{LB})}{V_{DB} \cdot (1 - F_{CB})}, & vbx \geq V_{LB} \end{cases}$$

and similar expressions for C_{JSV} and C_{JGV} .

6.6 Level 8 Temperature Effects

General definitions

$$Vt(T) = k_B \cdot \frac{T}{q} \quad \delta t = T - T_{nom}$$

If $TLEV = 0$ or 1 , $EG_{eff}(T) = 1.16 - 7.02 \times 10^{-4} \cdot \frac{T^2}{T + 1108}$

otherwise: $EG_{eff}(T) = EG - GAP1 \cdot \frac{T^2}{T + GAP2}$

Saturation current equations (DIOLEV ≠ 9)

The parameter $TLEVI$ controls the selection of the equations set used for the temperature behavior for the common diode currents.

$$IS(T) = IS \cdot \arg \quad JS(T) = JS \cdot \arg \quad JSW(T) = JSW \cdot \arg$$

For $TLEVI = 0$, no variation in relation to temperature is applied, so $\arg = 1$.

For $TLEVI = 1$, a standard equation, based on SPICE, is defined as:

$$\arg = \exp\left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)}\right) \cdot \left(\frac{T}{T_{nom}}\right)^{XTI}$$

For $TLEVI = 2$, a modified equation is defined as: $\arg = 2^{\delta t / ISTMP}$

For $TLEVI = 3$, an improved equation, based on SPICE, is defined as:

$$\arg = \exp\left(\frac{EG_{eff}(T_{nom})}{N \cdot Vt(T_{nom})} - \frac{EG_{eff}(T)}{N \cdot Vt(T)}\right) \cdot \left(\frac{T}{T_{nom}}\right)^{XTI/N}$$

Capacitance related temperature equations (DIOLEV ≠ 9)

The value of $TLEV_C$ determines which equations are used.

For $TLEV C = 0$,

$$\begin{aligned} PB(T) &= PB \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right) \\ PBSW(T) &= PBSW \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right) \\ CJ(T) &= CJ \cdot \left(1 + MJ \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta t - \frac{PB(T)}{PB} \right) \right) \\ CJSW(T) &= CJSW \cdot \left(1 + MJSW \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta t - \frac{PBSW(T)}{PBSW} \right) \right) \\ CBS(T) &= CBS \cdot \left(1 + MJ \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta t - \frac{PB(T)}{PB} \right) \right) \\ CBD(T) &= CBD \cdot \left(1 + MJ \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta t - \frac{PB(T)}{PB} \right) \right) \end{aligned}$$

For $TLEV C = 1$,

$$\begin{aligned} PB(T) &= PB - PTA \cdot \delta t & PBSW(T) &= PBSW - PTP \cdot \delta t \\ CJ(T) &= CJ \cdot (1 + CTA \cdot \delta t) & CJSW(T) &= CJSW \cdot (1 + CTP \cdot \delta t) \\ CBS(T) &= CBS \cdot (1 + CTA \cdot \delta t) & CBD(T) &= CBD \cdot (1 + CTA \cdot \delta t) \end{aligned}$$

For $TLEV C = 2$,

$$\begin{aligned} PB(T) &= PB - PTA \cdot \delta t & PBSW(T) &= PBSW - PTP \cdot \delta t \\ CJ(T) &= CJ \cdot \left(\frac{PB}{PB(T)} \right)^{MJ} & CJSW(T) &= CJSW \cdot \left(\frac{PBSW}{PBSW(T)} \right)^{MJSW} \\ CBS(T) &= CBS \cdot \left(\frac{PB}{PB(T)} \right)^{MJ} & CBD(T) &= CBD \cdot \left(\frac{PB}{PB(T)} \right)^{MJ} \end{aligned}$$

For $TLEV C = 3$,

$$PB(T) = PB + Dpb \cdot \frac{\delta t}{T_{nom}} \quad PBSW(T) = PBSW + Dpbsw \cdot \frac{\delta t}{T_{nom}}$$

$$CJ(T) = CJ \cdot \left(1 - 0.5 \cdot \frac{Dpb}{PB} \cdot \frac{\delta t}{T_{nom}} \right)$$

$$CJSW(T) = CJSW \cdot \left(1 - 0.5 \cdot \frac{Dpbsw}{PBSW} \cdot \frac{\delta t}{T_{nom}} \right)$$

$$CBS(T) = CBS \cdot \left(1 - 0.5 \cdot \frac{Dpb}{PB} \cdot \frac{\delta t}{T_{nom}} \right)$$

$$CBD(T) = CBD \cdot \left(1 - 0.5 \cdot \frac{Dpb}{PB} \cdot \frac{\delta t}{T_{nom}} \right)$$

where:

$$\begin{aligned} Dpb &= PB - EG_{eff}(T_{nom}) - 3 \cdot Vt(T_{nom}) + \\ &(EG_{eff}(T_{nom}) - EG) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + GAP2} \right) \end{aligned}$$

$$\begin{aligned} Dpbsw &= PBSW - EG_{eff}(T_{nom}) - 3 \cdot Vt(T_{nom}) + \\ &(EG_{eff}(T_{nom}) - EG) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + GAP2} \right) \end{aligned}$$

Temperature Update (DIOLEV=9)

In the case that **DIOLEV=9**, the following updates are performed.

The general rules, which apply to all three components of the JUNCAP model are:

$$EG_{eff}(T) = 1.16 - 7.02 \times 10^{-4} \cdot \frac{T^2}{T + 1108}$$

$$F_{TD} = \left(\frac{T}{T_{nom}} \right)^{1.5} \cdot \exp \left(\frac{EG_{eff}(T_{nom})}{2 \cdot Vt(T_{nom})} - \frac{EG_{eff}(T)}{2 \cdot Vt(T)} \right)$$

The internal reference parameters for the bottom component are specified by:

$$V_{DB} = VDBR \cdot \frac{T}{T_{nom}} - 2 \cdot Vt(T) \cdot \ln F_{TD}$$

$$C_{JB} = CJBR \cdot \left(\frac{VDBR - VR}{V_{DB}} \right)^{PB}$$

$$I_{SGB} = JSGBR \cdot F_{TD} \cdot \left(\frac{V_{DB}}{VDBR - VR} \right)^{PB}$$

$$I_{SDB} = JSDBR \cdot F_{TD}^2$$

Similar formulations hold for the locos-edge component:

$$V_{DS} = VDSR \cdot \frac{T}{T_{nom}} - 2 \cdot Vt(T) \cdot \ln F_{TD}$$

$$C_{JS} = CJSR \cdot \left(\frac{VDSR - VR}{V_{DS}} \right)^{PS}$$

$$I_{SGS} = JSGR \cdot F_{TD} \cdot \left(\frac{V_{DS}}{VDSR - VR} \right)^{PS}$$

$$I_{SDS} = JSDSR \cdot F_{TD}^2$$

Similar formulations hold for the gate-edge component:

$$V_{DG} = VDGR \cdot \frac{T}{T_{nom}} - 2 \cdot Vt(T) \cdot \ln F_{TD}$$

$$C_{JG} = CJGR \cdot \left(\frac{VDGR - VR}{V_{DG}} \right)^{PG}$$

$$I_{SGG} = JSGR \cdot F_{TD} \cdot \left(\frac{V_{DG}}{VDGR - VR} \right)^{PG}$$

$$I_{SDG} = JSGR \cdot F_{TD}^2$$

6.7 Level 8 Parameters

Nr.	Name	Description	Default	Units
Bulk Diode Current Related Parameters				
1	DIOLEV	Switch selector	1	
2	JS	Bottom bulk junction saturation current density	0	Am^{-2}
3	JSW	Sidewall bulk junction saturation current density	0	Am^{-1}
4	IS	Bulk junction saturation current	1×10^{-14}	A
5	N	Emission coefficient	1	
6	NDS	Reverse bias slope coefficient	1	
7	VNDS	Reverse bias transition voltage	-1	V
8	SBTH	Flag for reverse diode behavior (for PRECISE compatibility) 0 sets DIOLEV =1 and 1 sets DIOLEV =4	0	
Bulk Diode Capacitance Related Parameters				
9	CBD	Zero bias Bulk-Drain capacitance	0	F
10	CBS	Zero bias Bulk-Source capacitance	0	F
11	CJ	Zero bias bottom Bulk junction capacitance	0	Fm^{-2}
12	CJGATE	Zero bias gate-edge sidewall Bulk junction capacitance	0	Fm^{-1}
13	CJSW	Zero bias sidewall Bulk junction capacitance	0	Fm^{-1}
14	FC	Bulk junction forward bias capacitance coefficient	0.5	
15	MJ	Bulk junction bottom grading coefficient	0.5	
16	MJSW	Bulk junction sidewall grading coefficient	0.33	
17	PB	Bulk bottom junction potential	0.8	V
18	PBSW	Bulk sidewall junction potential	PB	V
19	TT	Transit time	0	s
JUNCAP Related Parameters (DIOLEV=9)				
20	VR	Voltage at which the parameters have been determined	0	V
21	JSGBR	Bottom saturation-current density due to electron-hole generation at $V = V_R$	1×10^{-3}	Am^{-2}
22	JSDBR	Bottom saturation-current density due to diffusion from back contact	1×10^{-3}	Am^{-2}
23	JSGSR	Sidewall saturation-current density due to electron-hole generation at $V = V_R$	1×10^{-3}	Am^{-1}
24	JSDSR	Sidewall saturation-current density due to diffusion from back contact	1×10^{-3}	Am^{-1}
25	JSGGR	Gate edge saturation-current density due to electron-hole generation at $V = V_R$	1×10^{-3}	Am^{-1}

Nr.	Name	Description	Default	Units
26	JSDGR	Gate edge saturation-current density due to diffusion from back contact	1×10^{-3}	Am^{-1}
27	NBJ	Emission coefficient of the bottom forward current	1	
28	NSJ	Emission coefficient of the sidewall forward current	1	
29	NGJ	Emission coefficient of the gate edge forward current	1	
30	CJBR	Bottom junction capacitance at $V = V_R$	1×10^{-12}	Fm^{-2}
31	CJSR	Sidewall junction capacitance at $V = V_R$	1×10^{-12}	Fm^{-1}
32	CJGR	Gate edge junction capacitance at $V = V_R$	1×10^{-12}	Fm^{-1}
33	VDBR	Diffusion voltage of the bottom junction at $T = T_R$	1	V
34	VDSR	Diffusion voltage of the sidewall junction at $T = T_R$	1	V
35	VDGR	Diffusion voltage of the gate edge junction at $T = T_R$	1	V
36	PB	Bottom-junction grading coefficient	0.4	
37	PS	Sidewall-junction grading coefficient	0.4	
38	PG	Gate edge-junction grading coefficient	0.4	

Temperature Effect Related Model Parameters

39	TNOM	Nominal temperature	27	$^{\circ}\text{C}$
40	TMOD	Model temperature	TNOM	$^{\circ}\text{C}$
41	TLEV	Temperature equation level selector	0	
42	TLEV_C	Temperature equation level selector for capacitances and potentials	0	
43	CTA	Junction capacitance CJ temperature coefficient	0	$^{\circ}\text{K}^{-1}$
44	CTP	Junction sidewall capacitance CJSW temperature coefficient	0	$^{\circ}\text{K}^{-1}$
45	PTA	Junction potential PB temperature coefficient	0	$\text{V}^{\circ}\text{K}^{-1}$
46	PTP	Junction potential PHB temperature coefficient	0	$\text{V}^{\circ}\text{K}^{-1}$
47	EG	Energy gap for P-N junction diode	1.11 ^a	eV
48	GAP1	First bandgap correction factor	7.02×10^{-4}	$\text{eV}^{\circ}\text{K}^{-1}$
49	GAP2	Second bandgap correction factor	1108	$^{\circ}\text{K}$
50	TLEV_I (LIS)	Saturation current temperature selector	1	
51	ISTMP	Number of degrees that doubles IS value	10	$^{\circ}\text{C}$
52	XTI	Saturation current temperature exponent	0	

a. if **TLEV=0** or **1**, **EG=1.11**
else **EG=1.16**

7.0 Noise Equations for All Levels

For all of the previous diode models, the same equation set for noise is applied. Refer to the noise model for a diode in [Figure 1-1 on page 1-2](#).

The noise contribution in the series resistance, RS , is a thermal one:

$$I_{NRS}^2 = \frac{4kT}{RS_{eff}}$$

The noise in the diode junction consists of shot and flicker noise as defined by:

$$I_{ND}^2 = 2 q Id + \frac{KF \cdot (Id)^{AF}}{f}$$

8.0 Level 9 (Philips Diode Level 500)

8.1 Level 9 (Philips Diode Level 500) Modeled Effects

The Philips Diode model Level 500 includes:

- Forward biasing
 - ideal current
 - non-ideal current including tunneling
- Reverse Biasing
 - Trap assisted tunneling
 - Shockley-Read-Hall generation
 - Band-to-band tunneling
 - Avalanche multiplication

- Breakdown
- Series resistances
- Charge storage effects
- Temperature scaling rules
- Noise model for RS and the ideal forward current

The model does not include:

- Noise from the non-ideal forward and reverse diode currents

8.2 Level 9 (Philips Diode Level 500) Equivalent Circuits

A full description of Philips Diode Level 500 is given below. The DC/transient and AC circuits are shown equivalently in [Figure 1-2](#) and [Figure 1-3](#) respectively.

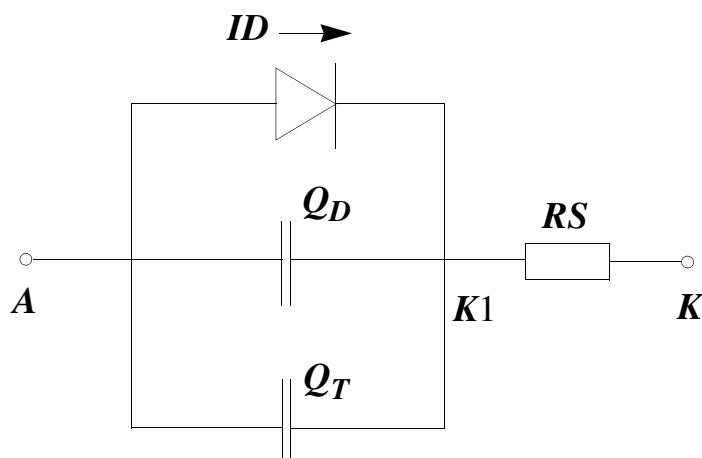


Figure 1-2. DC/Transient equivalent circuit for diode

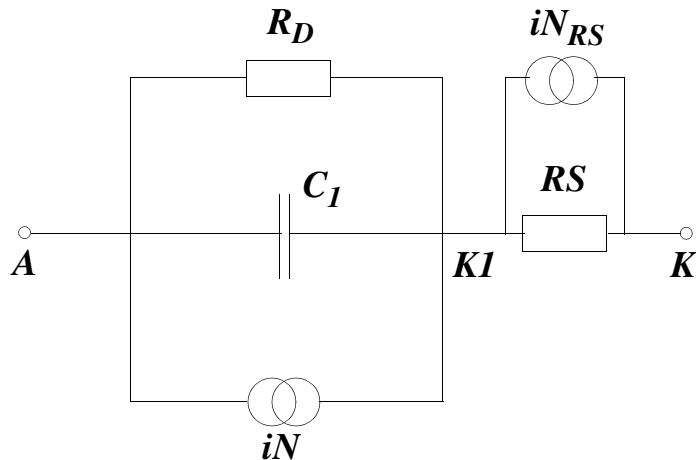


Figure 1-3. AC equivalent circuit for diode, including noise sources

8.3 Level 9 (Philips Diode Level 500) Equations

The actual simulation temperature is denoted by **TEMP** (in °C).

The temperature at which the parameters are determined is **TREF** (in °C.)

Conversions to Kelvins

$$T_K = TEMP + 273.15 + DTA$$

$$T_{RK} = TREF + 273.15$$

Thermal Voltages

$$k = 1.3806226 \cdot 10^{-23} JK^{-1}$$

$$q = 1.6021918 \cdot 10^{-19} C$$

$$V_T = \left(\frac{k}{q}\right) \cdot T_K$$

$$V_{TR} = \left(\frac{k}{q}\right) \cdot T_{RK}$$

Depletion Capacitances

$$F = \left(\frac{T_K}{T_{RK}} \right)^3 \cdot \exp \left[VG \cdot \left(\frac{1}{V_{TR}} - \frac{1}{V_T} \right) \right]$$

$$VD_T = \left[\left(\frac{VD}{V_{TR}} \right) - \ln(F) \right] \cdot V_T$$

$$CJ_T = CJ \cdot \left(\frac{VD}{VD_T} \right)^P$$

Transit Times

$$TAU_T = TAU \left(\frac{T_K}{T_{RK}} \right)^{1.8}$$

Saturation Current

$$IS_T = IS \cdot \left(\frac{T_K}{T_{RK}} \right)^{1.8} \cdot \exp \left[\frac{VG}{N} \cdot \left(\frac{1}{V_{TR}} - \frac{1}{V_T} \right) \right]$$

Shockley-Read-Hall Generation and Trap Assisted Tunneling

$$T_{up} = \left(\frac{T_K}{T_{RK}} \right)^{3/2} \cdot \exp \left[\frac{VG + VLC}{2} \cdot \left(\frac{1}{V_{TR}} - \frac{1}{V_T} \right) \right]$$

$$CSRH_T = CSRH \cdot T_{up}$$

$$CTAT_T = CTAT \cdot T_{up}$$

$$ETAT_T = 70.8 \cdot T_K^{3/2}$$

Band to Band Tunneling

$$CBBT_T = CBBT \text{ (temperature independent)}$$

$$F0 = 1.9 \times 10^7 \cdot \left(1.04 - \frac{4.21 \cdot 10^{-4} \cdot T_K^2}{636 + T_K} \right)$$

Avalanche Multiplication¹

$$dT = TEMP + DTA - 25^\circ C$$

$$Bn = 1.23 \cdot 10^6$$

$$Bn_T = Bn \cdot (1 + 7.2 \cdot 10^{-4} \cdot dT - 1.6 \cdot 10^{-6} \cdot dT^2)$$

Breakdown

$$VBR_T = VBR \cdot \left(\frac{T_K}{T_{RK}} \right)^{0.1}$$

$$EMVBR_T = EMVBR \cdot \left(\frac{VD_T + VBR_T}{VD + VBR} \right)^{(1-P)}$$

Resistance

$$RS_T = RS \cdot \left(\frac{T_K}{T_{RK}} \right)^{PTRS}$$

Model Constants and Parameter Related Constants

$$K = 0.01$$

$$KET = 0.1$$

$$ETM = 3$$

Maximum Electric Field and Depletion Layer Width at Zero Bias

1. 25°C is the reference temperature at which Bn has been determined

$$E_0 = \frac{EMVBR_T}{\left(1 + \frac{VBR_T}{VD_T}\right)^{1-P}}$$

$$W_0 = \frac{VD_T}{E_0 \cdot (1-P)}$$

Diode Currents

First the maximum reverse junction voltage is defined. Above this voltage the current will be extrapolated on a logarithmic scale.

$$V_j = \begin{cases} -0.99 \cdot VBR_T, & V_{AK1} < -0.99 VBR_T \\ V_{AK1}, & V_{AK1} \geq -0.99 VBR_T \end{cases}$$

Ideal Forward Current

$$Id_f = IS_T \left\{ \exp\left(\frac{V_j}{N \cdot V_T}\right) - 1 \right\}$$

Maximum Electric Field Depletion Layer Width

$$VD_j = \frac{\sqrt{\left\{ \left(1 - \frac{V_j}{VD_T}\right)^2 + \left(\frac{V_j}{VD_T}\right) \cdot K \right\}} + \left(1 - \frac{V_j}{VD_T}\right)}{2}$$

$$E_m = E_0 \cdot VD_j^{(1-P)}$$

$$W_d = W_0 \cdot VD_j^P$$

Shockley-Read-Hall Generation

$$I_{srh} = CSRH_T \cdot (W_d - W_0)$$

Trap Assisted Tunneling

$$ET_0 = \frac{\frac{E_0}{ETAT_T} + ETM - \sqrt{\left(\frac{E_0}{ETAT_T} - ETM\right)^2 + KET}}{2}$$

$$ET = \frac{\frac{E_m}{ETAT_T} + ETM - \sqrt{\left(\frac{E_m}{ETAT_T} - ETM\right)^2 + KET}}{2}$$

$$I_{tat} = CTAT \cdot W_d \cdot \left\{ \frac{\exp(ET^2) - \exp(ET_0^2)}{\frac{E_m}{ETAT_T}} \right\}$$

Non-ideal Forward Current including Tunneling

$$I_{S_{lf}} = CSRH_T \cdot \left\{ 6.28 + 38.58 \cdot \left(\frac{E_m}{ETAT_T} \right) \cdot \exp(ET^2) \right\} \cdot \frac{VT}{E_m}$$

$$I_{lf} = I_{S_{lf}} \cdot \frac{\exp\left(\frac{V_j}{N \cdot V_T}\right) - 1}{4 \cdot \exp\left(\frac{V_j}{2 \cdot N \cdot V_T}\right) + \exp\left(\frac{VLC}{2 \cdot N \cdot V_T}\right)} \cdot \exp\left(\frac{VLC}{2 \cdot N \cdot V_T}\right)$$

Band to Band Tunneling

$$I_{bbt} = \frac{-CBBT_T \cdot V_j}{\left(\frac{F0}{E_m}\right)^{1.5} \cdot \exp\left(\frac{F0}{E_m}\right)}$$

Avalanche Multiplication

$$\mu = 0.3295 \cdot \left(\frac{E_m}{EMVBR_T} \right)^2 \cdot \exp \left(\frac{Bn_T}{EMVBR_T} - \frac{Bn_T}{E_m} \right)$$

Total Diode Current

$$Id = \frac{(Id_f + I_{lf} - I_{srh}) \cdot \frac{1 + \exp(-2 \cdot \mu)}{2} - (I_{bbt} + I_{tat}) \cdot \exp(-\mu)}{1 - 2 \cdot \mu \cdot \{1 + \exp(-2 \cdot \mu)\}}$$

Extrapolation of the Reverse Current

$$I_{dBR} = Id \quad \text{at } V_j = -0.99VBR_T$$

$$G_{dBR} = \frac{dI_d}{dV_j} \quad \text{at } V_j = -0.99VBR_T$$

$$ID = \begin{cases} I_d & V_{AK1} \geq -0.99VBR_T \\ I_{dBR} \cdot \exp \left[\left(\frac{V_{AK1} + 0.99VBR_T}{I_{dBR}} \right) G_{dBR} \right] & V_{AK1} < -0.99VBR_T \end{cases}$$

Transient Model

Transient behavior is modeled using the DC equations.

Diffusion Charge

$$Q_D = TAU_T \cdot Id_f$$

Depletion Charge

$$FC = 1 - \left(\frac{1+P}{3} \right)^{\left(\frac{1}{P} \right)}$$

$$Q_{AT} = CJ_T \cdot \left(\frac{VD_T}{1-P} \right)$$

$$V_L = FC \cdot VD_T$$

$$C_L = CJ_T \cdot (1 - FC)^{-P}$$

$$Q_L = Q_{AT} \cdot \{1 - (1 - FC)^{(1-P)}\}$$

Then if $V_{AK1} < V_L$

$$Q_T = Q_{AT} \cdot \left[1 - \left\{ 1 - \left(\frac{V_{AK1}}{VD_T} \right) \right\}^{(1-P)} \right]$$

Or if $V_{AK1} \geq V_L$

$$Q_T = Q_L + C_L \cdot (V_{AK1} - V_L) \cdot \left\{ 1 + \frac{P \cdot (V_{AK1} - V_L)}{2 \cdot VD_T (1 - FC)} \right\}$$

AC Linearized Model

Using the appropriate definitions for the various circuit elements leads to the following equations:

$$R_D = \frac{1}{dID/dV_{AK1}}$$

Where dID/dV_{AK1} is the first derivative of the total diode current with respect to the internal voltage V_{AK1} .

The capacitances are defined as:

$$C_T = CJ_T \left\{ 1 - \left(\frac{V_{AK1}}{VD_T} \right) \right\}^{-P} \quad \text{for } V_{AK1} < V_L$$

$$C_T = C_L \cdot \left\{ 1 + \frac{P \cdot (V_{AK1} - V_L)}{VD_T \cdot (1 - FC)} \right\} \quad \text{for } V_{AK1} \geq V_L$$

$$C_1 = C_T + TA U_T \cdot \left(\frac{Id_f + IS_T}{N \cdot V_T} \right)$$

Noise Model

For noise analysis, noise sources are added to the small signal model as shown in [Figure 1-3](#). In these equations f represents the operation frequency of the transistor and Δf is the bandwidth. When Δf is taken as 1Hz, a noise density is obtained.

- Thermal Noise

$$\overline{iN_{RS}^2} = \frac{4 \cdot k \cdot T_K \cdot \Delta f}{RS_T}$$

- Current Noise (shot noise and $1/f$ noise)

The current noise is only modeled for the ideal forward current Id_f .

$$\overline{iN^2} = 2 \cdot q \cdot |Id_f| \cdot \Delta f + KF \cdot MULT \cdot \left| \frac{Id_f}{MULT} \right|^{AF} \cdot \frac{\Delta f}{f}$$

8.4 Level 9 (Philips Diode Level 500) Parameters

Nr.	Name	Description	Default	Units	Clip Low	Clip High
1	LEVEL	Model Level	9			
2	IS	Saturation Current	7.13×10^{-13}	A	0.0	
3	N	Junction emission co-efficient	1.044 ^a		0.1	
4	VLC	Voltage dependence at low forward currents	0.0	V		
5	VBR	Breakdown voltage	7.459	V	0.1	
6	EMVBR	Electric field at breakdown	1.36×10^8	V/m	1.0	
7	CSRH	Shockley-Read-Hall generation	7.44×10^{-5}	A/m	0.0	

Nr.	Name	Description	Default	Units	Clip Low	Clip High
8	CBBT	Band to band tunneling	3.255	A/V	0.0	
9	CTAT	Trap assisted tunneling	3.31×10^{-4}	A/m	0.0	
10	RS	Series resistance	0.0	Ω	0.0	
11	TAU	Transit time	500.0×10^{-12}	s	0.0	
12	CJ	Zero-bias depletion capacitance	7.0×10^{-12}	F	0.0	
13	VD	Diffusion voltage	0.90	V	0.05	
14	P	Grading co-efficient	0.40		0.05	0.99
15	TREF	Reference temperature	27.0	$^{\circ}\text{C}$	-273.15	
16	VG	Bandgap voltage	1.206	V	0.1	
17	PTRS	Power for temperature dependence of RS	0.0			
18	KF	Flickernoise co-efficient	0.0		0.0	
19	AF	Flickernoise exponent	1.0		0.01	
20	DTA	Difference between device temperature and ambient temperature	0.0	K		
21	MULT ^b	Multiplication factor	1.0		0.0	

a. Parameter N should be close to unity and is not intended to simulate a current other than the usual injection of holes/electrons.

b. This parameter may be used to put several parameters in parallel. The following parameters are multiplied by **MULT:** **IS CSRH CBBT CTAT CJ**

The following parameter is divided by **MULT:** **RS**

9.0 Level 21

Level 21 is a combination of the Level 9 current equations and Level 1 capacitance model with a mix in the temperature dependencies of both models.

9.1 Level 21 Scaling

The Level 21 model is a geometrical model, it is possible to scale different model parameters through the use of the following parameters: **AREA**, **PERI**, **SCALM**, **SCALE**, **SHRINK** and **M**.

The selector **SCALEV** selects the scaling equations used.

- If $SCALEV=1$

$$AREA_{eff} = AREA \cdot M$$

$$PERI_{eff} = PERI \cdot M$$

$$ISW_{eff} = PERI \cdot JSW$$

$$IS_{eff} = AREA \cdot JS$$

$$ISAT_{eff} = IS_{eff} + ISW_{eff}$$

$$CJSW_{eff} = CJSW \cdot PERI$$

$$CJO_{eff} = CJO \cdot AREA$$

$$RS_{eff} = RS / AREA$$

- If $SCALEV=2$ or 3

If L and W are given as element parameters and model parameters, the element parameters override the model parameters. If they are not given as element parameters and are given as model parameters the model parameters are used.

For L and W as element parameters:

$$Leff = L \cdot SCALE \cdot SHRINK + XWeff$$

$$Weff = W \cdot SCALE \cdot SHRINK + XWeff$$

If L and W used are model parameters:

$$Leff = L \cdot SCALM \cdot SHRINK + XWeff$$

$$Weff = W \cdot SCALM \cdot SHRINK + XWeff$$

If L and W are given then $AREA$ and $PERI$ are calculated via L and W :

$$AREA_{eff} = Weff \cdot Leff \cdot M$$

$$PERI_{eff} = (2 \cdot Weff + 2 \cdot Leff) \cdot M$$

Else if W and L are not given and $AREA$ and $PERI$ are specified they are used according to the following priority, if $AREA$ and $PERI$ are given as model parameters and element parameters, the element parameters overrides the model parameters, but if they are not given as element parameters the model parameters are used.

If $AREA$ and $PERI$ are element parameters:

$$\begin{aligned} AREA_{eff} &= AREA \cdot M \cdot SCALE^2 \cdot SHRINK^2 \\ PERI_{eff} &= PERI \cdot SCALE \cdot M \cdot SHRINK \end{aligned}$$

If $AREA$ and $PERI$ are model parameters:

$$\begin{aligned} AREA_{eff} &= AREA \cdot M \cdot SCALM^2 \cdot SHRINK^2 \\ PERI_{eff} &= PERI \cdot SCALM \cdot M \cdot SHRINK \end{aligned}$$

- If $SCALEV=2$

Parameters are scaled using $AREA(AREA_{eff})$, $PERI(PERI_{eff})$.

$$ISW_{eff} = PERI \cdot JSW$$

$$IS_{eff} = AREA \cdot JS$$

$$ISAT_{eff} = IS_{eff} + ISW_{eff}$$

$$CJSW_{eff} = CJSW \cdot PERI$$

$$CJO_{eff} = CJO \cdot AREA$$

$$RS_{eff} = RS / AREA$$

- If $SCALEV=3$

Parameters are scaled using $AREA(AREA_{eff})$, $PERI(PERI_{eff})$, $SCALE$ or $SCALM$ and $SHRINK$ as follows:

$$ISW_{eff} = PERI \cdot (JSW/SCALM)$$

$$IS_{eff} = AREA \cdot ((JS)/SCALM^2)$$

$$ISAT_{eff} = IS_{eff} + ISW_{eff}$$

$$CJSW_{eff} = (CJSW/SCALM) \cdot PERI$$

$$CJO_{eff} = (CJO/SCALM^2) \cdot AREA$$

$$RS_{eff} = (RS/SCALM^2)/(AREA)$$

The polysilicon and metal capacitor dimensions are determined by multiplying each by **SCALE** or by **SCALM** if specified as model parameters. These parameters are scaled if specified, regardless to **SCALEV**.

$$LM_{eff} = LM \cdot SCALE \cdot SHRINK$$

$$WM_{eff} = WM \cdot SCALE \cdot SHRINK$$

$$LP_{eff} = LP \cdot SCALE \cdot SHRINK$$

$$WP_{eff} = WP \cdot SCALE \cdot SHRINK$$

$$XP_{eff} = XP \cdot SCALM$$

$$XM_{eff} = XM \cdot SCALM$$

Scaling of CSRH, CTAT and CBBT parameters

$$\begin{aligned} CSHR_{eff} &= CSHR \cdot (CSRH_0 + CSRH_1 \cdot AREA_{eff} + CSRH_2 \cdot AREA_{eff}^2 \\ &+ CSRH_3 \cdot AREA_{eff}^3 + CSRH_4 \cdot PERI_{eff} + CSRH_5 \cdot PERI_{eff}^2 + CSRH_6 \cdot PERI_{eff}^3) \end{aligned}$$

$$\begin{aligned} CTAT_{eff} &= CTAT \cdot (CTAT_0 + CTAT_1 \cdot AREA_{eff} + CTAT_2 \cdot AREA_{eff}^2 \\ &+ CTAT_3 \cdot AREA_{eff}^3 + CTAT_4 \cdot PERI_{eff} + CTAT_5 \cdot PERI_{eff}^2 + CTAT_6 \cdot PERI_{eff}^3) \end{aligned}$$

$$\begin{aligned} CBBT_{eff} = & CBBT \cdot (CBBT_0 + CBBT_1 \cdot AREA_{eff} + CBBT_2 \cdot AREA_{eff}^2 \\ & + CBBT_3 \cdot AREA_{eff}^3 + CBBT_4 \cdot PERI_{eff} + CBBT_5 \cdot PERI_{eff}^2 + CBBT_6 \cdot PERI_{eff}^3) \end{aligned}$$

9.2 Level 21 Temperature Effects

The actual simulation temperature is denoted by **TEMP** (in C). The temperature at which the parameters are determined is **TREF** (in C).

Conversions to Kelvins

$$T_K = TEMP + 273.15 + DTA$$

$$T_{RK} = TREF + 273.15$$

Thermal Voltages

$$k = 1.3806226 \cdot 10^{-23} JK^{-1}$$

$$q = 1.6021918 \cdot 10^{-19} C$$

$$V_T = \left(\frac{k}{q}\right) \cdot T_K$$

$$V_{TR} = \left(\frac{k}{q}\right) \cdot T_{RK}$$

Transit Times

$$TAU_T = TAU \left(\frac{T_K}{T_{RK}}\right)^{1.8}$$

Saturation Current

$$IS_T = IS \cdot \left(\frac{T_K}{T_{RK}}\right)^{1.8} \cdot \exp\left[\frac{VG}{N} \cdot \left(\frac{1}{V_{TR}} - \frac{1}{V_T}\right)\right]$$

Shockley-Read-Hall Generation and Trap Assisted Tunneling

$$T_{up} = \left(\frac{T_K}{T_{RK}} \right)^{3/2} \cdot \exp \left[\frac{VG + VLC}{2} \cdot \left(\frac{1}{V_{TR}} - \frac{1}{V_T} \right) \right]$$

$$CSRH_T = CSRH_{eff} \cdot T_{up}$$

$$CTAT_T = CTAT_{eff} \cdot T_{up}$$

$$ETAT_T = 70.8 \cdot T_K^{3/2}$$

Band to Band Tunneling

$$CBBT_T = CBBT_{eff} \text{ (temperature independent)}$$

$$F0 = 1.9 \times 10^7 \cdot \left(1.04 - \frac{4.21 \cdot 10^{-4} \cdot T_K^2}{636 + T_K} \right)$$

Avalanche Multiplication¹

$$dT = TEMP + DTA - 25^\circ C$$

$$Bn = 1.23 \cdot 10^6$$

$$Bn_T = Bn \cdot (1 + 7.2 \cdot 10^{-4} \cdot dT - 1.6 \cdot 10^{-6} \cdot dT^2)$$

Breakdown

$$VBR_T = VBR \cdot \left(\frac{T_K}{T_{RK}} \right)^{0.1}$$

$$EMVBR_T = EMVBR \cdot \left(\frac{VD_T + VBR_T}{VD + VBR} \right)^{(1-P)}$$

Resistance

1. 25°C is the reference temperature at which **Bn** has been determined

$$RS_T = RS \cdot \left(\frac{T_K}{T_{RK}} \right)^{PTRS}$$

Model Constants and Parameter Related Constants

$$K = 0.01$$

$$KET = 0.1$$

$$ETM = 3$$

Maximum Electric Field and Depletion Layer Width at Zero Bias

$$E_0 = \frac{EMVBR_T}{\left(1 + \frac{VBR_T}{VD_T}\right)^{1-P}}$$

$$W_0 = \frac{VD_T}{E_0 \cdot (1 - P)}$$

Capacitance and contact potential related temperature equations

The effective Energy Gap of P-N junction is defined as:

If $TLEV=0$ or 1

$$EG_{ff}(T) = 1.16 - 7.02 \cdot 10^{-4} \cdot \frac{T^2}{T + 1108}$$

else ($TLEV=2$)

$$EG_{eff}(T) = EG - GAP1 \cdot \frac{T^2}{T + GAP2}$$

If **TLEV C=0**

$$VJ(T) = VJ \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right)$$

$$PHP(T) = PHP \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right)$$

$$CJO(T) = CJO \cdot \left(1 + MJ \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta T - \frac{VJ(T)}{VJ} \right) \right)$$

$$CJSW(T) = CJSW \cdot \left(1 + MJSW \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta T - \frac{PHP(T)}{PHP} \right) \right)$$

If **TLEV C=1**

$$VJ(T) = VJ - TPB \cdot \delta T$$

$$PHP(T) = PHP - TPHP \cdot \delta T$$

$$CJO(T) = CJO \cdot (1 + CTA \cdot \delta T)$$

$$CJSW(T) = CJSW \cdot (1 + CTP \cdot \delta T)$$

If **TLEV C=2**

$$VJ(T) = VJ - TPB \cdot \delta T$$

$$PHP(T) = PHP - TPHP \cdot \delta T$$

$$CJO(T) = CJO \cdot \left(\frac{VJ}{VJ(T)} \right)^{MJ}$$

$$CJSW(T) = CJSW \cdot \left(\frac{PHP}{PHP(T)} \right)^{MJSW}$$

If **TLEV=3**

$$\begin{aligned} VJ(T) &= VJ + dpbdt \cdot \delta T \\ PHP(T) &= PHP + dphpdt \cdot \delta T \end{aligned}$$

$$CJO(T) = CJO \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\delta T}{VJ} \right)$$

$$CJSW(T) = CJSW \cdot \left(1 - 0.5 \cdot dphpdt \cdot \frac{\delta T}{PHP} \right)$$

where for **TLEV=0** or **1**,

$$\begin{aligned} dpbdt &= \frac{EGnom + 3 \cdot vtnom + (1.16 - EGnom) \cdot \left(2 - \frac{Tnom}{Tnom + 1108} \right) - VJ}{Tnom} \\ dphpdt &= \frac{EGnom + 3 \cdot vtnom + (1.16 - EGnom) \cdot \left(2 - \frac{Tnom}{Tnom + 1108} \right) - PHP}{Tnom} \end{aligned}$$

and **TLEV=2**

$$\begin{aligned} dpbdt &= \frac{EGnom + 3 \cdot vtnom + (EG - EGnom) \cdot \left(2 - \frac{Tnom}{Tnom + \mathbf{GAP2}} \right) - VJ}{Tnom} \\ dphpdt &= \frac{EGnom + 3 \cdot vtnom + (EG - EGnom) \cdot \left(2 - \frac{Tnom}{Tnom + \mathbf{GAP2}} \right) - PHP}{Tnom} \end{aligned}$$

9.3 Level 21 Current Calculations

Diode Currents

First the maximum reverse junction voltage is defined. Above this voltage the current will be extrapolated on a logarithmic scale.

$$V_j = \begin{cases} -0.99 \cdot VBR_T, & V_{AK1} < -0.99 VBR_T \\ V_{AK1}, & V_{AK1} \geq -0.99 VBR_T \end{cases}$$

Ideal Forward Current

$$Id_f = IS_T \left\{ \exp\left(\frac{V_j}{N \cdot V_T}\right) - 1 \right\}$$

Maximum Electric Field Depletion Layer Width

$$VD_j = \frac{\sqrt{\left\{ \left(1 - \frac{V_j}{VD_T}\right)^2 + \left(\frac{V_j}{VD_T}\right) \cdot K \right\}} + \left(1 - \frac{V_j}{VD_T}\right)}{2}$$

$$E_m = E_0 \cdot VD_j^{(1-P)}$$

$$W_d = W_0 \cdot VD_j^P$$

Shockley-Read-Hall Generation

$$I_{srh} = CSRH_T \cdot (W_d - W_0)$$

Trap Assisted Tunneling

$$ET_0 = \frac{\frac{E_0}{ETAT_T} + ETM - \sqrt{\left(\frac{E_0}{ETAT_T} - ETM\right)^2 + KET}}{2}$$

$$ET = \frac{\frac{E_m}{ETAT_T} + ETM - \sqrt{\left(\frac{E_m}{ETAT_T} - ETM\right)^2 + KET}}{2}$$

$$I_{tat} = CTAT \cdot W_d \cdot \left\{ \frac{\exp(ET^2) - \exp(ET_0^2)}{\frac{E_m}{ETAT_T}} \right\}$$

Non-ideal Forward Current including Tunneling

$$I_{S_{lf}} = CSRH_T \cdot \left\{ 6.28 + 38.58 \cdot \left(\frac{E_m}{ETAT_T} \right) \cdot \exp(ET^2) \right\} \cdot \frac{VT}{E_m}$$

$$I_{lf} = I_{S_{lf}} \cdot \frac{\exp\left(\frac{V_j}{N \cdot V_T}\right) - 1}{4 \cdot \exp\left(\frac{V_j}{2 \cdot N \cdot V_T}\right) + \exp\left(\frac{VLC}{2 \cdot N \cdot V_T}\right)} \cdot \exp\left(\frac{VLC}{2 \cdot N \cdot V_T}\right)$$

Band to Band Tunneling

$$I_{bbt} = \frac{-CBBT_T \cdot V_j}{\left(\frac{F0}{E_m}\right)^{1.5} \cdot \exp\left(\frac{F0}{E_m}\right)}$$

Avalanche Multiplication

$$\mu = 0.3295 \cdot \left(\frac{E_m}{EMVBR_T} \right)^2 \cdot \exp\left(\frac{Bn_T}{EMVBR_T} - \frac{Bn_T}{E_m} \right)$$

Total Diode Current

$$Id = \frac{(Id_f + I_{lf} - I_{srh}) \cdot \frac{1 + \exp(-2 \cdot \mu)}{2} - (I_{bbt} + I_{tat}) \cdot \exp(-\mu)}{1 - 2 \cdot \mu \cdot \{1 + \exp(-2 \cdot \mu)\}}$$

Extrapolation of the Reverse Current

$$I_{dBR} = I_d \quad \text{at } V_j = -0.99VBR_T$$

$$G_{dBR} = \frac{dI_d}{dV_j} \quad \text{at } V_j = -0.99VBR_T$$

$$ID = \begin{cases} I_d & V_{AK1} \geq -0.99VBR_T \\ I_{dBR} \cdot \exp\left[\left(\frac{V_{AK1} + 0.99VBR_T}{I_{dBR}}\right) G_{dBR}\right] & V_{AK1} < -0.99VBR_T \end{cases}$$

9.4 Level 21 Capacitance Calculations

In this model, the total diode capacitance is given as the sum of the diffusion and depletion diode capacitances, the last one is described by a junction bottom (area dependence) and a junction periphery (perimeter dependence) as: $Cd = CDEPa + CDEPp + CDIFF + CMETAL + CPOLY$

Depletion Capacitance

DCAP is the selector for the capacitance model.

The following equations are for the case of **DCAP** = 1 or 2; for the case of **DCAP**=2, put **FC** = **FCS** = 0 in the equations.

Bottom and sidewall depletion capacitance are similar in expressions. In the case of the shottky diode style, the parameter **KMS** models the effect of a different behavior of the depletion capacitance.

The P-N junction depletion bottom capacitance **CDEPa** is modeled through **FC**, **CJO**, **VJ**, **MJ** and **KMS**.

If $vd < FC \cdot VJ - KMS$ then $CDEPa = CJO_{eff} \cdot \left(1 - \frac{vd + KMS}{VJ}\right)^{-Mj}$

else $CDEPa = \frac{CJO_{eff}}{(1 - FC)^{1 + Mj}} \cdot \left(1 - FC \cdot (1 + MJ) + \frac{MJ \cdot (vd + KMS)}{VJ}\right)$

The P-N junction depletion sidewall capacitance $CDEPp$ is modeled using FC , $CJSW$, VJ , $MJSW$ and KMS .

$$\text{If } vd < FC \cdot VJ - KMS \text{ then } CDEPp = CJSW_{eff} \cdot \left(1 - \frac{vd + KMS}{VJ}\right)^{-MJSW}$$

else

$$CDEPp = \frac{CJSW_{eff}}{(1 - FC)^{1 + MJSW}} \cdot \left(1 - FC \cdot (1 + MJSW) + \frac{MJSW \cdot (vd + KMS)}{VJ}\right)$$

Diffusion Capacitance

The diffusion capacitance $CDIFF$ is defined as:

$$CDIFF = TAU \cdot \frac{\partial Id}{\partial vd} = TAU \cdot gd$$

Metal and Polysilicon Capacitance

The metal and polysilicon capacitance are determined as follows:

$$C_{metal} = \left(\frac{\epsilon_{ox}}{XOI}\right) \cdot (WP_{eff} + XP_{eff}) \cdot (LP_{eff} + XP_{eff}) \cdot M$$

$$C_{poly} = \left(\frac{\epsilon_{ox}}{XOM}\right) \cdot (WM_{eff} + XM_{eff}) \cdot (LM_{eff} + XM_{eff}) \cdot M$$

9.5 Level 21 Parameters

Nr.	Name	Description	Default	Units
1	LEVEL	Model Level	21	
2	IS	Saturation current	7.13×10^{-13}	A
3	JS	Saturation current density	1.0×10^{-14}	aAm^{-2}
4	JSW	Sidewall saturation current	0	aAm^{-2}

Nr.	Name	Description	Default	Units
5	N^b	Junction emission coefficient	1.044	
6	VLC	Voltage dependence at low forward currents	0.0	V
7	VBR	Breakdown voltage	7.459	V
8	EMVBR	Electric field at breakdown	1.36×10^6	V/cm
9	CSRH	Shockley-Read-Hall generation	7.44×10^{-7}	A/cm
10	CBBT	Band to band tunneling	3.255	A/V
11	CTAT	Trap assisted tunneling	3.31×10^{-6}	A/cm
12	RS	Series resistance	0.0	Ω
13	TAU (TT,TF)	Transit time	500.0×10^{-12}	s
14	VD	Diffusion voltage	0.90	V
15	TREF	Reference temperature	27.0	C
16	VG	Bandgap voltage	1.206	V
17	PTRS	Power for temperature dependence of RS	0.0	
18	KF	Flicker noise coefficient	0.0	
19	AF	Flicker noise exponent	1.0	
20	DTA	Difference between device temperature and ambient temperature	0.0	K
21	EXP_FLAG^c	Forward current exponential limitation	20	
Capacitance Related Model Parameters				
22	DCAP	Capacitance equation selector	1	
23	CJP (CJO, CJ, CJA)	Zero-bias junction capacitance	0	^a Fm ⁻²
24	M(P,MJ,EXA)	Grading coefficient	0.5	
25	MCV^d (PCV, MJCVA, EXACV)	Grading coefficient for the capacitance model	M	
26	CJSW (CJP)	Bulk sidewall capacitance	0	^a Fm ⁻¹
27	MJSW (EXP)	Bulk sidewall capacitance	0.33	
28	FC	Coefficient for forward bias depletion capacitance formula	0.5	
29	FCS	Coefficient for forward bias depletion periphery capacitance formula	FC	
30	KMS	Metal-semiconductor charge storage parameter	0	
31	VJ(PB,PHI)	Junction potential	1	V
32	PHP	Periphery junction potential	PB	V
Metal and Polysilicon Capacitor Parameters				
33	LM	Length of metal capacitor	0	m

Nr.	Name	Description	Default	Units
34	L_P	Length of polysilicon capacitor	0	m
35	W_M	Width of metal capacitor	0	m
36	W_P	Width of polysilicon capacitor	0	m
37	X_M	Accounts for masking and etching effects	0	m
38	X_{OI}	Thickness of the poly to bulk oxide	1.0×10^3	A
39	X_{OM}	Thickness of the metal to bulk oxide	1.0×10^3	A
40	X_P	Accounts for masking and etching effects	0	m
Temperature Related Model Parameters				
41	E_G	Activation energy	1.11	eV
42	C_{TA}	Temperature coefficient for area junction capacitance (TLEVC=1)	0	$^{\circ}\text{K}^{-1}$
43	C_{TP}	Temperature coefficient for periphery junction capacitance (TLEVC=1)	0	$^{\circ}\text{K}^{-1}$
44	G_{AP1}	First bandgap correction factor	7.02×10^{-4}	$\text{eV}^{\circ}\text{K}^{-1}$
45	G_{AP2}	Second bandgap correction factor	1108	$^{\circ}\text{K}$
46	T_{PB} (TVJ)	Temperature coefficient for PB	0	$\text{V}^{\circ}\text{K}^{-1}$
47	T_{PHP}	Temperature coefficient for PHP	0	$\text{V}^{\circ}\text{K}^{-1}$
48	T_{M1}	Temperature coefficient (Linear) for MJCV	0	$^{\circ}\text{K}^{-1}$
49	T_{M2}	Temperature coefficient (Quadratic) for MJVC	0	$^{\circ}\text{K}^{-2}$
50	T_{TT1}	Temperature coefficient (Linear) for TT	0	$^{\circ}\text{K}^{-1}$
51	T_{TT2}	Temperature coefficient (Quadratic) for TT	0	$^{\circ}\text{K}^{-2}$
Scaling Model Parameters				
52	S_{CALEV}	Scaling equation selector	2	
53	A_{REA}	Junction area	1	
54	P_{ERI}	Junction periphery	0	
55	L	Length of diode		m
56	W	Width of diode		m
57	S_{CALM}	Model parameter scaling factor	1	
58	S_{HRIK}	Shrink factor	1	
59	C_{SRH_0}	First coefficient geometrical update for CSRH	1.0	-
60	C_{SRH_1}	Second coefficient geometrical update for CSRH	0.0	$1/\text{m}^2$
61	C_{SRH_2}	Third coefficient geometrical update for CSRH	0.0	$1/\text{m}^4$
62	C_{SRH_3}	Fourth coefficient geometrical update for CSRH	0.0	$1/\text{m}^6$
63	C_{SRH_4}	Fifth coefficient geometrical update for CSRH	0.0	$1/\text{m}$
64	C_{SRH_5}	Sixth coefficient geometrical update for CSRH	0.0	$1/\text{m}^2$

Nr.	Name	Description	Default	Units
65	CSRH_6	Seventh coefficient geometrical update for CSRH	0.0	1/m ³
66	CTAT_0	First coefficient geometrical update for CTAT	1.0	-
67	CTAT_1	Second coefficient geometrical update for CTAT	0.0	1/m ²
68	CTAT_2	Third coefficient geometrical update for CTAT	0.0	1/m ⁴
69	CTAT_3	Fourth coefficient geometrical update for CTAT	0.0	1/m ⁶
70	CTAT_4	Fifth coefficient geometrical update for CTAT	0.0	1/m
71	CTAT_5	Sixth coefficient geometrical update for CTAT	0.0	1/m ²
72	CTAT_6	Seventh coefficient geometrical update for CTAT	0.0	1/m ³
73	CBBT_0	First coefficient geometrical update for CBBT	1.0	-
74	CBBT_1	Second coefficient geometrical update for CBBT	0.0	1/m ²
75	CBBT_2	Third coefficient geometrical update for CBBT	0.0	1/m ⁴
76	CBBT_3	Fourth coefficient geometrical update for CBBT	0.0	1/m ⁶
77	CBBT_4	Fifth coefficient geometrical update for CBBT	0.0	1/m
78	CBBT_5	Sixth coefficient geometrical update for CBBT	0.0	1/m ²
79	CBBT_6	Seventh coefficient geometrical update for CBBT	0.0	1/m ³

- a. The units of the marked parameters has changed as they are updated with geometry.
Note, the SCALE option is only in effect if AREA an PERI are element parameters. If AREA and PERI are model parameters then SCALM is in effect
- b. Parameter N should be close to unity and is not intended to simulate a current other than the usual injection of holes/electrons.
- c. The forward current equation is written in the form $Idf = \exp((Vd/Vt/n) + \log(Is)) - Is$. If the exponential argument $(Vd/Vt/n) + \log(Is)$ exceeds the value of the parameter EXP_FLAG, the forward current equation is linearized. The default value is set to that of diode level 1.
- d. The difference between MCV and M is that MCV is updated by temperature as stated by diode level 1 equations. It is used in the capacitance model only.

Chapter 2 BJT Level 1 Equations

1.0 Overview

The Bipolar Junction Transistor (BJT) model in Eldo is an adaptation of the integral charge control model of Gummel and Poon. This modified Gummel-Poon model extends the original model to include several effects at high bias levels. The model automatically simplifies to the less complex Ebers-Moll model when using default values. Parameter names used in the modified Gummel-Poon model have been chosen to be more easily understood by the program user, and to better reflect both physical and circuit design thinking.

2.0 Definitions and Conventions

This section defines the equations for the Bipolar Junction Transistor.

2.1 Current convention and displays

As for other devices, the convention for current flow in the pins of the BJT (C, B, E, S) is assumed to be positive when current is entering into the device. The pin-currents may be printed or plotted using $I(Qx.C)$ for the collector pin, $I(Qx.B)$ for the base pin, $I(Qx.E)$ for the emitter pin and $I(Qx.S)$ for the substrate pin.

2.2 Structure conventions

Because of the different possible transistor structures in IC device fabrication, the simulation of two different bipolar transistor structures is allowed as vertical and lateral structure. The model types defined by keywords NPN and PNP automatically set a vertical structure while LPNP type sets the lateral structure for PNP device. In Precise mode, the structure choice is achieved through the **LEVEL**

model parameter, so that **LEVEL=1** sets the vertical structure and **LEVEL=2** sets the lateral one.

The connection points and orientation of the substrate diode and capacitance to the internal collector or internal base nodes depend on the chosen structure (respectively vertical or lateral).

2.3 NPN and PNP convention

All the following equations are valid for a NPN device. For a PNP device, all voltage and current signs have to be inverted to provide the correct equations.

2.4 Internal variables

- vbe defines the internal base-internal emitter voltage
- vbc defines the internal base-internal collector voltage
- vcS defines the internal collector-Substrate voltage (Vertical only)
- vBS defines the external base-Substrate voltage (Lateral only)
- vbS defines the internal base-Substrate voltage (Lateral only)
- vBc defines the external base-internal collector voltage
- vBC defines the external base-external collector voltage (Lateral only).

3.0 Equivalent Circuit Schematics

3.1 For DC and TRANSIENT analysis

Vertical structure

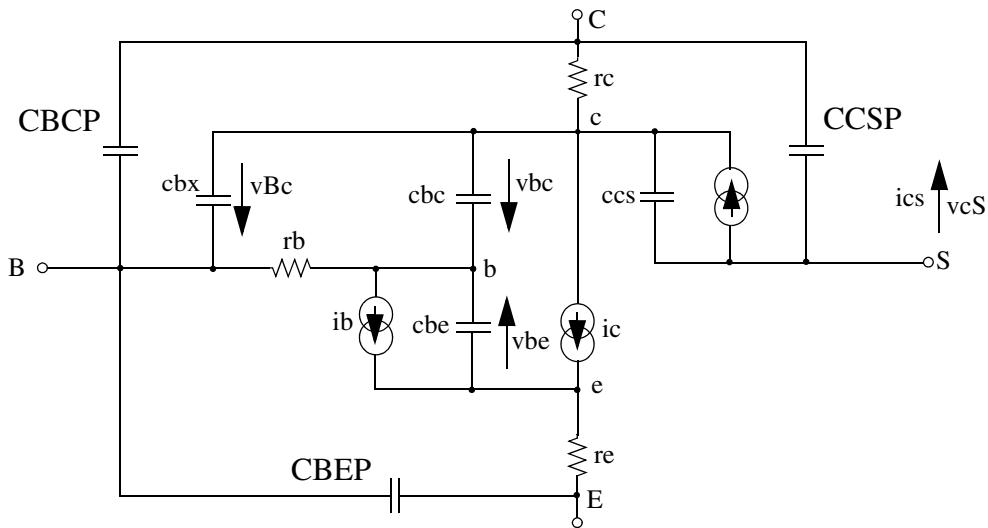


Figure 2-1. Equivalent circuit of vertical structure for DC and TRANSIENT analysis

Lateral structure

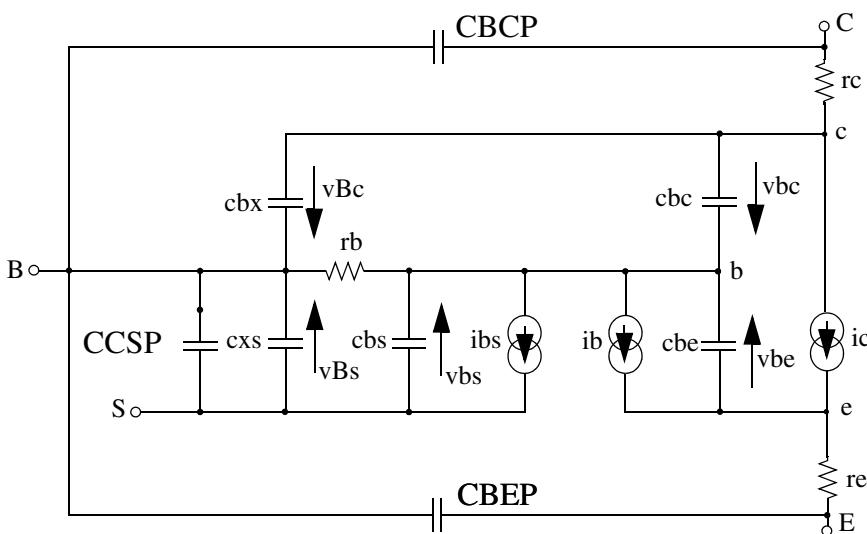


Figure 2-2. Equivalent circuit of lateral structure for DC and TRANSIENT analysis

3.2 For AC and NOISE analysis

Vertical structure

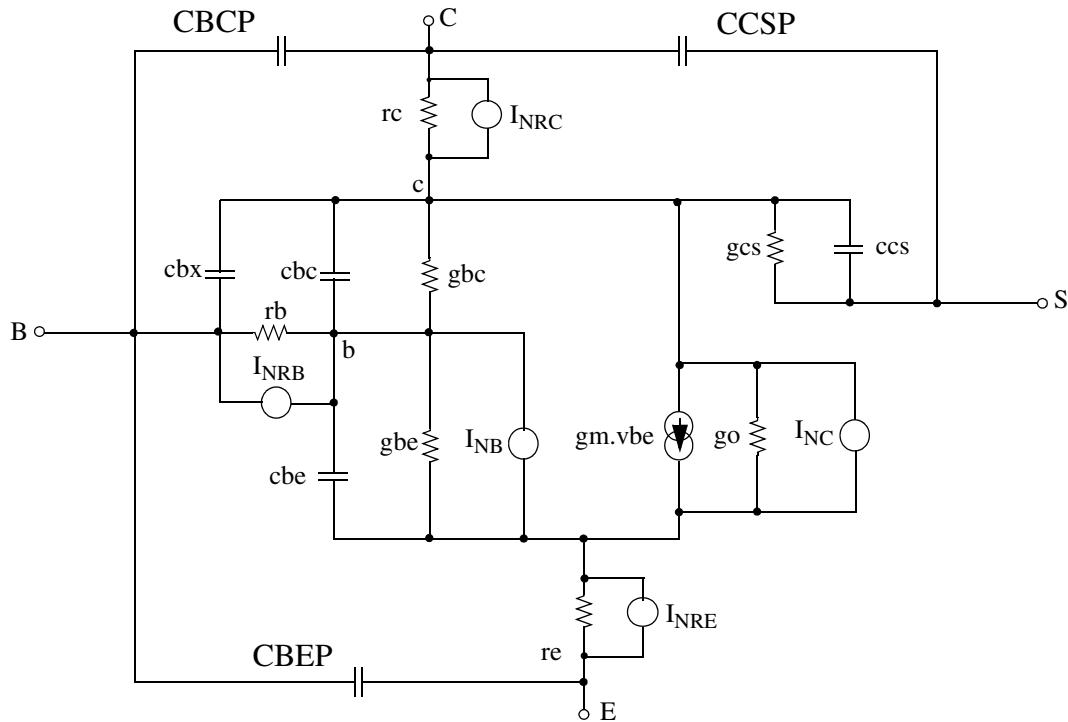


Figure 2-3. Equivalent circuit of vertical structure for AC & NOISE analysis

Lateral structure

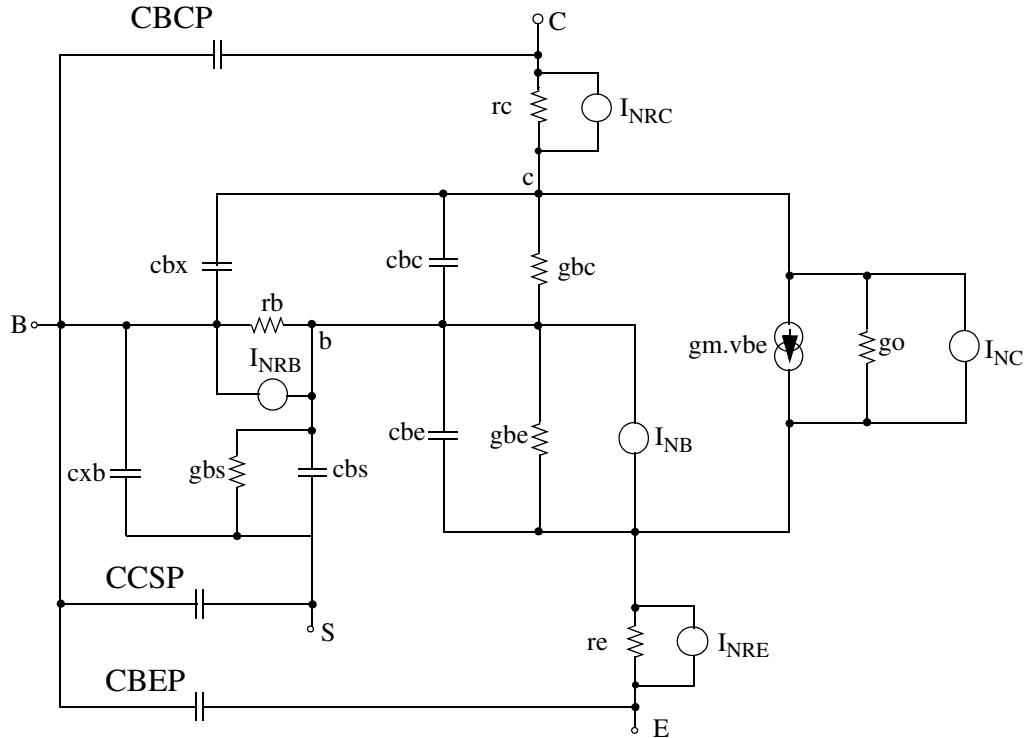


Figure 2-4. Equivalent circuit of lateral structure for AC & NOISE analysis

4.0 Scaling

If **IBE** and **IBC** are unspecified then **AREA_B** and **AREA_C** are not used and are set to the **AREA** value in all the equations.

If both **IBE** and **IBC** are specified then **AREA_B** and **AREA_C** are used as follows:

$$IBE_{eff} = IBE \cdot AREA \cdot M \quad IBC_{eff} = IBC \cdot AREA_B \cdot M$$

$$\text{Otherwise: } IBE_{eff} = IS \cdot AREA \cdot M \quad IBC_{eff} = IS \cdot AREA \cdot M$$

For a vertical structure device, the following relations apply:

If ISE is not specified then $ISE = C2 \cdot IS$

If ISC is not specified then $ISC = C4 \cdot IS$

$$ISE_{eff} = ISE \cdot AREA \cdot M \quad CJE_{eff} = CJE \cdot AREA \cdot M$$

$$ISC_{eff} = ISC \cdot AREAB \cdot M \quad CJC_{eff} = CJC \cdot AREAB \cdot M$$

$$ISS_{eff} = ISS \cdot AREAC \cdot M \quad CJS_{eff} = CJS \cdot AREAC \cdot M$$

The high current roll-off parameters IKF and IKR are scaled as follows:

$$IKF_{eff} = IKF \cdot AREA \cdot M \quad IKR_{eff} = IKR \cdot AREA \cdot M$$

For a lateral structure, $AREAB$ is replaced by $AREAC$, and $AREAC$ by $AREAB$, in all the equations.

5.0 DC Current Calculations

5.1 Collector and base currents

The forward current and gain characteristics are determined through parameters IS , IBE , ISE , BF , NF , NE and IKF . The parameters IS , IBC , ISC , BR , NR , NC and IKR determine the reverse current and gain characteristics. The elementary currents ibe , ibc , $iben$, $ibcn$ are determined as follows:

$$ibe = IBE_{eff} \cdot \left(\exp \frac{vbe}{NF \cdot Vt} - 1 \right) \quad ibc = IBC_{eff} \cdot \left(\exp \frac{vbc}{NR \cdot Vt} - 1 \right)$$

$$iben = ISE_{eff} \cdot \left(\exp \frac{vbe}{NE \cdot Vt} - 1 \right) \quad ibcn = ISC_{eff} \cdot \left(\exp \frac{vbc}{NC \cdot Vt} - 1 \right)$$

$iben$ and $ibcn$ represent the contribution of the recombination in the Base-Emitter and Base-Collector space charge regions at low injection levels.

The base charge factor qb is defined as: $qb = \frac{q1}{2} \cdot (1 + (1 + 4 \cdot q2)^{NKF})$

$$\text{where: } \frac{1}{q1} = 1 - \frac{vbc}{VAF} - \frac{vbc}{VAR} \quad q2 = \frac{ibe}{IKF_{eff}} + \frac{ibc}{IKR_{eff}}$$

where IKF_{eff} and IKR_{eff} are, respectively, the effective high current forward and reverse beta roll-off.

The total collector current, ic , and the total base current, ib , are calculated as:

$$ib = \frac{ibe}{BF} + \frac{ibc}{BR} + iben + ibcn \quad ic = \frac{ibe - ibc}{qb} - \frac{ibc}{BR} - ibcn$$

5.2 Substrate current

The substrate current is defined through the definition of a substrate diode, whose connection depends on the device structure (please refer also to the “[Structure conventions](#)” on page 2-1).

For the vertical BJT, the substrate diode current, ics , is defined as:

$$ics = ISS_{eff} \cdot \left(\exp \frac{vcS}{NSS \cdot Vt} - 1 \right)$$

For the lateral BJT, the substrate diode current, ibs , is defined as:

$$ibs = ISS_{eff} \cdot \left(\exp \frac{vbS}{NSS \cdot Vt} - 1 \right)$$

5.3 Quasi-saturation effects

Because power devices require increased voltage, current and power ratings, they present the problem of quasi-saturation. Therefore, the BJT model has been modified to include accurate modeling of this effect, through the addition of the model parameters **RSC**, **WC**, **WB**, **CONPO**, **TE** and **TBF**, if the **LQS** parameter is set to 1.

The critical collector current, $icrit$, is defined as:

$$icrit = \frac{CONPO - vbc}{RSC}$$

To accommodate both the reduction in available reverse-bias at the collector-base junction, and the expansion of base width which occurs as collector current is increased, the base push-out effect B is expressed as:

$$\begin{aligned} \text{If } & ic < icrit \quad \text{then} \quad B = 1 \\ \text{else} \quad & B = \left(1 + \frac{WC}{WB} \cdot \left(1 - \frac{icrit}{ic}\right)\right)^2 \end{aligned}$$

The qb and ic expressions are updated using the following equation for $q2$:

$$q2 = \frac{B \cdot ibe}{IKF_{eff}} + \frac{ibc}{IKR_{eff}}$$

The TF parameter is also updated as: $TF = TE + B \cdot TBF$ and is used as described in the Base-Emitter capacitance calculation section.

5.4 Series resistance

Three ohmic resistances rb , rc , re are included depending on RE , RC , RB , RBM , IRB model parameters mainly. They are calculated as:

$$rb = \frac{RB_{eff}}{M \cdot AREA} \quad rc = \frac{RC}{M \cdot AREA} \quad re = \frac{RE}{M \cdot AREA}$$

If IRB is not specified, $RB_{eff} = RBM + \frac{RB - RBM}{qb}$

else $RB_{eff} = RBM + 3 \cdot (RB - RBM) \cdot \left(\frac{\tan Z - Z}{Z \cdot \tan^2 Z}\right)$

where $Z = \frac{\pi^2}{24} \cdot \sqrt{\frac{IRB \cdot M \cdot AREA}{ib}} \cdot \left(\sqrt{1 + \frac{144 \cdot ib}{\pi^2 \cdot IRB \cdot M \cdot AREA}} - 1\right)$

6.0 Capacitance Calculations

DCAP is the selector for the capacitance model. If **DCAP**=2 then **FC**=0. The following equations are for the case of **DCAP**=1 or 2, for the case of **DCAP**=2 put **FC**=0 in the equations.

6.1 Base-emitter capacitance

The base-emitter capacitance, **cbe**, is the sum of the forward transit time (diffusion) capacitance and the depletion capacitance. So, **cbe** = **ctbe** + **cdbe**.

The transit time, **TF**, is bias dependent through parameters **XTF**, **ITF**, **VTF** to define the diffusion capacitance **ctbe** as follows:

$$ctbe = \frac{\partial}{\partial vbe} \left(TF \cdot \left(1 + XTF \cdot \left(\frac{ibe}{ibe + ITF \cdot M \cdot AREA} \right)^2 \cdot \exp\left(\frac{vbc}{1.44 \cdot VTF}\right) \right) \cdot \frac{ibe}{qb} \right)$$

The model parameters that influence the base-emitter depletion capacitance are **FC**, **CJE**, **VJE**, **MJE**.

$$\text{If } vbe < FC \cdot VJE \text{ then } cdbe = CJE_{eff} \cdot \left(1 - \frac{vbe}{VJE} \right)^{-MJE}$$

$$\text{else } cdbe = \frac{CJE_{eff}}{(1 - FC)^{1+MJE}} \cdot \left(1 - FC \cdot (1 + MJE) + \frac{MJE \cdot vbe}{VJE} \right)$$

6.2 Base-collector capacitance

The base-collector capacitance, **cbc**, is the sum of the reverse transit time (diffusion) capacitance through **TR** model parameter and the depletion capacitance through **CJC**, **FC**, **MJC**, **VJC**, **XCJC** model parameters.

To model the non-uniform charge distribution, the base-collector capacitance is distributed by connecting one capacitor, **cbx**, from the external base node to the internal collector node, controlled by the voltage **vBc**, and another by connecting

capacitor, c_{bc} , from the internal base node to the internal collector node, controlled by the voltage v_{bc} .

So, $c_{bc} = ctbc + XCJC \cdot cdbc$ and $c_{bx} = (1 - XCJC) \cdot cdbx$.

The diffusion capacitance, $ctbc$, is defined as: $ctbc = TR \cdot \frac{\partial ibc}{\partial vbc}$

The internal depletion capacitance, $cdbc$, is calculated as:

$$\text{If } v_{bc} < FC \cdot VJC \text{ then } cdbc = CJC_{eff} \cdot \left(1 - \frac{v_{bc}}{VJC}\right)^{-MJC}$$

$$\text{else } cdbc = \frac{CJC_{eff}}{(1 - FC)^{1 + MJC}} \cdot \left(1 - FC \cdot (1 + MJC) + \frac{MJC \cdot v_{bc}}{VJC}\right)$$

The external depletion capacitance, $cdbx$, is calculated as:

$$\text{If } v_{Bc} < FC \cdot VJC \text{ then } cdbx = CJC_{eff} \cdot \left(1 - \frac{v_{Bc}}{VJC}\right)^{-MJC}$$

$$\text{else } cdbx = \frac{CJC_{eff}}{(1 - FC)^{1 + MJC}} \cdot \left(1 - FC \cdot (1 + MJC) + \frac{MJC \cdot v_{Bc}}{VJC}\right)$$

6.3 Substrate capacitance

The connection of the substrate capacitance depends on the chosen (vertical or lateral) structure of the device.

For vertical BJT, the collector to substrate capacitance, ccs , is modeled as a depletion capacitance. The input model parameters affecting it are CJS , VJS , MJS .

$$\text{If } vcS < 0 \text{ then } ccs = CJS_{eff} \cdot \left(1 - \frac{vcS}{VJS}\right)^{-MJS}$$

$$\text{else } ccs = CJS_{eff} \cdot \left(1 + \frac{MJS \cdot vcS}{VJS}\right)$$

For lateral BJT, the base to substrate capacitances are modeled as depletion capacitances. The input model parameters affecting them are also **CJS**, **VJS**, **MJS**, where **VJS** represents the B-S zero built-in potential and **CJS** is the zero-bias base-substrate capacitance. Similarly to the collector capacitance, the base to substrate capacitance may be distributed between external and internal base nodes through the model parameter **XJBS**.

The internal base to substrate capacitance, **cbs**, is controlled by the voltage **vBS** as:

$$\text{If } vBS < 0 \text{ then } cbs = CJS_{eff} \cdot \left(1 - \frac{vBS}{VJS}\right)^{-MJS} \cdot XJBS$$

$$\text{else } cbs = CJS_{eff} \cdot \left(1 + \frac{MJS \cdot vBS}{VJS}\right) \cdot XJBS$$

The external base to substrate capacitance, **cxs**, is controlled by the voltage **vBS** as:

$$\text{If } vBS < 0 \text{ then } cxs = CJS_{eff} \cdot \left(1 - \frac{vBS}{VJS}\right)^{-MJS} \cdot (1 - XJBS)$$

$$\text{else } cxs = CJS_{eff} \cdot \left(1 + \frac{MJS \cdot vBS}{VJS}\right) \cdot (1 - XJBS)$$

7.0 Temperature Related Equations

7.1 General definitions

$$Vt(T) = k_B \cdot \frac{T}{q} \quad \delta T = T - T_{nom}$$

If **TLEV** = 2 then an improved effective Energy Gap of PN junction is used:

$$EG_{eff}(T) = EG - GAP1 \cdot \frac{T^2}{T + GAP2}$$

$$fact = \frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + XTI \cdot \ln \frac{T}{T_{nom}}$$

Otherwise they are defined as:

$$EG_{eff}(T) = 1.16 - 7.02 \cdot 10^{-4} \cdot \frac{T^2}{T + 1108}$$

$$fact = \frac{EG}{Vt(T_{nom})} - \frac{EG}{Vt(T)} + XTI \cdot \ln \frac{T}{T_{nom}}$$

7.2 Saturation current, beta, IKF, IKR and IRB equations

(**TLEV** = 0, 1 or 2)

If **TLEV** = 1 then a modified relation is applied for **factor** and calculated as:

$$factor = 1 + XTB \cdot \delta T$$

Otherwise if **TLEV** = 0 or 2:

$$factor = \left(\frac{T}{T_{nom}} \right)^{XTB}$$

If **TBF1** & **TBF2** are equal to 0 (**TBR1** & **TBR2** are equal to 0), the forward (and reverse) gain are then updated as:

$$\begin{aligned} BF(T) &= BF \cdot factor \\ BR(T) &= BR \cdot factor \end{aligned}$$

Otherwise, **BF** (and **BR**) are updated with the **TBF1** & **TBF2** (**TBR1** & **TBR2**) as shown in “Other temperature equations” on page 2-17.

$$\begin{aligned} IS(T) &= IS \cdot \exp(fact) & ISE(T) &= \frac{ISE}{factor} \cdot \exp\left(\frac{fact}{NE}\right) \\ ISC(T) &= \frac{ISC}{factor} \cdot \exp\left(\frac{fact}{NC}\right) & ISS(T) &= \frac{ISS}{factor} \cdot \exp\left(\frac{fact}{NS}\right) \end{aligned}$$

If both **IBE** and **IBC** are defined, then they vary as:

$$IBE(T) = IBE \cdot \exp\left(\frac{fact}{NF}\right) \quad IBC(T) = IBC \cdot \exp\left(\frac{fact}{NR}\right)$$

The parameters **IRB**, **IKF** and **IKR** are modified as follows (**TLEV=0, 1 or 2**):

$$\begin{aligned} IKF(T) &= IKF \cdot (1 + TIKF1 \cdot \delta T + TIKF2 \cdot \delta T^2) \\ IKR(T) &= IKR \cdot (1 + TIKR1 \cdot \delta T + TIKR2 \cdot \delta T^2) \\ IRB(T) &= IRB \cdot (1 + TIRB1 \cdot \delta T + TIRB2 \cdot \delta T^2) \end{aligned}$$

(TLEV = 3)

The temperature equations for the saturation currents are:

$$\begin{aligned} IS(T) &= IS^{(1 + TIS1 \cdot \delta T + TIS2 \cdot \delta T^2)} \\ IBE(T) &= IBE^{(1 + TIS1 \cdot \delta T + TIS2 \cdot \delta T^2)} \\ IBC(T) &= IBC^{(1 + TIS1 \cdot \delta T + TIS2 \cdot \delta T^2)} \\ ISE(T) &= ISE^{(1 + TISE1 \cdot \delta T + TISE2 \cdot \delta T^2)} \\ ISC(T) &= ISC^{(1 + TISC1 \cdot \delta T + TISC2 \cdot \delta T^2)} \\ ISS(T) &= ISS^{(1 + TISS1 \cdot \delta T + TISS2 \cdot \delta T^2)} \end{aligned}$$

The parameters **IRB**, **IKF** and **IKR** are modified as follows:

$$\begin{aligned} IRB(T) &= IRB^{(1 + TIRB1 \cdot \delta T + TIRB2 \cdot \delta T^2)} \\ IKF(T) &= IKF^{(1 + TIKF1 \cdot \delta T + TIKF2 \cdot \delta T^2)} \\ IKR(T) &= IKR^{(1 + TIKR1 \cdot \delta T + TIKR2 \cdot \delta T^2)} \end{aligned}$$

7.3 Resistance related temperature equations

$$RC(T) = RC \cdot (1 + TRC1 \cdot \delta T + TRC2 \cdot \delta T^2)$$

$$RE(T) = RE \cdot (1 + TRE1 \cdot \delta T + TRE2 \cdot \delta T^2)$$

$$RB(T) = RB \cdot (1 + TRB1 \cdot \delta T + TRB2 \cdot \delta T^2)$$

$$RBM(T) = RBM \cdot (1 + TRM1 \cdot \delta T + TRM2 \cdot \delta T^2)$$



The resistor values of ***RB***, ***RC***, ***RE*** and ***RBM*** after temperature update are clipped to 1×10^{-5} if less than 1×10^{-5} . This is only valid under the **ACM** flag.

7.4 Capacitance related temperature equations

The parameters ***MJE*** and ***MJC*** are updated using the following equations:

$$MJE(T) = MJE \cdot (1 + TMJE1 \cdot \delta T + TMJE2 \cdot \delta T^2)$$

$$MJC(T) = MJC \cdot (1 + TMJC1 \cdot \delta T + TMJC2 \cdot \delta T^2)$$

If (**TUDJS** = 1 and **TLEVVC**=0) or (**TLEVVC** = 1, 2 or 3) then ***MJS*** is updated as follows:

$$MJS(T) = MJS \cdot (1 + TMJS1 \cdot \delta T + TMJS2 \cdot \delta T^2)$$

For the case of **TLEVVC=0**

$$VJE(T) = VJE \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right)$$

$$CJE(T) = CJE \cdot \left(1 + MJE(T) \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta T - \frac{VJE(T)}{VJE} \right) \right)$$

$$VJC(T) = VJC \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right)$$

$$CJC(T) = CJC \cdot \left(1 + MJC(T) \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta T - \frac{VJC(T)}{VJC} \right) \right)$$

If **TUDJS** = 1 then **MJS**, **VJS**, and **CJS** are updated as follows:

$$VJS(T) = VJS \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right)$$

$$CJS(T) = CJS \cdot \left(1 + MJS(T) \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta T - \frac{VJS(T)}{VJS} \right) \right)$$

For the case of **TLEV=1**

$$CJE(T) = CJE \cdot (1 + CTE \cdot \delta T)$$

$$CJC(T) = CJC \cdot (1 + CTC \cdot \delta T)$$

$$CJS(T) = CJS \cdot (1 + CTS \cdot \delta T)$$

$$VJE(T) = VJE - TVJE \cdot \delta T$$

$$VJC(T) = VJC - TVJC \cdot \delta T$$

$$VJS(T) = VJS - TVJS \cdot \delta T$$

For the case of **TLEV=2**

$$CJE(T) = CJE \cdot \left(\frac{VJE}{VJE(T)} \right)^{MJE}$$

$$CJC(T) = CJC \cdot \left(\frac{VJC}{VJC(T)} \right)^{MJC}$$

$$CJS(T) = CJS \cdot \left(\frac{VJS}{VJS(T)} \right)^{MJS}$$

$$VJE(T) = VJE - TVJE \cdot \delta T$$

$$VJC(T) = VJC - TVJC \cdot \delta T$$

$$VJS(T) = VJS - TVJS \cdot \delta T$$

For the case of **TLEV=3**

$$CJE(T) = CJE \cdot \left(1 - 0.5 \cdot dvjedt \cdot \frac{\delta T}{VJE}\right)$$

$$CJC(T) = CJC \cdot \left(1 - 0.5 \cdot dvjcdt \cdot \frac{\delta T}{VJC}\right)$$

$$CJS(T) = CJS \cdot \left(1 - 0.5 \cdot dvjsdt \cdot \frac{\delta T}{VJS}\right)$$

$$VJE(T) = VJE + dvjedt \cdot \delta T$$

$$VJC(T) = VJC + dvjcdt \cdot \delta T$$

$$VJS(T) = VJS + dvjsdt \cdot \delta T$$

where for **TLEV=0, 1 or 3**

$$dvjedt = \frac{EG_{eff}(T_{nom}) + 3 \cdot Vt(T_{nom}) + (1.16 - EG_{eff}(T_{nom})) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + 1108}\right) - VJE}{T_{nom}}$$

$$dvjcdt = \frac{EG_{eff}(T_{nom}) + 3 \cdot Vt(T_{nom}) + (1.16 - EG_{eff}(T_{nom})) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + 1108}\right) - VJC}{T_{nom}}$$

$$dvjsdt = \frac{EG_{eff}(T_{nom}) + 3 \cdot Vt(T_{nom}) + (1.16 - EG_{eff}(T_{nom})) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + 1108}\right) - VJS}{T_{nom}}$$

while for **TLEV=2**

$$dvjedt = \frac{EG_{eff}(T_{nom}) + 3 \cdot Vt(T_{nom}) + (EG - EG_{eff}(T_{nom})) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + GAP2}\right) - VJE}{T_{nom}}$$

$$dvjcdt = \frac{EG_{eff}(T_{nom}) + 3 \cdot Vt(T_{nom}) + (EG - EG_{eff}(T_{nom})) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + GAP2}\right) - VJC}{T_{nom}}$$

$$dvjsdt = \frac{EG_{eff}(T_{nom}) + 3 \cdot Vt(T_{nom}) + (EG - EG_{eff}(T_{nom})) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + GAP2}\right) - VJS}{T_{nom}}$$

where, **EG_{nom}** is EG at nominal temperature;
vtnom is Vt at nominal temperature.

7.5 Other temperature equations

$$VAF(T) = VAF \cdot (1 + TVAF1 \cdot \delta T + TVAF2 \cdot \delta T^2)$$

$$VAR(T) = VAR \cdot (1 + TVAR1 \cdot \delta T + TVAR2 \cdot \delta T^2)$$

$$TF(T) = TF \cdot (1 + TTF1 \cdot \delta T + TTF2 \cdot \delta T^2)$$

$$TR(T) = TR \cdot (1 + TTR1 \cdot \delta T + TTR2 \cdot \delta T^2)$$

$$ITF(T) = ITF \cdot (1 + TITF1 \cdot \delta T + TITF2 \cdot \delta T^2)$$

$$NF(T) = NF \cdot (1 + TNF1 \cdot \delta T + TNF2 \cdot \delta T^2)$$

$$NR(T) = NR \cdot (1 + TNR1 \cdot \delta T + TNR2 \cdot \delta T^2)$$

$$NE(T) = NE \cdot (1 + TNE1 \cdot \delta T + TNE2 \cdot \delta T^2)$$

$$NC(T) = NC \cdot (1 + TNC1 \cdot \delta T + TNC2 \cdot \delta T^2)$$

$$NS(T) = NS \cdot (1 + TNS1 \cdot \delta T + TNS2 \cdot \delta T^2)$$

BF and **BR** are updated by temperature using the following equations for all **TLEVs**:

$$BF(T) = BF \cdot (1 + TBF1 \cdot \delta T + TBF2 \cdot \delta T^2)$$

$$BR(T) = BR \cdot (1 + TBR1 \cdot \delta T + TBR2 \cdot \delta T^2)$$

8.0 Noise

Two different noise sources exist. Refer to the noise model in [Figure 2-3 on page 2-4](#) and [Figure 2-4 on page 2-5](#).

Base to Emitter Noise

- Shot Noise

$$SI = 2 \times q \times IB$$

where IB is the current through the base.

- Flicker Noise

$$SI = \frac{KF \times IB^{AF}}{f}$$

Collector to Emitter Noise

- Shot Noise

$$SI = 2 \times q \times IC$$

where IC is the current through the collector.

Thermal Noise

$$SI = \frac{4 \times k \times T}{RB}, SI = \frac{4 \times k \times T}{RE}, SI = \frac{4 \times k \times T}{RC}$$

where RB, RE, RC , represent the base, emitter, collector resistances respectively.

9.0 Model Parameters

Nr.	Name	Description	Default	Units
DC Related Model Parameters				
1	IS	Transport saturation current	1.0×10^{-16}	A
2	IBE	Saturation current for base-emitter junction	0	A
3	IBC	Saturation current for base-collector junction	0	A
4	NR	Reverse current emission coefficient	1	
5	NF	Forward current emission coefficient	1	
6	BR (BRM)	Ideal maximum reverse beta	1	
7	BF (BFM)	Ideal maximum forward beta	100	
8	ISE (JLE)	B-E leakage saturation current	0	A
9	NE (NLE)	B-E leakage emission coefficient	1.5	
10	ISC (JLC)	B-C leakage saturation current	0	A
11	NC (NLC)	B-C leakage emission coefficient	2	
12	ISS	Saturation current for substrate junction	0	A
13	NS (NSS)	Substrate current emission coefficient	1	
14	VAF (VA, VBF)	Forward early voltage	∞	V
15	VAR (VBAR, VB, VRB, BV)	Reverse early voltage	∞	V
16	IKF (IK, JBF)	Corner current for forward beta high current roll-off	∞	A
17	IKR (JBR)	Corner current for reverse beta high current roll-off	∞	A
18	C2	Forward low-current non-ideal base current	0	A
19	C4	Reverse low-current non-ideal base current	0	A
20	NKF (NK)	Exponent for high current Beta roll-off	0.5	
Parasitic Resistance Related Model Parameters				
21	RB	Zero bias base resistance	0	Ω
22	RC	Collector resistance	0	Ω
23	RE	Emitter resistance	0	Ω
24	RBM	Minimum base resistance at high currents	RB	Ω
25	IRB (JRB, IOB)	Current where the base resistance falls halfway to its minimum value	∞	A
Parasitic Capacitance Related Model Parameters				
26	CBCP	External base-collector constant capacitance	0	F
27	CBEP	External base-emitter constant capacitance	0	F

Nr.	Name	Description	Default	Units
28	CCSP	External collector-substrate constant capacitance (vertical) or base-substrate (lateral)	0	F
Junction Capacitance Related Model Parameters				
29	DCAP	Capacitance model selector	1	
30	CJE	B-E zero-bias depletion capacitance	0	F
31	VJE (PE)	B-E built-in potential	0.75	V
32	MJE (ME)	B-E junction exponential factor	0.33	
33	CJC	B-C zero-bias depletion capacitance	0	F
34	VJC (PC)	B-C built-in potential	0.75	V
35	MJC (MC)	B-C junction exponential factor	0.33	
36	XCJC (CDIS)	Fraction of base-collector depletion capacitance connected to the internal base node	1	
37	XJBS	For lateral devices; Portion of the base-substrate depletion capacitance connected to the internal base node	1	
38	CJS (CCS, CSUB)	Zero-bias collector substrate capacitance	0	F
39	VJS (PS, CSUB)	Substrate junction built-in potential	0.75	V
40	MJS (MS, ESUB)	Substrate junction exponential factor	0	
41	FC	Coefficient for the calculation of the forward bias depletion capacitance	0.5	
Dynamic Model Parameters				
42	TF	Ideal forward transient time	0	s
43	XTF	Coefficient for bias dependence of TF	0	
44	VTF	Voltage describing dependence of TF on the base-collector voltage, VBC	∞	V
45	ITF (JTF)	High current parameter effecting TF	0	A
46	TR	Ideal reverse transit time	0	s
47	PTF	Excess phase at frequency=1.0/(TF .2p) Hertz	0	$^\circ$
Noise Related Model Parameters				
48	KF	Flicker noise coefficient	0	
49	AF	Flicker noise exponent	1	
Temperature Related Model Parameters				
50	TNOM (TREF)	Nominal temperature	27	°C
51	TMOD	Model temperature	TNOM	°C
52	TLEV	Temperature equation selector	0	
53	TLEVVC	Temperature equation selector for junction capacitance and potential	0	

Nr.	Name	Description	Default	Units
54	TUDJS	Flag for updating substrate junction capacitance, potential and exponential factor	1	
55	GAP1	First bandgap correction factor	7.02×10^{-4}	eV $^{\circ}\text{K}^{-1}$
56	GAP2	Second bandgap correction factor	1108	$^{\circ}\text{K}$
57	EG	Energy gap for temperature effect on IS	1.11	eV
58	XTB (TB, TCB)	Forward and reverse beta temperature exponent	0	
59	XTI	Temperature exponent for effect on IS	3	
60	TBF1	Temperature coefficient (Linear) for BF	0	$^{\circ}\text{C}^{-1}$
61	TBF2	Temperature coefficient (Quadratic) for BF	0	$^{\circ}\text{C}^{-2}$
62	TBR1	Temperature coefficient (Linear) for BR	0	$^{\circ}\text{C}^{-1}$
63	TBR2	Temperature coefficient (Quadratic) for BR	0	$^{\circ}\text{C}^{-2}$
64	TIRB1	Temperature coefficient (Linear) for IRB	0	$^{\circ}\text{C}^{-1}$
65	TIRB2	Temperature coefficient (Quadratic) for IRB	0	$^{\circ}\text{C}^{-2}$
66	TIKF1	Temperature coefficient (Linear) for IKF	0	$^{\circ}\text{C}^{-1}$
67	TIKF2	Temperature coefficient (Quadratic) for IKF	0	$^{\circ}\text{C}^{-2}$
68	TIKR1	Temperature coefficient (Linear) for IKR	0	$^{\circ}\text{C}^{-1}$
69	TIKR2	Temperature coefficient (Quadratic) for IKR	0	$^{\circ}\text{C}^{-2}$
70	TITF1	Temperature coefficient (Linear) for ITF	0	$^{\circ}\text{C}^{-1}$
71	TITF2	Temperature coefficient (Quadratic) for ITF	0	$^{\circ}\text{C}^{-2}$
72	TMJC1	Temperature coefficient (Linear) for MJC	0	$^{\circ}\text{K}^{-1}$
73	TMJC2	Temperature coefficient (Quadratic) for MJC	0	$^{\circ}\text{K}^{-2}$
74	TMJE1	Temperature coefficient (Linear) for MJE	0	$^{\circ}\text{K}^{-1}$
75	TMJE2	Temperature coefficient (Quadratic) for MJE	0	$^{\circ}\text{K}^{-2}$
76	TMJS1	Temperature coefficient (Linear) for MJS	0	$^{\circ}\text{K}^{-1}$
77	TMJS2	Temperature coefficient (Quadratic) for MJS	0	$^{\circ}\text{K}^{-2}$
78	TRB1 (TRB)	Temperature coefficient (Linear) for RB	0	$^{\circ}\text{C}^{-1}$
79	TRB2	Temperature coefficient (Quadratic) for RB	0	$^{\circ}\text{C}^{-2}$
80	TRC1 (TRC)	Temperature coefficient (Linear) for RC	0	$^{\circ}\text{C}^{-1}$
81	TRC2	Temperature coefficient (Quadratic) for RC	0	$^{\circ}\text{C}^{-2}$
82	TRE1 (TRE)	Temperature coefficient (Linear) for RE	0	$^{\circ}\text{C}^{-1}$
83	TRE2	Temperature coefficient (Quadratic) for RE	0	$^{\circ}\text{C}^{-2}$
84	TRM1 (TRBM1)	Temperature coefficient (Linear) for RBM	0	$^{\circ}\text{C}^{-1}$
85	TRM2 (TRBM2)	Temperature coefficient (Quadratic) for RBM	0	$^{\circ}\text{C}^{-2}$
86	TTF1	Temperature coefficient (Linear) for TF	0	$^{\circ}\text{K}^{-1}$
87	TTF2	Temperature coefficient (Quadratic) for TF	0	$^{\circ}\text{K}^{-2}$

Nr.	Name	Description	Default	Units
88	TTR1	Temperature coefficient (Linear) for TR	0	$^{\circ}\text{K}^{-1}$
89	TTR2	Temperature coefficient (Quadratic) for TR	0	$^{\circ}\text{K}^{-2}$
90	TVAF1	Temperature coefficient (Linear) for VAF	0	$^{\circ}\text{K}^{-1}$
91	TVAF2	Temperature coefficient (Quadratic) for VAF	0	$^{\circ}\text{K}^{-2}$
92	TVAR1	Temperature coefficient (Linear) for VAR	0	$^{\circ}\text{K}^{-1}$
93	TVAR2	Temperature coefficient (Quadratic) for VAR	0	$^{\circ}\text{K}^{-2}$
94	TISC1	Temperature coefficient (Linear) for ISC	0	$^{\circ}\text{K}^{-1}$
95	TISC2	Temperature coefficient (Quadratic) for ISC	0	$^{\circ}\text{K}^{-2}$
96	TIS1	Temperature coefficient (Linear) for IS or IBE and IBC	0	$^{\circ}\text{K}^{-1}$
97	TIS2	Temperature coefficient (Quadratic) for IS or IBE and IBC	0	$^{\circ}\text{K}^{-2}$
98	TISE1	Temperature coefficient (Linear) for ISE	0	$^{\circ}\text{K}^{-1}$
99	TISE2	Temperature coefficient (Quadratic) for ISE	0	$^{\circ}\text{K}^{-2}$
100	TISS1	Temperature coefficient (Linear) for ISS	0	$^{\circ}\text{K}^{-1}$
101	TISS2	Temperature coefficient (Quadratic) for ISS	0	$^{\circ}\text{K}^{-2}$
102	TNC1	Temperature coefficient (Linear) for NC	0	$^{\circ}\text{K}^{-1}$
103	TNC2	Temperature coefficient (Quadratic) for NC	0	$^{\circ}\text{K}^{-2}$
104	TNE1	Temperature coefficient (Linear) for NE	0	$^{\circ}\text{K}^{-1}$
105	TNE2	Temperature coefficient (Quadratic) for NE	0	$^{\circ}\text{K}^{-2}$
106	TNF1	Temperature coefficient (Linear) for NF	0	$^{\circ}\text{K}^{-1}$
107	TNF2	Temperature coefficient (Quadratic) for NF	0	$^{\circ}\text{K}^{-2}$
108	TNR1	Temperature coefficient (Linear) for NR	0	$^{\circ}\text{K}^{-1}$
109	TNR2	Temperature coefficient (Quadratic) for NR	0	$^{\circ}\text{K}^{-2}$
110	TNS1	Temperature coefficient (Linear) for NS	0	$^{\circ}\text{K}^{-1}$
111	TNS2	Temperature coefficient (Quadratic) for NS	0	$^{\circ}\text{K}^{-2}$
112	CTC	Temperature coefficient for zero-bias base collector capacitance (used with TLEVVC=1)	0	$^{\circ}\text{K}^{-1}$
113	CTE	Temperature coefficient for zero-bias base emitter capacitance (used with TLEVVC=1)	0	$^{\circ}\text{K}^{-1}$
114	CTS	Temperature coefficient for zero-bias substrate capacitance (used with TLEVVC=1)	0	$^{\circ}\text{K}^{-1}$
115	TVJC	Temperature coefficient for VJC (used with TLEVVC=1,2)	0	$\text{V}^{\circ}\text{K}^{-1}$
116	TVJE	Temperature coefficient for VJE (used with TLEVVC=1,2)	0	$\text{V}^{\circ}\text{K}^{-1}$
117	TVJS	Temperature coefficient for VJS (used with TLEVVC=1,2)	0	$\text{V}^{\circ}\text{K}^{-1}$

Nr.	Name	Description	Default	Units
PRECISE Compatibility Model Parameters				
118	TCBR1	PRECISE compatibility parameter for TRB1	0	$^{\circ}\text{C}^{-1}$
119	TCBR2	PRECISE compatibility parameter for TRB2	0	$^{\circ}\text{C}^{-2}$
120	TCCR1	PRECISE compatibility parameter for TRC1	0	$^{\circ}\text{C}^{-1}$
121	TCCR2	PRECISE compatibility parameter for TCR2	0	$^{\circ}\text{C}^{-2}$
122	TCER1	PRECISE compatibility parameter for TRE1	0	$^{\circ}\text{C}^{-1}$
123	TCER2	PRECISE compatibility parameter for TRE2	0	$^{\circ}\text{C}^{-2}$
PRECISE Model Parameters (Used ONLY in PRECISE Mode)				
124	ISS	Substrate diode saturation current	0	A
125	NSS (NS)	Substrate diode emission coefficient	1	
126	CONPO	Contact potential	0.5	V
127	LQS	Quasi-sat model index (if 0, Q-sat model not used)	0	
128	TE	Emitter delay time	1.0×10^{-6}	s
129	TBF	Base transit time	0.5×10^{-6}	s
130	RSC	n-region resistance	0	Ω
131	WC	n-region width	0	m
132	WB	p-base width	1.0×10^{-6}	m
133	TLEV	Temperature model switch		

Chapter 3

Mextram Equations

1.0 Introduction

This is the implementation of the Philips Mextram Bipolar Model 503.2 in Eldo. The basis of this work is the unclassified report 006/94 published by Philips Nat.lab., June 1995. In this model, the current through the epilayer is an explicit and continuous function of the internal and external base-collector junction voltages. The model covers all possible modes of operation such as ohmic current flow, saturated current flow and base push out both in the forward and reverse mode of operation.



Note For further information, please refer to the Philips Nat.lab. unclassified report Nr. 006/94 "The Mextram Bipolar Transistor Model, level 503.2" by H.C. de Graaff and W.J. Kloosterman issued in June 1995.

2.0 Survey of Modeled Effects

The model incorporates the following:

- Temperature effects
- Charge storage effects
- High-injection effects
- Built-in electric field in the base region
- Bias-dependent Early effect

- Low-level, non-ideal base currents
- Hard, and quasi-saturation
- Weak avalanche
- Hot carrier effects in the collector epilayer
- Explicit modeling of inactive regions
- Split base-collector depletion capacitance
- Current crowding and conductivity modulation for base resistance
- First order approximation of distributed high frequency effects in the intrinsic base (high frequency current crowding and excess phase-shifts).

3.0 Equivalent Circuits and Equations

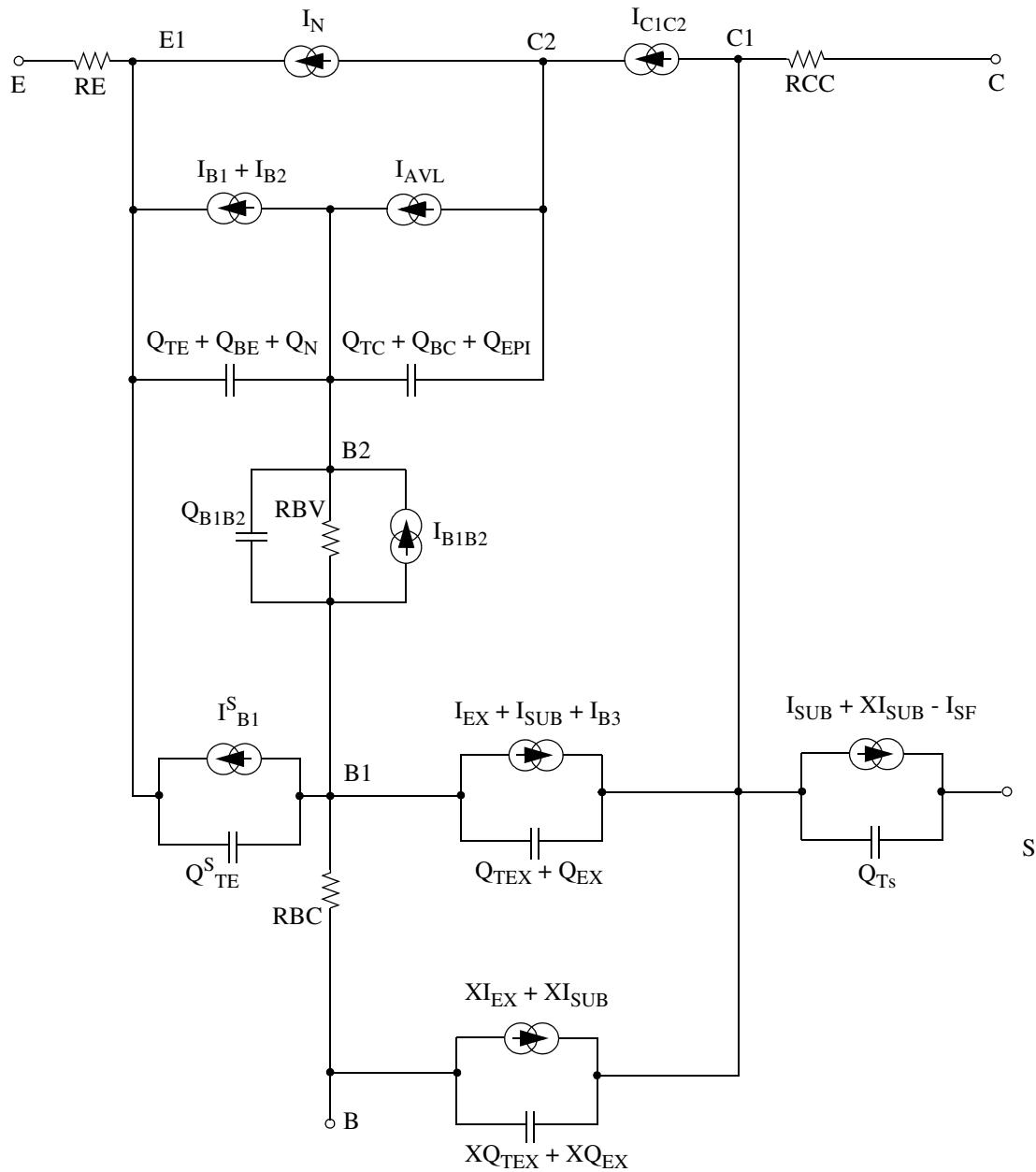


Figure 3-1. Equivalent circuit for the vertical NPN transistor

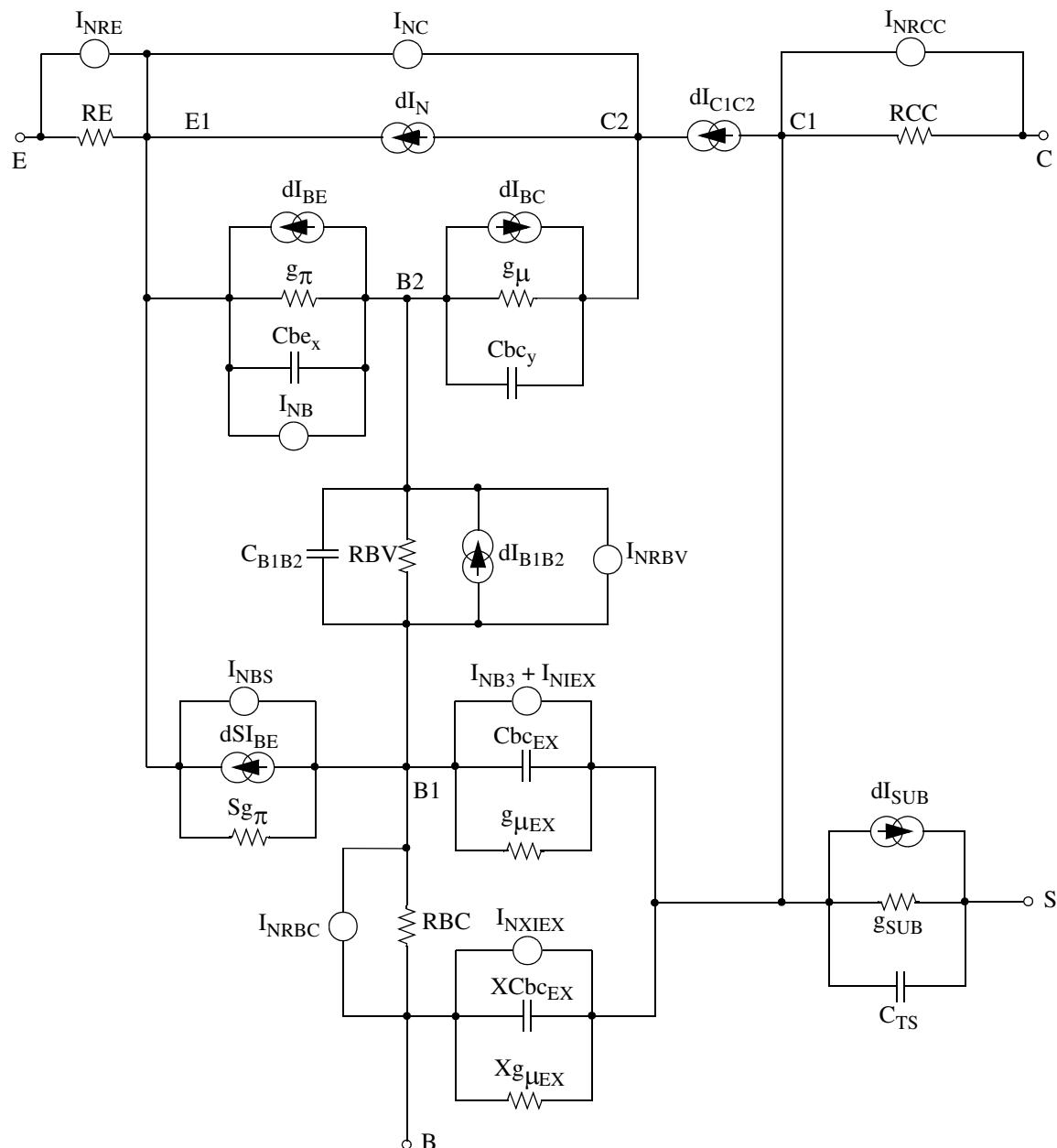


Figure 3-2. Small signal equivalent circuit for the vertical NPN transistor for AC and Noise Analyses

$$\begin{aligned}
dI_n &= g_x \cdot dVB_2E_1 + g_y \cdot dVB_2C_2 + g_z \cdot dVB_2C_1 \\
dIC_1C_2 &= grcv_x \cdot dVB_2E_1 + grcv_y \cdot dVB_2C_2 + grcv_z \cdot dVB_2C_1 \\
dI_{BE} &= j\omega \cdot (Cbe_y \cdot dVB_2C_2 + Cbe_z \cdot dVB_2C_1) \\
dI_{BC} &= g_{\mu x} \cdot dVB_2E_1 + g_{\mu z} \cdot dVB_2C_1 + j\omega \cdot (Cbc_x \cdot dVB_2E_1 + Cbc_z \cdot dVB_2C_1) \\
dIB_1B_2 &= grbv_x \cdot dVB_2E_1 + grbv_y \cdot dVB_2C_2 + grbv_z \cdot dVB_2C_1 + j\omega \cdot CB_1B_{2x} \cdot dVB_2E_1 \\
dSI_{BE} &= j\omega \cdot SC_{TE} \cdot dVB_2E_1 \\
dI_{SUB} &= g_{PNP} \cdot dVB_1C_1 + Xg_{PNP} \cdot dVBC_1
\end{aligned}$$

4.0 Model Constants

$$V_{lim} = 8.0 \cdot 10^6 \text{ cm/sec} \quad K = 0.01 \quad CK = 0.1$$

Constants **A** and **B** for impact ionization are dependent on transistor type.

For NPN: $A_n = 7.03 \cdot 10^5 \text{ cm}^{-1}$ and $B_n = 1.23 \cdot 10^6 \text{ V} \cdot \text{cm}^{-1}$

5.0 Temperature Effects

The actual simulation temperature is denoted by **TEMP** (in °C). The temperature at which the parameters are determined is **TREF** (in °C).

5.1 Conversions to Kelvin

$$\begin{aligned}
T &= TEMP + DTA + 273.15 & T_{nom} &= TREF + 273.15 \\
T_N &= \frac{T}{T_{nom}} & \delta T &= T - T_{nom}
\end{aligned}$$

5.2 Thermal voltage

$$V_t = \frac{k_B}{q} \cdot T \quad V_I = \frac{1}{V_t(T_{nom})} - \frac{1}{V_t}$$

5.3 Resistances

$$\begin{aligned} RBC_T &= RBC \cdot T_N^{AEX} & RBV_T &= RBV \cdot T_N^{AB} \\ RCC_T &= RCC \cdot T_N^{AC} & RCV_T &= RCV \cdot T_N^{AEPI} \end{aligned}$$

5.4 Depletion capacitance

The junction diffusion voltages VDE , VDC , and VDS with respect to the temperature are:

$$\begin{aligned} VDE_T &= -3 \cdot Vt \cdot \ln(T_N) + VDE \cdot T_N + (1 - T_N) \cdot VGB \\ VDC_T &= -3 \cdot Vt \cdot \ln(T_N) + VDC \cdot T_N + (1 - T_N) \cdot VGC \\ VDS_T &= -3 \cdot Vt \cdot \ln(T_N) + VDS \cdot T_N + (1 - T_N) \cdot VGS \end{aligned}$$

The temperature scaling rule for the zero depletion capacitances CJE and CJS are:

$$CJE_T = CJE \cdot \left(\frac{VDE}{VDE_T} \right)^{PE} \quad CJS_T = CJS \cdot \left(\frac{VDS}{VDS_T} \right)^{PS}$$

The collector depletion capacitance is divided into a variable and a constant part. The constant part is temperature independent.

$$CJC_T = CJC \cdot \left((1 - XP) \cdot \left(\frac{VDC}{VDC_T} \right)^{PC} + XP \right) \quad XP_T = XP \cdot \frac{CJC}{CJC_T}$$

5.5 Base charge

$$QE_T = (1 - XCJE) \cdot \frac{CJE_T \cdot VDE_T}{1 - PE}$$

$$QB0_T = g_{iT} \cdot Q_{imp} - QE_T - XCJC \cdot CJC_T \cdot VDC_T \cdot \left(\frac{1 - XP_T}{1 - PC} + XP_T \right)$$

with:

$$g_{iT} = \frac{-R_T + \sqrt{R_T^2 + 8 \cdot R_T}}{4} \quad (\text{for } R_T \rightarrow \infty : g_i = 1)$$

$$R_T = (T)^{1.5} \cdot \frac{4.82 \cdot 10^{15}}{NA} \cdot \exp\left(-\frac{VI}{Vt}\right)$$

$$Q_{imp} = \frac{1}{g_i} \cdot \left(QB0 + QE + XCJC \cdot CJC \cdot VDC \cdot \left(\frac{1 - XP}{1 - PC} + XP \right) \right)$$

$$QE = (1 - XCJE) \cdot \frac{CJE \cdot VDE}{1 - PE}$$

$$g_i = \frac{-R + \sqrt{R^2 + 8 \cdot R}}{4} \quad (\text{for } R \rightarrow \infty : g_i = 1)$$

$$R = (T_{nom})^{1.5} \cdot \frac{4.82 \cdot 10^{15}}{NA} \cdot \exp\left(-\frac{VI}{Vt(T_{nom})}\right)$$

Q_{imp} has to be calculated with all parameters values at the reference temperature.

5.6 Current gain

$$BF_T = BF \cdot T_N^{(3 \cdot 10^{-2} - 1.5 \cdot AB)} \cdot \exp((VGB - VGE) \cdot V_I)$$

The parameter **BRI** is assumed to be temperature independent.

5.7 Currents and voltages

$$IS_T = IS \cdot T_N^{(3.8 - 1.5 \cdot AB)} \cdot \exp(VGB \cdot V_I)$$

$$IBF_T = IBF \cdot T_N^2 \cdot \exp\left(\frac{VGJ}{2} \cdot V_I\right)$$

$$VLF_T = VLF - ER \cdot \delta T$$

$$IK_T = IK \cdot T_N^{(1 - AB)}$$

$$IBR_T = IBR \cdot T_N^2 \cdot \exp\left(\frac{VGC}{2} \cdot V_I\right)$$

$$VLR_T = VLR - ER \cdot \delta T$$

The temperature dependence of ***ISS*** and ***IKS*** is given by ***AS*** and ***VGS***. ***AS*** equals ***AC*** for a closed buried layer (***BN***) and ***AS*** equals ***AEPI*** for an open buried layer.

$$ISS_T = ISS \cdot T_N^{(3.5 + AS)} \cdot \exp(VGS \cdot V_I)$$

$$IKS_T = IKS \cdot T_N^{(1 - AS)}$$

5.8 Transit times

$$MTAU_T = \frac{MTAU}{MTAU - T_N \cdot (MTAU - 1)}$$

$$TAUNE_T = TAUNE \cdot T_N^{(1 + AB)} \cdot \left(\frac{\frac{T_{nom}}{\left(\frac{1}{MTAU}\right)}}{T} \right)^3$$

$$\cdot \exp\left(VGJ \cdot V_I + \frac{VGB}{MTAU_T \cdot Vt} - \frac{VGB}{MTAU \cdot Vt(T_{nom})}\right)$$

5.9 Avalanche parameter

$$\Delta T_1 = TREF - 25 \quad \Delta T_2 = TEMP + DTA - 25$$

$$AVL_T = AVL \cdot \frac{1 + 7.2 \cdot 10^{-4} \cdot \Delta T_2 - 1.6 \cdot 10^{-6} \cdot (\Delta T_2)^2}{1 + 7.2 \cdot 10^{-4} \cdot \Delta T_1 - 1.6 \cdot 10^{-6} \cdot (\Delta T_1)^2} \cdot \frac{CJC}{CJC_T}$$

6.0 Parameter Dependent Constants

$$ah0 = 2 \cdot \left(\frac{1 - \exp(-ETA)}{ETA} \right) \quad ahb = ah0 \quad alb = \exp(-ETA)$$

$$bh0 = \frac{1}{ah0} \quad bhb = bh0$$

$$bl0 = \frac{ETA - (1 - alb)}{(1 - alb)^2} \quad blb = \frac{1 - (ETA + 1) \cdot alb}{(1 - alb)^2}$$

7.0 Static Current Equations

7.1 Ideal forward and reverse current

$$I_F = IS_T \cdot \exp\left(\frac{V_{B2E1}}{Vt}\right) \quad I_R = IS_T \cdot \exp\left(\frac{V_{B2C2}}{Vt}\right)$$

7.2 The main current I_N

The Moll-Ross formulation is used to take into account high injection in the base. To avoid dividing by zero, the depletion charge term is modified.

$$q_0 = 1 + \frac{Q_{TE} + Q_{TC}}{QB0_T} \quad q_1 = \frac{q_0 + \sqrt{q_0^2 + K}}{2}$$

$$q_2 = \frac{Q_{BE} + Q_{BC}}{QB0_T} \quad I_N = \frac{I_F - I_R}{q_1 + q_2}$$

7.3 Forward base currents

The total ideal base current is separated into bulk and sidewall components. The bulk component depends on voltage V_{B2E1} and the sidewall component on voltage V_{B1E1} . The separation is given by the parameter $XIBI$.

Bulk component: $I_{B1} = (1 - XIBI) \cdot \frac{IS_T}{BF_T} \cdot \left(\exp\left(\frac{V_{B2E1}}{Vt}\right) - 1 \right)$

Sidewall component: $I_{B1}^S = XIBI \cdot \frac{IS_T}{BF_T} \cdot \left(\exp\left(\frac{V_{B1E1}}{Vt}\right) - 1 \right)$

The non-ideal forward base current, I_{B2} is given by:

$$I_{B2} = IBF_T \cdot \left(\frac{\exp\left(\frac{V_{B2E1}}{Vt}\right) - 1}{\exp\left(\frac{V_{B2E1}}{2 \cdot Vt}\right) + \exp\left(\frac{VLF_T}{2 \cdot Vt}\right)} \right) + G_{MIN} \cdot V_{B2E1}$$

7.4 Reverse base currents

The non-ideal reverse base current, I_{B3} is given by:

$$I_{B3} = IBR_T \cdot \left(\frac{\exp\left(\frac{V_{B1C1}}{Vt}\right) - 1}{\exp\left(\frac{V_{B1C1}}{2 \cdot Vt}\right) + \exp\left(\frac{VLR_T}{2 \cdot Vt}\right)} \right) + G_{MIN} \cdot V_{B1C1}$$

The substrate current (holes injected from base to substrate), I_{SUB} , including high injection is given by:

$$I_{SUB} = \frac{2 \cdot ISS_T \cdot \left(\exp\left(\frac{V_{B1C1}}{Vt}\right) - 1 \right)}{1 + \sqrt{1 + 4 \cdot \frac{IS_T}{IKS_T} \cdot \left(\exp\left(\frac{V_{B1C1}}{Vt}\right) - 1 \right)}}$$



The ideal collector-substrate current, I_{SF} is given by:

Note $I_{SF} = ISS_T \cdot \left(\exp\left(\frac{V_{SC1}}{Vt}\right) - 1 \right)$

The extrinsic base current (electrons injected from collector to extrinsic base), I_{EX} is given by:

$$g_1 = \frac{4 \cdot IS_T \cdot (aho)^2}{IK_T \cdot (alb)^2} \cdot \exp\left(\frac{V_{B1C1}}{Vt}\right) \quad n_{BEX} = alb \cdot \frac{g_1}{2 \cdot (1 + \sqrt{1 + g_1})}$$

$$g_{BEX} = \frac{1}{BRI} \quad I_{EX} = g_{EX} \cdot \left(\frac{alb + n_{BEX}}{ahb + n_{BEX}} \cdot \frac{IK_T}{ahb} \cdot n_{BEX} - IS_T \right)$$

7.5 Weak avalanche current

If $I_N \leq 0$ or $I_{CAP} \leq 0$ then $I_{AVL} = 0$

The current I_{CAP} is defined in “Intrinsic collector depletion charge QTC₁” on page 3-16.

At a low current level the internal junction voltage is:

$$V_J = -V_{B2C1} - I_{CAP} \cdot RCV_T$$

If $V_J > -0.9 \cdot VDC_T$ then:

$$WD_{EPI} = \frac{AVL_T}{B_n \cdot XP_T}$$

$$F_C^{-1} = (1 - XP_T) \cdot \frac{\left(1 - \frac{I_{CAP}}{IHC}\right)^{MC}}{\left(1 + \frac{V_J}{VDC_T}\right)^{PC}} + XP_T$$

$$W_D = F_C \cdot \frac{AVL_T}{B_n}$$

$$dEW = F_C \cdot VDC_T \cdot \frac{B_n}{AVL_T}$$

$$E_0 = \frac{V_J + VDC_T}{W_D} + dEW \cdot \left(1 - \frac{I_{CAP}}{IHC}\right) + \frac{I_{CAP} \cdot RCV_T}{WD_{EPI}}$$

$$E_1 = \frac{V_J + VDC_T}{W_D} + \frac{I_{CAP} \cdot RCV_T}{WD_{EPI}}$$

If $EXAVL = 0$ then $EM = E0$

The generation of avalanche current increases at high current levels. This is taken into account when flag $EXVAL = 1$.

If $EXVAL = 1$ then:

$$\frac{X_I}{W_{EPI}} = \frac{E_C}{I_{C1C2} \cdot RCV_T} \quad SH_W = 1 + 2 \cdot SFH \cdot \left(1 + 2 \cdot \frac{X_I}{W_{EPI}}\right)$$

$$E_2 = \frac{-V_{B2C1} + VDC_T}{W_D \cdot \left(1 - \frac{X_I}{2 \cdot W_{EPI}}\right)^2} - dEW \cdot \left(1 - \frac{X_I}{W_{EPI}}\right) \cdot \left(EFI - \frac{I_N}{IHC \cdot SH_W}\right)$$

$$E_M = E_0 + \frac{E_2 - E_0 + \sqrt{(E_2 - E_0)^2 + CK \cdot \frac{I_{CAP}}{IHC} \cdot E_1^2}}{2}$$

E_C and I_{C1C2} are determined by the equations shown later in this chapter.

The intersection point, X_D , and the avalanche current becomes:

$$X_D = \frac{E_M \cdot W_D}{2 \cdot (E_M - E_1)}$$

$$G_{EM} = \frac{A_n}{B_n} \cdot E_M \cdot X_D \cdot \left(\exp\left(\frac{-B_n}{E_M}\right) - \exp\left(\frac{-B_n}{E_M} \cdot \left(1 + \frac{W_D}{X_D}\right)\right) \right)$$

$$G_{MAX} = \frac{V_T}{I_N \cdot (RBC_T + RB2)} + \frac{q_1 + q_2}{BF_T} + \frac{RE}{RBC_T + RB2}$$

$$I_{AVL} = I_N \cdot \frac{G_{EM} \cdot G_{MAX}}{G_{EM} \cdot (1 + G_{MAX}) + G_{MAX}}$$

If $V_J \leq -0.9 \cdot VDC_T$ then $I_{AVL} = 0$.

7.6 Series resistances

emitter: RE = constant

collector: RCC = constant

base: RBC = constant

7.7 Variable base resistance

The variable part of the base resistance is modulated by the base charges and takes into account the base current crowding:

$$RB2 = \frac{3 \cdot RBV_T}{q_1 + q_2} \quad I_{B1B2} = \frac{2 \cdot Vt}{RB2} \cdot \left(\exp\left(\frac{V_{B1B2}}{Vt}\right) - 1 \right) + \frac{V_{B1B2}}{RB2}$$

The base charge terms q_1 and q_2 are as defined earlier in this chapter.

7.8 Variable collector resistance

This model of the epilayer resistance takes into account:

- The decrease in resistance due to the carriers injected from the base if only the internal base-collector junction is forward biased (quasi-saturation) and if both the internal and external base-collector junctions are forward biased (reverse mode of operation)
- Ohmic current flow at low level densities
- Space charge limited current flow at high current densities
- Current spreading in the epilayer

The epilayer current is computed by solving a cubic equation.

If $V_{B2C2} - V_{B2C1} > 0$ (forward mode) then:

$$S_F = \frac{2 \cdot SFH}{1 + SFH} \quad V = \frac{V_{B2C2} - V_{B2C1}}{IHC \cdot RCV_T}$$

$$E = \frac{E_C}{IHC \cdot RCV_T} \quad R = \frac{RCV_T}{SCRCV}$$

$$A_2 = -2 \cdot E - \frac{V + R \cdot V^2 + E}{1 + V}$$

$$A_1 = \frac{E^2 \cdot (3 + V) + 2 \cdot E \cdot V - S_F \cdot E \cdot R \cdot V^2}{1 + V}$$

$$A_0 = -\frac{E^2 \cdot (E + V)}{1 + V}$$

$$q = \frac{A_1}{3} - \frac{A_2^2}{9} \quad r = \frac{A_1 \cdot A_2 - 3 \cdot A_0}{6} - \frac{A_2^3}{27}$$

$$s = \sqrt[3]{q^3 + r^2} \quad s_1 = (r + s)^{1/3} \quad s_2 = (r - s)^{1/3}$$

The argument of the square root of the equation for s above may become negative. Then s , s_1 and s_2 are complex. In such cases, the magnitudes of the imaginary parts of s_1 and s_2 are equal but differ in sign.

$$\text{Finally: } I_{C1C2} = IHC \cdot \left(s_1 + s_2 - \frac{A_2}{3} \right)$$

If $V_{B2C2} - V_{B2C1} \leq 0$ (reverse mode) then:

$$I_{C1C2} = \frac{E_C + V_{B2C2} - V_{B2C1}}{RCV_T}$$

$$E_C = V_T \cdot \left(K_0 - K_W - \ln \left(\frac{K_0 + 1}{K_W + 1} \right) \right)$$

$$K_0 = \sqrt{1 + 4 \cdot \exp((V_{B2C2} - VDC_T)/Vt)}$$

$$K_W = \sqrt{1 + 4 \cdot \exp((V_{B2C1} - VDC_T)/Vt)}$$

8.0 Charge Equations

8.1 Emitter depletion charge Q_{TE}

The total base-emitter depletion charge depends on V_{B2E1} :

$$Q_{TE}^{tot} = \frac{CJE_T \cdot VDE_T \cdot (1 + K)}{1 - PE + K} \cdot \left(1 - \frac{(1 + K)^{\left(\frac{PE}{2}\right)} \cdot \left(1 - \frac{V_{B2E1}}{VDE_T} \right)}{\left(\left(1 - \frac{V_{B2E1}}{VDE_T} \right)^2 + K \right)^{\left(\frac{PE}{2}\right)}} \right)$$

The total base-emitter depletion capacitance is separated into bulk and sidewall components.

$$Q_{TE} = (1 - XCJE) \cdot Q_{TE}^{tot} \quad Q_{TE}^S = XCJE \cdot Q_{TE}^{tot}$$

8.2 Intrinsic collector depletion charge Q_{TC_1}

The base-collector depletion charge is divided into a constant (parameter XP) and a variable part. The constant part represents the finite thickness of the epilayer. The depletion charge is a function of the internal and external base-collector junction voltage.

If $V_{B2C2} - V_{B2C1} > 0$ then:

$$I_{CAP} = \frac{IHC \cdot (V_{B2C2} - V_{B2C1})}{V_{B2C2} - V_{B2C1} + IHC \cdot RCV_T} \quad CKI = CK + \frac{I_{CAP}}{IHC}$$

If $V_{B2C2} - V_{B2C1} \leq 0$ then: $I_{CAP} = \frac{V_{B2C2} - V_{B2C1}}{RCV_T} \quad CKI = CK$

$$VC_1 = \frac{(1 + CK)^{\left(\frac{PC}{2}\right)} \cdot \left(1 - \frac{V_{B2C2}}{VDC_T}\right)}{\left(\left(1 - \frac{V_{B2C2}}{VDC_T}\right)^2 + CKI\right)^{\left(\frac{PC}{2}\right)}} \cdot \left(1 - \frac{I_{CAP}}{IHC}\right)^{MC}$$

$$VC_V = \frac{VDC_T \cdot (1 - XP_T) \cdot (1 + CK)}{1 - PC + CK} \cdot (1 - VC_1)$$

Finally: $Q_{TC_1} = XCJC \cdot CJC_T \cdot (VC_V - XP_T \cdot (I_{CAP} \cdot RCV_T - V_{B2C2}))$

8.3 Collector transit time in quasi-saturation ΔQ_{SAT}

The current through the epilayer without injection ($E_C = 0$) is:

$$V_{C1C2} = V_{B2C2} - V_{B2C1}$$

$$I_{(EC=0)} = \frac{IHC \cdot SCRVC \cdot V_{C1C2} + V_{C1C2}^2}{SCRVC \cdot (IHC \cdot RCV_T + V_{C1C2})}$$

To force the same current I_{C1C2} through the epilayer without injection, we need an epilayer voltage of $V_{(EC = 0)}$:

$$B_1 = 0.5 \cdot SCRCV \cdot (I_{C1C2} - IHC)$$

$$B_2 = SCRCV \cdot IHC \cdot RCV_T \cdot I_{C1C2}$$

$$V_{(EC = 0)} = B_1 + \sqrt{B_1 \cdot B_1 + B_2}$$

The differential resistance $R_{(EC = 0)} = (\partial V_{(EC = 0)}) / (\partial I_{C1C2})$ is given by:

$$R_{(EC = 0)} = \frac{SCRCV \cdot (V_{(EC = 0)} + IHC \cdot RCV_T)^2}{V_{(EC = 0)}^2 + 2 \cdot V_{(EC = 0)} \cdot IHC \cdot RCV_T + SCRCV \cdot IHC^2 \cdot RCV_T}$$

The collector transit time in quasi-saturation now becomes:

$$\Delta Q_{SAT} = R_{(EC = 0)} \cdot \frac{\partial Q_{TC1}}{\partial V_{B2C2}} \cdot (I_{C1C2} - I_{(EC = 0)})$$

The total collector depletion and transit time charge is:

if $I_{C1C2} > 0$ then $Q_{TC} = Q_{TC1} + \Delta Q_{SAT}$

if $I_{C1C2} \leq 0$ then $Q_{TC} = Q_{TC1}$

8.4 Extrinsic collector depletion charges Q_{TEX} and XQ_{TEX}

The extrinsic collector depletion charge is partitioned between the nodes $B1$ and CI and nodes B and CI respectively independent of flag $EXMOD$.

$$\begin{aligned}
VTEX_1 &= \frac{(1 + CK)^{\left(\frac{PC}{2}\right)} \cdot \left(1 - \frac{V_{B1C1}}{VDC_T}\right)}{\left(\left(1 - \frac{V_{B1C1}}{VDC_T}\right)^2 + CK\right)^{\left(\frac{PC}{2}\right)}} \\
VTEX_V &= \frac{VDC_T \cdot (1 - XP_T) \cdot (1 + CK)}{1 - PC + CK} \cdot (1 - VTEX_1) \\
Q_{TEX} &= (1 - XEXT) \cdot (1 - XCJC) \cdot CJC_T \cdot (VTEX_V + XP_T \cdot V_{B1C1}) \\
XVTEX_1 &= \frac{(1 + CK)^{\left(\frac{PC}{2}\right)} \cdot \left(1 - \frac{V_{BC1}}{VDC_T}\right)}{\left(\left(1 - \frac{V_{BC1}}{VDC_T}\right)^2 + CK\right)^{\left(\frac{PC}{2}\right)}} \\
XVTEX_V &= \frac{VDC_T \cdot (1 - XP_T) \cdot (1 + CK)}{1 - PC + CK} \cdot (1 - XVTEX_1) \\
XQ_{TEX} &= XEXT \cdot (1 - XCJC) \cdot CJC_T \cdot (XVTEX_V + XP_T \cdot V_{BC1})
\end{aligned}$$

8.5 Depletion charge Q_{TS}

$$Q_{TS} = \frac{CJS_T \cdot VDS_T \cdot (1 + K)}{1 - PS + K} \cdot \left(1 - \frac{(1 + K)^{\left(\frac{PS}{2}\right)} \cdot \left(1 - \frac{V_{SC1}}{VDS_T}\right)}{\left(\left(1 - \frac{V_{SC1}}{VDS_T}\right)^2 + K\right)^{\left(\frac{PS}{2}\right)}} \right)$$

8.6 Stored base charges Q_{BE} and Q_{BC}

$$Q_B = q_1 \cdot Q_{B0_T} \quad f_1 = \frac{4 \cdot IS_T \cdot (ah0)^2}{IK_T} \cdot \exp\left(\frac{V_{B2E1}}{Vt}\right)$$

$$n_0 = \frac{f_1}{2 \cdot (1 + \sqrt{1 + f_1})}$$

$$Q_{BE} = Q_B \cdot n_0 \cdot \left(\frac{\frac{1}{2} + \left(\frac{ah0}{4} \right) + n_0}{\left(\frac{1}{2} + \frac{ah0}{4} \right) \cdot \frac{bh0}{bl0} + n_0} \right) \cdot bh0$$

$$f_2 = \frac{4 \cdot IS_T \cdot (ah0)^2}{IK_T \cdot (alb)^2} \cdot \exp\left(\frac{V_{B2C2}}{Vt}\right)$$

$$n_B = alb \cdot \frac{f_2}{2 \cdot (1 + \sqrt{1 + f_2})} \quad Q_{BC} = Q_B \cdot n_B \cdot \left(\frac{alb \cdot blb + n_B}{alb \cdot bhb + n_B} \right) \cdot bhb$$

8.7 Neutral and emitter charge

$$Q_{N0} = TAUNE_T \cdot IK_T \cdot \left(\frac{IS_T}{IK_T} \right)^{\left(\frac{1}{MTAU_T} \right)} \cdot \sqrt{MTAU_T \cdot (2 - MTAU_T)}$$

$$\cdot \left(\left(\frac{MTAU_T - 1}{2 \cdot (2 - MTAU_T)} \right)^{\left(1 - \frac{1}{MTAU_T} \right)} \right)$$

$$Q_N = Q_{N0} \cdot \left(\exp\left(\frac{V_{B2E1}}{Vt \cdot MTAU_T}\right) - 1 \right)$$

8.8 Stored epilayer charge

If $|V_{B2C1} - V_{B2C2}| > 1 \cdot 10^{-8}$ then:

$$Q_{EPI} = \frac{IS_T \cdot QB0_T}{I_{C1C2}} \cdot \left(\exp\left(\frac{V_{B2C2}}{Vt}\right) - \exp\left(\frac{V_{B2C1}}{Vt}\right) \right)$$

If $|V_{B2C1} - V_{B2C2}| \leq 1 \cdot 10^{-8}$ then:

$$Q_{EPI} = RCV_T \cdot IS_T \cdot QB0_T \cdot \exp\left(\frac{VDC_T}{Vt}\right) \cdot \frac{p_0 + p_w}{2 \cdot Vt}$$

where:

$$p_0 = \frac{2}{1 + K_0} \cdot \exp\left(\frac{V_{B2C2} - VDC_T}{Vt}\right) \quad p_w = \frac{2}{1 + K_W} \cdot \exp\left(\frac{V_{B2C1} - VDC_T}{Vt}\right)$$

9.0 Extrinsic Charges

$$g_2 = 4 \cdot \exp\left(\frac{V_{B1C1} - VDC_T}{V_T}\right) \quad p_{WEX} = \frac{g_2}{2 \cdot (1 + \sqrt{1 + g_2})}$$

$$g_3 = \frac{RCV_T \cdot IS_T}{V_T} \cdot \exp\left(\frac{VDC_T}{V_T}\right) \quad g_4 = \frac{alb \cdot blb + n_{BEX}}{alb \cdot bhb + n_{BEX}} \cdot bhb$$

$$Q_{EX} = QB0_T \cdot \left(\frac{1 - XCJC}{XCJC} \right) \cdot (g_3 \cdot p_{WEX} + g_4 \cdot n_{BEX})$$

10.0 Extended Modeling of the Reverse Current Gain $EXMOD=1$

10.1 Currents

The base currents I_{EX} and I_{SUB} are redefined:

$$I_{EX} = (1 - XEXT) \cdot I_{EX} \quad I_{SUB} = (1 - XEXT) \cdot I_{SUB}$$

A part $XEXT$ of the base current of the extrinsic transistor is connected to the base terminal:

$$XIM_{SUB} = XEXT \cdot \frac{2 \cdot ISS_T \cdot \left(\exp\left(\frac{V_{BC1}}{Vt}\right) - 1 \right)}{1 + \sqrt{1 + 4 \cdot \frac{IS_T}{IKS_T} \cdot \left(\exp\left(\frac{V_{BC1}}{Vt}\right) - 1 \right)}}$$

$$Xg_1 = \frac{4 \cdot IS_T \cdot (aho)^2}{IK_T \cdot (alb)^2} \cdot \exp\left(\frac{V_{BC1}}{Vt}\right) \quad Xn_{BEX} = alb \cdot \frac{Xg_1}{2 \cdot (1 + \sqrt{1 + Xg_1})}$$

$$XIM_{EX} = XEXT \cdot g_{EX} \cdot \left(\frac{alb + Xn_{BEX}}{ahb + Xn_{BEX}} \cdot \frac{IK_T}{ahb} \cdot Xn_{BEX} - IS_T \right)$$

To improve convergency behavior, the conductivity of branch $b-c1$ is limited to $1/RCC_T$

$$V_{EX} = V_t \cdot \left(\ln\left(\frac{V_t}{XEXT \cdot (IS_T \cdot g_{EX} + ISS_T) \cdot RCC_T}\right) + 2 \right)$$

$$VB_{EX} = \frac{-(V_{EX} - V_{BC1}) + \sqrt{(V_{EX} - V_{BC1})^2 + K}}{2}$$

$$F_{EX} = \frac{VB_{EX}}{RCC_T \cdot (XIM_{EX} + XIM_{SUB}) + VB_{EX}}$$

$$XI_{SUB} = F_{EX} \cdot XIM_{SUB} \quad XI_{EX} = F_{EX} \cdot XIM_{EX}$$

10.2 Charges

The charge Q_{EX} is redefined:

$$Q_{EX} = (1 - XEXT) \cdot Q_{EX} \quad Xg_2 = 4 \cdot \exp\left(\frac{V_{BC1} - VDC_T}{V_t}\right)$$

$$Xp_{WEX} = \frac{Xg_2}{2 \cdot (1 + \sqrt{1 + Xg_2})} \quad Xg_4 = \frac{alb \cdot blb + Xn_{BEX}}{alb \cdot bhb + Xn_{BEX}} \cdot bhb$$

$$XQ_{EX} = F_{EX} \cdot XEXT \cdot QB0_T \cdot \frac{1 - XCJC}{XCJC} \cdot (g_3 \cdot Xp_{WEX} + Xg_4 \cdot Xn_{BEX})$$



The depletion charges $QTEX$ and $XQTEX$ are distributed always over the internal and external base node independent of $EXMOD$.

11.0 Distributed High Frequency Effects in the Intrinsic Base

Distributed high frequency effects are modeled, in first order approximation, both in the lateral direction (current crowding) and in the vertical direction (excess phase-shift). The distributed effects are an optional part of the Mextram model and can be switched on and off by the flag ***EXPHI***. On: ***EXPHI*** = 1, and off: ***EXPHI*** = 0.

The high frequency current crowding is modeled by:

$$C_B = \frac{1}{5} \cdot \left(\frac{\partial Q_{TE}}{\partial V_{B2E1}} + \frac{\partial Q_{BE}}{\partial V_{B2E1}} + \frac{\partial Q_N}{\partial V_{B2E1}} \right) \quad Q_{B1B2} = C_B \cdot V_{B1B2}$$

For reasons of simplicity, only the forward depletion and diffusion charges are taken into account. The partial derivative of Q_{B1B2} with respect to V_{B2E1} has to be neglected in AC analysis. In transient analysis the convergency behavior may be improved by approximating this derivative with:

$$\frac{\partial Q_{B1B2}}{\partial V_{B2E1}} = \left(\frac{\partial Q_{BE}}{\partial V_{B2E1}} + \frac{\partial Q_N}{\partial V_{B2E1}} \right) \cdot \left(\frac{V_{B1B2}}{5 \cdot V_T} \right)$$

In the vertical direction (excess phase-shift) base-charge-partitioning is used. For simplicity, it is only implemented for the forward base charge, (Q_{BE}) and for low level injection. Accordingly, Q_{BE} and Q_{BC} are redefined as:

$$Q_{BE'} = (1 - q_C) \cdot Q_{BE} \quad Q_{BC'} = q_C \cdot Q_{BE} + Q_{BC}$$

$$q_C = \frac{2 + ETA - (2 - ETA) \cdot \exp(ETA)}{2 - ETA - (1 - ETA) \cdot \exp(ETA) - \exp(-ETA)}$$

For $ETA = 0$ the partitioning factor q_c is 1/3.

12.0 Noise Model

For noise analysis, noise current sources are added to the small signal equivalent circuit.

12.1 Thermal noise

$$\overline{IN_{RE}}^2 = \frac{4 \cdot k_B \cdot T}{RE} \cdot \Delta f$$

$$\overline{IN_{RBC}}^2 = \frac{4 \cdot k_B \cdot T}{RBC_T} \cdot \Delta f$$

$$\overline{IN_{RCC}}^2 = \frac{4 \cdot k_B \cdot T}{RCC_T} \cdot \Delta f$$

For the variable part of the base resistance a different formula is used, taking into account the effect of current crowding on noise behavior.

$$\overline{IN_{RBV}}^2 = \frac{5.26 \cdot k_B \cdot T}{RB2} \cdot \left(1 + 2 \cdot \exp\left(\frac{V_{B1B2}}{V_t}\right)\right)^{\left(\frac{3}{4}\right)} \cdot \Delta f$$

12.2 Collector current shot noise

$$\overline{IN_C}^2 = 2 \cdot q \cdot |I_N| \cdot \Delta f$$

12.3 Forward base current shot noise and 1/f noise

$$\begin{aligned} \overline{IN_B}^2 &= \left(2 \cdot q \cdot (|I_{B1}| + |I_{B2}|) + \right. \\ &\quad \left. \frac{AREA}{f} \cdot \left(KFN \cdot \left(\frac{|I_{B2}|}{AREA}\right)^2 + KF \cdot \left(\frac{|I_{B1}|}{AREA}\right)^{AF}\right)\right) \cdot \Delta f \end{aligned}$$

12.4 Emitter-base sidewall current shot noise and 1/f noise

$$\overline{IN_{BS}}^2 = \left(2 \cdot q \cdot |I_{B1}^S| + \frac{AREA}{f} \cdot KF \cdot \left(\frac{|I_{B1}^S|}{AREA}\right)^{AF}\right) \cdot \Delta f$$

12.5 Reverse base current shot noise and 1/f noise

$$\overline{IN_{B3}^2} = \left(2 \cdot q \cdot |I_{B3}| + \frac{AREA}{f} \cdot KF \cdot \left(\frac{|I_{B3}|}{AREA} \right)^{AF} \right) \cdot \Delta f$$

12.6 Extrinsic current shot noise and 1/f noise

$$\overline{IN_{EX}^2} = \left(2 \cdot q \cdot |I_{EX}| + \frac{KF}{f} \cdot \left(\frac{|I_{EX}|}{AREA} \right)^{AF} \cdot AREA \right) \cdot \Delta f$$

If **EXMOD** = 1 we also have:

$$\overline{IN_{XIE}^2} = \left(2 \cdot q \cdot |XI_{EX}| + \frac{KF}{f} \cdot \left(\frac{|XI_{EX}|}{AREA} \right)^{AF} \cdot AREA \right) \cdot \Delta f$$

13.0 Model Parameters

Nr.	Name	Description	Default	Units
1	AB	Temperature coefficient resistivity base	1.35	
2	AC	Temperature coefficient resistivity of the buried layer	0.4	
3	AEPI	Temperature coefficient resistivity of the epilayer	2.15	
4	AEX	Temperature coefficient resistivity of the extrinsic base	1	
5	AF	Flicker noise exponent	1	
6	AS	For closed buried layer: AS = AC otherwise AS = AEPI	2.15	
7	AVL	Weak avalanche parameter	50	
8	BF	Ideal forward current gain	140	
9	BRI	Ideal reverse current gain	16	
10	CJC	Zero-bias collector-base depletion capacitance	1.3×10^{-13}	F
11	CJE	Zero bias emitter-base depletion capacitance	2.5×10^{-13}	F
12	CJS	Zero bias collector-substrate depletion capacitance	1×10^{-12}	F
13	DTA	Difference of the device temperature to the ambient temperature	0	K
14	EFI	Electric field intercept (with EXAVL = 1)	0.7	
15	ER	Temperature coefficient of VLF and VLR	2×10^{-3}	
16	ETA	Factor of the built-in field of the base	4	

Nr.	Name	Description	Default	Units
17	EXAVL	Flag for modeling of avalanche currents	0	
18	EXMOD	Flag of the extended modeling of the reverse current gain	1	
19	EXPHI	Flag for the distributed high frequency effects in transient	0	
20	IBF	Saturation of the non-ideal forward base current	2×10^{-14}	A
21	IBR	Saturation current of the non-ideal reverse base current	8×10^{-15}	A
22	IHC	Critical current for hot carriers	3×10^{-3}	A
23	IK	High-Injection knee current	1.5×10^{-2}	A
24	IKS	Knee current of the substrate	5×10^{-6}	A
25	IS	Collector-emitter saturation current	5×10^{-17}	A
26	ISS	Base-substrate saturation current	6×10^{-16}	A
27	KF	Flicker noise coefficient ideal base current	2×10^{-16}	
28	KFN	Flicker noise coefficient non-ideal base current	2×10^{-16}	
29	MC	Collector current modulation coefficient	0.5	
30	MTAU	Non-ideality factor of the neutral and emitter charge	1.18	
31	NA	Maximum base dope concentration	3×10^{17}	cm^{-3}
32	PC	Collector-base grading coefficient variable part	0.4	
33	PE	Emitter-base grading coefficient	0.33	
34	PS	Collector-substrate grading coefficient	0.33	
35	QBO	Base charge at zero bias	1.2×10^{-12}	C
36	RBC	Constant part of the base resistance	50	Ω
37	RBV	Variable part of the base resistance at zero bias	100	Ω
38	RCC	Constant part of the collector resistance	25	Ω
39	RCV	Resistance of the un-modulated epilayer	750	Ω
40	RE	Emitter series resistance	2	Ω
41	SCRCV	Space charge resistance of the epilayer	1×10^3	Ω
42	SFH	Current spreading factor epilayer	0.6	
43	TAUNE	Minimum delay time of the neutral and emitter charge	3×10^{-10}	s
44	TREF	Reference temperature	27	$^{\circ}\text{C}$
45	VDC	Collector-base diffusion voltage	0.6	V
46	VDE	Emitter-base diffusion voltage	0.9	V
47	VDS	Collector-substrate diffusion voltage	0.5	V
48	VGB	Band-gap voltage of the base	1.18	V
49	VGC	Band-gap voltage of the collector	1.205	V
50	VGE	Band-gap voltage of the emitter	1.01	V
51	VGJ	Band-gap voltage recombination emitter-base junction	1.1	V

Nr.	Name	Description	Default	Units
52	VGS	Band-gap voltage for the substrate	1.15	V
53	VI	Ionization voltage base dope	4×10^{-2}	V
54	VLF	Cross-over voltage of the non-ideal forward base current	0.5	V
55	VLR	Cross-over voltage of the non-ideal reverse base current	0.5	V
56	XCJC	Fraction of the collector-base depletion capacitance under the emitter area	0.1	
57	XCJE	Fraction of the emitter-base depletion capacitance that belongs to the sidewall	0.5	
58	XEXT	Part of IEX , QEX , QTEX and ISUB that depends on the base-collector voltage VBC1	0.5	
59	XIBI	Fraction of ideal base current that belongs to the sidewall	0	
60	XP	Constant part of CJC	0.2	

**Note**

For the instance parameters, the device parameter **MULT** of the original Philips model is replaced by **AREA** in Eldo. This parameter may be used to put several transistors in parallel. The following parameters are multiplied by **AREA**:
IS, **IK**, **IBF**, **IBR**, **ISS**, **IKS**, **QB0**, **IHC**, **CJE**, **CJC**, **CJS**
The following parameters are divided by **AREA**:
RCC, **RCV**, **SCRCV**, **RBC**, **RBV**, **RE**

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Chapter 4

BJT Level 5 Equations

1.0 Overview

The improved Berkeley model is based on the Level 1 model (Gummel Poon). It includes several additional effects such as:

- Variable RC resistance due to velocity saturation.
- Quasi-saturation model based on a publication from G.M. Kull et al.
- Additional temperature effects.
- Variable exponent for high current roll off.

2.0 Definitions and Conventions

2.1 Current convention and displays

As for other devices, the convention for current flow in the pins of the BJT (C, B, E, S) is assumed to be positive when current is entering into the device. The pin-currents may be printed or plotted using $I(Qx.C)$ for the collector pin, $I(Qx.B)$ for the base pin, $I(Qx.E)$ for the emitter pin and $I(Qx.S)$ for the substrate pin.

2.2 Structure conventions

Because of the different possible transistor structures in IC device fabrication, the simulation of two different bipolar transistor structures is allowed as vertical and lateral structure. The model types defined by keywords NPN and PNP

automatically set a vertical structure while LPNP type sets the lateral structure for PNP device.

The connection points and orientation of the substrate diode and capacitance to the internal collector or internal base nodes depend on the chosen structure (respectively vertical or lateral).

2.3 NPN and PNP convention

All the following equations are valid for a NPN device. For an PNP device, all voltage and current signs have to be inverted to provide the correct equations.

2.4 Internal variables

- vbe defines the internal base-internal emitter voltage
- Vbc defines the internal base-internal collector voltage
- VcS defines the internal collector-to-substrate voltage (vertical only)
- vBS defines the external base-substrate voltage (lateral only)
- vbS defines the internal base-substrate voltage (lateral only)
- VBC defines the external base-internal collector voltage
- $Vbc1$ defines the internal base-internal collector 1 voltage
- $vc1C$ defines the external collector-internal collector 1 voltage

3.0 Equivalent Circuit Schematics

3.1 For DC and TRANSIENT analysis

Vertical structure

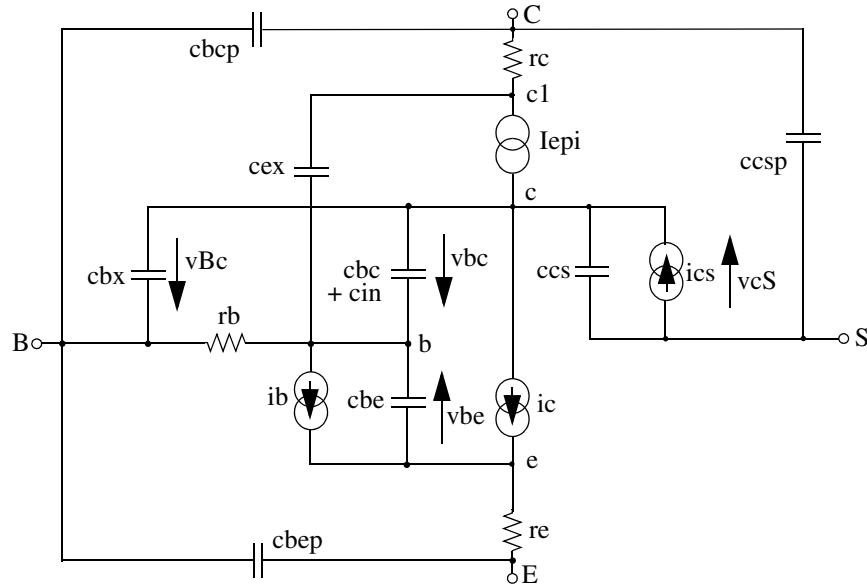


Figure 4-1. Equivalent circuit of vertical structure for DC and TRANSIENT analysis

Lateral structure

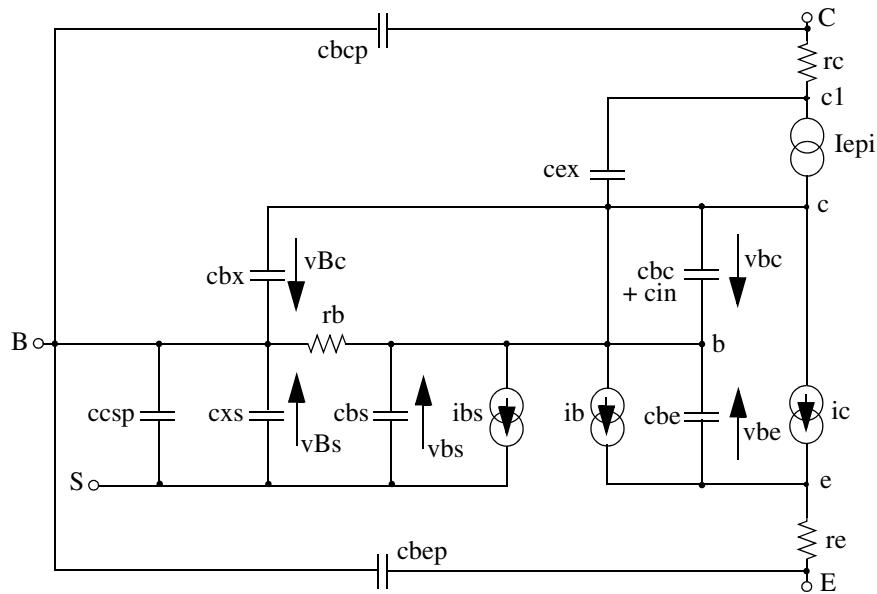


Figure 4-2. Equivalent circuit of lateral structure for DC and TRANSIENT analysis

3.2 For AC and NOISE analysis

Vertical structure

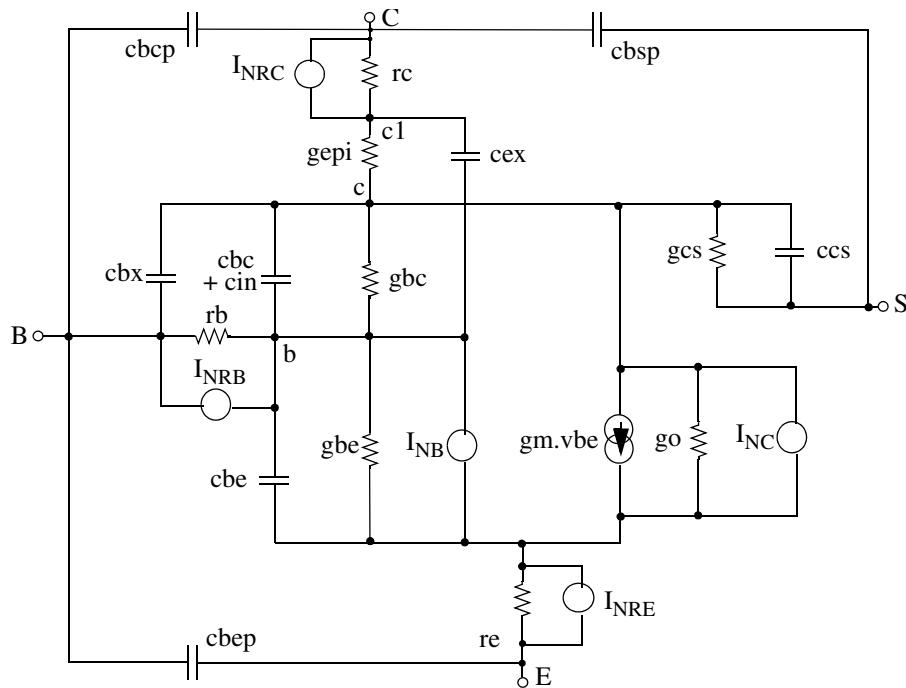


Figure 4-3. Equivalent circuit of vertical structure for AC & NOISE analysis

Lateral structure

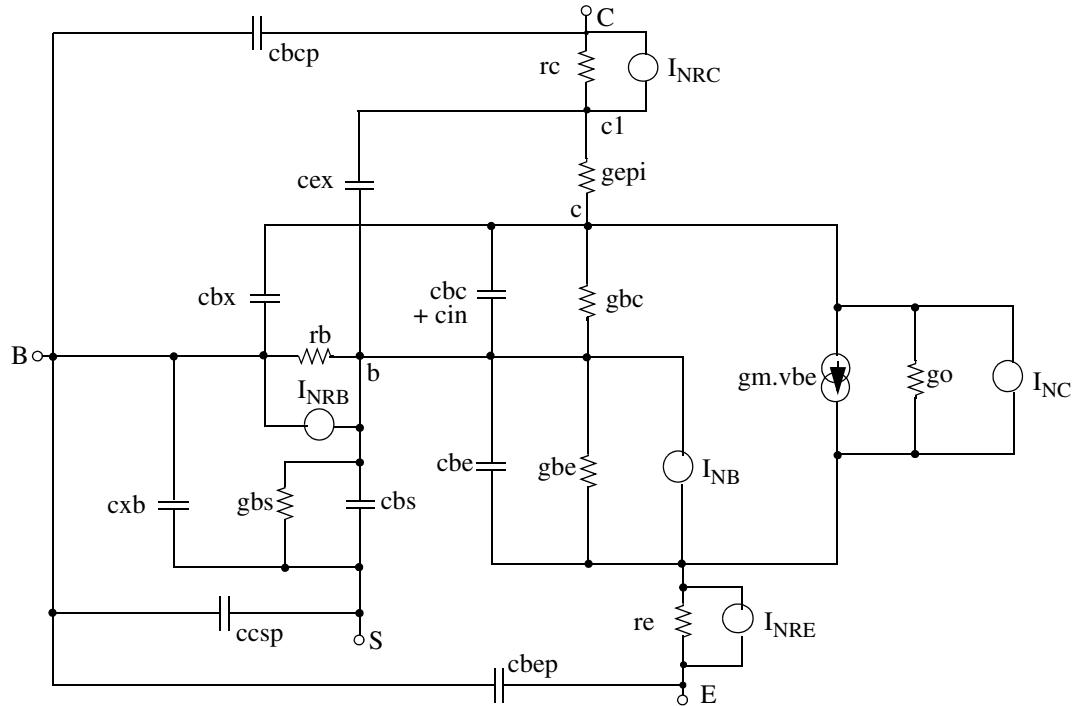


Figure 4-4. Equivalent circuit of lateral structure for AC & NOISE analysis

4.0 Scaling

If ***IBE*** and ***IBC*** are unspecified then ***AREAB*** and ***AREAC*** are not used and are set to the ***AREA*** value in all the equations.

If both ***IBE*** and ***IBC*** are specified then ***AREAB*** and ***AREAC*** are used as follows:

$$IBE_{eff} = IBE \cdot AREA \cdot M \quad IBC_{eff} = IBC \cdot AREAB \cdot M$$

Otherwise:

$$IBE_{eff} = IS \cdot AREA \cdot M \quad IBC_{eff} = IS \cdot AREA \cdot M$$

For a vertical structure device, the following relations apply:

$$\begin{aligned} ISE_{eff} &= ISE \cdot AREA \cdot M & CJE_{eff} &= CJE \cdot AREA \cdot M \\ ISC_{eff} &= ISC \cdot AREAB \cdot M & CJC_{eff} &= CJC \cdot AREAB \cdot M \\ ISS_{eff} &= ISS \cdot AREAC \cdot M & CJS_{eff} &= CJS \cdot AREAC \cdot M \end{aligned}$$

The Quasi-saturation effects are scaled as:

$$RCO_{eff} = \frac{RCO}{AREA \cdot M} \quad QCO_{eff} = QCO \cdot AREA \cdot M$$

Parasitic capacitances are scaled as:

$$\begin{aligned} CBCP_{eff} &= CBCP \cdot AREA \cdot M \\ CBEP_{eff} &= CBEP \cdot AREA \cdot M \\ CCSP_{eff} &= CCSP \cdot AREA \cdot M \end{aligned}$$

The high current roll-off parameters ***IKF*** and ***IKR*** are scaled as follows:

$$IKF_{eff} = IKF \cdot AREA \cdot M \quad IKR_{eff} = IKR \cdot AREA \cdot M$$

For a lateral structure, ***AREAB*** is replaced by ***AREAC***, and ***AREAC*** by ***AREAB***, in all the equations.

5.0 DC Current Calculations

5.1 Collector and base currents

The forward current and gain characteristics are determined through parameters ***IS***, ***IBE***, ***ISE***, ***BF***, ***NF***, ***NE*** and ***IKF***. The parameters ***IS***, ***IBC***, ***ISC***, ***BR***, ***NR***, ***NC*** and ***IKR*** determine the reverse current and gain characteristics. The elementary currents ***ibe***, ***ibc***, ***iben***, ***ibcn*** are determined as follows:

$$ibe = IBE_{eff} \cdot \left(\exp \frac{vbe}{NF \cdot Vt} - 1 \right) \quad ibc = IBC_{eff} \cdot \left(\exp \frac{Vbc}{NR \cdot Vt} - 1 \right)$$

$$iben = ISE_{eff} \cdot \left(\exp \frac{vbe}{NE \cdot Vt} - 1 \right) \quad ibcn = ISC_{eff} \cdot \left(\exp \frac{Vbc}{NC \cdot Vt} - 1 \right)$$

iben and ***ibcn*** represent the contribution of the recombination in the Base-Emitter and Base-Collector space charge regions at low injection levels.

The base charge factor ***qb*** is defined as: $qb = \frac{q1}{2} \cdot \left(1 + (1 + 4 \cdot q2)^{NKF} \right)$

$$\text{where: } \frac{1}{q1} = 1 - \frac{Vbc}{VAF} - \frac{vbc}{VAR} \quad q2 = \frac{ibe}{IKF_{eff}} + \frac{ibc}{IKR_{eff}}$$

where ***IKF_{eff}*** and ***IKR_{eff}*** are, respectively, the effective high current forward and reverse beta roll-off.

The total collector current, ***ic***, and the total base current, ***ib***, are calculated as:

$$ib = \frac{ibe}{BF} + \frac{ibc}{BR} + iben + ibcn \quad ic = \frac{ibe - ibc}{qb} - \frac{ibc}{BR} - ibcn$$

5.2 Substrate current

The substrate current is defined through the definition of a substrate diode, whose connection depends on the device structure (please also refer to “[Structure conventions](#)” on page 4-1).

For the vertical BJT, the substrate diode current i_{cs} is:

$$i_{cs} = ISS_{eff} \cdot \left(\exp \frac{V_{cS}}{NSS \cdot V_t} - 1 \right)$$

For the lateral BJT, the substrate diode current i_{bs} is:

$$i_{bs} = ISS_{eff} \cdot \left(\exp \frac{vbS}{NSS \cdot V_t} - 1 \right)$$

5.3 Quasi-saturation effects

Because power devices require increased voltage, current and power ratings, they present the problem of quasi-saturation. So, the BJT model has been modified to include modeling of this effect using the approach developed in the paper by Kull and Co.

The epitaxial current I_{epi} is determined by the following equations:

$$I_{epi} = \frac{k_{in} - k_{ex} - \log \left(\frac{1 + k_{in}}{1 + k_{ex}} \right) + \frac{V_{bc} - V_{bc1}}{V_t}}{\frac{RCO_{eff}}{V_t} \cdot \left(1 + \frac{|V_{bc} - V_{bc1}|}{V_0} \right)}$$

where:

$$k_{in} = \sqrt{1 + GAMMA \cdot \exp \frac{V_{bc}}{V_t}} \quad k_{ex} = \sqrt{1 + GAMMA \cdot \exp \frac{V_{bc1}}{V_t}}$$

Associated with this current, two charges, Q_{in} and Q_{ex} are defined as:

$$Qin = QCO_{eff} \cdot \left(kin - 1 - \frac{GAMMA}{2} \right) \quad Qex = QCO_{eff} \cdot \left(kex - 1 - \frac{GAMMA}{2} \right)$$

These charges are used to define ***c_{in}*** and ***c_{ex}*** capacitances as:

$$c_{in} = \frac{\partial}{\partial Vbc} Qin \quad c_{ex} = \frac{\partial}{\partial Vbc1} Qex$$

5.4 Series resistance

Three ohmic resistances ***rb***, ***rc***, ***re*** are included depending on ***RE***, ***RC***, ***RB***, ***RBM***, ***IRB*** model parameters mainly. They are calculated as:

$$rb = \frac{RB_{eff}}{M \cdot AREA} \quad rc = \frac{RC_{eff}}{M \cdot AREA} \quad re = \frac{RE}{M \cdot AREA}$$

If ***IRB*** is not specified, $RB_{eff} = RBM + \frac{RB - RBM}{qb}$

$$\text{else } RB_{eff} = RBM + \frac{\tan Z - Z}{Z \cdot \tan^2 Z}$$

$$\text{where } Z = \frac{\pi^2}{24} \cdot \sqrt{\frac{IRB \cdot M \cdot AREA}{ib}} \cdot \left(\sqrt{1 + \frac{144 \cdot ib}{\pi^2 \cdot IRB \cdot M \cdot AREA}} - 1 \right)$$

If ***VORC*** is not specified, $RC_{eff} = RC$ else $RC_{eff} = RC \cdot \left(1 + \frac{Vc1C}{VORC} \right)$

6.0 Capacitance Calculations

DCAP is the selector for the capacitance model. If **DCAP**=2 then **FC**=0. The following equations are for the case of **DCAP**=1 or 2, for the case of **DCAP**=2 put **FC**=0 in the equations.

6.1 Base-emitter capacitance

The base-emitter capacitance, **cbe**, is the sum of the forward transit time (diffusion) capacitance and the depletion capacitance. Therefore, **cbe** = **ctbe** + **cdbe**.

The transit time, **TF**, is bias dependent through parameters **XTF**, **ITF**, **VTF** to define the diffusion capacitance **ctbe** as follows:

$$ctbe = \frac{\partial}{\partial vbe} \left(TF \cdot \left(1 + XTF \cdot \left(\frac{ibe}{ibe + ITF \cdot M \cdot AREA} \right)^2 \cdot \exp\left(\frac{Vbc}{1.44 \cdot VTF}\right) \right) \cdot \frac{ibe}{qb} \right)$$

The model parameters that influence the base-emitter depletion capacitance are **FC**, **CJE**, **VJE**, **MJE**.

$$\text{If } vbe < FC \cdot VJE \text{ then } cdbe = CJE_{eff} \cdot \left(1 - \frac{vbe}{VJE} \right)^{-MJE}$$

$$\text{else } cdbe = \frac{CJE_{eff}}{(1 - FC)^{1 + MJE}} \cdot \left(1 - FC \cdot (1 + MJE) + \frac{MJE \cdot vbe}{VJE} \right)$$

6.2 Base-collector capacitance

The base-collector capacitance, **cbc**, is the sum of the reverse transit time (diffusion) capacitance through **TR** model parameter and the depletion capacitance through **CJC**, **FC**, **MJC**, **VJC**, **XCJC** model parameters.

To model the non-uniform charge distribution, the base-collector capacitance is distributed by connecting one capacitor, **cbx**, from the external base node to the internal collector node, controlled by the voltage **vBc**, and another by connecting

capacitor, c_{bc} , from the internal base node to the internal collector node, controlled by the voltage v_{bc} .

So, $c_{bc} = ctbc + XCJC \cdot cdbc$ and $c_{bx} = (1 - XCJC) \cdot cdbx$.

The diffusion capacitance, $ctbc$, is defined as: $ctbc = TR \cdot \frac{\partial ibc}{\partial Vbc}$

The internal depletion capacitance, $cdbc$, is calculated as:

$$\text{If } v_{bc} < FC \cdot VJC \text{ then } cdbc = CJC_{eff} \cdot \left(1 - \frac{Vbc}{VJC}\right)^{-MJC}$$

$$\text{else } cdbc = \frac{CJC_{eff}}{(1 - FC)^{1+MJC}} \cdot \left(1 - FC \cdot (1 + MJC) + \frac{MJC \cdot Vbc}{VJC}\right)$$

The external depletion capacitance, $cdbx$, is calculated as:

$$\text{If } VBc < FC \cdot VJC \text{ then } cdbx = CJC_{eff} \cdot \left(1 - \frac{VBc}{VJC}\right)^{-MJC}$$

$$\text{else } cdbx = \frac{CJC_{eff}}{(1 - FC)^{1+MJC}} \cdot \left(1 - FC \cdot (1 + MJC) + \frac{MJC \cdot VBc}{VJC}\right)$$

6.3 Substrate capacitance

The connection of the substrate capacitance depends on the chosen (vertical or lateral) structure of the device.

For vertical BJT, the collector to substrate capacitance, ccs , is modeled as a depletion capacitance. The input model parameters affecting it are **CJS**, **VJS**, **MJS**.

$$\text{If } VcS < 0 \text{ then } ccs = CJS_{eff} \cdot \left(1 - \frac{VcS}{VJS}\right)^{-MJS}$$

$$\text{else } ccs = CJS_{eff} \cdot \left(1 + \frac{MJS \cdot VcS}{VJS}\right)$$

For lateral BJT, the base to substrate capacitances are modeled as depletion capacitances. The input model parameters affecting them are also **CJS**, **VJS**, **MJS**, where **VJS** represents the B-S zero built-in potential and **CJS** is the zero-bias base-substrate capacitance. Similarly to the collector capacitance, the base to substrate capacitance may be distributed between external and internal base nodes through the model parameter **XJBS**.

The internal base to substrate capacitance, **cbs**, is controlled by the voltage **vBS** as:

$$\text{If } vBS < 0 \text{ then } cbs = CJS_{eff} \cdot \left(1 - \frac{vBS}{VJC}\right)^{-MJS} \cdot XJBS$$

$$\text{else } cbs = CJS_{eff} \cdot \left(1 + \frac{MJS \cdot vBS}{VJS}\right) \cdot XJBS$$

The external base to substrate capacitance, **cxs**, is controlled by the voltage **vBS** as:

$$\text{If } vBS < 0 \text{ then } cxs = CJS_{eff} \cdot \left(1 - \frac{vBS}{VJC}\right)^{-MJS} \cdot (1 - XJBS)$$

$$\text{else } cxs = CJS_{eff} \cdot \left(1 + \frac{MJS \cdot vBS}{VJS}\right) \cdot (1 - XJBS)$$

7.0 Temperature Related Equations

7.1 General definitions

$$Vt(T) = k_B \cdot \frac{T}{q} \quad \delta T = T - T_{nom}$$

If **TLEV** = 2 then an improved effective Energy Gap of PN junction is used:

$$EG_{eff}(T) = EG - GAP1 \cdot \frac{T^2}{T + GAP2}$$

$$fact = \frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + XTI \cdot \ln \frac{T}{T_{nom}}$$

Otherwise they are defined as:

$$EG_{eff}(T) = 1.16 - 7.02 \cdot 10^{-4} \cdot \frac{T^2}{T + 1108}$$

$$fact = \frac{EG}{Vt(T_{nom})} - \frac{EG}{Vt(T)} + XTI \cdot \ln \frac{T}{T_{nom}}$$

7.2 Saturation current, beta, IKF, IKR and IRB equations

(**TLEV** = 0, 1 or 2)

If **TLEV** = 1 then a modified relation is applied for **factor** and calculated as:

$$factor = 1 + XTB \cdot \delta T$$

otherwise if **TLEV** = 0 or 2:

$$factor = \left(\frac{T}{T_{nom}} \right)^{XTB}$$

If **TBF1** & **TBF2** are equal to 0 (**TBR1** & **TBR2** are equal to 0), the forward (and reverse) gain are then updated as:

$$BF(T) = BF \cdot factor$$

$$BR(T) = BR \cdot factor$$

Otherwise, ***BF*** (and ***BR***) are updated with the ***TBF1 & TBF2 (TBR1 & TBR2)*** as shown in “[Other temperature equations](#)” on page 4-20.

$$IS(T) = IS \cdot \exp(fact) \quad ISE(T) = \frac{ISE}{factor} \cdot \exp\left(\frac{fact}{NE}\right)$$

$$ISC(T) = \frac{ISC}{factor} \cdot \exp\left(\frac{fact}{NC}\right) \quad ISS(T) = \frac{ISS}{factor} \cdot \exp\left(\frac{fact}{NS}\right)$$

If both ***IBE*** and ***IBC*** are defined, then they vary as:

$$IBE(T) = IBE \cdot \exp\left(\frac{fact}{NF}\right) \quad IBC(T) = IBC \cdot \exp\left(\frac{fact}{NR}\right)$$

The parameters ***IRB***, ***IKF*** and ***IKR*** are modified as follows (***TLEV=0, 1 or 2***):

$$\begin{aligned} IKF(T) &= IKF \cdot (1 + TIKF1 \cdot \delta T + TIKF2 \cdot \delta T^2) \\ IKR(T) &= IKR \cdot (1 + TIKR1 \cdot \delta T + TIKR2 \cdot \delta T^2) \\ IRB(T) &= IRB \cdot (1 + TIRB1 \cdot \delta T + TIRB2 \cdot \delta T^2) \end{aligned}$$

(***TLEV = 3***)

The temperature equations for the saturation currents are:

$$\begin{aligned} IS(T) &= IS^{(1 + TIS1 \cdot \delta T + TIS2 \cdot \delta T^2)} \\ IBE(T) &= IBE^{(1 + TIS1 \cdot \delta T + TIS2 \cdot \delta T^2)} \\ IBC(T) &= IBC^{(1 + TIS1 \cdot \delta T + TIS2 \cdot \delta T^2)} \\ ISE(T) &= ISE^{(1 + TISE1 \cdot \delta T + TISE2 \cdot \delta T^2)} \\ ISC(T) &= ISC^{(1 + TISC1 \cdot \delta T + TISC2 \cdot \delta T^2)} \\ ISS(T) &= ISS^{(1 + TISS1 \cdot \delta T + TISS2 \cdot \delta T^2)} \end{aligned}$$

The parameters ***IRB***, ***IKF*** and ***IKR*** are modified as follows:

$$IRB(T) = IRB^{(1 + TIRB1 \cdot \delta T + TIRB2 \cdot \delta T^2)}$$

$$IKF(T) = IKF^{(1 + TIKF1 \cdot \delta T + TIKF2 \cdot \delta T^2)}$$

$$IKR(T) = IKR^{(1 + TIKR1 \cdot \delta T + TIKR2 \cdot \delta T^2)}$$

7.3 Resistance related temperature equations

$$RC(T) = RC \cdot (1 + TRC1 \cdot \delta T + TRC2 \cdot \delta T^2)$$

$$RE(T) = RE \cdot (1 + TRE1 \cdot \delta T + TRE2 \cdot \delta T^2)$$

$$RB(T) = RB \cdot (1 + TRB1 \cdot \delta T + TRB2 \cdot \delta T^2)$$

$$RBM(T) = RBM \cdot (1 + TRM1 \cdot \delta T + TRM2 \cdot \delta T^2)$$



The resistor values of ***RB***, ***RC***, ***RE*** and ***RBM*** after temperature update are clipped to 1×10^{-5} if less than 1×10^{-5} . This is only valid under the **ACM** flag.

7.4 Capacitance related temperature equations

The parameters ***MJE*** and ***MJC*** are updated using the following equations:

$$MJE(T) = MJE \cdot (1 + TMJE1 \cdot \delta T + TMJE2 \cdot \delta T^2)$$

$$MJC(T) = MJC \cdot (1 + TMJC1 \cdot \delta T + TMJC2 \cdot \delta T^2)$$

If (**TUDJS** = 1 and **TLEV=0**) or (**TLEV=1, 2 or 3**) then ***MJS*** is updated as follows:

$$MJS(T) = MJS \cdot (1 + TMJS1 \cdot \delta T + TMJS2 \cdot \delta T^2)$$

For the case of **TLEV=0**

$$VJE(T) = VJE \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right)$$

$$CJE(T) = CJE \cdot \left(1 + MJE(T) \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta T - \frac{VJE(T)}{VJE} \right) \right)$$

$$VJC(T) = VJC \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right)$$

$$CJC(T) = CJC \cdot \left(1 + MJC(T) \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta T - \frac{VJC(T)}{VJC} \right) \right)$$

If **TUDJS = 1** then **MJS**, **VJS**, and **CJS** are updated as follows:

$$VJS(T) = VJS \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right)$$

$$CJS(T) = CJS \cdot \left(1 + MJS(T) \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta T - \frac{VJS(T)}{VJS} \right) \right)$$

For the case of **TLEV=1**

$$CJE(T) = CJE \cdot (1 + CTE \cdot \delta T)$$

$$CJC(T) = CJC \cdot (1 + CTC \cdot \delta T)$$

$$CJS(T) = CJS \cdot (1 + CTS \cdot \delta T)$$

$$VJE(T) = VJE - TVJE \cdot \delta T$$

$$VJC(T) = VJC - TVJC \cdot \delta T$$

$$VJS(T) = VJS - TVJS \cdot \delta T$$

For the case of **TLEV=2**

$$CJE(T) = CJE \cdot \left(\frac{VJE}{VJE(T)} \right)^{MJE}$$

$$CJC(T) = CJC \cdot \left(\frac{VJC}{VJC(T)} \right)^{MJC}$$

$$CJS(T) = CJS \cdot \left(\frac{VJS}{VJS(T)} \right)^{MJS}$$

$$VJE(T) = VJE - TVJE \cdot \delta T$$

$$VJC(T) = VJC - TVJC \cdot \delta T$$

$$VJS(T) = VJS - TVJS \cdot \delta T$$

For the case of **TLEV=3**

$$CJE(T) = CJE \cdot \left(1 - 0.5 \cdot dvjedt \cdot \frac{\delta T}{VJE} \right)$$

$$CJC(T) = CJC \cdot \left(1 - 0.5 \cdot dvjcdt \cdot \frac{\delta T}{VJC} \right)$$

$$CJS(T) = CJS \cdot \left(1 - 0.5 \cdot dvjsdt \cdot \frac{\delta T}{VJS} \right)$$

$$VJE(T) = VJE + dvjedt \cdot \delta T$$

$$VJC(T) = VJC + dvjcdt \cdot \delta T$$

$$VJS(T) = VJS + dvjsdt \cdot \delta T$$

where for **TLEV=0,1 or 3**

$$\begin{aligned} dvjedt &= -\frac{EG_{eff}(T_{nom}) + 3 \cdot Vt(T_{nom}) + (1.16 - EG_{eff}(T_{nom})) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + 1108}\right) - VJE}{T_{nom}} \\ dvjcdt &= -\frac{EG_{eff}(T_{nom}) + 3 \cdot Vt(T_{nom}) + (1.16 - EG_{eff}(T_{nom})) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + 1108}\right) - VJC}{T_{nom}} \\ dvjsdt &= -\frac{EG_{eff}(T_{nom}) + 3 \cdot Vt(T_{nom}) + (1.16 - EG_{eff}(T_{nom})) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + 1108}\right) - VJS}{T_{nom}} \end{aligned}$$

while for **TLEV=2**

$$\begin{aligned} dvjedt &= -\frac{EG_{eff}(T_{nom}) + 3 \cdot Vt(T_{nom}) + (EG - EG_{eff}(T_{nom})) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + GAP2}\right) - VJE}{T_{nom}} \\ dvjcdt &= -\frac{EG_{eff}(T_{nom}) + 3 \cdot Vt(T_{nom}) + (EG - EG_{eff}(T_{nom})) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + GAP2}\right) - VJC}{T_{nom}} \\ dvjsdt &= -\frac{EG_{eff}(T_{nom}) + 3 \cdot Vt(T_{nom}) + (EG - EG_{eff}(T_{nom})) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + GAP2}\right) - VJS}{T_{nom}} \end{aligned}$$

where, **EGnom** is EG at nominal temperature; **vtnom** is Vt at nominal temperature.

7.5 Quasi-saturation temperatures

$$GAMMA(T) = GAMMA \cdot \exp\left(fact + (XTG - XTI) \cdot \ln \frac{T}{T_{nom}}\right)$$

$$RCO(T) = RCO \cdot \left(\frac{T}{T_{nom}}\right)^{XTRCO} \quad VO(T) = VO \cdot \left(\frac{T}{T_{nom}}\right)^{XTVO}$$

7.6 Other temperature equations

$$VAF(T) = VAF \cdot (1 + TVAF1 \cdot \delta T + TVAF2 \cdot \delta T^2)$$

$$VAR(T) = VAR \cdot (1 + TVAR1 \cdot \delta T + TVAR2 \cdot \delta T^2)$$

$$TF(T) = TF \cdot (1 + TTF1 \cdot \delta T + TTF2 \cdot \delta T^2)$$

$$TR(T) = TR \cdot (1 + TTR1 \cdot \delta T + TTR2 \cdot \delta T^2)$$

$$ITF(T) = ITF \cdot (1 + TITF1 \cdot \delta T + TITF2 \cdot \delta T^2)$$

$$NF(T) = NF \cdot (1 + TNF1 \cdot \delta T + TNF2 \cdot \delta T^2)$$

$$NR(T) = NR \cdot (1 + TNR1 \cdot \delta T + TNR2 \cdot \delta T^2)$$

$$NE(T) = NE \cdot (1 + TNE1 \cdot \delta T + TNE2 \cdot \delta T^2)$$

$$NC(T) = NC \cdot (1 + TNC1 \cdot \delta T + TNC2 \cdot \delta T^2)$$

$$NS(T) = NS \cdot (1 + TNS1 \cdot \delta T + TNS2 \cdot \delta T^2)$$

BF and **BR** are updated by temperature using the following equations for all **TLEVs**:

$$BF(T) = BF \cdot (1 + TBF1 \cdot \delta T + TBF2 \cdot \delta T^2)$$

$$BR(T) = BR \cdot (1 + TBR1 \cdot \delta T + TBR2 \cdot \delta T^2)$$

8.0 Noise

Two different noise sources exist. Refer to the noise model in [Figure 4-3 on page 4-5](#).

Base to Emitter Noise

- Shot Noise

$$SI = 2 \times q \times IB$$

where **IB** is the current through the base.

- Flicker Noise

$$SI = \frac{KF \times IB^{AF}}{f}$$

Collector to Emitter Noise

- Shot Noise

$$SI = 2 \times q \times IC$$

where IC is the current through the collector.

- Thermal Noise

$$SI = \frac{4 \times k \times T}{RB}, SI = \frac{4 \times k \times T}{RE}, SI = \frac{4 \times k \times T}{RC}$$

9.0 Model Parameters

Nr.	Name	Description	Default	Units
DC Related Model Parameters				
1	IS	Transport saturation current	1.0×10^{-16}	A
2	IBE	Saturation current for base-emitter junction	0	A
3	IBC	Saturation current for base-collector junction	0	A
4	NR	Reverse current emission coefficient	1	
5	NF	Forward current emission coefficient	1	
6	BR (BRM)	Ideal maximum reverse beta	1	
7	BF (BFM)	Ideal maximum forward beta	100	
8	ISE (JLE)	B-E leakage saturation current	0	A
9	NE (NLE)	B-E leakage emission coefficient	1.5	
10	ISC (JLC)	B-C leakage saturation current	0	A
11	NC (NLC)	B-C leakage emission coefficient	2	
12	ISS	Saturation current for substrate junction	0	A
13	NS (NSS)	Substrate current emission coefficient	1	
14	VAF (VA, VBF)	Forward early voltage	∞	V
15	VAR (VB, VRB)	Reverse early voltage	∞	V

Nr.	Name	Description	Default	Units
16	IKF (IK, JBF)	Corner current for forward beta high current roll-off	∞	A
17	IKR (JBR)	Corner current for reverse beta high current roll-off	∞	A
18	NKF (NK)	Exponent for high current beta roll-off	0.5	
Quasi-saturation Related Model Parameters				
19	GAMMA	Expitaxial doping factor	1.5×10^{-11}	
20	RCO	Expitaxial region resistance	0	Ω
21	VO	Thickness of the oxide layer	10	V
22	QCO	Expitaxial charge factor	0	Cb
23	XTG	GAMMA temperature exponent	XTI	
24	XTRCO (BEX)	RCO temperature exponent	2.42	
25	XTVO (BEXV)	vo temperature exponent	1.90	
26	BRS (BRSG)	Reverse beta for substrate BJT	0	
Parasitic Resistance Related Model Parameters				
27	RB	Zero bias base resistance	0	Ω
28	RC	Collector resistance	0	Ω
29	RE	Emitter resistance	0	Ω
30	RBM	Minimum base resistance at high currents	RB	Ω
31	IRB (JRB, IOB)	Current where the base resistance falls halfway to its minimum value	∞	A
32	VORC	Velocity saturation factor	0	V
Parasitic Capacitance Related Model Parameters				
33	CBCP	External base-collector constant capacitance	0	F
34	CBEP	External base-emitter constant capacitance	0	F
35	CCSP	External collector-substrate constant capacitance (vertical) or base-substrate (lateral)	0	F
Junction Capacitance Related Model Parameters				
36	DCAP	Capacitance model selector	1	
37	CJE	B-E zero-bias depletion capacitance	0	F
38	VJE (PE)	B-E built-in potential	0.75	V
39	MJE (ME)	B-E junction exponential factor	0.33	
40	CJC	B-C zero-bias depletion capacitance	0	F
41	VJC (PC)	B-C built-in potential	0.75	V
42	MJC (MC)	B-C junction exponential factor	0.33	
43	XCJC (CDIS)	Fraction of base-collector depletion capacitance connected to the internal base node	1	

Nr.	Name	Description	Default	Units
44	XJBS	For lateral devices; portion of the base-substrate depletion capacitance connected to the internal base node	1	
45	CJS (CCS,CSUB)	Zero-bias collector substrate capacitance	0	F
46	VJS (PS,PSUB)	Substrate junction built-in potential	0.75	V
47	MJS (MS,ESUB)	Substrate junction exponential factor	0	
48	FC	Coefficient for the calculation of the forward bias depletion capacitance	0.5	
Dynamic Model Parameters				
49	TF	Ideal forward transient time	0	s
50	XTF	Coefficient for bias dependence of TF	0	
51	VTF	Voltage describing dependence of TF on the base-collector voltage, VBC	∞	V
52	ITF (JTF)	High current parameter effecting TF	0	A
53	TR	Ideal reverse transit time	0	s
54	PTF	Excess phase at frequency=1.0/(TF .2 π) Hertz	0	°C
Noise Related Model Parameters				
55	KF	Flicker noise coefficient	0	
56	AF	Flicker noise exponent	1	
Temperature Related Model Parameters				
57	TNOM (TREF)	Nominal temperature	27	°C
58	TMOD	Model temperature	TNOM	°C
59	TLEV	Temperature equation selector	0	
60	TLEVC	Temperature equation selector for junction capacitance and potential	0	
61	TUDJS	Flag for updating substrate junction capacitance, potential and exponential factor	1	
62	GAP1	First bandgap correction factor	7.02×10^{-4}	eV×°K ⁻¹
63	GAP2	Second bandgap correction factor	1108	°K
64	EG	Energy gap for temperature effect on IS	1.11	eV
65	XTB (TB, TCB)	Forward and reverse beta temperature exponent	0	
66	XTI	Temperature exponent for effect on IS	3	
67	TBF1	Temperature coefficient (Linear) for BF	0	°C ⁻¹
68	TBF2	Temperature coefficient (Quadratic) for BF	0	°C ⁻²
69	TBR1	Temperature coefficient (Linear) for BR	0	°C ⁻¹
70	TBR2	Temperature coefficient (Quadratic) for BR	0	°C ⁻²

Nr.	Name	Description	Default	Units
71	TIRB1	Temperature coefficient (Linear) for IRB	0	$^{\circ}\text{C}^{-1}$
72	TIRB2	Temperature coefficient (Quadratic) for IRB	0	$^{\circ}\text{C}^{-2}$
73	TIKF1	Temperature coefficient (Linear) for IKF	0	$^{\circ}\text{C}^{-1}$
74	TIKF2	Temperature coefficient (Quadratic) for IKF	0	$^{\circ}\text{C}^{-2}$
75	TIKR1	Temperature coefficient (Linear) for IKR	0	$^{\circ}\text{C}^{-1}$
76	TIKR2	Temperature coefficient (Quadratic) for IKR	0	$^{\circ}\text{C}^{-2}$
77	TITF1	Temperature coefficient (Linear) for ITF	0	$^{\circ}\text{C}^{-1}$
78	TITF2	Temperature coefficient (Quadratic) for ITF	0	$^{\circ}\text{C}^{-2}$
79	TMJC1	Temperature coefficient (Linear) for MJC	0	$^{\circ}\text{K}^{-1}$
80	TMJC2	Temperature coefficient (Quadratic) for MJC	0	$^{\circ}\text{K}^{-2}$
81	TMJE1	Temperature coefficient (Linear) for MJE	0	$^{\circ}\text{K}^{-1}$
82	TMJE2	Temperature coefficient (Quadratic) for MJE	0	$^{\circ}\text{K}^{-2}$
83	TMJS1	Temperature coefficient (Linear) for MJS	0	$^{\circ}\text{K}^{-1}$
84	TMJS2	Temperature coefficient (Quadratic) for MJS	0	$^{\circ}\text{K}^{-2}$
85	TRB1	Temperature coefficient (Linear) for RB	0	$^{\circ}\text{C}^{-1}$
86	TRB2	Temperature coefficient (Quadratic) for RB	0	$^{\circ}\text{C}^{-2}$
87	TRC1 (TRC)	Temperature coefficient (Linear) for RC	0	$^{\circ}\text{C}^{-1}$
88	TRC2	Temperature coefficient (Quadratic) for RC	0	$^{\circ}\text{C}^{-2}$
89	TRE1 (TRE)	Temperature coefficient (Linear) for RE	0	$^{\circ}\text{C}^{-1}$
90	TRE2	Temperature coefficient (Quadratic) for RE	0	$^{\circ}\text{C}^{-2}$
91	TRM1 (TRBM1)	Temperature coefficient (Linear) for RBM	0	$^{\circ}\text{C}^{-1}$
92	TRM2 (TRBM2)	Temperature coefficient (Quadratic) for RBM	0	$^{\circ}\text{C}^{-2}$
93	TTF1	Temperature coefficient (Linear) for TF	0	$^{\circ}\text{K}^{-1}$
94	TTF2	Temperature coefficient (Quadratic) for TF	0	$^{\circ}\text{K}^{-2}$
95	TTR1	Temperature coefficient (Linear) for TR	0	$^{\circ}\text{K}^{-1}$
96	TTR2	Temperature coefficient (Quadratic) for TR	0	$^{\circ}\text{K}^{-2}$
97	TVAF1	Temperature coefficient (Linear) for VAF	0	$^{\circ}\text{K}^{-1}$
98	TVAF2	Temperature coefficient (Quadratic) for VAF	0	$^{\circ}\text{K}^{-2}$
99	TVAR1	Temperature coefficient (Linear) for VAR	0	$^{\circ}\text{K}^{-1}$
100	TVAR2	Temperature coefficient (Quadratic) for VAR	0	$^{\circ}\text{K}^{-2}$
101	TISC1	Temperature coefficient (Linear) for ISC	0	$^{\circ}\text{K}^{-1}$
102	TISC2	Temperature coefficient (Quadratic) for ISC	0	$^{\circ}\text{K}^{-2}$
103	TIS1	Temperature coefficient (Linear) for IS or IBE and IBC	0	$^{\circ}\text{K}^{-1}$

Nr.	Name	Description	Default	Units
104	TIS2	Temperature coefficient (Quadratic) for IS or IBE and IBC	0	$^{\circ}\text{K}^{-2}$
105	TISE1	Temperature coefficient (Linear) for ISE	0	$^{\circ}\text{K}^{-1}$
106	TISE2	Temperature coefficient (Quadratic) for ISE	0	$^{\circ}\text{K}^{-2}$
107	TISS1	Temperature coefficient (Linear) for ISS	0	$^{\circ}\text{K}^{-1}$
108	TISS2	Temperature coefficient (Quadratic) for ISS	0	$^{\circ}\text{K}^{-2}$
109	TNC1	Temperature coefficient (Linear) for NC	0	$^{\circ}\text{K}^{-1}$
110	TNC2	Temperature coefficient (Quadratic) for NC	0	$^{\circ}\text{K}^{-2}$
111	TNE1	Temperature coefficient (Linear) for NE	0	$^{\circ}\text{K}^{-1}$
112	TNE2	Temperature coefficient (Quadratic) for NE	0	$^{\circ}\text{K}^{-2}$
113	TNF1	Temperature coefficient (Linear) for NF	0	$^{\circ}\text{K}^{-1}$
114	TNF2	Temperature coefficient (Quadratic) for NF	0	$^{\circ}\text{K}^{-2}$
115	TNR1	Temperature coefficient (Linear) for NR	0	$^{\circ}\text{K}^{-1}$
116	TNR2	Temperature coefficient (Quadratic) for NR	0	$^{\circ}\text{K}^{-2}$
117	TNS1	Temperature coefficient (Linear) for NS	0	$^{\circ}\text{K}^{-1}$
118	TNS2	Temperature coefficient (Quadratic) for NS	0	$^{\circ}\text{K}^{-2}$
119	CTC	Temperature coefficient for zero-bias base collector capacitance (used with TLEVc=1)	0	$^{\circ}\text{K}^{-1}$
120	CTE	Temperature coefficient for zero-bias base emitter capacitance (used with TLEVc=1)	0	$^{\circ}\text{K}^{-1}$
121	CTS	Temperature coefficient for zero-bias substrate capacitance (used with TLEVc=1)	0	$^{\circ}\text{K}^{-1}$
122	TVJC	Temperature coefficient for VJC (used with TLEVc=1,2)	0	$\text{V}^{\circ}\text{K}^{-1}$
123	TVJE	Temperature coefficient for VJE (used with TLEVc=1,2)	0	$\text{V}^{\circ}\text{K}^{-1}$
124	TVJS	Temperature coefficient for VJS (used with TLEVc=1,2)	0	$\text{V}^{\circ}\text{K}^{-1}$

Chapter 5

VBIC Equations

1.0 Introduction

The VBIC model is a Bipolar Junction Transistor (BJT) model. VBIC stands for Vertical Bipolar InterCompany Model. The VBIC model was developed as an industry-standard, public domain replacement for the SPICE Gummel-Poon (SGP) model. VBIC is designed to be as similar as possible to the SGP model, yet overcomes its major deficiencies. VBIC improvements on SGP:

- Improved Early effect modeling
- Quasi-saturation modeling
- Parasitic substrate transistor modeling
- Parasitic fixed (oxide) capacitance modeling
- Includes an avalanche multiplication model
- Improved temperature modeling
- Base current is decoupled from collector current
- Electro-thermal modeling.

1.1 VBIC versions

Two versions of the VBIC model are available in Eldo: versions v1.1.5 and v1.2. The VBIC model is implemented in Eldo as Level 8. The different versions are accessible through the Eldo **VERSION** specification:

Parameter Value	VBIC Version
VERSION=1.2	VBIC v1.2 (default)
VERSION=1.15	VBIC v1.1.5



v1.1.5 of VBIC model was formerly Level 21 in Eldo.

Note



User's can visit the following web site to view the documentation of the older version v1.1.5:

<http://www.fht-esslingen.de/institute/iafgp/neu/VBIC/index.html>

1.2 VBIC v1.2 updates

- Base-emitter breakdown model added
- Reach-through model added for B-C depletion capacitance
- Limited exponential version added
- Problem in psibi mapping with temperature corrected
- **DTEMP** local temperature difference parameter added
- **VERS** and **VREV** (version revision) parameters added
- NKF high current beta rolloff parameter added
- Temperature dependence added to **IKF**
- Ability to select **SGP** qb formulation added (**QBM**)
- Ability to separate **IS** for fwd and rev added (**ISRR**)
- Fixed collector-substrate capacitance added (**CCSO**)
- Separate temperature coefficients added for **RCX**, **RBX**, **RBP**.

2.0 Typical Structures used for VBIC Modeling

Examples used in this chapter are mostly for 4-terminal vertical NPN transistors, [Figure 5-1](#) and [Figure 5-2](#) show typical structures that VBIC is intended to model. VBIC can also be used for vertical PNP modeling, and for HBT modeling, but it is not directly targeted at lateral BJT modeling. Vertical PNPs in smartpower technologies are often 5-terminal devices, and VBIC can be used in a subcircuit to model such devices, however this does not properly model transistor action of the second parasitic BJT.

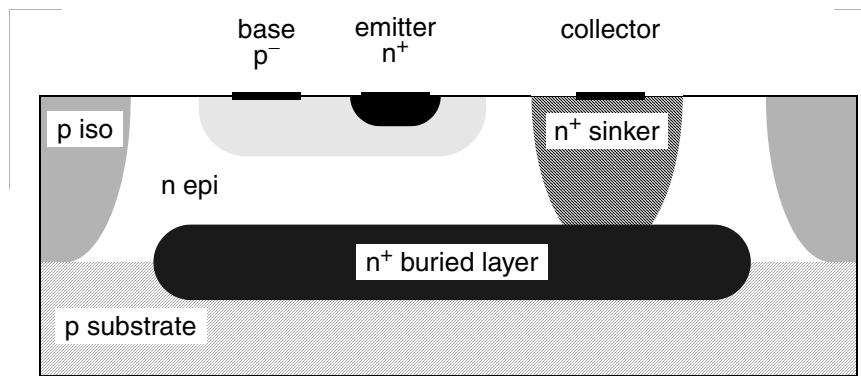


Figure 5-1. Junction isolated diffused NPN structure

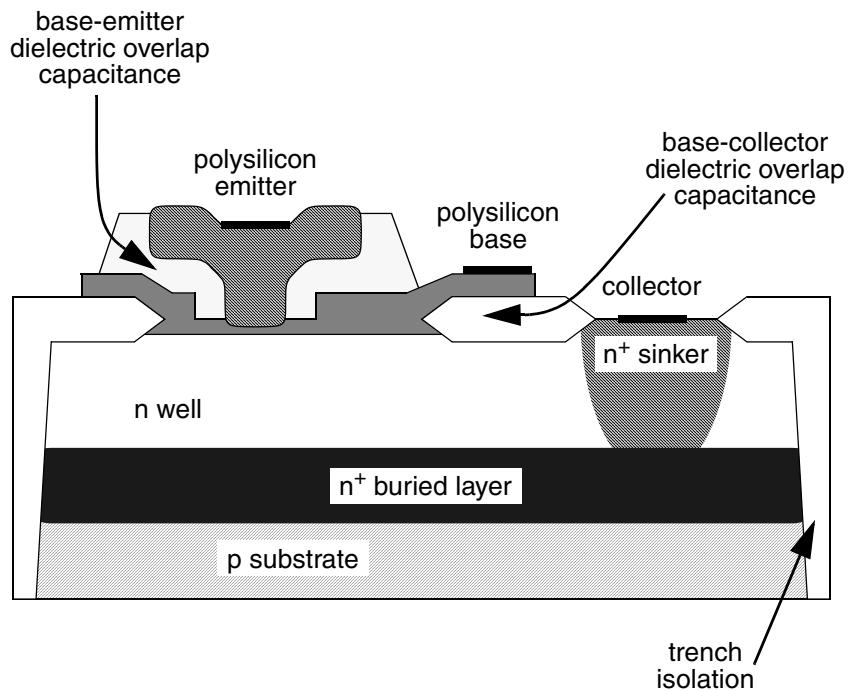


Figure 5-2. Trench isolated double poly NPN structure

Compact models for circuit simulation should scale properly with device geometry. However, for BJTs the plethora of layout topologies and structure make this impossible to do in a comprehensive manner. Therefore VBIC explicitly does not include any geometry mappings. It is assumed that geometry scaling for VBIC will be handled either in pre-processing for the generation of model libraries for circuit simulation, or via scaling relations specific to a particular technology implemented either in the simulator or the CAD system used for design.

3.0 VBIC Equivalent Network

Figure 5-3 shows the equivalent network of VBIC, which includes an intrinsic NPN transistor, a parasitic PNP transistor, parasitic resistances and capacitances, a local thermal network (used only with the electrothermal version of the model), and a circuit that implements excess phase for the forward transport current I_{tzf} .

For the electrothermal version of VBIC the branch currents and charges in the electrical part of the model also depend on the local temperature rise, the voltage on the node dt. The thermal equivalent circuit includes two nodes external to the

model so that the local heating and dissipation can be connected to a thermal network that models the thermal properties of the material in which the BJT and surrounding devices are built.

Although the equivalent network of [Figure 5-3](#) is drawn with resistances (fixed and bias dependent), capacitances, and current sources, the elements should generally be considered as voltage controlled current sources $I(V_1, V_2, \dots, V_3)$ and voltage controlled charge sources $Q(V_1, V_2, \dots, V_3)$. Simple resistors and capacitors are then current and charge sources, respectively, controlled only by the voltage across them. Branch currents and charges that are controlled by more than one branch voltage, e.g. R_{BI}/q_b and Q_{be} , include trans-conductance and trans-capacitance elements when they are linearized, as is required for DC solution and for AC, noise and transient simulations.

[Table 5-1](#) lists each of the elements of the VBIC equivalent network of [Figure 5-3](#), with a short description of the function of the element.

Name	Element
I_{tzf}	Forward transport current, zero phase
I_{txf}	Forward transport current, with excess phase
Q_{cxf}, F_{lxf}	Excess phase circuit capacitance and inductance
I_{tzr}	Reverse transport current, zero phase
I_{be}	Intrinsic base-emitter current
I_{bex}	Extrinsic (side) base-emitter current
Q_{be}	Intrinsic base-emitter charge (depletion and diffusion)
Q_{bex}	Extrinsic (side) base-emitter charge (depletion only)
I_{bc}	Intrinsic base-collector current
I_{gc}	base-collector weak avalanche current
Q_{bc}	Intrinsic base-collector charge (depletion and diffusion)
Q_{bcx}	Extrinsic base-collector charge (diffusion only)
I_{tfp}	Parasitic forward transport current
I_{trp}	Parasitic reverse transport current
I_{bep}	Parasitic base-emitter current

Name	Element
Q_{bep}	Parasitic base-emitter charge (depletion and diffusion)
I_{bcp}	Parasitic base-collector current
Q_{bcp}	Parasitic base-collector charge (depletion only)
R_{CX}	Extrinsic collector resistance (fixed)
R_{CI}	Intrinsic collector resistance (modulated)
R_{BX}	Extrinsic base resistance (fixed)
R_{BI}/q_b	Intrinsic base resistance (modulated)
R_E	Emitter resistance (fixed)
R_{BIP}/q_{bp}	Parasitic base resistance (modulated)
R_S	Substrate resistance (fixed)
C_{BEO}	Parasitic base-emitter overlap capacitance (fixed)
C_{BCO}	Parasitic base-collector overlap capacitance (fixed)
I_{th}	Thermal (heat generation) source
R_{TH}, C_{TH}	Thermal resistance and capacitance (fixed)

Table 5-1. Elements of VBIC equivalent network

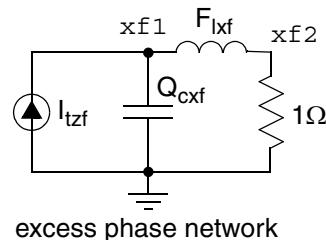
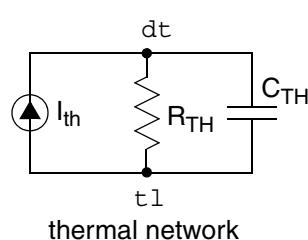
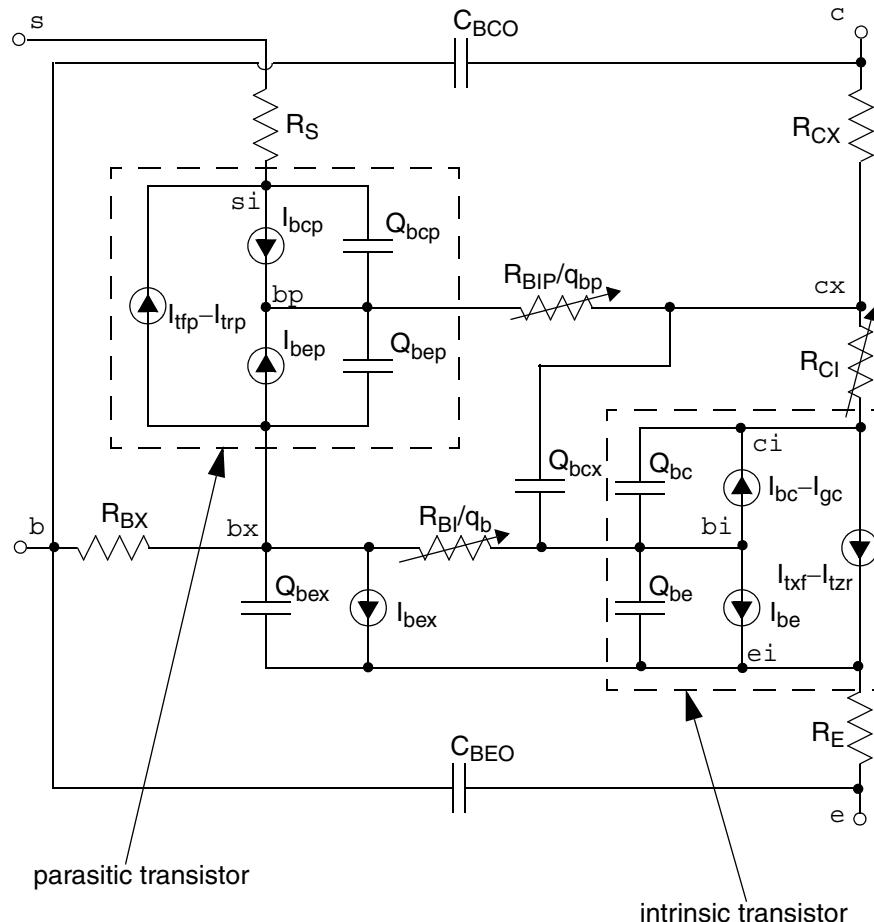


Figure 5-3. VBIC equivalent network

4.0 VBIC Model Formulation

The core of VBIC, as with most BJT models, is the transport (collector) current model, which follows directly from Gummel (1970). For electrons, the continuity equation is

$$\nabla \bullet \mathbf{J}_e = q \left(\frac{\partial n}{\partial t} + R_e - G_e \right) \quad (4.0-1)$$

where \mathbf{J}_e is the electron current density, q is the magnitude of the electronic charge, n is the mobile electron concentration, and R_e and G_e are the electron recombination and generation rates, respectively. The drift-diffusion relation for electrons is

$$\mathbf{J}_e = \mu_e (kT \nabla n - qn \nabla \psi) = -q\mu_e n \nabla \phi_e \quad (4.0-2)$$

where μ_e is the electron mobility, k is Boltzmann's constant, T is the temperature in degrees Kelvin, ψ is the electrostatic potential, and ϕ_e is the electron quasi-Fermi potential. The mobile electron concentration is

$$n = n_{ie} \exp\left(\frac{\psi - \phi_e}{V_{tv}}\right) \quad (4.0-3)$$

where n_{ie} is the effective intrinsic concentration, including bandgap narrowing, and $V_{tv} = kT/q$ is the thermal voltage.

$$p = n_{ie} \exp\left(\frac{\phi_h - \psi}{V_{tv}}\right) \quad (4.0-4)$$

gives the mobile hole concentration, where ϕ_h is the hole quasi-Fermi potential.

[Figure 5-4](#) shows a representative 1-dimensional doping profile of a vertical NPN, through the region of the device under the emitter where bipolar transistor action occurs.

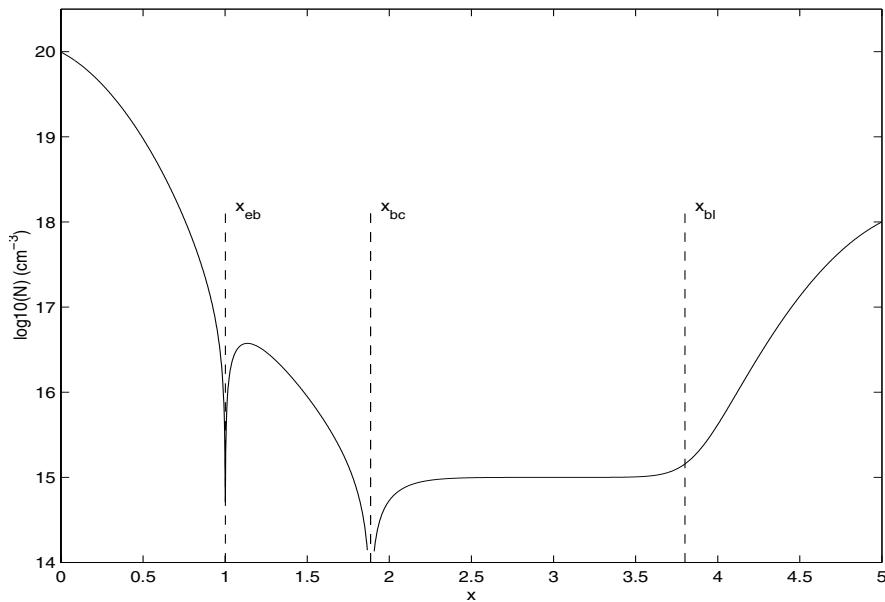


Figure 5-4. 1-dimensional doping profile

Analysis of the transport in the base region of a BJT is based on equations (4.0-1) and (4.0-2). In the steady state in the x dimension only, ignoring recombination and generation (which is generally reasonable for the base of a BJT), gives

$$\frac{\partial J_{ex}}{\partial x} = 0 \quad (4.0-5)$$

directly from equation (4.0-1), and

$$J_{ex} = \text{constant} = -q\mu_e n \frac{\partial \phi_e}{\partial x} = q\mu_e n_{ie} V_{tv} \exp\left(\frac{\psi}{V_{tv}}\right) \frac{\partial \exp(-\phi_e/V_{tv})}{\partial x} \quad (4.0-6)$$

follows after some manipulation. Integrating equation (4.0-6) from the emitter ($x = x_{eb}$, where $\phi_e = \phi_{ee}$) to the collector ($x = x_{bc}$, where $\phi_e = \phi_{ec}$) through the base gives

$$J_{ex} = qV_{tv} \frac{\exp(-\phi_{ec}/V_{tv}) - \exp(-\phi_{ee}/V_{tv})}{\int_{x_{eb}}^{x_{bc}} \frac{\exp(-\psi/V_{tv})}{\mu_e n_{ie}} dx} \quad (4.0-7)$$

where ψ , μ_e and n_{ie} are all functions of position x . Multiplying both the numerator and the denominator of equation (4.0-7) by $\exp(\phi_h/V_{tv})$, and noting that the difference between hole and electron quasi-Fermi potentials across a junction is just the voltage applied across the junction, gives

$$J_{ex} = qV_{tv} \frac{\exp(V_{bci}/V_{tv}) - \exp(V_{bei}/V_{tv})}{\int_{x_{be}}^{x_{bc}} \frac{p}{\mu_e n_{ie}^2} dx} \quad (4.0-8)$$

where $V_{bei} = \phi_h - \phi_{ee}$ is the intrinsic base-emitter voltage, between nodes bi and ei of the equivalent network of Figure 5-3, and $V_{bci} = \phi_h - \phi_{ec}$ is the intrinsic base-collector voltage, between nodes bi and ci. Equation (4.0-8) is the basis of Gummel-Poon type BJT models (Gummel 1970). It shows that the collector current varies exponentially with applied bias, and is controlled by the integrated base charge, which is commonly called the base Gummel number.



Note The limits of integration through the base are not rigorously defined above. The analysis is valid across any region in which the hole quasi-Fermi level is constant. In practice, it is convenient to define the base region as where ϕ_h is constant.

Use of equation (4.0-8) in VBIC requires the base charge to be modeled as a function of applied bias. For VBIC the base charge is normalized with respect to its value at zero applied bias, and includes depletion and diffusion components (Gummel, 1970; Getreu, 1976). The VBIC (zero excess phase) forward and reverse transport currents are

$$I_{tzf} = I_S \frac{\exp(V_{bei}/(N_F V_{tv})) - 1}{q_b} \quad (4.0-9)$$

$$I_{tzr} = I_S \frac{\exp(V_{bci}/(N_R V_{tv})) - 1}{q_b} \quad (4.0-10)$$

where I_S is the transport saturation current, N_F and N_R are the forward and reverse ideality factors, and q_b is the normalized base charge. The ideality factors

are introduced as parameters, rather being forced to be 1, to allow flexibility in modeling, to recognize that the theoretical analyses above are approximate, because non-ideal transport behavior is observed in HBTs, and for compatibility with the SGP model.

Consider a BJT operating in low level injection, in the forward active model so that $V_{bei} > 0$ and $V_{cei} = V_{bei} - V_{bci} > 0$. Considering only the transport current, and ignoring the Early effect, the power dissipated is

$$\begin{aligned} I_S \left(\exp\left(\frac{V_{bei}}{N_F V_{tv}}\right) - \exp\left(\frac{V_{bci}}{N_R V_{tv}}\right) \right) V_{cei} \\ = I_S \exp\left(\frac{V_{bei}}{N_F V_{tv}}\right) \left(1 - \exp\left(\frac{V_{bci}}{V_{tv}} \left(\frac{1}{N_R} - \frac{1}{N_F} \right)\right) \exp\left(-\frac{V_{cei}}{N_R V_{tv}}\right) \right) V_{cei} \end{aligned} \quad (4.0-11)$$

For the power dissipation to be positive, which it must be physically, it follows that

$$\exp\left(\frac{V_{bei}}{V_{tv}} \left(\frac{1}{N_R} - \frac{1}{N_F} \right)\right) \exp\left(-\frac{V_{cei}}{N_R V_{tv}}\right) \leq 1 \quad (4.0-12)$$

must hold. Given that V_{cei} can be arbitrarily close to zero, so that $\exp(-V_{cei}/(N_R V_{tv}))$ can be arbitrarily close to unity, equation (4.0-12) implies that

$$\frac{1}{N_R} - \frac{1}{N_F} \leq 0 \quad (4.0-13)$$

and hence

$$N_F \leq N_R \quad (4.0-14)$$

for the power dissipation to be positive. A similar analysis in the reverse active region of operation shows that the power dissipation is

$$I_S \exp\left(\frac{V_{bci}}{N_R V_{tv}}\right) \left(1 - \exp\left(\frac{V_{bci}}{V_{tv}} \left(\frac{1}{N_F} - \frac{1}{N_R} \right)\right) \exp\left(-\frac{V_{eci}}{N_F V_{tv}}\right) \right) V_{eci} \quad (4.0-15)$$

and because $V_{bci} > 0$ and $V_{eci} = V_{bci} - V_{bei} > 0$ this implies that

$$N_R \leq N_F. \quad (4.0-16)$$

Equations (4.0-14) and (4.0-16) mean that

$$N_R = N_F \quad (4.0-17)$$

must hold, for the model to be passive and not generate power. Although equation (4.0-17) was derived under some restrictive approximations, and data from HBTs clearly shows that $N_R \neq N_F$, it is apparent that with certain values of model parameters VBIC (and SGP) can be nonpassive.

It is undesirable for a model to rely on having certain values of model parameters to display reasonable behavior, a good model should always have reasonable behavior regardless of model parameter values. Therefore for silicon devices it is recommended that $N_R = N_F$ be maintained for VBIC.

The normalized base charge is

$$\begin{aligned} q_b &= q_1 + \frac{q_2}{q_b} \\ q_1 &= 1 + \frac{q_{je}}{V_{ER}} + \frac{q_{jc}}{V_{EF}} \\ q_2 &= \frac{I_S(\exp(V_{bei}/(N_F V_{tv})) - 1)}{I_{KF}} + \frac{I_S(\exp(V_{bci}/(N_R V_{tv})) - 1)}{I_{KR}} \end{aligned} \quad (4.0-18)$$

where V_{EF} and V_{ER} are the forward and reverse Early voltages, and I_{KF} and I_{KR} are the forward and reverse knee currents. The normalized depletion charges are

$$q_{je} = q_j(V_{bei}, P_E, M_E, F_C, A_{JE}), q_{jc} = q_j(V_{bci}, P_C, M_C, F_C, A_{JC}) \quad (4.0-19)$$

where P_E and P_C are the built-in potentials and M_E and M_C are the grading coefficients of the base-emitter and base-collector junctions, respectively. The normalized depletion charge function q_j is such that

$$c_j(V, P, M, F_C, A) = \frac{\partial q_j(V, P, M, F_C, A)}{\partial V} \approx \frac{1}{(1 - V/P)^M} \quad (4.0-20)$$

for reverse and low forward bias. If the depletion capacitance smoothing parameters A_{JE} and A_{JC} are less than zero c_j smoothly limits to its value at $F_C P$, otherwise c_j linearly increases for $V > F_C P$ to match the SGP model, see [Figure 5-5](#).

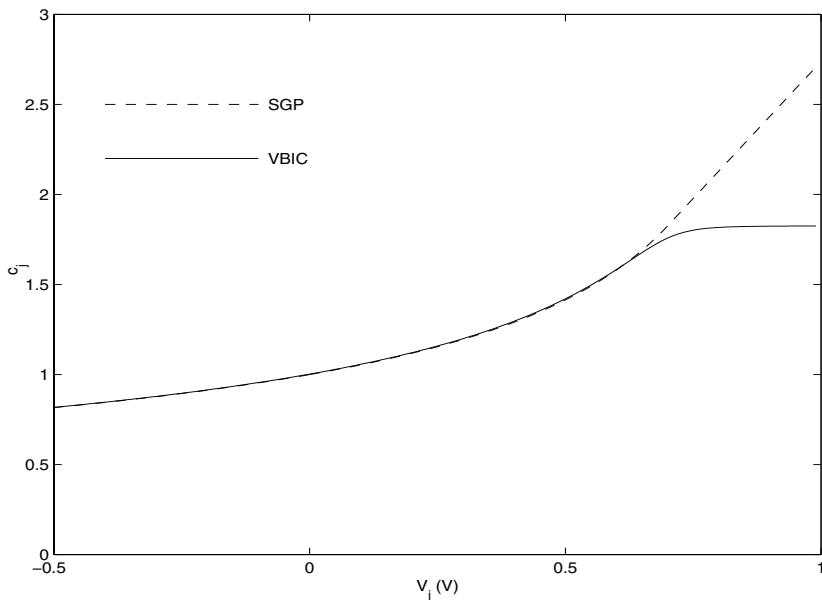


Figure 5-5. C_∞ Continuous normalized depletion capacitance model

The Early voltage components model the variation in q_b caused by changes in the depletion regions at the base-emitter and base-collector junctions, and the knee current components model the effects of high level injection. In this analysis the high level injection is considered to be in the base, whereas in normal NPNs it occurs when the base pushes out into the more lightly doped collector. This is handled in VBIC with the quasi-saturation model detailed on the following pages.

If the excess phase delay T_D is set to zero then I_{txf} in [Figure 5-3](#) is just the I_{tzf} of equation (4.0-9). If $T_D > 0$ then the capacitance and inductance of the excess phase network of [Figure 5-3](#) are set to T_D and $T_D/3$ respectively, and in the s domain the transfer function of the excess phase network is

$$V(xf2) = \frac{3I_{tzf}/T_D^2}{s^2 + 3s/T_D + 3/T_D^2} \quad (4.0-21)$$

which implements a second order polynomial approximation to ideal excess phase (Weil, 1978). The voltage on node xf2 is then directly used as I_{txf} . This implementation of excess phase is consistent between small signal and transient analyses in a circuit simulator, and is independent of the numerical algorithms within a simulator. This is an advantage over an ideal excess phase model, as used in some simulators, which can only be implemented for small signal analysis. This leads to inconsistencies between small signal and transient simulations. Further, the implementation of a direct form of equation (4.0-21) in a circuit simulator depends on the numerical integration algorithms employed (Weil, 1978), whereas the equivalent network approach does not. Note that although the excess phase network in Figure 5-3 looks like it introduces 3 extra unknowns (2 node voltages and the inductor current) into the modified nodal formulation commonly used within circuit simulators, it can actually be implemented with only 2 additional simulation variables, by taking advantage of the observation that the voltage at node xf2 is equivalent to the current in the inductor.

The intrinsic charges are

$$Q_{be} = C_{JE}W_{BE}q_{je} + \tau_F I_{tzf} \quad (4.0-22)$$

where C_{JE} is the zero bias base-emitter depletion capacitance, W_{BE} is the partitioning of the base-emitter depletion capacitance between intrinsic and extrinsic components, q_{je} is defined in equation (4.0-19). τ_F is the forward transit time, modeled as

$$\tau_F = T_F(1 + Q_{TF}q_1) \left(1 + X_{TF} \exp\left(\frac{V_{bci}}{1.44V_{TF}}\right) \left(\frac{q_b I_{tzf}}{q_b I_{tzf} + I_{TF}} \right)^2 \right) \quad (4.0-23)$$

which is the SGP model, with an additional term in q_1 added to model the change in base transit time as the base-emitter and base-collector depletion region edges move with bias. The extrinsic base-emitter charge is

$$Q_{bex} = C_{JE}(1 - W_{BE})q_j(V_{bex}, P_E, M_E, F_C, A_{JE}) \quad (4.0-24)$$

where it is apparent that $0 \leq W_{BE} \leq 1$ should hold, and V_{bex} is the extrinsic base-emitter bias, between nodes bx and ei in [Figure 5-3](#).

The intrinsic base-collector charge is

$$Q_{bc} = C_{JC}q_{jc} + T_R q_b I_{tzr} + Q_{CO}K_{bci} \quad (4.0-25)$$

where C_{JC} is the zero bias base-collector depletion capacitance, q_{jc} is defined in equation [\(4.0-19\)](#), and T_R is the reverse transit time. The term $Q_{CO}K_{bci}$ models the diffusion charge associated with base pushout into the collector, and it and a similar extrinsic term

$$Q_{bcx} = Q_{CO}K_{bcx} \quad (4.0-26)$$

will be addressed below.

The base charge appears in both the transport current model, via the normalized base charge, and explicitly in the charge elements. By comparing the equivalent terms it is apparent that

$$C_{JE}V_{ER} = C_{JC}V_{EF}(A_e/A_c) = T_F I_{KF} = T_R I_{KR} = \int_0^w p dx = Q_{b0} \quad (4.0-27)$$

should be true for the transport and charge models to be consistent (where the second term includes only the portion of C_{JC} under the emitter, because the analyses are for the 1 dimensional intrinsic transistor). The relations [\(4.0-27\)](#) are not enforced in VBIC, both for compatibility with SGP, and to allow more degrees of freedom in fitting measured device characteristics. However, these relations are important for building process and geometry level models on top of VBIC, which are required for accurate statistical BJT modeling (McAndrew, 1997).

The major difference between the above transport current formulation of VBIC and that of SGP is the Early effect modeling via the q_1 term. In SGP this is approximated by (Nagel, 1975)

$$q_1 = \frac{1}{1 - \frac{V_{bei}}{V_{AR}} - \frac{V_{bci}}{V_{AF}}} . \quad (4.0-28)$$

Equation (4.0-28) cannot model the bias dependence of output conductance well over a wide range of biases, because it has linearized the dependence of depletion charge on applied bias. Figure 5-6 compares I_e/g_o^r modeling of VBIC and SGP. SGP cannot even qualitatively model the observed trends in measured data, it has the linear variation of equation (4.0-28), whereas VBIC models the onset of a fully depleted base region well. Therefore for improved accuracy of modeling, backward compatibility of VBIC to SGP for the Early effect modeling was not maintained.

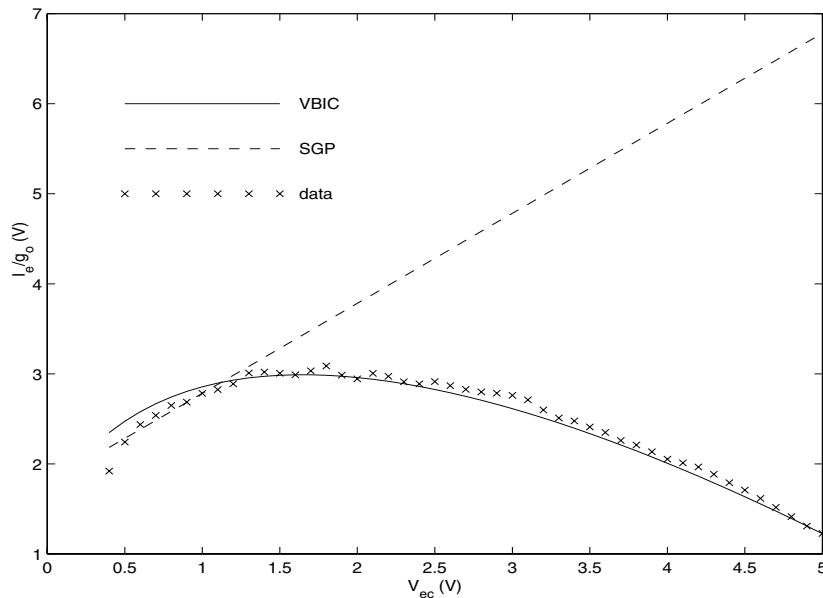


Figure 5-6. Early effect modeling of VBIC and SGP

The base current elements of VBIC model recombination and generation currents. Three mechanisms are important, Shockley-Read-Hall recombination,

$$R_{srh} = \frac{np - n_{ie}^2}{\tau_h(n + n_{ie}) + \tau_e(p + n_{ie})} , \quad (4.0-29)$$

where τ_e and τ_h are the electron and hole trapping lifetimes, respectively, Auger recombination,

$$R_{aug} = (c_e n + c_h p)(np - n_{ie}^2), \quad (4.0-30)$$

where c_e and c_h are the Auger rate constants for electrons and holes, respectively, and surface hole recombination, modeled as a recombination current density

$$J_{hec} = qS_h(p_{ec} - p_{ec0}) \quad (4.0-31)$$

where S_h is the hole surface recombination velocity at the emitter, p_{ec} is the hole concentration at the emitter contact, and p_{ec0} is the equilibrium value for p_{ec} . All analyses below are for situations well out of equilibrium, so $np \gg n_{ie}^2$.

For a shallow emitter, equating the surface recombination current density for holes to the hole diffusion current from the edge of the base gives

$$qS_h p_{ec} \approx qV_{tv}\mu_h \frac{\partial p}{\partial x} \approx qV_{tv}\mu_h \frac{n_{ie}^2 \exp(V_{bei}/V_{tv})/N_d - p_{ec}}{w_e} \quad (4.0-32)$$

where μ_h is the hole mobility, N_d is the doping density in the emitter (so the equilibrium hole concentration is nearly n_{ie}^2/N_d), and w_e is the depth of the emitter. This gives

$$p_{ec} \approx \frac{n_{ie}^2 \exp(V_{bei}/V_{tv})}{N_d(1 + S_h w_e / (V_{tv} \mu_h))} \quad (4.0-33)$$

and thus the surface recombination current is close to proportional to $\exp(V_{bei}/V_{tv})$.

For recombination in the quasi neutral emitter $n \approx N_d \gg p$, and $np \gg n_{ie}^2$, therefore

$$R_{srh} \approx \frac{p}{\tau_h}, R_{aug} \approx c_e n^2 p \quad (4.0-34)$$

and because p is proportional to $\exp(V_{bei}/V_{tv})$ the quasi neutral region recombination current is also close to proportional to $\exp(V_{bei}/V_{tv})$.

In the base-emitter space charge region there is little Auger recombination (this process involves 3 interacting mobile carriers and is only likely in regions of high carrier concentrations), so Shockley-Read-Hall recombination dominates. $\phi_e \approx 0$ and $\phi_h \approx V_{bei}$ in this region, so from equations (4.0-3), (4.0-4), and (4.0-29),

$$R_{srh} \approx \frac{n_{ie} \exp(V_{bei}/V_{tv})}{\tau_h(\exp(\psi/V_{tv}) + 1) + \tau_e(\exp((V_{bei} - \psi)/V_{tv}) + 1)} . \quad (4.0-35)$$

This rate is maximized for

$$\psi = \frac{V_{bei} - V_{tv} \log(\tau_h/\tau_e)}{2} \quad (4.0-36)$$

and for $\tau_h \approx \tau_e$ has a value

$$R_{srh} \approx \frac{n_{ie} \exp(V_{bei}/(2V_{tv}))}{\tau_h + \tau_e} . \quad (4.0-37)$$

The space charge recombination current is therefore close to proportional to $\exp(V_{bei}/(2V_{tv}))$.

Based on the above physical analyses, the base-emitter component of the intrinsic transistor base current in VBIC is modeled as

$$I_{be} = W_{BE} \left(I_{BEI} \left(\exp \left(\frac{V_{bei}}{N_{EI} V_{tv}} \right) - 1 \right) + I_{BEN} \left(\exp \left(\frac{V_{bei}}{N_{EN} V_{tv}} \right) - 1 \right) \right) \quad (4.0-38)$$

which includes both an ideal component, modeled with a saturation current I_{BEI} and ideality factor $N_{EI} \approx 1$, that comprises the emitter contact and quasi neutral region recombination, and a nonideal component for the space charge region component, modeled with saturation current I_{BEN} and ideality factor $N_{EN} \approx 2$. The ideality factors are treated as model parameters, and can be quite different from

the values of 1 or 2 for HBTs. The base-collector component is similarly modeled as

$$I_{bc} = I_{BCI} \left(\exp\left(\frac{V_{bci}}{N_{CI} V_{tv}}\right) - 1 \right) + I_{BCN} \left(\exp\left(\frac{V_{bci}}{N_{CN} V_{tv}}\right) - 1 \right) . \quad (4.0-39)$$

The extrinsic base-emitter recombination current is

$$I_{bex} = (1 - W_{BE}) \left(I_{BEI} \left(\exp\left(\frac{V_{bex}}{N_{EI} V_{tv}}\right) - 1 \right) + I_{BEN} \left(\exp\left(\frac{V_{bex}}{N_{EN} V_{tv}}\right) - 1 \right) \right) . \quad (4.0-40)$$

From the physical analyses above, it is clear that the collector current primarily depends on the base doping, and the base current depends primarily on recombination and generation in the emitter region. Consequently, very different physical mechanisms control the collector and base currents. Relating them via a phenomenological parameter such as B_F , which is done in the SGP model, is therefore undesirable, and causes problems for statistical BJT modeling (McAndrew, 1997). This is why VBIC explicitly separates the base and collector current modeling.

The weak avalanche current I_{gc} is (Kloosterman, 1988)

$$I_{gc} = (I_{tzf} - I_{tzr} - I_{bc}) A_{VC1} V_{gci} \exp(-A_{VC2} V_{gci}^{M_C - 1}) \quad (4.0-41)$$

where A_{VC1} and A_{VC2} are model parameters, and V_{gci} is $P_C - V_{bci}$ limited, in a C_∞ continuous manner, to be greater than 0.

The intrinsic base resistance R_{BI} is modulated by the normalized base charge q_b . This accounts both for the base width variation from the Early effect, and the decrease in resistivity from increased mobile carrier concentration under high level injection conditions. VBIC does not include the I_{RB} emitter crowding modulation model of SGP. This effect can be taken into account, to a first order, by using the parameter W_{BE} to partition some of the base-emitter component of base current to I_{bex} , which is “external” to R_{BI} . This does not work well over all biases, however a simple model of emitter crowding, consistent for both DC and AC modeling, has not yet been developed.

If the model is biased so that the base region becomes depleted of charge, the modulated base resistance R_{BI}/q_b can become very large. q_b is limited to a lower value of 10^{-4} in VBIC (in a C_∞ continuous manner), but this is still sufficiently small to allow the model to support an unrealistically high V_{be} during a transient simulation for a device coming out of having a depleted base region.

Multidimensional effects cause the device to turn on in a distributed manner from the edge of the emitter under such circumstances, and partitioning some of the base-emitter component of base current to I_{bex} prevents modeling the unrealistically high V_{be} values.

The parasitic transistor is modeled in a similar way to the intrinsic transistor.

$$I_{tfp} = I_{SP} \frac{W_{SP} \exp\left(\frac{V_{bep}}{N_{FP} V_{tv}}\right) + (1 - W_{SP}) \exp\left(\frac{V_{bci}}{N_{FP} V_{tv}}\right) - 1}{q_{bp}} \quad (4.0-42)$$

$$I_{trp} = I_{SP} \frac{\exp(V_{bcp}/(N_{FP} V_{tv})) - 1}{q_{bp}} \quad (4.0-43)$$

where the parasitic normalized base charge includes only a forward high level injection component,

$$q_{bp} = 1 + \frac{I_{SP} \left(W_{SP} \exp\left(\frac{V_{bep}}{N_{FP} V_{tv}}\right) + (1 - W_{SP}) \exp\left(\frac{V_{bci}}{N_{FP} V_{tv}}\right) - 1 \right)}{q_{bp} I_{KP}} \quad (4.0-44)$$

Here I_{SP} , N_{FP} , and I_{KP} are the saturation current, ideality factor, and knee current for the parasitic transistor. The biases V_{bep} and V_{bcp} are between nodes bx and bp, and si and bp, respectively. The partitioning factor W_{SP} can be used to select a base-emitter control bias for the parasitic transistor either from between nodes bx and bp, or from the base-collector of the intrinsic transistor, between nodes bi and ci, as [Figure 5-3](#) shows. The structure of a particular transistor determines which is more appropriate.

Although VBIC does not include a complete Gummel-Poon transistor for the parasitic, it does model the most important aspects of the behavior of this device. The parasitic transport current, including high level injection, models the substrate current when the intrinsic transistor goes into saturation. This is not included in the SGP model, yet is critical for accurate modeling of BJT behavior in saturation.

The other elements of the parasitic transistor model are

$$I_{bep} = I_{BEIP} \left(\exp \left(\frac{V_{bep}}{N_{CI} V_{tv}} \right) - 1 \right) + I_{BENP} \left(\exp \left(\frac{V_{bep}}{N_{CN} V_{tv}} \right) - 1 \right) , \quad (4.0-45)$$

$$I_{bcp} = I_{BCIP} \left(\exp \left(\frac{V_{bcp}}{N_{CIP} V_{tv}} \right) - 1 \right) + I_{BCNP} \left(\exp \left(\frac{V_{bcp}}{N_{CNP} V_{tv}} \right) - 1 \right) , \quad (4.0-46)$$

$$Q_{bep} = C_{JEP} q_j (V_{bep}, P_C, M_C, F_C, A_{JC}) + T_R q_{bp} I_{tfp} , \quad (4.0-47)$$

and

$$Q_{bcp} = C_{JCP} q_j (V_{bcp}, P_S, M_S, F_C, A_{JS}) . \quad (4.0-48)$$

The parasitic base-collector charge Q_{bcp} is important for modeling collector-substrate capacitance. And although it normally should be reverse biased, the parasitic base-collector base current component I_{bcp} is important for detecting any inadvertent forward biasing of the collector-substrate junction. The parasitic base-emitter components are nearly in parallel with the intrinsic base-collector components. This means that these elements could be modeled via I_{bc} and Q_{bc} , however the parasitic base-emitter elements are still useful for accurate modeling of the distributed nature of devices. The parasitic transistor modeling is completed with the modulated parasitic base resistance R_{BIP}/q_{bp} .

One of the major deficiencies of the SGP model is its lack of modeling of quasi-saturation, when the base pushes into, and modulates the conductivity of, the collector. The Kull-Nagel model (Kull, 1985) is the most widely accepted basis for quasi-saturation modeling. However, this model can exhibit a negative output conductance at high V_{be} , see [Figure 5-7](#). VBIC modifies the Kull-Nagel model to avoid the negative output conductance problem, and includes an empirical model of the increase of collector current at high bias.

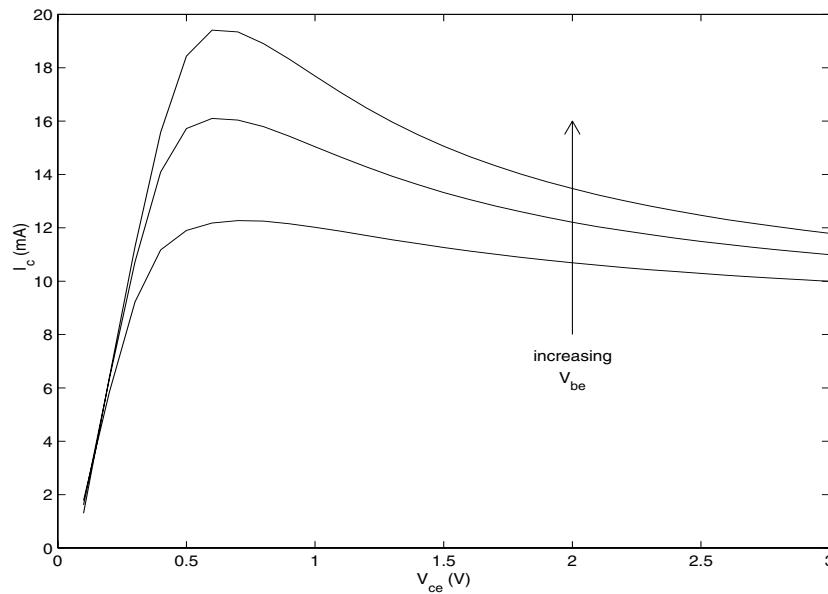


Figure 5-7. Negative output conductance from the Kull-Nagel model

Consider the lightly doped collector region between the base-collector junction x_{bc} and the highly doped buried layer x_{bl} in Figure 5-4. Integrating equation (4.0-2) across this region gives

$$J_{ex} = -\frac{q\mu_e}{x_{bl} - x_{bc}} \int_{\phi_{ec}}^{\phi_{ex}} n \, d\phi_e \quad (4.0-49)$$

where ϕ_{ex} is the electron quasi-Fermi potential at the buried layer. Quasi-neutrality in the lightly doped collector region, $n = p + N$ where N is the net doping level, gives

$$np = p(p + N) = n_{ie}^2 \exp\left(\frac{\phi_h - \phi_e}{V_{tv}}\right). \quad (4.0-50)$$

Differentiating and manipulating terms

$$(2p + N)\frac{\partial p}{\partial x} = -\frac{n_{ie}^2}{V_{tv}} \exp\left(\frac{\phi_h - \phi_e}{V_{tv}}\right) \frac{\partial \phi_e}{\partial x} = -\frac{np}{V_{tv}} \frac{\partial \phi_e}{\partial x} \quad (4.0-51)$$

and substituting equation (4.0-51) into equation (4.0-49) gives

$$J_{ex} = \frac{qV_{tv}\mu_e}{x_{bl}-x_{bc}} \int_{p_{bc}}^{p_{bl}} \left(2 + \frac{N}{p}\right) dp = \frac{qV_{tv}\mu_e}{x_{bl}-x_{bc}} \left(2(p_{bl}-p_{bc}) + N \log\left(\frac{p_{bl}}{p_{bc}}\right)\right) \quad (4.0-52)$$

where p_{bc} and p_{bl} are the mobile hole concentrations at $x = x_{bc}$ and $x = x_{bl}$, respectively. At the base-collector junction, equation (4.0-50) gives a mobile electron concentration

$$n_{bc} = \frac{N}{2} \left(1 + \sqrt{1 + \frac{4n_{ie}^2}{N^2} \exp\left(\frac{V_{bci}}{V_{tv}}\right)} \right) \quad (4.0-53)$$

and similarly at the buried layer

$$n_{bl} = \frac{N}{2} \left(1 + \sqrt{1 + \frac{4n_{ie}^2}{N^2} \exp\left(\frac{V_{bcx}}{V_{tv}}\right)} \right) \quad (4.0-54)$$

where V_{bcx} is the extrinsic base-collector bias, between nodes bi and cx of Figure 5-3. Therefore

$$p_{bl} - p_{bc} = n_{bl} - n_{bc} = \frac{N}{2} \left(\sqrt{1 + \frac{4n_{ie}^2}{N^2} \exp\left(\frac{V_{bcx}}{V_{tv}}\right)} - \sqrt{1 + \frac{4n_{ie}^2}{N^2} \exp\left(\frac{V_{bci}}{V_{tv}}\right)} \right) \quad (4.0-55)$$

and

$$\frac{p_{bl}}{p_{bc}} = \frac{n_{bc}}{n_{bl}} \exp\left(\frac{V_{bcx} - V_{bci}}{V_{tv}}\right) = \frac{\frac{1}{2} \sqrt{1 + \frac{4n_{ie}^2}{N^2} \exp\left(\frac{V_{bcx}}{V_{tv}}\right)}}{\frac{1}{2} \sqrt{1 + \frac{4n_{ie}^2}{N^2} \exp\left(\frac{V_{bci}}{V_{tv}}\right)}} \exp\left(\frac{V_{bcx} - V_{bci}}{V_{tv}}\right). \quad (4.0-56)$$

Substituting equations (4.0-55) and (4.0-56) into equation (4.0-52) gives the Kull-Nagel quasi-saturation model (without velocity saturation) for the lightly doped collector

$$I_{epi0} = \frac{V_{rci} + V_{tv} \left(K_{bci} - K_{bcx} - \log \left(\frac{K_{bci} + 1}{K_{bcx} + 1} \right) \right)}{R_{CI}} \quad (4.0-57)$$

$$K_{bci} = \sqrt{1 + G_{AMM} \exp \left(\frac{V_{bci}}{V_{tv}} \right)}, K_{bcx} = \sqrt{1 + G_{AMM} \exp \left(\frac{V_{bcx}}{V_{tv}} \right)} \quad (4.0-58)$$

where $V_{rci} = V_{bci} - V_{bcx}$ is the bias across the intrinsic collector resistance $R_{CI} = (x_{bl} - x_{bc}) / (qAN\mu_e)$ (A being the area), and $G_{AMM} = (2n_{ie}/N)^2$ is the collector doping factor parameter. VBIC models the current in the modulated resistor R_{CI} as

$$I_{rci} = \frac{I_{epi0}}{\sqrt{1 + \left(\frac{R_{CI} I_{epi0} / V_O}{1 + \sqrt{0.01 + V_{rci}^2 / (2V_O H_{RCF})}} \right)^2}}. \quad (4.0-59)$$

This accounts for velocity saturation modeled as $\mu_e = \mu_{e0} / \sqrt{1 + (\mu_{e0} \nabla \phi_e / v_{sat})^2}$ rather than the original formulation (Kull, 1985) $\mu_e = \mu_{e0} / (1 + \mu_{e0} |\nabla \phi_e| / v_{sat})$, and so avoids the discontinuity in derivative of the absolute value function. The formulation used in VBIC also avoids the negative output conductance apparent in [Figure 5-7](#), and empirically models the increase in collector with increased V_{rci} at high V_{bci} via the H_{RCF} term.

The temperature mappings of the VBIC parameters are as follows. All resistance temperature variations are modeled with the empirical mobility temperature relation (Jacoboni, 1977)

$$R(T) = R(T_{nom}) \left(\frac{T}{T_{nom}} \right)^{X_R} \quad (4.0-60)$$

with separate exponents X_R for each of the emitter, base, collector, and substrate. The temperatures here are all in degrees Kelvin. The saturation currents vary with temperature as, for example for I_S ,

$$I_S(T) = I_S(T_{nom}) \left(\left(\frac{T}{T_{nom}} \right)^{X_{IS}} \exp \left(-E_A \frac{1 - T/T_{nom}}{V_{tv}} \right) \right)^{1/N_F} \quad (4.0-61)$$

where there is a separate exponent X_{IS} and activation energy E_A for each saturation current. The built-in potential P and zero bias junction capacitance C_J parameters are modeled over temperature similarly to the SGP model, with a modification to avoid the built-in potential going negative for high temperatures (Booth, 1993),

$$P(T) = \Psi + \frac{2kT}{q} \ln \left(\frac{1 + \sqrt{1 + 4 \exp(-q\Psi/kT)}}{2} \right), \quad (4.0-62)$$

$$\begin{aligned} \Psi &= \frac{2kT}{q} \ln \left(\exp \left(\frac{qP(T_{nom})}{2kT_{nom}} \right) - \exp \left(-\frac{qP(T_{nom})}{2kT_{nom}} \right) \right) \\ &\quad - \frac{3kt}{q} \ln \left(\frac{T}{T_{nom}} \right) - E_A \left(\frac{T}{T_{nom}} - 1 \right) \end{aligned}, \quad (4.0-63)$$

$$C_J(T) = C_J(T_{nom}) \left(\frac{P(T_{nom})}{P(T)} \right)^M. \quad (4.0-64)$$

N_F , N_R and A_{VC1} are modeled as having a linear temperature dependence. The collector doping parameter G_{AMM} is modeled over temperature as in equation (4.0-61), and the collector drift saturation voltage V_O is modeled over temperature as in equation (4.0-60) (Kull, 1985).

The electrothermal modeling in VBIC follows the formulation of Vogelsong (1989) and McAndrew (1992). All of the branch constituent relations detailed above are modified to include a dependence on the local temperature rise, the voltage at the node Δt , as defined in the temperature mappings above. This greatly complicates the modeling equations, however the procedure for doing this is completely automated in VBIC, and is done using symbolic algebra software. The power dissipation I_{th} is

$$\begin{aligned} I_{th} &= I_{be} V_{bei} + I_{bex} V_{bex} + I_{bc} V_{bci} + (I_{tzf} - I_{tzr})(V_{bei} - V_{bci}) + I_{bep} V_{bep} \\ &\quad + I_{bcp} V_{bcp} + (I_{tfp} - I_{trp})(V_{bep} - V_{bcp}) + I_{rcx} V_{rcx} + I_{rci} V_{rci} \\ &\quad + I_{rbx} V_{rbx} + I_{rbi} V_{rbi} + I_{re} V_{re} + I_{rbp} V_{rbp} + I_{rs} V_{rs} - I_{gc} V_{bci} \end{aligned} \quad (4.0-65)$$

which is the sum of the products of branch currents and branch voltages over all elements of the VBIC equivalent network that do not store energy.



In the VBIC implementation of electrothermal modeling, all of the branch constituent relations defined above become significantly more complex because of the implicit dependence on the local temperature node d_t , through the model parameters which are functions of temperature. Although this results in a more complex model than if simple, first order effects were grafted on to the electrical model, it is the only way to guarantee modeling accuracy and consistency. The VBIC electrothermal code is automatically generated, with the temperature dependent parameter mappings being merged with the electrical branch constituent relations, and the derivatives being automatically generated via symbolic differentiation.

5.0 Parameter Extraction

Because of the similarity of some parts of VBIC to SGP, some parts of the parameter extraction strategy for VBIC are similar to those for SGP (Parker, 1995). However, the additional modeling features of VBIC require additional extraction algorithms, and because, unlike SGP, the DC and AC (capacitance) models are linked in VBIC through the Early effect model the extraction of the Early voltages requires the junction depletion capacitances to be modeled.

The first step in VBIC characterization (parameter determination) is therefore to extract the junction depletion capacitance parameters. This is easily done by using nonlinear least squares optimization to fit measured $C(V)$ data for each of the base-emitter, base-collector, and collector-substrate junctions. The base-collector capacitance is partitioned between C_{JC} and C_{JEP} based on the relative geometries of the intrinsic (under the emitter) and extrinsic portions of the base-collector junction.

From forward output data at low V_{be} bias and reverse output data at low V_{bc} bias the output conductances normalized by current, g_o^f/I_c and g_o^r/I_e , are calculated, and then the solution of

$$\begin{bmatrix} q_{bcf} - c_{bcf}/(g_o^f/I_c) & q_{bef} \\ q_{bcr} & q_{ber} - c_{ber}/(g_o^r/I_e) \end{bmatrix} \begin{bmatrix} 1/V_{EF} \\ 1/V_{ER} \end{bmatrix} = \begin{bmatrix} -1 \\ -1 \end{bmatrix} \quad (5.0-1)$$

gives the VBIC Early voltages (McAndrew 1996). In equation (5.0-1) $q_{bef}(V_{be}^f, P_E, M_E)$ and $q_{bcf}(V_{bc}^f, P_C, M_C)$ the normalized base-emitter and base-collector depletion charges for the forward bias case, respectively, $q_{ber}(V_{be}^r, P_E, M_E)$ and $q_{bcr}(V_{bc}^r, P_C, M_C)$ are these charges for the reverse bias case, $c_{bcf} = \partial q_{bcf} / \partial V_{bc}^f$, and $c_{ber} = \partial q_{ber} / \partial V_{be}^r$.

The saturation currents and ideality factors for the various transport and recombination/generation currents can be extracted in the usual manner from the slopes and intercepts of the variation of the logarithms of the currents as functions of the applied voltages. The data needs to be filtered to exclude high level injection and resistive debiasing effects. This is easily done by analyzing the derivative of the $\log(I)$ versus V data and excluding points that do not lie within some reasonable fraction, 5 to 10%, of its maximum value. The values obtained are then refined by optimization to fit the low bias data, both ideal and nonideal components. The activation energies for all saturation currents are determined by optimizing the fit to measured data, again filtered to keep only low biases, taken over temperature.

The knee currents can be determined as the current level at which the current gain drops to half its value.

Existing methods can be used to obtain initial values for the resistances. This can be difficult, and it is desirable to include both DC and AC data. Many of the simple procedures that have been proposed for BJT resistance calculation are based on oversimplifications of the model, and do not give realistic values. Optimization is used to refine the initial values, again preferably using DC and AC data. The quasi-saturation parameters are likewise obtained by optimization to output curves that show significant quasi-saturation effects. Other parameters, such as knee currents and Early voltages, should also be refined in this optimization.

The avalanche model parameters are optimized to fit the output conductance of data that is affected by avalanche.

Because VBIC has the same transit time model as SGP, the existing techniques for SGP transit time characterization are directly applicable to VBIC. However, the quasi-saturation model also affects high frequency modeling, via Q_{CO} , particularly where f_T falls rapidly with increasing I_c , so optimization is again used to fit the AC data.

Several techniques are available for characterizing the thermal resistance and capacitance. Physical calculation from layout can be used. However for R_{TH} if the electrical parameters are characterized at low bias and/or using pulsed measurements (Schaefer, 1996) then R_{TH} can be determined by optimizing the fit to high current data that shows significant self heating.

6.0 Relationship between SGP and VBIC Parameters

Although VBIC offers many advantages over SGP, it was intended to default to being as close to SGP as possible. The Early effect model is the principle difference in formulation between VBIC and SGP, the other features of VBIC are additions that, with the default parameters, are not active. Therefore, the easiest way to get started with VBIC is to use SGP as a base, and then incrementally include the features that are of greatest benefit for a given application. To help this [Table 5-2](#) lists simple mappings from SGP parameters to VBIC parameters.

VBIC	Mapping	VBIC	Mapping	VBIC	Mapping
R_{CX}	R_C	M_C	M_{JC}	X_{TF}	X_{TF}
R_{CI}	0	C_{JCP}	C_{JS}	V_{TF}	V_{TF}
R_{BX}	R_{BM}	P_S	V_{JS}	I_{TF}	I_{TF}
R_{BI}	$R_B - R_{BM}$	M_S	M_{JS}	T_R	T_R
R_E	R_E	I_{BEI}	I_S/B_F	T_D	$\pi T_F P_{TF} / 180$
I_S	I_S	N_{EI}	N_F	E_A	E_G
N_F	N_F	I_{BEN}	I_{SE}	E_{AIE}	E_G
N_R	N_R	N_{EN}	N_E	E_{AIC}	E_G

VBIC	Mapping	VBIC	Mapping	VBIC	Mapping
F_C	F_C	I_{BCI}	I_S/B_R	E_{ANE}	E_G
C_{JE}	C_{JE}	N_{CI}	N_R	E_{ANC}	E_G
P_E	V_{JE}	I_{BCN}	I_{SC}	X_{IS}	X_{TI}
M_E	M_{JE}	N_{CN}	N_C	X_{II}	$X_{TI} - X_{TB}$
C_{JC}	$C_{JC}X_{CJC}$	I_{KF}	I_{KF}	X_{IN}	$X_{TI} - X_{TB}$
C_{JEP}	$C_{JC}(1 - X_{CJC})$	I_{KR}	I_{KR}	K_{FN}	K_F
P_C	V_{JC}	T_F	T_F	A_{FN}	A_F

Table 5-2. Mappings from SGP to VBIC parameters

The Early voltages are the only parameters for which there is no direct mapping from SGP to VBIC. Because the Early effect models differ, the bias dependence of output conductance g_o cannot be matched between VBIC and SGP. Therefore the VBIC Early voltage parameters are derived from the SGP Early voltage parameters V_{AF} and V_{AR} by matching g_o^f/I_c and g_o^r/I_e between the two models at specific values of forward bias, V_{be}^f and V_{bc}^f , and reverse bias, V_{bc}^r and V_{be}^r (McAndrew, 1996). From the SGP model

$$\frac{g_o^f}{I_c} = \frac{1/V_{AF}}{1 - V_{be}^f/V_{AR} - V_{bc}^f/V_{AF}} \quad (6.0-1)$$

$$\frac{g_o^r}{I_e} = \frac{1/V_{AR}}{1 - V_{be}^r/V_{AR} - V_{bc}^r/V_{AF}} \quad (6.0-2)$$

are calculated, and then equation (5.0-1) is solved for V_{EF} and V_{ER} .

There is one other difference between the default parameters for VBIC and SGP. The F_C parameter, that limits how close to the built-in potential the junction voltage can go, for depletion charge and capacitance calculation, is 0.5 for SGP. This is too low and does not allow reasonable modeling of depletion capacitance into moderate forward bias. The VBIC default value is 0.9.

7.0 VBIC DC Modeling

[Figure 5-8](#) through to [Figure 5-10](#) compare DC modeling of VBIC to SGP. The improved accuracy of modeling the quasi-saturation region is apparent, as is the improved modeling of output conductance. The Early effect model, modulated collector resistance model, and weak avalanche model all contribute to the improvement in VBIC compared to SGP. [Figure 5-8](#) shows that SGP can model either the onset of quasi-saturation, with a high value of R_C , or deep saturation, with a low value of R_C , but not both.

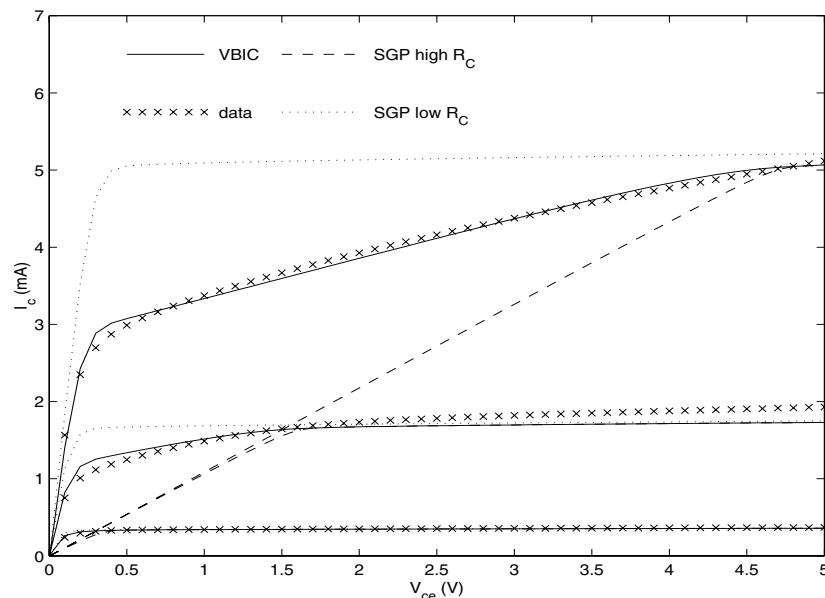


Figure 5-8. Forward output data with significant quasi-saturation

[Figure 5-9](#) and [Figure 5-10](#) show that it is important to look at g_o as well as I_c when evaluating the accuracy of a model. Apart from the quasi-saturation region in [Figure 5-9](#), it looks as if both models are reasonable. However the qualitative and quantitative shortcomings of SGP become apparent in [Figure 5-10](#), and using a logarithmic scale for g_o allows the accuracy of the models to be observed over a wide dynamic range. In addition, the output resistance $R_o = 1/g_o$ is easy to interpret from a logarithmic abscissa, because $\log(R_o) = -\log(g_o)$.

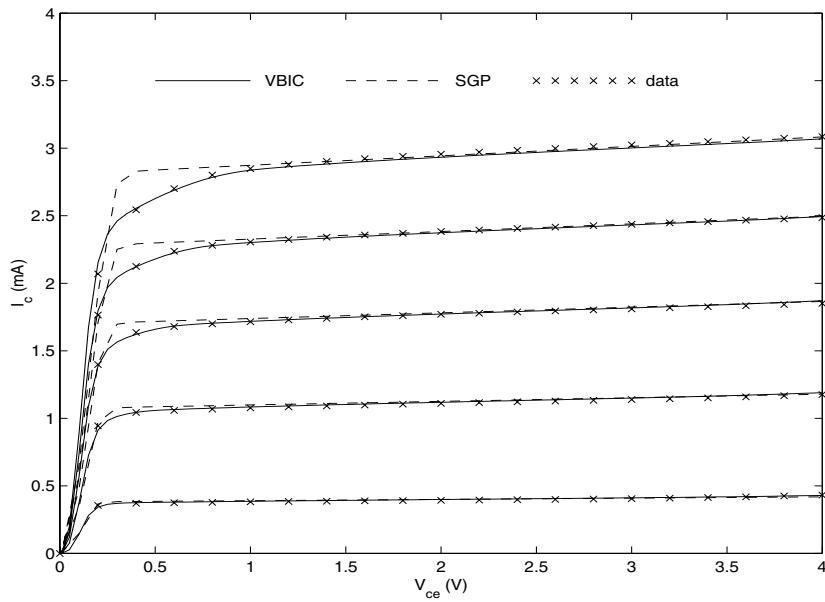


Figure 5-9. Forward output modeling comparison

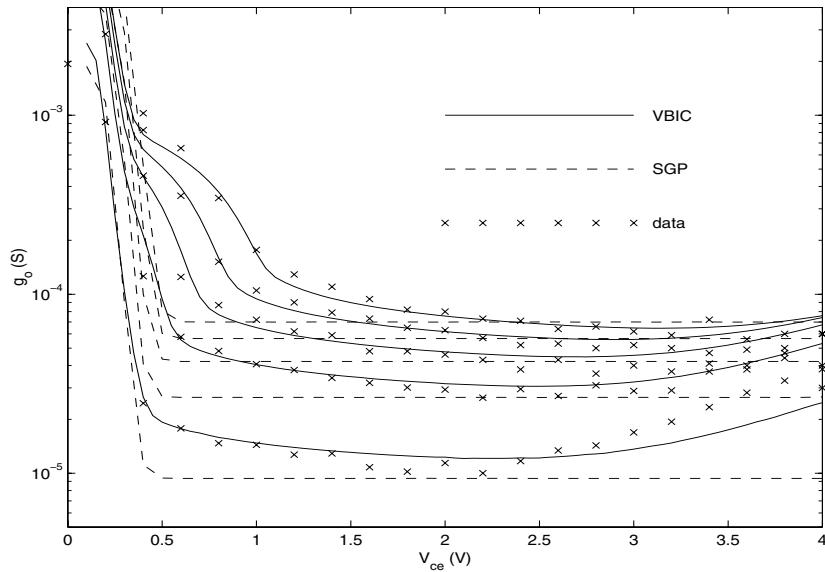


Figure 5-10. Output conductance modeling, from data of Figure 5-9

8.0 Electrothermal Examples

The coupled electrothermal (self heating) modeling capability is a major feature of VBIC. Self heating is significant for GaAs HBTs, because the thermal conductivity of GaAs is relatively low, and can also be important for silicon BJTs.

In contrast to silicon, GaAs HBTs have a negative temperature coefficient for $\beta = I_c/I_b$. This means that for a fixed base current I_b drive the collector current I_c decreases as temperature increases. [Figure 5-11](#) shows output characteristics of a GaAs HBT with I_b swept from 20 to 100 μ A in steps of 20 μ A. The main source of heating is from $I_c V_{ce}$. At low I_c and/or low V_{ce} there is little self heating, but at high I_c and V_{ce} , to the upper right in [Figure 5-11](#), there is significant self heating, which causes β and therefore I_c to decrease, which causes the output conductance g_o to become negative.

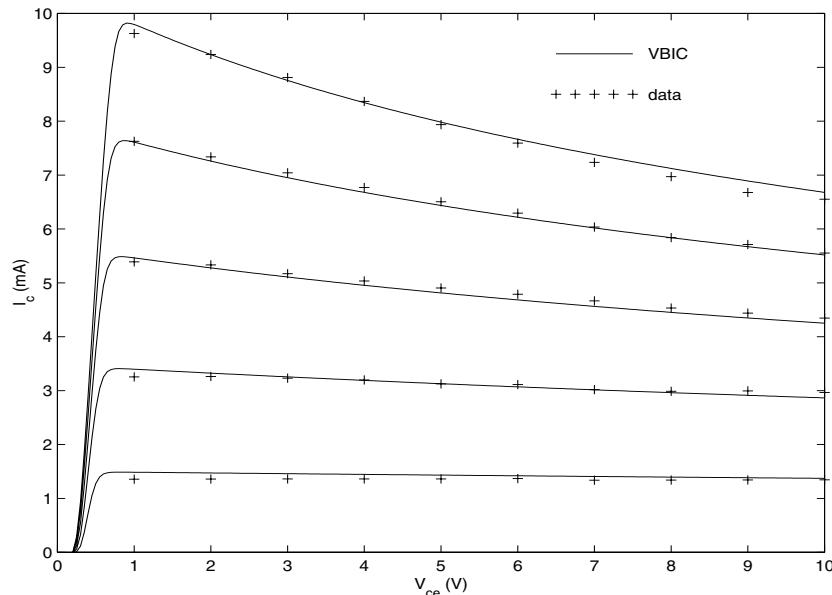


Figure 5-11. GaAs HBT electrothermal modeling with VBIC

Self heating can also cause output resistance R_o degradation in silicon BJTs.

[Figure 5-12](#) shows this degradation, and for amplifiers operated at high current densities this can cause the small signal gain to decrease by a factor of up to about

3. This significantly affects the small signal gain of amplifiers, and shows that electrothermal effects can be important for silicon BJTs.

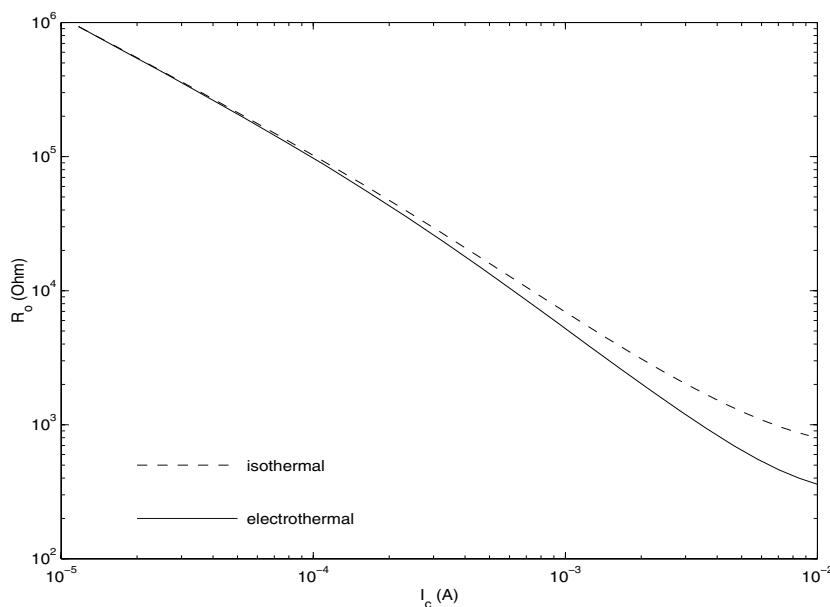


Figure 5-12. Output resistance degradation caused by self heating

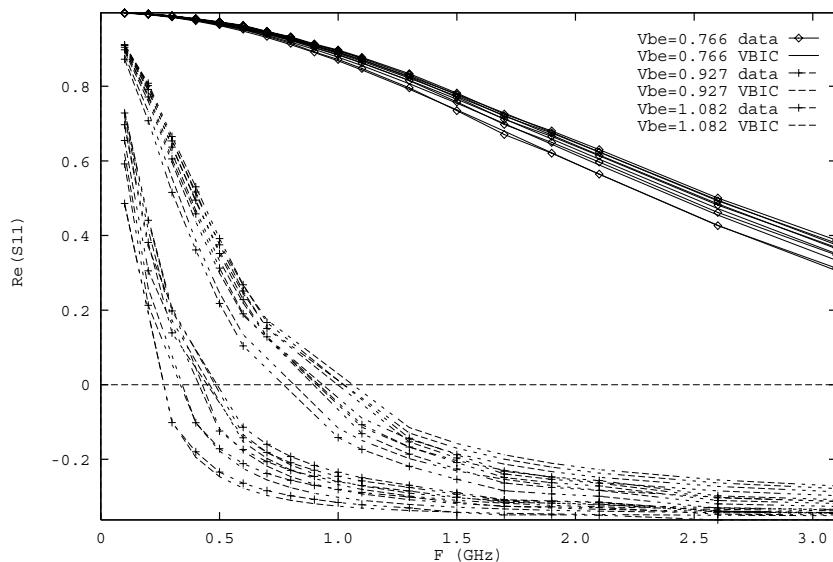
9.0 High Frequency Modeling

Although VBIC maintains, for the present, the forward transit time model of SGP, it still has improved high frequency modeling because of the improvements in other parts of the model, primarily the quasi-saturation modeling which includes additional diffusion charge modeling compared to SGP.

Figure 5-13 through to Figure 5-20 show fits of VBIC to measured s -parameter data, for the listed values of V_{be} , and V_{ce} varying from 1.0 to 3.0V in steps of 0.5V. The accuracy of VBIC is qualitatively clear, over a wide variety of different characteristics over the different biases.

Table 5-3 compares the RMS errors of the VBIC and SGP fits to the measured s -parameter data, summed over all biases and all frequencies. The models were optimized in the same optimization tool, using the same optimization strategy, to the same data. The improvement in fit is quantitatively apparent.

Parameter	SGP RMS Re error (%)	VBIC RMS Re error (%)	SGP RMS Im error (%)	VBIC RMS Im error (%)
s_{11}	99.9	7.0	65.2	6.2
s_{12}	112.6	12.0	34.6	6.9
s_{21}	209.6	14.3	81.6	8.3
s_{22}	31.3	8.5	63.8	8.5

Table 5-3. Comparison of SGP and VBIC fits to s-parameter data**Figure 5-13. VBIC modeling of the real part of s_{11}**

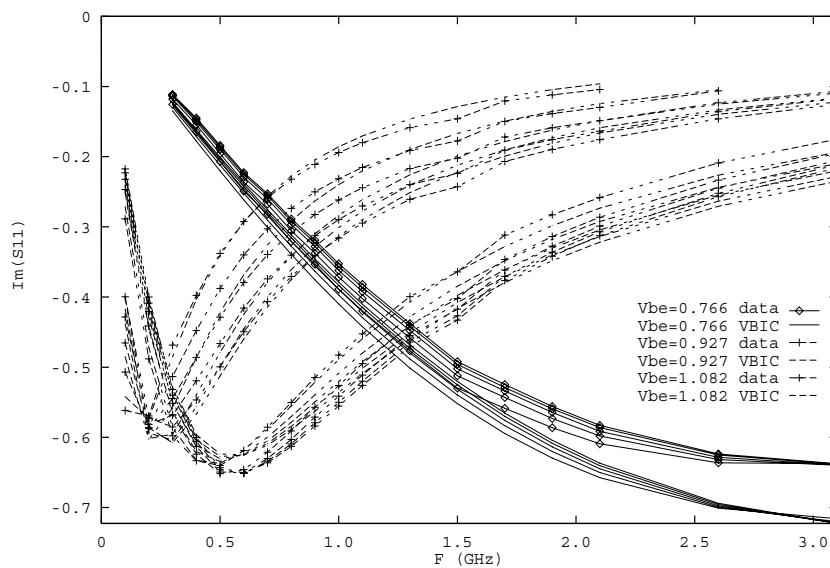


Figure 5-14. VBIC modeling of the imaginary part of s_{11}

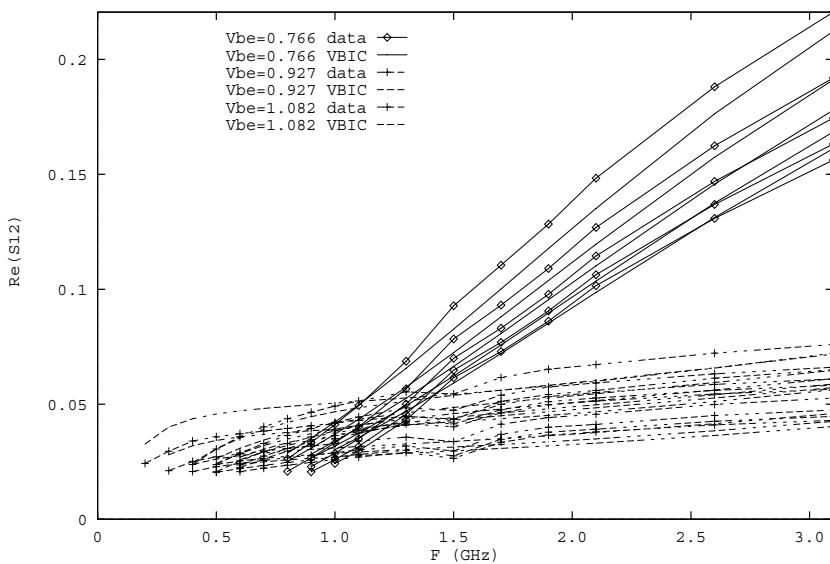


Figure 5-15. VBIC modeling of the real part of s_{12}

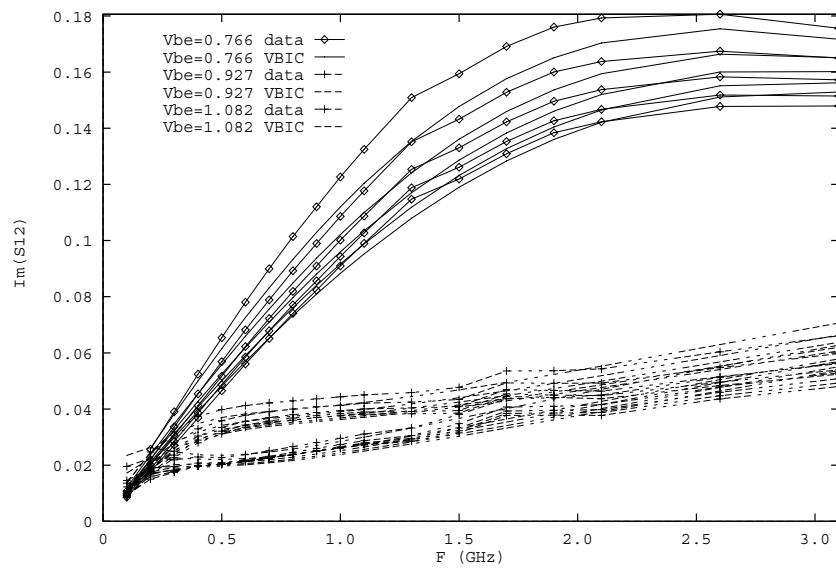


Figure 5-16. VBIC modeling of the imaginary part of s_{12}

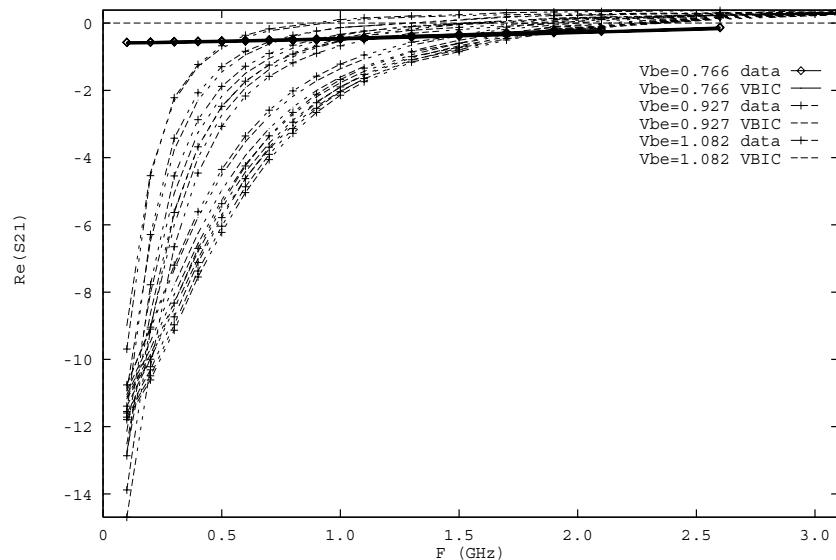


Figure 5-17. VBIC modeling of the real part of s_{21}

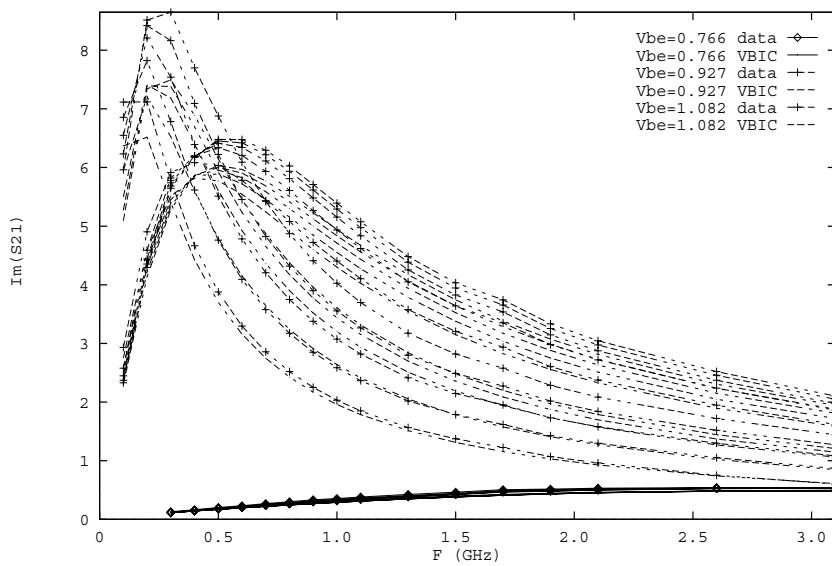


Figure 5-18. VBIC modeling of the imaginary part of s_{21}

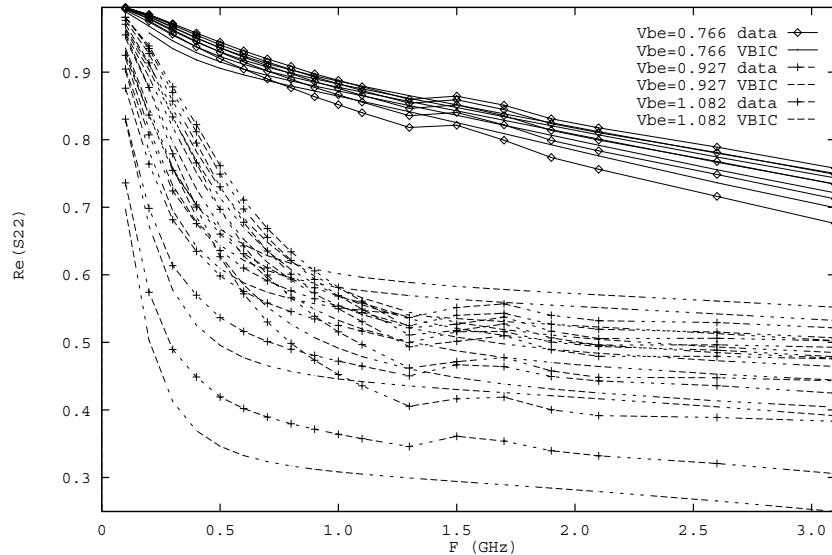


Figure 5-19. VBIC modeling of the real part of s_{22}

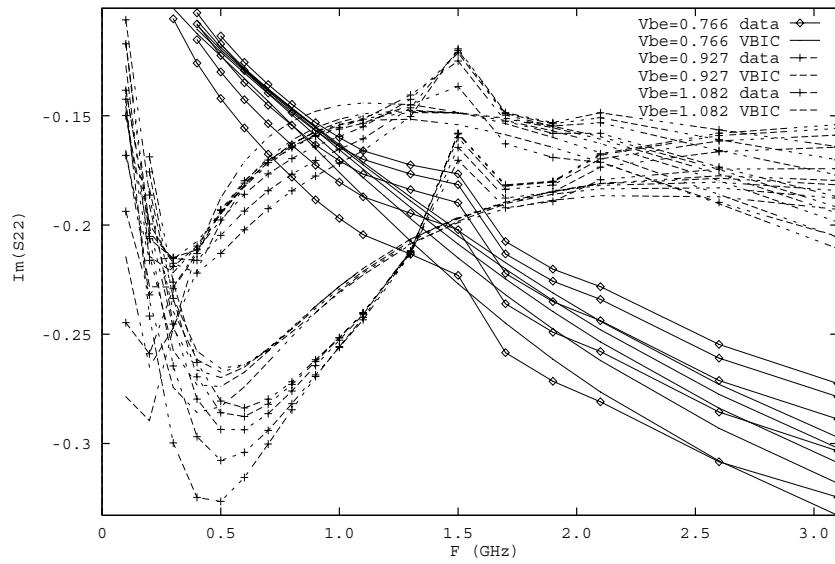


Figure 5-20. VBIC modeling of the imaginary part of s_{22}

10.0 Parameter List for v1.2

Nr.	Name	Description	Default	Units
1	TNOM	Nominal measurement temperature of parameters	27.0	°C
2	RCX	Extrinsic collector resistance	0.0	Ω
3	RCI	Intrinsic collector resistance	0.0	Ω
4	VO	epi drift saturation voltage	0.0	V
5	GAMM	epi doping parameter	0.0	
6	HRCF	High current RC factor	0.0	
7	RBX	Extrinsic base resistance	0.0	Ω
8	RBI	Intrinsic base resistance	0.0	Ω
9	RE	Extrinsic emitter resistance	0.0	Ω
10	RS	Extrinsic substrate resistance	0.0	Ω
11	RBP	Parasitic transistor base resistance	0.0	Ω
12	IS	Transport saturation current	1.0×10^{-16}	A
13	NF	Forward emission coefficient (ideality factor)	1.0	
14	NR	Reverse emission coefficient (ideality factor)	1.0	
15	FC	Forward bias depletion capacitance limit	0.9	

Nr.	Name	Description	Default	Units
16	CBEO	Extrinsic base-emitter overlap capacitance	0.0	F
17	CJE	Zero-bias base-emitter depletion capacitance	0.0	F
18	PE	Base-emitter built-in potential	0.75	V
19	ME	Base-emitter grading coefficient	0.33	
20	AJE	Base-emitter capacitance smoothing factor	-0.5	
21	CBCO	Extrinsic base-collector overlap capacitance	0.0	F
22	CJC	Zero-bias intrinsic base-collector depletion capacitance	0.0	F
23	QCO	epi charge parameter	0.0	C
24	CJEP	Zero-bias extrinsic base-collector depletion capacitance	0.0	F
25	PC	Base-collector built-in potential	0.75	V
26	MC	Base-collector grading coefficient	0.33	
27	AJC	Base-collector capacitance smoothing factor	-0.5	
28	CJCP	Zero-bias substrate-collector depletion capacitance	0.0	F
29	PS	Substrate-collector built-in potential	0.75	V
30	MS	Substrate-collector grading coefficient	0.33	
31	AJS	Substrate-collector capacitance smoothing factor	-0.5	
32	IBEI	Ideal base-emitter saturation current	1.0×10^{-18}	A
33	WBE	Partitioning of IBEI , IBEN , and CJE between Ibe/Qbe and Ibex/Qbex	1.0	
34	NEI	Ideal base-emitter emission coefficient	1.0	
35	IBEN	Non-ideal base-emitter saturation current	0.0	A
36	NEN	Non-ideal base-emitter emission coefficient	2.0	
37	IBCI	Non-ideal base-collector saturation current	1.0×10^{-16}	A
38	NCI	Ideal base-collector emission coefficient	1.0	
39	IBCN	Non-ideal base-collector saturation current	0.0	A
40	NCN	Non-ideal base-collector emission coefficient	2.0	
41	AVC1	Base-collector weak avalanche parameter 1	0.0	V^{-1}
42	AVC2	Base-collector weak avalanche parameter 2	0.0	
43	ISP	Parasitic transport saturation current	0.0	A
44	WSP	Partitioning of Iccp between Vbep and Vbci	1.0	
45	NFP	Parasitic emission coefficient (ideality factor)	1.0	
46	IBEIP	Ideal parasitic base-emitter saturation current	0.0	A
47	IBENP	Non-ideal parasitic base-emitter saturation current	0.0	A
48	IBCIP	Ideal parasitic base-collector saturation current	0.0	A

Nr.	Name	Description	Default	Units
49	NCIP	Ideal parasitic base-collector emission coefficient	1.0	
50	IBCNP	Non-ideal parasitic base-collector saturation current	0.0	A
51	NCNP	Non-ideal parasitic base-collector emission coefficient	2.0	
52	VEF	Forward Early voltage (zero means infinite)	0.0	V
53	VER	Reverse Early voltage (zero means infinite)	0.0	V
54	IKF	Forward knee current (zero means infinite)	0.0	A
55	IKR	Reverse knee current (zero means infinite)	0.0	A
56	IKP	Parasitic knee current (zero means infinite)	0.0	A
57	TF	Forward transit time	0.0	s
58	QTF	Variation of TF with base-width modulation	0.0	
59	XTF	TF bias dependence coefficient	0.0	
60	VTF	TF dependence on V _{bci} coefficient	0.0	V
61	ITF	v dependence on I _c coefficient	0.0	A
62	TR	Reverse transit time	0.0	s
63	TD	Forward excess-phase delay time	0.0	s
64	KFN	Base-emitter flicker noise constant	0.0	
65	AFN	Base-emitter flicker noise exponent	1.0	
66	BFN	Base-emitter flicker noise 1/f dependence	1.0	
67	XRE	Temperature exponent of RE	0	
68	XRBI	Temperature exponent of RBI	0	
69	XRCI	Temperature exponent of RCI	0	
70	XRS	Temperature exponent of RS	0	
71	XVO	Temperature exponent of vo	0	
72	EA	Activation energy for IS	1.12	V
73	EAIE	Activation energy for IBEI	1.12	V
74	EAIC	Activation energy for IBCI and IBEIP	1.12	V
75	EAIS	Activation energy for IBCIP	1.12	V
76	EANE	Activation energy for IBEN	1.12	V
77	EANC	Activation energy for IBCN and IBENP	1.12	V
78	EANS	Activation energy for IBENP	1.12	V
79	XIS	Temperature exponent of IS	3.0	
80	XII	Temperature exponent of IBEI , IBCI , IBEIP , IBCIP	3.0	
81	XIN	Temperature exponent of IBEN , IBCN , IBENP , IBCNP	3.0	
82	TNF	Temperature exponent of NF	0.0	°C ⁻¹
83	TAVC	Temperature exponent of AVC2	0.0	°C ⁻¹

Nr.	Name	Description	Default	Units
84	RTH	Thermal resistance	0.0	$^{\circ}\text{C}\text{W}^{-1}$
85	CTH	Thermal capacitance	0.0	$\text{J}^{\circ}\text{C}^{-1}$
86	VRT	Reach-through voltage for Cbc limiting	0.0	V
87	ART	Smoothing parameter for reach-through	0.1	
88	CCSO	Extrinsic collector-substrate overlap capacitance	0.0	F
89	QBM	Base charge model selection parameter	0.0	
90	NKF	High current beta roll-off parameter	0.5	
91	XIKF	Temperature exponent of IKF	0	
92	XRCX	Temperature exponent of RCX	0	
93	XRBX	Temperature exponent of RBX	0	
94	XRBP	Temperature exponent of RBP	0	
95	ISRR	Ratio of reverse to forward transport saturation current	1.0	
96	XISR	Temperature exponent for ISRR	0.0	
97	DEAR	Delta activation energy for ISRR	0.0	V
98	EAP	Extivation energy for ISP	1.12	V
99	VBBE	Base-emitter breakdown voltage	0.0	V
100	NBBE	Base-emitter breakdown emission coefficient	1.0	
101	IBBE	Base-emitter breakdown current	1.0×10^{-6}	A
102	TVBBe1	Linear temperature coefficient of VBBe	0.0	$^{\circ}\text{C}^{-1}$
103	TVBBe2	Quadratic temperature coefficient of VBBe	0.0	$^{\circ}\text{C}^{-2}$
104	TNBBe	Temperature coefficient of NBBE	0.0	
105	EBBE	$\exp(-\text{VBBe}/(\text{NBBE}^*Vtv))$	0.0	
106	DTEMP	Local temperature rise	0.0	$^{\circ}\text{C}$
107	VERS	Version number	1.2	
108	VREV	Revision number	0.0	

11.0 Parameter List for v1.1.5

Nr.	Name	Description	Default	Units
1	TNOM	Nominal measurement temperature of parameters	27	°C
2	RCX	Extrinsic collector resistance	0.0	Ω
3	RCI	Intrinsic collector resistance	0.0	Ω
4	VO	epi drift saturation voltage	0.0	V
5	GAMM	epi doping parameter	0.0	
6	HRCF	High current RC factor	1.0	
7	RBX	Extrinsic base resistance	0.0	Ω
8	RBI	Intrinsic base resistance	0.0	Ω
9	RE	Emit resistance	0.0	Ω
10	RS	Subs resistance	0.0	Ω
11	RBP	Parasitic base resistance	0.0	Ω
12	IS	Transport saturation current	1.0×10^{-16}	A
13	NF	Forward emission coefficient	1.0	
14	NR	Reverse emission coefficient	1.0	
15	FC	Forward bias depletion capacitance limit	0.9	
16	CBE0	Extrinsic b-e overlap capacitance	0.0	F
17	CJE	b-e zero bias capacitance	0.0	F
18	PE	b-e built-in potential	0.75	V
19	ME	b-e grading coefficient	0.33	
20	AJE	b-e capacitance smoothing factor	-0.5	
21	CBC0	Extrinsic b-c overlap capacitance	0.0	F
22	CJC	b-c intrinsic zero bias capacitance	0.0	F
23	QCO	epi charge parameter	0.0	C
24	CJEP	b-c extrinsic zero bias capacitance	0.0	F
25	PC	b-c built-in potential	0.75	V
26	MC	b-c grading coefficient	0.33	
27	AJC	b-c capacitance smoothing factor	-0.5	
28	CJCP	s-c zero bias capacitance	0.0	F
29	PS	s-c built-in potential	0.75	V
30	MS	s-c grading coefficient	0.33	
31	AJS	s-c capacitance smoothing factor	-0.5	

Nr.	Name	Description	Default	Units
32	I_{BEI}	Ideal b-e saturation current	1.0×10^{-18}	A
33	W_{BE}	Portion of I_{BEI} from V _{bei} , 1-W _{BE} from V _{bex}	1.0	
34	N_{EI}	Ideal b-e emission coefficient	1.0	
35	I_{BEN}	Non-ideal b-e saturation current	0.0	A
36	N_{EN}	Non-ideal b-e emission coefficient	2.0	
37	I_{BCI}	Ideal b-c saturation current	1.0×10^{-16}	A
38	N_{CI}	Ideal b-c emission coefficient	1.0	
39	I_{BCN}	Non-ideal b-c saturation current	0.0	A
40	N_{CN}	Non-ideal b-c emission coefficient	2.0	
41	A_{VC1}	b-c weak avalanche parameter 1	0.0	V ⁻¹
42	A_{VC2}	b-c weak avalanche parameter 2	0.0	
43	I_{SP}	Parasitic transport saturation current	0.0	A
44	W_{SP}	Portion of I_{CCP} from V _{bep} , 1-W _{SP} from V _{bci}	1.0	
45	N_{FP}	Parasitic Forward emission coefficient	1.0	
46	I_{BEIP}	Ideal parasitic b-e saturation current	0.0	A
47	I_{BENP}	Non-ideal parasitic b-e saturation current	0.0	A
48	I_{BCIP}	Idea parasitic b-c saturation current	0.0	A
49	N_{CIP}	Ideal parasitic b-c emission coefficient	1.0	
50	I_{BCNP}	Non-ideal parasitic b-c saturation current	0.0	A
51	N_{CNP}	Non-ideal parasitic b-c emission coefficient	2.0	
52	V_{EF}	Forward Early voltage, zero means infinity	0.0	V
53	V_{ER}	Reverse Early voltage, zero means infinity	0.0	V
54	I_{KF}	Forward knee current, zero means infinity	0.0	A
55	I_{KR}	Reverse knee current, zero means infinity	0.0	A
56	I_{KP}	Parasitic knee current, zero means infinity	0.0	A
57	T_F	Forward transit time	0.0	s
58	Q_{TF}	Variation of T_F with base-width modulation	0.0	
59	X_{TF}	Coefficient of T_F bias dependence	0.0	
60	V_{TF}	Coefficient of T_F dependence on V _{bc}	0.0	V
61	I_{TF}	Coefficient of T_F dependence in I _c	0.0	A
62	T_R	Reverse transit time	0.0	s
63	T_D	Forward excess-phase delay time	0.0	s
64	K_{FN}	b-e flicker noise constant	0.0	
65	A_{FN}	b-e flicker noise exponent	1.0	
66	B_{FN}	b-e flicker noise 1/f dependence	1.0	

Nr.	Name	Description	Default	Units
67	XRE	Temperature exponent of emit resistance	0.0	
68	XRB	Temperature exponent of base resistance	0.0	
69	XRC	Temperature exponent of coll resistance	0.0	
70	XRS	Temperature exponent of subs resistance	0.0	
71	XVO	Temperature exponent of vo	0.0	
72	EA	Activation energy for IS	1.12	V
73	EAIE	Activation energy for IBEI	1.12	V
74	EAIC	Activation energy for IBCI/IBEIP	1.12	V
75	EAIS	Activation energy for IBCIP	1.12	V
76	EANE	Activation energy for IBEN	1.12	V
77	EANC	Activation energy for IBCN/IBENP	1.12	V
78	EANS	Activation energy for IBCP	1.12	V
79	XIS	Temperature exponent of IS	3.0	
80	XII	Temperature exponent of IBEI, IBCI, IBEIP, IBCIP	3.0	
81	XIN	Temperature exponent of IBEN, IBCN, IBENP, IBCNP	3.0	
82	TNF	Temperature coefficient of NF	0.0	$^{\circ}\text{C}^{-1}$
83	TAVC	Temperature coefficient of AVC2	0.0	$^{\circ}\text{C}^{-1}$
84	RTH	Thermal resistance	0.0	$^{\circ}\text{CW}^{-1}$
85	CTH	Thermal capacitance	0.0	$\text{J}^{\circ}\text{C}^{-1}$

11.1 Parameter aliases

This section lists parameter aliases, primarily for parameters that contain the number 0 (zero) or the letter O.

TNOM **TN0M, TREF**

VO **V0**

CBE0 **CBE0**

CBC0 **CBC0**

QCO **QC0**

XVO **XV0**

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Chapter 6

HICUM Equations

1.0 Introduction

HICUM (HIgh CUrrent bipolar compact transistor Model) is an advanced transistor model for bipolar transistors with main emphasis on circuit design for high-speed applications. The model has been developed and continuously improved for about 15 years. Work started about 1982 at Ruhr-University Bochum, Germany, with major emphasis on high-speed ECL-type circuits for fibre-optic applications. The model has been extended to high-speed small-signal applications since 1989 as well as to SiGe HBTs since 1993.

HICUM development resulted from the experience that the SPICE Gummel-Poon model (SGPM) is not accurate enough for high-speed large-signal transient applications and the required high collector current densities. Other major disadvantages of the SGPM are lack of sufficient physical background, poor description of base resistance and (quasi-)saturation effects.

Major features of HICUM (and advantages over the SGPM) are:

- Accurate description of the high-current operating region (including quasi-saturation and saturation).
- Distributed modelling of external base-collector region.
- Emitter periphery injection and charge storage is taken into account.
- Internal base resistance is dependent on operating point (conductivity modulation AND emitter current crowding), as well as emitter geometry.
- Sufficiently physical model equations allowing predictions of temperature and process variations as well as scalability even at high current densities.

- Parasitic capacitances, independent on operating point, are available in the equivalent circuit, representing base-emitter and base-collector oxide overlaps, that become significant for small-size transistors.
- Weak avalanche breakdown is available.
- Self-heating effects can be simulated for d.c., AC and transient operation.
- Non-quasi-static effects, resulting in a delay of collector current AND stored minority charge, are modelled consistently as function of bias for small-signal and large-signal operation.
- Collector current spreading is included in minority charge and collector current formulation.
- Extensions for graded-base SiGe HBTs have been derived using the Generalized Integral Charge-Control Relation (GICCR); the GICCR also permits modelling of HBTs with bandgap difference within the junction, as long as thermionic emission can be neglected.
- Base-emitter tunneling model is available (used for reverse bias leakage current simulation).
- Simple parasitic substrate transistor is included in the equivalent circuit.
- Sufficiently simple parallel RC network taking into account the frequency dependent coupling between collector and substrate terminal.
- Parameter extraction is closely related to the process enabling parametric yield simulation; parameter extraction procedure and list of test structures are available; HICUM parameters can be determined using standard measurement equipment and mostly simple extraction procedures.
- Simple equivalent circuit and numerical formulation of model equations result in easy implementation and relatively fast execution time.

These features together with the choice of easily measurable capacitances and transit time yield high accuracy, compared to the SGPM, for d.c., small-signal high-frequency and, in particular, high-speed large-signal transient simulation.

Also, HICUM is laterally scaleable up to high collector current densities; the scaling algorithm is generic and has been applied to the SGPM (at low current densities) already by several companies.

1.1 Version selection

When the model parameter **VERSION** is set to a value of 2.1 or higher, some new equations are used. When set to less than 2.1, the old equations are used. Details can be found where applicable within the chapter.

Parameter Value	HICUM Version
VERSION=2.1	HICUM 2.1 (Default)
VERSION<2.1	HICUM previous versions

2.0 Equivalent Circuit

Compared to the SGPM the equivalent circuit (EC) of HICUM/Level2 contains two additional circuit nodes, namely B^* and S' in [Figure 6-1](#). The node B^* , which separates the operating point dependent internal base resistance from the operating point independent external component, is required to take into account emitter periphery effects, which can play a significant role in modern transistors. This node is also employed for an improved modelling of the distributed nature of the external base-collector (BC) region by splitting the external BC capacitance C_{BCx} over r_{Bx} in form of a π -type equivalent circuit for the corresponding RC transmission line(s). As a further advantage of introducing the node B^* , high-frequency small-signal emitter current crowding can be correctly taken into account by the capacitance C_{rBi} . An emitter oxide capacitance C_{Eox} , that becomes significant for advanced base-emitter (BE) self-aligning technologies, and a BC oxide capacitance C_{Cox} , which is included in the C_{BCx} element, is taken into account, too, compared to the SGPM.

In contrast to other models, the influence of the internal collector series resistance is (partially) taken into account by the model equations for the transfer current i_T and the minority charge which is represented by the elements C_{dE} and C_{dC} in [Figure 6-1](#). As a consequence, the collector terminal C' of the internal transistor is

(physically) located at the end of the epitaxial (or n-well) collector region. This approach not only avoids additional complicated and computationally expensive model equations for an “internal collector resistance” but also saves one node. The chosen approach has been demonstrated to be accurate for a wide range of existing bipolar technologies.

The reliable design of high-speed circuits often requires the consideration of the coupling between the buried layer and the substrate terminal S. Since the substrate material consists of both a resistive and capacitive component, as a first (rough) approach a substrate network with a resistance r_{Su} and a capacitance C_{Su} is introduced, leading to the “internal” substrate node S*.

A possibly existing substrate transistor has been taken into account by using a simple transport model. As in the SGPM, this can also be realized by a subcircuit (Section 13.0) and setting r_{Su} and C_{js} to zero in the HICUM equivalent circuit. In advanced bipolar processes, the emitter terminal of the substrate transistor (B*) moves towards the (npn) base contact (B) which makes the external realization of such a parasitic transistor by a subcircuit even easier. The substrate transistor—if it is not avoided by proper layout measures—only might turn on for operation at very low CE voltages (“very” hard saturation).

The physical meaning and modelling of all EC elements in [Figure 6-1](#) is discussed below in more detail.

The description in the following text is given for a npn transistor, which is mostly used type of bipolar transistors. For vertical pnp transistors, the model can be applied by interchanging the signs of terminal voltages and currents. Lateral pnp transistors could be described by a composition of HICUM/L2 models but usually a subcircuit consisting of three simple transport models (e.g. HICUM/0) is considered to be more appropriate.

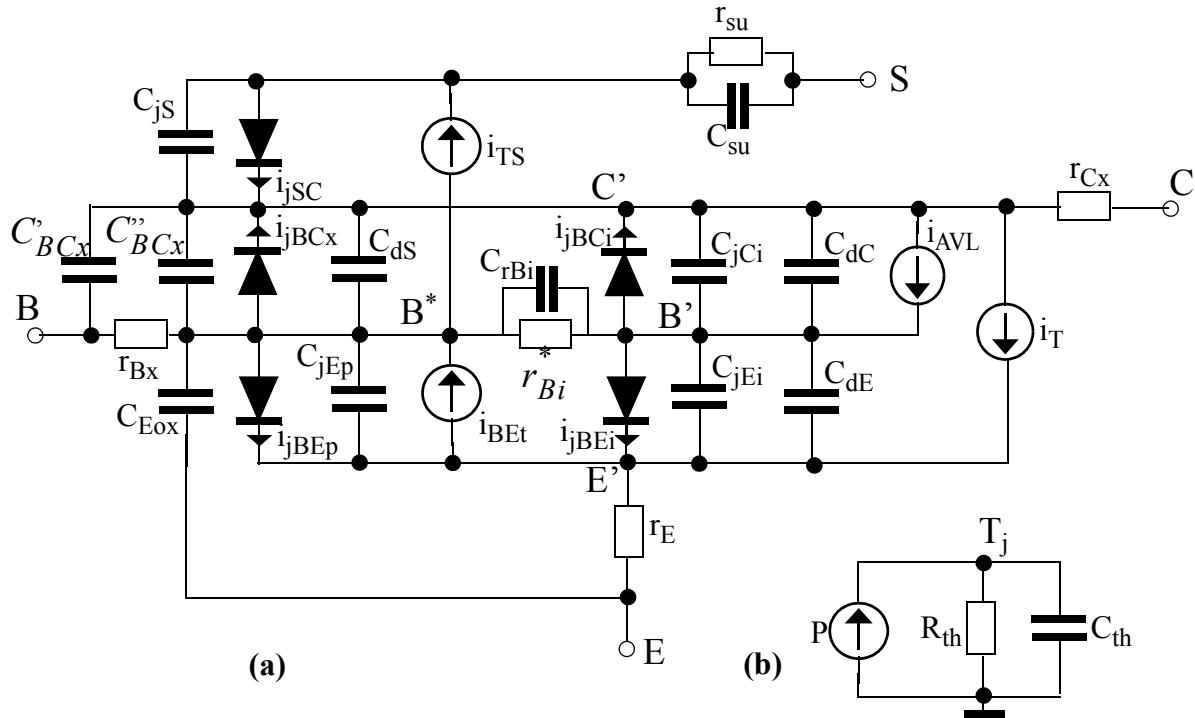


Figure 6-1. (a) Large-signal HICUM/Level2 equivalent circuit. The external BC capacitance consists of a depletion and a bias independent (e.g. oxide) capacitance with the ratio C_{BCx}/C''_{BCx} being adjusted with respect to proper modelling of the h.f. behavior.
(b) Thermal network used for self-heating calculation.

3.0 Quasi-Static Transfer Current

The transfer current of a vertical homo- and hetero-junction transistor can be described by a generalized form of the ICCR that can also be extended to 2D and 3D transistor structures with narrow emitter stripes or very small contact windows. The various steps to arrive at the final equation for the transfer current i_T are outlined below, demonstrating the modular structure of the model equations.

3.1 Basic formulation

The result of the one-dimensional (1D) GICCR is:

For Version < v2.1

$$i_T = \frac{c_{10}}{Q_{p,T}} \left[\exp\left(\frac{v_{B'E'}}{V_T}\right) - \exp\left(\frac{v_{B'C'}}{V_T}\right) \right] \quad (3.1-1)$$

For Version ≥ v2.1

$$i_T = \frac{c_{10}}{Q_{p,T}} \left[\exp\left(\frac{v_{B'E'}}{V_T \cdot MCF}\right) - \exp\left(\frac{v_{B'C'}}{V_T \cdot MCF}\right) \right] \quad (3.1-2)$$

with the constant:

$$c_{10} = (qA_E)^2 V_T \overline{\mu_{nB} n_{iB}^2} \quad (3.1-3)$$

$v_{B'E'}$ and $v_{B'C'}$ are the terminal voltages of the 1D transistor if the integration leading to the modified hole charge, $Q_{p,T}$, is performed throughout the total 1D transistor, i.e. between its emitter and collector contact. $\overline{\mu_{nB} n_{iB}^2}$ is an average value for the base region.

$Q_{p,T}$ consists of a weighted sum of charges

$$Q_{p,T} = Q_{p0} + h_{jEi} Q_{jEi} + h_{jCi} Q_{jCi} + Q_{f,T} + Q_{r,T} \quad (3.1-4)$$

The hole charge at thermal equilibrium, Q_{p0} , is a model parameter. Q_{jEi} and Q_{jCi} are the depletion charges stored within the BE and BC junction. $Q_{f,T}$ and $Q_{r,T}$ are (weighed) minority charges stored in the total (1D) transistor [41]. The various components in the minority charges and the weighting factors will be discussed in more detail below.

3.2 Extension to the 2D (3D) case and influence of internal base resistance

The 1D transistor structure can be transformed into a 2D or 3D structure by multiplying all area specific 1D model parameters with the emitter area of the

transistor. This defines the internal transistor, i.e. the structure under the emitter window. As a result, the lateral voltage drop caused by the base current has to be taken into account for calculating $v_{B'E'}$ and $v_{B'C'}$ in (3.1-1). This requires an appropriate definition and model for the internal base resistance by which then $v_{B'E'}$ and $v_{B'C'}$ are becoming “averaged” terminal voltages to ensure a correct description of the electrical (terminal) characteristics of the internal transistor.

3.3 Emitter periphery injection

The carrier injection at the emitter periphery junction and the corresponding transfer current component through the external base can be taken into account by defining an effective electrical emitter width b_E and length l_E [25], [27], [44], which are usually larger than the emitter window dimensions. This results in an effective size for the internal transistor in the 2D and 3D case with the effective emitter area A_E . By multiplication of all area specific 1D model parameters with A_E (rather than A_{E0}) it was shown in [44], that (3.1-1) can then be directly applied without any loss of accuracy at low current densities. At high current densities, however, this approach can become less accurate, and another extension is usually required which will be discussed later. $v_{B'E'}$ and $v_{B'C'}$ are now the terminal voltages of the effective internal transistor (Figure 6-1), and the components Q_{jEi} and Q_{jCi} in the charge $Q_{p,T}$ are now defined for the effective internal transistor.

Besides lateral scalability of the model, the major advantages of this approach are that (i) a single equation can be used throughout the total operating region and (ii) a single transfer current source element can be used in the EC (Figure 6-1) to describe even transistors with strong 2D and 3D effects.

3.4 Heterojunction bipolar transistors (HBTs)

The generalized ICCR [41] results in the following expression for the weighed minority charge:

$$Q_{f,T} = h_{fE}Q_{fE} + Q_{fB} + h_{fC}Q_{fC} \quad (3.4-1)$$

with Q_{fE} , Q_{fB} as the actual minority charges in the emitter and base, respectively. $Q_{fC,T}$ is a collector minority charge that includes a bias dependent weighting

function due to lateral current spreading (see later). The weighing factors h_{fE} and h_{fC} as well as h_{jEi} and h_{jCi} in (3.1-4) are given by the differences and grading of the bandgap between the various transistor regions in a HBT.

Assuming a linearly graded bandgap in the base, the model parameter h_{jCi} can be expressed analytically as a function of the grading coefficient a_G [52]:

$$h_{jCi} \approx \exp\left(-\frac{a_G w_{B0}}{V_T}\right) \quad (3.4-2)$$

with w_{B0} as the neutral base width in equilibrium. The corresponding factor for the BE charge, h_{jEi} , can be set to 1 for present Si-based processes and is therefore omitted in the following text for the time being.

The weighting factors [41]:

$$h_{fE} = \frac{\overline{\mu_{nB} n_{iB}^2}}{\overline{\mu_{nE} n_{iE}^2}} \quad \text{and} \quad h_{fC} = \frac{\overline{\mu_{nB} n_{iB}^2}}{\overline{\mu_{nC} n_{iC}^2}} \quad (3.4-3)$$

are model parameters that take into account the different values for effective intrinsic carrier concentration n_i and mobility μ_n of the neutral transistor regions. h_{jCi} , h_{fE} , and h_{fC} are considered to be model parameters in order to make the model applicable also in cases where the doping and physical values are unknown.

For SiGe heterojunction transistors, h_{fC} can be significantly larger than 1 while h_{jCi} is less than 1 explaining the larger Early voltages measured in those transistors. In contrast, for most homojunction transistors these parameters assume values close to 1 although they are becoming more relevant, too, in advanced homojunction transistors due to high-doping effects.

For HBTs, such as those fabricated in III-V semiconductors, that contain a significant energy difference in the conduction band, also thermionic emission and even tunneling may have to be accounted for.

3.5 High current densities

Earlier investigations of a variety of doping profiles have shown that (3.1-1) becomes less accurate at high collector current densities due to current spreading in the epitaxial collector [35], i.e. if J_{nx} becomes spatially dependent. This 2D/3D effect can be taken into account according to the derivation of the ICCR, by evaluating the weighting function:

$$h_{jn} = \frac{|J_{nx}|}{I_T/A_E} \quad (3.5-1)$$

in the integrand for the 2D and 3D case. (J_{nx} is the vertical electron current density). The consequence is a modified collector charge $Q_{fC,T}$ that has to be inserted into the ICCR instead of the actual charge Q_{fC} that is given 6-12.

Applying the same methodology as described in [44], the following expression can be derived for the 2D case ($l_E \gg b_E$):

$$Q_{fC,T} = 2\tau_{pCs} I_T w^2 \frac{\zeta_b w - \ln(1 + \zeta_b w)}{\zeta_b^2} \quad (3.5-2)$$

with w ($=w_i/w_C$) as normalized bias dependent injection width (6-12). In the model implementation, the calculation of this term can be combined efficiently with the calculation of Q_{fC} . At high current densities, in the presence of current spreading, the ratio:

$$\frac{Q_{fC,T}}{Q_{fC}} = h_{jn}(I_T, V_{CE}, b_E, l_E) = 4 \frac{\zeta_b w - \ln(1 + \zeta_b w)}{(1 + \zeta_b w)^2 - 1 - 2 \ln(1 + \zeta_b w)} \quad (3.5-3)$$

becomes less than one. This leads to an increase in the transfer current for the 2D case compared to the 1D case, which has been also observed by device simulation [44] and experimentally [[27], [35]]. The previously described version of HICUM contains a simplified modelling of this effect by replacing the constant c_{10} by the empirical function $c_1 = c_{10} (1 + i_T/I_{Ch})$ [35] with I_{Ch} as a model parameter. In the

present version, the simplified description is still maintained, but a numerically more stable expression is being used:

$$c_1 = c_{10} \left(1 + \frac{i_{Tf}}{I_{Ch}} \right) \quad (3.5-4)$$

The value of I_{Ch} is (roughly) proportional to the emitter area.

For $Q_{r,T}$ the actual charge Q_r is being used.

3.6 Final transfer current model formulation

Mathematically, i_T in (3.1-1) can be split into a “forward” component:

For Version < v2.1

$$i_{Tf} = \frac{c_1}{Q_{p,T}} \exp\left(\frac{V_{B'E'}}{V_T}\right) \quad (3.6-1)$$

For Version ≥ v2.1

$$i_{Tf} = \frac{c_1}{Q_{p,T}} \exp\left(\frac{V_{B'E'}}{V_T \cdot MCF}\right) \quad (3.6-2)$$

and a “reverse” (better: inverse) component:

$$i_{Tr} = \frac{c_{10}}{Q_{p,T}} \exp\left(\frac{V_{B'C}}{V_T}\right) \quad (3.6-3)$$

in which the influence of the collector current spreading at forward operation has been dropped, i.e. $c_1=c_{10}$. Physically, i_{Tf} represents the electron current flowing from emitter to collector at forward operation at $\exp(V_{C'E'}/V_T) \gg 1$.

Analogously, i_{Tr} represents the electron current flowing from collector to emitter at inverse operation with $\exp(-V_{C'E'}/V_T) \gg 1$. This separation of i_T simplifies

both the implementation of the solution of the non-linear transfer current formulation as well as the modelling of the minority charge components.

(3.6-1) can be re-arranged to give an explicit expression for:

$$i_{Tf} = i_{Tf1} \left(1 + \frac{i_{Tf1}}{I_{Ch}} \right) \quad (3.6-4)$$

as function of $Q_{p,T}$ and a 1D current component:

For Version < v2.1

$$i_{Tf1} = \frac{c_{10}}{Q_{p,T}} \exp\left(\frac{v_{BE}}{V_T}\right) \quad (3.6-5)$$

For Version ≥ v2.1

$$i_{Tf1} = \frac{c_{10}}{Q_{p,T}} \exp\left(\frac{v_{BE}}{V_T \cdot MCF}\right) \quad (3.6-6)$$

The present non-symmetry between the formulations for i_{Tf} and i_{Tr} can be eliminated by using (3.5-2) which would also eliminate the parameter I_{Ch} .

In general, the ICCR is a non-linear implicit equation for either i_T or $Q_{p,T}$, respectively. Since $Q_{p,T}$ is the common variable in both current components i_{Tf} and i_{Tr} , the ICCR is solved in HICUM for $Q_{p,T}$ by employing Newton-Raphson iteration¹. However, as long as $Q_{f,T}$ and Q_r are linearly varying functions of the respective current, i.e. the transit times are current *independent*, the ICCR reduces to a quadratic equation, with an explicit solution for $Q_{p,T}$ (assuming $c_1 = c_{10}$ at low current densities):

1. In the SGPM, the solution is obtained by significant simplifications of the minority charge terms, leading to an (explicit) quadratic equation. Such an approach is valid only at low current densities without simplification.

For Version $\geq v2.1$

$$Q_{p,T} = \frac{Q_{p,low}}{2} + \sqrt{\left(\frac{Q_{p,low}}{2}\right)^2 + \tau_{f0}c_{10}\exp\left(\frac{v_{B'E}}{V_T}\right) + \tau_r c_{10}\exp\left(\frac{v_{B'C}}{V_T}\right)} \quad (3.6-7)$$

For Version $\geq v2.1$

$$Q_{p,T} = \frac{Q_{p,low}}{2} + \sqrt{\left(\frac{Q_{p,low}}{2}\right)^2 + \tau_{f0}c_{10}\exp\left(\frac{v_{B'E}}{V_T \cdot MCF}\right) + \tau_r c_{10}\exp\left(\frac{v_{B'C}}{V_T}\right)} \quad (3.6-8)$$

with the hole charge at low current densities:

$$Q_{p,low} = Q_{p0} + Q_{jEi} + h_{jCi}Q_{jCi} \quad (3.6-9)$$

Inserting the above solution into i_{Tf} and i_{Tr} and adding the minority charge terms provides quite a useful initial guess for the Newton iteration at higher current densities:

$$Q_{p,T,initial} = Q_{p,low} + \tau_{f0}i_{Tf} + \tau_r i_{Tr} \quad (3.6-10)$$

As a comment on the ICCR formulation in HICUM, note that the usual saturation current is simply given by:

$$I_S = \frac{c_{10}}{Q_{p0}} \quad (3.6-11)$$

4.0 Minority Charge, Transit Times, and Diffusion Capacitances

The minority charge is divided into a “forward” and a “reverse” (or inverse) component. The forward component, Q_f , is considered to be dependent on the forward transfer current, i_{Tf} , while the reverse component, Q_r , is considered to be dependent on the reverse transfer current, i_{Tr} . The large-signal charge components

can be determined by integrating the respective small-signal transit times, defined as:

$$\tau = \frac{dQ}{dI} \quad (4.0-1)$$

rather than $t = Q/I$.

4.1 Base-emitter voltage controlled minority charge

The operating point dependent minority charge stored in a forward biased (vertical) transistor can be determined from the transit time t_f by simple integration:

$$Q_f = \int_0^{i_{Tf}} \tau_f di \quad (4.1-1)$$

t_f can be extracted from the measured transit frequency vs. d.c. collector current $I_C (=I_T)$ at forward operation for different voltages v_{CE} or v_{BC} as a parameter ([24] and 6-12). The current and voltage dependent transit time is modelled in HICUM by two components:

$$\tau_f(v_{CE}, i_{Tf}) = \tau_{f0} + \Delta\tau_f \quad (4.1-2)$$

where τ_{f0} is the low-current transit time, and $\Delta\tau_f$ represents the increase of the transit time at high collector current densities. Figure 6-2 shows the typically observed behavior of t_f and its various components, for which physics-based equations will be given later in this section. It is important to note, that the sum of all physically (from carrier densities) calculated storage times, $t_{m\Sigma}$, equals the transit time t_f , that is extracted from small-signal results using the measurement method.

The minority charge model in HICUM uses an “effective” collector voltage:

$$v_{ceff} = V_T \left[\ln \left(1 + \exp \left(\frac{v_c - V_T}{V_T} \right) \right) + 1 \right] \quad (4.1-3)$$

with:

$$v_c = v_{CE} - V_{CEs} \approx V_{DCi} - v_{B'C} \quad (4.1-4)$$

The internal CE saturation voltage $V_{C'E's}$ ($\approx V_{DEi} - V_{DCi}$) is a model parameter. The smoothing function for v_{ceff} has been implemented in order to provide a smooth behavior of the critical current (see later) and the forward minority charge for small and negative values of v_c .

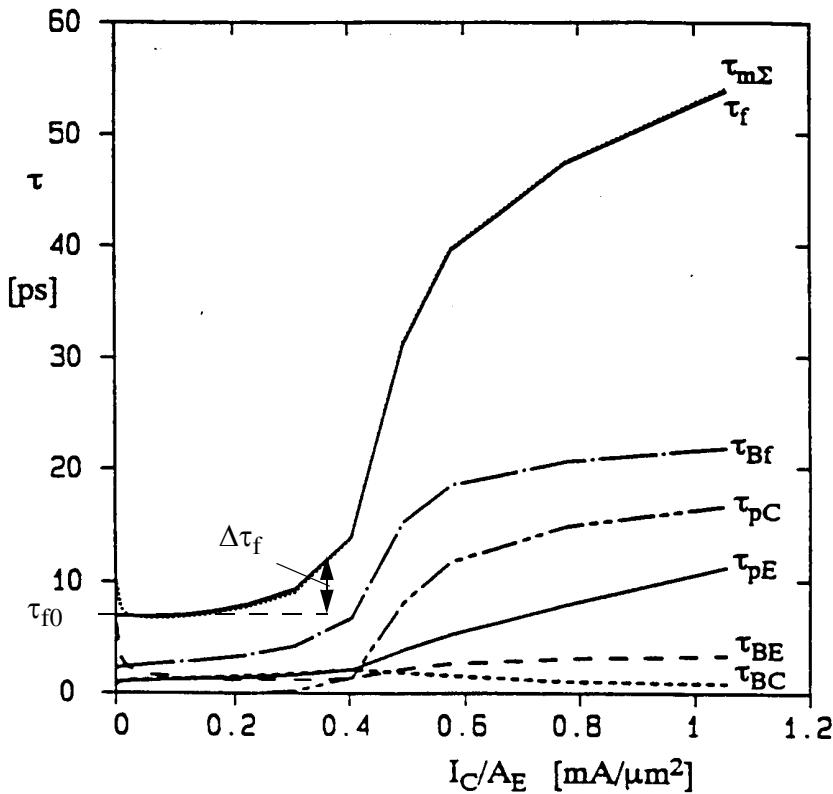


Figure 6-2. Charge storage and transit time components vs. collector current density. The components τ_{Bf} , τ_{pc} , τ_{pe} , τ_{BE} , τ_{BC} , and $\tau_{m\Sigma}$ were calculated from 1D device simulation, while τ_B was extracted from small-signal simulations and f_T using the measurement method.

As Figure 6-3 shows, v_{ceff} is equal to v_c for values larger than about $2V_{C'E's}$ and approaches the thermal voltage V_T as the limit for negative values.

The transit time and minority charge model used in HICUM and its derivation are discussed in detail in [47]. In this text, the most important equations and their physical meaning are summarized.

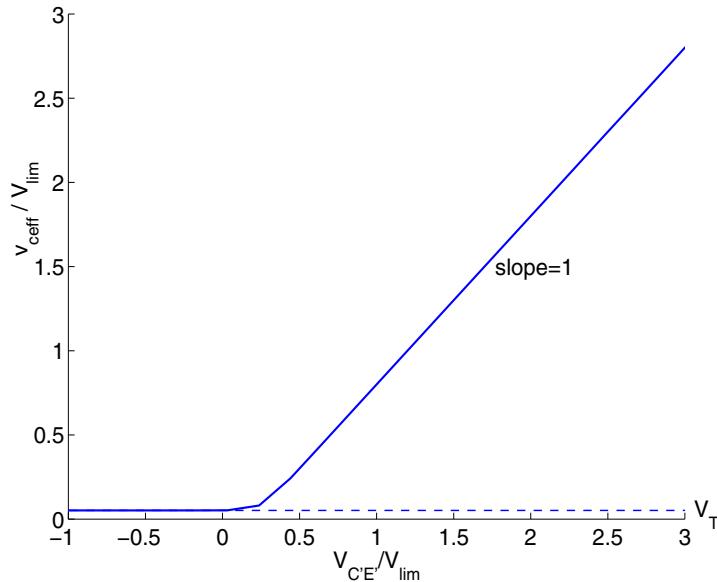


Figure 6-3. Normalized effective collector voltage vs. normalized (internal) collector voltage showing the behavior of the smoothing function.

4.2 Low-current densities

The low-current component t_{f0} depends on the collector-base (or collector-emitter voltage) only:

$$\tau_{f0} = \tau_0 + \Delta\tau_{0h}(c - 1) + \tau_{Bfvl} \left(\frac{1}{c} - 1 \right) \quad (4.2-1)$$

with the (reciprocal) normalized internal BC depletion capacitance $c = C_{jCi0}/C_{jCi}(V_{B'C'})$. The first time constant, τ_0 , represents the sum of voltage

independent components of various transistor regions and their values at $V_{B'C} = 0$; this condition already defines how to extract its value. The second term represents the net voltage dependent change caused by the Early-effect and the transit time through the BC space charge region: for $\Delta\tau_{0h} < 0$ the Early effect dominates while for $\Delta\tau_{0h} > 0$ the transit time increase caused by the widening of the BC space charge region at large voltages dominates. The third term takes into account the finite carrier velocity in the BC space charge region resulting in a carrier jam at low voltages $V_{C'E}$.

[Figure 6-4](#) shows two examples for the voltage dependence of the low-current transit time and its two voltage dependent components. The axis values have been normalized to the model parameters τ_0 and V_{DCi} , respectively. The upper figure (a) contains a behavior that is (more) typical for a relatively slow high-voltage transistor, which is characterized by a relatively wide and low-doped collector region under the emitter. In this case, τ_{f0} increases with increasing $V_{C'E}$ ($= V_{B'E} - V_{B'C}$) due to the widening of the BC space charge region. Toward very low $V_{C'E}$ the drift velocity within the BC space charge region decreases, and the respective (third) term in [\(4.2-1\)](#) dominates the voltage dependence, which leads again to an increase of τ_{f0} and to a minimum around $V_{B'C}=0$.

The lower figure (b) shows the typical behavior for a high-speed transistor with, e.g., a selectively implanted collector and a thin base. With increasing reverse bias, the BC space charge region does extend noticeably also into the base, resulting in a (slightly) negative value of $\Delta\tau_{0h}$ and a decrease of the respective component. Therefore, τ_{f0} decreases with increasing $V_{C'E}$.

The respective low-current forward minority charge is simply given by:

$$Q_{f0} = \tau_{f0} i_{Tf} \quad (4.2-2)$$

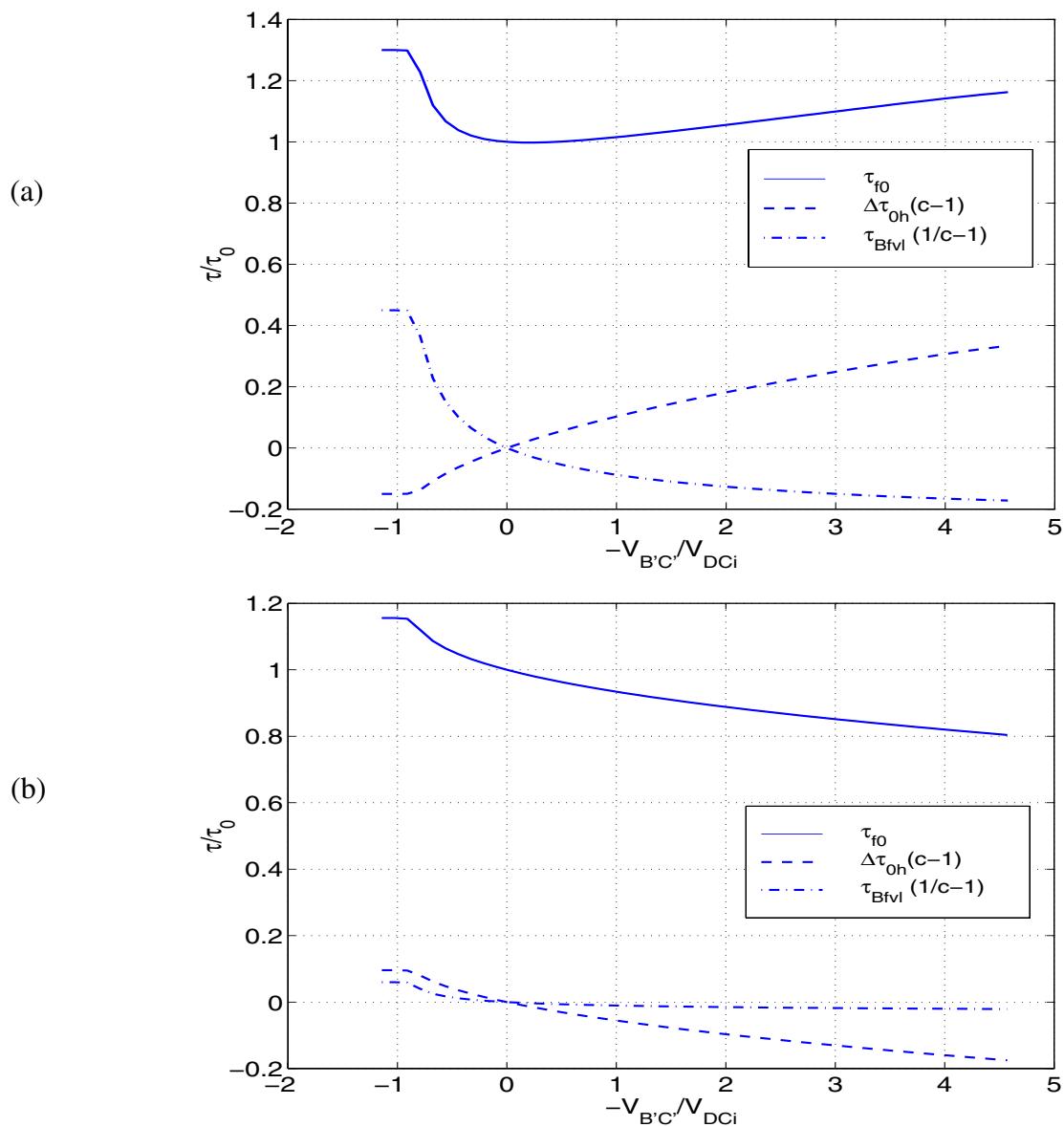


Figure 6-4. Normalized low-current transit time and its components as a function of normalized (internal) BC voltage: (a) for a “high-voltage” transistor ($\tau_0=10\text{ps}$, $\Delta\tau_{0h}=2.5\text{ps}$, $\tau_{Bfvl}=3\text{ps}$), (b) for a “high-speed” transistor ($\tau_0=2.5\text{ps}$, $\Delta\tau_{0h}=-0.4\text{ps}$, $\tau_{Bfvl}=0.1\text{ps}$).

4.3 Medium and high current densities

At medium current densities, the electric field at the BC junction starts to decrease, and the BC junction region becomes quasi-neutral at high current densities. This is often called Kirk-effect [15]. In HICUM, the onset of high-current effects is characterized by the critical current [36]:

$$I_{CK} = \frac{v_{ceff}}{r_{Ci0}} \frac{1}{\sqrt{1 + \left(\frac{v_{ceff}}{V_{lim}}\right)^2}} \left[1 + \frac{x + \sqrt{x^2 + 10^{-3}}}{2} \right] \quad (4.3-1)$$

with $x = (v_{ceff} V_{lim}) / V_{PT}$ in the smoothing function that connects the cases of low and high electric fields in the collector. The other (model) parameters are the internal collector resistance at low electric fields:

$$r_{Ci0} = \frac{w_C}{q \mu_{nC0} N_{Ci} A_E} \frac{1}{f_{cs}} \quad (4.3-2)$$

the voltage defining the boundary between low and high electric fields in the collector:

$$V_{lim} = \frac{v_{sn}}{\mu_{nC0}} w_C \quad (4.3-3)$$

and the (collector) punch-through voltage:

$$V_{PT} = \frac{q N_{Ci}}{2 \epsilon} w_C^2 \quad (4.3-4)$$

As the above relations show, I_{CK} depends on the electron saturation drift velocity, v_{sn} , and the electron low-field mobility, μ_{nC0} , as well as on width w_C and (average) doping N_{Ci} of the internal collector. The current spreading factor f_{cs} , which is discussed in “[Lateral Scaling](#)” on page 6-73, facilitates lateral scaling [44] and is calculated by any parameter generation or extraction program. Despite

their physical relationship r_{Ci0} , V_{lim} and V_{PT} are considered to be model parameters in order to offer a more flexible parameter extraction and broader application of the model. However, their physics-based relationship is very useful for temperature and statistical modelling.

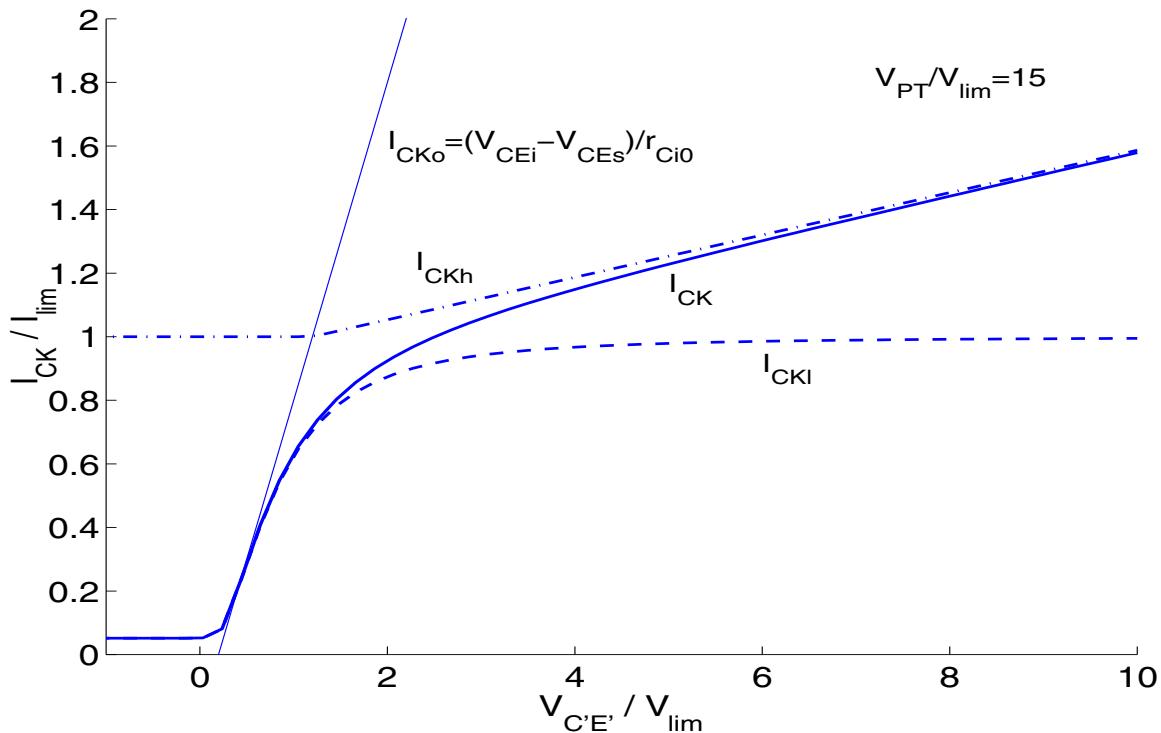


Figure 6-5. Normalized critical current I_{CK} vs. normalized internal CE voltage and related single components: $I_{CKI} = (v_{ceff}/r_{Ci0})/\sqrt{1 + (v_{ceff}/V_{lim})^2}$ from low-voltage theory; $I_{CKh} = I_{lim} [1 + (v_{ceff} - V_{lim})/V_{PT}]$ from high-voltage theory with $I_{lim} = V_{lim}/r_{Ci0}$.

The consequence of the changing electric field in the BC junction at medium current densities is, first of all, an increase in the neutral base width and, therefore, in the base component of the transit time; second, also the transit time through the BC space charge region may increase, depending on how large the electric field is. Third, the corresponding decrease of the small-signal current gain leads to an increase of the emitter component. Since the current independent part of this

component has already been taken into account in τ_{f0} only the change (increase) has to be modelled:

$$\Delta\tau_{Ef} = \tau_{Ef0} \left(\frac{i_{Tf}}{I_{CK}} \right)^{g_{\tau E}} \quad (4.3-5)$$

with the model parameters $g_{\tau E}$ and the storage time:

$$\tau_{Ef0} = \frac{\tau_{pE0}}{\beta_0} \approx \frac{1}{\beta_0} \left(\frac{w_E}{v_{Ke}} + \frac{w_E^2}{2\mu_{pE} V_T} \right) \quad (4.3-6)$$

which depends on the low-frequency common-emitter small-signal current gain β_0 and the hole transit time τ_{pE0} in which w_E , μ_{pE} , and v_{Ke} are the width, hole mobility and the effective hole contact recombination velocity of the neutral emitter, respectively. The corresponding charge stored in the neutral emitter is:

$$\Delta Q_{Ef} = \Delta\tau_{Ef} \frac{i_{Tf}}{1 + g_{\tau E}} \quad (4.3-7)$$

For the neutral collector, the full hole charge storage contribution has to be taken into account here [[35], [36]]:

$$Q_{pC} = \tau_{pCs} i_{Tf} w^2 \quad (4.3-8)$$

with the saturation storage time of the neutral collector:

$$\tau_{pCs} = \frac{w_C^2}{4\mu_{nC0} V_T} \quad (4.3-9)$$

The normalized injection width:

$$\frac{w}{w_C} = \frac{i + \sqrt{i^2 + a_{hc}}}{1 + \sqrt{1 + a_{hc}}} \quad (4.3-10)$$

is bias dependent via the variable:

$$i = 1 - \frac{I_{CK}}{i_{Tf}} \quad (4.3-11)$$

while a_{hc} is considered to be a model parameter. By using a smoothing function for w rather than the original expression i in (4.3-10), the collector charge is made continuously differentiable over the whole bias region.

Device simulations for many different processes have shown that the shape of the current dependence of the neutral base component τ_{Bf} , is very similar to that of the collector portion τ_{pC} due to the coupling of these regions by the carrier density at the BC junction. As a consequence, the bias dependent increase of the base charge at high-current densities is similarly expressed as:

$$\Delta Q_{fB} = \tau_{Bfvs} i_{Tf} w^2 \quad (4.3-12)$$

with the saturation storage time reached at high current densities:

$$\tau_{Bfvs} = \frac{w_{Bm} w_C}{2 G_{\zeta_i} \mu_{nC0} V_T} \quad (4.3-13)$$

w_{Bm} is the metallurgical base width, and $G_{\zeta_i} (\geq 1)$ is a factor that depends on the drift field in the neutral base [47].

In HICUM, the total storage time constant:

$$\tau_{hcs} = \tau_{pCs} + \tau_{Bfvs} = \frac{w_C^2}{4 \mu_{nC0} V_T} + \frac{w_{Bm} w_C}{2 G_{\zeta_i} \mu_{nC0} V_T} \quad (4.3-14)$$

is used as a model parameter to make the model application more flexible. As discussed in “[Lateral Scaling](#)” on page 6-73, collector current spreading and associated lateral scaling at high current densities requires a partitioning between base and collector component. For this, the model parameter:

$$f_{\tau hc} = \frac{\tau_{pCs}}{\tau_{hcs}} = \frac{w_C}{w_C + 2w_{Bm}} \quad (4.3-15)$$

is introduced as partitioning constant.

[Figure 6-6](#) shows a sketch of the current dependence of the *additional* transit time Δt_f and its various components, calculated with the equations given above and using model parameters that are typical for a high-speed process.

In the 1D case, the collector and base component can be lumped together, leading to the expression for the additionally stored minority charge in the base and collector region at high current densities:

$$\Delta Q_{fh} = \tau_{hcs} i_{Tf} w^2 \quad (4.3-16)$$

The corresponding increase of the transit time at high-current densities is then given by:

$$\Delta \tau_{fh} = \tau_{hcs} w^2 \left[1 + \frac{2}{\frac{i_{Tf}}{I_{CK}} \sqrt{i^2 + a_{hc}}} \right] \quad (4.3-17)$$

For this 1D case, f_{thc} has to be set to zero.

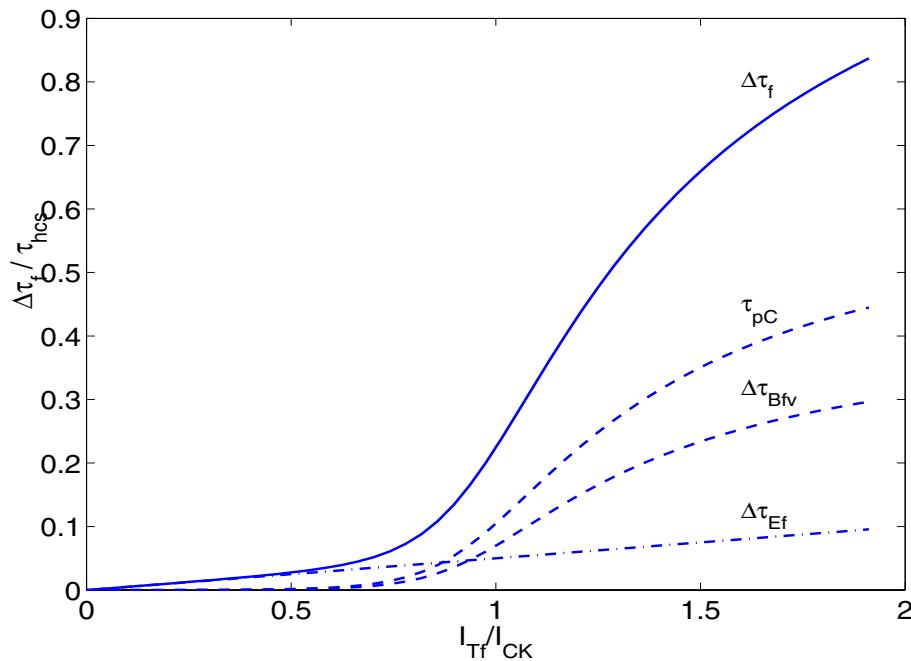


Figure 6-6. Sketch of normalized transit time $\Delta\tau_f$ vs. normalized forward collector current I_{Tf} , including the various components: collector component τ_{pc} , additional base component $\Delta\tau_{Bf}$, and additional emitter contribution $\Delta\tau_{Ef}$.

The total minority charge in the various operating regions, that is used for transient or high-frequency analysis, is then calculated according to (4.0-1) and consists of the following contributions:

$$Q_f = Q_{f0} + \Delta Q_{Ef} + \Delta Q_{fh} \quad (4.3-18)$$

while the total forward transit time (or storage time) is given by:

$$\tau_f = \tau_{f0} + \Delta\tau_{Ef} + \Delta\tau_{fh} \quad (4.3-19)$$

If the lateral scaling capability is used, ΔQ_{fh} and Δt_{fh} are composed of their separately calculated base and collector contribution (Section 18.0). The above equations contain physical and process parameters that facilitate predictions of the electrical characteristics as a function of process variations.

4.4 Base-collector voltage controlled minority charge

For forward transistor operation in high-speed applications the portion of the minority charge which is exclusively controlled by the base-collector voltage is often negligible or only a small fraction of the total minority charge. Therefore, including this charge in Q_f causes only negligible error in transient operation of transistors in high-speed circuits. For small-signal high-frequency operation in the high-current region, which is a very unusual case, the base-collector voltage controlled charge may be taken into account by including its diffusion capacitance in the total internal base collector capacitance [16].

Alternatively, the BC diffusion charge can be modelled by the simple relation:

$$Q_r = \tau_r i_{Tr} \quad (4.4-1)$$

with the inverse transit time τ_r as a model parameter.

5.0 Depletion Charges and Capacitances

Modelling of depletion charges (Q_j) and capacitances (C_j) as a function of the voltage v across the respective junction is partially based on classical theory that gives within a certain operating range:

$$Q_j = \int_0^v C_j dv = \frac{C_{j0} V_D}{1-z} \left[1 - \left(1 - \frac{v}{V_D} \right)^{(1-z)} \right] \quad (5.0-1)$$

and

$$C_j = \frac{C_{j0}}{\left(1 - \frac{v}{V_D} \right)^z} \quad (5.0-2)$$

The zero bias capacitance C_{j0} , the diffusion (or built-in) voltage V_D as well as the exponent coefficient z are model parameters. Due to the pole at forward bias, i.e.

$v=V_D$, however, the above formula is not yet suited for a compact model from both a numerical and physics-based point of view. The respective modification will be described for the BE depletion capacitance.

At high reverse voltages the epitaxial collector can become fully depleted up to the buried layer. This punch- (or reach-)through effect is also not included in the classical equation above (and in the SGPM). The corresponding extension will be discussed for the BC depletion capacitance.

5.1 Base-emitter junction

Figure 6-7 shows the voltage dependence of a BE depletion capacitance at forward bias. The symbols were obtained from 1D device simulation, with depletion and minority charge defined as in [42]. The depletion capacitance follows quite well the classical equation up to a certain voltage, which is close to the turn-on voltage of a transistor used for switching applications. In contrast to the classical equation, the capacitances then reaches a maximum within the “practical” operation range of a transistor. Towards very high forward bias, the capacitance even decreases to zero, since the total depletion charge has to be limited from a physical point of view.

The modified equation employed in HICUM is described below for the example of the internal BE depletion capacitance with the (classical) model parameters C_{jEi0} , V_{DEi} , z_{Ei} , and the additional model parameter a_{jEi} . The latter is defined in Figure 6-7 as the ratio of the maximum value to the zero-bias value and can directly be extracted from f_T measurements at low current densities (e.g. [2], [17]). As a consequence, C_{jEi} is kept at its maximum value in HICUM to maintain consistency between measurement and model. Keeping C_{jEi} constant is also justified, because at high forward bias, i.e. beyond the maximum, the diffusion capacitance becomes orders of magnitude larger than C_{jEi} . The reverse bias region of the BE depletion capacitance and charge is described by the classical equations.

For modeling the peripheral BE depletion capacitance, the corresponding model parameters C_{jEp0} , V_{DEp} , z_{Ep} , a_{jEp} as well as the voltage and v_{B^*E} have to be inserted.

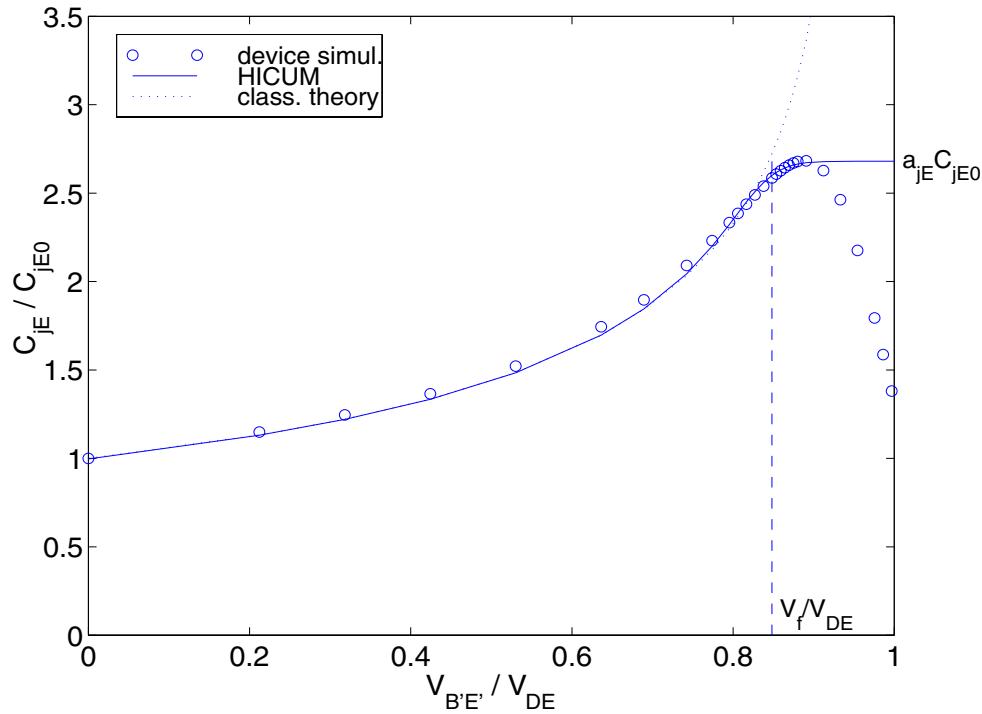


Figure 6-7. Typical dependence of BE depletion capacitance on junction voltage at forward bias: comparison between 1D device simulation, HICUM, classical theory. In addition, characteristic variables used in the model equations have been inserted.

The forward bias depletion capacitance model consists of a classical portion and a component for medium and large forward bias (Figure 6-7):

$$C_{jEi} = \frac{C_{jEi0}}{(1 - v_j/V_{DEi})^{z_{Ei}}} \cdot \frac{e}{1 + e} + a_{jEi} C_{jEi0} \frac{1}{1 + e} \quad (5.1-1)$$

with:

$$e = \exp\left(\frac{V_f - v_{BE}}{V_T}\right) \quad (5.1-2)$$

and the smoothing function for the auxiliary voltage:

$$v_j = V_f - V_T \ln[1 + e] < V_f \quad (5.1-3)$$

V_f is the voltage at which at large forward bias the capacitance of the classical expression intercepts the maximum constant value ([Figure 6-7](#)):

$$V_f = V_{DEi} [1 - a_{jEi}]^{-(1/z_{Ei})} \quad (5.1-4)$$

The corresponding charge equation reads:

$$Q_{jEi} = \frac{C_{jEi0} V_{DEi}}{1 - z_{Ei}} \left[1 - \left(1 - \frac{v_j}{V_{DEi}}\right)^{(1 - z_{Ei})} \right] + a_{jEi} C_{jEi0} (v_{B'E} - v_j) \quad (5.1-5)$$

and Q_{jEp} is calculated similarly.

5.2 Internal base-collector junction

The BC junction is usually operated at reverse bias. If the internal voltage $-v_{B'C'}$ exceeds the effective punch-through voltage (see later), the epitaxial collector region becomes fully depleted. For an ideal step-like transition from the epitaxial collector to the buried-layer the corresponding capacitance would remain constant (like a plate capacitance). However, in reality the doping concentration increases with only a finite slope towards the maximum buried layer concentration. As a consequence, C_{jCi} still decreases even beyond punch-through, but with a weaker voltage dependence.

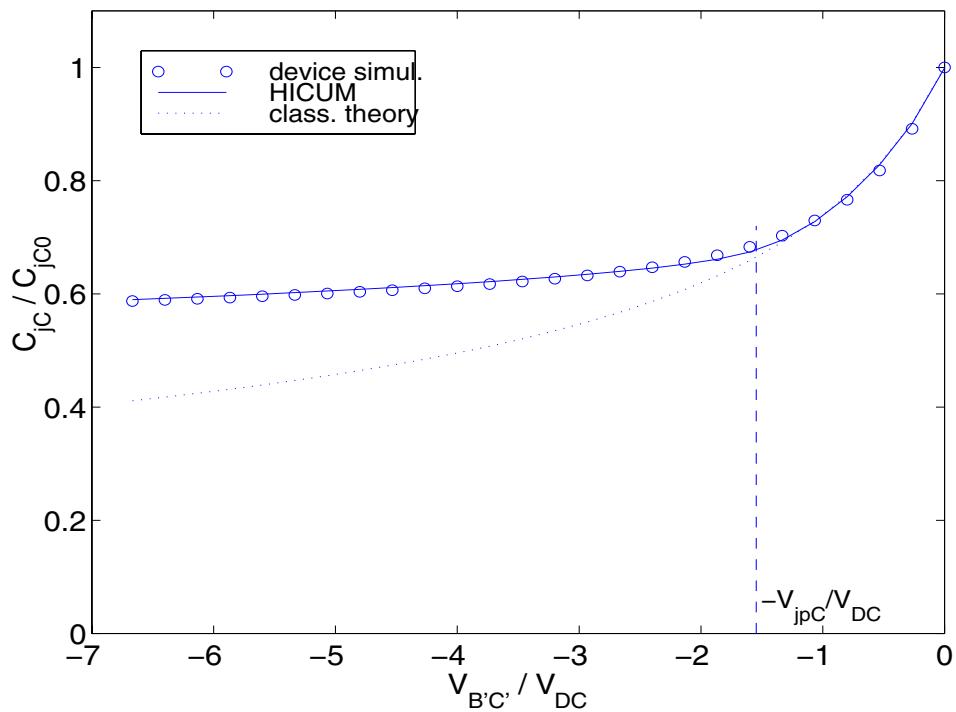


Figure 6-8. Typical dependence of a BC depletion capacitance on junction voltage at reverse bias: comparison between 1D device simulation (symbols), HICUM (solid line), classical theory (dashed line). In addition, characteristic variables used in the model equations have been inserted.

Before the capacitance equation is explained in detail, it is helpful to define a number of variables that are needed in the equations. The effective punch-through voltage is given by:

$$V_{jPCi} = V_{PTCi} - V_{DCi} = \frac{qN_{Ci}}{2\epsilon}w_{Ci}^2 - V_{DCi} \quad (5.2-1)$$

which is shown in Figure 6-8. For flexibility and accuracy reasons as well as in order to simplify and decouple parameter extraction, V_{PTCi} is considered as separate model parameter rather than using V_P from the I_{CK} formulation. For predictive modeling $V_{PTCi}=V_P$ is certainly a good initial guess.

The voltage defining the boundary between the classical expression and the maximum (constant) value at large forward bias was already defined for the BE junction capacitance ([Figure 6-7](#)); in terms of the respective BC model parameters it reads here:

$$V_{fCi} = V_{DCi} [1 - a_{jCi}]^{-(1/z_{Ci})} \quad (5.2-2)$$

The voltage at which the transition from medium to large reverse bias (slowly) starts, is defined as:

$$V_r = 0.1 V_{jPCi} + 4 V_T \quad (5.2-3)$$

In the following, “large reverse” bias is defined as $V_{BCi} \leq -V_{jPCi}$, “medium” bias is defined as $V_{jPCi} < V_{BCi} < V_{fCi}$, and “large forward” bias is defined as $V_{BCi} \geq V_{fCi}$.

The depletion capacitance consists of three components:

$$C_{jCi} = C_{jCi,cl} + C_{jCi,PT} + C_{jCi,fb} \quad (5.2-4)$$

which are discussed below in more detail.

$C_{jCi,cl}$ represents the contribution at medium bias:

$$C_{jCi,cl} = \frac{C_{jCi0}}{(1 - v_{j,m}/V_{DCi})^{z_{Ci}}} \cdot \frac{e_{j,r}}{1 + e_{j,r}} \frac{e_{j,m}}{1 + e_{j,m}} \quad (5.2-5)$$

which contains the classical equation as the first term. The last two product terms result from smoothing functions for the respective BC junction voltage, that enable a continuously differentiable transition to the two adjacent bias regions. Like for the BE depletion capacitance, the numerical overflow at large forward bias is avoided by replacing V_{BCi} with the auxiliary (smoothed) voltage:

$$v_{j,r} = V_{fCi} - V_T \ln[1 + e_{j,r}] \quad (5.2-6)$$

with:

$$e_{j,r} = \exp\left(\frac{V_{fCi} - v_{B'C}}{V_T}\right) \quad (5.2-7)$$

which contains the actual junction voltage. Analogously to C_{jE} , the forward bias value (for $e(v_{j,r}) = 0$) is limited to a maximum:

$$C_{jCi,fb} = a_{jCi} C_{jCi0} \frac{1}{1 + e_{j,r}} \quad (5.2-8)$$

with a_{jCi} as model parameter. The last term is again a continuously differentiable function that enables a smooth transition between large forward and medium bias.

Finally, $C_{jCi,PT}$ represents the large reverse bias region around and beyond punch-through:

$$C_{jCi,PT} = \frac{C_{jCi0,r}}{(1 - v_{j,r}/V_{DCi})^{z_{Ci,r}}} \cdot \frac{1}{1 + e_{j,m}} \quad (5.2-9)$$

Here, the first term contains the classical voltage dependence, but now with different parameters $C_{jCi0,r}$ and $z_{Ci,r}$, which model the weak bias dependence under punch-through conditions and will be discussed later. In this case, the auxiliary voltage is given by the smoothing function:

$$v_{j,m} = -V_{jPCi} + V_r \ln[1 + e(v_{j,m})] \quad (5.2-10)$$

with:

$$e_{j,m} = \exp\left(\frac{V_{jPCi} + v_{j,r}}{V_r}\right) \quad (5.2-11)$$

which now depends on the auxiliary voltage $v_{j,r}$ in order to enable a smooth capacitance and charge behavior over all bias regions. Note, that $v_{j,r}$ equals $v_{B'C}$ at large reverse bias.

The corresponding depletion charge is then obtained by integration of C_{jCi} :

$$Q_{jCi} = \underbrace{Q_{jCi,m}}_{\substack{\text{medium} \\ \text{bias}}} + \underbrace{Q_{jCi,r}}_{\substack{\text{reverse} \\ \text{bias}}} - \underbrace{Q_{jCi,c}}_{\text{correction}} + \underbrace{a_{jCi} C_{jCi0} (v_{B'C} - v_{j,r})}_{\text{large forward bias}} \quad (5.2-12)$$

with the component at medium bias:

$$Q_{jCi,m} = \frac{C_{jCi0} V_{DCi}}{1 - z_{Ci}} \left[1 - \left(1 - \frac{v_{j,m}}{V_{DCi}} \right)^{1 - z_{Ci}} \right] \quad (5.2-13)$$

the component at large reverse bias:

$$Q_{jCi,r} = \frac{C_{jCi0,r} V_{DCi}}{1 - z_{Ci,r}} \left[1 - \left(1 - \frac{v_{j,r}}{V_{DCi}} \right)^{1 - z_{Ci,r}} \right] \quad (5.2-14)$$

and a “correction” component:

$$Q_{jCi,c} = \frac{C_{jCi0,r} V_{DCi}}{1 - z_{Ci,r}} \left[1 - \left(1 - \frac{v_{j,m}}{V_{DCi}} \right)^{1 - z_{Ci,r}} \right] \quad (5.2-15)$$

that results from the integration process. The parameters $C_{jCi0,r}$ and $z_{Ci,r}$ in the last two components are required to model the weaker voltage dependence under punch-through conditions, compared to the voltage dependence at medium bias. $C_{jCi0,r}$ can be calculated from the punch-through voltage as:

$$C_{jCi0,r} = C_{jCi0} \cdot \left(\frac{V_{DCi}}{V_{PTCi}} \right)^{(z_{Ci} - z_{Ci,r})} \quad (5.2-16)$$

while $z_{Ci,r}$ is internally set to $z_{Ci}/4$. The latter turned out to be a good compromise for the investigated cases. As consequence, both $C_{jCi0,r}$ and $z_{Ci,r}$ are only internal parameters and do not have to be extracted and externally specified. If required, however, it would be sufficient to make $z_{Ci,r}$ a user model parameter.

At high current densities C_{jCi} becomes also current dependent as discussed, e.g., in [35]. The respective (smooth) expressions for both capacitance and charge require complicated expressions which can increase simulation time significantly. As discussed in [16] for small-signal applications, a pure voltage dependent model for C_{jCi} proved to be sufficient, since transistors in (small-signal) analog circuits are not operated at high current densities. For large-signal transient applications, however, the influence of a current dependent C_{jCi} is negligible, especially at higher current densities. Therefore, the current dependence of C_{jCi} is neglected in the present HICUM version.

5.3 External base-collector junction

The external base-collector depletion capacitance consists of a bottom and a peripheral part. The parameter extraction tool merges these portions, that may have different model parameters, first into a single element (with a single set of model parameters), which is then partitioned into two capacitance elements across the external base resistance r_{Bx} (Figure 6-1), according to a first-order high-frequency approximation of the RC transmission line behavior of the external base. The merging procedure, which is also required for simpler equivalent circuit structures, reduces the number of model parameters to be specified for the circuit simulator.

A possible alternative is to determine the partitioning from measurements of, e.g., high-frequency S-parameters. However, it was found that such a partitioning factor (strongly) depends on the measurement method and conditions used and, therefore, can assume non-physical values.

The partitioning of the total capacitance $C_{BCx} = C_{jCx}(v) + C_{Cox}$ (see also Section 8.0) across r_{Bx} requires the additional model parameter f_{BC} , which is dependent on geometry and technology specific parameters and which is calculated by the

parameter extraction tool. According to f_{BC} the capacitances are split as follows in the present HICUM implementation (Figure 6-1):

$$C_{BCx} = C'_{BCx} + C''_{BCx} = (1 - f_{BC})C_{BCx} + f_{BC}C_{BCx} \quad (5.3-1)$$

Depending on the values for f_{BC} , C_{Cox} and C_{jCx} as well as according to the nature of the capacitance components different cases have to be distinguished. For instance, if f_{BC} is larger than C_{Cox}/C_{jCx} then part of C_{Cox} has to be connected to node B* (i.e. *behind* r_{Bx}). Since C_{Cox} is closest to the base contact usually the major portion or even the total value has to be connected to the base terminal B. The various cases are taken into account based on the zero-bias depletion capacitance rather than the voltage dependent value in order to reduce arithmetic operation count. The implementation is as follows:

$$C'_{BCx0} = (1 - f_{BC}) C_{BCx0}$$

```

if(C'_{BCx0} ≥ C_{Cox}) then
  C'_{Cox} = C_{Cox}
  C''_{Cox} = 0
  C'_{jCx0} = C'_{BCx0} - C_{Cox}
  C''_{jCx0} = C_{jCx0} - C'_{jCx0}
else
  C'_{Cox} = C'_{BCx0}
  C''_{Cox} = C_{Cox} - C'_{Cox}
  C'_{jCx0} = 0
  C''_{jCx0} = C_{jCx0}
endif
```

Since the depletion charge of the external BC junction does not depend on the transfer current, the purely voltage dependent expressions given for C_{jCi} and Q_{jCi} can be employed for C_{jCx} and Q_{jCx} by simply inserting the model parameters C_{jCx0} , V_{DCx} , z_{Cx} , and V_{PTCx} . The punch-through voltage (and capacitance) of the external collector region is usually different from that of the internal region due to their different epi widths and—in case of a selectively implanted collector—the different doping concentrations in the internal and external region.

5.4 Collector-substrate junction

The CS depletion charge and capacitance are modelled by the same type of formula as employed for the bottom part of the external BC charge and capacitance. The corresponding model parameters are C_{js0} , V_{js} , z_S , and V_{PTS} . Taking into account the punch-through effect may be necessary for technologies containing a semi-insulating substrate (layer). For most technologies, however, there is no punch-through effect at the CS junction, and V_{PTS} can be set to “infinity”.

Since the CS junction is modelled by a single element, C_{js} contains—from a physical point of view—both the bottom and peripheral portion of that junction; i.e., the model parameters result from merging the corresponding voltage dependent portions [51], [48] (see also [Figure 6-26](#)).

For certain applications and processes, an additional substrate coupling network in series to C_{js} as well as a substrate transistor may be necessary. These extensions are discussed later.

6.0 Static Base Current Components

The base current flowing into the emitter can be separated into a bottom and peripheral component. The bottom portion models the current injected across the (*effective*) emitter area, and the peripheral component models the current injected across the peripheral BE junction. Each of these components contains the current contributions caused by volume (SRH and Auger) recombination, by surface recombination, by tunneling, and by an (*effective*) interface recombination velocity at the emitter “contact”. The physical modelling of all these effects including the modulation of the neutral emitter width in advanced and heterojunction bipolar transistors would require a complicated and computationally time expensive description as well as a significantly increased effort in parameter determination. From a practical application point of view, however, a simpler approach does exist that is sufficiently accurate.

The following equations describe the d.c. and quasi-static component of the base current, which are applicable also at high frequencies. Note, that at high switching

speeds or frequencies, the dynamic (capacitive) component of the base current becomes much larger than the d.c./quasi-static component, so that its correct modeling is of higher importance for those applications.

The quasi-static internal base current, which represents injection across the bottom emitter area, is modelled in HICUM as:

$$i_{jBEi} = I_{BEiS} \left[\exp\left(\frac{v_{B'E}}{m_{BEi} V_T}\right) - 1 \right] + I_{REiS} \left[\exp\left(\frac{v_{B'E}}{m_{REi} V_T}\right) - 1 \right] \quad (6.0-1)$$

The saturation currents I_{BEiS} and I_{REiS} as well as the non-ideality coefficients m_{BEi} and m_{REi} are model parameters. The first component in the above formula represents the current injected into the neutral emitter; a corresponding $m_{BEi} > 1$ represents effects such as Auger recombination and the (very small) modulation of the width of the neutral emitter region. The second component represents the loss in the space charge region due to volume and surface recombination; the value of m_{REi} is usually in the range of 1.5 to 2 so that this component only plays a role at low injection. It is used to model the decrease of the current gain at low current densities.

Analogously, the quasi-static base current injected across the emitter periphery is given by:

$$i_{jBEp} = I_{BEpS} \left[\exp\left(\frac{v_{B'E}^*}{m_{BEp} V_T}\right) - 1 \right] + I_{REpS} \left[\exp\left(\frac{v_{B'E}^*}{m_{REp} V_T}\right) - 1 \right] \quad (6.0-2)$$

The saturation currents I_{BEpS} and I_{REpS} as well as the non-ideality factors m_{BEp} and m_{REp} are model parameters.

Since the recombination at low forward bias is more pronounced at the emitter periphery compared to the bottom, its contribution ($I_{REiS} \dots$) to the internal base current component may often be omitted in order to simplify the model and the parameter determination.

In hard-saturation or for inverse operation the current contributions across the base-collector junction become significant. The component of the internal BC junction is:

$$i_{jBCi} = I_{BCiS} \left[\exp\left(\frac{v_{B'C}}{m_{BCi} V_T}\right) - 1 \right] \quad (6.0-3)$$

The component for the external BC junction reads correspondingly:

$$i_{jBCx} = I_{BCxS} \left[\exp\left(\frac{v_{B^*C}}{m_{BCx} V_T}\right) - 1 \right] \quad (6.0-4)$$

In many practical cases, both components can be combined into one, i_{jBC} , between B^* and C' , without loss of accuracy (in, e.g., the output characteristics). This simplifies parameter extraction and reduces the number of model parameters.

7.0 Internal Base Resistance

In HICUM the internal and external base resistance are separately treated. The value of the internal base resistance r_{Bi} depends strongly on operating point, temperature, and mode of transistor operation (d.c., transient, h.f. small-signal). Especially the last mentioned dependence is a very complicated issue for high-speed large-signal switching processes.

The d.c. internal base resistance is modelled by:

$$r_{Bi} = r_i \psi(\eta) \quad (7.0-1)$$

and is in HICUM/Level2 defined by the *effective* emitter dimensions b_E and l_E . The conductivity modulated internal base resistance:

$$r_i = r_{Bi0} \frac{Q_{p0} + \Delta Q_{r0}}{Q_p + \Delta Q_{r0}} = r_{Bi0} \frac{Q_0}{Q_0 + \Delta Q_p} \quad (7.0-2)$$

contains the bias dependent hole charge Q_p (and ΔQ_p , respectively) as well as a “corrected” zero-bias charge [27], [29]:

$$\Delta Q_{r0} = f_{dQr0} Q_{p0} \quad (7.0-3)$$

The factor f_{dQr0} and the zero-bias internal base resistance r_{Bi0} are model parameters. r_{Bi0} is calculated by the parameter extraction tool as a function of emitter geometry and zero-bias internal base sheet resistance r_{SBi0} . Figure 6-9 shows the typical bias dependence of the (normalized) internal base sheet resistance; the ratio r_{SBi}/r_{SBi0} is proportional to r_i/r_{Bi0} . For a transistor with n_E emitter contacts (or stripes), n_E+1 base contacts, and arbitrary aspect ratio $l_E/b_E \geq 1$:

$$r_{Bi0} = r_{SBi0} \frac{b_E}{l_E n_E} g_i \quad (7.0-4)$$

with the geometry function [37], [39]:

$$g_i = \frac{1}{12} - \left(\frac{1}{12} - \frac{1}{28.6} \right) \frac{b_E}{l_E} \quad (7.0-5)$$

The effect of emitter current crowding is described for all aspect ratios $l_E/b_E \geq 1$ by the function [37], [39], [28]:

$$\psi(\eta) = \frac{\ln(1 + \eta)}{\eta} \quad (7.0-6)$$

with the current crowding factor:

$$\eta = f_{geo} \frac{r_i i_{jBEi}}{V_T} \quad (7.0-7)$$

The factor f_{geo} is a model parameter which takes into account the geometry dependence of emitter current crowding (see Section 17.0).

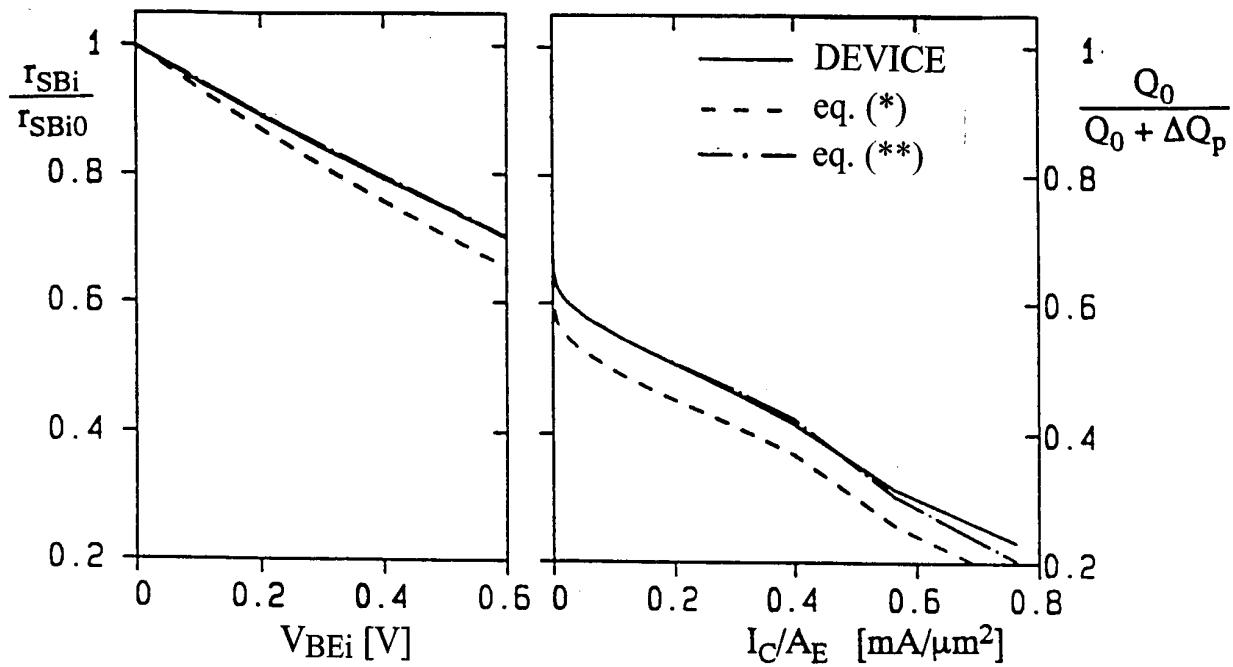


Figure 6-9. Typical bias dependence of the normalized internal base sheet resistance and comparison to (7.0-2) with $f_{dQr0}=0$ (labeled *) and $f_{dQr0}>0$ (labeled **)) [29]. DEVICE corresponds to (1D) numerical device simulation, $Q_0 = Q_{p0}+Q_{r0}$, and $\Delta Q_p = Q_p-Q_{p0}$; ($V_{BEi}=V_{B'E'}$).

For transistors with narrow emitter contacts (or stripes) the influence of the charge storage at the emitter periphery on the dynamic transistor behavior can significantly increase. In order to obtain acceptable computation times and keep the extraction effort reasonable, the HICUM/LEVEL2 equivalent circuit does not contain a complete peripheral transistor element. Therefore, the peripheral charge has to be taken into account by modifying existing elements. The internal base impedance seen between the terminals B^*-E' is decreased by the (effective) peripheral charge Q_{fp} to:

$$r_{Bi}^* = r_{Bi0} \frac{\Delta Q_i}{\Delta Q_p} = r_{Bi0} \frac{\Delta Q_i}{\Delta Q_i + Q_{fp}} \quad (7.0-8)$$

ΔQ_i is the change of the hole charge in the internal transistor during a switching process. For model implementation, however, ΔQ_i is approximated by the corresponding change of hole charge w.r.t. equilibrium; i.e.

$\Delta Q_i = Q_{jEi} + Q_{jCi} + Q_{fi}$. With the (measurable) ratio f_{Qi} ($= Q_{fi}/Q_f$) of internal *minority* charge over total minority charge as a model parameter, $Q_{fp} = Q_f(1-f_{Qi})$ can be calculated. Note, the denominator is equal to $Q_{jEi} + Q_{jCi} + Q_f$ so that Q_{fp} is not required to be explicitly known or calculated.

For the (high-frequency) small-signal case a similar expression can be derived [16]:

$$r_{Bi}^* = r_{Bi0} \frac{C_i}{C_i + C_{dEp}} \quad (7.0-9)$$

with $C_{dEp} = C_{dE}(1-f_{Qi})$ as the peripheral diffusion capacitance and:

$$C_i = C_{jEi} + C_{jCi} + C_{dEi} + C_{dCi} \quad (7.0-10)$$

as the total capacitance connected to the *internal* base node B'. The use of r_{Bi}^* from (7.0-8) gives for slow transients or low frequencies a (small) difference compared to the actual d.c. value of r_{Bi} . However, that deviation is usually insignificant because the influence of the peripheral charge or capacitance is large only for narrow emitter stripes where the d.c. internal base resistance is comparatively small.

8.0 External (Parasitic) Bias Independent Capacitances

In addition to junction and diffusion capacitances, that are both operating point dependent, there may exist constant oxide capacitances between base and emitter as well as base and collector. The base-emitter oxide capacitance C_{Eox} is caused by the overlap of emitter poly over base poly. The base collector oxide capacitance C_{Cox} is caused by the overlap of base poly and contact region over the

buried layer (or the epi collector). The significance of these capacitances depends on the technology considered. In order to make HICUM applicable for an as large as possible variety of technologies two “oxide” capacitances are included in the equivalent circuit of [Figure 6-1](#).

C_{Eox} takes into account the overlap of emitter and base connection, e.g., n⁺ poly-silicon separated from p⁺ poly-silicon by the thin spacer oxide in double self-aligned transistors ([Figure 6-10](#)).

In many modern bipolar technologies the base contact is located on a field oxide and causes an additional oxide capacitance C_{Cox} between base and collector terminal ([Figure 6-11](#)). This capacitance is included in the equivalent circuit within C_{BCx} since its partitioning across r_{Bx} depends on the technology. The parameter f_{BC} determines the actual partitioning of C_{Cox} , too.

Both oxide capacitances are strongly geometry dependent and either have to be measured using proper test structures or can be calculated by the parameter extraction tool.

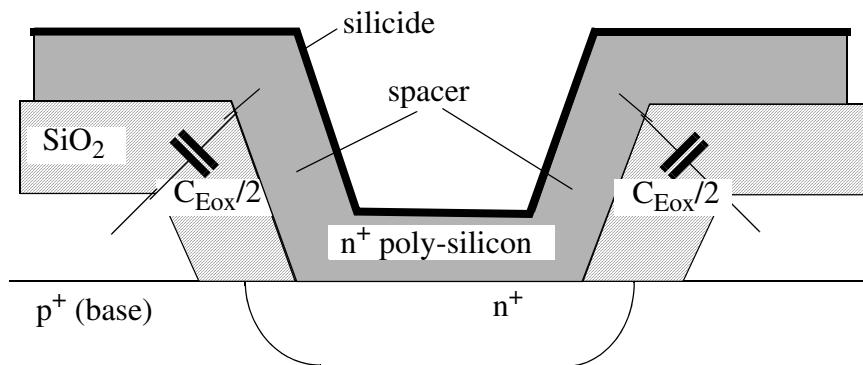


Figure 6-10. Physical origin of the BE isolation overlap capacitance C_{Eox}

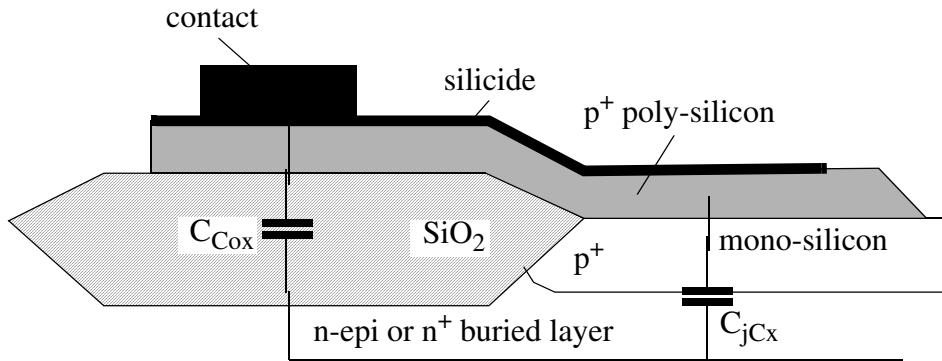


Figure 6-11. Physical origin of the BC isolation overlap capacitance C_{Cox}

9.0 External Series Resistances

The resistive regions of the external transistor and the emitter contact are represented in the equivalent circuit of Figure 6-1 by bias independent series resistances. The reason for including a substrate resistance in the equivalent circuit will be discussed in Section 12.0.

9.1 External base resistance

Figure 6-12 contains a cross section through the external base region of a double-poly self-aligned bipolar transistor. The external base resistance r_{Bx} consists of the following components:

- base contact resistance, r_{BK} ;
- resistance of the poly-silicon on the field oxide, r_{po} ;
- resistance of the poly-silicon on the mono-silicon, r_{pm} ;
- (link) resistance under the spacer, r_{sp} .

The value of each of these components depends on the dimensions of the region and the corresponding sheet resistance or specific resistivity [37], [39]. The external base resistance is then given by:

$$r_{Bx} = r_{BK} + r_{po} + r_{pm} + r_{sp} \quad (9.1-1)$$

Many advanced processes use a silicide with a sheet resistance of typically 2-4 Ω/sq . As a consequence, r_{po} and a portion of r_{pm} are significantly reduced and become small compared to the contact and, especially, the link resistance.

For short emitters and transistors with a one-sided base contact only, 3D effects become important that are taken into account by the parameter extraction tool's resistance calculations according to [37], [39].

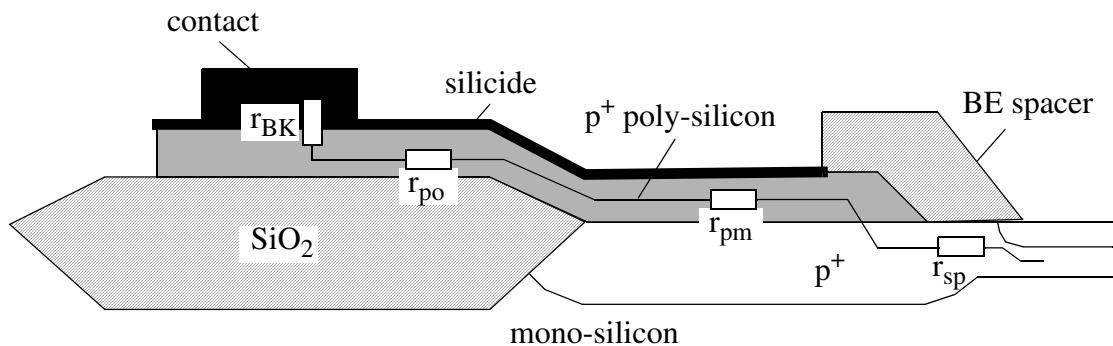


Figure 6-12. The various components of the external base resistance

9.2 External collector resistance

Figure 6-13 contains a cross section through the buried layer and collector region of a bipolar transistor. The external collector resistance r_{Cx} consists of the following components:

- collector contact resistance, r_{CK} ;
- resistance of the sinker region, r_{sink} , connecting contact and buried layer;
- resistance of the buried layer, r_{bl} .

The value of each of these components depends on the dimensions of the region and the corresponding sheet resistance or specific resistivity [51], [48]. The external collector resistance is then given by:

$$r_{Cx} = r_{CK} + r_{sink} + r_{bl} \quad (9.2-1)$$

The external collector resistance does *not* contain any resistance component from the epitaxial layer under the emitter. If r_{CK} is determined by the poly-mono-silicon interface resistance it would be approximately the same as the emitter contact resistance.

The distributed collector current flow in multi-emitter transistors as well as a different number and location of collector stripes (or contacts) is taken into account in the parameter extraction tool by using special formulas. Also, for short emitter (and collector) stripes, current spreading in the buried layer is included in the resistance calculations.

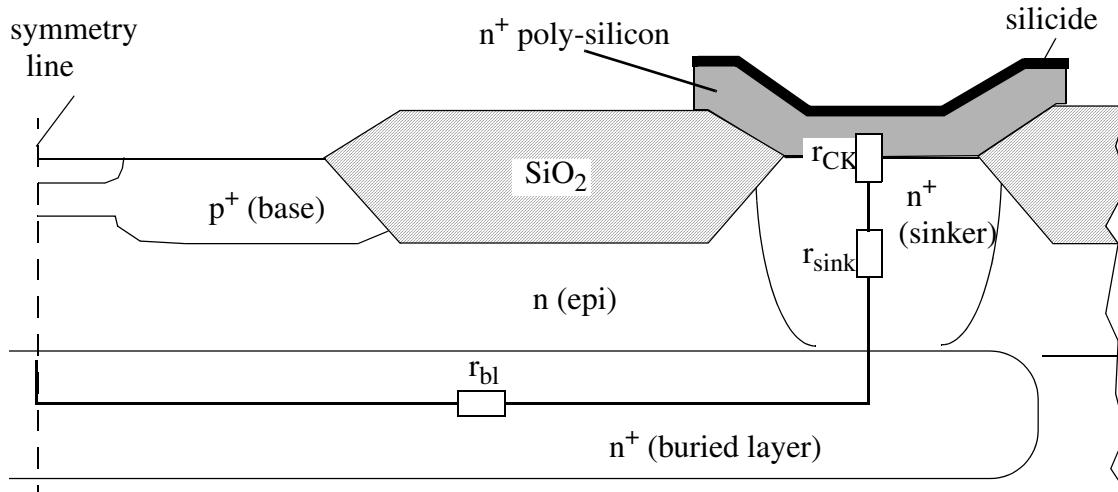


Figure 6-13. The various components of the external collector resistance

9.3 Emitter resistance

The emitter resistance r_E consists of the following (major) components:

- metallization resistance, r_{Em} ,
- poly-silicon resistance, r_{Ep} ;
- resistance of the interface between poly-silicon and mono-silicon, r_{Ei} ,
- resistance of the mono-silicon bulk region, r_{Eb} .

So far, measurements have been showing mostly a direct proportionality of r_E with the reciprocal emitter window area. As a consequence, it is assumed that the emitter resistance for technologies with poly-silicon emitter is mainly determined by the resistance r_i at the interface between poly- and mono-silicon, and that contributions from the other regions are of minor importance. However, this has to be verified for each particular process.

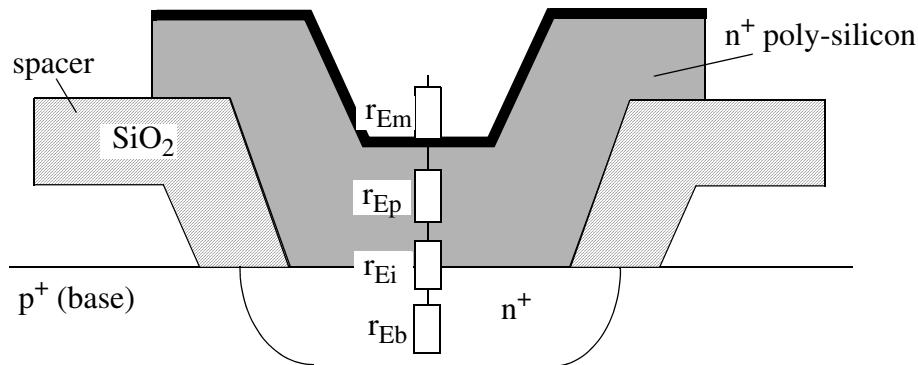


Figure 6-14. The various components of the emitter resistance

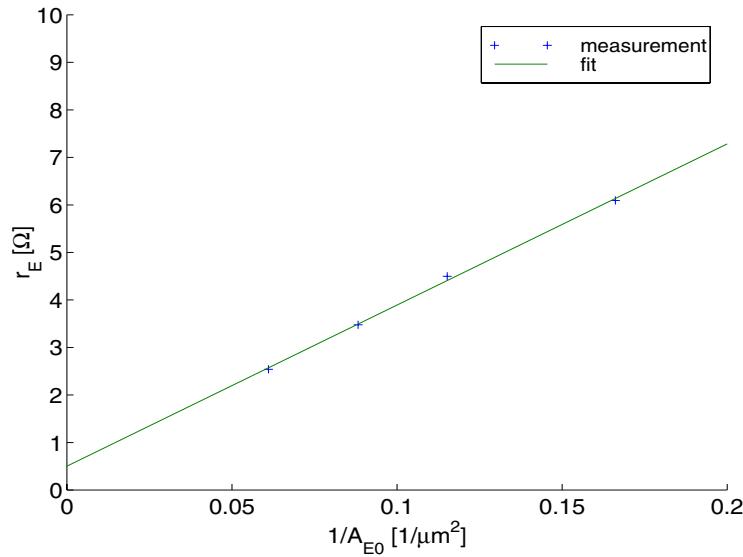


Figure 6-15. Measured emitter resistance vs. reciprocal emitter window area and comparison to the scaling equation

$r_E = \bar{r}_E / A_E + r_0$ with \bar{r}_E as area specific emitter resistance in $[\Omega \mu\text{m}^2]$ and r_0 as residual (parasitic) probe resistance.

10.0 Non-Quasi-Static Effects

Non-quasi-static (NQS) effects are occurring at high-frequencies or fast switching processes. Note, that the designation “high” or “fast” is relative and depends on the technology employed. NQS effects exist in both vertical and lateral spatial direction.

10.1 Vertical direction

It is well-known from “classical” transistor theory that at high frequencies the minority charge Q_f and the transfer current i_T are reacting delayed w.r.t. the voltages across both pn-junction (e.g. [57]). This effect is taken into account in HICUM by introducing additional delay times for both Q_f and I_{Tf} . These additional delay times are modelled as a function of bias by relating them to the transit time [16]:

$$\tau_2 = \alpha_{Qf}\tau_f \quad \text{and} \quad \tau_m = \alpha_{iT}\tau_f \quad (10.1-1)$$

The factors α_{Qf} and α_{iT} are model parameters. The assumption of a stiff coupling between the additional delay times and the transit time has to be regarded as a first order approximation, especially at high current densities where a certain current dependence of α_{Qf} and α_{iT} has been observed [43]. However, it is questionable whether a more complicated modelling of τ_2 and τ_m is justified from an application point of view [16]. Note, that the SGPM only allows τ_m to be specified for *one* (fixed) operating point. Figure 6-16 shows the NQS factors as a function of collector current density for a 15GHz process.

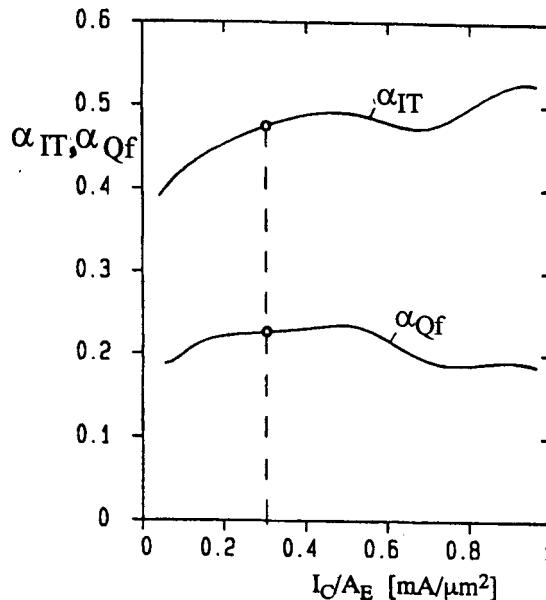


Figure 6-16. NQS factors as a function of collector current density calculated from 1D device simulation; $V_{CE} = 1.5V$.

The additional time delay, which results in an excess phase in the frequency domain, is implemented in HICUM using a second order Bessel polynomial [56] for both time and frequency domain analysis in order to maintain consistency of the respective results. The ideal delay proposed in [57] would cause implementation problems in a circuit simulator for time domain analysis. The use of a Bessel polynomial avoids those problems and leads to the same results in the frequency range of practical interest.

10.2 Lateral direction

Dynamic emitter current crowding causes at high frequencies (or fast transients) a reduction of the impedance seen into the internal base node compared to d.c. or low-frequency conditions.

For the small-signal case the distributed character of the internal base region can be modelled by shunting an adequate capacitance C_{rBi} in parallel to the d.c. resistance r_{Bi} . An analytical treatment of the small-signal input impedance of a stripe emitter transistor with $l_E/b_E \gg 1$ results for not too high frequencies in:

$$C_{rBi} = f_{CrBi} C_i \quad (10.2-1)$$

with C_i as the total capacitance connected to the internal base node B' and the factor $f_{CrBi}=0.2$ [23]. In general, f_{CrBi} depends on the emitter geometry; for instance, it increases (slightly) for smaller emitter aspect ratios. Therefore and to provide maximum flexibility, f_{CrBi} is considered as a model parameter.

For fast large-signal transient applications, the use of C_i is less justified since the transient current crowding violates the assumptions upon which the derivation of (10.2-1) is based.

11.0 Breakdown

11.1 Collector-Base Breakdown

HICUM contains a breakdown model for the base-collector junction that is valid for a weak avalanche effect and a planar breakdown occurring in the internal transistor, i.e. below the emitter. The latter is a reasonable assumption because published measurements for (self-aligned) poly-silicon emitter transistors show such a planar breakdown rather than a breakdown at the periphery of the external BC-junction. The model, which is described also in [45], is intended to indicate the onset of breakdown. In how far, however, it is suited for a simulation and design of circuits somewhat within the breakdown regime depends on the numerical robustness of the particular circuit simulator. Also, the present model

does not include breakdown at high current densities, where the maximum electric field occurs at the buried layer rather than at the BC junction. The related instabilities (such as snap-back) would cause convergence problems for most circuit simulators.

The model equation for the element I_{AVL} in Figure 6-1 is based on the well-known relationship:

$$i_{AVL} = I_T \int_0^{w_{BC}} a_n \exp(-b_n/|E|) dx \quad (11.1-1)$$

The ionization rate a_n and the field b_n are coefficients describing the Avalanche process, E is the electric field within the junction region, x is the ordinate in vertical direction, and w_{BC} is the width of the BC depletion region. From this, the avalanche generation current can be approximated by:

$$i_{AVL} = i_T f_{AVL}(V_{DCi} - V_{B'C}) \exp\left(-\frac{q_{AVL}}{C_{jCi}} (V_{DCi} - V_{B'C})\right) \quad (11.1-2)$$

with the model parameters:

$$f_{AVL} = 2a_n/b_n \quad (11.1-3)$$

$$q_{AVL} = b_n \epsilon A_E / 2 \quad (11.1-4)$$

which depend on emitter area, physical data and temperature (via a_n and b_n).

The possible numerical instability at $V_{B'C}=V_{DCi}$ can be avoided by replacing the term $(V_{DCi}-V_{B'C})$ by the normalized depletion capacitance, $C_c=C_{jCi}(V_{B'C})/C_{jCi0}$, leading to the expression:

$$i_{AVL} = I_T \frac{f_{AVL} V_{DCi}}{C_c^{1/z_{Ci}}} \exp\left(-\frac{q_{AVL}}{C_{jCi0} V_{DCi}} C_c^{(1/z_{Ci}-1)}\right) \quad (11.1-5)$$

which is continuously differentiable via C_c . From a computational point of view, however, i_{AVL} can also simply be set to zero for $V_{B'C} \geq 0$. At large reverse bias $V_{B'C} < -q_{AVL}/C_{jCi0}$, i_{AVL} is linearized to avoid convergence problems.

[Figure 6-17](#) shows the ratio i_{AVL}/I_T , which is proportional to the multiplication factor, as function of the normalized BC voltage for different values of the exponent coefficient $q_{AVL}/(C_{jCi0}V_{DCi})$.

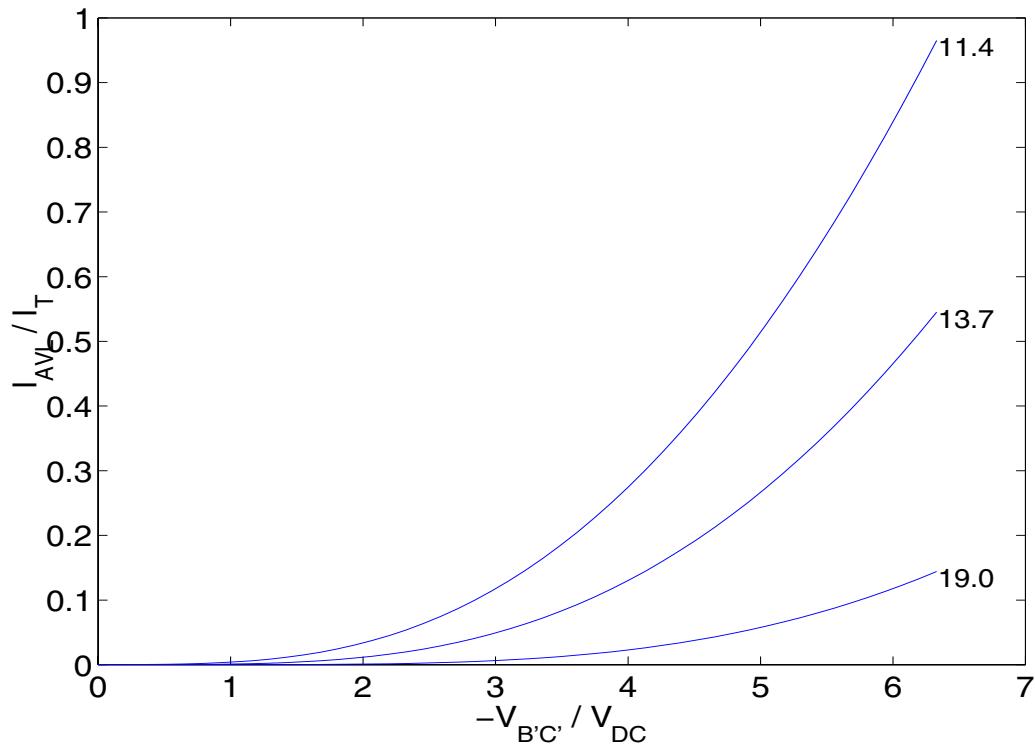


Figure 6-17. Avalanche current i_{AVL} normalized to the transfer current I_T as a function of the normalized BC voltage for various values of the exponent coefficient $q_{AVL}/(C_{jCi0}V_{DCi})$ (see labels). Model parameter used: $C_{jCi0}=0.56\text{fF}/\mu\text{m}^2$, $V_{DCi}=0.79\text{V}$, $z_{Ci}=0.307$.

11.2 Emitter-base breakdown

In advanced bipolar transistors the EB breakdown voltage is usually around 1...3V due to the high doping concentrations. As a result, the breakdown effect in advanced (high-speed) transistors corresponds to a tunnelling mechanism.

The model equation employed in HICUM [45] is based on the expression for the tunnelling current density [50]:

$$J_{BEt} = \frac{\sqrt{2m^*/E_G} q^3 (-V)}{h^2} E_{BEj} \exp\left[-\frac{8\pi\sqrt{2m^*E_G}E_G}{3qhE_{BEj}}\right] \quad (11.2-1)$$

E_G is the bandgap energy, m^* is the effective electron mass, h is the Planck constant, and V is the voltage across the respective BE junction; i.e. $V=V_{B'E'}$ for the bottom junction or $V=V_{B*E'}$ for the perimeter junction. E_{BEj} is the electric field at the junction which—according to the theory of abrupt junctions—can be expressed as:

$$E_{BEj} = 2 \frac{V_{DE} - V}{w_{BE}} \quad (11.2-2)$$

with V_{DE} as built-in voltage of the respective junction. w_{BE} is the space charge region width of that junction and given by:

$$w_{BE} = w_{BE0} (1 - V/V_{DE})^{z_E} \quad (11.2-3)$$

with the zero-bias value:

$$w_{BE0} = \begin{cases} \epsilon_{Si} A_{E0} / C_{jEi0} & , \text{bottom junction} \\ \epsilon_{Si} P_{E0} \left(0.8 \frac{\pi}{2} x_{je}\right) / C_{jEp0} & , \text{perimeter junction} \end{cases} \quad (11.2-4)$$

P_{E0} and A_{E0} are the emitter window perimeter and area, respectively, and x_{je} is the vertical junction depth. C_{jEi0} and C_{jEp0} are the zero-bias depletion capacitance of the bottom and perimeter junction, respectively. The factor $0.8(\pi/2)x_{je}$ approximates the perimeter junction curvature caused by lateral outdiffusion of the emitter doping. Inserting (11.2-2 to 11.2-4) back into (11.2-1), defining a normalized voltage $V_e=V/V_{DE}$, and multiplying with the respective area yields for the tunnelling current:

$$I_{BEt} = I_{BEtS}(-V_e)(1-V_e)^{1-z_E} \exp[-a_{BEt}(1-V_e)^{z_E-1}] \quad (11.2-5)$$

Figure 6-18 shows the normalized tunneling current as a function of normalized junction voltage.

For numerical reasons, the $1-V_e$ terms are converted to terms that contain the respective normalized bias dependent depletion capacitance $C_e=C_jE(V)/C_{jE0}$, which has been made numerically stable at $V_e=1$. Using the classical $C_jE(V)$ relationship which is valid at the reverse bias of interest:

$$(1-V_e)C_e = C_e^{1-1/z_E} \quad (11.2-6)$$

leads to the final formulation:

$$I_{BEt} = I_{BEtS}(-V_e)C_e^{1-1/z_E} \exp[-a_{BEt}C_e^{1/z_E-1}] \quad (11.2-7)$$

The “saturation” current:

$$I_{BEtS} = 2 \frac{\sqrt{2m^*/E_G} q^3 V_{DE}^2}{h^2 \epsilon_{Si}} C_{jE0} \quad (11.2-8)$$

and the coefficient:

$$a_{BEt} = \frac{8\pi \sqrt{2m^*E_G} E_G}{3qh} \frac{w_{BE0}}{2V_{DE}} \quad (11.2-9)$$

are model parameters, that depend on physical and process data as well as on geometry. i_{BEt} is a continuously differentiable expression since the depletion capacitance is continuously differentiable.

In most processes, the breakdown effect occurs first at the peripheral emitter junction, because the doping concentrations are highest there, and due to the curvature of that junction which leads to a narrower space-charge region and, thus, to a higher electric field. In this case, C_{jE0} , V_{DE} , z_E , and V_e in the above equations have to be replaced by C_{jEp0} , V_{DEp} , and z_{Ep} and v_{B^*E}/V_{DEp} .

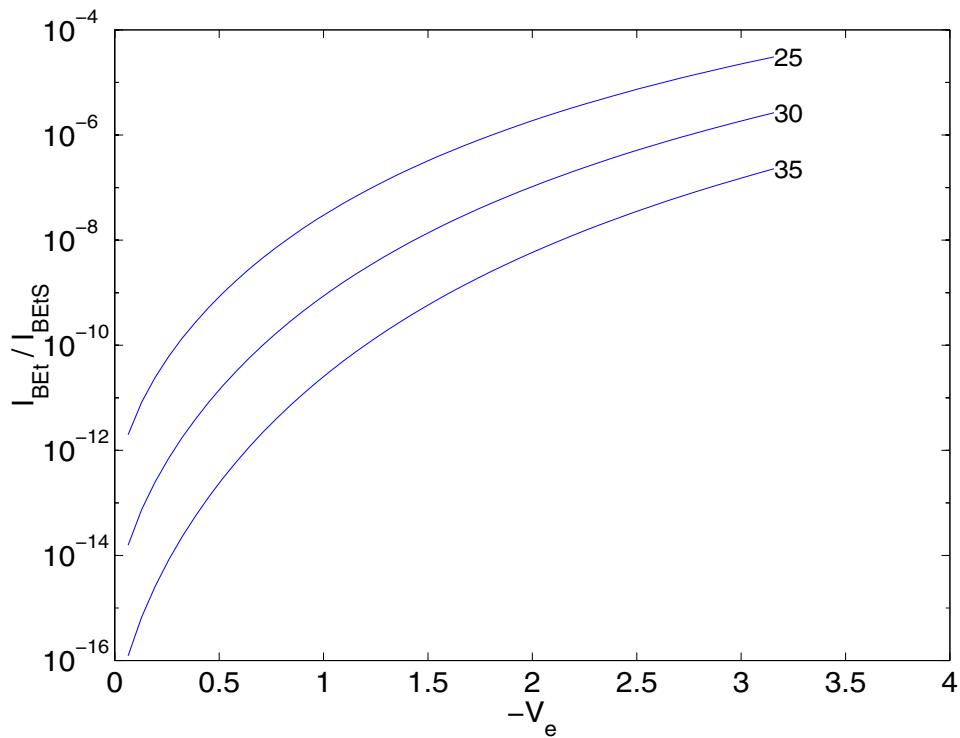


Figure 6-18. Normalized tunneling current as a function of normalized junction voltage $V_e=V/V_{DE}$ for various values of a_{BEt} . Model parameters used: $V_{DE}=0.95V$, $z_E=0.5$.

12.0 Substrate Network

The substrate contact of a transistor may be at the bottom of the wafer only or, more preferably, at the surface. But even the surface contact is usually located relatively far away from the CS junction, so that a significant resistance r_{Su} may exist in series to the CS depletion capacitance, due to the usually quite high substrate resistivity ρ_{Su} . In addition, the high permittivity of silicon, ϵ_{Si} , leads to a capacitance C_{Su} in parallel to r_{Su} that becomes important at high operating speed. Physically, the connection between the substrate contact and the CS depletion capacitance can be partitioned into a bulk (or bottom) and a periphery RC network [22] (also [Figure 6-26](#)), each of which having the time constant $\tau_{Si}=\rho_{Su}\epsilon_{Si}$. For practical applications in a compact model, however, a simplified network is employed that combines bottom and periphery components into one RC equivalent circuit ([Figure 6-1](#)).

The values of r_{Su} and C_{Su} are strongly geometry dependent and are calculated by the parameter extraction tool.

[Figure 6-19](#) shows the impact of the substrate coupling on the frequency dependent output conductance of a 25GHz process.

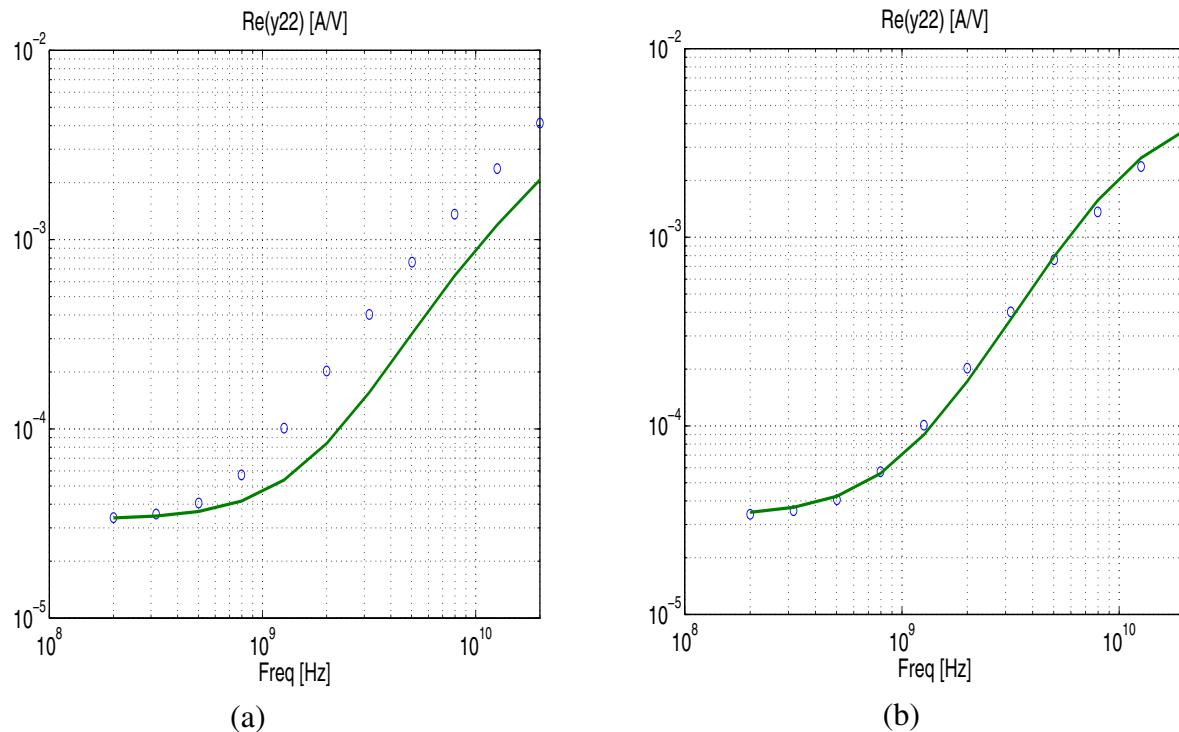


Figure 6-19. Impact of intra-device substrate-coupling on transistor output conductance ($g_o=\text{real}(y_{22})$) as function of frequency.

Comparison of measurements (symbols) and HICUM (lines): (a) model without substrate network r_{su} , C_{su} ; (b) model with substrate network. Emitter size: $0.4 \times 14 \mu\text{m}^2$; bias point: $I_C/A_E=0.22 \text{ mA}/\mu\text{m}^2$, $V_{CE}=0.8 \text{ V}$.

13.0 Parasitic Substrate Transistor

Under certain electrical circumstances, the parasitic substrate transistor can be turned on, depending also on the processes and layout of the transistor. First of all, one can distinguish between a bulk substrate transistor given by the buried layer area and—dependent on the process—a peripheral substrate transistor. The most likely electrical condition for turning on the substrate transistor is a forward-biased BC junction which occurs either at high current densities under the emitter (internal BC junction) or if the transistor is operated in hard saturation (external and internal BC junction). An example for this are power amplifiers, in which the

transistor is operated in hard saturation with $V_{CE} \rightarrow V_{CEs}$ and strongly forward biased V_{BC} . Another condition for turning on the substrate transistor is a forward biased CS junction caused by voltage drops in the substrate (latch-up).

Since the bulk substrate transistor usually has a current gain of less than 1 due to the highly doped and wide buried layer, its influence is negligible and needs not to be considered at high collector current densities. Device simulations confirmed this for an advanced bipolar process. A peripheral substrate transistor action can be avoided by a surrounding collector sinker with high enough doping concentration at the buried layer depth. Also, this peripheral transistor does not exist at all in trench-isolated processes.

In (npn) transistors without surrounding collector sinker, however, the epitaxial collector acts as a lightly doped base between the external base (now the emitter) and the substrate (now the collector), resulting in a pnp transistor with considerable current gain that may be required to be modelled in addition to the vertical npn transistor. HICUM contains a simplified substrate transistor model in order to take the corresponding effects into account.

The parasitic substrate transistor consists of the elements i_{Ts} , i_{SC} , C_{js} , i_{BCx} and C_{BCx} in the equivalent circuit of [Figure 6-1](#). While C_{js} , i_{BCx} and C_{BCx} already belong to the standard HICUM equivalent circuit, a substrate *transistor* action requires the addition of a substrate transfer current source. Since substrate transistor action is considered as second order effect, a simplified model has been chosen for i_{Ts} :

$$i_{Ts} = I_{TsS} \left[\exp\left(\frac{v_B * C}{m_{Sf} V_T}\right) - \exp\left(\frac{v_{Sr} * C}{m_{Sr} V_T}\right) \right] \quad (13.0-1)$$

with the saturation current I_{TsS} and the emission coefficients m_{Sf} and m_{Sr} as model parameters. The second term is relevant if the SC junction becomes forward biased. In this case, also a “base” current component exists, that is modelled by the diode equation:

$$i_{SC} = I_{SCS} \left[\exp\left(\frac{v_{SC}}{m_{SC} V_T}\right) - 1 \right] \quad (13.0-2)$$

with the saturation current I_{SCS} and the emission coefficient m_{SC} as model parameters.

The minority charge storage in the epitaxial region under the external base is taken into account by a diffusion charge

$$Q_{dS} = \tau_{Sf} I_{TS} \quad (13.0-3)$$

with the forward transit time τ_{Sf} as a model parameter of the substrate transistor. τ_{Sf} depends on the average current path (neutral base width) under the external base and at the buried layer periphery. So far, the classical base transit time expression turned out to be a good approximation for estimating the value of τ_{Sf} . Also, device simulations have shown that for high-speed processes the stored charge represented by Q_{dS} has only negligible effect on transistor switching out of hard saturation.



Note In advanced bipolar processes the emitter terminal of the substrate transistor (B^*) moves towards the (npn) base contact (B), which makes the external realization of such a parasitic transistor by a subcircuit even easier.

14.0 Small-signal Equivalent Circuit

Figure 6-20 shows the small-signal EC, that can be derived from the large-signal EC in Figure 6-1. Nonlinear elements that depend on their branch voltage only, such as diodes, have been replaced by their conductances. Nonlinear elements that are controlled by other than their branch voltage, such as transfer current sources and the avalanche current source, are replaced by the respective controlled source and a possible conductance. The latter contains the direct dependence of the nonlinear current source on the branch voltage while the controlled source is designated by a complex current symbol. The respective derivatives for the nonlinear elements are given below and can be calculated once the currents and charges are available.

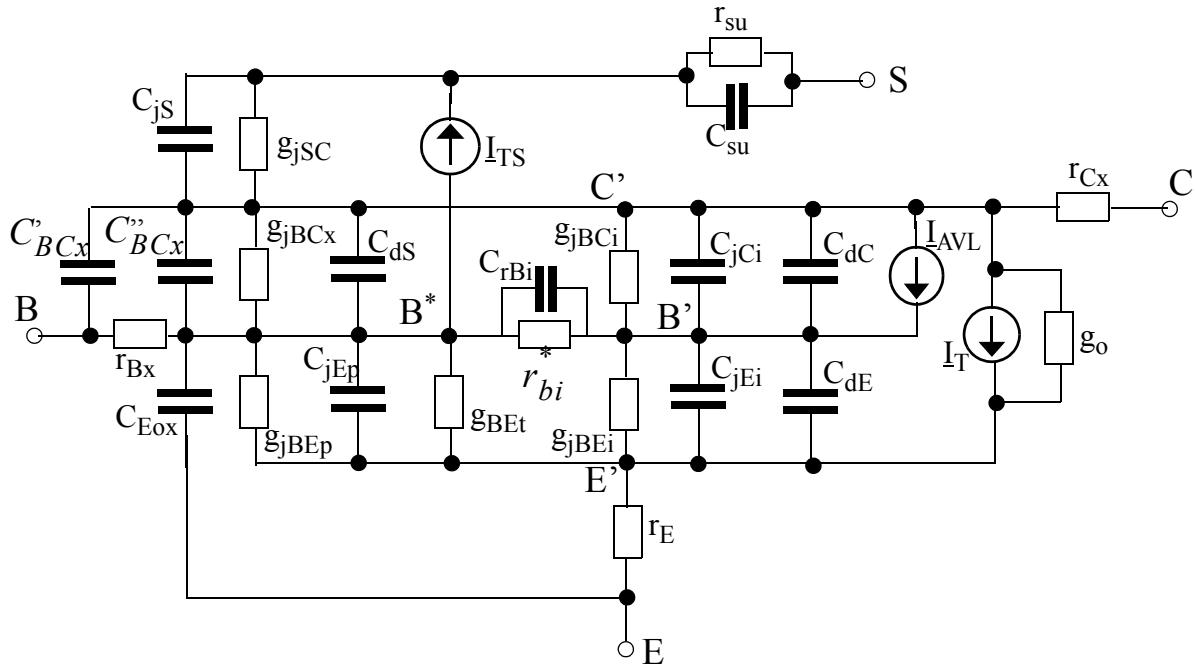


Figure 6-20. Small-signal HICUM/Level2 equivalent circuit. The external BC capacitance consists of a depletion and a bias independent (e.g. oxide) capacitance with the ratio $C_{BCx}/C_{''BCx}$ being adjusted with respect to proper modelling of the h.f. behavior.

The capacitances C_{BCx} , C_{jEp} , C_{jEi} , C_{jCi} and C_{jS} , the parasitic overlap capacitances, and the (bias independent) series resistances have already been defined in the previous sections. The diode element current equations are linearized as usual to give the respective conductances g_{jBEp} , g_{jBEi} , g_{jBCi} , g_{jBCx} , g_{jSC} , which read in general:

$$g_{jn} = \frac{I_{nS}}{m_n V_T} \exp\left(\frac{V}{m_n V_T}\right) = \frac{I_{jn} + I_{nS}}{m_n V_T} \quad (14.0-1)$$

with $n=\{BEp, BEi, BCi, BCx, SC\}$ and V as the respective branch voltage.

The conductance of the tunneling current element follows directly from (11.2-5):

$$g_{BEt} = \frac{dI_{BEt}}{dV} = -\frac{I_{BEtS}}{V_{DE}} \exp\left[-\frac{a_{BEt}}{(1-V_e)^{1-z_E}}\right] \left[1 - \frac{V_e(1-z_E)}{1-V_e} [(1-V_e)^{1-z_E} + a_{BEt}] \right]$$

in which $1-V_e$ can be converted into the continuously differentiable capacitance ratio:

$$g_{BEt} = -\frac{I_{BEtS}}{V_{DE}} \exp(-a_{BEt} C_e^{1/z_E - 1}) [1 - V_e(1-z_E) C_e^{1/z_E} (C_e^{1/z_E - 1} + a_{BEt})]$$

The forward transfer i_{Tf} current depends on $V_{B'E'}$ and $V_{B'C'}$ (or $V_{C'E'}$) and, therefore, leads to a voltage controlled current source $g_{mf}V_{B'E'}$ and the output conductance element g_o . The various conductances of the transfer current that are required for the small-signal equivalent circuit are calculated in HICUM/L0 as follows:

$$S_{fb} = \left. \frac{dI_{Tf}}{dV_{B'E'}} \right|_{V_{B'C'}} = \frac{I_{Tf1}}{V_T \cdot MCF} \cdot \frac{Q_{p,T} + \tau_r I_{Tr} - HJEI \cdot C_{jEi} V_T MCF}{Q_{p,T} + \tau_r I_{Tr} + \tau_{f,T} I_{Tf1} d_{ch}} d_{ch} \quad (14.0-2)$$

with I_{Tf1} from (3.6-5), $Q_{p,T}$ from (3.1-4):

$$d_{ch} = 1 + 2I_{Tf1}/I_{ch} \quad (14.0-3)$$

and

$$\tau_{f,T} = \left. \frac{dQ_{f,T}}{dI_{Tf}} \right|_{V_{B'C'}} \quad (14.0-4)$$

The forward component of the output conductance reads:

$$S_{fc} = \left. \frac{dI_{Tf}}{dV_{B'C'}} \right|_{V_{B'E'}} = -\frac{I_{Tf1}}{V_{Af}} \cdot \frac{d}{1 + d \tau_{f,T} I_{Tf1} / Q_{p,T}} \quad (14.0-5)$$

with a bias dependent “Early” voltage:

$$V_{Af} = \frac{Q_{p,T}}{h_{jci}C_{jCi} + \left. \frac{dQ_f}{dV_{B'C}} \right|_{V_{B'E}}} \quad (14.0-6)$$

and the (bias dependent) factors:

$$d = d_{ch} \frac{e}{1+e} \quad \text{and} \quad e = \exp\left(\frac{v_c}{V_T} - 1\right) \quad (14.0-7)$$

The latter factor results from the smoothing function for I_{CK} .

The corresponding inverse conductances are:

$$S_{rb} = \left. \frac{dI_{Tr}}{dV_{B'E}} \right|_{V_{B'C}} = \frac{I_{Tr}}{V_T} \cdot \frac{Q_{p,T} - (C_{jEi} + h_{jci}C_{jCi} + \tau_{f,T}S_{fb})V_T}{Q_{p,T} + \tau_r I_{Tr}} \quad (14.0-8)$$

and

$$S_{rc} = \left. \frac{dI_{Tr}}{dV_{B'C}} \right|_{V_{B'E}} = -\frac{I_{Tr}}{V_T} \cdot \frac{Q_{p,T} + (\tau_{f,T}S_{fc} - h_{jci}C_{jCi})V_T}{Q_{p,T} + \tau_r I_{Tr}} \quad (14.0-9)$$

From these derivatives follows the transconductance in common-emitter configuration ($dV_{B'E}=dV_{B'C}$):

$$g_m = \left. \frac{dI_T}{dV_{B'E}} \right|_{V_{CE''}} = y_{21}(\omega=0) = S_{fb} + S_{fc} \quad (14.0-10)$$

and the output conductance in common-emitter configuration:

$$g_o = \left. \frac{dI_T}{dV_{CE}} \right|_{V_{B'E'}} = y_{22}(\omega=0) = -(S_{fc} + S_{rc}) \quad (14.0-11)$$

The resulting small-signal transfer current is then given by:

$$I_T = S_{fb} V_{B'E'} - S_{rb} V_{B'C} \quad (14.0-12)$$

If non-quasi-static effects are included, the transconductances become complex variables.

Outside of the high-current region, the forward conductances reduce to:

$$g_m \approx g_{mf} = \frac{I_{Tf1}}{V_T} \cdot \frac{Q_p - C_{jEi} V_T}{Q_{p,T} + \tau_f J_{Tf}} \quad (14.0-13)$$

and

$$g_o \approx I_{Tf} \frac{h_{jci} C_{jCi}}{Q_p + \tau_f J_{Tf}} \approx \frac{I_{Tf1}}{V_{Af}} \quad (14.0-14)$$

Since $h_{jCi} < 1$ for (positive) a bandgap grading in the base, an HBT has a higher Early voltage and lower output conductance than a homojunction transistor.

The conductances of the avalanche current element read:

$$g_{AVL,b} = \left. \frac{dI_{AVL}}{dV_{B'E'}} \right|_{V_{B'C}} = k_{AVL} S_{fb} - g_a \quad (14.0-15)$$

and

$$g_{AVL,c} = \left. \frac{dI_{AVL}}{dV_{B'C}} \right|_{V_{B'E'}} = k_{AVL} S_{fc} + g_a \quad (14.0-16)$$

with the “multiplication” factor (11.1-5):

$$k_{AVL} = \frac{f_{AVL} V_{DCi}}{C_c^{1/z_{Ci}}} \exp\left(-\frac{q_{AVL}}{C_{jCi0} V_{DCi}} C_c^{(1/z_{Ci}-1)}\right) \quad (14.0-17)$$

and the conductance:

$$g_a = \frac{I_{AVL}}{V_{DCi}} C_c^{1/z_{Ci}} \left[1 + \frac{q_{AVL}}{C_{jCi0} V_{DCi}} C_c^{(1/z_{Ci}-1)} (1 - z_{ci}) \right] \quad (14.0-18)$$

The transconductance and small-signal transfer current of the parasitic substrate transistor, which is described by a simple transport model, are given by:

$$g_{Ts} = \frac{I_{Ts} + I_{TSS}}{m_{Sf} V_T} \quad \text{and} \quad I_{Ts} = g_{Ts} (\underline{V}_{B'C} - \underline{V}_{SC}) \quad (14.0-19)$$

The BE diffusion capacitance is given by:

$$C_{dE} = \tau_f S_{fb} \quad (14.0-20)$$

while the BC diffusion capacitance is approximated by:

$$C_{dC} = \tau_r S_{rc} + \tau_{hcs} g_{of} \quad (14.0-21)$$

The diffusion capacitance of the parasitic substrate transistors is given by:

$$C_{dS} = \tau_{Sf} g_{TS} \quad (14.0-22)$$

and is connected in parallel to C''_{BCx} .

Although the base resistance is bias dependent, the d.c. value is used also for the small-signal case:

$$r_{bi}^* = r_{Bi}^* \quad (14.0-23)$$

which so far turned out to be a reasonable approximation, while at the same time simplifying the implementation significantly.

Derivatives of dissipated power P with respect to temperature are also taken into account in the thermal model for self-heating.

15.0 Noise Model

The noise behavior is modelled by employing the small-signal equivalent circuit in [Figure 6-20](#) and adding to all series resistances, diodes, and to the transfer current source their corresponding equivalent noise current sources. Compared to the SGPM, the more sophisticated equivalent circuit and more accurate model equations of HICUM/L2 allow a more accurate overall description of the noise behavior, especially at high frequencies (e.g. [\[46\]](#)).

In ohmic resistances thermal noise is taken into account by an equivalent noise current source

$$\overline{I_r^2} = \frac{4k_B T \Delta f}{r} \quad (15.0-1)$$

with $r = r_E, r_{Cx}, r_{Bx}$, or $r_{Bi,n}$ (see below). k_B is the Boltzmann constant, T the temperature, and Δf is the frequency interval. Investigations have shown that for certain processes a distributed model of the internal base yields an improved description of the high-frequency noise behavior. However, in order to avoid either swapping transistor models as a function of simulation mode or larger simulation time in general by using a two- or multi-transistor model, a factor k_{rBi} is available as an additional model parameter. Therefore, for noise calculations, a modified internal base resistance can be used:

$$r_{Bi,n}^* = k_{rBi} r_{Bi}^* \quad (15.0-2)$$

Shot noise is assumed for the transfer current:

$$\overline{I_T^2} = 2qI_T \Delta f \quad (15.0-3)$$

the avalanche current I_{AVL} , and for diode currents, i.e. currents across junctions:

$$\overline{I_{j\text{diode}}^2} = 2qI_{j\text{diode}} \Delta f \quad (15.0-4)$$

with $\text{diode} = \{\mathbf{BEi}, \mathbf{BCi}, \mathbf{BEP}, \mathbf{BCx}, \mathbf{CS}\}$.

The base current components injected across the BE junction also contain flicker noise, which depends inversely on the frequency f . Investigations of flicker noise in polysilicon-emitter bipolar transistors seem to indicate that the flicker noise is generated at the poly-silicon to mono-silicon interface [4], [5], [6]. This corresponds to a strong correlation between the bottom and perimeter component. As a consequence, and for simplification of the noise model and its implementation, the present version contains only one flicker noise source in parallel to g_{jBEi} that combines the bottom and perimeter current:

$$\overline{I_{BE}^2} = k_F (I_{jBEi} + I_{jBEP})^{a_F} \frac{\Delta f}{f} \quad (15.0-5)$$

with k_F and a_F as model parameters. Deviations from the 1/f behavior, which can be caused by, e.g. random telegraph noise, cannot be taken into account by the employed model.

16.0 Temperature Dependence

Temperature dependence is described in HICUM via those model parameters that are related to physical quantities like intrinsic carrier density or mobility. In the following formulas, T_0 is the reference temperature for which the model parameters have been determined. The formulas are valid for a temperature range between about 250K and 400K, assuming that the model parameters are determined around $T_0 = 300\text{K}$. The validity range depends somewhat on the technology considered. A more detailed description of the physical background of certain formulas employed in HICUM is given in [35], [36].

For all quantities that contain the bandgap energy or its equivalent bandgap voltage V_G , respectively, the assumption of a linear dependence of bandgap with

temperature is sufficient in the temperature range specified above. In most circuit simulators, though, this is assumed only for the saturation currents, which are most sensitive to temperature changes, while for the built-in voltages often a more complicated function $V_G(T)$ is used (e.g. [50]) which is valid down to quite low temperatures. However, since effects such as freeze-out are usually not taken into account by compact models, it is not recommended to use a model below about 250K unless its parameters have been extracted or at least verified especially for that temperature range.

For numerical reasons (over- or underflow), some of the original equations have to be modified, mostly towards very temperatures. The respective smoothing functions to be used for circuit simulator implementation are also given below. It is assumed that every circuit simulator prevents negative or zero temperature.

16.1 Transfer current

The transfer current is strongly temperature dependent via the intrinsic carrier density n_i . Since the square of n_i is contained in the ICCR constant c_{10} , this leads to:

$$c_{10}(T) = c_{10}(T_0) \left(\frac{T}{T_0} \right)^3 \exp \left[\frac{V_{Gb}}{V_T(T)} \left(\frac{T}{T_0} - 1 \right) \right] \quad (16.1-1)$$

The (over the base region) *averaged* bandgap voltage V_{Gb} is a model parameter and

$$V_T(T) = k_B T / q \quad (16.1-2)$$

is the temperature dependent value of the thermal voltage.

The zero-bias hole charge Q_{p0} is only weakly temperature dependent via the influence of base width change with temperature, that is mainly caused by the change in depletion width of the BE junction:

$$Q_{p0}(T) = Q_{p0}(T_0) \left[1 + \frac{z_{Ei}}{2} \left\{ 1 - \frac{V_{DEi}(T)}{V_{DEi}(T_0)} \right\} \right] \quad (16.1-3)$$

No additional model parameters are required here. Also, for typical values of V_{DEi} in the order of V_{Gb} the value of Q_{p0} will remain positive up to extremely temperatures. Therefore, a smoothing function is omitted here to keep the computational effort minimal, particularly during self-heating calculations.

16.2 Base currents and current gain

The current gain B can be modelled as a linear function of T ,

$$B(T) = B(T_0) [1 + \alpha_B \Delta T] \quad (16.2-1)$$

with the relative temperature coefficient $\alpha_B = (1/B)(dB/dT)$ at $T=T_0$ and for $I_C=\text{const}$ as a model parameter which can be easily measured. Since in HICUM not the current gain but the physically independent base current is described, the respective saturation currents are modelled as a function of temperature:

$$I_{BS}(T) = I_{BS}(T_0) \left(\frac{T}{T_0} \right)^{3MCF/m_B} \exp \left[\frac{V_{Gb} MCF}{m_B V_T(T)} \left(\frac{T}{T_0} - 1 \right) - \alpha_B \Delta T \right] \quad (16.2-2)$$

Like the transfer current the main contribution to the temperature dependence is caused by the intrinsic carrier density. However, the relevant bandgap is given by the emitter region and, thus, the V_{Gb} term is corrected here by the term $\alpha_B \Delta T$ with $\Delta T = T - T_0$. Additionally, the influence of the non-ideality factor m_B ($= m_{BEi}$, m_{BEP} ...), which is assumed to be temperature independent, is taken into account.

Similar relations are used for the saturation currents of the other base current components after inserting the respective model parameters.

16.3 Transit time and minority charge

The critical current density I_{CK}/A_E depends on temperature via physical parameters like mobility of the epitaxial collector and saturation velocity. The internal collector resistance contains the low-field electron mobility and reads:

$$r_{Ci}(T) = r_{Ci}(T_0) \left(\frac{T}{T_0} \right)^{\zeta_{Ci}} \quad (16.3-1)$$

The model parameter ζ_{Ci} is a function of the collector doping concentration (e.g. [35], [47]). The voltage V_{lim} contains both mobility and saturation velocity, and it follows:

$$V_{lim}(T) = V_{lim}(T_0)(1 - \alpha_{vs}\Delta T) \left(\frac{T}{T_0} \right)^{\zeta_{Ci}} \quad (16.3-2)$$

with the relative temperature coefficient α_{vs} of the (electron) saturation velocity as model parameter. Designating the above original voltage as V_{lim}^o , numerical problems due to negative values of V_{lim} in I_{CK} at very high temperatures are avoided by using the smoothing function:

$$V_{lim} = V_T + V_T \ln \left[1 + \exp \left(\frac{V_{lim}^o - V_T}{V_T} \right) \right] \quad (16.3-3)$$

The CE saturation voltage can be modelled as a linear function of temperature:

$$V_{CEs}(T) = V_{CEs}(T_0)[1 + \alpha_{CEs}\Delta T] \quad (16.3-4)$$

with α_{CEs} as a model parameter. Its value can be estimated from the difference between the respective relative temperature coefficients of the built-in voltages V_{DEi} and V_{DCi} .

The temperature dependence of the transit time model is given in [47]. Except for the low-current transit time, no additional model parameters are required. The

low-current portion of the transit time, τ_{f0} , as a function of temperature is mainly determined by the quadratic temperature dependence of the parameter τ_0 :

$$\tau_0(T) = \tau_0(T_0)[1 + \alpha_{\tau0}\Delta T + k_{\tau0}\Delta T^2] \quad (16.3-5)$$

The model parameters α_{t0} and k_{t0} can be expressed by physical quantities.

The time constants τ_{Bfvs} and τ_{pCs} depend on temperature via the same diffusivity (of the collector) and, therefore, the temperature dependence of the composite parameter τ_{hcs} can be expressed as:

$$\tau_{hcs}(T) = \tau_{hcs}(T_0)\left(\frac{T}{T_0}\right)^{(\zeta_{Ci}-1)} \quad (16.3-6)$$

The emitter time constant τ_{Ef0} depend on temperature via mainly the hole diffusivity in the neutral emitter and the current gain. Assuming a large emitter concentration with a negligible temperature dependence of the mobility, the following expression can be obtained:

$$\tau_{Ef0}(T) = \tau_{Ef0}(T_0) \frac{T/T_0}{1 + \alpha_B\Delta T} \quad (16.3-7)$$

which does not require an additional model parameter. Possible numerical problems at extreme temperatures (very high or very low, dependent on the sign of α_B) have to be avoided though; for this, instead of the original denominator $a_o = (1+\alpha_B\Delta T)$ the following denominator is used:

$$a = \frac{a_o + \sqrt{a_o^2 + 0.01}}{2} \quad (16.3-8)$$

The temperature dependence of the minority charge and of the additional delay times, that model vertical NQS effects, follows automatically from that of the transit time using (4.1-1) and (10.1-1), respectively.

16.4 Depletion charges and capacitances

The key parameter for the temperature dependence of the depletion charges and capacitances is the diffusion (or built-in) voltage. From its proportionality to the bandgap follows:

$$V_D(T) = V_D(T_0) \frac{T}{T_0} - V_{Gj} \left(\frac{T}{T_0} - 1 \right) - 3 V_T \ln \left(\frac{T}{T_0} \right) \quad (16.4-1)$$

The bandgap voltage V_{Gj} corresponds to the vs. T=0 extrapolated bandgap voltage including (possible) high doping effects occurring at the respective pn-junction. For simplification, V_{Gj} can be set equal to V_{Gb} , but this depends on whether the junction related bandgap voltage is available as parameter in the particular circuit simulator. Designating the above original voltage as V_D^o , numerical problems due to negative values at (very) high temperatures are avoided by using the smoothing function:

$$V_D = V_{D\alpha} + V_{T0} \ln \left[1 + \exp \left(\frac{V_D^o - V_{D\alpha}}{V_T} \right) \right] \text{ with } V_{D\alpha} = 1.001 \frac{V_D(T_0)}{\alpha_{j0}} \quad (16.4-2)$$

In ELDO and SPICE-like simulators, the built-in temperature dependence of the depletion charge parameters is used, which is the same as for the SGPM and so far proved to be sufficiently accurate for silicon-based applications.

The zero-bias junction capacitance can be expressed generally as $C_{j0} \sim V_D^{-z}$ so that its temperature dependence can be directly calculated from that of V_D :

$$C_{j0}(T) = C_{j0}(T_0) \left(\frac{V_D(T_0)}{V_D(T)} \right)^z \quad (16.4-3)$$

The temperature dependence of the depletion charge follows automatically from (2.1.4-1a) by applying the above formulas and assuming that the exponent-factor z does not depend on temperature.

The parameter a_j determining the maximum value of a depletion capacitance at forward bias is (empirically) modified as follows:

$$\alpha_j(T) = \alpha_j(T_0) \frac{V_D(T)}{V_D(T_0)} \quad (16.4-4)$$

As can be seen in [Figure 6-21](#), the zero-bias capacitance increases, and the maximum as well as the voltage at the maximum decrease with increasing temperature.

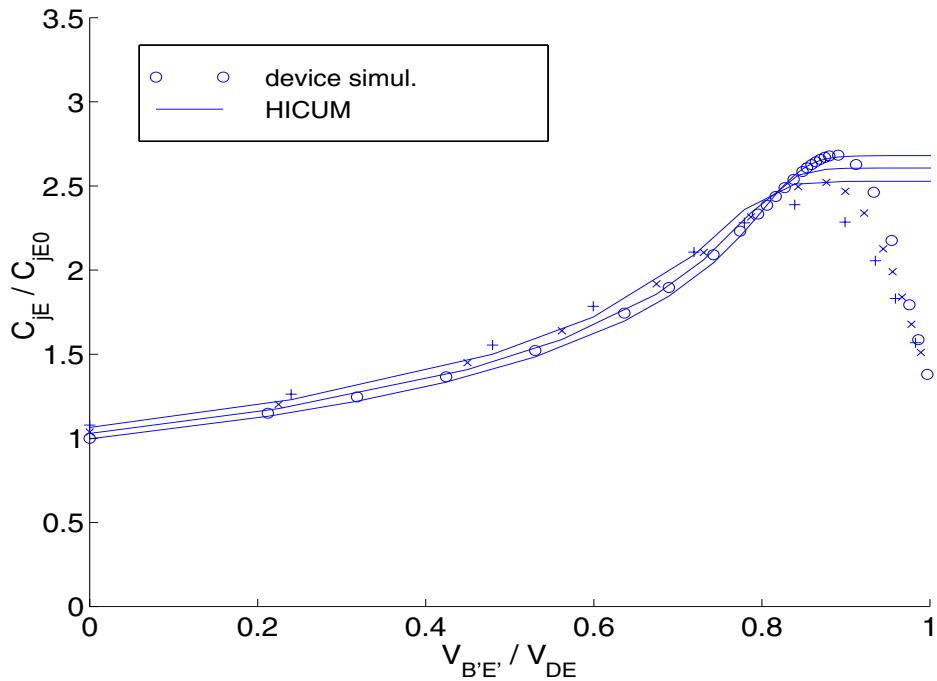


Figure 6-21. Temperature dependence of the base-emitter depletion capacitance, normalized to its zero-bias value at 300K, vs. normalized applied voltage: comparison between 1D device simulation (symbols) and model equation (lines). The curves are for the temperatures: T/K = 300 (o), 350 (*), 400 (+).

16.5 Series resistances

The internal base resistance depends on temperature mainly via the mobility in the neutral base region, which is contained in the internal base sheet resistance. Thus, the zero-bias resistance is described as:

$$r_{Bi0}(T) = r_{Bi0}(T_0) \left(\frac{T}{T_0} \right)^{\zeta_{rBi}} \quad (16.5-1)$$

The model parameter ζ_{rBi} is a function of the (average) base doping concentration ($r_{Ci0}(T)$). Conductivity modulation and emitter current crowding in r_{Bi} are automatically described as a function of T by the corresponding charges and currents. The shunt capacitance C_{rBi} is temperature dependent via the capacitances of the internal transistor.

External base resistance r_{Bx} , external collector resistance r_{Cx} , and emitter series resistance follow a similar relationship as r_{Bi0} . This requires the model parameters ζ_{rBx} , ζ_{rCx} and ζ_{rE} which are a function of the (average) doping concentrations within the corresponding regions.

[Figure 6-22](#) shows the various types of temperature dependence that can be modelled with the above equation.

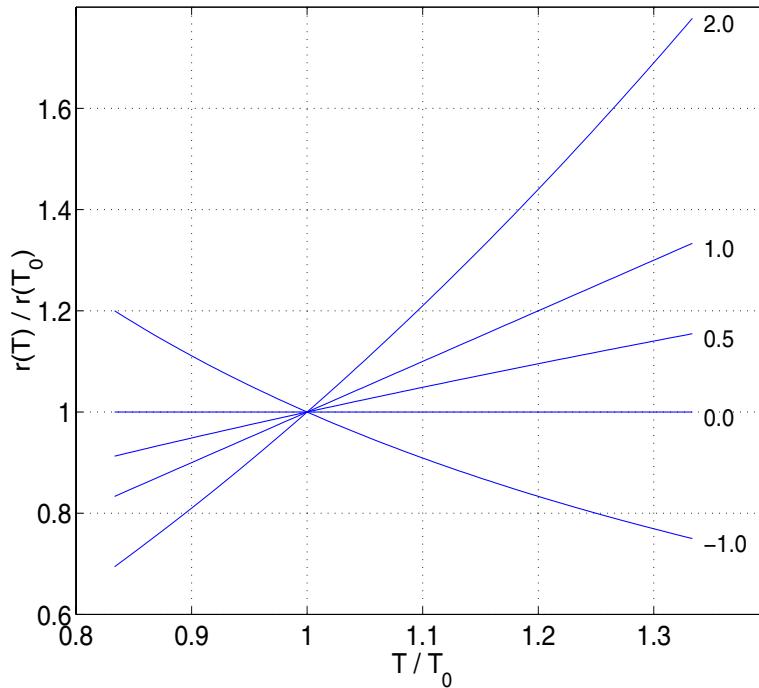


Figure 6-22. Normalized resistance as a function of temperature according to (16.5-1) for different values of ζ_r ($= \zeta_{rBi}, \zeta_{rBx}, \zeta_{rCx}$ or ζ_{rE}) as parameter.

16.6 Breakdown

Base-collector junction (avalanche effect)

The temperature dependence of the coefficients describing avalanche breakdown can be described as [20]:

$$a_n(T) = a_n(T_0) \exp(\alpha_{na} \Delta T) \quad (16.6-1)$$

$$b_n(T) = b_n(T_0) \exp(\alpha_{nb} \Delta T) \quad (16.6-2)$$

with $\Delta T = T - T_0$ and the temperature coefficients α_{na} and α_{nb} . Insertion of these equations into (11.1-3 and 11.1-4) gives for the model parameters

$$f_{AVL}(T) = f_{AVL}(T_0) \exp(\alpha_{fav} \Delta T) \quad (16.6-3)$$

$$q_{AVL}(T) = q_{AVL}(T_0) \exp(\alpha_{qav} \Delta T) \quad (16.6-4)$$

with the temperature coefficients $\alpha_{fav} = \alpha_{na} - \alpha_{nb}$ and $\alpha_{qav} = \alpha_{nb}$ which are considered as model parameters. According to a more recent study in [18], the temperature dependence of the parameter a_n is negligible while only b_n varies slightly with temperature. Therefore, the exp-function reduces to (or can be approximated by) its first series terms, i.e. $\exp(\alpha_{nb}\Delta T) \approx 1 + \alpha_{nb}\Delta T$.

Base-emitter junction (tunnelling effect)

The temperature dependence of the parameters describing BE tunnelling is mainly determined by the bandgap's temperature dependence. The saturation current is then given by [45]:

$$I_{BEtS}(T) = I_{BEtS}(T_0) \sqrt{\frac{V_G(T_0)}{V_G(T)}} \left(\frac{V_{DEp}(T)}{V_{DEp}(T_0)} \right)^2 \frac{C_{jEp0}(T)}{C_{jEp0}(T_0)} \quad (16.6-5)$$

The exponent-coefficient as a function of temperature reads:

$$a_{BEt}(T) = a_{BEt}(T_0) \left(\frac{V_G(T)}{V_G(T_0)} \right)^{3/2} \frac{V_{DEp}(T)}{V_{DEp}(T_0)} \approx a_{BEt}(T_0) \quad (16.6-6)$$

No additional model parameters are required if either the simulator internal bandgap voltage is used or $V_G=V_{Gb}$ is inserted which is a reasonable approximation.

17.0 Self-heating

The increase of the transistor's “junction” temperature T_j caused by self-heating is calculated using a thermal network as shown in Figure 6-1b. The current source corresponds to the power dissipated in the device, and the node voltage corresponds to the junction temperature. The calculation requires the thermal resistance, R_{th} , and thermal capacitance, C_{th} , (of the particular transistor) as model parameters. The thermal network is solved together with each transistor model (provided $R_{th}>0$) for d.c. and transient operation. The node voltage is

passed on to the model routine in order to calculate the temperature dependent model parameters.

The power is calculated from all relevant dissipative elements in the equivalent circuit, excluding any energy storage elements:

$$P = |I_T V_{C'E}| + \sum |I_{jd} V_{diode}| + |I_{AVL} V_{B'C}| + \sum \Delta V_n^2 / r_n \quad (17.0-1)$$

with $d=\{BEp, BCx, BEi, BCi, SC\}$, V_{diode} as respective diode voltage, r_n as (non-zero) series resistances ($n=\{Bx, E, Cx, Bi\}$), and ΔV_n as the corresponding voltage drop across those resistances.

Note that only *self*-heating is presently taken into account but not the thermal coupling between different devices on the chip, which is a much more complicated topic and does not directly belong to a transistor model. However, the already existing temperature node of the model can be used for modelling thermal coupling in a circuit.

18.0 Lateral Scaling

This section contains a brief description of the geometry scaling used for HICUM in order to explain the general idea. The scaling formulas—as far as they are bias independent—are implemented in the parameter extraction tool which is used to generate model parameters for a given transistor configuration. The description of the full set of lateral scaling equations would go beyond the scope of this text. Note, that due to the many different processes the geometry scaling of bipolar transistors is often more complicated than for MOS transistors. However, a quite general way of geometry scaling has been developed, that has proved to be applicable to a large variety of processes.

18.1 Transfer current

The geometry dependent parameters of the transfer current are:

$$c_{10} \sim A_E^2, \quad Q_{p0} \sim A_E, \quad I_{Ch} \sim A_E$$

with A_E as the effective emitter area.

18.2 Base current components

The base current components can be split into a bottom and a periphery contribution. For the BE junction, the bottom component is scaled proportional to the effective emitter area. As a consequence, the periphery component has to be corrected by the amount of current already taken into account by widening the emitter to an effective area in order to keep the total BE base current the same.

The base current across the internal base collector junction is scaled with the effective emitter area, while the current across the external BC junction is scaled with the external BC area minus the effective emitter area.

18.3 Minority charge and transit times

The formulas given in “[Minority Charge, Transit Times, and Diffusion Capacitances](#)” on page 6-12 for τ_{f0} , $\Delta\tau_{fh}$ and the corresponding charge Q_f were derived from one-dimensional (1D) considerations and can be employed if transistors with a fixed emitter width b_E are used, which is assumed to be much smaller than the emitter length l_E . However, for narrow or short emitter stripes, 2D and 3D effects occur that will result in less physical values for some of the parameters (such as r_{Cio}) as well as in different “shapes” of the bias dependence of the transit time. Furthermore, if variable emitter widths and lengths down to the minimum allowed dimensions have to be modelled, the 1D equations would require a different set of model parameters for every size or at least for a certain set of sizes (“binning”). As a consequence, a scalable transit time model is preferred which is given below [44].

18.4 Low current densities

The transit time at low current densities can be expressed as a function of emitter dimensions through its model parameter:

$$\tau_0 = \tau_{0i} \frac{1 + (\tau_{f0p}/\tau_{f0i})\gamma_C P_E/A_{E0}}{1 + \gamma_C P_E/A_{E0}} \quad (18.4-1)$$

with $P_E = P_{E0} + 4\gamma_C$, $A_{E0} = b_{E0}l_{E0}$. The ratio of the transit time of the peripheral transistor to that of the bottom transistor, τ_{f0p}/τ_{f0i} , as well as τ_{0i} are the parameter extraction tool input parameters.

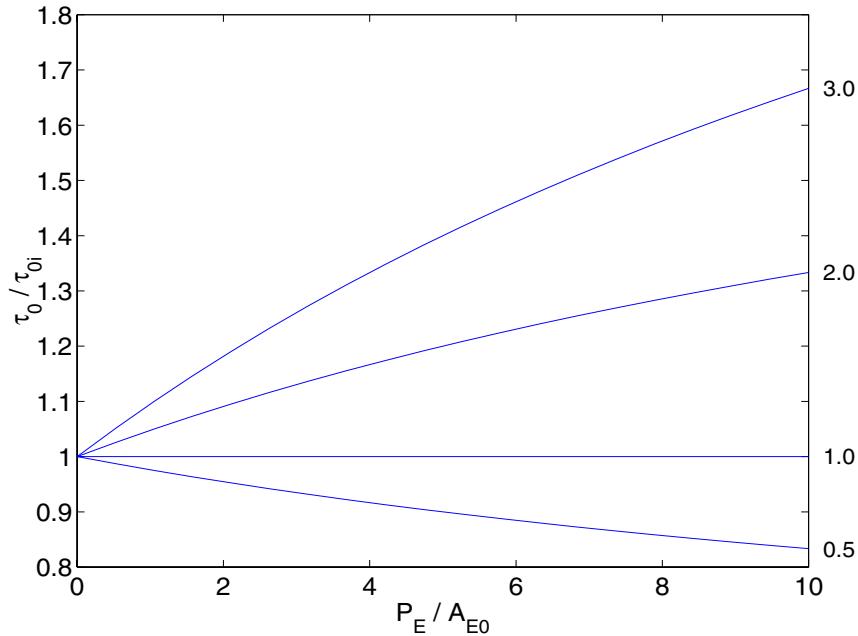


Figure 6-23. Normalized low-current transit time as a function of emitter geometry for various ratios of τ_{f0p}/τ_{f0i} . Model parameter used: $\gamma_C=0.05\mu\text{m}$.

18.5 Critical current (density)

Collector current spreading leads to a lower effective current density and, as a result, a larger critical current density than the one scaled by the emitter area only. This can be described by:

$$I_{CK} = I_{CK,1D} f_{cs} \quad (18.5-1)$$

with the current spreading factor:

$$f_{cs} = \begin{cases} \frac{\zeta_b - \zeta_l}{\ln[(1 + \zeta_b)/(1 + \zeta_l)]} & , \quad l_{E0} > b_{E0} \\ 1 + \zeta_b & , \quad l_{E0} = b_{E0} \end{cases} \quad (18.5-2)$$

which becomes larger than 1 if current spreading occurs. Since the factor f_{cs} can be incorporated into the model parameter r_{Ci0} (4.3-2), it does not appear as additional model parameter for HICUM. The new model parameters that also determine the bias dependent lateral scaling (see below) are:

$$\zeta_b = 2 \frac{w_C}{b_E} \tan \delta_C \quad \text{and} \quad \zeta_l = 2 \frac{w_C}{l_E} \tan \delta_C \quad (18.5-3)$$

They depend on the collector current spreading angle δ_C which is a parameter extraction tool parameter.

[Figure 6-24](#) shows the factor f_{cs} as a function of various parameters.

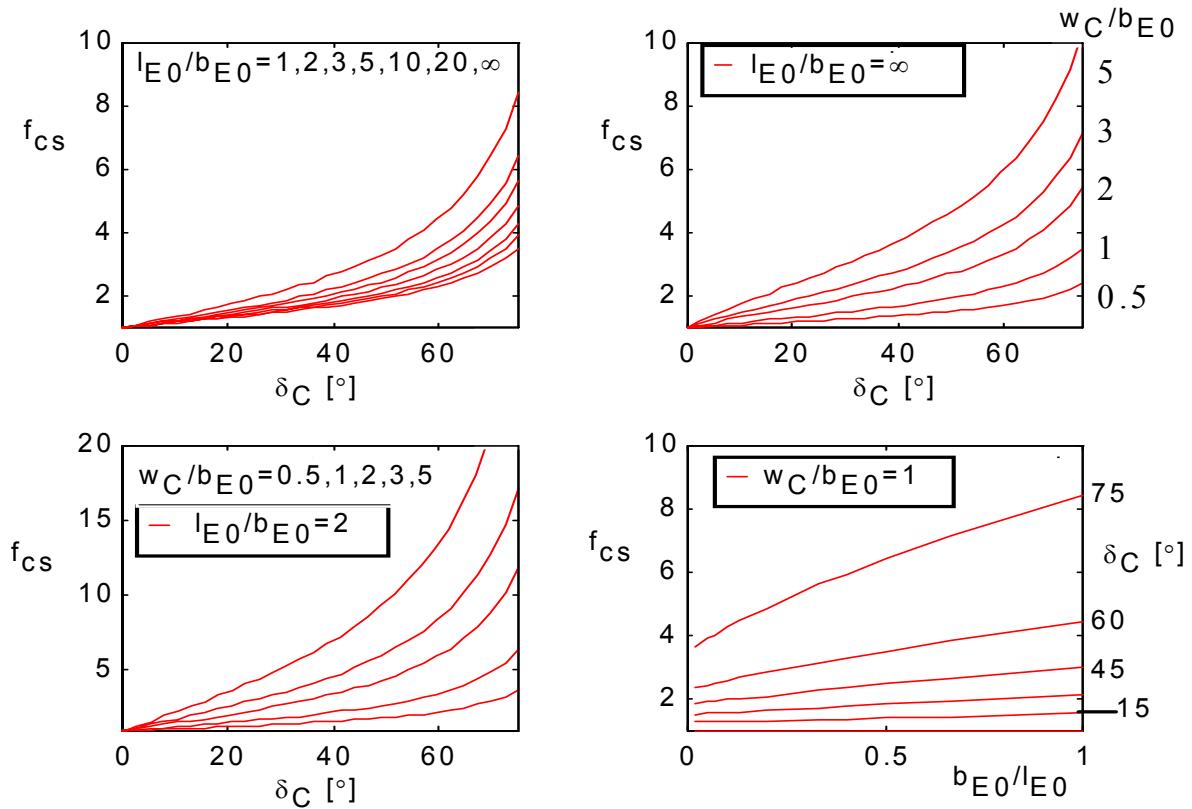


Figure 6-24. Collector current spreading factor vs. current spreading angle and ratio of emitter width to length, respectively, for a variety of parameters; upper left: emitter aspect ratio variation; upper right: variation of epi to emitter width for a long stripe transistor; lower left: same as before, but for a short transistor; lower right: variation of angle (in degrees).

18.6 High current densities

If the transistor enters the high-current region, minority charge is stored in the collector within the injection zone w_i which is strongly bias dependent. This width also depends on the collector current spreading angle and can be calculated as:

$$w_i = w_C \begin{cases} \frac{\kappa - 1}{\zeta_l - \kappa \zeta_b} & , l_{E0} > b_{E0} \\ \frac{1}{\zeta_b} \left[\frac{1 + \zeta_b}{1 + i_{ck} \zeta_b} - 1 \right] & , l_{E0} = b_{E0} \end{cases} \quad (18.6-1)$$

with:

$$\kappa = \frac{1 + \zeta_l}{1 + \zeta_b} \exp \left[i_{ck} \ln \left(\frac{1 + \zeta_b}{1 + \zeta_l} \right) \right] = \left(\frac{1 + \zeta_b}{1 + \zeta_l} \right)^{i_{ck}-1} \quad (18.6-2)$$

and the normalized current:

$$i_{ck} = 1 - \frac{i + \sqrt{i^2 + a_{hc}}}{1 + \sqrt{1 + a_{hc}}} \quad \text{with} \quad i = 1 - \frac{I_{CK}}{I_{Tf}} \quad (18.6-3)$$

[Figure 6-25](#) shows the normalized injection width as a function of normalized (forward) collector current with the current spreading angle δ_C as a parameter. $\delta_C=0$ corresponds to the 1D case; with increasing spreading angle, the current density in the collector is reduced and, therefore, the extension of the injection width decreases relative to the 1D case. Compared to long transistors (Fig. (a)), which correspond to the 2D case with $l_E \gg b_E$, the impact of current spreading is smaller than for a square-emitter transistor (Fig. (b)), since in the latter the current can spread in all four directions.

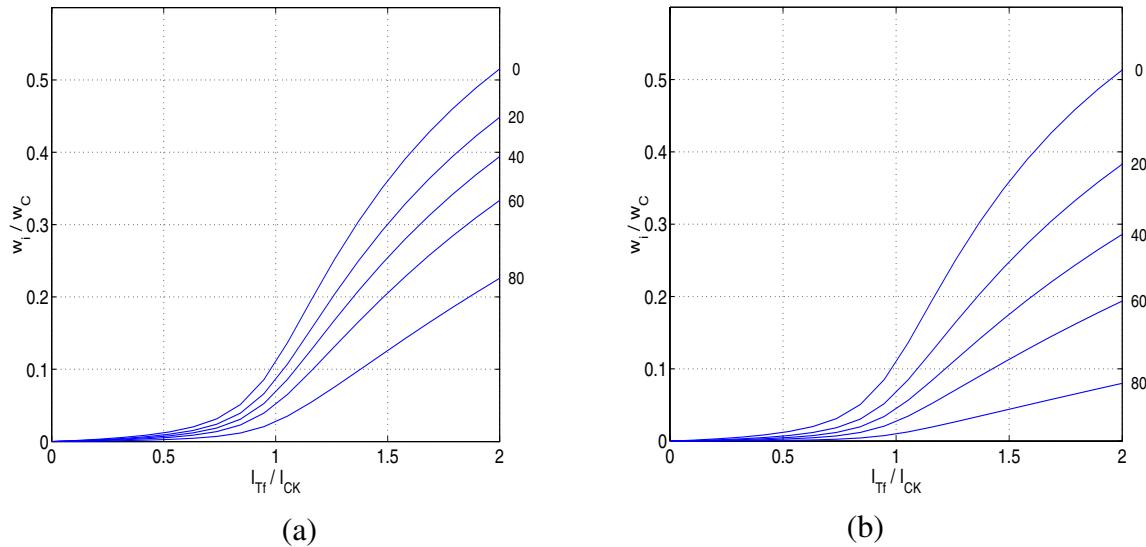


Figure 6-25. Normalized injection width as a function of normalized (forward) collector current for various current spreading angles d_C : (a) long emitter $I_E \gg b_E$; (b) square-emitter $I_E = b_E$. Parameters: $w_C/b_E = 1$, $a h c = 0.05$, $w_C/I_E = 0.01$ for (a) and $w_C/I_E = 1$ for (b).

Also, the equations for τ_{pC} and Q_{pC} have to be extended in order to be able to describe the bias dependence of the occurring 2D and 3D current spreading effects [44]:

$$Q_{fC} = \tau_{pCS} I_{Tf} \begin{cases} 2 \frac{f_{Ci} \ln\left(\frac{1 + \zeta_b w}{1 + \zeta_l w}\right) - f_{Cb} + f_{Cl}}{\zeta_b - \zeta_l}, & l_{E0} > b_{E0} \\ \frac{1 + \zeta_b w / 3}{1 + \zeta_b w}, & l_{E0} = b_{E0} \end{cases} \quad (18.6-4)$$

with $w=w_i/w_C$ as normalized injection width, $\tau_{pCS}=f_{thc}\tau_{hcs}$, and the auxiliary (bias dependent) functions:

$$f_{Ci} = w + \frac{\zeta_b + \zeta_l}{2} w^2 + \frac{\zeta_b \zeta_l}{3} w^3 \quad (18.6-5)$$

$$f_{Cb} = \frac{1}{\zeta_b} \left(1 - \frac{\zeta_l}{\zeta_b} \right) \left[\frac{x^2 [2 \ln x - 1] + 1}{4} \right] + \frac{1}{\zeta_b} \frac{\zeta_l}{\zeta_b} \left[\frac{x^3 [3 \ln x - 1] + 1}{9} \right] \quad (18.6-6)$$

with $x = 1 + \zeta_b w$ and

$$f_{Cl} = f_{Cb} (\zeta_b \leftrightarrow \zeta_l) \quad (18.6-7)$$

i.e. f_{Cl} has the same form as f_{Cb} but with ζ_b and ζ_l interchanged.

In the implementation of these equations, potential divisions by zero, that could occur for $\zeta_b = 0$ or $\zeta_l = 0$ or $\zeta_b = \zeta_l = 0$ (1D case), have been taken into account by appropriate series expansions, which then also include the 1D theory described before.

The base charge component at high current densities, ΔQ_{fb} , is still calculated without current spreading, using the saturation storage time $\tau_{BfvS} = \tau_{hcs} (1 - f_{thc})$.

18.7 Depletion charges and capacitances

Internal capacitances and charges are scaled with the effective emitter area.

Scaling of external capacitances and charges depends on their physical origin:

- The geometry dependent peripheral BE depletion capacitance is calculated from the difference between the total and “effective” internal BE capacitance.
- The various components of the external BC depletion capacitance are calculated from the corresponding capacitance per area or perimeter (“specific” values) times the respective area or perimeter, with the latter one including corner contributions as well.
- The CS capacitance components are calculated from their respective specific values and the buried layer bottom area as well as from the dimensions of the peripheral substrate junction. [Figure 6-26](#) shows the various components that contribute to the peripheral CS depletion capacitance of a junction isolated bipolar transistor.

Also, BC and CS capacitance values can be predicted by the parameter extraction tool based on collector doping and specific substrate resistance.

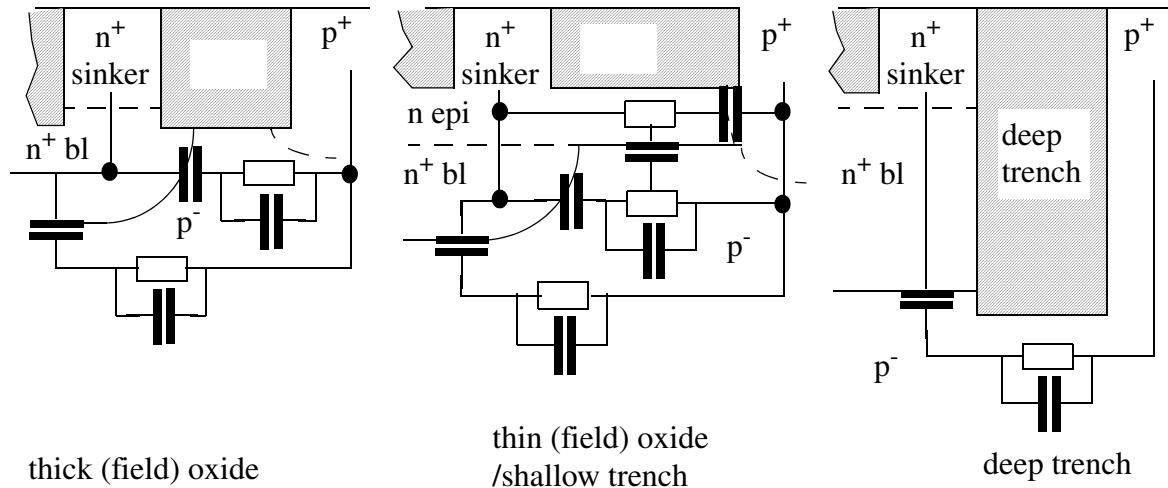


Figure 6-26. Process variants of the CS junction, including components for modelling the depletion capacitance and intra-device substrate coupling.

18.8 Series resistances

The series resistances of a bipolar transistor depend strongly on geometry and contact configuration of the respective transistor. The geometry scaling of the internal and external base resistance is described in [28], [37], [39].

The external series resistances r_E and r_{Cx} can be calculated by the parameter extraction tool from specific resistances, sheet resistances and design rules, taking into account various transistor configurations. This method, which allows an independent determination of series resistances, is believed to be more accurate and flexible than (“direct”) extraction from measurements since reliable methods for measuring these resistances do not exist. Most measurement methods are either applicable to a particular process, a certain bias range, or a certain transistor operation (d.c. or small-signal), and validity limits are often unknown or difficult to assess.

18.9 Breakdown

The avalanche effect formulation contains only q_{AVL} as directly area dependent parameter, besides variables such as transfer current and internal BC capacitance, the scaling of which is already being taken care of.

Under the assumption that in a modern bipolar transistor tunnelling occurs at the emitter periphery junction, the geometry dependence is given by the perimeter P_E of the emitter.

18.10 Parasitic substrate transistor

Since it is assumed that for most bipolar processes the substrate transistor is determined by its peripheral component, all current related parameters are scaled by the CS perimeter length. The CS depletion capacitance was already discussed before. The transit time scales vertically with the distance between the epi-substrate and the BC junction.

18.11 Self-heating

Presently, R_{th} and C_{th} are scaled as follows with the effective emitter dimensions,

$$R_{th} = r_{th} f_{th} \quad \text{and} \quad C_{th} = c_{th} / f_{th} \quad (18.11-1)$$

with the geometry function [13]:

$$f_{th} = \frac{\ln(4l_E/b_E)}{l_E} \quad (18.11-2)$$

r_{th} and c_{th} are the parameter extraction tool parameters, that are defined for a *reference* structure with $b_{E,ref}$ and $l_{E,ref}$. This scaling rule is certainly a rough approximation and has to be verified for a given processes.

Figure 6-27 shows the dependence of the thermal resistance on emitter width for constant emitter length. The variation is quite small and could also be described

by a simple linear function. More measurement results are needed to establish a reliable geometry scaling rule for the thermal elements.

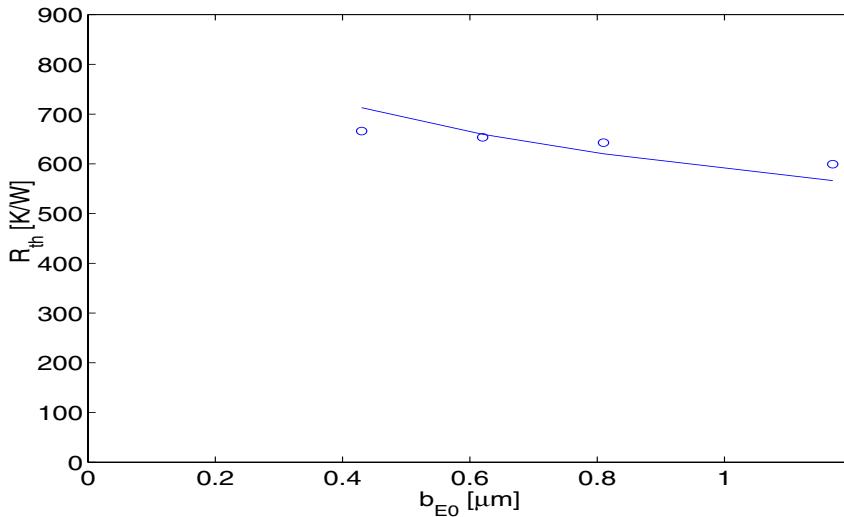


Figure 6-27. Thermal resistance as a function of emitter width at constant emitter length: comparison between measurements (symbols) and analytical equation (line)

19.0 Model Parameter List for HICUM

Conventionally, the complete set of model parameters has to be specified by a “.model card”. The corresponding list of parameters is given below.

The following list is divided into parameters related to the internal transistor, the emitter periphery, the external transistor and in parameters for additional physical effects such as noise and temperature dependence. In addition, every block is subdivided into groups for each element of the equivalent circuit shown in [Figure 6-1](#). Although the total number of model parameters appears to be large, less time and effort has to be spent for model parameter extraction—if the same effects are considered as in the SGPM—due to (a) the physical nature and modularity of the model formulation and (b) the reliable and clearly defined extraction procedure.



Note Not every parameter always has to be specified for a particular process or application in order to achieve the required accuracy. For example, certain parameters are related to HBTs and, therefore, can be left at their default values for homojunction transistors.

Many HICUM parameters have been chosen as simple factors, that are related to physically meaningful basic parameters like a capacitance, charge or transit time. This choice significantly reduces changes (and the probability of errors) in the parameter list if the basic parameters are changed for, e.g. statistical simulation, because the factors often assume very similar values even for different process technologies.

The “factor” in the last column contains information about the type of calculation for the corresponding model parameter in case M (> 1) devices are connected in parallel: multiplication of the parameter value is indicated by M while division is indicated by 1/M and no reaction by leaving the entry blank. Caution is required if the factor is applied to r_{su} , R_{th} and C_{th} . In the latter case, no thermal interaction between the devices is assumed for simple scaling to be valid.

Nr.	Name	Description	Default	Units	Factor
1	LEVEL	Model level for Eldo	9		
2	VERSION	Version control parameter	2.1		
Internal Transistor					
Transfer Current					
3	TNOM	Temperature at which the parameters are specified	27	°C	
4	IS (C10)	Transport saturation current ($C_{10}=IS \cdot Q_{P0}$)	1×10^{-16} 2×10^{-30}	A	
5	QPO	Zero-bias hole charge	2×10^{-14}	C	M
6	ICH	High-current correction for 2D and 3D effects	1×10^{20}	A	M
7	HFC	Collector minority charge weighting factor in HBTs	1.0		
8	HFE	Emitter minority charge weighting factor in HBTs	1.0		

Nr.	Name	Description	Default	Units	Factor
9	HJCI	b-c depletion charge weighting factor in HBTs	1.0		
10	HJEI	b-e depletion charge weighting factor in HBTs	1.0		
11	MCF	non-ideality factor in III-V HBTs (caused by e.g. thermionic emission)	1.0		
Base-Emitter Current Components					
12	IBEIS	Internal b-e saturation current	1×10^{-18}	A	M
13	MBEI	Internal b-e non-ideality factor	1		
14	IRESIS	Internal b-e recombination saturation current	1×10^{-30}	A	M
15	MREI	Internal b-e recombination non-ideality factor	2		
16	IBEPS	Peripheral b-e saturation current	1×10^{-30}	A	M
17	MBEP	Peripheral b-e non-ideality factor	1		
18	IРЕPS	Peripheral b-e recombination saturation current	1×10^{-30}	A	M
19	MREP	Peripheral b-e recombination non-ideality factor	2		
Base-Collector Current Components					
20	IBCIS	Internal b-c saturation current	1×10^{-16}	A	M
21	MBCI	Internal b-c non-ideality factor	1		
22	IBCXS	External b-c saturation current	1×10^{-30}	A	M
23	MBCX	External b-c non-ideality factor	1		
Base-Emitter Tunneling Current					
24	IBETS	b-e tunneling saturation current	0	A	M
25	ABET	Exponent factor of tunneling current	40		
Base-Collector Avalanche Current					
26	FAVL	Factor of avalanche current	0	V^{-1}	
27	QAVL	Exponent factor of avalanche current	0	C	M
Series Resistances					
28	RBI0	Zero-bias internal base series resistance	0	Ω	M^{-1}
29	RBX	External base series resistance	0	Ω	M^{-1}
30	FGE0	Factor for geometry dependence of emitter current crowding	0.6557		
31	FDQR0	Correction factor for modulation by the b-e and b-c space charge region	0		
32	FCRBI	Ratio of HF shunt to total internal capacitance	0		
33	RE	Emitter series resistance	0	Ω	M^{-1}
34	RCX	External collector series resistance	0	Ω	M^{-1}

Nr.	Name	Description	Default	Units	Factor
Substrate Transistor					
35	ITSS	Saturation transfer current of substrate transistor	1×10^{-30}	A	M
36	MSF	Forward non-ideality factor of substrate transistor	1		
37	ISCS	Saturation current of c-s diode	1×10^{-30}	A	M
38	MSC	Non-ideality factor of the c-s diode	1		
39	TSF	Transit time of the substrate transistor	0	s	
40	ZETACX	Temperature coefficient of <i>TSF</i>	0		
Collector Substrate Coupling Network (Intra Device)					
41	RSU	Substrate coupling series resistance	0	Ω	M^{-1}
42	CSU	Substrate coupling capacitance	0	F	
Junction Capacitances					
Base-Emitter Junction Capacitance					
43	CJEI0	Internal b-e zero-bias depletion capacitance	0	F	M
44	VDEI	Internal b-e built-in potential	0.9	V	
45	ZEI	Internal b-e grading coefficient	0.5		
46	ALJEI	Factor for adjusting the maximum value of the internal b-e depletion capacitance	2.5		
47	CJEP0	Peripheral b-e zero-bias depletion capacitance	1×10^{-25}	F	M
48	VDEP	Peripheral b-e built-in potential	0.9	V	
49	ZEP	Peripheral b-e grading coefficient	0.5		
50	ALJEP	Factor for adjusting the maximum value of the peripheral b-e depletion capacitance	2.5		
Base-Collector Junction Capacitance					
51	CJCI0	Internal zero-bias b-c depletion capacitance	0	F	M
52	VDCI	Internal b-c built-in potential	0.7	V	
53	ZCI	Internal b-c grading coefficient	0.4		
54	VPTCI	Internal b-c punch-through voltage	1×10^{20}	V	
55	CJCX0	Internal b-c zero-bias depletion capacitance	0	F	M
56	VDCX	External b-c built-in potential	0.7	V	
57	ZCX	External b-c grading coefficient	0.4		
58	VPTCX	External b-c punch-through voltage	1×10^{20}	V	
Collector-Substrate Junction Capacitance					
59	CJS0	c-s zero-bias depletion capacitance	0	F	M
60	VDS	c-s built-in potential	0.6	V	

Nr.	Name	Description	Default	Units	Factor
61	ZS	c-s grading coefficient	0.5		
62	VPTS	c-s punch-through voltage	1×10^{20}	V	
Diffusion Capacitances					
Base-Emitter Diffusion Capacitance					
63	TO	Forward low-current transit time at $V_{BC} = 0$ V	0	s	
64	DTOH	Time constant for base and b-c space charge region width modulation	0	s	
65	TBVL	Modeling carrier jam at low V_{CE}	0	s	
66	TEFO	Neutral emitter transit time	0	s	
67	GTFE	Exponent for current dependent emitter transit time	1		
68	THCS	Saturation time constant at high current densities	0	s	
69	ALHC	Smoothing factor for current dependence of base and collector transit time	0.1		
70	FTHC	Partitioning factor for base and collector portion	0		
71	RCIO	Internal collector resistance at low electric field	150	Ω	M^{-1}
72	VLIM	Voltage separating ohmic and space charge region regime	0.4	V	
73	VPT	Collector punch-through voltage	3	V	
74	VCES	Internal c-e saturation voltage	0.1	V	
75	TR	Reverse transit time	0	s	
Isolation Capacitances					
76	CEOX	b-e isolation capacitance	0	F	M
77	CCOX	b-c isolation capacitance	0	F	M
78	FBC	Partitioning factor for external b-c capacitance	0		
Non-Quasi-Static Effects					
79	ALQF	Factor for additional delay time of Q_F	0		
80	ALIT	Factor for additional delay time of I_T	0		
Noise					
81	KF	Flicker noise coefficient	0		
82	AF	Flicker noise exponent factor	2		
Lateral Scaling					
83	LATB	Scaling factor for collector minority charge in direction of the emitter width W_E	0		
84	LATL	Scaling factor for collector minority charge in direction of the emitter length l_E	0		

Nr.	Name	Description	Default	Units	Factor
85	FQI	Ratio of internal to total minority charge	1		
Temperature Dependence					
86	VGB	Bandgap-voltage at 0°K	1.17	°K ⁻¹	
87	ALB	Relative temperature coefficient of forward current gain	5×10 ⁻³	°K ⁻¹	
88	ALTO	First-order relative temperature coefficient of t_{f0}	0	°K ⁻¹	
89	KTO	Second-order relative temperature coefficient of t_{f0}	0	°K ⁻²	
90	ZETACI	Temperature exponent factor of r_{Ci0}	0		
91	ALVS	Relative coefficient of saturation drift velocity	0	°K ⁻¹	
92	ALCES	Relative coefficient of V_{CES}	0	V°K ⁻¹	
93	ZETARBI	Temperature exponent of internal base resistance	0		
94	ZETARBX	Temperature exponent factor of external base	0		
95	ZETARCX	Temperature exponent of external collector	0		
96	ZETARE	Temperature exponent of emitter resistance	0		
97	ALFAV	Relative temperature coefficient for F_{AVL}	8.3×10 ⁻⁴	°K ⁻¹	
98	ALQAV	Relative temperature coefficient for Q_{AVL}	2.0×10 ⁻³	°K ⁻¹	
Self Heating					
99	RTH	Thermal resistance	0	°KΩ ⁻¹	M ⁻¹
100	CTH	Thermal capacitance	0	Ws°K ⁻¹	M

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Chapter 7

Mextram 504 Equations

1.0 Introduction

This is the implementation of the Philips Mextram Bipolar Model 504 in Eldo. The basis of this work is the unclassified report NL-UR 2000/811 published by Philips Nat.Lab., April 2001. The Mextram 504 model is implemented in Eldo as LEVEL=22.

Mextram 504 has two main improvements with respect to Mextram 503. The description of the currents and changes is much smoother as a function of bias, and the parameter extraction has been improved.

- The increased smoothness results in a better description of the characteristics, of the first-order derivatives (like the output conductance and the cut-off frequency) and of the higher-order derivatives (like the third-order harmonic distortion).
- The parameter extraction of Mextram 504 has been made more transparent by making the various parts of the model more independent of each other. This means that parameters can more easily be changed without influencing other parts of the model. A few transit-time parameters have been added to increase the flexibility of the cut-off frequency description. The improved parameter extraction also leads to a better description.

The Mextram model gives a good description of bipolar transistors in all kinds of processes. It also scales excellently over temperature and geometry.

Mextram 504 has two special formulations dedicated to the description of *SiGe* transistors (an improved Early-effect description and the addition of neutral-base recombination).

Mextram 504.1 is the new version of Mextram 504 released by Philips in September 2001 and updated in March 2002. It includes the following enhancements:

- Model Enhancements
 - Lower bound on R_{th} is now 0°C/W.
 - Small changes in F_{ex} and Q_{b1b2} to enhance robustness.
- Changes in implementation for improved numerical stability
 - Numerical stability improvement of X_i / W_{epi} at small V_{c1c2} .
 - Numerical stability of P_θ^* .



For further information, please refer to the Philips Nat.Lab. unclassified report [NL-UR 2000/811 “The Mextram Bipolar Transistor Model, level 504”](#) by J.C.J Paasschens and W.J Kloosterman and the Philips Nat.Lab. unclassified report [NL-UR 2002/806 “Model derivation of Mextram 504, The physics behind the model”](#) by J.C.J Paasschens, W.J Kloosterman, and R. v.d. Toorn.

2.0 Model Parameters

The parameters denoted with a ‘*’ are not used in the DC model.

Nr.	Name	Description	Default	Units	Clip Low	Clip High
1	LEVEL	Model level, must be set to 22	22			
2	VERSION	Model version, can be either 504 or 504.1	504.1			
3	MULT	Multiplication factor	1.0		0.0	
4	TREF	Reference temperature	25°C	°C	-273.15	
5	DTA	Difference between the device temperature and ambient temperature $T_{device} = T_{ambient} + DTA$	0.0	°C		

Nr.	Name	Description	Default	Units	Clip Low	Clip High
6	EXMOD	Flag for extended modelling of the reverse current gain	1.0		0.0	1.0
7	EXPHI	*Flag for the distributed high-frequency effects in transient	1.0		0.0	1.0
8	EXAVL	Flag for extended modelling of avalanche currents	0.0		0.0	1.0
9	IS	Collector-emitter saturation current	22.0×10^{-18}	A	0.0	
10	IK	Collector-emitter high injection knee current	0.1	A	1.0×10^{-12}	
11	VER	Reverse Early voltage	2.5	V	0.01	
12	VEF	Forward Early voltage	44.0	V	0.01	
13	BF	Ideal forward current gain	215.0		1.0×10^{-4}	
14	IBF	Saturation current of the non-ideal forward base current	2.7×10^{-15}	A	0.0	
15	MLF	Non-ideality factor of the non-ideal forward base current	2.0		0.1	
16	XIBI	Part of ideal base current that belongs to the sidewall	0.0		0.0	0.1
17	BRI	Ideal reverse current gain	7.0		1.0×10^{-4}	
18	IBR	Saturation current of the non-ideal reverse base current	1.0×10^{-15}	A	0.0	
19	VLR	Cross-over voltage of the non-ideal reverse base current	0.2	V		
20	XEXT	Part of I_{ex} , Q_{tex} , Q_{ex} and I_{sub} that depends on V_{BC1} instead of V_{BIC1}	0.63		0.0	0.1
21	WAVL	Epilayer thickness used in weak-avalanche model	1.1×10^{-6}	m	1.0×10^{-9}	
22	VAVL	Voltage determining curvature of avalanche current	3.0	V	0.01	
23	SFH	Current spreading factor of avalanche model (when EXAVL=1)	0.3		0.0	
24	RE	Emitter resistance	5.0	W	1.0×10^{-6}	
25	RBC	Constant part of the base resistance	23.0	W	1.0×10^{-6}	
26	RBV	Zero-bias value of the variable part of the base resistance	18.0	W	1.0×10^{-6}	
27	RCC	Constant part of the collector resistance	12.0	W	1.0×10^{-6}	
28	RCV	Resistance of the un-modulated epilayer	150.0	W	1.0×10^{-6}	
29	SCRCV	Space charge resistance of the epilayer	1250.0	W	1.0×10^{-6}	

Nr.	Name	Description	Default	Units	Clip Low	Clip High
30	IHC	Critical current for velocity saturation in the epilayer	4.0×10^{-3}	A	1.0×10^{-12}	
31	AXI	Smoothness parameter for the onset of quasi-saturation	0.3		0.02	
32	CJE	*Zero-bias emitter-base depletion capacitance	73.0×10^{-15}	F	0.0	
33	VDE	Emitter-base diffusion voltage	0.95	V	0.05	
34	PE	Emitter-base grading coefficient	0.4		0.01	0.99
35	XCJE	*Fraction of the emitter-base depletion capacitance that belongs to the sidewall	0.4		0.0	1.0
36	CBEO	*Emitter-base overlap capacitance	0.0		0.0	
37	CJC	*Zero-bias collector-base depletion capacitance	78.0×10^{-15}	F	0.0	
38	VDC	Collector-base diffusion voltage	0.68	V	0.05	
39	PC	Collector-base grading coefficient	0.5		0.01	0.99
40	XP	Constant part of CJC	0.35		0.0	0.99
41	MC	Coefficient for the current modulation of the collector-base depletion capacitance	0.5		0.0	1.0
42	XCJC	*Fraction of the collector-base depletion capacitance under the emitter	32.0×10^{-3}		0.0	1.0
43	CBCO	*Collector-base overlap capacitance	0.0		0.0	
44	MTAU	*Non-ideality factor of the emitter stored charge	1.0		0.1	
45	TAUE	*Minimum transit time of stored emitter charge	2.0×10^{-12}	s	0.0	
46	TAUB	*Transit time of stored base charge	4.2×10^{-12}	s	0.0	
47	TEPI	Transit time of stored epilayer charge	41.0×10^{-12}	s	0.0	
48	TAUR	*Transit time of the reverse extrinsic stored base charge	520.0×10^{-12}	s	0.0	
49	DEG	Band-gap difference over the base	0.0	eV		
50	XREC	Pre-factor of the recombination part of I_{B1}	0.0		0.0	
51	AQBO	Temperature coefficient of the zero bias charge	0.3			
52	AE	Temperature coefficient of the resistivity of the emitter	0.0			
53	AB	Temperature coefficient of the resistivity of the base	0.1			

Nr.	Name	Description	Default	Units	Clip Low	Clip High
54	A_{EPI}	Temperature coefficient of the resistivity of the epilayer	2.5			
55	A_{EX}	Temperature coefficient of the resistivity of the extrinsic base	0.62			
56	A_C	Temperature coefficient of the resistivity of the buried layer	2.0			
57	DVG_{BF}	Band-gap voltage difference of forward current gain	50.0×10^{-3}	V		
58	DVG_{BR}	Band-gap voltage difference of reverse current gain	45.0×10^{-3}	V		
59	V_{GB}	Band-gap voltage of the base	1.17	V	0.1	
60	V_{GC}	Band-gap voltage of the collector	1.18	V	0.1	
61	V_{GJ}	Band-gap voltage recombination emitter-base junction	1.15	V	0.1	
62	DVG_{TE}	*Band-gap voltage difference of emitter stored charge	0.05	V		
63	A_F	Exponent of the Flicker-noise	2.0		0.01	
64	K_F	Flicker-noise coefficient of the ideal base current	20.0×10^{-12}		0.00	
65	K_{FN}	Flicker-noise coefficient of the non-ideal base current	20.0×10^{-12}		0.0	
66	I_{SS}	Base-substrate saturation current	48.0×10^{-18}	A	0.0	
67	I_{KS}	Base-substrate high injection knee current	250.0×10^{-6}	A	1.0×10^{-12}	
68	C_{JS}	*Zero-bias collector-substrate depletion capacitance	315.0×10^{-15}	F	0.0	
69	V_{D_S}	*Collector-substrate diffusion voltage	0.62	V	0.05	
70	P_S	*Collector-substrate grading coefficient	0.34		0.01	0.99
71	V_{GS}	Band-gap voltage of the substrate	1.20	V	0.1	
72	A_S	For a closed buried layer: $A_S = A_C$, and for an open buried layer: $A_S = A_{epi}$	1.58			
73	R_{TH}	Thermal resistance	300	°C/W	1.0×10^{-6}	
74	C_{TH}	*Thermal capacitance	3.0×10^{-9}	J/°C	0.0	

Printing/Plotting States

If a state from the list below is to be monitored by the user, the user has to type in the netlist for a given transistor Q1 to monitor, for example In:

.PLOT DC S (Q1->In)	for DC or
.PLOT AC S (Q1->In)	for AC or
.PLOT TRAN S (Q1->In)	for TRAN

The same is applied to the following list of states:

Monitored Only Under the condition of DBXMOD=1



DBXMOD is an instance parameter that defaults to 0.

Note

The actual currents:

Quantity	Description
In	Main current
Ic1c2	Epilayer current
Ib1b2	Pinched-base current
Ib1	Ideal forward base current
Is	Ideal side-wall base current
Ib2	Non-ideal forward base current
Ib3	Non-ideal reverse base current
Iavl	Avalanche current
Iex	Extrinsic reverse base current
XIex	Extrinsic reverse base current
Isub	Substrate current
XIsub	Substrate current
Isf	Substrate failure current

The actual charges:

Quantity	Description
Q_e	Emitter charge or emitter neutral charge
Q_{te}	Base-emitter depletion charge
SQ_{te}	Sidewall Base-emitter depletion charge
Q_{be}	Base-emitter diffusion charge
Q_{bc}	Base-collector diffusion charge
Q_{tc}	Base-collector depletion charge
Q_{epi}	Epilayer diffusion charge
Q_{b1b2}	AC current crowding charge
Q_{tex}	Extrinsic base-collector depletion charge
XQ_{tex}	Extrinsic base-collector depletion charge
Q_{ex}	Extrinsic base-collector diffusion charge
XQ_{ex}	Extrinsic base-collector diffusion charge
Q_{ts}	Collector-substrate depletion charge

The small-signal equivalent circuit conductance:

Quantity	Description
G_x	Forward transconductance
G_y	Reverse transconductance
G_z	Reverse transconductance
SG_{pi}	Conductance sidewall b-e junction
G_{pix}	Conductance floor b-e junction
G_{piy}	Early effect on recombination base current
G_{piz}	Early effect on recombination base current
G_{mux}	Early effect on avalanche current limiting
G_{muy}	Conductance of avalanche current
G_{mu_z}	Conductance of avalanche current
G_{muex}	Conductance extrinsic b-c junction
XG_{muex}	Conductance extrinsic b-c junction
G_{rcvy}	Conductance of epilayer current
G_{rcvz}	Conductance of epilayer current

Quantity	Description
$Grbvx$	Early effect on base resistance
$Grbvy$	Early effect on base resistance
$Grbvz$	Early effect on base resistance
Gs	Conductance parasitic PNP transistor
XGs	Conductance parasitic PNP transistor
Gsf	Conductance substrate failure current

The small-signal equivalent circuit capacitances:

Quantity	Description
$SCbe$	Capacitance sidewall b-e junction
$Cbex$	Capacitance floor b-e junction
$Cbey$	Early effect on b-e diffusion charge
$Cbez$	Early effect on b-e diffusion charge
$Cbcx$	Early effect on b-c diffusion charge
$Cbcy$	Capacitance floor b-c junction
$Cbcz$	Capacitance floor b-c junction
$Cbcex$	Capacitance extrinsic b-c junction
$XCbcex$	Capacitance extrinsic b-c junction
$Cb1b2$	Capacitance AC current crowding
$Cb1b2x$	idem (only used in transient analysis)
Cts	Capacitance s-c junction

Thermal node voltage:

Quantity	Description
$Vtemp$	Thermal node voltage

Chapter 8

Modella Equations

1.0 Introduction

The Modella (*Model lateral*) model (Eldo Level = 23) developed by Philips provides an accurate model dedicated to lateral PNP devices. This new model is based on a totally new approach, accounting for the complex bi-dimensional structure of lateral transistors. The Modella model allows the simulation of lateral devices using real physically based parameters, instead of using less accurate empirically-modified vertical models, such as Gummel-Poon.

In the design of bipolar analog integrated circuits, greater flexibility is often achieved when both NPN and PNP transistors are incorporated in the circuit design. Many present day bipolar production processes use the conventional lateral PNP as the standard PNP transistor structure. For accurate modeling of such a lateral PNP transistor it is important to take the complex two-dimensional nature of the transistor into account. The physics based Modella model (*Model lateral*) does exactly this. Using a modeling approach whereby the main currents and charges are independently related to bias-dependent minority carrier concentrations. Current crowding effects, high injection effects, and a bias dependent output impedance are all taken into account.

2.0 Modeled Effects

The Modella model accounts for the bi-dimensional structure of lateral PNP devices, modeling physical effects such as:

- Temperature effects.
- Charge storage effects.

- Excess-phase shift for current and storage charges.
- Substrate effects and parasitic PNP.
- High-injection effects.
- Built-in electric field in the base region.
- Bias-dependent Early effect.
- Low-level non-ideal base currents.
- Hard and quasi saturation.
- Weak avalanche.
- Current crowding (DC, AC and Transient) and conductivity modulation of the base resistance.
- Hot carrier effects in the collector epilayer.
- Explicit modeling of inactive regions.
- Split base-collector depletion capacitance.

3.0 Equivalent Circuit

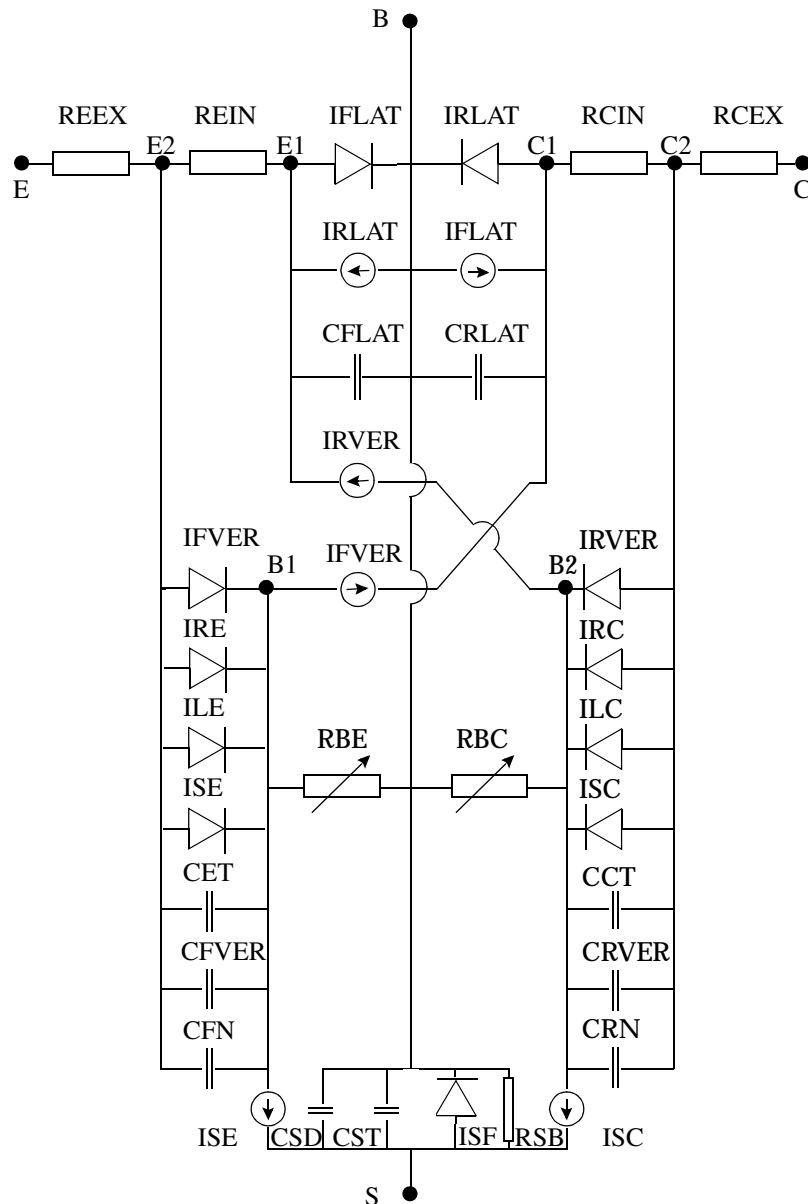


Figure 8-1. Large signal equivalent circuit

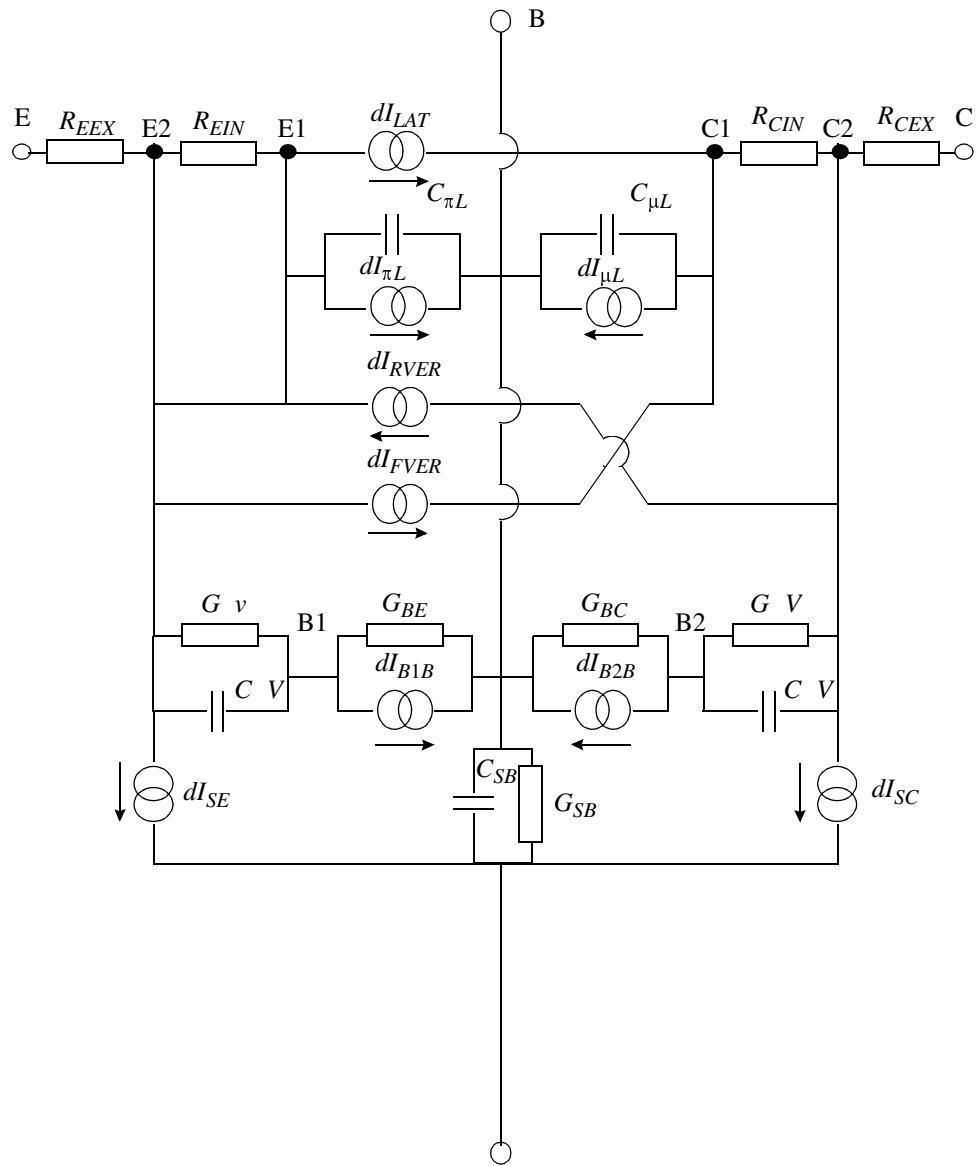


Figure 8-2. AC equivalent circuit

4.0 Documentation



For the full documentation on the Philips Modella model and for further information please visit:
http://www.semiconductors.philips.com/Philips_Models/bipolar/modella/

5.0 Model Parameters

Nr.	Name	Description	Default	Clipping		Units
				Low	High	
1	LEVEL	Model level, must be set to 23	23	-	-	-
2	IS	Collector-emitter saturation current	1.80×10^{-16}	0.0	-	A
3	BF	Ideal forward common-emitter current gain	131.00	1.0×10^{-4}	-	
4	IBF	Saturation current of non-ideal forward base current	2.60×10^{-14}	0.0	-	A
5	VLF	Cross-over voltage of non-ideal forward base current	0.54	-	-	V
6	IK	High injection knee current	1.10×10^{-4}	0.0	-	A
7	XIFV	Vertical fraction of forward current	0.43	0.0	1.0	-
8	EAFL	Early voltage of the lateral forward current component at zero collector-base bias	20.50	0.01	-	V
9	EAFV	Early voltage of the vertical forward current component at zero collector-base bias	75.00	0.01	-	V
10	BR	Ideal reverse common-emitter current gain	25.00	1.0×10^{-4}	-	-
11	IBR	Saturation current of non-ideal reverse base current	1.20×10^{-13}	0.0	-	A
12	VLR	Cross-over voltage of non-ideal reverse base current	0.48	-	-	V
13	XIRV	Vertical fraction of reverse current	0.43	0.0	1.0	-
14	EARL	Early voltage of the lateral reverse current component at zero emitter-base bias	13.10	0.01	-	V
15	EARV	Early voltage of the vertical reverse current component at zero emitter-base bias	104.00	0.01	-	V
16	XES	Ratio between saturation current of e-b-s transistor and e-b-c transistor	2.70×10^{-3}	0.0	-	-
17	XHES	Fraction of substrate current of e-b-s transistor subject to high injection	0.70	0.0	1.0	-
18	XCS	Ratio between the saturation current of c-b-s transistor and c-b-e transistor	3.00	0.0	-	-

Nr.	Name	Description	Default	Clipping		Units
				Low	High	
19	XHCS	Fraction of substrate current of c-b-s transistor subject to high injection	1.00	0.0	1.0	-
20	ISS	Saturation current of substrate-base diode	4.00×10^{-13}	0.0	-	A
21	RCEX	External part of the collector resistance	5.00	1.0×10^{-6}	-	Ω
22	RCIN	Internal part of the collector resistance	47.00	1.0×10^{-6}	-	Ω
23	RBCC	Constant part of the base resistance RBC	10.00	1.0×10^{-6}	-	Ω
24	RBCV	Variable part of the base resistance RBC	10.00	0.0	-	Ω
25	RBE _C	Constant part of the base resistance RBE	10.00	1.0×10^{-6}	-	Ω
26	RBE _V	Variable part of the base resistance RBE	50.00	0.0	-	Ω
27	REEX	External part of the emitter resistance	27.00	1.0×10^{-6}	-	Ω
28	REIN	Internal part of the emitter resistance	66.00	1.0×10^{-6}	-	Ω
29	RSB	Substrate-base leakage resistance	1.00×10^{15}	1.0×10^{-6}	-	Ω
30	TLAT	Low injection (forward and reverse) transit time of charge stored in the epilayer between emitter and collector	2.40×10^{-9}	0.0	-	s
31	TFVR	Low injection forward transit time due to charge stored in the epilayer under the emitter	3.00×10^{-8}	0.0	-	s
32	TFN	Low injection forward transit time due to charge stored in the emitter and the buried layer under the emitter	2.00×10^{-10}	0.0	-	s
33	CJE	Zero-bias emitter-base depletion capacitance	6.10×10^{-14}	0.0	-	F
34	VDE	Emitter-base diffusion voltage	0.52	0.05	-	V
35	P _E	Emitter-base grading coefficient	0.30	0.01	0.99	-
36	TRVR	Low injection reverse transit time due to charge stored in the epilayer under the collector	1.00×10^{-9}	0.0	-	s

Nr.	Name	Description	Default	Clipping		Units
				Low	High	
37	TRN	Low injection reverse transit time due to charge stored in the collector and the buried layer under the collector	3.00×10^{-9}	0.0	-	s
38	CJC	Zero-bias collector-base depletion capacitance	3.90×10^{-13}	0.0	-	F
39	VDC	Collector-base diffusion voltage	0.57	0.05	-	V
40	PC	Collector-base grading coefficient	0.36	0.01	0.99	-
41	CJS	Zero-bias substrate-base depletion capacitance	1.30×10^{-12}	0.0	-	F
42	VDS	Substrate-base diffusion voltage	0.52	0.05	-	V
43	PS	Substrate-base grading coefficient	0.35	0.01	0.99	-
44	TREF	Reference temperature of the parameter set	25.00	-273.15	-	°C
45	DTA	Difference between the device temperature and the ambient analysis temperature	0.00	-	-	°C
46	VGEB	Bandgap voltage of the emitter-base depletion region	1.206	0.1	-	V
47	VGCB	Bandgap voltage of the collector-base depletion region	1.206	0.1	-	V
48	VGSB	Bandgap voltage of the substrate-base depletion region	1.206	0.1	-	V
49	VGB	Bandgap voltage of the base between emitter and collector	1.206	0.1	-	V
50	VGE	Bandgap voltage of the emitter	1.206	0.1	-	V
51	VGJE	Bandgap voltage recombination emitter-base junction	1.123	0.1	-	V
52	AE	Temperature coefficient of BF	4.48	-	-	-
53	SPB	Temperature coefficient of the epitaxial base hole mobility	2.853	-	-	-
54	SNB	Temperature coefficient of the epitaxial base electron mobility	2.60	-	-	-
55	SNBN	Temperature coefficient of buried layer electron mobility	0.30	-	-	-
56	SPE	Temperature coefficient of emitter hole mobility	0.73	-	-	-
57	SPC	Temperature coefficient of collector hole mobility	0.73	-	-	-

Nr.	Name	Description	Default	Clipping		Units
				Low	High	
58	SX	Temperature coefficient of combined minority carrier mobilities in the emitter and buried layer	1.00	-	-	-
59	KF	Flickernoise coefficient	0.00	0.0	-	-
60	AF	Flickernoise exponent	1.00	0.01	-	-
61	EXPHI	Excess phase shift	0.00	0.0	-	rad



The parameter **MULT** in the Philips documentation is treated as a *device* parameter in Eldo and is equivalent to the **M** device parameter in Eldo.



The Modella model is *only* dedicated for Lateral PNP transistors. If an NPN, PNP or LNPN is used then the following warning is issued:

"Modella is a LATERAL PNP BJT model. Please check the model card and refer to the documentation".

6.0 Example of a Modella Model Card

```
.MODEL modella_model LPNP LEVEL=23
+ IS= 1.8E-16 BF= 131.0 IBF= 2.6E-14 VLF= 0.54 IK= 1.1E-04
+ XIFV=0.43 EAFL= 20.5 EAFV= 75.0 BR= 25.0 IBR= 1.2E-13
+ VLR= 0.48 XIRV= 0.43 EARL= 13.1 EARV= 104.0 XES= 2.7E-3
+ XHES= 0.70 XCS= 3.0 XHCS= 1.0 ISS= 4.0E-13 RCEX= 5.0
+ RCIN= 47.0 RBCC= 10.0 RBCV= 10.0 RBE= 10.0 RBEV= 50.0
+ REEX= 27.0 REIN= 66.0 RSB= 1.E15 TLAT= 2.4E-9 TFVR= 3.0E-8
+ TFN= 2.0E-10 CJE= 6.1E-14 VDE= 0.52 PE= 0.3 TRVR= 1.0E-9
+ TRN= 3.0E-9 CJC= 3.9E-13 VDC= 0.57 PC= 0.36 CJS= 1.3E-12
+ VDS= 0.52 PS= 0.35 TREF= 25.00 DTA= 0.0 VGEB = 1.206
+ VGCB= 1.206 VGSB= 1.206 VGB= 1.206 VGE= 1.206 VGJE= 1.123
+ AE= 4.48 SPB= 2.853 SNB= 2.6 SNBN= 0.3 SPE= 0.73 SPC= 0.73
+ SX= 1.0 KF= 1.0 AF= 1.0 EXPHI= 1
```

7.0 DC Operating Point Output

The DC operating point output facility gives information on the state of a device at its operating point. The following table shows the DC operating points that are printed in the *.chi* file in an OP and AC analysis.

DC operating point	Description
REEX	External emitter resistance
REIN	Internal emitter resistance
RCEX	External collector resistance
RCIN	Internal collector resistance
GFL	Forward conductance, lateral path: $\partial I_{FLAT} / \partial V_{E1B1}$
GRL	Reverse conductance, lateral path: $\partial I_{RLAT} / \partial V_{C1B}$
G11	Forward conductance, vertical path: $\partial I_{FVER} / \partial E_{2B1}$
G12	Collector Early-effect on I_{FVER} : $\partial I_{FVER} / \partial V_{C1B}$
G21	Emitter Early-effect on I_{RVER} : $\partial I_{RVER} / \partial V_{E1B}$
G22	Reverse conductance, vertical path: $\partial I_{RVER} / \partial V_{C2B2}$
GPIV	Conductance e-b junction: $\partial (I_{RE} + I_{LE}) / \partial V_{E2B1}$
GMUV	Conductance c-b junction: $\partial (I_{RC} + I_{LC}) / \partial V_{C2B2}$
GBE	Emitter-side: base conductance B1-B: $\partial I_{B1B} / \partial V_{B1B}$
GIBE	Emitter Early-effect on I_{B1B} : $\partial I_{B1B} / \partial V_{E2B1}$
GBC	Collector-side: base conductance B2-B: $\partial I_{B2B} / \partial V_{B2B}$
GIBC	Collector Early-effect on I_{B2B} : $\partial I_{B2B} / \partial V_{C2B2}$
CPIL	Forward diffusion capacitance, lateral path: $\partial Q_{FLAT} / \partial V_{E1B}$
CIPIL	Collector Early-effect on Q_{FLAT} : $\partial Q_{FLAT} / \partial V_{C1B}$
CPIV	Forward total capacitance, vertical path: $\partial (Q_{TE} + Q_{FVER} + Q_{FN}) / \partial V_{E2B1}$
CMUL	Reverse diffusion capacitance, lateral path: $\partial Q_{RLAT} / \partial V_{C1B}$
CIMUL	Emitter Early-effect on Q_{RLAT} : $\partial Q_{RLAT} / \partial V_{E1B}$
CMUV	Reverse total capacitance, vertical path: $\partial (Q_{tc} + Q_{rver} + Q_{rn}) / \partial V_{C2B2}$
GISE	Transconductance (parasitic PNP) e-b-s transistor: $\partial I_{SE} / \partial V_{E2B1}$
GISC	Transconductance (parasitic PNP) c-b-s transistor: $\partial I_{SC} / \partial V_{C2B2}$
GSB	Conductance s-b junction: $(\partial I_{SF} / \partial V_{SB}) + 1/R_{SB}$
CSB	Total capacitance s-b junction: $(\partial Q_{TS} / \partial V_{SB}) + (\partial Q_{SD} / \partial V_{SB})$

The user may print or plot a state from the previous table. To print or plot a state from the table above for $Q1$, a BJT transistor, the following syntax is required:

- For DC
.PLOT DC S (Q1->GBE)
- For AC
.PLOT AC S (Q1->GBE)
- For Transient
.PLOT TRAN S (Q1->GBE)

The same can be applied to all listed in the table.

8.0 References

- Philips Modelbook, Modella Chapter (Chapter 9)
- “MODELLA - A New Physics-Based Compact Model for Lateral p-n-p Transistors”, F.G. O’Hara, J.J.H. van den Biesen, H.C. de Graaff, W.J. Kloosterman and J.B. Foley, IEEE Trans. Electron Devices, vol. ED-39, no. 11, pp. 2553-2561, 1992
- “Physically Based Compact Modelling of Lateral PNP Transistors”, F.G. O’Hara, Philips Research, Nat.Lab. Unclassified Report 2001/804, 2001.

Chapter 9

JFET & MESFET Equations

1.0 Introduction

The JFET model is derived from the FET model of Schichman and Hodges. Special material definitions make it possible to use the same basic equations for both Silicon JFETs and Gallium Arsenide MESFETs.

2.0 Equivalent Circuit Schematics

The diagrams below illustrate the equivalent circuits used for JFET/MESFET in different configurations. The ideal diode equations model are used to determine the current flow through the node's gate-to-drain and the node's gate-to-source.

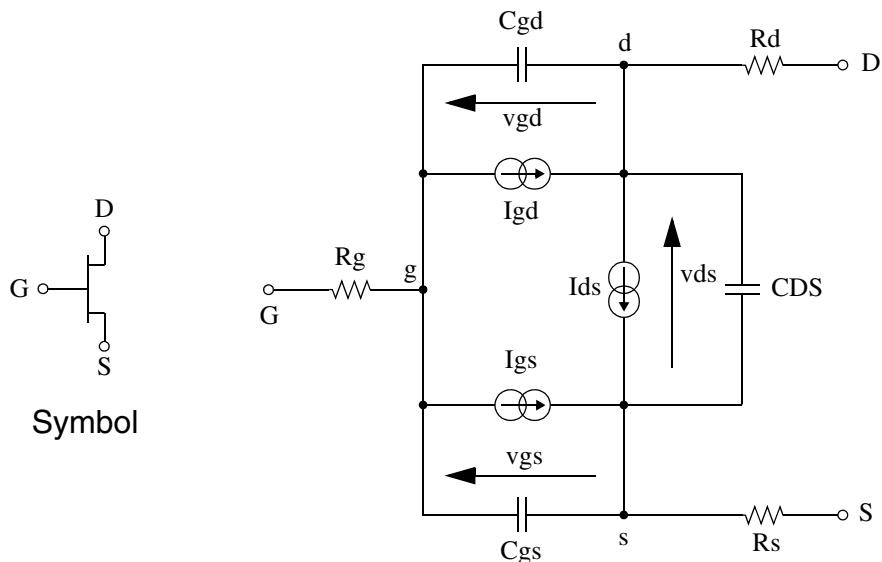


Figure 9-1. Equivalent circuit for DC, TRANSIENT



For DC analysis, gate-drain and gate-source capacitances, CGD and CGS , are not included in the circuit.

For the MESFET models a parasitic resistance, Rg , and a capacitance, CDS , are also included.

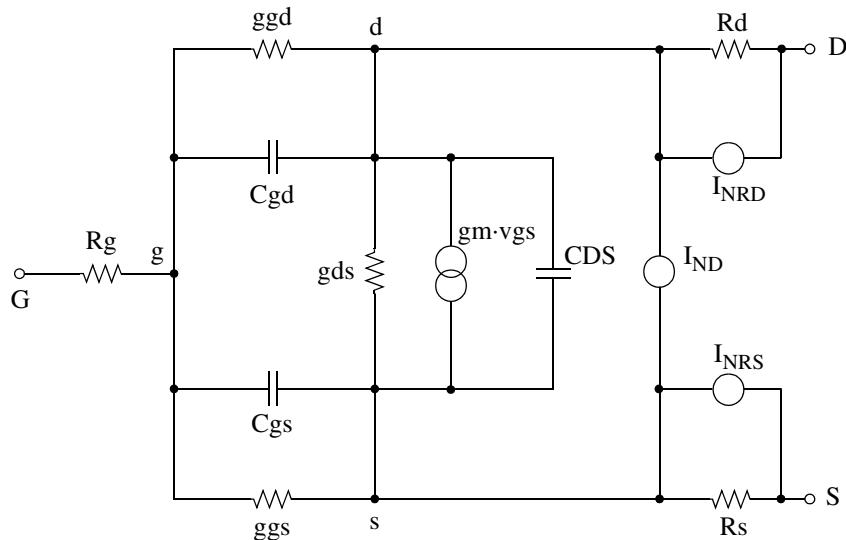


Figure 9-2. Equivalent circuit for AC, NOISE

2.1 Circuit Topology (TOM3)

The TOM3 GD model is defined by a specific subcircuit and a set of device equations. The GD topology utilizes local feedback which decreases the DC output conductance to model drain dispersion and self heating.

The main difference between TOM2 and TOM3 is in the way that the device is modelled. This can be seen in the equivalent circuit, [Figure 9-3](#), where the original TOM2 model is inside the dotted area. For the TOM2 model to be used as an accurate TOM3 model required the addition of external diodes and a Voltage Controlled Voltage Source.

The TOM3 model could be used in a reduced topology (AC/DC) with no external subcircuit elements except the access resistors. However, in this case the diodes,

$D3$ and $D4$, will account for both leakage and forward current components. This is controlled by setting the **GDMOD** parameter to 0 (default) and to switch to the GD topology set **GDMOD=1**.



See the subcircuit listing 9-29 for more information.

Note

GD topology (GDMOD=1)

The GD circuit removes the extrinsic resistors and gate diodes from the FET, defining and scaling them separately as subcircuit elements. The TOM3 large-signal equivalent circuit, Figure 9-3, shows the resistors $\{r_g, r_d$ and $r_s\}$ and gate diodes $\{D1$ and $D2\}$ as separate elements.

The external diodes $\{D1$ and $D2\}$ are standard “library” diode elements which model the forward gate current. The intrinsic diode pair, $\{D3$ and $D4\}$, are internally defined in TOM3 to model reverse gate leakage.

The GD feedback is provided by a voltage controlled voltage source (VCVS) connected to the gate of the intrinsic device. By sampling the output voltage V_{DS} , the VCVS reduces the value of the output conductance for frequencies below the GD corner. The corner frequency for the GD feedback is defined by the RC network and the parameter **TAU_GD**.

AC/DC topology (GDMOD=0)

The outer pair of diodes, D1 and D2, should not exist, and the inner pair, D3 and D4, will account for the forward and leakage current components.

2.2 Gate Current I_G

The gate diodes in TOM2 used the default SPICE model. Additional parameters were needed to model gate leakage currents having little or no temperature dependence. The additional leakage parameters $\{I_{LK}$ and $\varphi_{LK}\}$ were added to the existing model and the source code modified accordingly. The GD topology uses two diode pairs to model the gate current. The outer pair, $\{D_1$ and $D_2\}$, carry the

forward gate currents $\{I_{GS}$ and $I_{GD}\}$ depending upon the external gate voltages $\{V_{GSE}$ and $V_{GDE}\}$. These diodes are “library” diode elements with standard temperature dependence and are based outside of the GD feedback. The forward current diodes are also “ideal” in the sense of having zero junction capacitance and zero series resistance. The reverse leakage currents, $\{I_{LS}$ and $I_{LD}\}$, are carried by diodes $\{D3$ and $D4\}$ depending upon internal voltages $\{V_{GSI}$ and $V_{GDI}\}$ which are inside the GD feedback. The leakage diodes are custom defined by the TOM3 device equations and have no temperature dependence. Both diodes in each pair are assumed identical and use the same parameters.

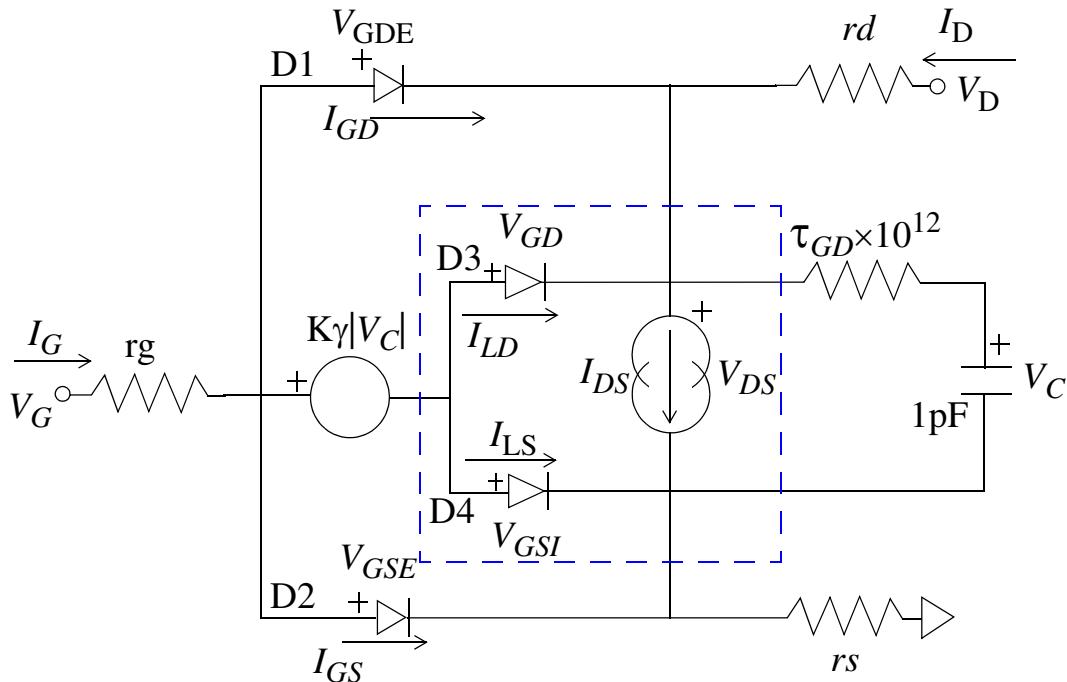


Figure 9-3. GD model circuit topology



The gain of the VCVS is calculated from the absolute value of the capacitor voltage $|V_C|$, making the circuit operate correctly in either the normal ($V_{DS}>0$) or inverted modes ($V_{DS}<0$) if the absolute value of this voltage is not used, the circuit will not work correctly for $V_{DS}>0$.

3.0 Internal Variables

- vds defines the internal drain-source voltage
- vgs defines the internal gate-source voltage
- vgd defines the internal gate-drain voltage.

The different current derivatives are defined as follows:

$$gm = \frac{\delta Ids}{\delta vgs} \quad gds = \frac{\delta Ids}{\delta vds} \quad ggd = \frac{\delta Igd}{\delta vgd} \quad ggs = \frac{\delta Igs}{\delta vgs}$$

4.0 Scaling

$$CGD_{eff} = CGD \cdot AREA \quad CGS_{eff} = CGS \cdot AREA$$

$$CDS_{eff} = CDS \cdot AREA$$

$$IS_{eff} = IS \cdot AREA \quad ISR_{eff} = ISR \cdot AREA$$

$$BETA_{eff} = BETA \cdot AREA$$

4.1 Drain resistance

Parameter scaling method can be selected by the ***RD_SCALE*** parameter:

- for ***RD_SCALE*** = 0: $Rd = \frac{RD}{AREA}$
- for ***RD_SCALE*** = 1: $Rd = AREA \cdot RD$
- for ***RD_SCALE*** = 2: $Rd = RD$

4.2 Source resistance

Parameter scaling method can be selected by the ***RS_SCALE*** parameter:

- for ***RS_SCALE*** = 0: $Rs = \frac{RS}{AREA}$

- for $RS_SCALE = 1$: $R_s = AREA \cdot RS$
- for $RS_SCALE = 2$: $R_s = RS$

4.3 Gate resistance

Parameter scaling method can be selected by the RG_SCALE parameter:

- for $RG_SCALE = 0$: $R_g = \frac{RG}{AREA}$
- for $RG_SCALE = 1$: $R_g = AREA \cdot RG$
- for $RG_SCALE = 2$: $R_g = RG$

5.0 Static Current Equations

5.1 Gate to drain current

$$I_{gd} = IGD_{normal} + IGD_{recomb} + IGD_{ion}$$

If $v_{gd} > MAXARG \cdot N \cdot VT$ then:

$$IGD_{normal} = IS_{eff} \cdot \left(\exp\left(\frac{v_{gd}}{N \cdot VT}\right) - 1 \right) + LGMIN \cdot v_{gd}$$

If $v_{gd} \leq MAXARG \cdot N \cdot VT$ then: $IGD_{normal} = -IS_{eff} + LGMIN \cdot v_{gd}$

only for $Level=2, 7$:

If $ISR = 0.0$ then $IGD_{recomb} = GMIN \cdot v_{gd}$

else $IGD_{recomb} = ISR_{eff} \cdot \left(\exp\left(\frac{v_{gd}}{NR \cdot VT}\right) - 1 \right) \cdot \left(\left(1 - \frac{v_{gd}}{PB} \right)^2 + 5 \cdot 10^{-3} \right)^{\frac{M}{2}}$

only for $Level = 2$:

If $0 < vgs - VTO < vds$ then:

$$IGD_{ion} = Ids \cdot ALPHA \cdot (vds - vgs + VTO) \cdot \exp\left(-\frac{VK}{vds - (vgs - VTO)}\right)$$

else $IGD_{ion} = 0$



- $N = 1$ for **Level** = 1
- **LGMIN=GMIN** for **Level** 1, else **LGMIN** = 0
- **MAXARG** = -10 for **Level** = 2, 3, 6, 8, 9 **MAXARG** = -5 for **Level** = 1, 7.

5.2 Gate to source current

$$Igs = IGS_{normal} + IGS_{recomb} + IGS_{ion}$$

If $vgs > MAXARG \cdot N \cdot VT$ then:

$$IGS_{normal} = IS_{eff} \cdot \left(\exp\left(\frac{vgs}{N \cdot VT}\right) - 1 \right) + LGMIN \cdot vgs$$

If $vgs \leq MAXARG \cdot N \cdot VT$ then: $IGS_{normal} = -IS_{eff} + LGMIN \cdot vgs$

only for **Level** = 2, 7:

If $ISR = 0.0$ then $IGS_{recomb} = GMIN \cdot vgs$

$$\text{else } IGS_{recomb} = ISR_{eff} \cdot \left(\exp\left(\frac{vgs}{NR \cdot VT}\right) - 1 \right) \cdot \left(\left(1 - \frac{vgs}{PB} \right)^2 + 5 \cdot 10^{-3} \right)^{\frac{M}{2}}$$

only for **Level** = 2:

if $0 < vds - VTO < vgs$ then:

$$IGS_{ion} = Ids \cdot ALPHA \cdot (vgs - vds + VTO) \cdot \exp\left(-\frac{VK}{vgs - (vds - VTO)}\right)$$

else $IGS_{ion} = 0$

Gate junction currents if MODLEV=1

$$I_{gs(gd)} = \begin{cases} is \left(e^{\frac{V_{gs(gd)}}{nV_t}} - 1 \right) & \text{if } V_{gs(gd)} \leq V_{Expl} \\ I_{offset} + G_{Expl}V_{gs(gd)} & \text{otherwise} \end{cases}$$

where V_t is the thermal voltage given by $V_t = \frac{kT}{q}$,

$V_{Expl} = nV_t \ln \left[1 + \frac{imelt}{is} \right]$ is the forward explosion voltage,

$G_{Expl} = \frac{(imelt + is)}{nV_t}$ is the conductance at V_{Expl} , and

$I_{offset} = imelt - V_{Expl}G_{Expl}$ is the current linearly extrapolated to $V = 0$ from V_{Expl} .

5.3 Leakage currents—Level 9, Update=3 (TOM3)

$$I_{LS} = I_{LK} \left(1 - \exp\left(\frac{-V_{GSI}}{\varphi_{LK}}\right) \right)$$

$$I_{LD} = I_{LK} \left(1 - \exp\left(\frac{-V_{GDI}}{\varphi_{LK}}\right) \right)$$

$$\therefore G_{LS} = \left(\frac{I_{LK}}{\varphi_{LK}} \right) \left(\exp \left(\frac{-V_{GSI}}{\varphi_{LK}} \right) \right)$$

$$G_{LD} = \left(\frac{I_{LK}}{\varphi_{LK}} \right) \left(\exp \left(\frac{-V_{GDI}}{\varphi_{LK}} \right) \right)$$

6.0 Drain-Source Current Equations

As the device is symmetrical, in the following equations, only the forward region equations are presented. For all models the following definitions are made:

In the forward region ($vds \geq 0$): $Vgst = vgs - VTO$ $vds = vds$

In the reverse region ($vds < 0$): $Vgst = vgd - VTO$ $vds = -vds$

The non-linear current source Ids , represents the DC characteristics of the JFET model and is determined by the following equations:

6.1 IDS current—Level 1

For $Vgst < 0$: $Ids = 0$

For $0 < Vgst < vds$: $Ids = BETA_{eff} \cdot {Vgst}^2 \cdot (1 + LAMBDA_{eff} \cdot vds)$

For $0 < vds < Vgst$:

$$Ids = BETA_{eff} \cdot vds \cdot (2 \cdot Vgst - vds) \cdot (1 + LAMBDA_{eff} \cdot vds)$$

where: $LAMBDA_{eff} = LAMBDA \cdot (1 + LAMBDA \cdot Vgst)$ if $MODLEV=1$,

$LAMBDA_{eff} = LAMBDA$ otherwise.

6.2 IDS current—Level 2

For $V_{gst} < 0$: $Ids = 0$

For $0 < V_{gst} < vds$: $Ids = \text{BETA}_{eff} \cdot V_{gst}^2 \cdot (1 + \text{LAMBDA} \cdot vds)$

For $0 < vds < V_{gst}$:

$$Ids = \text{BETA}_{eff} \cdot vds \cdot (2 \cdot V_{gst} - vds) \cdot (1 + \text{LAMBDA} \cdot vds)$$

6.3 IDS current—Level 3

In the channel pinch-off region ($V_{gst} < 0$): $Ids = 0$

In the saturation region, forward bias ($0 < V_{gst} \leq vds, vgs \geq 0$):

$$Ids = \text{BETA}_{eff} \cdot V_{gst}^2 \cdot (1 + \text{LAMBDA} \cdot (vds - V_{gst}) \cdot (1 + \text{LAM1} \cdot vgs))$$

In the saturation region, reverse bias ($0 < V_{gst} < vds, vgs < 0$):

$$Ids = \text{BETA}_{eff} \cdot vgs^2 \cdot \left(1 - \text{LAMBDA} \cdot (vds - V_{gst}) \cdot \frac{V_{gst}}{VTO} \right)$$

In the linear region ($0 < vds < V_{gst}$): $Ids = \text{BETA}_{eff} \cdot vds \cdot (2 \cdot V_{gst} - vds)$

The non-linear current source Ids , represents the DC characteristics of the MESFET model and is determined by the following equations:

6.4 IDS current—Level 6 (Curtice)

In the pinch-off region ($vgs \leq 0$): $Ids = 0$

In the conduction region ($vgs > VTO$):

$$Ids = \text{BETA}_{eff} \cdot (vgs - VTO)^2 \cdot (1 + \text{LAMBDA} \cdot vds) \cdot \tanh(\text{ALPHA} \cdot vds)$$

6.5 Transient effect

$$Ids = Ids(vgs, vds)_{DC} - \frac{\partial}{\partial vgs} Ids \cdot TAU \cdot \frac{d}{dt} vgs$$

6.6 IDS current—Level 7 (Shichman & Hodge)

In the pinch-off region ($Vgst < 0$): $Ids = 0$

In the saturation region ($0 < Vgst < K \cdot vds$):

$$Ids = BETA_{eff} \cdot Vgst^2 \cdot (1 + LAMBDA \cdot K \cdot vds)$$

In the linear region ($0 < K \cdot vds < Vgst$):

$$Ids = BETA_{eff} \cdot K \cdot vds \cdot (2 \cdot Vgst - K \cdot vds) \cdot (1 + LAMBDA \cdot K \cdot vds)$$

6.7 Transient effect

$$Ids(t) = Ids(vgs(t - TAU), vds(t))$$

6.8 IDS current—Level 8 (Statz)

$Vgst \geq 0$:

In the saturation region ($3/ALPHA > vds > 0$ and $Vgst \geq 0$):

$$Ids = \frac{BETA_{eff} \cdot Vgst^2}{1 + B \cdot Vgst} \cdot \left(1 - \left(1 - \frac{ALPHA \cdot vds}{3}\right)^3\right) \cdot (1 + LAMBDA \cdot vds)$$

In the linear region ($vds \geq 3/ALPHA$ and $Vgst \geq 0$):

$$Ids = \frac{BETA_{eff} \cdot Vgst^2}{1 + B \cdot Vgst} \cdot (1 + LAMBDA \cdot vds)$$

In the pinch-off region ($Vgst < 0$): $Ids = 0$

6.9 IDS current—Level 9, Update=1 (TriQuint)

Level 9, Update = 1 is the implementation of the TriQuint GaAS MESFET model.

In the saturation region ($3/\text{ALPHA} > vds > 0$):

$$IDS0 = \text{BETA}_{eff} \cdot (Vgst + GAMMA \cdot vds)^Q \cdot \left(1 - \left(1 - \frac{\text{ALPHA} \cdot vds}{3}\right)^3\right)$$

In the linear region ($vds \geq 3/\text{ALPHA}$):

$$IDS0 = \text{BETA}_{eff} \cdot (Vgst - GAMMA \cdot vds)^Q \cdot (1 + LAMBDA \cdot vds)$$

Finally: $Ids = \frac{IDS0}{1 + VDELTA \cdot vds \cdot IDS0}$

6.10 IDS current—Level 9, Update=2 (TOM2)

Level 9, Update = 2 is the implementation of the TOM2 model.

$$Ids = \frac{IDS0}{1 + VDELTA \cdot vds \cdot IDS0}$$

where:

$$IDS0 = \text{BETA}_{eff} \cdot VG^Q \cdot FD(\text{ALPHA} \cdot VDS)$$

$$FD(x) = \frac{x}{\sqrt{1+x^2}}$$

$$VG = Q \cdot V_{st} \cdot \ln \left[\exp \left(\frac{Vgst + GAMMA \cdot vds}{Q \cdot V_{st}} \right) + 1 \right]$$

$$V_{st} = (NG + ND \cdot vds) \cdot Vt$$

6.11 IDS current—Level 9, Update=3 (TOM3)

Level 9, Update = 3 is the implementation of the TOM3 model.

$$I_{DS} = I_0(1 + LAMBDA \cdot V_{DS}C)$$

where:

$$I_0 = BETA(V_G)^Q \cdot f_k$$

$$f_k = \frac{ALPHA \cdot V_{DS}}{[1 + (ALPHA \cdot V_{DS})^k]^{1/k}}$$

$$V_G = Q \cdot V_{ST} \cdot \log[1 + \exp(\mu)]$$

$$\mu = \frac{V_{GSI} - V_{TO} + GAMMA \cdot V_{DS}}{QV_{ST}}$$

$$V_{ST} = V_{ST0}(1 + M_{ST0}V_{DS})$$

The small-signal conductances are computed from:

$$G_M = \left(\frac{Q \cdot BETA \cdot f_k(V_G)^{Q-1}}{1 + \exp(-\mu)} \right) (1 + LAMBDA \cdot V_{DS})$$

$$G_{DS} = LAMBDA \cdot I_0 + g_m \left(GAMMA - \frac{(V_{GSI} - V_{TO} + GAMMA \cdot V_{DS})M_{ST0}}{1 + M_{ST0}V_{DS}} \right) \\ + \left[\left(\frac{QI_0M_{ST0}}{1 + M_{ST0}V_{DS}} \right) + \left(\frac{ALPHA \cdot BETA(V_G)^Q}{[1 + (ALPHA \cdot V_{DS})^k]^{1+1/k}} \right) \right] (1 + LAMBDA \cdot V_{DS})$$

7.0 Capacitance Equations

7.1 Levels 1, 2, 3, 6, 7 calculations

Charge storage is modeled by nonlinear depletion layer capacitances for both gate junctions. These capacitances are defined by parameters **CGS**, **CGD**, **M**, **FC** and **PB**.

The gate-drain capacitance is calculated as follows:

$$\text{If } vgd < FC \cdot PB \text{ then: } Cgd = CGD_{eff} \cdot \left(1 - \frac{vgd}{PB}\right)^{-M}$$

$$\text{otherwise: } Cgd = CGD_{eff} \cdot \frac{1 - FC(1 + M) + \left(M \cdot \frac{vgd}{PB}\right)}{(1 - FC)^{1 + M}}$$

The gate-source capacitance is calculated as follows:

$$\text{If } vgs < FC \cdot PB \text{ then: } Cgs = CGS_{eff} \cdot \left(1 - \frac{vgs}{PB}\right)^{-M}$$

$$\text{otherwise: } Cgs = CGS_{eff} \cdot \frac{1 - FC(1 + M) + \left(M \cdot \frac{vgs}{PB}\right)}{(1 - FC)^{1 + M}}$$

7.2 Levels 8 and 9 calculations

$$Cgs = CGS_{eff} \cdot \frac{K1 \cdot K2}{\sqrt{1 - \frac{V_{new}}{PB}}} + CGD_{eff} \cdot K3$$

$$Cgd = CGS_{eff} \cdot \frac{K1 \cdot K3}{\sqrt{1 - \frac{V_{new}}{PB}}} + CGD_{eff} \cdot K2$$

where:

$$K1 = \frac{1}{2} \left(1 + \frac{(V_{eff} - VTO)}{\sqrt{(V_{eff} - VTO)^2 + VDELT A^2}} \right)$$

$$V_{eff} = \frac{1}{2} \left(vgs + vgd + \sqrt{(vgs - vgd)^2 + \left(\frac{1}{ALPHA}\right)^2} \right)$$

$$K2 = \frac{1}{2} \left(1 + \frac{(vgs - vgd)}{\sqrt{(vgs - vgd)^2 + \left(\frac{1}{ALPHA}\right)^2}} \right)$$

$$K3 = \frac{1}{2} \left(1 - \frac{(vgs - vgd)}{\sqrt{(vgs - vgd)^2 + \left(\frac{1}{ALPHA}\right)^2}} \right)$$

$$V_{new} = \min \left(\left(\frac{1}{2} (V_{eff} + VTO + \sqrt{(V_{eff} - VTO)^2 + VDELT A^2}) \right), VMAX \right)$$

7.3 Capacitance and charge calculations—Level9, Update=3 (TOM3)

High Power Gate Charge

For several decades below I_{max} , the gate charge and channel current closely follow the empirical relation:

$$Q_{GH} \triangleq Q_{CQH} \log \left(1 + \frac{I_{DS}}{Q_{GI0}} \right) + Q_{GSH} V_{GSI} + Q_{GDH} V_{GDI}$$

where “H” denotes “High-power” operation. The voltage derivatives give the capacitances:

$$C_{GSH} = \frac{\delta Q_{GH}}{\delta V_{GSI}} = \left(\frac{Q_{GQH}}{I_{DS} + Q_{GI0}} \right) \left(\frac{\delta I_{DS}}{\delta V_{GSI}} \right) + Q_{GSH}$$

$$C_{GSH} = (g_m + g_{ds}) \left(\frac{Q_{GQH}}{I_{DS} + Q_{GI0}} \right) + Q_{GSH}$$

$$C_{GDH} = \frac{\delta Q_{GH}}{\delta V_{GDI}} = \left(\frac{Q_{GQH}}{I_{DS} + Q_{GI0}} \right) \left(\frac{\delta I_{DS}}{\delta V_{GDI}} \right) + Q_{GDH}$$

$$C_{GDH} = -g_{ds} \left(\frac{Q_{GQH}}{I_{DS} + Q_{GI0}} \right) + Q_{GDH}$$

The constant terms $\{Q_{GSH}$ and $Q_{GDH}\}$ model the “sidewall capacitance”, and the conductance terms are derived from I_{DS} in the *common-gate* frame. Adding the constant Q_{GI0} prevents singularity at the origin but limits the accuracy at low voltage and low current operation.

Low Power Gate Charge

A separate equation is used for “low power” regions where the gate charge is approximated by:

$$Q_{GL} \triangleq qgl + Q_{GCL}(V_{GSI} + V_{GDI})$$

where

$$qgl = Q_{GQ} \exp[Q_{GAG}(V_{GSI} + V_{GDI})] \cosh(Q_{GAD}V_{DS})$$

with the associated (low power) capacitances:

$$C_{GSL} = qgl[Q_{GAG} + Q_{GAD} \tanh(Q_{GAD}V_{DS})] + Q_{GCL}$$

$$C_{GDL} = qgl[Q_{GAG} - Q_{GAD} \tanh(Q_{GAD}V_{DS})] + Q_{GCL}$$

The constant gate charge Q_{GCL} forces equality in equilibrium and is matched to the high power functions.

Transition Function

With separate functions for the low power and high power operating points, a transition function was used to switch between them. A suitable function is an exponential using the device power in the argument:

$$f_T \triangleq \exp[-Q_{GGB}I_{DS}V_{DS}]$$

with derivatives:

$$\begin{aligned}\frac{\delta f_T}{\delta V_{GSI}} &= -Q_{GGB}[I_{DS} + (g_m + g_{ds})V_{DS}]f_T \\ \frac{\delta f_T}{\delta V_{GDI}} &= Q_{GGB}[I_{DS} + g_{ds}V_{DS}]f_T\end{aligned}$$

Combined Gate Charge

The overall gate charge uses the transition function with the separate charge equations, and adds a fixed constant, making:

$$\begin{aligned}Q_{GG} &= Q_{GL}f_T + Q_{GH}(1-f_T) + Q_{GG0}(V_{GSI} + V_{GDI}) \\ Q_{GS} &= Q_{GSL}f_T + Q_{GSH}(1-f_T) + (Q_{GL}-Q_{GH})\left(\frac{\delta f_T}{\delta V_{GSI}}\right) + Q_{GG0} \\ Q_{GD} &= Q_{GDL}f_T + Q_{GDH}(1-f_T) + (Q_{GL}-Q_{GH})\left(\frac{\delta f_T}{\delta V_{GDI}}\right) + Q_{GG0}\end{aligned}$$

8.0 Temperature Effects

$$VTO(T) = VTO + VTOTC \cdot \delta t$$

$$BETA(T) = BETA \cdot 1.01^{BETATC \cdot \delta t}$$

$$IS(T) = IS \cdot \frac{T}{T_{nom}}^{\frac{XTI}{N}} \cdot \exp\left(\frac{\delta t}{T_{nom}} \cdot \frac{EG}{N \cdot Vt}\right)$$

$$ISR(T) = ISR \cdot \frac{T}{T_{nom}}^{\frac{XTI}{NR}} \cdot \exp\left(\frac{\delta t}{T_{nom}} \cdot \frac{EG}{NR \cdot Vt}\right)$$

$$PB(T) = PB \cdot \frac{T}{T_{nom}} - 3 \cdot Vt \cdot \ln\left(\frac{T}{T_{nom}}\right) - EG(T_{nom}) \cdot \frac{T}{T_{nom}} + EG(T)$$

$$\delta T = T - T_{nom}$$

$$RD(T) = RD \cdot (1 + TRG1 \cdot \delta T)$$

$$RS(T) = RS \cdot (1 + TRS1 \cdot \delta T)$$

$$RG(T) = RG \cdot (1 + TRG1 \cdot \delta T)$$

8.1 If MODLEV=1

Transconductance Temperature

$$Beta = Beta \times \left(\frac{T}{T_{nom} + bto}\right)^{bte}$$

$$LAMBDA = LAMBDA \times \left(\frac{T}{T_{nom} + lto}\right)^{lte}$$

$$LAMBDA1 = LAMBDA1 \times \left(\frac{T}{T_{nom} + lto}\right)^{lte}$$

Parasitic Resistors

$$deltaT = T - T_{nom}$$

$$\text{tempFactor} = 1.0 + \text{deltaT}(\text{tc1deltaT} + \text{tc2})$$

$R_{xeff} = \text{tempFactor}R_x$ where x could be g , d or s .

TLEV=0 Gate-Source and Gate-Drain Capacitance

$$cgs = cgs_{nom} \left\{ 1 + mj \left[0.0004(T - T_{nom}) + \frac{(pb - pb_{nom})}{pb} \right] \right\}$$

$$cgd = cgd_{nom} \left\{ 1 + mj \left[0.0004(T - T_{nom}) + \frac{(pb - pb_{nom})}{pb} \right] \right\}$$

Junction Potential

$$pb = pb_{nom} \left(\frac{T}{T_{nom}} \right) - 3V_t \ln \left[\frac{T}{T_{nom}} \right] + E_{g,nom} \left(\frac{T}{T_{nom}} \right) + E_g$$

Energy Band Gap

$$E_g(T) = \begin{cases} eg - \frac{gap1 \times T^2}{T + gap2} & \text{if } tlev = 2 \\ \left(1.17 - \frac{4.73 \times 10^{-4} T^2}{T + 636} \right) & \text{if } tlev = 0 \text{ or } 1 \end{cases}$$

Gate Junction Current

$$is = is_{nom} \left(\frac{T}{T_{nom}} \right)^{xti} \exp \left[\frac{E_{g,nom}}{V_{t,nom}} - \frac{E_g}{V_t} \right]$$

8.2 Levels 2, 3, 7, 8, 9 Update=1 only

$$EG(T) = EG(T_{nom}) + 7.02 \cdot 10^{-4} \cdot \left(\frac{T_{nom}^2}{T_{nom} + 1108} - \frac{T^2}{T + 1108} \right)$$

$$CGS(T) = CGS \cdot \left(1 + M \cdot \left(4 \cdot 10^{-4} \cdot (T - T_{nom}) + 1 - \frac{PB(T)}{PB} \right) \right)$$

$$CGD(T) = CGD \cdot \left(1 + M \cdot \left(4 \cdot 10^{-4} \cdot (T - T_{nom}) + 1 - \frac{PB(T)}{PB} \right) \right)$$

8.3 Level 9, Update=2 only

$$PB(T) = PB + PBTC \cdot \delta T$$

$$VMAX(T) = VMAX + PBTC \cdot \delta T$$

$$ALPHA(T) = ALPHA \cdot 1.01^{ALPHATC \cdot \delta T}$$

$$GAMMA(T) = GAMMA + GAMMATC \cdot \delta T$$

$$CGS(T) = CGS \cdot (1 + CGSTC \cdot \delta T)$$

$$CGD(T) = CGD \cdot (1 + CGDTC \cdot \delta T)$$

8.4 Level 9, Update=3 only

$$V_{ST0} \triangleq VST + VST_TC(T - T_{NOM})$$

$$M_{ST0} \triangleq MST + MST_TC(T - T_{NOM})$$

$$ALPHA(T) = ALPHA \cdot 1.01^{ALPHATC \cdot \delta T}$$

$$GAMMA(T) = GAMMA + GAMMATC \cdot \delta T$$

9.0 Noise

Refer to the noise model in [Figure 9-2 on page 9-2](#).

9.1 Thermal noise

The thermal noise equation applies to **RS** and **RD** resistances as: $I_{NR}^2 = \frac{4kT}{R}$

9.2 Channel noise

The total channel noise is the sum of channel thermal noise and flicker noise contributions:

$$I_{ND}^2 = \frac{8 \times k \times T \times gm}{3} + \frac{KF \times Ids^{AF}}{f}$$

Channel thermal noise

- If .OPTION JTHNOISE=0 or .MODEL ... THMLEV=0:

$$SI = \frac{8 \times k \times T \times gm}{3}$$

- If .OPTION JTHNOISE=1 or .MODEL ... THMLEV=1:

$$\text{if } vds > vdsat \text{ then: } SI = \frac{8 \times k \times T \times gm}{3}$$

$$\text{else } SI = 4kT \times (gm + gds)$$

- If .OPTION JTHNOISE=2 or .MODEL ... THMLEV=2:

$$SI = \frac{8kT}{3} \times (gm + gds) \times \left(\frac{3}{2} - \frac{Vdseff}{2VDSAT} \right)$$

$$\text{where } Vdseff = \min(Vds, VDSAT)$$

10.0 JFET Parameters

10.1 Model Parameters for LEVEL= 1, 2 and 3

Nr.	Name	Description	Default			Units
1	LEVEL	Model Selector	1	2	3	
2	MODLEV^a	Model enhancement selector	0	0	0	
DC Related Parameters						
3	VTO	Zero bias threshold voltage	-2	-2	-2	V
4	ALPHA	Ionization coefficient		0		
5	BETA	Transconductance coefficient	10^{-4}	10^{-4}	10^{-4}	AV^{-2}
6	LAMBDA	Channel length modulation coefficient	0	0	0	V^{-1}
7	LAM1	Channel length gate modulation coefficient			0	V^{-1}
8	IS	Gate junction saturation current	10^{-14}	10^{-14}	10^{-14}	A
9	ISR	Gate junction recombination parameter		0		A
10	N	Gate junction emission coefficient		1	1	
11	NR	ISR emission coefficient		2		
12	VK	Ionization knee voltage		0		V
Capacitance Related Parameters						
13	CGD	Zero-bias gate-drain junction capacitance	0	0	0	F
14	CGS	Zero-bias gate-source junction capacitance	0	0	0	F
15	M	Junction capacitance grading coefficient	0.5	0.5	0.5	
16	PB	Built-in gate p-n potential	1	1	1	V
17	FC	Forward depletion capacitance coefficient	0.5	0.5	0.5	
18	TT	Transit time			0	s
19	CAPOP	Capacitor model selector	1	1	2	
Parasitic Resistor Related Parameters						
20	RD	Drain resistance	0	0	0	Ω
21	RS	Source resistance	0	0	0	Ω
22	RD_SCALE	Drain resistance scaling method	0	0	0	
23	RS_SCALE	Source resistance scaling method	0	0	0	
Noise Related Parameters						
24	KF	Flicker noise coefficient	0	0	0	
25	AF	Flicker noise exponent	1	1	1	

Nr.	Name	Description	Default			Units
Temperature Related Coefficients						
26	EG	Bandgap voltage	1.11	1.11	1.11	eV
27	VTOTC	VTO temperature coefficient		0	0	$\text{V}^{\circ}\text{K}^{-1}$
28	BETATC	BETA temperature coefficient		0	0	$\text{V}^{\circ}\text{K}^{-1}$
29	XTI	IS temperature coefficient	3	3	3	
30	TRD1	RD temperature coefficient		0	0	$^{\circ}\text{K}^{-1}$
31	TRS1	RS temperature coefficient		0	0	$^{\circ}\text{K}^{-1}$
32	TMOD	Model temperature	TNOM	TNOM	TNOM	$^{\circ}\text{C}$
33	TNOM	Nominal temperature	27	27	27	$^{\circ}\text{C}$

a. If *MODLEV* is enabled, the following parameters are enabled, see table below.

Table 9-4. MODLEV=1 specific parameters

Name	Description	Default/Unit
LAMBDA1	Channel length gate modulation coefficient	0 V^{-1}
TLEV	EG temp update selector	0
TLEVVC	Capacitance temp update selector (currently TLEVVC=0 is the only enabled level)	0
BTO	Beta temperature offset	$0 \text{ }^{\circ}\text{K}$
BTE	Beta temp. exponent	0
LTO	Lambda & Lambda1 temp. offset	$0 \text{ }^{\circ}\text{K}$
LTE	Lambda & LAMBDA1 temp. exponent	0
GAP1	EG temp. coefficient	$7.02\text{e-}4 \text{ V}^{\circ}\text{K}^{-1}$
GAP2	EG temp offset	$1108 \text{ }^{\circ}\text{K}$
TC1	Access resistance temp. coefficient	$0 \text{ }^{\circ}\text{K}^{-1}$
TC2	Access resistance quadratic temp coefficient	$0 \text{ }^{\circ}\text{K}^{-2}$
IMELT	Gate junction limiting current	1

1.0 MESFET Parameters

1.1 Model Parameters for LEVEL= 6, 7 and 8

Nr.	Name	Description	Default			Units
1	LEVEL	Model selector	6	7	8	
DC Related Parameters						
2	VTO	Zero bias threshold voltage	-2.5	-2.5	-2.5	V
3	ALPHA	Parameter influencing saturation voltage	2	2	2	V ⁻¹
4	BETA	Transconductance coefficient	1.0×10 ⁻⁴	1.0×10 ⁻⁴	1.0×10 ⁻⁴	AV ⁻²
5	LAMBDA	Channel length modulation coefficient	0	0	0	V ⁻¹
6	GAMMA	Static feedback parameter				
7	DELTA	Output feedback parameter				(AV) ⁻¹
8	Q	Power-law parameter				
9	IS	Gate junction saturation current	1×10 ⁻¹⁴	1×10 ⁻¹⁴	1×10 ⁻¹⁴	A
10	ISR	Gate junction recombination parameter		0		A
11	N	Gate junction emission coefficient	1	1	1	
12	NR	ISR emission coefficient		2		
13	VK	Ionization knee voltage		0		V
14	B	Doping tail parameter			0.3	V ⁻¹
15	K	VDS multiplication factor		1		
Capacitance Related Parameters						
16	CGD	Zero-bias gate-drain junction capacitance	0	0	0	F
17	CGS	Zero-bias gate-source junction capacitance	0	0	0	F
18	CDS	Drain-source capacitance	0	0	0	F
19	M	Junction capacitance grading coefficient	0.5	0.5	0.5	
20	PB^a	Built-in gate p-n potential	1	1	1	V
21	FC	Forward depletion capacitance coefficient	0.5	0.5	0.5	
22	TAU^b	Conduction current delay time	0	0	0	s
23	TT	Gate delay time	0	0	0	s

Nr.	Name	Description	Default			Units
24	VMAX	Capacitance limiting voltage			0.5	V
25	VDELTA	Capacitance transition voltage			0.2	V
26	CAPOP	Capacitor model selector	1	1		
Parasitic Resistor Related Parameters						
27	RD	Drain resistance	0	0	0	Ω
28	RG	Gate resistance	0	0	0	Ω
29	RS	Source resistance	0	0	0	Ω
30	RD_SCALE	Drain resistance scaling method	0	0	0	
31	RS_SCALE	Source resistance scaling method	0	0	0	
32	RG_SCALE	Gate resistance scaling method	0	0	0	
Noise Related Parameters						
33	KF	Flicker noise coefficient	0	0	0	
34	AF	Flicker noise exponent	1	1	1	
Temperature Related Coefficients						
35	EG	Bandgap voltage	1.52	1.52	1.52	eV
36	VTOTC	VTO temperature coefficient	0	0	0	$V^{\circ}K^{-1}$
37	BETATC	BETA temperature coefficient	0	0	0	$V^{\circ}K^{-1}$
38	XTI	IS temperature coefficient	3	3	3	
39	TRG1	RG temperature coefficient	0	0	0	$^{\circ}K^{-1}$
40	TRD1	RD temperature coefficient	0	0	0	$^{\circ}K^{-1}$
41	TRS1	RS temperature coefficient	0	0	0	$^{\circ}K^{-1}$
42	TMOD	Model temperature	TNOM	TNOM	TNOM	$^{\circ}C$
43	TNOM	Nominal temperature	27	27	27	$^{\circ}C$

- a. In Precise and other simulators the parameter name for **PB** is **VBI**.
- b. In Precise **TAU** is used for the description of the gate delay effect in **Level=1** and **DELAY** in **Level=2**, this is now described by the same parameter with different calculation methods.

1.2 Model Parameters for LEVEL=9, UPDATE=1, 2 and 3

Nr.	Name	Description	Default			Units
1	LEVEL	Model selector	9	9	9	
2	UPDATE	Model sub-selector	1	2	3	
DC Related Parameters						
3	VTO	Zero bias threshold voltage	-2.5	-2.5	-2.5	V
4	ALPHA	Parameter influencing saturation voltage	2	2	2	V ⁻¹
5	BETA	Transconductance coefficient	1.0×10 ⁻⁴	0.1	0.1	AV ²
6	LAMBDA	Channel length modulation coefficient				V ⁻¹
7	GAMMA	Static feedback parameter	0	0	0	
8	DELTA	Output feedback parameter	0	0.2	0.2	(AV) ⁻¹
9	Q	Power-law parameter	2	2	2	
10	IS	Gate junction saturation current	1×10 ⁻¹⁴	1×10 ⁻¹⁴	1×10 ⁻¹⁴	A
11	ISR	Gate junction recombination parameter				A
12	N	Gate junction emission coefficient	1	1	1	
13	NR	ISR emission coefficient				
14	VK	Ionization knee voltage				V
15	B	Doping tail parameter				V ⁻¹
16	K	v _{DS} multiplication factor				
Capacitance Related Parameters						
17	CGD	Zero-bias gate-drain junction capacitance	0	0	0	F
18	CGS	Zero-bias gate-source junction capacitance	0	0	0	F
19	CDS	Drain-source capacitance	0	0	0	F
20	M	Junction capacitance grading coefficient	0.5	0.5	0.5	
21	PB^a	Built-in gate p-n potential	1	1	1	V
22	FC	Forward depletion capacitance coefficient	0.5	0.5	0.5	
23	TAU^b	Conduction current delay time				s
24	TT	Gate delay time	0	0	0	s
25	VMAX	Capacitance limiting voltage	0.5	0.5	0.5	V

Nr.	Name	Description	Default			Units
26	VDELTA		0.2	0.2	0.2	V
27	CAPOP	Capacitor model selector				
Parasitic Resistor Related Parameters						
28	RD	Drain resistance	0	0	0	Ω
29	RG	Gate resistance	0	0	0	Ω
30	RS	Source resistance	0	0	0	Ω
31	RD_SCALE	Drain resistance scaling method	0	0	0	
32	RS_SCALE	Source resistance scaling method	0	0	0	
33	RG_SCALE	Gate resistance scaling method	0	2	2	
Noise Related Parameters						
34	KF	Flicker noise coefficient	0	0	0	
35	AF	Flicker noise exponent	1	1	1	
Temperature Related Coefficients						
36	EG	Bandgap voltage	1.52	1.52	1.52	eV
37	VTOTC	VTO temperature coefficient	0	0	0	$V^{\circ}K^{-1}$
38	BETATC	BETA temperature coefficient	0	0	0	$V^{\circ}K^{-1}$
39	XTI	IS temperature coefficient	3	3	3	
40	TRG1	RG temperature coefficient	0	0	0	$^{\circ}K^{-1}$
41	TRD1	RD temperature coefficient	0	0	0	$^{\circ}K^{-1}$
42	TRS1	RS temperature coefficient	0	0	0	$^{\circ}K^{-1}$
43	TMOD	Model temperature	TNOM	TNOM	TNOM	$^{\circ}C$
44	TNOM	Nominal temperature	27	27	27	$^{\circ}C$

- a. In Precise and other simulators the parameter name for **PB** is **VBI**.
- b. In Precise **TAU** is used for the description of the gate delay effect in **Level=1** and **DELAY** in **Level=2**, this is now described by the same parameter with different calculation methods.

Level 9 (Update=2) specific parameters

Nr.	Name	Description	Default	Units
1	NG	Subthreshold slope gate parameter	0	
2	ND	Subthreshold slope drain parameter	0	V^{-1}
3	ALPHATC	ALPHA temperature coefficient	0	K^{-1}
4	GAMMATC	GAMMA temperature coefficient	0	K^{-1}
5	PBTC	PB temperature coefficient	0	K^{-1}
6	CGDTC	CGD temperature coefficient	0	K^{-1}
7	CGSTC	CGS temperature coefficient	0	K^{-1}

Level 9 (Update=3) specific parameters

Nr.	Name	Description	Default	Units
1	GDMOD	Topology selector	0	
2	ALPHATC	ALPHA temperature coefficient	0	K ⁻¹
3	GAMMATC	GAMMA temperature coefficient	0	K ⁻¹
4	MSTTC	Temperature coefficient of MST	0	V ⁻¹ °K ⁻¹
5	VSTTC	Temperature coefficient of vst	0	V°K ⁻¹
6	K	Knee function order	2	
7	VST	Sub-threshold current coefficient	0.0257	V
8	MST	Sub-threshold current coefficient	0	V ⁻¹
9	ILK	Gate leakage saturation current	0	A
10	PLK	Gate leakage built in potential	2	V
11	QGIO	Removes singularity at $I_{DS}=0$	1×10^{-6}	A
12	QGG0	Fixed constant added to the overall gate charge	0	F
13	QGAG		0.7	V ⁻¹
14	QGAD		0.9	V ⁻¹
15	QGGB		270.0	V ⁻¹ A ⁻¹
16	QGCL		0.3×10^{-15}	F
17	QGSH	Models the sidewall capacitance	0.1×10^{-15}	F
18	QGDH	Models the sidewall capacitance	0.4×10^{-15}	F
19	QGQH		0.3×10^{-15}	C
20	QGQL		0.3×10^{-15}	C

Equivalent name definitions

- *Level 9 (Update=1 and Update= 2)*

VBI is an alias to **PB**

- *Level 9 (Update= 2)*

VBITC is an alias to **VBITCE** which is an alias to **PBTC**

ALPHATCE is an alias to **ALPHATC**

CGSTCE is an alias to **CGSTC**

CGDTCE is an alias to **CGDTC**

- **Level 9 (Update= 3)**

MSTTCE is an alias to **MSTTC**

VSTTCE is an alias to **VSTTC**

QGIO is an alias to **QGI0**

2.0 TOM3 Subcircuit

2.1 GD subckt (GDMOD=1)

```
.Subckt name DRAIN GATE SOURCE W=0 Ng=1
C1 n5  n3  1.0e-1
R1 n1  n5  1.0e7
E1 n4  n2  VALUE={ 0.033*ABS(V(n5,n3)) }           Equation (1)
J1 n1  n2  n3  DLM {W*Ng}
RD DRAIN  n1  {680/(W*Ng)}  TC=0.0044
RS SOURCE  n3  {370/(W*Ng)}  TC=0.016
RG GATE    n4  {.10*W/Ng + 750/(W*Ng)}
D1 n4  n1  Dg {W*Ng}
D2 n4  n3  Dg {W*Ng}
.model dg d Is=15.0e-15 n=1.25 XTI=2.50 Eg=.9
.Model DLM pjf Level=9 update=3 GDMOD=1
+ VTO = 0.5
+ IS = 1E-12
+ N = 1.5
+ XTI = 0
+ EG = 0.9
.ends DFETgd
```

The VALUES (not the connections i.e. nodes) of the different parameters in the subcircuit may be modified as required by the circuit or application EXCEPT for equation (1), which should be left as it is.

2.2 AC/DC subckt (GDMOD=0)

```
.Subckt name DRAIN GATE SOURCE W=0 Ng=1
J1 n1  n2  n3  DLM {W*Ng}
RD DRAIN  n1  { 680 / (W*Ng) }  TC=0.0044
RS SOURCE  n3  { 370 / (W*Ng) }  TC=0.016
RG GATE    n2  { .10*W/Ng + 750 / (W*Ng) }
.Model DLM pjf Level=9 update=3 GDMOD=0
+ VTO = 0.5
.ends DFETgd
```

Chapter 10

Common Equations

1.0 Overview

In this section we discuss the different model equations that may be used for the computation of the extrinsic part of the MOS model, using the 5 parameters **ARLEV (ACM)**, **RLEV**, **ALEV**, **DIOLEV** and **DCAPLEV**. The parameter **ARLEV (ACM)** has priority over **ALEV** and **RLEV**, so if it is specified then **ALEV=RLEV=ARLEV (ACM)** if **.OPTION ACM** or model parameter **OPTACM** is not set.



ACM is an alias to **ARLEV**.

Note

The MOS models that these equations concern are: Level 1, 2, 3, 12, 13, 16, 17, MOSP9 (59), BSIM1 (8), BSIM2 (11), BSIM3v2 (47), BSIM3v3 (53), EKV (44).

1.1 Common Model Parameters

Name	Description	Default	Units
ACM	Flag to control which parasitic models are to be used	0	
OPTACM^a	Flag to enable ACM control over parasitic models	0	
CALCACM^b	Flag to control the area and perimeter calculations when ACM=12	0	

a. The model parameter **OPTACM**, when set to 1, has the same effect as **.option ACM**. The only difference is that the latter affects all of the model cards in the netlist, while the former affects the model card that it is specified in.

b. The model parameter **CALCACM** will accept either 0 (default) or 1. It is used only with **.option ACM** or **OPTACM=1**, and **ACM=12**. By default (**CALCACM=0**), sets the value of **ALEV** to 0 but if it is set to 1, it **ALEV** will be set to 2.

2.0 Equivalent Circuits for MOS Transistors

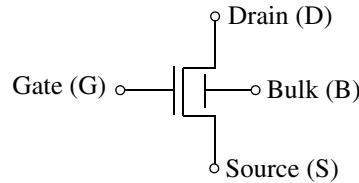


Figure 10-1. Symbol

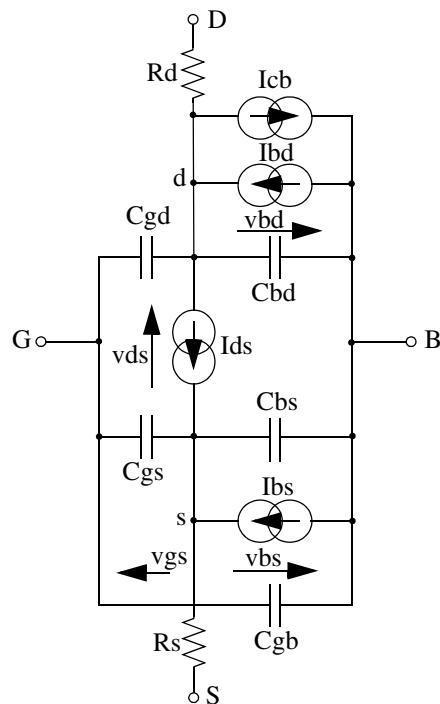


Figure 10-2. Equivalent circuit of “capacitance” style model for DC and TRANSIENT analysis

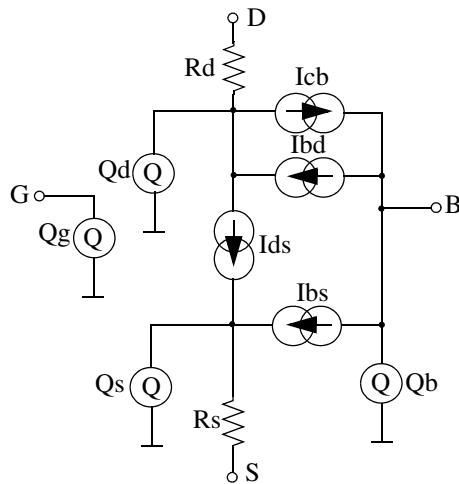


Figure 10-3. Equivalent circuit of “charge” style model for DC and TRANSIENT analysis

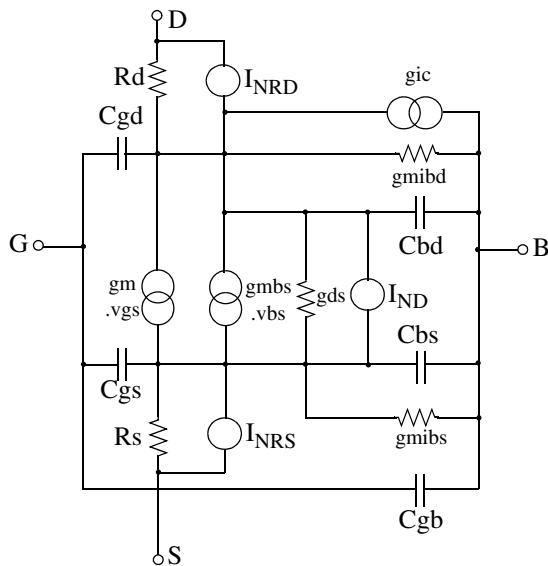


Figure 10-4. Equivalent circuit for AC and NOISE analysis

The main contribution to the MOS behavior is provided by the drain–source current, Ids .

An additional contribution caused by Impact Ionization effects creates another current, Icb .

Both currents are described in the model sections and constitute the intrinsic model behavior.

For AC and noise analysis, the partial derivatives of \mathbf{Ids} with respect to the voltages v_{gs} , v_{ds} , and v_{bs} are used. They are defined as follows:

Transconductance Output conductance Bulk transconductance

$$gm = \frac{\partial Ids}{\partial v_{gs}} \quad gds = \frac{\partial Ids}{\partial v_{ds}} \quad gmb = \frac{\partial Ids}{\partial v_{bs}}$$

In the same way, partial derivatives of Icb are defined as:

$$gicb_{v_{bs}} = \frac{\partial Icb}{\partial v_{bs}} \quad gicb_{v_{ds}} = \frac{\partial Icb}{\partial v_{ds}} \quad gicb_{v_{gs}} = \frac{\partial Icb}{\partial v_{gs}}$$

and they are used as follows:

$$gic = gicb_{v_{bs}} \times v_{bs} + gicb_{v_{ds}} \times v_{ds} + gicb_{v_{gs}} \times v_{gs}$$

The intrinsic currents are represented by the bulk-drain and bulk-source junction currents Ibd and Ibs . The partial derivatives are defined as:

$$gmibs = \frac{\partial Ibs}{\partial v_{bs}} \quad gmibd = \frac{\partial Ibd}{\partial v_{bd}}$$

For dynamic behavior, depending on the model, two approaches are possible:

- Capacitance approach
A set of five capacitances Cgd , Cgb , Cgs , Cbd , and Cbs are used to model the dynamic behavior of the model. When used, these capacitances are described in each model.
- Charge approach
Instead of using capacitances, it is also possible to model the dynamic behavior in terms of charges. This allows an interesting property of MOS devices, namely, charge conservation, to be utilized. This technique requires the introduction of a charge at each of the device nodes QD , QB , QS , and QG as shown in the diagram. The charges are described in each model section.

In addition to intrinsic static and dynamic behavior, there is also extrinsic behavior. Extrinsic behavior is related to a number of parasitic effects introduced during fabrication of the silicon and are included in the extrinsic model.

The extrinsic model includes:

- parasitic access drain and source resistances (**Rd** and **Rs**)
- parasitic static bulk diode effects (**Ibd** and **Ibs**)
- parasitic dynamic bulk diode effects (**Cbd** and **Cbs**)
- the related Areas and Perimeters calculations
- the related Temperature behavior.

To simplify the usage of these parasitic elements they are common to each different Eldo model. Equations that are common to each model are used to achieve this goal.



Note The default values for these common equations may differ from one model to another, to ensure compatibility with earlier software releases and external software.

3.0 Scaling Rules

$$LDIF_{scal} = LDIF \cdot scalm \quad HDIF_{scal} = HDIF \cdot scalm \cdot WMLT$$

$$DL_{scal} = DL \cdot scalm \quad DW_{scal} = DW \cdot scalm$$

$$LD_{scal} = LD \cdot scalm \quad WD_{scal} = WD \cdot scalm$$

$$AD_{scal} = \frac{AD}{scalm \cdot scalm} \quad AS_{scal} = \frac{AS}{scalm \cdot scalm} v_{tvt}$$

$$PD_{scal} = \frac{PD}{scalm} \quad PS_{scal} = \frac{PS}{scalm}$$

$$JS_{scal} = \frac{JS}{scalm \cdot scalm} \quad JSW_{scal} = \frac{JSW}{scalm}$$

$$CJ_{scal} = \frac{CJ}{scalm \cdot scalm} \quad CJSW_{scal} = \frac{CJSW}{scalm}$$

$$CJGATE_{scal} = \frac{CJGATE}{scalm}$$



The model parameter scaling factor **SCALM** can be defined for all model cards in the netlist using **.OPTION SCALM=val**, or can be individually defined for each model card using the model parameter **SCALM**. This overrides the global **SCALM** value defined using the **.OPTION** command.

4.0 Access Resistance Equations

Eldo offers various possibilities of access resistance calculation thanks to the **RLEV** parameter. These possibilities range from simple equation sets to full geometrical access resistance calculations, with various default value initializations.

4.1 Related model parameters

Name	Description	Default	Units
RLEV	Switch selector	*	
RD	Drain ohmic resistance	0	Ω
RS	Source ohmic resistance	0	Ω
RSH	Drain and Source diffusion sheet resistance	0	Ω/sq
RDC	Additional drain resistance due to contact resistance	0	Ω
RSC	Additional source resistance due to contact resistance	0	Ω
LD	Lateral diffusion into channel from source and drain diffusion	0*	m
LDIF	Length of lightly doped diffusion adjacent to gate	0	m
HDIR	Length of heavily doped diffusion from contact to lightly doped region	0	m

* dependent on the model used, see table below:

Model (Eldo Level)	RLEV default value
Level (12,13,16,17), BSIM1 (8)	0
EKV (44)	2
BSIM3v2 (47), BSIM3v3 (53)	4
Level (1,2,3), MOS9 (53), BSIM2 (11), MM11 (63,65)	6

4.2 Related device parameters

- ***nrs***: Number of squares for source resistance
- ***nrd***: Number of squares for drain resistance
- ***RSC***: Additional source resistance due to contact resistance, this parameter has priority over the one in the **.MODEL** card
- ***RDC***: Additional drain resistance due to contact resistance, this parameter has priority over the one in the **.MODEL** card
- ***M***: Number of parallel transistors.

4.3 Related options

In the **.OPTION** command, the following parameters may be set:

- ***scalm***: Sets the size multiplier for the model parameters in mosfet models, the default value is 1
- ***defnrs***: Default value for ***nrs***
- ***defnrd***: Default value for ***nrd***
- ***rmos***: In order to decrease the number of nodes to be evaluated, Eldo doesn't automatically create access resistors as external components. This approximation can cause some convergence problems, especially when the value of these resistances, voltage or current are important. In this case the usage of the ***RMOS*** option is recommended as it creates access resistors as external components.

- **acm:** Refer to “[.OPTION ACM](#)” on page 10-43 for more details.

4.4 Equations



Note

In the coming lines, two W 's are referred to: W_{eff} and W_j . W_{eff} refers to the effective channel width calculated in each model, W_j refers to the junction width.

RLEV = 0

- Source access resistance RS_{eff}

$$\text{If } nrs > 0 \text{ then } RS_{eff} = \frac{RSH \cdot nrs + RSC}{M} \text{ else } RS_{eff} = \frac{RS + RSC}{M}$$

- Drain access resistance RD_{eff}

$$\text{If } nrd > 0 \text{ then } RD_{eff} = \frac{RSH \cdot nrd + RDC}{M} \text{ else } RD_{eff} = \frac{RD + RDC}{M}$$



Note

Default values for nrd and nrs are set to **defnrd** and **defnrs** when they are specified, otherwise these parameters are set to 0.

RLEV = 1

- Source access resistance RS_{eff}

$$RS_{eff} = \frac{RS \cdot (LD_{scal} + LDIF_{scal})}{M \cdot W_j} + \frac{nrs \cdot RSH + RSC}{M}$$

- Drain access resistance RD_{eff}

$$RD_{eff} = \frac{RD \cdot (LD_{scal} + LDIF_{scal})}{M \cdot W_j} + \frac{nrd \cdot RSH + RDC}{M}$$



The same conditions apply to ***nrs***, ***nrd*** as those for the case of ***RLEV=0***

Note

W_j is computed as: $W_j = W_{eff} + DW_{scal}$

If **.OPTION ACM** or parameter **OPTACM=1** is specified and **ACM=1**, $W_j = W_{drawn}WMLT + XW_{scal}$

RLEV = 2 and ***RLEV = 3***

- Source access resistance ***RS_{eff}***

$$\text{If } nrs > 0 \text{ then } RS_{eff} = \frac{RS \cdot (LD_{scal} + LDIF_{scal})}{M \cdot W_j} + \frac{RSH \cdot nrs + RSC}{M}$$

$$\text{else } RS_{eff} = \frac{RS \cdot (LD_{scal} + LDIF_{scal})}{M \cdot W_j} + \frac{HDIF_{scal} \cdot RSH}{M \cdot W_j} + \frac{RSC}{M}$$

- Drain access resistance ***RD_{eff}***

$$\text{If } nrd > 0 \text{ then } RD_{eff} = \frac{RD \cdot (LD_{scal} + LDIF_{scal})}{M \cdot W_j} + \frac{RSH \cdot nrd + RDC}{M}$$

$$\text{else } RD_{eff} = \frac{RD \cdot (LD_{scal} + LDIF_{scal})}{M \cdot W_j} + \frac{HDIF_{scal} \cdot RSH}{M \cdot W_j} + \frac{RDC}{M}$$



The default values for ***nrs*** and ***nrd*** are not equal to ***defnrd***, ***defnrs***. In this case these options are not applicable.

Note

W_j is computed as: $W_j = W_{eff} + DW_{scal}$

If **.OPTION ACM** or parameter **OPTACM=1** is specified and **ACM=2** or **3**, $W_j = W_{drawn}WMLT + XW_{scal}$

RLEV = 4

- Source access resistance ***RS_{eff}***

If $LDIF_{scal} \leq 0$ then $RS_{eff} = \frac{RS}{M}$

else, if $nrs > 0$ then $RS_{eff} = \frac{RS \cdot (LD_{scal} + LDIF_{scal})}{M \cdot W_{eff}} + \frac{nrs \cdot RSH}{M}$

else $RS_{eff} = \frac{RS \cdot (LD_{scal} + LDIF_{scal})}{M \cdot W_{eff}} + \frac{HDIF_{scal} \cdot RSH}{M \cdot W_{eff}}$

- Drain access resistance RD_{eff}

If $LDIF_{scal} \leq 0$ then $RD_{eff} = \frac{RD}{M}$

else, if $nrs > 0$ then $RD_{eff} = \frac{RD \cdot (LD_{scal} + LDIF_{scal})}{M \cdot W_{eff}} + \frac{nrd \cdot RSH}{M}$

else $RD_{eff} = \frac{RD \cdot (LD_{scal} + LDIF_{scal})}{M \cdot W_{eff}} + \frac{HDIF_{scal} \cdot RSH}{M \cdot W_{eff}}$



The default values for nrs and nrd are equal to $defnrs$, $defnrd$ which are set to 1.0 when $HDIF$ is not specified.

RLEV = 5

- Source access resistance RS_{eff}

If $RS > 0$ then $RS_{eff} = \frac{RS}{M}$ else $RS_{eff} = nrs \cdot \frac{RSH}{M}$

- Drain access resistance RD_{eff}

If $RD > 0$ then $RD_{eff} = \frac{RD}{M}$ else $RD_{eff} = nrd \cdot \frac{RSH}{M}$



The default values for nrd and nrs are set to $defnrd$ and $defnrs$ when they are specified. Otherwise these parameters are set to 1.0, except for BSIM models where they are set to 0.0.

RLEV = 6

- Source access resistance RS_{eff}

$$\text{If } nrs > 0 \text{ then } RS_{eff} = \frac{nrs \cdot RSH}{M} \text{ else } RS_{eff} = \frac{RS}{M}$$

- Drain access resistance RD_{eff}

$$\text{If } nrd > 0 \text{ then } RD_{eff} = \frac{nrd \cdot RSH}{M} \text{ else } RD_{eff} = \frac{RD}{M}$$



The same conditions apply to nrs , nrd as those for the case of $RLEV=0$.

Note

RLEV = 7

- Source access resistance RS_{eff}

$$\text{If } nrs > 0 \text{ then } RS_{eff} = \frac{nrs \cdot RSH}{M} \text{ else } RS_{eff} = \frac{LDIF_{eff}}{M \cdot W_{eff}} \cdot RSH$$

- Drain access resistance RD_{eff}

$$\text{If } nrd > 0 \text{ then } RD_{eff} = \frac{nrd \cdot RSH}{M} \text{ else } RD_{eff} = \frac{LDIF_{eff}}{M \cdot W_{eff}} \cdot RSH$$



This case is only used with $ALEV = 7$.

Note

5.0 Area Computation

As it is used in MOS junction currents and capacitances, “Area Computation” methods are an important consideration. Default values for the different cases are also provided.

5.1 Related model parameters

Name	Description	Default	Units
ALEV	Switch selector	*	
DL	Length account for masking and etching effects	0	
DW^a	Width account for masking and etching effects	0	m
LMLT	Length diffusion layer shrink reduction factor	1	
WMLT	Width diffusion layer shrink reduction factor	1	
WD	Lateral diffusion into channel from bulk along width	0	

a. for **ALEV=7**, the definition is “total channel width correction.”

* dependent on the model used, see table below:

Model (Eldo Level)	ALEV default value
Level (12,13,16,17), BSIM1 (8), BSIM3v3 (53)	0
EKV (44), BSIM3v2 (47)	2
Level (1,2,3), MOS9 (53), BSIM2 (11), MM11 (63,65)	6

5.2 Related device parameters

- **AD**: Drain area
- **AS**: Source area
- **PD**: Drain perimeter
- **PS**: Source perimeter
- **geo**: Switch which determines the layout of the device

geo = 0 (Default value) indicates the drain and source of the device are not shared by the other devices

geo = 1 indicates the drain is shared with another device

geo = 2 indicates the source is shared with another device

geo = 3 indicates the source and drain are shared with another device

5.3 Related options

In the **.OPTION** command the following parameters may be set:

- ***scalm***: Sets the size multiplier for the model parameters in mosfet models, the default value is 1
- ***XA***: Diffusion length for MOS S/D calculation. For more details, see “[OPTION XA](#)” on page 10-14.
- ***old_alev0***: Retrieves the old special case of $ALEV=0$ equations for BSIM3v3.1 and BSIM3v3.2.
- ***defas***: Default value for ***AS***
- ***defad***: Default value for ***AD***
- ***defpd***: Default value for ***PD***
- ***defps***: Default value for ***PS***
- ***scale***: This option is needed if you want to use a scaling factor for the device’s parameter (***AD***, ***AS***, ***PD***, ***PS***, ***L***, ***W***). This option is global, so it concerns all devices present in the netlist file.
- ***acm***: Refer to “[.OPTION ACM](#)” on page 10-43 for more details.



Note When $ALEV = 1, 2, 3$ the options ***defXX*** are not applicable. However, they could be applicable for $ALEV = 2, 3$ if **.OPTION USEDEFAP** is set.



For the expression of W_{eff} , please refer to the Effective channel width for each model.



Note In the coming lines, two W ’s are referred to: W_{eff} and W_j . W_{eff} refers to the effective channel width calculated in each model, W_j refers to the junction width.

5.4 OPTION XA

If (.OPTION XA)

If **AS** is not specified then $AS_{eff} = W_{eff} \cdot XA$

If **AD** is not specified then $AD_{eff} = W_{eff} \cdot XA$

If **PS** is not specified then $PS_{eff} = W_{eff} + 2 \cdot XA$

If **PD** is not specified then $PD_{eff} = W_{eff} + 2 \cdot XA$

5.5 Equations

If (.OPTION XA) is not specified, Eldo will select between the following equations according to the ALEV selector.

ALEV = 0

- Source area AS_{eff}

If **AS** is specified then $AS_{eff} = AS \cdot WMLT \cdot WMLT$

else if **defas** is specified then $AS_{eff} = defas$

else $AS_{eff} = 0$

- Drain area AD_{eff}

If **AD** is specified then $AD_{eff} = AD \cdot WMLT \cdot WMLT$

else if **defad** is specified then $AD_{eff} = defad$

else $AD_{eff} = 0$

- Source perimeter PS_{eff}

If **PS** is specified then $PS_{eff} = PS \cdot WMLT$

else if **defps** is specified then $PS_{eff} = defps$

else $PS_{eff} = 0$

- Drain perimeter PD_{eff}

If PD is specified then $PD_{eff} = PD \cdot WMLT$

else if $defpd$ is specified then $PD_{eff} = defpd$

else $PD_{eff} = 0$

'Old' Special Case of $ALEV=0$ for MODEL=BSIM3v3.1 & BSIM3v3.2



Note

There used to be a special case for BSIM3v3.1 and BSIM3v3.2 given by the equations below. These equations are no longer used by default. However, they can be used if `.OPTION old_alev0` is specified.

- Source area AS_{eff}

If AS is specified then $AS_{eff} = AS$ else $AS_{eff} = 0$

- Drain area AD_{eff}

If AD is specified then $AD_{eff} = AD$ else $AD_{eff} = 0$

- Source and Drain perimeter $PS_{eff} = PD_{eff} = W_{eff}$

$ALEV = 1$

- Source and Drain area $AS_{eff} = AD_{eff} = W_j \cdot WMLT$
- Source and Drain perimeter $PS_{eff} = PD_{eff} = W_j$



Note

The Source and Drain area have a length dimension (m), not an area dimension (m^2). This should be taken into consideration for the units of quantities used for diode current calculation (J_s) to be in A/m not A/ m^2 and also for quantities used in junction capacitance calculation (C_j) to be in F/m not F/ m^2 .



W_j is computed as: $W_j = W_{eff} + DW_{scal}$
 If **.OPTION ACM** or parameter **OPTACM=1** is specified and
ACM=1, $W_j = W_{drawn}WMLT + XW_{scal}$

ALEV = 2

- Source area AS_{eff}

If AS is specified then $AS_{eff} = AS \cdot WMLT \cdot WMLT$

else if **defas** is specified then $AS_{eff} = defas$

else $AS_{eff} = 2 \cdot HDIF_{scal} \cdot W_j$

- Drain area AD_{eff}

If AD is specified then $AD_{eff} = AD \cdot WMLT \cdot WMLT$

else if **defad** is specified then $AD_{eff} = defad$

else $AD_{eff} = 2 \cdot HDIF_{scal} \cdot W_j$

- Source perimeter PS_{eff}

If PS is specified then $PS_{eff} = PS \cdot WMLT$

else if **defps** is specified then $PS_{eff} = defps$

else $PS_{eff} = 4 \cdot HDIF_{scal} + 2 \cdot W_j$

- Drain perimeter PD_{eff}

If PD is specified then $PD_{eff} = PD \cdot WMLT$

else if **defpd** is specified then $PD_{eff} = defpd$

$$\text{else } PD_{eff} = 4 \cdot HDIF_{scal} + 2 \cdot W_j$$



Note W_j is computed as: $W_j = W_{eff} + DW_{scal}$
 If **.OPTION ACM** or parameter **OPTACM=1** is specified and
ACM=2, $W_j = W_{drawn}WMLT + XW_{scal}$

ALEV = 3

- Source area AS_{eff}

If AS is specified then $AS_{eff} = AS \cdot WMLT \cdot WMLT$

else if $defas$ is specified then $AS_{eff} = defas$

else if $geo=0$ or 1 then $AS_{eff} = 2 \cdot HDIF_{scal} \cdot W_j$

else if $geo=2$ or 3 then $AS_{eff} = HDIF_{scal} \cdot W_j$

- Drain area AD_{eff}

If AD is specified then $AD_{eff} = AD \cdot WMLT \cdot WMLT$

else if $defad$ is specified then $AD_{eff} = defad$

else if $geo=0$ or 2 then $AD_{eff} = 2 \cdot HDIF_{scal} \cdot W_j$

else if $geo=1$ or 3 then $AD_{eff} = HDIF_{scal} \cdot W_j$

- Source perimeter PS_{eff}

If PS is specified then $PS_{eff} = PS \cdot WMLT$

else if $defps$ is specified then $PS_{eff} = defps$

else if $geo=0$ or 1 then $PS_{eff} = 4 \cdot HDIF_{scal} + W_j$

else if $geo=2$ or 3 then $PS_{eff} = 2 \cdot HDIF_{scal}$

- Drain perimeter PD_{eff}

If PD is specified then $PD_{eff} = PD \cdot WMLT$

else if $defpd$ is specified then $PD_{eff} = defpd$

else if $geo=0$ or 2 then $PD_{eff} = 4 \cdot HDIF_{scal} + W_j$

else if $geo=1$ or 3 then $PD_{eff} = 2 \cdot HDIF_{scal}$



W_j is computed as: $W_j = W_{eff} + DW_{scal}$

If **.OPTION ACM** or parameter **OPTACM=1** is specified and **ACM=3**, $W_j = W_{drawn}WMLT + XW_{scal}$

ALEV = 4

- Source area AS_{eff}

If AS is specified then $AS_{eff} = AS$

else if $defas$ is specified then $AS_{eff} = defas/(SCALM)^2$

else $AS_{eff} = 0$

- Drain area AD_{eff}

If AD is specified then $AD_{eff} = AD$

else if $defad$ is specified then $AD_{eff} = defad/(SCALM)^2$

else $AD_{eff} = 0$

- Drain perimeter PD_{eff}

If PD is specified then $PD_{eff} = PD$

else if $defps$ is specified then $PS_{eff} = defps/(SCALM)$

else $PD_{eff} = 0$

- Source perimeter PS_{eff}

If PS is specified then $PS_{eff} = PS$

else if $defpd$ is specified then $PD_{eff} = defpd/(SCALM)$

else $PS_{eff} = 0$

ALEV = 5, 6

- Source area AS_{eff}

If AS is specified then $AS_{eff} = AS$

else if $defas$ is specified then $AS_{eff} = defas$

else $AS_{eff} = 0$

- Drain area AD_{eff}

If AD is specified then $AD_{eff} = AD$

else if $defad$ is specified then $AD_{eff} = defad$

else $AD_{eff} = 0$

- Drain perimeter PD_{eff}

If PD is specified then $PD_{eff} = PD$

else if $defpd$ is specified then $PD_{eff} = defpd$

else $PD_{eff} = 0$

- Source perimeter PS_{eff}

If PS is specified then $PS_{eff} = PS$

else if $defps$ is specified then $PS_{eff} = defps$

else $PS_{eff} = 0$

- If AS , AD , PD and PS are all not specified and $LDIF_{eff}$ is not zero

$$\text{then } AS_{eff} = W_{eff} \cdot LDIF_{eff}$$

$$AD_{eff} = W_{eff} \cdot LDIF_{eff}$$

$$PS_{eff} = 2 \cdot (W_{eff} + LDIF_{eff})$$

$$PD_{eff} = 2 \cdot (W_{eff} + LDIF_{eff})$$

ALEV = 7

- Source area AS_{eff}

If AS is specified then $AS_{eff} = AS$

else if $defas$ is specified then $AS_{eff} = defas$

else $AS_{eff} = W_j \cdot LDIF_{eff}$

- Drain area AD_{eff}

If AD is specified then $AD_{eff} = AD$

else if $defad$ is specified then $AD_{eff} = defad$

else $AD_{eff} = W_j \cdot LDIF_{eff}$

- Drain perimeter PD_{eff}

If PD is specified then $PD_{eff} = PD$

else if $defpd$ is specified then $PD_{eff} = defpd$

else $PD_{eff} = 2 \cdot (W_j + LDIF_{eff})$

- Source perimeter PS_{eff}

If PS is specified then $PS_{eff} = PS$

else if $defps$ is specified then $PS_{eff} = defps$

$$\text{else } PS_{eff} = 2 \cdot (W_j + LDIF_{eff})$$



This case is only used with $RLEV = 7$,
 $W_j = (W_{eff} \cdot WMLT - 2 \cdot DW_{scal})$ and
 $LDIF_{eff} = (LDIF_{scal} \cdot WMLT - DW_{scal})$

6.0 Diode Current Computation (DIOLEV \neq 9)

6.1 Related model parameters

Name	Description	Default	Units
DIOLEV	Switch selector	*	
JS	Bottom bulk junction saturation current density	0	Am $^{-2}$
JSW	Sidewall bulk junction saturation current density	0	Am $^{-1}$
IS	Bulk junction saturation current	1×10^{-14}	A
N	Emission coefficient	1	
NDS	Reverse bias slope coefficient	1	
VNDS	Reverse bias transition voltage	-1	V
SBTH	Flag for reverse diode behavior (for PRECISE compatibility) 0 sets DIOLEV=1 and 1 sets DIOLEV=4	0	

* dependent on the model used, see table below:

Model (Eldo Level)	DIOLEV default value
Level (1,2,3), MOS9 (53), BSIM3v2 (47)	1
Level (12,13,16,17),	2
BSIM1 (8), BSIM2 (11)	3
EKV (44)	4
BSIM3v3 (53)	5
MM11 (63,65)	6

6.2 Related device parameters

- M : Number of parallel transistors

6.3 Related options

In the **.OPTION** command the following parameters may be set:

- ***scalm***: Sets the size multiplier for the model parameters in mosfet models, the default value is 1.
- ***acm***: Refer to “[.OPTION ACM](#)” on page 10-43 for more details.

6.4 Initialization

If (BSIM3v3 and version > 3.05)

If ($AX_{eff} = 0$ and $PX_{eff} = 0$)

If (AX is specified and PX is specified)

$Isatbx = 0$

else

$Isatbx = M \cdot IS$

else

$Isatbx = M \cdot (JS \cdot AX_{eff} + JSW \cdot PX_{eff})$

else:

If $Val = M \cdot (JS_{scal} \cdot AS_{eff} + JSW_{scal} \cdot PS_{eff}) > 0$

$Isatbs = Val$

else

$Isatbs = M \cdot IS$

If $Val = M \cdot (JS_{scal} \cdot AD_{eff} + JSW_{scal} \cdot PD_{eff}) > 0$

$Isatbd = Val$

else

$$Isatbd = M \cdot IS$$



Note For Levels 12, 13, 16, 17, and BSIM1, if **Isatbd** or **Isatbs** is below $1 \times 10^{-15} \text{ A}$, it is set to $1 \times 10^{-15} \text{ A}$ respectively.

For the BSIM2 model, if **Isatbd** or **Isatbs** is below $1 \times 10^{-18} \text{ A}$, it is set to $1 \times 10^{-18} \text{ A}$ respectively (except in PRECISE mode).

6.5 Equations

x is used to represent either the drain or the source diode currents. The bulk-x diode current, **Ibx**, is expressed as follows:

If $vbx > 0$ (forward mode): $Ibx = Isatbx \cdot \left(\exp \frac{vbx}{N \cdot Vt} - 1 \right)$

otherwise (reverse mode):

- o **DIOLEV = 1:** $Ibx = Isatbx \cdot \frac{vbx}{N \cdot Vt}$

- o **DIOLEV = 2:**

If $VNDS \leq vbx \leq 0$ then $Ibx = Isatbx \cdot vbx$

else $Ibx = Isatbx \cdot \left(VNDS + \frac{vbx - VNDS}{NDS} \right)$

- o **DIOLEV = 3:**

If $VNDS \leq vbx \leq 0$ then $Ibx = Isatbx \cdot \frac{vbx}{N \cdot Vt}$

else $Ibx = \frac{Isatbx}{N \cdot Vt} \cdot \left(VNDS + \frac{vbx - VNDS}{NDS} \right)$

- o **DIOLEV = 4:**

If $vbx < -10 \cdot N \cdot Vt$ then $Ibx = -Isatbx$

else $Ibx = Isatbx \cdot \left(\exp \frac{vbx}{N \cdot Vt} - 1 \right)$

- **DIOLEV = 5:**

If $vbx < -5 \cdot N \cdot Vt$ then $Ibx = -Isatbx$

$$\text{else } Ib_{x} = Isatbx \cdot \left(\exp \frac{vbx}{N \cdot Vt} - 1 \right)$$

- **DIOLEV = 6:**

$$\text{If } vbx < 0.5 \text{ then } Ib_{x} = Isatbx \cdot \left(\exp \frac{vbx}{N \cdot Vt} - 1 \right)$$

$$\text{else } Ib_{x} = Isat \cdot \left(\exp \frac{0.5}{N \cdot Vt} - 1 \right) + \left(\frac{Isat}{N \cdot Vt} \right) \left(\exp \frac{0.5}{N \cdot Vt} \right) (vbx - 0.5)$$

- **DIOLEV = 7:**

This model was added specifically for BSIM3v3.2. For model equations refer to “[Diode IV model](#)” on page 18-36.

7.0 Diode Current Equations (DIOLEV=9)

This level is used to implement the JUNCAP junction diode model.

7.1 Related model parameters

Name	Description	Default	Units
VR	Voltage at which the parameters have been determined	0	V
JSGBR	Bottom saturation-current density due to electron-hole generation at $V = V_R$	1×10^{-3}	Am^{-2}
JSDBR	Bottom saturation-current density due to diffusion from back contact	1×10^{-3}	Am^{-2}
JSGSR	Sidewall saturation-current density due to electron-hole generation at $V = V_R$	1×10^{-3}	Am^{-1}
JSDSR	Sidewall saturation-current density due to diffusion from back contact	1×10^{-3}	Am^{-1}
JSGGR	Gate-edge saturation-current density due to electron-hole generation at $V = V_R$	1×10^{-3}	Am^{-1}
JSDGR	Gate-edge saturation-current density due to diffusion from back contact	1×10^{-3}	Am^{-1}
NBJ	Emission coefficient of the bottom forward current	1	

Name	Description	Default	Units
NSJ	Emission coefficient of the sidewall forward current	1	
NGJ	Emission coefficient of the gate-edge forward current	1	
CJBR	Bottom junction capacitance at $V = V_R$	1×10^{-12}	Fm $^{-2}$
CJSR	Sidewall junction capacitance at $V = V_R$	1×10^{-12}	Fm $^{-1}$
CJGR	Gate-edge junction capacitance at $V = V_R$	1×10^{-12}	Fm $^{-1}$
VDBR	Diffusion voltage of the bottom junction at $T = T_{nom}$	1	V
VDSR	Diffusion voltage of the sidewall junction at $T = T_{nom}$	1	V
VDGR	Diffusion voltage of the gate-edge junction at $T = T_{nom}$	1	V
PB	Bottom-junction grading coefficient	0.4	
PS	Sidewall junction grading coefficient	0.4	
PG	Gate-edge-junction grading coefficient	0.4	
TRDIO9	Nominal temperature for Juncap junction diode model	TNOM (TR)	°C

The bottom diffusion current, I_{DB} , is expressed as:

$$I_{DB} = I_{SDB} \cdot \left(\exp\left(\frac{vbx}{NBJ \cdot \phi_{TD}}\right) - 1 \right)$$

The bottom generation current, I_{GB} , is expressed as:

$$I_{GB} = \begin{cases} I_{SGB} \cdot \left(\frac{V_{DB} - vbx}{V_{DB}} \right)^{PB} \cdot \left(\exp\left(\frac{vbx}{NBJ \cdot \phi_{TD}}\right) - 1 \right), & vbx \leq 0.0 \\ I_{SGB} \cdot \left(\frac{V_{AB}}{vbx + V_{AB}} \right)^2 \cdot \left(1 - \exp\left(\frac{-vbx}{NBJ \cdot \phi_{TD}}\right) \right), & vbx > 0.0 \end{cases}$$

$$\text{where } V_{AB} = \frac{2 \cdot V_{DB}}{PB}$$

The sidewall diffusion current, I_{DS} , is expressed as:

$$I_{DS} = I_{SDS} \cdot \left(\exp\left(\frac{vbx}{NSJ \cdot \phi_{TD}}\right) - 1 \right)$$

The sidewall generation current, I_{GS} , is expressed as:

$$I_{GS} = \begin{cases} I_{SGS} \cdot \left(\frac{V_{DS} - vbx}{V_{DS}} \right)^{PS} \cdot \left(\exp\left(\frac{vbx}{NSJ \cdot \phi_{TD}}\right) - 1 \right), & vbx \leq 0.0 \\ I_{SGS} \cdot \left(\frac{V_{AS}}{vbx + V_{AS}} \right)^2 \cdot \left(1 - \exp\left(\frac{-vbx}{NSJ \cdot \phi_{TD}}\right) \right), & vbx > 0.0 \end{cases}$$

$$\text{where } V_{AS} = \frac{2 \cdot V_{DS}}{PS}$$

The gate-edge diffusion current, I_{DG} , is expressed as:

$$I_{DG} = I_{SDG} \cdot \left(\exp\left(\frac{vbx}{NGJ \cdot \phi_{TD}}\right) - 1 \right)$$

The gate-edge generation current, I_{GG} , is expressed as:

$$I_{GG} = \begin{cases} I_{SGG} \cdot \left(\frac{V_{DG} - vbx}{V_{DG}} \right)^{PG} \cdot \left(\exp\left(\frac{vbx}{NGJ \cdot \phi_{TD}}\right) - 1 \right), & vbx \leq 0.0 \\ I_{SGG} \cdot \left(\frac{V_{AG}}{vbx + V_{AG}} \right)^2 \cdot \left(1 - \exp\left(\frac{-vbx}{NGJ \cdot \phi_{TD}}\right) \right), & vbx > 0.0 \end{cases}$$

$$\text{where } V_{AB} = \frac{2 \cdot V_{DG}}{PG}$$

The total junction current Ibx can be expressed as:

$$Ibx = AX_{eff} \cdot (I_{DB} + I_{GB}) + PX_{eff} \cdot (I_{DS} + I_{GS}) + W_{eff} \cdot (I_{DG} + I_{GG})$$

8.0 Junction Capacitances/Charges (DIOLEV \neq 9)

Charge storage is modeled by three constant capacitors, **CGSO**, **CGDO** and **CGBO**. Capacitances taken into account are the non-linear thin-oxide capacitance distributed among the gate, source, drain and bulk regions, and the non-linear depletion-layer capacitances for both substrate junctions divided into bottom and periphery, which vary as the **MJ** and **MJSW** power of junction voltage respectively, and are determined by the parameters **CBD**, **CBS**, **CJ**, **CJSW**, **MJ**, **MJSW** and **PB**. The model is the piecewise linear voltage dependent capacitance model proposed by Meyer.

8.1 Related model parameters

Name	Description	Default	Units
DCAPLEV	Switch selector	*	
CBD	Zero bias Bulk-Drain capacitance	0	F
CBS	Zero bias Bulk-Source capacitance	0	F
CJ	Zero bias bottom Bulk junction capacitance	0*	Fm ⁻²
CJGATE	Zero bias gate-edge sidewall Bulk junction capacitance (only used when ALEV= 3 and DCAPLEV= 0)	0	Fm ⁻¹
CJSW	Zero bias sidewall Bulk junction capacitance	0	Fm ⁻¹
FC	Bulk junction forward bias capacitance coefficient	0.5*	
MJ	Bulk junction bottom grading coefficient	0.5	
MJSW	Bulk junction sidewall grading coefficient	0.33	
PB	Bulk bottom junction potential	0.8*	V
PBSW	Bulk sidewall junction potential	PB	V
TT	Transit time	0	s

* dependent on the model used, see table below:

Model (Eldo Level)	DCAPLEV default value
Level (12,13,16,17), BSIM1 (8)	0
BSIM3v2 (47)	1

Model (Eldo Level)	DCAPLEV default value
Level (1,2,3), MOS9 (53), BSIM2 (11), EKV (44)	2
BSIM3v3 (53)	4
MM11 (63,65)	-

8.2 Related device parameters

- M : Number of parallel transistors

8.3 Related options

In the **.OPTION** command the following parameters may be set:

- **scalm**: Sets the size multiplier for the model parameters in mosfet models, the default value is 1.
- **acm**: Refer to “[.OPTION ACM](#)” on page 10-43 for more details.



In the coming lines, two W 's are referred to: W_{eff} and W_j . W_{eff} refers to the effective channel width calculated in each model, W_j refers to the junction width.

8.4 Initialization

$CjaX$ and $CjpX$ means either the $Cjas$, $Cjps$ and $Cjad$, $Cjpd$.

AX_{eff} , PX_{eff} , CBX means either AS_{eff} , PS_{eff} , CBS and AD_{eff} , PD_{eff} , CBD .

- $DCAPLEV = 0$

If $Val = AX_{eff} \cdot CJ_{scal} + PX_{eff} \cdot CJSW_{scal} + CJGATE_{scal} \cdot W_j > 0$

then $CjaX = M \cdot AX_{eff} \cdot CJ_{scal}$

and $CjpX = M \cdot (PX_{eff} \cdot CJSW_{scal} + CJGATE_{scal} \cdot W_j)$

else $CjaX = M \cdot CBX$ and $CjpX = 0$



W_j is computed as: $W_j = W_{eff} + DW_{scal}$
 If .OPTION ACM or parameter OPTACM=1 is specified and
 $ACM=3$, $W_j = W_{drawn} + XW_{scal}$

- $DCAPLEV = 1$

$$CjpX = M \cdot PX_{eff} \cdot CJSW_{scal}$$

If $CJ > 0$ then $CjaX = M \cdot AX_{eff} \cdot CJ_{scal}$ else $CjaX = M \cdot CBX$

- $DCAPLEV = 2$

$$CjpX = M \cdot PX_{eff} \cdot CJSW_{scal}$$

If $CBX > 0$ then $CjaX = M \cdot CBX$ else $CjaX = M \cdot AX_{eff} \cdot CJ_{scal}$

- $DCAPLEV = 3$

$$CjpX = M \cdot PX_{eff} \cdot CJSW_{scal}$$

If $CJ > 0$ then $CjaX = M \cdot AX_{eff} \cdot CJ_{scal}$

else if $CjpX > 0$ then $Cjax = 0$

else $CjaX = M \cdot CBX$

- $DCAPLEV = 4$

This was added specifically for BSIM3 v3.1 and v3.2.

$$CjaX = M \cdot AX_{eff} \cdot CJ_{scal}$$

If $PX_{eff} < W_{eff}$ then $CjpXg = M \cdot CJSWG \cdot PX_{eff}$ $CjpX = 0$

else if $PX_{eff} > W_{eff}$ then

$$CjpXg = M \cdot CJSWG \cdot W_{eff}$$

If $ALEV=3$, and PX & $defpx$ are not defined:

$$CjpX = M \cdot CJSW \cdot PX_{eff}$$

$$\text{else } CjpX = M \cdot CJSW \cdot (PX_{eff} - W_{eff})$$


Note

This special case is for users wishing to use $DCAPLEV=4$ in conjunction with $ALEV=3$, while specifying the *geo* parameter.

- $DCAPLEV = 5$

$$CjaX = M \cdot AX_{eff} \cdot CJ_{scal}$$

$$\text{If } (PX_{eff} \leq W_j)$$

$$\text{then } CjpX = M \cdot (CJGATE_{scal} \cdot PX_{eff})$$

$$\text{else } CjpX = M \cdot ((PX_{eff} - W_j) \cdot CJSW_{scal} + CJGATE_{scal} \cdot W_j)$$

$$\text{If } (CjaX = 0 \text{ and } CjpX = 0)$$

$$\text{then } CjaX = M \cdot CBX$$


Note

W_j is computed as: $W_j = W_{eff} + DW_{scal}$

If **.OPTION ACM** or parameter **OPTACM=1** is specified and **ACM=2**, $W_j = W_{drawn}WMLT + XW_{scal}$

8.5 Equations



x is used to represent either the Drain or the Source diode capacitance.

Note

The Bulk capacitance Cbx is expressed as the sum of bottomwall, sidewall depletion capacitances and diffusion capacitance.

$$Cbx = Cbx_{bottom} + Cbx_{sidewall} + Cbx_{diff}$$

The bottomwall capacitance Cbx_{bottom} is expressed as:

- for $vbx \leq FC \cdot PB$ then $Cbx_{bottom} = Cjax \cdot \left(1 - \frac{vbx}{PB}\right)^{-MJ}$
- else $Cbx_{bottom} = \frac{Cjax}{(1 - FC)^{1+MJ}} \cdot \left(1 - FC \cdot (1 + MJ) + \frac{MJ \cdot vbx}{PB}\right)$

The sidewall depletion capacitance $Cbx_{sidewall}$ is expressed as:

- for $vbx \leq FC \cdot PBSW$ then $Cbx_{sidewall} = Cjpx \cdot \left(1 - \frac{vbx}{PBSW}\right)^{-MJSW}$

else

$$Cbx_{sidewall} = \frac{Cjpx}{(1 - FC)^{1+MJSW}} \cdot \left(1 - FC \cdot (1 + MJSW) + p, \frac{MJSW \cdot vbx}{PBSW}\right)$$

The diffusion capacitance Cbx_{diff} is expressed as:

- for $TT > 0$ then $Cbx_{diff} = TT \cdot \frac{\partial Ibx}{\partial vbx}$
- else $Cbx_{diff} = 0$



Note

For a charge conservation model the charges expressions are computed as follows:

$$Qbx = \int_0^{vbx} Cbx \cdot \partial vbx$$

8.6 Equations used with DCAPLEV=4



Note

x is used to represent either the Drain or the Source diode capacitance.

The bottomwall capacitance Cbx_{bottom} is expressed as:

- If $vbx < 0$ then $Cbx_{bottom} = CJax \cdot \left(1 - \frac{vbx}{PB}\right)^{-MJ}$

$$\text{else } Cbx_{bottom} = CJaX \cdot \left(1 + \frac{MJ \cdot vbx}{PB}\right)$$

The sidewall depletion capacitance along field oxide $Cbx_{sidewall}$ is expressed as:

- If $vbx < 0$ then $Cbx_{sidewall} = CjpX \cdot \left(1 - \frac{vbx}{PBSW}\right)^{-MJSW}$
- else $Cbx_{sidewall} = CjpX \cdot \left(1 + \frac{MJSW \cdot vbx}{PBSW}\right)$

The sidewall depletion capacitance along gate side $Cbx_{sidewall}$ is expressed as:

- If $vbx < 0$ then $Cbx_{sidewallg} = CjpXg \cdot \left(1 - \frac{vbx}{PBSWG}\right)^{-MJSWG}$
- else $Cbx_{sidewallg} = CjpXg \cdot \left(1 + \frac{MJSWG \cdot vbx}{PBSWG}\right)$

8.7 Compatibility between ALEV & DCAPLEV

ALEV is the switch selector which chooses a model for the Area Computation.

DCAPLEV is the switch selector which chooses a model for the Junction Capacitance Computation.

Due to the dependence of the Junction Capacitance on the Area, here we present some advice on the combinations of **ALEV** and **DCAPLEV**.

For the case of **ALEV=3** and both **AS** and **defas** (**AD** and **defad**) not specified, the **geo** parameter is used to specify whether the junction is shared or not. In this case, the perimeter returned by this routine is not the whole perimeter: the sidewall near the gate side is not included in the perimeter. This is done to allow for separate contributions of the capacitance, one due to the gate sidewall and the other due to the rest of the perimeter, i.e.

$$CjpX = CJSW \cdot PX_{eff} + CJGATE \cdot W_j \quad DCAPLEV = 0$$

In this case, specifying **DCAPLEV**=1, 2, or 3 is not advisable, since they calculate the sidewall capacitance as follows: $C_{jpX} = C_{JSW} \cdot P_{X_{eff}}$. Here, the value of the perimeter is physically incorrect since it lacks the gate sidewall.

For this reason, if the user specifies both **ALEV**=3 and **DCAPLEV**=1, 2 or 3, a warning message is displayed telling the user that special care should be taken when using **ALEV**=3 with any of **DCAPLEV**=1, 2 or 3.

If **ALEV**=3 is used, **DCAPLEV**=0 is recommended, or **DCAPLEV**=4 in the case of BSIM3v3.



Please refer to “[Junction capacitances/charge model \(DCAPLEV=4\)](#)” on [page 18-34](#) for more information on this special case.

9.0 Capacitance Model (DIOLEV=9)



Please refer to the parameter table in “[Diode Current Equations \(DIOLEV=9\)](#)” on [page 10-24](#).

AX_{eff} , PX_{eff} , Cbx , vbx means either AS_{eff} , PS_{eff} , Cbs , vbs and AD_{eff} , PD_{eff} , Cbd , vbd , when referring to either bulk-source or bulk-drain junctions respectively.

The total capacitance **Cbx** can be described by the sum of three elementary capacitances which represent the bottom, sidewall and gate-edge contributions:

$$Cbx = AX_{eff} \cdot C_{JBV} + PX_{eff} \cdot C_{JSV} + W_{eff} \cdot C_{JGV}$$

In order to prevent an unlimited increase of the voltage derivative of the elementary capacitor, it is split into two parts: the original power function and an additional quadratic function. At the cross-over point between these regions, indicated by $V_{L...}$, the following parameters are defined:

$$F_{CB} = 1 - \left(\frac{1 + PB}{3} \right)^{\frac{1}{PB}} \quad V_{LB} = F_{CB} \cdot V_{DB} \quad C_{LB} = C_{JB} (1 - F_{CB})^{-PB}$$

The capacitance C_{JBV} of the bottom area is calculated as:

$$C_{JBV} = \begin{cases} C_{JB} \cdot \left(1 - \frac{vbx}{V_{DB}}\right)^{-PB}, & vbx < V_{LB} \\ C_{LB} + \frac{C_{LB} \cdot PB \cdot (vbx - V_{LB})}{V_{DB} \cdot (1 - F_{CB})}, & vbx \geq V_{LB} \end{cases}$$

and similar expressions for C_{JSV} and C_{JGV} .

10.0 Temperature Effects

The temperature of a semiconductor model can be defined in Eldo using the **TMOD** parameter. If this parameter is not present the global circuit temperature **TNOM** is assumed. The individual model temperature of a device can be set by using the optional instance parameter **T**.

10.1 Related model parameters

Name	Description	Default	Units
TNOM (TR)	Nominal temperature (TR for MOSP9 only)	27	°C
TMOD	Model temperature	TNOM	°C
TLEV	Temperature equation level selector	0	
TLEVC	Temperature equation level selector for capacitances and potentials	0	
CTA (TCJ)	Junction capacitance CJ temperature coefficient	0	°K ⁻¹
CTP (TCJSW)	Junction sidewall capacitance CJSW temperature coefficient	0	°K ⁻¹
PTA (TPB)	Junction potential PB temperature coefficient	0	V°K ⁻¹
PTP (TPBSW)	Junction potential PHB temperature coefficient	0	V°K ⁻¹
EG	Energy gap for PN junction diode	1.11 ^a	eV
GAP1	First bandgap correction factor	7.02×10 ⁻⁴	eV°K ⁻¹
GAP2	Second bandgap correction factor	1108	°K
TLEVI (LIS)	Saturation current temperature selector	1 ^b	
ISTMP	Number of degrees that doubles IS value	10	°C

Name	Description	Default	Units
XTI	Saturation current temperature exponent	0	
TLEVR	Access resistances temperature selector	1	
TRD1 (TC1,TRD)	Temperature coefficient (linear) for RD	0	°K ⁻¹
TRD2 (TC2)	Temperature coefficient (quadratic) for RD	0	°K ⁻²
TRS1 (TRS)	Temperature coefficient (linear) for RS	0	°K ⁻¹
TRS2	Temperature coefficient (quadratic) for RS	0	°K ⁻²
TRSH1	Temperature coefficient (linear) for RSH	0	°K ⁻¹
TRSH2	Temperature coefficient (quadratic) for RSH	0	°K ⁻²

- a. if **TLEV**=0 or 1, **EG**=1.11
else **EG**=1.16
b. For BSIM3v3.1, **TLEVI(LIS)** default = 3.
For MOSP9, **TLEVI(LIS)** default = 0.

10.2 General definitions

$$Vt(T) = k_B \cdot \frac{T}{q} \quad \delta t = T - T_{nom}$$

If **TLEV** = 0 or 1, $EG_{eff}(T) = 1.16 - 7.02 \times 10^{-4} \cdot \frac{T^2}{T + 1108}$

otherwise: $EG_{eff}(T) = EG - GAP1 \cdot \frac{T^2}{T + GAP2}$

10.3 Access resistance related temperature equations

The parameter **TLEVR** allows selection of the equation sets that may be used.

When **TLEVR** = 0, a simplified model is defined as:

$$RD(T) = RD \cdot \arg \quad RS(T) = RS \cdot \arg \quad RSH(T) = RSH \cdot \arg$$

where $\arg = 1 + TRD1 \cdot \delta t + TRD2 \cdot \delta t^2$

When **TLEVR** = 1, a complete model is defined as:

$$RD(T) = RD \cdot (1 + TRD1 \cdot \delta t + TRD2 \cdot \delta t^2)$$

$$RS(T) = RS \cdot (1 + TRS1 \cdot \delta t + TRS2 \cdot \delta t^2)$$

$$RSH(T) = RSH \cdot (1 + TRSH1 \cdot \delta t + TRSH2 \cdot \delta t^2)$$

10.4 Saturation current equations (DIOLEV \neq 9)



If **.OPTION ACM** is specified, and **ACM** \geq 10, and **AXeff & PXeff** are both equal to 0, **Isat** is fixed to $1.0e^{-14}$ and no further temperature update is done.

The parameter **TLEVI** controls the selection of the equations set used for the temperature behavior for the common diode currents.

$$IS(T) = IS \cdot \arg \quad JS(T) = JS \cdot \arg \quad JSW(T) = JSW \cdot \arg$$

For **TLEVI** = 0, no variation in relation to temperature is applied, so **arg** = 1.

For **TLEVI** = 1, a standard equation, based on SPICE, is defined as:

$$\arg = \exp\left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)}\right) \cdot \left(\frac{T}{T_{nom}}\right)^{XTI}$$

For **TLEVI** = 2, a modified equation is defined as: $\arg = 2^{\delta t / ISTMP}$

For **TLEVI** = 3, an improved equation, based on SPICE, is defined as:

$$\arg = \exp\left(\frac{EG_{eff}(T_{nom})}{N \cdot Vt(T_{nom})} - \frac{EG_{eff}(T)}{N \cdot Vt(T)}\right) \cdot \left(\frac{T}{T_{nom}}\right)^{XTI/N}$$

10.5 Capacitance related temperature equations (DIOLEV \neq 9)



If **.OPTION ACM** is specified and **ACM** \geq 10, no junction capacitance temperature update is done.

Note

The value of **TLEV**C determines which equations are used.

For **TLEV**C = 0,

$$PB(T) = PB \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right)$$

$$PBSW(T) = PBSW \cdot \frac{T}{T_{nom}} - Vt(T) \cdot \left(\frac{EG_{eff}(T_{nom})}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} + 3 \cdot \ln \frac{T}{T_{nom}} \right)$$

$$CJ(T) = CJ \cdot \left(1 + MJ \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta t - \frac{PB(T)}{PB} \right) \right)$$

$$CJSW(T) = CJSW \cdot \left(1 + MJSW \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta t - \frac{PBSW(T)}{PBSW} \right) \right)$$

$$CJGATE(T) = CJGATE \cdot \left(1 + MJSW \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta t - \frac{PBSW(T)}{PBSW} \right) \right)$$

$$CBS(T) = CBS \cdot \left(1 + MJ \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta t - \frac{PB(T)}{PB} \right) \right)$$

$$CBD(T) = CBD \cdot \left(1 + MJ \cdot \left(1 + 4 \cdot 10^{-4} \cdot \delta t - \frac{PB(T)}{PB} \right) \right)$$

For $TLEV\mathbf{C} = 1$,

$$\begin{aligned} PB(T) &= PB - PTA \cdot \delta t \\ PBSW(T) &= PBSW - PTP \cdot \delta t \\ CJ(T) &= CJ \cdot (1 + CTA \cdot \delta t) \\ CJSW(T) &= CJSW \cdot (1 + CTP \cdot \delta t) \\ CJGATE(T) &= CJGATE \cdot (1 + CTP \cdot \delta t) \\ CBS(T) &= CBS \cdot (1 + CTA \cdot \delta t) \\ CBD(T) &= CBD \cdot (1 + CTA \cdot \delta t) \end{aligned}$$

For $TLEV\mathbf{C} = 2$,

$$\begin{aligned} PB(T) &= PB - PTA \cdot \delta t \\ PBSW(T) &= PBSW - PTP \cdot \delta t \\ CJ(T) &= CJ \cdot \left(\frac{PB}{PB(T)} \right)^{MJ} \\ CJSW(T) &= CJSW \cdot \left(\frac{PBSW}{PBSW(T)} \right)^{MJSW} \\ CJGATE(T) &= CJGATE \cdot \left(\frac{PBSW}{PBSW(T)} \right)^{MJSW} \\ CBS(T) &= CBS \cdot \left(\frac{PB}{PB(T)} \right)^{MJ} \\ CBD(T) &= CBD \cdot \left(\frac{PB}{PB(T)} \right)^{MJ} \end{aligned}$$

For $TLEV\mathbf{C} = 3$,

$$\begin{aligned} PB(T) &= PB + Dpb \cdot \frac{\delta t}{T_{nom}} \\ PBSW(T) &= PBSW + Dpbsw \cdot \frac{\delta t}{T_{nom}} \end{aligned}$$

$$CJ(T) = CJ \cdot \left(1 - 0.5 \cdot \frac{Dpb}{PB} \cdot \frac{\delta t}{T_{nom}} \right)$$

$$CJSW(T) = CJSW \cdot \left(1 - 0.5 \cdot \frac{Dpb_{sw}}{PBSW} \cdot \frac{\delta t}{T_{nom}} \right)$$

$$CJGATE(T) = CJGATE \cdot \left(1 - 0.5 \cdot \frac{Dpb_{sw}}{PBSW} \cdot \frac{\delta t}{T_{nom}} \right)$$

$$CBS(T) = CBS \cdot \left(1 - 0.5 \cdot \frac{Dpb}{PB} \cdot \frac{\delta t}{T_{nom}} \right)$$

$$CBD(T) = CBD \cdot \left(1 - 0.5 \cdot \frac{Dpb}{PB} \cdot \frac{\delta t}{T_{nom}} \right)$$

where:

$$\begin{aligned} Dpb &= PB - EG_{eff}(T_{nom}) - 3 \cdot Vt(T_{nom}) + \\ &(EG_{eff}(T_{nom}) - EG) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + GAP2} \right) \end{aligned}$$

$$\begin{aligned} Dpb_{sw} &= PBSW - EG_{eff}(T_{nom}) - 3 \cdot Vt(T_{nom}) + \\ &(EG_{eff}(T_{nom}) - EG) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + GAP2} \right) \end{aligned}$$

10.6 Surface potential temperature equations (Levels 1, 2, 3 & 16)

For $TLEV C = 0$,

$$PHI(T) = PHI \cdot \left(\frac{T}{T_{nom}} \right) - Vt(T) \cdot \left[3 \cdot \ln \left(\frac{T}{T_{nom}} \right) + \frac{EG_{nom}}{Vt(T_{nom})} - \frac{EG_{eff}(T)}{Vt(T)} \right]$$

For $TLEV C = 1$,

$$PHI(T) = PHI - PTC \cdot \Delta T$$

If the **PHI** parameter is not specified, it is calculated as follows:

$$PHI(T) = 2 \cdot Vt(T) \cdot \ln\left(\frac{NSUB}{ni}\right)$$

The intrinsic carrier concentration, **ni**, must be temperature updated, and it is calculated from the silicon bandgap at room temperature.

$$ni = 145 \times 10^{16} \cdot \left(\frac{T}{TNOM}\right)^{3/2} \cdot \exp\left[EG \cdot \left(\frac{T}{TNOM} - 1\right) \cdot \left(\frac{1}{2 \cdot Vt(T)}\right)\right]$$

For **TLEV**C = 2,

$$PHI(T) = PHI - PTC \cdot \Delta T$$

For **TLEV**C = 3,

$$PHI(T) = PHI + dphidt \cdot \Delta T$$

where for **TLEV** = 0 or 1:

$$dphidt =$$

$$\frac{\left[EG_{nom} + 3 \cdot Vt(T_{nom}) + (1.16 - EG_{nom}) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + 1108}\right) - PHI\right]}{T_{nom}}$$

and for **TLEV** = 2:

$$dphidt =$$

$$\frac{\left[EG_{nom} + 3 \cdot Vt(T_{nom}) + (EG - EG_{nom}) \cdot \left(2 - \frac{T_{nom}}{T_{nom} + GAP2}\right) - PHI\right]}{T_{nom}}$$

10.7 Threshold voltage temperature equations (Levels 1, 2, 3 & 16)

The threshold temperature equations are as follows:

For $TLEV\mathbf{C} = 0$,

$$VTO(T) = Vbi(T) + GAMMA \cdot PHI(T)^{1/2}$$

$$Vbi(T) = Vbi(T_{nom}) + \frac{PHI(T) - PHI}{2} + \frac{EG_{nom} - EG(T)}{2}$$

For $TLEV\mathbf{C} = 1$,

$$VTO(T) = VTO - TCV \cdot \Delta T$$

$$Vbi(T) = VTO(T) - GAMMA \cdot PHI(T)^{1/2}$$

For $TLEV\mathbf{C} = 2$,

$$VTO(T) = VTO + \left(1 + \frac{GAMMA}{2 \cdot PHI^{1/2}}\right) \cdot dphidt \cdot \Delta T$$

$$Vbi(T) = VTO(T) - GAMMA \cdot (PHI(T))^{1/2}$$

10.8 Mobility temperature equations (Levels 1, 2, 3 & 16)

The MOS mobility temperature equations are as follows:

$$UO(T) = UO \cdot \left(\frac{T}{T_{nom}}\right)^{BEX}$$

$$KP(T) = KP \cdot \left(\frac{T}{T_{nom}}\right)^{BEX}$$

$$F1(T) = F1 \cdot \left(\frac{T}{T_{nom}}\right)^{F1EX}$$

10.9 Temperature Update (DIOLEV=9)



Please refer to the parameter table in “Diode Current Equations (DIOLEV=9)” on page 10-24.

In the case that **DIOLEV=9**, the following updates are performed.

The general rules, which apply to all three components of the JUNCAP model are:

$$Vt(T) = k_B \cdot \frac{T}{q} \quad \delta t = T - TRDIO9$$

$$EG_{eff}(T) = 1.16 - 7.02 \times 10^{-4} \cdot \frac{T^2}{T + 1108}$$

$$F_{TD} = \left(\frac{T}{TRDIO9} \right)^{1.5} \cdot \exp \left(\frac{EG_{eff}(TRDIO9)}{2 \cdot Vt(TRDIO9)} - \frac{EG_{eff}(T)}{2 \cdot Vt(T)} \right)$$

The internal reference parameters for the bottom component are specified by:

$$V_{DB} = VDBR \cdot \frac{T}{TRDIO9} - 2 \cdot Vt(T) \cdot \ln F_{TD}$$

$$C_{JB} = CJBR \cdot \left(\frac{VDBR - VR}{V_{DB}} \right)^{PB}$$

$$I_{SGB} = JSGBR \cdot F_{TD} \cdot \left(\frac{V_{DB}}{VDBR - VR} \right)^{PB}$$

$$I_{SDB} = JSGBR \cdot F_{TD}^2$$

Similar formulations hold for the sidewall component:

$$V_{DS} = VDSR \cdot \frac{T}{TRDIO9} - 2 \cdot Vt(T) \cdot \ln F_{TD}$$

$$C_{JS} = CJSR \cdot \left(\frac{VDSR - VR}{V_{DS}} \right)^{PS}$$

$$I_{SGS} = JSGR \cdot F_{TD} \cdot \left(\frac{V_{DS}}{VDSR - VR} \right)^{PS}$$

$$I_{SDS} = JSRSR \cdot F_{TD}^2$$

Similar formulations hold for the gate-edge component:

$$V_{DG} = VDGR \cdot \frac{T}{TRDIO9} - 2 \cdot Vt(T) \cdot \ln F_{TD}$$

$$C_{JG} = CJGR \cdot \left(\frac{VDGR - VR}{V_{DG}} \right)^{PG}$$

$$I_{SGG} = JSGR \cdot F_{TD} \cdot \left(\frac{V_{DG}}{VDGR - VR} \right)^{PG}$$

$$I_{SDG} = JSDGR \cdot F_{TD}^2$$

11.0 .OPTION ACM

Usually **ACM** is just a parameter which is an alias to **ARLEV**; i.e. it overwrites the values of **ALEV** & **RLEV**. However, if you specify **.OPTION ACM** in the netlist, then **ACM** has a much more effective role. It chooses the whole set of the junction diodes selectors; namely: **ALEV**, **RLEV**, **DIOLEV**, **DCAPLEV**, etc. Moreover, it affects the method of calculation of W_j' used for the calculation of the areas and perimeters of the junction, **Isat** calculation, default values setting, etc. Below is a list of the affect **.OPTION ACM** has:

- Sets the junction diode selectors, depending on the value of the **ACM** parameter set, according to the following table:

ACM^a	ALEV	RLEV	DIOLEV	DCAPLEV
0	0	0	2	3
1	1	1	2	3
2	2	2	2	5
3	3	3	2	0
10	0	0	6/7 ^b	4

ACM^a	ALEV	RLEV	DIOLEV	DCAPLEV
11	0	1	6/7 ^b	4
12	0/2 ^c	2	6/7 ^b	4
13	0	3	6/7 ^b	4

- a. If ACM is not given, $ACM=0$
in this case,
if ($ALEV$ & $RLEV$ & $DIOLEV$ & $DCAPLEV$ are not specified)
they take the values corresponding to $ACM=0$
else
they are left as they are
b. For $ACM=10$ to 13 , $DIOLEV=6$ is used with BSIM3v3.1, while $DIOLEV=7$ is used with BSIM3v3.2
c. For $ACM=12$, $ALEV=0$ is used when $CALCACM=0$ or not specified, while $ALEV=2$ is used when $CALCACM=1$

- Sets the default values of the following parameters if not already specified:
 - $PB=0.8$
 - $PHP (PBSW)=PB$
 - if ($ACM<10$) $XTI=0$
else $XTI=3$
 - if ($ACM<10$) $IS=0$ A
else $IS=1.0\times10^{-14}$ A
 - $JS=0$ Am $^{-2}$
 - $CJ=5.7911\times10^{-4}$ Fm $^{-2}$
 - $CJSW=0$ Fm $^{-1}$
 - $CJGATE = CJSW$ Fm $^{-1}$
 - $XPART=1$ (BSIM3v3 parameter)
 - $CAPMOD=0$ (BSIM3v3 parameter)

- Fixes the following parameters:
 - $TLEVI=3$
 - $TLEVRI=1$
 - $TRD2 = TRS2 = TRSH1 = TRSH2 = 0$
 - $FC=0$
- Issues a warning if the calculated $PXeff < Wj$
- If $ACM \geq 10$, $Isat$ is fixed to 1.0×10^{-14} if $AXeff = PXeff = 0$ with no further temperature update
- If $ACM \geq 10$, no temperature update is done for the junction capacitances for BSIM3v3 version < 3.2 only. For version 3.2, the temperature update is done normally.
- Changes the calculation of W_j for $ALEV=1, 2, 3$; $RLEV=1, 2, 3$; and $DCAPLEV=0, 5$ as follows:

$$W_j = W_{drawn} WMLT + XW_{scal}$$
- The BJT level 1 and level 5 resistor values of RB , RC , RE and RBM after temperature update are clipped to 1×10^{-5} if less than 1×10^{-5} .

12.0 OPTACM Model Parameter

A model parameter named **OPTACM** is implemented for all the common approach models. This parameter has the same effect as **.OPTION ACM** but is specific to one model, i.e. **.OPTION ACM** affects all the models in the netlist, whereas setting **OPTACM=1** in one of the models, has the effect of **.OPTION ACM** on this specific model and has no effect at all on the other models. By default, **OPTACM** is set to 0. Note: The effect on the model depends on the value of the **ACM** parameter set.

Setting **OPTACM=2** in one of the models also has the effect of option **ACM** on this specific model but with the following differences:

- If **ACM** is not already specified, it takes the default value of 10 instead of 0.
- If not already specified, BSIM3v3 model parameters **XPART** and **CAPMOD** will take their standard default value defined by the BSIM3v3 version used, instead of taking the default values of 1 and 0 respectively.



Please refer to “[.OPTION ACM](#)” on page 10-43 for more details about **.OPTION ACM**.

13.0 Noise Models in MOSFETs

Some MOSFET models, such as those listed below, have their own intrinsic noise models. They do not use Eldo models:

- AMS (Level 15)
- BNR-MISNAN (Level 46)
- CSEM (Level 48)
- Motorola SSIM (Level 54)
- BSIM3SOI (Level 55 & 56)
- MOS 9 (Level 59)
- BSIM4 (Level 60)

For BSIM3v3, EKV, and ST MOS models, when **THMLEV** (or **FLKLEV**) = 0, the internal default model is used, and not the default model of Eldo. Nevertheless, you can still use any of the other Eldo models specified with values not equal to 0.

13.1 Flicker Noise Models

- .OPTION flicker_noise=0 or .MODEL ... FLKLEV=0
(default model as implemented in SPICE)



Note

The model parameter **FLKLEV** has the same effect on the model as the more global **.OPTION flicker_noise**.

$$SI = \frac{KF \times ID^{AF}}{COX \times f \times Leff^2}$$

- .OPTION flicker_noise=1 or .MODEL ... FLKLEV=1

$$SI = \frac{KF \times gm^2}{COX \times Weff \times Leff \times f^{AF}}$$

- .OPTION flicker_noise=2 or .MODEL ... FLKLEV=2

$$SI = \frac{KF \times gm^2}{COX^2 \times Weff \times Leff \times f^{AF}}$$

- .OPTION flicker_noise=3 or .MODEL ... FLKLEV=3

$$SI = \frac{KF \times ID^{AF}}{COX \times f \times Weff \times Leff}$$

13.2 Thermal Noise Models

- Modified SPICE Noise Model: default model
(.OPTION thermal_noise=0 or .MODEL ... THMLEV=0)

$$SI = \frac{8 \times k \times T \times gm}{3}$$

- Strong Inversion Model
(.OPTION thermal_noise=1 or .MODEL ... THMLEV=1)

$$SI = 4 \times k \times T \times g_{tot} \times K(a)$$

$$K(a) = \frac{2}{3} \times \frac{1+a+a^2}{1+a}, \quad a = 1 - \frac{V_{ds}}{V_{dsat}}$$

for $V_{ds} < V_{dsat}$, else $a=0$.

$$g_{tot} = gm + g_{ds} + g_{mb}$$

$$gm = \frac{dIds}{dV_{gs}}, \quad g_{ds} = \frac{dIds}{dV_{ds}}, \quad g_{mb} = \frac{dIds}{dV_{bs}}$$

- Weak & Strong Inversion Model

(.OPTION thermal_noise=2 or .MODEL ... THMLEV=2)

$$SI = 4 \times k \times T \times g_{tot} \times K(a)$$

$$K(a) = \frac{1}{1+if} \times \left(\frac{1+a}{2} + if \times \frac{2}{3} \times \frac{1+\sqrt{a+a^2}}{1+\sqrt{a}} \right), \quad a = \frac{ir}{if},$$

$$if = \Psi\left(\frac{V_{dsat}}{V_t}\right), \quad ir = \Psi\left(\frac{V_{dsat}-V_{ds}}{V_t}\right),$$

$$V_t = \frac{k \times T}{q}, \quad \Psi(x) = \ln(1+e^{x/2}) \times \ln(1+e^{x/2})$$

- Weak & Strong Inversion Model with Short Channel Effects

(.OPTION thermal_noise=3 or .MODEL ... THMLEV=3)

$$SI = 4 \times k \times T \times \left(K(a) \times g_{tot} \times \frac{L}{L-\Delta L} + Ids \times \frac{\Delta L}{Ecrit \times L^2} \right)$$

$$\Delta L = \frac{V_{ds} - V_{dsat}}{V_{ea} + V_{ds}} \times L$$

if $V_{ds} < V_{dsat}$ or $V_{dssat} = 0$ then ΔL is 0, else it is as specified above.

$$K(a) = \frac{1}{1+if} \times \left(\frac{1+a}{2} + if \times \frac{2}{3} \times \frac{1+\sqrt{a+a^2}}{1+\sqrt{a}} \right), \quad a = \frac{ir}{if}$$

- Strong Inversion Model with Short Channel Effects

(.OPTION thermal_noise=4 or .MODEL ... THMLEV=4)

$$SI = 4 \times k \times T \times \left(K(a) \times g_{tot} \times \frac{L}{L - \Delta L} \times \frac{2}{3} + Ids \times \frac{\Delta L}{Ecrit \times L^2} \right)$$

$$K(a) = \frac{1 + a + a^2}{1 + a}, \quad a = 1 - \frac{V_{ds}}{V_{dsat}} \text{ for } V_{ds} < V_{dsat}, \text{ else } a=0.$$

$$g_{tot} = gm + gds + gmb$$

$$gm = \frac{dIds}{dVgs}, \quad gds = \frac{dIds}{dVds}, \quad gmb = \frac{dIds}{dVbs}$$

$\Delta L = 0$ for $V_{ds} < V_{dsat}$ or $V_{dsat} = 0$, else it is as

$$\text{specified by: } \Delta L = \frac{V_{ds} - V_{dsat}}{V_{ea} + V_{ds}} \times L$$

Chapter 11

MOS Level 1, 2, 3 Equations

1.0 Berkeley Spice Model General Threshold Voltage Equations

1.1 Calculation of GAMMA, PHI and VTO

Bulk threshold parameter *GAMMA*

Unless **GAMMA** is assigned a value, it is calculated as:

$$GAMMA = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot NSUB}}{COX}$$

Surface potential *PHI*

Unless **PHI** is assigned a value, it is calculated as: $PHI = 2 \cdot V_t \cdot \ln\left(\frac{NSUB}{ni}\right)$

Where V_t is the thermal voltage.

Zero bias threshold voltage

Unless **VTO** is assigned a value, it is calculated as:

$$VTO = WK - \frac{q \cdot NSS}{COX} + GAMMA \cdot \sqrt{PHI} + PHI$$

Where **WK** is calculated as follows:

If **TPG** is equal to either 1 or -1 then: $WK = type \frac{(-TPG \cdot eg - PHI)}{2}$

Else if TPG equals 0 then: $WK = -0.05 - \frac{eg}{2} - type\left(\frac{PHI}{2}\right)$

Where $type$ is 1 for n-channel and -1 for p-channel.

$$eg = 1.16 - \left(7.02 \cdot 10^{-4} \cdot \frac{TNOM^2}{TNOM + 1108} \right)$$

Effective channel length and width

These are determined as follows:

$$L_{eff} = L - 2 \cdot LD_{scal} \quad W_{eff} = L - 2 \cdot WD_{scal}$$

For PRECISE compatibility the equations are:

$$\begin{aligned} L_{eff} &= L \cdot LMLT + DELL_{scal} - DL_{scal} - 2 \cdot LD_{scal} \\ W_{eff} &= W \cdot WMLT + DELW_{scal} - DW_{scal} - 2 \cdot WD_{scal} \end{aligned}$$

For Level 12, 13, and 17 the effective length and width are determined as:

$$\begin{aligned} L_{eff} &= L \cdot LMLT + DL_{scal} - 2 \cdot (LD_{scal} - DEL_{scal}) \\ W_{eff} &= W \cdot WMLT + DW_{scal} - 2 \cdot WD_{scal} \end{aligned}$$

2.0 MOSFET Level 1 Equations

This level is fairly simple because it does not contain any mobility degradation model, carrier saturation effect or weak inversion model.

2.1 Threshold voltage V_{th}

If $VBS \leq 0$ then: $V_{th} = V_{bi} + GAMMA \cdot \sqrt{PHI - vbs}$

else: $V_{th} = V_{bi} + GAMMA \cdot \left(\sqrt{PHI} - \left(0.5 \cdot \frac{vbs}{\sqrt{PHI}} \right) \right)$

where: $V_{bi} = VTO - GAMMA \cdot \sqrt{PHI}$

2.2 Saturation voltage V_{dsat}

The saturation voltage level 1 is due to pinch-off at the drain side and is calculated using the following relationship:

$$V_{dsat} = vgs - V_{th}$$

2.3 I_{ds} current equations

For the Cut-off Region ($vgs < V_{th}$): $I_{ds} = 0$

For both Linear Region ($vgs > V_{th}$ and $vds \leq V_{dsat}$)

and Saturation Region ($vgs > V_{th}$ and $vds > V_{dsat}$):

$$I_{ds} = KP \cdot \frac{W_{eff}}{L_{eff}} \cdot (1 + LAMBDA \cdot vds) \cdot \left(vgs - V_{th} - \frac{V_{dsmin}}{2} \right) \cdot V_{dsmin}$$

where: $V_{dsmin} = \min(vds, V_{dsat})$ and if KP is unspecified: $KP = UO \cdot COX$

3.0 MOSFET Level 2 Equations

3.1 Threshold voltage V_{th}

Definition of internal parameters

Depletion widths W_s and W_d are determined as follows:

$$W_s = \sqrt{\frac{2 \cdot \varepsilon_{si}}{q \cdot NSUB} \cdot (PHI - vbs)} \quad \text{and} \quad W_d = \sqrt{\frac{2 \cdot \varepsilon_{si}}{q \cdot NSUB} \cdot (PHI - vbd)}$$

The narrow width effect is included through η as:

$$\eta = 1 + DELTA \cdot \frac{\pi \varepsilon_{si}}{4Co \cdot W_{eff}}$$

The short channel effect is included through γ .

$$\gamma = GAMMA \left(1 - \frac{XJ}{L_{eff}} \left[\sqrt{1 + \frac{2W_s}{XJ}} + \sqrt{1 + \frac{2W_d}{XJ}} - 2 \right] \right)$$

The built-in voltage, V_{bi} is defined as follows:

$$V_{bi} = VTO - GAMMA \sqrt{PHI} + (\eta - 1) \cdot (PHI - vbs)$$

The effective threshold voltage is calculated as follows:

$$V_{th} = V_{bi} + \gamma \sqrt{PHI - vbs}$$

-  See “Berkeley Spice Model General Threshold Voltage Equations” on page 11-1 for the calculation of **GAMMA**, **PHI** and **VTO**.

Mobility reduction

In order to simulate the reduction of mobility with an increase in the gate voltage, the effective mobility, U_{eff} , is calculated as:

$$U_{eff} = U_o \left(\frac{UCRIT \cdot \epsilon_{si}}{COX \cdot (vgs - V_{th}) - UTRA \cdot vds} \right)^{UEXP}$$

The value of the term in parenthesis is limited between 0 and 1.

-  See also “Level 2 Precise compatibility” on page 11-7.



Unless **KP** is assigned a value, it is calculated as:

$$KP = UO \cdot COX$$

Note

In order to be Spice compatible, when **KP** is specified, the parameter U_{eff} is not calculated and its value is then the default value or else the specified value. So the user is advised to only use the parameter U_{eff} or to make sure that the previous equality is correct (especially when **VMAX** is specified).

Channel length modulation

The channel length modulation effect is introduced by modifying the Ids current as follows:

$$Ids = \frac{Ids}{1 - \lambda vds}$$

The value of λ is calculated unless the parameter **LAMBDA** is specified, then:

$\lambda = LAMBDA$ otherwise:

If **VMAX** > 0 then:

$$\lambda = \frac{X_d}{\sqrt{NEFF} \cdot L_{eff} \cdot vds} \cdot \left(\left[\left(\frac{VMAX \cdot X_d}{2 \cdot U_{eff} \cdot \sqrt{NEFF}} \right)^2 + vds - V_{dsat} \right]^{\frac{1}{2}} - \frac{VMAX \cdot X_d}{2 \cdot U_{eff} \cdot \sqrt{NEFF}} \right)$$

$$\text{else: } \lambda = \frac{X_d}{L_{eff} \cdot vds} \cdot \left[\frac{vds - V_{dsat}}{4} + \left\{ 1 + \left(\frac{vds - V_{dsat}}{4} \right)^2 \right\}^{\frac{1}{2}} \right]^{\frac{1}{2}}$$

Where X_d is calculated as: $X_d = \sqrt{\frac{2\varepsilon_{si}}{q \cdot NSUB}}$



See also “Level 2 Precise compatibility” on page 11-7.

Saturation voltage V_{dsat}

$$V_{sat} = \frac{vgs - V_{bi}}{\eta} + \left(\frac{\gamma}{\sqrt{2} \cdot \eta} \right)^2 \times \left(1 - \sqrt{1 + \left(\frac{2n}{\gamma} \right)^2 \times \left(\frac{vgs - V_{bi}}{\eta} + PHI - vbs \right)} \right)$$

If **VMAX** is specified, a different V_{dsat} calculation is performed.

Else if **ECRIT** is specified, Eldo modifies V_{sat} to include carrier velocity saturation effect:

$$V_{dsat} = V_{sat} = ECRIT \cdot L_{eff} - \sqrt{V_{sat}^2 + (ECRIT \cdot L_{eff})^2}$$

Otherwise: $V_{dsat} = V_{sat}$



See also “Level 2 Precise compatibility” on page 11-7.

Ids current equations

Current is calculated for three different regions determined by Gate to Source voltage vgs , Drain to Source voltage vds and Bulk to Source voltage vbs and is written as $Ids(vgs, vds, vbs)$.

- Cut-off Region or Subthreshold Region $vgs < V_{th}$

Unless NFS is assigned a value, the Ids current is given by:

$$Ids(vgs, vds, vbs) = 0$$

Otherwise, a modified threshold voltage V_{on} is calculated as:

$$V_{on} = V_{th} + IENH \cdot X_n \cdot V_t$$

Where V_t is the thermal voltage and:

$$X_n = \eta + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2\sqrt{PHI - vbs}} - \left(\sqrt{PHI - vbs} \cdot \frac{\partial \gamma}{\partial vbs} \right)$$

$\frac{\partial \gamma}{\partial vbs}$ is the partial derivative with respect to the voltage from the Bulk to the Source.

V_{on} is then used in the Drain current equations as: $vgs < V_{on}$

$$Ids(vgs, vds, vbs) = Ids(V_{on}, V_{dsmin}, vbs) \exp\left(\frac{vgs - V_{on}}{V_t \cdot X_n}\right)$$

where: $V_{dsmin} = \min(vds, V_{dsat})$ and: $Ids(vgs, vds, vbs)$ is calculated in the linear and saturation regions.



The modified threshold voltage V_{on} is also used in the Inversion Region instead of V_{th} which is used mainly in the mobility equations.

- Saturation & Linear Region

$$Ids(vgs, vds, vbs) =$$

$$\beta \cdot \left(\left(vgs - V_{bi} - \frac{\eta \cdot V_{dsmin}}{2} \right) \cdot V_{dsmin} - \frac{2}{3} \cdot \gamma \cdot \left((PHI - vbd)^{\frac{3}{2}} - (PHI - vbs)^{\frac{3}{2}} \right) \right)$$

$$\text{where: } \beta = COX \cdot U_{eff} \cdot \frac{W_{eff}}{L_{eff}}$$



See the following “Mobility Reduction” section for U_{eff} .

3.2 Level 2 PRECISE compatibility

Mobility reduction

The parameter **LMOB** enables the definition of one of several mobility degradation equations. The default value is **LMOB=1**.

$$\text{For } LMOB=1: \quad U_{eff} = UO \cdot \left(\frac{UCRIT \cdot \varepsilon_{si}}{COX(vgs - V_{th})} \right)^{UEXP}$$

For **LMOB=2**:

$$U_{eff} = \frac{UO}{1 + UCRIT \cdot \frac{V_{gs} - V_{th}}{TOX} + \frac{V_{dsmin}}{UTRA \cdot L_{eff}} + UEXP \cdot \sqrt{vbs}}$$

$$\text{For } LMOB=3: \quad U_{eff} = \frac{UO}{1 + UCRIT \cdot (vgs - V_{th})^{UEXP}}$$

Channel length modulation

The parameter **LCLM** enables the use of several channel length modulation equations. The default is **LCLM = 1**. The modification of I_{ds} is achieved by replacing L_{eff} by L_o in the previous sections.

For **LCLM = 1**: $L_o = L_{eff} \cdot (1 - \lambda \cdot vds)$

Where if **LAMBDA** is specified, $\lambda = LAMBDA$.

$$\text{Otherwise: } \lambda = \frac{X_d}{L_{eff} \cdot vds} \sqrt{\frac{vds - V_{sat}}{4} + \sqrt{\left(\frac{vds - V_{dsat}}{4}\right)^2 + 1}}$$

$$\text{and: } X_d = \sqrt{\frac{2\epsilon_{si}}{q \cdot NSUB}}$$

For **LCLM = 2**:

If $vds \geq V_{dsat}$ then: $L_o = L_{eff} - \Delta L$, else: $L_o = L_{eff}$.

$$\text{where: } \Delta L = X_d \sqrt{\left(\frac{X_d \cdot VMAX}{2U_{eff}}\right)^2 + vds - V_{dsat}} - \frac{VMAX \cdot X_d^2}{2U_{eff}}$$

$$\text{and: } X_d = \sqrt{\frac{2\epsilon_{si}}{q \cdot NEFF \cdot NSUB}}$$

For **LCLM = 3** (used with parameter **K1**):

If $vds \geq V_{dsat}$ then: $L_o = L_{eff} - \Delta L$ else: $L_o = L_{eff}$

$$\text{where: } \Delta L = \frac{\lambda L_{eff}}{1 + K1 \cdot L_{eff}} (vds - V_{dsat})$$



For λ calculations, see the case where **LCLM = 1**.

Saturation voltage V_{dsat}

The parameter $LVSAT$ enables the use of one of several saturation voltage equations. The default value is $LVSAT = 1$. Regardless of the value of $LVSAT$, V_{sat} is calculated as previously shown.

$$\text{For } LVSAT = 1: \quad V_{dsat} = V_{sat}$$

For $LVSAT = 2$: Use the parameter $VMAX$ from which V_{dsat} is calculated according to the following equation:

$$VMAX =$$

$$\frac{U_{eff} \cdot \left(\frac{vgs - V_{bi} - \eta V_{dsat}}{2} \cdot V_{dsat} - \frac{2}{3} \cdot \gamma \cdot \left((V_{dsat} + PHI - vbs)^{\frac{3}{2}} - (PHI - vbs)^{\frac{3}{2}} \right) \right)}{L_{eff} \cdot (vgs - V_{bi} - \eta \cdot V_{dsat} - \gamma \cdot \sqrt{V_{dsat} + PHI - vbs})}$$



For more information, see “*The Simulation of MOS Integrated Circuits Using Spice 2*” by Andrei-Vladiminesco and Sally Liv. Memorandum No. UCB/ER1 M80/7 February 1980.

$$\text{For } LVSAT = 3: \quad V_{dsat} = V_{sat} + V_c - \sqrt{V_{sat}^2 + V_c^2}$$

$$\text{Where: } \quad V_c = L_{eff} \cdot VMAX$$

4.0 MOSFET Level 3 Equations

4.1 Threshold voltage V_{th}

Definition of internal parameters

The term W_p is the depletion layer width of a planar junction.

$$W_p = \sqrt{\frac{2\epsilon_{si}}{q \cdot NSUB} \cdot (PHI - vbs)}$$

The term W_c is the depletion layer width of a cylindrical junction.

$$W_c = XJ \left[0.0631353 + 0.8013292 \cdot \frac{W_p}{XJ} - \left(0.01110777 \cdot \left(\frac{W_p}{XJ} \right)^2 \right) \right]$$

The term λ_n expresses the effect of narrow width.

$$\lambda_n = \frac{DELTA \cdot \pi \cdot \epsilon_{si}}{2 \cdot COX \cdot W_{eff}}$$

The term λ_s expresses the effect of short channel.

$$\lambda_s = 1 - \frac{XJ}{L_{eff}} \cdot \left(\frac{LD + W_c}{XJ} \cdot \sqrt{1 - \left(\frac{W_p}{XJ + W_p} \right)^2} - \frac{LD}{XJ} \right)$$

The built-in voltage V_{bi} is defined as follows:

$$V_{bi} = VTO - GAMMA \cdot \sqrt{PHI}$$

The effective threshold voltage is defined as follows:

$$V_{th} = V_{bi} - \frac{8.14 \times 10^{-22} \cdot ETA}{COX \cdot L_{eff}^3} \cdot vds + GAMMA \cdot \lambda_s \cdot \sqrt{PHI - vbs} + \lambda_n \cdot (PHI - vbs)$$

With the PRECISE option, use 8.15×10^{-22} as the constant instead of 8.14×10^{-22} .



See “Berkeley Spice Model General Threshold Voltage Equations” on page 11-1 for the calculation of **GAMMA**, **PHI** and **VTO**.

4.2 Mobility reduction

Effective mobility, U_{eff} , is calculated as follows:

$$\text{If } VMAX \leq 0 \text{ then: } U_{eff} = V_s \quad \text{else: } U_{eff} = \frac{U_s}{1 + \frac{V_{dsmin}}{V_c}}$$

$$\text{where the effective surface mobility } U_s \text{ is: } U_s = \frac{U_O}{1 + THETA(vgs - V_{th})}$$

$$\text{and: } V_c = \frac{VMAX \cdot L_{eff}}{U_s} \quad \text{and} \quad V_{dsmin} = \min(vds, V_{dsat})$$

4.3 Channel length modulation

The channel length modulation effect is included by modifying the Ids current in the saturation region as follows:

$$Ids = \frac{Ids}{1 - \frac{\Delta L}{L_{eff}}}$$

Where the channel length reduction ΔL is calculated as follows:

$$\text{If } VMAX \leq 0 \text{ then: } \Delta L = X_d \cdot KAPPA \cdot \sqrt{vds - V_{dsat}}$$

$$\text{else: } \Delta L = -\frac{E_p \cdot X_d^2}{2} \left[\left(\frac{E_p \cdot X_d^2}{2} \right)^2 + KAPPA \cdot X_d^2 \cdot (vds - V_{dsat}) \right]^{\frac{1}{2}}$$

where E_p is the lateral electric field at the pinch-off point.

$$E_p = \frac{I_{dsat}}{g_{dsat} \cdot L_{eff}} \quad \text{and} \quad X_d = \sqrt{\frac{2\epsilon_{si}}{q \cdot NSUB}}$$

4.4 Saturation voltage V_{dsat}

$$V_{sat} = \frac{vgs - V_{th}}{1 + \lambda_b}$$

If $VMAX \leq 0$ then: $V_{dsat} = V_{sat}$

else: $V_{dsat} = V_{sat} + V_c - \sqrt{V_{sat}^2 + V_c^2}$

where the expression for V_c is given in the “Mobility reduction” on page 11-11.

4.5 I_{ds} current equations

Current is calculated for three different regions determined by Gate to Source voltage, Drain to Source voltage and Bulk to Source voltage and is written as I_{ds} (vgs, vds, vbs).

Cut-off or subthreshold region $vgs < V_{th}$

Unless NFS is assigned a value, the I_{ds} current is given by the following equation:

$$I_{ds}(vgs, vds, vbs) = 0$$

Otherwise, a modified threshold voltage V_{on} is calculated as follows:

$$V_{on} = V_{th} + V_t \cdot X_n \cdot IENH$$

where V_t is the Thermal voltage.

$$X_n = 1 + \frac{q \cdot NFS}{COX} + \frac{1}{2} \cdot \left[\frac{GAMMA \cdot \lambda_s}{\sqrt{PHI - vbs}} + \lambda_n \right]$$

V_{on} is then used in the current equations as follows:

If $vgs < V_{on}$ then: $Ids(vgs, vds, vbs) = Ids(V_{on}, V_{dsmin}, V_{bs}) \cdot \exp\left(\frac{vgs - V_{on}}{V_t \cdot X_n}\right)$

where: $V_{dsmin} = \min(vds, V_{dsat})$



Note

The modified threshold voltage is not used in the inversion Region.

4.6 Linear & saturation region

$$Ids(vgs, vds, vbs) = \beta \cdot \left(vgs - V_{th} - \frac{1 + \lambda_b}{2} \cdot V_{dsmin} \right) \cdot V_{dsmin}$$

Where: $\beta = U_{eff} \cdot COX \cdot \frac{W_{eff}}{L_{eff}}$ and $\lambda_b = \lambda_n + \frac{GAMMA \cdot \lambda_s}{4 \cdot \sqrt{PHI - vbs}}$



Note

In the above equation the factor 4 should be 2, but since SPICE uses a factor of 4, HSPICE uses a factor of 4 as well.

4.7 Modified Eldo Level=3 (Level=13)

Surface mobility UO , is calculated as follows:

$$UO = UO \left(\frac{T}{T_{nom}} \right)^{BEX}$$

Transconductance KP , is calculated as follows:

$$KP = KP \left(\frac{T}{T_{nom}} \right)^{BEX}$$

where T is the simulation temperature.

5.0 MOSFET Gate Capacitances Equations

There are different formulations for the Berkeley Spice Model gate capacitances. The user selects these formulations by using the input parameter **CAPLEV** or **LCAP** (precise compatibility).

5.1 Definitions

It is possible to use **COX** & **TOX** separately as follows:

- If both (**COX** and **TOX**) are NOT given: the default values are used
- If only one (**COX** or **TOX**) is given: the other is calculated from the one provided using the relation **COX=EPSOX/TOX**
- If both (**COX** and **TOX**) are given: **COX** is used as is for the capacitance, while **TOX** is used as is in other expressions giving other model parameters.

The effective MOS capacitance value **CAPOX** is calculated as follows:

$$CAPOX = COX \cdot W_{eff} \cdot L_{eff}$$

5.2 Spice Meyer gate capacitances—CAPLEV=0

For precise compatibility these equations corresponded to **LCAP** = 2.

- Accumulation: ($vgs - Vth \leq -PHI$)

$$Cgb = CAPOX; Cgd = 0; Cgs = 0$$

- Accumulation: ($vgs - Vth \leq -PHI/2$)

$$Cgb = -CAPOX \cdot \frac{vgs - Vth}{PHI}; Cgd = 0; Cgs = 0$$

- Depletion: ($vgs - Vth \leq 0$)

$$Cgb = -CAPOX \cdot \frac{vgs - Vth}{PHI}; Cgd = 0;$$

$$Cgs = \frac{CAPOX}{1.5} \cdot \left(\frac{2 \cdot (vgs - Vth)}{PHI} + 1 \right)$$

- Strong inversion: ($vgs - Vth > 0$)

- linear region: ($vds < Vdsat$)

$$Cgb = 0$$

$$Cgd = \frac{CAPOX}{1.5} \cdot \left(1 - \left(\frac{Vdsat - vbs}{2 \cdot (Vdsat - vbs) - vdb} \right)^2 \right)$$

$$Cgs = \frac{CAPOX}{1.5} \cdot \left(1 - \left(\frac{Vdsat - vds}{2 \cdot (Vdsat - vbs) - vdb} \right)^2 \right)$$

- saturation region: ($vds \geq Vdsat$)

$$Cgb = 0; Cgd = 0; Cgs = \frac{CAPOX}{1.5}$$

5.3 Modified Meyer gate capacitances—CAPLEV=1

- Gate-Bulk capacitance

- Accumulation: ($vgs \leq Vfb + vbs$)

$$Cgb = CAPOX$$

- Depletion: ($vgs \leq Vth$)

$$Cgb = \frac{CAPOX}{\left(1 + \left(\frac{2}{GAMMA} \right)^2 \cdot (vgs - vbs - Vfb) \right)^{CGBEX}}$$

- Strong inversion: ($vgs > Vth$)

$$Cgb = \frac{CAPOX}{\left(1 + \left(\frac{2}{GAMMA}\right)^2 \cdot (GAMMA \cdot \sqrt{PHI - vbs} + PHI - vbs)\right)^{CGBEX}}$$

**Note**

For Precise compatibility, $CGBEX$ is not a parameter and is replaced by 0.5.

- Gate-Drain capacitance

- Low vds ($vds < 0.1$)

- Accumulation: ($vgs \leq Vth$)

$$Cgd = \frac{CAPOX}{1.5} \cdot Gm \cdot Dm$$

- Weak inversion: ($vgs < Vth + 0.1$)

$$Cgd = \frac{CAPOX}{1.5} \cdot \left(Dm + 10 \cdot (vgs - Vth) \cdot \max\left(1 - \frac{0.01}{(0.2 - vds)^2}, 0\right) \right)$$

- Strong inversion: ($vgs \geq Vth + 0.1$)

$$Cgd = \frac{CAPOX}{1.5} \cdot \max\left(Dm; 1 - \left(\frac{vgs - Vth}{2 \cdot (vgs - Vth) - vds}\right)^2\right)$$

- High vds ($vds \geq 0.1$)

- Accumulation: ($vgs \leq Vth$)

$$Cgd = \frac{CAPOX}{1.5} \cdot Gm \cdot Dp$$

- Saturation region: ($vgs < Vth + vds$)

$$Cgd = \frac{CAPOX}{1.5} \cdot Dp$$

- Strong inversion: ($vgs \geq Vth + vds$)

$$Cgd = \frac{CAPOX}{1.5} \cdot \max(Dp; 1 - \left(\frac{vgs - Vth}{2 \cdot (vgs - Vth) - vds} \right)^2)$$

- Gate-Source capacitance

- Low vds ($vds < 0.1$)

- Accumulation: ($vgs \leq Vth$)

$$Cgs = \frac{CAPOX}{1.5} \cdot Gm \cdot Dm$$

- Weak inversion: ($vgs < Vth + 0.1$)

$$Cgs = \frac{CAPOX}{1.5} \cdot \left(Dm + 10 \cdot (vgs - Vth) \cdot \left(1 - \left(\frac{0.1 - vds}{0.2 - vds} \right)^2 - Dm \right) \right)$$

- Strong inversion: ($vgs \geq Vth + 0.1$)

$$Cgs = \frac{CAPOX}{1.5} \cdot \left(1 - \left(\frac{vgs - Vth - vds}{2 \cdot (vgs - Vth) - vds} \right)^2 \right)$$

- High vds ($vds \geq 0.1$)

- Accumulation: ($vgs \leq Vth$)

$$Cgs = \frac{CAPOX}{1.5} \cdot Gm$$

- Weak inversion: ($vgs < Vth + vds$)

$$Cgs = \frac{CAPOX}{1.5}$$

- Strong inversion: ($vgs \geq Vth + vds$)

$$Cgs = \frac{CAPOX}{1.5} \cdot \left(1 - \left(\frac{vgs - Vth - vds}{2 \cdot (vgs - Vth) - vds} \right)^2 \right)$$

Where Gm , Dm , Dp are smoothing functions that depend on vgs and vds . The expressions are different for standard Eldo mode and Precise compatibility mode.

5.4 Parameterized modified Meyer capacitances— CAPLEV=2

The **CAPLEV=2** Meyer capacitance model is the more general form of Meyer capacitance. The **CAPLEV=1** Meyer capacitance model is the special case of **CAPLEV=2** when $CF1=0$, $CF2=0.1$, and $CF3=1$.

In the following equations, Gm , Gp , Dm , and DDp are smoothing factors. They are not user-defined parameters.

- Gate-Bulk capacitance (Cgb)

- Accumulation: ($vgs \leq vfb - vsb$)

$$Cgb = CAPOX$$

- Depletion: ($vgs \leq Vth$)

$$Cgs = \frac{CAPOX}{\left(1 + 4 \cdot \frac{vgs + vsb - vfb}{GAMMA^2}\right)^{1/2}}$$

- Inversion: ($vgs > Vth$)

$$Cgb = \frac{Gp \cdot CAPOX}{\left[1 + 4 \cdot \frac{GAMMA \cdot (PHI + vsb)^{1/2} + PHI + vsb}{GAMMA^2}\right]^{1/2}}$$

- Gate-Source capacitance (Cgs)

- Low vds ($vds < 0.1$)

- Accumulation: ($vgs < Vth - CF1$)

$$C_{gs} = CF5 \cdot CAPOX \cdot Gm \cdot Dm$$

- Depletion: ($vgs \leq Vth + CF2 - CF1$)

$$C_{gs} = CF5 \cdot CAPOX \cdot$$

$$\left\{ \frac{vgs - Vth + CF1}{CF2} \cdot \left[1 - \left(CF2 - \frac{vds}{2 \cdot CF2 - vds} \right)^2 - Dm \right] + Dm \right\}$$

- Strong Inversion:
($vgs > Vth + \max(CF2 - CF1, CF3 \cdot vds)$ **UPDATE=0**)

Strong Inversion: ($vgs > Vth + CF2 - CF1$, **UPDATE=1**)

$$C_{gs} = CF5 \cdot CAPOX \cdot \left\{ 1 - \left[\frac{vgs - Vth + CF1 - vds}{2 \cdot (vgs - Vth + CF1) - vds} \right]^2 \right\}$$

- High vds ($vds \geq 0.1$)

- Accumulation: ($vgs < Vth - CF1$)

$$C_{gs} = CF5 \cdot CAPOX \cdot Gm \cdot Dp \quad CF1 \neq 0$$

$$C_{gs} = CF5 \cdot CAPOX \cdot Gm \quad CF1 = 0$$

- Weak Inversion: ($vgs < Vth + CF2 - CF1$, $CF1 \neq 0$)

$$C_{gs} = CF5 \cdot CAPOX \cdot \max\left(\frac{vgs - Vth + CF1}{CF2}, Dp\right)$$

- Saturation: ($vgs < Vth + CF3 \cdot vds$)

$$C_{gs} = CF5 \cdot CAPOX$$

- Linear Region: ($vgs > Vth + CF3 \cdot vds$)

$$C_{gs} = CF5 \cdot CAPOX \cdot \left\{ 1 - \left[\frac{vgs - Vth - vds}{2 \cdot (vgs - Vth) - vds} \right]^2 \right\}, UPDATE = 0, CF1 = 0$$

$$C_{gs} = CF5 \cdot CAPOX \cdot \left\{ 1 - \left[\frac{vgs - Vth - CF3 \cdot vds}{2 \cdot (vgs - Vth) - CF3 \cdot vds} \right]^2 \right\}, UPDATE = 1$$

- Gate-Drain capacitance (C_{gd})

- Low vds ($vds < 0.1$)
 - Accumulation: ($vgs \leq Vth - CF1$)

$$C_{gd} = CF5 \cdot CAPOX \cdot Gm \cdot Dm$$

- Weak Inversion: ($vgs < Vth + CF2 - CF1$)

$$C_{gd} = CF5 \cdot CAPOX \cdot$$

$$\left\{ Dm + \frac{vgs - Vth + CF1}{CF2} \cdot \max \left[0, 1 - \left(\frac{CF2}{2 \cdot CF2 - vds} \right)^2 - Dm \right] \right\}$$

- Strong Inversion: ($vgs \geq Vth + CF2 - CF1$)

$$C_{gd} = CF5 \cdot CAPOX \cdot \max \left\{ Dm, 1 - \left[\frac{vgs - Vth + CF1}{2 \cdot (vgs - Vth + CF1) - vds} \right]^2 \right\}$$

- High vds ($vds > 0.1$)
 - Accumulation: ($vgs \leq Vth - CF1$)

$$C_{gd} = CF5 \cdot CAPOX \cdot Gm \cdot DDp$$

- Saturation Region: ($vgs \leq Vth + CF3 \cdot vds$)

$$Cgd = CF5 \cdot CAPOX \cdot DDp$$



In the above equation, DDp is a function of $CF3$ if $UPDATE=1$.

Note

- Linear Region: ($vgs > Vth + CF3 \cdot vds$)

$$Cgd = CF5 \cdot CAPOX \cdot \max\left\{DDp, 1 - \left[\frac{vgs - Vth}{2 \cdot (vgs - Vth) - CF3 \cdot vds}\right]^2\right\}$$

6.0 Charge Equations

In Eldo there are two charge control models that may be selected for capacitances formulation with the **CAPLEV** parameter. The first formulation accessible through **CAPLEV** = 3 is compatible with the SPICE2G.6 program but have discontinuity that can cause some convergence problem, so its use is not recommended. The second is the ANACAD improved version accessible through **CAPLEV** = 4, and ensures continuity in the different regions of operations, and consistency with the current equations.

Both charge conservation method are based on a paper by Donald E. Ward and Robert W. Dutton, ("A Charge-Oriented Model for MOS Transistor Capacitances" *IEEE Journal of Solid State Circuits*, vol. SC-13, pp 703-707, Oct 1978) and need the additional parameter **XQC** which determines the channel charge partitioning between drain and source in saturation region.

6.1 Charge equations for Level 2

Applicable to Eldo Levels 2, 12, and 17.

- Accumulation: ($vgs \leq Vfb + vbs$)

$$Qg = CAPOX \cdot (vgs - vbs - Vfb)$$

$$Qb = -Qg; Qs = Qd = 0$$

- Substhreshold: ($vgs > Vfb + vbs$)

$$Qg = CAPOX \cdot \frac{\gamma^2}{2} \cdot \left(\sqrt{1 + \frac{4 \cdot (vgs - vbs - Vfb)}{\gamma^2}} - 1 \right)$$

$$Qb = -Qg; Qs = Qd = 0$$

- Strong inversion: ($vgs > Vth$)

$$Qg = CAPOX \cdot \left(\frac{U_g^2 \cdot (U_d - U_s) - \frac{2}{3} \cdot \gamma \cdot U_g \cdot (U_d^{3/2} - U_s^{3/2})}{F(U_g, U_d, U_g)} \right. \\ \left. - \frac{U_g \cdot (U_d^2 - U_s^2) + \frac{2}{5} \cdot \gamma \cdot (U_d^{5/2} - U_s^{5/2}) + \frac{1}{3} \cdot (U_d^3 - U_s^3)}{F(U_g, U_d, U_g)} \right)$$

$$Qb = -CAPOX \cdot$$

$$\left(\frac{\frac{2}{3} \cdot U_g \cdot \gamma \cdot (U_d^{3/2} - U_s^{3/2}) - \frac{1}{2} \cdot \gamma^2 \cdot (U_d^2 - U_s^2) - \frac{2}{5} \cdot \gamma \cdot (U_d^{5/2} - U_s^{5/2})}{F(U_g, U_d, U_g)} \right)$$

$$Qd = -Xqc \cdot (Qg + Qb); Qs = (Xqc - 1) \cdot (Qg + Qb)$$

where:

- Xqc is the partitioning factor that may vary from 0.5 when $vds = 0$ to XQC parameter value in saturation region.
- $F(U_g, U_d, U_g) = U_g \cdot (U_d - U_s) - \frac{2}{3} \cdot \gamma \cdot (U_d^{3/2} - U_s^{3/2}) - \frac{1}{2} \cdot (U_d^2 - U_s^2)$
and: $Ug = vgb - Vfb$, $Us = vsb + PHI$, $Ud = vdb + PHI$
- In saturation, vdb should be replaced by $Vdsat - vbs$

6.2 Charge equations for Level 3

Applying to Eldo Levels 3 and 13.

- Accumulation: ($vgs \leq Vfb + vbs$)

$$Qg = CAPOX \cdot (vgs - vbs - Vfb)$$

$$Qb = -Qg; Qs = Qd = 0$$

- Subthreshold: ($vgs > Vfb + vbs$)

$$Qg = CAPOX \cdot \frac{\gamma^2}{2} \cdot \left(\sqrt{1 + \frac{4 \cdot (vgs - vbs - Vfb)}{\gamma^2}} - 1 \right)$$

$$Qb = -Qg; Qs = Qd = 0$$

- Strong inversion: ($vgs > Vth$)

$$Qg = CAPOX \cdot \left(vgs - Vfb - PHI - \frac{Vde}{2} + \frac{(1 + \lambda_b) \cdot Vde^2}{12 \cdot (vgs - Vth - (1 + \lambda_b) \cdot Vde/2)} \right)$$

$$\begin{aligned} Qb = CAPOX \cdot & \left(-Vth + Vfb + PHI - \frac{\lambda_b \cdot Vde}{2} + \right. \\ & \left. \frac{\lambda_b \cdot (1 + \lambda_b) \cdot Vde^2}{12 \cdot (vgs - Vth - (1 + \lambda_b) \cdot Vde/2)} \right) \end{aligned}$$

$$Qd = -Xqc \cdot (Qg + Qb); Qs = (Xqc - 1) \cdot (Qg + Qb)$$

Where:

- $Vde = \min(vds; Vdsat)$
- See the “MOSFET Level3 Equations” for λ_b calculation.
- Xqc is the partitioning factor that may vary from 0.5 when $vds = 0$ to XQC parameter value in saturation region.

7.0 Berkeley Spice Model Parameters

The parameter tables are presented in the following pages. The first table shows a list of the model parameters in Eldo mode. The second is for the Precise option.

7.1 Model parameters

Nr.	LEVEL 1 2 3	Name	Description	Default	Units
1	X X X	LEVEL	Model index	1	
Drain Current (Id) Related Model Parameters					
2	X X X	VTO	Zero-bias threshold voltage		V
3	X X X	KP^a	Transconductance parameter	2.0×10^{-5}	AV^{-2}
4	X X X	GAMMA^b	Bulk threshold parameter	0	$\text{V}^{1/2}$
5	X X X	PHI	Surface potential	0.6	V
6	X X	LAMBDA	Channel-length modulation	0	V^{-1}
7	X X X	UO^c	Surface mobility	600	$\text{cm}^2(\text{Vs})^{-1}$
8	X X	VMAX	Maximum drift velocity of carriers	0	ms^{-1}
9	X	THETA	Mobility modulation	0	V^{-1}
10	X	UCRIT	Critical field for mobility degradation	10^4	Vcm^{-1}
11	X	UEXP	Critical field exponent for mobility degradation	0	
12	X	NEFF	Total channel charge coefficient	1	
13	X	ETA	Static feedback	0	
14	X	KAPPA	Saturation field factor	0.2	V^{-1}
15	X X	DELTA	Width effect on threshold voltage	0	V^{-1}
MOS Process Related Model Parameters					
16	X X X	NSUB	Substrate doping	0	cm^{-3}
17	X X	NSS	Surface state density	0	cm^{-2}
18	X X	NFS	Fast surface state density	0	$\text{V}^{-1}\text{cm}^{-2}$
19	X X X	TPG	Type of gate material: TPG=0 —Aluminium gate TPG=1 —Same as Source-Drain diffusion TPG=-1 —Opposite to Source-Drain diffusion	1	
20	X X X	TOX^d	Oxide thickness	10^{-7}	m
21	X X	XJ	Metallurgical junction depth	0	m
Temperature Effect Related Model Parameters					
22	X X X	TCV	Threshold temperature coefficient	0	$\text{V}^\circ\text{C}^{-1}$

Nr.	LEVEL 1 2 3	Name	Description	Default	Units
23	X X X	BEX	Mobility temperature coefficient	-1.5	
Dynamic Model and Overlap Capacitance Related Model Parameters					
24	X X X	CGDO	Gate-drain overlap capacitance	0	Fm ⁻¹
25	X X X	CGSO	Gate-source overlap capacitance	0	Fm ⁻¹
26	X X X	CGBO	Gate-bulk overlap capacitance	0	Fm ⁻¹
27	X X	XQC	charge partition value and selector	1	
28	X X	CAPLEV	Capacitance model selector	0	
29	X X X	COX ^d	Oxide capacitance	3.45×10 ⁻⁴	Fm ⁻²

a. For modified Eldo Level=3 (Level=13): if **KP** is not specified, it is calculated from **UO** and **TOX** if they are specified.

b. If **GAMMA** is not specified, **NSUB** is used instead in the calculations.

c. For modified Eldo Level=3 (Level=13): if the **KP** parameter is specified, **UO** is calculated from **KP**.

d. The value of **COX** is calculated using the value of the **TOX** parameter.

X.Indicates that the parameter is used by the Levels (1, 2 or 3) marked with an X.

7.2 Model parameters with Precise option

Nr.	LEVEL 1 2 3	Name	Description	Default	Units
1	X X X	LEVEL	Model index	1	
Drain Current (Id) Related Model Parameters					
2	X X X	VTO	Zero-bias threshold voltage		V
3	X X X	KP	Transconductance parameter	6.8×10 ⁻⁶	AV ⁻²
4	X X X	GAMMA ^a	Bulk threshold parameter	0.528	V ^{1/2}
5	X X X	PHI	Surface potential	0.596	V
6	X X	LAMBDA	Channel-length modulation	0	V ⁻¹
7	X X X	UO	Surface mobility	200	cm ² (Vs) ⁻¹
8	X X	VMAX	Maximum drift velocity of carriers	0	ms ⁻¹
9	X	THETA	Mobility modulation	0	V ⁻¹
10	X	UCRIT	Critical field for mobility degradation	1.0×10 ⁴	Vcm ⁻¹
11	X	UEXP	Critical field exponent for mobility degradation	0	
12	X	NEFF	Total channel charge coefficient	1	
13	X	ETA	Static feedback	0	
14	X	KAPPA	Saturation field factor	0.2	V ⁻¹
15	X X	DELTA	Width effect on threshold voltage	0	V ⁻¹

Nr.	LEVEL 1 2 3	Name	Description	Default	Units
Mobility Related Model Parameters					
16	X	LMOB	Determines the mobility equation (1, 2, 3)	1	
17	X	LVSAT	Determines the saturation voltage equation (1, 2, 3)	1	
18	X	LCLM	Determines the channel length modulation equation (1, 2, 3)	1	
19	X	K1	Channel length modulation factor	0	
Temperature Effect Related Model Parameters					
20	X X X	TCV	Threshold temperature coefficient	0	V°C ⁻¹
21	X X X	BEX	Mobility temperature coefficient	-1.5	
MOS Process Related Model Parameters					
22	X X X	DELL	Length increment	0	m
23	X X X	DELW	Width increment	0	m
24	X X X	NSUB	Substrate doping	1.0×10 ¹⁵	cm ⁻³
25	X X X	NSS	Surface state density	0	cm ⁻²
26	X X	NFS	Fast surface state density	0	cm ⁻²
27	X X X	TPG	Type of gate material: TPG=0—Aluminium gate TPG=1—Same as Source-Drain diffusion TPG=-1—Opposite to Source-Drain diffusion	1	
28	X X X	TOX ^b	Oxide thickness	1.0×10 ⁻⁷	m
29	X X X	XJ	Metallurgical junction depth	0	m
Dynamic Model and Overlap Capacitance Related Model Parameters					
30	X X X	CGDO	Gate-drain overlap capacitance	0	Fm ⁻¹
31	X X X	CGSO	Gate-source overlap capacitance	0	Fm ⁻¹
32	X X X	CGBO	Gate-bulk overlap capacitance	0	Fm ⁻¹
33	X X	XQC	charge partition value and selector	1	
34	X X X	COX ^a	Oxide capacitance	3.45×10 ⁻⁴	Fm ⁻²
35	X X X	LCAP	Determines the capacitance equations (1,2,3) 1—Modified Meyer's capacitance model 2—SPICE Meyer's capacitance model 3—Change model control except Level 1	1	
36	X X X	METO	Metal overlap	0	m
Parasitic Resistance Related Model Parameters					
37	X X X	LDIF	Lateral diffusion beyond the gate	0	m

a. If **GAMMA** is not specified, **NSUB** is used instead in the calculations.

b. The value of **COX** is calculated using the value of the **TOX** parameter.

X.Indicates that the parameter is used by the Levels (1, 2 or 3) marked with an X.

Chapter 12

MOS Level 4, 5, 6 Equations

1.0 Introduction

Three Merckel model levels are presently available as Levels 4, 5 and 6. These models are defined by their own set of parameters, which can be easily extracted from measurements.

The Level 4 model is a charge control model and the DC characteristics are the same as in Level 6.

The Level 5 model is very similar to that of SPICE Level 1, but it also takes into account the effect of mobility modulation through **TG**. The early effect is modeled by **KE** instead of **LAMBDA** as in SPICE models.

The Level 6 model is more accurate, and it is especially dedicated to submicron technologies; the threshold dependencies on geometries are modeled by **VE** instead of **LAMBDA** as in SPICE models.

The capacitance models are close to those of SPICE. The bulk junction capacitances vary with the power of $-1/2$ of the junction voltage. Overlap capacitances are computed from the **REC** parameter. **LDIF** is used for computation of the drain and source perimeters and areas, if the parameters for **AD**, **AS**, **PD** and **PS** are missing in the declaration of the MOS transistor.

2.0 Equations Common to Levels 4, 5 and 6

2.1 Effective length and width calculations

$$W_{eff} = W(1 - SH) - DW \quad L_{eff} = L(1 - SH) - DL$$

$$LDIF_{eff} = LDIF(1 - SH) - \frac{DW}{2}$$

2.2 Initialization

If Kp is positive $KO1 = KP/2$,

else if $KO > 1$, $KO1 = KO$, else $KO1 = \frac{MUO \cdot Cox}{2}$ where $Cox = \frac{\varepsilon_0 \cdot \varepsilon_{si}}{EOX}$

If $VL = 0$, then $Td = 0$, else $Td = \frac{MUO}{L_{eff} \cdot VL}$

2.3 Temperature dependence (Common to levels 4, 5 and 6)

NMOS

$$MU0(T) = MU0 \cdot \left(\frac{T}{T0}\right)^{-1.9} \quad KO1(T) = KO1 \cdot \left(\frac{T}{T0}\right)^{-1.9}$$

$$VT0(T) = VT0 - \left(\frac{T - T0}{1500}\right)$$

PMOS

$$MU0(T) = MU0 \cdot \left(\frac{T}{T_0}\right)^{-1.7} \quad KO1(T) = KO1 \cdot \left(\frac{T}{T_0}\right)^{-1.7}$$

$$VT0(T) = VT0 - \left(\frac{T-T_0}{1000}\right) \quad TG(T) = TG \cdot \left(\frac{T}{T_0}\right)^{-1}$$

3.0 Level 4

3.1 Threshold voltage

The threshold voltage V_{th} , is calculated as:

$$V_{th} = VTO + Kb1 \cdot (\sqrt{DPHIF - vbs} - \sqrt{DPHIF})$$

$$\text{where: } Kb1 = KB \cdot \left(1 + \frac{GW}{Weff} - \frac{GL}{Leff}\right)$$

$$\text{If } NFS > 0 \text{ then, } Von = V_{th} + V_t \cdot \left(\frac{Kb1}{2 \cdot \sqrt{DPHIF - vbs}} - \frac{NFS}{Cox} + 1\right)$$

else $Von = V_{th}$

If $vgs > von$, then $Vgth = vgs - V_{th}$,

else $Vgth = von - V_{th}$

The effective early voltage, Vea , is calculated as: $Vea = VE \cdot (L_{eff} \cdot Vgth)^{\frac{2}{3}}$

3.2 Saturation voltage

The saturation voltage, V_{dss} , is calculated as: $V_{dss} = \frac{V_{gth1}}{1 + \sqrt{1 + \frac{V_{gth1}}{V_{ed}}}}$

where: $V_{gth1} = \frac{2 \cdot V_{gth}}{1 + D_0}$ and $D_0 = \frac{DINF}{\sqrt{1 - \frac{vbs}{DPHIF}}} \cdot \left(1 + \frac{KW}{Weff} - \frac{KL}{Leff}\right)$

For an NMOS device, $V_{ed} = \frac{Vea}{1 + Td^2 \cdot (Vea + V_{gth1}) \cdot V_{gth1} \cdot 0.5}$

For a PMOS device, $V_{ed} = \frac{Vea}{1 + Td \cdot (Vea + V_{gth1})}$

3.3 Ids current calculation

In the linear region ($vds < V_{dss}$):

$$IdsO = KO1 \cdot \frac{Weff}{Leff} \cdot vds \cdot \left(\frac{2 \cdot V_{gth} - vds \cdot (1 + D_0)}{1 + TG \cdot \left(V_{gth} - \frac{(1 - D_0) \cdot vds}{2} \right)} \right)$$

In the saturation region, ($vds \geq V_{dss}$):

$$IdssO = KO1 \cdot \frac{Weff}{Leff} \cdot V_{dss} \cdot \left(\frac{2 \cdot V_{gth} - V_{dss} \cdot (1 + D_0)}{1 + TG \cdot \left(V_{gth} - \frac{(1 - D_0) \cdot V_{dss}}{2} \right)} \right)$$

$$IdsO = IdssO \cdot \frac{vds + Vea}{V_{dss} + Vea}$$

The final current, Ids , is calculated for an NMOS device as:

$$I_{ds} = \frac{I_{dsO}}{\sqrt{1 + (T_d \cdot \min(v_{ds}, V_{dss}))^2}}$$

and for a PMOS device as: $I_{ds} = \frac{I_{dsO}}{1 + T_d \cdot \min(v_{ds}, V_{dss})}$

3.4 Subthreshold current

If $NFS > 0$, and $v_{gs} < V_{on}$, then: $I_{ds} = I_{ds} \cdot \exp\left(\frac{v_{gs} - V_{on}}{V_{on} - V_{th}}\right)$

4.0 Level 5

4.1 Threshold voltage

$$V_{th} = V_{TO} + KB \cdot (\sqrt{DPHIF} - v_{bs} - \sqrt{DPHIF})$$

$$V_{gth} = v_{gs} - V_{th} \quad V_{ght0} = v_{gs} - VT_0$$

4.2 Early voltage

If $KE > 0$ then $V_{ea} = KE \cdot L_{eff}$

else if $NB > 0$ then $V_{ea} = 1.5810 \cdot 10^{-7} \cdot L_{eff} \cdot \sqrt{NB}$

else $V_{ea} = 10^4$

4.3 Saturation voltage

The saturation voltage, V_{dss} , is calculated as: $V_{dss} = V_{ed} \cdot \left(\sqrt{1 + \frac{V_{gth1}}{V_{ed}}} - 1 \right)$

where: $V_{gth1} = \frac{2 \cdot V_{gth}}{1 + D_0}$ and $D_0 = \frac{KB}{2.5 \cdot \sqrt{DPHIF} - v_{bs}}$

$$\text{For an NMOS device, } V_{ed} = \frac{V_{ea}}{1 + 1.25 \cdot Td^2 \cdot V_{ea}}$$

$$\text{For an PMOS device, } V_{ed} = \frac{V_{ea}}{1 + Td \cdot V_{ea}}$$

4.4 Ids current calculations

In the linear region ($vds < Vdss$):

$$I_{dsO} = KO1 \cdot \frac{Weff}{Leff} \cdot vds \cdot \left(\frac{2 \cdot Vgth - vds \cdot (1 + D_0)}{1 + TG \cdot Vgth0} \right)$$

In the saturation region, ($vds \geq Vdss$):

$$I_{dssO} = KO1 \cdot \frac{Weff}{Leff} \cdot Vdss \cdot \left(\frac{2 \cdot Vgth - Vdss \cdot (1 + D_0)}{1 + TG \cdot Vgth0} \right)$$

$$I_{dsO} = I_{dssO} \cdot \frac{vds + V_{ea}}{Vdss + V_{ea}}$$

The final current, Ids , is calculated for an NMOS device as:

$$Ids = \frac{I_{dsO}}{\sqrt{1 + 1.25 \cdot Td^2 \cdot \min(vds, Vdss)}}$$

$$\text{and for a PMOS device as: } Ids = \frac{I_{dsO}}{1 + Td \cdot \min(vds, Vdss)}$$

5.0 Level 6

5.1 Threshold voltage

The threshold voltage Vth , is calculated as:

$$Vth = VTO + Kb1 \cdot (\sqrt{DPHIF - vbs} - \sqrt{DPHIF})$$

$$\text{where: } Kb1 = KB \cdot \left(1 + \frac{GW}{Weff} - \frac{GL}{Leff} \right)$$

$$\text{If } NFS > 0 \text{ then, } Von = Vth + Vt \cdot \left(\frac{Kb1}{2 \cdot \sqrt{DPHIF - vbs}} + \frac{NFS}{Cox} + 1 \right)$$

else $Von = Vth$

If $vgs > von$, then $Vgth = vgs - Vth$,

else $Vgth = von - Vth$

The effective early voltage, Vea , is calculated as: $Vea = VE \cdot (Leff \cdot Vgth)^{\frac{2}{3}}$

5.2 Saturation voltage

The saturation voltage, $Vdss$, is calculated as: $Vdss = \frac{Vgth1}{1 + \sqrt[3]{1 + \frac{Vgth1}{Ved}}}$

where: $Vgth1 = \frac{2 \cdot Vgth}{1 + D_0}$ and $D_0 = \frac{DINF}{\sqrt{1 - \frac{vbs}{DPHIF}}} \cdot \left(1 + \frac{KW}{Weff} - \frac{KL}{Leff} \right)$

For an NMOS device, $Ved = \frac{Vea}{1 + Td^2 \cdot (Vea + Vgth1) \cdot Vgth1 \cdot 0.5}$

For an PMOS device, $Ved = \frac{Vea}{1 + Td \cdot (Vea + Vgth1)}$

5.3 Ids current calculations

In the linear region ($vds < Vdss$):

$$Id_{SO} = KO_1 \cdot \frac{Weff}{Leff} \cdot vds \cdot \left(\frac{2 \cdot Vgth - vds \cdot (1 + D_0)}{1 + TG \cdot \left(Vgth - \frac{(1 - D_0) \cdot vds}{2} \right)} \right)$$

In the saturation region, ($vds \geq Vdss$):

$$Id_{SSO} = KO_1 \cdot \frac{Weff}{Leff} \cdot Vdss \cdot \left(\frac{2 \cdot Vgth - Vdss \cdot (1 + D_0)}{1 + TG \cdot \left(Vgth - \frac{(1 - D_0) \cdot Vdss}{2} \right)} \right)$$

$$Id_{SO} = Id_{SSO} \cdot \frac{vds + Vea}{Vdss + Vea}$$

The final current, Ids , is calculated for an NMOS device as:

$$Ids = \frac{Id_{SO}}{\sqrt{1 + (Td \cdot \min(vds, Vdss))^2}}$$

and for a PMOS device as: $Ids = \frac{Id_{SO}}{1 + Td \cdot \min(vds, Vdss)}$

5.4 Subthreshold current

If $NFS > 0$, and $vgs < Von$, then: $Ids = Id_{SO} \cdot \exp\left(\frac{vgs - Von}{Von - Vth}\right)$

6.0 Model Parameters

Nr.	LEVEL 4 5 6	Name	Description	Default	Units
1	X X X	NIV	Model index		
Drain Current (Id) Related Model Parameters					
2	X X X	VT0	Zero-bias threshold voltage	0.5	V
3	X X X	KO	$MU_0 \times COX / 2$	0	AV^{-2}
4	X X X	KB	Bulk threshold parameter	0.1	$V^{-1/2}$
5	X X X	DPHIF	Surface potential	0.6	V
6	X X X	MU0	Low field surface mobility	800	$cm^2(Vs)^{-1}$
7	X X X	VL	Maximum drift velocity	2×10^5	ms^{-1}
8	X X X	TG	Gate field effect coefficient on mobility	0.1	V^{-1}
9	X X	KW	Small-scale correction (Current)	0	
10	X X	KL	Small-scale correction (Current)	0	
11	X X	GW	Small-scale correction (VT_0)	0	
12	X X	GL	Small-scale correction (VT_0)	0	
13	X X	DINF	Small-scale correction (VT_0)	0.1	
14	X X	KE	Early voltage coefficient	0	m^{-1}
15	X X	VE	Early voltage coefficient	10	$m^{-2/3}V^{1/3}$
16	X X X	SH	Shrink coefficient	0	
MOS Process Related Model Parameters					
17	X X X	NB	Substrate doping	2×10^{16}	cm^{-3}
18	X X X	NFS	Channel surface doping	0	$V^{-1}cm^{-2}$
19	X X X	EOX	Oxide thickness	10^{-7}	m
20	X X X	DW	Transverse overlap	0	m
21	X X X	DL	Longitudinal overlap	0	m
Overlap Capacitance and Dynamic Model Related Model Parameters					
22	X X X	REC	Gate/drain or gate/source overlap	0	m
23	X X X	CDIFS0	Bulk junction capacitance	10^{-4}	Fm^{-2}
24	X X X	CDIFP0	Bulk junction capacitance	5×10^{-11}	Fm^{-1}
Parasitic Resistance Related Model Parameters					
25	X X X	RS	Source ohmic resistance	0	Ω
26	X X X	RD	Drain ohmic resistance	0	Ω
27	X X X	LDIF	Diffusion length	0	m

Nr.	LEVEL 4 5 6	Name	Description	Default	Units
Temperature Effect Related Model Parameters					
28	X X X	TNOM	Nominal temperature	27	°C
29	X X X	TMOD	Model temperature	TNOM	°C
Noise Effect Related Model Parameters					
30	X X X	AF	Flicker noise exponent	1	
31	X X X	KF	Flicker noise coefficient	0	
32	X X X	FLKLEV	Flicker noise level selector	0	
33	X X X	THMLEV	Thermal noise level selector	0	
Geometric Range Related Model Parameters					
34	X X X	WMIN	Model geometric range parameters. These model parameters give the range of the physical length and width dimensions to which the MOSFET model applies; used in conjunction with the .option modwl command	1	µm
35	X X X	WMAX		2000	µm
36	X X X	LMIN		1	µm
37	X X X	LMAX		100	µm

X.Denotes the parameter is used by the specified Levels (4, 5 or 6) marked with an X.

Chapter 13

BSIM1 Equations

1.0 Introduction

The Berkeley Short Channel IGFET Model (BSIM1) is a semi-empirical model proposed by the University of Berkeley (California). It was adopted to cope with rapid advances of technologies and fits well for submicron technologies. The major effects modeled in BSIM1 include:

- Vertical dependence of carrier mobility
- Carrier velocity saturation
- Drain induced barrier lowering
- Depletion charge sharing by the source and the drain
- Non-uniform doping profile for ion-implanted devices
- Channel length modulation
- Subthreshold conduction
- Geometrical dependence

2.0 Useful Internal Parameters

2.1 Effective channel length and width

The effective channel length and width are determined as follows:

If DL is given: $L_{eff} = L \cdot LMLT - DL_{scal}$

otherwise: $L_{eff} = L \cdot LMLT + XL_{scal} - 2 \cdot LD_{scal}$

If DW is given: $W_{eff} = W \cdot WMLT - DW_{scal}$

otherwise: $W_{eff} = W \cdot WMLT + XW_{scal} - 2 \cdot WD_{scal}$

In Precise compatibility mode, the equations are:

$$L_{eff} = L \cdot LMLT + DELL_{scal} - 2 \cdot LD_{scal} - DL_{scal}$$

$$W_{eff} = W \cdot WMLT + DELW_{scal} - 2 \cdot WD_{scal} - DW_{scal}$$

2.2 Geometrically related parameters

The following equation is applied to the parameter list given below.

$$\begin{aligned} param_g &= param + Lparam \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}} \right) + \\ &Wparam \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}} \right) \end{aligned}$$

VFB, PHI, K1, K2, ETA, X2E, X3E, X2MZ, U0, X2U0, U1, X2U1, X3U1, MUS, X2MS, X3MS, N0, NB, ND

$$\beta0_0 = \frac{MUZ \cdot Cox \cdot W_{eff}}{L_{eff}} \quad \beta0_B = \frac{X2MZ_g \cdot Cox \cdot W_{eff}}{L_{eff}}$$

$$\beta S_0 = \frac{MUS_g \cdot Cox \cdot W_{eff}}{L_{eff}} \quad \beta S_B = \frac{X2MS_g \cdot Cox \cdot W_{eff}}{L_{eff}}$$

$$\beta S_D = \frac{X3MS_g \cdot Cox \cdot W_{eff}}{L_{eff}}$$

2.3 Voltage dependent parameters ($param_v$)

- Gate field mobility reduction

$$U0_{gv} = U0_g + X2V0_g \cdot vbs$$

- Drain field mobility reduction

$$U1_{gv} = U1_g + X2U1_g \cdot vbs + X3U1_g \cdot (vds - VDD)$$

- Linear vds threshold coefficient

If **UPDATE** = 1,

$$ETA_{gv} = ETA_g + X2E_g \cdot (vbs - PHI_g) + X3E_g \cdot (vds - VDD)$$

$$\text{else: } ETA_{gv} = ETA_g + X2E_g \cdot vbs + X3E_g \cdot (vds - VDD)$$

- Subthreshold slope coefficient

$$N_{gv} = N0_g + NB_g \cdot vbs + ND_g \cdot vds$$

3.0 Static Current Equations

3.1 Threshold voltage

The threshold voltage Vth is calculated as follows:

$$Vth = VFB_g + PHI_g + K1_g \cdot \sqrt{PHI_g - vbs} - K2_g \cdot (PHI_g - vbs) - ETA_{gv} \cdot vds$$

3.2 Drain saturation voltage

The drain saturation voltage $Vdsat$ is calculated as follows: $Vdsat = \frac{vgs - Vth}{A_v \cdot \sqrt{K_p}}$

$$\text{where: } K_p = \frac{1 + V_c + \sqrt{1 + 2 \cdot V_c}}{2}, A_v = 1 + \frac{Gg_{gv} \cdot K1_g}{2 \cdot \sqrt{PHI_g - vbs}},$$

$$Vc = \frac{U1_{gv} \cdot (vgs - Vth)}{A_v} \text{ and } Gg_{gv} = 1 - \frac{1}{1.744 + 0.8364 \cdot (PHI_g - vbs)}$$

3.3 Drain Current in the Linear region

In the linear region the Drain current Ids is given by the following equation:

$$Ids = \frac{\beta eta}{1 + U0_{gv} \cdot (vgs - Vth)} \cdot \frac{vds}{1 + U1_{gv} \cdot vds} \cdot \left((vgs - Vth) - \frac{A_v}{2} \cdot vds \right)$$

where:

$$\beta eta = \beta vds_0 \cdot \left(\frac{vds}{VDD} - 1 \right)^2 + \beta vdd \cdot \left(2 - \frac{vds}{VDD} \right) \cdot \frac{vds}{VDD} + \beta S_D \cdot vds \cdot \left(\frac{vds}{VDD} - 1 \right)$$

with:

- o the value of βeta at $vds = 0$ is given by $\beta vds_0 = \beta 0_0 + \beta 0_B \cdot vbs$
- o the value of βeta at $vds = VDD$ is given by $\beta vdd = \beta S_0 + \beta S_B \cdot vbs$

3.4 Drain Current in the Saturation region

The saturation Drain current is described as follows:

$$Ids = \frac{\beta eta}{1 + U0_{gv} \cdot (vgs - Vth)} \cdot \frac{(vgs - Vth)^2}{2 \cdot A_v \cdot K_p}$$

3.5 Subthreshold current

The subthreshold current I_{sub} is calculated when the subthreshold slope coefficient $N0$ is less than 200. The current I_{sub} is also added to Ids in the strong inversion.

$$I_{sub} = \frac{Il_{im} \cdot I_{exp}}{Il_{im} + I_{exp}}$$

where the upper Il_{im} to the subthreshold current is calculated as follows:

$$Il_{im} = \beta_0 \cdot \frac{(3 \cdot Vt)^2}{2}$$

$$I_{exp} = \beta_0 \cdot Vt^2 \cdot \exp(1.8) \cdot Wgs \cdot Wds$$

where Wgs and Wds are given by the following:

.OPTION BSIM1Cont=1 (default)

$$Wds = 1 - e^{\frac{-Vds}{Vt}}$$

$$Wgs = e^{\frac{(Vgs - Vth)}{Ngv \cdot Vt}}$$

.OPTION BSIM1Cont=2

$$Wds = 1 - e^{\frac{-Vds}{Vt}}$$

$$Wgs = e^{\frac{(Vgs - Vth)}{Ngv \cdot Vt}}$$



Here $\frac{(Vgs - Vth)}{Ngv \cdot Vt}$ is limited to a maximum of 20.

.OPTION BSIM1Cont=3

$$W_{ds} = 1 - e^{\frac{-V_{ds}}{57V_t}}$$

$$W_{gs} = e^{\frac{(V_{gs} - V_{th})}{N_{gv} \cdot V_t}}$$



Here $\frac{(V_{gs} - V_{th})}{N_{gv} \cdot V_t}$ is limited to a minimum of -18 and a maximum of 35.

.OPTION BSIM1Cont=4

$$W_{ds} = \frac{V_{ds}/V_t}{2 + V_{ds}/V_t}$$

$$W_{gs} = e^{\frac{(V_{gs} - V_{th})}{N_{gv} \cdot V_t}}$$



Here $\frac{(V_{gs} - V_{th})}{N_{gv} \cdot V_t}$ is limited to a maximum of 1.

4.0 Charge Equations

4.1 Definitions

A special charge Threshold voltage, V_{th0} , is defined as:

$$V_{th0} = VFB_g + PHI_g + K1_g \cdot \sqrt{PHI_g - vbs}$$

A specific charge Saturation voltage, V_{dsat0} , is defined as:

$$V_{dsat0} = \frac{vgs - V_{th0}}{A_v}$$

The value of C_{ox} is calculated from the value of TOX as follows: $C_{ox} = \frac{e_{ox}}{TOX}$

where e_{ox} is the Permittivity of SiO_2 and is calculated as follows:

$$e_{ox} = 3.9 \times \epsilon_0 \text{ Fm}^{-1}; \text{ where: } \epsilon_0 = \text{Permittivity in a Vacuum} = 8.854214871 \times 10^{-12}$$

The effective capacitance of the device is defined as:

$$CAPOX = C_{ox} \cdot W_{eff} \cdot L_{eff}$$

Some intermediate variables are defined as:

$$\begin{aligned} Arg1 &= \frac{1}{2} - \frac{A_v \cdot vds}{12 \cdot (vgs - V_{th0} - 0.5 \cdot vds)} \\ Arg2 &= \frac{(vgs - V_{th0})^2 - 0.75 \cdot (vgs \cdot V_{th0}) + 0.15 \cdot (A_v - vds)^2}{6 \cdot (vgs - V_{th0} - 0.5 \cdot A_v \cdot vds)^2} \end{aligned}$$

4.2 Charge calculations

In the accumulation region ($vgs \leq VFB_g + vbs$)

$$Q_g = CAPOX \cdot (vgs - vbs - VFB_g) \quad Q_b = -Q_g \quad Q_d = Q_s = 0$$

In the subthreshold region ($vbs + VFB_g < vgs \leq V_{th0}$)

$$Q_g = CAPOX \cdot \frac{K1_g^2}{2} \cdot \left(\sqrt{1 + \frac{4 \cdot (vgs - vbs - VFB_g)}{K1_g^2}} - 1 \right)$$

$$Q_b = -Q_g \quad Q_d = Q_s = 0$$

In the triode region ($vgs > V_{th0}$) and ($vds \leq V_{dsat0}$)

$$Q_g = CAPOX \cdot (vgs - VFB_g - PHI_g - vds \cdot Arg1)$$

$$Q_b = CAPOX \cdot (-V_{th0} + VFB_g + PHI_g + vds \cdot (1 - A_v) \cdot Arg1)$$

- When $XPART = 1$, a 0/100 charge partition model is used:

$$Qd = -CAPOX \cdot \left(\frac{vgs - Vth0}{2} - A_v \cdot vds \cdot (0.75 - 1.5 \cdot Arg1) \right)$$

$$Qs = -(Qg + Qd + Qb)$$

- When $XPART = 0.5$, a 50/50 charge partition model is used:

$$Qd = \frac{1}{2} \cdot (Qg + Qb) \quad Qs = Qd$$

- When $XPART = 0.4$, a 40/60 charge partition model is used:

$$Qd = -CAPOX \cdot \left(\frac{vgs - Vth0 - A_v \cdot vds}{2} + A_v \cdot vds \cdot Arg2 \right)$$

$$Qs = -(Qg - Qd - Qb)$$

In the saturation region ($vgs > Vth0$) and ($vds > Vdsat0$)

$$Qg = CAPOX \cdot \left(vgs - VFB_g - PHI_g - \frac{vgs - Vth0}{3 \cdot A_v} \right)$$

$$Qb = CAPOX \cdot \left(VFB_g + PHI_g - Vth0 + (1 - A_v) \cdot \frac{vgs - Vth0}{3 \cdot A_v} \right)$$

The Drain charge Qd and Source charge Qs expressions depend on the $XPART$ parameter value as follows:

- When $XPART = 1$, a 0/100 charge partition model is used:

$$Qd = 0 \quad Qs = -(Qg + Qb)$$

- When $XPART = 0.5$, a 50/50 charge partition model is used:

$$Qd = \frac{-CAPOX}{3} \cdot (vgs - Vth0) \quad Qs = Qd$$

- When $XPART = 0.4$, a 40/60 charge partition model is used:

$$Qd = \frac{-4 \cdot CAPOX}{15} \cdot (vgs - Vth0) \quad Qs = \frac{3}{2} \cdot Qd$$

5.0 Temperature Effects

Specific model temperature effects are as follows:

$$\begin{aligned} MUZ(T) &= MUZ \cdot \left(\frac{T}{T_{nom}} \right)^{BEX} & MUS_g(T) &= MUS_g \cdot \left(\frac{T}{T_{nom}} \right)^{BEX} \\ X3MS_g(T) &= X3MS_g \cdot \left(\frac{T}{T_{nom}} \right)^{BEX} & U1gv(T) &= U1gv \cdot \left(\frac{T}{T_{nom}} \right)^{FEX} \\ Vth(T) &= Vth - TCV \cdot (T - T_{nom}) \end{aligned}$$

Additional effects when **UPDATE = 2**

$$X2MS_g(T) = X2MS_g \cdot \left(\frac{T}{T_{nom}} \right)^{BEX} \quad X3MZ_g(T) = X3MZ_g \cdot \left(\frac{T}{T_{nom}} \right)^{BEX}$$

6.0 Model Parameters

The complete list of model parameters is shown in the table on the following pages. Parameters marked with a * after the parameter name also have corresponding parameters with a width and length dependency. For example, **VFB** is the basic parameter (with unit V), then **LVFB** and **WVFB** also exist and have units of $V \times \mu m$. The parameter names marked with letters (a, b, c, ...) have a different value in the case of simulation with **.OPTION PRECISE** and the corresponding values are given in the table footnote.

Nr.	Name	Description	Default	Units
Threshold Voltage Related Model Parameters				
1	VFB^{a*}	Flat band voltage	0	V
2	PHI^{b*}	Surface potential	0	V
3	K1*	Body effect coefficient	0	$V^{1/2}$

Nr.	Name	Description	Default	Units
4	K2^c*	Drain-source depletion charge sharing coefficient	0	
5	ETA*	Zero bias drain induced barrier lowering coefficient	0	
6	X2E*	Sensitivity of drain induced barrier lowering effect to substrate bias	0	V ⁻¹
7	X3E*	Sensitivity of drain induced barrier lowering effect to drain bias at Vds=Vdd	0	V ⁻¹
Mobility Related Model Parameters				
8	MUZ^d	Zero bias mobility	0	cm ² (Vs) ⁻¹
9	X2MZ*	Sensitivity of mobility to substrate bias at Vds=0	0	cm ² V ⁻² s ⁻¹
10	MUS^e*	Mobility at zero substrate bias at Vds=Vdd	0	cm ² (Vs) ⁻¹
11	X2MS*	Sensitivity of mobility to substrate bias at Vds=Vdd	0	cm ² V ⁻² s ⁻¹
12	X3MS*	Sensitivity of mobility to drain bias at Vds=Vdd	0	cm ² V ⁻² s ⁻¹
Mobility Modulation Related Model Parameters				
13	U0*	Zero bias transverse field mobility degradation coefficient	0	V ⁻¹
14	X2U0*	Sensitivity of transverse field mobility degradation effect to substrate bias	0	V ⁻²
Velocity Saturation Related Model Parameters				
15	U1^f*	Zero bias velocity saturation coefficient	0	μmV ⁻¹
16	X2U1*	Sensitivity of velocity saturation effect to substrate bias	0	μmV ⁻²
17	X3U1*	Sensitivity of velocity sat. effect on drain bias at Vds=Vdd	0	μmV ⁻²
Subthreshold Related Parameters				
18	N0*	Zero bias subthreshold slope coefficient	200	
19	NB*	Sensitivity of subthreshold slope to substrate bias	0	
20	ND*	Sensitivity of subthreshold slope to drain bias	0	
Impact Ionization Related Model Parameters				
21	ALPHA*	Impact ionization current coefficient	0	V ⁻¹
22	VCR*	Critical Voltage	0	V
Geometry, and Length & Width Modulation Related Model Parameters				
23	LREF	Channel length reference		m
24	WREF	Channel width reference		m
25	XW	Accounts for masking and etching effects. Not used with PRECISE option	0	m
26	XL	Accounts for masking and etching effects. Not used with PRECISE option	0	m
27	WDEF	Source-drain junction default width	0	m
Temperature Effect Related Model Parameters				
28	BEX	Low field mobility	-1.5	

Nr.	Name	Description	Default	Units
29	FEX	Temperature exponent for MUZ and MUS mobility parameters	0	
30	TCV	Flat-band voltage temperature coefficient	0	V°K ⁻¹
31	PTC	Temperature coefficient of Fermi potential PHI (TLEV C=1, 2 only)	0	V°K ⁻¹
Overlap Capacitance Related, and Dynamic Model Parameters				
32	CGDO ^g	Gate-drain overlap capacitance per meter channel width	0	Fm ⁻¹
33	CGSO ^h	Gate-source overlap capacitance per meter channel width	0	Fm ⁻¹
34	CGBO ⁱ	Gate-bulk overlap capacitance per meter channel length	0	Fm ⁻¹
35	XPART ^j	Gate oxide capacitance charge model flag	0	
Process and Parameter Extraction Related Model Parameters				
36	TOX ^k	Gate oxide thickness	3.0×10 ⁻²	μm
37	VDD ^l	Measurement bias voltage	5	V
PRECISE Model Parameters (Used ONLY in PRECISE Mode)				
38	DELL	Source-drain junction length reduction	0	m
39	DELW	Width increment	0	m
40	METO	Metal overlap	0	m

- a. Default value is -1 with PRECISE option.
- b. Default value is 0.576 with PRECISE option.
- c. Default value is 1 with PRECISE option.
- d. Default value is 600 with PRECISE option.
- e. Default value is 600 with PRECISE option.
- f. Default value is -0.6 with PRECISE option.
- g. Default value is calculated with PRECISE option.
- h. Default value is calculated with PRECISE option.
- i. Default value is calculated with PRECISE option.
- j. A value of **XPART**=0 selects a 40/60 drain/source charge partition in saturation.
A value of **XPART**=0.5 selects a 50/50 drain/source charge partition.
A value of **XPART**=1 selects a 0/100 drain/source charge partition.
- k. The unit is meters and the default value is 0.1 μm with PRECISE option.
- l. Default value is 5 with PRECISE option.

Specific BSIM1 initialization for parasitic common approach MOS parameters:

```
ALEV=0; RLEV=0; DIOLEV=3; DCAPLEV=0
if XJ is specified then LD=0.75×XJ otherwise LD=0;
in PRECISE mode, CJ=0 otherwise CJ=4.5×10-5;
FC is not a BSIM1 parameter, therefore it is set to 0.
```

Chapter 14

BSIM2 Equations

1.0 Introduction

Based on the BSIM1 model, BSIM2 was developed by the University of Berkeley (California) to correct BSIM1 problems. BSIM2 has been successfully used to model the drain current and output resistance of MOSFET's with gate oxide as thin as 3.6 nm and channel length as small as 0.2 μm .

Based on recent physical understanding of deep-submicron MOSFET's, it was found that the important effects to be included in MOSFET modeling are:

- Vertical dependence of carrier mobility
- Carrier velocity saturation
- Drain induced barrier lowering
- Depletion charge sharing by the source and the drain
- Non-uniform doping profile for ion-implanted devices
- Channel length modulation
- Subthreshold conduction
- Geometric dependence
- Source/Drain parasitic resistance
- Hot electron induced output resistance reduction
- Inversion layer capacitance.

Except for the three last effects, most of these were already present in the BSIM1 model. In order to develop a consistent model, these effects were re-examined using new deep-submicron MOSFET considerations and their implementation. The charge model was derived from its drain-current counterpart to ensure model consistency of device physics. Charge conservation is also guaranteed.

2.0 Useful Internal Parameters

2.1 Effective channel length and width

The effective channel length and width are determined as follows:

If DL is given: $L_{eff} = L \cdot LMLT - DL_{scal}$

otherwise: $L_{eff} = L \cdot LMLT + XL_{scal} - 2 \cdot LD_{scal}$

If DW is given: $W_{eff} = W \cdot WMLT - DW_{scal}$

otherwise: $W_{eff} = W \cdot WMLT + XW_{scal} - 2 \cdot WD_{scal}$

For Precise compatibility the equations are:

$$L_{eff} = L \cdot LMLT + DELL_{scal} - 2 \cdot LD_{scal} - DL_{scal}$$

$$W_{eff} = W \cdot WMLT + DELW_{scal} - 2 \cdot WD_{scal} - DW_{scal}$$

2.2 Geometrically related parameters

The following equation is applied to the parameter list given below:

$$param_g = param + \frac{Lparam}{L_{eff}} + \frac{Wparam}{W_{eff}}$$

VFB, PHI, K1, K2, ETA, ETAB, MU0B, MUS0, MUSB, MU20, MU2B, MU2G, MU30, MU3B, MU3G, MU40, MU4B, MU4G, UA0, UAB, UB0, UBB, U10, U1B, U1D, N0, NB, ND, VOF0, VOFB, VOFD, AI0, AIB, BI0, BIB, VGHIGH, VGLOW

Some β definitions are also useful and are defined as follows:

$$\beta 0_0 = \frac{MU0 \cdot Cox \cdot W_{eff}}{L_{eff}} \quad \beta 0_B = \frac{MU0B_g \cdot Cox \cdot W_{eff}}{L_{eff}}$$

$$\beta S_0 = \frac{MUS0_g \cdot Cox \cdot W_{eff}}{L_{eff}} \quad \beta S_B = \frac{MUSB_g \cdot Cox \cdot W_{eff}}{L_{eff}}$$

$$\beta 2_0 = \frac{MU20_g \cdot Cox \cdot W_{eff}}{L_{eff}} \quad \beta 2_B = \frac{MU2B_g \cdot Cox \cdot W_{eff}}{L_{eff}}$$

$$\beta 2_G = \frac{MU2G_g \cdot Cox \cdot W_{eff}}{L_{eff}}$$

$$\beta 3_0 = \frac{MU30_g \cdot Cox \cdot W_{eff}}{L_{eff}} \quad \beta 3_B = \frac{MU3B_g \cdot Cox \cdot W_{eff}}{L_{eff}}$$

$$\beta 3_G = \frac{MU3G_g \cdot Cox \cdot W_{eff}}{L_{eff}}$$

$$\beta 4_0 = \frac{MU40_g \cdot Cox \cdot W_{eff}}{L_{eff}} \quad \beta 4_B = \frac{MU4B_g \cdot Cox \cdot W_{eff}}{L_{eff}}$$

$$\beta 4_G = \frac{MU4G_g \cdot Cox \cdot W_{eff}}{L_{eff}}$$

2.3 Voltage dependent parameters ($param_v$)

- First order parameter of vertical field effect: $UA_{gv} = UA0_g + UAB_g \cdot vbs$
- Second order parameter of vertical field effect:
 $UB_{gv} = UB0_g + UBB_g \cdot vbs$
- Mobility reduction factor: $U1_{gv} = U10_g + U1B_g \cdot vbs$
- Exponential parameters for **gds** degradation due to high field:

$$AI_{gv} = AI0_g + AIB_g \cdot vbs \quad \text{and}$$

$$BI_{gv} = BI0_g + BIB_g \cdot vbs$$

- Threshold voltage offset in the substreshold region:

$$VOF_{gv} = VOF0_g + VOFB_g \cdot vbs + VOFD_g \cdot vds$$

- Subthreshold swing coefficient:

$$N_{gv} = N0_g + \frac{NB_g}{\sqrt{PHI_g - vbs}} + ND_g \cdot vds$$

- Drain induced barrier lowering coefficient:

$$ETA_{gv} = ETA_g + ETAB_g \cdot vbs$$

- Channel conductance coefficients:

$$\beta_{eta0} = \beta0_0 + \beta0_B \cdot vbs$$

$$\beta_{eta2} = \beta2_0 + \beta2_B \cdot vbs + \beta2_G \cdot vgs$$

$$\beta_{eta3} = \beta3_0 + \beta3_B \cdot vbs + \beta3_G \cdot vgs$$

$$\beta_{eta4} = \beta4_0 + \beta4_B \cdot vbs + \beta4_G \cdot vgs$$

$$\beta_{eta1} = \beta_{etas} - (\beta_{eta0} + VDD \cdot (\beta_{eta3} - VDD \cdot \beta_{eta4}))$$

where: $\beta_{etas} = \beta S_0 + \beta S_B \cdot vbs$

3.0 Static Current Equations

3.1 Threshold voltage

The threshold voltage Vth is calculated as follows:

$$Vth = VFB_g + PHI_g + K1_g \cdot \sqrt{PHI_g - vbs} - K2_g \cdot (PHI_g - vbs) - ETA_{gv} \cdot vds$$

3.2 Drain saturation voltage

The drain saturation voltage V_{dsat} is calculated as follows: $V_{dsat} = \frac{vgs - Vth}{A_v \cdot \sqrt{K_p}}$

$$\text{where: } K_p = \frac{1 + V_c + \sqrt{1 + 2 \cdot V_c}}{2} \quad V_c = \frac{U1_{gv} \cdot (vgs - Vth)}{A_v \cdot Uvert}$$

$$Uvert = 1 + (vgs - Vth) \cdot (UA_{gv} + UB_{gv} \cdot (vgs - Vth))$$

$$A_v = 1 + \frac{Gg_{gv} \cdot K1_g}{2 \cdot \sqrt{PHI_g - vbs}} \quad Gg_{gv} = 1 - \frac{1}{1.744 + 0.8364 \cdot (PHI_g - vbs)}$$

3.3 Drain Current in the Linear region

In the linear region the Drain current Ids is given by the following equation:

$$Ids = \beta_{eff} \cdot \left((vgs - Vth) - \frac{A_v}{2} \cdot vds \right)$$

$$\text{where: } \beta_{eff} = \frac{\beta_{eta}}{Uvert + U1 \cdot vds} \quad U1 = U1_{gv} \cdot \left(1 - U1D_g \cdot \left(\frac{vds - V_{dsat}}{V_{dsat}} \right)^2 \right)$$

$$\beta_{eta} = \beta_{eta0} + \beta_{eta1} \cdot \tanh\left(\frac{\beta_{eta2} \cdot vds}{V_{dsat}}\right) + vds \cdot (\beta_{eta3} - \beta_{eta4} \cdot vds)$$

3.4 Drain Current in the Saturation region

The saturation drain current is described as: $Ids = \beta_{eff} \cdot \frac{(vgs - Vth)^2}{2 \cdot A_v \cdot K_p} \cdot FR$

$$\text{where: } \beta_{eff} = \frac{\beta_{eta}}{Uvert} \quad \text{and} \quad FR = 1 + AI_{gv} \cdot \exp\left(\frac{BI_{gv}}{V_{dsat} - vds}\right)$$

3.5 Drain Current in the Weak inversion region

The lower bound V_{g1} and upper bound V_{g2} are defined as follows:

$$Vg1 = Vth + VGLOW_g \quad Vg2 = Vth + VGHIGH_g$$

When $vgs < Vg1$, the subthreshold current is defined as follows:

$$Ids = \beta \cdot \eta_{eff} \cdot Vt^2 \cdot \exp\left(\frac{vgs - Vth}{N_{gv} \cdot Vt}\right) + VOF_{gv} \cdot \left(1 - \exp\left(-\frac{vds}{Vt}\right)\right) \cdot FR$$

where Vt is the thermal voltage.

3.6 Drain Current in the Transition region

In the weak inversion to strong inversion ($V_{g1} \leq vgs \leq V_{g2}$), a vgs_{eff} voltage is defined by the following cubic splint function:

$$vgs_{eff} = C0 + C1 \cdot (vgs - Vth) + C2 \cdot (vgs - Vth)^2 + C3 \cdot (vgs - Vth)^3$$

where the Ci coefficients are determined so that the current and its derivative remains continuous at both boundaries V_{g1} and V_{g2} in relation to other regions of operation.

vgs_{eff} replaces $(vgs - Vth)$ in linear or saturation drain current calculations.

4.0 Charge Equations

4.1 Definitions

The effective gate voltage $Vgst$ is defined as follows: $Vgst = vgs - Vth$

The value of Cox is calculated from the value of TOX as follows: $Cox = \frac{eox}{TOX}$

where eox is the Permittivity of SiO_2 and is calculated as follows:

$$eox = 3.9 \times \epsilon_0 \text{ Fm}^{-1}; \text{ where: } \epsilon_0 = \text{Permittivity in a Vacuum} = 8.854214871 \times 10^{-12}$$

The effective capacitance of the device is defined as:

$$CAPOX = Cox \cdot W_{eff} \cdot L_{eff}$$

Q_{bulk} intermediate variable is defined as:

$$Q_{bulk} = \frac{1}{3} \cdot CAPOX \cdot (Vth - vbs - VFB_g)$$

4.2 Charge calculations

In the accumulation region ($vgb < VFB_g$)

$$Qg = CAPOX \cdot (vgb - VFB_g)$$

$$Qb = -Qg$$

$$Qd = 0$$

In the subthreshold region ($vbs + VFB_g < vgs < Vth + VGLOW_g$)

$$Qg = CAPOX \cdot (vgb - VFB_g) \cdot$$

$$\left(1.0 - \frac{vgb - VFB_g}{vgb - VFB_g - Vgst} + \frac{1}{3} \cdot \left(\frac{vgb - VFB_g}{vgb - VFB_g - Vgst} \right)^2 \right)$$

$$Qb = -Qg \quad Qd = 0$$

In the saturation region ($vds > Vdsat$)

$$Qg = \frac{2}{3} \cdot CAPOX \cdot Vgst + Q_{bulk} \quad Qb = -Q_{bulk}$$

$$Qd = -\frac{4}{15} \cdot CAPOX \cdot Vgst$$

In the linear region ($vds < Vdsat$)

$$Qg = \frac{2}{3} \cdot CAPOX \cdot Vgst \cdot \frac{3.0 \cdot (1.0 - fact) + fact^2}{2.0 - fact} + Qbulk$$

$$Qb = -Qbulk$$

$$Qd = \frac{1}{3} \cdot CAPOX \cdot Vgst \cdot \left(\frac{3.0 \cdot (1.0 - fact \cdot (17/15 - 0.4 \cdot fact))}{2.0 - fact} - \frac{0.2 \cdot fact \cdot (1.0 - fact)}{(2.0 - fact)^2} \right)$$

where: $fact = \frac{vds}{Vdsat}$

5.0 Temperature Effects

Specific model temperature effects are as follows:

$$U1_{gv}(T) = U1_{gv} \cdot \left(\frac{T}{T_{nom}} \right)^{FEX} \quad Vth(T) = Vth - TCV \cdot (T - T_{nom})$$

The mobility is adjusted through βeta according to: $\beta\text{eta}(T) = \beta \cdot \left(\frac{T}{T_{nom}} \right)^{BEX}$

6.0 Model Parameters

The complete list of model parameters is shown in the table on the following pages. Parameters marked in the table with a * after the parameter name also have corresponding parameters with a width and length dependency. For example, **VFB** is the basic parameter (with unit V), then **LVFB** and **WVFB** also exist and have units of V × μm. The parameter names marked with letters (a, b, c, ...) have a different value in the case of simulation with **.OPTION PRECISE** and the corresponding values are given in the table footnote.

Nr.	Name	Description	Default	Units
Threshold Voltage Related Model Parameters				
1	VFB*	Flat band voltage	-1	V
2	PHI*	Surface potential	0.75	V
3	K1^a*	Body effect coefficient	0.8	V ^{1/2}
4	K2^b*	Non-uniform doping effect	0	
5	ETA0*	Drain induced barrier lowering coefficient at Vbs=0	0	
6	ETAB*	Sensitivity of η to Vbs	0	V ⁻¹
Mobility Related Model Parameters				
7	MU0	Low field mobility	400	cm ² (Vs) ⁻¹
8	MU0B*	Sensitivity of μ_0 to Vbs	0	cm ² V ⁻² s ⁻¹
9	MUS0*	Mobility extracted at Vds=Vdd and Vbs=0	500	cm ² (Vs) ⁻¹
10	MUSB*	Sensitivity of μ_{sat} to Vbs	0	cm ² V ⁻² s ⁻¹
11	MU20*	Empirical parameter to model the output resistance	1.5	
12	MU2B*	Sensitivity of m_2 to Vbs	0	V ⁻¹
13	MU2G*	Sensitivity of m_2 to Vgs	0	V ⁻¹
14	MU30^c*	Empirical parameter to model the output resistance	0	cm ² V ⁻² s ⁻¹
15	MU3B*	Sensitivity of m_3 to Vbs	0	cm ² V ⁻³ s ⁻¹
16	MU3G*	Sensitivity of m_3 to Vgs	0	cm ² V ⁻³ s ⁻¹
17	MU40*	Empirical parameter to model the output resistance	0	cm ² V ⁻³ s ⁻¹
18	MU4B*	Sensitivity of m_4 to Vbs	0	cm ² V ⁻⁴ s ⁻¹
19	MU4G	Sensitivity of m_4 to Vgs	0	cm ² V ⁻⁴ s ⁻¹
20	VDD	Maximum Vds	5	V
21	VGG	Maximum Vgs	5	V
22	VBB^d	Maximum Vbs	-5	V
23	VGHIGH*	Upper bound of the transition level	0.2	V
24	VGLOW*	Lower bound of the transition level	-0.15	V
Mobility Modulation Related Model Parameters				
25	UA0*	Mobility reduction due to vertical field at Vbs=0	0.2	V ⁻¹
26	UAB*	Sensitivity of U_a to Vbs	0	V ⁻²
27	UB0*	Mobility reduction due to vertical field at Vbs=0	0	V ⁻²
28	UBB*	Sensitivity of U_b to Vbs	0	V ⁻³
Velocity Saturation Related Model Parameters				
29	U10*	Velocity saturation at Vds=Vdd and Vbs=0	0.1	V ⁻¹
30	U1B*	Sensitivity of U_1 to Vbs	0	V ⁻²

Nr.	Name	Description	Default	Units
31	U1D*	Sensitivity of U_1 to V_{ds}	0	V^{-2}
Subthreshold Related Parameters				
32	N0^e*	Subthreshold swing	1.4	
33	NB*	Sensitivity of n to V_{bs}	0.5	$V^{1/2}$
34	ND*	Sensitivity of n to V_{ds}	0	V^{-1}
35	VOFO*	Threshold voltage offset in the subthreshold region	1.8	
36	VOFB*	Sensitivity of n to V_{bs}	0	V^{-1}
37	VOFD*	Sensitivity of n to V_{ds}	0	V^{-1}
Hot Electron Related Parameters				
38	A10*	Hot electron induced output resistance degradation coefficient	0	
39	A1B*	Sensitivity of A_i to V_{bs}	0	V^{-1}
40	B10*	Hot electron induced output resistance degradation coefficient	0	V
41	B1B*	Sensitivity of B_i to V_{bs}	0	
Temperature Effect Related Model Parameters				
42	BEX	Low field mobility	-1.5	
43	FEX	Temperature exponent for $MU0$ mobility parameters	0	
44	TCV	Threshold voltage temperature coefficient	0	$V^{\circ}K^{-1}$
45	PTC	Fermi potential Φ_F temperature coefficient	0	$V^{\circ}K^{-1}$
Overlap Capacitance Related, and Dynamic Model Parameters				
46	CGDO^f	Gate-drain overlap capacitance per meter channel width	0	Fm^{-1}
47	CGSO^g	Gate-source overlap capacitance per meter channel width	0	Fm^{-1}
48	CGBO^h	Gate-bulk overlap capacitance per meter channel length	0	Fm^{-1}
49	XPART	Gate oxide capacitance charge model flag	0	
MOS Process Related Model Parameters				
50	TOX	Oxide thickness	0.03	μm
PRECISE Model Parameters (Used ONLY in PRECISE Mode)				
51	DELL	Source-drain length reduction	0	μm
52	DELW	Width increment	0	μm
53	METO	Metal overlap	0	m

- a. Default value is 0 $V^{1/2}$ with PRECISE option.
- b. Default value is 1 with PRECISE option.
- c. Default value is $10 \text{ cm}^2 \text{V}^{-2} \text{s}^{-1}$ with PRECISE option.
- d. Default value is 5V with PRECISE option.
- e. Default value is 200 with PRECISE option.
- f. Default value is calculated with PRECISE option.

- g. Default value is calculated with PRECISE option.
- h. Default value is calculated with PRECISE option.

Specific BSIM2 initialization for parasitics common approach MOS parameters:

```
ALEV=6; RLEV=0; DIOLEV=3; DCAPLEV=2  
if XJ is specified then LD=0.75×XJ; otherwise LD=0;  
CJ=0;  
FC is not a BSIM2 parameter, therefore it is set to 0.
```

Chapter 15

EKV MOSFET Equations

1.0 Introduction

The EKV model was originally developed by the EPFL (Ecole Polytechnique Fédérale de Lausanne), namely MM Enz, Krummenacher and Vittoz, hence the name. It is the result of many years of investigations to find a model that deals correctly with analog problems. Consequently, it may solve the problems of analog designers mainly in low voltage and low current applications and in terms of realistic behavior for currents, conductances and capacitances.

A compatible version of the EKV model is available in Eldo. This signifies that former versions of the model are also available. The compatibility covers versions v2.3 up to, and including, the new v2.6 (revision 4). The different versions are accessible through the model parameter **UPDATE** which can be used as shown in the table below. By default, the EKV model version v2.3 is selected.

Parameter Value	EKV Version
UPDATE=2.3 or UPDATE=23	EKV v2.3 (Default)
UPDATE=2.5 or UPDATE=25	EKV v2.5
UPDATE=2.61 or UPDATE=26.1	EKV v2.6 (Revision 1)
UPDATE=2.6 or UPDATE=26 UPDATE=2.62 or UPDATE=26.2	EKV v2.6 (Revision 2)
UPDATE=2.63 or UPDATE=26.3	EKV v2.6 (Revision 3)
UPDATE=2.64 or UPDATE=26.4	EKV v2.6 (Revision 4)

1.1 Model evolution since v2.3

Version 2.3

The model version 2.3 mainly includes the following effects:

- Impact ionization currents
- Simplified interpolation function
- More continuous equations outside the ‘normal’ operation area
- Modification of the ‘n’ calculation.

Version 2.5

- Adds a new dynamic charge/capacitance model
- A new analytic weak-to-strong inversion interpolation function $F(v)$ has been adapted for the new “charge conserving” dynamic, quasi-static charge/capacitance model. Numerically the new function $F(v)$ is very close to the former function used, ensuring close compatibility for DC. For AC and Transient applications, the choice is introduced between the former 5-capacitances model, and the new charge/capacitance model.
- Adds a new model for Reverse Short Channel Effect (RSCE), improving scaling behavior for submicron and deep submicron technologies (two new parameters, $Q0$ and LK). Fully compatible with former versions, since the new effect is by default off ($Q0=0$), and can be added if required.

Version 2.6 (revision 1)

- Adds a new and more physical mobility reduction model (new parameter **E0** is used instead of **THETA**).
- Some changes in narrow-channel effects improving the charge/capacitance model’s behavior for narrow devices.

Version 2.6 (revision 2)

- Intrinsic time constant τ_0 is calculated as a function of the effective β factor (including vertical field dependent mobility and short-channel effects) instead of maximum mobility according to the **KP** parameter. Therefore, the **NQS** time constant has an additional gate voltage dependence, resulting in more conservative (lower) estimation of the **NQS** time constant at high **VG**, and additional dependence on short-channel effects.
- Thermal noise power spectral density $S_{thermal}$ is calculated as a function of the effective beta factor (including vertical field dependent mobility and short-channel effects) instead of the maximum mobility according to the **KP** parameter. So $S_{thermal}$ has an additional gate voltage and short-channel effect dependence.
- An option is introduced to calculate the electrical parameters **COX**, **GAMMA** and/or **PHI**, **VTO**, **KP** and **UCRIT** as a function of the optional parameters **TOX**, **NSUB**, **VFB**, **UO**, and **VMAX**, respectively. **NSUB** and **UO** have cm as length units. Therefore, this accommodates scaling behavior and allows more meaningful statistical circuit simulation due to decorrelation of physical effects. Compatible with former revisions except for default calculation of the parameters mentioned, if the optional parameters are specified.
- The simple mobility model of former model versions, using the parameter **THETA**, is reinstated as an option. Therefore, this simplifies adaptation from earlier model versions to the current version.
- The analytical expression for the threshold voltage V_{th} in the operating point information is modified to include charge-sharing and reverse short-channel effects. The analytical expression for the saturation voltage **VDSAT** in the operating point information is modified such that its value is non-zero in weak inversion. This leads to improved information for the designer.

Version 2.6 (revision 3)

The Revision 3 for EKV v2.6 (v2.63) has a new model entitled charges/transcapacitances, this model has an improved asymptotic behavior. A single equation for the pinch-off voltage VP is used for the depletion-to-accumulation transition, thus eliminating the case statement formerly used. No additional parameters are introduced. It has been the aim to maintain backward compatibility with the former Revision 2 of EKV v2.6 as closely as possible so that the same parameter sets can be used in most cases. Compatibility issues are addressed in the following section.

Other small changes have occurred since EKV v2.3 to improve the model's continuity outside the normal range of operation and thus ease convergence issues. These changes do not affect the model's behavior in the normal range of operation.

Version 2.6 (revision 4)

Revision 4 for EKV v2.6 (v2.64) has been modified to include parameters XL and XW ; the masking and etching parameters for L and W . A default scheme has also been introduced linking the channel length/width correction parameters DL/DW with the diffusion length/width parameters LD/WD . In addition, length/width multiplication parameters $LMLT/WMLT$ have also been introduced.

1.2 Compatibility between v2.3, v2.5 and v2.6

With the continuing development of the EKV model, several new features have been added as mentioned in the previous section. New features have been added mostly in a way such that other modeled effects remain unchanged, and that formerly used parameter sets can be reasonably used with the newer versions. However, some restrictions should be observed. These are listed below:

Static model

- v2.3 and v2.5 are compatible if the RSCE effect is not used in v2.5 (which is by default off).
- If v2.6 is to be used with former v2.3 parameters, the following recommendations should be observed:

- For v2.6 (revision 1), the new mobility parameter **E0** should be adapted such that it gives comparable results to the former parameter used: **THETA**.
For v2.6 (revision 2) the simple mobility model using the parameter **THETA** is reinstated and hence there are no modifications required.
- Narrow channel model parameters **DW** and **WETA** have to be adapted (if they remain unchanged, the strong inversion current and transconductances may differ by up to 10-15% for narrow-channel devices, depending on parameter values and bias range). Typically, **WETA** should be increased by 5-10%, and **DW** needs to be adapted such that inversion current is increased.

Dynamic model

(i) $XQC=1$ (Capacitance model)

v2.3, v2.5 and v2.6 are all compatible for all ranges of frequency.

(ii) $XQC=0$ (Charge model)

v2.6 results of $XQC=0$ are close to $XQC=1$.

v2.5 results of $XQC=0$ may differ from $XQC=1$, depending on the value of the narrow-channel effect parameter **WETA**.

Both v2.5 and v2.6 charge models should not be used for frequencies above 1×10^9 Hz.

Backward compatibility of v2.63 with v2.62

For the static IV curves, the differences between the model versions are almost negligible. A small difference in simulated current results in very deep weak inversion, due to the slightly reduced weak inversion slope, or at high back biases, where a small residual threshold voltage offset (less than 10mV) can be observed. Using the same DC model parameters in v2.63 as in v2.62 should not result in significantly changed circuit behavior in most applications.

Charges can differ significantly between the two versions mostly for short and/or narrow devices. This is of limited importance however, and is by far outweighed by the improved asymptotic behavior of the transcapacitances. Transcapacitances are now smooth in the depletion/accumulation transition due to a mathematical conditioning.

Total gate capacitance reaches $COX \times Weff \times Leff$ correctly both in accumulation and inversion, now also for short and/or narrow devices. Symmetry such as for ($Cgs - Csg$), ($Cgd - Cdg$), ($Cgb - Cbg$) is significantly improved. Dynamic behavior may be significantly improved for a number of applications. In some cases, overlap capacitance parameters may need to be adapted when using v2.62 parameter sets.

The non-quasistatic (NQS) model is modified for v2.63 (v2.63 results differ than v2.62).

2.0 Static Intrinsic Model Equations

Intrinsic model equations are presented for an N-channel MOSFET. Voltages are all referred to the local substrate:

$(V_G = V_{GB})$ Intrinsic gate-to-bulk voltage

$(V_S = V_{SB})$ Intrinsic source-to-bulk voltage

$(V_D = V_{DB})$ Intrinsic drain-to-bulk voltage

V_S and V_D are the intrinsic voltages, which means that the voltage drop over extrinsic resistive elements is supposed to have already been accounted for. V_D is the electrical drain voltage such that $V_D \geq V_S$, as the device is inherently symmetric. P-channel MOSFETs are dealt with as pseudo-N-channel, i.e. the polarity of all the voltages (V_G , V_S , V_D , as well as **VFB**, **VTO** and **TCV**) is inverted prior to computing the current for P-channel, which is given a negative sign. No other distinctions are made between N-channel and P-channel, with the exception of the η factor for effective mobility calculation.

The model is basically formulated as a ‘single expression’, which preserves continuity of first- and higher-order derivatives with respect to any terminal voltage, in the entire range of validity of the model. The analytical expressions of first-order derivatives are not presented in this document but are also available.

2.1 EKV model equations version 2.6

Drain-to-source current

$$I_{DS} = I_S \cdot (i_f - i'_r)$$

$$I_S = 2 \cdot n \cdot \beta \cdot V_t^2 \quad \text{Specific current}$$

$$V_t = \frac{k \cdot T}{q} \quad \text{Thermal voltage}$$


Note

This drain current expression is a single equation, valid in all operating regions: weak, moderate and strong inversion, non-saturation and saturation. It is therefore not only continuous among all these regions, but also continuously derivable.

Effective channel length and width

$$L_{eff} = L + DL$$

$$W_{eff} = W + DW$$


Note

DL and **DW** normally have a negative value due to the above definition.

If UPDATE=2.64 or UPDATE=26.4 are present in the .MODEL command, the following equations are active:

$$L_{eff} = LMLT(L + DL + XL)$$

$$W_{eff} = WMLT(W + DW + XW)$$

Default scheme associating ***DL/DW*** with ***LD/WD***

If ***DL*** is given but ***LD*** is not given, $LD = -DL/2.0$.

If ***DL*** is not given but ***LD*** is given, $DL = -2.0 \cdot LD$.

When both ***DL*** and ***LD*** are given, if $DL \neq -2 \cdot LD$, then $LD = -DL/2$. The following warning message will be shown:

"Specified LD ignored. LD set to -DL/2."

If neither ***DL*** or ***LD*** are given, then both ***DL*** and ***LD*** are equal to 0.

LD is the diffusion length parameter and ***WD*** is the diffusion width parameter.

The above rules also apply for the width parameters ***DW*** and ***WD***.

Short distance matching

Random mismatch between two transistors which are identical in layout and close to each other, is in most cases suitably described by a law following the inverse of the square root of the transistors' area. The following relationships have been adopted:

$$\begin{aligned} VTO_a &= VTO + \frac{AVTO}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}} \\ KP_a &= KP \cdot \left(1 + \frac{AKP}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}} \right) \\ GAMMA_a &= GAMMA + \frac{AGAMMA}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}} \end{aligned}$$

These model equations are only applicable in Monte Carlo and sensitivity simulations.



Note

Since negative values for both KP_a and $GAMMA_a$ are not physically meaningful, these are clipped at zero.

Reverse short-channel effect

$$C_\varepsilon = 4 \cdot (22 \times 10^{-3})^2$$

$$C_A = 0.028$$

$$\xi = C_A \cdot \left(10 \cdot \frac{L_{eff}}{L_K} - 1 \right)$$

$$\Delta V_{RSCE} = \frac{2 \cdot Q_0}{COX} \cdot \frac{1}{\left[1 + \frac{1}{2} \cdot (\xi + \sqrt{\xi^2 + C_\varepsilon}) \right]^2}$$

Effective gate voltage including RSCE

$$V_G' = V_G - VTO_a - \Delta V_{RSCE} + PHI + GAMMA_a \sqrt{PHI}$$

Long-channel pinch-off voltage

$$V_{P0} = \begin{cases} V_G' - PHI - GAMMA_a \left(\sqrt{V_G' + \left(\frac{GAMMA_a}{2} \right)^2} - \frac{GAMMA_a}{2} \right) & \text{for: } V_G' > 0 \\ -PHI & \text{for: } V_G' \leq 0 \end{cases}$$

Bias and geometry dependent body effect factor

$$V'_{S(D)} = \frac{1}{2} \cdot [V_{S(D)} + PHI + \sqrt{(V_{S(D)} + PHI)^2 + (4V_t)^2}]$$

$$\gamma^\circ = GAMMA_a - \frac{\varepsilon_0 \cdot \varepsilon_{Si}}{COX} \cdot \left[\frac{LETA}{L_{eff}} \cdot (\sqrt{V'_S} + \sqrt{V'_D}) - \frac{3 \cdot WETA}{W_{eff}} \cdot \sqrt{V_{P0}} \right]$$

$$\gamma' = \frac{1}{2} \cdot (\gamma^\circ + \sqrt{\gamma^\circ^2 + 0.1 \cdot V_t})$$

Pinch-off voltage including short and narrow channel effects

$$V_P = \begin{cases} V'_G - \text{PHI} - \gamma' \cdot \left(\sqrt{V'_G + \left(\frac{\gamma'}{2}\right)^2} - \frac{\gamma'}{2} \right) & \text{for: } V'_G > 0 \\ -\text{PHI} & \text{for: } V'_G \leq 0 \end{cases}$$



The pinch-off voltage accounts for channel doping effects such as threshold voltage and substrate effect. For long-channel devices, V_p is a function of gate voltage; for short-channel devices, it also becomes a function of source and drain voltage due to the charge-sharing effect.

Slope factor

$$n = 1 + \frac{\text{GAMMA}_a}{2 \cdot \sqrt{V_P + \text{PHI} + 4V_t}}$$



The slope factor (or body effect factor), which is primarily a function of the gate voltage, is linked to the weak inversion slope.

Velocity saturation current

$$V_{DSS} = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \sqrt{i_f}} - \frac{1}{2} \right]$$

$$V_C = \text{UCRIT} \cdot L_{eff}$$

Drain-to-source saturation voltage

$$V'_{DSS} = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \left(\sqrt{i_f} - \frac{3}{4} \cdot \ln(i_f) \right)} - \frac{1}{2} \right] + V_t \cdot \left[\ln\left(\frac{V_C}{2V_t}\right) - 0.6 \right]$$

Channel length modulation

$$\Delta V = 4 \cdot V_t \cdot \sqrt{\text{LAMBDA} \cdot \left(\sqrt{i_f} - \frac{V_{DSS}}{V_t} \right) + \frac{1}{64}}$$

$$V_{ds} = \frac{V_D - V_S}{2}$$

$$V_{ip} = \sqrt{V_{DSS}^2 + \Delta V^2} - \sqrt{(V_{ds} - V_{DSS})^2 + \Delta V^2}$$

$$L_C = \sqrt{\frac{\varepsilon_0 \varepsilon_{si}}{\text{COX}}} \cdot \text{xJ} \text{ with}$$

$$\varepsilon_0 \varepsilon_{si} = \text{SCALE} \cdot 104.5 \times 10^{-12} [F/m]$$

$$\Delta L = \text{LAMBDA} \cdot L_C \cdot \ln \left(1 + \frac{V_{ds} - V_{ip}}{L_C \cdot \text{UCRIT}} \right)$$



This is the only place where scaling is required in the EKV model.

Equivalent channel length including CLM and velocity saturation

$$L_{eq} = \frac{1}{2} \cdot (L' + \sqrt{L'^2 + L_{min}^2})$$

$$L' = L_{eff} - \Delta L + \frac{V_{ds} + V_{ip}}{\text{UCRIT}}$$

$$L_{min} = L_{eff}/10$$

Normalized currents and interpolation function

Forward normalized current:

$$i_f = F \left[\frac{V_P - V_S}{V_t} \right]$$

Reverse normalized current:

$$i_r' = \left\{ F \left[\frac{V_P - V_{ds} - V_S - \sqrt{V_{DSS}^2 + \Delta V^2} + \sqrt{(V_{ds} - V_{DSS})^2 + \Delta V^2}}{V_t} \right] \right\}$$

Large signal interpolation function

$F(v)$ is the large-signal interpolation function relating the normalized currents to the normalized voltages. A simple and accurate expression for the transconductance interpolation allows a consistent formulation of the large-signal interpolation function and the dynamic model for the intrinsic charges (and capacitances) as well as the intrinsic time constant.

$$gms \cdot V_t / I_D = \frac{\sqrt{0.25 + i} - 0.5}{i}$$

Large-signal interpolation function:

$$y = \sqrt{0.25 + i} - 0.5$$

$$v = 2y + \ln(y)$$

Unfortunately, the above equation cannot be inverted; however it can be inverted using a Newton-Raphson iterative scheme. A simplification of this algorithm leads to the following expressions for the large signal interpolation function that avoids iteration, ensuring continuous behavior at the boundaries:

$$z_0 = \begin{cases} \frac{2}{1.3 + v - \ln(v + 1.6)} & \text{for: } v \geq -0.35 \\ 1.55 + \exp(-v) & \text{for: } -15 \leq v < -0.35 \end{cases}$$

$$z_1 = \frac{2 + z_0}{1 + v + \ln(z_0)}$$

$$y = \begin{cases} \frac{1 + v + \ln(z_1)}{2 + z_1} & \text{for: } v > -15 \\ \frac{1}{2 + \exp(-v)} & \text{for: } v \leq -15 \end{cases}$$

$$i = y \cdot (1 + y)$$

Simplified large signal interpolation function

For hand calculations, an analytically simple interpolation function, presenting the same asymptotic behavior with slightly reduced accuracy, is often used. This interpolation function is also available for circuit simulation by setting the EKV interpolation function selector **EKVINT=1**.

$$F(v) = [\ln(1 + \exp(v/2))]^2$$



The large signal interpolation function selector **EKVINT** applies to all model versions.

Note

Transconductance factor & mobility reduction due to vertical field

$$\beta = \frac{\beta_0'}{1 + \frac{C_{OX}}{E_0 \cdot \epsilon_0 \epsilon_{si}} \cdot V_t \cdot |q_B + \eta \cdot q_I|}$$

$$\beta_0' = \beta_0 \cdot \left(1 + \frac{C_{OX}}{\epsilon_0 \cdot \epsilon_{si}} \cdot q_{B0} \right)$$

$$\beta_0 = K_P \cdot \frac{N_P \cdot W_{eff}}{N_S \cdot L_{eq}}$$



Note The use of the device parameter NP (or M) gives accurate results for simulation of parallel devices, whereas the use of NS for series devices is only approximate.

$$\eta = \begin{cases} 1/2 & \text{for NMOS} \\ 1/3 & \text{for PMOS} \end{cases}$$

$$q_{B0} = \text{GAMMA}_a \cdot \sqrt{\text{PHI}}$$

For definition of the normalized bulk and inversion charges q_B and q_I please refer to the section on the node charges.

The use of β'_0 ensures that $\beta \approx \beta_0$ when $q_I \ll q_B$. The formulation of β arises from the integration of the local effective field as a function of depletion and inversion charge densities along the channel. No substrate bias dependency is needed due to the inclusion of depletion charge. Note that the resulting mobility expression also depends on V_{DS} .

Impact ionization current

$$I_B = \begin{cases} I_{DS} \cdot \frac{I_{BA}}{I_{BB}} \cdot V_{ib} \cdot \exp\left(\frac{-I_{BB} \cdot L_C}{V_{ib}}\right) & \text{for: } V_{ib} > 0 \\ 0 & \text{for: } V_{ib} \leq 0 \end{cases}$$

$$V_{ib} = V_D - V_S - 2 \cdot I_{BN} \cdot V_{DSS}$$

**Note**

The factor 2 in the expression for V_{ib} accounts for the fact that the numerical value of V_{DSS} is half the actual saturation voltage. Further note that the substrate current is intended to be treated as a component of the total extrinsic drain current, flowing from the drain to the bulk. The total drain current is therefore expressed as $I_D = I_{DS} + I_{DB}$.

The substrate current therefore also affects the total extrinsic conductances, in particular the drain conductance.

2.2 EKV model equations Version 2.5

Only the equations that differ from version 2.6 are listed here; they replace the corresponding equations in the [EKV model equations version 2.6](#) section.

Transconductance factor

$$\beta = K_P \cdot \frac{W_{eff}}{L_{eq}} \cdot \frac{1}{1 + \text{THETA} \cdot V'_P}$$

Pinch-off voltage including short and narrow channel effects

$$V'_P = \begin{cases} V'_G - \text{PHI} - \gamma' \cdot \left(\sqrt{V'_G + \left(\frac{\gamma'}{2}\right)^2} - \frac{\gamma'}{2} \right) & \text{for: } V'_G > 0 \\ -\text{PHI} & \text{for: } V'_G \leq 0 \end{cases}$$

$$\text{where: } V'_G = V_G - \text{VTO} + \text{PHI} + \text{GAMMA} \cdot \sqrt{\text{PHI}}$$

$$\gamma' = \text{GAMMA} - \frac{\epsilon_0 \cdot \epsilon_{Si}}{\text{COX}} \cdot$$

$$\left[\left(\frac{\text{LETA}}{L + \text{DL}} - \frac{3 \cdot \text{WETA}}{W + \text{DW}} \right) \cdot \sqrt{V'_S + \text{PHI}} + \frac{\text{LETA}}{L + \text{DL}} \cdot \sqrt{V'_D + \text{PHI}} \right]$$

$$V'_{S(D)} = \frac{1}{2} \cdot [V_{S(D)} - \text{PHI} + \sqrt{(V_{S(D)} + \text{PHI})^2 + (4V_t)^2}]$$

$$V'_P = \frac{1}{2} \cdot (V_P + \sqrt{V_P^2 + 2V_t^2})$$

2.3 EKV model equations Version 2.3

Only the equations that differ from version 2.5 are listed here; they replace the corresponding equations in the [EKV model equations Version 2.5](#) section.

Drain-to-source saturation voltage

$$V'_{DSS} = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \left(\sqrt{i_f} - \frac{3}{4} \cdot \ln(i_f) \right)} - \frac{1}{2} \right] + V_t \cdot \left[\ln\left(\frac{V_C}{2V_t}\right) - 1 \right]$$

Large signal interpolation function

$F(v)$ is the large-signal interpolation function relating the normalized currents to the normalized voltages. In the version for computer simulation, this function is closely approximated with analytical functions using four intervals, since it cannot be directly expressed analytically. Each partial interpolation function uses up to four coefficients, which are available with the model code.

$$F(v) = \begin{cases} i_a = \frac{e^v}{1 + c_{A0} \cdot e^v} & \text{for: } v < -3 \\ i_b = \frac{c_{B0} \cdot e^{c_{B1} \cdot v}}{1 + c_{B2} \cdot e^{c_{B3} \cdot v}} & \text{for: } -3 \leq v < -1 \\ i_c = \left[\frac{c_{C0} \cdot e^{c_{C1} \cdot v}}{1 + c_{C2} \cdot e^{c_{C3} \cdot v}} \right]^2 & \text{for: } -1 \leq v < 2.5 \\ i_d = [c_{D0} + c_{D1} \cdot v - c_{D2} \cdot \ln(c_{D3} + v)]^2 & \text{for: } v \geq 2.5 \end{cases}$$

3.0 Quasi-Static Model Equations

A new dynamic model is present in EKV versions v2.5 and v2.6.

3.1 Dynamic model for the intrinsic node charges (v2.5 and v2.6 only)

$$n_q = 1 + \frac{\text{GAMMA}_a}{2 \cdot \sqrt{V_P + \text{PHI} + 10^{-6}}}$$

Normalized intrinsic node charges

$$x_f = \sqrt{\frac{1}{4} + i_f}$$

$$x_r = \sqrt{\frac{1}{4} + i_r}$$

$$q_D = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_r^3 + 6x_r^2x_f + 4x_rx_f^2 + 2x_f^3}{(x_f + x_r)^2} - \frac{1}{2} \right)$$

$$q_S = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_f^3 + 6x_f^2x_r + 4x_fx_r^2 + 2x_r^3}{(x_f + x_r)^2} - \frac{1}{2} \right)$$

$$q_I = q_S + q_D = -n_q \cdot \left(\frac{4}{3} \cdot \frac{x_f^2 + x_fx_r + x_r^2}{x_f + x_r} - 1 \right)$$

$$q_B = \begin{cases} \left(-\text{GAMMA}_a \cdot \sqrt{V_P + \text{PHI} + 10^{-6}} \right) \cdot \frac{1}{V_t} - \left(\frac{n_q - 1}{n_q} \right) \cdot q_I & \text{for: } V'_G > 0 \\ -V'_G \cdot \frac{1}{V_t} & \text{for: } V'_G \leq 0 \end{cases}$$

$$q_G = -q_I - q_{OX} - q_B$$

q_{OX} is a fixed oxide charge assumed to be zero. The above equation expresses the charge conservation among the four nodes of the transistor.

Total node charges

$$C_{ox} = \text{COX} \cdot \text{NP} \cdot W_{eff} \cdot \text{NS} \cdot L_{eff}$$

$$Q_I = C_{ox} \cdot V_t \cdot q_I$$

$$Q_B = C_{ox} \cdot V_t \cdot q_B$$

$$Q_D = C_{ox} \cdot V_t \cdot q_D$$

$$Q_S = C_{ox} \cdot V_t \cdot q_S$$

$$Q_G = C_{ox} \cdot V_t \cdot q_G$$

3.2 Intrinsic capacitances (for versions EKV v2.5 and v2.6 only)

Transcapacitances

The intrinsic capacitances are obtained through derivation of the node charges with respect to the voltages between the nodes.

$$C_{xy} = \pm \frac{\partial}{\partial y}(Q_x)$$

where $x, y = D, G, S, B$.

In the above equation, the positive sign is chosen when $x = y$, and the negative sign otherwise. This results in simple and continuous analytical expressions for all the transcapacitances in terms of x_f , x_r , the pinch-off voltage and the slope factor, and derivatives thereof, from weak to strong inversion and non-saturation to saturation.

A simpler model using the five intrinsic capacitances, can be obtained when neglecting the slight dependence on the slope factor n , resulting in the following simple functions:

Normalized intrinsic capacitances

$$c_{gs} = \frac{2}{3} \cdot \left(1 - \frac{x_r^2 - x_r + \frac{1}{2}x_f}{(x_f + x_r)^2} \right)$$

$$c_{gd} = \frac{2}{3} \cdot \left(1 - \frac{x_f^2 - x_f + \frac{1}{2}x_r}{(x_f + x_r)^2} \right)$$

$$c_{gb} = \left(\frac{n_q - 1}{n_q} \right) \cdot (1 - c_{gs} - c_{gd})$$

$$c_{sb} = (n_q - 1) \cdot c_{gs}$$

$$c_{db} = (n_q - 1) \cdot c_{gd}$$

Total intrinsic capacitances

$$C_{gs} = C_{ox} \cdot c_{gs}$$

$$C_{gd} = C_{ox} \cdot c_{gd}$$

$$C_{gb} = C_{ox} \cdot c_{gb}$$

$$C_{sb} = C_{ox} \cdot c_{sb}$$

$$C_{db} = C_{ox} \cdot c_{db}$$

3.3 Intrinsic capacitances for version=2.3

Reverse normalized current for intrinsic capacitances

$$i_r = F \left[\frac{V_P - V_D}{V_t} \right]$$

Interpolation functions

$$c_{gsw}(i) = \frac{i}{\sqrt{1 + \frac{1}{2} \cdot \sqrt{i} + i}}$$

$$c_{gss}(i_f, i_r) = \frac{2}{3} \cdot \left[1 - \frac{i_r}{(\sqrt{i_f} + \sqrt{i_r})^2} \right]$$

$$c_{gs}(i_f, i_r) = \frac{c_{gsw}(i_f) \cdot c_{gss}(i_f, i_r)}{c_{gsw}(i_f) + c_{gss}(i_f, i_r)}$$

$$c_{gbw} = c_{gsw}(i_f) + c_{gsw}(i_r)$$

$$c_{gbs} = \frac{2}{3} \cdot \left[1 + 2 \cdot \frac{\sqrt{i_f \cdot i_r}}{(\sqrt{i_f} + \sqrt{i_r})^2} \right]$$

$$c_{gb} = \begin{cases} \frac{\text{GAMMA}}{2 \cdot \sqrt{V_P + \text{PHI} + \text{GAMMA}}} \cdot \left(1 - \frac{c_{gbw} \cdot c_{gbs}}{c_{gbw} + c_{gbs}} \right) & \text{for: } V_P > -\text{PHI} \\ 1 - \frac{c_{gbw} \cdot c_{gbs}}{c_{gbw} + c_{gbs}} & \text{for: } V_P \leq -\text{PHI} \end{cases}$$

Intrinsic capacitances equations

$$C_{ox} = W_{eff} \cdot L_{eff} \cdot \text{COX}$$

$$C_{gsi} = C_{ox} \cdot c_{gs}(i_f, i_r)$$

$$C_{gdi} = C_{ox} \cdot c_{gs}(i_r, i_f)$$

$$C_{gbi} = C_{ox} \cdot c_{gb}$$

$$C_{sbi} = C_{ox} \cdot (n - 1) \cdot c_{gs}(i_f, i_r)$$

$$C_{dbi} = C_{ox} \cdot (n - 1) \cdot c_{gs}(i_r, i_f)$$

3.4 Overlap capacitances (for all versions)

$$C_{gsov} = W_{eff} \cdot CGSO$$

$$C_{gdov} = W_{eff} \cdot CGDO$$

$$C_{gbov} = L_{eff} \cdot CGBO$$

3.5 Total capacitances (for all versions)

$$C_{gs} = C_{gsi} + C_{gsov}$$

$$C_{gd} = C_{gdi} + C_{gdov}$$

$$C_{gb} = C_{gbi} + C_{gbov}$$

$$C_{sb} = C_{sbi} + C_{sbj}$$

$$C_{db} = C_{dbi} + C_{dbj}$$



These capacitances are *valid in all regions of operation*.

Note

4.0 Non-Quasi-Static (NQS) Model Equations

4.1 NQS model equations for versions > 2.3

The EKV model includes a first order NQS model for small-signal (.AC) simulations. The expression of the NQS drain current is obtained from the quasi-static value of the drain current which is then 1st-order low-pass filtered according to:

$$I_{DS}(s) = \frac{I_{DSq}(s)}{1 + NQS \cdot s \cdot \tau}$$

where NQS is a flag (model parameter) allowing the NQS model to be disabled and τ is the characteristic time constant which depends on the bias according to:

$$\tau = \tau_0 \cdot \frac{4}{15} \cdot \frac{(x_f^2 + 3x_fx_r + x_r^2)}{(x_f + x_r)^3}$$

τ_0 is the intrinsic time constant defined as:

$$\tau_0 = \frac{\text{COX} \cdot (\text{NS} \cdot L_{eff})^2}{2 \cdot K_P \cdot V_t} = \frac{(\text{NS} \cdot L_{eff})^2}{2 \cdot \mu \cdot V_t}$$

The corresponding small-signal (.AC) transadmittances are then given by:

$$Y_m(s) = \frac{g_m}{1 + \text{NQS} \cdot s \cdot \tau}$$

$$Y_{ms}(s) = \frac{g_{ms}}{1 + \text{NQS} \cdot s \cdot \tau}$$

$$Y_{mbs}(s) = Y_{ms}(s) - Y_m(s) - g_{ds}$$

where g_m , g_{ms} and g_{ds} are the transconductances and output conductance evaluated at the operating point.

4.2 NQS model equations for version=2.3

Exactly the same as for versions>2.3, except:

$$\tau = \frac{\tau_0}{3} \cdot \left(1 + \frac{25}{16} \cdot \left(\frac{(\sqrt{i_f} + \sqrt{i_r})^3}{i_f + 3 \cdot \sqrt{i_f \cdot i_r} + i_r} \right)^2 \right)^{-\frac{1}{2}}$$

5.0 Intrinsic Noise Model Equations

The noise is modeled by a current source ***INDS*** between intrinsic source and drain. It is composed of a thermal noise component and a flicker noise component and has the following Power Spectral Density (PSD):

$$S_{INDS} = S_{thermal} + S_{flicker}$$



Note

Eldo has different thermal and flicker noise models for Mosfets. You can choose any of these models using either the model parameters ***THMLEV*** and ***FLKLEV***, or with the options **.OPTION thermal_noise=VAL** and **.OPTION flicker_noise=VAL**. The default value for ***THMLEV*** and ***FLKLEV*** is 0. EKV model replaces the default model (model 0) by its own internal default model. When you specify ***THMLEV*** (or ***FLKLEV***) = 0 in EKV, you actually choose the internal default model of EKV and not the default model of Eldo. Nevertheless, you can still use any of the other Eldo models specified by values not equal to 0.

5.1 Thermal noise

For version 2.6 (revision 2)

The thermal noise component PSD is given by:

$$S_{thermal} = 4 \cdot k \cdot T \cdot \beta \cdot |q_I|$$



Note

The above thermal noise expression is *valid in all regions of operation*, including for small V_{DS} .

For other versions (including v2.6—revision 1)

The thermal noise component PSD is given by:

$$S_{thermal} = 4 \cdot k \cdot T \cdot \xi \cdot g_{ms} = 4 \cdot k \cdot T \cdot \xi \cdot (g_m + g_{mbs} + g_{ds})$$

where g_{ms} is the source transconductance and γ is the noise factor defined as:

$$\xi = \frac{1}{1+i_f} \cdot \left[\frac{1}{2} \cdot (1+\alpha) + \frac{2}{3} \cdot i_f \cdot \frac{1+\alpha+\sqrt{\alpha}}{1+\sqrt{\alpha}} \right] \quad \text{where: } \alpha = \frac{i_r}{i_f}$$

5.2 Flicker noise

The flicker noise component PSD is given by:

$$S_{flicker} = \frac{K_F \cdot g_m^2}{N_P \cdot W_{eff} \cdot N_S \cdot L_{eff} \cdot C_{OX} \cdot f^{AF}}$$

6.0 Temperature Effects

Implementation of temperature effects as well as default values may be implementation dependent; please consult the documentation of your simulator.

$TEMP$ = operating temperature in °C $T = TEMP+273$ operating temperature in K

$TNOM$ = reference temperature in °C $T_{ref} = TNOM+273$ reference temperature in K

$$V_t(T) = \frac{k \cdot T}{q} \quad \text{Thermal voltage}$$

$$E_g(T) = 1.16 - 0.000702 \cdot \frac{T^2}{T+1108} \quad \text{Energy gap}$$

6.1 Intrinsic parameters temperature update

$$VTO(T) = VTO - TCV \cdot (T - T_{ref})$$

$$KP(T) = KP \cdot \left(\frac{T}{T_{ref}} \right)^{BEX}$$

$$UCRIT(T) = UCRIT \cdot \left(\frac{T}{T_{ref}} \right)^{UCEX}$$

$$\text{PHI}(T) = \text{PHI} \cdot \frac{T}{T_{ref}} - 3 \cdot V_t \cdot \ln\left(\frac{T}{T_{ref}}\right) - E_g(T_{ref}) \cdot \frac{T}{T_{ref}} + E_g(T)$$

$$\text{IBB}(T) = \text{IBB} \cdot [1.0 + \text{IBBT} \cdot (T - T_{ref})]$$

7.0 Operating Point Information

At operating points, the following information is displayed:

- numerical values of: I_{DS} , V_G , V_S , V_D , g_m , g_{ms} , g_{mbs} , g_{ds} , V_P , n , I_S , i_f , ir , i_r' , τ , τ_0
intrinsic and total capacitances, junction currents
- transconductance efficiency factor: $tef = g_{ms} \cdot V_t / I_{DS}$
- 'early voltage': $VM = I_{DS} / g_{ds}$
- overdrive voltage: $n \cdot (V_P - V_S) \approx V_G - VTO - n \cdot V_S$
- a flag for saturation/non-saturation, depending on the following criterion:

$$'SAT' \quad or \quad '1' \quad \quad \quad \text{if} \quad \frac{i_f}{i_r} > \text{SATLIM}$$

$$'LIN' \quad or \quad '0' \quad \quad \quad \text{if} \quad \frac{i_f}{i_r} \leq \text{SATLIM}$$

8.0 Estimation and Limits of Intrinsic Model Parameters

The EKV intrinsic model parameters can be roughly estimated from Spice level 2/3 parameters as indicated in the table below if no parameter extraction facility is available. Attention has to be paid to respective units of the parameters. This estimation method can be helpful and generally gives reasonable results. Nevertheless be aware that the underlying modeling in Spice level 2/3 and in the

EKV model is not the same, even if the names and the function of several parameters are similar.

Lower and upper limits indicated in the table should give an idea on the order of magnitude of the parameters but do not necessarily correspond to physically meaningful limits. They may help to get physically meaningful parameter sets when using nonlinear optimization techniques to extract EKV model parameters.

Name	Units	Default	Example	'Lower'	'Upper'	Estimation
COX	Fm ⁻²	0.7×10 ⁻³	1.5×10 ⁻³			ϵ_{ox}/TOX
XJ	m	0.1×10 ⁻⁶	0.15×10 ⁻⁶	0.01×10 ⁻⁶	1.0×10 ⁻⁶	XJ
VTO	V	0.5	0.7	0.1	2.0	VTO
GAMMA	V ^{1/2}	1.0	0.7	0.0	2.0	$\sqrt{2q\epsilon_{si} \cdot NSUB / COX}$
PHI	V	0.7	0.5	0.3	2.0	$2V_t \cdot \ln(NSUB/n_i)$
KP	AV ⁻²	50×10 ⁻⁶	80×10 ⁻⁶	10×10 ⁻⁶	150×10 ⁻⁶	U0 · COX
THETA	V ⁻¹	0.0	0.04	0.0	0.2	
UCRIT	Vm ⁻¹	2×10 ⁶	1.8×10 ⁶	1×10 ⁶	15×10 ⁶	VMAX/U0
DL	m	0.0	-0.25×L _{min}	-0.5×L _{min}	0.0	XL - 2 · LD
DW	m	0.0	-0.1×W _{min}	-0.5×W _{min}	0.0	XW - 2 · WD
LAMBDA		0.5	0.8	0.0	5.0	
LETA		0.1	0.3	0.001	5.0	
WEWA		0.25	0.2	0.001	5.0	
IBA	m ⁻¹	0.0	2.0×10 ⁸	0.0	5.0×10 ⁸	ALPHA · VCR / L _C
IBB	Vm ⁻¹	3.0×10 ⁸	2.0×10 ⁸	1.8×10 ⁸	4.0×10 ⁸	VCR / L _C
IBN		1.0	0.6	0.4	1.0	

$$\epsilon_{ox} = 0.0345 \times 10^{-9} \text{ Fm}^{-1}$$

$$q = 1.609 \times 10^{-19} \text{ C}$$

$$k = 1.381 \times 10^{-23} (\text{AsV})^\circ \text{K}^{-1}$$

$$L_C = \sqrt{\epsilon_{si} \cdot XJ / COX}$$

$$\epsilon_{si} = 0.104 \times 10^{-9} \text{ Fm}^{-1}$$

$$n_i = 1.45 \times 10^{15} \text{ m}^{-3}$$

$$V_t = kTq^{-1} = 0.0259 \text{ V}$$



Parameters in this table assume that m (meter) has been chosen as length unit. L_{min} and W_{min} are the minimum drawn length and width of the transistors. Example values are indicated for N-channel devices.

9.0 Model Parameters

Setup parameters

Nr.	Name	Description	Default
1	UPDATE	EKV model version selector ^a	2.3
2	EKVINT	EKV large signal interpolation function selector ^b	0
3	NQS	Non-Quasi-Static (NQS) operation switch	0 ^c
4	SATLIM	Ratio defining the saturation limit ^d i_f/i_r	10^4
5	SCALEM	Parameter scaling factor	1
6	XQC	Charge/Capacitance model selector ^e	1

- a. The EKV model v2.3 is selected by default. Newer versions 2.5 and 2.6, can be accessed by specifying the appropriate value of the model version selector, e.g. UPDATE=2.6. or UPDATE=26, etc.
- b. By default, a precise interpolation function is selected (EKVINT=0). A simple interpolation function (see “Normalized currents and interpolation function” on page 15-12) can be chosen for analytical purposes (EKVINT=1).
- c. **NQS**=1 switches Non-Quasi-Static operation on, default is off; see 15-21.
- d. Only used for operating point information; see 15-25.
- e. When $XQC \leq 0.5$, this selects the Charge model. When $XQC > 0.5$, this selects the capacitance mode.

Nr.	Name	Description	Default	Units
Process Related Parameters				
7	COX	Gate oxide capacitance per unit area	7.0×10^{-4}	Fm^{-2}
8	TOX	Oxide thickness (For v2.6 revision 2)		m
9	NSUB	Channel doping (For v2.6 revision 2)		cm^{-3}
10	XJ	Junction depth	0.1×10^{-6}	m
11	DW^a	Channel width correction	0	m
12	DL	Channel length correction	0	m

Nr.	Name	Description	Default	Units
13	XL	Etching effects on length	0	m
14	XW	Etching effects on width	0	m
15	LD^b	Diffusion length parameter	0	
16	WD	Diffusion width parameter	0	
17	LMLT	Length multiplier	1.0	
18	WMLT	Width multiplier	1.0	
Basic Model Parameters				
19	VTO (VT0)	Long-channel threshold voltage	0.5	V
20	VFB	Flat-band voltage		V
21	GAMMA	Body effect parameter	1.0	V ^{1/2}
22	PHI	Bulk Fermi potential (*2)	0.7	V
23	KP	Transconductance parameter	50×10 ⁻⁶	AV ⁻²
24	E0^c (EO)	Mobility reduction coefficient (EKV v2.6)	1.0×10 ⁶	Vm ⁻¹
25	THETA	Mobility reduction coefficient	0	V ⁻¹
26	UO	Low-field mobility (For v2.6 revision 2)		cm ² (Vs) ⁻¹
27	VMAX	Saturation velocity (For v2.6 revision 2)		ms ⁻¹
28	UCRIT	Longitudinal critical field	2.0×10 ⁶	Vm ⁻¹
Fine Tuning Parameters for Short- and Narrow-Channel Effects				
29	LAMBDA	Depletion length coefficient (channel length mod.)	0.5	
30	WETA	Narrow channel effect coefficient	0.25	
31	LETA	Short channel effect coefficient	0.1	
Reverse Short Channel Effect Parameters (version≥2.5)				
32	Q0 (QO)	Reverse short channel effect peak density	0	Asm ⁻²
33	LK	Reverse short channel effect characteristic length	0.29	m
Impact Ionization Related Parameters				
34	IBA	First impact ionization coefficient	0	m ⁻¹
35	IBB	Second impact ionization coefficient	3.0×10 ⁸	Vm ⁻¹
36	IBN	Saturation voltage factor for impact ionization	1.0	
Intrinsic Model Temperature Parameters				
37	TCV	Threshold voltage temperature coefficient	0.0	V°K ⁻¹

Nr.	Name	Description	Default	Units
38	BEX	Mobility temperature exponent	-1.5	
39	UCEX	Longitudinal critical field temperature exponent	0.8	
40	IBBT	Temperature coefficient for IBB (model version 2.3)	0.0	°K ⁻¹
Matching Parameters (version 2.6 only)				
41	AVTO (AVT0)	Area related threshold voltage mismatch parameter	0.0	Vm
42	AKP	Area related gain mismatch parameter	0.0	m
43	AGAMMA	Area related body effect mismatch parameter	0.0	(V ^{1/2})×m
Noise Parameters				
44	KF	Flicker noise coefficient	0	
45	AF	Flicker noise exponent	1	
46	FLKLEV	Flicker noise model selector		
Gate Overlap Parameters				
47	CGSO (CGS0)	Gate-source overlap capacitance/channel width	0	Fm ⁻¹
48	CGDO (CGD0)	Gate-drain overlap capacitance/channel width	0	Fm ⁻¹
49	CGBO (CGB0)	Gate-bulk overlap capacitance/channel length	0	Fm ⁻¹

- a. **DL** and **DW** parameters generally have a negative value; see effective length and width calculation.
- b. **LD** and **WD** parameters default to 0, however this figure can vary according to the effective length and width calculation equations as shown [15-8](#). Applies only to v2.6 (Revision 4).
- c. **E0** is used for version 2.6 only.

Parameter units

Special care should be taken for all parameters that depend on the length unit chosen (**COX**, **XJ**, **UCRIT**, **DL**, **DW**, etc.). See **SCALM** setup parameter.

Parameter preprocessing (intrinsic parameters initialization, version 2.6 revision 2)

The basic intrinsic model parameters **COX**, **GAMMA**, **PHI**, **VTO**, **KP** and **UCRIT** are related to the fundamental process parameters **TOX**, **NSUB**, **VFB**, **UO**, **VMAX**, respectively, similarly as in early SPICE models. For the purpose of statistical circuit simulation, it is desirable to introduce parameter variations on the level of the latter parameters. These dependencies are also of interest if device scaling is to be analyzed, and are useful when parameter sets should be obtained

from other MOSFET models. Therefore the possibility is introduced to use the following relations:

If COX is not specified, then it is initialized as:

$$\text{For } TOX > 0 \ COX = \epsilon_{ox}/TOX$$

otherwise $COX = \text{default}$

If $GAMMA$ is not specified, then it is initialized as:

$$\text{For } NSUB > 0 \ GAMMA = \frac{\sqrt{2q\epsilon_{si} \cdot (NSUB \cdot 10^6)}}{COX}$$

otherwise $GAMMA = \text{default}$

If PHI is not specified, then it is initialized as:

$$\text{For } NSUB > 0 \ PHI = 2V_t(TNOM) \cdot \ln\left(\frac{NSUB \cdot 10^6}{ni(TNOM)}\right)$$

otherwise $PHI = \text{default}$

If VTO is not specified, then it is initialized as:

$$\text{For } VFB \text{ is specified } VTO = VFB + PHI + GAMMA \cdot \sqrt{PHI}$$

otherwise $VTO = \text{default}$

If KP is not specified, then it is initialized as:

$$\text{For } UO > 0 \ KP = (UO \cdot 10^6) \cdot COX$$

otherwise $KP = \text{default}$

If $UCRIT$ is not specified, then it is initialized as:

$$\text{For } UO > 0, VMAX > 0 \ UCRIT = VMAX/(UO \cdot 10^{-4})$$

otherwise $UCRIT = \text{default}$

If $E0$ is not specified, then a simplified mobility model is used with the parameter $THETA$:

If $THETA$ is specified $E0 = 0$

otherwise $E0 = default$



Note The value zero is given to $E0$ here, indicating that the simplified mobility model is used in conjunction with $THETA$ instead of the standard mobility model.

Notes about parameters

- For parasitic models, EKV uses Eldo MOS common equations with the following default values:
 $ALEV=2$; $ARLEV=2$; $RLEV=2$; $DCAPLEV=2$; $DIOLEV=5$.
- Access resistance related temperature equations have been moved to the common equations; therefore the parameters $TR1$ and $TR2$ become $TDR1$ and $TDR2$ respectively.

10.0 References

Papers on the model and the associated parameter extraction

A detailed description of the theory underlying the EKV model is given in the following literature references:

- [1] C. C. Enz, F. Krummenacher and E. A. Vittoz: "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications," accepted for publication in the special issue of the AICSP on Low-Voltage and Low-Power Circuits, to be issued July, 1995.

Considerations on parameter extraction can be found in the following literature references:

- [2] C. C. Enz, M. Bucher, F. Krummenacher: "A Simple MOS Transistor Model for Low-Voltage and Low-Current Analog Circuits Design and Simulation," European Hewlett-Packard IC-CAP Users Meeting, 10-11 Oct. 1994.
- [3] G. A. S. Machado, C. C. Enz, M. Bucher: "Estimating key parameters for the EKV MOST Model for Analogue Circuits Design and Simulation," International Circuits and Systems Conference ISCAS'95.

Chapter 16

MISNAN Equations

1.0 Introduction

MISNAN is a physically-based, continuous, scalable, quasi-static model of the MOSFET. With a single set of model parameters, it is capable of accurate representation of electrical characteristics for device structures ranging from long-channel to minimum channel length for a given processing technology. Being physically-based and scalable, the model can be applied effectively for statistical modeling purposes. MISNAN was developed by Nortel (formerly Northern Telecom/Bell Northern Research) in Ottawa, Canada.

The model is continuous in the sense that the same defining relationships are used for all conditions of operation: matching of relationships between ‘operating regions’ does not arise, which is particularly important for analog simulation applications. The basic current transport equation for the channel is expressed in terms of the semiconductor surface potential at its source and drain boundaries, determined for each bias point by solution of the ‘surface equation’—an approach originated by Y.A. El-Mansy [1].

The model is charge-defined, with incremental capacitances consistent with stored charges for all operating conditions; it is charge-conserving. A sheet-charge channel transport relationship incorporates dependence of the carrier mobility on gate oxide electric field and longitudinal field. Saturation mode operation is specified through a condition that expresses the limitation of the gradual channel approximation at the drain end of the channel, and invokes a ‘rectangular box’ representation of the drain space-charge region [2]. The stored charge/capacitance model involves partitioning of the total channel charge between source and drain terminals: this is carried out on the basis of equal channel volume lumps adjacent to the source and drain boundaries.

Temperature effects in the model are represented via temperature dependence of low-field mobility and scatter-limited carrier velocity (also of surface trap density in the case of the noise model) as well as the pervasive influence of thermal voltage.

Modeling of source and drain junction diodes recognizes separate injection and generation/recombination components of current, and separate components of junction capacitance, for the junction planar area and for the gate and field oxide peripheries.

Asymmetry of the device structure is provided for in regard to values of sideways diffusion length of source and drain (gate overlap), source and drain series resistances, and fringing capacitances between gate and source or drain.

For a detailed presentation of the physical basis and analytical relationships of MISNAN, see [3]. The noise model is based on the treatment of channel thermal noise and $1/f$ noise given in [4] and [5]. Application of MISNAN for statistical modeling is presented in [6].

The MISNAN model has undergone extensive development and verification over the past 15 years in support of CMOS and BiCMOS technologies for designing high-speed and analog telecommunication products. For the determination of model parameters an automatic extraction system is available.

2.0 Model Inputs

The inputs to the model comprise of the following:

1. Device dimensions (drawn)

L_g gate length

W_g gate width

A_d drain junction area

A_s source junction area

P_d drain junction periphery

P_s source junction periphery.

2. Model parameters (see “[Model Parameters](#)” on page 16-31).

3. Node voltages of the intrinsic MOSFET

V_G gate voltage

V_D drain voltage

V_S source voltage

V_B substrate voltage.

4. Temperature.

Effective channel length L and width W are derived from gate length L_g and width W_g by taking into account drain and source sideways diffusion (lengthwise gate overlap) and bird’s beak inclusion of width in addition to photolithographic corrections to the ‘drawn’ dimensions. The substrate is represented as being of uniform doping density (N_A, N_D) with a surface ‘spike’ of charge included in Q_{ss} .

The intrinsic device model equations are developed for an n-channel MOSFET, and are expressed in terms of normalized voltages (in units of kT/q) referenced to device substrate and flatband condition. For p-channel devices, sign changes are applied to the input node voltages after referencing to substrate and flatband, and corresponding sign changes are applied to currents and stored charges at the output of the model.

3.0 Flatband Voltage

For the basic MOS structure (large area substrate with oxide and gate), the normalized flatband voltage is:

$$U_{FB0} = \Phi_g - \frac{Q_{ss}}{C_{ox}} \cdot \frac{q}{kT} - U_F = V_{FB0} \cdot \frac{q}{kT}$$

where Φ_g is the gate Fermi potential, Q_{ss} is the effective gate oxide interface charge/unit area, C_{ox} is the oxide capacitance/unit area, and U_F is the normalized Fermi voltage of the substrate given by:

$$U_F = \ln(N_A/n_i)$$

where n_i is the intrinsic carrier density in silicon.

The gate oxide capacitance C_{ox} is given by:

$$C_{ox} = \epsilon_{ox}/t_{ox}$$

where t_{ox} is the gate oxide thickness.

Short and narrow channel effects are represented as modifications ΔU_{FB} of U_{FB0} to give the “effective” flatband voltage reference U_{FB} used for defining the gate voltage variable of the model:

$$U_{FB} = U_{FB0} + \Delta U_{FB}$$

4.0 Normalized Voltage Variables

The drain, source and gate voltages are referenced to the device substrate and normalized in units of kT/q as follows:

$$X_d = (V_D - V_B) \cdot \frac{q}{kT}$$

$$X_s = (V_S - V_B) \cdot \frac{q}{kT}$$

$$U_g = (V_G - V_B) \cdot \frac{q}{kT} - U_{FB}$$

5.0 Basic Device Quantities

The analytical relationships of the model are expressed in terms of the following basic quantities:

$$a = C_{ox} \cdot \sqrt{\frac{kT}{q} \cdot \frac{1}{2\epsilon_s q N_A}}$$

$$A_1 = \frac{1}{2a^2}$$

$$U_{sm} = U_g + A_1 - \sqrt{A_1(2U_g + A_1)}$$

where U_{sm} is the “maximum surface potential” with respect to bulk substrate and flatband reference for a given U_g (corresponding to the pinch-off condition with no surface inversion charge).

6.0 Short- and Narrow-Channel Effects

6.1 Short-channel effect

This is represented as a combination of the charge sharing approach of Yau [7] and the “box analysis” approach of Ratnakumar and Meindl [8]. The flatband voltage modification due to the short-channel effect is:

$$\Delta U_{FBS} = \frac{q}{kT} \cdot \frac{2K_1 \exp\left(-\frac{\pi L}{4d}\right)}{d} \cdot \frac{\Delta Q_S + \Delta Q_D}{C_{ox}WL}$$

where:

$$d = \sqrt{\frac{kT}{q} \cdot \frac{4K_2 \epsilon_s U_F}{q N_A}}$$

and K_1, K_2 are fitting parameters with unity default values. The depletion charges $\Delta Q_S, \Delta Q_D$ ‘lost’ due to two-dimensional charge sharing at the source and drain ends of the channel are:

$$\Delta Q_S = -\frac{qN_A Wr_j W_{dS}}{2} \cdot \left(\sqrt{1 + \frac{2W_{dS}}{r_j}} - 1 \right)$$

$$\Delta Q_D = -\frac{qN_A Wr_j W_{dD}}{2} \cdot \left(\sqrt{1 + \frac{2W_{dD}}{r_j}} - 1 \right)$$

where r_j is the junction radius and W_{dS}, W_{dD} are approximations to the depletion layer radial thickness at source and drain:

$$W_{dS} = \sqrt{\frac{2\varepsilon_s}{qN_A} \cdot \left[\frac{kT}{q} \cdot (1.5U_F + 0.275) + V_{SB} \right]}$$

$$W_{dD} = \sqrt{\frac{2\varepsilon_s}{qN_A} \cdot \left[\frac{kT}{q} \cdot (1.5U_F + 0.275) + V_{DB} \right]}$$

6.2 Narrow-channel effect

The modification of flatband voltage is:

$$\Delta U_{FBn} = -\frac{q}{kT} \cdot \frac{2\Delta Q}{C_{ox}WL} \cdot K_3$$

where ΔQ is the fringing depletion layer charge at each width edge of the channel, the value of which is represented as dependent on the surface potential distribution along the channel, and K_3 is a fitting parameter with unity default value. With the surface potential distribution modeled as parabolic between the source and drain boundary values, the fringing depletion layer charge is:

$$\Delta Q = -2\varepsilon_s L \frac{kT}{q} \left[\tilde{U}_{ss} + (\tilde{U}_{sm} - \tilde{U}_{ss}) \left(1 - \frac{2}{3} \cdot \frac{1-f^3}{1-f^2} \right) \right]$$

where:

$$\tilde{U}_{ss} = X_s + 2U_F$$

$$\tilde{U}_{sm} = \tilde{U}_g + A_1 - \sqrt{A_1 \cdot (2\tilde{U}_g + A_1)}$$

$$\tilde{U}_g = (V_G - V_{FB}) \cdot \frac{q}{kT} - (U_{FB0} + \Delta U_{FBs})$$

$$f = \exp\left(-\frac{X_d - X_s}{\tilde{U}_{sm} - \tilde{U}_{ss}}\right)$$

6.3 Effective flatband voltage

The effective flatband voltage includes the short-channel and narrow-channel effects and is given by:

$$U_{FB} = U_{FB0} + \Delta U_{FBs} + \Delta U_{FBn}$$

7.0 Boundary Surface Potential

Under all operating conditions, the relationships of the model are defined in terms of the normalized surface potentials U_{ss} , U_{sd} at the source and drain boundaries of the channel. These potentials are determined on the basis of the gradual channel approximation by solution of the classical one-dimensional “surface equation” (Gauss’ law applied normal to the silicon surface), with the assumptions of the complete depletion approximation and operation sufficiently above the flatband condition for the effect of majority carriers to be negligible. Under these conditions the surface equation is:

$$\exp(U_s - \zeta - 2U_F) = a^2 \cdot (U_g - U_s)^2 - U_s$$

where:

$$\zeta = X_s, X_d$$

The surface equation is solved numerically for the source and drain boundaries of the channel by applying two Newton-Raphson steps to the following ‘initial guess’ U_{si} :

$$\text{i. } U_{sm} \leq \zeta + 2U_F$$

$$U_{si} = U_{sm}$$

$$\text{ii. } U_{sm} > \zeta + 2U_F$$

$$U_{si} = \zeta + 2U_F + \max(\ln(m), 0)$$

where:

$$m = a^2 \cdot (U_g - \zeta - 2U_F)^2 - (\zeta + 2U_F)$$

and $\max(x,y)$ signifies the larger value of x and y .

The initial guess U_{si} is a continuous function of U_g .

Second-order Newton-Raphson improvement is expressed by:

$$U_s^{j+1} = U_s^j - \frac{F}{F'} \cdot \left[1 - \frac{FF''}{2(F')^2} \right]$$

where:

$$F = a^2(U_g - U_s)^2 - U_s - F_e$$

$$F' = \frac{\partial F}{\partial U_s} = -2a^2(U_g - U_s) - 1 - F_e$$

$$F'' = \frac{\partial^2 F}{\partial U_s^2} = 2a^2 - F_e$$

with:

$$F_e = \exp(U_s - \zeta - 2U_F)$$

This procedure gives U_s as a continuous function of U_g since two Newton-Raphson steps are always applied.

8.0 Boundary Charge Densities

The channel is represented by a sheet channel model for which, on the basis of the gradual channel and complete depletion approximations, the semiconductor (substrate), depletion layer, and mobile charge densities Q_s , Q_{dep} , Q_m per unit area are:

$$Q_s = -C_{ox}(U_g - U_s) \cdot \frac{kT}{q}$$

$$Q_{dep} = -\sqrt{2\varepsilon_s q N_A U_s \cdot \frac{kT}{q}}$$

$$Q_m = Q_s - Q_{dep}$$

The drain current and the stored charges in the intrinsic device are expressed in terms of these charge densities for the boundary values of U_s .

9.0 Drain Current

For the sheet charge model, the drain current is given by:

$$I_D = \frac{W}{L}\mu_{eff} \left[\frac{kT}{q}(Q_{md} - Q_{ms}) + \frac{1}{2C_{ox}}(Q_{ss}^2 - Q_{sd}^2) + \frac{1}{3\varepsilon_s q N_A}(Q_{depd}^3 - Q_{deps}^3) \right]$$

The first term in the above equation represents diffusion current, the others drift current.

μ_{eff} is the effective mobility of the channel which depends on both the longitudinal and the normal (gate) electric field (see section 10.0).

The above value of I_D corresponds to the classical long channel device. It is modified when the device operates in the saturation mode (see sections 11.0 & 12.0).

10.0 Mobility Model

The effective mobility μ_{eff} represents electric field effects in the channel on the basis of addition of carrier scattering rates associated with the longitudinal and normal field effects. Normalizing with respect to the low-field mobility μ_0 , μ_{eff} is defined as follows:

$$\frac{\mu_0}{\mu_{eff}} = F_F = 1 + (F_L - 1) + (F_G - 1)$$

where, representing longitudinal field effects alone,

$$F_L = (1 + h^n)^{\frac{1}{n}}$$

$$h = \frac{kT}{q} \cdot \frac{\mu_0}{v_0} \cdot \frac{(U_{sd} - U_{ss})}{L}$$

and representing normal gate-field effects alone,

$$F_G = 1 + K_g \cdot \frac{\left(U_g - \frac{U_{sd} + U_{ss}}{2} \right)}{t_{ox}} \cdot \frac{kT}{q}$$

In these expressions, v_0 is the scatter-limited velocity of carriers and t_{ox} the oxide thickness. The mobility is thus characterized by four parameters, μ_0 , v_0 , n and K_g , which are chosen to fit DC characteristic data in the parameter extraction procedure.

Used in the saturation region model of section 12.0 are the following derivatives:

$$S_L = \frac{dF_L}{dU_{sd}} = \frac{kT}{q} \cdot \frac{\mu_0}{\nu_0} \cdot \frac{h^{n-1}}{L(1+h^n)^{1-\frac{1}{n}}}$$

$$S_G = \frac{dF_G}{dU_{sd}} = -\frac{kT}{q} \cdot \frac{K_g}{2t_{ox}}$$

$$S_F = \frac{dF_F}{dU_{sd}} = S_L + S_G$$

11.0 Saturation Condition

Saturation region operation is defined in terms of a ‘saturation reference condition’ which specifies operating bias conditions for which the gradual channel approximation may be regarded as valid along the entire channel between source and drain boundaries, with the drain current given by the I_D expression of section 9.0. A reference value U_{sdr} of the normalized drain surface potential is defined as representing the maximum value of the ratio of longitudinal-to-normal electric field at the drain boundary for the gradual channel approximation to apply. For larger values of U_{sd} (i.e. $U_{sd} > U_{sdr}$), the device is considered to be in saturation and the saturation region model of section 12.0 comes into play. The saturation reference potential is specified as follows:

$$U_{sdr} = U_{ss} + \frac{U_{sm} - U_{ss}}{1.05 + \frac{t_{ox}}{L} \cdot [\alpha + \beta \sqrt{a} \cdot (U_{sm} - U_{ss})]}$$

where the controlling parameters α , β are normally set at default values of:

$$\alpha = 5.0$$

$$\beta = \sqrt{1/8}$$

12.0 Saturation Region Model

If $U_{sd} > U_{sdr}$, the saturation model is invoked. A space charge region, represented by a ‘rectangular box model’, is formed at the drain end of the channel, shortening the classical channel length to L' . At the saturation reference condition ($U_{sd} = U_{sdr}$), $L' = L$ and the drain current is I_{Dr} , evaluated from the I_D expression of section 9.0. For $U_{sd} > U_{sdr}$, $L' < L$ and $I_D > I_{Dr}$. Analysis of the drain space charge region model gives a solution for I_D in the form:

$$I_D = I_{Dr} \cdot \exp(M_1) \cdot \exp(M_2)$$

where at the saturation reference condition: $M_1 = M_2 = 0$

With practical device structures, $M_2 \ll 1$ under all operating conditions, and with negligible error:

$$I_D = I_{Dr} \cdot \exp(M_1) \cdot (1 + M_2)$$

This expression for I_D is implemented in MISNAN.

The rectangular box model of the drain space charge region allows an “average” doping density to be specified as $R_{dop} N_A$ where R_{dop} is a “doping ratio” parameter. The charge of mobile carriers in this region, the effect of which becomes significant at high drain current values, is taken into account in the analysis of the space charge region model and influences the depth x_D of the rectangular box below the silicon surface; this depth is as follows:

$$x_D = x_T \left(\sqrt{b_m^2 + \frac{1}{R_{dop}}} - b_m \right)$$

where:

$$x_T = 2 \cdot \frac{\epsilon_s}{\epsilon_{ox}} \cdot t_{ox} \cdot \frac{U_{sm}}{U_g - U_{sm}}$$

and:

$$b_m = \frac{1}{R_{dop}} \cdot \frac{I_{Dr}}{2qv_0WN_Ax_T}$$

12.1 Function M_1

The function M_1 takes the form:

$$M_1 = \frac{F_{Gr}}{F_{Fr}} \cdot \frac{1}{L} \cdot f$$

where F_{Gr}, F_{Fr} are the values of F_G, F_F at the saturation reference condition where $U_{sd} = U_{sdr}$. The function f is defined as:

$$f = \frac{1}{D} \cdot \int_{1/D}^{\theta} \left[\frac{1}{x \cdot \sqrt{k_1 x^2 + k_2 x + k_3}} \right] dx$$

where:

$$D = \frac{1}{F_{Fr}} \left[S_{Lr} - \left(\frac{F_{Lr} - 1}{F_{Gr}} \right) S_{Gr} \right]$$

$$\theta = U_{sd} - U_{sdr} + \frac{1}{D}$$

$$k_1 = \frac{1}{t_{ox}x_D} = \frac{C_{ox}}{\varepsilon_{ox}x_D}$$

$$k_2 = B - \frac{2k_1}{D}$$

$$k_3 = C - \frac{B}{D} + \frac{k_1}{D^2}$$

$$\text{and: } C = \left(\frac{q}{kT} \cdot \frac{1}{L} \cdot \frac{F_{Gr}}{\frac{g_{dr}}{I_{Dr}} \cdot \frac{F_{Fr}}{F_{dr}} + \frac{q}{kT} \cdot S_{Gr}} \right)^2$$

while:

$$B = 2C \left[P_1 - P_4 \left(P_1 + P_2 - \frac{S_{Fr}}{F_{Fr}} \right) \cdot \frac{S_{Gr}}{F_{Gr}} + P_2 - P_3 D - \frac{P_1 P_3 P_4}{F_{dr} g_{dr}} \cdot S_{gdr} \right]$$

where:

$$P_1 = \frac{g_{dr}}{F_{dr} I_{Dr}} \cdot \frac{kT}{q}$$

$$P_2 = \frac{1 - F_{dr}}{F_{dr} (U_{sm} - U_{sdr})}$$

$$P_3 = \frac{F_{Fr}}{F_{Gr}}$$

$$P_4 = L \sqrt{C}$$

$$\text{and: } F_{dr} = \frac{dU_{sd}}{dX_d} \Big|_r = \frac{\eta_{dr}^2 + \frac{\eta_{dr}}{a} - U_g}{\eta_{dr}^2 + \left(2a + \frac{1}{a}\right)\eta_{dr} + 1 - U_g}$$

$$\text{with: } \eta_{dr} = a(U_g - U_{sdr})$$

while:

$$S_{gdr} = \frac{dg_d}{dX_d} \Big|_r = \frac{1}{F_{Fr}} \left[-\frac{\mu_0 W}{L} F_{dr} \cdot \frac{kT}{q} C_{ox} \left(1 + \frac{\varepsilon_s N_A}{C_{ox}} \cdot \frac{1}{-Q_{depdr}} \right) - (1 + F_{dr}) S_{Fr} g_{dr} \right]$$

The quantities I_{Dr} , Q_{depdr} follow from the channel region expressions of sections 9.0 and 10.0 at the saturation reference condition. The drain conductance g_{dr} of the channel region is:

$$g_{dr} = \frac{1}{F_{Fr}} \left\{ -\frac{\mu_0 W}{L} \left[Q_{mdr} + \frac{kT}{q} \left(\frac{q\varepsilon_s N_A}{Q_{depdr}} - C_{ox} \right) \right] - I_{Dr} F_{dr} S_{Fr} \cdot \frac{q}{kT} \right\}$$

The above expression for B is derived from the consideration of continuity of drain conductance g_d through the saturation reference condition.

The integral f is given by the following closed form expressions:

$$f = \frac{1}{D\sqrt{k_3}} \cdot \ln \left[\frac{\sqrt{k_1 + k_2 D + k_3 D^2} + D\sqrt{k_3} + \frac{k_2}{2\sqrt{k_3}}}{\frac{\sqrt{k_1 z^2 + k_2 z D + k_3 D^2} + D\sqrt{k_3} + \frac{k_2}{2\sqrt{k_3}}}{z}} \right] \quad \text{for } k_3 \geq 0$$

where: $z = 1 + D(U_{sd} - U_{sdr})$

or:

$$f = \frac{1}{D\sqrt{-k_3}} \cdot \left[\operatorname{asin} \left(\frac{k_2 z + 2k_3 D}{z\sqrt{k_2^2 - 4k_1 k_3}} \right) - \operatorname{asin} \left(\frac{k_2 + 2k_3 D}{\sqrt{k_2^2 - 4k_1 k_3}} \right) \right] \quad \text{for } k_3 < 0$$

In the first expression for $f(k_3 \geq 0)$, the quantities $\sqrt{k_1 + k_2 D + k_3 D^2}$ and $\sqrt{k_1 z^2 + k_2 z D + k_3 D^2}$ as they stand cause numerical problems for z approaching 1 when the device operates in deep threshold, the quantities underneath the $\sqrt{}$ being expressed as the difference between two almost equal terms. This difficulty is eliminated when the expressions for k_1 , k_2 , k_3 above are substituted, giving:

$$\sqrt{k_1 + k_2 D + k_3 D^2} = D\sqrt{C}$$

$$\text{and: } \sqrt{k_1 z^2 + k_2 z D + k_3 D^2} = D \sqrt{C} \cdot \sqrt{\frac{k_1 u^2}{CD^2} + \frac{B}{C} u + 1}$$

where: $u = z - 1$

12.2 Function M_2

$$M_2 = \frac{1}{F_{Fr}} \cdot \frac{kT}{q} \cdot \frac{K_g}{2t_{ox}} (w + \gamma w^2)$$

where:

$$w = (U_{sm} - U_{sdr}) \left[1 - \exp\left(-\frac{U_{sd} - U_{sdr}}{U_{sm} - U_{sdr}}\right) \right]$$

$$\gamma = \frac{0.75 \cdot K_{sat}}{U_{sm} - U_{sdr}}$$

and K_{sat} is a fitting parameter with default value 1.0.

13.0 Model in Deep Subthreshold

For channel boundary surface potentials such that $(X + 2U_F) - U_s \gg 1$, where $X = X_s, X_d$, the definition of Q_m involves the difference between two almost equal quantities Q_{dep} and Q_s (see section 8.0). Under these conditions, referred to here as ‘deep subthreshold’, to circumvent numerical problems Q_m is expressed analytically with respect to the value at a reference ‘limit’ condition defined as:

$$U_{sl} = X_s + 2U_F - N$$

$$U_{gl} = U_{sl} + \frac{\sqrt{U_{sl} + e^N}}{a}$$

From considerations of numerical accuracy in implementation, $N = 3$ is chosen.

For $U_s < U_{sl}$, an accurate approximate expression for U_s , derived from the surface equation of section 7.0 is as follows:

$$U_s = U_{sm} - \Delta U_{sm}$$

where:

$$\Delta U_{sm} = \frac{\exp(U_{sm} - X - 2U_F)}{2a^2(U_g - U_{sm}) + 1}$$

The channel charge density Q_m at source or drain boundary is derived as:

$$Q_m = Q_{ml} \left[\exp(U_{sm} - U_{sml}) \cdot \sqrt{\frac{U_{sml}}{U_{sm}}} \right]$$

where:

$$U_{sml} = U_{gl} + A_1 - \sqrt{A_1(2U_{gl} + A_1)}$$

The drain current is calculated on the basis that the drift current component of channel current and the electric field dependence of channel mobility are negligible, giving:

$$I_D = I_{Dl} \cdot \exp(U_{sm} - U_{sml}) \cdot \sqrt{\frac{U_{sml}}{U_{sm}}}$$

Q_{ml} and I_{Dl} are the values calculated at the ‘limit’ condition from the relationships of sections 7.0 & 8.0.

14.0 Stored Charges

14.1 Intrinsic long-channel MOSFET

Quasi-static stored charges are formulated as follows:

$$Q_G = WC_{ox} \cdot \frac{kT}{q} \int_0^L [U_g - U_s(y)] dy$$

$$Q_S = W \int_0^{L/2} Q_m(y) dy$$

$$Q_D = W \int_{L/2}^L Q_m(y) dy$$

$$Q_B = -Q_G - Q_S - Q_D$$

where y is the position along the channel from the source boundary reference and $Q_m(y)$ is defined in terms of $U_s(y)$ as in section 8.0.

Analytical relationships for the stored charges are obtained by expressing $U_s(y)$ as a parabolic distribution between the known boundary values U_{ss} at $y = 0$ and U_{sd} at $y = L$:

$$U_s = U_{sm} - \sqrt{\frac{y_m - y}{K_y}}$$

where:

$$y_m = \frac{L}{1 - \left(\frac{U_{sm} - U_{sd}}{U_{sm} - U_{ss}} \right)^2}$$

$$K_y = \frac{L}{(U_{sm} - U_{ss})^2 - (U_{sm} - U_{sd})^2}$$

$$\text{Then, } Q_G = WLC_{ox} \cdot \frac{kT}{q} \left[U_g - U_{sm} + \frac{2}{3}(U_{sm} - U_{ss}) \cdot \frac{1-f^3}{1-f^2} \right]$$

$$\text{where: } f = \frac{U_{sm} - U_{sd}}{U_{sm} - U_{ss}}$$

The total channel charge is defined as follows:

$$Q_M = -Q_G - Q_{DEP}$$

where:

$$Q_{DEP} = -WL \sqrt{2\epsilon_s q N_A \cdot \frac{kT}{q}} \cdot \frac{\left(\frac{U_{sm}}{3} - \frac{U_{sd}}{5}\right) \cdot U_{sd}^{\frac{3}{2}} - \left(\frac{U_{sm}}{3} - \frac{U_{ss}}{5}\right) \cdot U_{ss}^{\frac{3}{2}}}{(U_{sm} - U_{ss})^2 \cdot (1-f^2)}$$

The partitioning of Q_M into source and drain components Q_S, Q_D is by analytical approximation to the above integral expressions:

$$Q_S = Q_M \cdot \frac{Q_{ms} + Q_{md} + F_p \left(\frac{Q_{ms} - Q_{md}}{2} \right)}{Q_{ms} + 3Q_{md} + F_p(Q_{ms} - Q_{md})}$$

$$Q_D = Q_M - Q_S$$

$$\text{where: } F_p = 1 - 1.35 \left(\frac{Q_{ms} - Q_{md}}{Q_{ms}} \right)^{\frac{5}{2}}$$

14.2 Intrinsic MOSFET with short-channel effects

Due to the surface potential distribution in the drain and source space charge regions at the ends of the channel, the stored charges above for the ideal long-channel device are modified to the following “intrinsic device” values:

$$Q_{Gi} = Q_G - Q_{SSc} - Q_{Dsc}$$

$$Q_{Si} = Q_S + Q_{SSc}$$

$$Q_{Di} = Q_D + Q_{Dsc}$$

where, with:

$$U_{J0} = 0.55 \cdot \frac{q}{kT} + U_F$$

$$U_{JS} = X_s + U_{J0}$$

$$U_{JD} = X_d + U_{J0}$$

$$Q_{SSc} = A_4 \left(U_{JS}^{\frac{3}{2}} - U_{J0}^{\frac{3}{2}} \right)$$

$$Q_{Dsc} = A_4 \left(U_{JD}^{\frac{3}{2}} - U_{J0}^{\frac{3}{2}} \right)$$

and:

$$A_4 = \frac{kT}{q} \cdot \frac{WC_{ox}}{3} \sqrt{\frac{kT}{q} \cdot \frac{\varepsilon_s}{0.699qN_A} \cdot K_{sc}}$$

where K_{sc} is a fitting parameter with a default value of 1.0.

14.3 Deep subthreshold operation

For operation in deep subthreshold, when $U_g < U_{gl}$, the stored charges of the intrinsic MOSFET are modified as follows:

(i) For $0 \leq U_g < U_{gl}$:

$$Q_{Gi} = Q_{Gil} + \frac{C_{ox}}{a} \cdot \frac{kT}{q} \cdot (\eta_m R - \eta_{ml} R_l) - (Q_{Sil} + Q_{Dil})(M - 1)$$

where:

$$\eta_m = a(U_g - U_{sm})$$

$$\eta_{ml} = a(U_g - U_{sml})$$

$$M = \exp(U_{sm} - U_{sml})$$

and:

$$R = 1 - \frac{\Delta_{sl} + \Delta_{dl}}{4U_{sml}} \cdot M$$

$$R_l = 1 - \frac{\Delta_{sl} + \Delta_{dl}}{4U_{sml}}$$

where:

$$\Delta_{sl} = U_{sml} - U_{ssl}$$

$$\Delta_{dl} = U_{sml} - U_{ndl}$$

while:

$$Q_{Si} = Q_{Sil} \cdot M$$

$$Q_{Di} = Q_{Dil} \cdot M$$

and Q_{Gil} , Q_{Sil} , Q_{Dil} are the values calculated at the ‘limit’ condition.

(ii) For $U_g \leq 0$:

$$Q_{Gi} = Q_{Gi}|_{U_g=0} + C_{ox}WL \cdot \frac{kT}{q} U_g$$

$$Q_{Si} = Q_{Si}|_{U_g=0}$$

$$Q_{Di} = Q_{Di}|_{U_g=0}$$

14.4 Representation of MOS capacitor behavior in the vicinity of flatband

In order to model charge storage and capacitance behavior in the vicinity of flatband it is necessary to represent the effects of majority carriers (which are not included in the surface equation of section 7.0, and in the relationships presented so far). With the above definition of gate charge Q_{Gi} , MISNAN gives a gate capacitance that rises to C_{ox} per unit gate area as U_g approaches 0 (flatband), and is constant at this value for $U_g < 0$. The effect of majority carriers is represented by adding the charge Q_{Gdif} to Q_{Gi} and $-Q_{Gdif}$ to Q_{Bi} , where:

$$Q_{Gdif} = C_{dif}U_r \left[1 - \exp\left(\frac{U_g}{U_r}\right) \right]$$

with:

$$C_{dif} = C_{ox}WL - C_{g0}$$

$$C_{g0} = \frac{C_{ox}WL}{1 + \sqrt{2} \cdot a}$$

and:

$$U_r = \frac{C_{dif}}{S_{g0} - S_{00}}$$

$$S_{00} = -\frac{C_{g0}}{3} \left(1 - \frac{C_{g0}}{C_{ox}WL}\right)^2$$

while:

$$S_{g0} = -2a^2 C_{ox} WL \text{ for } U_g \geq 0$$

$$S_{g0} = 0 \text{ for } U_g < 0$$

With Q_{Gdif} added to Q_{Gi} of section 14.3, the corresponding gate capacitance:

$$\frac{\partial}{\partial V_G} (Q_{Gi} + Q_{Gdif})$$

is a good approximation to the classical MOS capacitance, with the value C_{g0} at flatband and continuity through the flatband condition.

14.5 Extrinsic stored charges

Added to the above stored charges are charge contributions corresponding to gate overlap capacitance and fringing capacitance at the ends of the channel, and capacitance due to width extensions of the gate in the taper transitions to field oxide. The additional extrinsic charges are:

$$Q_{Gext} = -Q_{Sext} - Q_{Dext} + \frac{kT}{q} \cdot (U_g - U_{FB0}) \cdot 2L \left(\frac{C_{ox} + C_{pts}}{2} \right) \Delta W_{gt}$$

$$Q_{Sext} = -\frac{kT}{q} \cdot (U_g - U_{FB0} - X_s) \cdot W(C_{ox} \Delta L_s + C_{frs})$$

$$Q_{Dext} = -\frac{kT}{q} \cdot (U_g - U_{FB0} - X_d) \cdot W(C_{ox} \Delta L_d + C_{frd})$$

where:

- i. $\Delta L_s, \Delta L_d$ are the gate overlap distances at source and drain respectively (in general specified as unequal).
- ii. C_{frs}, C_{frd} are the fringing capacitances, per unit gate width, at the source and drain ends respectively of the gate (i.e. beyond the gate overlap regions).
- iii. C_{pts} is the capacitance per unit area between gate poly and substrate over the gate-to-field oxide transition at the edge of the gate, and ΔW_{gt} is the width of this transition along the length edges of the gate.

15.0 Junction Diodes

Source and drain junction diode models represent components of current flow for the mechanisms of carrier injection and generation/recombination. These current components, together with stored charges, are modeled for the junction area, junction periphery under gate oxide and junction periphery under field oxide.

The following expressions apply for the source-substrate junction diode.

The current flowing substrate-to-source is:

$$I_{BS} = I_{IS} + I_{GRS}$$

where the injection component is:

$$I_{IS} = I_{IS0}[\exp(-X_s) - 1]$$

with:

$$I_{IS0} = A_s I_{i0} + P_{gs} I_{ig0} + P_{fs} I_{if0}$$

and the generation/recombination component is:

$$I_{GRS} = I_{GRS0} \left[\exp\left(-\frac{X_s}{2}\right) - 1 \right]$$

with:

$$I_{GSR0} = A_s I_{gr0} + P_{gs} I_{grg0} + P_{fs} I_{grf0}$$

The various quantities in these current expressions are as follows:

A_s	source junction area
P_{gs}	source junction periphery under gate oxide
P_{fs}	source junction periphery under field oxide
I_{i0}	injection saturation current per unit junction area
I_{ig0}	injection saturation current per unit length of periphery under gate oxide
I_{if0}	injection saturation current per unit length of periphery under field oxide
I_{gr0}	generation/recombination saturation current per unit junction area
I_{grg0}	generation/recombination saturation current per unit length of periphery under gate oxide
I_{grf0}	generation/recombination saturation current per unit length of periphery under field oxide.

The component of substrate charge for the source junction diode is defined in terms of the junction capacitance C_{BS} :

$$C_{BS} = C_{BS0} \frac{1}{\left(1 + \frac{X_s}{U_{J0}}\right)^{N_s}}$$

where:

$$U_{J0} = 0.55 \cdot \frac{q}{kT} + U_F$$

$$C_{BS0} = A_{as} C_{j0} + P_{gs} C_{jg0} + P_{fs} C_{jf0}$$

$$N_s = \frac{N_a A_{as} C_{j0} + N_g P_{gs} C_{g0} + N_f P_{fs} C_{f0}}{C_{BS0}}$$

and:

C_{j0} zero bias junction capacitance per unit area

C_{jg0} zero bias junction capacitance per unit length of gate-oxide periphery

C_{jf0} zero bias junction capacitance per unit length of field-oxide periphery

N_a junction capacitance coefficient for area component

N_g junction capacitance coefficient for gate-oxide periphery component

N_f junction capacitance coefficient for field-oxide periphery component.

The substrate stored charge component is:

$$Q_{BS} = -\frac{kT}{q} U_J \left(\frac{C_{BS} \left(1 + \frac{X_s}{U_J} \right) - C_{BS0}}{1 - N_s} \right)$$

Corresponding expressions to the above apply with change of subscript from s to d throughout, for the current I_{DB} flowing from substrate to drain and the substrate stored charge Q_{BD} .

The total stored charges for the MOSFET (subscript T) combine the intrinsic and extrinsic components of section 14.0 with those for the junction diodes:

$$Q_{GT} = Q_{Gi} + Q_{Gdif} + Q_{Gext}$$

$$Q_{ST} = Q_{Si} + Q_{Sext} - Q_{BS}$$

$$Q_{DT} = Q_{Di} + Q_{Dext} - Q_{BD}$$

$$Q_{BT} = -Q_{GT} - Q_{ST} - Q_{DT}$$

The intrinsic MOSFET components Q_{Gi} , Q_{Si} , Q_{Di} are as per sections 14.1 & 14.2 for operation at and above the limit condition ($U_g \geq U_{gl}$) and as per section 14.3 for operation in deep subthreshold ($U_g < U_{gl}$).

16.0 Conductances and Capacitances

The basic dependent variables of the model are currents and stored charges. The small-signal conductances and capacitances, also delivered as outputs from the model, are the partial derivatives of currents and charges respectively, and are in general calculated from a combination of analytical expressions, and numerical differences for small increments in the node voltages. As far as possible, unless not computationally expedient from cpu time considerations, analytical expressions for partial derivatives are used.

Outputs from the model are:

(i) Conductances:

$$g_m = \frac{\partial I_D}{\partial V_G}$$

$$g_s = \frac{\partial I_D}{\partial V_S}$$

$$g_d = \frac{\partial I_D}{\partial V_D}$$

$$g_{js} = - \frac{\partial I_{BS}}{\partial V_S}$$

$$g_{jd} = - \frac{\partial I_{BD}}{\partial V_D}$$

(ii) Capacitances:

$$C_{gg} = \frac{\partial Q_{GT}}{\partial V_G}$$

$$C_{gs} = - \frac{\partial Q_{GT}}{\partial V_S}$$

$$C_{gd} = - \frac{\partial Q_{GT}}{\partial V_D}$$

$$C_{sg} = - \frac{\partial Q_{ST}}{\partial V_G}$$

$$C_{ss} = \frac{\partial Q_{ST}}{\partial V_S}$$

$$C_{sd} = - \frac{\partial Q_{ST}}{\partial V_D}$$

$$C_{dg} = - \frac{\partial Q_{DT}}{\partial V_G}$$

$$C_{ds} = - \frac{\partial Q_{DT}}{\partial V_S}$$

$$C_{dd} = \frac{\partial Q_{DT}}{\partial V_D}$$

17.0 Extrinsic Series Resistances

Added to the model as external elements are the source and drain resistances:

$$R_S = R_{WS}/W$$

$$R_D = R_{WD}/W$$

where R_{WS} , R_{WD} are the source and drain resistances for unit channel width.

18.0 Noise Model

The MISNAN noise model represents the channel thermal noise and 1/f noise of the intrinsic MOSFET implemented on the basis of the approaches of [4] and [5]. Thermal noise sources corresponding to the series source and drain resistances R_S and R_D are also included as well as shot noise sources for the junction diodes.

19.0 Equivalence: Model Parameter Symbols & Names

The symbols used in the text and the corresponding model parameter names are listed in order of appearance:

Symbol	Name
Φ_g	PHI
Q_{ss}	QSS
C_{ox}	COX
N_A	DOP
r_j	XJ

Symbol	Name
K_1	SCRAT
K_2	SCIND
K_3	NCRAT
μ_0	MU
K_g	KG
ν_0	V0
n	FIND
α	SADR
β	SBDR
R_{dop}	DOPRAT
K_{sat}	SATPR
K_{sc}	SCCF
C_{frs}	CGFRS
C_{frd}	CGFRD
ΔW_{gt}	WTGF
C_{pts}	CPTS
I_{i0}	IS
I_{ig0}	ISG
I_{if0}	ISF
I_{gr0}	IG
I_{grg0}	IGG
I_{grf0}	IGF
C_{j0}	CJO
C_{jg0}	CJGO
C_{jf0}	CJFO
N_a	ENA
N_g	ENG
N_f	ENF
R_{ws}	RWS
R_{wd}	RWD

20.0 Model Parameters

Name	Description	Default	Units
LEVEL		46	
Intrinsic MOS Parameters			
COX	Gate-oxide capacitance per unit area		F cm ⁻²
DOP	Substrate doping		cm ⁻³
PHI	Gate Fermi potential		V
QSS	Effective gate-oxide charge per unit area		C cm ⁻²
Geometric Parameters			
LVAR	Gate length correction		μm
WVAR	Gate width correction		μm
DLS	Sideways diffusion length of source region	0	μm
DLD	Sideways diffusion length of drain region	0	μm
DL	Sideways diffusion length of source/drain region in a symmetrical device	0	μm
DW	Sideways bird's beak inclusion of channel width		μm
Small-Geometry Threshold Voltage Parameters			
XJ	Source/drain-to-substrate junction depth		μm
SCRAT	Short-channel threshold voltage ratio		
SCIND	Short-channel threshold voltage index		
NCRAT	Narrow-channel threshold voltage ratio		
Mobility Parameters			
MU	Low-field carrier mobility		cm ² (Vs) ⁻¹
MUTXP	Temperature coefficient for carrier mobility		
KG	Gate field factor		cm V ⁻¹
V0	Carrier scatter-limited velocity		cm s ⁻¹
V0TXP	Temperature coefficient of scatter limited velocity		
FIND	Index factor for longitudinal field dependence of mobility		
Saturation Parameters			
DPRAT	Drain space charge region/channel doping ratio		
SATPR	Saturation region shaping factor		
SBDR	Parameter (primary) controlling the onset of saturation	0.353553391	
SADR	Parameter (secondary) controlling the onset of saturation	5.0	
Short-Channel Capacitance Model			

Name	Description	Default	Units
SCCF	Short channel capacitance factor		
Extrinsic MOSFET Parameters			
RWS	Source series resistance for unit channel width	0	$\Omega \mu\text{m}$
RWD	Drain series resistance for unit channel width	0	$\Omega \mu\text{m}$
RSD	Symmetry flag; used also as source/drain resistance for unit channel width in the case of a symmetrical device		$\Omega \mu\text{m}$
WTGF	Width of transition from gate oxide to field oxide under poly		μm
CPTS	Polysilicon-to-substrate capacitance		F cm^{-2}
CGFRS	Fringing field capacitance between gate and source	0	F cm^{-1}
CGFRD	Fringing field capacitance between gate and drain	0	F cm^{-1}
CGFR	Fringing capacitance between gate and source/drain for a symmetrical device	0	F cm^{-1}
Source/Drain Junction Diode Parameters			
IS	Injection saturation current per unit area of source/drain region		A cm^{-2}
ISG	Injection saturation current per unit length of gate-oxide periphery		A cm^{-1}
ISF	Injection saturation current per unit length of field-oxide periphery		A cm^{-1}
IG	Generation/recombination saturation current per unit area of source/drain region		A cm^{-2}
IGG	Generation/recombination saturation current per unit length of gate-oxide periphery		A cm^{-1}
IGF	Generation/recombination saturation current per unit length of field-oxide periphery		A cm^{-1}
CJO	Zero bias junction capacitance per unit area		F cm^{-2}
ENA	Junction capacitance coefficient for area component		
CJGO	Zero bias junction capacitance per unit length of gate-oxide periphery		F cm^{-1}
ENG	Junction capacitance coefficient for gate-oxide periphery component		
CJFO	Zero bias junction capacitance per unit length of field-oxide periphery		F cm^{-1}
ENF	Junction capacitance coefficient for field-oxide periphery component		
Noise Model Parameters			
NT	Surface trap density		cm^{-2}
NTTX	Surface trap density temperature coefficient		
FIDX	1/f noise frequency coefficient		
BETA	Thermal noise proportionality constant		

Name	Description	Default	Units
SGMA	Capture cross-section for carriers at surface		cm ²
XTAU	Characteristic length of trap distribution in gate oxide		cm
WBAR	Barrier height for tunneling		V
DEPT	Maximum depth of traps in gate-oxide		cm

Notes

1. Internally, the model is specified as asymmetrical in regard to values of sideways diffusion length **DLS** and **DLD** of source and drain, source and drain series resistances **RWS** and **RWD** and fringing capacitances **CGFRS** between gate and source and **CGFRD** between gate and drain.

The parameter **RSD** is designated as a “symmetry flag” and must be set to a negative number (e.g. -1) to ensure that, in the general asymmetrical case, the numerical values of **DLS**, **DLD**, **RWS**, **RWD**, **CGFRS**, **CGFRD** are loaded from the model parameter set and used in the simulations. Under these conditions (**RSD** set negative), a device can be made symmetrical by ensuring that **DLS = DLD**, **RWS = RWD** and **CGFRS = CGFRD** in the model parameter set.

Setting **RSD** to a positive number (or zero), the parameters **DLS**, **DLD**, **RWS**, **RWD**, **CGFRS**, **CGFRD** in the model parameter set are ignored and the device is treated as symmetrical. Instead, the parameters **DL**, **RSD** and **CGFR** are used to determine the sideways diffusion lengths, series resistances and fringing capacitances at the source and drain channel ends. The value of **RSD** then signifies also the drain or source series resistance for unit channel width.

2. The effective values of channel length and width are defined as:

$$L = L_{drawn} + LVAR + DLS + DLD$$

$$W = W_{drawn} + WVAR - 2DW$$

3. The parameters **SADR** and **SBDR** control the ‘saturation condition’ which defines the point at which the saturation model is invoked. These model parameters are normally not specified and assume their default values: **SADR** = 5.0, **SBDR** = $(1/8)^{1/2}$ [3].

21.0 References

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Chapter 17

BSIM3v2 Equations

1.0 Introduction

BSIM3 version 2 is a physical model developed by the University of Berkeley (California). It is based on a coherent quasi two-dimensional analysis of the MOSFET device structure, taking into account the effects of device geometry and process parameters. It allows users to accurately model MOSFET behavior for up-to-date submicron technologies.

BSIM3v2 model includes properly such effects as:

- threshold voltage reduction due to short and narrow channel effects
- non-uniform doping effect
- mobility reduction due to vertical field
- carrier velocity saturation
- channel-length modulation (CLM)
- drain induced barrier lowering (DIBL)
- substrate current induced body effect (SCBE)
- subthreshold conduction
- source/drain parasitic resistance effect
- bulk charge effect.

The charge model was derived from its drain-current counterpart to ensure model consistency of device physics. Charge conservation is also guaranteed. Also, three possible drain-source sharings are possible.

2.0 Useful Internal Parameters

2.1 Initialization

If PHI is not given, then it is defined as: $\text{PHI} = 2 \cdot Vt \cdot \ln\left(\frac{\text{NPEAK}}{ni}\right)$

If VBI is not given, then it is defined as: $\text{VBI} = Vt \cdot \ln\left(\frac{ND \cdot \text{NPEAK}}{ni^2}\right)$

If GAMMA1 is not given, then it is defined as:

$$\text{GAMMA1} = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot \text{NPEAK}}}{C_{ox}}$$

If GAMMA2 is not given, then it is defined as:

$$\text{GAMMA2} = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot \text{NSUB}}}{C_{ox}}$$

If VTH0 is not given, then it is defined as: $\text{VTH0} = VFB + \text{PHI} + K1 \cdot \sqrt{\text{PHI}}$

else VFB is defined as: $\text{VFB} = \text{VTH0} - \text{PHI} - K1 \cdot \sqrt{\text{PHI}}$

If LITL is not given, then it is defined as: $\text{LITL} = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} \cdot XJ \cdot TOX}$

If VBX is not given, then it is defined as: $\text{VBX} = \text{PHI} - \frac{q \cdot \text{NPEAK} \cdot XT^2}{2 \cdot \varepsilon_{si}}$

If $K1$ and $K2$ are not given then:

$$K1 = GAMMA2 - 2 \cdot K2 \cdot \sqrt{PHI - VBM}$$

$$K2 = (GAMMA1 - GAMMA2) \cdot \frac{\sqrt{PHI - VBX} - \sqrt{PHI}}{2 \cdot \sqrt{PHI} \cdot (\sqrt{PHI - VBM} - \sqrt{PHI}) + VBM}$$

If $CGDO$ is not specified, it is calculated as follows:

if DL is specified:
 for $DL > 0$ $CGDO = DL \cdot Cox$
 for $DL < 0$ $CGDO = 0$

otherwise: $CGDO = 0.5 \cdot XJ \cdot Cox$

If $CGSO$ is not specified, it is calculated as follows:

if DL is specified:
 for $DL > 0$ $CGSO = DL \cdot Cox$
 for $DL < 0$ $CGSO = 0$

otherwise: $CGDO = 0.5 \cdot XJ \cdot Cox$

2.2 Effective channel length and width

The effective channel length and width are determined as follows:

$$L_{eff} = L \cdot LMLT + XL_{scal} - 2 \cdot DL_{scal}$$

$$W_{eff} = W \cdot WMLT + XW_{scal} - 2 \cdot DW_{scal}$$

3.0 Static Current Equations

3.1 Threshold voltage

The f factor is defined as follows:

$$\text{If } vbs \leq 0 \text{ then } f = \sqrt{PHI - vbs} \text{ otherwise } f = \frac{PHI \cdot \sqrt{PHI}}{PHI + 0.5 \cdot vbs}$$

The threshold voltage Vth is defined as:

$$V_{th} = V_{TH0} + K1 \cdot (f - \sqrt{PHI}) - K2 \cdot vbs + (K3 + K3B \cdot vbs) \cdot \frac{TOX \cdot PHI}{W_{eff} + W0} \\ + K1 \cdot \left(\sqrt{1 + \frac{NLX \cdot \sqrt{PHI}}{L_{eff} \cdot f}} - 1 \right) \cdot \sqrt{PHI} - DV_{th0} + Dv_{th}(T)$$

where:

$$lt = \sqrt{\frac{\epsilon_{si} \cdot TOX \cdot X_{dep}}{\epsilon_{ox}}} \cdot (1 + DVT2 \cdot vbs) \quad X_{dep} = \sqrt{\frac{2 \cdot \epsilon_{si}}{q \cdot NPEAK}} \cdot f$$

$$DV_{th0} = DVT0 \cdot Theta0 \cdot (VBI - PHI)$$

$$Theta0 = \exp\left(-DVT1 \cdot \frac{Leff}{2 \cdot lt}\right) + 2 \cdot \exp\left(-DVT1 \cdot \frac{Leff}{lt}\right)$$

3.2 Poly gate depletion effect

To take into account the Poly Gate-Si Depletion effect, if $NGATE$ is not given, then V_{gseff} is set to vgs , otherwise the effective gate source voltage V_{gseff} is updated as follows:

$$V_{gseff} = VFB + PHI + K \cdot \left(\sqrt{1 + \frac{2 \cdot (vgs - VFB - PHI)}{K}} - 1 \right)$$

$$\text{where: } K = \frac{q \cdot NGATE \cdot \epsilon_{si}}{Cox^2}$$

3.3 Mobility

The effective mobility is defined as: $U_{eff} = \frac{U\theta(T)}{U_{vert}}$

$$\text{where: } V_{gsvth} = V_{gseff} + V_{th}(vds=0)$$

$$U_{vert} = 1 + Ua(T) \cdot \frac{V_{gsvth}}{TOX} + Ub(T) \cdot \left(\frac{V_{gsvth}}{TOX} \right)^2 + Uc(T) \cdot vbs$$

3.4 Drain saturation voltage

We introduce the following parameters:

$$V_{gst} = V_{gs_{eff}} - V_{th}(vds=0) \quad R_{ds} = RDS0 + \frac{RDSW}{Weff}$$

$$Esat = \frac{2 \cdot V_{sat}(T)}{U_{eff}} \quad Rfactor = R_{ds} \cdot Cox \cdot Weff \cdot V_{sat}$$

$$\lambda = A1 \cdot V_{gst} + A2 \quad (\lambda \text{ is limited to be less than or equal to 1})$$

A bulk effect is introduced through the parameter ***Abulk*** defined as follows:

If **BULKMOD** is set to 1, then

$$Abulk = \left(1 + \frac{K1}{2 \cdot \sqrt{PHI - vbs}} \cdot \frac{A0 \cdot Leff}{Leff + 2 \cdot \sqrt{XJ \cdot Xdep}} \right) \cdot \frac{1}{1 + KETA \cdot vbs}$$

$$\text{otherwise: } Abulk = \frac{K1}{2 \cdot \sqrt{PHI}} \cdot \frac{A0 \cdot Leff}{Leff + 2 \cdot \sqrt{XJ \cdot Xdep}} \cdot \frac{1}{1 + KETA \cdot vbs}$$

Finally, the saturation voltage ***Vdsat*** is defined as follows:

- For ***Rds*=0** and $\lambda=1$:

$$V_{dsat} = \frac{Esat \cdot V_{gst} \cdot Leff}{Abulk \cdot Esat \cdot Leff + V_{gst}}$$

- For ***Rds*>0** or $\lambda \neq 1$:

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4 \cdot a \cdot c}}{2 \cdot a}$$

where:

$$a = Abulk \cdot \left(Abulk \cdot Rfactor + \frac{1}{\lambda} - 1 \right)$$

$$b = -Vgst \cdot \left(\frac{2}{\lambda} - 1 \right) - Abulk \cdot (Esat \cdot Leff + 3 \cdot Rfactor \cdot Vgst)$$

$$c = Esat \cdot Vgst \cdot Leff + 2 \cdot Rfactor \cdot Vgst^2$$

3.5 DC current calculation

The different regions of operation are defined as follows:

- For $Vgst > 0$ and $Vds \leq Vdsat$, the device operates in the Linear region.
 - For $Vgst > 0$ and $Vds > Vdsat$, the device operates in the Saturation region.
 - The Subthreshold region is defined according to the flag **SUBTHMOD**:
 - If **SUBTHMOD = 0**, then no subthreshold current is applied.
 - If **SUBTHMOD = 1**, then BSIM1 subthreshold current model is used.
 - If **SUBTHMOD = 2** or **3**, then BSIM3 subthreshold model is used and a transition region is defined as:
 - For $Vg_{low} < Vgst < Vg_{high}$, the device operates in transition region,
 - For $Vgst \leq Vg_{low}$, the device operates in subthreshold region,
 - For $Vgst \geq Vg_{high}$, the device operates in linear or saturation region,
- where the Vg_{low} , Vg_{high} variables are defined as follows:

$$Vg_{low} = VGLOW - Pdibl$$

$$Vg_{high} = VGHIGH + Pdibl$$

and

$$Pdibl = (ETA0 + ETAB \cdot vbs) \cdot Theta_dibl \cdot vds$$

$$\Theta_{dibl} = \exp\left(-DSUB \cdot \frac{Leff}{2 \cdot lt0}\right) + 2 \cdot \exp\left(-DSUB \cdot \frac{Leff}{lt0}\right)$$

3.6 Linear region

In the linear region, the drain current Ids is defined as:

$$Ids = Ids0 \cdot \frac{vds}{vds + Rds \cdot Ids0}$$

where $Ids0$ is defined as:

$$Ids0 = Ueff \cdot Cox \cdot \frac{Weff}{Leff} \cdot \frac{Esat \cdot Leff \cdot vds}{Esat \cdot Leff + vds} \cdot (Vgst - 0.5 \cdot Abulk \cdot vds)$$

3.7 Saturation region

The Early voltage $Vasat$ at the saturation point ($vds = Vdsat$) is defined as:

$$Vasat = \frac{Esat \cdot Leff + Vdsat + 2 \cdot Rfactor \cdot (Vgst - 0.5 \cdot Abulk \cdot Vdsat)}{2/\lambda - 1 + Abulk \cdot Rfactor}$$

The Early voltage Va calculation is selected depending on the value of the **SATMOD** parameter.

If **SATMOD** = 1, then a semi-empirical Early voltage model is selected as:

$$Va = Vasat + \left(1 + \frac{PVAG \cdot Vgst}{Esat \cdot Leff}\right) \cdot \left(1 + \frac{LDD \cdot ETA}{LITL}\right) \cdot Vb$$

where:

$$Vb = \left(1 - \frac{vds - Vdsat}{2 \cdot EM \cdot LITL}\right) \cdot \frac{(Abulk \cdot Esat \cdot Leff + Vgst) \cdot (vds \cdot Vdsat)}{PCLM \cdot Abulk \cdot Esat \cdot LITL}$$

If **SATMOD** = 2, then a fully physical Early voltage model is selected as:

$$Va = Vasat + \left(1 + \frac{PVAG \cdot Vgst}{Esat \cdot Leff}\right) \cdot \left(1 + ETA \cdot \frac{LDD}{LITL}\right) \cdot \left(\frac{1}{Vaclm} + \frac{1}{Vadibl}\right)^{-1}$$

The Early voltage due to Channel Length Modulation effect **Vaclm** is expressed as:

$$Vaclm = \frac{vds - Vdsat}{PCLM} \cdot \frac{Abulk \cdot Esat \cdot Leff + Vgst}{Abulk \cdot Esat \cdot LITL}$$

The Early voltage due to Drain Induced Barrier Lowering effect **Vadibl** is expressed as:

$$Vadibl = \frac{1}{Thetarout} \cdot \left(Vgst - \frac{Abulk \cdot Vdsat \cdot Vgst}{Abulk \cdot Vdsat + Vgst}\right)$$

$$Thetarout = PDIBL1 \cdot \left(\exp \frac{-DROUT \cdot Leff}{2 \cdot lt0} + 2 \cdot \exp \frac{-DROUT \cdot Leff}{lt0}\right)$$

$$+ PDIBL2$$

$$lt0 = \sqrt{\frac{\epsilon_{si}}{\epsilon_{ox}} \cdot TOX \cdot Xdep(vbs=0)}$$

The Early voltage due to Substrate Current induced Body Effect **Vascbe** is expressed as:

$$Vascbe = \frac{Leff}{PSCBE2} \cdot \exp\left(\frac{PSCBE1 \cdot LITL}{vds - Vdsat}\right)$$

Finally, the saturation current **Idsat** and the drain current **Ids** are expressed as follows:

$$\begin{aligned} Idsat &= Cox \cdot Weff \cdot Vsat \cdot \lambda \cdot (Vgst - Abulk \cdot Vdsat) \\ Ids &= Idsat \cdot \left(1 + \frac{vds - Vdsat}{Va}\right) \cdot \left(1 + \frac{vds - Vdsat}{Vascbe}\right) \end{aligned}$$

3.8 Subthreshold region

$$Cd = \sqrt{\frac{q \cdot \varepsilon_{si} \cdot NPEAK}{2 \cdot (PHI - vbs)}}$$

The subthreshold swing parameter n is defined as:

$$n = 1 + NFACTOR \cdot \frac{Cd}{Cox} + \frac{CDSC + CDSCB \cdot vbs}{Cox} \cdot Theta0 + \frac{CIT}{Cox}$$

The reference current $Is0$ is defined as follows:

$$Is0 = U0 \cdot \frac{Weff}{Leff} \cdot Vt^2 \cdot \sqrt{\frac{q \cdot \varepsilon_{si} \cdot NPEAK}{2 \cdot PHI}}$$

In the subthreshold region, the drain current Ids is defined in relation to the **SUBTHMOD** parameter as follows:

If **SUBTHMOD = 0**, then no subthreshold model is applied, so $Ids = 0$.

If **SUBTHMOD = 1**, the BSIM1 subthreshold current model is applied as:

$$Ids = \frac{Ilimit \cdot Iexp}{Ilimit + Iexp} \cdot \left(1 - \exp\frac{-vds}{Vt}\right)$$

where:

$$Ilimit = 4.5 \cdot Is0 \cdot \exp\frac{Pdibl}{n \cdot Vt}$$

$$Iexp = Is0 \cdot \exp\left(\frac{Vgst - VOFF + Pdibl}{n \cdot Vt}\right)$$

If **SUBTHMOD = 2** or **3**, the BSIM3 subthreshold current model is applied for $Vgst \leq Vg_{low}$ as follows:

$$Ids = Is0 \cdot \exp\left(\frac{Vgst - VOFF + Pdibl}{n \cdot Vt}\right) \cdot \left(1 - \exp\frac{-vds}{Vt}\right)$$

3.9 Transition region

The transition region is only defined for **SUBTHMOD = 2** or **3** and when the device operates in the following conditions $Vg_{low} < Vgst < Vg_{high}$, then the drain current **Ids** is defined as follows:

If **SUBTHMOD = 2** then:

$$\begin{aligned} Ids_{low} &= Ids(Vgst=Vg_{low}) & Ids_{high} &= Ids(Vgst=Vg_{high}) \\ Ids &= (1-t)^2 \cdot Ids_{low} + 2 \cdot (1-t) \cdot t \cdot Ip + t^2 \cdot Ids_{high} \end{aligned}$$

If **SUBTHMOD = 3** then:

$$\begin{aligned} Ids_{low} &= \ln(Ids(Vgst=Vg_{low})) & Ids_{high} &= \ln(Ids(Vgst=Vg_{high})) \\ Ids &= \exp((1-t)^2 \cdot Ids_{low} + 2 \cdot (1-t) \cdot t \cdot Ip + t^2 \cdot Ids_{high}) \end{aligned}$$

where:

$$\begin{aligned} t &= \left(\frac{Vp - Vg_{low}}{Vg_{low} + Vg_{high} - 2 \cdot Vp} \right) \cdot \sqrt{1 + \frac{(Vg_{low} + Vg_{high} - 2 \cdot Vp) \cdot (Vgst \cdot Vg_{low})}{(Vp - Vg_{low})^2} - 1} \\ Vp &= \frac{(gm_{high} \cdot Vg_{high} - gm_{low} \cdot Vg_{low}) - (Ids_{high} - Ids_{low})}{gm_{high} - gm_{low}} \\ Ip &= Ids_{low} + gm_{low} \cdot (Vp - Vg_{low}) \\ gm_{low} &= \frac{\partial Ids}{\partial Vgs}(Vgst=Vg_{low}) & gm_{high} &= \frac{\partial Ids}{\partial Vgs}(Vgst=Vg_{high}) \end{aligned}$$

4.0 Charge Equations

4.1 Definitions

The value of C_{ox} is calculated from the value of TOX as follows: $C_{ox} = \frac{e_{ox}}{TOX}$

where e_{ox} is the Permittivity of SiO_2 and is calculated as follows:

$$e_{ox} = 3.9 \times \epsilon_0 \text{ Fm}^{-1}; \text{ where: } \epsilon_0 = \text{Permittivity in a Vacuum} = 8.854214871 \times 10^{-12}$$

The effective capacitance of the device is defined as $C_{eff} = C_{ox} \cdot W_{eff} \cdot L_{eff}$

The effective flatband voltage is defined as $V_{fb} = V_{th} - PHI - K1 \cdot f$.

4.2 Charge calculations

In the accumulation region ($(V1 = Vgs_{eff} - vbs - Vfb)$ is negative)

$$Q_{gate} = C_{eff} \cdot V1 \quad Q_{drain} = Q_{source} = 0$$

In the subthreshold region ($Vgst$ is negative)

$$Q_{gate} = C_{eff} \cdot K1 \cdot \left(\sqrt{\frac{K1^2}{4} + V1} - \frac{K1}{2} \right) \quad Q_{drain} = Q_{source} = 0$$

In the linear region ($vds < Vds_{sat}$ and $Vgst$ is positive)

$$Q_{gate} = C_{eff} \cdot \left(Vgs_{eff} - PHI - Vfb - \frac{vds}{2} \cdot \left(1 - \frac{vds}{3 \cdot (2 \cdot Vds_{sat} - vds)} \right) \right)$$

The Drain charge Q_{drain} and Source charge Q_{source} expressions depend on the $XPART$ parameter value as follows:

- When $XPART = 1$, a 0/100 charge partition model is used:

$$Q_{drain} = -C_{eff} \cdot \frac{V_{gst}}{V_{dsat}} \cdot \frac{(vds - V_{dsat})^2}{2 \cdot V_{dsat} - vds}$$

$$Q_{source} = C_{eff} \cdot \frac{V_{gst}}{4 \cdot V_{dsat}} \cdot \left(\frac{vds^2}{3 \cdot (2 \cdot V_{dsat} - vds)} - 2 \cdot V_{dsat} - vds \right)$$

- When $XPART = 0.5$, a 50/50 charge partition model is used:

$$Q_{drain} = Q_{source} = -C_{eff} \cdot \frac{V_{gst}}{4 \cdot V_{dsat}} \cdot \left(\frac{vds^2}{3 \cdot (2 \cdot V_{dsat} - vds)} - 2 \cdot V_{dsat} - vds \right)$$

- When $XPART = 0$, a 40/60 charge partition model is used:

$$Q_{drain} = C_{eff} \cdot \frac{V_{gst}}{4 \cdot V_{dsat}} \cdot \left(vds \cdot \frac{16 \cdot V_{dsat}^2 - 18 \cdot V_{dsat} \cdot vds + 4.8 \cdot vds^2}{3 \cdot (2 \cdot V_{dsat} - vds)} - 2 \cdot V_{dsat} \right)$$

$$Q_{source} = -Q_{drain} - C_{eff} \cdot \frac{V_{gst}}{2 \cdot V_{dsat}} \cdot \left(\frac{vds^2}{3 \cdot (2 \cdot V_{dsat} - vds)} + 2 \cdot V_{dsat} - vds \right)$$

In the saturation region ($vds \geq V_{dsat}$ and V_{gst} is positive)

$$Q_{gate} = C_{eff} \cdot \left(V_{gs_{eff}} - PHI - V_{fb} - \frac{V_{dsat}}{3} \right)$$

The Drain charge Q_{drain} and Source charge Q_{source} expressions depend on the $XPART$ parameter value as follows:

- When $XPART = 1$, a 0/100 charge partition model is used:

$$Q_{drain} = 0 \quad Q_{source} = -\frac{2}{3} \cdot C_{eff} \cdot V_{gst}$$

- When $XPART = 0.5$, a 50/50 charge partition model is used:

$$Q_{drain} = Q_{source} = -\frac{1}{3} \cdot C_{eff} \cdot V_{gst}$$

- When $XPART = 0$, a 40/60 charge partition model is used:

$$Q_{drain} = -\frac{0.8}{3} \cdot C_{eff} \cdot V_{gst} \quad Q_{source} = -0.4 \cdot C_{eff} \cdot V_{gst}$$

5.0 Temperature Effects

Specific model temperature effects are as follows:

$$V_t(T) = \frac{k_B \cdot T}{q}$$

$$Eg(T) = 1.16 - 7.02 \cdot 10^{-4} \cdot \frac{T^2}{T + 1108}$$

$$ni(T) = NI \cdot \left(\frac{T}{300.15} \right)^{1.5} \cdot \exp \left(21.5565981 - \frac{Eg(T)}{2 \cdot V_t(T)} \right)$$

$$DVth(T) = \left(KT1 + \frac{KT1L}{Leff} + KT2 \cdot vbs \right) \cdot \left(\frac{T}{TNOM} - 1 \right)$$

$$Ua(T) = UA + UA1 \cdot \left(\frac{T}{TNOM} - 1 \right)$$

$$Ub(T) = UB + UB1 \cdot \left(\frac{T}{TNOM} - 1 \right)$$

$$Uc(T) = UC + UC1 \cdot \left(\frac{T}{TNOM} - 1 \right)$$

$$U0(T) = U0 \cdot \left(\frac{T}{TNOM} \right)^{UTE}$$

$$Vsat(T) = VSAT - AT \cdot \left(\frac{T}{TNOM} - 1 \right)$$

6.0 Model Parameters

Nr.	Name	Description	Default	Units
1	SUBTHMOD	Subthreshold model selector	2	
2	SATMOD	Saturation model selector	2	
3	BULKMOD	Bulk effect model selector	1 (NMOS)	
			2 (PMOS)	
Threshold Voltage Related Model Parameters				
4	VFB	Flat band voltage	-1 ^a	V
5	PHI	Strong inversion surface potential	b	V
6	K1	First order body effect coefficient	0.53 ^c	V ^{1/2}
7	K2	Second order body effect coefficient	-0.0186 ^c	
8	K3	Narrow width coefficient	80	
9	K3B	Body effect coefficient of K3	0	V ⁻¹
10	ND	Drain-source doping	1.0×10 ²²	cm ⁻³
11	NPEAK	Peak doping	1.7×10 ¹⁷	cm ⁻³
12	VBX	V _{th} transition voltage	d	V
13	VTH0	Threshold voltage at v _{bs} =0 and small v _{ds}	e	V
14	VOFF	Threshold voltage offset	-0.11	V
15	DVT0	First coefficient of short-channel effect on V _{th}	2.2	
16	DVT1	Second coefficient of short-channel effect on V _{th}	0.53	
17	DVT2	Body coefficient of short-channel effect on V _{th}	-3.2×10 ⁻²²	V ⁻¹
18	KETA	Body-bias coefficient of bulk charge effect	-0.047	V ⁻¹
19	VBI	Drain-substrate junction build-in potential	f	V
20	VBM	Maximum applied body bias in V _{th} calculation	-5	V
21	PSCBE1	First substrate current body-effect parameter	4.24×10 ⁸	Vm ⁻¹
22	PSCBE2	Second substrate current body-effect parameter	1.0×10 ⁻⁵	mV ⁻¹
23	GAMMA1	Body effect coefficient near the surface	g	V ^{1/2}
24	GAMMA2	Body effect coefficient in the bulk	h	V ^{1/2}
Mobility Related Model Parameters				
25	UA	First-order mobility degradation coefficient	2.25×10 ⁻⁹	mV ⁻¹
26	UB	Second-order mobility degradation coefficient	5.87×10 ⁻¹⁹	(mV ⁻¹) ²
27	UC	Body effect of mobility	4.65×10 ⁻²	V ⁻¹

Nr.	Name	Description	Default	Units
28	U0	Mobility at nominal temperature	0.067 (NMOS) 0.025 (PMOS)	$\text{m}^2(\text{Vs})^{-1}$
Subthreshold Related Parameters				
29	DSUB	DIBL coefficient exponent	DROUT	
30	ETA0	DIBL coefficient in subthreshold	0.08	
31	ETAB	Body-bias coefficient for DIBL effect in subthreshold	-0.07	V^{-1}
32	NFACTOR	Subthreshold swing factor	1	
33	VGHIGH	Upper bound of transition region	0.12	V^{-1}
34	VGLOW	Lower bound of transition region	-0.12	V^{-1}
Velocity Saturation Related Model Parameters				
35	EM	Maximum electric field	4.1×10^7	Vm^{-1}
36	ETA	Effective drain voltage coefficient due to LDD	0.3	
37	PCLM	Channel length modulation parameter	1.3	
38	PDIBL1	First DIBL effect coefficient in output resistance	0.39	
39	PDIBL2	Second DIBL effect coefficient in output resistance	0.0086	
40	DROUT	L dependence exponent in DIBL	0.56	
41	A0	Bulk charge effect coefficient for channel length	1 (BULKMOD=1) 4.4 (BULKMOD=2)	
42	A1	First non-saturation effect parameter	0 (NMOS) 0.23 (PMOS)	V^{-1}
43	A2	Second non-saturation effect parameter	1 (NMOS) 0.08 (PMOS)	
44	PVAG	Gate dependence of Early voltage	0	
45	VSAT	Saturation velocity	8.0×10^6	cm s^{-1}
Geometry, and Length & Width Modulation Related Model Parameters				
46	LDD	Length of LDD region	0	m
47	W0	Narrow width parameter	2.5×10^{-6}	m
48	XL	Etching effects on Length	0	m
49	XW	Etching effects on Width	0	m
Temperature Effect Related Model Parameters				
50	AT	Temperature coefficient for saturation velocity	3.3×10^4	ms^{-1}
51	UTE	Mobility temperature exponent	-1.5	
52	KT1	Temperature coefficient of threshold voltage	-0.11	V
53	KT1L	Length sensitivity of KT1	0	mV

Nr.	Name	Description	Default	Units
54	KT2	Body-bias sensitivity of KT1	0.022	
55	UA1	Temperature coefficient for UA	4.31×10^{-9}	mV^{-1}
56	UB1	Temperature coefficient for UB	-7.61×10^{-18}	$(\text{mV}^{-1})^2$
57	UC1	Temperature coefficient for UC	-0.056	V^{-1}
Overlap Capacitance Related, and Dynamic Model Parameters				
58	CGBO	Bulk-gate overlap capacitance per length	0	Fm^{-1}
59	CGDO	Drain-gate overlap capacitance per width	i	Fm^{-1}
60	CGSO	Source-gate overlap capacitance per width	j	Fm^{-1}
61	XPART	Flag for channel charge partitioning	1	
Parasitic Resistance and Capacitance Related Model Parameters				
62	RDS0	Parasitic resistance	0	Ω
63	RDSW	Parasitic resistance with respect to unit width	0	$\Omega \mu\text{m}$
64	CDSC	Drain/source to channel coupling resistance	2.4×10^{-4}	Fm^{-2}
65	CDSCB	Body-bias coefficient of CDSC	0	$\text{FV}^{-1}\text{m}^{-2}$
66	CIT	Interface trap capacitance	0	Fm^{-2}
Process and Parameter Extraction Related Model Parameters				
67	TOX	Gate oxide thickness	1.5×10^{-8}	m
68	NGATE	Poly-gate doping	0	cm^{-3}
69	NSUB	Substrate doping	6×10^{16}	cm^{-3}
70	XT	Doping depth	1.55×10^{-7}	m
71	LITL	Depth of current path	k	m
72	NLX	Lateral non-uniform doping parameter	1.74×10^{-7}	m
Noise Effect Related Model Parameters				
73	A	First Flicker noise parameter	1×10^{16} (NMOS)	$\text{V}^{-1}\text{m}^{-2}$
			9.9×10^{14} (PMOS)	
74	B	Second Flicker noise parameter	5×10^4 (NMOS)	V^{-1}
			2.4×10^3 (PMOS)	
75	C	Third Flicker noise parameter	-1.4×10^{-8} (NMOS)	V^{-1}m^2
			1.4×10^{-8} (PMOS)	

- a. If **VTH0** is specified, then **VFB** is calculated using **VTH0**, **PHI** and **K1**.
- b. If **PHI** is not specified, it is calculated using **NPEAK**.
- c. If both **K1** and **K2** are not specified, they are calculated using **GAMMA1**, **GAMMA2**, **PHI**, **VBX**, **VBM**.
- d. If **VBX** is not specified, it is calculated using **PHI**, **NPEAK** and **XT**.
- e. If **VTH0** is not specified, it is calculated using **VFB**, **PHI** and **K1**.
- f. If **VBI** is not specified, it is calculated using **ND** and **NPEAK**.
- g. If **GAMMA1** is not specified, it is calculated using **NPEAK** and **Cox**.
- h. If **GAMMA2** is not specified, it is calculated using **NSUB** and **Cox**.

- i. If $CGDO$ is not specified, it is calculated using DL , XJ and Cox .
- j. If $CGSO$ is not specified, it is calculated using DL , XJ and Cox .
- k. If $LITL$ is not specified, it is calculated using TOX and XJ .

6.1 Note about parameters

- $NPEAK$, $NGATE$, ND and $U0$ may be entered in meters or centimeters:
 $NPEAK$ is converted to cm^{-3} as follows: if $NPEAK$ is greater than 10^{20} , it is multiplied by 10^{-6} .
 $NGATE$ is converted to cm^{-3} as follows: if $NGATE$ is greater than 10^{23} , it is multiplied by 10^{-6} .
 ND is converted to cm^{-3} as follows: if ND is greater than 10^{24} , it is multiplied by 10^{-6} .
 $U0$ is converted to $\text{m}^2(\text{Vs})^{-1}$ as follows: if $U0$ is greater than 1, it is multiplied by 10^{-4} .
 $NSUB$ must be entered in cm^{-3} .
- For parasitic models, BSIM3v2 uses Eldo MOS Common Equations with default value:
 $ALEV=2$; $RLEV=4$; $DCAPLEV=1$; $DIOLEV=1$.
As a consequence, you may use LD , WD instead of DL , DW . Respectively, if DL , DW are given, they will be used for common equation initialization instead of LD and WD . For junction capacitances, parameter default values differ from common approach.

Chapter 18

BSIM3v3 Equations

1.0 Introduction

The BSIM3v3 model is implemented in Eldo as LEVEL=53. BSIM3v3 has been extensively modified from its previous release BSIM3v2. The physical effects modeled are the same as BSIM3v2. In addition to those, the new advancements are:

- A single drain current expression to describe current and output conductance characteristics from subthreshold to strong inversion as well as from the linear to the saturation operating region.
- New width dependencies for bulk charge and source/drain resistance (**Rds**)
- New capacitance models for both intrinsic and extrinsic capacitances
- A new noise model
- A new relaxation time model for characterizing the non-quasi-static effect for improved transient modeling.

To avoid any model discontinuity caused by certain parameters or unusual operation bias conditions, BSIM3v3 has been improved. Information regarding these improvements is provided below.

BSIM3v3 is available in three versions: BSIM3v3, BSIM3v3.1, and the most recent, BSIM3v3.2. According to Berkeley's recommendation, version BSIM3v3.2 is split into four versions:

- BSIM3v3.2.1
uses bias-dependent **Vfb** for **CAPMOD**=1 and 2

- BSIM3v3.2.2
uses bias-independent Vfb for **CAPMOD=1** and 2
- BSIM3v3.2.3
- BSIM3v3.2.4

BSIM3v3.2.1 and BSIM3v3.2.2 have all the features of BSIM3v3.2. However, they differ only in the Vfb as described above. BSIM3v3.2.3 is compatible with BSIM3v3.2.2 except for some bug fixes and issuing some warnings. BSIM3v3.2.4 includes some bug fixes in the noise model.

Throughout the manual, BSIM3v3.2 will indicate all of BSIM3v3.2.1, BSIM3v3.2.2, BSIM3v3.2.3 and BSIM3v3.2.4 unless any of them is explicitly stated.

The different versions, BSIM3v3, BSIM3v3.1 and BSIM3v3.2.x, are accessible through the model parameter **VER**. By default, BSIM3v3.2.4 (**VER=3.24**) is selected.

Parameter Value	BSIM3v3 Version
VER (VERSION) =3.24	BSIM3v3.2.4 (Default)
VER (VERSION) =3.23	BSIM3v3.2.3
VER (VERSION) =3.22	BSIM3v3.2.2 (Also if VER=3.2)
VER (VERSION) =3.21	BSIM3v3.2.1
VER (VERSION) =3.1	BSIM3v3.1
VER (VERSION) =3.0	BSIM3v3

1.1 BSIM3v3.2.4 enhancements

This version of BSIM3 includes two bug fixes in the noise model. One is a correction in the thermal noise model and the other is in the flicker noise model. Thermal noise has been improved by adding the **Rds** effect to the noise equation. Unified flicker noise is now smooth over all bias regions including from the linear region to saturation region. Both improvements were first introduced in BSIM4.0.0 and have been thoroughly tested. The flicker noise fix will likely necessitate re-extraction of the parameters for the unified flicker noise model.

1.2 BSIM3v3.2.3 enhancements

The release of BSIM3v3.2.3 includes the Berkeley defect fixes released in October 2001. A list of these defect fixes is presented below:

- The $1/f$ noise bug fix avoids negative DelClm when calculating noise density by turning off the second part of the noise density equation.
- The model parameter **ACDE** is a **CAPMOD** 3 parameter and is now checked only when **CAPMOD=3** to avoid warning messages when other capMods are used.
- In order to avoid changing model parameter values given by the model card due to update by temperature, three more pre-calculated variables are added and assigned for temperature parameters of parasitic diodes.

1.3 BSIM3v3.2 enhancements

- An original and accurate charge thickness capacitance model considering the finite charge layer thickness (quantum effects). This model is smooth, continuous and very accurate through all regions of operations.
- Improved modeling of C-V characteristics at the weak to strong inversion transition
- Adding the **TOX** dependence into the threshold voltage **Vth** model
- Adding the flatband voltage **Vfb** as a new model parameter
- Improved substrate current scalability with channel length
- Restructuring of the non-quasi-static NQS model
- Adding temperature dependence into the diode junction capacitance
- DC diode model now supporting a resistance-free diode and current-limiting feature (selected by setting **DIOLEV = 7**)

- Option of using the inversion charge of **CAPMOD 0, 1, 2 or 3** to evaluate the BSIM3 thermal noise
- Elimination of the small negative capacitance of **C_{gs}** and **C_{gd}** in the accumulation-depletion regions
- Introducing a separate set of channel-width and length dependence parameters (**LLC , LWC , $LWLC$, WLC , WWC and $WWLC$**) to calculate **$Weff$** and **$Leff$** for the C-V model for better fitting of the capacitance data.
- Adding parameter checking to avoid bad values for certain parameters.

The release of BSIM3v3.2 includes the Berkeley defect fixes released on March 27th, 1999. A list of these defect fixes is presented below:

- Potential non-zero **$Vdseff$** and **$VdseffCV$** at **$Vds=0.0$**
- Potential discontinuity in diode I-V
- The derivative of **$Tcen$** missing in an if-else statement in **CAPMOD=3**
- The derivative of **$Abulk$** with respect to **Vg** missing when **$Abulk<0.1$**
- ***ScalingFactor*** missing in some NQS matrix elements (Eldo didn't suffer from this defect in previous releases and thus no changes were made here).

1.4 Backward compatibility of BSIM3v3.2 with BSIM3v3.1

Even when all new model parameters are given their default values, the following code modifications could result in inconsistencies between BSIM3v3.2 and BSIM3v3.1:

- Junction diode model since **$IJTH$** default = 0.1

For version 3.2, the junction diode model is selected via **$DIOLEV=7$** which is the default. The default value of the parameter **$IJTH$** (Diode limiting current) is 0.1. Hence there is no default backward compatibility if **$IJTH$** is not specified. The user must explicitly select **$DIOLEV=6$** (default for

version 3.1 is **DIOLEV=6**, or select any other **DIOLEV** model of those in Eldo) to retain the backward compatibility.

- Bias-independent Flat-band Voltage (**vfbzb**) for **CAPMOD** 1 and 2. (Backward compatible for the case of BSIM3v3.2.1)

The default for version 3.2 is **CAPMOD=3**, the default for version 3.1 is **CAPMOD=2**. Hence there is no default backward compatibility in this area. Also if the user selects **CAPMOD=1** or **2** with version 3.2 the results will differ from those with version 3.1. Selecting **CAPMOD** 1 or 2 with version 3.2 will use the **Vfb** zero bias calculated from **Vth**, while the **CAPMOD** 1 or 2 of version 3.1 will use the old bias dependent **Vfb**. However backward compatibility can be retained by specifying **CAPMOD=1** or **2** with **VER(VERSION)=3.21** instead of 3.2.

- Using CV **Qinv** for BSIM3 thermal noise evaluation

For version 3.2, the option of using C-V inversion charge equations of **CAPMOD** 0, 1, 2 or 3 to calculate the BSIM3 thermal noise when **NOIMOD == 2** or **4**. The old channel charge equation is used for version 3.1. Hence backward compatibility cannot be retained.

- Re-implementation of NQS model

The NQS model is re-implemented in version 3.2. A new charge partitioning scheme is used which is physically consistent with that in the quasi-static C-V model and significantly improves the simulation performance. Additionally, the old NQS model is kept for version 3.1. Hence backward compatibility cannot be retained.

For all other modifications backward compatibility will be completely retained by leaving the new parameters at their default values.

2.0 Additional Features

2.1 BSIM4 Gate Current inside BSIM3v3

Due to the continual decrease in device dimensions, the oxide thickness in new technologies is very small, so much so that the gate current is noticeable. Many companies would model the gate current with BSIM3v3 model in the form of a SUBCKT, however, this would slow the simulation a great deal. The gate current model of BSIM4 has, therefore, been incorporated inside BSIM3v3.

Having the gate current inside the compact model should be much faster than in the form of a SUBCKT. The model parameters used in BSIM4 should be used for the gate current. The two main selectors are ***IGCMOD*** & ***IGBMOD***. If either of these flags equal 1, the gate current will be calculated and the values taken will not be equal to 0. If both of these selectors are equal to 0 or not specified, the gate current is not calculated and the simulation will proceed as before.

-  These parameters can be found in the [BSIM4 Gate Current Model](#) section of the parameter table.
-  For further details, please refer to the [BSIM4 Equations](#) chapter, from which you can access the full BSIM4 documentation.

2.2 BSIM4 Gate-Induced Drain Leakage Current inside BSIM3v3

The gate induced drain leakage current (GIDL current) is gaining more importance in new technologies from day to day. Many companies would model the GIDL current with BSIM3v3 model, using a SUBCKT, however, this would slow the simulation. The GIDL current model of BSIM4 has therefore been incorporated inside BSIM3v3 to increase the simulation speed. The model parameters used in BSIM4 should be used for the GIDL current. These four main parameters are ***AGIDL***, ***BGIDL***, ***CGIDL*** & ***EGIDL***. If any of these parameters are specified, the GIDL current will be calculated. If none of the parameters are specified, the GIDL current is not calculated and the simulation will proceed as before.

- i** These parameters can be found in the [BSIM4 Gate-Induced Drain Leakage Model Parameters](#) section of the parameter table.
- i** For further details, please refer to the [BSIM4 Equations](#) chapter, from which you can access the full BSIM4 documentation.

2.3 BSIM3SOI DTOXCV Parameter inside BSIM3v3

There have been a number of problems regarding **CAPMOD=3** of BSIM3v3. The most serious symptom is the capacitance reduction (C_{gg}) in the strong inversion region if **CAPMOD** was changed from 0 to 3. BSIMPD is an SOI model formulated on top of the BSIM3v3 framework and also has the same trouble. The Berkeley team proposed an additional parameter, **DTOXCV**, in **CAPMOD=3** of BSIMPDv2.2.3 to solve this issue. This has also been added to BSIM3v3.

- i** This parameter can be found in the [Process Parameters](#) section of the parameter table.
- i** For further details, please refer to the [BSIM3SOI v2.x and v3.x Equations](#) chapter, from which you can access the full BSIM3SOI documentation.

2.4 Compatibility option for negative **Rds** values

By default, negative **Rds** values are clipped to zero. An Eldo option is available to allow negative **Rds** values: **.OPTION RDSWTPOS=0 | 1**. Default value is 1, which means Eldo clips negative **Rds** values (after temperature update) to zero. To allow negative **Rds** values, set the option to 0.



When this option is used to allow negative **Rds** values, the results may be unpredictable, or even cause the simulation to fail.

3.0 Useful Internal Parameters

3.1 Initialization

If **UPDATEPHI** = 0:

$$\textbf{PHI} \text{ is internally calculated as: } \textbf{PHI} = 2 \cdot V_t(T_{nom}) \cdot \ln\left(\frac{NCH}{ni(T_{nom})}\right)$$

$$\textbf{VBI} \text{ is internally calculated as: } \textbf{VBI} = V_t(T_{nom}) \cdot \ln\left(\frac{ND \cdot NCH}{ni(T_{nom})^2}\right)$$

else

$$\textbf{PHI} \text{ is internally calculated as: } \textbf{PHI} = 2 \cdot V_t(T) \cdot \ln\left(\frac{NCH}{ni(T)}\right)$$

$$\textbf{VBI} \text{ is internally calculated as: } \textbf{VBI} = V_t(T) \cdot \ln\left(\frac{ND \cdot NCH}{ni(T)^2}\right)$$

If **NCH** is not given and **GAMMA1** is given, **NCH** is defined as:

$$NCH = \frac{\textbf{GAMMA1}^2 \cdot Cox^2}{2 \cdot q \cdot \epsilon_{si}}$$

If both **GAMMA1** and **NCH** are not given, **NCH** default value is $1.7 \times 10^{17} \text{ cm}^{-3}$ and **GAMMA1** is calculated from **NCH**.

$$\text{If } \textbf{GAMMA1} \text{ is not given, it is defined as: } \textbf{GAMMA1} = \frac{\sqrt{2 \cdot q \cdot \epsilon_{si} \cdot NCH}}{Cox}$$

$$\text{If } \textbf{GAMMA2} \text{ is not given, it is defined as: } \textbf{GAMMA2} = \frac{\sqrt{2 \cdot q \cdot \epsilon_{si} \cdot NSUB}}{Cox}$$

If $VTH0$ is not given, it is defined as: $VTH0 = Vfb + PHI + K1ox \cdot \sqrt{PHI}$

Where flatband voltage Vfb is now used as a model parameter VFB . Default value for flatband voltage is $VFB=-1$. But if $VTH0$ is given, Vfb is calculated from the previous equation, Regardless to whether it is given as model parameter or not.

The parameter $DELVT0$ is added to the parameter $VTH0$ whether $VTH0$ is given or calculated from VFB . $DELVT0$ can be specified as a model parameter and/or as an element parameter.

$$VTH0 = VTH0 + DELVT0_{Model} + DELVT0_{Element}$$

If VBX is not given, it is defined as: $VBX = PHI - \frac{q \cdot NCH \cdot XT^2}{2 \cdot \epsilon_{si}}$

If $K1$ and $K2$ are not given then:

$$K2 = (GAMMA1 - GAMMA2) \cdot \frac{\sqrt{PHI - VBX} - \sqrt{PHI}}{2 \cdot \sqrt{PHI} \cdot (\sqrt{PHI - VBM} - \sqrt{PHI}) + VBM}$$

$$K1 = GAMMA2 - 2 \cdot K2 \cdot \sqrt{PHI - VBM}$$

If $VER = 3.2$

$$K1ox = K1 \cdot \left(\frac{TOX}{TOXM} \right)$$

$$K2ox = K2 \cdot \left(\frac{TOX}{TOXM} \right)$$

$$\begin{aligned} & \text{else } K1ox = K1 \\ & \text{else } K2ox = K2 \end{aligned}$$

If $CGSO$ is not given, it is defined as follows:

If DLC given and $DLC > 0$:

$$CGSO = DLC \cdot Cox - CGSL \text{ if } CGSO < 0 \text{ then } CGSO = 0$$

otherwise: $CGSO = 0.6 \cdot XJ \cdot Cox$

If $CGDO$ is not given, it is defined as follows:

If DLC given and $DLC > 0$:

$$CGDO = DLC \cdot Cox - CGDL \text{ if } CGDO < 0 \text{ then } CGDO = 0$$

otherwise: $CGDO = 0.6 \cdot XJ \cdot Cox$

If CF is not given, it is defined as: $CF = \frac{2\varepsilon_{ox}}{\pi} \cdot \log\left(1 + \frac{4 \times 10^{-7}}{TOX}\right)$

CF is added to parameters $CGSO$ and $CGDO$.

3.2 Effective channel length and width

$$L_{mask} = L_{mask} \cdot LM LT$$

$$W_{mask} = W_{mask} \cdot WM LT$$

$$L_{eff} = L_{printed} - 2 \cdot dL$$

$$W_{eff} = W_{printed} - 2 \cdot (dW + DWG \cdot Vgst_eff + DWB \cdot (\sqrt{Phis} - \sqrt{PHI}))$$

where $L_{printed} = L_{drawn} + XL$ and $W_{printed} = W_{drawn} + XW$

$$dL = LINT + \frac{LL}{L_{printed}^{LLN}} + \frac{LW}{W_{printed}^{LWN}} + \frac{LWL}{L_{printed}^{LLN} \cdot W_{printed}^{LWN}}$$

with:

$$dW = WINT + \frac{WL}{L_{printed}^{WLN}} + \frac{WW}{W_{printed}^{WWN}} + \frac{WWL}{L_{printed}^{WLN} \cdot W_{printed}^{WWN}}$$

4.0 Static Current Equations

4.1 Threshold voltage

Bulk voltage on device is clamped to values above V_{bsc} as:

$$v_{bs} = V_{bsc} + \frac{1}{2}(v_{bs} - V_{bsc} - \delta_1 + \sqrt{(v_{bs} - V_{bsc} - \delta_1)^2 - 4 \cdot \delta_1 \cdot V_{bsc}})$$

$$\text{where } V_{bsc} = 0.9 \cdot \left(PHI - \frac{K1ox^2}{4 \cdot K2^2} \right) \text{ and } \delta_1 = 10^{-3}$$

The Threshold voltage V_{th} is defined as follows:

$$\begin{aligned} V_{th} = & V_{TH0} + K1ox \cdot \sqrt{Phis} - K1 \cdot \sqrt{PHI} - K2ox \cdot v_{bs} - DV_{th0} - DV_{th0_W} + \\ & DV_{th0}(T) - Pdibl + (K3 + K3B \cdot v_{bs}) \cdot \frac{TOX \cdot PHI}{W_{eff} + W0} + \\ & K1 \cdot \sqrt{PHI} \cdot \left(\sqrt{1 + \frac{NLX}{L_{eff}}} - 1 \right) \end{aligned}$$

$$\text{If } v_{bs} \leq 0 \text{ then: } \sqrt{Phis} = \sqrt{PHI - v_{bs}} \quad \text{else} \quad \sqrt{Phis} = \frac{PHI \cdot \sqrt{PHI}}{PHI + 0.5 \cdot v_{bs}}$$

$$DV_{th0} = DVT0 \cdot (VBI - PHI) \cdot Theta_0$$

$$DV_{th0_W} = DVT0_W \cdot (VBI - PHI) \cdot Theta_{0W}$$

$$Theta_0 = \exp\left(-DVT1 \cdot \frac{L_{eff}}{2Lt}\right) + 2 \cdot \exp\left(-DVT1 \cdot \frac{L_{eff}}{Lt}\right)$$

$$Theta_{0W} = \exp\left(-DVT1_W \cdot \frac{L_{eff} \cdot W_{eff}}{2Lt_W}\right) + 2 \cdot \exp\left(-DVT1_W \cdot \frac{L_{eff} \cdot W_{eff}}{Lt_W}\right)$$

$$Lt = \sqrt{\frac{\epsilon_{si} \cdot TOX \cdot Xdep}{\epsilon_{ox}}} \cdot (1 + DVT2 \cdot vbs) ; Lt_0 = Lt(vbs = 0)$$

$$Lt_W = \sqrt{\frac{\epsilon_{si} \cdot TOX \cdot Xdep}{\epsilon_{ox}}} \cdot (1 + DVT2W \cdot vbs)$$

$$Xdep = \sqrt{\frac{2\epsilon_{si}}{q \cdot NCH}} \cdot \sqrt{Phis}$$

$$Pdibl = vds \cdot (ETA0 + ETAB \cdot vbs) \cdot$$

$$\left(\exp\left(-DSUB \cdot \frac{L_{eff}}{2Lt_0}\right) + 2 \cdot \exp\left(-DSUB \cdot \frac{L_{eff}}{Lt_0}\right) \right)$$

4.2 Poly gate depletion effect

Poly Gate depletion effect is taken into account by the parameter **NGATE**. When this parameter is given, **vgs** is updated as:

$$Vgs_{eff} = Vfb + PHI + K \cdot \left(\sqrt{1 + \frac{2 \cdot (vgs - Vfb - PHI)}{K}} - 1 \right)$$

$$\text{where } K = \frac{q \cdot \epsilon_{si} \cdot NGATE}{Cox^2}$$

Otherwise, $Vgs_{eff} = vgs$

4.3 Subthreshold model

Subthreshold current is taken into account as a unified function of **Vgs**, Effective **Vgs-Vth** is then given by:

$$Vgst_{eff} = \frac{2 \cdot n \cdot V_t \cdot \ln\left(1 + \exp\left(\frac{Vgs_{eff} - Vth}{2 \cdot n \cdot V_t}\right)\right)}{1 + 2 \cdot n \cdot Cox \cdot \sqrt{\frac{2PHI}{q \cdot \epsilon_{si} \cdot NCH}} \cdot \exp\left(-\frac{Vgs_{eff} - Vth - 2VOFF}{2 \cdot n \cdot V_t}\right)}$$

where n is the subthreshold swing factor determined by:

$$n = 1 + NFACTOR \cdot \frac{Cd}{Cox} + Theta_0 \cdot \frac{CDSC + CDSCB \cdot vbs + CDSCD \cdot vds}{Cox} + \frac{CIT}{Cox}$$

$$Cd = \frac{\epsilon_{si}}{Xdep}$$

4.4 Mobility calculation

- For $MOBMOD = 1$:

$$\mu_{eff} = \frac{\mu_0(T)}{1 + (\mu_A(T) + \mu_C(T) \cdot vbs) \cdot \frac{Vgst_{eff} + 2Vth}{TOX} + \mu_B(T) \cdot \left(\frac{Vgst_{eff} + 2Vth}{TOX}\right)^2}$$

- For $MOBMOD = 2$:

$$\mu_{eff} = \frac{\mu_0(T)}{1 + (\mu_A(T) + \mu_C(T) \cdot vbs) \cdot \frac{Vgst_{eff}}{TOX} + \mu_B(T) \cdot \left(\frac{Vgst_{eff}}{TOX}\right)^2}$$

- For $MOBMOD = 3$:

$$\mu_{eff} = \frac{\mu_0(T)}{1 + \left(\mu_A(T) \cdot \frac{Vgst_{eff} + 2Vth}{TOX} + \mu_B(T) \cdot \left(\frac{Vgst_{eff} + 2Vth}{TOX}\right)^2\right) \cdot (1 + \mu_C(T)vbs)}$$

4.5 Drain saturation voltage

The channel resistance, Rds is defined by:

$$Rds = \frac{Rdsw(T) \cdot (1 + PRWG \cdot Vgst_{eff} + PRWB \cdot (\sqrt{Phis} - \sqrt{PHI}))}{W_{eff}^{WR}}$$

The bulk effect, $Abulk$ is included with:

$$Abulk_0 = \left(1 + \frac{K1ox}{2\sqrt{Phis}} \cdot \left(\frac{A0 \cdot L_{eff}}{L_{eff} + 2\sqrt{XJ \cdot Xdep}} + \frac{B0}{W_{eff} + B1} \right) \right) \cdot \frac{1}{1 + KETA \cdot vbs}$$

$$Abulk = Abulk_0 - AGS \cdot A0 \cdot \frac{Vgst_{eff}}{1 + KETA \cdot vbs} \cdot \frac{K1ox}{2\sqrt{Phis}} \cdot \left(\frac{L_{eff}}{L_{eff} + 2\sqrt{XJ \cdot Xdep}} \right)^3$$

and we introduce the following terms for the equations below:

$$\lambda = A1 \cdot Vgst_{eff} + A2 \quad (\lambda \text{ is clamped to be less than 1})$$

$$Esat = \frac{2Vs(T)}{\mu_{eff}} ; Rfactor = W_{eff} \cdot Vs(T) \cdot Cox \cdot Rds$$

Finally, the saturation voltage, $Vdsat$ is calculated as follows:

- For $Rds = 0$ and $\lambda = 1$: $Vdsat = \frac{Esat \cdot L_{eff} \cdot (Vgst_{eff} + 2V_t)}{Abulk \cdot Esat \cdot L_{eff} + Vgst_{eff} + 2V_t}$
- For $Rds > 0$ or $\lambda \neq 1$: $Vdsat = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$

where:

$$a = A_{bulk}^2 \cdot Rfactor + \left(\frac{1}{\lambda} - 1 \right) \cdot A_{bulk}$$

$$b = -(V_{gst_{eff}} + 2V_t) \left(\frac{2}{\lambda} - 1 \right) - A_{bulk} \cdot (E_{sat} \cdot L_{eff} + 3 \cdot Rfactor \cdot (V_{gst_{eff}} + 2V_t))$$

$$c = E_{sat} \cdot L_{eff} \cdot (V_{gst_{eff}} + 2V_t) + 2 \cdot Rfactor \cdot (V_{gst_{eff}} + 2V_t)^2$$

4.6 Effective Vds

A smooth function is used for vds to make a transition between linear and saturation region:

$$Vdseff = Vdsat - \frac{1}{2} \cdot (V1 + \sqrt{V1^2 + 4 \cdot DELTA \cdot Vdsat})$$

where: $V1 = Vdsat - vds - DELTA$

4.7 Drain current expression

The drain current is given by the global expression:

$$Ids = \frac{Ids_0}{1 + \frac{Rds \cdot Ids_0}{Vdseff}} \cdot \left(1 + \frac{vds - Vdseff}{V_A} \right) \cdot \left(1 + \frac{vds - Vdseff}{V_{ASCBE}} \right)$$

The linear drain current in the channel is:

$$Ids_0 = \frac{W_{eff}}{L_{eff}} \cdot Cox \cdot \mu_{eff} \cdot V_{gst_{eff}} \cdot \frac{\left(1 - A_{bulk} \cdot \frac{Vdseff}{2(V_{gst_{eff}} + 2V_t)} \right) \cdot Vdseff}{\frac{1 + Vdseff}{(E_{sat} \cdot L_{eff})}}$$

The early voltage is:

$$V_A = V_{Asat} + \left(1 + \frac{PVAG \cdot V_{gst_{eff}}}{E_{sat} \cdot L_{eff}} \right) \cdot \left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBL}} \right)^{-1}$$

where the different components of the early voltage are as follows:

The Early voltage at $vds = Vdsat$:

$$V_{Asat} = \frac{Esat \cdot L_{eff} + Vdsat + 2 \cdot Rfactor \cdot Vgst_{eff} \cdot \left(1 - \frac{Abulk \cdot Vdsat}{2(Vgst_{eff} + 2V_t)}\right)}{\frac{2}{\lambda} - 1 + Rfactor \cdot Abulk}$$

The Early voltage due to Channel Length Modulation effect (CLM):

$$V_{ACLM} = \frac{Abulk \cdot Esat \cdot L_{eff} + Vgst_{eff}}{PCLM \cdot Abulk \cdot Esat \cdot Litl} \cdot (vds - Vdseff)$$

The Early voltage due to Drain Induced Barrier Lowering effect (DIBL):

$$V_{ADIBL} = \frac{(Vgst_{eff} + 2V_t)}{\theta_{rout} \cdot (1 + PDIBLCB \cdot vbs)} \cdot \left(1 - \frac{Abulk \cdot Vdsat}{Abulk \cdot Vdsat + Vgst_{eff} + 2V_t}\right)$$

The Early voltage due to Substrate Current Induced Body effect (SCBE):

$$V_{ASCBE} = \frac{L_{eff}}{PSCBE2} \cdot \exp\left(\frac{PSCBE1 \cdot Litl}{vds - Vdseff}\right)$$

with:

$$Litl = \sqrt{\frac{\epsilon_{si} \cdot TOX \cdot XJ}{\epsilon_{ox}}}$$

$$\theta_{rout} = PDIBLC1 \cdot \left(\exp\left(-DROUT \cdot \frac{L_{eff}}{2Lt_0}\right) + 2 \cdot \exp\left(-DROUT \cdot \frac{L_{eff}}{Lt_0}\right) \right)$$

$$+ PDIBLC2$$

4.8 Substrate current

The substrate current model I_{cb} is defined as:

- For $IIMOD=0$ (default), BSIM3v3 impact ionization model:

$$I_{cb} = \frac{\text{ALPHA0} + \text{ALPHA1} \cdot L_{eff}}{L_{eff}} \cdot (vds - Vdseff) \cdot \exp\left(\frac{\text{BETA0}}{vds - Vdseff}\right)$$

$$\cdot \frac{Ids_0}{1 + \frac{Rds \cdot Ids_0}{Vdseff}} \cdot \left(1 + \frac{vds - Vdseff}{V_A}\right)$$

Parameters **ALPHA0**, **ALPHA1** and **BETA0** refer to ionization currents. The parameter **ALPHA1** is introduced in BSIM3v3.2, and defaults to 0.0 for backward compatibility with BSIM3v3.1.

- For $IIMOD=1$, global model:

$$I_{cb} = \text{ALPHAEff} \cdot (vds - Vdseff) \cdot Ids \cdot \exp\left(\frac{VCReff}{vds - Vdseff}\right)$$

where:

$$\text{ALPHAEff} = \text{ALPHA} + \text{LALPHA} \cdot \left(\frac{1}{Leff} - \frac{1}{Lref}\right) + \text{WALPHA} \cdot \left(\frac{1}{Weff} - \frac{1}{Wref}\right)$$

$$VCReff = VCR + LVCR \cdot \left(\frac{1}{Leff} - \frac{1}{Lref}\right) + WVCR \cdot \left(\frac{1}{Weff} - \frac{1}{Wref}\right)$$

ALPHA, **LALPHA**, **WALPHA**, **VCR**, **LVCR**, **WVCR**, **Lref**, **Wref** are all model card parameters and are the same as those for the global impact ionization model of MOS levels 1, 2, 3.

5.0 Charge Equations

5.1 Definitions

The value of C_{ox} is calculated from the value of TOX as follows: $C_{ox} = \frac{e_{ox}}{TOX}$

where e_{ox} is the Permittivity of SiO_2 and is calculated as follows:

$$e_{ox} = 3.9 \times \epsilon_0 \text{ Fm}^{-1}; \text{ where: } \epsilon_0 = \text{Permittivity in a Vacuum} = 8.854214871 \times 10^{-12}$$

The effective capacitance of the device is defined as:

$$C_{eff} = C_{ox} \cdot L_{active} \cdot W_{active}$$

Specific geometrical initializations are calculated for the charge model as follows:

$$L_{active} = L_{printed} - 2 \cdot dL_{CV}$$

$$W_{active} = W_{printed} - 2 \cdot dW_{CV}$$

where $L_{printed} = L_{drawn} + XL$ and $W_{printed} = W_{drawn} + XW$

$$dL_{CV} = DLC + \frac{LLC}{L_{printed}^{LLN}} + \frac{LWC}{W_{printed}^{LWN}} + \frac{LWLC}{L_{printed}^{LLN} \cdot W_{printed}^{LWN}}$$

and

$$dW_{CV} = DWC + \frac{WLC}{L_{printed}^{WLN}} + \frac{WWC}{W_{printed}^{WWN}} + \frac{WWLC}{L_{printed}^{WLN} \cdot W_{printed}^{WWN}}$$

It can be seen that the parameters **LLC**, **LWC**, **LWLC**, **WLC**, **WWC** and **WWLC** replace the DC parameters **LL**, **LW**, **LWL**, **WL**, **WW** and **WWL** respectively for BSIM3v3.2. These new parameters default to the DC parameters for backward compatibility with BSIM3v3.1.

The effective flatband voltage is defined as: $V_{fb} = V_{th} - PHI - K1_{ox} \cdot \sqrt{Phis}$

The short channel effect is defined as: $A_{bulk'} = A_{bulk_0} \cdot \left(1 + \left(\frac{CLC}{L_{eff}}\right)^{CLE}\right)$

$$A_{bulk0} = \left(1 + \frac{K1}{2\sqrt{PHI - Vbs}} \cdot \left\{ \frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_f X_{dep}}} + \frac{B_0}{W_{eff} + B_1} \right\} \right) \cdot \frac{1}{1 + KETA \cdot Vbs}$$

5.2 Intrinsic charge model

(When $XPART < 0$, the intrinsic charge model is turned off.)

Parameters

Nr.	Name	Description	Default	Units
1	VFCBV	Flatband Voltage parameter for CAPMOD=0	-1	V
2	LVFCBV	Length dependence of VFCBV	0	Vm
3	WVFCBV	Width dependence of VFCBV	0	Vm
4	PVFCBV	Cross-term dependence of VFCBV	0	Vm

For $CAPMOD = 0$, $Vfb = VFBCV$

In the accumulation region ($V1 = Vgs_{eff} - vfs - Vfb < 0$):

$$Q_g = C_{eff} \cdot V1$$

$$Q_{sub} = -Q_g$$

$$Q_{inv} = 0$$

In the subthreshold region ($Vgs < Vth$):

$$Q_b = -C_{eff} \cdot \frac{K1^2}{2} \cdot \left(-1 + \sqrt{1 + \frac{4V1}{K1^2}} \right)$$

$$Q_g = -Q_b$$

$$Q_{inv} = 0$$

In the strong inversion region ($Vgs > Vth$):

$$Vdsat_{cv} = \frac{Vgs - V_{th}}{Abulk'}$$

$$Abulk' = Abulk0 \cdot \left(1 + \left(\frac{CLC}{L_{eff}}\right)^{CLE}\right)$$

$$Abulk0 = \left(1 + \frac{K1ox}{2\sqrt{PHI - Vbs}} \cdot \left\{ \frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}} + \frac{B_0}{W_{eff} + B_1} \right\}\right) \cdot \frac{1}{1 + KETA \cdot Vbs}$$

$$V_{th} = Vfb + PHI + K1 \cdot \sqrt{PHI - Vbseff}$$

- When $XPART = 0.5$, a 50/50 charge partition model is used:

In the linear region ($Vds < Vdsat$):

$$Q_g = C_{eff} \cdot \left(Vgs - Vfb - PHI - \frac{Vds}{2} + \frac{Abulk' \cdot Vds^2}{12 \cdot \left(Vgs - V_{th} - \frac{Abulk' \cdot Vds}{2} \right)} \right)$$

$$Q_{inv} = -C_{eff} \cdot \left(Vgs - V_{th} - \frac{Abulk' \cdot Vds}{2} + \frac{Abulk'^2 \cdot Vds^2}{12 \cdot \left(Vgs - V_{th} - \frac{Abulk' \cdot Vds}{2} \right)} \right)$$

$$Q_b = C_{eff} \cdot$$

$$\left(Vfb - V_{th} + PHI + \frac{(1 - Abulk') \cdot Vds}{2} + \frac{(1 - Abulk') \cdot Abulk' \cdot Vds^2}{12 \cdot \left(Vgs - V_{th} - \frac{Abulk' \cdot Vds}{2} \right)} \right)$$

$$Q_s = Q_d = 0.5Q_{inv}$$

In the saturation region ($Vds \geq Vdsat$):

$$Q_g = C_{eff} \cdot \left(Vgs - Vfb - PHI - \frac{Vdsat}{3} \right)$$

$$Q_s = Q_d = -\frac{1}{3} \cdot C_{eff} \cdot (Vgs - V_{th})$$

$$Q_b = -C_{eff} \cdot \left(Vfb + PHI - V_{th} + \frac{(1 - Abulk') \cdot Vdsat}{3} \right)$$

- When $XPART = 0$, a 40/60 charge partition model is used:

In the linear region ($Vds < Vdsat$):

$$Q_g = C_{eff} \cdot \left(Vgs - Vfb - PHI - \frac{Vds}{2} + \frac{Abulk' \cdot Vds^2}{12 \cdot \left(Vgs - V_{th} - \frac{Abulk' \cdot Vds}{2} \right)} \right)$$

$$Q_{inv} = -C_{eff} \cdot \left(Vgs - V_{th} - \frac{Abulk' \cdot Vds}{2} + \frac{Abulk'^2 \cdot Vds^2}{12 \cdot \left(Vgs - V_{th} - \frac{Abulk' \cdot Vds}{2} \right)} \right)$$

$$Q_b = C_{eff} \cdot$$

$$\left(Vfb - V_{th} + PHI + \frac{(1 - Abulk') \cdot Vds}{2} - \frac{(1 - Abulk') \cdot Abulk' \cdot Vds^2}{12 \cdot \left(Vgs - V_{th} - \frac{Abulk' \cdot Vds}{2} \right)} \right)$$

$$Q_d = -C_{eff} \cdot \left(\frac{Vgs - V_{th}}{2} - \frac{Abulk'}{2} \cdot Vds + \frac{Abulk' \cdot Vds \cdot \left(\frac{(Vgs - V_{th})^2}{6} - \frac{Abulk' \cdot Vds \cdot (Vgs - V_{th})}{8} + \frac{(Abulk' \cdot Vds)^2}{40} \right)}{\left(Vgs - V_{th} - \frac{Abulk' \cdot Vds}{2} \right)^2} \right)$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

In the saturation region ($Vds \geq Vdsat$):

$$Q_g = C_{eff} \cdot \left(Vgs - Vfb - PHI - \frac{Vdsat}{3} \right)$$

$$Q_d = -\frac{4}{15} \cdot C_{eff} \cdot (Vgs - V_{th})$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

$$Q_b = -C_{eff} \cdot \left(Vfb + PHI - V_{th} + \frac{(1 - Abulk') \cdot Vdsat}{3} \right)$$

- When $XPART = 1$, a 0/100 charge partition model is used:

In the linear region ($Vds < Vdsat$):

$$Q_g = C_{eff} \cdot \left(Vgs - Vfb - PHI - \frac{Vds}{2} + \frac{Abulk' \cdot Vds^2}{12 \cdot \left(Vgs - V_{th} - \frac{Abulk' \cdot Vds}{2} \right)} \right)$$

$$Q_{inv} = -C_{eff} \cdot \left(Vgs - V_{th} - \frac{Abulk' \cdot Vds}{2} + \frac{Abulk'^2 \cdot Vds^2}{12 \cdot \left(Vgs - V_{th} - \frac{Abulk' \cdot Vds}{2} \right)} \right)$$

$$\begin{aligned}
Q_b &= C_{eff} \cdot \left(V_{fb} - V_{th} + PHI \right. \\
&\quad \left. + \frac{(1 - A_{bulk'}) \cdot V_{ds}}{2} - \frac{(1 - A_{bulk'}) \cdot A_{bulk'} \cdot V_{ds}^2}{12 \cdot \left(V_{gs} - V_{th} - \frac{A_{bulk'} \cdot V_{ds}}{2} \right)} \right) \\
Q_d &= -C_{eff} \cdot \left(\frac{V_{gs} - V_{th}}{2} + \frac{A_{bulk'}}{2} \cdot V_{ds} - \frac{(A_{bulk'} \cdot V_{ds})^2}{24 \cdot \left(V_{gs} - V_{th} - \frac{A_{bulk'} \cdot V_{ds}}{2} \right)} \right) \\
Q_s &= -(Q_g + Q_b + Q_d)
\end{aligned}$$

In the saturation region ($V_{ds} \geq V_{dsat}$):

$$\begin{aligned}
Q_g &= C_{eff} \cdot \left(V_{gs} - V_{fb} - PHI - \frac{V_{dsat}}{3} \right) \\
Q_b &= C_{eff} \cdot \left(V_{fb} + PHI - V_{th} + \frac{(1 - A_{bulk'}) \cdot V_{dsat}}{3} \right) \\
Q_d &= 0 \quad Q_s = -(Q_g + Q_b)
\end{aligned}$$

For $CAPMOD = 1, 2 \& 3$:

$V_{gst_{effcv}}$ is redefined for capacitance calculation as:

$$V_{gst_{effcv}} = n \cdot NOFF \cdot V_t \cdot \ln \left(1 + \exp \left(\frac{V_{gs_{eff}} - V_{th} - VOFFCV}{n \cdot NOFF \cdot V_t} \right) \right)$$

Where $NOFF$ and $VOFFCV$ are new model parameters of **BSIM3v3.2**. They are introduced to adjust the CV curve shape around $V_{gs} \approx V_{th}$. For backward compatibility with **version 3.1**, $NOFF$ defaults to 1.0 and $VOFFCV$ defaults to 0.0. If ($NOFF < 0.1$) and ($NOFF > 4.0$), or if ($VOFFCV < -0.5$) and ($VOFFCV > 0.5$), then $NOFF$ and $VOFFCV$ are set to 1.0 and 0.0 respectively.

> 0.5), warning messages will be given. $Vgst_{effcv}$ has been re-implemented to avoid any potential discontinuities and numerical instabilities.

The specific saturation voltage is defined as: $Vdsat_{cv} = \frac{Vgst_{effcv}}{Abulk'}$

For $CAPMOD = 1$, the previous BSIM3v2 charge model is used.

If $VER < 3.22$, the Vfb is calculated from:

$$Vfb = Vth - PHI - K1ox \cdot \sqrt{PHI - Vbs_{eff}}$$

otherwise Vfb is calculated from the above equation but under bias independent Vth (this is for the case of BSIM3v3.2.2).

In the accumulation region ($(V1 = Vgs_{effcv} - vbs - Vfb) \leq 0$):

$$Q_{g1} = C_{eff} \cdot V1$$

In the depletion region ($(V1 = Vgs_{effcv} - vbs - Vfb) > 0$):

$$Q_{g1} = C_{eff} \cdot \frac{K1ox^2}{2} \cdot \left(\sqrt{1 + \frac{4V1}{K1ox^2}} - 1 \right)$$

In the saturation region ($vds \geq Vdsat_{cv}$):

$$Q_{g2} = C_{eff} \cdot \left(Vgst_{effcv} - \frac{Vdsat_{cv}}{3} \right)$$

The Drain charge Qd and Source charge Qs expressions depend on the $XPART$ parameter value as follows:

- When $XPART = 0$, a 40/60 charge partition model is used:

$$Q_d = -\frac{4}{15} \cdot C_{eff} \cdot Vgst_{effcv} \quad Q_s = -\frac{2}{5} \cdot C_{eff} \cdot Vgst_{effcv}$$

- When $XPART = 0.5$, a 50/50 charge partition model is used:

$$Q_d = Q_s = -\frac{1}{3} \cdot C_{eff} \cdot Vgst_{effcv}$$

- When $XPART = 1$, a 0/100 charge partition model is used:

$$Q_d = 0 \quad Q_s = -\frac{2}{3} \cdot C_{eff} \cdot Vgst_{effcv}$$

In the linear region ($vds < Vdsat_{cv}$):

$$Q_{g2} = C_{eff} \cdot \left(Vgst_{effcv} - \frac{vds}{2} + \frac{vds^2}{6 \cdot (2Vdsat_{cv} - vds)} \right)$$

The Drain charge Qd and Source charge Qs expressions depend on the $XPART$ parameter value as follows:

- When $XPART = 0$, a 40/60 charge partition model is used:

$$Q_s = \frac{-2 \cdot C_{eff} \cdot A_{bulk'}}{(2Vdsat_{cv} - vds)^2} \cdot \left(Vdsat_{cv}^3 - \frac{4}{3} \cdot Vdsat_{cv}^2 \cdot vds + \frac{2}{3} \cdot Vdsat_{cv} \cdot vds^2 - \frac{2}{15} \cdot vds^3 \right)$$

$$Q_d = \frac{-2 \cdot C_{eff} \cdot A_{bulk'}}{(2Vdsat_{cv} - vds)^2} \cdot \left(Vdsat_{cv}^3 - \frac{5}{3} \cdot Vdsat_{cv}^2 \cdot vds + Vdsat_{cv} \cdot vds^2 - \frac{1}{5} \cdot vds^3 \right)$$

- When $XPART = 0.5$, a 50/50 charge partition model is used:

$$Q_s = Q_d = -\frac{C_{eff} \cdot A_{bulk'}}{2} \cdot \left(Vdsat_{cv} - \frac{vds}{2} + \frac{vds^2}{6 \cdot (2 \cdot Vdsat_{cv} - vds)} \right)$$

- When $XPART = 1$, a 0/100 charge partition model is used:

$$Q_s = -C_{eff} \cdot A_{bulk'} \cdot \left(\frac{Vdsat_{cv}}{2} + \frac{vds}{4} - \frac{vds^2}{12 \cdot (2 \cdot Vdsat_{cv} - vds)} \right)$$

$$Q_d = -C_{eff} \cdot A_{bulk'} \cdot \left(\frac{Vdsat_{cv}}{2} - \frac{3vds}{4} - \frac{vds^2}{4 \cdot (2 \cdot Vdsat_{cv} - vds)} \right)$$

The gate charge, Q_g is finally calculated as: $Q_g = Q_{g1} + Q_{g2}$

For $CAPMOD = 2$, the BSIM3v3 charge model is defined using a single equation to model each charge for all regions, from accumulation to depletion and from linear to saturation.

If $VER < 3.22$, the Vfb is calculated from:

$$Vfb = Vth - PHI - K1ox \cdot \sqrt{PHI - Vbs_{eff}}$$

otherwise Vfb is calculated from the above equation but under bias independent Vth (this is for the case of BSIM3v3.2.2).

A smooth flatband voltage function covering depletion and accumulation regions is defined as:

$$\text{if } Vfb \leq 0 \text{ then } Vfb_{eff} = Vfb - 0.5 \cdot (V_3 + \sqrt{V_3^2 - 4\delta \cdot Vfb})$$

$$\text{else } Vfb_{eff} = Vfb - 0.5 \cdot (V_3 + \sqrt{V_3^2 + 4\delta \cdot Vfb})$$

$$\text{where } V_3 = Vfb - (Vgs_{eff} - vbs) - \delta \quad \text{and } \delta = 2 \cdot 10^{-2}$$

then:

$$Q_{acc} = -C_{eff} \cdot (Vfb_{eff} - Vfb)$$

$$Q_{sub0} = -C_{eff} \cdot \frac{K1ox^2}{2} \cdot \left(\sqrt{1 + \frac{4(Vgb - Vfb_{eff} - Vgst_{effcv})}{K1ox^2}} - 1 \right)$$

A smooth drain-source voltage function covering linear and saturation regions is defined as:

$$Vds_{cv} = Vdsat_{cv} - 0.5 \cdot (V_4 + \sqrt{V_4^2 + 4\delta \cdot Vdsat_{cv}})$$

where $V_4 = Vdsat_{cv} - vds - \delta$

then:

$$Q_{inv} = -C_{eff} \cdot \left(Vgst_{effcv} - \frac{Abulk' \cdot Vds_{cv}}{2} + \frac{Abulk'^2 \cdot Vds_{cv}^2}{6 \cdot (2 \cdot Vgst_{effcv} - Abulk' \cdot Vds_{cv})} \right)$$

$$\delta Q_{sub} = C_{eff} \cdot (1 - Abulk') \left(-\frac{Vds_{cv}}{2} + \frac{Abulk' \cdot Vds_{cv}^2}{6 \cdot (2 \cdot Vgst_{effcv} - Abulk' \cdot Vds_{cv})} \right)$$

Gate and bulk charges are given by:

$$Q_g = -(Q_{inv} + Q_{acc} + Q_{sub0} + \delta Q_{sub})$$

$$Q_b = Q_{acc} + Q_{sub0} + \delta Q_{sub}$$

The Drain charge Q_d and Source charge Q_s expressions depend on the **XPART** parameter value as follows:

- When **XPART** = 0, a 40/60 charge partition model is used:

$$Q_s = \frac{-2 \cdot C_{eff} \cdot Abulk'}{(2 \cdot Vdsat_{cv} - Vds_{cv})^2} \cdot$$

$$\left(Vdsat_{cv}^3 - \frac{4}{3} \cdot Vdsat_{cv}^2 \cdot Vds_{cv} + \frac{2}{3} \cdot Vdsat_{cv} \cdot Vds_{cv}^2 - \frac{2}{15} \cdot Vds_{cv}^3 \right)$$

$$Q_d = \frac{-2 \cdot C_{eff} \cdot Abulk'}{(2 \cdot Vdsat_{cv} - Vds_{cv})^2} \cdot$$

$$\left(Vdsat_{cv}^3 - \frac{5}{3} \cdot Vdsat_{cv}^2 \cdot Vds_{cv} + Vdsat_{cv} \cdot Vds_{cv}^2 - \frac{1}{5} \cdot Vds_{cv}^3 \right)$$

- When $XPART = 0.5$, a 50/50 charge partition model is used:

$$Q_s = Q_d = -\frac{C_{eff} \cdot A_{bulk'}}{2} \cdot \left(V_{dsat_{cv}} - \frac{V_{ds_{cv}}}{2} + \frac{V_{ds_{cv}}^2}{6 \cdot (2 \cdot V_{dsat_{cv}} - V_{ds_{cv}})} \right)$$

- When $XPART = 1$, a 0/100 charge partition model is used:

$$Q_s = -C_{eff} \cdot A_{bulk'} \left(\frac{V_{dsat_{cv}}}{2} + \frac{V_{ds_{cv}}}{4} - \frac{V_{ds_{cv}}^2}{12 \cdot (2 \cdot V_{dsat_{cv}} - V_{ds_{cv}})} \right)$$

$$Q_d = -C_{eff} \cdot A_{bulk'} \left(\frac{V_{dsat_{cv}}}{2} - \frac{3 \cdot V_{ds_{cv}}}{4} + \frac{V_{ds_{cv}}^2}{4 \cdot (2 \cdot V_{dsat_{cv}} - V_{ds_{cv}})} \right)$$

For $CAPMOD = 3$, the charge-thickness model is used (new in BSIM3v3.2).

This only supports zero bias Vfb i.e. Vfb is calculated from bias independent Vth regardless of the version number. This differs from $CAPMOD=1$ and 2.

$$\text{if } Vfb \leq 0 \text{ then } Vfb_{eff} = Vfb - 0.5 \cdot (V_3 + \sqrt{V_3^2 - 4\delta \cdot Vfb})$$

$$\text{else } Vfb_{eff} = Vfb - 0.5 \cdot (V_3 + \sqrt{V_3^2 + 4\delta \cdot Vfb})$$

$$\text{where } V_3 = Vfb - (Vgs_{eff} - vbs) - \delta \quad \text{and } \delta = 2 \cdot 10^{-2}$$

then:

$$Q_{acc} = W_{active} \cdot L_{active} \cdot C_{oxeff} \cdot Vgbacc$$

where:

$$Vgbacc = \frac{1}{2} \cdot (V_0 + \sqrt{V_0^2 + 4\delta Vfb})$$

$$V_0 = Vfb + Vbseff - Vgs - \delta$$

$$C_{oxeff} = \frac{C_{ox} \cdot C_{cen}}{C_{ox}_{cv} + C_{cen}}$$

$$C_{ox}_{cv} = \frac{eox}{TOX - DTOXCV}$$

- X_{DC} for accumulation and depletion

The DC charge thickness in the accumulation and depletion regions can be expressed by:

$$X_{DC} = \frac{1}{3}L_{debye} \exp \left[ACDE \cdot \left(\frac{N_{sub}}{2 \times 10^{16}} \right)^{-0.25} \cdot \frac{vgs - vbs - vfb}{TOX} \right]$$

where X_{DC} has units of cm and $(vgs - vbs - vfb)/TOX$ has units of MV/cm. The model parameter **acde** is introduced for better fitting with a default value of 1. For numerical stability, the following equation is used instead:

$$X_{DC} = X_{max} - \frac{1}{2} \left(X_0 + \sqrt{X_0^2 + 4\delta_x X_{max}} \right)$$

where $X_0 = X_{max} - X_{DC} - \delta_x$

and $X_{max} = L_{debye}/3$; $\delta_x = 10^{-3}TOX$

- X_{DC} of inversion charge

The inversion charge layer thickness can be formulated as:



W and **L** here are W_{active} and L_{active} .

Note

$$X_{DC} = \frac{1.9 \times 10^{-7}}{1 + \left(\frac{Vgst_{eff} + 4(V_{th} - vfb - 2\Phi_B)}{2TOX} \right)^{0.7}}$$

- Body charge thickness in inversion

$$\Phi_\delta = PHI - 2\Phi_B = V_t \ln \left(\frac{Vgst_{eff, cv} \cdot (Vgst_{eff, cv} + 2K1ox \sqrt{2\Phi_B})}{MOIN \cdot K1ox \cdot V_t^2} + 1 \right)$$

$$Q_{sub0} = -WL \cdot Cox_{eff} \cdot \frac{K1ox^2}{2} \cdot \left[-1 + \sqrt{1 + \frac{4(vgs - Vfb_{eff} - Vbs_{eff} - Vgst_{eff, cv})}{K1ox^2}} \right]$$

$$Vcv_{eff} = V_{dsat} + \frac{1}{2} \cdot (V_1 + \sqrt{V_1^2 + 4\delta_3 V_{dsat}})$$

$$V_1 = V_{dsat} - V_{ds} - \delta_3$$

$$V_{dsat} = \frac{Vgst_{eff, cv} - \Phi_\delta}{Abulk'}$$

$$Q_{inv} = -WL \cdot Cox_{eff} \cdot$$

$$\left[Vgst_{eff, cv} - \Phi_\delta - \frac{1}{2} Abulk' Vcv_{eff} + \frac{Abulk'^2 Vcv_{eff}^2}{12 \left(Vgst_{eff, cv} - \Phi_\delta - \frac{Abulk' Vcv_{eff}}{2} \right)} \right]$$

$$\delta Q_{sub} = WL \cdot Cox_{eff} \cdot \left[\frac{1 - Abulk'}{2} Vcv_{eff} - \frac{(1 - Abulk') Abulk'^2 Vcv_{eff}^2}{12 \left(Vgst_{eff, cv} - \Phi_\delta - \frac{Abulk' Vcv_{eff}}{2} \right)} \right]$$

- 50/50 Charge Partition

$$Q_S = Q_D = \frac{1}{2}Q_{inv} = -\frac{WL \cdot Cox_{eff}}{2}.$$

$$\left[Vgst_{eff, cv} - \Phi_\delta - \frac{1}{2}Abulk' \cdot Vcv_{eff} + \frac{Abulk'^2 Vcv_{eff}^2}{12 \left(Vgst_{eff, cv} - \Phi_\delta - \frac{Abulk' Vcv_{eff}}{2} \right)} \right]$$

- 40/60 Charge Partition

$$Q_S = -\frac{WL \cdot Cox_{eff}}{2 \left(Vgst_{eff, cv} - \Phi_\delta - \frac{Abulk' Vcv_{eff}}{2} \right)^2}.$$

$$\left[(Vgst_{eff, cv} - \Phi_\delta)^3 - \frac{4}{3}(Vgst_{eff, cv} - \Phi_\delta)^2 Abulk' Vcv_{eff} \right.$$

$$\left. + \frac{2}{3}(Vgst_{eff, cv} - \Phi_\delta)(Abulk' Vcv_{eff})^2 - \frac{2}{15}(Abulk' Vcv_{eff})^3 \right]$$

$$Q_D = -\frac{WL \cdot Cox_{eff}}{2 \left(Vgst_{eff, cv} - \Phi_\delta - \frac{Abulk' Vcv_{eff}}{2} \right)^2}.$$

$$\left[(Vgst_{eff, cv} - \Phi_\delta)^3 - \frac{5}{3}(Vgst_{eff, cv} - \Phi_\delta)^2 Abulk' Vcv_{eff} \right.$$

$$\left. + (Vgst_{eff, cv} - \Phi_\delta)(Abulk' Vcv_{eff})^2 - \frac{1}{5}(Abulk' Vcv_{eff})^3 \right]$$

- 0/100 Charge Partition

$$Q_S = -\frac{WL \cdot Cox_{eff}}{2}.$$

$$\left[Vgst_{eff, cv} - \varphi_\delta + \frac{1}{2} Abulk' Vcv_{eff} - \frac{Abulk'^2 Vcv_{eff}^2}{12 \left(Vgst_{eff, cv} - \varphi_\delta - \frac{Abulk' Vcv_{eff}}{2} \right)} \right]$$

$$Q_D = -\frac{WL \cdot Cox_{eff}}{2}.$$

$$\left[Vgst_{eff, cv} - \varphi_\delta - \frac{3}{2} Abulk' Vcv_{eff} + \frac{Abulk'^2 Vcv_{eff}^2}{4 \left(Vgst_{eff, cv} - \varphi_\delta - \frac{Abulk' Vcv_{eff}}{2} \right)} \right]$$

5.3 Overlap charge calculation

For BSIM3v3, specific overlap charges are calculated in relation to the **CAPMOD** parameter.

For **CAPMOD** = 0:

Drain overlap charge:

$$\frac{Q_{overlap, d}}{W_{active}} = CGDO \cdot vgd$$

Source overlap charge:

$$\frac{Q_{overlap, s}}{W_{active}} = CGSO \cdot vgs$$

For **CAPMOD = 1:**

Drain overlap charge:

If $vgd < 0$:

$$\frac{Q_{overlap,d}}{W_{active}} = CGDO \cdot vgd - CGDL \cdot \frac{CKAPPA}{2} \cdot \left(\sqrt{1 - \frac{4 \cdot vgd}{CKAPPA}} - 1 \right)$$

If $vgd \geq 0$: $Q_{overlap,d} = W_{active} \cdot (CGDO + CGDL) \cdot vgd$

Source overlap charge:

If $vgs < 0$:

$$\frac{Q_{overlap,s}}{W_{active}} = CGSO \cdot vgs - CGSL \cdot \frac{CKAPPA}{2} \cdot \left(\sqrt{1 - \frac{4 \cdot vgs}{CKAPPA}} - 1 \right)$$

If $vgs \geq 0$: $Q_{overlap,s} = W_{active} \cdot (CGSO + CGSL) \cdot vgs$

For **CAPMOD = 2:**

Drain overlap charge:

$$vgd_{ov} = \frac{1}{2} \cdot \left((vgd + \delta) - \sqrt{(vgd + \delta)^2 + 4\delta} \right)$$

$$\begin{aligned} \frac{Q_{overlap,d}}{W_{active}} = & CGDO \cdot vgd + \\ & CGDL \cdot \left(vgd - vgd_{ov} - \frac{CKAPPA}{2} \cdot \left(\sqrt{1 - \frac{4 \cdot vgd_{ov}}{CKAPPA}} - 1 \right) \right) \end{aligned}$$

Source overlap charge:

$$vgs_{ov} = \frac{1}{2} \cdot \left((vgs + \delta) - \sqrt{(vgs + \delta)^2 + 4\delta} \right)$$

$$\frac{Q_{overlap,s}}{W_{active}} = CGSO \cdot vgs + \\ CGSL \cdot \left(vgs - vgs_{ov} - \frac{CKAPPA}{2} \cdot \left(\sqrt{1 - \frac{4 \cdot vgs_{ov}}{CKAPPA}} - 1 \right) \right)$$

5.4 Junction capacitances/charge model (DCAPLEV=4)



DCAPLEV=4 is used only for BSIM3v3.1.



Please refer to “Junction Capacitance/Charge Model Parameters” on page 18-52 for the model parameters.

5.5 Initialization

$CjaX$ and $CjpX$ means either the $Cjas$, $Cjps$ and $Cjad$, $Cjpd$.

AX_{eff} , PX_{eff} , CBX means either AS_{eff} , PS_{eff} , CBS and AD_{eff} , PD_{eff} , CBD .

- **DCAPLEV = 4**

$$CjaX = M \cdot AX_{eff} \cdot CJ_{scal}$$

$$\text{If } PX_{eff} < W_{eff} \text{ then } CjpXg = M \cdot CJSWG \cdot PX_{eff} \quad CjpX = 0$$

$$\text{else if } PX_{eff} > W_{eff} \text{ then}$$

$$CjpXg = M \cdot CJSWG \cdot W_{eff}$$

If $ALEV=3$, and PX & $defpx$ are not defined:

$$CjpX = M \cdot CJSW \cdot PX_{eff}$$

else

$$C_{jpX} = M \cdot CJSW \cdot (P_{X_{eff}} - W_{eff})$$



This special case is for users wishing to use **DCAPLEV=4** in conjunction with **ALEV=3**, while specifying the **geo** parameter.

Note

5.6 Equations



x is used to represent either the Drain or the Source diode capacitance.

Note

The bottomwall capacitance **Cbx_{bottom}** is expressed as:

- If $v_{bx} < 0$ then $C_{bx_{bottom}} = C_{JaX} \cdot \left(1 - \frac{v_{bx}}{P_B}\right)^{-MJ}$
- else $C_{bx_{bottom}} = C_{JaX} \cdot \left(1 + \frac{MJ \cdot v_{bx}}{P_B}\right)$

The sidewall depletion capacitance along field oxide **Cbx_{sidewall}** is expressed as:

- If $v_{bx} < 0$ then $C_{bx_{sidewall}} = C_{jpX} \cdot \left(1 - \frac{v_{bx}}{P_{BSW}}\right)^{-MJSW}$
- else $C_{bx_{sidewall}} = C_{jpX} \cdot \left(1 + \frac{MJSW \cdot v_{bx}}{P_{BSW}}\right)$

The sidewall depletion capacitance along gate side **Cbx_{sidewall}** is expressed as:

- If $v_{bx} < 0$ then $C_{bx_{sidewallg}} = C_{jpXg} \cdot \left(1 - \frac{v_{bx}}{P_{BSWG}}\right)^{-MJSWG}$
- else $C_{bx_{sidewallg}} = C_{jpXg} \cdot \left(1 + \frac{MJSWG \cdot v_{bx}}{P_{BSWG}}\right)$

5.7 Temperature updating

This is introduced in BSIM3v3.2, by using the two parameters **TPBSWG** and **TCJSWG** for the updating of **CJSWG** and **PBSWG**.

$$CJSWG(T) = CJSWG \cdot (1 + TCJSWG \cdot \delta T)$$

$$PBSWG(T) = PBSWG - (TPBSWG \cdot \delta T)$$

5.8 Diode IV model

The diode IV modeling supports a resistance-free diode model and a current-limiting feature by introducing the model parameter **IJTH** (default 0.1A). If **IJTH** is explicitly specified to be zero, a resistance-free diode model will be triggered; otherwise two critical junction voltages, **Vjsm** for S/B diode, and **Vjdm** for D/B diode, will be computed from the value of **IJTH**. This model can be selected by setting **DIOLEV=7** in the model card with **VER=3.2**.

5.9 Modeling the S/B Diode

If the S/B saturation current **Isbs** is larger than zero, the following equations are used to calculate the S/B diode current **Ibs**.

- **IJTH** is equal to zero: A resistance-free diode.

$$Ibs = Isbs \left(\exp\left(\frac{Vbs}{N \cdot Vth}\right) - 1 \right) + G_{min} Vbs$$

where $N \cdot Vth = (NJ \cdot (k_B T)) / q$; **NJ** is a model parameter, known as the junction emission coefficient.

- **IJTH** is non-zero: Current limiting feature.

If $Vbs < Vjsm$:

$$Ibs = Isbs \left(\exp\left(\frac{Vbs}{N \cdot Vth}\right) - 1 \right) + G_{min} Vbs$$

otherwise:

$$Ibs = IJTH + \frac{IJTH + Isbs}{N \cdot Vth} (Vbs - Vjsm) + G_{min} Vbs$$

with **Vjsm** computed by:

$$V_{jsm} = N \cdot V_{th} \cdot \ln\left(\frac{IJTH}{Isbs} + 1\right)$$

The saturation current $Isbs$ is given by:

$$Isbs = AS \cdot JS(T) + PS \cdot JSW(T)$$

where $JS(T)$ is the junction saturation current density, AS is the source junction area, $JSW(T)$ is the sidewall junction saturation current density, PS is the perimeter of the source junction. $JS(T)$ and $JSW(T)$ are functions of temperature and can be written as:

$$JS(T) = JS \cdot \exp\left(\frac{\frac{Eg(T_{nom})}{V_{th}(T_{nom})} - \frac{Eg(T)}{V_{th}(T)} + XTI \cdot \ln\left(\frac{T}{T_{nom}}\right)}{NJ}\right)$$

$$JSW(T) = JSW \cdot \exp\left(\frac{\frac{Eg(T_{nom})}{V_{th}(T_{nom})} - \frac{Eg(T)}{V_{th}(T)} + XTI \cdot \ln\left(\frac{T}{T_{nom}}\right)}{NJ}\right)$$

The energy band-gap $Eg(T_{nom})$ and $Eg(T)$ at the nominal and operating temperatures are expressed as follows:

$$Eg(T_{nom}) = 1.16 - 7.02 \times 10^{-4} \cdot \frac{T_{nom}^2}{T_{nom} + 1108}$$

$$Eg(T) = 1.16 - 7.02 \times 10^{-4} \cdot \frac{T^2}{T + 1108}$$

In the above derivations, JS is the saturation current density at T_{nom} . If JS is not given, $JS = 1 \times 10^{-4} \text{ Am}^{-2}$. JSW is the sidewall saturation current density at T_{nom} , with a default value of zero.

If $Isbs$ is not positive, Ibs is calculated by:

$$Ibs = G_{min} \cdot Vbs$$

5.10 Modeling the D/B Diode

If the D/B saturation current $Isbd$ is larger than zero, the following equations are used to calculate the D/B diode current Ibd .

- $IJTH$ is equal to zero: A resistance-free diode.

$$Ibd = Isbd \left(\exp\left(\frac{Vbd}{N \cdot Vth}\right) - 1 \right) + G_{min} Vbd$$

- $IJTH$ is non-zero: Current limiting feature.

If $Vbd < Vjdm$:

$$Ibd = Isbd \left(\exp\left(\frac{Vbd}{N \cdot Vth}\right) - 1 \right) + G_{min} Vbd$$

otherwise:

$$Ibd = IJTH + \frac{IJTH + Isbd}{N \cdot Vth} (Vbd - Vjdm) + G_{min} Vbd$$

with $Vjdm$ computed by:

$$Vjdm = N \cdot Vth \cdot \ln\left(\frac{IJTH}{Isbd} + 1\right)$$

The saturation current $Isbd$ is given by:

$$Isbd = Ad \cdot Js(T) + Pd \cdot Jsw(T)$$

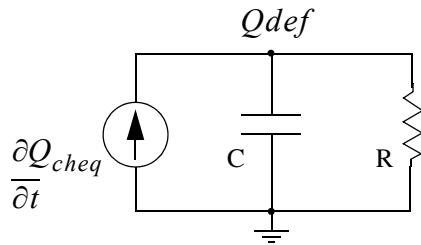
where Ad is the drain junction area and Pd is the perimeter of the drain junction. If $Isbd$ is not positive, Ibd is calculated by:

$$Ibd = G_{min} \cdot Vbd$$

6.0 Non-Quasi-Static (NQS) Model Equations

For the BSIM3v3 model, a new node Q_{def} is added to the device to take into account the amount of excessive charge in the device channel.

Using the relaxation time concept, the NQS transient effect is implemented with the following subcircuit:



The R-C value is the relaxation time constant for charging and discharging the channel. Q_{def} will decay exponentially into the channel with a bias dependent NQS relaxation time τ ; where τ is the overall relaxation time in the channel and Q_{cheq} is the global channel charge.

$$\frac{1.0}{\tau} = \frac{1.0}{\tau_{diff}} + \frac{1.0}{\tau_{drift}}$$

$$Q_{cheq} = Q_{drain} + Q_{source} = -(Q_{gate} + Q_{bulk})$$

Under strong inversion, conduction is mainly due to drift current and is given by:

$$\tau_{drift} = \frac{COX \cdot W_{eff} \cdot L_{eff}^3}{ELM \cdot \mu_{eff} \cdot Q_{cheq}}$$

Under weak inversion, conduction is mainly due to diffusion current and is given by:

$$\tau_{diff} = \frac{L_{eff}^2}{16 \cdot \mu_{eff} \cdot V_t}$$

Then Q_{def} is assigned to the source, drain, gate dynamic currents as:

$$i_s = -Ids_{DC} + X_s \cdot \frac{Q_{def}}{\tau}$$

$$i_d = Ids_{DC} + X_d \cdot \frac{Q_{def}}{\tau}$$

Where X_d and X_s are the partitioning parameters ($X_d + X_s = 1$):

$$X_d = \left(\frac{Q_{drain}}{Q_{drain} + Q_{source}} \right)$$

$$X_s = \left(\frac{Q_{source}}{Q_{source} + Q_{drain}} \right)$$

In BSIM3v3.2 the charge partitioning scheme used in the quasi-static model is used here together with the two above equations, with checking the value of Q_{cheq} . In this case:

if $Q_{cheq} \leq 10 - 5 \cdot COX \cdot Wactive \cdot Lactive$

If $XPART < 0.5$, $X_d = 0.4$.

else if $XPART > 0.5$, $X_d = 0.0$.

else $X_d = 0.5$.

otherwise use the equations of $X_d = Q_{drain} / Q_{cheq}$

The BSIM3v3 model includes a first-order NQS model for small signal (.AC) simulations. The expression of Q_{def} is obtained by:

$$Q_{def}(S) = \frac{\tau \cdot S}{1.0 + \tau \cdot S} \cdot Q_{cheq}(S)$$

The corresponding small signal transadmittances are then given by:

$$Y_m(S) = g_m + \frac{\partial}{\partial v_{gs}} \left(X_d \cdot \frac{S}{1.0 + \tau \cdot S} \cdot Q_{cheq} \right)$$

$$Y_{ms}(S) = g_{ms} + \frac{\partial}{\partial v_{bs}} \left(X_d \cdot \frac{S}{1.0 + \tau \cdot S} \cdot Q_{cheq} \right)$$

$$Y_{mbs}(S) = Y_{ms}(S) - (Y_m(S) - g_{ds})$$

7.0 Temperature Effects

The temperature related equations are as follows:

$$V_t(T) = \frac{k_B \cdot T}{q}$$

$$Eg(T) = 1.16 - 7.02 \times 10^{-4} \cdot \frac{T^2}{T + 1108}$$

$$ni(T) = NI \cdot \left(\frac{T}{300.15} \right)^{1.5} \cdot \exp \left(21.5565981 - \frac{Eg(T)}{2 \cdot V_t(T)} \right)$$

$$DVth0(T) = \left(KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot v_{bs} \right) \cdot \left(\frac{T}{TNOM} - 1 \right)$$

$$\mu_0(T) = U0 \cdot \left(\frac{T}{TNOM} \right)^{UTE}$$

$$\mu_A(T) = UA + UA1 \cdot \left(\frac{T}{TNOM} - 1 \right)$$

$$\mu_B(T) = UB + UB1 \cdot \left(\frac{T}{TNOM} - 1 \right)$$

$$\mu_C(T) = UC + UC1 \cdot \left(\frac{T}{TNOM} - 1 \right)$$

$$RdsW(T) = RDSW + PRT \cdot \left(\frac{T}{TNOM} - 1 \right)$$

$$Vsat(T) = VSAT - AT \cdot \left(\frac{T}{TNOM} - 1 \right)$$

if (**UPDATEPHI** = 1)

PHI is internally calculated as: $\text{PHI}(T) = 2 \cdot V_t(T) \cdot \ln\left(\frac{NCH}{ni(T)}\right)$

VBI is internally calculated as: $\text{VBI}(T) = V_t(T) \cdot \ln\left(\frac{ND \cdot NCH}{ni(T)^2}\right)$

8.0 Noise Model

8.1 General

Eldo has different thermal and flicker noise models for Mosfets. You can choose any of these models using either the model parameters **THMLEV** and **FLKLEV**, or with **.OPTION thermal_noise=VAL** and **.OPTION flicker_noise=VAL**.

The default value for **THMLEV** and **FLKLEV** is 0.

Some models replace the default model (model 0) by their own internal default model. EKV are examples of these models. Therefore, when you specify **THMLEV=0** in EKV, you actually choose the internal default model of EKV and not the default model of Eldo. Nevertheless, you can still use any of the other models specified by values not equal to 0.

Concerning BSIM3v3, as mentioned above, to enable it to choose its own internal model, you have to set **THMLEV** and **FLKLEV** to 0. The internal model itself is divided into submodels selected by the model parameter **NOIMOD**. **NOIMOD** can take a value from 1 to 4 to select the required combination of thermal & flicker noise models. These models are explained in the next section.

It is clear that **NOIMOD** has no effect on the thermal noise if **THMLEV** is specified to a value not equal to 0 (or equal to 0 with **NOIFLAG=1**). Similarly, **NOIMOD** has no effect on the flicker noise if **FLKLEV** is specified to a value not equal to 0 (or equal to 0 with **NOIFLAG=1**). Consequently, **NOIMOD** is only effective if the noise parameter (**THMLEV** or **FLKLEV**) is set to 0 to be able to choose the internal default model of BSIM3v3 and not the default model of Eldo. If **NOIFLAG=1**, Eldo will choose the default model.

8.2 BSIM3v3 Noise Models

Specific BSIM3v3 noise model is implemented in Eldo by default as **FLKLEV = 0** and **THMLEV = 0**. All other Eldo noise models are available by setting **FLKLEV** and **THMLEV** in the model statement or by the following command:

```
.option thermal_noise=<VAL> flicker_noise=<VAL>
```

With the **NOIMOD** parameter it is possible to use different combinations of thermal and flicker noise models as shown in the table below:

NOIMOD	Spice2		BSIM3	
	Thermal	Flk	Thermal	Flk
1	✓	✓		
2			✓	✓
3	✓			✓
4		✓	✓	

8.3 Thermal Noise

The channel conductance Thermal Noise is defined as follows:

$$\text{For } \mathbf{NOIMOD} = 1 \& 3: \overline{i_{n, th}^2} = \frac{8k_B T}{3} \cdot (g_m + g_{ds} + g_{mb}) \cdot \Delta f$$

For **NOIMOD = 2 & 4:**

$$\text{If } VER = 3.24: \overline{i_{n, th}^2} = \frac{4k_B T \mu_{eff}}{L_{eff}^2 + \mu_{eff} |Q_{inv}| \cdot R_{ds}} \cdot |Q_{inv}| \cdot \Delta f$$

$$\text{Else: } \overline{i_{n, th}^2} = \frac{4k_B T \mu_{eff}}{L_{eff}^2} \cdot |Q_{inv}| \cdot \Delta f$$

If **VER = 3.2:**

Q_{inv} is the inversion channel charge computed from the capacitance models (**CAPMOD = 0, 1, 2 or 3**).

$$\text{Else: } Q_{inv} = -C_{eff} \cdot Vgst_{eff} \cdot \left(1 - \frac{A_{bulk}}{2(Vgst_{eff} + 2V_t)} \cdot Vds_{eff} \right)$$

8.4 Flicker Noise Model

The Flicker Noise Model is defined as follows:

$$\text{For } NOIMOD = 1 \& 4: \overline{i_{n,f}^2} = \frac{KF \cdot Ids^{AF}}{Cox \cdot L_{eff}^2 \cdot f^{EF}}$$

For **NOIMOD = 2 & 3:**

- If **VER = 3.24** the following equations are used:

if **KSTAR** is specified, **NOIB** is calculated from it as follows:

$$NOIB = \frac{KSTAR}{K \cdot T \cdot Cox \cdot Vgst_{eff}}$$

else **NOIB** is used as specified or by its default value if not specified.

When $vgs \geq Vth + 0.1$:

$$S_{si} = \frac{q^2 \cdot V_t \cdot \mu_{eff} \cdot Ids}{1 \times 10^8 \cdot Cox \cdot A_{bulk} \cdot L_{eff}^2 \cdot f^{EF}} \cdot \left[NOIA \cdot \log\left(\frac{N_0 + NSTAR}{N_l + NSTAR}\right) + NOIB \cdot (N_0 - N_l) + NOIC \cdot \frac{N_0^2 - N_l^2}{2} \right] + \frac{V_t \cdot Ids^2 \cdot \Delta L_{clm}}{W_{eff} \cdot L_{eff}^2 \cdot f^{EF}} \cdot \frac{NOIA + NOIB \cdot N_l + NOIC \cdot N_l^2}{(N_l + NSTAR)^2}$$

with:

$$N_0 = \frac{Cox}{q} \cdot V_{gst_{eff}} \quad N_l = \frac{Cox}{q} \cdot V_{gst_{eff}} \cdot \left(1 - \frac{A_{bulk} \cdot V_{ds_{eff}}}{V_{gst_{eff}} + 2V_t}\right)$$

if $vds > V_{dsat}$ $\Delta L_{clm} = Litl \cdot \log\left(\frac{vds - V_{ds_{eff}}}{Litl \cdot Esat} + \frac{EM}{Esat}\right)$ else $\Delta L_{clm} = 0$

Note that if the value of parameter EM is zero, ΔL_{clm} is set to zero.

then: $\overline{i_{n,f}^2} = S_{si} \cdot \Delta f$

When $vgs < Vth + 0.1$:

$$S_{limit} = S_{si}(vgs = Vth + 0.1)$$

$$S_{wi} = \frac{NOIA \cdot V_t \cdot Ids^2}{1 \times 10^8 \cdot W_{eff} \cdot L_{eff} \cdot f^{EF} \cdot (NSTAR)^2}$$

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{limit}}{S_{wi} + S_{limit}} \cdot \Delta f$$

If **FLKFLAG** is set to 1, **Swi** is always used in conjunction with **Ssi** even if $Vgs > Vth + 0.1$; i.e. if (**FLKFLAG**=1)

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{si}}{S_{wi} + S_{si}} \cdot \Delta f$$

Note that if the value of the quantity **Swi** + **Ssi** is negative the whole spectral density is set to zero.

- Else if $VER < 3.24$ the following equations are used:

if $KSTAR$ is specified, $NOIB$ is calculated from it as follows:

$$NOIB = \frac{KSTAR}{K \cdot T \cdot Cox \cdot (Vgs - Vth)}$$

else $NOIB$ is used as specified or by its default value if not specified.

When $vgs \geq Vth + 0.1$:

$$S_{si} = \frac{q^2 \cdot V_t \cdot \mu_{eff} \cdot Ids}{1 \times 10^8 \cdot Cox \cdot L_{eff}^2 \cdot f^{EF}} \cdot \left[NOIA \cdot \log\left(\frac{N_0 + NSTAR}{N_l + NSTAR}\right) + NOIB \cdot (N_0 - N_l) + NOIC \cdot \frac{N_0^2 - N_l^2}{2} \right] + \frac{V_t \cdot Ids^2 \cdot \Delta L_{clm}}{W_{eff} \cdot L_{eff}^2 \cdot f^{EF}} \cdot \frac{NOIA + NOIB \cdot N_l + NOIC \cdot N_l^2}{(N_l + NSTAR)^2}$$

with:

$$N_0 = \frac{Cox}{q} \cdot (Vgs - Vth) \quad N_l = \frac{Cox}{q} \cdot (Vgs - Vth - \min(vds, Vdsat))$$

$$\text{if } vds > Vdsat \quad \Delta L_{clm} = Litl \cdot \log\left(\frac{vds - Vdsat}{Litl \cdot Esat} + EM\right) \quad \text{else } \Delta L_{clm} = 0$$

Note that if the value of parameter EM is zero, ΔL_{clm} is set to zero.

$$\text{then: } \overline{i_{n,f}^2} = S_{si} \cdot \Delta f$$

When $vgs < Vth + 0.1$:

$$S_{limit} = S_{si}(vgs = Vth + 0.1) \quad S_{wi} = \frac{NOIA \cdot V_t \cdot Ids^2}{1 \times 10^8 \cdot W_{eff} \cdot L_{eff} \cdot f^{EF} \cdot (NSTAR)^2}$$

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{limit}}{S_{wi} + S_{limit}} \cdot \Delta f$$

If **FLKFLAG** is set to 1, **Swi** is always used in conjunction with **Ssi** even if $Vgs > Vth + 0.1$; i.e. if (**FLKFLAG**=1)

When $vgs \geq Vth + 0.1$:

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{si}}{S_{wi} + S_{si}} \cdot \Delta f$$

When $vgs < Vth + 0.1$:

$$S_{limit} = S_{si}(vgs = Vth + 0.1)$$

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{limit}}{S_{wi} + S_{limit}} \cdot \Delta f$$

Note that if the value of the quantity **Swi** + **Ssi** is negative the whole spectral density is set to zero.

9.0 Model Parameters

Nr.	Name	Description	Default	Units
1	VER (VERSION)	Version Selector	3.24	
2	PARAMCHK	Model parameters range checking flag	0	
Threshold Parameters				
3	VTH0 (VTHO)	Threshold voltage at vbs=0 for large L	a	V
4	DELVT0 (DELVTO)	Zero-bias threshold voltage shift. Can be specified as a model and/or element parameter; they are added together	0	V
5	VFB	DC flatband voltage	-1 ^b	V
6	VBM	Maximum applied body bias in Vth calculation	-5	V
7	K1	First order body effect coefficient	0.53 ^c	V ^{1/2}
8	K2	Second order body effect coefficient	-0.0186 ^b	
9	K3	Narrow width coefficient	80	
10	K3B	Body effect coefficient of K3	0	V ⁻¹
11	W0 (WO)	Narrow width parameter	2.5×10 ⁻⁶	m

Nr.	Name	Description	Default	Units
12	NLX	Lateral non-uniform doping parameter	1.74×10^{-7}	m
13	DVT0W (DVTOW)	First coefficient of narrow width effect at small L	0	
14	DVT1W	Second coefficient of narrow width effect at small L	5.3×10^6	m^{-1}
15	DVT2W	Body coefficient of narrow width effect at small L	-3.2×10^{-2}	V^{-1}
16	DVT0 (DVTO)	First coefficient of short-channel effect on Vth	2.2	
17	DVT1	Second coefficient of short-channel effect on Vth	0.53	
18	DVT2	Body coefficient of short-channel effect on Vth	-3.2×10^{-2}	V^{-1}
Subthreshold Parameters				
19	VOFF	Offset voltage in subthreshold for high W and L	-0.08	V
20	NFACTOR	Subthreshold swing factor	1	
21	ETA0 (ETAO)	DIBL coefficient in subthreshold	0.08	
22	ETAB	Body-bias coefficient for DIBL effect in subthreshold	-0.07	V^{-1}
23	DSUB	DIBL coefficient exponent	DROUT	
24	CIT	Interface trap capacitance	0	Fm^{-2}
25	CDSC	Drain/source to channel coupling resistance	2.4×10^{-4}	Fm^{-2}
26	CDSCB	Body-bias coefficient of CDSC	0	$\text{FV}^{-1}\text{m}^{-2}$
27	CDSCD	Drain-bias coefficient of CDSC	0	$\text{FV}^{-1}\text{m}^{-2}$
Saturation Parameters				
28	MOBMOD	Mobility model selector	1	
29	U0 (UO)	Mobility at nominal temperature	0.067 (N) 0.025 (P)	$\text{m}^2(\text{Vs})^{-1}$
30	UA	First-order mobility degradation coefficient	2.25×10^{-9}	mV^{-1}
31	UB	Second-order mobility degradation coefficient	5.87×10^{-19}	$(\text{mV}^{-1})^2$
32	UC	Body effect of mobility degradation coefficient (MOBMOD=1,2) (MOBMOD=3)	- 4.65×10^{-11} -0.0465	mV^{-2} V^{-1}
33	VSAT	Saturation velocity	8.0×10^4	ms^{-1}
34	AGS	Gate bias coefficient of Bulk charge effect	0	V^{-1}
35	A0 (AO)	Bulk charge effect coefficient for channel length	1	
36	B0 (BO)	Bulk charge effect coefficient for channel width	0	m
37	B1	Bulk charge effect width offset	0	m
38	KETA	Body-bias coefficient of bulk charge effect	-0.047	V^{-1}
39	A1	First non-saturation effect parameter	0	V^{-1}

Nr.	Name	Description	Default	Units
40	A2	Second non-saturation effect parameter	1	
41	RDSW	Parasitic resistance per unit width	0	$\Omega \mu\text{m}^{\text{WR}}$
42	PRWG	Gate coefficient of RDSW	0	V^{-1}
43	PRWB	Body coefficient of RDSW	0	$\text{V}^{-1/2}$
44	WR	Width offset for RDS calculation	1	
45	PCLM	Channel length modulation parameter	1.3	
46	PDIBLC1	First DIBL effect coefficient in output resistance	0.39	
47	PDIBLC2	Second DIBL effect coefficient in output resistance	0.0086	
48	PDIBLCB	Body-bias coefficient of DIBL	0	V^{-1}
49	DROUT	L dependence exponent in DIBL	0.56	
50	PSCBE1	First substrate current body-effect parameter	4.24×10^8	Vm^{-1}
51	PSCBE2	Second substrate current body-effect parameter	1.0×10^{-5}	mV^{-1}
52	PVAG	Gate dependence of Early voltage	0	
53	DELTA	Effective Vds parameter	0.01	V
Ionization Current Parameters				
54	ALPHA0 (ALPHAO)	First impact ionization current parameter	0	mV^{-1}
55	ALPHA1	Substrate current parameter	0	V^{-1}
56	BETA0 (BETAO)	Second impact ionization current parameter	30	V
57	IIMOD	Impact ionization switch	0	
Temperature Effect Parameters				
58	KT1	Temperature coefficient of threshold voltage	-0.11	V
59	KT1L	Length sensitivity of KT1	0	mV
60	KT2	Body-bias sensitivity of KT1	0.022	
61	UTE	Mobility temperature exponent	-1.5	
62	UA1	Temperature coefficient for UA	4.31×10^{-9}	mV^{-1}
63	UB1	Temperature coefficient for UB	-7.61×10^{-18}	$(\text{mV}^{-1})^2$
64	UC1	Temperature coefficient for UC (MOBMOD=1,2)	-5.6×10^{-11}	mV^{-2}
		Temperature coefficient for UC (MOBMOD=3)	-0.056	V^{-1}
65	AT	Temperature coefficient for saturation velocity	3.3×10^4	ms^{-1}
66	PRT	Temperature coefficient for RDSW	0	$\Omega \mu\text{m}$
Dynamic Parameters				
67	CAPMOD	Flag for capacitance model	1	
68	XPART	Flag for partitioning model	0	

Nr.	Name	Description	Default	Units
69	CGSO	Non LDD region source-gate overlap capacitance per width	d	Fm ⁻¹
70	CGDO	Non LDD region drain-gate overlap capacitance per width	e	Fm ⁻¹
71	CGBO	Bulk-gate overlap capacitance per length	0	Fm ⁻¹
72	CGSL (CGS1)	Light doped source-gate region overlap capacitance	0	Fm ⁻¹
73	CGDL (CGD1)	Light doped drain-gate region overlap capacitance	0	Fm ⁻¹
74	CKAPPA	Coefficient for lightly doped region overlap capacitance	0.6	V
75	CF	Fringing field capacitance	7.3×10 ^{-5f}	Fm ⁻¹
76	CLC	Constant term for short channel model	1.0×10 ⁻⁷	m
77	CLE	Exponential term for short channel model	0.6	
78	NOFF	CV parameter in VgsteffCV for the weak to strong inversion region	1	
79	VOFFCV	CV parameter in VgsteffCV for the weak to strong inversion region	0	V
80	ACDE	Exponential coefficient for charge thickness in the accumulation and depletion regions	1	mV ⁻¹
81	MOIN	Coefficient for the gate-bias dependent surface potential	15	V ^{1/2}
Non-Quasi-Static Parameters				
82	NQSMOD	Flag for the Non-Quasi-Static model	0	
83	ELM	Elmore constant of the channel	5	
Process Parameters				
84	GAMMA1	Body effect coefficient near the surface	g	V ^{1/2}
85	GAMMA2	Body effect coefficient in the bulk	h	V ^{1/2}
86	VBX	vbs at which depletion width equals xt	i	V
87	XT	Doping depth	1.55×10 ⁻⁷	m
88	TOX	Gate oxide thickness	1.5×10 ⁻⁸	m
89	TOXM	Gate oxide thickness TOX value at which parameters are extracted	TOX	m
90	DTOXCV	Adjusting parameter for gate oxide thickness in C-V model for CAPMOD=3	0	
91	XJ	Junction depth	1.5×10 ⁻⁷	m
92	NCH (NPEAK)	Channel doping	1.7×10 ^{17j}	cm ⁻³
93	NSUB	Substrate doping	6.0×10 ¹⁶	cm ⁻³

Nr.	Name	Description	Default	Units
94	NGATE	Poly-gate doping	0	cm^{-3}
95	ND	Drain-source doping	1.0×10^{20}	cm^{-3}
Width & Length Parameters				
96	LINT	Length offset on one side for I-V	0	m
97	WINT	Width offset on one side for I-V without bias	0	m
98	DWG	Coefficient of W_{eff} 's gate dependence	0	mV^{-1}
99	DWB	Coefficient of W_{eff} 's bulk dependence	0	$\text{mV}^{-1/2}$
100	DLC	Length offset on one side for C-V	LINT	m
101	DWC	Width offset on one side for C-V	WINT	m
102	WL	Coefficient of length dependence for width offset	0	m^{WLN}
103	WLC	Coefficient of length dependence for C-V width offset	WL	m^{WLN}
104	WLN	Power of length dependence for width offset	1	
105	WW	Coefficient of width dependence for width offset	0	m^{WWN}
106	WWC	Coefficient of width dependence for C-V width offset	WW	m^{WWN}
107	WWN	Power of width dependence for width offset	1	
108	WWL	Coefficient of length and width cross-term for width offset	0	$\text{m}^{WLN+WWN}$
109	WWLC	Coefficient of length and width cross-term for C-V width offset	WWL	$\text{m}^{WLN+WWN}$
110	LL	Coefficient of length dependence for length offset	0	m^{LLN}
111	LLC	Coefficient of length dependence for C-V length offset	LL	m^{LLN}
112	LLN	Power of length dependence for length offset	1	
113	LW	Coefficient of width dependence for length offset	0	m^{LWN}
114	LWC	Coefficient of width dependence for C-V length offset	LW	m^{LWN}
115	LWN	Power of width dependence for length offset	1	
116	LWL	Coefficient of length and width cross-term for length offset	0	$\text{m}^{LLN+LWN}$
117	LWLC	Coefficient of length and width cross-term for C-V length offset	LWI	$\text{m}^{LLN+LWN}$
118	XL	Etching effects on Length	0	m
119	XW	Etching effects on Width	0	m
Noise Parameters				
120	NOIMOD	Flag for noise model	1	
121	AF	Flicker noise frequency exponent for NOIMOD=1	1	

Nr.	Name	Description	Default	Units
122	KF	Flicker noise parameter	0	
123	EF	Flicker noise frequency exponent for NOIMOD=2	1	
124	EM	Maximum electric field	4.1×10^7	Vm^{-1}
125	NOIA	First Flicker noise parameter	1×10^{20} (N)	
			9.9×10^{18} (P)	
126	NOIB	Second Flicker noise parameter	5×10^4 (N)	
			2.4×10^3 (P)	
127	NOIC	Third Flicker noise parameter	-1.4×10^{-12} (N)	
			1.4×10^{-12} (P)	
128	NSTAR	Fourth Flicker noise parameter	2.0×10^{20}	
129	KSTAR	Fourth Flicker noise parameter		
130	FLKFLAG	Flicker noise selector used in case NOIMOD=2, 3	0	
131	GDSNOI	Thermal noise scaling factor in case option ACM is used and THMLEV=1	1^k	
132	NOIFLAG	Flag to enable the internal Eldo default noise equation	0 ^l	
Diode Parameters (Added in Version 3.2)				
133	IJTH	Diode limiting current	calculated	A
134	TPB (PTA)	Temperature coefficient of PB^m	0	$\text{V}^\circ\text{K}^{-1}$
135	TPBSW (PTP)	Temperature coefficient of $PBSW^n$	0	$\text{V}^\circ\text{K}^{-1}$
136	TCJ (CTA)	Temperature coefficient of CJ^0	0	$^\circ\text{K}^{-1}$
137	TCJSW (CTP)	Temperature coefficient of $CJSW^p$	0	$^\circ\text{K}^{-1}$
Junction Capacitance/Charge Model Parameters				
138	CJSWG	Source-drain gate sidewall junction capacitance per unit length at zero bias	CJSW	Fm^{-1}
139	MJSWG	Source-drain gate sidewall junction capacitance grading coefficient	MJSW	
140	PBSWG	Source-drain gate sidewall junction built-in potential	PBSW	V
141	TPBSWG	Temperature coefficient of $PBSWG$	0	$\text{V}^\circ\text{K}^{-1}$
142	TCJSWG	Temperature coefficient of $CJSW^p$	0	$^\circ\text{K}^{-1}$
BSIM4 Gate Current Model				
143	IGCMOD	Gate-to-channel tunneling current model selector	0	
144	IGBMOD	Gate-to-substrate tunneling current model selector	0	
145	TOXE	Electrical gate equivalent oxide thickness	3.0e-9	m
146	TOXREF	Nominal gate oxide thickness for gate dielectric tunneling current model only	3.0e-9	m

Nr.	Name	Description	Default	Units
147	DLCIG	Source/drain overlap length for I_{gs} and I_{gd}	LINT	
148	AIGC	Parameter for I_{gcs} and I_{gcd}	0.054 (NMOS) 0.31 (PMOS)	(Fs ² /g) ^{0.5} m ⁻¹
149	BIGC	Parameter for I_{gcs} and I_{gcd}	0.054 (NMOS) 0.024 (PMOS)	(Fs ² /g) ^{0.5} m ⁻¹ V ⁻¹
150	CIGC	Parameter for I_{gcs} and I_{gcd}	0.006	V ⁻¹
151	NIGC	Parameter for I_{gcs} , I_{gcd} , I_{gs} and I_{gd}	1.0	
152	AIGSD	Parameter for I_{gs} and I_{gd}	0.43 (NMOS) 0.31 (PMOS)	(Fs ² /g) ^{0.5} m ⁻¹
153	BIGSD	Parameter for I_{gs} and I_{gd}	0.054 (NMOS) 0.024 (PMOS)	(Fs ² /g) ^{0.5} m ⁻¹ V ⁻¹
154	CIGSD	Parameter for I_{gs} and I_{gd}	0.075 (NMOS) 0.03 (PMOS)	V ⁻¹
155	AIGBACC	Parameter for I_{gb} in accumulation	0.43	(Fs ² /g) ^{0.5} m ⁻¹
156	BIGBACC	Parameter for I_{gb} in accumulation	0.054	(Fs ² /g) ^{0.5} m ⁻¹
157	CIGBACC	Parameter for I_{gb} in accumulation	0.075	V ⁻¹
158	AIGBINV	Parameter for I_{gb} in inversion	0.35	(Fs ² /g) ^{0.5} m ⁻¹
159	BIGBINV	Parameter for I_{gb} in inversion	0.03	(Fs ² /g) ^{0.5} m ⁻¹ V ⁻¹
160	CIGBINV	Parameter for I_{gb} in inversion	0.006	V ⁻¹
161	PIGCD	V_{ds} dependence of I_{gcs} and I_{gcd}	1.0	
162	POXEDGE	Factor for the gate oxide thickness in source/drain overlap regions	1.0	
163	NTOX	Exponent for the gate oxide ratio	1.0	
164	NSD	Source/drain doping concentration Fatal error if not positive	1.0e20	cm ⁻³
165	NIGBACC	Parameter for I_{gb} in accumulation	1.0	
166	NIGBINV	Parameter for I_{gb} in inversion	3.0	
167	EIGBINV	Parameter for I_{gb} in inversion	1.1	V

BSIM4 Gate-Induced Drain Leakage Model Parameters

168	AGIDL	Pre-exponential coefficient for GIDL	0.0	mho
169	BGIDL	Exponential coefficient for GIDL	2.3e9	V/m
170	CGIDL	Parameter for body-bias effect on GIDL	0.5	V ³
171	EGIDL	Fitting parameter for band bending for GIDL	0.8	V
172	DWJ	Offset of the S/D junction width	DWC	

- a. If $VTH0$ is not specified, it is calculated using VFB , PHI and $K1$.
- b. If $VTH0$ is specified, VFB is calculated using $VTH0$, PHI and $K1$.
- c. If both $K1$ and $K2$ are not specified, they are calculated using $GAMMA1$, $GAMMA2$, PHI , VBX , VBM .
- d. If $CGSO$ is not specified, it is calculated using DLC , XJ and Cox .

- e. If **CGDO** is not specified, it is calculated using **DLC**, **XJ** and **Cox**.
- f. If **CF** is not specified, it is calculated using **TOX**.
- g. If **GAMMA1** is not specified, it is calculated using **NCH** and **Cox**.
- h. If **GAMMA2** is not specified, it is calculated using **NSUB** and **Cox**.
- i. If **VBX** is not specified, it is calculated using **PHI**, **NCH** and **XT**.
- j. If **GAMMA1** is specified, **NCH** is calculated using **GAMMA1** and **Cox**.
- k. **GDSNOI** will function only when specified in the **.OPTION ACM** command and when **THMLEV=1**.
- l. **NOIFLAG** is a model parameter set to 1 only when **THMLEV=0** and the user wants to enable the internal Eldo default noise equation.
- m. If It is an alias to the parameter **PTA**, and the related equations are in the Common Equations chapter, **TLEV** must be equal 1 to be able to use this parameter.
- n. If It is an alias to the parameter **PTB**, and the related equations are in the Common Equations chapter, **TLEV** must be equal 1 to be able to use this parameter.
- o. If It is an alias to the parameter **CTA**, and the related equations are in the Common Equations chapter, **TLEV** must be equal 1 to be able to use this parameter.
- p. If It is an alias to the parameter **CTP**, and the related equations are in the Common Equations chapter, **TLEV** must be equal 1 to be able to use this parameter.

9.1 Notes about Parameters

- **NCH**, **NGATE** and **U0** may be entered in meters or centimeters:
NCH is converted to cm^{-3} as follows: if **NCH** is greater than 10^{20} , it is multiplied by 10^{-6} .
NGATE is converted to cm^{-3} as follows: if **NGATE** is greater than 10^{23} , it is multiplied by 10^{-6} .
U0 is converted to $\text{m}^2(\text{Vs})^{-1}$ as follows: if **U0** is greater than 1, it is multiplied by 10^{-4} .
NSUB must be entered in cm^{-3} .
- Specific BSIM3v3 initialization for parasitic common approach MOS parameters:
For **ALEV**, **RLEV**, **DCAPLEV** and **DIOLEV** please refer to the table in the [Common Equations](#) chapter.
 $C_J = 5 \times 10^{-4}$; $C_{JSW} = 5 \times 10^{-10}$; $P_B = 1$; $P_{BSW} = 1$;
FC is not a BSIM3v3 parameter, therefore it is set to 0.
As a consequence, you may use **LD**, **WD** instead of **LINT**, **WINT** or **DL**, **DW** instead of **DLC**, **DWC**. Respectively, **LINT**, **WINT** and **DLC**, **DWC** will be used for common equation initialization.
- As **LINT** and **LD** are both the same the user should only specify one parameter (**LINT** or **LD**). If both **LINT** and **LD** are specified then Eldo will return the following warning:

Double definition for parameter(s) LD.

Only the value of **LD** will be printed in the .chi file.

- For derivative computation in BSIM3v3, a parameter **DERIV** has been added. By default, **DERIV**=1 for analytical derivatives. **DERIV** may be set to 0 (or with the command **.option mnumer**) for the finite difference method.
- The different versions, BSIM3v3.2, BSIM3v3.1 and BSIM3v3, can also be selected by using the command **.option bsim3ver = 3.2, 3.1 or 3.0**.
- Parameter checking is added in BSIM3v3.2 to avoid bad values of certain parameters as follows:
 If **PSCBE2** ≤ 0.0, the user will be warned for the poor value used.
 If (**MOIN** < 5.0) or (**MOIN** > 25.0), a warning message will be given.
 If (**ACDE** < 0.4) or (**ACDE** > 1.6), a warning message will be given.
 If (**NOFF** < 0.1) or (**NOFF** > 4.0), a warning message will be given.
 If (**VOFFCV** < -0.5) or (**VOFFCV** > 0.5), a warning message will be given.
 If (**IJTH** < 0.0), fatal error occurs.
 If (**TOXM** <= 0.0), fatal error occurs

9.2 BSIM3v3 Binning Parameters

In this section, we provide the list of BSIM3v3 parameters which can be binned. For example, the **X0** parameter dependence with **Leff** and **Weff** is given by:

$$X0 = X0 + \frac{LX0}{Leff} + \frac{WX0}{Weff} + \frac{PX0}{Leff \times Weff}$$

In the case of **VTH0**; **LX0**, **WX0** and **PX0** are replaced by **LVTH0**, **WVTH0** and **PVTH0** respectively.

In the following, we give the BSIM3v3 parameters which can be binned and the corresponding binning parameters. The following parameters can be binned:

VTH0, VBM, K1, K2, K3, K3B, W0, NLX, DVT0W, DVT1W, DVT2W, DVT0, DVT1, DVT2, VOFF, NFACTOR, ETA0, ETAB, DSUB, CIT, CDSC, CDSCB, CDSCD, U0, UA, UB, UC, VSAT, AGS, A0, B0, B1, KETA, A1, A2, RDSW,

PRWG, PRWB, WR, PCLM, PDIBLC1, PDIBLC2, PDIBLCB, DROUT, PSCBE1, PSCBE2, PVAG, DELTA, ALPHA0, BETA0, KT1, KT1L, KT2, UTE, UAI, UB1, UC1, AT, PRT, CGSL, CGDL, CKAPPA, CF, CLC, CLE, ELM, GAMMA1, GAMMA2, VBX, XT, XJ, NCH, NSUB, NGATE, DWG, DWB, VFB, NOFF, VOFFCV, ALPHA1, ACDE, MOIN.

The corresponding binning parameters are shown in the table below:

LVTH0	WVTH0	PVTH0	LVBM	WVBM	PVBM
LK1	WK1	PK1	LK2	WK2	PK2
LK3	WK3	PK3	LK3B	WK3B	PK3B
LW0	WW0	PW0	LNlx	WNlx	PNlx
LDVT0W	WDVT0W	PDVT0W	LDVT1W	WDVT1W	PDVT1W
LDVT2W	WDVT2W	PDVT2W	LDVT0	WDVT0	PDVT0
LDVT1	WDVT1	PDVT1	LDVT2	WDVT2	PDVT2
LVOFF	WVOFF	PVOFF	LNFACtor	WNFACTOr	PNFACTOr
LETA0	WEta0	PETA0	LETAB	WEtab	PETAB
LDSUB	WDSUB	PDSUB	LCIT	WCIT	PCIT
LCDSC	WCDSC	PCDSC	LCDSCB	WCDSCB	PCDSCB
LCDSCD	WCDSCD	PCDSCD	LU0	WU0	PU0
LUA	WUA	PUA	LUB	WUB	PUB
LUC	WUC	PUC	LVSAT	WVSAT	PVSAT
LAGS	WAGS	PAGS	LA0	WA0	PA0
LB0	WB0	PB0	LB1	WB1	PB1
LKETA	WKETA	PKETA	LA1	WA1	PA1
LA2	WA2	PA2	LRDSW	WRDSW	PRDSW
LPRWG	WPRWG	PPRWG	LPRWB	WPRWB	PPRWB
LWR	WWR	PWR	LPCLM	WPCLM	PPCLM
LPDIBLC1	WPDIBLC1	PPDIBLC1	LPDIBLC2	WPDIBLC2	PPDIBLC2
LPDIBLCB	WPDIBLCB	PPDIBLCB	LDROUT	WDROUT	PDROUT
LPSCBE1	WPSCBE1	PPSCBE1	LPSCBE2	WPSCBE2	PPSCBE2

LPVAG	WPVAG	PPVAG	LDELTA	WDELTA	PDELTA
LALPHA0	WALPHA0	PALPHA0	LBETA0	WBETA0	PBETA0
LKT1	WKT1	PKT1	LKT1L	WKT1L	PKT1L
LKT2	WKT2	PKT2	LUTE	WUTE	PUTE
LUA1	WUA1	PUA1	LUB1	WUB1	PUB1
LUC1	WUC1	PUC1	LAT	WAT	PAT
LPRT	WPRT	PPRT	LCGSL	WCGSL	PCGSL
LCGDL	WCGDL	PCGDL	LCKAPPA	WCKAPPA	PCKAPPA
LCF	WCF	PCF	LCLC	WCLC	PCLC
LCLE	WCLE	PCLE	LELM	WELM	PELM
LGAMMA1	WGAMMA1	PGAMMA1	LGAMMA2	WGAMMA2	PGAMMA2
LVBX	WVBX	PVBX	LXT	WXT	PXT
LXJ	WXJ	PXJ	LNCH	WNCH	PNCH
LNSUB	WNSUB	PNSUB	LNGATE	WNGATE	PNGATE
LDWG	WDWG	PDWG	LDWB	WDWB	PDWB
LVFB	WVFB	PVFB	LNOFF	WNOFF	PNOFF
LVOFFFCV	WVOFFFCV	PVOFFFCV	LALPHA1	WALPHA1	PALPHA1
LACDE	WACDE	PACDE	LMOIN	WMOIN	PMOIN

9.3 BINUNIT Parameter Selector

This parameter (**BINUNIT**) is used for units selected of **Leff** and **Weff** in the binning equation:

If **BINUNIT** = 1, **Leff** and **Weff** have the units of micron.

If **BINUNIT** = 0, **Leff** and **Weff** have the units of meter.



If the binning parameters are used, the **VTH**, **PHI** and **VBI** are displayed in `name_file.chi` only in `.OP` case.

Note

10.0 Model Parameters Range Checking

The following table shows the model parameters range checking which is implemented in BSIM3v3. Some of them are conditioned by setting **PARAMCHK=1** and some are always checked.

Nr.	Condition	PARAMCHK	Result
Errors			
1	TOX ≤ 0		Error
2	TOXM ≤ 0		Error
3	IJTH < 0		Error
4	NCH ≤ 0		Error
5	NSUB ≤ 0		Error
6	NGATE < 0 or NGATE $> 1.0 \times 10^{25}$		Error
7	XJ < 0		Error
8	DVT1 < 0		Error
9	DVT1W < 0		Error
10	DSUB < 0		Error
11	DELTA < 0		Error
12	PCLM ≤ 0		Error
13	DROUT < 0		Error
14	CLC < 0		Error
15	CKAPPA ≤ 0		Error
16	U0(T) ≤ 0		Error
17	VSAT(T) ≤ 0		Error
18	NLX $< -Leff$		Error
19	W0 $= -Wj$		Error
20	B1 $= -Wj$		Error
Warnings not conditioned by PARAMCHK			
21	CAPMOD < 0 or CAPMOD > 3		Warning
22	VFBFLAG > 0 and CAPMOD $\neq 0$		Warning
23	XPART < 0		Warning
24	NQSMOD = 1 and XPART $\neq 0$		Warning
25	LREFF < 0		Warning
26	WREFF < 0		Warning
27	PHPG < 0.1		Warning
28	PSCBE2 ≤ 0		Warning

Nr.	Condition	PARAMCHK	Result
29	$\text{NOFF} < 0.1$ or $\text{NOFF} > 4$		Warning
30	$\text{VOFFCV} < -0.5$ or $\text{VOFFCV} > 0.5$		Warning
31	$\text{MOIN} < 5$ or $\text{MOIN} > 25$		Warning
32	$\text{ACDE} < 0.4$ or $\text{ACDE} > 1.6$		Warning
Warnings only if PARAMCHK=1			
33	$\text{TOX} < 1.0 \times 10^{-10}$	1	Warning
34	$\text{CGDO} < 0$	1	Warning
35	$\text{CGSO} < 0$	1	Warning
36	$\text{CGBO} < 0$	1	Warning
37	$\text{NLX} < 0$	1	Warning
38	$\text{NCH} \leq 1.0 \times 10^{15}$ or $\text{NCH} > 1.0 \times 10^{21}$	1	Warning
39	$\text{NSUB} \leq 1.0 \times 10^{14}$ or $\text{NSUB} > 1.0 \times 10^{21}$	1	Warning
40	$\text{NAGATE} \leq 1.0 \times 10^{18}$	1	Warning
41	$\text{DVT0} < 0$	1	Warning
42	$\text{NFACTOR} < 0$	1	Warning
43	$\text{CDSC} < 0$	1	Warning
44	$\text{CDSCD} < 0$	1	Warning
45	$\text{ETAO} < 0$	1	Warning
46	$\text{A2} < 0.01$ or $\text{A2} > 1$	1	Warning
47	$\text{RDSW} < 0$	1	Warning
48	$\text{PDIBL1} < 0$	1	Warning
49	$\text{PDIBL2} < 0$	1	Warning
50	$\text{VSAT(T)} < 1.0 \times 10^3$	1	Warning
51	$\text{Leff} < 1.0 \times 10^{-9}$	1	Warning
52	$\text{LeffCV} < 1.0 \times 10^{-9}$	1	Warning
53	$\text{Wj} < 1.0 \times 10^{-9}$	1	Warning
54	$\text{WjCV} < 1.0 \times 10^{-9}$	1	Warning
55	$1.0 \times 10^{-6}/(\text{W0}+\text{Wj}) > 10$	1	Warning
56	$1.0 \times 10^{-6}/(\text{B1}+\text{Wj}) > 10$	1	Warning
57	$\text{Rds} < 0.001$	1	Warning

11.0 Printing and Plotting BSIM3v3 Output States

The three capacitance states can be printed/plotted for any BSIM3v3 instance using the syntax `S (Mxx->state)`. For example, `CAPGDO` can be printed by specifying:

- `.PLOT DC S (Mxx->CAPGDO)` for DC or
- `.PLOT AC S (Mxx->CAPGDO)` for AC or
- `.PLOT TRAN S (Mxx->CAPGDO)` for TRAN

Table 18-1. Berkeley BSIM3v3 States

State	Description
<code>CAPGDO</code>	Gate-Drain overlap capacitance
<code>CAPGSO</code>	Gate-Source overlap capacitance
<code>CAPGBO</code>	Gate-Bulk overlap capacitance

Chapter 19

BSIM3SOI Equations

1.0 Introduction

BSIM3SOI v1.3 is an officially released SOI (Silicon On Insulator) MOSFET model from the Device Group at the University of California at Berkeley. The model can be used for both Partially Depleted (PD) and Fully Depleted (FD) devices. Many advanced concepts are introduced so as to allow transition between PD and FD operation dynamically and continuously, namely the *Dynamic Depletion Approach*. The basic I-V model is modified from the BSIM3v3.1 equation set. The major features are summarized as follows:

- Dynamic depletion approach is applied on both I-V and C-V. Charge and Drain current are scalable with T_{box} and T_{si} continuously.
- Supports external body bias and backgate bias; a total of 6 nodes.
- Real floating body simulation in both I-V and C-V. Body potential is properly bounded by diode and C-V formulation.
- Self heating.
- An improved impact ionization current model.
- Various diode leakage components and parasitic bipolar current included.
- New depletion charge model (**EBCI**) introduced for better accuracy in capacitive coupling prediction. An improved BSIM3v3 based model is added as well.
- Dynamic depletion selector (**DDMOD**) to suit different requirements for SOI technologies.

- Single I-V expression as in BSIM3v3.1 to guarantee continuities of I_{ds} , G_{ds} and G_m and their derivatives for all bias conditions.

A typical SOI MOSFET structure is shown in Figure 19-1. The device is formed on a thin SOI film of thickness T_{si} on top of a layer of buried oxide with thickness T_{box} . In the floating body configuration, there are four external biases which are gate voltage (V_g), drain voltage (V_d), source voltage (V_s) and substrate bias (V_e). The voltage of internal body node (V_b) is usually iterated in circuit simulation. If a body contact is applied, there will be one more external bias, the external body contact voltage (V_p).

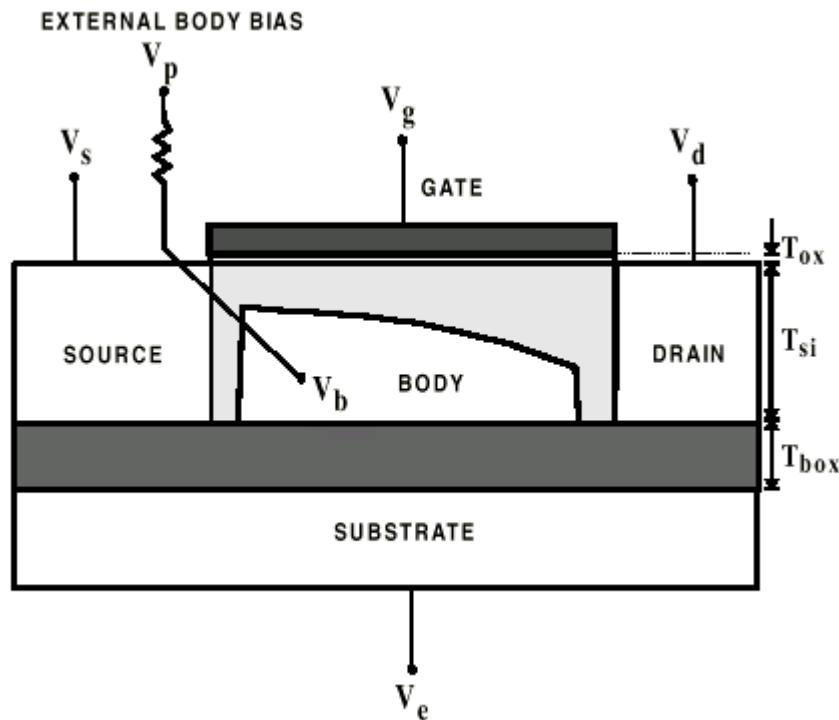


Figure 19-1. Schematic of a typical SOI MOSFET

2.0 I-V Model

For $DDMOD = 0$; V_{bs0t} , V_{bs0} , V_{thfd} , V_{bs0eff} , $V_{bs0teff}$ are not used.

2.1 V_{bs0} —Body potential at full depletion and strong inversion conditions

(assuming no substrate depletion)

$$T_{sieff} = \sqrt{TSI^2 - 2\frac{\varepsilon_{si}VBSA}{qN_a}} \quad C_{sieff} = \frac{\varepsilon_{si}}{T_{sieff}} \quad Q_{sieff} = qN_a T_{sieff}$$

$$V_{bs0t} = \phi_s - 0.5 \cdot \frac{Q_{si}}{C_{si}} + VBSA + DVBD0 \cdot \left[\exp\left(-DVBD1 \frac{L_{eff}}{2litl}\right) + 2 \exp\left(-DVBD1 \frac{L_{eff}}{litl}\right) \right] \cdot (V_{bi} - \phi_s)$$

- For $DDMOD = 1$

$$V_{bs0} = V_{bs0t}$$

- For $DDMOD = 2$

$$V_{bs0} = V_{bs0t} - KB1 \frac{V_{bs0t} - V_{es} + V_{fbb}}{1 + \frac{C_{sieff}}{C_{box}}}$$

2.2 V_{thfd} —Threshold voltage at fully depleted condition ($V_{bs} = V_{bs0}$)

$$V_{thfd} = V_{th}(V_{bs} = V_{bs0})$$

2.3 V_{bs0eff} / $V_{bs0teff}$ —Effective V_{bs0} / V_{bs0t} for all V_{gs}

$$T_0 = 0.5[(V_{thfd} - V_{gs_eff}) - \delta_1 + \sqrt{[(V_{thfd} - V_{gs_eff}) - \delta_1]^2 + \delta_1^2}]$$

$$V_{bs0teff} = V_{bs0t} - T_0$$

- For $DDMOD = 1$

$$V_{bs0eff} = V_{bs0teff}$$

- For $DDMOD = 2$

$$V_{bs0eff} = V_{bs0} - (n_{Fb} \cdot T_0)$$

$$n_{Fb} = \frac{1}{1 + K3B \frac{C_{box}}{C_{ox}} \sqrt{1 + \frac{4}{K1^2} (\phi_s + K1 \sqrt{\phi_s - V_{bs0mos}} - V_{bs0mos})}}$$

where V_{bs0mos} is the effective V_{bs} when $V_{bs} = V_{bs0}$.

It basically makes V_{bs0eff} & $V_{bs0teff}$ a function of V_{gs} as the following if $V_{gs} < V_{thfd}$.

$$\begin{aligned} V_{bs0eff} &= V_{bs0} + n_{Fb} \cdot (V_{gs} - V_{thfd}) \\ V_{bs0teff} &= V_{bs0t} + (V_{gs} - V_{thfd}) \end{aligned}$$

2.4 V_{bsdio}

- For $DDMOD = 0$

$$V_{bsdio} = V_{bs}$$

- For $DDMOD = 1$ or 2

$$T_0 = V_{bs} - V_{bs0eff} - offset - \delta$$

$$V_{bsdio} = V_{bs0eff} + offset + 0.5 \cdot [T_0 + \sqrt{T_0^2 + \delta^2}]$$

V_{bsdio} is at least higher than V_{bs0eff} by offset. By default, $offset=0.02$ and $\delta=0.02$.

2.5 V_{bseff} —Equivalent V_{bs} bias for MOS IV calculation

- For $DDMOD = 0$ or 1

$$V_{bsmos} = V_{bsdio}$$

- For $DDMOD = 2$

$$T_1 = 0.5[(V_{bs0teff} - V_{bsdio}) - \delta_2 + \sqrt{[(V_{bs0teff} - V_{bsdio}) - \delta_2]^2 + \delta_2^2}]$$

$$V_{bsmos} = V_{bsdio} - \frac{C_{sieff} T_1^2}{2 \cdot Q_{sieff}}$$

It basically makes V_{bsmos} a function of $V_{bs0teff}$ as the following if $V_{bsdio} < V_{bs0teff}$

$$V_{bsmos} = V_{bsdio} - \frac{C_{sieff} (V_{bs0teff} - V_{bsdio})^2}{2 \cdot Q_{sieff}}$$

otherwise

$$V_{bsmos} = V_{bs}$$



V_{bs} is properly bounded to V_{bs0eff} because of the diode implementation

Note

$V_{bseff} = V_{bsmos}$ is limited to $\phi_s - DELP$ by the following conversion:

$$V_{bseff} = (\phi_s - DELP) - 0.5 \left[(\phi_s - DELP - V_{bsmos}) - \delta_1 + \sqrt{[(\phi_s - DELP - V_{bsmos}) - \delta_1]^2 + 4\delta_1(\phi_s - DELP)} \right]$$

2.6 Threshold Voltage

$$\begin{aligned}
 V_{th} = & VTHO + K1(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}) - K2 V_{bseff} \\
 & + K1 \left(\sqrt{1 + \frac{NLX}{L_{eff}}} - 1 \right) \sqrt{\Phi_s} + (K3 + K3B V_{bseff}) \frac{TOX}{W_{eff} + WO} \Phi_s \\
 & - DVT0 W \left(\exp \left(-DVT1 W \frac{W_{eff} L_{eff}}{2l_{tw}} \right) + 2 \exp \left(-DVT1 W \frac{W_{eff} L_{eff}}{l_{tw}} \right) \right) (V_{bi} - \Phi_s) \\
 & - DVT0 \left(\left(\exp \left(-DVT1 \frac{L_{eff}}{2l_t} \right) + 2 \exp \left(-DVT1 \frac{L_{eff}}{l_t} \right) \right) (V_{bi} - \Phi_s) \right. \\
 & \left. - \left(\exp \left(-DSUB \frac{L_{eff}}{2l_{to}} \right) + 2 \exp \left(-DSUB \frac{L_{eff}}{l_{to}} \right) \right) (ETAO + ETAB \cdot V_{bseff}) V_{ds} \right. \\
 l_t = & \sqrt{\frac{\epsilon_{si} X_{dep}}{C_{ox}}} (1 + DVT2 \cdot V_{bseff}) \\
 l_{tw} = & \sqrt{\frac{\epsilon_{si} X_{dep}}{C_{ox}}} (1 + DVT2 W \cdot V_{bseff}) \\
 l_{to} = & \sqrt{\frac{\epsilon_{si} X_{dep0}}{C_{ox}}} \\
 X_{dep} = & \sqrt{\frac{2\epsilon_{si}(\Phi_s - V_{bseff})}{qNCH}} \\
 X_{dep0} = & \sqrt{\frac{2\epsilon_{si}\Phi_s}{qNCH}}
 \end{aligned}$$

$$V_{bi} = v_t \ln \left(\frac{NCH \cdot N_{DS}}{n_i^2} \right)$$

$$l_{itl} = \sqrt{3XJ \cdot TOX}$$

2.7 Poly depletion effect

$$V_{poly} + \frac{1}{2} X_{poly} E_{poly} = \frac{qNGATE \cdot X_{poly}^2}{2\epsilon_{si}}$$

$$\epsilon_{ox} E_{ox} = \epsilon_{si} E_{poly} = 2q\epsilon_{si} NGATE \cdot V_{poly}$$

$$V_{gs} - V_{FB} - \phi_x = V_{poly} + V_{ox}$$

$$a(V_{gs} - V_{FB} - \phi_s - V_{poly}) = 0$$

$$a = \frac{\epsilon_{ox}^2}{2q\epsilon_{si} NGATE \cdot TOX^2}$$

$$V_{gs_eff} = V_{FB} + \phi_s + \frac{q\epsilon_{si} NGATE \cdot TOX^2}{\epsilon_{ox}^2} \left(\sqrt{1 + \frac{2\epsilon_{ox}^2 (V_{gs} - V_{FB} - \phi_s)}{q\epsilon_{si} NGATE \cdot TOX^2}} - 1 \right)$$

2.8 Effective V_{gst} for all region (with Polysilicon Depletion Effect)

$$V_{gsteff} = \frac{2nv_t \ln \left[1 + \exp \left(\frac{V_{gs_eff} - V_{th}}{2nv_t} \right) \right]}{1 + 2NC_{ox} \sqrt{\frac{2\phi_s}{q\epsilon_{si} NCH}} \cdot \exp \left(-\frac{V_{gs_eff} - V_{th} - 2VOFF}{2nv_t} \right)}$$

$$\begin{aligned}
 n = & 1 + NFACTOR \cdot \frac{\varepsilon_{si}/X_{dep}}{C_{ox}} \\
 & + \frac{(CDSC + CDSCDV_{ds} + CDSCBV_{bseff}) \left(\exp\left(-DVT1 \frac{L_{eff}}{2l_t}\right) + 2 \exp\left(-DVT1 \frac{L_{eff}}{l_t}\right) \right)}{C_{ox}} \\
 & + \frac{CIT}{C_{ox}}
 \end{aligned}$$

2.9 Effective Bulk Charge Factor

- If $DDMOD = 0$

$$A_{beff} = A_{bulk}$$

- If $DDMOD = 1$ or 2

$$V_{cs} = V_{bs} - V_{bs0eff}$$

$$T_1 = 1 - 0.5 \left[\left(1 - \frac{V_{cs}}{ABPV_{gsteff}} \right) - \delta_1 + \sqrt{\left[\left(1 - \frac{V_{cs}}{ABPV_{gsteff}} \right) - \delta_1 \right]^2 + \delta_1^2} \right]$$

$$X_{csat} = MXC \cdot T_1^2 + (1 - MXC)T_1$$

X_{csat} is a parameter describing the dynamic depletion effect for a given V_{gs} . It varies within $(0, 1)$. The parameter MXC is used to adjust the slope of transition.

$$\begin{aligned}
 A_{bulk} = & 1 + \left(\frac{K_1}{2\sqrt{\phi_s}} \left(\frac{A0L_{eff}}{L_{eff} + 2\sqrt{TSI \cdot X_{dep}}} \left(1 - AGS \cdot V_{gsteff} \left(\frac{L_{eff}}{L_{eff} + 2\sqrt{TSI \cdot X_{dep}}} \right)^2 \right) \right. \right. \\
 & \left. \left. + \frac{B0}{W_{eff} + B1} \right) \right) \frac{1}{1 + KETA \cdot V_{bseff}}
 \end{aligned}$$

$$A_{beff} = X_{csat} A_{bulk} + (1 - X_{csat}) A_{dice}$$

$$A_{dice} = \frac{ADICE0}{1 + C_{boxt}/C_{ox}}$$

$$C_{boxt} = \frac{C_{si}C_{box}}{C_{si} + C_{box}}$$

2.10 Mobility and Saturation Velocity

- For **MOBMOD=1**

$$\mu_{eff} = \frac{\mu_0}{1 + (UA + UC \cdot V_{bseff})\left(\frac{V_{gsteff} + 2V_{th}}{TOX}\right) + UB\left(\frac{V_{gsteff} + 2V_{th}}{TOX}\right)^2}$$

- For **MOBMOD=2**

$$\mu_{eff} = \frac{\mu_0}{1 + (UA + UC \cdot V_{bseff})\left(\frac{V_{gsteff}}{TOX}\right) + UB\left(\frac{V_{gsteff}}{TOX}\right)^2}$$

- For **MOBMOD=3**

$$\mu_{eff} = \frac{\mu_0}{1 + \left[UA\left(\frac{V_{gsteff} + 2V_{th}}{TOX}\right) + UB\left(\frac{V_{gsteff} + 2V_{th}}{TOX}\right)^2\right](1 + UC \cdot V_{bseff})}$$

2.11 Drain Saturation Voltage

- For $R_{ds}>0$ or $\lambda \neq 1$

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

$$a = A_{beff}^2 W_{eff} VSAT C_{ox} R_{DS} + \left(\frac{1}{\lambda} - 1\right) A_{beff}$$

$$\begin{aligned}
 b &= -\left((V_{gsteff} + 2v_t) \left(\frac{2}{\lambda} - 1 \right) + A_{beff} E_{sat} L_{eff} \right. \\
 &\quad \left. + 3A_{beff} (V_{gsteff} + 2v_t) W_{eff} VSAT C_{ox} R_{DS} \right) \\
 c &= (V_{gsteff} + 2v_t) E_{sat} L_{eff} + 2(V_{gsteff} + 2v_t)^2 W_{eff} VSAT C_{ox} R_{DS} \\
 \lambda &= A1 V_{gsteff} + A2
 \end{aligned}$$

- For $R_{ds}=0$, $\lambda=1$

$$\begin{aligned}
 V_{dsat} &= \frac{E_{sat} L_{eff} (V_{gsteff} + 2v_t)}{A_{beff} E_{sat} L_{eff} + (V_{gsteff} + 2v_t)} \\
 E_{sat} &= \frac{2VSAT}{\mu_{eff}}
 \end{aligned}$$

2.12 V_{dseff}

$$V_{dseff} = V_{dsat} - \frac{1}{2} (V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}})$$

δ is parameter Delta.

2.13 Drain current expression

$$I_{ds, MOSFET} = \frac{I_{ds0}(V_{dseff})}{1 + \frac{R_{ds} I_{ds0}(V_{dseff})}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A} \right)$$

$$\beta = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}}$$

$$I_{ds0} = \frac{\beta V_{gsteff} \left(1 - A_{beff} \frac{V_{dseff}}{2[V_{gsteff} + 2v_t]} \right) V_{dseff}}{1 + \frac{V_{dseff}}{E_{sat} L_{eff}}}$$

$$V_A = V_{Asat} + \left(1 + \frac{PVAG \cdot V_{gsteff}}{E_{sat} L_{eff}} \right) \left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}} \right)^{-1}$$

$$V_{ACLM} = \frac{A_{beff} E_{sat} L_{eff} + V_{gsteff}}{PCLM \cdot A_{beff} E_{sat} litl} (V_{ds} - V_{dseff})$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{\theta_{rout}(1 + PDIBLCB \cdot V_{bseff})} \left(1 - \frac{A_{beff} V_{dsat}}{A_{beff} V_{dsat} + 2v_t} \right)$$

$$\theta_{rout} = PDIBLC1 \left[\exp \left(-DROUT \frac{L_{eff}}{2l_{t0}} \right) + 2 \exp \left(-DROUT \frac{L_{eff}}{l_{t0}} \right) \right]$$

+ PDIBLC2

$$V_{Asat} = \frac{E_{sat} L_{eff} + V_{dsat} + 2R_{DS} VSAT C_{ox} W_{eff} V_{gsteff} \left[1 - \frac{A_{beff} V_{dsat}}{2(V_{gsteff} + 2v_t)} \right]}{\frac{2}{\lambda} - 1 + R_{ds} \cdot VSAT \cdot C_{ox} W_{eff} A_{beff}}$$

$$litl = \sqrt{\frac{\epsilon_{si} TOX \cdot TSI}{\epsilon_{ox}}}$$

2.14 Drain/Source Resistance

$$R_{ds} = RDSW \cdot \frac{1 + PRWG \cdot V_{gsteff} + PRWB(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})}{(10^6 W_{eff})^{WR}}$$

2.15 Impact Ionization Current

$$I_{ii} = \frac{\text{ALPHA0} + \text{ALPHA1}L_{eff}}{L_{eff}} \cdot I_d \cdot V_{ds eff ii} \cdot \exp\left(-\frac{\text{BETA0}}{V_{ds eff ii}}\right)$$

$$V_{dsat ii} = \frac{E_{sat} L_{eff} V_{gst}}{M_1 E_{sat} L_{eff} + M_2 V_{gst}}$$

$$M_1 = AII + \frac{BII}{L_{eff}} \quad M_2 = 1 + \left(\frac{CII}{V_{ds} - DII}\right)^2$$

$V_{ds eff ii}$ is calculated the same way as $V_{ds eff}$ with V_{dsat} replaced by $V_{dsat ii}$.

M_2 is bounded to 3.0 to avoid problems at low V_{ds} .

If $A_{ii}=0$, the $V_{dsat ii}$ and $V_{ds eff ii}$ calculations are skipped, and $V_{dsat ii} = V_{dsat}$, $V_{ds eff ii} = V_{ds eff}$.

2.16 Gate-Induced-Drain-Leakage (GIDL)

- At drain

$$I_{dgidl} = W_{eff} \cdot AGIDL \cdot E_s \cdot \exp\left(-\frac{BGIDL}{E_s}\right)$$

$$E_s = \frac{V_{ds} - V_{gs} - \chi}{3 \cdot TOX}$$

- At source

$$I_{sgidl} = W_{eff} \cdot AGIDL \cdot E_s \cdot \exp\left(-\frac{BGIDL}{E_s}\right)$$

$$E_s = \frac{-V_{gs} - \chi}{3 \cdot TOX}$$

Default of χ is 1.2V. If E_s is negative, I_{dgidl} and I_{sgidl} are set to zero.

2.17 Body contact current

$$R_{bp} = RBODY \frac{W_{eff}}{L_{eff}} \quad R_{bodyext} = RBSH \cdot N_{rb}$$

- For 4-T device

$$I_{bp} = 0$$

- For 5-T device

- if **DDMOD** = 0

$$I_{bp} = \frac{V_{bp}}{R_{bp} + R_{bodyext}}$$

- if **DDMOD** = 1 or 2

$$I_{bp} = \frac{V_{bp}}{\frac{R_{bp}}{\sqrt{V_{bs} - V_{bs0eff}}} + R_{bodyext}}$$

2.18 Diode and BJT currents

For source side:

- Body-to-Source/Drain diffusion

$$I_{bs1} = W_{eff} \cdot TSI \cdot j_{sdif} \left(e^{\frac{V_{bs}}{NDIODE \cdot V_t}} - 1 \right)$$

$$I_{bd1} = W_{eff} \cdot TSI \cdot j_{sdif} \left(e^{\frac{V_{bd}}{NDIODE \cdot V_t}} - 1 \right)$$

- Recombination in depletion region

$$I_{bs2} = W_{eff} \cdot TSI \cdot j_{srec} \left(e^{\frac{V_{bs}}{2NDIODE \cdot V_t}} - 1 \right)$$

$$I_{bd2} = W_{eff} \cdot TSI \cdot j_{srec} \left(e^{\frac{V_{bd}}{2NDIODE \cdot V_t}} - 1 \right)$$

- Recombination in neutral body

$$I_{bs3} = (1 - \alpha_{bjt}) \cdot W_{eff} \cdot TSI \cdot j_{sbjt} \left(e^{\frac{V_{bs}}{NDIODE \cdot V_t}} - 1 \right)$$

$$I_{bd3} = (1 - \alpha_{bjt}) \cdot W_{eff} \cdot TSI \cdot j_{sbjt} \left(e^{\frac{V_{bd}}{NDIODE \cdot V_t}} - 1 \right)$$

- Reversed bias tunneling leakage

$$I_{bs4} = W_{eff} \cdot TSI \cdot j_{stun} \left(1 - e^{-\frac{V_{bs}}{NTUN \cdot V_t}} \right)$$

$$I_{bd4} = W_{eff} \cdot TSI \cdot j_{stun} \left(1 - e^{-\frac{V_{bd}}{NTUN \cdot V_t}} \right)$$

- Bipolar Transport Factor

$$W_b = L_{eff} - KBJT1 \cdot V_{ds}$$

$$\alpha_{bjt} = 1 - 0.5 \left(\frac{W_b}{EDL} \right)^2$$

- BJT currents

$$I_{bjt} = W_{eff} \cdot TSI \cdot j_{sbjt} \left(e^{\frac{V_{bs}}{NDIODE \cdot V_t}} - e^{\frac{V_{bd}}{NDIODE \cdot V_t}} \right)$$

$$I_c = I_{bjt} - I_{bs3} + I_{bd3}$$

- Total body-source current

$$I_{bs} = I_{bs1} + I_{bs2} + I_{bs3} + I_{bs4}$$

$$I_{bd} = I_{bd1} + I_{bd2} + I_{bd3} + I_{bd4}$$

2.19 Total body current

$$I_{ii} + I_{dgidl} + I_{sgidl} - I_{bs} - I_{bd} - I_{bp} = 0$$

2.20 Temperature effects

$$V_{th(T)} = V_{th(Tnom)} + \left(KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{bseff} \right) \left(\frac{T}{T_{nom}} - 1 \right)$$

$$UO_{(T)} = UO_{(Tnom)} \left(\frac{T}{T_{nom}} \right)^{UTE}$$

$$VSAT_{(T)} = VSAT_{(Tnom)} - AT \left(\frac{T}{T_{nom}} - 1 \right)$$

$$RDSW_{(T)} = RDSW_{(Tnom)} + PRT \left(\frac{T}{T_{nom}} - 1 \right)$$

$$UA_{(T)} = UA_{(Tnom)} + UA1 \left(\frac{T}{T_{nom}} - 1 \right)$$

$$UB_{(T)} = UB_{(Tnom)} + UB1 \left(\frac{T}{T_{nom}} - 1 \right)$$

$$UC_{(T)} = UC_{(T_{nom})} + UC1 \left(\frac{T}{T_{nom}} - 1 \right)$$

$$R_{th} = RTH0 \cdot \sqrt{\frac{TBOX}{TSI}} / W_{eff}$$

$$C_{th} = CTH0 \cdot TSI$$

$$R_{th} = RTH0 \cdot \sqrt{\frac{TBOX}{TSI}} / W_{eff}$$

$$C_{th} = CTH0 \cdot TSI$$

$$j_{sbjt} = ISBJT \left(\frac{T}{T_{nom}} \right)^{\frac{XBJT}{NDIODE}} \cdot \exp \left[-\frac{qE_g(300)}{NDIODEkT} \left(1 - \frac{T}{T_{nom}} \right) \right]$$

$$j_{sdif} = ISDIF \left(\frac{T}{T_{nom}} \right)^{\frac{XSDIF}{NDIODE}} \cdot \exp \left[-\frac{qE_g(300)}{NDIODEkT} \left(1 - \frac{T}{T_{nom}} \right) \right]$$

$$j_{srec} = ISREC \left(\frac{T}{T_{nom}} \right)^{\frac{XSREC}{2NDIODE}} \cdot \exp \left[-\frac{qE_g(300)}{2NDIODEkT} \left(1 - \frac{T}{T_{nom}} \right) \right]$$

$$j_{stun} = ISTUN \left(\frac{T}{T_{nom}} \right)^{\frac{XSTUN}{NTUN}}$$

$E_g(300)$ is the energy gap energy at 300K.

3.0 C-V Model

3.1 Dimension Dependence

$$\delta W_{eff} = DWC + \frac{WL}{L^{WLN}} + \frac{WW}{W^{WWN}} + \frac{WWL}{L^{WLN}W^{WWN}}$$

$$\delta L_{eff} = DLC + \frac{LL}{L^{LLN}} + \frac{LW}{W^{LWN}} + \frac{LWL}{L^{LLN}W^{LWN}}$$

$$L_{active} = L_{drawn} - 2\delta L_{eff}$$

$$W_{active} = W_{drawn} - 2\delta W_{eff}$$

3.2 Charge Conservation

$$Q_{Bf} = Q_{ac0} + Q_{sub0} + Q_{subs}$$

$$Q_{inv} = Q_{inv,s} + Q_{inv,d}$$

$$Q_g = -(Q_{inv} + Q_{Bf} + Q_{e2})$$

$$Q_e = Q_{e1} + Q_{e2}$$

$$Q_b = Q_{Bf} - Q_{e1} + Q_{js} + Q_{jd}$$

$$Q_s = Q_{inv,s} - Q_{js}$$

$$Q_d = Q_{inv,d} - Q_{jd}$$

$$Q_g + Q_e + Q_b + Q_s + Q_d = 0$$

3.3 Front Gate Body Charge

Accumulation Charge

$$V_{FBeff} = V_{fb} - 0.5((V_{fb} - V_{gb} - \delta) + \sqrt{(V_{fb} - V_{gb} - \delta)^2 + \delta^2})$$

$$\text{where } V_{gb} = V_{gs} - V_{bseff}$$

$$V_{fb} = V_{th} - \phi_s - K1 \sqrt{\phi_s - V_{bseff}}$$

$$V_{gsteff, cv} = nv_t \ln \left(1 + \exp \left[\frac{V_{gs} - V_{th}}{nv_t} \right] \right)$$

$$Q_{acc} = -W_{active}L_{active}C_{ox}(V_{FBeff} - V_{fb})$$

Gate Induced Depletion Charge

$$Q_{sub0} = -W_{active}L_{active}C_{ox} \frac{K1^2}{2} \left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{FBeff} - V_{gsteffcv} - V_{bseff})}{K1^2}} \right)$$

Drain Induced Depletion Charge

- For **CAPMOD = 2**

$$V_{dsatCV} = \frac{V_{gsteffCV}}{A_{bulkCV}}$$

$$V_{dsCV} = V_{dsatCV} - \frac{1}{2}(V_{dsatCV} - V_{ds} - \delta + \sqrt{(V_{dsatCV} - V_{ds} - \delta)^2 + 4\delta V_{dsatCV}})$$

- For **DDMOD=0**

$$Q_{subs1} = WL_{eff}K1C_{ox}(A_{bulkCV} - 1) \cdot \left[0.5 \cdot V_{dsCV} - \frac{A_{bulkCV}V_{dsCV}^2}{12(V_{gsteffCV} - 0.5A_{bulkCV}V_{dsCV})} \right]$$

$$Q_{subs2} = 0$$

- For **DDMOD=1/2**

$$V_{csCV} = V_{cs} + 0.5(V_{dsCV} - V_{cs} + \delta - \sqrt{(V_{dsCV} - V_{cs} + \delta)^2 + 4\delta V_{dsCV}})$$

V_{dsCV} is equal to V_{dsatCV} when V_{dseff} is equal to V_{dsatCV} .

$$X_c = \frac{[2V_{dsatCV} - V_{csCV}]V_{csCV}}{[2V_{dsatCV} - V_{dsCV}]V_{dsCV}}$$

$$Q_{subs1} = WL_{eff}K1C_{ox}X_c(A_{bulkCV} - 1)$$

$$\cdot \left[0.5 \cdot V_{csCV} - \frac{A_{bulkCV}V_{csCV}^2}{12(V_{gsteffCV} - 0.5(A_{bulkCV}V_{csCV}))} \right]$$

$$Q_{subs2} = WL_{eff}K1C_{ox}(A_{bulkCV} - 1)V_{cs}(1 - X_c)$$

- For **CAPMOD = 3**

$$V_{dsatCV} = V_{gsteff} + K1\sqrt{\phi_s} + \frac{K1^2}{2} - K1\sqrt{V_{gsteff} + K1\sqrt{\phi_s} + \phi_s + \frac{K1^2}{4}}$$

$$V_{dsCV} = V_{dseff} + (V_{dsatCV} - V_{dsat})\left(\frac{V_{dseff}}{V_{dsat}}\right)^2$$

- For **DDMOD=0**

$$Q_{subs1} = W_{eff}L_{eff}C_{ox}K1 \cdot \\ K1 \left[\frac{2}{3}(V_{gsteff} + K1\sqrt{\phi_s - V_{bs}} + (\phi_s - V_{bs})) \left((\phi_s + V_{dsCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right) \right. \\ \left. - 0.4 \left((\phi_s + V_{dsCV} - V_{bs})^{\frac{5}{2}} - (\phi_s - V_{bs})^{\frac{5}{2}} \right) - K1V_{dsCV}((\phi_s - V_{bs}) + 0.5V_{dsCV}) \right] \\ / \left(V_{dsCV}(V_{gsteff} + K1\sqrt{\phi_s - V_{bs}} - 0.5V_{dsCV}) - \frac{2}{3}K1 \left[(\phi_s + V_{dsCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right] \right)$$

$$Q_{subs2} = 0$$

- For **DDMOD=1 or 2**

$$V_{csCV} = V_{cs} + 0.5(V_{dsCV} - V_{cs} + \delta - \sqrt{(V_{dsCV} - V_{cs} + \delta)^2 + 4\delta V_{dsCV}})$$

$$X_c = \frac{V_{csCV}(V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} - 0.5 V_{csCV}) - \frac{2}{3}K1 \left[(\phi_s + V_{csCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right]}{V_{dsCV}(V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} - 0.5 V_{dsCV}) - \frac{2}{3}K1 \left[(\phi_s + V_{dsCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right]}$$

$$Q_{subs1} = W_{eff}L_{eff}C_{ox}K1 \cdot$$

$$K1 \left[\frac{2}{3}(V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} + (\phi_s - V_{bs})) \left((\phi_s + V_{csCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right) \right.$$

$$\left. - 0.4 \left((\phi_s + V_{csCV} - V_{bs})^{\frac{5}{2}} - (\phi_s - V_{bs})^{\frac{5}{2}} \right) - K1 V_{csCV} ((\phi_s - V_{bs}) + 0.5 V_{dsCV}) \right]$$

$$\left/ \left(V_{dsCV}(V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} - 0.5 V_{dsCV}) - \frac{2}{3}K1 \left[(\phi_s + V_{dsCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right] \right) \right.$$

$$Q_{subs2} = W_{effCV}L_{effCV}C_{ox}K1 \sqrt{\phi_s - V_{bs0eff}} \cdot (1 - X_c)$$

Back Gate Body Charge

- For **DDMOD=0**

$$Q_{e1} = WL C_{box} (V_{es} - V_{fbb} - V_{bs})$$

$$Q_{e2} = 0$$

- For **DDMOD=1 or 2**

$$Q_{sicv} = C_{ox}WL \frac{K1^2}{2} \left[1 - \sqrt{1 + \frac{4(\phi_s + K1 \sqrt{\phi_s - V_{bs0t}} - V_{bs0t})}{K1^2}} \right]$$

$$Q_{bf0} = C_{ox} \frac{K1^2}{2} \left[1 - \sqrt{1 + \frac{4(\phi_s + K1 \sqrt{\phi_s - V_{bs0mos}} - V_{bs0mos})}{K1^2}} \right]$$

$$Q_{e1} = -Q_{sicv} + Q_{bf0} - WX_c L C_{box} (V_{bs} - V_{bs0})$$

$$Q_{e2} = -WLC_{boxt} \frac{1-X_c}{2} (V_{dsCV} - V_{csCV})$$

3.4 Inversion Charge

$$Q_{inv} = -W_{active} L_{active} C_{ox} \cdot$$

$$\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right) + \frac{A_{bulkCV}^2 V_{cveff}^2}{12 \left(V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right)}$$

50/50 Charge Partition

$$Q_{inv,s} = Q_{inv,d} = 0.5 \cdot Q_{inv}$$

40/60 Charge Partition

$$Q_{inv,s} = -\frac{W_{active}L_{active}C_{ox}}{2\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff}\right)^2} \cdot \\ \left(V_{gsteffCV}^3 - \frac{4}{3}V_{gsteffCV}^2(A_{bulkCV}V_{cveff}) \right. \\ \left. + \frac{2}{3}V_{gsteff}(A_{bulkCV}V_{cveff})^2 - \frac{2}{15}(A_{bulkCV}V_{cveff})^3 \right)$$

$$Q_{inv,d} = -\frac{W_{active}L_{active}C_{ox}}{2\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff}\right)^2} \cdot \\ \left(V_{gsteffCV}^3 - \frac{5}{3}V_{gsteffCV}^2(A_{bulkCV}V_{cveff}) \right. \\ \left. + V_{gsteff}(A_{bulkCV}V_{cveff})^2 - \frac{1}{5}(A_{bulkCV}V_{cveff})^3 \right)$$

0/100 Charge Partition

$$Q_{inv,s} = -W_{active}L_{active}C_{ox} \cdot \\ \left(\frac{V_{gsteffCV}}{2} + \frac{A_{bulkCV}V_{cveff}}{4} - \frac{(A_{bulkCV}V_{cveff})^2}{24\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff}\right)} \right)$$

$$Q_{inv, d} = -W_{active} L_{active} C_{ox}.$$

$$\left(\frac{V_{gsteffCV}}{2} - \frac{3A_{bulkCV}V_{cveff}}{4} - \frac{(A_{bulkCV}V_{cveff})^2}{8\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff}\right)} \right)$$

3.5 Overlap Capacitance

Source Overlap Capacitance

$$V_{gs_overlap} = \frac{1}{2} \left\{ (V_{gs} + \delta) + \sqrt{(V_{gs} + \delta)^2 + 4\delta} \right\}$$

$$\begin{aligned} \frac{Q_{overlap, s}}{W_{active}} &= CGS0 \cdot V_{gs} \\ &+ CGS1 \left\{ V_{gs} - V_{gs_overlap} + \frac{CKAPPA}{2} \left(-1 + \sqrt{1 + \frac{4V_{gs_overlap}}{CKAPPA}} \right) \right\} \end{aligned}$$

Drain Overlap Capacitance

$$V_{gd_overlap} = \frac{1}{2} \left\{ (V_{gd} + \delta) + \sqrt{(V_{gd} + \delta)^2 + 4\delta} \right\}$$

$$\begin{aligned} \frac{Q_{overlap, d}}{W_{active}} &= CGD0 \cdot V_{gd} \\ &+ CGD1 \left\{ V_{gd} - V_{gd_overlap} + \frac{CKAPPA}{2} \left(-1 + \sqrt{1 + \frac{4V_{gd_overlap}}{CKAPPA}} \right) \right\} \end{aligned}$$

Gate Overlap Capacitance

$$Q_{overlap,g} = -(Q_{overlap,s} + Q_{overlap,d})$$

Source/Drain Junction Charge

- For $V_{bs} < 0$

$$Q_{jswg} = CJSWG \frac{TSI}{10^{-7}} \frac{PBSWG}{1 - MJSWG} \left[1 - \left(1 - \frac{V_{bs}}{PBSWG} \right)^{1 - MJSWG} \right] + TT \cdot I_{bs1}$$

else

$$Q_{jswg} = CJSWG \frac{TSI}{10^{-7}} V_{bs} \left[1 + \frac{0.5MJSWG \cdot V_{bs}}{PBSWG} \right] + TT \cdot I_{bs1}$$

- For $V_{bd} < 0$

$$Q_{jdwg} = CJSWG \frac{TSI}{10^{-7}} \frac{PBSWG}{1 - MJSWG} \left[1 - \left(1 - \frac{V_{bd}}{PBSWG} \right)^{1 - MJSWG} \right] + TT \cdot I_{bd1}$$

else

$$Q_{jdwg} = CJSWG \frac{TSI}{10^{-7}} V_{bs} \left[1 + \frac{0.5MJSWG \cdot V_{bd}}{PBSWG} \right] + TT \cdot I_{bd1}$$

3.6 Extrinsic Charges

Bottom S/D to Substrate Charge

$$C_{sid,e} = \begin{cases} C_{box} & \text{if } V_{s/d,e} < V_{sdfb} \\ C_{box} - \frac{1}{ASD}(C_{box} - C_{min})\left(\frac{V_{s/d,e} - V_{sdfb}}{V_{sdth} - V_{sdfb}}\right)^2 & \text{elseif } V_{s/d,e} < V_{sdfb} + ASD(V_{sdth} - V_{sdfb}) \\ C_{min} + \frac{1}{1-ASD}(C_{box} - C_{min})\left(\frac{V_{s/d,e} - V_{sdth}}{V_{sdth} - V_{sdfb}}\right)^2 & \text{elseif } V_{s/d,e} < V_{sdth} \\ C_{min} & \text{else} \end{cases}$$

Sidewall S/D to Substrate Charge

$$C_{sdesw} = CSDESW \log\left(1 + \frac{TSI}{TBOX}\right)$$

Gate to substrate overlap charge

$$C_{egov} = CEG0(V_{gs} - V_{es})$$

3.7 Helper Charge

Only used for **DDMOD**=1 and 2.

$$\begin{aligned} Q_{ex} &= F_{ex} \cdot K1 \cdot C_{ox} \cdot (V_{bs} - V_{bsdio}) \\ Q_b^+ &= Q_{ex} \quad Q_e^- = Q_{ex} \end{aligned}$$

4.0 Printing/Plotting States

The instance parameter **DEBUG** allows users to turn on debugging information selectively. Internal parameters (e.g. **par**) for an instance (e.g. **m1**) can be plotted using this command.

```
.plot <Analysis_Type> S(m1 -> par)
```

Example

```
.plot DC S(m1 -> body)
```

By default, **DEBUG** is set to zero and two internal parameters will be available for plotting.

Quantity	Description
<i>body</i>	V_b value iterated by SPICE
<i>temp</i>	Device temperature with self-heating mode turned on.

If **DEBUG** is set to one, more internal parameters are available for plotting. This serves debugging purposes when there is a convergence problem. This can also help the user to understand the model more. Here is the list of internal parameters:

Quantity	Description
<i>Vbs</i>	V_{bsdio} used by the MOS I-V/C-V calculation
<i>Vt</i>	Threshold voltage
<i>Ids</i>	MOS current
<i>Ic</i>	BJT current
<i>Ibs</i>	Body to source diode current
<i>Ibd</i>	Body to drain diode current
<i>Iii</i>	Impact ionization current
<i>Igidl</i>	GIDL current at drain side
<i>Itun</i>	Tunneling current at drain side
<i>Ibp</i>	External body contact to internal body current
<i>Abeff</i>	Effective bulk charge factor
<i>Vbs0eff</i>	Minimum body potential for given external bias
<i>Vbseff</i>	Effective body voltage
<i>Gds</i>	Derivative of Ids with respect to Vds
<i>Gm</i>	Derivative of Ids with respect to Vgs
<i>Gmb</i>	Derivative of Ids with respect to Vbs
<i>Gme</i>	Derivative of Ids with respect to Ves
<i>Gmibs</i>	Derivative of Ibs with respect to Vbs
<i>Gmibd</i>	Derivative of Ibd with respect to Vbd
<i>Rbp</i>	B/P resistance

The following parameters are only valid if charge computation is required:

Quantity	Description
X_c	Partial depletion factor
Q_{bf}	Channel depletion charge
Q_{jd}	Parasitic drain junction charge
Q_{js}	Parasitic source junction charge
Q_x	where x could be any of: d, g, s, e, or b: charge inside drain, gate, source, substrate, or body respectively
C_{xy}	where x and y could be any of: d, g, s, e, or b: transcapacitance between nodes x and y
C_{bsj}	B/S junction capacitance
C_{bdj}	B/D junction capacitance

In the case of self-heating:

Quantity	Description
I_{th}	Thermal power dissipated inside the device

5.0 .OP Printout

The following parameters are printed in the **.OP** analysis:

$V_{gs}, V_{ds}, V_{bs}, I_{ds}, I_{bs}, I_{bd}, V_{th}, V_{dsat}, G_m, G_{ds}, G_{mb}, G_{me}, C_{gg}, C_{gd}, C_{gs}, C_{ge}, C_{gb}, C_{dg}, C_{dd}, C_{ds}, C_{de}, C_{db}, C_{sg}, C_{sd}, C_{ss}, C_{se}, C_{sb}, C_{eg}, C_{ed}, C_{es}, C_{ee}, C_{eb}.$

6.0 Parameter List

Nr.	Name	Description	Default	Units
1	LEVEL	Level 55 for BSIM3SOI	55	
Model Control Parameters				
2	DDMOD	Flag for Dynamic Depletion (DD) Mode 0 - no DD calculation 1 - DD without backgate effect 2 - DD with backgate effect 3 - Ideal FD mode, no floating body	2	
3	SHMOD	Flag for self-heating 0 - no self-heating, 1 - self-heating	0	
4	MOBMOD	Mobility model selector	1	
5	CAPMOD ^a	Flag for the short channel capacitance model	2	
6	NOIMOD	Flag for Noise model	1	
Process Parameters				
7	TSI	Silicon film thickness	10^{-7}	m
8	TBOX	Buried oxide thickness	3×10^{-7}	m
9	TOX	Gate oxide thickness	1×10^{-8}	m
10	XJ	S/D junction depth	b	m
11	NCH	Channel doping concentration	1.7×10^{17}	cm^{-3}
12	NSUB ^c	Substrate doping concentration	6×10^{16}	cm^{-3}
13	NGATE	Poly gate doping concentration	0	cm^{-3}
DC Parameters				
14	VTH0 ^d	Threshold voltage at Vbs=0 for long and wide device	0.7	
15	K1	First order body effect coefficient	0.53	$\text{V}^{1/2}$
16	K2	Second order body effect coefficient	-0.0186	
17	K3	Narrow width coefficient	0	
18	K3B	Body effect coefficient of K3	0	V^{-1}
19	VBSA	Transition body voltage offset	0	V
20	DELP	Constant for limiting Vbseff to ϕ_s	0.02	V
21	KB1	Coefficient of Vbs0 dependency on Ves	1	
22	KB3	Coefficient of Vbs0 dependency on Vgs at subthreshold region	1	
23	DVBDO	First coefficient of Vbs0 dependency on Leff	0	V
24	DVBD1	Second coefficient of Vbs0 dependency on Leff	0	V

Nr.	Name	Description	Default	Units
25	W0	Narrow width parameter	2.5×10^{-6}	m
26	NLX	Lateral non-uniform doping parameter	1.74×10^{-7}	m
27	DVT0	first coefficient of short-channel effect on Vth	2.2	
28	DVT1	Second coefficient of short-channel effect on Vth	0.53	
29	DVT2	Body-bias coefficient of short-channel effect on Vth	-0.032	V ⁻¹
30	DVT0W	first coefficient of narrow width effect on Vth for small channel length	0	
31	DVT1W	Second coefficient of narrow width effect on Vth for small channel length	5.3×10^6	
32	DVT2W	Body-bias coefficient of narrow width effect on Vth for small channel length	-0.032	V ⁻¹
33	U0	Mobility at Temp = Tnom NMOSFET PMOSFET	670 250	cm ² (Vs) ⁻¹
34	UA	First-order mobility degradation coefficient	2.25×10^{-9}	mV ⁻¹
35	UB	Second-order mobility degradation coefficient	5.9×10^{-19}	(mV ⁻¹) ²
36	UC	Body-effect of mobility degradation coefficient	-0.0465	V ⁻¹
37	VSAT	Saturation velocity at Temp=Tnom	8×10^4	ms ⁻¹
38	A0	Bulk charge effect coefficient for channel length	1.0	
39	AGS	Gate bias coefficient of Abulk	0.0	V ⁻¹
40	B0	Bulk charge effect coefficient for channel width	0.0	m
41	B1	Bulk charge effect width offset	0.0	m
42	KETA	Body-bias coefficient of bulk charge effect	-0.6	m
43	ABP	Coefficient of Abeff dependency on Vgst	1.0	
44	MXC	Fitting parameter for Abeff calculation	-0.9	
45	ADICE0	DICE bulk charge factor	1	
46	A1	First non-saturation effect parameter	0.0	V ⁻¹
47	A2	Second non-saturation effect parameter	1.0	0
48	RDSW	Parasitic resistance with respect to unit width	100	$\Omega \mu\text{m}^{\text{WR}}$
49	PRWB	Body effect coefficient of RDSW	0	V ⁻¹
50	PRWG	Gate bias effect coefficient of RDSW	0	V ^{-1/2}
51	WR	Width offset from W_{eff} for Rds calculation	1	
52	WINT	Width offset fitting parameter from I-V without bias	0.0	m
53	LINT	Length offset fitting parameter from I-V without bias	0.0	m
54	DWG	Coefficient of W_{eff} 's gate dependence	0.0	mV ⁻¹
55	DWB	Coefficient of W_{eff} 's substrate body bias dependence	0.0	mV ^{-1/2}

Nr.	Name	Description	Default	Units
56	VOFF	Offset voltage in the subthreshold region for large W and L	-0.08	V
57	NFACTOR	Subthreshold swing factor	1	
58	ETA0	DIBL coefficient in subthreshold region	0.08	
59	ETAB	Body-bias coefficient for the subthreshold DIBL effect	-0.07	V ⁻¹
60	DSUB	DIBL coefficient exponent	0.56	
61	CIT	Interface trap capacitance	0.0	Fm ⁻²
62	CDSC	Drain/Source to channel coupling capacitance	2.4x10 ⁻⁴	Fm ⁻²
63	CDSCB	Body-bias sensitivity of CDSC	0	Fm ⁻²
64	CDSCD	Drain-bias sensitivity of CDSC	0	Fm ⁻²
65	PCLM	Channel length modulation parameter	1.3	
66	PDIBL1	First output resistance DIBL effect correction parameter	0.39	
67	PDIBL2	Second output resistance DIBL effect correction parameter	0.0086	
68	DROUT	L dependence coefficient of the DIBL correction parameter in Rout	0.56	
69	PVAG	Gate dependence of Early voltage	0.0	
70	DELTA	Effective Vds parameter	0.01	
71	AII	1st Leff dependence Vdsatii parameter	0.0	V ⁻¹
72	BII	2nd Leff dependence Vdsatii parameter	0.0	mV ⁻¹
73	CII	1st Vds dependence Vdsatii parameter	0.0	
74	DII	2nd dependence Vdsatii parameter	-1.0	V
75	ALPHA0	The first parameter of impact ionization current	0.0	mV ⁻¹
76	ALPHA1	The second parameter of impact ionization current	1.0	V ⁻¹
77	BETA0	The third parameter of impact ionization current	30	V
78	AGIDL	GIDL constant	0.0	Ω^{-1}
79	BGIDL	GIDL exponential coefficient	0.0	Vm ⁻¹
80	NGIDL	GIDL Vds enhancement coefficient	1.2	V
81	NTUN	Reverse tunneling non-ideality factor	10.0	
82	NDIODE	Diode non-ideality factor	1.0	
83	ISBJT	BJT injection saturation current	1x10 ⁻⁶	Am ⁻²
84	ISDIF	Body to source/drain injection saturation current	0.0	Am ⁻²
85	ISREC	Recombination in depletion saturation current	1x10 ⁻⁵	Am ⁻²
86	ISTUN	Reverse tunneling saturation current	0.0	Am ⁻²
87	EDL	Electron diffusion length	2x10 ⁻⁶	m

Nr.	Name	Description	Default	Units
88	KBJT1	Parasitic bipolar early effect coefficient	0	mV^{-1}
89	RBODY	Intrinsic body contact sheet resistance	0.0	$\Omega \text{ m}^{-2}$
90	RBSH	Extrinsic body contact sheet resistance	0.0	$\Omega \text{ m}^{-2}$
91	RSH	Source drain sheet resistance in ohm per square	0.0	Ω/sq
AC and Capacitance Parameters				
92	XPART	Charge partitioning rate flag	0	
93	CGSO	Non LDD region source-gate overlap capacitance per channel length	e	Fm^{-1}
94	CGDO	Non LDD region drain-gate overlap capacitance per channel length	f	Fm^{-1}
95	CGEO	Gate substrate overlap capacitance per unit channel length	0.0	Fm^{-1}
96	CJSWG	Source/Drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Tsi)	1×10^{-10}	Fm^{-1}
97	PBSWG	Source/Drain (gate side) sidewall junction capacitance built in potential	0.7	V
98	MJSWG	Source/Drain (gate side) sidewall junction capacitance grading coefficient	0.5	V
99	TT	Diffusion capacitance transit time coefficient	1ps	s
100	VSDFB	Source/drain bottom diffusion capacitance flatband voltage	g	V
101	VSDTH	Source/drain bottom diffusion capacitance threshold voltage	h	V
102	CSDMIN	Source/drain bottom diffusion minimum capacitance	i	V
103	ASD	Source/drain bottom diffusion smoothing parameter	0.3	
104	CSDESW	Source/drain sidewall fringing capacitance per unit length	0.0	Fm^{-1}
105	CGS1	Light doped source-gate region overlap capacitance	0.0	Fm^{-1}
106	CGD1	Light doped drain-gate region overlap capacitance	0.0	Fm^{-1}
107	CKAPPA	Coefficient for lightly doped region overlap capacitance fringing field capacitance	0.6	Fm^{-1}
108	CF	Gate to source/drain fringing field capacitance	j	Fm^{-1}
109	CLC	Constant term for the short channel model	0.1×10^{-7}	m
110	CLE	Exponential term for the short channel model	0.0	
111	DLC	Length offset fitting parameter from C-V	LINT	m
112	DWC	Width offset fitting parameter from C-V	WINT	m
Temperature Parameters				
113	TNOM	Temperature at which parameters are expected	27	$^{\circ}\text{C}$
114	UTE	Mobility temperature exponent	-1.5	

Nr.	Name	Description	Default	Units
115	KT1	Temperature coefficient for threshold voltage	-0.11	V
116	KT11	Channel length dependence of the temperature coefficient for threshold voltage	0.0	Vm
117	KT2	Body-bias coefficient of the Vth temperature effect	0.022	
118	UA1	Temperature coefficient for UA	4.31x10 ⁻⁹	mV ⁻¹
119	UB1	Temperature coefficient for UB	-7.61x10 ⁻¹⁸	(mV ⁻¹) ²
120	UC1	Temperature coefficient for UC	-0.056 ^k	V ⁻¹
121	AT	Temperature coefficient for saturation velocity	3.3x10 ⁴	ms ⁻¹
122	CTH0	Normalized thermal capacity	0	m°C(Ws) ⁻¹
123	PRT	Temperature coefficient for RDSW	0	Ω μm
124	RTH0	Normalized thermal resistance	0	m°CW ⁻¹
125	XBJT	Power dependence of jbjt on temperature	2	
126	XDIF	Power dependence of jdif on temperature	2	
127	XREC	Power dependence of jrec on temperature	20	
128	XTUN	Power dependence of jtun on temperature	0	

- a. **CAPMOD** 0 and 1 are no longer supported by BSIM3SOI.
- b. In modern SOI technology, source/drain extension or LDD are commonly used. As a result, the source/drain junction depth (**XJ**) can be different from the silicon film thickness (**TSI**). By default, if **XJ** is not given, it is set to **TSI**. **XJ** is not allowed to be greater than **TSI**.
- c. BSIM3SOI refers substrate to the silicon below buried oxide, not the well region in BSIM3. It is used to calculate backgate flatband voltage (**V_{fb}**) and parameters related to source/drain diffusion bottom capacitance (**VSDTH**, **VSDFB**, **CSDMIN**). Positive **NSUB** means the same type of doping as the body and negative **NSUB** means opposite type of doping.
- d. For FD device, **VTH0** is not equal to the measured long and wide device threshold voltage because **V_{bs0}** is higher than zero.

- e. If **CGSO** is not given then it is calculated using:
if (**DLC** is given and is greater 0) then,

$$\text{CGSO} = \text{p1} = (\text{DLC} * \text{cox}) - \text{cgs1}$$

if (the previously calculated **CGSO** < 0), then

$$\text{CGSO} = 0$$

else **CGSO** = 0.6 * **TSI** * **cox**

f. **CGDO** is calculated in a way similar to **CGSO**.

g. If (**NSUB** is positive)

$$V_{sdfb} = -\frac{kT}{q} \log\left(\frac{10^{20} \cdot \text{NSUB}}{n_i \cdot n_i}\right) - 0.3 \quad \text{else} \quad V_{sdfb} = -\frac{kT}{q} \log\left(\frac{10^{20}}{\text{NSUB}}\right) + 0.3$$

$$\text{h. } \phi_{sd} = 2 \frac{kT}{q} \log\left(\frac{|\text{NSUB}|}{n_i}\right) \quad \gamma_{sd} = \frac{5.753 \times 10^{-12} \sqrt{|\text{NSUB}|}}{C_{box}}$$

If (**NSUB** is positive)

$$V_{sdth} = \text{VSDFB} + \phi_{sd} + \gamma_{sd} \sqrt{\phi_{sd}} \quad \text{else} \quad V_{sdth} = \text{VSDFB} - \phi_{sd} - \gamma_{sd} \sqrt{\phi_{sd}}$$

$$\text{i. } X_{sddep} = \sqrt{\frac{2\epsilon_{si}\phi_{sd}}{q|NSUB \cdot 10^6|}} \quad C_{sddep} = \frac{\epsilon_{si}}{X_{sddep}} \quad C_{sdmin} = \frac{C_{sddep}C_{box}}{C_{sddep} + C_{box}}$$

$$\text{j. If } CF \text{ is not given then it is calculated using } CF = \frac{2\epsilon_{ox}}{\pi} \ln\left(1 + \frac{4 \times 10^{-7}}{TOX}\right)$$

k. For **MOBMOD**=1 and 2, the unit is mV⁻². Default is -5.6×10⁻¹¹.

For **MOBMOD**=3, unit is V⁻¹ and default is -0.056.

Chapter 20

BSIM3SOI v2.x and v3.x Equations

1.0 Introduction

The BSIM3SOI v2.x and v3.x models are implemented in Eldo as LEVEL=56. **BSIMSOI** is the officially released SOI (Silicon On Insulator) MOSFET model from the Device Group at the University of California at Berkeley. Both BSIMSOI v2.x and v3.x models can be used for Partially Depleted (**PD**) and Fully Depleted (**FD**) devices. For the BSIMSOIv2.x model many advanced concepts were introduced so as to allow transition between **PD** and **FD** operation dynamically and continuously, namely the *Dynamic Depletion Approach (DD)*. The user is able to select one of these three modes using a parameter selector called **SOIMOD**. For more information please refer to [SOIMOD selection](#). The basic I-V model is modified from the **BSIM3v3.1** equation set.



- Note** The different versions available are:
PD: v2.1, v2.2.1, v2.2.2, v2.2.3, v3.0, v3.1 and v3.1.1;
FD: v2.1, v3.1 and v3.1.1;
DD: v2.1.

1.1 Version Selection

The different versions are accessible through the model parameter **VERSION** as shown in the table below. By default, BSIM3SOIv3.1.1 (**VERSION**=3.11) is selected.

Parameter Value	BSIM3SOI Version
VERSION=3.11	BSIM3SOIv3.1.1 (Default)
VERSION=3.1	BSIM3SOIv3.1
VERSION=3.0	BSIM3SOIv3.0
VERSION=2.23	BSIM3SOIv2.2.3

Parameter Value	BSIM3SOI Version
VERSION=2.22	BSIM3SOIv2.2.2
VERSION=2.21	BSIM3SOIv2.2.1
VERSION=2.1	BSIM3SOIv2.1

1.2 SOIMOD selection

Parameter selector **SOIMOD** was an Eldo specific model parameter in the v2.x versions. Beginning version v3.0, it is a Berkeley standard model parameter to select between various SOI models: PD, FD and DD. For versions v3.0 and v3.1, the **SOIMOD** values have changed in Eldo to be compatible with the Berkeley standard values. Please see the following table:

Model	SOIMOD for v2.x (Eldo specific)	SOIMOD for v3.0 (Spice compatible)	SOIMOD for v3.1 (Spice compatible)
PD	1	0 (default)	0 (default)
DD	2 (default)	-	-
FD	3	-	2
FD module over PD^a	-	1	1

a. The FD module is an addition of some equations over the PD module to make the PD module also fit FD devices.

The different versions are handled separately inside this chapter. See “[BSIMPDv2.x](#)” on page 20-5, “[BSIMFDv2.x](#)” on page 20-43, “[BSIMDDv2.1](#)” on page 20-72, and “[BSIM3SOIv3.x](#)” on page 20-101.

1.3 TNODEOUT keyword

TNODEOUT is a keyword that can be specified in the instantiation statement of an SOI device as follows:

```
Mxx nd ng ns ne <np> <nb> <nT> mname <L=val> <W=val> TNODEOUT
```

- If **TNODEOUT** is not specified, the user can specify four nodes for a device with floating body. Specifying five nodes implies that the fifth node is the external body contact node, with a body resistance between the internal and external terminals. This configuration applies to a distributed body resistance simulation. Specifying six nodes implies a body contacted case with an accessible internal body node (sixth node). Specifying seven nodes

implies that the seventh node is the temperature node. This may be used to model thermal coupling.

- If **TNODEOUT** is specified, simulation interprets the last node as the temperature node. You can specify five nodes for a device with floating body. Specifying six nodes implies body contact. Seven nodes is a body contacted case with an accessible internal body node.

1.4 BSIM3SOI features

The major features are summarized as follows:

- Dynamic depletion approach is applied on both I-V and C-V. Charge and Drain current are scalable with **TBOX** and **TSI** continuously.
- Supports external body bias and backgate bias; a total of 6 nodes.
- Real floating body simulation in both I-V and C-V. Body potential is properly bounded by diode and C-V formulation.
- Self heating implementation improved over the alpha version.
- An improved impact ionization current model.
- Various diode leakage components and parasitic bipolar current included.
- New depletion charge model (**EBCI**) introduced for better accuracy in capacitive coupling prediction. An improved BSIM3v3 based model is also included.
- Dynamic depletion can suit different requirements for SOI technologies.
- Single I-V expression as in BSIM3v3.1 to guarantee the continuity of I_{ds} , G_{ds} and G_m and their derivatives for all bias conditions.

A typical SOI MOSFET structure is shown in [Figure 20-1](#). The device is formed on a thin SOI film of thickness T_{si} on top of a layer of buried oxide with thickness T_{box} . In the floating body configuration, there are four external biases which are gate voltage (V_g), drain voltage (V_d), source voltage (V_s) and substrate bias (V_e).

The voltage of internal body node (V_b) is usually iterated in circuit simulation. If a body contact is applied, there will be one more external bias, the external body contact voltage (V_p).

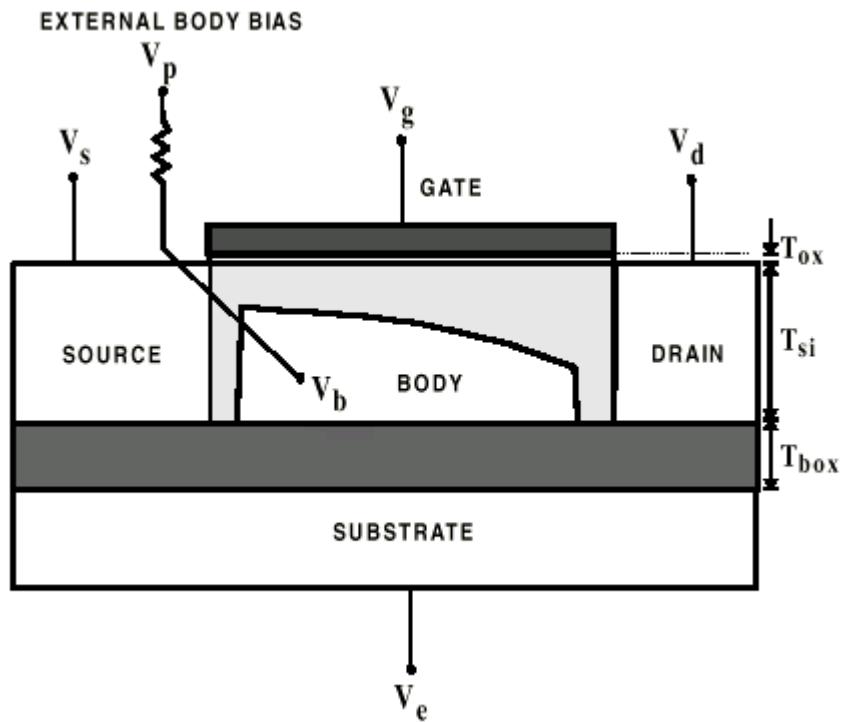


Figure 20-1. Schematic of a typical SOI MOSFET

2.0 BSIM3SOIv2.x

2.1 BSIMPDv2.x

BSIMPD is a Partially Depleted (PD) Silicon-on-Insulator (SOI) MOSFET model for SPICE simulation. This model is formulated on top of the BSIM3v3 framework [1]. It shares the same basic equations with the bulk model so that the physical nature and smoothness of BSIM3v3 are retained. Most parameters related to general MOSFET operation (non-SOI specific) are directly imported from BSIM3v3 to ensure parameter compatibility.

Many enhanced features are included in BSIMPD through the joint effort of the BSIM Team at UC Berkeley and IBM Semiconductor Research and Development Center (SRDC) at East Fishkill. In particular, the model has been tested extensively within IBM on its state-of-the-art high speed SOI technology.

The latest version, BSIMPDv3.1.1, is implemented in Eldo. A version control parameter **VERSION** allows the use of older versions if required.

BSIMPD, a derivative of BSIM3SOIv1.3 [2], has the following features and enhancements:

- Real floating body simulation in both I-V and C-V. The body potential is determined by the balance of all the body current components.
- An improved parasitic bipolar current model. This includes enhancements in the various diode leakage components, second order effects (high-level injection and Early effect), diffusion charge equation, and temperature dependence of the diode junction capacitance.
- An improved impact-ionization current model. The contribution from BJT current is also modeled by the parameter FBGJII.
- The gate-body tunneling (substrate current) is added to the BSIMPDv2.2.1 version to enhance the model accuracy. This gate current model is only available in version \geq 2.2.1.

- Enhancements in the threshold voltage and bulk charge formulation of the high positive body bias regime.
- Instance parameters ($Pdbcp$, $Psbcn$, $Agbcn$, $Aebcn$, Nbc) are provided to model the parasitics of devices with various body-contact and isolation structures.
- An external body node (the 6th node) and other improvements are introduced to facilitate the modeling of distributed body-resistance.
- Self heating. An external temperature node (the 7th node) is supported to facilitate the simulation of thermal coupling among neighboring devices.
- A unique SOI low frequency noise model, including a new excess noise resulting from the floating body effect [3].
- Width dependence of the body effect is modeled by parameters ($K1$, $K1w1$, $K1w2$).
- Improved history dependence of the body charges with two new parameters, ($Fbody$, $DLCB$).
- An instance parameter $Vbsusr$ is provided for users to set the transient initial condition of the body potential.
- The new charge-thickness capacitance model introduced in BSIM3v3.2 [4], capMod=3, is included.

BSIMPDv2.2.2 enhancements

The improvements of BSIMPDv2.2.2 include:

- A better temperature dependence of oxide tunneling current.
- An instance parameter $FRBODY$ to account for the layout-dependent distributed body RC effect.
- Bug fixes regarding the gate current implementation. Related modifications to some of the equations are highlighted later in the chapter.

BSIMPDv2.2.3 enhancements

The improvements of BSIMPDv2.2.3 include:

- CV delta L and delta W are now dependent on geometry
- The gate-body-tunneling residue problem in the low bias regime has been fixed
- An additional parameter (*dtoxcv*) has been added to *capMod*=3 to improve flexibility
- Additional defects have been corrected.



For further information, visit the website:
<http://www-device.eecs.berkeley.edu/~bsimsoi>

2.2 BSIMPD I-V Model

Body Voltages

V_{bsh} is equal to the V_{bs} bounded between (V_{bsc}, f_{s1}). V_{bsh} is used in V_{th} and A_{bulk} calculations.

$$T1 = V_{bsc} + 0.5 \left[V_{bs} - V_{bsc} - \delta + \sqrt{\left(V_{bs} - V_{bsc} - \delta \right)^2 - 4\delta V_{bsc}} \right], V_{bsc} = -5V$$

$$V_{bsh} = \phi_{s1} - 0.5 \left[\phi_{s1} - T1 - \delta + \sqrt{\left(\phi_{s1} - T1 - \delta \right)^2 + 4\delta T1} \right], \phi_{s1} = 1.5V$$

V_{bsh} is further limited to $0.95\phi_s$ to give V_{bseff} .

$$V_{bseff} = \phi_{s0} - 0.5 \left[\phi_{s0} - V_{bsh} - \delta + \sqrt{\left(\phi_{s0} - V_{bsh} - \delta \right)^2 + 4\delta V_{bsh}} \right], \phi_{s0} = 0.95\phi_s$$

Effective Channel Length and Width

$$\begin{aligned}
 dW' &= WINT + \frac{WL}{L^{WLN}} + \frac{WW}{W^{WWN}} + \frac{WWL}{L^{WLN}W^{WWN}} \\
 dW &= dW' + dW_g V_{gsteff} + dW_b (\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}) \\
 dL &= LINT + \frac{LL}{L^{LLN}} + \frac{LW}{W^{LWN}} + \frac{LWL}{L^{LLN}W^{LWN}} \\
 L_{eff} &= L_{drawn} - 2dL \\
 W_{eff} &= W_{drawn} - N_{bc} dW_{bc} - (2 - N_{bc}) dW \\
 W_{eff}' &= W_{drawn} - N_{bc} dW_{bc} - (2 - N_{bc}) dW' \\
 W_{diode} &= \frac{W_{eff}'}{N_{seg}} + P_{dbcp} \\
 W_{dios} &= \frac{W_{eff}'}{N_{seg}} + P_{sbcp}
 \end{aligned}$$

Threshold Voltage

$$\begin{aligned}
 V_{th} &= VTHO + K1(\sqrt{\Phi_s}) - K2 V_{bseff} \\
 &+ K1\left(\sqrt{1 + \frac{NLX}{L_{eff}}} - 1\right) \sqrt{\Phi_s} + (K3 + K3B \cdot V_{bseff}) \frac{TOX}{W_{eff} + WO} \Phi_s \\
 &- DVT0W \left(\exp\left(-DVT1W \frac{W_{eff}L_{eff}}{2l_{tw}}\right) + 2 \exp\left(-DVT1W \frac{W_{eff}L_{eff}}{l_{tw}}\right) \right) (V_{bi} - \Phi_s) \\
 &- DVT0 \left(\left(\exp\left(-DVT1 \frac{L_{eff}}{2l_t}\right) + 2 \exp\left(-DVT1 \frac{L_{eff}}{l_t}\right) \right) (V_{bi} - \Phi_s) \right. \\
 &\quad \left. - \left(\exp\left(-DSUB \frac{L_{eff}}{2l_{to}}\right) + 2 \exp\left(-DSUB \frac{L_{eff}}{l_{to}}\right) \right) (ETAO + ETAB \cdot V_{bseff}) V_{ds} \right. \\
 &\quad \left. sqrtPhisExt = \sqrt{\Phi_s - V_{bseff}} + (V_{bsh} - V_{bseff}), s = \frac{1}{s \sqrt{\Phi_s - \Phi_{s0}}} \right)
 \end{aligned}$$

$$K1_{eff} = K1 \left(1 + \frac{K1W1}{W_{eff} + K1W2} \right)$$

$$l_{tw} = \sqrt{\frac{\epsilon_{si} X_{dep}}{C_{ox}}} (1 + DVT2 W \cdot V_{bseff}) \quad l_{to} = \sqrt{\frac{\epsilon_{si} X_{dep0}}{C_{ox}}}$$

$$X_{dep} = \sqrt{\frac{2\epsilon_{si}(\Phi_s - V_{bseff})}{qNCH}} \quad X_{dep0} = \sqrt{\frac{2\epsilon_{si}\Phi_s}{qNCH}}$$

$$V_{bi} = v_t \ln \left(\frac{NCH \cdot N_{DS}}{n_i^2} \right) \quad litl = \sqrt{3TSI \cdot TOX}$$

Poly depletion effect

$$V_{poly} + \frac{1}{2} X_{poly} E_{poly} = \frac{qNGATE \cdot X_{poly}^2}{2\epsilon_{si}}$$

$$\epsilon_{ox} E_{ox} = \epsilon_{si} E_{poly} = \sqrt{2q\epsilon_{si} NGATE \cdot V_{poly}}$$

$$V_{gs} - V_{FB} - \phi_x = V_{poly} + V_{ox}$$

$$a(V_{gs} - V_{FB} - \phi_s - V_{poly})^2 - V_{poly} = 0$$

$$a = \frac{\epsilon_{ox}^2}{2q\epsilon_{si} NGATE \cdot TOX^2}$$

$$V_{gs_eff} = V_{FB} + \phi_s + \frac{q\epsilon_{si} NGATE \cdot TOX^2}{\epsilon_{ox}^2} \left(\sqrt{1 + \frac{2\epsilon_{ox}^2(V_{gs} - V_{FB} - \phi_s)}{q\epsilon_{si} NGATE \cdot TOX^2}} - 1 \right)$$

Effective V_{gst} for all region (with Polysilicon Depletion Effect)

$$V_{gsteff} = \frac{2n\tau_t \ln \left[1 + \exp \left(\frac{V_{gs_eff} - V_{th}}{2n\tau_t} \right) \right]}{1 + 2nC_{ox} \sqrt{\frac{2\phi_s}{q\epsilon_{si}NCH}} \cdot \exp \left(-\frac{V_{gs_eff} - V_{th} - 2VOFF}{2n\tau_t} \right)}$$

$$n = 1 + NFACTOR \cdot \frac{\epsilon_{si}/X_{dep}}{C_{ox}} + \frac{(CDSC + CDSCD \cdot V_{ds} + CDSCB \cdot V_{bs}) \left(\exp \left(-DVT1 \frac{L_{eff}}{2l_t} \right) + 2 \exp \left(-DVT1 \frac{L_{eff}}{l_t} \right) \right)}{C_{ox}} + \frac{CIT}{C_{ox}}$$

Effective Bulk Charge Factor

$$A_{bulk} = 1 + \left(\frac{K1_{eff}}{2 \sqrt{\phi_s + KETAS - \frac{V_{bsh}}{1 + KETA \cdot V_{bsh}}}} \left(\frac{A0L_{eff}}{L_{eff} + 2 \sqrt{TSI \cdot X_{dep}}} \cdot \right. \right. \\ \left. \left. \left(1 - AGS \cdot V_{gsteff} \left(\frac{L_{eff}}{L_{eff} + 2 \sqrt{TSI \cdot X_{dep}}} \right)^2 \right) + \frac{B0}{W_{eff} + B1} \right) \right)$$

$$A_{bulk0} = A_{bulk}(V_{gsteff} = 0)$$

Mobility and Saturation Velocity

- For $MOBMOD=1$

$$\mu_{eff} = \frac{\mu_0}{1 + (UA + UC \cdot V_{bs}) \left(\frac{V_{gsteff} + 2V_{th}}{TOX} \right) + UB \left(\frac{V_{gsteff} + 2V_{th}}{TOX} \right)^2}$$

- For ***MOBMOD***=2

$$\mu_{eff} = \frac{\mu_0}{1 + (UA + UC \cdot V_{bseff})\left(\frac{V_{gsteff}}{TOX}\right) + UB\left(\frac{V_{gsteff}}{TOX}\right)^2}$$

- For ***MOBMOD***=3

$$\mu_{eff} = \frac{\mu_0}{1 + \left[UA\left(\frac{V_{gsteff} + 2V_{th}}{TOX}\right) + UB\left(\frac{V_{gsteff} + 2V_{th}}{TOX}\right)^2 \right] (1 + UC \cdot V_{bseff})}$$

Drain Saturation Voltage

- For ***R_{ds}***>0 or $\lambda \neq 1$

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

$$a = A_{bulk}^2 W_{eff} VSAT \cdot C_{ox} R_{DS} + \left(\frac{1}{\lambda} - 1\right) A_{bulk}$$

$$\begin{aligned} b = & -\left((V_{gsteff} + 2v_t)\left(\frac{2}{\lambda} - 1\right) + A_{bulk} E_{sat} L_{eff} \right. \\ & \left. + 3A_{bulk}(V_{gsteff} + 2v_t)W_{eff} VSAT \cdot C_{ox} R_{DS} \right) \end{aligned}$$

$$c = (V_{gsteff} + 2v_t)E_{sat}L_{eff} + 2(V_{gsteff} + 2v_t)^2 W_{eff} VSAT \cdot C_{ox} R_{DS}$$

$$\lambda = A1 V_{gsteff} + A2$$

- For ***R_{ds}***=0, $\lambda=1$

$$V_{dsat} = \frac{E_{sat} L_{eff} (V_{gsteff} + 2v_t)}{A_{bulk} E_{sat} L_{eff} + (V_{gsteff} + 2v_t)}$$

$$E_{sat} = \frac{2VSAT}{\mu_{eff}}$$

V_{dseff}

$$V_{dseff} = V_{dsat} - \frac{1}{2}(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}})$$

Drain current expression

$$I_{ds, MOSFET} = \frac{1}{N_{seg}} \cdot \frac{I_{ds0}(V_{dseff})}{1 + \frac{R_{ds}I_{ds0}(V_{dseff})}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A} \right)$$

$$\beta = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}}$$

$$I_{ds0} = \frac{\beta V_{gsteff} \left(1 - A_{bulk} \frac{V_{dseff}}{2[V_{gsteff} + 2v_t]} \right) V_{dseff}}{1 + \frac{V_{dseff}}{E_{sat} L_{eff}}}$$

$$V_A = V_{Asat} + \left(1 + \frac{PVAG \cdot V_{gsteff}}{E_{sat} L_{eff}} \right) \left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}} \right)^{-1}$$

$$V_{ACLM} = \frac{A_{bulk} E_{sat} L_{eff} + V_{gsteff}}{PCLM \cdot A_{bulk} E_{sat} l_{itl}} (V_{ds} - V_{dseff})$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{\theta_{rout} (1 + PDIBLCB \cdot V_{bseff})} \left(1 - \frac{A_{bulk} V_{dsat}}{A_{bulk} V_{dsat} + 2v_t} \right)$$

$$\theta_{rout} = PDIBLC1 \left[\exp \left(-DROUT \frac{L_{eff}}{2l_{t0}} \right) + 2 \exp \left(-DROUT \frac{L_{eff}}{l_{t0}} \right) \right] + PDIBLC2$$

$$V_{Asat} = \frac{E_{sat}L_{eff} + V_{dsat} + 2R_{DS}VSAT \cdot C_{ox}W_{eff}V_{gsteff} \left[1 - \frac{A_{bulk}V_{dsat}}{2(V_{gsteff} + 2v_t)} \right]}{\frac{2}{\lambda} - 1 + R_{DS}VSAT \cdot C_{ox}W_{eff}A_{bulk}}$$

$$l_{itl} = \sqrt{\frac{\epsilon_{si}TOX \cdot TSI}{\epsilon_{ox}}}$$

Drain/Source Resistance

$$R_{ds} = R_{DSW} \cdot \frac{1 + PRWG \cdot V_{gsteff} + PRWB(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})}{(10^6 W'_{eff})^{WR}}$$

Impact Ionization Current

$$I_{ii} = ALPHA0(I_{ds, MOSFET} + F_{bjtii}I_c) \cdot$$

$$\exp\left(-\frac{V_{diff}}{BETA2 + BETA1 V_{diff} + BETA0 V_{diff}^2}\right)$$

$$V_{diff} = V_{ds} - V_{dsatii}$$

$$V_{dsatii} = VgsStep + \left[V_{dsatii0} \left(1 + TII \left(\frac{T}{TNOM} - 1 \right) \right) - \frac{LII}{L_{eff}} \right]$$

$$VgsStep = \left(\frac{E_{satii}L_{eff}}{1 + E_{satii}L_{eff}} \right) \left(\frac{1}{1 + SII1 \cdot V_{gsteff}} + SII2 \right) \left(\frac{SII0 \cdot V_{gst}}{1 + SIID \cdot V_{ds}} \right)$$

Gate-Induced-Drain-Leakage (GIDL)

- At drain

$$I_{dgidl} = W_{diod} A GIDL \cdot E_s \cdot \exp\left(-\frac{B GIDL}{E_s}\right)$$

$$E_s = \frac{V_{ds} - V_{gs} - \chi}{3 \cdot TOX}$$

- At source

$$I_{sgidl} = W_{dios} A GIDL \cdot E_s \cdot \exp\left(-\frac{B GIDL}{E_s}\right)$$

$$E_s = \frac{-V_{gs} - \chi}{3 \cdot TOX}$$



If E_s is negative, I_{gidl} is set to zero for both drain and source.

Note

Body contact current

If $VERSION \geq 2.22$

$$R_{bp} = \frac{FRBODY \cdot RBODY \cdot RHALO}{(2 \cdot RBODY + RHALO \cdot L_{eff})} \cdot \frac{W_{eff}}{N_{seg}}$$

Else if $VERSION \geq 2.21$

$$R_{bp} = \frac{RBODY \cdot RHALO}{(2 \cdot RBODY + RHALO \cdot L_{eff})} \cdot \frac{W_{eff}}{N_{seg}}$$

Else

$$R_{bp} = RBODY0 \frac{\left(\frac{W_{eff}}{N_{seg}}\right)}{L_{eff}} \quad R_{bodyext} = RBSH \cdot N_{rb}$$

- For 4-T device

$$I_{bp} = 0$$

- For 5-T device

$$I_{bp} = \frac{V_{bp}}{R_{bp} + R_{bodyext}}$$

Diode and BJT currents

- For source side:

Bipolar Transport Factor

$$\alpha_{bjt} = \exp\left[-0.5\left(\frac{L_{eff}}{L_n}\right)^2\right]$$

Body-to-Source/drain Diffusion

$$I_{bs1} = W_{dios} TSI j_{sdif} \left(\exp\left(\frac{V_{bs}}{NDIODE \cdot V_t}\right) - 1 \right)$$

$$I_{bd1} = W_{diode} TSI j_{sdif} \left(\exp\left(\frac{V_{bd}}{NDIODE \cdot V_t}\right) - 1 \right)$$

Recombination/trap-assisted Tunneling in the Depletion Region

$$I_{bjt} = W_{dios} \cdot TSI \cdot j_{srec} \left(\exp\left(\frac{V_{bs}}{0.026n_{recf}}\right) - \exp\left(\frac{V_{sb}}{0.026n_{recr}} \cdot \frac{V_{rec0}}{V_{rec0} + V_{sb}}\right) \right)$$

$$I_{bd2} = W_{diode} \cdot TSI \cdot j_{srec} \left(\exp\left(\frac{V_{bd}}{0.026n_{recf}}\right) - \exp\left(\frac{V_{db}}{0.026n_{recr}} \cdot \frac{V_{rec0}}{V_{rec0} + V_{db}}\right) \right)$$

Reversed bias tunneling leakage

$$I_{bs4} = W_{dios} \cdot TSI \cdot j_{stun} \left(1 - \exp \left(\frac{NTUN \cdot V_{sb}}{V_{tun0} + V_{sb}} \right) \right)$$

$$I_{bd4} = W_{diode} \cdot TSI \cdot j_{stun} \left(1 - \exp \left(\frac{NTUN \cdot V_{db}}{V_{tun0} + V_{db}} \right) \right)$$

Recombination in neutral body

$$I_{bs3} = (1 - \alpha_{bjt}) I_{en} \left[\exp \left(\frac{V_{bs}}{NDIODE \cdot V_t} \right) - 1 \right] \cdot \frac{1}{\sqrt{E_{hlis} + 1}}$$

$$I_{bd3} = (1 - \alpha_{bjt}) I_{en} \left[\exp \left(\frac{V_{bd}}{NDIODE \cdot V_t} \right) - 1 \right] \cdot \frac{1}{\sqrt{E_{hlid} + 1}}$$

$$I_{en} = \frac{W'_{eff}}{N_{seg}} TSI \cdot j_{sbjt} \left[L_{bjt0} \left(\frac{1}{L_{eff}} + \frac{1}{L_n} \right) - 1 \right]^{Nbjt}$$

$$E_{hlis} = A_{hli_eff} \left[\exp \left(\frac{V_{bs}}{NDIODE \cdot V_t} \right) - 1 \right]$$

$$E_{hlid} = A_{hli_eff} \left[\exp \left(\frac{V_{bd}}{NDIODE \cdot V_t} \right) - 1 \right]$$

$$A_{hli_eff} = A_{hli} \exp \left[\frac{-E_g(300K)}{NDIODE \cdot V_t} XBJT \left(1 - \frac{T}{TNOM} \right) \right]$$

BJT collector current

$$I_c = \alpha_{bjt} I_{bs3} \left\{ \exp \left(\frac{V_{bs}}{NDIODE \cdot V_t} \right) - \exp \left(\frac{V_{bs}}{NDIODE \cdot V_t} \right) \right\} \frac{1}{E_{2nd}}$$

$$E_{2nd} = \frac{E_{ely} + \sqrt{E_{ely}^2 + 4E_{hli}}}{2}$$

$$E_{ely} = 1 + \frac{V_{bs} + V_{bd}}{V_{Abjt} + A_{ely}L_{eff}}$$

$$E_{hli} = E_{hlis} + E_{hlid}$$

Total body-source/drain current

$$I_{bs} = I_{bs1} + I_{bs2} + I_{bs3} + I_{bs4}$$

$$I_{bd} = I_{bd1} + I_{bd2} + I_{bd3} + I_{bd4}$$

Gate Direct Tunneling Current Model

As the gate oxide thickness is scaled down to 3 nm and below, gate leakage current due to carrier direct tunneling becomes important. This tunneling happens between the gate and silicon beneath the gate oxide. The tunneling carriers can be either electrons or holes, or both, either from the conduction band or valence band, depending on (the type of the gate and) the bias regime.

In BSIM3SOI, the gate tunneling components include the tunneling current between gate and substrate/body (I_{gb}). [Figure 20-2](#) shows the schematic gate tunneling current flows.

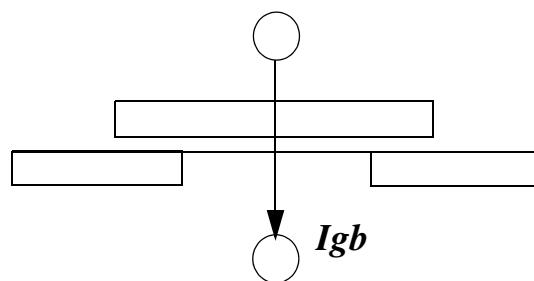


Figure 20-2. Schematic gate current components flowing between NMOST terminals in version

Model selectors

One global selector is provided to turn on or off the tunneling components. $IGMOD=1$ turns on I_{gb} . When the selector is set to zero, no gate tunneling current is modeled.

Voltage Across Oxide V_{ox}

The oxide voltage V_{ox} is written as $V_{ox} = V_{oxacc} - V_{oxdepinv}$ with

$$V_{oxacc} = V_{fbzb} - V_{FBeff}$$

$$V_{oxdepinv} = K_{1ox}\sqrt{\Phi_s} + V_{gsteff}$$

The above equations are valid and continuous from accumulation through depletion to inversion. V_{fbzb} is the flat-band voltage calculated from zero-bias V_{th} by

$$V_{fbzb} = V_{th}|_{zero\,V_{bs}and\,V_{ds}} - \Phi_s - K_1\sqrt{\Phi_s}$$

and

$$V_{FBeff} = V_{fbzb} - 0.5 \left[(V_{fbzb} - V_{gb} - 0.02) + \sqrt{(V_{fbzb} - V_{gb} - 0.02)^2 + 0.08V_{fbzb}} \right]$$

Equations for Tunneling Currents

- Gate-to-Substrate Current:

$$I_{gb} = I_{gbacc} + I_{gbinv}$$

I_{gbacc} , determined by ECB (Electron tunneling from Conduction Band) is significant in accumulation and given by:

$$I_{gbacc} = W_{eff} \cdot L_{eff} \cdot A \cdot OxideRatio \cdot V_{gb} \cdot V_{aux} \cdot$$

$$\exp \left[\frac{-B \cdot TOXQM \cdot (ALPHAGB2 - BETAGB2 \cdot V_{oxacc})}{(1 - V_{oxacc}/VGB2)} \right]$$

where the physical constants $A = 4.9758 \times 10^{-7}$ A/V²,
 $B = 2.357 \times 10^{10}$ (g/F-s²)^{0.5}, and

$$OxideRatio = \left(\frac{TOXREF}{TOXQM} \right)^{NTOX} \cdot \frac{1}{TOXQM^2}$$

If $VERSION \geq 2.22$

$$V_{aux} = VECB \cdot \log \left(1 + \exp \left[-\frac{V_{gb} - V_{fbzb}}{VECB} \right] \right)$$

Else

$$V_{aux} = NECB \cdot v_t \cdot \log \left(1 + \exp \left[-\frac{V_{gb} - V_{fbzb}}{NECB \cdot v_t} \right] \right)$$

I_{gbinv} , determined by EVB (Electron tunneling from Valence Band) is significant in inversion and given by:

$$I_{gbinv} = W_{eff} \cdot L_{eff} \cdot A \cdot OxideRatio \cdot V_{gb} \cdot V_{aux} \cdot$$

$$\exp \left[\frac{-B \cdot TOXQM \cdot (ALPHAGB1 - BETAGB1 \cdot V_{oxdepinv})}{(1 - V_{oxdepinv}/VGB1)} \right]$$

where the physical constants $A = 3.7622 \times 10^{-7}$ A/V²,
 $B = 3.1051 \times 10^{10}$ (g/F-s²)^{0.5}, and

If $VERSION \geq 2.22$

$$V_{aux} = VEVB \cdot \log\left(1 + \exp\left[\frac{V_{oxdepinv} - EBG}{VEVB}\right]\right)$$

Else

$$V_{aux} = NEVB \cdot v_t \cdot \log\left(1 + \exp\left[\frac{V_{oxdepinv} - EBG}{NEVB \cdot v_t}\right]\right)$$

Total body current

$$I_{ii} + I_{dgidl} + I_{sgidl} - I_{bs} - I_{bd} - I_{bp} + I_{gb} = 0$$

Temperature effects

$$V_{th(T)} = V_{th(TNOM)} + \left(KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{bseff}\right) \left(\frac{T}{TNOM} - 1\right)$$

$$UO_{(T)} = UO_{(TNOM)} \left(\frac{T}{TNOM}\right)^{UTE}$$

$$VSAT_{(T)} = VSAT_{(TNOM)} - AT \left(\frac{T}{TNOM} - 1\right)$$

$$RDSW_{(T)} = RDSW_{(TNOM)} + PRT \left(\frac{T}{TNOM} - 1\right)$$

$$UA_{(T)} = UA_{(TNOM)} + UA1 \left(\frac{T}{TNOM} - 1\right)$$

$$UB_{(T)} = UB_{(TNOM)} + UB1 \left(\frac{T}{TNOM} - 1\right)$$

$$UC_{(T)} = UC_{(TNOM)} + UC1 \left(\frac{T}{TNOM} - 1\right)$$

$$R_{th} = \frac{RTH0}{\left(\frac{W'_{eff}}{N_{seg}}\right)} \quad C_{th} = CTH0 \frac{W'_{eff}}{N_{seg}}$$

$$j_{sbjt} = j_{sbjt0} \exp \left[-\frac{E_g(300K)}{NDiode \cdot kT} X_{bjt} \left(1 - \frac{T}{TNOM} \right) \right]$$

$$j_{sdif} = j_{sdif0} \exp \left[-\frac{E_g(300K)}{NDiode \cdot kT} X_{dif} \left(1 - \frac{T}{TNOM} \right) \right]$$

$$j_{srec} = j_{srec0} \exp \left[-\frac{E_g(300K)}{NDiode \cdot kT} X_{rec} \left(1 - \frac{T}{TNOM} \right) \right]$$

$$j_{stun} = j_{stuno} \exp \left[XTUN \left(\frac{T}{TNOM} - 1 \right) \right]$$

$$n_{recf} = n_{recf0} \left[1 + nt_{recf} \left(\frac{T}{TNOM} - 1 \right) \right]$$

$$n_{recr} = n_{recr0} \left[1 + nt_{recr} \left(\frac{T}{TNOM} - 1 \right) \right]$$

E_g is the energy gap energy at 300K.

2.3 BSIMPD C-V Model

Dimension Dependence

$$\delta W_{eff} = DWC + \frac{WLC}{L^{WLN}} + \frac{WWC}{W^{WWN}} + \frac{WWLC}{L^{WLN} W^{WWN}}$$

$$\delta L_{eff} = DLC + \frac{LLC}{L^{LLN}} + \frac{LWC}{W^{LWN}} + \frac{LWLC}{L^{LLN} W^{LWN}}$$

$$L_{active} = L_{drawn} - 2\delta L_{eff}$$

$$L_{activeB} = L_{active} - DLCB$$

$$L_{activeBG} = L_{activeB} - 2\delta L_{bg}$$

$$W_{active} = W_{drawn} - N_{bc} dW_{bc} - (2 - N_{bc}) \delta W_{eff}$$

$$W_{diosCV} = \frac{W_{active}}{N_{seg}} + P_{sbcp}$$

$$W_{diodeCV} = \frac{W_{active}}{N_{seg}} + P_{dbcp}$$

Charge Conservation

$$Q_{Bf} = Q_{acc} + Q_{sub0} + Q_{subs}$$

$$Q_{inv} = Q_{inv,s} + Q_{inv,d}$$

$$Q_g = -(Q_{inv} + Q_{Bf})$$

$$Q_b = Q_{Bf} - Q_e + Q_{js} + Q_{jd}$$

$$Q_s = Q_{inv,s} - Q_{js}$$

$$Q_d = Q_{inv,d} - Q_{jd}$$

$$Q_g + Q_e + Q_b + Q_s + Q_d = 0$$

Intrinsic Charges

CAPMOD=2

Front Gate Body Charge

Accumulation Charge

$$V_{FBeff} = V_{fb} - 0.5 \left((V_{fb} - V_{gb} - \delta) + \sqrt{(V_{fb} - V_{gb} - \delta)^2 + \delta^2} \right)$$

$$\text{where } V_{gb} = V_{gs} - V_{bseff}$$

$$V_{fb} = V_{th} - \phi_s - K1_{eff} \sqrt{\phi_s - V_{bseff} + delvt}$$

$$V_{gsteffCV} = nv_t \ln \left(1 + \exp \left[\frac{V_{gs} - V_{th}}{nv_t} \right] \cdot \exp \left[\frac{delvt}{nv_t} \right] \right)$$

$$Q_{acc} = -F_{body} \left(\frac{W_{active} L_{active}}{N_{seg}} + A_{gbcp} \right) C_{ox} (V_{FBeff} - V_{fb})$$

Gate Induced Depletion Charge

$$Q_{sub0} = -F_{body} \left(\frac{W_{active} L_{activeB}}{N_{seg}} + A_{gbcp} \right) C_{ox} \frac{K1_{eff}^2}{2} .$$

$$\left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{FBeff} - V_{gsteffCV} - V_{bseff})}{K1_{eff}^2}} \right)$$

$$V_{dsatCV} = \frac{V_{gsteffCV}}{A_{bulkCV}}$$

$$A_{bulk0} = 1 + \left(\frac{CLC}{L_{activeB}} \right)^{CLE}$$

$$V_{dsCV} = V_{dsatCV} - \frac{1}{2}(V_{dsatCV} - V_{ds} - \delta + \sqrt{(V_{dsatCV} - V_{ds} - \delta)^2 + 4\delta V_{dsatCV}})$$

$$Q_{subs} = F_{body} \left(\frac{W_{active} L_{activeB}}{N_{seg}} + A_{gbcp} \right) K1_{eff} C_{ox} .$$

$$(A_{bulkCV} - 1) \left(\frac{V_{dsCV}}{2} - \frac{A_{bulkCV} V_{dsCV}^2}{12 \left(V_{gsteffCV} - \frac{A_{bulkCV} V_{dsCV}}{2} \right)} \right)$$

Back Gate Body Charge

$$Q_e = k_{b1} F_{body} \left(\frac{W_{active} L_{activeB}}{N_{seg}} + A_{ebcp} \right) C_{box} (V_{es} - V_{fbb} - V_{bseff})$$

Inversion Charge

$$V_{cveff} = V_{dsat, CV} - 0.5 \left\{ V_4 + \sqrt{V_4^2 + 4\delta_4 V_{dsat, CV}} \right\}$$

where $V_4 = V_{dsat, CV} - V_{ds} - \delta_4; \delta_4 = 0.02$

$$Q_{inv} = - \left(\frac{W_{active} L_{activeB}}{N_{seg}} + A_{gbcp} \right) C_{ox} \cdot$$

$$\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right) + \frac{A_{bulkCV}^2 V_{cveff}^2}{12 \left(V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right)}$$

50/50 Charge Partition

$$Q_{inv,s} = Q_{inv,d} = 0.5 \cdot Q_{inv}$$

40/60 Charge Partition

$$Q_{inv,s} = - \frac{\left(\frac{W_{active} L_{activeB}}{N_{seg}} + A_{gbcp} \right) C_{ox}}{2 \left(V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right)^2} \cdot$$

$$\left(V_{gsteffCV}^3 - \frac{4}{3} V_{gsteffCV}^2 (A_{bulkCV} V_{cveff}) + \frac{2}{3} V_{gsteff} (A_{bulkCV} V_{cveff})^2 - \frac{2}{15} (A_{bulkCV} V_{cveff})^3 \right)$$

$$Q_{inv,d} = -\frac{\left(\frac{W_{active}L_{activeB}}{N_{seg}} + A_{gbcp}\right)C_{ox}}{2\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff}\right)^2}.$$

$$\left(V_{gsteffCV}^3 - \frac{5}{3}V_{gsteffCV}^2(A_{bulkCV}V_{cveff}) + V_{gsteff}(A_{bulkCV}V_{cveff})^2 - \frac{1}{5}(A_{bulkCV}V_{cveff})^3\right)$$

0/100 Charge Partition

$$Q_{inv,s} = -\left(\frac{W_{active}L_{activeB}}{N_{seg}} + A_{gbcp}\right)C_{ox}.$$

$$\left(\frac{V_{gsteffCV}}{2} + \frac{A_{bulkCV}V_{cveff}}{4} - \frac{(A_{bulkCV}V_{cveff})^2}{24\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff}\right)}\right)$$

$$Q_{inv,d} = -\left(\frac{W_{active}L_{activeB}}{N_{seg}} + A_{gbcp}\right)C_{ox}.$$

$$\left(\frac{V_{gsteffCV}}{2} - \frac{3A_{bulkCV}V_{cveff}}{4} - \frac{(A_{bulkCV}V_{cveff})^2}{8\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff}\right)}\right)$$

CAPMOD=3 (Charge-Thickness Mode)

CAPMOD=3 is different from CAPMOD=2, in that only zero-bias flat band voltages calculated from bias-independent threshold voltages are supported.

- i** See Chapter 4 of the *BSIM3v3.2 Users's Manual* from Berkeley for the finite thickness (X_{DC}) formulation.

Front Gate Body Charge

Accumulation Charge

$$V_{FB_{eff}} = V_{fb} - 0.5 \left((V_{fb} - V_{gb} - \delta) + \sqrt{(V_{fb} - V_{gb} - \delta)^2 + \delta^2} \right)$$

$$\text{where } V_{gb} = V_{gs} - V_{bseff}$$

$$V_{fb} = V_{th} - \phi_s - K1_{eff} \sqrt{\phi_s - V_{bseff}}$$

$$Q_{acc} = -F_{body} \left(\frac{W_{active} L_{active}}{N_{seg}} + A_{gbcp} \right) C_{oxeff} V_{gbacc}$$

$$V_{gbacc} = 0.5(V_0 + \sqrt{V_0^2 + 4\delta V_{fb}})$$

$$V_0 = V_{fb} + V_{bseff} - V_{gs} - \delta$$

$$C_{oxeff} = \frac{C_{ox} C_{cen}}{C_{ox} + C_{cen}}$$

$$C_{cen} = \frac{\epsilon_{Si}}{X_{DC}}$$

Gate Induced Depletion Charge

$$Q_{sub0} = -F_{body} \left(\frac{W_{active} L_{activeB}}{N_{seg}} + A_{gbcp} \right) C_{oxeff} \frac{K1_{eff}^2}{2} \cdot \\ \left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{FB_{eff}} - V_{gsteff}CV - V_{bseff})}{K1_{eff}^2}} \right)$$

Drain Induced Depletion Charge

$$V_{dsatCV} = \frac{V_{gsteff}CV - \Phi_\delta}{A_{bulkCV}}$$

$$\Phi_\delta = \Phi_s - 2\Phi_B = v_t \ln \left[1 + \frac{V_{gsteffCV}(V_{gsteffCV} + 2K1_{eff}\sqrt{2\Phi_B})}{moinK1_{eff}v_t^2} \right]$$

$$V_{dsCV} = V_{dsatCV} - \frac{1}{2}(V_{dsatCV} - V_{ds} - \delta + \sqrt{(V_{dsatCV} - V_{ds} - \delta)^2 + 4\delta V_{dsatCV}})$$

$$Q_{subs} = F_{body} \left(\frac{W_{active}L_{activeB}}{N_{seg}} + A_{gbcp} \right) K1_{eff} C_{oxeff}.$$

$$(A_{bulkCV} - 1) \left(\frac{V_{dsCV}}{2} - \frac{A_{bulkCV} V_{dsCV}^2}{12 \left(V_{gsteffCV} - \frac{A_{bulkCV} V_{dsCV}}{2} \right)} \right)$$

Back Gate Body Charge

$$Q_e = k_{b1} F_{body} \left(\frac{W_{active}L_{activeBG}}{N_{seg}} + A_{ebcp} \right) C_{box} (V_{es} - V_{fbb} - V_{bseff})$$

Inversion Charge

$$V_{cveff} = V_{dsat, CV} - 0.5 \left\{ V_4 + \sqrt{V_4^2 + 4\delta_4 V_{dsat, CV}} \right\}$$

$$\text{where } V_4 = V_{dsat, CV} - V_{ds} - \delta_4; \delta_4 = 0.02$$

$$Q_{inv} = -\left(\frac{W_{active}L_{activeB}}{N_{seg}} + A_{gbcp}\right)C_{oxeff}.$$

$$\left(\left(V_{gsteffCV} - \Phi_\delta - \frac{A_{bulkCV}}{2} V_{cveff} \right) + \frac{A_{bulkCV}^2 V_{cveff}^2}{12 \left(V_{gsteffCV} - \Phi_\delta - \frac{A_{bulkCV}}{2} V_{cveff} \right)} \right)$$

50/50 Charge Partition

$$Q_{inv,s} = Q_{inv,d} = 0.5Q_{inv}$$

40/60 Charge Partition

$$Q_{inv,s} = -\frac{\left(\frac{W_{active}L_{activeB}}{N_{seg}} + A_{gbcp}\right)C_{oxeff}}{2\left(V_{gsteffCV} - \Phi_\delta - \frac{A_{bulkCV}}{2} V_{cveff}\right)^2}.$$

$$\left((V_{gsteffCV} - \Phi_\delta)^3 - \frac{4}{3}(V_{gsteffCV} - \Phi_\delta)^2(A_{bulkCV}V_{cveff}) + \frac{2}{3}(V_{gsteff} - \Phi_\delta) \cdot \right.$$

$$\left. (A_{bulkCV}V_{cveff})^2 - \frac{2}{15}(A_{bulkCV}V_{cveff})^3 \right)$$

$$Q_{inv, d} = -\frac{\left(\frac{W_{active}L_{activeB}}{N_{seg}} + A_{gbcp}\right)C_{oxeff}}{2\left(V_{gsteffCV} - \Phi_\delta - \frac{A_{bulkCV}}{2}V_{cveff}\right)^2}.$$

$$\left((V_{gsteffCV} - \Phi_\delta)^3 - \frac{5}{3}(V_{gsteffCV} - \Phi_\delta)^2(A_{bulkCV}V_{cveff}) + (V_{gsteff} - \Phi_\delta) \cdot \right.$$

$$\left.(A_{bulkCV}V_{cveff})^2 - \frac{1}{5}(A_{bulkCV}V_{cveff})^3\right)$$

0/100 Charge Partition

$$Q_{inv, s} = -\left(\frac{W_{active}L_{active}}{N_{seg}} + A_{gbcp}\right)C_{oxeff}.$$

$$\left(\frac{V_{gsteffCV} - \Phi_\delta}{2} + \frac{A_{bulkCV}V_{cveff}}{4} - \frac{(A_{bulkCV}V_{cveff})^2}{24\left(V_{gsteffCV} - \Phi_\delta - \frac{A_{bulkCV}}{2}V_{cveff}\right)}\right)$$

$$Q_{inv, d} = -\left(\frac{W_{active}L_{active}}{N_{seg}} + A_{gbcp}\right)C_{oxeff}.$$

$$\left(\frac{V_{gsteffCV} - \Phi_\delta}{2} - \frac{3A_{bulkCV}V_{cveff}}{4} - \frac{(A_{bulkCV}V_{cveff})^2}{8\left(V_{gsteffCV} - \Phi_\delta - \frac{A_{bulkCV}}{2}V_{cveff}\right)}\right)$$

Overlap Capacitance

Source Overlap Charge

$$V_{gs_overlap} = \frac{1}{2} \left\{ (V_{gs} + \delta) + \sqrt{(V_{gs} + \delta)^2 + 4\delta} \right\}$$

$$\frac{Q_{overlap,s}}{W_{diosCV}} = CGS0 \cdot V_{gs}$$

$$+ CGS1 \left\{ V_{gs} - V_{gs_overlap} + \frac{CKAPPA}{2} \left(-1 + \sqrt{1 + \frac{4V_{gs_overlap}}{CKAPPA}} \right) \right\}$$

Drain Overlap Charge

$$V_{gd_overlap} = \frac{1}{2} \left\{ (V_{gd} + \delta) + \sqrt{(V_{gd} + \delta)^2 + 4\delta} \right\}$$

$$\frac{Q_{overlap,d}}{W_{diodeCV}} = CGD0 \cdot V_{gd}$$

$$+ CGD1 \left\{ V_{gd} - V_{gd_overlap} + \frac{CKAPPA}{2} \left(-1 + \sqrt{1 + \frac{4V_{gd_overlap}}{CKAPPA}} \right) \right\}$$

Gate Overlap Charge

$$Q_{overlap,g} = -(Q_{overlap,s} + Q_{overlap,d})$$

Source/Drain Junction Charge

- For $V_{bs} < 0.95\phi_s$

$$Q_{jswg} = Q_{bsdep} + Q_{bsdif}$$

else

$$Q_{jswg} = C_{bsdep}(0.95\phi_s)(V_{bs} - 0.95\phi_s) + Q_{bsdif}$$

- For $V_{bd} < 0.95\phi_s$

$$Q_{jdwg} = Q_{bddep} + Q_{bddif}$$

else

$$Q_{jdwg} = C_{bddep}(0.95\phi_s)(V_{bd} - 0.95\phi_s) + Q_{bddif}$$

where

$$Q_{bsdep} = W_{doisCV}CJSWG \frac{TSI}{10^{-7}} \frac{PBSWG}{1 - MJSWG} \left[1 - \left(1 - \frac{V_{bs}}{PBSWG} \right)^{1 - MJSWG} \right]$$

$$Q_{bddep} = W_{doidCV}CJSWG \frac{TSI}{10^{-7}} \frac{PBSWG}{1 - MJSWG} \left[1 - \left(1 - \frac{V_{bd}}{PBSWG} \right)^{1 - MJSWG} \right]$$

$$Q_{bsdif} = \frac{W'_{eff}}{N_{seg}} TSI \cdot J_{sbjt} \left[1 + L_{dif0} \left(L_{bj0} \left(\frac{1}{L_{eff}} + \frac{1}{L_n} \right)^{N_{dif}} \right) \right] \\ \left[\exp \left(\left(\frac{V_{bs}}{NDOIDE \cdot V_t} \right) - 1 \right) \right] \frac{1}{\sqrt{E_{hlis} + 1}}$$

$$Q_{bddif} = \frac{W'_{eff}}{N_{seg}} TSI \cdot J_{sbjt} \left[1 + L_{dif0} \left(L_{bj0} \left(\frac{1}{L_{eff}} + \frac{1}{L_n} \right)^{N_{dif}} \right) \right] \\ \left[\exp \left(\left(\frac{V_{bd}}{NDOIDE \cdot V_t} \right) - 1 \right) \right] \frac{1}{\sqrt{E_{hlid} + 1}}$$

$$C_{sjwg} = C_{sjwg0}[1 + t_{cjswg}(T - TNOM)]$$

$$P_{bswg} = C_{bswg0}[1 + t_{pbswg}(T - TNOM)]$$

2.4 BSIMPD Noise Models

With the **NOIMOD** parameter it is possible to use different combinations of thermal and flicker noise models as shown in the table below:

	Spice2		BSIM3	
NOIMOD	Thermal	Flk	Thermal	Flk
1	✓	✓		
2			✓	✓
3	✓			✓
4		✓	✓	

Noise in Access resistance

There are two sources for this noise: one near the drain and the other near the source.

The value for the drain side noise is defined as:

$$\overline{i_{n, th}^2} = 4(k_B T) \cdot Nrd \cdot RSH \cdot \Delta f$$

The value for the source side noise is defined as:

$$\overline{i_{n, th}^2} = 4(k_B T) \cdot Nrs \cdot RSH \cdot \Delta f$$

Shot Noise

Shot Noise is present for all SOI models except for the **FD** devices, shot noise is defined as follows:

$$\overline{i_{n, th}^2} = 2 \cdot NOIF \cdot Ibs \cdot \Delta f$$

Thermal Noise

The channel conductance Thermal Noise is defined as follows:

For **NOIMOD** = 1 & 3: $\overline{i_{n, th}^2} = \frac{8k_B T}{3} \cdot (g_m + g_{ds} + g_{mb}) \cdot \Delta f$

For **NOIMOD = 2 & 4:**

For all models, *except* **PD** model **VER = 2.23**:

$$\overline{i_{n, th}^2} = \frac{4k_B T \mu_{eff}}{L_{eff}^2} \cdot |Q_{inv}| \cdot \Delta f$$

$$\text{For } \mathbf{PD} \text{ model } \mathbf{VER = 2.23}: \overline{i_{n, th}^2} = \frac{4k_B T \mu_{eff}}{\mu_{eff} |Q_{inv}| Rds + L_{eff}^2} \cdot |Q_{inv}| \cdot \Delta f$$

Flicker Noise Model

The Flicker Noise Model is defined as follows:

$$\text{For } \mathbf{NOIMOD = 1 \& 4}: \overline{i_{n,f}^2} = \frac{KF \cdot Ids^{AF}}{Cox \cdot L_{eff}^2 \cdot f^{EF}}$$

For **NOIMOD = 2 & 3:**

when $vgs \geq Vth + 0.1$:

$$S_{si} = \frac{q^2 \cdot V_t \cdot \mu_{eff} \cdot Ids}{1 \times 10^8 \cdot Cox \cdot L_{eff}^2 \cdot f^{EF}} \cdot \left[NOIA \cdot \log\left(\frac{N_0 + NSTAR}{N_l + NSTAR}\right) + NOIB \cdot (N_0 - N_l) + NOIC \cdot \frac{N_0^2 - N_l^2}{2} \right] + \frac{V_t \cdot Ids^2 \cdot \Delta L_{clm}}{W_{eff} \cdot L_{eff}^2 \cdot f^{EF}} \cdot \frac{NOIA + NOIB \cdot N_l + NOIC \cdot N_l^2}{(N_l + NSTAR)^2}$$

with:

$$N_0 = \frac{Cox}{q} \cdot (Vgs - Vth) \quad N_l = \frac{Cox}{q} \cdot (Vgs - Vth - \min(vds, Vdsat))$$

$$\text{if } vds > Vdsat \quad \Delta L_{clm} = Litl \cdot \log\left(\frac{vds - Vdsat}{Litl \cdot Esat} + \frac{EM}{Esat}\right) \quad \text{else } \Delta L_{clm} = 0$$

$$\text{then: } \overline{i_{n,f}^2} = S_{si} \cdot \Delta f$$

when $vgs < Vth + 0.1$:

$$S_{limit} = S_{si}(vgs = Vth + 0.1)$$

$$S_{wi} = \frac{NOIA \cdot V_t \cdot Ids^2}{1 \times 10^8 \cdot W_{eff} \cdot L_{eff} \cdot f^{EF} \cdot (NSTAR)^2}$$

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{limit}}{S_{wi} + S_{limit}} \cdot \Delta f$$

If **FLKFLAG** is set to 1, **Swi** is always used in conjunction with **Ssi** even if $Vgs > Vth + 0.1$; i.e. if (**FLKFLAG=1**).

when $vgs \geq Vth + 0.1$:

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{si}}{S_{wi} + S_{si}} \cdot \Delta f$$

when $vgs < Vth + 0.1$:

$$S_{limit} = S_{si}(vgs = Vth + 0.1)$$

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{limit}}{S_{wi} + S_{limit}} \cdot \Delta f$$

Noise Printing

The above mentioned noise values could be printed or plotted for each used device as model states via the print/plot command with the following state notation:

Quantity	Description
RDNOISE	Noise in the drain access resistance
RSNOISE	Noise in the source access resistance
SHOTNOISE	Shot noise
THERMNOISE	Thermal noise
FLKNOISE	Flicker noise
NOISE	Total noise

2.5 BSIMPDv2.x Parameter List

Berkeley SPICE BSIM3SOI PD Parameters

Berkeley SPICE BSIM3SOI PD Parameters

Nr.	Name	Description	Default	Units	Binned?
1	LEVEL	Level 56 for BSIM3SOI	-	-	
2	SOIMOD	SOI model selector; for more details refer to “ SOIMOD selection ” on page 20-2	if VERSION<3.0 SOIMOD=2 (DD) else SOIMOD=0 (PD)		
3	VERSION	Version control parameter; for more details refer to “ Version Selection ” on page 20-1	3.11		
4	IGMOD	Gate current model selector	0	-	
Model Control Parameters					
5	SHMOD	Flag for self-heating 0 - no self-heating, 1 - self-heating	0		
6	MOBMOD	Mobility model selector	1		
7	CAPMOD^a	Flag for the short channel capacitance model	2		
8	NOIMOD	Flag for Noise model	1		
Process Parameters					
9	TSI	Silicon film thickness	10^{-7}	m	
10	TBOX	Buried oxide thickness	3×10^{-7}	m	
11	TOX	Gate oxide thickness	1×10^{-8}	m	
12	DTOXCV	Adjusting parameter for gate oxide thickness in C-V model for CAPMOD=3	0		
13	NCH (NPEAK)	Channel doping concentration	1.7×10^{17}	cm^{-3}	Yes
14	XJ^b	Source drain junction depth		m	
15	NSUB^c	Substrate doping concentration	6×10^{16}	cm^{-3}	Yes
16	NGATE	Poly gate doping concentration	0	cm^{-3}	Yes
17	GAMMA1	Body effect coefficient near the surface	d	$\text{V}^{1/2}$	Yes
18	GAMMA2	Body effect coefficient in the bulk	e	$\text{V}^{1/2}$	Yes
19	VBX	Body effect coefficient near the surface	f	V	Yes
DC Parameters					
20	VTH0	Threshold voltage at $V_{bs}=0$ for long and wide device	0.7		Yes
21	K1	First order body effect coefficient	0.6	$\text{V}^{1/2}$	Yes

Berkeley SPICE BSIM3SOI PD Parameters

Nr.	Name	Description	Default	Units	Binned?
22	K1W1	First body effect width parameter		m	Yes
23	K1W2	Second body effect width parameter		m	Yes
24	K2	Second order body effect coefficient	0		Yes
25	K3	Narrow width coefficient	0		Yes
26	K3B	Body effect coefficient of K3	0	V ⁻¹	Yes
27	KB1	Scaling factor for backgate charge	1		Yes
28	KB3	Coefficient of V_{bs0} dependency on V_{gs} at subthreshold region	1		Yes
29	NLX	Lateral non-uniform doping parameter	1.74×10 ⁻⁷	m	Yes
30	DVT0	First coefficient of short-channel effect on V_{th}	2.2		Yes
31	DVT1	Second coefficient of short-channel effect on V_{th}	0.53		Yes
32	DVT2	Body-bias coefficient of short-channel effect on V_{th}	-0.032	V ⁻¹	Yes
33	DVT0W	First coefficient of narrow width effect on V_{th} for small channel length	0		Yes
34	DVT1W	Second coefficient of narrow width effect on V_{th} for small channel length	5.3×10 ⁶		Yes
35	DVT2W	Body-bias coefficient of narrow width effect on V_{th} for small channel length	-0.032	V ⁻¹	Yes
36	U0	Mobility at Temp = TNOM NMOSFET PMOSFET	670 250	cm ² (Vs) ⁻¹	Yes
37	UA	First-order mobility degradation coefficient	2.25×10 ⁻⁹	mV ⁻¹	Yes
38	UB	Second-order mobility degradation coefficient	5.9×10 ⁻¹⁹	(mV ⁻¹) ²	Yes
39	UC	Body-effect of mobility degradation coefficient	-0.0465	V ⁻¹	Yes
40	VSAT	Saturation velocity at Temp=TNOM	8×10 ⁴	ms ⁻¹	Yes
41	A0	Bulk charge effect coefficient for channel length	1.0		Yes
42	AGS	Gate bias coefficient of A_{bulk}	0	V ⁻¹	Yes
43	B0	Bulk charge effect coefficient for channel width	0	m	Yes
44	B1	Bulk charge effect width offset	0	m	Yes
45	KETA	Body-bias coefficient of bulk charge effect	-0.6	V ⁻¹	Yes
46	KETAS	Surface potential adjustment for bulk charge effect	0	V	Yes
47	ADICE0	DICE bulk charge factor	1		Yes
48	A1	First non-saturation effect parameter	0	V ⁻¹	Yes

Berkeley SPICE BSIM3SOI PD Parameters

Nr.	Name	Description	Default	Units	Binned?
49	A2	Second non-saturation effect parameter	1.0	0	Yes
50	RDSW	Parasitic resistance with respect to unit width	100	$\Omega \mu\text{m}^{\text{WR}}$	Yes
51	PRWB	Body effect coefficient of RDSW	0	V^{-1}	Yes
52	PRWG	Gate bias effect coefficient of RDSW	0	$\text{V}^{-1/2}$	Yes
53	WR	Width offset from W_{eff} for Rds calculation	1		Yes
54	WINT	Width offset fitting parameter from I-V without bias	0	m	
55	LINT	Length offset fitting parameter from I-V without bias	0	m	
56	DWG	Coefficient of W_{eff} 's gate dependence	0	mV^{-1}	Yes
57	DWB	Coefficient of W_{eff} 's substrate body bias dependence	0	$\text{mV}^{-1/2}$	Yes
58	DWBC	Width offset voltage in the subthreshold region for large W and L	0	m	
59	VOFF	Offset voltage in the subthreshold region for large W and L	-0.08	V	Yes
60	ETA0	DIBL coefficient in subthreshold region	0.08		Yes
61	ETAB	Body-bias coefficient for the subthreshold DIBL effect	-0.07	V^{-1}	Yes
62	DSUB	DIBL coefficient exponent	0.56		Yes
63	CIT	Interface trap capacitance	0	Fm^{-2}	Yes
64	CDSC	Drain/Source to channel coupling capacitance	2.4×10^{-4}	Fm^{-2}	Yes
65	CDSCB	Body-bias sensitivity of CDSC	0	Fm^{-2}	Yes
66	CDSCD	Drain-bias sensitivity of CDSC	0	Fm^{-2}	Yes
67	PCLM	Channel length modulation parameter	1.3		Yes
68	PDIBL1	First output resistance DIBL effect correction parameter	0.39		Yes
69	PDIBL2	Second output resistance DIBL effect correction parameter	0.086		Yes
70	PDIBLB	Body-biad coefficient of DIBL	0.0	$1/\text{V}$	Yes
71	DROUT	L dependence coefficient of the DIBL correction parameter in Rout	0.56		Yes
72	PVAG	Gate dependence of Early voltage	0		Yes
73	DELTA	Effective V_{ds} parameter	0.01		Yes
74	ALPHA0	The first parameter of impact ionization current	0	mV^{-1}	Yes

Berkeley SPICE BSIM3SOI PD Parameters

Nr.	Name	Description	Default	Units	Binned?
75	FBJTII	Fraction of bipolar current affecting the impact ionization	0		Yes
76	BETA0	First V_{ds} dependant parameter of impact ionization current	30	V^{-1}	Yes
77	BETA1	Second V_{ds} dependant parameter of impact ionization current			Yes
78	BETA2	Third V_{ds} dependant parameter of impact ionization current	0.1	V	Yes
79	VDSATII0	Nominal drain saturation voltage at threshold for impact ionization current	0.9	V	Yes
80	TII	Temperature dependent parameter for impact ionization current	0		
81	LII	Channel length dependent parameter at threshold for impact ionization current	0		Yes
82	ESATII	Saturation channel electric field for impact ionization current	1×10^7	Vm^{-1}	Yes
83	SII0	First V_{gs} dependent parameter for impact ionization current	0.5	V^{-1}	Yes
84	SII1	Second V_{gs} dependent parameter for impact ionization current	0.1	V^{-1}	Yes
85	SII2	Third V_{gs} dependent parameter for impact ionization current	0	V^{-1}	Yes
86	SIID	V_{ds} dependent parameter of drain saturation voltage for impact ionization current	0	V^{-1}	Yes
87	AGIDL	GIDL constant	0	Ω^{-1}	Yes
88	BGIDL	GIDL exponential coefficient	0	Vm^{-1}	Yes
89	NGIDL	GIDL V_{ds} enhancement coefficient	1.2	V	Yes
90	NTUN	Reverse tunneling non-ideality factor	10.0		Yes
91	NDIODE	Diode non-ideality factor	1.0		Yes
92	NRECF0	Recombination non-ideality factor at forward bias	2.0		Yes
93	NRECR0	Recombination non-ideality factor at reversed bias	10		Yes
94	ISBJT	BJT injection saturation current	1×10^{-6}	Am^{-2}	Yes
95	ISDIF	Body to source/drain injection saturation current	0	Am^{-2}	Yes
96	ISREC	Recombination in depletion saturation current	1×10^{-5}	Am^{-2}	Yes
97	ISTUN	Reverse tunneling saturation current	0	Am^{-2}	Yes
98	LN	Electron/hole diffusion length	2×10^{-6}	m	

Berkeley SPICE BSIM3SOI PD Parameters

Nr.	Name	Description	Default	Units	Binned?
99	VRECO	Voltage dependent parameter for recombination current	0	V	Yes
100	VTUN0	Voltage dependent parameter for tunneling current	0	V	Yes
101	NBJT	Power coefficient of channel length dependency for bipolar current	1		Yes
102	LBJT0	Reference channel length for bipolar current	2×10^{-7}	m	Yes
103	VABJT	Early voltage for bipolar current	10	V	Yes
104	AELY	Channel length dependency of early voltage for bipolar current	0	Vm^{-1}	Yes
105	AHLI	High level injection parameter for bipolar current	0		Yes
106	RBODY	Intrinsic body contact sheet resistance	0	$\Omega \text{ m}^{-2}$	
107	RBSH	Extrinsic body contact sheet resistance	0	$\Omega \text{ m}^{-2}$	
108	RSH	Source drain sheet resistance in ohm per square	0	Ω/square	
AC and Capacitance Parameters					
109	XPART	Charge partitioning rate flag	0		
110	CGSO	Non LDD region source-gate overlap capacitance per channel length	^g calculated	Fm^{-1}	
111	CGDO	Non LDD region drain-gate overlap capacitance per channel length	^h calculated	Fm^{-1}	
112	CGEO	Gate substrate overlap capacitance per unit channel length	0	Fm^{-1}	
113	CJSWG	Source/Drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm T_{si})	1×10^{-10}	Fm^{-2}	
114	PBSWG	Source/Drain (gate side) sidewall junction capacitance built in potential	0.7	V	
115	MJSWG	Source/Drain (gate side) sidewall junction capacitance grading coefficient	0.5	V	
116	TT	Diffusion capacitance transit time coefficient	1×10^{-12}	s	
117	NDIF	Power coefficient of channel length dependency for diffusion capacitance	1		
118	LDIF0	Channel-length dependency coefficient of diffusion capacitance	1		
119	VSDFB	Source/drain bottom diffusion capacitance flatband voltage	ⁱ calculated	V	Yes
120	VSDTH	Source/drain bottom diffusion capacitance threshold voltage	ⁱ calculated	V	Yes

Berkeley SPICE BSIM3SOI PD Parameters

Nr.	Name	Description	Default	Units	Binned?
121	CSDMIN	Source/drain bottom diffusion minimum capacitance	$k_{\text{calculated}}$	Fm^2	
122	ASD	Source/drain bottom diffusion smoothing parameter	0.3		
123	CSDESW	Source/drain sidewall fringing capacitance per unit length	0	Fm^{-1}	
124	CGS1	Light doped source-gate region overlap capacitance	0	Fm^{-1}	
125	CGD1	Light doped drain-gate region overlap capacitance	0	Fm^{-1}	
126	CKAPPA	Coefficient for lightly doped region overlap capacitance fringing field capacitance	0.6	Fm^{-1}	
127	CF	Gate to source/drain fringing field capacitance	$k_{\text{calculated}}$	Fm^{-1}	
128	CLC	Constant term for the short channel model	0.1×10^{-7}	m	
129	CLE	Exponential term for the short channel model	0		
130	DLC	Length offset fitting parameter from C-V	LINT	m	
131	DLCB	Length offset fitting parameter for body charge	LINT		
132	DLBG	Length offset fitting parameter for backgate charge	0	m	
133	DWC	Width offset fitting parameter from C-V	WINT	m	
134	DELVT	Threshold voltage adjust for C-V	0	V	Yes
135	FBODY	Scaling factor for body charge	1.0		
136	ACDE	Exponential coefficient for charge thickness in CAPMOD=3 for accumulation and depletion regions	1.0	mV^{-1}	Yes
137	MOIN	Coefficient for the gate-bias dependent surface potential	15	$\text{V}^{1/2}$	Yes
Gate Current Parameters					
138	TOXQM	Oxide thickness for IgB calculation	m_{TOX}	m	
139	WTH0	Minimum width for thermal resistance calculation	$n0.0$	m	
140	RHALO	Body halo sheet resistance	$n1 \times 10^{15}$	OHM/m^2	
141	NTOX	Power term of gate current	$n1$		
142	TOXREF	Target oxide thickness	$n2.5 \times 10^{-9}$	m	
143	EBG	Effective bandgap in gate current calculation	$n1.2$	V	
144	NEVB	Valence-band electron non-ideality factor	$n3$		

Berkeley SPICE BSIM3SOI PD Parameters

Nr.	Name	Description	Default	Units	Binned?
145	ALPHAGB1	First V_{ox} dependent parameter for gate current in inversion	$^n0.35$	$(1/m)$ $[(\text{Fs}^2)/\text{g}]^{0.5}$	
146	BETAGB1	Second V_{ox} dependent parameter for gate current in inversion	$^n0.03$	$(1/\text{mV})$ $[(\text{Fs}^2)/\text{g}]^{0.5}$	
147	VGB1	Third V_{ox} dependent parameter for gate current in inversion	n300	V	
148	NECB	Conduction-band electron non-ideality factor	n1		
149	ALPHAGB2	First V_{ox} dependent parameter for gate current in accumulation	$^n0.43$	$(1/m)$ $[(\text{Fs}^2)/\text{g}]^{0.5}$	
150	BETAGB2	Second V_{ox} dependent parameter for gate current in accumulation	$^n0.05$	$(1/\text{mV})$ $[(\text{Fs}^2)/\text{g}]^{0.5}$	
151	VGB2	Third V_{ox} dependent parameter for gate current in accumulation	n17	V	
152	VOXH	The limit of V_{ox} in gate current calculation	$^n5.0$	V	
153	DELTAVOX	Smoothing parameter in the V_{ox} smoothing function	$^m0.005$	V	
154	VECB^o	V_{aux} parameter for valence-band electron tunneling	0.075	V	
155	VEVB^o	V_{aux} parameter for conductance-band electron tunneling	0.026	V	
156	FRBODY (instance parameter)	Layout dependent body-resistance coefficient	1		

Temperature Parameters

157	TNOM	Temperature at which parameters are expected	27	°C	
158	UTE	Mobility temperature exponent	-1.5		
159	KT1	Temperature coefficient for threshold voltage	-0.11	V	
160	KT11	Channel length dependence of the temperature coefficient for threshold voltage	0	Vm	
161	KT2	Body-bias coefficient of the V_{th} temperature effect	0.022		
162	UA1	Temperature coefficient for uA	4.31×10^{-9}	mV^{-1}	
163	UB1	Temperature coefficient for uB	-7.61×10^{-18}	$(\text{mV}^{-1})^2$	
164	UC1	Temperature coefficient for uC	-0.056^p	V^{-1}	
165	AT	Temperature coefficient for saturation velocity	3.3×10^4	ms^{-1}	
166	CTH0	Normalized thermal capacity	0	$\text{m}^\circ\text{C}(\text{Ws})^{-1}$	
167	TCJSWG	Temperature coefficient of C_{jswg}	0	$^\circ\text{K}^{-1}$	
168	TPBSWG	Temperature coefficient of P_{bswg}	0	$\text{V}^\circ\text{K}^{-1}$	

Berkeley SPICE BSIM3SOI PD Parameters

Nr.	Name	Description	Default	Units	Binned?
169	PRT	Temperature coefficient for RDSW	0	$\Omega \mu\text{m}$	
170	RTH0	Normalized thermal resistance	0	$\text{m}^\circ\text{CW}^{-1}$	
171	NTRECF	Temperature coefficient of N_{recf}	0		
172	NTRECR	Temperature coefficient of N_{recr}	0		
173	XBJT	Power dependence of j_{bit} on temperature	2		
174	XDIF	Power dependence of j_{dif} on temperature	2		
175	XREC	Power dependence of j_{rec} on temperature	20		
176	XTUN	Power dependence of j_{tun} on temperature	0		

- a. BSIMPD2.0 supports **CAPMOD**=2 and 3 only. **CAPMOD** 0 and 1 are not supported.
- b. In modern SOI technology, source/drain extension or LDD are commonly used. As a result, the source/drain junction depth (**XJ**) can be different from the silicon film thickness (**TSI**). By default, if **XJ** is not given, it is set to **TSI**. **XJ** is not allowed to be greater than **TSI**.
- c. BSIM3SOI refers substrate to the silicon below buried oxide, not the well region in BSIM3. It is used to calculate backgate flatband voltage (V_{fb}) and parameters related to source/drain diffusion bottom capacitance (**VS-DTH**, **VSDFB**, **CSDMIN**). Positive **NSUB** means the same type of doping as the body and negative **NSUB** means opposite type of doping.
- d. If **GAMMA1** is not specified, it is calculated using **NCH** and **Cox**.
- e. If **GAMMA2** is not specified, it is calculated using **NSUB** and **Cox**.
- f. If **VBX** is not specified, it is calculated using **PHI**, **NCH** and **XT**.
- g. If **CGSO** is not given then it is calculated using:
 - if (**DLC** is given and is greater than 0) then, $CGSO = p1 = (DLC \times cox) - cgs1$
 - if (the previously calculated $CGSO < 0$), then $CGSO = 0$
 - else $CGSO = 0.6 \times TSI \times cox$
- h. **CGDO** is calculated in a similar way to **CGSO**
- i. If (**NSUB** is positive)
 - $VSDFB = -\frac{kT}{q} \log\left(\frac{10^{20} \cdot NSUB}{n_i \cdot n_i}\right) - 0.3$
 - else $VSDFB = -\frac{kT}{q} \log\left(\frac{10^{20}}{NSUB}\right) + 0.3$
 - j. If (**NSUB** is positive)

$$\phi_{sd} = 2 \frac{kT}{q} \log\left(\frac{NSUB}{n_i}\right) \quad \gamma_{sd} = \frac{5.753 \times 10^{-12} \sqrt{NSUB}}{C_{box}}$$

$$VSDTH = VSDFB + \phi_{sd} + \gamma_{sd} \sqrt{\phi_{sd}}$$

$$\text{else } \phi_{sd} = 2 \frac{kT}{q} \log\left(-\frac{NSUB}{n_i}\right) \quad \gamma_{sd} = \frac{5.753 \times 10^{-12} \sqrt{-NSUB}}{C_{box}}$$

$$VSDTH = VSDFB - \phi_{sd} - \gamma_{sd} \sqrt{\phi_{sd}}$$

$$\text{k. } X_{sddep} = \sqrt{\frac{2\epsilon_{si}\phi_{sd}}{q|NSUB \cdot 10^6|}} \quad C_{sddep} = \frac{\epsilon_{si}}{X_{sddep}} \quad C_{sdmin} = \frac{C_{sddep}C_{box}}{C_{sddep} + C_{box}}$$

l. If CF is not given then it is calculated using $CF = \frac{2\epsilon_{ox}}{\pi} \ln\left(1 + \frac{4 \times 10^{-7}}{TOX}\right)$

m. Fatal error if not positive.

n. Should not be negative; if negative warning message is displayed.

o. These parameters are applicable only to $VERSION \geq 2.22$

p. For $MOBMOD=1$ and 2, the unit is mV^{-2} . Default is -5.6×10^{-11} .

For $MOBMOD=3$, the unit is V^{-1} . Default is -0.056.

2.6 BSIMFDv2.x

BSIMSOI is the officially released SOI (Silicon On Insulator) MOSFET model from the Device Group at the University of California at Berkeley. The model can be used for both Partially Depleted (PD) and Fully Depleted (FD) devices. This section is only about FD. The basic I-V model is modified from the BSIM3v3.1 equation set. The major features are summarized as follows:

- Supports external body bias and backgate bias; a total of 6 nodes.
- Real floating body simulation in both I-V and C-V. Body potential is properly bounded by diode and C-V formulation.
- Self heating implementation improved over the alpha version.
- An improved impact ionization current model.
- Various diode leakage components and parasitic bipolar current included.
- New depletion charge model (**EBCI**) introduced for better accuracy in capacitive coupling prediction. An improved BSIM3v3 based model is added as well.
- Single I-V expression as in BSIM3v3.1 to guarantee continuities of I_{ds} , G_{ds} and G_m and their derivatives for all bias conditions.

2.7 BSIMFD I-V Model

V_{bs0}—Body potential at full depletion & strong inversion conditions

(assuming no substrate depletion)

$$T_{sieff} = \sqrt{TSI^2 - 2\frac{\epsilon_{si}VBSA}{qN_a}} \quad C_{sieff} = \frac{\epsilon_{si}}{T_{sieff}} \quad Q_{sieff} = qN_a T_{sieff}$$

$$V_{bs0t} = \phi_s - 0.5 \cdot \frac{Q_{si}}{C_{si}} + VBSA + DVBD0 \cdot \left[\exp\left(-DVBD1 \frac{L_{eff}}{2litl}\right) + 2 \exp\left(-DVBD1 \frac{L_{eff}}{litl}\right) \right] \cdot (V_{bi} - \phi_s)$$

$$V_{bs0} = V_{bs0t} - KB1 \frac{V_{bs0t} - V_{es} + V_{fbb}}{1 + \frac{C_{sieff}}{C_{box}}}$$

V_{thfd}—Threshold voltage at fully depleted condition (V_{bs} = V_{bs0})

$$V_{thfd} = V_{th}(V_{bs} = V_{bs0})$$

V_{bs0eff}/V_{bs0teff}—Effective V_{bs0}/V_{bs0t} for all V_{gs}

$$T_0 = 0.5 \left[(V_{thfd} - V_{gs_eff}) - \delta_1 + \sqrt{\left[(V_{thfd} - V_{gs_eff}) - \delta_1 \right]^2 + \delta_1^2} \right]$$

$$V_{bs0teff} = V_{bs0t} - T_0$$

$$V_{bs0eff} = V_{bs0} - n_{Fb} \cdot T_0$$

$$n_{Fb} = \frac{1}{1 + K3B \frac{C_{box}}{C_{ox}} \sqrt{1 + \frac{4}{K1^2} (\phi_s + K1 \sqrt{\phi_s - V_{bs0mos}} - V_{bs0mos})}}$$

where V_{bs0mos} is the effective V_{bs} when V_{bs} = V_{bs0}.

It basically makes V_{bs0eff} & $V_{bs0teff}$ a function of V_{gs} as the following if $V_{gs} < V_{thfd}$.

$$V_{bs0eff} = V_{bs0} + n_{Fb} \cdot (V_{gs} - V_{thfd})$$

$$V_{bs0teff} = V_{bs0t} + (V_{gs} - V_{thfd})$$

V_{bseff}—Equivalent V_{bs} bias for MOS IV calculation

$$T_1 = 0.5 \left[(V_{bs0teff} - V_{bs}) - \delta_2 + \sqrt{\left[(V_{bs0teff} - V_{bs}) - \delta_2 \right]^2 + \delta_2^2} \right]$$

$$V_{bsmos} = V_{bs} - \frac{C_{sieff} T_1^2}{2 \cdot Q_{sieff}}$$

It basically makes V_{bsmos} a function of $V_{bs0teff}$ as the following if $V_{bs} < V_{bs0teff}$

$$V_{bsmos} = V_{bs} - \frac{C_{sieff} (V_{bs0teff} - V_{bs})^2}{2 \cdot Q_{sieff}}$$

otherwise

$$V_{bsmos} = V_{bs}$$



V_{bs} is properly bounded to V_{bs0eff} because of the diode implementation.

Note

$V_{bseff} = V_{bsmos}$ is limited to $\phi_s - DELP$ by the following conversion:

$$V_{bseff} = (\phi_s - DELP) - 0.5 \left[(\phi_s - DELP - V_{bsmos}) - \delta_1 + \sqrt{\left[(\phi_s - DELP - V_{bsmos}) - \delta_1 \right]^2 + 4\delta_1(\phi_s - DELP)} \right]$$

Threshold Voltage

$$\begin{aligned}
 V_{th} = & VTHO + K1(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}) - K2V_{bseff} \\
 & + K1\left(\sqrt{1 + \frac{NLX}{L_{eff}}} - 1\right)\sqrt{\Phi_s} + (K3 + K3B \cdot V_{bseff})\frac{TOX}{W_{eff} + WO}\Phi_s \\
 & - DVT0W\left(\exp\left(-DVT1W\frac{W_{eff}L_{eff}}{2l_{tw}}\right) + 2\exp\left(-DVT1W\frac{W_{eff}L_{eff}}{l_{tw}}\right)\right)(V_{bi} - \Phi_s) \\
 & - DVT0\left(\left(\exp\left(-DVT1\frac{L_{eff}}{2l_t}\right) + 2\exp\left(-DVT1\frac{L_{eff}}{l_t}\right)\right)(V_{bi} - \Phi_s)\right. \\
 & \left. - \left(\exp\left(-DSUB\frac{L_{eff}}{2l_{to}}\right) + 2\exp\left(-DSUB\frac{L_{eff}}{l_{to}}\right)\right)(ETAO + ETAB \cdot V_{bseff})V_{ds}\right) \\
 l_t = & \sqrt{\frac{\epsilon_{si}X_{dep}}{C_{ox}}}(1 + DVT2 \cdot V_{bseff}) \\
 l_{tw} = & \sqrt{\frac{\epsilon_{si}X_{dep}}{C_{ox}}}(1 + DVT2W \cdot V_{bseff}) \quad l_{to} = \sqrt{\frac{\epsilon_{si}X_{dep0}}{C_{ox}}} \\
 X_{dep} = & \sqrt{\frac{2\epsilon_{si}(\Phi_s - V_{bseff})}{qNCH}} \quad X_{dep0} = \sqrt{\frac{2\epsilon_{si}\Phi_s}{qNCH}} \\
 V_{bi} = & v_t \ln\left(\frac{NCH \cdot N_{DS}}{n_i^2}\right) \quad litl = \sqrt{3TSI \cdot TOX}
 \end{aligned}$$

Poly depletion effect

$$V_{poly} + \frac{1}{2}X_{poly}E_{poly} = \frac{qNGATE \cdot X_{poly}^2}{2\epsilon_{si}}$$

$$\epsilon_{ox}E_{ox} = \epsilon_{si}E_{poly} = \sqrt{2q\epsilon_{si}NGATE \cdot V_{poly}}$$

$$V_{gs} - V_{FB} - \phi_x = V_{poly} + V_{ox}$$

$$a(V_{gs} - V_{FB} - \phi_s - V_{poly})^2 - V_{poly} = 0$$

$$a = \frac{\epsilon_{ox}^2}{2q\epsilon_{si}N GATE \cdot TOX^2}$$

$$V_{gs_eff} = V_{FB} + \phi_s + \frac{q\epsilon_{si}N GATE \cdot TOX^2}{\epsilon_{ox}^2} \left(\sqrt{1 + \frac{2\epsilon_{ox}^2(V_{gs} - V_{FB} - \phi_s)}{q\epsilon_{si}N GATE \cdot TOX^2}} - 1 \right)$$

Effective V_{gst} for all region (with Polysilicon Depletion Effect)

$$V_{gsteff} = \frac{2n\nu_t \ln \left[1 + \exp \left(\frac{V_{gs_eff} - V_{th}}{2n\nu_t} \right) \right]}{1 + 2nC_{ox} \sqrt{\frac{2\phi_s}{q\epsilon_{si}N CH}} \cdot \exp \left(-\frac{V_{gs_eff} - V_{th} - 2V_{OFF}}{2n\nu_t} \right)}$$

$$n = 1 + NFACTOR \cdot \frac{\epsilon_{si}/X_{dep}}{C_{ox}} + \frac{(CDSC + CDSCD \cdot V_{ds} + CDSCB \cdot V_{bs_eff}) \left(\exp \left(-DVT1 \frac{L_{eff}}{2l_t} \right) + 2 \exp \left(-DVT1 \frac{L_{eff}}{l_t} \right) \right)}{C_{ox}} + \frac{CIT}{C_{ox}}$$

Effective Bulk Charge Factor

$$V_{cs} = V_{bs} - V_{bs0eff}$$

$$T_1 = 1 - 0.5 \left[\left(1 - \frac{V_{cs}}{ABP \cdot V_{gsteff}} \right) - \delta_1 + \sqrt{\left[\left(1 - \frac{V_{cs}}{ABP \cdot V_{gsteff}} \right) - \delta_1 \right]^2 + \delta_1^2} \right]$$

$$X_{csat} = MXC \cdot T_1^2 + (1 - MXC)T_1$$

X_{csat} is a parameter describing the dynamic depletion effect for a given V_{gs} . It varies within (0, 1). The parameter MXC is used to adjust the slope of transition.

$$A_{bulk} = 1 + \left(\frac{K_1}{2\sqrt{\phi_s}} \left(\frac{A0L_{eff}}{L_{eff} + 2\sqrt{TSI \cdot X_{dep}}} \left(1 - AGS \cdot V_{gsteff} \left(\frac{L_{eff}}{L_{eff} + 2\sqrt{TSI \cdot X_{dep}}} \right)^2 \right) \right. \right. \\ \left. \left. + \frac{B0}{W_{eff} + B1} \right) \right) \frac{1}{1 + KETA \cdot V_{bseff}}$$

$$A_{beff} = X_{csat} A_{bulk} + (1 - X_{csat}) A_{dice}$$

$$A_{dice} = \frac{ADICE0}{1 + C_{boxt}/C_{ox}}$$

$$C_{boxt} = \frac{C_{si}C_{box}}{C_{si} + C_{box}}$$

Mobility and Saturation Velocity

$$\mu_{eff} = \frac{\mu_0}{1 + (UA + UC \cdot V_{bseff}) \left(\frac{V_{gsteff}}{TOX} \right) + UB \left(\frac{V_{gsteff}}{TOX} \right)^2}$$

- For **MOBMOD=3**

$$\mu_{eff} = \frac{\mu_0}{1 + \left[UA \left(\frac{V_{gsteff} + 2V_{th}}{TOX} \right) + UB \left(\frac{V_{gsteff} + 2V_{th}}{TOX} \right)^2 \right] (1 + UC \cdot V_{bseff})}$$

Drain Saturation Voltage

- For $R_{ds}>0$ or $\lambda \neq 1$

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

$$a = A_{beff}^2 W_{eff} VSAT \cdot C_{ox} R_{DS} + \left(\frac{1}{\lambda} - 1 \right) A_{beff}$$

$$b = -\left((V_{gsteff} + 2v_t) \left(\frac{2}{\lambda} - 1 \right) + A_{beff} E_{sat} L_{eff} \right.$$

$$\left. + 3A_{beff}(V_{gsteff} + 2v_t) W_{eff} VSAT \cdot C_{ox} R_{DS} \right)$$

$$c = (V_{gsteff} + 2v_t) E_{sat} L_{eff} + 2(V_{gsteff} + 2v_t)^2 W_{eff} VSAT \cdot C_{ox} R_{DS}$$

$$\lambda = A1 V_{gsteff} + A2$$

- For $R_{ds}=0, \lambda=1$

$$V_{dsat} = \frac{E_{sat} L_{eff} (V_{gsteff} + 2v_t)}{A_{beff} E_{sat} L_{eff} + (V_{gsteff} + 2v_t)}$$

$$E_{sat} = \frac{2VSAT}{\mu_{eff}}$$

V_{dseff}

$$V_{dseff} = V_{dsat} - \frac{1}{2} (V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}})$$

δ is parameter **DELTA**.

Drain current expression

$$I_{ds, MOSFET} = \frac{I_{ds0}(V_{dseff})}{1 + \frac{R_{ds} I_{ds0}(V_{dseff})}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A} \right)$$

$$\beta = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}}$$

$$I_{ds0} = \frac{\beta V_{gsteff} \left(1 - A_{beff} \frac{V_{dseff}}{2[V_{gsteff} + 2v_t]} \right) V_{dseff}}{1 + \frac{V_{dseff}}{E_{sat} L_{eff}}}$$

$$V_A = V_{Asat} + \left(1 + \frac{PVAG \cdot V_{gsteff}}{E_{sat} L_{eff}} \right) \left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}} \right)^{-1}$$

$$V_{ACLM} = \frac{A_{beff} E_{sat} L_{eff} + V_{gsteff}}{PCLM \cdot A_{beff} E_{sat} litl} (V_{ds} - V_{dseff})$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{\theta_{rout}(1 + PDIBLCB \cdot V_{bseff})} \left(1 - \frac{A_{beff} V_{dsat}}{A_{beff} V_{dsat} + 2v_t} \right)$$

$$\theta_{rout} = PDIBLC1 \left[\exp\left(-DROUT \frac{L_{eff}}{2l_{t0}}\right) + 2 \exp\left(-DROUT \frac{L_{eff}}{l_{t0}}\right) \right] + PDIBLC2$$

$$V_{Asat} = \frac{E_{sat} L_{eff} + V_{dsat} + 2R_{DS} VSAT \cdot C_{ox} W_{eff} V_{gsteff} \left[1 - \frac{A_{beff} V_{dsat}}{2(V_{gsteff} + 2v_t)} \right]}{\frac{2}{\lambda} - 1 + R_{DS} VSAT \cdot C_{ox} W_{eff} A_{beff}}$$

$$litl = \sqrt{\frac{\epsilon_{si} TOX \cdot TSI}{\epsilon_{ox}}}$$

Drain/Source Resistance

$$R_{ds} = RDSW \cdot \frac{1 + PRWG \cdot V_{gsteff} + PRWB(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})}{(10^6 W_{eff})^{WR}}$$

Impact Ionization Current

$$I_{ii} = \frac{ALPHA0 + ALPHA1 L_{eff}}{L_{eff}} \cdot I_d \cdot V_{dseffii} \cdot \exp\left(-\frac{BETA0}{V_{dseffii}}\right)$$

$$V_{dsatii} = \frac{E_{sat}L_{eff}V_{gst}}{M_1E_{sat}L_{eff} + M_2V_{gst}}$$

$$M_1 = AII + \frac{BII}{L_{eff}} \quad M_2 = 1 + \left(\frac{CII}{V_{ds} - DII} \right)^2$$

$V_{dseffii}$ is calculated the same way as V_{dseff} with V_{dsat} replaced by V_{dsatii} .

Gate-Induced-Drain-Leakage (GIDL)

- At drain

$$I_{dgidl} = W_{eff} A GIDL \cdot E_s \cdot \exp\left(-\frac{BGIDL}{E_s}\right)$$

$$E_s = \frac{V_{ds} - V_{gs} - NGIDL}{3 \cdot TOX}$$

- At source

$$I_{sgidl} = W_{eff} A GIDL \cdot E_s \cdot \exp\left(-\frac{BGIDL}{E_s}\right)$$

$$E_s = \frac{-V_{gs} - NGIDL}{3 \cdot TOX}$$

Default of χ is 1.2V.

If E_s is negative, I_{gidl} is set to zero for both drain and source.

Body contact current

$$R_{bp} = RBODY0 \frac{W_{eff}}{L_{eff}} \quad R_{bodyext} = RBSH \cdot N_{rb}$$

- For 4-T device

$$I_{bp} = 0$$

- For 5-T device

$$I_{bp} = \frac{V_{bp}}{\frac{R_{bp}}{\sqrt{V_{bs} - V_{bs0eff}}} + R_{bodyext}}$$

Diode and BJT currents

- For source side:

Bipolar Transport Factor

$$W_b = L_{eff} - KBJT1 \cdot V_{ds}$$

$$\alpha_{bjt} = 1 - 0.5 \left(\frac{W_b}{EDL} \right)^2$$

V_{bs0} for diode current

$$V_{bs0_dio} = 0.5 \left[V_{bs0eff} - \delta_1 + \sqrt{[V_{bs0eff} - \delta_1]^2 + 4\delta_1} \right]$$

BJT emitter current

$$I_{bjt} = W_{eff} \cdot TSI \cdot j_{sbjt} \left(e^{\frac{V_{bs}}{NDIODE \cdot V_t}} - e^{\frac{V_{bs0_dio}}{NDIODE \cdot V_t}} \right) \left(1 - e^{-\frac{V_{ds}}{2NDIODE \cdot V_t}} \right)$$

Body-to-Source diffusion

$$I_{bs1} = W_{eff} \cdot TSI \cdot j_{sdif} \left(e^{\frac{V_{bs}}{NDIODE \cdot V_t}} - e^{\frac{V_{bs0_dio}}{NDIODE \cdot V_t}} \right)$$

Recombination in depletion region

$$I_{bs2} = W_{eff} \cdot TSI \cdot j_{srec} \left(e^{\frac{V_{bs}}{2NDIODE \cdot V_t}} - e^{\frac{V_{bs0_dio}}{NDIODE \cdot V_t}} \right)$$

Reversed bias tunneling leakage

$$I_{bs4} = W_{eff} \cdot TSI \cdot j_{stun} \left(1 - e^{-\frac{V_{bs}}{NTUN \cdot V_t}} \right)$$

Recombination in neutral body

$$I_{bs3} = (1 - \alpha_{bjt}) I_{bjt}$$

BJT collector current

$$I_c = I_{bjt} - I_{bs3}$$

Total body-source current

$$I_{bs} = I_{bs1} + I_{bs2} + I_{bs3} + I_{bs4}$$

- For drain side

if $V_{bd} > V_{bs0_dio}$

$$I_{bd1} = W_{eff} \cdot TSI \cdot j_{sdif} \left(e^{\frac{V_{bd}}{n \cdot V_t}} - e^{\frac{V_{bs0_dio}}{n \cdot V_t}} \right)$$

$$I_{bd2} = W_{eff} \cdot TSI \cdot j_{srec} \left(e^{\frac{V_{bd}}{2n \cdot V_t}} - e^{\frac{V_{bs0_dio}}{n \cdot V_t}} \right)$$

else

$$I_{bd1} = W_{eff} \cdot TSI \cdot j_{sdif} \left(e^{\frac{V_{bd} - V_{bs0_dio}}{NDIODE \cdot V_t}} - 1 \right)$$

$$I_{bd2} = W_{eff} \cdot TSI \cdot j_{srec} \left(e^{\frac{V_{bd} - V_{bs0}}{2NDIODE \cdot V_t}} - 1 \right)$$

$$I_{bd4} = W_{eff} \cdot TSI \cdot j_{stun} \left(1 - e^{-\frac{V_{bd}}{NTUN \cdot V_t}} \right)$$

Total body-drain current

$$I_{bd} = I_{bd1} + I_{bd2} + I_{bd4}$$

Total body current

$$I_{ii} + I_{dgidl} + I_{sgidl} - I_{bs} - I_{bd} - I_{bp} = 0$$

Temperature effects

$$V_{th(T)} = V_{th(T_{nom})} + \left(KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{bseff} \right) \left(\frac{T}{T_{nom}} - 1 \right)$$

$$UO_{(T)} = UO_{(T_{nom})} \left(\frac{T}{T_{nom}} \right)^{UTE}$$

$$VSAT_{(T)} = VSAT_{(T_{nom})} - AT \left(\frac{T}{T_{nom}} - 1 \right)$$

$$RDSW_{(T)} = RDSW_{(T_{nom})} + PRT \left(\frac{T}{T_{nom}} - 1 \right)$$

$$UA_{(T)} = UA_{(T_{nom})} + UA1\left(\frac{T}{T_{nom}} - 1\right)$$

$$UB_{(T)} = UB_{(T_{nom})} + UB1\left(\frac{T}{T_{nom}} - 1\right)$$

$$UC_{(T)} = UC_{(T_{nom})} + UC1\left(\frac{T}{T_{nom}} - 1\right)$$

$$R_{th} = RTH0 \cdot \sqrt{\frac{TBOX}{TSI}} / W_{eff} \quad C_{th} = CTH0 \cdot W_{eff}$$

$$j_{sbjt} = ISBJT\left(\frac{T}{T_{nom}}\right)^{\frac{XBJT}{NDIODE}} \exp\left[-\frac{qE_g(300)}{NDIODE \cdot kT}\left(1 - \frac{T}{T_{nom}}\right)\right]$$

$$j_{sdif} = ISDIF\left(\frac{T}{T_{nom}}\right)^{\frac{XSdif}{NDIODE}} \exp\left[-\frac{qE_g(300)}{NDIODE \cdot kT}\left(1 - \frac{T}{T_{nom}}\right)\right]$$

$$j_{srec} = ISREC\left(\frac{T}{T_{nom}}\right)^{\frac{XSREC}{2 \cdot NDIODE}} \exp\left[-\frac{qE_g(300)}{2 \cdot NDIODE \cdot kT}\left(1 - \frac{T}{T_{nom}}\right)\right]$$

$$j_{stun} = ISTUN\left(\frac{T}{T_{nom}}\right)^{\frac{XSTUN}{NTUN}}$$

E_g(300) is the energy gap energy at 300K.

2.8 BSIMFD C-V Model

Dimension Dependence

$$\delta W_{eff} = DWC + \frac{WL}{L^{WLN}} + \frac{WW}{W^{WWN}} + \frac{WWL}{L^{WLN}W^{WWN}}$$

$$\delta L_{eff} = DLC + \frac{LL}{L^{LLN}} + \frac{LW}{W^{LWN}} + \frac{LWL}{L^{LLN}W^{LWN}}$$

$$L_{active} = L_{drawn} - 2\delta L_{eff}$$

$$W_{active} = W_{drawn} - 2\delta W_{eff}$$

Charge Conservation

$$Q_{Bf} = Q_{ac0} + Q_{sub0} + Q_{subs}$$

$$Q_{inv} = Q_{inv,s} + Q_{inv,d}$$

$$Q_g = -(Q_{inv} + Q_{Bf} + Q_{e2})$$

$$Q_e = Q_{e1} + Q_{e2}$$

$$Q_b = Q_{Bf} - Q_{e1} + Q_{js} + Q_{jd}$$

$$Q_s = Q_{inv,s} - Q_{js}$$

$$Q_d = Q_{inv,d} - Q_{jd}$$

$$Q_g + Q_e + Q_b + Q_s + Q_d = 0$$

Front Gate Body Charge

Accumulation Charge

$$V_{FBeff} = V_{fb} - 0.5 \left((V_{fb} - V_{gb} - \delta) + \sqrt{(V_{fb} - V_{gb} - \delta)^2 + \delta^2} \right)$$

$$\text{where } V_{gb} = V_{gs} - V_{bseff}$$

$$V_{fb} = V_{th} - \phi_s - K1 \sqrt{\phi_s - V_{bseff}}$$

$$V_{gsteff, cv} = nv_t \ln \left(1 + \exp \left[\frac{V_{gs} - V_{th}}{nv_t} \right] \right)$$

$$Q_{acc} = -W_{active} L_{active} C_{ox} (V_{FBeff} - V_{fb})$$

Gate Induced Depletion Charge

$$Q_{sub0} = -W_{active} L_{active} C_{ox} \frac{K1^2}{2} \left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{FBeff} - V_{gsteffcv} - V_{bseff})}{K1^2}} \right)$$

Drain Induced Depletion Charge

- For **CAPMOD = 2**

$$V_{dsatCV} = \frac{V_{gsteffCV}}{A_{bulkCV}}$$

$$V_{dsCV} = V_{dsatCV} - \frac{1}{2}(V_{dsatCV} - V_{ds} - \delta + \sqrt{(V_{dsatCV} - V_{ds} - \delta)^2 + 4\delta V_{dsatCV}})$$

- For **DDMOD=0**

$$Q_{subs1} = WL_{eff} K1 C_{ox} (A_{bulkCV} - 1)$$

$$\cdot \left[0.5 \cdot V_{dsCV} - \frac{A_{bulkCV} V_{dsCV}^2}{12(V_{gsteffCV} - 0.5 A_{bulkCV} V_{dsCV})} \right]$$

$$Q_{subs2} = 0$$

- For **DDMOD=1/2**

$$V_{csCV} = V_{cs} + 0.5 \left(V_{dsCV} - V_{cs} + \delta - \sqrt{(V_{dsCV} - V_{cs} + \delta)^2 + 4\delta V_{dsCV}} \right)$$

V_{dsCV} is equal to V_{dsatCV} when V_{dseff} is equal to V_{dsatCV} .

$$X_c = \frac{\left[2V_{dsatCV} - V_{csCV}\right]V_{csCV}}{\left[2V_{dsatCV} - V_{dsCV}\right]V_{dsCV}}$$

$$Q_{subs1} = WL_{eff}K1C_{ox}X_c(A_{bulkCV} - 1)$$

$$\cdot \left[0.5 \cdot V_{csCV} - \frac{A_{bulkCV}V_{csCV}^2}{12(V_{gsteffCV} - 0.5(A_{bulkCV}V_{csCV}))} \right]$$

$$Q_{subs2} = WL_{eff}K1C_{ox}(A_{bulkCV} - 1)V_{cs}(1 - X_c)$$

- For **CAPMOD = 3**

$$V_{dsatCV} = V_{gsteff} + K1 \sqrt{\phi_s} + \frac{K1^2}{2} - K1 \sqrt{V_{gsteff} + K1 \sqrt{\phi_s} + \phi_s + \frac{K1^2}{4}}$$

$$V_{dsCV} = V_{dseff} + (V_{dsatCV} - V_{dsat}) \left(\frac{V_{dseff}}{V_{dsat}} \right)^2$$

- For **DDMOD=0**

$$Q_{subs1} = W_{eff}L_{eff}C_{ox}K1 \cdot$$

$$\begin{aligned} & K1 \left[\frac{2}{3} (V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} + (\phi_s - V_{bs})) \left((\phi_s + V_{dsCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right) \right. \\ & - 0.4 \left((\phi_s + V_{dsCV} - V_{bs})^{\frac{5}{2}} - (\phi_s - V_{bs})^{\frac{5}{2}} \right) - K1 V_{dsCV} ((\phi_s - V_{bs}) + 0.5 V_{dsCV}) \Big] \\ & / \left(V_{dsCV} (V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} - 0.5 V_{dsCV}) - \frac{2}{3} K1 \left[(\phi_s + V_{dsCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right] \right) \end{aligned}$$

$$Q_{subs2} = 0$$

- For **DDMOD=1** or **2**

$$V_{csCV} = V_{cs} + 0.5(V_{dsCV} - V_{cs} + \delta - \sqrt{(V_{dsCV} - V_{cs} + \delta)^2 + 4\delta V_{dsCV}})$$

$$X_c = \frac{V_{csCV}(V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} - 0.5 V_{csCV}) - \frac{2}{3}K1 \left[(\phi_s + V_{csCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right]}{V_{dsCV}(V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} - 0.5 V_{dsCV}) - \frac{2}{3}K1 \left[(\phi_s + V_{dsCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right]}$$

$$Q_{subs1} = W_{eff}L_{eff}C_{ox}K1 \cdot$$

$$K1 \left[\frac{2}{3}(V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} + (\phi_s - V_{bs})) \left((\phi_s + V_{csCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right) \right.$$

$$\left. - 0.4 \left((\phi_s + V_{csCV} - V_{bs})^{\frac{5}{2}} - (\phi_s - V_{bs})^{\frac{5}{2}} \right) - K1 V_{csCV} ((\phi_s - V_{bs}) + 0.5 V_{dsCV}) \right]$$

$$\left/ \left(V_{dsCV}(V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} - 0.5 V_{dsCV}) - \frac{2}{3}K1 \left[(\phi_s + V_{dsCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right] \right) \right.$$

$$Q_{subs2} = W_{effCV}L_{effCV}C_{ox}K1 \sqrt{\phi_s - V_{bs0eff}} \cdot (1 - X_c)$$

Back Gate Body Charge

- For **DDMOD=0**

$$Q_{e1} = WLC_{box}(V_{es} - V_{fbb} - V_{bs})$$

$$Q_{e2} = 0$$

- For **DDMOD=1** or **2**

$$Q_{sicv} = C_{ox}WL \frac{K1^2}{2} \left[1 - \sqrt{1 + \frac{4(\phi_s + K1 \sqrt{\phi_s - V_{bs0t}} - V_{bs0t})}{K1^2}} \right]$$

$$Q_{bf0} = C_{ox} \frac{K1^2}{2} \left[1 - \sqrt{1 + \frac{4(\phi_s + K1 \sqrt{\phi_s - V_{bs0mos}} - V_{bs0mos})}{K1^2}} \right]$$

$$Q_{e1} = -Q_{sicv} + Q_{bf0} - WX_c L C_{box} (V_{bs} - V_{bs0})$$

$$Q_{e2} = -WLC_{boxt} \frac{1-X_c}{2} (V_{dsCV} - V_{csCV})$$

Inversion Charge

$$Q_{inv} = -W_{active}L_{active}C_{ox} \cdot \left(\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right) + \frac{A_{bulkCV}^2 V_{cveff}^2}{12 \left(V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right)} \right)$$

50/50 Charge Partition

$$Q_{inv,s} = Q_{inv,d} = 0.5 \cdot Q_{inv}$$

40/60 Charge Partition

$$Q_{inv,s} = -\frac{W_{active}L_{active}C_{ox}}{2 \left(V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right)^2} \cdot \\ \left(V_{gsteffCV}^3 - \frac{4}{3} V_{gsteffCV}^2 (A_{bulkCV} V_{cveff}) + \frac{2}{3} V_{gsteff} (A_{bulkCV} V_{cveff})^2 - \frac{2}{15} (A_{bulkCV} V_{cveff})^3 \right)$$

$$Q_{inv,d} = -\frac{W_{active}L_{active}C_{ox}}{2(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff})^2} \cdot \left(V_{gsteffCV}^3 - \frac{5}{3}V_{gsteffCV}^2(A_{bulkCV}V_{cveff}) + V_{gsteff}(A_{bulkCV}V_{cveff})^2 - \frac{1}{5}(A_{bulkCV}V_{cveff})^3 \right)$$

0/100 Charge Partition

$$Q_{inv,s} = -W_{active}L_{active}C_{ox} \cdot \left(\frac{V_{gsteffCV}}{2} + \frac{A_{bulkCV}V_{cveff}}{4} - \frac{(A_{bulkCV}V_{cveff})^2}{24(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff})} \right)$$

$$Q_{inv,d} = -W_{active}L_{active}C_{ox} \cdot \left(\frac{V_{gsteffCV}}{2} - \frac{3A_{bulkCV}V_{cveff}}{4} - \frac{(A_{bulkCV}V_{cveff})^2}{8(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff})} \right)$$

Overlap Capacitance

Source Overlap Capacitance

$$V_{gs_overlap} = \frac{1}{2} \left\{ (V_{gs} + \delta) + \sqrt{(V_{gs} + \delta)^2 + 4\delta} \right\}$$

$$\frac{Q_{overlap,s}}{W_{active}} = CGS0 \cdot V_{gs}$$

$$+ CGS1 \left\{ V_{gs} - V_{gs_overlap} + \frac{CKAPPA}{2} \left(-1 + \sqrt{1 + \frac{4V_{gs_overlap}}{CKAPPA}} \right) \right\}$$

Drain Overlap Capacitance

$$V_{gd_overlap} = \frac{1}{2} \left\{ (V_{gd} + \delta) + \sqrt{(V_{gd} + \delta)^2 + 4\delta} \right\}$$

$$\begin{aligned} \frac{Q_{overlap,d}}{W_{active}} &= CGD0 \cdot V_{gd} \\ &+ CGD1 \left\{ V_{gd} - V_{gd_overlap} + \frac{CKAPPA}{2} \left(-1 + \sqrt{1 + \frac{4V_{gd_overlap}}{CKAPPA}} \right) \right\} \end{aligned}$$

Gate Overlap Capacitance

$$Q_{overlap,g} = -(Q_{overlap,s} + Q_{overlap,d})$$

Source/Drain Junction Charge

- For $V_{bs} < 0$

$$Q_{jswg} = CJSWG \frac{TSI}{10^{-7}} \frac{PBSWG}{1 - MJSWG} \left[1 - \left(1 - \frac{V_{bs}}{PBSWG} \right)^{1 - MJSWG} \right] + TT \cdot I_{bs1}$$

else

$$Q_{jswg} = CJSWG \frac{TSI}{10^{-7}} V_{bs} \left[1 + \frac{0.5MJSWG \cdot V_{bs}}{PBSWG} \right] + TT \cdot I_{bs1}$$

- For $V_{bd} < 0$

$$Q_{jdwg} = CJSWG \frac{TSI}{10^{-7}} \frac{PBSWG}{1 - MJSWG} \left[1 - \left(1 - \frac{V_{bd}}{PBSWG} \right)^{1 - MJSWG} \right] + TT \cdot I_{bd1}$$

else

$$Q_{jdwg} = CJSWG \frac{TSI}{10^{-7}} V_{bd} \left[1 + \frac{0.5MJSWG \cdot V_{bd}}{PBSWG} \right] + TT \cdot I_{bd1}$$

Extrinsic Charges

Bottom S/D to Substrate Charge

$$C_{sid,e} = \begin{cases} C_{box} & \text{if } V_{s/d,e} < V_{sdfb} \\ C_{box} - \frac{1}{ASD}(C_{box} - C_{min})\left(\frac{V_{s/d,e} - V_{sdfb}}{V_{sdth} - V_{sdfb}}\right)^2 & \text{elseif } V_{s/d,e} < V_{sdfb} + ASD(V_{sdth} - V_{sdfb}) \\ C_{min} + \frac{1}{1-ASD}(C_{box} - C_{min})\left(\frac{V_{s/d,e} - V_{sdth}}{V_{sdth} - V_{sdfb}}\right)^2 & \text{elseif } V_{s/d,e} < V_{sdth} \\ C_{min} & \text{else} \end{cases}$$

Sidewall S/D to Substrate Charge

$$C_{sdesw} = CSDESW \log\left(1 + \frac{TSI}{TBOX}\right)$$

Gate to substrate overlap charge

$$C_{egov} = CEG0(V_{gs} - V_{es})$$

Helper Charge

Only used for **DDMOD=1** and **2**.

$$\begin{aligned} Q_{ex} &= F_{ex} \cdot K1 \cdot C_{ox} \cdot (V_{bs} - V_{bsdio}) \\ Q_b &+= Q_{ex}, \quad Q_e -= Q_{ex} \end{aligned}$$

2.9 BSIMFD Noise Models

With the **NOIMOD** parameter it is possible to use different combinations of thermal and flicker noise models as shown in the table below:

	Spice2		BSIM3	
NOIMOD	Thermal	Flk	Thermal	Flk
1	✓	✓		
2			✓	✓
3	✓			✓
4		✓	✓	

Noise in Access resistance

There are two sources for this noise: one near the drain and the other near the source.

The value for the drain side noise is defined as:

$$\overline{i_{n, th}^2} = 4(k_B T) \cdot Nrd \cdot RSH \cdot \Delta f$$

The value for the source side noise is defined as:

$$\overline{i_{n, th}^2} = 4(k_B T) \cdot Nrs \cdot RSH \cdot \Delta f$$

Thermal Noise

The channel conductance Thermal Noise is defined as follows:

$$\text{For } NOIMOD = 1 \& 3: \overline{i_{n, th}^2} = \frac{8k_B T}{3} \cdot (g_m + g_{ds} + g_{mb}) \cdot \Delta f$$

$$\text{For } NOIMOD = 2 \& 4: \overline{i_{n, th}^2} = \frac{4k_B T \mu_{eff}}{L_{eff}^2} \cdot |Q_{inv}| \cdot \Delta f$$

Flicker Noise Model

The Flicker Noise Model is defined as follows:

$$\text{For } NOIMOD = 1 \& 4: \overline{i_{n, f}^2} = \frac{KF \cdot Ids^{AF}}{Cox \cdot L_{eff}^2 \cdot f^{EF}}$$

For $NOIMOD = 2 \& 3$:

when $vgs \geq Vth + 0.1$:

$$S_{si} = \frac{q^2 \cdot V_t \cdot \mu_{eff} \cdot Ids}{1 \times 10^8 \cdot Cox \cdot L_{eff}^2 \cdot f^{EF}} \cdot \left[NOIA \cdot \log\left(\frac{N_0 + NSTAR}{N_l + NSTAR}\right) + NOIB \cdot (N_0 - N_l) + NOIC \cdot \frac{N_0^2 - N_l^2}{2} \right] + \frac{V_t \cdot Ids^2 \cdot \Delta L_{clm}}{W_{eff} \cdot L_{eff}^2 \cdot f^{EF}} \cdot \frac{NOIA + NOIB \cdot N_l + NOIC \cdot N_l^2}{(N_l + NSTAR)^2}$$

with:

$$N_0 = \frac{Cox}{q} \cdot (Vgs - Vth) \quad N_l = \frac{Cox}{q} \cdot (Vgs - Vth - \min(vds, Vdsat))$$

$$\text{if } vds > Vdsat \quad \Delta L_{clm} = Litl \cdot \log\left(\frac{vds - Vdsat}{Litl \cdot Esat} + \frac{EM}{Esat}\right) \text{ else } \Delta L_{clm} = 0$$

$$\text{then: } \overline{i_{n,f}^2} = S_{si} \cdot \Delta f$$

when $vgs < Vth + 0.1$:

$$S_{limit} = S_{si}(vgs = Vth + 0.1)$$

$$S_{wi} = \frac{NOIA \cdot V_t \cdot Ids^2}{1 \times 10^8 \cdot W_{eff} \cdot L_{eff} \cdot f^{EF} \cdot (NSTAR)^2}$$

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{limit}}{S_{wi} + S_{limit}} \cdot \Delta f$$

If $FLKFLAG$ is set to 1, Swi is always used in conjunction with Ssi even if $Vgs > Vth + 0.1$; i.e. if ($FLKFLAG=1$).

when $vgs \geq Vth + 0.1$:

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{si}}{S_{wi} + S_{si}} \cdot \Delta f$$

when $vgs < Vth + 0.1$:

$$S_{limit} = S_{si}(vgs = Vth + 0.1)$$

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{limit}}{S_{wi} + S_{limit}} \cdot \Delta f$$

Noise Printing

The above mentioned noise values could be printed or plotted for each used device as model states via the print/plot command with the following state notation:

Quantity	Description
RDNOISE	Noise in the drain access resistance
RSNOISE	Noise in the source access resistance
SHOTNOISE	Shot noise
THERMNOISE	Thermal noise
FLKNOISE	Flicker noise
NOISE	Total noise

2.10 BSIMFD v2.1 Parameter List

Berkeley SPICE BSIM3SOI FD v2.1 Parameters

Nr.	Name	Description	Default	Units	Binned?
1	LEVEL	Level 56 for BSIM3SOI	-	-	
2	SOIMOD	SOIMOD should be 3 to select BSIM3SOI FD	2	-	
Model Control Parameters					
3	SHMOD	Flag for self-heating 0 - no self-heating, 1 - self-heating	0		
4	MOBMOD	Mobility model selector	1		
5	CAPMOD^a	Flag for the short channel capacitance model	2		
6	NOIMOD	Flag for Noise model	1		
Process Parameters					
7	TSI	Silicon film thickness	10^{-7}	m	

Berkeley SPICE BSIM3SOI FD v2.1 Parameters

Nr.	Name	Description	Default	Units	Binned?
8	TBOX	Buried oxide thickness	3×10^{-7}	m	
9	TOX	Gate oxide thickness	1×10^{-8}	m	
10	NCH (NPEAK)	Channel doping concentration	1.7×10^{17}	cm^{-3}	Yes
11	NSUB ^b	Substrate doping concentration	6×10^{16}	cm^{-3}	Yes
12	NGATE	Poly gate doping concentration	0	cm^{-3}	Yes
13	GAMMA1	Body effect coefficient near the surface	c	$\text{V}^{1/2}$	Yes
14	GAMMA2	Body effect coefficient in the bulk	d	$\text{V}^{1/2}$	Yes
15	VBX	Body effect coefficient near the surface	e	V	Yes
DC Parameters					
16	VTH0 ^f	Threshold voltage at $V_{bs}=0$ for long and wide device	0.7		Yes
17	K1	First order body effect coefficient	0.6	$\text{V}^{1/2}$	Yes
18	K2	Second order body effect coefficient	0		Yes
19	K3	Narrow width coefficient	0		Yes
20	K3B	Body effect coefficient of K3	0	V^{-1}	Yes
21	VBSA	Transition body voltage offset	0	V	Yes
22	DELP	Constant for limiting $V_{bs,eff}$ to ϕ_s	0.02	V	Yes
23	KB1	Coefficient of $V_{bs,0}$ dependency on V_{es}	1		Yes
24	KB3	Coefficient of $V_{bs,0}$ dependency on V_{gs} at subthreshold region	1		Yes
25	DVBDO (DVBDO)	First coefficient of $V_{bs,0}$ dependency on L_{eff}	0	V	Yes
26	DVBD1	Second coefficient of $V_{bs,0}$ dependency on L_{eff}	0	V	Yes
27	W0	Narrow width parameter	0	m	Yes
28	NLX	Lateral non-uniform doping parameter	1.74×10^{-7}	m	Yes
29	DVT0	First coefficient of short-channel effect on V_{th}	2.2		Yes
30	DVT1	Second coefficient of short-channel effect on V_{th}	0.53		Yes
31	DVT2	Body-bias coefficient of short-channel effect on V_{th}	-0.032	V^{-1}	Yes
32	DVT0W	First coefficient of narrow width effect on V_{th} for small channel length	0		Yes
33	DVT1W	Second coefficient of narrow width effect on V_{th} for small channel length	5.3×10^6		Yes
34	DVT2W	Body-bias coefficient of narrow width effect on V_{th} for small channel length	-0.032	V^{-1}	Yes

Berkeley SPICE BSIM3SOI FD v2.1 Parameters

Nr.	Name	Description	Default	Units	Binned?
35	U0	Mobility at Temp = TNOM NMOSFET PMOSFET	670 250	$\text{cm}^2(\text{Vs})^{-1}$	Yes
36	UA	First-order mobility degradation coefficient	2.25×10^{-9}	mV^{-1}	Yes
37	UB	Second-order mobility degradation coefficient	5.9×10^{-19}	$(\text{mV}^{-1})^2$	Yes
38	UC	Body-effect of mobility degradation coefficient	-0.0465	V^{-1}	Yes
39	VSAT	Saturation velocity at Temp =TNOM	8×10^4	ms^{-1}	Yes
40	A0	Bulk charge effect coefficient for channel length	1.0		Yes
41	AGS	Gate bias coefficient of A_{bulk}	0	V^{-1}	Yes
42	B0	Bulk charge effect coefficient for channel width	0	m	Yes
43	B1	Bulk charge effect width offset	0	m	Yes
44	KETA	Body-bias coefficient of bulk charge effect	-0.6	V^{-1}	Yes
45	ABP	Coefficient of A_{beff} dependency on V_{gst}	1.0		Yes
46	MXC	Fitting parameter for A_{beff} calculation	-0.9		Yes
47	ADICE0	DICE bulk charge factor	1		Yes
48	A1	First non-saturation effect parameter	0	V^{-1}	Yes
49	A2	Second non-saturation effect parameter	1.0	0	Yes
50	RDSW	Parasitic resistance with respect to unit width	100	$\Omega \mu\text{m}^{\text{WR}}$	Yes
51	PRWB	Body effect coefficient of RDSW	0	V^{-1}	Yes
52	PRWG	Gate bias effect coefficient of RDSW	0	$\text{V}^{-1/2}$	Yes
53	WR	Width offset from W_{eff} for Rds calculation	1		Yes
54	WINT	Width offset fitting parameter from I-V without bias	0	m	
55	LINT	Length offset fitting parameter from I-V without bias	0	m	
56	DWG	Coefficient of W_{eff} 's gate dependence	0	mV^{-1}	Yes
57	DWB	Coefficient of W_{eff} 's substrate body bias dependence	0	$\text{mV}^{-1/2}$	Yes
58	VOFF	Offset voltage in the subthreshold region for large W and L	-0.08	V	Yes
59	NFACTOR	Subthreshold swing factor	1		Yes
60	ETA0	DIBL coefficient in subthreshold region	0.08		Yes
61	ETAB	Body-bias coefficient for the subthreshold DIBL effect	-0.07	V^{-1}	Yes
62	DSUB	DIBL coefficient exponent	0.56		Yes
63	CIT	Interface trap capacitance	0.0	Fm^{-2}	Yes
64	CDSC	Drain/Source to channel coupling capacitance	2.4×10^{-4}	Fm^{-2}	Yes

Berkeley SPICE BSIM3SOI FD v2.1 Parameters

Nr.	Name	Description	Default	Units	Binned?
65	CDSCB	Body-bias sensitivity of CDSC	0	Fm ⁻²	Yes
66	CDSCD	Drain-bias sensitivity of CDSC	0	Fm ⁻²	Yes
67	PCLM	Channel length modulation parameter	1.3		Yes
68	PDIBL1	First output resistance DIBL effect correction parameter	0.39		Yes
69	PDIBL2	Second output resistance DIBL effect correction parameter	0.086		Yes
70	PDIBLB	Body-biad coefficient of DIBL	0.0	1/V	Yes
71	DROUT	L dependence coefficient of the DIBL correction parameter in Rout	0.56		Yes
72	PVAG	Gate dependence of Early voltage	0		Yes
73	DELTA	Effective V_{ds} parameter	0.01		Yes
74	AII	1st L_{eff} dependence V_{dsatii} parameter	0	V ⁻¹	Yes
75	BII	2nd L_{eff} dependence V_{dsatii} parameter	0	mV ⁻¹	Yes
76	CII	1st V_{ds} dependence V_{dsatii} parameter	0		Yes
77	DII	2nd dependence V_{dsatii} parameter	-1.0	V	Yes
78	ALPHA0	The first parameter of impact ionization current	0	mV ⁻¹	Yes
79	ALPHA1	The second parameter of impact ionization current	1.0	V ⁻¹	Yes
80	BETA0	The third parameter of impact ionization current	30	V	Yes
81	AGIDL	GIDL constant	0	Ω^{-1}	Yes
82	BGIDL	GIDL exponential coefficient	0	Vm ⁻¹	Yes
83	NGIDL	GIDL V_{ds} enhancement coefficient	1.2	V	Yes
84	NTUN	Reverse tunneling non-ideality factor	10.0		Yes
85	NDIODE	Diode non-ideality factor	1.0		Yes
86	NRECF0	Recombination non-ideality factor at forward bias	2.0		Yes
87	NRECR0	Recombination non-ideality factor at reversed bias	10		Yes
88	ISBJT	BJT injection saturation current	1×10^{-6}	Am ⁻²	Yes
89	ISDIF	Body to source/drain injection saturation current	0	Am ⁻²	Yes
90	ISREC	Recombination in depletion saturation current	1×10^{-5}	Am ⁻²	Yes
91	ISTUN	Reverse tunneling saturation current	0	Am ⁻²	Yes
92	EDL	Electron diffusion length	2×10^{-6}	m	Yes
93	KBJT1	Parasitic bipolar early effect coefficient	0	mV ⁻¹	Yes
94	RBODY	Intrinsic body contact sheet resistance	0	$\Omega \text{ m}^{-2}$	
95	RBSH	Extrinsic body contact sheet resistance	0	$\Omega \text{ m}^{-2}$	

Berkeley SPICE BSIM3SOI FD v2.1 Parameters

Nr.	Name	Description	Default	Units	Binned?
96	RSH	Source drain sheet resistance in ohm per square	0	Ω/square	
AC and Capacitance Parameters					
97	XPART	Charge partitioning rate flag	0		
98	CGSO	Non LDD region source-gate overlap capacitance per channel length	^g calculated	Fm^{-1}	
99	CGDO	Non LDD region drain-gate overlap capacitance per channel length	^h calculated	Fm^{-1}	
100	CGEO	Gate substrate overlap capacitance per unit channel length	0	Fm^{-1}	
101	CJSWG	Source/Drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm T_{si})	1×10^{-10}	Fm^{-2}	
102	PBSWG	Source/Drain (gate side) sidewall junction capacitance built in potential	0.7	V	
103	MJSWG	Source/Drain (gate side) sidewall junction capacitance grading coefficient	0.5	V	
104	TT	Diffusion capacitance transit time coefficient	1ps	s	
105	VSDFB	Source/drain bottom diffusion capacitance flat-band voltage	ⁱ calculated	V	Yes
106	VSDTH	Source/drain bottom diffusion capacitance threshold voltage	^j calculated	V	Yes
107	CSDMIN	Source/drain bottom diffusion minimum capacitance	^k calculated	Fm^2	
108	ASD	Source/drain bottom diffusion smoothing parameter	0.3		
109	CSDESW	Source/drain sidewall fringing capacitance per unit length	0	Fm^{-1}	
110	CGS1	Light doped source-gate region overlap capacitance	0	Fm^{-1}	
111	CGD1	Light doped drain-gate region overlap capacitance	0	Fm^{-1}	
112	CKAPPA	Coefficient for lightly doped region overlap capacitance fringing field capacitance	0.6	Fm^{-1}	
113	CF	Gate to source/drain fringing field capacitance	^l calculated	Fm^{-1}	
114	CLC	Constant term for the short channel model	0.1×10^{-7}	m	
115	CLE	Exponential term for the short channel model	0		
116	DLC	Length offset fitting parameter from C-V	LINT	m	
117	DWC	Width offset fitting parameter from C-V	WINT	m	
Temperature Parameters					
118	TNOM	Temperature at which parameters are expected	27	°C	
119	UTE	Mobility temperature exponent	-1.5		

Berkeley SPICE BSIM3SOI FD v2.1 Parameters

Nr.	Name	Description	Default	Units	Binned?
120	KT1	Temperature coefficient for threshold voltage	-0.11	V	
121	KT11	Channel length dependence of the temperature coefficient for threshold voltage	0	Vm	
122	KT2	Body-bias coefficient of the Vth temperature effect	0.022		
123	UA1	Temperature coefficient for UA	4.31×10^{-9}	mV^{-1}	
124	UB1	Temperature coefficient for UB	-7.61×10^{-18}	$(\text{mV}^{-1})^2$	
125	UC1	Temperature coefficient for UC	-0.056 ^m	V^{-1}	
126	AT	Temperature coefficient for saturation velocity	3.3×10^4	ms^{-1}	
127	CTH0	Normalized thermal capacity	0	$\text{m}^\circ\text{C(Ws)}^{-1}$	
128	PRT	Temperature coefficient for RDSW	0	$\Omega \mu\text{m}$	
129	RTH0	Normalized thermal resistance	0	$\text{m}^\circ\text{CW}^{-1}$	
130	XBJT	Power dependence of j_{bjt} on temperature	2		
131	XDIF	Power dependence of j_{dif} on temperature	2		
132	XREC	Power dependence of j_{rec} on temperature	20		
133	XTUN	Power dependence of j_{tun} on temperature	0		

- a. **CAPMOD** 0 and 1 do not have the dynamic depletion calculation. Therefore DDMOD does not work with these **CAPMOD**.
- b. BSIM3SOI refers substrate to the silicon below buried oxide, not the well region in BSIM3. It is used to calculate backgate flatband voltage (**V_{fb}**) and parameters related to source/drain diffusion bottom capacitance (**VSDTH**, **VSDFB**, **CSDMIN**). Positive **NSUB** means the same type of doping as the body and negative **NSUB** means opposite type of doping.
- c. If **GAMMA1** is not specified, it is calculated using **NCH** and **Cox**.
- d. If **GAMMA2** is not specified, it is calculated using **NSUB** and **Cox**.
- e. If **VBX** is not specified, it is calculated using **PHI**, **NCH** and **XT**.
- f. For FD device, **VTH0** is not equal to the measured long and wide device threshold voltage because **V_{bs0}** is higher than zero.
- g. If **CGSO** is not given then it is calculated using:
if (**DLC** is given and is greater than 0) then,
CGSO = p1 = (DLC × cox) - cgs1
if (the previously calculated **CGSO < 0**), then
CGSO = 0
else **CGSO = 0.6 × TSI × cox**
- h. **CGDO** is calculated in a similar way to **CGSO**
- i. If (**NSUB** is positive)

$$V_{sdfb} = -\frac{kT}{q} \log \left(\frac{10^{20} \cdot NSUB}{n_i \cdot n_i} \right) - 0.3$$

$$\text{else } V_{sdfb} = -\frac{kT}{q} \log \left(\frac{10^{20}}{NSUB} \right) + 0.3$$

j. If ($NSUB$ is positive)

$$\phi_{sd} = 2 \frac{kT}{q} \log\left(\frac{NSUB}{n_i}\right) \quad \gamma_{sd} = \frac{5.753 \times 10^{-12} \sqrt{NSUB}}{C_{box}}$$

$$V_{sdth} = VSDFB + \phi_{sd} + \gamma_{sd} \sqrt{\phi_{sd}}$$

$$\text{else } \phi_{sd} = 2 \frac{kT}{q} \log\left(-\frac{NSUB}{n_i}\right) \quad \gamma_{sd} = \frac{5.753 \times 10^{-12} \sqrt{-NSUB}}{C_{box}}$$

$$V_{sdth} = VSDFB - \phi_{sd} - \gamma_{sd} \sqrt{\phi_{sd}}$$

$$\text{k. } X_{sddep} = \sqrt{\frac{2\varepsilon_{si}\phi_{sd}}{q|NSUB \cdot 10^6|}} \quad C_{sddep} = \frac{\varepsilon_{si}}{X_{sddep}} \quad C_{sdmin} = \frac{C_{sddep}C_{box}}{C_{sddep} + C_{box}}$$

$$\text{l. If } CF \text{ is not given then it is calculated using } CF = \frac{2\varepsilon_{ox}}{\pi} \ln\left(1 + \frac{4 \times 10^{-7}}{TOX}\right)$$

m. For $MOBMOD=1$ and 2 , the unit is mV^{-2} . Default is -5.6×10^{-11} .

For $MOBMOD=3$, the unit is V^{-1} . Default is -0.056 .

2.11 BSIMDDv2.1

2.12 BSIMDD I-V Model

V_{bs0} —Body potential at full depletion and strong inversion conditions

(assuming no substrate depletion)

$$T_{sieff} = \sqrt{TSI^2 - 2 \frac{\varepsilon_{si} VBSA}{q N_a}} \quad C_{sieff} = \frac{\varepsilon_{si}}{T_{sieff}} \quad Q_{sieff} = q N_a T_{sieff}$$

$$V_{bs0t} = \phi_s - 0.5 \cdot \frac{Q_{si}}{C_{si}} + VBSA +$$

$$DVBD0 \cdot \left[\exp\left(-DVBD1 \frac{L_{eff}}{2litl}\right) + 2 \exp\left(-DVBD1 \frac{L_{eff}}{litl}\right) \right] \cdot (V_{bi} - \phi_s)$$

$$V_{bs0} = V_{bs0t} - KB1 \frac{V_{bs0t} - V_{es} + V_{fbb}}{1 + \frac{C_{sieff}}{C_{box}}}$$

V_{thfd}—Threshold voltage at fully depleted condition (V_{bs} = V_{bs0})

$$V_{thfd} = V_{th}(V_{bs} = V_{bs0})$$

V_{bs0eff}/V_{bs0teff}—Effective V_{bs0}/V_{bs0t} for all V_{gs}

$$T_0 = 0.5 \left[(V_{thfd} - V_{gs_eff}) - \delta_1 + \sqrt{\left[(V_{thfd} - V_{gs_eff}) - \delta_1 \right]^2 + \delta_1^2} \right]$$

$$V_{bs0teff} = V_{bs0t} - T_0$$

$$V_{bs0eff} = V_{bs0} - n_{Fb} \cdot T_0$$

$$n_{Fb} = \frac{1}{1 + K3B \frac{C_{box}}{C_{ox}} \sqrt{1 + \frac{4}{K1^2} (\phi_s + K1 \sqrt{\phi_s - V_{bs0mos}} - V_{bs0mos})}}$$

where V_{bs0mos} is the effective V_{bs} when $V_{bs} = V_{bs0}$.

It basically makes V_{bs0eff} & $V_{bs0teff}$ a function of V_{gs} as the following if $V_{gs} < V_{thfd}$.

$$V_{bs0eff} = V_{bs0} + n_{Fb} \cdot (V_{gs} - V_{thfd})$$

$$V_{bs0teff} = V_{bs0t} + (V_{gs} - V_{thfd})$$

V_{bseff}—Equivalent V_{bs} bias for MOS IV calculation

$$T_1 = 0.5 \left[(V_{bs0teff} - V_{bs}) - \delta_2 + \sqrt{\left[(V_{bs0teff} - V_{bs}) - \delta_2 \right]^2 + \delta_2^2} \right]$$

$$V_{bsmos} = V_{bs} - \frac{C_{sieff} T_1^2}{2 \cdot Q_{sieff}}$$

It basically makes V_{bsmos} a function of $V_{bs0teff}$ as the following if $V_{bs} < V_{bs0teff}$

$$V_{bsmos} = V_{bs} - \frac{C_{sieff}(V_{bs0teff} - V_{bs})^2}{2 \cdot Q_{sieff}}$$

otherwise

$$V_{bsmos} = V_{bs}$$



V_{bs} is properly bounded to V_{bs0eff} because of the diode implementation.

Note

$V_{bseff} = V_{bsmos}$ is limited to $\phi_s - DELP$ by the following conversion:

$$V_{bseff} = (\phi_s - DELP) - 0.5 \left[(\phi_s - DELP - V_{bsmos}) - \delta_1 + \sqrt{\left[(\phi_s - DELP - V_{bsmos}) - \delta_1 \right]^2 + 4\delta_1(\phi_s - DELP)} \right]$$

Threshold Voltage

$$\begin{aligned} V_{th} = & VTHO + K1(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}) - K2V_{bseff} \\ & + K1 \left(\sqrt{1 + \frac{NLX}{L_{eff}} - 1} \right) \sqrt{\Phi_s} + (K3 + K3B \cdot V_{bseff}) \frac{TOX}{W_{eff} + WO} \Phi_s \\ & - DVT0W \left(\exp \left(-DVT1W \frac{W_{eff}L_{eff}}{2l_{tw}} \right) + 2 \exp \left(-DVT1W \frac{W_{eff}L_{eff}}{l_{tw}} \right) \right) (V_{bi} - \Phi_s) \\ & - DVT0 \left(\left(\exp \left(-DVT1 \frac{L_{eff}}{2l_t} \right) + 2 \exp \left(-DVT1 \frac{L_{eff}}{l_t} \right) \right) (V_{bi} - \Phi_s) \right. \\ & \left. - \left(\exp \left(-DSUB \frac{L_{eff}}{2l_{to}} \right) + 2 \exp \left(-DSUB \frac{L_{eff}}{l_{to}} \right) \right) (ETAO + ETAB \cdot V_{bseff}) V_{ds} \right. \end{aligned}$$

$$\begin{aligned}
 l_t &= \sqrt{\frac{\epsilon_{si} X_{dep}}{C_{ox}}} (1 + DVT2 \cdot V_{bseff}) \\
 l_{tw} &= \sqrt{\frac{\epsilon_{si} X_{dep}}{C_{ox}}} (1 + DVT2 W \cdot V_{bseff}) \quad l_{to} = \sqrt{\frac{\epsilon_{si} X_{dep0}}{C_{ox}}} \\
 X_{dep} &= \sqrt{\frac{2\epsilon_{si}(\Phi_s - V_{bseff})}{qNCH}} \quad X_{dep0} = \sqrt{\frac{2\epsilon_{si}\Phi_s}{qNCH}} \\
 V_{bi} &= v_t \ln \left(\frac{NCH \cdot N_{DS}}{n_i^2} \right) \quad litl = \sqrt{3TSI \cdot TOX}
 \end{aligned}$$

Poly depletion effect

$$V_{poly} + \frac{1}{2} X_{poly} E_{poly} = \frac{qNGATE \cdot X_{poly}^2}{2\epsilon_{si}}$$

$$\epsilon_{ox} E_{ox} = \epsilon_{si} E_{poly} = \sqrt{2q\epsilon_{si}NGATE \cdot V_{poly}}$$

$$V_{gs} - V_{FB} - \phi_s = V_{poly} + V_{ox}$$

$$a(V_{gs} - V_{FB} - \phi_s - V_{poly})^2 - V_{poly} = 0$$

$$a = \frac{\epsilon_{ox}^2}{2q\epsilon_{si}NGATE \cdot TOX^2}$$

$$V_{gs_eff} = V_{FB} + \phi_s + \frac{q\epsilon_{si}NGATE \cdot TOX^2}{\epsilon_{ox}^2} \left(\sqrt{1 + \frac{2\epsilon_{ox}^2(V_{gs} - V_{FB} - \phi_s)}{q\epsilon_{si}NGATE \cdot TOX^2}} - 1 \right)$$

Effective V_{gst} for all region (with Polysilicon Depletion Effect)

$$V_{gsteff} = \frac{2nV_t \ln \left[1 + \exp \left(\frac{V_{gs_eff} - V_{th}}{2nV_t} \right) \right]}{1 + 2nC_{ox} \sqrt{\frac{2\phi_s}{q\varepsilon_{si}NCH}} \cdot \exp \left(-\frac{V_{gs_eff} - V_{th} - 2VOFF}{2nV_t} \right)}$$

$$n = 1 + NFACTOR \cdot \frac{\varepsilon_{si}/X_{dep}}{C_{ox}} + \frac{(CDSC + CDSCD \cdot V_{ds} + CDSCB \cdot V_{bs_{eff}}) \left(\exp \left(-DVT1 \frac{L_{eff}}{2l_t} \right) + 2 \exp \left(-DVT1 \frac{L_{eff}}{l_t} \right) \right)}{C_{ox}} + \frac{CIT}{C_{ox}}$$

Effective Bulk Charge Factor

$$V_{cs} = V_{bs} - V_{bs0eff}$$

$$T_1 = 1 - 0.5 \left[\left(1 - \frac{V_{cs}}{ABP \cdot V_{gsteff}} \right) - \delta_1 + \sqrt{\left[\left(1 - \frac{V_{cs}}{ABP \cdot V_{gsteff}} \right) - \delta_1 \right]^2 + \delta_1^2} \right]$$

$$X_{csat} = MXC \cdot T_1^2 + (1 - MXC)T_1$$

X_{csat} is a parameter describing the dynamic depletion effect for a given V_{gs} . It varies within (0, 1). The parameter MXC is used to adjust the slope of transition.

$$A_{bulk} = 1 + \left(\frac{K_1}{2\sqrt{\phi_s}} \left(\frac{A0L_{eff}}{L_{eff} + 2\sqrt{TSI \cdot X_{dep}}} \left(1 - AGS \cdot V_{gsteff} \left(\frac{L_{eff}}{L_{eff} + 2\sqrt{TSI \cdot X_{dep}}} \right)^2 \right) \right. \right. \\ \left. \left. + \frac{B0}{W_{eff} + B1} \right) \right) \frac{1}{1 + KETA \cdot V_{bs_{eff}}}$$

$$A_{beff} = X_{csat}A_{bulk} + (1 - X_{csat})A_{dice}$$

$$A_{dice} = \frac{ADICE0}{1 + \left(\frac{C_{boxt}}{C_{ox}}\right)}$$

$$C_{boxt} = \frac{C_{si}C_{box}}{C_{si} + C_{box}}$$

Mobility and Saturation Velocity

- For **MOBMOD=1**

$$\mu_{eff} = \frac{\mu_0}{1 + (UA + UC \cdot V_{bseff})\left(\frac{V_{gsteff} + 2V_{th}}{TOX}\right) + UB\left(\frac{V_{gsteff} + 2V_{th}}{TOX}\right)^2}$$

- For **MOBMOD=2**

$$\mu_{eff} = \frac{\mu_0}{1 + (UA + UC \cdot V_{bseff})\left(\frac{V_{gsteff}}{TOX}\right) + UB\left(\frac{V_{gsteff}}{TOX}\right)^2}$$

- For **MOBMOD=3**

$$\mu_{eff} = \frac{\mu_0}{1 + \left[UA\left(\frac{V_{gsteff} + 2V_{th}}{TOX}\right) + UB\left(\frac{V_{gsteff} + 2V_{th}}{TOX}\right)^2\right](1 + UC \cdot V_{bseff})}$$

Drain Saturation Voltage

- For $R_{ds}>0$ or $\lambda \neq 1$

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

$$a = A_{beff}^2 W_{eff} VSAT \cdot C_{ox} R_{DS} + \left(\frac{1}{\lambda} - 1\right) A_{beff}$$

$$\begin{aligned}
 b &= -\left((V_{gsteff} + 2v_t) \left(\frac{2}{\lambda} - 1 \right) + A_{beff} E_{sat} L_{eff} \right. \\
 &\quad \left. + 3A_{beff}(V_{gsteff} + 2v_t) W_{eff} VSAT \cdot C_{ox} R_{DS} \right) \\
 c &= (V_{gsteff} + 2v_t) E_{sat} L_{eff} + 2(V_{gsteff} + 2v_t)^2 W_{eff} VSAT \cdot C_{ox} R_{DS} \\
 \lambda &= A1 V_{gsteff} + A2
 \end{aligned}$$

- For $R_{ds}=0$, $\lambda=1$

$$\begin{aligned}
 V_{dsat} &= \frac{E_{sat} L_{eff} (V_{gsteff} + 2v_t)}{A_{beff} E_{sat} L_{eff} + (V_{gsteff} + 2v_t)} \\
 E_{sat} &= \frac{2VSAT}{\mu_{eff}}
 \end{aligned}$$

V_{dseff}

$$V_{dseff} = V_{dsat} - \frac{1}{2} (V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}})$$

δ is parameter **DELTA**.

Drain current expression

$$I_{ds, MOSFET} = \frac{I_{ds0}(V_{dseff})}{1 + \frac{R_{ds} I_{ds0}(V_{dseff})}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A} \right)$$

$$\beta = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}}$$

$$I_{ds0} = \frac{\beta V_{gsteff} \left(1 - A_{beff} \frac{V_{dseff}}{2[V_{gsteff} + 2v_t]} \right) V_{dseff}}{1 + \frac{V_{dseff}}{E_{sat} L_{eff}}}$$

$$V_A = V_{Asat} + \left(1 + \frac{PVAG \cdot V_{gsteff}}{E_{sat} L_{eff}} \right) \left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}} \right)^{-1}$$

$$V_{ACLM} = \frac{A_{beff} E_{sat} L_{eff} + V_{gsteff}}{PCLM \cdot A_{beff} E_{sat} litl} (V_{ds} - V_{dseff})$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{\theta_{rout}(1 + PDIBLCB \cdot V_{bseff})} \left(1 - \frac{A_{beff} V_{dsat}}{A_{beff} V_{dsat} + 2v_t} \right)$$

$$\theta_{rout} = PDIBLC1 \left[\exp\left(-DROUT \frac{L_{eff}}{2l_{t0}}\right) + 2 \exp\left(-DROUT \frac{L_{eff}}{l_{t0}}\right) \right] + PDIBLC2$$

$$V_{Asat} = \frac{E_{sat} L_{eff} + V_{dsat} + 2R_{DS} VSAT \cdot C_{ox} W_{eff} V_{gsteff} \left[1 - \frac{A_{beff} V_{dsat}}{2(V_{gsteff} + 2v_t)} \right]}{\frac{2}{\lambda} - 1 + R_{DS} VSAT \cdot C_{ox} W_{eff} A_{beff}}$$

$$litl = \sqrt{\frac{\epsilon_{si} TOX \cdot TSI}{\epsilon_{ox}}}$$

Drain/Source Resistance

$$R_{ds} = RDSW \cdot \frac{1 + PRWG \cdot V_{gsteff} + PRWB(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})}{(10^6 W_{eff})^{WR}}$$

Impact Ionization Current

$$I_{ii} = \frac{ALPHA0 + ALPHA1 L_{eff}}{L_{eff}} \cdot I_d \cdot V_{dseffii} \cdot \exp\left(-\frac{BETA0}{V_{dseffii}}\right)$$

$$V_{dsatii} = \frac{E_{sat}L_{eff}V_{gst}}{M_1E_{sat}L_{eff} + M_2V_{gst}}$$

$$M_1 = AII + \frac{BII}{L_{eff}} \quad M_2 = 1 + \left(\frac{CII}{V_{ds} - DII} \right)^2$$

$V_{dseffii}$ is calculated the same way as V_{dseff} with V_{dsat} replaced by V_{dsatii} .

Gate-Induced-Drain-Leakage (GIDL)

- At drain

$$I_{dgidl} = W_{eff} \cdot AGIDL \cdot E_s \cdot \exp\left(-\frac{BGIDL}{E_s}\right)$$

$$E_s = \frac{V_{ds} - V_{gs} - \chi}{3 \cdot TOX}$$

- At source

$$I_{sgidl} = W_{eff} \cdot AGIDL \cdot E_s \cdot \exp\left(-\frac{BGIDL}{E_s}\right)$$

$$E_s = \frac{-V_{gs} - \chi}{3 \cdot TOX}$$

Default of χ is 1.2V.

If E_s is negative, I_{gidl} is set to zero for both drain and source.

Body contact current

$$R_{bp} = RBODY0 \frac{W_{eff}}{L_{eff}} \quad R_{bodyext} = RBSH \cdot N_{rb}$$

- For 4-T device

$$I_{bp} = 0$$

- For 5-T device

$$I_{bp} = \frac{V_{bp}}{\frac{R_{bp}}{\sqrt{V_{bs} - V_{bs0eff}}} + R_{bodyext}}$$

Diode and BJT currents

- For source side:

Bipolar Transport Factor

$$W_b = L_{eff} - KBJT1 \cdot V_{ds}$$

$$\alpha_{bjt} = 1 - 0.5 \left(\frac{W_b}{EDL} \right)^2$$

V_{bs0} for diode current

$$V_{bs0_dio} = 0.5 \left[V_{bs0eff} - \delta_1 + \sqrt{[V_{bs0eff} - \delta_1]^2 + 4\delta_1} \right]$$

BJT emitter current

$$I_{bjt} = W_{eff} \cdot TSI \cdot j_{sbjt} \left(e^{\frac{V_{bs}}{NDIODE \cdot V_t}} - e^{\frac{V_{bs0_dio}}{NDIODE \cdot V_t}} \right) \left(1 - e^{-\frac{V_{ds}}{2NDIODE \cdot V_t}} \right)$$

Body-to-Source diffusion

$$I_{bs1} = W_{eff} \cdot TSI \cdot j_{sdif} \left(e^{\frac{V_{bs}}{NDIODE \cdot V_t}} - e^{\frac{V_{bs0_dio}}{NDIODE \cdot V_t}} \right)$$

Recombination in depletion region

$$I_{bs2} = W_{eff} \cdot TSI \cdot j_{srec} \left(e^{\frac{V_{bs}}{2NDIODE \cdot V_t}} - e^{\frac{V_{bs0_dio}}{2NDIODE \cdot V_t}} \right)$$

Reversed bias tunneling leakage

$$I_{bs4} = W_{eff} \cdot TSI \cdot j_{stun} \left(1 - e^{-\frac{V_{bs}}{NTUN \cdot V_t}} \right)$$

Recombination in neutral body

$$I_{bs3} = (1 - \alpha_{bjt}) I_{bjt}$$

BJT collector current

$$I_c = I_{bjt} - I_{bs3}$$

Total body-source current

$$I_{bs} = I_{bs1} + I_{bs2} + I_{bs3} + I_{bs4}$$

- For drain side

if $V_{bd} > V_{bs0_dio}$

$$I_{bd1} = W_{eff} \cdot TSI \cdot j_{sdif} \left(e^{\frac{V_{bd}}{n \cdot V_t}} - e^{\frac{V_{bs0_dio}}{n \cdot V_t}} \right)$$

$$I_{bd2} = W_{eff} \cdot TSI \cdot j_{srec} \left(e^{\frac{V_{bd}}{2n \cdot V_t}} - e^{\frac{V_{bs0_dio}}{2n \cdot V_t}} \right)$$

else

$$I_{bd1} = W_{eff} \cdot TSI \cdot j_{sdif} \left(e^{\frac{V_{bd} - V_{bs0_dio}}{NDIODE \cdot V_t}} - 1 \right)$$

$$I_{bd2} = W_{eff} \cdot TSI \cdot j_{srec} \left(e^{\frac{V_{bd} - V_{bs0}}{2NDIODE \cdot V_t}} - 1 \right)$$

$$I_{bd4} = W_{eff} \cdot TSI \cdot j_{stun} \left(1 - e^{-\frac{V_{bd}}{NTUN \cdot V_t}} \right)$$

Total body-drain current

$$I_{bd} = I_{bd1} + I_{bd2} + I_{bd4}$$

Total body current

$$I_{ii} + I_{dgidl} + I_{sgidl} - I_{bs} - I_{bd} - I_{bp} = 0$$

Temperature effects

$$V_{th(T)} = V_{th(T_{nom})} + \left(KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{bseff} \right) \left(\frac{T}{T_{nom}} - 1 \right)$$

$$UO_{(T)} = UO_{(T_{nom})} \left(\frac{T}{T_{nom}} \right)^{UTE}$$

$$VSAT_{(T)} = VSAT_{(T_{nom})} - AT \left(\frac{T}{T_{nom}} - 1 \right)$$

$$RDSW_{(T)} = RDSW_{(T_{nom})} + PRT \left(\frac{T}{T_{nom}} - 1 \right)$$

$$UA_{(T)} = UA_{(T_{nom})} + UA1\left(\frac{T}{T_{nom}} - 1\right)$$

$$UB_{(T)} = UB_{(T_{nom})} + UB1\left(\frac{T}{T_{nom}} - 1\right)$$

$$UC_{(T)} = UC_{(T_{nom})} + UC1\left(\frac{T}{T_{nom}} - 1\right)$$

$$R_{th} = RTH0 \cdot \sqrt{\frac{TBOX}{TSI}} \quad C_{th} = CTH0 \cdot W_{eff}$$

$$j_{sbjt} = ISBJT\left(\frac{T}{T_{nom}}\right)^{\frac{XBJT}{NDIODE}} \exp\left[-\frac{qE_g(300)}{NDIODE \cdot kT}\left(1 - \frac{T}{T_{nom}}\right)\right]$$

$$j_{sdif} = ISDIF\left(\frac{T}{T_{nom}}\right)^{\frac{XSdif}{NDIODE}} \exp\left[-\frac{qE_g(300)}{NDIODE \cdot kT}\left(1 - \frac{T}{T_{nom}}\right)\right]$$

$$j_{srec} = ISREC\left(\frac{T}{T_{nom}}\right)^{\frac{XSREC}{2 \cdot NDIODE}} \exp\left[-\frac{qE_g(300)}{2 \cdot NDIODE \cdot kT}\left(1 - \frac{T}{T_{nom}}\right)\right]$$

$$j_{stun} = ISTUN\left(\frac{T}{T_{nom}}\right)^{\frac{XSTUN}{NTUN}}$$

$E_g(300)$ is the energy gap energy at 300K.

2.13 BSIMDD C-V Model

Dimension Dependence

$$\delta W_{eff} = DWC + \frac{WL}{L^{WLN}} + \frac{WW}{W^{WWN}} + \frac{WWL}{L^{WLN}W^{WWN}}$$

$$\delta L_{eff} = DLC + \frac{LL}{L^{LLN}} + \frac{LW}{W^{LWN}} + \frac{LWL}{L^{LLN}W^{LWN}}$$

$$L_{active} = L_{drawn} - 2\delta L_{eff}$$

$$W_{active} = W_{drawn} - 2\delta W_{eff}$$

Charge Conservation

$$Q_{Bf} = Q_{ac0} + Q_{sub0} + Q_{subs}$$

$$Q_{inv} = Q_{inv,s} + Q_{inv,d}$$

$$Q_g = -(Q_{inv} + Q_{Bf} + Q_{e2})$$

$$Q_e = Q_{e1} + Q_{e2}$$

$$Q_b = Q_{Bf} - Q_{e1} + Q_{js} + Q_{jd}$$

$$Q_s = Q_{inv,s} - Q_{js}$$

$$Q_d = Q_{inv,d} - Q_{jd}$$

$$Q_g + Q_e + Q_b + Q_s + Q_d = 0$$

Front Gate Body Charge

Accumulation Charge

$$V_{FBeff} = V_{fb} - 0.5 \left((V_{fb} - V_{gb} - \delta) + \sqrt{(V_{fb} - V_{gb} - \delta)^2 + \delta^2} \right)$$

$$\text{where } V_{gb} = V_{gs} - V_{bseff}$$

$$V_{fb} = V_{th} - \phi_s - K1 \sqrt{\phi_s - V_{bseff}}$$

$$V_{gsteff, cv} = nv_t \ln \left(1 + \exp \left[\frac{V_{gs} - V_{th}}{nv_t} \right] \right)$$

$$Q_{acc} = -W_{active} L_{active} C_{ox} (V_{FBeff} - V_{fb})$$

Gate Induced Depletion Charge

$$Q_{sub0} = -W_{active} L_{active} C_{ox} \frac{K1^2}{2} \left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{FBeff} - V_{gsteffcv} - V_{bseff})}{K1^2}} \right)$$

Drain Induced Depletion Charge

- For **CAPMOD = 2**

$$V_{dsatCV} = \frac{V_{gsteffCV}}{A_{bulkCV}}$$

$$V_{dsCV} = V_{dsatCV} - 0.5(V_{dsatCV} - V_{ds} - \delta + \sqrt{(V_{dsatCV} - V_{ds} - \delta)^2 + 4\delta V_{dsatCV}})$$

$$V_{csCV} = V_{cs} + 0.5 \left(V_{dsCV} - V_{cs} + \delta - \sqrt{(V_{dsCV} - V_{cs} + \delta)^2 + 4\delta V_{dsCV}} \right)$$

V_{dsCV} is equal to V_{dsatCV} when V_{dseff} is equal to V_{dsatCV} .

$$X_c = \frac{\left[2V_{dsatCV} - V_{csCV} \right] V_{csCV}}{\left[2V_{dsatCV} - V_{dsCV} \right] V_{dsCV}}$$

- For **CAPMOD = 3**

$$V_{dsatCV} = V_{gsteff} + K1 \sqrt{\phi_s + \frac{K1^2}{2}} - K1 \sqrt{V_{gsteff} + K1 \sqrt{\phi_s + \phi_s + \frac{K1^2}{4}}}$$

$$V_{dsCV} = V_{dseff} + (V_{dsatCV} - V_{dsat}) \left(\frac{V_{dseff}}{V_{dsat}} \right)^2$$

$$V_{csCV} = V_{cs} + 0.5(V_{dsCV} - V_{cs} + \delta - \sqrt{(V_{dsCV} - V_{cs} + \delta)^2 + 4\delta V_{dsCV}})$$

$$X_c = \frac{V_{csCV}(V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} - 0.5 V_{csCV}) - \frac{2}{3} K1 \left[(\phi_s + V_{csCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right]}{V_{dsCV}(V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} - 0.5 V_{dsCV}) - \frac{2}{3} K1 \left[(\phi_s + V_{dsCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right]}$$

$$Q_{subs1} = W_{eff} L_{eff} C_{ox} K1 \cdot$$

$$\begin{aligned} & K1 \left[\frac{2}{3} (V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} + (\phi_s - V_{bs})) \left((\phi_s + V_{csCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right) \right. \\ & - 0.4 \left((\phi_s + V_{csCV} - V_{bs})^{\frac{5}{2}} - (\phi_s - V_{bs})^{\frac{5}{2}} \right) - K1 V_{csCV} ((\phi_s - V_{bs}) + 0.5 V_{dsCV}) \Big] \\ & / \left(V_{dsCV}(V_{gsteff} + K1 \sqrt{\phi_s - V_{bs}} - 0.5 V_{dsCV}) - \frac{2}{3} K1 \left[(\phi_s + V_{dsCV} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}} \right] \right) \end{aligned}$$

$$Q_{subs2} = W_{effCV} L_{effCV} C_{ox} K1 \sqrt{\phi_s - V_{bs0eff}} \cdot (1 - X_c)$$

Back Gate Body Charge

$$Q_{sicv} = C_{ox} WL \frac{K1^2}{2} \left[1 - \sqrt{1 + \frac{4(\phi_s + K1 \sqrt{\phi_s - V_{bs0t}} - V_{bs0t})}{K1^2}} \right]$$

$$Q_{bf0} = C_{ox} \frac{K1^2}{2} \left[1 - \sqrt{1 + \frac{4(\phi_s + K1 \sqrt{\phi_s - V_{bs0mos}} - V_{bs0mos})}{K1^2}} \right]$$

$$Q_{e1} = -Q_{sicv} + Q_{bf0} - WX_c LC_{box}(V_{bs} - V_{bs0})$$

$$Q_{e2} = -WLC_{boxt} \frac{1-X_c}{2}(V_{dsCV} - V_{csCV})$$

Inversion Charge

$$Q_{inv} = -W_{active} L_{active} C_{ox} \cdot \left(\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right) + \frac{A_{bulkCV}^2 V_{cveff}^2}{12 \left(V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right)} \right)$$

50/50 Charge Partition

$$Q_{inv,s} = Q_{inv,d} = 0.5 \cdot Q_{inv}$$

40/60 Charge Partition

$$Q_{inv,s} = -\frac{W_{active} L_{active} C_{ox}}{2 \left(V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right)^2} \cdot \left(V_{gsteffCV}^3 - \frac{4}{3} V_{gsteffCV}^2 (A_{bulkCV} V_{cveff}) + \frac{2}{3} V_{gsteff} (A_{bulkCV} V_{cveff})^2 - \frac{2}{15} (A_{bulkCV} V_{cveff})^3 \right)$$

$$Q_{inv,d} = -\frac{W_{active} L_{active} C_{ox}}{2 \left(V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right)^2} \cdot \left(V_{gsteffCV}^3 - \frac{5}{3} V_{gsteffCV}^2 (A_{bulkCV} V_{cveff}) + V_{gsteff} (A_{bulkCV} V_{cveff})^2 - \frac{1}{5} (A_{bulkCV} V_{cveff})^3 \right)$$

0/100 Charge Partition

$$Q_{inv,s} = -W_{active} L_{active} C_{ox} \cdot \left(\frac{V_{gsteffCV}}{2} + \frac{A_{bulkCV} V_{cveff}}{4} - \frac{(A_{bulkCV} V_{cveff})^2}{24 \left(V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right)} \right)$$

$$Q_{inv,d} = -W_{active}L_{active}C_{ox} \cdot \left(\frac{V_{gsteffCV}}{2} - \frac{3A_{bulkCV}V_{cveff}}{4} - \frac{(A_{bulkCV}V_{cveff})^2}{8(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{cveff})} \right)$$

Overlap Capacitance

Source Overlap Capacitance

$$V_{gs_overlap} = \frac{1}{2} \left\{ (V_{gs} + \delta) + \sqrt{(V_{gs} + \delta)^2 + 4\delta} \right\}$$

$$\begin{aligned} \frac{Q_{overlap,s}}{W_{active}} &= CGS0 \cdot V_{gs} \\ &+ CGS1 \left\{ V_{gs} - V_{gs_overlap} + \frac{CKAPPA}{2} \left(-1 + \sqrt{1 + \frac{4V_{gs_overlap}}{CKAPPA}} \right) \right\} \end{aligned}$$

Drain Overlap Capacitance

$$V_{gd_overlap} = \frac{1}{2} \left\{ (V_{gd} + \delta) + \sqrt{(V_{gd} + \delta)^2 + 4\delta} \right\}$$

$$\begin{aligned} \frac{Q_{overlap,d}}{W_{active}} &= CGD0 \cdot V_{gd} \\ &+ CGD1 \left\{ V_{gd} - V_{gd_overlap} + \frac{CKAPPA}{2} \left(-1 + \sqrt{1 + \frac{4V_{gd_overlap}}{CKAPPA}} \right) \right\} \end{aligned}$$

Gate Overlap Capacitance

$$Q_{overlap,g} = -(Q_{overlap,s} + Q_{overlap,d})$$

Source/Drain Junction Charge

- For $V_{bs} < 0$

$$Q_{jswg} = CJSWG \frac{TSI}{10^{-7}} G1 \frac{PBSWG}{1 - MJSWG} \left[1 - \left(1 - \frac{V_{bs}}{PBSWG} \right)^{1 - MJSWG} \right] + TT \cdot I_{bs1}$$

else

$$Q_{jswg} = CJSWG \frac{TSI}{10^{-7}} G1 \cdot V_{bs} \left[1 + \frac{0.5MJSWG \cdot V_{bs}}{PBSWG} \right] + TT \cdot I_{bs1}$$

- For $V_{bd} < 0$

$$Q_{jdwg} = CJSWG \frac{TSI}{10^{-7}} G2 \frac{PBSWG}{1 - MJSWG} \left[1 - \left(1 - \frac{V_{bd}}{PBSWG} \right)^{1 - MJSWG} \right] + TT \cdot I_{bd1}$$

else

$$Q_{jdwg} = CJSWG \frac{TSI}{10^{-7}} G2 \cdot V_{bs} \left[1 + \frac{0.5MJSWG \cdot V_{bd}}{PBSWG} \right] + TT \cdot I_{bd1}$$

Source: $G1 = \sqrt{\phi_s - V_{bs0eff}} - \sqrt{\phi_s - V_{bs}}$

Drain: $G2 = \sqrt{\phi_s - V_{bs0eff}} - \sqrt{\phi_s - V_{cs}}$

Extrinsic Charges

Bottom S/D to Substrate Charge

$$C_{sid,e} = \begin{cases} C_{box} & \text{if } V_{s/d,e} < V_{sdfb} \\ C_{box} - \frac{1}{ASD}(C_{box} - C_{min})\left(\frac{V_{s/d,e} - V_{sdfb}}{V_{sdth} - V_{sdfb}}\right)^2 & \text{elseif } V_{s/d,e} < V_{sdfb} + ASD(V_{sdth} - V_{sdfb}) \\ C_{min} + \frac{1}{1-ASD}(C_{box} - C_{min})\left(\frac{V_{s/d,e} - V_{sdth}}{V_{sdth} - V_{sdfb}}\right)^2 & \text{elseif } V_{s/d,e} < V_{sdth} \\ C_{min} & \text{else} \end{cases}$$

Sidewall S/D to Substrate Charge

$$C_{sdesw} = CSDESW \log\left(1 + \frac{TSI}{TBOX}\right)$$

Gate to substrate overlap charge

$$C_{egov} = CEG0(V_{gs} - V_{es})$$

2.14 BSIMDD Noise Models

With the **NOIMOD** parameter it is possible to use different combinations of thermal and flicker noise models as shown in the table below:

	Spice2		BSIM3	
NOIMOD	Thermal	Flk	Thermal	Flk
1	✓	✓		
2			✓	✓
3	✓			✓
4		✓	✓	

Noise in Access resistance

There are two sources for this noise: one near the drain and the other near the source.

The value for the drain side noise is defined as:

$$\overline{i_{n, th}^2} = 4(k_B T) \cdot Nrd \cdot RSH \cdot \Delta f$$

The value for the source side noise is defined as:

$$\overline{i_{n, th}^2} = 4(k_B T) \cdot Nrs \cdot RSH \cdot \Delta f$$

Shot Noise

Shot Noise is present for all SOI models except for the FD devices, shot noise is defined as follows:

$$\overline{i_{n, th}^2} = 2 \cdot NOIF \cdot Ibs \cdot \Delta f$$

Thermal Noise

The channel conductance Thermal Noise is defined as follows:

$$\text{For } NOIMOD = 1 \& 3: \overline{i_{n, th}^2} = \frac{8k_B T}{3} \cdot (g_m + g_{ds} + g_{mb}) \cdot \Delta f$$

$$\text{For } NOIMOD = 2 \& 4: \overline{i_{n, th}^2} = \frac{4k_B T \mu_{eff}}{L_{eff}^2} \cdot |Q_{inv}| \cdot \Delta f$$

Flicker Noise Model

The Flicker Noise Model is defined as follows:

$$\text{For } NOIMOD = 1 \& 4: \overline{i_{n, f}^2} = \frac{KF \cdot Ids^{AF}}{Cox \cdot L_{eff}^2 \cdot f^{EF}}$$

For $NOIMOD = 2 \& 3$:

when $vgs \geq Vth + 0.1$:

$$S_{si} = \frac{q^2 \cdot V_t \cdot \mu_{eff} \cdot Ids}{1 \times 10^8 \cdot Cox \cdot L_{eff}^2 \cdot f^{EF}} \cdot \left[NOIA \cdot \log\left(\frac{N_0 + NSTAR}{N_l + NSTAR}\right) + NOIB \cdot (N_0 - N_l) + NOIC \cdot \frac{N_0^2 - N_l^2}{2} \right] + \frac{V_t \cdot Ids^2 \cdot \Delta L_{clm}}{W_{eff} \cdot L_{eff}^2 \cdot f^{EF}} \cdot \frac{NOIA + NOIB \cdot N_l + NOIC \cdot N_l^2}{(N_l + NSTAR)^2}$$

with:

$$N_0 = \frac{Cox}{q} \cdot (Vgs - Vth) \quad N_l = \frac{Cox}{q} \cdot (Vgs - Vth - \min(vds, Vdsat))$$

$$\text{if } vds > Vdsat \quad \Delta L_{clm} = Litl \cdot \log\left(\frac{vds - Vdsat}{Litl \cdot Esat} + \frac{EM}{Esat}\right) \text{ else } \Delta L_{clm} = 0$$

$$\text{then: } \overline{i_{n,f}^2} = S_{si} \cdot \Delta f$$

when $vgs < Vth + 0.1$:

$$S_{limit} = S_{si}(vgs = Vth + 0.1)$$

$$S_{wi} = \frac{NOIA \cdot V_t \cdot Ids^2}{1 \times 10^8 \cdot W_{eff} \cdot L_{eff} \cdot f^{EF} \cdot (NSTAR)^2}$$

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{limit}}{S_{wi} + S_{limit}} \cdot \Delta f$$

If $FLKFLAG$ is set to 1, Swi is always used in conjunction with Ssi even if $Vgs > Vth + 0.1$; i.e. if ($FLKFLAG=1$).

when $vgs \geq Vth + 0.1$:

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{si}}{S_{wi} + S_{si}} \cdot \Delta f$$

when $vgs < Vth + 0.1$:

$$S_{limit} = S_{si}(vgs = Vth + 0.1)$$

$$\overline{i_{n,f}^2} = \frac{S_{wi} \cdot S_{limit}}{S_{wi} + S_{limit}} \cdot \Delta f$$

Noise Printing

The above mentioned noise values could be printed or plotted for each used device as model states via the print/plot command with the following state notation:

Quantity	Description
RDNOISE	Noise in the drain access resistance
RSNOISE	Noise in the source access resistance
SHOTNOISE	Shot noise
THERMNOISE	Thermal noise
FLKNOISE	Flicker noise
NOISE	Total noise

2.15 BSIMDDv2.1 Parameter List

Berkeley SPICE BSIM3SOI DD Parameters

Nr.	Name	Description	Default	Units	Binned?
1	LEVEL	Level 56 for BSIM3SOI	-	-	
2	SOIMOD	SOIMOD should be 2 to select BSIM3SOI DD	2	-	
Model Control Parameters					
3	SHMOD	Flag for self-heating 0 - no self-heating, 1 - self-heating	0		
4	MOBMOD	Mobility model selector	1		
5	CAPMOD^a	Flag for the short channel capacitance model	2		
6	NOIMOD	Flag for Noise model	1		
Process Parameters					
7	TSI	Silicon film thickness	10^{-7}	m	

Berkeley SPICE BSIM3SOI DD Parameters

Nr.	Name	Description	Default	Units	Binned?
8	TBOX	Buried oxide thickness	3×10^{-7}	m	
9	TOX	Gate oxide thickness	1×10^{-8}	m	
10	NCH (NPEAK)	Channel doping concentration	1.7×10^{17}	cm^{-3}	Yes
11	NSUB ^b	Substrate doping concentration	6×10^{16}	cm^{-3}	Yes
12	NGATE	Poly gate doping concentration	0	cm^{-3}	Yes
13	GAMMA1	Body effect coefficient near the surface	c	$\text{V}^{1/2}$	Yes
14	GAMMA2	Body effect coefficient in the bulk	d	$\text{V}^{1/2}$	Yes
15	VBX	Body effect coefficient near the surface	e	V	Yes
DC Parameters					
16	VTH0	Threshold voltage at $V_{bs}=0$ for long and wide device	0.7		Yes
17	K1	First order body effect coefficient	0.6	$\text{V}^{1/2}$	Yes
18	K2	Second order body effect coefficient	0		Yes
19	K3	Narrow width coefficient	0		Yes
20	K3B	Body effect coefficient of K3	0	V^{-1}	Yes
21	VBSA	Transition body voltage offset	0	V	Yes
22	DELP	Constant for limiting $V_{bs\text{eff}}$ to ϕ_s	0.02	V	Yes
23	KB1	Coefficient of V_{bs0} dependency on V_{es}	1		Yes
24	KB3	Coefficient of V_{bs0} dependency on V_{gs} at subthreshold region	1		Yes
25	DVBDO (DVBDO)	First coefficient of V_{bs0} dependency on L_{eff}	0	V	Yes
26	DVBD1	Second coefficient of V_{bs0} dependency on L_{eff}	0	V	Yes
27	W0	Narrow width parameter	0	m	Yes
28	NLX	Lateral non-uniform doping parameter	1.74×10^{-7}	m	Yes
29	DVT0	First coefficient of short-channel effect on V_{th}	2.2		Yes
30	DVT1	Second coefficient of short-channel effect on V_{th}	0.53		Yes
31	DVT2	Body-bias coefficient of short-channel effect on V_{th}	-0.032	V^{-1}	Yes
32	DVT0W	First coefficient of narrow width effect on V_{th} for small channel length	0		Yes
33	DVT1W	Second coefficient of narrow width effect on V_{th} for small channel length	5.3×10^6		Yes

Berkeley SPICE BSIM3SOI DD Parameters

Nr.	Name	Description	Default	Units	Binned?
34	DVT2W	Body-bias coefficient of narrow width effect on V_{th} for small channel length	-0.032	V^{-1}	Yes
35	U0	Mobility at $\text{Temp} = \text{TNOM}$ NMOSFET PMOSFET	670 250	$\text{cm}^2(\text{Vs})^{-1}$	Yes
36	UA	First-order mobility degradation coefficient	2.25×10^{-9}	mV^{-1}	Yes
37	UB	Second-order mobility degradation coefficient	5.9×10^{-19}	$(\text{mV}^{-1})^2$	Yes
38	UC	Body-effect of mobility degradation coefficient	-0.0465	V^{-1}	Yes
39	VSAT	Saturation velocity at $\text{Temp}=\text{TNOM}$	8×10^4	ms^{-1}	Yes
40	A0	Bulk charge effect coefficient for channel length	1.0		Yes
41	AGS	Gate bias coefficient of A_{bulk}	0	V^{-1}	Yes
42	B0	Bulk charge effect coefficient for channel width	0	m	Yes
43	B1	Bulk charge effect width offset	0	m	Yes
44	KETA	Body-bias coefficient of bulk charge effect	-0.6	V^{-1}	Yes
45	ABP	Coefficient of A_{beff} dependency on V_{gst}	1.0		Yes
46	MXC	Fitting parameter for A_{beff} calculation	-0.9		Yes
47	ADICE0	DICE bulk charge factor	1		Yes
48	A1	First non-saturation effect parameter	0	V^{-1}	Yes
49	A2	Second non-saturation effect parameter	1.0	0	Yes
50	RDSW	Parasitic resistance with respect to unit width	100	$\Omega \mu\text{m}^{\text{WR}}$	Yes
51	PRWB	Body effect coefficient of RDSW	0	V^{-1}	Yes
52	PRWG	Gate bias effect coefficient of RDSW	0	$V^{-1/2}$	Yes
53	WR	Width offset from W_{eff} for Rds calculation	1		Yes
54	WINT	Width offset fitting parameter from I-V without bias	0	m	
55	LINT	Length offset fitting parameter from I-V without bias	0	m	
56	DWG	Coefficient of W_{eff} 's gate dependence	0	mV^{-1}	Yes
57	DWB	Coefficient of W_{eff} 's substrate body bias dependence	0	$\text{mV}^{-1/2}$	Yes
58	VOFF	Offset voltage in the subthreshold region for large W and L	-0.08	V	Yes
59	NFACTOR	Subthreshold swing factor	1		Yes
60	ETAO	DIBL coefficient in subthreshold region	0.08		Yes

Berkeley SPICE BSIM3SOI DD Parameters

Nr.	Name	Description	Default	Units	Binned?
61	ETAB	Body-bias coefficient for the subthreshold DIBL effect	-0.07	V ⁻¹	Yes
62	DSUB	DIBL coefficient exponent	0.56		Yes
63	CIT	Interface trap capacitance	0	Fm ⁻²	Yes
64	CDSC	Drain/Source to channel coupling capacitance	2.4×10 ⁻⁴	Fm ⁻²	Yes
65	CDSCB	Body-bias sensitivity of CDSC	0	Fm ⁻²	Yes
66	CDSCD	Drain-bias sensitivity of CDSC	0	Fm ⁻²	Yes
67	PCLM	Channel length modulation parameter	1.3		Yes
68	PDIBL1	First output resistance DIBL effect correction parameter	0.39		Yes
69	PDIBL2	Second output resistance DIBL effect correction parameter	0.086		Yes
70	PDIBLB	Body-biad coefficient of DIBL	0.0	1/V	Yes
71	DROUT	L dependence coefficient of the DIBL correction parameter in Rout	0.56		Yes
72	PVAG	Gate dependence of Early voltage	0		Yes
73	DELTA	Effective V_{ds} parameter	0.01		Yes
74	AII	1st L_{eff} dependence V_{dsatii} parameter	0	V ⁻¹	Yes
75	BII	2nd L_{eff} dependence V_{dsatii} parameter	0	mV ⁻¹	Yes
76	CII	1st V_{ds} dependence V_{dsatii} parameter	0		Yes
77	DII	2nd dependence V_{dsatii} parameter	-1.0	V	Yes
78	ALPHA0	The first parameter of impact ionization current	0	mV ⁻¹	Yes
79	ALPHA1	The second parameter of impact ionization current	1.0	V ⁻¹	Yes
80	BETA0	The third parameter of impact ionization current	30	V	Yes
81	AGIDL	GIDL constant	0	Ω ⁻¹	Yes
82	BGIDL	GIDL exponential coefficient	0	Vm ⁻¹	Yes
83	NGIDL	GIDL V_{ds} enhancement coefficient	1.2	V	Yes
84	NTUN	Reverse tunneling non-ideality factor	10.0		Yes
85	NDIODE	Diode non-ideality factor	1.0		Yes
86	NRECF0	Recombination non-ideality factor at forward bias	2.0		Yes
87	NRECR0	Recombination non-ideality factor at reversed bias	10		Yes
88	ISBJT	BJT injection saturation current	1×10 ⁻⁶	Am ⁻²	Yes

Berkeley SPICE BSIM3SOI DD Parameters

Nr.	Name	Description	Default	Units	Binned?
89	ISDIF	Body to source/drain injection saturation current	0	Am^{-2}	Yes
90	ISREC	Recombination in depletion saturation current	1×10^{-5}	Am^{-2}	Yes
91	ISTUN	Reverse tunneling saturation current	0	Am^{-2}	Yes
92	EDL	Electron diffusion length	2×10^{-6}	m	Yes
93	KBJT1	Parasitic bipolar early effect coefficient	0	mV^{-1}	Yes
94	RBODY	Intrinsic body contact sheet resistance	0	$\Omega \text{ m}^{-2}$	
95	RBSH	Extrinsic body contact sheet resistance	0	$\Omega \text{ m}^{-2}$	
96	RSH	Source drain sheet resistance in ohm per square	0	Ω/square	

AC and Capacitance Parameters

97	XPART	Charge partitioning rate flag	0		
98	CGSO	Non LDD region source-gate overlap capacitance per channel length	^f calculated	Fm^{-1}	
99	CGDO	Non LDD region drain-gate overlap capacitance per channel length	^g calculated	Fm^{-1}	
100	CGEO	Gate substrate overlap capacitance per unit channel length	0	Fm^{-1}	
101	CJSWG	Source/Drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm T_{si})	1×10^{-10}	Fm^{-2}	
102	PBSWG	Source/Drain (gate side) sidewall junction capacitance built in potential	0.7	V	
103	MJSWG	Source/Drain (gate side) sidewall junction capacitance grading coefficient	0.5	V	
104	TT	Diffusion capacitance transit time coefficient	1×10^{-12}	s	
105	VSDFB	Source/drain bottom diffusion capacitance flatband voltage	^h calculated	V	Yes
106	VSDTH	Source/drain bottom diffusion capacitance threshold voltage	ⁱ calculated	V	Yes
107	CSDMIN	Source/drain bottom diffusion minimum capacitance	^j calculated	Fm^2	
108	ASD	Source/drain bottom diffusion smoothing parameter	0.3		
109	CSDESW	Source/drain sidewall fringing capacitance per unit length	0	Fm^{-1}	
110	CGS1	Light doped source-gate region overlap capacitance	0	Fm^{-1}	
111	CGD1	Light doped drain-gate region overlap capacitance	0	Fm^{-1}	

Berkeley SPICE BSIM3SOI DD Parameters

Nr.	Name	Description	Default	Units	Binned?
112	CKAPPA	Coefficient for lightly doped region overlap capacitance fringing field capacitance	0.6	Fm ⁻¹	
113	CF	Gate to source/drain fringing field capacitance	$k_{\text{calculated}}$	Fm ⁻¹	
114	CLC	Constant term for the short channel model	0.1×10^{-7}	m	
115	CLE	Exponential term for the short channel model	0		
116	DLC	Length offset fitting parameter from C-V	LINT	m	
117	DWC	Width offset fitting parameter from C-V	WINT	m	
Temperature Parameters					
118	TNOM	Temperature at which parameters are expected	27	°C	
119	UTE	Mobility temperature exponent	-1.5		
120	KT1	Temperature coefficient for threshold voltage	-0.11	V	
121	KT11	Channel length dependence of the temperature coefficient for threshold voltage	0	Vm	
122	KT2	Body-bias coefficient of the Vth temperature effect	0.022		
123	UA1	Temperature coefficient for UA	4.31×10^{-9}	mV ⁻¹	
124	UB1	Temperature coefficient for UB	-7.61×10^{-18}	(mV ⁻¹) ²	
125	UC1	Temperature coefficient for UC	-0.056 ^l	V ⁻¹	
126	AT	Temperature coefficient for saturation velocity	3.3×10^4	ms ⁻¹	
127	CTH0	Normalized thermal capacity	0	m°C(Ws) ⁻¹	
128	PRT	Temperature coefficient for RDSW	0	Ω μm	
129	RTH0	Normalized thermal resistance	0	m°CW ⁻¹	
130	XBJT	Power dependence of j_{bjt} on temperature	2		
131	XDIF	Power dependence of j_{dif} on temperature	2		
132	XREC	Power dependence of j_{rec} on temperature	20		
133	XTUN	Power dependence of j_{tun} on temperature	0		

- a. **CAPMOD** 0 and 1 do not have the dynamic depletion calculation. Therefore DDMOD does not work with these **CAPMOD**.
- b. BSIM3SOI refers substrate to the silicon below buried oxide, not the well region in BSIM3. It is used to calculate backgate flatband voltage (V_{fb}) and parameters related to source/drain diffusion bottom capacitance (**VS-DTH**, **VSDFB**, **CSDMIN**). Positive **NSUB** means the same type of doping as the body and negative **NSUB** means opposite type of doping.
- c. If **GAMMA1** is not specified, it is calculated using **NCH** and **Cox**.
- d. If **GAMMA2** is not specified, it is calculated using **NSUB** and **Cox**.
- e. If **VBX** is not specified, it is calculated using **PHI**, **NCH** and **XT**.

f. If **CGSO** is not given then it is calculated using:

if (**DLC** is given and is greater than 0) then,

$$\text{CGSO} = p1 = (\text{DLC} \times \text{cox}) - \text{cgs1}$$

if (the previously calculated **CGSO** < 0), then

$$\text{CGSO} = 0$$

$$\text{else } \text{CGSO} = 0.6 \times \text{TSI} \times \text{cox}$$

g. **CGDO** is calculated in a similar way to **CGSO**

h. If (**NSUB** is positive)

$$VSDFB = -\frac{kT}{q} \log\left(\frac{10^{20} \cdot \text{NSUB}}{n_i \cdot n_i}\right) - 0.3$$

$$\text{else } VSDFB = -\frac{kT}{q} \log\left(\frac{10^{20}}{\text{NSUB}}\right) + 0.3$$

i. If (**NSUB** is positive)

$$\phi_{sd} = 2 \frac{kT}{q} \log\left(\frac{\text{NSUB}}{n_i}\right) \quad \gamma_{sd} = \frac{5.753 \times 10^{-12} \sqrt{\text{NSUB}}}{C_{box}}$$

$$VSDTH = VSDFB + \phi_{sd} + \gamma_{sd} \sqrt{\phi_{sd}}$$

$$\text{else } \phi_{sd} = 2 \frac{kT}{q} \log\left(-\frac{\text{NSUB}}{n_i}\right) \quad \gamma_{sd} = \frac{5.753 \times 10^{-12} \sqrt{-\text{NSUB}}}{C_{box}}$$

$$VSDTH = VSDFB - \phi_{sd} - \gamma_{sd} \sqrt{\phi_{sd}}$$

$$\text{j. } X_{sddep} = \sqrt{\frac{2 \epsilon_{si} \phi_{sd}}{q |\text{NSUB} \cdot 10^6|}} \quad C_{sddep} = \frac{\epsilon_{si}}{X_{sddep}} \quad CSDMIN = \frac{C_{sddep} C_{box}}{C_{sddep} + C_{box}}$$

$$\text{k. If } CF \text{ is not given then it is calculated using } CF = \frac{2 \epsilon_{ox}}{\pi} \ln\left(1 + \frac{4 \times 10^{-7}}{TOX}\right)$$

l. For **MOBMOD**=1 and 2, the unit is mV⁻². Default is -5.6×10⁻¹¹.

For **MOBMOD**=3, the unit is V⁻¹. Default is -0.056.

3.0 BSIM3SOIv3.x

Using BSIMPD as a foundation, a unified model is implemented for both PD and FD SOI circuit designs based on the concept of body-source built-in potential lowering.

In this version, BSIMSOI is constructed based on the concept of body-source built-in potential lowering, ΔV_{bi} . There are three modes (*soiMod* = 0, 1, 2) in BSIMSOI: BSIMPD (*soiMod* = 0) can be used to model the PD SOI device, where the body potential is independent of ΔV_{bi} ($V_{BS} > \Delta V_{bi}$). Therefore the calculation of ΔV_{bi} is skipped in this mode. On the other hand, the ideal FD model (*soiMod* = 2) is for the FD device with body potential equal to ΔV_{bi} . Hence the calculation of body current/charge, which is essential to the PD model, is skipped. For the unified SOI model (*soiMod* = 1), however, both ΔV_{bi} and body current/charge are calculated to capture the floating-body behavior exhibited in FD devices.



BSIMDD is not available for BSIM3SOIv3.x.

Note

3.1 BSIM3SOIv3.1.1

BSIM3SOIv3.1.1 is the latest BSIM3SOI released by Berkeley. BSIM3SOIv3.1.1 bug fixes are:

- Temperature derivative of the variable $Vgst2Vtm$
- Discontinuity in the length dependence of bipolar current
- Discontinuity in *capMod*=3
- Making *IgMod* an alias for *IgbMod* to keep compatibility
- Change the lower bound of *ACDE* to 0.1

BSIM3SOI v3.1.1 is the default version when **LEVEL=56** is specified. To choose another version, please refer to “[Version Selection](#)” on page 20-1.

3.2 BSIM3SOIv3.1

BSIM3SOIv3.1 enhancements:

- An ideal Full-Depletion (FD) module (*soiMod*=2) has been provided for the strongly FD SOI devices (without the floating-body effect).
- The BSIM RF gate resistance model has been provided for SOI devices operated in the high frequency regime.
- Enhanced binning capability.



See [page 20-108](#) for a list of binned parameters.



Note Using BSIMPD as a foundation, a unified model is implemented for both PD and FD SOI circuit designs based on the concept of body-source built-in potential lowering.

This version also includes a list of bug fixes:

- Reduce *gmin* between gate and drain by order of magnitude 6
- Scale *Aechvb* and *AechvbEdge* by *NSEG*
- Fix the *Igb* bug in the AC matrix stamping
- Fix the source/drain swapping error of the source/drain overlap capacitance
- *AbulkCV* in *Qinv*
- *qgmid* is added for the computation of the associated charge current.

3.3 BSIM3SOIv3.0

BSIM3SOIv3.0 introduces some improvements and fixes to BSIM3SOI PD v2.2.3. It also introduces an FD module (not independent) added on top of the PD module for fitting FD SOI devices. The improvements of BSIM3SOIv3.0 include:

- A new Full-Depletion (FD) module has been included to provide better fitting to FD SOI
- Gate to channel/drain/source currents are included
- The calculation of the derivatives of V_{gsteff} about $DELVT$ has been fixed
- The default value of $CTH0$ has changed from 0 to 1e-5
- The variable $Esatii \times Leff$ has been scaled by 1V

3.4 BSIMSOIv3.x Model Equations

- If `soimod` is set to 0 (default), then the model equations used are identical to the BSIMPDv2.x equations.
- i** The BSIMPDv2.x equations can be found on page [20-7 through to 20-64](#).
- If `soimod` is set to 1, then the following equations (FD module) are added on top of the BSIMPD module.

Body voltages

$$V_{bs0} = \frac{C_{Si}}{C_{Si} + C_{BOX}} \cdot \left(phi - \frac{qN_{ch}}{2\varepsilon_{Si}} \cdot {T_{Si}}^2 + V_{nonideal} + \Delta V_{DIBL} \right) \\ + \eta_e \frac{C_{BOX}}{C_{Si} + C_{BOX}} \cdot (V_{es} - V_{FBb})$$

Where:

$$C_{Si} = \frac{\varepsilon_{Si}}{T_{Si}}, \quad C_{BOX} = \frac{\varepsilon_{OX}}{T_{BOX}}, \quad C_{OX} = \frac{\varepsilon_{OX}}{T_{OX}} \\ \Delta V_{DIBL} = D_{vbd0} \left(\exp\left(-D_{vbd1} \frac{L_{eff}}{2l}\right) + 2 \exp\left(-D_{vbd1} \frac{L_{eff}}{l}\right) \right) \cdot (V_{bi} - 2\Phi_B)$$

$$\eta_e = K_{1b} - K_{2b} \cdot \left(\exp\left(-D_{k2b} \frac{L_{eff}}{2l}\right) + 2 \exp\left(-D_{k2b} \frac{L_{eff}}{l}\right) \right)$$

$$\begin{aligned} phi = & \phi_{ON} - \frac{C_{OX}}{C_{OX} + (C_{Si}^{-1} + C_{BOX}^{-1})^{-1}} \cdot N_{OFF,FD} V_t \cdot \\ & \ln\left(1 + \exp\left(\frac{V_{th,FD} - V_{gs_eff} - V_{OFF,FD}}{N_{OFF,FD} V_t}\right)\right) \end{aligned}$$

$$\phi_{ON} = 2\Phi_B + V_t \ln\left(1 + \frac{V_{gsteff,FD}(V_{gsteff,FD} + 2K1\sqrt{2\Phi_B})}{M_{in,FD} \cdot K1 \cdot V_t^2}\right)$$

$$V_{gsteff,FD} = N_{OFF,FD} V_t \cdot \ln\left(1 + \exp\left(\frac{V_{gs_eff} - V_{th,FD} - V_{OFF,FD}}{N_{OFF,FD} V_t}\right)\right)$$

N_{ch} is the channel doping concentration. V_{FBb} is the backgate flatband voltage. $V_{th,FD}$ is the threshold voltage at $V_{bs} = V_{bs0}(\phi_{ON} = 2\Phi_B)$. V_t is thermal voltage. $K1$ is the body effect coefficient.

The lower bound of V_{bs} (SPICE solution) is set to V_{bs0} . V_{bsmos} is calculated by:

$$V_{bsmos} = V_{bs} - \frac{C_{Si}}{2qN_{ch}T_{Si}} (V_{bs0}(T_{OX} \rightarrow \infty) - V_{bs})^2 \text{ If } V_{bs} \leq V_{bs0}(T_{OX} \rightarrow \infty)$$

Else $V_{bsmos} = V_{bs}$

The subsequent clamping of V_{bsmos} will use the same equation that is used in BSIMPD.

Gate-to-channel current (Igc) and gate-to-S/D current (Igs and Igd)

I_{gc} is determined by ECB (Electron tunneling from Conduction Band) for NMOS devices and HVB (Hole tunneling from Valence Band) for PMOS devices, respectively.

$$I_{gc} = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gs_eff} \cdot V_{aux} \cdot \\ \exp[-B \cdot T_{oxqm}(a_{igc} - b_{igc} \cdot V_{oxdepinv}) \cdot (1 + c_{igc} \cdot V_{oxdepinv})]$$

Where:

$$\text{For NMOS devices: } A = 4.97232e^{-7} \text{ A/V}^2, B = 7.45669e^{11} (\text{g/F-s}^2)^{0.5}$$

$$\text{For PMOS devices: } A = 3.42537e^{-7} \text{ A/V}^2, B = 1.16645e^{12} (\text{g/F-s}^2)^{0.5}$$

$$V_{aux} = n_{igc} \cdot V_m \cdot \log\left(1 + \exp\left(\frac{V_{gs_eff} - V_{th0}}{n_{igc} \cdot V_{tm}}\right)\right)$$

$$T_{oxRatio} = \left(\frac{T_{oxref}}{T_{oxqm}}\right)^{ntox} \cdot \frac{1}{T_{oxqm}^2}$$

I_{gs} represents the gate tunneling current between the gate and the source diffusion region.

I_{gd} represents the gate tunneling current between the gate and the drain diffusion region.

I_{gs} and I_{gd} are determined by ECB for NMOS and by HVB for PMOS, respectively.

$$I_{gs} = W_{eff} Dl_{cig} \cdot A \cdot T_{oxRatioEdge} \cdot V_{gs} \cdot V_{gs} \cdot \\ \exp[-B \cdot T_{oxqm} \cdot P_{oxedge} \cdot (a_{igsd} - b_{igsd} \cdot V_{gs}) \cdot (1 + c_{igsd} \cdot V_{gs})]$$

$$I_{gd} = W_{eff} Dl_{cig} \cdot A \cdot T_{oxRatioEdge} \cdot V_{gd} \cdot V_{gd} \cdot \\ \exp[-B \cdot T_{oxqm} \cdot P_{oxedge} \cdot (a_{igsd} - b_{igsd} \cdot V_{gd}) \cdot (1 + c_{igsd} \cdot V_{gd})]$$

Where:

$$\text{For NMOS devices: } A = 4.97232e^{-7} \text{ A/V}^2, B = 7.45669e^{11} (\text{g/F-s}^2)^{0.5}$$

For PMOS devices: $A = 3.42537e^{-7} \text{ A/V}^2$, $B = 1.16645e^{12} (\text{g/F-s}^2)^{0.5}$

$$T_{oxRatioEdge} = \left(\frac{T_{oxref}}{T_{oxqm} \cdot P_{oxedge}} \right)^{ntox} \cdot \frac{1}{(T_{oxqm} \cdot P_{oxedge})^2}$$

$$V_{gs} = \sqrt{(V_{gs} - V_{fbsd})^2 + 1.0e^{-4}}$$

$$V_{gd} = \sqrt{(V_{gd} - V_{fbsd})^2 + 1.0e^{-4}}$$

Partition of I_{gc}

To take in to consideration the drain bias effects, I_{gc} is split into two components, I_{gcs} and I_{gcd} , given by: $I_{gc} = I_{gcs} + I_{gcd}$.

$$I_{gcs} = I_{gc} \cdot \frac{pi \gcd \cdot V_{ds} + \exp(-pi \gcd \cdot V_{ds}) - 1 + 1.0e^{-4}}{pi \gcd^2 \cdot V_{ds}^2 + 2.0e^{-4}}$$

$$I_{gcd} = I_{gc} \cdot \frac{1 - (pi \gcd \cdot V_{ds} + 1) \cdot \exp(-pi \gcd \cdot V_{ds}) + 1.0e^{-4}}{pi \gcd^2 \cdot V_{ds}^2 + 2.0e^{-4}}$$

3.5 BSIMSOIv3.x Parameter List

The parameters listed below are BSIM3SOIv3.1 specific parameters. They are “in addition” to the v2.x parameter table beginning [page 20-35](#).

Berkeley SPICE BSIM3SOIv3.1 RF Parameters

Nr.	Name	Description	Default	Units	Binned?
1	RGATEMOD	Gate resistance model selector rgateMod = 0 No gate resistance rgateMod = 1 Constant gate resistance rgateMod = 2 Rii model with variable resistance rgateMod = 3 Rii model with two nodes	0	-	
2	XRCRG1	Parameter for distributed channel-resistance effect for intrinsic input resistance	12.0	-	Yes

Nr.	Name	Description	Default	Units	Binned?
3	XRCRG2	Parameter to account for the excess channel diffusion resistance for intrinsic input resistance	1.0	-	Yes
4	NGCON	Number of gate contacts	1	-	
5	XGW	Distance from the gate contact to the channel edge	0.0	m	
6	XGL	Offset of the gate length due to variations in patterning	0.0	m	
7	RSHG ^a	Gate electrode sheet resistance	0.1	ohm/square	

a. Should not be negative.

Berkeley SPICE BSIM3SOIv3.0 Parameters

Nr.	Name	Description	Default	Units	Binned?
1	VBSA	Offset voltage due to non-idealities	0	V	Yes
2	NOFFF	Smoothing parameter in FD module	1	-	
3	VOFFF	Smoothing parameter in FD module	0	V	
4	K1B	First backgate body effect parameter	1	-	
5	K2B	Second backgate body effect parameter for short channel effect	0	-	
6	DK2B	Third backgate body effect parameter for short channel effect	0	-	
7	DVBDO (DVBDO)	First short channel effect parameter in FD module	0	-	Yes
8	DVBD1	Second short channel effect parameter in FD module	0	-	Yes
9	MOINFD	Gate bias dependence coefficient of surface potential in an FD module	1e3	-	

Berkeley SPICE BSIM3SOI PD v3.0 Parameters Gate Tunneling Parameters

Nr.	Name	Description	Default	Units	Note	Binned?
1	IGCMOD	Global model selector for I_{gs} , I_{gd} , I_{gcs} and I_{gcd} current components	0		IGCMOD=1 turns on I_{gs} , I_{gd} , I_{gcs} and I_{gcd}	
2	IGBMOD	Global model selector for I_{gb} current	0		IGBMOD=1 turns on I_{gb}	
3	AIGC	Parameter for I_{gs} , I_{gd} , I_{gcs} and I_{gcd}	NMOS: 0.43 PMOS: 0.31	$(Fs^2/g)^{0.5}$ m^{-1}	-	Yes
4	BIGC	Parameter for I_{gcs} and I_{gcd}	NMOS: 0.054 PMOS: 0.024	$(Fs^2/g)^{0.5}$ $(mV)^{-1}$	-	Yes

Nr.	Name	Description	Default	Units	Note	Binned?
5	CIGC	Parameter for I_{gcs} and I_{gcd}	NMOS: 0.075 PMOS: 0.03	V ⁻¹	-	Yes
6	AIGSD	Parameter for I_{gs} and I_{gd}	NMOS: 0.43 PMOS: 0.31	(Fs ² /g) ^{0.5} m ⁻¹	-	Yes
7	BIGSD	Parameter for I_{gs} and I_{gd}	NMOS: 0.054 PMOS: 0.024	(Fs ² /g) ^{0.5} (mV) ⁻¹	-	Yes
8	CIGSD	Parameter for I_{gs} and I_{gd}	NMOS: 0.075 PMOS: 0.03	V ⁻¹	-	Yes
9	DLCIG	S/D overlap length for I_{gs}/I_{gd}	Lint		-	
10	NIGC	Parameter for I_{gs} , I_{gd} , I_{gcs} and I_{gcd}	1.0		a	Yes
11	POXEDGE	Factor for the gate oxide thickness in the S/D overlap regions	1.0		a	Yes
12	PIGCD	V_{ds} dependence of I_{gcs} and I_{gcd}	1.0		a	Yes

a. If the value is less than or equal to zero, fatal errors are issued.

3.6 Enhanced Binned Parameters for BSIM3SOIv3.1

These are not binned in previous versions.

XJ	ALPHAGB1	ALPHAGB2	BETAGB1	BETAGB2	NDIF
NTRECF	NTRECR	XBJT	XDIF	XREC	XTUN
CGDL	CGSL	CKAPPA	UTE	KT1	KT2
KT1L	UA1	UB1	UC1	AT	PRT

4.0 Printing/Plotting BSIM3SOI v2.x and v3.x States

All states can be printed or plotted if the instance parameter `debug` or the alternative parameter `dbxmod` is equal to 1.

Printing/Plotting BSIM3SOI MOSFET Static States

Quantity	Description
<i>Ids</i>	MOS channel current
<i>Gds</i>	Derivative of <i>Ids</i> with respect to <i>Vds</i>
<i>Gm</i>	Derivative of <i>Ids</i> with respect to <i>Vgs</i>
<i>Gmb</i>	Derivative of <i>Ids</i> with respect to <i>Vbs</i>
<i>Gme</i>	Derivative of <i>Ids</i> with respect to <i>Ves</i>
<i>Gmt</i>	Derivative of <i>Ids</i> with respect to the thermal node voltage (self-heating)
<i>Iii</i>	Impact ionization current
<i>Giid</i>	Derivative of <i>Iii</i> with respect to <i>Vds</i>
<i>Giig</i>	Derivative of <i>Iii</i> with respect to <i>Vgs</i>
<i>Giib</i>	Derivative of <i>Iii</i> with respect to <i>Vbs</i>
<i>Giie</i>	Derivative of <i>Iii</i> with respect to <i>Ves</i>
<i>Giit</i>	Derivative of <i>Iii</i> with respect to the thermal node voltage (self-heating)
<i>Ibs</i>	Body to source diode current
<i>Gjsd</i>	Derivative of <i>Ibs</i> with respect to <i>Vds</i>
<i>Gjsg</i>	Derivative of <i>Ibs</i> with respect to <i>Vgs</i>
<i>Gjsb</i>	Derivative of <i>Ibs</i> with respect to <i>Vbs</i>
<i>Gmibs</i>	Derivative of <i>Ibs</i> with respect to <i>Vbs</i> (alias to <i>Gjsb</i>)
<i>Gjst</i>	Derivative of <i>Ibs</i> with respect to the thermal node voltage (self-heating)
<i>Ibd</i>	Body to drain diode current
<i>Gjdd</i>	Derivative of <i>Ibd</i> with respect to <i>Vds</i>
<i>Gjdg</i>	Derivative of <i>Ibd</i> with respect to <i>Vgs</i>
<i>Gjdb</i>	Derivative of <i>Ibd</i> with respect to <i>Vbs</i>
<i>Gmibd</i>	Derivative of <i>Ibd</i> with respect to <i>Vbd</i>
<i>Gjdt</i>	Derivative of <i>Ibd</i> with respect to the thermal node voltage (self-heating)
<i>Ibp</i>	Body to drain diode current

Printing/Plotting BSIM3SOI v2.x and v3.x StatesBSIM3SOI v2.x and v3.x Equations

Quantity	Description
<i>Gbpds</i>	Derivative of I_{bp} with respect to V_{ds}
<i>Gpgs</i>	Derivative of I_{bp} with respect to V_{gs}
<i>Gpbs</i>	Derivative of I_{bp} with respect to V_{bs}
<i>Gpes</i>	Derivative of I_{bp} with respect to V_{es}
<i>Gpps</i>	Derivative of I_{bp} with respect to V_{ps}
<i>Gbpt</i>	Derivative of I_{bp} with respect to the thermal node voltage (self-heating)
<i>Idaccess</i>	Drain Access current
<i>Gdaccess</i>	Drain Access conductance
<i>Isaccess</i>	Source Access current
<i>Gsaccess</i>	Source Access conductance
<i>Rbp</i>	B/P body resistance
<i>Body</i>	V_b value iterated by Eldo

Printing/Plotting BSIMPD v2.2.1 and higher MOSFET Static States

Quantity	Description
<i>Igb</i>	Gate body current
<i>Gigd</i>	Derivative of I_{gb} with respect to V_{ds}
<i>Gigg</i>	Derivative of I_{gb} with respect to V_{gs}
<i>Gigb</i>	Derivative of I_{gb} with respect to V_{bs}
<i>Gigt</i>	Derivative of I_{gb} with respect to the thermal node voltage (self-heating)

In the case of self-heating:

Quantity	Description
<i>Temp</i>	Device temperature with self-heating mode turned on
<i>Ith</i>	Thermal power dissipated inside the device
<i>Ith_Vd</i>	Derivative of I_{th} with respect to V_{ds}
<i>Ith_Vg</i>	Derivative of I_{th} with respect to V_{gs}
<i>Ith_Vb</i>	Derivative of I_{th} with respect to V_{bs}
<i>Ith_Ve</i>	Derivative of I_{th} with respect to V_{es}
<i>Ith_Deltemp</i>	Derivative of I_{th} with respect to the thermal node voltage
<i>Irth</i>	Thermal current flowing in R_{th}
<i>Gth</i>	Derivative of I_{th} with respect to the thermal node voltage

Printing/Plotting BSIM3SOI MOSFET Dynamic States

Quantity	Description
Q_{gate}	Gate Charge
Q_{drn}	Drain Charge
Q_{src}	Source Charge
Q_{sub}	Substrate (backgate) Charge
Q_{body}	Internal Body Charge
Q_{gdo}	Gate-Drain overlap charge
Q_{gso}	Gate-Source overlap charge
Q_{geo}	Gate-Substrate (backgate) overlap charge
C_{gdo}	Gate-Drain overlap capacitance
C_{gso}	Gate-Source overlap capacitance
C_{geo}	Gate-Substrate (backgate) overlap capacitance
C_{xy}	where x and y could be any of: d, g, s, e, b: transcapacitance between nodes x and y; i.e. derivative of Q_x with respect to V_y
C_{xy}	where x and y could be any of: d, g, s, e, b: transcapacitance between nodes x and y; i.e. derivative of Q_x with respect to V_y
C_{bsj}	B/S intrinsic junction capacitance
C_{bdj}	B/D intrinsic junction capacitance

In the case of self-heating:

Quantity	Description
C_{gt}	Derivative of Q_{gate} with respect to the thermal node voltage
C_{dt}	Derivative of Q_{drn} with respect to the thermal node voltage
C_{st}	Derivative of Q_{src} with respect to the thermal node voltage
C_{et}	Derivative of Q_{sub} with respect to the thermal node voltage
Q_{th}	Thermal node Charge
C_{th}	Thermal node Capacitance

4.1 .OP Print out

The following parameters are printed in the `.OP` analysis:

$Vgs, Vds, Vbs, Ids, Ibs, Ibd, Vth, Vdsat, Gm, Gds, Gmb, Gme, Cgg, Cgd,$
 $Cgs, Cge, Cgb, Cdg, Cdd, Cds, Cde, Cdb, Csg, Csd, Css, Cse, Csb, Ceg,$
 $Ced, Ces, Cee, Ceb.$

5.0 References

- [1] Y. Cheng, M. C. Jeng, Z. H. Liu, J. Huang M. Chan, P. K. Ko, and C. Hu, “A Physical and Scalable I-V Model in BSIM3v3 for Analog/Digital Circuit Simulation”, IEEE Trans. On Elec. Dev., vol. 42, p. 2, Feb 1997.
- [2] BSIM3SOIv1.3 User’s Manual, UC Berkeley, Department of EECS.
- [3] W. Jin, P. C. H. Chan, S. K. H. Fung, P. K. Ko, “A Physically-Based Low-Frequency Noise Model for NFD SOI MOSFET’s”, IEEE Intl. SOI conf., pp. 23-24, 1998.
- [4] BSIM3v3.2 User’s Manual, UC Berkeley, Department of EECS.

Chapter 21

MOS Model 9 Equations

1.0 Introduction

Philips MOS 9 model is a compact model for MOS transistor, intended for the simulation of circuit behavior with emphasis on analog applications. This model has been developed originally by Philips Electronics N.V. and is now in the public domain.

The main characteristics of this model that ensure proper operations in the analog domain are the following:

- the consistency of current and charges description by using the same carrier-density and electrical-field expressions
- a good transition from weak to strong inversion
- a good transition from linear to saturation region
- the continuity for all charges and current expressions and their derivatives
- a reduced parameter set to describe an individual transistor.



For more information on this model, you can refer to the following paper: “*Compact Modeling for Analog Circuit Simulation*” by R.M.D.A Velghe, D.B.M Klaasen, and F.M Klaasen, IEDM Technical Digest, pp.485-488, 1993.

The implementation in Eldo is based on the unclassified report NL-UR 003/94 “MOS MODEL 9, level 902” issued in June 1995. The current implementation is MOS Model 9, level 903.

1.1 Changes between MOS level 903 and MOS level 902

- A new flicker noise model has been added, which can be selected by setting the switch **NFMOD** to 1. Selecting the default value **NFMOD = 0** yields the previous level 902 flicker noise model. In this way backwards compatibility is achieved.
- The coefficients W_{DOG} and f_{θ_1} have been put in their logical position in the list of scaling parameters.

1.2 Version selection

The model parameter **VERSION** can be set to values of 903.1 (default) or 903.2. When set to 903.2, it allows the model parameter **THE3R** to take negative values, otherwise **THE3R** is clipped to zero if negative.

Parameter Value	Effect on THE3R
VERSION=903.1	Clip THE3R to zero if negative
VERSION=903.2	Allows THE3R to take negative values

2.0 Preprocessing and Clipping

2.1 Effective channel length and width

$$Leff = L + LVAR - 2 \cdot LAP \quad Weff = W + WVAR - 2 \cdot WOT$$



$Leff$ and $Weff$ after calculation cannot be less than 0!

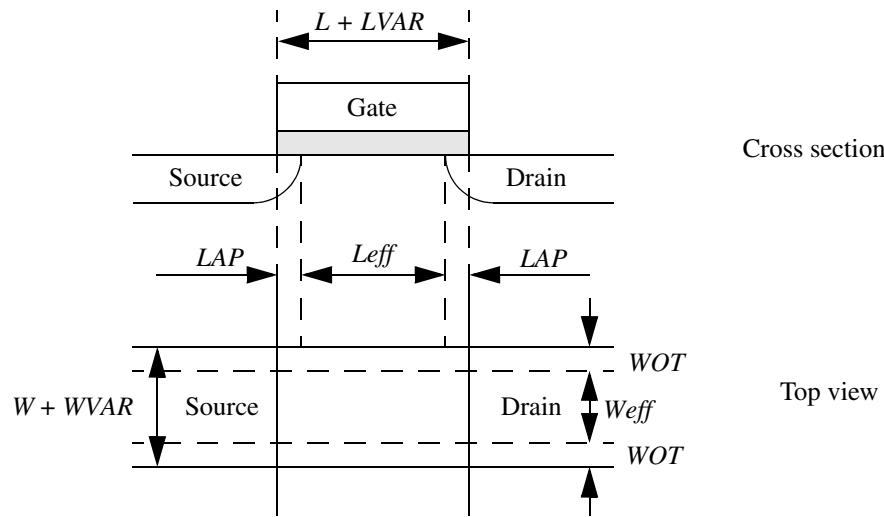


Figure 21-1. Specification of the dimensions of an MOS transistor

2.2 Calculation of the threshold voltage parameters

$$V_{T0} = \tilde{V}_{T0} + \left(\frac{1}{L_{eff}} - \frac{1}{LER} \right) \cdot SLVTO + \left(\frac{1}{L_{eff}^2} - \frac{1}{LER^2} \right) \cdot SL2VTO + \left(\frac{1}{Weff} - \frac{1}{WER} \right) \cdot SWVTO$$

$$k_\theta = KOR + \left(\frac{1}{L_{eff}} - \frac{1}{LER} \right) \cdot SLKO + \left(\frac{1}{Weff} - \frac{1}{WER} \right) \cdot SWKO$$

$$K = KR + \left(\frac{1}{L_{eff}} - \frac{1}{LER} \right) \cdot SLK + \left(\frac{1}{Weff} - \frac{1}{WER} \right) \cdot SWK$$

$$V_{SBX} = VSBXR + \left(\frac{1}{L_{eff}} - \frac{1}{LER} \right) \cdot SLVSBX + \left(\frac{1}{Weff} - \frac{1}{WER} \right) \cdot SWVSBX$$

2.3 Calculation of the channel-current parameters

$$\beta = \tilde{\beta} \cdot \frac{W_{eff}}{L_{eff}} \cdot M$$

$$WEDOG = WDOG + WVAR - 2 \cdot WOT$$



WEDOG after calculation must be \leq ***WER***.

If ***WDOG*** \leq ***W (W_drawn)***

$$\theta_1 = \tilde{\theta}_1 + \left(\frac{1}{L_{eff}} - \frac{1}{LER} \right) \cdot SLTHE1 + \left(\frac{1}{W_{eff}} - \frac{1}{WER} \right) \cdot SWTHE1$$

else

$$\begin{aligned} \theta_1 = \tilde{\theta}_1 &+ \left(\frac{1}{L_{eff}} - \frac{1}{LER} \right) \cdot SLTHE1 + \left(\frac{1}{W_{eff}} - \frac{1}{WER} \right) \cdot SWTHE1 \\ &+ \left(\frac{W_{eff}}{WEDOG} - 1 \right) \cdot \left(\frac{FTHE1}{L_{eff}} \right) \cdot SLTHE1 \end{aligned}$$

while for ***THE2*** and ***THE3***

$$\theta_2 = \tilde{\theta}_2 + \left(\frac{1}{L_{eff}} - \frac{1}{LER} \right) \cdot SLTHE2 + \left(\frac{1}{W_{eff}} - \frac{1}{WER} \right) \cdot SWTHE2$$

$$\theta_3 = \tilde{\theta}_3 + \left(\frac{1}{L_{eff}} - \frac{1}{LER} \right) \cdot SLTHE3 + \left(\frac{1}{W_{eff}} - \frac{1}{WER} \right) \cdot SWTHE3$$

2.4 Calculation of drain-feedback parameters

$$\gamma_1 = GAM1R + \left(\frac{1}{Leff} - \frac{1}{LER} \right) \cdot SLGAM1 + \left(\frac{1}{Weff} - \frac{1}{WER} \right) \cdot SWGAM1$$

$$\alpha = ALPR + \left(\frac{1}{Leff^{ETAALP}} - \frac{1}{LER^{ETAALP}} \right) \cdot SLALP + \left(\frac{1}{Weff} - \frac{1}{WER} \right) \cdot SWALP$$

$$V_P = V_{PR} \cdot \left(\frac{Leff}{LER} \right)$$

2.5 Calculation of subthreshold parameters

$$\gamma_{00} = GAMOOR + \left(\frac{1}{Leff^2} - \frac{1}{LER^2} \right) \cdot SLGAMOO$$

$$m_0 = \tilde{m}_0 + \left(\frac{1}{\sqrt{Leff}} - \frac{1}{\sqrt{LER}} \right) \cdot SLMO$$

$$\varsigma_1 = ZET1R + \left(\frac{1}{Leff^{ETAZET}} - \frac{1}{LER^{ETAZET}} \right) \cdot SLZET1$$

$$V_{SBT} = VSBTR + \left(\frac{1}{Leff} - \frac{1}{LER} \right) \cdot SLVBST$$

2.6 Calculation of weak avalanche parameters

$$a_1 = \tilde{a}_1 + \left(\frac{1}{Leff} - \frac{1}{LER} \right) \cdot SLA1 + \left(\frac{1}{Weff} - \frac{1}{WER} \right) \cdot SWA1$$

$$a_2 = A2R + \left(\frac{1}{Leff} - \frac{1}{LER} \right) \cdot SLA2 + \left(\frac{1}{Weff} - \frac{1}{WER} \right) \cdot SWA2$$

$$a_3 = A3R + \left(\frac{1}{Leff} - \frac{1}{LER} \right) \cdot SLA3 + \left(\frac{1}{Weff} - \frac{1}{WER} \right) \cdot SWA3$$

2.7 Calculation of charge parameters

$$C_{ox} = \varepsilon_{ox} \cdot \frac{Weff \cdot Leff}{TOX} \cdot M$$

$$C_{GDO} = Weff \cdot M \cdot COL \quad C_{GSO} = Weff \cdot M \cdot COL$$

2.8 Calculation of Noise parameters

$$N_F = \frac{WER \cdot LER \cdot NFR}{Weff \cdot Leff \cdot M}$$

$$NFA = NFAR \cdot \frac{WER \cdot LER}{Weff \cdot Leff}$$

$$NFB = NFBR \cdot \frac{WER \cdot LER}{Weff \cdot Leff}$$

$$NFC = NFCR \cdot \frac{WER \cdot LER}{Weff \cdot Leff}$$

2.9 Clipping

For very uncommon geometries or temperatures, the preprocessing rules may generate parameters that are outside a physically realistic range or that may create difficulties in the numerical evaluation of the model. In order to prevent this, all parameters after being updated, are clipped if their values are beyond a certain limit. This is a part of the model itself.

This is shown in the original Philips code, commenting for example:

Negative values for the parameters **THE1**, **THE2**, **THE3**, **GAM00** and **GAM1** should be clipped but not give a warning in the geometrical model.

Eldo should give the following warning:

```
Warning 240: OBJECT "MN1":  
          Parameter GAM00 has been clipped to 0.0  
Warning 240: OBJECT "MN1":  
          Parameter GAM1 has been clipped to 0.0  
Warning 240: OBJECT "MN1":  
          Parameter THE1 has been clipped to 0.0
```

Warning 240: OBJECT "MN1":

Parameter THE2 has been clipped to 0.0

The default values and clipping values as used by *Pstar* for the parameters of the electrical MOS model, level 903 (n-channel) are listed below.

No.	Name	Units	Default	Clip low	Clip high
1	LEVEL	-	903	-	-
2	VTO	V	7.099154 x 10 ⁻⁰¹		-
3	KO	V ^{-1/2}	6.478116 x 10 ⁻⁰¹	1.0 x 10 ⁻¹²	-
4	K	V ^{-1/2}	4.280174 x 10 ⁻⁰¹	a	-
5	PHIB	V	6.225999 x 10 ⁻⁰¹	1.0 x 10 ⁻¹²	-
6	VSBX	V	6.599578 x 10 ⁻⁰¹	1.0 x 10 ⁻¹²	-
7	BET	AV ⁻²	1.418789 x 10 ⁻⁰³	0.0	-
8	THE1	V ⁻¹	1.923533 x 10 ⁻⁰¹	0.0	-
9	THE2	V ^{-1/2}	1.144632 x 10 ⁻⁰²	0.0	1.0
10	THE3	V ⁻¹	1.381597 x 10 ⁻⁰¹	0.0	-
11	GAM1	V ^(1-ηDS)	1.476930 x 10 ⁻⁰¹	0.0	-
12	ETADS	-	6.000000 x 10 ⁻⁰¹	-	-
13	ALP	-	2.878165 x 10 ⁻⁰³	0.0	-
14	VP	V	3.338182 x 10 ⁻⁰¹	1.0 x 10 ⁻¹²	
15	GAM00	-	1.861785 x 10 ⁻⁰²	0.0	-
16	ETAGAM	-	2.000000 x 10 ⁺⁰⁰	-	-
17	MO	-	5.024606 x 10 ⁻⁰¹	1.0 x 10 ⁻¹²	-
18	ETAM	-	2.000000 x 10 ⁺⁰⁰	-	-
19	PHIT	V	2.662680 x 10 ⁻⁰²	0.0	-
20	ZET1	-	4.074464 x 10 ⁻⁰¹	1.0 x 10 ⁻¹²	-
21	VSBT	V	2.025926 x 10 ⁺⁰⁰	0.0	-
22	A1	-	6.022073 x 10 ⁺⁰⁰	0.0	-
23	A2	V	3.801696 x 10 ⁺⁰¹	1.0 x 10 ⁻¹²	-
24	A3	-	6.407407 x 10 ⁻⁰¹	0.0	-
25	COX	F	2.979787 x 10 ⁻¹⁴	0.0	-
26	CGDO	F	6.392000 x 10 ⁻¹⁵	0.0	-
27	CGSO	F	6.392000 x 10 ⁻¹⁵	0.0	-
28	NT	J	2.563182 x 10 ⁻²⁰	0.0	-

No.	Name	Units	Default	Clip low	Clip high
29	NFMOD	-	0	-	-
30	NF	V ²	-	-	-
31	NFA	V ⁻¹ m ⁻⁴	7.15 x 10 ²²	10 ⁻¹²	-
32	NFB	V ⁻¹ m ⁻²	2.16 x 10 ⁷	-	-
33	NFC	V ⁻¹	0	-	-
34	TOX	m	25 x 10 ⁻⁹	-	-
35	MULT	-	1.0	0.0	-

a. The lower bound for $K = K_0 \cdot \frac{\sqrt{hyp_1(-V_{SBX}, \varepsilon_2)}}{\sqrt{V_{SBX} + \phi_B}}$

The default values and clipping values as used by **Pstar** for the parameters of the electrical MOS model, level 903 (p-channel) are listed below.

No.	Name	Units	Default	Clip low	Clip high
1	LEVEL	-	903	-	-
2	VTO	V	1.082125 x 10 ⁺⁰⁰	-	-
3	KO	V ^{-1/2}	4.280174 x 10 ⁻⁰¹	1.0 x 10 ⁻¹²	-
4	K	V ^{-1/2}	4.280174 x 10 ⁻⁰¹	a	-
5	PHIB	V	6.225999 x 10 ⁻⁰¹	1.0 x 10 ⁻¹²	-
6	VSBX	V	1.000000 x 10 ⁻¹²	1.0 x 10 ⁻¹²	-
7	BET	AV ⁻²	4.841498 x 10 ⁻⁰⁴	0.0	-
8	THE1	V ⁻¹	2.046809 x 10 ⁻⁰¹	0.0	-
9	THE2	V ^{-1/2}	1.492490 x 10 ⁻⁰¹	0.0	1.0
10	THE3	V ⁻¹	3.267633 x 10 ⁻⁰²	0.0	-
11	GAM1	V ^(1-ηDS)	9.905701 x 10 ⁻⁰¹	0.0	-
12	ETADS	-	6.000000 x 10 ⁻⁰¹	-	-
13	ALP	-	4.766925 x 10 ⁻⁰²	0.0	-
14	VP	V	1.861200 x 10 ⁻⁰¹	1.0 x 10 ⁻¹²	-
15	GAM00	-	1.118334 x 10 ⁻⁰²	0.0	-
16	ETAGAM	-	1.000000 x 10 ⁺⁰⁰	-	-
17	MO	-	3.801987 x 10 ⁻⁰¹	1.0 x 10 ⁻¹²	-
18	ETAM	-	1.000000 x 10 ⁺⁰⁰	-	-

No.	Name	Units	Default	Clip low	Clip high
19	PHIT	V	2.662680×10^{-02}	0.0	-
20	ZET1	-	$1.270446 \times 10^{+00}$	1.0×10^{-12}	-
21	VSBT	V	$1.000000 \times 10^{+02}$	0.0	-
22	A1	-	$6.858299 \times 10^{+00}$	0.0	-
23	A2	V	$5.732410 \times 10^{+01}$	1.0×10^{-12}	-
24	A3	-	4.254087×10^{-01}	0.0	-
25	COX	F	2.717113×10^{-14}	0.0	-
26	CGDO	F	6.358400×10^{-15}	0.0	-
27	CGSO	F	6.358400×10^{-15}	0.0	-
28	NT	J	2.216522×10^{-20}	0.0	-
29	NFMOD	-	0	-	-
30	NF	V^2	-	-	-
31	NFA	$V^{-1} m^{-4}$	1.53×10^{22}	10^{-12}	
32	NFB	$V^{-1} m^{-2}$	4.06×10^6	-	-
33	NFC	V^{-1}	2.92×10^{-10}	-	-
34	TOX	m	25×10^{-9}	-	-
35	MULT	-	1.0	0.0	-

a. The lower bound for $K = K_0 \cdot \frac{\sqrt{hyp_1(-V_{SBX}, \varepsilon_2)}}{\sqrt{V_{SBX} + \phi_B}}$

3.0 Extended Equations

3.1 Useful functions

$$hyp_1(x; \varepsilon) = \frac{1}{2} \cdot \left(x + \sqrt{x^2 + 4 \cdot \varepsilon^2} \right)$$

$$hyp_2(x; x_0, \varepsilon) = x - hyp_1(x - x_0; \varepsilon)$$

$$hyp_3(x; x_0, \varepsilon) = hyp_2(x; x_0, \varepsilon) - hyp_2(0; x_0, \varepsilon)$$

$$hyp_4(x; x_0, \varepsilon) = hyp_1(x - x_0; \varepsilon) - hyp_1(-x_0; \varepsilon)$$

$$hyp_5(x; x_0, \varepsilon) = x_0 - hyp_1\left(x_0 - x - \frac{\varepsilon^2}{x_0}, \varepsilon\right)$$

3.2 Constant definitions

$\varepsilon_1 = 10^{-2}$	$\varepsilon_4 = 5 \cdot 10^{-4}$	$\lambda_1 = 0.1$	$\lambda_5 = 0.1$
$\varepsilon_2 = 0.1$	$\varepsilon_6 = 0.03$	$\lambda_2 = 10^{-4}$	$\lambda_6 = 0.3$
$\varepsilon_3 = 10^{-2}$	$\varepsilon_7 = 10^{-12}$	$\lambda_3 = 10^{-8}$	$\lambda_7 = 37$
		$\lambda_4 = 0.3$	$\lambda_8 = 0.1$

3.3 Extended current equations

$$h_1 = hyp_1\left(vsb + \frac{1}{2} \cdot \Phi_B; \varepsilon_1\right) + \frac{1}{2} \cdot \Phi_B$$

$$v_s = \sqrt{h_1}$$

$$v_{s0} = \sqrt{\Phi_B}$$

$$v_{st} = \sqrt{V_{SBT} + \Phi_B}$$

$$v_{sx} = \sqrt{V_{SBX} + \Phi_B}$$

$$\Delta V_{T0} = k \cdot \left(\sqrt{hyp_4(vsb; V_{SBX}, \varepsilon_2) + \left(\frac{k}{k_0}\right)^2 \cdot v_{sx}^2} - \left(\frac{k}{k_0}\right) \cdot v_{sx} \right)$$

$$+ k_0 \cdot (\sqrt{h_1 - hyp_4(vsb; V_{SBX}, \varepsilon_2)} - v_{s0})$$

$$V_{T1} = V_{T0} + \Delta V_{T0}$$

$$v_{s1} = hyp_2(v_s; v_{st}, \varepsilon_3)$$

$$\gamma_0 = \gamma_{00} \cdot \left(\frac{v_{s1}}{v_{s0}}\right)^{ETAGAMR}$$

$$V_{GT1} = hyp_1(vgs - V_{T1}; \varepsilon_4)$$

$$\Delta V_{T1} = \left(-\gamma_0 - (\gamma_1 \cdot (vds + \lambda_2)^{ETADSR-1} - \gamma_0) \cdot \frac{V_{GT1}^2}{0.5 + V_{GT1}^2} \right) \cdot \frac{vds^2}{vds + \lambda_1}$$

$$V_{T2} = V_{T1} + \Delta V_{T1}$$

$$m = 1 + m_0 \cdot \left(\frac{v_{s0}}{v_{s1}}\right)^{ETAMR}$$

$$V_{GT2} = vgs - V_{T2}$$

$$V_{GTA} = 2 \cdot m \cdot \Phi_T \cdot \lambda_7$$

$$G_1 = \begin{cases} \exp\left(\frac{V_{GT2}}{2 \cdot m \cdot \Phi_T}\right), & V_{GT2} < V_{GTA} \\ \text{No assignment is necessary,} & V_{GT2} \geq V_{GTA} \end{cases}$$

$$V_{GT3} = \begin{cases} 2 \cdot m \cdot \Phi_T \cdot \ln(1 + G_1) + \lambda_3, & V_{GT2} < V_{GTA} \\ V_{GT2} + \lambda_3, & V_{GT2} \geq V_{GTA} \end{cases}$$

$$\delta_1 = \frac{\lambda_4}{v_s} \cdot \left(k + \frac{(k_0 - k) \cdot V_{SBX}^2}{V_{SBX}^2 + (\lambda_5 \cdot V_{GT1} + vsb)^2} \right)$$

$$V_{DSS1} = \frac{V_{GT3}}{1 + \delta_1} \cdot \frac{2}{1 + \sqrt{1 + \frac{2 \cdot \theta_3 \cdot V_{GT3}}{1 + \delta_1}}}$$

$$\varepsilon_5 = \lambda_6 \cdot \frac{V_{DSS1}}{1 + V_{DSS1}}$$

$$V_{DS1} = hyp_5(vds; V_{DSS1}, \varepsilon_5)$$

$$G_2 = 1 + \alpha \cdot \ln\left(1 + \frac{vds - V_{DS1}}{V_P}\right)$$

$$G_3 = \begin{cases} \frac{\zeta_1 \cdot \left(1 - \exp\left(\frac{-vds}{\Phi_T}\right)\right) + G_1 \cdot G_2}{\frac{1}{\zeta_1} + G_1}, & V_{GT2} < V_{GTA} \\ G_2, & V_{GT2} \geq V_{GTA} \end{cases}$$

$$Ids = \beta \cdot G_3 \cdot \frac{V_{GT3} \cdot V_{DS1} - \left(\frac{1 + \delta_1}{2}\right) \cdot V_{DS1}^2}{(1 + \theta_1 \cdot V_{GT1} + \theta_2 \cdot (v_s - v_{s0})) \cdot (1 + \theta_3 \cdot V_{DS1})}$$

$$V_{DSA} = a_3 \cdot V_{DSS1}$$

$$Icb = \begin{cases} 0, & vds < V_{DSA} \\ Ids \cdot a_1 \cdot \exp\left(\frac{-a_2}{vds - V_{DSA}}\right), & vds \geq V_{DSA} \end{cases}$$

3.4 Extended charge equations

$$vdb = vds + vsb$$

$$h_2 = hyp_1\left(vdb + \frac{1}{2} \cdot \Phi_B; \varepsilon_1\right) + \frac{1}{2} \cdot \Phi_B$$

$$\Delta V_{T0d} = k \cdot \left(\sqrt{hyp_4(vdb; V_{SBX}, \varepsilon_2) + \left(\frac{k}{k_0}\right)^2 \cdot v_{sx}^2} - \left(\frac{k}{k_0}\right) \cdot v_{sx} \right) \\ + k_0 \cdot (\sqrt{h_2 - hyp_4(vdb; V_{SBX}, \varepsilon_2)} - v_{s0})$$

$$V_{T1d} = V_{T0} + \Delta V_{T0d}$$

$$\delta_2 = \frac{\partial V_{T2}}{\partial vsb} - \frac{\partial V_{T2}}{\partial vgs} - \frac{\partial V_{T2}}{\partial vds}$$

$$\Delta_2 = -\frac{\partial V_{GT3}}{\partial vsb} + \frac{\partial V_{GT3}}{\partial vgs} + \frac{\partial V_{GT3}}{\partial vds}$$

$$V_{DSS2} = \frac{V_{GT3}}{1 + \delta_2} \cdot \frac{2}{1 + \sqrt{1 + \frac{2 \cdot \theta_3 \cdot V_{GT3}}{1 + \delta_2}}}$$

$$\varepsilon_7 = \lambda_8 \cdot \frac{V_{DSS2}}{1 + V_{DSS2}}$$

$$V_{DS2} = hyp_5(vds; V_{DSS2}, \varepsilon_7)$$

$$F_J = \frac{(1 + \delta_2) \cdot (1 + \theta_3 \cdot V_{DS2}) \cdot V_{DS2}}{2 \cdot V_{GT3} - (1 + \delta_2) \cdot V_{DS2}}$$

$$Q_D = -Cox \cdot \left(\frac{1}{2} \cdot V_{GT3} + \Delta_2 \cdot V_{DS2} \cdot \left(\frac{1}{12} \cdot F_J + \frac{1}{60} \cdot F_J^2 - \frac{1}{3} \right) \right)$$

$$Q_S = -Cox \cdot \left(\frac{1}{2} \cdot V_{GT3} + \Delta_2 \cdot V_{DS2} \cdot \left(\frac{1}{12} \cdot F_J - \frac{1}{60} \cdot F_J^2 - \frac{1}{6} \right) \right)$$

$$vgb = vgs + vsb$$

$$V_{FB} = V_{T0} - \Phi_B - k_0 \sqrt{\Phi_B}$$

$$Q_{BS} = \begin{cases} -Cox \cdot hyp_3(vgb - V_{FB}; vsb + V_{T1} - V_{FB}, \varepsilon_6), & vgb < V_{FB} \\ -Cox \cdot k_0 \left(-\frac{k_0}{2} + \sqrt{\left(\frac{k_0}{2}\right)^2 + hyp_3(vgb - V_{FB}; vsb + V_{T1} - V_{FB}, \varepsilon_6)} \right), & vgb \geq V_{FB} \end{cases}$$

$$Q_{BD} = \begin{cases} -Cox \cdot hyp_3(vgb - V_{FB}; V_{DS2} + vsb + V_{T1d} - V_{FB}, \varepsilon_6), & vgb < V_{FB} \\ -Cox \cdot k_0 \left(-\frac{k_0}{2} + \sqrt{\left(\frac{k_0}{2}\right)^2 + hyp_3(vgb - V_{FB}; V_{DS2} + vsb + V_{T1d} - V_{FB}, \varepsilon_6)} \right), & vgb \geq V_{FB} \end{cases}$$

$$Q_B = \frac{1}{2} \cdot (Q_{BS} + Q_{BD})$$

$$Q_G = -(Q_D + Q_S + Q_B)$$

3.5 Extended noise equations

$$g_m = \frac{\partial I_{DS}}{\partial vgs}$$

$$F_I = \frac{(1 + \delta_1) \cdot (1 + \theta_3 \cdot V_{DS1}) \cdot V_{DS1}}{2 \cdot V_{GT3} - (1 + \delta_1) \cdot V_{DS1}}$$

$$h_3 = \beta \cdot G_3 \cdot \left(\frac{V_{GT3} - \frac{1}{2} \cdot (1 + \delta_1) \cdot V_{DS1}}{(1 + \theta_1 \cdot V_{GT1} + \theta_2 \cdot (v_s - v_{s0})) \cdot (1 + \theta_3 \cdot V_{DS1})} \right)$$

$$h_4 = 1 + \theta_3 \cdot V_{DS1} + \frac{1}{3} \cdot F_I^2$$

$$h_5 = \frac{V_{DSS1}}{2 \cdot \Phi_T}$$

$$h_6 = \begin{cases} h_3 \cdot h_4, & h_4 < h_5 \\ h_3 \cdot h_5, & h_4 \geq h_5 \end{cases}$$

$$S_{th} = N_T \cdot h_6$$

If **NFMOD** = 0 then:

$$S_{fl} = N_F \cdot \frac{g_m^2}{f}$$

If **NFMOD** = 1 then:

$$N_0 = \frac{\varepsilon_{ox}}{qt_{ox}} \cdot V_{GT3}$$

$$N_L = \frac{\varepsilon_{ox}}{qt_{ox}} \cdot (V_{GT3} - V_{DS1})$$

$$N'' = \frac{\varepsilon_{ox}}{qt_{ox}} \cdot \phi_T \cdot (m_0 + 1)$$

$$S_{wi} = N_{FA} \cdot \frac{\phi_T \cdot I_{DS}^2}{f \cdot N''^2}$$

$$S_{si} = \frac{\phi_T \cdot q^2 \cdot I_{DS} \cdot \beta \cdot t_{ox}^2}{f \cdot \varepsilon_{ox}^2 \cdot \{1 + \theta_1 \cdot V_{GT1} + \theta_2 \cdot (u_s - u_{s0})\}}$$

$$\cdot \left[N_{FA} \cdot \ln \left(\frac{N_0 + N''}{N_L + N''} \right) + N_{FB} \cdot (N_0 - N_L) + \frac{1}{2} \cdot N_{FC} \cdot (N_0^2 - N_L^2) \right]$$

$$+ \frac{\phi_T \cdot I_{DS}^2}{f} \cdot \frac{G_2 - 1}{G_2} \cdot \left\{ \frac{N_{FA} + N_{FB} \cdot N_L + N_{FC} \cdot N_L^2}{(N_L + N'')^2} \right\}$$

$$S_{fl} = \frac{S_{si} \cdot S_{wi}}{(S_{si} + S_{wi})}$$

$$S_{ig} = N_T \cdot \frac{(2 \cdot \pi \cdot f \cdot Cox)^2 \cdot g_m}{3 \cdot (g_m^2 + 0.075 \cdot (2 \cdot \pi \cdot f \cdot Cox)^2)}$$

$$\rho_{igth} = 0.4j$$

$$S_{igth} = \rho_{igth} \cdot N_T \cdot 2 \cdot \pi \cdot f \cdot Cox \cdot \sqrt{\frac{g_m \cdot h_6}{3 \cdot (g_m^2 + 0.075 \cdot (2 \cdot \pi \cdot f \cdot Cox)^2)}}$$

4.0 Temperature Effects

$$\delta T = T - T_{nom}$$

$$\tilde{V}_{T\theta} = VTO + \delta T \cdot STVTO$$

$$S_{T;\phi_B} = \frac{PHIBR - 1.13 - 2.5 \cdot 10^{-4} \cdot T_{nom}}{300}$$

$$\phi_B = PHIBR + \delta T \cdot S_{T;\phi_B}$$

$$\tilde{\beta} = BETASQ \cdot \left(\frac{T_{nom}}{T} \right)^{ETABET}$$

$$\tilde{\theta}_1 = THE1R + \delta T \cdot STTHE1R$$

$$SLTHE1 = SLTHE1R + \delta T \cdot STLTHE1$$

$$\tilde{\theta}_2 = THE2R + \delta T \cdot STTHE2R$$

$$SLTHE2 = SLTHE2R + \delta T \cdot STLTHE2$$

$$\tilde{\theta}_3 = THE3R + \delta T \cdot STTHE3R$$

$$SLTHE3 = SLTHE3R + \delta T \cdot STLTHE3$$

$$\tilde{m}_0 = MOR + \delta T \cdot STM0$$

$$\Phi_T = \frac{k_B \cdot T}{q}$$

$$\tilde{a}_I = AIR + \delta T \cdot STA1$$

$$N_T = \frac{T}{T_{nom}} \cdot NTR$$

5.0 .OP Printout

When simulating MM9 models and performing a **.OP** analysis, the following parameters are printed out in the **.chi** file.

Vt0 V_{T0} with **L** and **W** effects

Vt1 $V_{T1} = V_{T0} + \Delta V_{T0}$ (V_{T1} with **Vbs** effect)

Vth Final threshold voltage $V_{T2} = V_{T1} + \Delta V_{T1}$

Vth_d $V_{gs} - V_{th}$

Isub Substrate current



Vth and **Vth_d** are always printed in the **.OP** analysis for all models. **Vt0** and **Vt1** are done specifically for MM9.

Note

6.0 Model Parameters

In the table below, there are three sets of default values for each parameter, each corresponding to the following settings of **INIT**:

1. **INIT** = 1
2. **INIT** = 0—NMOS type
3. **INIT** = 0—PMOS type

Nr.	Name	Description	Default values, set by INIT			Units
			(1)	(2)	(3)	
1	INIT	Selector for default values	1 ^a	0 ^a	0 ^a	
2	VERSION	Version selector; when set to 903.2 it allows THE3R to take negative values	903.1	903.1	903.1	
3	AF	Flicker noise exponent	1	1	1	
4	TOX	Thickness of oxide layer	2.5×10^{-8}	2.5×10^{-8}	2.5×10^{-8}	m
5	CGBO	Gate-bulk overlap capacitance	0	0	0	Fm ⁻¹
6	CGDO	Gate-drain overlap capacitance	0	0 ^b	0 ^b	Fm ⁻¹

Nr.	Name	Description	Default values, set by INIT			Units
			(1)	(2)	(3)	
7	CGSO	Gate-source overlap capacitance	0	0 ^b	0 ^b	Fm ⁻¹
8	COL	Gate overlap capacitance	0	3.2×10 ⁻⁴	3.2×10 ⁻⁴	Fm ⁻¹
9	LER	Effective channel length of the reference transistor	0	1.1×10 ⁻⁶	1.25×10 ⁻⁶	m
10	WER	Effective channel width of the reference transistor	0	20×10 ⁻⁶	20×10 ⁻⁶	m
11	VTOR	Threshold voltage at zero back-bias for the reference transistor at the reference temperature	1	0.73	1.1	V
12	STVTO	Coefficient of the temperature dependence of V_{T0}	0	-1.2×10 ⁻³	-1.7×10 ⁻³	V°K ⁻¹
13	SLVTO	Coefficient of the length dependence of V_{T0}	0	-1.35×10 ⁻⁷	3.5×10 ⁻⁸	Vm
14	SL2VTO	Second coefficient of the length dependence of V_{T0}	0	0	0	Vm ²
15	SWVTO	Coefficient of the width dependence of V_{T0}	0	1.3×10 ⁻⁷	5.0×10 ⁻⁸	Vm
16	KOR	Low-back-bias body factor for the reference transistor	1	0.65	0.47	V ^{1/2}
17	SLKO	Coefficient of the length dependence of k_0	0	-1.3×10 ⁻⁷	-2.0×10 ⁻⁷	V ^{1/2} m
18	SWKO	Coefficient of the width dependence of k_0	0	2.0×10 ⁻⁹	1.15×10 ⁻⁷	V ^{1/2} m
19	KR	High-back-bias body factor for the reference transistor	1	0.11	0.47	V ^{1/2}
20	SLK	Coefficient of the length dependence of k	0	-2.8×10 ⁻⁷	-2.0×10 ⁻⁷	V ^{1/2} m
21	SWK	Coefficient of the width dependence of k	0	2.75×10 ⁻⁷	1.15×10 ⁻⁷	V ^{1/2} m
22	PHIBR	Surface potential at strong inversion for the reference transistor at the reference temperature	0.6	0.65	0.65	V
23	VSBXR	Transition voltage for the dual- k -factor model for reference transistor	0.6	0.66	1.0×10 ⁻¹²	V
24	SLVSBX	Coefficient of the length dependence of V_{SBX}	0	0	0	Vm
25	SWVSBX	Coefficient of the width dependence of V_{SBX}	0	-6.75×10 ⁻⁷	0	Vm

Nr.	Name	Description	Default values, set by INIT			Units
			(1)	(2)	(3)	
26	BETSQ	Gain factor for an infinite square transistor at the reference temperature	1.0×10^{-4}	8.3×10^{-5}	2.61×10^{-5}	AV^{-2}
27	ETABET	Exponent of the temperature dependence of the gain factor	0	1.6	1.6	
28	WDOG	Characteristic drawn gate width, below which dogboning appears	0	0	0	m
29	FTHE1	Coefficient describing the width dependence of THE1 for $W < \text{WDOG}$	0	0	0	
30	THE1R	Coefficient of the mobility reduction due to the gate-induced field for the reference transistor at the reference temperature	0	0.19	0.19	V^{-1}
31	STTHE1R	Coefficient of the temperature dependence of θ_1 for the reference transistor	0	0	0	$\text{V}^{-1}\text{K}^{-1}$
32	SLTHE1R	Coefficient of the length dependence of θ_1 at the reference temperature	0	1.4×10^{-7}	7.0×10^{-8}	V^{-1}m
33	STLTHE1	Coefficient of the temperature dependence of the length dependence of θ_1	0	0	0	$\text{V}^{-1}\text{m}^\circ\text{K}^{-1}$
34	SWTHE1	Coefficient of the width dependence of θ_1	0	-5.8×10^{-8}	-8.0×10^{-8}	V^{-1}m
35	THE2R	Coefficient of the mobility reduction due to the back-bias for the reference transistor at the reference temperature	0	1.2×10^{-2}	0.165	$\text{V}^{-1/2}$
36	STTHE2R	Coefficient of the temperature dependence of θ_2 for the reference transistor	0	0	0	$\text{V}^{-1/2}\text{K}^{-1}$
37	SLTHE2R	Coefficient of the length dependence of θ_2 at the reference temperature	0	-3.3×10^{-8}	-7.5×10^{-8}	$\text{V}^{-1/2}\text{m}$
38	STLTHE2	Coefficient of the temperature dependence of the length dependence of θ_2	0	0	0	$\text{V}^{-1/2}\text{m}^\circ\text{K}^{-1}$
39	SWTHE2	Coefficient of the width dependence of θ_2	0	3.0×10^{-8}	2.0×10^{-8}	$\text{V}^{-1/2}\text{m}$

Nr.	Name	Description	Default values, set by INIT			Units
			(1)	(2)	(3)	
40	THE3R^c	Coefficient of the mobility reduction due to the lateral field for the reference transistor at the reference temperature	0	0.145	2.7×10^{-2}	V ⁻¹
41	STTHE3R	Coefficient of the temperature dependence of θ_3 for the reference transistor	0	-6.6×10^{-4}	0	V ⁻¹ °K ⁻¹
42	SLTHE3R	Coefficient of the length dependence of θ_3 at the reference temperature	0	1.85×10^{-7}	2.7×10^{-8}	V ⁻¹ m
43	STLTHE3	Coefficient of the temperature dependence of the length dependence of θ_3	0	-6.2×10^{-10}	0	V ⁻¹ m°K ⁻¹
44	SWTHE3	Coefficient of the width dependence of θ_3	0	2.0×10^{-8}	1.1×10^{-8}	V ⁻¹ m
45	GAM1R	Coefficient for the drain induced threshold shift for large gate drive for the reference transistor	0	0.145	7.7×10^{-2}	V ^(1 - n_{ps})
46	SLGAM1	Coefficient of the length dependence of γ_1	0	1.6×10^{-7}	1.05×10^{-7}	V ^(1 - n_{ps}) m
47	SWGAM1	Coefficient of the width dependence of γ_1	0	-1.0×10^{-8}	-1.1×10^{-8}	V ^(1 - n_{ps}) m
48	ETADSR	Exponent of V_{DS} dependence of γ_1 for the reference transistor	1	0.6	0.6	
49	ALPR	Factor of the channel-length modulation for the reference transistor	0	3.0×10^{-3}	4.4×10^{-2}	
50	ETAALP	Exponent of the length dependence of α	0	0.15	0.17	
51	SLALP	Coefficient of the length dependence of α	0	-5.65×10^{-3}	9.0×10^{-3}	m ^{n_α}
52	SWALP	Coefficient of the width dependence of α	0	1.67×10^{-9}	1.8×10^{-10}	m
53	VPR	Characteristic voltage of the channel-length modulation for the reference transistor	1.0×10^{-12}	0.34	0.235	V
54	GAMOOR	Coefficient of the drain induced threshold shift at zero gate drive for the reference transistor	0	1.8×10^{-2}	7.0×10^{-3}	
55	SLGAMOO	Coefficient of the length dependence of γ_{00}	0	2.0×10^{-14}	1.1×10^{-14}	m ²

Nr.	Name	Description	Default values, set by INIT			Units
			(1)	(2)	(3)	
56	ETAGAMR	Exponent of the back-bias dependence of γ_0 for the reference transistor	0	2.0	1.0	
57	MOR	Factor of the subthreshold slope for the reference transistor at the reference temperature	1.0×10^{-12}	0.5	0.375	
58	STMO	Coefficient of the temperature dependence of m_0	0	0	0	$^{\circ}\text{K}^{-1}$
59	SLMO	Coefficient of the length dependence of m_0	0	2.8×10^{-4}	4.7×10^{-5}	$\text{m}^{-1/2}$
60	ETAMR	Exponent of the back-bias dependence of m for the reference transistor	0	2.0	1.0	
61	ZET1R	Weak inversion correction factor for the reference transistor	1.0×10^{-12}	0.42	1.3	
62	ETAZET	Exponent of the length dependence of ζ_1	0	0.17	3.0×10^{-2}	
63	SLZET1	Coefficient of the length dependence of ζ_1	0	-0.39	-2.8	m^{η_ζ}
64	VSBTR	Limiting voltage of the V_{SB} dependence of m and γ_0 for the reference transistor	0	2.1	1.0×10^2	V
65	SLVSBT	Coefficient of the length dependence of V_{SBT}	0	-4.4×10^{-6}	0	Vm
66	A1R	Factor for the weak-avalanche current for the reference transistor at the reference temperature	0	6.0	10	
67	STA1	Coefficient of the temperature dependence of a_1	0	0	0	$^{\circ}\text{K}^{-1}$
68	SLA1	Coefficient of the length dependence of a_1	0	1.3×10^{-6}	-1.5×10^{-5}	m
69	SWA1	Coefficient of the width dependence of a_1	0	3.0×10^{-6}	3.0×10^{-5}	m
70	A2R	Exponent for the weak-avalanche current for the reference transistor at the reference temperature	1.0×10^{-12}	38	59	V
71	SLA2	Coefficient of the length dependence of a_2	0	1.0×10^{-6}	-8.0×10^{-6}	Vm
72	SWA2	Coefficient of the width dependence of a_2	0	2.0×10^{-6}	1.5×10^{-5}	m

Nr.	Name	Description	Default values, set by INIT			Units
			(1)	(2)	(3)	
73	A3R	Factor of the drain-source voltage above which the weak-avalanche occurs, for the reference transistor	0	0.65	0.52	
74	SLA3	Coefficient of the length dependence of a_3	0	-5.5×10^{-7}	-4.5×10^{-7}	m
75	SWA3	Coefficient of the width dependence of a_3	0	0	-1.4×10^{-7}	m
76	NTR	Coefficient of the thermal noise for the reference transistor	0	2.44×10^{-20}	2.11×10^{-20}	J
77	NFR	Coefficient of the flicker noise for the reference transistor	0	7.0×10^{-11}	2.14×10^{-11}	V ²
78	NFMOD	Switch that selects either old or new flicker noise model	0	0	0	
79	NFAR	First coefficient of the flicker noise (for NFMOD =1)	0	7.15×10^{22}	1.53×10^{22}	V ⁻¹ m ⁻⁴
80	NFBR	Second coefficient of the flicker noise (for NFMOD =1)	0	2.16×10^7	4.06×10^6	V ⁻¹ m ⁻²
81	NFCR	Third coefficient of the flicker noise (for NFMOD =1)	0	0	2.92×10^{-10}	V ⁻¹

- a. The default value for **INIT** is 0
- b. If both **CGDO** and **CGSO** are not defined, the value of **COL** is used.
- c. When the model parameter **VERSION** is set to 903.2, **THE3R** is allowed to take negative values, otherwise it is clipped to zero if negative.

In addition to the Philips syntax for the parameters, some equivalences to common approach parameters are made as shown in the table below. In these cases, the same default values are used.

Philips	Eldo
LVAR	DL
LAP	LD
WVAR	DW
WOT	WD
NFR	KF
TR	TNOM

Additionally, all the parameters available for the common approach are available for this model together with the corresponding equations set for parasitics. Furthermore, **AF** slope for noise has been added in Eldo. The overlap capacitances may be defined through the Philips parameter **COL** or through **CGDO**, **CGSO**. **CGBO** is also introduced.

The instantiation parameter **MULT** that indicates the number of devices in parallel is called **M** in Eldo.

The present restrictions in Eldo v4.x w.r.t. Philips implementation is that noise equations only include **Sfl** and **Sth** terms.

Chapter 22

BSIM4 Equations

1.0 Introduction

The BSIM4 model is implemented in Eldo as LEVEL=60. There are five versions of this model, BSIM4.0.0, BSIM4.1.0, BSIM4.2.0, BSIM4.2.1 and BSIM4.3.0 (default).



BSIM4 accepts the M factor.

Note

The BSIM4 model has been developed to explicitly address many issues in modeling sub-0.13 micron CMOS technology and RF high-speed CMOS circuit simulation. BSIM4 has the following major improvements and additions over BSIM3v3:

- An accurate new model of the intrinsic input resistance (R_{ii}) for both RF, high-frequency analog and high-speed digital applications.
- Flexible substrate resistance network for RF modeling.
- A new accurate channel thermal noise model and a noise partition model for the induced gate noise.
- A non-quasi-static (NQS) model that is consistent with the R_{ii} -based RF model and a consistent AC model that accounts for the NQS effect in both transconductances and capacitances.
- An accurate gate direct tunneling model.

- A comprehensive and versatile geometry-dependent parasitics model for various source/drain connections and multi-finger devices.
- Improved model for steep vertical retrograde doping profiles.
- Better model for pocket-implanted devices in Vth, bulk charge effect model, and Rout.
- Asymmetrical and bias-dependent source/drain resistance, either internal or external to the intrinsic MOSFET at the user's discretion.
- Acceptance of either the electrical or physical gate oxide thickness as the model input at the user's choice in a physically accurate manner.
- The quantum mechanical charge-layer-thickness model for both IV and CV.
- A more accurate mobility model for predictive modeling.
- A gate-induced drain leakage (GIDL) current model, available in BSIM for the first time.
- An improved unified flicker (1/f) noise model, which is smooth over all bias regions and considers the bulk charge effect.
- Different diode IV and CV characteristics for source and drain junctions.
- Junction diode breakdown with or without current limiting.
- Dielectric constant of the gate dielectric as a model parameter.

1.1 BSIM4.1.0 enhancements

The following modifications have been introduced in BSIM4.1.0:

- An analytical equation for the model parameter PIGCD when it is not specified. In the partitioning of the Ig_C current (part of the Gate tunneling current), if the model parameter PIGCD is not specified, it is given by:
$$\text{PIGCD} = (\text{B} \cdot \text{TOXE} / \text{Vgsteff}^2) (1 - \text{Vdseff} / 2 \cdot \text{Vgsteff})$$

- Long-channel Vdsat used to eliminate the spike in thermal noise with tnoimod=0
- Remove warning in case NF > 500

1.2 BSIM4.2.0 enhancements

The improvements incorporated into BSIM4.2.0 are:

- Bug fixes
- Addition of two new parameters XL and XW

XL and XW are geometry offset parameters due to mask/etch effect with default values of 0.0. They are used to update the value of L and W as shown below:

$$L_{new} = L + XL$$

$$W_{new} = \frac{W}{NF} + XW$$

L_{new} and W_{new} are then used to make further calculations.



With these changes, the BSIM3 parasitic resistance model becomes a compatible subset of the BSIM4 parasitic resistance model.

1.3 BSIM4.2.1 enhancements

The following modifications have been introduced in BSIM4.2.1:

- Bug fixes:
 - 1/f noise model bug fix
problem: negative DelClm under certain conditions of voltage bias, temperature, L, and W.
 - Bug fix for Narrow Width Effect.

- Addition of Gate Induced Source Leakage (GISL). This has an enormous impact on circuit simulation convergence.

$$I_{GISL} = AGIDL \cdot W_{effCJ} \cdot Nf \cdot \frac{-V_{ds} - V_{gde} - EGIDL}{3 \cdot T_{oxe}} \\ \cdot \exp\left(-\frac{3 \cdot T_{oxe} \cdot BGIDL}{-V_{ds} - V_{gde} - EGIDL}\right) \cdot \frac{V_{sb}^3}{CGIDL + V_{sb}^3}$$

- L, W, Tox Parameter Warning Limit.
Recommended values here are for a meaningful output of BSIM4.

	Original	Now	Recommended
LEFF (m)	5e-8	1e-9	1e-8
LEFFEVT (m)	5e-8	1e-9	1e-8
WEFF (m)	1e-7	1e-9	1e-7
WEFFEVT(m)	1e-7	1e-9	1e-7
TOXE (m)	1e-9	1e-10	5e-10
TOXP (m)	1e-9	1e-10	5e-10
TOXM (m)	1e-9	1e-10	5e-10

- ACDE warning messages for capMod 2 only (not for other capacitance models).

1.4 BSIM4.3.0 enhancements

BSIM4.3.0 has the following major improvements and additions over BSIM4.2.1:

- A new scalable stress effect model for process induced stress effect; device performance becoming thus a function of the active area geometry and the location of the device in the active area;
- A unified current-saturation model that includes all mechanisms of current saturation—velocity saturation, velocity overshoot and source end velocity limit;
- A new temperature model format that allows convenient prediction of temperature effects on saturation velocity, mobility, and S/D resistances;

- Enhanced accuracy and flexibility of holistic thermal noise model;
- Improved accuracy of forward body bias model; and
- Extension of gate direct tunneling model to multiple-layer gate dielectrics.

Also, this version includes some Bug Fixes:

- Parameter CKAPPAS and CKAPPAD checking.
- Igate not saturation with VDS.
- Cgg error in CapMod=1.
- Thermal noise error.
- Typo error in Drain diode current.
- Rdsmod=0, rds scaling with NF.
- Gate shot noise calculation swapping.

1.5 Use of Juncap diode (**DIOLEV=9.0**) with BSIM4

The Juncap diode (**DIOLEV=9**) can be used as a parasitic diode for the MOSFET instead of that provided by Berkeley.

The Juncap diode can be chosen by specifying the model card parameter **DIOLEV=9.0**. Values for **DIOLEV** other than 9.0 will give a warning and the diode quantities will be calculated using the Berkeley parasitic diodes.

The parameters and equations of the Juncap diode (**DIOLEV= 9.0**) can all be found in the section “[Level 8 Equations](#)” on page 1-19.



Note The initialization of device parameters (*PS*, *AS*, *PD*, *AD*) and calculation of geometrical quantities (*PSeff*, *ASeff*, *PDeff*, *ADeff*) are all Berkeley standard for BSIM4; not those of the common equations.

1.6 Version selection

The different versions, BSIM4.0.0, BSIM4.1.0, BSIM4.2.0, BSIM4.2.1 and BSIM4.3.0, are accessible through the model parameter **VERSION**. By default, BSIM4.3.0 (**VERSION**=4.3) is selected.

Parameter Value	BSIM4 Version
VERSION =4.3	BSIM4.3.0 (Default)
VERSION =4.21	BSIM4.2.1
VERSION =4.2	BSIM4.2.0
VERSION =4.1	BSIM4.1.0
VERSION =4.0	BSIM4.0.0

1.7 Documentation

- i** User's can access the full documentation of the Berkeley BSIM4.2.0 model by selecting the link below:
[BSIM4.2.0 MOSFET Model - User's Manual](#)

- i** User's can access the full documentation of the Berkeley BSIM4.1.0 model by selecting the link below:
[BSIM4.1.0 MOSFET Model - User's Manual](#)

- i** Additionally, the following web site can be visited for further information:
<http://www-device.eecs.berkeley.edu/>

2.0 BSIM4 Parameters

Nr.	Name	Description	Default	Binnable?	Notes
1	LEVEL	Eldo model selector	60	N/A	Must be set to 60 to select BSIM4 model
2	VERSION	Model version number	4.3	N/A	BSIM4 latest official release
3	BINUNIT	Binning unit selector	1	N/A	-
4	PARAMCHK	Switch for parameter value check	1	N/A	Parameters checked
5	MOBMOD	Mobility model selector	1	N/A	-
6	RDSMOD	Bias-dependent source/drain resistance model selector	0	N/A	R_{ds} (V) modeled internally through IV equation
7	IGCMOD	Gate-to-channel tunneling current model selector	0	N/A	OFF
8	IGBMOD	Gate-to-substrate tunneling current model selector	0	N/A	OFF
9	CAPMOD	Capacitance model selector	2	N/A	-
10	RGATEMOD (also an instance parameter)	Gate resistance model selector	0 (no gate resistance)	N/A	-
11	RBODYMOD (also an instance parameter)	Substrate resistance network model selector	0 (network off)	N/A	-
12	TRNQSMOD (also an instance parameter)	Transient NQS model selector	0	N/A	OFF
13	ACNQSMOD (also an instance parameter)	AC small-signal NQS model selector	0	N/A	OFF
14	FNOIMOD	Flicker noise model selector	1	N/A	-
15	TNOIMOD	Thermal noise model selector	0	N/A	-
16	DIOMOD	Source/drain junction diode IV model selector	1	N/A	-

Nr.	Name	Description	Default	Binnable?	Notes
17	TEMPMOD	Temperature mode selector	0	No	Not valid for versions < 4.3 If 0, original model is used If 1, new format used
18	PERMOD	Whether PS/PD (when given) includes the gate-edge perimeter	1 (including the gate-edge perimeter)	N/A	-
19	GEOMOD (also an instance parameter)	Geometry-dependent parasitics model selector specifying how the end S/D diffusions are connected	0 (isolated)	N/A	-
20	RGEOMOD (instance parameter only)	Source/drain diffusion resistance and contact model selector specifying the end S/D contact type: point, wide or merged, and how S/D parasitics resistance is computed	0 (no S/D diffusion resistance)	N/A	-

Process Parameters

21	EPSROX	Gate dielectric constant relative to vacuum	3.9 (SiO_2)	No	Typically ≥ 3.9
22	TOXE	Electrical gate equivalent oxide thickness	3.0e-9m	No	Fatal error if not positive
23	TOXP	Physical gate equivalent oxide thickness	TOXE	No	Fatal error if not positive
24	TOXM	Tox at which parameters are extracted	TOXE	No	Fatal error if not positive
25	DTOX	Defined as (TOXE-TOXP)	0.0m	No	-
26	XJ	S/D junction depth	1.5e-7m	Yes	-
27	GAMMA1	Body-effect coefficient near the surface	calculated $V^{1/2}$		a
28	GAMMA2	Body-effect coefficient in the bulk	calculated $V^{1/2}$		a
29	NDEP	Channel doping concentration at depletion edge for zero body bias	$1.7\text{e}17\text{cm}^{-3}$	Yes	b
30	NSUB	Substrate doping concentration	$6.0\text{e}16\text{cm}^{-3}$	Yes	-
31	NGATE	Poly Si gate doping concentration	0.0cm^{-3}	Yes	-
32	NSD	Source/drain doping concentration Fatal error if not positive	$1.0\text{e}20\text{cm}^{-3}$	Yes	-

Nr.	Name	Description	Default	Binnable?	Notes
33	VBX	V_{bs} at which the depletion region width equals XT	calculated (V)	No	c
34	XT	Doping depth	1.55e-7m	Yes	-
35	RSH	Source/drain sheet resistance	0.0 ohm/ square	No	Should not be negative
36	RSHG	Gate electrode sheet resistance	0.1 ohm/ square	No	Should not be negative

Basic Model Parameters

37	VTH0 or VTHO	Long-channel threshold voltage at $V_{bs} = 0$	0.7V (NMOS) -0.7V (PMOS)	Yes	d
38	DELVT0 (DELVTO) (also an instance parameter)	Zero-bias threshold voltage shift. Can be specified as a model and/or element parameter; they are added together	0 V		e
39	VFB	Flat-band voltage	-1.0V	Yes	d
40	PHIN	Non-uniform vertical doping effect on surface potential	0.0V	Yes	-
41	K1	First-order body bias coefficient	$0.5V^{1/2}$	Yes	f
42	K2	Second-order body bias coefficient	0.0	Yes	e
43	K3	Narrow width coefficient	80.0	Yes	-
44	K3B	Body effect coefficient of K3	$0.0 V^{-1}$	Yes	-
45	W0	Narrow width parameter	2.5e-6m	Yes	-
46	LPE0	Lateral non-uniform doping parameter at $V_{bs} = 0$	1.74e-7m	Yes	-
47	LPEB	Lateral non-uniform doping effect on K1	0.0m	Yes	-
48	VBM	Maximum applied body bias in VTH0 calculation	-3.0V	Yes	-
49	DVT0	First coefficient of short-channel effect on V_{th}	2.2	Yes	-
50	DVT1	Second coefficient of short-channel effect on V_{th}	0.53	Yes	-
51	DVT2	Body-bias coefficient of short-channel effect on V_{th}	$-0.032V^{-1}$	Yes	-
52	DVTPO	First coefficient of drain-induced V_{th} shift due to for long-channel pocket devices	0.0m	Yes	Not modeled if binned DVTP0 ≤ 0.0
53	DVTPI	First coefficient of drain-induced V_{th} shift due to for long-channel pocket devices	$0.0V^{-1}$	Yes	-

Nr.	Name	Description	Default	Binnable?	Notes
54	DVT0W	First coefficient of narrow width effect on V_{th} for small channel length	0.0	Yes	-
55	DVT1W	Second coefficient of narrow width effect on V_{th} for small channel length	$5.3e6m^{-1}$	Yes	-
56	DVT2W	Body-bias coefficient of narrow width effect for small channel length	$-0.032V^{-1}$	Yes	-
57	U0	Low-field mobility	$0.067 m^2/(Vs)$ (NMOS); $0.025 m^2/(Vs)$ PMOS	Yes	-
58	UA	Coefficient of first-order mobility degradation due to vertical field	$1.0e-9m/V$ for MOBMOD =0 & 1; $1.0e-15m/V$ for MOBMOD=2	Yes	-
59	UB	Coefficient of second-order mobility degradation due to vertical field	$1.0e-19m^2/v^2$	Yes	-
60	UC	Coefficient of mobility degradation due to body-bias effect	$-0.0465V^{-1}$ for MOBMOD=1; $-0.0465e-9 /V^2$ for MOBMOD =0 and 2	Yes	-
61	EU	Exponent for mobility degradation of MOBMOD=2	1.67 (NMOS); 1.0 (PMOS)	Yes	-
62	VSAT	Saturation velocity	$8.0e4m/s$	Yes	-
63	A0	Coefficient of channel-length dependence of bulk charge effect	1.0	Yes	-
64	AGS	Coefficient of V_{gs} dependence of bulk charge effect	$0.0V^{-1}$	Yes	-
65	B0	Bulk charge effect coefficient for channel width	0.0m	Yes	-
66	B1	Bulk charge effect width offset	0.0m	Yes	-
67	KETA	Body-bias coefficient of bulk charge effect	$-0.047V^{-1}$	Yes	-
68	A1	First non-saturation effect parameter	$0.0V^{-1}$	Yes	-
69	A2	Second non-saturation factor	1.0	Yes	-
70	WINT	Channel-width offset parameter	0.0m	Yes	-
71	LINT	Channel-length offset parameter	0.0m	Yes	-
72	DWG	Coefficient of gate bias dependence of W_{eff}	$0.0m/V$	Yes	-

Nr.	Name	Description	Default	Binnable?	Notes
73	DWB	Coefficient of body bias dependence of W_{eff} bias dependence	0.0m/V ^{1/2}	Yes	-
74	VOFF	Offset voltage in subthreshold region for large W and L	-0.08V	Yes	-
75	VOFFL	Channel-length dependence of VOFF	0.0mV	No	-
76	MINV	V_{gsteff} fitting parameter for moderate inversion condition	0.0	Yes	-
77	NFACTOR	Subthreshold swing factor	1.0	Yes	-
78	ETA0	DIBL coefficient in subthreshold region	0.08	Yes	-
79	ETAB	Body-bias coefficient for the sub-threshold DIBL effect	-0.07V ⁻¹	Yes	-
80	DSUB	DIBL coefficient exponent in sub-threshold region	DROUT	Yes	-
81	CIT	Interface trap capacitance	0.0F/m ²	Yes	-
82	CDSC	coupling capacitance between source/drain and channel	2.4e-4F/m ²	Yes	-
83	CDSCB	Body-bias sensitivity of CDSC	0.0F/(Vm ²)	Yes	-
84	CDSCD	Drain-bias sensitivity of CDSC	0.0(F/Vm ²)	Yes	-
85	PCLM	Channel length modulation parameter	1.3	Yes	-
86	PDIBLC1	Parameter for DIBL effect on Rout	0.39	Yes	-
87	PDIBLC2	Parameter for DIBL effect on Rout	0.0086	Yes	-
88	PDIBLCB	Body bias coefficient of DIBL effect	0.0V ⁻¹	Yes	-
89	DROUT	Channel-length dependence of DIBL	0.56	Yes	-2
90	PSCBE1	First substrate current induced body-effect parameter	4.24e8V/m	Yes	-
91	PSCBE2	Second substrate current induced body-effect parameter	1.0e-5m/V	Yes	-
92	PVAG	Gate-bias dependence of Early voltage	0.0	Yes	-
93	DELTA	Parameter for DC V_{dseff}	0.01V	Yes	-

Nr.	Name	Description	Default	Binnable?	Notes
94	FPROUT	Effect of pocket implant on Rout degradation	0.0V/m 0.5	Yes	Not modeled if binned FPROUT not positive
95	PDITS	Impact of drain-induced V_{th} shift on Rout	0.0V ⁻¹	Yes	Not modeled if binned PDITS=0; Fatal error if binned PDITS negative
96	PDITSL	Channel-length dependence of drain-induced V_{th} shift for Rout	0.0m ⁻¹	Yes	-
97	PDITSD	V_{ds} dependence of drain-induced V_{th} shift for Rout	0.0V ⁻¹	Yes	-
98	LAMBDA	Velocity overshoot coefficient	0.0	Yes	Not valid for versions < 4.3 If not given or (≤ 0.0), velocity overshoot will be turned off
99	VTL	Thermal velocity	2.05e5 m/s	Yes	Not valid for versions < 4.3 If not given or (≤ 0.0), source end thermal velocity limit will be turned off
100	LC	Velocity back scattering coefficient	0.0 m	No	Not valid for versions < 4.3 ~5e9m at room temperature
101	XN	Velocity back scattering coefficient	3.0	Yes	Not valid for versions < 4.3

Parameters for Asymmetric and Bias-Dependent R_{ds} Model

102	RDSW	Zero bias LDD resistance per unit width for RDSMOD=0	200.0 ohm(μm) ^{WR}	Yes	If negative, reset to 0.0
103	RDSWMIN	LDD resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=0	0.0 ohm(μm) ^{WR}	No	-
104	RDW	Zero bias lightly-doped drain resistance $R_d(V)$ per unit width for RDS MOD=1	100.0 ohm(μm) ^{WR}	Yes	-
105	RDWMIN	Lightly-doped drain resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=1	0.0 ohm(μm) ^{WR}	No	-

Nr.	Name	Description	Default	Binnable?	Notes
106	RSW	Zero bias lightly-doped source resistance $R_s(V)$ per unit width for RDS MOD=1	$100.0 \text{ ohm}(\mu\text{m})^{\text{WR}}$	Yes	-
107	RSWMIN	Lightly-doped source resistance per unit width at high V_{gs} and zero V_{bs} for	$0.0 \text{ ohm}(\mu\text{m})^{\text{WR}}$	No	-
108	PRWG	Gate-bias dependence of LDD resistance	1.0V^{-1}	Yes	-
109	PRWB	Body-bias dependence of LDD resistance	$0.0\text{V}^{-0.5}$	Yes	-
110	WR	Channel-width dependence parameter of LDD resistance	1.0	Yes	-
111	NRS (instance parameter only)	Number of source diffusion squares	1.0	No	-
112	NRD (instance parameter only)	Number of drain diffusion squares	1.0	No	-

Impact Ionization Current Model Parameters

113	ALPHA0	First parameter of impact ionization	0.0Am/V	Yes	-
114	ALPHA1	lsub parameter for length scaling	0.0A/V	Yes	-
115	BETA0	The second parameter of impact ionization current	30.0V	Yes	-

Gate-Induced Drain Leakage Model Parameters

116	AGIDL	Pre-exponential coefficient for GIDL	0.0mho	Yes	$I_{gidl}=0.0$ if binned AGIDL=0.0
117	BGIDL	Exponential coefficient for GIDL	2.3e9V/m	Yes	$I_{gidl}=0.0$ if binned BGIDL=0.0
118	CGIDL	Parameter for body-bias effect on GIDL	0.5V^3	Yes	-
119	EGIDL	Fitting parameter for band bending for GIDL	0.8V	Yes	-

Gate Dielectric Tunneling Current Model Parameters

120	AIGBACC	Parameter for I_{gb} in accumulation	$0.43 (\text{Fs}^2/\text{g})^{0.5} \text{ m}^{-1}$	Yes	-
121	BIGBACC	Parameter for I_{gb} in accumulation	$0.054 (\text{Fs}^2/\text{g})^{0.5} \text{ m}^{-1}$	Yes	-
122	CIGBACC	Parameter for I_{gb} in accumulation	0.075V^{-1}	Yes	-
123	NIGBACC	Parameter for I_{gb} in accumulation	1.0	Yes	Fatal error if binned value not positive

Nr.	Name	Description	Default	Binnable?	Notes
124	AIGBINV	Parameter for I_{gb} in inversion	$0.35 (\text{Fs}^2/\text{g})^{0.5} \text{m}^{-1}$	Yes	-
125	BIGBINV	Parameter for I_{gb} in inversion	$0.03 (\text{Fs}^2/\text{g})^{0.5} \text{m}^{-1} \text{V}^{-1}$	Yes	-
126	CIGBINV	Parameter for I_{gb} in inversion	0.006V^{-1}	Yes	-
127	EIGBINV	Parameter for I_{gb} in inversion	1.1V	Yes	-
128	NIGBINV	Parameter for I_{gb} in inversion	3.0	Yes	Fatal error if binned value not positive
129	AIGC	Parameter for I_{gcs} and I_{gcd}	$0.054 \text{ (NMOS)} \text{ and } 0.31 \text{ (PMOS)} (\text{Fs}^2/\text{g})^{0.5} \text{m}^{-1}$	Yes	-
130	BIGC	Parameter for I_{gcs} and I_{gcd}	$0.054 \text{ (NMOS)} \text{ and } 0.024 \text{ (PMOS)} (\text{Fs}^2/\text{g})^{0.5} \text{m}^{-1} \text{V}^{-1}$	Yes	-
131	CIGC	Parameter for I_{gcs} and I_{gcd}	$0.075 \text{ (NMOS)} \text{ and } 0.03 \text{ (PMOS)} \text{ V}^{-1}$	Yes	-
132	AIGSD	Parameter for I_{gs} and I_{gd}	$0.43 \text{ (NMOS)} \text{ and } 0.31 \text{ (PMOS)} (\text{Fs}^2/\text{g})^{0.5} \text{m}^{-1}$	Yes	-
133	BIGSD	Parameter for I_{gs} and I_{gd}	$0.054 \text{ (NMOS)} \text{ and } 0.024 \text{ (PMOS)} (\text{Fs}^2/\text{g})^{0.5} \text{m}^{-1} \text{V}^{-1}$	Yes	-
134	CIGSD	Parameter for I_{gs} and I_{gd}	$0.075 \text{ (NMOS)} \text{ and } 0.03 \text{ (PMOS)} \text{ V}^{-1}$	Yes	-
135	DLCIG	Source/drain overlap length for I_{gs} and I_{gd}	LINT	Yes	-
136	NIGC	Parameter for I_{gcs} , I_{gcd} , I_{gs} and I_{gd}	1.0	Yes	Fatal error if binned value not positive
137	POXEDGE	Factor for the gate oxide thickness in source/drain overlap regions	1.0	Yes	Fatal error if binned value not positive
138	PIGCD	V_{ds} dependence of I_{gcs} and I_{gcd}	1.0	Yes	Fatal error if binned value not positive
139	NTOX	Exponent for the gate oxide ratio	1.0	Yes	-
140	TOXREF	Nominal gate oxide thickness for gate dielectric tunneling current model only	3.0e-9m	No	Fatal error if not positive
Charge and Capacitance Model Parameters					
141	XPART	Charge partition parameter	0.0	No	-

Nr.	Name	Description	Default	Binnable?	Notes
142	CGSO	Non LDD region source-gate overlap capacitance per unit channel width	calculated (F/m)	No	g
143	CGDO	Non LDD region drain-gate overlap capacitance per unit channel width	calculated (F/m)	No	f
144	CGBO	Gate-bulk overlap capacitance per unit channel length	0.0F/m	No	f
145	CGSL	Overlap capacitance between gate and lightly-doped source region	0.0F/m	Yes	-
146	CGDL	Overlap capacitance between gate and lightly-doped source region	0.0F/m	Yes	-
147	CKAPPAS	Coefficient of bias-dependent overlap capacitance for the source side	0.6V	Yes	If VERSION <4.3: If not positive, reset to default If VERSION ≥4.3: If <0.02 reset to 0.02
148	CKAPPAD	Coefficient of bias-dependent overlap capacitance for the drain side	CKAPPAS	Yes	If VERSION <4.3: If not positive, reset to default If VERSION ≥4.3: If <0.02, reset to 0.02
149	CF	Fringing field capacitance	calculated (F/m)	Yes	h
150	CLC	Constant term for the short channel model	1.0e-7m	Yes	-
151	CLE	Exponential term for the short channel model	0.6	Yes	-
152	DLC	Channel-length offset parameter for CV model	LINT (m)	No	-
153	DWC	Channel-width offset parameter for CV model	WINT (m)	No	-
154	VFBCV	Flat-band voltage parameter (for CAPMOD=0 only)	-1.0V	Yes	-
155	NOFF	CV parameter in $V_{gsteff}CV$ for weak to strong inversion	1.0	Yes	-
156	VOFFCV	CV parameter in $V_{gsteff}CV$ for week to strong inversion	0.0V	Yes	-
157	ACDE	Exponential coefficient for charge thickness in CAPMOD=2 for accumulation and depletion regions	1.0m/V	Yes	-

Nr.	Name	Description	Default	Binnable?	Notes
158	MOIN	Coefficient for the gate-bias dependent surface potential	15.0	Yes	-
High-Speed/RF Model Parameters					
159	XRCRG1	Parameter for distributed channel-resistance effect for both intrinsic-input resistance and charge-deficit NQS models	12.	Yes	Warning message issued if binned XRCRG1 ≤ 0.0
160	XRCRG2	Parameter to account for the excess channel diffusion resistance for both intrinsic input resistance and charge-deficit NQS models	1.0	Yes	-
161	RBPB (also an instance parameter)	Resistance connected between bNodePrime and bNode	50.0ohm	No	If $< 1.0e-3 \Omega$, reset to $1.0e-3 \Omega$
162	RBDP (also an instance parameter)	Resistance connected between bNodePrime and dbNode	50.0ohm	No	If $< 1.0e-3 \Omega$, reset to $1.0e-3 \Omega$
163	RBPS (also an instance parameter)	Resistance connected between bNodePrime and sbNode	50.0ohm	No	If $< 1.0e-3 \Omega$, reset to $1.0e-3 \Omega$
164	RBDB (also an instance parameter)	Resistance connected between dbNode and bNode	50.0ohm	No	If $< 1.0e-3 \Omega$, reset to $1.0e-3 \Omega$
165	GMIN	Conductance in parallel with each of the five substrate resistances to avoid potential numerical instability due to unreasonably too large a substrate resistance	1.0e-12mho	No	Warning message issued if $< 1.0e-20$ mho
Flicker and Thermal Noise Model Parameters					
166	NOIA	Flicker noise parameter A	$6.25e41 (\text{eV})^{-1} \text{s}^{1-\text{EF}} \text{m}^{-3}$ for NMOS; $6.188e40 (\text{eV})^{-1} \text{s}^{1-\text{EF}} \text{m}^{-3}$ for PMOS	No	-
167	NOIB	Flicker noise parameter B	$3.125e26 (\text{eV})^{-1} \text{s}^{1-\text{EF}} \text{m}^{-1}$ for NMOS; $1.5e25 (\text{eV})^{-1} \text{s}^{1-\text{EF}} \text{m}^{-1}$ for PMOS	No	-
168	NOIC	Flicker noise parameter C	$8.75 (\text{eV})^{-1} \text{s}^{1-\text{EF}} \text{m}$	No	-
169	EM	Saturation field	$4.1e7 \text{V/m}$	No	-
170	AF	Flicker noise exponent	1.0	No	-
171	EF	Flicker noise frequency exponent	1.0	No	-

Nr.	Name	Description	Default	Binnable?	Notes
172	KF	Flicker noise coefficient	$A^{2-EF} s^{1-EF}$	No	-
173	NTNOI	Noise factor for short-channel devices for TNOIMOD=0 only	1.0	No	-
174	TNOIA	Coefficient of channel-length dependence of total channel thermal noise	1.5	No	-
175	TNOIB	Channel-length dependence parameter for channel thermal noise partitioning	3.5	No	-
176	RNOIA	Thermal noise coefficient	0.577	No	Not valid for versions < 4.3
177	RNOIB	Thermal noise coefficient	0.37	No	Not valid for versions < 4.3

Layout-Dependent Parasitics Model Parameters

178	DMCG	Distance from S/D contact center to the gate edge	0.0m	No	-
179	DMCI	Distance from S/D contact center to the isolation edge in the channel-length direction	DMCG	No	-
180	DMDG	Same as DMCG but for merged device only	0.0m	No	-
181	DMCGT	DMCG of test structures	0.0m	No	-
182	NF (instance parameter only)	Number of device fingers	1	No	Fatal error if less than one; if greater than 500 reset to 20
183	DWJ	Offset of the S/D junction width	DWC (in CV model)	No	-
184	MIN (instance parameter only)	Whether to minimize the number of drain or source diffusions for number fingered device	0 (minimize the drain diffusion number)	No	-
185	XGW	Distance from the gate contact to the channel edge	0.0m	No	-
186	XGL	Offset of the gate length due to variations in patterning	0.0m	No	-
187	NGCON	Number of gate contacts	1	No	Fatal error if less than one; if not equal to 1 or 2, warning message issued and reset to 1

Nr.	Name	Description	Default	Binnable?	Notes
Asymmetric Source/Drain Junction Diode Model Parameters					
188	IJTHSREV IJTHDREV	Limiting current in reverse bias region	IJTHSREV=0.1A IJTHDREV= IJTHSREV	No	If not positive, reset to 0.1A
189	IJTHSFWD IJTHDFWD	Limiting current in forward bias region	IJTHSFWD=0.1A IJTHDFWD= IJHS-FWD	No	If not positive, reset to 0.1A
190	XJBVS XJBVD	Fitting parameter for diode break-down	XJBVS=1.0 XJBVD=XJBVS	No	i
191	BVS BVD	Breakdown voltage	BVS=10.0V BVD=BVS	No	If not positive, reset
192	JSS JSD	Bottom junction reverse saturation current density	JSS=1.0e-4A/m ² JSD=JSS	No	-
193	JSWS JSWD	Isolation-edge sidewall reverse saturation current density	JSWS=0.0A/m JSWD=JSWS	No	-
194	JSWGS JSWGD	Gate-edge sidewall reverse saturation current density	JSWGS=0.0A/m JSWGD=JSWGS	No	-
195	CJS CJD	Bottom junction capacitance per unit area at zero bias	CJS=5.0e-4 F/m ² CJD=CJS	No	-
196	MJS MJD	Bottom junction capacitance grating coefficient	MJS=0.5 MJD=MJS	No	-
197	MJSWS MJSWD	Isolation-edge sidewall junction capacitance grading coefficient	MJSWS=0.33 MJSWD=MJSWS	No	-
198	CJSWS CJSWD	Isolation-edge sidewall junction capacitance per unit area	CJSWS=5.0e-10 F/m CJSWD=CJSWS	No	-
199	CJSWGS CJSWGD	Gate-edge sidewall junction capacitance per unit length	CJSWGS=CJSWS CJSWGD=CJSWS	No	-
200	MJSWGS MJSWGD	Gate-edge sidewall junction capacitance grading coefficient	MJSWGS=MJSWS MJSWGD=MJSWS	No	-
201	PBS PBD	Bottom junction built-in potential	PBS=1.0V PBD=PBS	No	-
202	PBSWD	Isolation-edge sidewall junction built-in potential	PBSWS=1.0V PBSWD=PBSWS	No	-
203	PBSWGS PBSWGD	Gate-edge sidewall junction built-in potential	PBSWGS=PBSWS PBSWGD=PBSWS	No	-
Temperature Dependence Parameters					
204	TNOM	Temperature at which parameters are extracted	27°C	No	-
205	UTE	Mobility temperature exponent	-1.5	Yes	-

Nr.	Name	Description	Default	Binnable?	Notes
206	KT1	Temperature coefficient for threshold voltage	-0.11V	Yes	-
207	KT1L	Channel length dependence of the temperature coefficient for threshold voltage	0.0Vm	Yes	-
208	KT2	Body-bias coefficient of Vth temperature effect	0.022	Yes	-
209	UA1	Temperature coefficient for UA	1.0e-9m/V	Yes	-
210	UB1	Temperature coefficient for UB	-1.0e-18 (m/V) ²	Yes	-
211	UC1	Temperature coefficient for UC	0.067V ⁻¹ for MOBMOD=1; 0.025m/V ² for MOBMOD= 0 and 2	Yes	-
212	AT	Temperature coefficient for saturation velocity	3.3e4m/s	Yes	-
213	PRT	Temperature coefficient for Rds _w	0.0ohm-m	Yes	-
214	NJS, NJD	Emission coefficients of junction for source and drain junctions, respectively	NJS=1.0; NJD=NJS	No	-
215	XTIS, XTID	Junction current temperature exponents for source and drain junctions, respectively	XTIS=3.0; XTID=XTIS	No	-
216	TPB	Temperature coefficient of PB	0.0V/K	No	-
217	TPBSW	Temperature coefficient of PBSW	0.0V/K	No	-
218	TPBSWG	Temperature coefficient of PBSWG	0.0V/K	No	-
219	TCJ	Temperature coefficient of CJ	0.0K ⁻¹	No	-
220	TCJSW	Temperature coefficient of CJSW	0.0K ⁻¹	No	-
221	TCJSWG	Temperature coefficient of CJSWG	0.0K ⁻¹	No	-
Stress Effect Parameters (Not valid for versions < 4.3)					
222	SA (instance parameter only)	Distance between OD edge to Poly from one side	0.0		If not given or (≤ 0), stress effect will be turned off
223	SB (instance parameter only)	Distance between OD edge to Poly from other side	0.0		If not given or (≤ 0), stress effect will be turned off

Nr.	Name	Description	Default	Binnable?	Notes
224	SD (instance parameter only)	Distance between neighboring fingers	0.0		For NF>1: If not given or (≤ 0), stress effect will be turned off
225	SAREF	Reference distance between OD and edge to poly of one side	1e-06 m	No	>0.0
226	SBREF	Reference distance between OD and edge to poly of other side	1e-06 m	No	>0.0
227	WL0D	Width parameter for stress effect	0.0 m	No	-
228	KU0	Mobility degradation/enhancement coefficient for stress effect	0.0 m	No	-
229	KVSAT	Saturation velocity degradation enhancement parameter for stress effect	0.0 m	No	$-1 \leq KVSAT \leq 1$
230	TKU0	Temperature coefficient of KU0	0.0	No	-
231	LKU0	Length dependence of KU0	$0.0 \text{ m}^{\text{LLODKU0}}$	No	-
232	WKU0	Width dependence of KU0	$0.0 \text{ m}^{\text{WL0DKU0}}$	No	-
233	PKU0	Cross-term dependence of KU0	$m^{\frac{0.0}{\text{LLODKU0+WL0DKU0}}}$	No	-
234	LLODKU0	Length parameter for U0 stress effect	0.0	No	>0
235	WL0DKU0	Width parameter for U0 stress effect	0.0	No	>0
236	KVTH0	Threshold shift parameter for stress effect	0.0 Vm	No	-
237	LKVTH0	Length dependence of KVTH0	$0.0 \text{ Vm}^{\text{LLODVTH}}$	No	-
238	WKVTH0	Width dependence of KVTH0	$0.0 \text{ Vm}^{\text{WL0DVTH}}$	No	-
239	PKVTH0	Cross-term dependence of KVTH0	$Vm^{\frac{0.0}{\text{LLODVTH+WL0DVTH}}}$	No	-
240	LLODVTH	Length parameter for KVTH0 stress effect	0.0	No	>0
241	WL0DVTH	Width parameter for KVTH0 stress effect	0.0	No	>0
242	STK2	K2 shift factor related to VTH0 change	0.0 m	No	-
243	LODK2	K2 shift modification factor for stress effect	1.0	No	>0

Nr.	Name	Description	Default	Binnable?	Notes
244	STETA0	ETA0 shift factor related to VTH0 change	0.0 m	No	-
245	LODETA0	ETA0 shift modification factor for stress effect	1.0	No	>0
dW and dL Parameters					
246	WL	Coefficient of length dependence for width offset	0.0m ^{WLN}	No	-
247	WLN	Power of length dependence of width offset	1.0	No	-
248	WW	Coefficient of width dependence for width offset	0.0m ^{WWN}	No	-
249	WWN	Power of width dependence of width offset	1.0	No	-
250	WWL	Coefficient of length and width cross term dependence for width offset	0.0m ^{WWN+WLN}	No	-
251	LL	Coefficient of length dependence for length offset	0.0m ^{LLN}	No	-
252	LLN	Power of length dependence for length offset	1.0	No	-
253	LW	Coefficient of width dependence for length offset	0.0m ^{LWN}	No	-
254	LWN	Power of width dependence for length offset	1.0	No	-
255	LWL	Coefficient of length and width cross term dependence for length offset	0.0m ^{LWN+LLN}	No	-
256	LLC	Coefficient of length dependence for CV channel length offset	LL	No	-
257	LWC	Coefficient of width dependence for CV channel length offset	LW	No	-
258	LWLC	Coefficient of length and width cross-term dependence for CV channel length offset	LWL	No	-
259	WLC	Coefficient of length dependence for CV channel width offset	WL	No	-
260	WWC	Coefficient of width dependence for CV channel width offset	WW	No	-
261	xw	W offset for channel width due to mask/etch effect	0.0		Not valid for versions < 4.2

Nr.	Name	Description	Default	Binnable?	Notes
262	XL	L offset for channel width due to mask/etch effect	0.0		Not valid for versions < 4.2
Range Parameters for Model Application					
263	LMIN	Minimum channel length	0.0m	No	-
264	LMAX	Maximum channel length	1.0m	No	-
265	WMIN	Minimum channel width	0.0m	No	-
266	WMAX	Maximum channel width	1.0m	No	-
Geometry Scaling Parameters					
267	LMLT	Length diffusion layer shrink reduction factor	1		j
268	WMLT	Width diffusion layer shrink reduction factor	1		

a. If **GAMMA1** is not given, it is calculated by

$$GAMMA1 = \frac{\sqrt{2q\epsilon_{si}NDEP}}{C_{oxe}}$$

If **GAMMA2** is not given, it is calculated by

$$GAMMA2 = \frac{\sqrt{2q\epsilon_{si}NSUB}}{C_{oxe}}$$

b. If **NDEP** is not given and **GAMMA1** is given, **NDEP** is calculated from

$$NDEP = \frac{GAMMA1^2 C_{oxe}}{2q\epsilon_{si}}$$

If both **GAMMA1** and **NDEP** are not given, **NDEP** defaults to $1.7e17\text{cm}^{-3}$ and **GAMMA1** is calculated from **NDEP**.

c. If **VBX** is not given, it is calculated by

$$\frac{qNDEP \cdot XT^2}{2\epsilon_{si}} = \Phi_s - VBX$$

d. If **VTH0** is not given, it is calculated by

$$VTH0 = VFB + \Phi_s + K1 \sqrt{\Phi_s - V_{bs}}$$

where **VFB** = -1.0. If **VTH0** is given, **VFB** defaults to

$$VFB = VTH0 - \Phi_s - K1 \sqrt{\Phi_s - V_{bs}}$$

e. The parameter **DELVT0** is added to the parameter **VTH0** whether **VTH0** is given or calculated from **VFB**:

$$VTH0 = VTH0 + DELVT0_{Model} + DELVT0_{Element}$$

f. If **K1** and **K2** are not given, they are calculated by

$$K1 = GAMMA2 - 2k2 \sqrt{\Phi_s - VBM}$$

$$K2 = \frac{(GAMMA1 - GAMMA2)(\sqrt{\Phi_s - VBX} - \sqrt{\Phi_s})}{2 \sqrt{\Phi_s(\sqrt{\Phi_s} - VBM - \sqrt{\Phi_s}) + VBM}}$$

g. If **CGSO** is not given, it is calculated by

if (**DLC** is given and > 0.0)

$$CGSO = DLC \cdot C_{oxe} - CGSL$$

if (**CGSO** < 0.0), **CGSO** = 0.0

else

$$CGSO = 0.6 \cdot XJ \cdot C_{oxe}$$

If **CGDO** is not given, it is calculated by

if (**DLC** is given and > 0.0)

$$CGDO = DLC \cdot C_{oxe} - CGDL$$

if (**CGDO** < 0.0), **CGDO** = 0.0

else

$$CGDO = 0.6 \cdot XJ \cdot C_{oxe}$$

If **CGBO** is not given, it is calculated by

$$CGBO = 2 \cdot DWC \cdot C_{oxe}$$

h. If **CF** is not given, it is calculated by

$$CF = \frac{2 \cdot ESPROX \cdot \epsilon_0}{\pi} \cdot \log\left(1 + \frac{4.0e - 7}{TOXE}\right)$$

i. For **DIOMOD** = 0, if **XJBVS** < 0.0, it is reset to 1.0.

For **DIOMOD** = 2, if **XJBVS** ≤ 0.0, it is reset to 1.0.

For **DIOMOD** = 0, if **XJBVD** < 0.0, it is reset to 1.0.

For **DIOMOD** = 2, if **XJBVD** ≤ 0.0, it is reset to 1.0.

j. They are used as geometry multipliers, such that:

L(used) = **LMLT** × **L**(given)

W(used) = **WMLT** × **W**(given)

PS(used) = **WMLT** × **PS**(given)

PD(used) = **WMLT** × **PD**(given)

AS(used) = **WMLT**² × **AS**(given)

AD(used) = **WMLT**² × **AD**(given)

3.0 Printing or Plotting a State from the BSIM4 States Structure

If a state from the list below is to be monitored by the user, the user has to type in the netlist for a given transistor M1 to monitor, for example Gm:

. PLOT DC S (M1 ->Gm)	for DC or
. PLOT AC S (M1 ->Gm)	for AC or
. PLOT TRAN S (M1 ->Gm)	for TRAN

The same is applied to the following list of states:

Quantity	Description
IDS	Channel current
GDS	Channel conductance
GM	Channel transconductance dI_{ds}/dV_{gs}
GMBS	Channel transconductance dI_{ds}/dV_{bs}
ISUB	Substrate current
IGIDL	Gidl current
IGISL	Gisl current
IBD	Bulk/Drain diode current
GBD	Bulk/Drain diode conductance
IBS	Bulk/Source diode current
GBS	Bulk/Source diode conductance
IGS	Gate/Source current
IGCS	Gate/Source Channel current
IGD	Gate/Drain current
IGCD	Gate/Drain Channel current
IGB	Gate/Bulk current
GRGEELTD	Electrode Gate conductance
GCRG	Channel-Reflected Gate conductance
QGATE	Intrinsic Gate charge
CGG	Intrinsic Gate/Gate capacitance
CGD	Intrinsic Gate/Drain capacitance

Quantity	Description
<i>CGS</i>	Intrinsic Gate/Source capacitance
<i>CGB</i>	Intrinsic Gate/Bulk capacitance
<i>QDRN</i>	Intrinsic Drain charge
<i>CDG</i>	Intrinsic Drain/Gate capacitance
<i>CDD</i>	Intrinsic Drain/Drain capacitance
<i>CDS</i>	Intrinsic Drain/Source capacitance
<i>CDB</i>	Intrinsic Drain/Bulk capacitance
<i>QSRC</i>	Intrinsic Source charge
<i>CSG</i>	Intrinsic Source/Gate capacitance
<i>CSD</i>	Intrinsic Source/Drain capacitance
<i>CSS</i>	Intrinsic Source/Source capacitance
<i>CSB</i>	Intrinsic Source/Bulk capacitance
<i>QBULK</i>	Intrinsic Bulk charge
<i>CBG</i>	Intrinsic Bulk/Gate capacitance
<i>CBD</i>	Intrinsic Bulk/Drain capacitance
<i>CBS</i>	Intrinsic Bulk/Source capacitance
<i>CBB</i>	Intrinsic Bulk/Bulk capacitance
<i>QJBS</i>	Bulk/Source junction charge
<i>CJBS</i>	Bulk/Source junction capacitance
<i>QJBD</i>	Bulk/Drain junction charge
<i>CJBD</i>	Bulk/Drain junction capacitance
<i>UEFF</i>	Effective mobility
<i>VTH</i>	Threshold voltage
<i>VDSS</i>	Saturation voltage
<i>VDSAT</i>	Saturation voltage/* alias */
<i>TOTNOISE</i>	Total noise
<i>RDNOISE</i>	Noise due to resistance RD
<i>RSNOISE</i>	Noise due to resistance RS
<i>RGNOISE</i>	Noise due to resistance RG
<i>RBPSNOISE</i>	Noise due to resistance RBPS
<i>RBPDNOISE</i>	Noise due to resistance RBPS
<i>RBPBNOISE</i>	Noise due to resistance RBPB
<i>RBSBNOISE</i>	Noise due to resistance RBSB

Quantity	Description
<i>RBDBNOISE</i>	Noise due to resistance RBDB
<i>IGSNOISE</i>	Noise due to current IGS
<i>IGDNOISE</i>	Noise due to current IGD
<i>IGBNOISE</i>	Noise due to current IGB
<i>THERMNOISE</i>	Thermal noise
<i>FLKNOISE</i>	Flicker noise



The states with the “Intrinsic” description—*Qgate*, *Qdrn*, *Qsrc*, *Qbulk* and all *Cxy*—are intrinsic quantities. This means they do not include any parasitic effects such as the junction charge/capacitance or overlap charge/capacitance.

Monitored Only Under the condition of *DBXMOD=1*



DBXMOD is an instance parameter that defaults to 0.

Quantity	Description
<i>IDEDT</i>	<i>Idedtot</i>
<i>GDTOT</i>	Drain Conductance
<i>IEST</i>	<i>Iesttot</i>
<i>GSTOT</i>	Source Conductance
<i>GDTOTG</i>	<i>Gdtotg</i>
<i>GDTOTD</i>	<i>Gdtotd</i>
<i>GDTOTB</i>	<i>Gdtotb</i>
<i>GSTOTG</i>	<i>Gstotg</i>
<i>GSTOTD</i>	<i>Gstotd</i>
<i>GSTOTB</i>	<i>Gstotb</i>
<i>GCRGG</i>	<i>Gcrgg</i>
<i>GCRGD</i>	<i>Gcrgd</i>
<i>GCRGB</i>	<i>Gcrgb</i>

Chapter 23

TFT Polysilicon Model

1.0 Introduction

This is the modified polysilicon TFT model based on the original work at Rensselaer Polytechnic Institute (RPI). The TFT polysilicon model is implemented in Eldo as LEVEL=62.

The TFT model is a complete model developed for CAD and is based on the new universal charge control concept which guarantees stability and conversion. The unified DC model covers all regimes of operation and the AC model accurately reproduces frequency dispersion of capacitances (because of low mobility, carrier transit time is quiet; the signal period for even low frequency signals). This model provides automatic scaling of model parameters to accurately model a wide range of device geometries and physical based parameters can be easily extracted from experimental data. This model includes the following effects for drain current:

Kink Effect

- impact ionization with feedback

Above Threshold

- based on the crystalline MOSFET model
- field effect mobility becomes a function of gate bias
- field effect mobility accounts for trap states

Subthreshold Current

- diffusion like model:

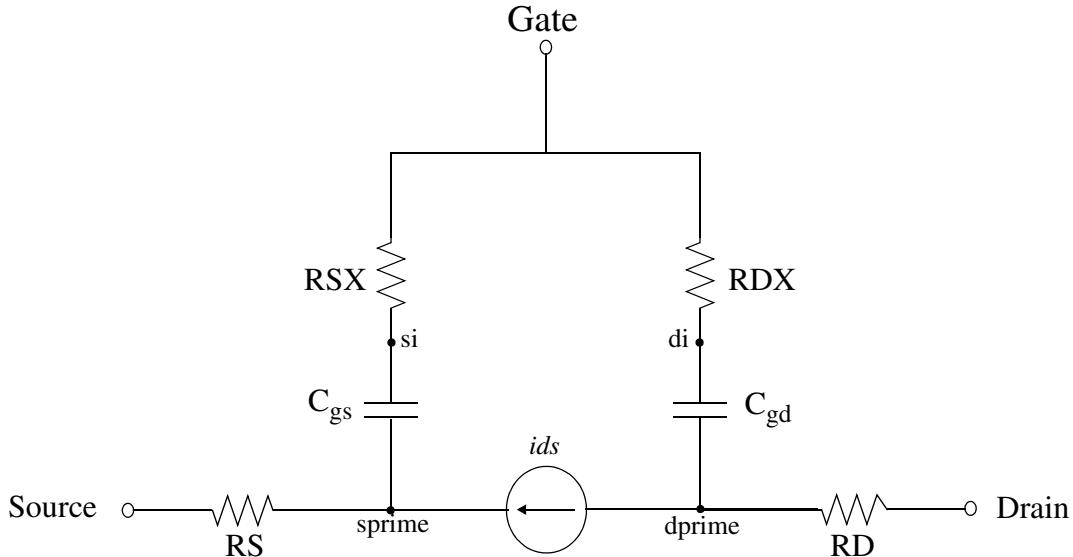
Leakage Current

- thermionic emission
- reverse bias drain current function of:
 - a. electric field near drain
 - b. temperature
- independent of channel length

Temperature Effects

- subthreshold swing
- subthreshold mobility
- threshold voltage
- field effect mobility

2.0 Model Structure



3.0 Effective Dimensions Calculation

The calculation of the effective length and width is adjusted to take the effects of etching and diffusion into account so that:

$$L_{eff} = L \cdot SCALE \cdot LMLT + XL \cdot SCALM - 2 \cdot WD \cdot SCALM$$

$$W_{eff} = W \cdot SCALE \cdot WMLT + XW \cdot SCALM - 2 \cdot WD \cdot SCALM$$

If **STANDMOD** ≠ 0:

$$W_j = W_{eff}$$

else:

$$W_j = W \cdot SCALE \cdot WMLT + XW \cdot SCALM$$

4.0 DC Current Equations

The following equations describe the drain current ids in the polysilicon TFT model. Variables in small letters are output variables.

4.1 Total Drain Current

IDSMOD: this flag determines the method used to calculate Ids .

When **IDSMOD=0:**

$$I_{ds} = \left(\frac{I_a \cdot I_{sub}}{I_a + I_{sub}} + I_{leak} \right) \cdot (1 + \Delta kink)$$

When **IDSMOD=1:**

$$I_{ds} = \left(\frac{I_a \cdot I_{sub}}{I_a + I_{sub}} \right) \cdot (1 + \Delta kink) + I_{leak}$$

4.2 Subthreshold Current

$$I_{sub} = MUS \cdot F_{cox} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{sth}^2 \cdot \exp\left(\frac{V_{gt}}{V_{sth}}\right) \cdot \left(1 - \exp\frac{vds}{V_{sth}}\right)$$

$$F_{cox} = \frac{\epsilon_{ox}}{TOX}$$

$$V_{sth} = ETA \cdot V_{th}$$

$$V_{th} = \frac{k \cdot temp}{q} \text{ (where temp is the device temperature.)}$$

$$V_{gt} = vgs - vteff$$

When $VTMOD=0$:

$$vteff = V_{tx} - \frac{AT \cdot vds^2 + BT}{Leff}$$

When $VTMOD=1$:

$$vteff = V_{tx} - \frac{AT \cdot vds^2 + BT}{Leff \cdot \left(1 + \exp\left(\frac{vgs - VST - V_{tx}}{VSI}\right)\right)}$$

4.3 Above Threshold Current

If $vds \leq vdsat$:

$$I_a = \frac{\mu_{FET} \cdot F_{cox} \cdot W_{eff}}{Leff} \left(V_{gte} \cdot vds - \frac{vds^2}{2 \cdot Tasat} \right)$$

else:

$$I_a = \frac{\mu_{FET} \cdot F_{cox} \cdot W_{eff} \cdot V_{gte}^2 \cdot Tasat}{2 \cdot Leff}$$

where:

$$\frac{1}{\mu_{FET}} = \frac{1}{MU0} + \frac{1}{Tmu1 \cdot \left(\frac{2 \cdot V_{gte}}{V_{sth}}\right)^{MMU}}$$

$$V_{gte} = V_{sth} \cdot \left[1 + \frac{V_{gt}}{2 \cdot V_{sth}} + \sqrt{DELT A^2 + \left(\frac{V_{gt}}{2 \cdot V_{sth}} - 1\right)^2} \right]$$

4.4 Kink Effect

For very large drain biases, the kink effect is observed. It is modeled as impact in a narrow region near the drain. The expression can be written as:

$$\Delta kink = A_{kinkt} \cdot (vds - V_{dsep}) \cdot \exp\left(\frac{-VKINK}{vds - V_{dsep}}\right)$$

$$A_{kinkt} = \frac{1}{VKINK} \left(\frac{LKINK}{leff} \right)^{MK}$$

$$V_{dsep} = \frac{vds}{\left(1 + \left(\frac{vds}{vdsat}\right)^3\right)^{\frac{1}{3}}} - V_{th}$$

$$vdsat = Tasat \cdot V_{gte}$$

4.5 Subthreshold Leakage Current

Subthreshold leakage current is the result of the thermionic field emission of carriers through the grain boundary trap states and is described by:

$$I_{leak} = IO \cdot Weff \cdot \left[\exp\left(\frac{q \cdot BLK \cdot vds}{k \cdot temp}\right) - 1 \right] \cdot [X_{tfe} + X_{te}] + I_{diode}$$

$$X_{te} = \frac{X_{tfe, lo} \cdot X_{tfe, hi}}{X_{tfe, lo} + X_{tfe, hi}}$$

where:

$$X_{te} = \exp(-Wc)$$

$$Wc = \frac{Ec - Et}{k \cdot temp} = \frac{0.55eV}{k \cdot temp}$$

If $Pf \leq F_{lo}$ then:

$$X_{tfe, lo} = \frac{4\sqrt{\pi}}{3} \cdot Pf \cdot \exp\left(\frac{4}{27} \cdot Pf^2 - Wc\right)$$

else:

$$X_{tfe, lo} = X_{tfe, lo} F_{lo} \cdot \exp\left[\left(\frac{8F_{lo}}{27} + \frac{1}{F_{lo}}\right) \cdot (Pf - F_{lo})\right]$$

where:

$$Pf = \frac{Fmin}{2} \left[1 + \frac{\frac{F_f}{F_{fo}}}{Fmin} + \sqrt{DELTA^2 + \left(\frac{\frac{F_f}{F_{fo}}}{Fmin} - 1\right)^2} \right]$$

$$Fmin = 1e-4$$

$$F_f = \left(\frac{vds}{DD} - \frac{vgs - VFB}{DG} \right)$$

$$F_{fo} = (k \cdot temp)^{\frac{3}{2}} \cdot \left(\frac{4}{3} \cdot \frac{2\pi \cdot \sqrt{2\pi^*}}{q \cdot h} \right)$$

$$\pi^* = 0.27 \cdot m_0$$

$$F_{lo} = \frac{3}{2} \cdot (\sqrt{Wc + 1} - 1)$$

If $Pf < F_{hi}$ then:

$$X_{tfe, hi} = \frac{2Wc}{3} \cdot \exp\left(1 - \frac{2Wc}{3}\right)$$

else:

$$X_{tfe, hi} = \left(1 - \frac{3\sqrt{Wc}}{2 \cdot Pf}\right)^{-1} \cdot \exp\left[\frac{-Wc^{\frac{2}{3}}}{Pf}\right]$$

$$F_{hi} = 3 \cdot \left(\frac{Wc^{\frac{3}{2}}}{2 \cdot Wc - 3}\right)$$

$$I_{diode} = IOO \cdot weff \cdot \exp\left(-\frac{EB}{k \cdot temp}\right) \left[-\exp\left(\frac{q \cdot vds}{k \cdot temp}\right) + 1 \right]$$

4.6 Threshold Voltage

If VTO is not specified:

$$V_t = VON - DVT$$

else:

$$V_t = VTO$$

4.7 Temperature Dependence

$$V_{tx} = TYPE \cdot V_t - DVTO \cdot (temp - TNOM)$$

$$Tmu1 = MU1 + DMU1(temp - TNOM)$$

$$Tasat = ASAT - \frac{LASAT}{Leff} - DASAT \cdot (temp - TNOM)$$

4.8 Access Resistance Calculation

ACM = 0

If ($NRS \cdot RSH > 0$)

$$Rseff = NRS \cdot RSH + RSC$$

else:

$$Rseff = RS + RSC$$

If ($NRD \cdot RSH > 0$)

$$Rdeff = NRD \cdot RSH + RDC$$

else:

$$Rdeff = RD + RDC$$

ACM = 1

$$Rseff = (LD + LDIF) \cdot SCALM / W_j \cdot RS + NRS \cdot RSH + RSC$$

$$Rdeff = (LD + LDIF) \cdot SCALM / W_j \cdot RD + NRD \cdot RSH + RDC$$

ACM = 2 or 3

If $STANDMOD \neq 0$:

$$HDIFscal = HDIF \cdot SCALM \cdot WMLT$$

else:

$$HDIFscal = HDIF \cdot SCALM$$

If NRS given then as above,

$$Rseff = (LD + LDIF) \cdot SCALM / W_j \cdot RS + NRS \cdot RSH + RSC$$

else:

$$R_{eff} = RSC + \frac{HDIFscal}{W_j} \cdot RSH + (LD + LDIF) \cdot \frac{SCALM}{W_j} \cdot RS$$

If **NRD** given then as above,

$$R_{deff} = (LD + LDIF) \cdot SCALM / W_j \cdot RD + NRD \cdot RSH + RDC$$

else:

$$R_{deff} = RDC + \frac{HDIFscal}{W_j} \cdot RSH + (LD + LDIF) \cdot \frac{SCALM}{W_j} \cdot RD$$

4.9 Frequency Dispersion

The resistances **rsx** and **rdx** are placed in a series with source and drain capacitances. **rsx** and **rdx** are defined as follows:

If (**RSX** and **RSX** ≠ 0)

$$rsx = RSX$$

else:

$$rsx = \left. \frac{Rch}{KSS} \right|_{vds} \text{ or}$$

If (**RDX** and **RDX** ≠ 0)

$$rdx = RDX$$

else:

$$rdx = \left. \frac{Rch}{KSS} \right|_{vds}$$

where:

$$\frac{1}{Rch} = \frac{\partial Ids}{\partial vds}$$

4.10 Capacitance Equations

Intrinsic Capacitances

The capacitance model is selected by using the **CAPMOD** selector. The **CAPMOD** selection affects the run time and simulation accuracy. The following TFT capacitance models are currently supported:

CAPMOD = 1	Meyer Capacitances adapted from RPI model capacitance.
CAPMOD = 0	RPI capacitance model (default).

CAPMOD = 1: Meyer Model

If (ZEROC) then $Capgs = Capgd = 0$

else:

$$V_{gst} = vgs - vteff$$

If $V_{gst} \leq -\frac{Phi}{2}$ then $Capgs = Capgd = 0$

where $\text{Phi} = 0.6$

If $-\frac{Phi}{2} \leq V_{gst} \leq 0$ then

$$Capgd = 0 \text{ and } Capgs = \frac{4 \cdot V_{gst} \cdot Cox}{3 \cdot Phi} + \frac{2 \cdot Cox}{3}$$

$$Cox = \frac{Weff \cdot Leff \cdot \epsilon_{ox}}{TOX}$$

If $V_{gst} > 0$ then

If $v_{ds} \geq v_{dsat}$ then

$$Capgd = 0 \text{ and } Capgs = \frac{2 \cdot Cox}{3}$$

else:

$$Capgd = \frac{2 \cdot Cox}{3} \cdot \left[1 - \left(\frac{v_{dsat}}{2 \cdot v_{dsat} - V_{dse}} \right)^2 \right]$$

$$Capgs = \frac{2 \cdot Cox}{3} \cdot \left[1 - \left(\frac{v_{dsat} - V_{dse}}{2 \cdot v_{dsat} - V_{dse}} \right)^2 \right]$$

CAPMOD = 0: RPI Capacitance Model

$$Capgs = Cf + \frac{2 \cdot Cgcs}{3} \cdot \left[1 - \left(\frac{v_{dsat} - V_{dse}}{2 \cdot v_{dsat} - V_{dse}} \right) \right]$$

$$Capgd = Cf + \frac{2 \cdot Cgcd}{3} \cdot \left[1 - \left(\frac{v_{dsat} - V_{dse}}{2 \cdot v_{dsat} - V_{dse}} \right) \right]$$

$$Cf = 0.5 \cdot \epsilon si \cdot Weff$$

$$Cgcd = \frac{Cox}{1 + \eta_{cd} \exp\left(-\frac{V_{gt} - v_{ds}}{\eta_{cd} \cdot V_{th}}\right)}$$

$$Cgcs = \frac{Cox}{1 + ETAC0 \cdot \exp\left(-\frac{V_{gt}}{ETAC0 \cdot V_{th}}\right)}$$

$$Cox = \frac{Weff \cdot Leff \cdot \epsilon ox}{Tox}$$

$$\eta_{cd} = ETAC0 + ETAC00 \cdot V_{dse}$$

$$V_{dse} = \frac{vds}{\left(1 + \left(\frac{vds}{vdsat}\right)^{MC}\right)^{\frac{1}{MC}}}$$

The Overlap Capacitance Calculation

$$W = W \cdot SCALE \cdot WMLT + XW \cdot SCALM$$

If **CGSO** is given, then:

$$\text{GateSourceOVERLAP CAP} = W \cdot \frac{CGSO}{SCALM}$$

else:

$$\text{GateSourceOVERLAP CAP} = W \cdot (LD + METO) \cdot \frac{COX}{SCALM}$$

If **CGDO** is given, then:

$$\text{GateDrainOVERLAP CAP} = W \cdot \frac{CGDO}{SCALM}$$

else:

$$\text{GateDrainOVERLAP CAP} = W \cdot (LD + METO) \cdot \frac{COX}{SCALM}$$

5.0 Model Parameters

Nr.	Name	Description	Default	Units
1	ASAT (ALPHASAT)	Proportionality constant of V_{dsat}	1.0	
2	AT	$DIBL$ parameter 1	3e-8	m/V
3	BLK	Leakage barrier lowering constant	1e-3	MV
4	BT	$DIBL$ parameter 2	1.9e-6	MV
5	CAPMOD	Model capacitance selector	0	
6	DASAT	Temperature coefficient of ASAT	0	1°C
7	DD^a	V_{ds} field constant	0 ^b	m
8	DELTA	Transition width parameter	4.0	
9	DG^a	V_{gs} field constant	0 ^c	m
10	DMU1	Temperature coefficient of MU1	0	cm ² /(Vs°C)
11	DVT (DVON)	The difference between V_{ON} and the threshold voltage	0	V
12	DVT0	Temperature coefficient of $VT0$	0	cm ² /(Vs°C)
13	EB	Barrier height of diode	0.68	eV
14	ETA (ETAI)	Subthreshold ideality factor	7	
15	ETAC0	Capacitance subthreshold ideality factor at zero drain bias	ETA	
16	ETAC00	Capacitance subthreshold coefficient of drain bias	0	1/V
17	I0 (CLK)	Leakage scaling constant	6.0	A/m
18	I00	Reverse diode saturation constant	150.0	A/m
19	KSS	Small signal constant similar to Elmore constant in BSIM3v3 (used when RSX and RDX =0)	0	
20	LASAT	Coefficient for length dependence of ASAT	0	m
21	LKINK	Kink effect constant	19e-6	m
22	MC	Capacitance knee shape parameter	3.0	
23	MK (MKINK)	Kink effect exponent	1.3	
24	M (MMU)	Low field mobility exponent	1.7	
25	MU0	High field mobility	100	cm ² /(Vs)
26	MU1	Low field mobility parameter	0.0022	cm ² /(Vs)
27	MUS	Subthreshold mobility	1.0	cm ² /(Vs)
28	RDX (RF)	Resistance in series with Cap_{gd}	0	Ω
29	RSX (RI)	Resistance in series with Cap_{gs}	0	Ω

Nr.	Name	Description	Default	Units
30	TOX	Thin-oxide thickness	1.0e-7	m
31	VFB	Flat band voltage	-0.1 (n) 0.1 (p)	v
32	VKINK	Kink effect voltage	9.1	v
33	VON	On-voltage	0	v
34	VSI	First parameter for v_{gs} dependence	2.0	v
35	VST	Second parameter for v_{gs} dependence	2.0	v
36	VTO	Zero-Bias threshold voltage	VON-DVT	v
37	ZEROC	Allow non-calculations of capacitor (only available for Meyer modified model: CAPMOD=1)	0	
38	RD	Series drain access resistor	0	Ω
39	RS	Series source access resistor	0	Ω
40	CGSO	Gate - Source overlap capacitance per meter channel width	0	F/m
41	CGDO	Gate - Drain overlap capacitance per meter channel	0	F/m
42	AD (1)	V_{ds} field constant	1/1400e-10	1/m
43	AG (1)	V_{gs} field constant	1/2000e-10	1/m
44	RSH	Drain and source diffusion sheet	0	Ω/m^2
45	VTMOD	Flag to determine the VTEFF calculation method	1	
46	EXPLIM^d		1	
47	VDSLIM^e		1	
48	IDSMOD	Flag to determine the I_{ds} calculation method	1	
49	STANDMOD	Flag to control default values for parameters DD , DG , and XJ , and control access resistance calculations.	0	

- a. **DD** has priority over **AD**. If **DD** is given then $AD=1/DD$
- b. **DG** has priority over **AG**. If **DG** is given then $AG=1/DG$
- c. The default value of **DD** is 1.4e-7 if **STANDMOD=1**.
- d. The default value of **DG** is 2.0e-7 if **STANDMOD=1**.
- e. Allows user to limit the exponential functions in order to avoid FPE. May result in some loss of accuracy in the case of high voltages.
- f. Allows the user to limit the internal drain source voltage during iterations to avoid convergence or FPE problems. Sometimes voltage limiting can increase the simulation time.

5.1 Parasitic Parameters (Access Resistance and Overlap Capacitance Parameters)

Nr.	Name	Description	Default	Units
1	ACM	Area Calculation Method	0	
2	RDC	Additional drain resistance due to contact resistance	0	
3	RSC	Additional source resistance due to contact resistance	0	
4	HDIF	Length of heavily doped diffusion from contact to lightly doped region	0	$HDIF \times SCALM$
5	LD	Lateral diffusion into channel from source and drain diffusion	$0.75 \times XJ$	$LD \times SCALM$
6	LDIF	Length of lightly doped diffusion adjacent to gate	0	$LDIF \times SCALM$
7	WMLT	Width diffusion layer shrink reduction factor	1	
8	XJ	Metallurgical junction depth	$1.5e-7^a$	
9	SCALM	Scale factor for model parameters	1	
10	METO	Fringing field factor for gate to source and gate to drain overlap capacitance	0	$METO \times SCALM$
11	WD	Lateral diffusion into channel from bulk along width	0	$WD \times SCALM$
12	COX	Oxide capacitance	1	$COX / SCALM^2$
13	LMLT	Length shrink factor	0	
14	XW	Accounts for masking and etching effects in W_{eff} calculation	0	$XW \times SCALM$
15	XL	Accounts for masking and etching effects in L_{eff} calculation	0	$XL \times SCALM$

a. The default value of **XJ** is 0.0 if **STANDMOD**=1.



Instance parameters used are the same as those normally used for all mosfet transistors with one remark:

RSC & RDC are instant parameters and model card parameters.

RSC & RDC specified as instant parameters have HIGHER PRIORITY than the model card parameters.

If not specified then they are initialized with the same value as the MODEL CARD parameter and not with ZERO!

5.2 Printing and Plotting Output States

States can be printed or plotted. As this is a Gudm model, you can print/plot states in the following manner:

```
.PRINT/PLOT <ANALYSIS_TYPE> S (Mname->state)
```

for example:

```
.PRINT DC S (M1->Ids)
```

The states and descriptions are listed below:

Static states

Quantity	Description
<i>Ids</i>	Channel current flowing between dprime and sprime
<i>Gds</i>	dI_{ds}/dV_{ds} ($V_{ds}=V(dprime)-V(sprime)$)
<i>Gm</i>	dI_{ds}/dV_{gs} ($V_{gs}=V(g)-V(sprime)$)
<i>Igs</i>	Gate current component flowing in RSX between Gate and si (middle node connecting the capacitor and resistance in the gate sprime branch)
<i>Gsx/Gi</i>	dI_{gs}/dV_{gsi} ($V_{gsi}=V(g)-V(si)$)
<i>dgdsdvgs0</i>	dI_{gs}/dV_{gs} ($V_{gs}=V(g)-V(sprime)$) at $V_{ds}=0$
<i>Igd</i>	Gate current component flowing in RDX between Gate and di (middle node connecting the capacitor and resistance in the gate dprime branch)
<i>Gdx/Gf</i>	dI_{gd}/dV_{gdi} ($V_{gdi}=V(g)-V(di)$)
<i>dgdsdvgs</i>	dI_{gd}/dV_{gs} ($V_{gs}=V(g)-V(sprime)$)
<i>dgdsdvds</i>	dI_{gd}/dV_{ds} ($V_{gs}=V(dprime)-V(sprime)$)
<i>Iddp</i>	Current flowing in drain access resistance
<i>Gd</i>	dI_{ddp}/dV_{ddp} ($V_{ddp}=V(d)-V(dprime)$)
<i>Issp</i>	Current flowing in source access resistance
<i>Gs</i>	dI_{ssp}/dV_{ssp} ($V_{ssp}=V(s)-V(sprime)$)

Dynamic states

Quantity	Description
<i>Qgs/Qgsav</i>	Charge stored in capacitance between si and sprime
<i>Cgsav</i>	dQ_{gs}/dV_{sisp} ($V_{sisp}=V(si)-V(sprime)$)

Quantity	Description
C_{gs}	Instantaneous gate source capacitance
Q_{gd}/Q_{gdav}	Charge stored in capacitance between di and dprime
C_{gdav}	dQ_{gd}/dV_{didp} ($V_{didp}=V(di)-V(dprime)$)
C_{gd}	Instantaneous gate drain capacitance

6.0 References

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Chapter 24

MOS Model 11 Equations

1.0 Introduction

A new compact model for MOS transistors has been developed. Philips MOS Model 11 (MM11), the successor of Philips MOS Model 9, MM11 not only gives an accurate description of charges and currents and their first-order derivatives (transconductance, conductance, capacitances), but also of their higher-order derivatives. In other words it gives an accurate description of MOSFET distortion behavior, and as such MM11 is suitable for digital, analog as well as RF circuit design.

MOS Model 11 is a symmetrical, surface-potential-based model. It includes an accurate description of all physical effects important for modern and future CMOS technologies, such as, for example, gate tunnelling current, influence of pocket implants, poly-depletion, quantum-mechanical effects and bias-dependent overlap capacitances.

There are two versions of this model: Level 1100 and Level 1101. This chapter is divided into two sections accordingly.



- [MOS Model 11 Level 1100 Equations](#)
- [MOS Model 11 Level 1101 Equations](#)

Documentation



User's can access the full documentation of the Philips MOS Model 11 (MM11) by visiting the web site for further information:
http://www.semiconductors.philips.com/Philips_Models/mos_models/model11/index.html

2.0 MOS Model 11 Level 1101 Equations

The MM11 model (Level 1101) is implemented in Eldo as LEVEL=63.

Level 1101 is an updated version of Level 1100. It uses the same basic equations as Level 1100, but uses different geometry scaling rules. It includes two types of geometrical scaling rules: physical rules and binning rules. Moreover, the temperature scaling has been implemented on the “miniset” level instead of the “maxiset” level as was the case for Level 1100.



For information on the MM11 model (Level 1100), see [MOS Model 11 Level 1100 Equations](#).

History of Model

A first test version of the compact MOS model, MOS MODEL 11, Level 1101, has been put in the public domain in December 2001. Future changes and additions to the model will be documented by extending or changing the documentation in the Philips unclassified report.

A first test version of the compact MOS model, MOS MODEL 11, has been put in the public domain in April 2001. Future changes and additions to the model will be documented by extending or changing the documentation in the Philips unclassified report.

December 2001 Release of MOS MODEL 11, level 1101, test version

June 2002 Release of MOS MODEL 11, level 1101
Errors corrected in model implementation:

- A new variable ξ_{ox} has been added, see eqs. (2.50) and (6.36), in order to improve the charge description. In the previous version of MOS MODEL 11, level 1101, it was assumed that $\xi_{ox} = \xi$, which is not accurate for large values of body factor k_0

- A more accurate description of total gate charge Q_G and bulk charge Q_B has been implemented, see eqs. (2.109), (2.110), (6.101) and (6.102)
- Thermal noise density S_{th} should be larger than or equal to zero for all possible parameter values, see Section 6.1 and eq. (6.106)
- Physical geometry scaling rule of parameter m_0 , see eq. (5.21), has been improved introducing one physical geometry scaling parameter m_{00} , see Sections 3.4.1, 8.3.1 and 8.3.2
- Upper clipping limit of physical geometry scaling parameter L_{min} has been changed to 2.5×10^{-6} m, see Sections 8.3.1 and 8.3.2, in order to prevent problems in scaling relation (5.23)

December 2002

Update of MOS MODEL 11, level 1101

Error corrected in model implementation:

- In the model expressions, source and drain are internally interchanged for $V_{DS} < 0$, see Fig. 4.1. Overlap capacitance parameters $CGDO$ and $CGSO$, however, should still be assigned to the external drain and source, respectively. This was not the case in the previous release of the model, but the error has been corrected in this update, see Fig. 4.1. Note that this does not affect the model behaviour for normal MOSFETs where $CGDO = CGSO$, but it may be of influence when MOS MODEL 11 is used in a DMOS transistor model where $CGDO \neq CGSO$.

Gate-induced drain leakage (GIDL) has been included in the model. The GIDL-model is backward compatible, i.e., the GIDL current is zero by default. The following has been added:

- Physical model eqs. (2.98)-(2.101) and resulting implemented model eqs. (6.90)-(6.93)
- Embedding of I_{GIDL} and I_{GISL} in Fig. 4.1
- Miniset parameters in Sections 2.1.1, 8.2.1 and 8.2.2: A_{GIDL} , B_{GIDL} , $S_{T;BGIDL}$, C_{GIDL}

- Physical geometrical scaling parameters in Section 3.4.1, 8.3.1 and 8.3.2: A_{GIDL} , B_{GIDL} , $S_{T;BGIDL}$, C_{GIDL}
- Binning geometrical scaling parameters in Sections 3.4.2, 8.4.1 and 8.4.2: $P_{0;AGIDL}$, $P_{L;AGIDL}$, $P_{W;AGIDL}$, $P_{LW;AGIDL}$, $P_{0;BGIDL}$, $P_{L;BGIDL}$, $P_{W;BGIDL}$, $P_{LW;BGIDL}$, $P_{0;CGIDL}$, $P_{L;CGIDL}$, $P_{W;CGIDL}$, $P_{LW;CGIDL}$, $P_{0;T;BGIDL}$, $P_{L;T;BGIDL}$, $P_{W;T;BGIDL}$, $P_{LW;T;BGIDL}$
- Temperature scaling relation (5.96)
- Physical geometrical scaling relation (5.30)
- Binning geometrical scaling relations (5.62), (5.63), (5.64) and (5.81)

2.1 MM 11 (1101) Model Parameters

MM11 (1101(0)) Parameters

MM11 Level 1101(0) is specified with **BINNING=0.0** (Physical rule).

Nr.	Name	Default		Clipping		Units
		N-type	P-type	Low	High	
1	LVAR	0	0	-	-	m
2	LAP	4×10^{-8}	4×10^{-8}	-	-	m
3	WVAR	0	0	-	-	m
4	WOT	0	0	-	-	m
5	TR	27.0	27.0	-273.15	-	°C
6	VFB	-1.05	-1.05	-	-	V
7	STVFB	0.50×10^{-3}	0.50×10^{-3}	-	-	VK ⁻¹
8	KOR	0.5	0.5	-	-	V ^{1/2}
9	SLKO	0	0	-	-	-
10	SL2KO	0	0	-	-	-
11	SWKO	0	0	-	-	-
12	KPINV	0	0	-	-	V ^{-1/2}
13	PHIBR	0.95	0.95	-	-	V

Nr.	Name	Default		Clipping		Units
		N-type	P-type	Low	High	
14	STPHIB	-8.5×10^{-4}	-8.5×10^{-4}	-	-	VK^{-2}
15	SLPHIB	0	0	-	-	-
16	SL2PHIB	0	0	-	-	-
17	SWPHIB	0	0	-	-	-
18	BETSQ	3.709×10^{-4}	1.15×10^{-4}	-	-	AV^{-2}
19	SLETABET	0	0	-	-	-
20	ETABETR	1.3	0.5	-	-	-
21	FBET1	0	0	-	-	-
22	LP1	0.8×10^{-6}	0.8×10^{-6}	1.0×10^{-10}	-	m
23	FBET2	0	0	-	-	-
24	LP2	0.8×10^{-6}	0.8×10^{-6}	1.0×10^{-10}	-	m
25	THESRR	0.4	0.73	-	-	V^{-1}
26	ETASR	0.65	0.5	-	-	-
27	SWTHESR	0	0	-	-	-
28	THEPHR	1.29×10^{-2}	1.00×10^{-3}	-	-	V^{-1}
29	ETAPH	1.35	3.75	-	-	-
30	SWTHEPH	0	0	-	-	m
31	ETAMOBR	1.4	3	-	-	-
32	STETAMOB	0	0	-	-	K^{-1}
33	SWETAMOB	0	0	-	-	-
34	NU	2	2	1	-	-
35	NUEXP	5.25	3.23	-	-	-
36	THERR	0.155	0.08	1.0×10^{-10}	-	V^{-1}
37	ETAR	0.95	0.4	-	-	-
38	SWTHER	0	0	-	-	m
39	THER1	0	0	-	-	V
40	THER2	1	1	-	-	V
41	THESATR	0.5	0.2	-	-	V^{-1}
42	ETASAT	1.04	0.86	-	-	-
43	SLTHESAT	1	1	-	-	-
44	THESATEXP	1	1	0	-	-
45	SWTHESAT	0	0	-	-	m
46	THETHR	1×10^{-3}	0.5×10^{-3}	-	-	V^{-3}

Nr.	Name	Default		Clipping		Units
		N-type	P-type	Low	High	
47	THETHEXP	1	1	0	-	-
48	SWTHETH	0	0	-	-	m
49	SDIBLO	1×10^{-4}	1×10^{-4}	-	-	$V^{-1/2}$
50	SDIBLEXP	1.35	1.35	-	-	-
51	MOR	0	0	-	-	-
52	MOEXP	1.34	1.34	-	-	-
53	SSFR	6.25×10^{-3}	6.25×10^{-3}	-	-	$V^{-1/2}$
54	SLSSF	1	1	-	-	m
55	SWSSF	0	0	-	-	m
56	ALPR	0.01	0.01	-	-	-
57	SLALP	1	1	-	-	-
58	ALPEXP	1	1	0	-	-
59	SWALP	0	0	-	-	m
60	VP	0.05	0.05	-	-	V
61	LMINT ^a	0.15×10^{-6}	0.15×10^{-6}	1×10^{-10}	-	m
62	A1R	6	6	-	-	-
63	STA1	0	0	-	-	$^{\circ}K^{-1}$
64	SLA1	0	0	-	-	-
65	SWA1	0	0	-	-	-
66	A2R	38	38	-	-	V
67	SLA2	0	0	-	-	-
68	SWA2	0	0	-	-	-
69	A3R	1	1	-	-	-
70	SLA3	0	0	-	-	-
71	SWA3	0	0	-	-	-
72	IGINVR	0	0	-	-	AV^2
73	BINV	48	87.5	-	-	V
74	IGACCR	0	0	-	-	AV^2
75	BACC	48	48	-	-	V
76	VFB0V	0	0	-	-	V
77	KOV	2.5	2.5	1×10^{-12}	-	$V^{1/2}$
78	IGOVR	0	0	0	-	AV^2

Nr.	Name	Default		Clipping		Units
		N-type	P-type	Low	High	
79	TOX	3.2×10^{-9}	3.2×10^{-9}	1×10^{-12}	-	m
80	COL	0.32×10^{-9}	3.2×10^{-16}	-	-	F
81	GATENOISE	0	0	0	1	-
82	NT	1.656×10^{-20}	1.656×10^{-20}	0	-	J
83	NFAR	1.573×10^{23}	3.825×10^{24}	-	-	$V^{-1}m^{-4}$
84	NFBR	4.752×10^9	1.015×10^9	-	-	$V^{-1}m^{-2}$
85	NFCR	0	7.3×10^{-8}	-	-	V^{-1}

a. The model parameter LMIN in Philips documentation is modified to LMINT in Eldo to avoid any conflict between this parameter and the model parameters LMIN, LMAX, WMIN, and WMAX which are responsible for the specification of bin corners in Binned model cards in Eldo.



The parameters L , W and DTA are used to calculate the electrical parameters of the actual transistor as specified in the section on parameter preprocessing.



For the case of parameters L and W in Philips documentation, they are treated as device parameters in Eldo. Similarly, $MULT$ is equivalent to the **M** device parameter in Eldo. The DTA parameter in Philips documentation is equivalent to **DTEMP** in Eldo.

MM11 (1101(1)) Parameters

MM11 Level 1101(1) is specified with **BINNING=1.0** (Binning rule).

Nr.	Name	Default		Clipping		Units
		N-type	P-type	Low	High	
1	LVAR	0	0	-	-	m
2	LAP	4×10^{-8}	4×10^{-8}	-	-	m
3	WVAR	0	0	-	-	m
4	WOT	0	0	-	-	m
5	TR	27.0	27.0	-273.15	-	°C
6	VFB	-1.05	-1.05	-	-	V
7	POKO	0.5	0.5	-	-	$V^{1/2}$

Nr.	Name	Default		Clipping		Units
		N-type	P-type	Low	High	
8	PLKO	0	0	-	-	V ^{1/2}
9	PWKO	0	0	-	-	V ^{1/2}
10	PLWKO	0	0	-	-	V ^{1/2}
11	KPINV	0	0	-	-	V ^{-1/2}
12	POPHIB	0.95	0.95	-	-	V
13	PLPHIB	0	0	-	-	V
14	PWPHEB	0	0	-	-	V
15	PLWPHIB	0	0	-	-	V
16	POBET	1.922×10 ⁻³	3.814×10 ⁻⁴	-	-	AV ⁻²
17	PLBET	0	0	-	-	AV ⁻²
18	PWBET	0	0	-	-	AV ⁻²
19	PLWBET	0	0	-	-	AV ⁻²
20	POTHESR	0.3562	0.73	-	-	V ⁻¹
21	PLTHESR	0	0	-	-	V ⁻¹
22	PWTHERSR	0	0	-	-	V ⁻¹
23	PLWTHESR	0	0	-	-	V ⁻¹
24	POTHEPH	1.29×10 ⁻²	1×10 ⁻³	-	-	V ⁻¹
25	PLTHEPH	0	0	-	-	V ⁻¹
26	PWTHEPH	0	0	-	-	V ⁻¹
27	PLWTHEPH	0	0	-	-	V ⁻¹
28	POETAMOB	1.4	3	-	-	-
29	PLETAMOB	0	0	-	-	-
30	PWETAMOB	0	0	-	-	-
31	PLWETAMOB	0	0	-	-	-
32	POTHER	8.12×10 ⁻²	7.9×10 ⁻²	-	-	V ⁻¹
33	PLTHER	0	0	-	-	V ⁻¹
34	PWTHER	0	0	-	-	V ⁻¹
35	PLWTHER	0	0	-	-	V ⁻¹
36	THER1	0	0	-	-	V
37	THER2	1	1	-	-	V
38	POTHESAT	2.513×10 ⁻¹	1.728×10 ⁻¹	-	-	V ⁻¹
39	PLTHESAT	0	0	-	-	V ⁻¹

Nr.	Name	Default		Clipping		Units
		N-type	P-type	Low	High	
40	PWTHESAT	0	0	-	-	V ⁻¹
41	PLWTHESAT	0	0	-	-	V ⁻¹
42	POTHETH	1.0×10 ⁻⁵	0	-	-	V ⁻³
43	PLTHETH	0	0	-	-	V ⁻³
44	PWTHETH	0	0	-	-	V ⁻³
45	PLWTHETH	0	0	-	-	V ⁻³
46	POSDIBL	8.53×10 ⁻⁴	3.551×10 ⁻⁵	-	-	V ^{-1/2}
47	PLSDIBL	0	0	-	-	V ^{-1/2}
48	PWSDIBL	0	0	-	-	V ^{-1/2}
49	PLWSDIBL	0	0	-	-	V ^{-1/2}
50	POMO	0	0	-	-	-
51	PLMO	0	0	-	-	-
52	PWMO	0	0	-	-	-
53	PLWMO	0	0	-	-	-
54	POSSF	0.012	0.01	-	-	V ^{-1/2}
55	PLSSF	0	0	-	-	V ^{-1/2}
56	PWSSF	0	0	-	-	V ^{-1/2}
57	PLWSSF	0	0	-	-	V ^{-1/2}
58	POALP	2.5×10 ⁻²	2.5×10 ⁻²	-	-	-
59	PLALP	0	0	-	-	-
60	PWALP	0	0	-	-	-
61	PLWALP	0	0	-	-	-
62	VP	5×10 ⁻²	5×10 ⁻²	-	-	V
63	POMEXP	0.2	0.2	-	-	-
64	PLMEXP	0	0	-	-	-
65	PWMEXP	0	0	-	-	-
66	PLWMEXP	0	0	-	-	-
67	POA1	6.022	6.858	-	-	-
68	PLA1	0	0	-	-	-
69	PWA1	0	0	-	-	-
70	PLWA1	0	0	-	-	-
71	POA2	38.02	57.32	-	-	V

Nr.	Name	Default		Clipping		Units
		N-type	P-type	Low	High	
72	PLA2	0	0	-	-	V
73	PWA2	0	0	-	-	V
74	PLWA2	0	0	-	-	V
75	POA3	6.407×10^{-1}	4.254×10^{-1}	-	-	-
76	PLA3	0	0	-	-	-
77	PWA3	0	0	-	-	-
78	PLWA3	0	0	-	-	-
79	POIGINV	0	0	-	-	AV^2
80	PLIGINV	0	0	-	-	AV^2
81	PWIGINV	0	0	-	-	AV^2
82	PLWIGINV	0	0	-	-	AV^2
83	POBINV	48	48	-	-	V
84	PLBINV	0	0	-	-	V
85	PWBINV	0	0	-	-	V
86	PLWBINV	0	0	-	-	V
87	POIGACC	0	0	-	-	AV^2
88	PLIGACC	0	0	-	-	AV^2
89	PWIGACC	0	0	-	-	AV^2
90	PLWIGACC	0	0	-	-	AV^2
91	POBACC	48.0	87.50	-	-	V
92	PLBACC	0	0	-	-	V
93	PWBACC	0	0	-	-	V
94	PLWBACC	0	0	-	-	V
95	VFB0V	0	0	-	-	V
96	KOV	2.5	2.5	1×10^{-12}	-	$V^{1/2}$
97	POIGOV	0	0	-	-	AV^2
98	PLIGOV	0	0	-	-	AV^2
99	PWIGOV	0	0	-	-	AV^2
100	PLWIGOV	0	0	-	-	AV^2
101	TOX	3.2×10^{-9}	3.2×10^{-9}	1×10^{-12}	-	m
102	POCOX	2.98×10^{-14}	2.717×10^{-14}	-	-	F
103	PLCOX	0	0	-	-	F

Nr.	Name	Default		Clipping		Units
		N-type	P-type	Low	High	
104	PWCOX	0	0	-	-	F
105	PLWCOX	0	0	-	-	F
106	POCGDO	6.392×10^{-15}	6.358×10^{-15}	-	-	F
107	PLCGDO	0	0	-	-	F
108	PWCGDO	0	0	-	-	F
109	PLWCGDO	0	0	-	-	F
110	POCGSO	6.392×10^{-15}	6.358×10^{-15}	-	-	F
111	PLCGSO	0	0	-	-	F
112	PWCGSO	0	0	-	-	F
113	PLWCGSO	0	0	-	-	F
114	GATENOISE	0	0	0	1	-
115	NT	1.656×10^{-20}	1.656×10^{-20}	0	-	J
116	PONFA	8.323×10^{22}	1.900×10^{22}	-	-	$V^1 m^{-4}$
117	PLNFA	0	0	-	-	$V^1 m^{-4}$
118	PWNFA	0	0	-	-	$V^1 m^{-4}$
119	PLWNFA	0	0	-	-	$V^1 m^{-4}$
120	PONFB	2.514×10^7	5.043×10^6	-	-	$V^1 m^{-2}$
121	PLNFB	0	0	-	-	$V^1 m^{-2}$
122	PWNFB	0	0	-	-	$V^1 m^{-2}$
123	PLWNFB	0	0	-	-	$V^1 m^{-2}$
124	PONFC	0	3.627×10^{-10}	-	-	V^1
125	PLNFC	0	0	-	-	V^1
126	PWNFC	0	0	-	-	V^1
127	PLWNFC	0	0	-	-	V^1
128	POTVFB	0.5×10^{-3}	0.5×10^{-3}	-	-	VK^{-1}
129	PLTVFB	0	0	-	-	VK^{-1}
130	PWTVF	0	0	-	-	VK^{-1}
131	PLWTVFB	0	0	-	-	VK^{-1}
132	POTPHIB	-8.5×10^{-4}	-8.5×10^{-4}	-	-	VK^{-1}
133	PLTPHIB	0	0	-	-	VK^{-1}
134	PWTPHIB	0	0	-	-	VK^{-1}
135	PLWTPHIB	0	0	-	-	VK^{-1}

Nr.	Name	Default		Clipping		Units
		N-type	P-type	Low	High	
136	POTETABET	1.3	0.5	-	-	-
137	PLTETABET	0	0	-	-	-
138	PWTETABET	0	0	-	-	-
139	PLWETABET	0	0	-	-	-
140	POTETASR	0.65	0.5	-	-	-
141	PLTETASR	0	0	-	-	-
142	PWTETASR	0	0	-	-	-
143	PLWETASR	0	0	-	-	-
144	POTETAPH	1.35	3.750	-	-	-
145	PLTETAPH	0	0	-	-	-
146	PWTETAPH	0	0	-	-	-
147	PLWETAPH	0	0	-	-	-
148	POTETAMOB	0	0	-	-	K^{-1}
149	PLTETAMOB	0	0	-	-	K^{-1}
150	PWTETAMOB	0	0	-	-	K^{-1}
151	PLWETETAMOB	0	0	-	-	K^{-1}
152	NU	2	2	-	-	-
153	POTNUEXP	5.25	3.23	-	-	-
154	PLTNUEXP	0	0	-	-	-
155	PWTNUEXP	0	0	-	-	-
156	PLWTNUEXP	0	0	-	-	-
157	POTETAR	0.95	0.4	-	-	-
158	PLTETAR	0	0	-	-	-
159	PWTETAR	0	0	-	-	-
160	PLWETETAR	0	0	-	-	-
161	POTETASAT	1.04	0.86	-	-	-
162	PLTETASAT	0	0	-	-	-
163	PWTETASAT	0	0	-	-	-
164	PLWETETASAT	0	0	-	-	-
165	POTA1	0	0	-	-	K^{-1}
166	PLTA1	0	0	-	-	K^{-1}
167	PWTA1	0	0	-	-	K^{-1}

Nr.	Name	Default		Clipping		Units
		N-type	P-type	Low	High	
168	PLWTA1	0	0	-	-	K ⁻¹



The parameters L , W and DTA are used to calculate the electrical parameters of the actual transistor as specified in the section on parameter preprocessing.



For the case of parameters L and W in Philips documentation, they are treated as device parameters in Eldo. Similarly, $MULT$ is equivalent to the **M** device parameter in Eldo. The DTA parameter in Philips documentation is equivalent to **DTEMP** in Eldo.

2.2 DC operating points

The following is a list of the DC operating points that are printed in the *.chi* file in OP and AC analysis.



The last three DC operating points can only appear in a Noise analysis.



For all C_{xy} below, it indicates the derivative of the charge Q at the terminal x to the voltage at terminal y , when all other terminals remain constant

DC operating point	Description
IDS	Channel current,excluding avalanche and tunnel currents
IVAL	substrate current due to Weak avalanche current
IGS	Gate to Source current due to direct tunneling
IGD	Gate to Drain current due to direct tunneling
IGB	Gate to Bulk current due to direct tunneling
VDS	Drain-source voltage
VGS	Gate-source voltage
VSB	Source-bulk voltage

DC operating point	Description
VTO	Zero-bias threshold voltage
VTS	Threshold voltage including back-bias effects
VTH	Threshold voltage including back-bias and drain-bias effects
VGT	Effective gate derive voltage including back-bias and drain-bias effects
VDSS	Drain saturation voltage at actual bias
VSAT	Saturation limit
GM	Channel transconductance dIds/dVgs (assumed VDS > 0)
GMB	Substrate-transconductance dIds/dVbs
GDS	Output conductance dIds/dVds
Qd	Intrinsic Drain charge
Qs	Intrinsic Source charge
Qb	Intrinsic Bulk charge
Qg	Intrinsic Gate charge
CGDOL	Gate-drain overlap capacitance of the actual transistor
CGSOL	Gate-source overlap capacitance of the actual transistor
WEFF	Effective channel width for the geometrical models
LEFF	Effective channel length for the geometrical models
U	Transistor gain
ROUT	Small-signal output resistance
VEARLY	Equivalent Early voltage
KEFF	Body effect parameter
BEFF	Gain factor
FUG	Unity gain frequency at actual bias
CDD	
CDG	
CDS	
CDB	
CGD	
CGG	
CGS	
CGB	
CSD	
CSG	
CSS	
CSB	

DC operating point	Description
CBD	
CBG	
CBS	
CBB	
SQRTSFW	Input-referred RMS white noise voltage density
SQRTSFF	Input-referred RMS white noise voltage density at 1 KHz
FKNEE	Cross-over frequency above which white noise is dominant

Printing or plotting a state from the MM11 States structure

If a state from the list below is to be monitored by the user, the user has to type in the netlist for a given transistor M1 to monitor, for example Gm:

- .PLOT DC S(M1->Gm) for DC or
- .PLOT AC S(M1->Gm) for AC or
- .PLOT TRAN S(M1->Gm) for TRAN

The same is applied to the following list of states.



Note For all C_{xy} below, it indicates the derivative of the charge Q at the terminal x to the voltage at terminal y , when all other terminals remain constant.

DC operating point	Description
IDS	Channel current, excluding avalanche and tunnel currents
IGS	Gate to Source current due to direct tunneling
IGD	Gate to Drain current due to direct tunneling
IGB	Gate to Bulk current due to direct tunneling
VDS	Drain-source voltage
VGS	Gate-source voltage
VSB	Source-bulk voltage
VTO	Zero-bias threshold voltage
VTS	Threshold voltage including back-bias effects
VTH	Threshold voltage including back-bias and drain-bias effects
VGT	Effective gate derive voltage including back-bias and drain-bias effects
VDSS	Drain saturation voltage at actual bias

DC operating point	Description
VSAT	Saturation limit
GM	Channel transconductance dIds/dVgs (assumed VDS > 0)
GMB	Substrate-transconductance dIds/dVbs
GDS	Output conductance dIds/dVds
Qd	Intrinsic Drain charge
Qs	Intrinsic Source charge
Qb	Intrinsic Bulk charge
Qg	Intrinsic Gate charge
CGDOL	Gate-drain overlap capacitance of the actual transistor
CGSOL	Gate-source overlap capacitance of the actual transistor
WEFF	Effective channel width for the geometrical models
LEFF	Effective channel length for the geometrical models
U	Transistor gain
ROUT	Small-signal output resistance
VEARLY	Equivalent Early voltage
KEFF	Body effect parameter
BEFF	Gain factor
FUG	Unity gain frequency at actual bias
CDD	
CDG	
CDS	
CDB	
CGD	
CGG	
CGS	
CGB	
CSD	
CSG	
CSS	
CSB	
CBD	
CBG	
CBS	
CBB	

3.0 MOS Model 11 Level 1100 Equations

The MM11 model (Level 1100) is implemented in Eldo as LEVEL=65.



For information on the MM11 model (Level 1101), see [MOS Model 11 Level 1101 Equations](#).

History of Model

A first test version of the compact MOS model, MOS MODEL 11, has been put in the public domain in April 2001. Future changes and additions to the model will be documented by extending or changing the documentation in the Philips unclassified report.

April 2001	Release of MOS MODEL 11, level 1100, test version
December 2001	Release of MOS MODEL 11, level 1100 Error corrected in model implementation: Internal parameter V_{limit} changed from $5\phi_T$ to $4\phi_T$.

3.1 MM 11 (1100) Model Parameters

Nr.	Name	Description	Default		Units
			N-type	P-type	
1	LEVEL	Eldo model selector	65	65	-
2	LER	Effective channel length of the reference transistor	1.0×10^{-6}	1.0×10^{-6}	m
3	WER	Effective channel width of the reference transistor	10×10^{-6}	10×10^{-6}	m
4	LVAR	Difference between the actual and the programmed poly-silicon gate length	0	0	m
5	LAP	Effective channel length reduction per side due to the lateral diffusion of the source/drain dopant ions	0.04×10^{-6}	0.04×10^{-6}	m

Nr.	Name	Description	Default		Units
			N-type	P-type	
6	WVAR	Difference between the actual and the programmed field-oxide opening.	0	0	m
7	WOT	Effective reduction of the channel width per side due to the lateral diffusion of the channel-stop dopant ions	0	0	m
8	TR	Temperature at which the parameters for the reference transistor have been determined	27.0	27.0	°C
9	VFBR	Flat-band voltage for the reference transistor at the reference temperature	-1.05	-1.05	V
10	STVFB	Coefficient of the temperature	0.50×10^{-3}	0.50×10^{-3}	VK ⁻¹
11	KOR	Body-effect factor for the reference transistor	0.5	0.5	V ^{1/2}
12	SLKO	Coefficient of the length dependence of k_0	0	0	V ^{1/2} m
13	SL2KO	Second coefficient of the length dependence of k_0	0	0	V ^{1/2} m ²
14	SWKO	Coefficient of the width dependence of k_0	0	0	V ^{1/2} m
15	KPINV	Inverse of body-effect factor of the poly-silicon gate	0	0	V ^{-1/2}
16	PHIBR	Surface potential at the onset of strong inversion at the reference temperature	0.95	0.95	V
17	SLPHIB	Coefficient of the length dependence of ϕ_B	0	0	Vm
18	SL2PHIB	Second coefficient of the length dependence of ϕ_B	0	0	Vm ²
19	SWPHIB	Coefficient of the width dependence of ϕ_B	0	0	Vm
20	BETSQ	Gain factor for an infinite square transistor at the reference temperature	370.9×10^{-6}	1.15×10^{-4}	AV ⁻²
21	ETABET	Exponent of the temperature dependence of the gain factor	1.3	0.5	-
22	FBET1	Relative mobility decrease due to first lateral profile	0	0	-

Nr.	Name	Description	Default		Units
			N-type	P-type	
23	LP1	Characteristic length of first lateral profile	0.8×10^{-6}	0.8×10^{-6}	m
24	FBET2	Relative mobility decrease due to second lateral profile	0	0	-
25	LP2	Characteristic length of second lateral profile	0.8×10^{-6}	0.8×10^{-6}	m
26	THESRR	Coefficient of the mobility reduction due to the surface roughness scattering for the reference transistor at the reference temperature	0.4	0.73	V^{-1}
27	SWTHESR	Coefficient of the width dependence of θ_{sf}	0	0	m
28	THEPHR	Coefficient of the mobility reduction due to the phonon scattering for the reference transistor at the reference temperature	1.29×10^{-2}	1.00×10^{-2}	V^{-1}
29	ETAPH	Exponent of the temperature dependence of θ_{ph} for the reference transistor	1.75	1.75	-
30	SWTHEPH	Coefficient of the width dependence of θ_{ph}	0	0	m
31	ETAMOBR	Effective field parameter for dependence on depletion/inversion charge for the reference transistor	1.4	3	-
32	STETAMOB	Coefficient of the temperature dependence of η_{mob}	0	0	K^{-1}
33	SWETAMOB	Coefficient of the width dependence of η_{mob}	0	0	m
34	NUR	Exponent of the field dependence of the mobility model minus 1 (ie. v-1) at the reference temperature	1	1	-
35	NUEXP	Exponent of the temperature dependence of parameter v	5.25	3.23	-
36	THERR	Coefficient of the series resistance for the reference transistor at the reference temperature	0.155	0.08	V^{-1}
37	ETAR	Exponent of the temperature dependence of θ_R	0.95	0.4	-
38	SWTHER	Coefficient of the width dependence of θ_R	0	0	m

Nr.	Name	Description	Default		Units
			N-type	P-type	
39	THER1	Numerator of the gate voltage dependent part of series resistance for the reference transistor	0	0	V
40	THER2	Denominator of the gate voltage dependent part of series resistance for the reference transistor	1	1	V
41	THESATR	Velocity saturation parameter due to optical/acoustic phonon scattering for the reference transistor at the reference temperature	0.5	0.2	V ⁻¹
42	SLTHESAT	Coefficient of the length dependence of θ_{sat}	1	1	-
43	THESATEXP	Exponent of the length dependence of θ_{sat}	1	1	-
44	ETASAT	Exponent of the temperature dependence of θ_{sat}	1.04	0.86	-
45	SWTHESAT	Coefficient of the width dependence of θ_{sat}	0	0	m
46	THETHR	Coefficient of self-heating for the reference transistor at the reference temperature	1×10 ⁻³	0.5×10 ⁻³	V ⁻³
47	THETHEXP	Exponent of the length dependence of θ_{Th}	1	1	-
48	SWTHETH	Coefficient of the width dependence of θ_{Th}	0	0	m
49	SDIBLO	Drain-induced barrier lowering parameter for the reference transistor	2×10 ⁻³	1.00×10 ⁻³	V ^{-1/2}
50	SDIBLEXP	Exponent of the length dependence of σ_{dibl}	1.35	1.35	-
51	MOR	Parameter for short-channel subthreshold slope for the reference transistor	0	0	-
52	MOEXP	Exponent of the length dependence of m_0	1.34	1.34	-
53	SSFR	Static feedback parameter for the reference transistor	6.25×10 ⁻³	6.25×10 ⁻³	V ^{-1/2}

Nr.	Name	Description	Default		Units
			N-type	P-type	
54	SLSSF	Coefficient of the length dependence of σ_{sf}	1×10^{-6}	1×10^{-6}	m
55	SWSSF	Coefficient of the width dependence of σ_{sf}	0	0	m
56	ALPR	Factor of the channel length modulation for the reference transistor	0.01	0.01	-
57	SLALP	Coefficient of the length dependence of α	1	1	-
58	ALPEXP	Exponent of the length dependence of α	1	1	-
59	SWALP	Coefficient of the width dependence of α	0	0	m
60	VP	Characteristic voltage of the channel length modulation	0.05	0.05	V
61	LMINT^a	Minimum effective channel length in technology, used for calculation of smoothing factor m	0.15×10^{-6}	0.15×10^{-6}	m
62	A1R	Factor of the weak-avalanche current for the reference transistor at the reference temperature	6	6	-
63	STA1	Coefficient of the temperature dependence of a_1	0	0	$^{\circ}\text{K}^{-1}$
64	SLA1	Coefficient of the length dependence of a_1	0	0	m
65	SWA1	Coefficient of the width dependence of a_1	0	0	m
66	A2R	Exponent of the weak-avalanche current for the reference transistor at the reference temperature	38	38	V
67	SLA2	Coefficient of the length dependence of a_2	0	0	Vm
68	SWA2	Coefficient of the width dependence of a_2	0	0	m
69	A3R	Factor of the drain-source voltage above which the weak-avalanche occurs, for the reference transistor	1	1	-
70	SLA3	Coefficient of the length dependence of a_3	0	0	m

Nr.	Name	Description	Default		Units
			N-type	P-type	
71	SWA3	Coefficient of the width dependence of a_3	0	0	m
72	IGINVR	Gain factor for intrinsic gate tunnelling current in inversion for the reference transistor	0	0	AV ²
73	BINV	Probability factor for intrinsic gate tunneling current in inversion	48	87.5	V
74	IGACCR	Gain factor for intrinsic gate tunnelling current in accumulation for the reference transistor	0.0	0.0	AV ²
75	BACC	Probability factor for intrinsic gate tunnelling current in accumulation	48	48	V
76	VFBOV	Flat-band voltage for the Source/Drain overlap extensions	0	0	V
77	KOV	Body-effect factor for the Source/Drain overlap extensions	2.5	2.5	V ^{1/2}
78	IGOVR	Gain factor for Source/Drain overlap gate tunnelling current for the reference transistor	0	0	AV ²
79	TOX	Thickness of the gate oxide layer	3.2×10^{-9}	3.2×10^{-9}	m
80	COL	Gate overlap capacitance per unit channel width	0.32×10^{-9}	0.32×10^{-9}	Fm ⁻¹
81	GATENOISE	Flag for in/exclusion of induced gate thermal noise	0	0	-
82	NTR	Coefficient of the thermal noise for the reference transistor	1.6564×10^{-20}	1.6564×10^{-20}	J
83	NFAR	First coefficient of the flicker noise for the reference transistor	1.573×10^{22}	3.825×10^{23}	V ⁻¹ m ⁻⁴
84	NFBR	Second coefficient of the flicker noise for the reference transistor	4.752×10^8	1.015×10^8	V ⁻¹ m ⁻²
85	NFCR	Third coefficient of the flicker noise for the reference transistor	0	7.3×10^{-9}	V ⁻¹

a. The model parameter LMIN in Philips documentation is modified to LMINT in Eldo to avoid any conflict between this parameter and the model parameters LMIN, LMAX, WMIN, and WMAX which are responsible for the specification of bin corners in Binned model cards in Eldo.



Note For the case of parameters *L* and *W* in Philips documentation, they are treated as device parameters in Eldo. Similarly, *MULT* is equivalent to the **M** device parameter in Eldo. The *DTA* parameter in Philips documentation is equivalent to **DTEMP** in Eldo.

3.2 DC operating points

The following is a list of the DC operating points that are printed in the *.chi* file in OP and AC analysis.



The last three DC operating points can only appear in a Noise analysis.

Note



For all C_{xy} below, it indicates the derivative of the charge Q at the terminal x to the voltage at terminal y , when all other terminals remain constant

DC operating point	Description
IDS	Channel current,excluding avalanche and tunnel currents
IVAL	substrate current due to Weak avalanche current
IGS	Gate to Source current due to direct tunneling
IGD	Gate to Drain current due to direct tunneling
IGB	Gate to Bulk current due to direct tunneling
VDS	Drain-source voltage
VGS	Gate-source voltage
VSB	Source-bulk voltage
VTO	Zero-bias threshold voltage
VTS	Threshold voltage including back-bias effects
VTH	Threshold voltage including back-bias and drain-bias effects
VGT	Effective gate derive voltage including back-bias and drain-bias effects
VDSS	Drain saturation voltage at actual bias
VSAT	Saturation limit
GM	Channel transconductance dI_{ds}/dV_{gs} (assumed $V_{ds} > 0$)
GMB	Substrate-transconductance dI_{ds}/dV_{bs}
GDS	Output conductance dI_{ds}/dV_{ds}
Qd	Intrinsic Drain charge
Qs	Intrinsic Source charge
Qb	Intrinsic Bulk charge
Qg	Intrinsic Gate charge

DC operating point	Description
CGDOL	Gate-drain overlap capacitance of the actual transistor
CGSOL	Gate-source overlap capacitance of the actual transistor
WEFF	Effective channel width for the geometrical models
LEFF	Effective channel length for the geometrical models
U	Transistor gain
ROUT	Small-signal output resistance
VEARLY	Equivalent Early voltage
KEFF	Body effect parameter
BEFF	Gain factor
FUG	Unity gain frequency at actual bias
CDD	
CDG	
CDS	
CDB	
CGD	
CGG	
CGS	
CGB	
CSD	
CSG	
CSS	
CSB	
CBD	
CBG	
CBS	
CBB	
SQRTSFW	Input-referred RMS white noise voltage density
SQRTSFF	Input-referred RMS white noise voltage density at 1 KHz
FKNEE	Cross-over frequency above which white noise is dominant

Printing or plotting a state from the MM11 States structure

If a state from the list below is to be monitored by the user, the user has to type in the netlist for a given transistor M1 to monitor, for example Gm:

- .PLOT DC S (M1 ->Gm) for DC or
- .PLOT AC S (M1 ->Gm) for AC or
- .PLOT TRAN S (M1 ->Gm) for TRAN

The same is applied to the following list of states.



For all C_{xy} below, it indicates the derivative of the charge Q at the terminal x to the voltage at terminal y , when all other terminals remain constant.

DC operating point	Description
IDS	Channel current, excluding avalanche and tunnel currents
IGS	Gate to Source current due to direct tunneling
IGD	Gate to Drain current due to direct tunneling
IGB	Gate to Bulk current due to direct tunneling
VDS	Drain-source voltage
VGS	Gate-source voltage
VSB	Source-bulk voltage
VTO	Zero-bias threshold voltage
VTS	Threshold voltage including back-bias effects
VTH	Threshold voltage including back-bias and drain-bias effects
VGT	Effective gate derive voltage including back-bias and drain-bias effects
VDSS	Drain saturation voltage at actual bias
VSAT	Saturation limit
GM	Channel transconductance dI_{ds}/dV_{gs} (assumed $V_{ds} > 0$)
GMB	Substrate-transconductance dI_{ds}/dV_{bs}
GDS	Output conductance dI_{ds}/dV_{ds}
Qd	Intrinsic Drain charge
Qs	Intrinsic Source charge
Qb	Intrinsic Bulk charge
Qg	Intrinsic Gate charge
CGDOL	Gate-drain overlap capacitance of the actual transistor

DC operating point	Description
CGSOL	Gate-source overlap capacitance of the actual transistor
WEFF	Effective channel width for the geometrical models
LEFF	Effective channel length for the geometrical models
U	Transistor gain
ROUT	Small-signal output resistance
VEARLY	Equivalent Early voltage
KEFF	Body effect parameter
BEFF	Gain factor
FUG	Unity gain frequency at actual bias
CDD	
CDG	
CDS	
CDB	
CGD	
CGG	
CGS	
CGB	
CSD	
CSG	
CSS	
CSB	
CBD	
CBG	
CBS	
CBB	

Chapter 25

TFT Amorphous-Si Model

1.0 Introduction

This is the modified amorphous-silicon TFT model based on the original work at Rensselaer Polytechnic Institute (RPI). The TFT Amorphous-Si model is implemented in Eldo as LEVEL=64. The model provides the following features and benefits:

- Uses the new, universal charge control concept, which guarantees stability and convergence
- Unified DC models cover all regimes of operation
- AC models accurately reproduces C_{gc} frequency dispersion
- Automatic scaling of model parameters to accurately model a wide range of device geometries
- Temperature dependence included
- A minimum number of physically based parameters that can easily be extracted from experimental data and related back to the fabrication steps

This model includes the following effects for drain current:

Above Threshold

- Modified charge control model; induced charge trapped in localized states
- Field effect mobility becomes a function of gate bias
- Band mobility dominated by lattice scattering

Below Threshold

- Fermi level located in deep localized states
- Relate position of Fermi level including the deep DOS back to the gate bias

Hole-Induced Leakage Current

- Empirical expression for current at large negative bias biases

Temperature Effects

- Linear dependence of threshold voltage
- Temperature activated field-effect mobility
- Temperature activated leakage current
- Temperature dependence of subthreshold slope: possible back channel effect

2.0 Model Structure

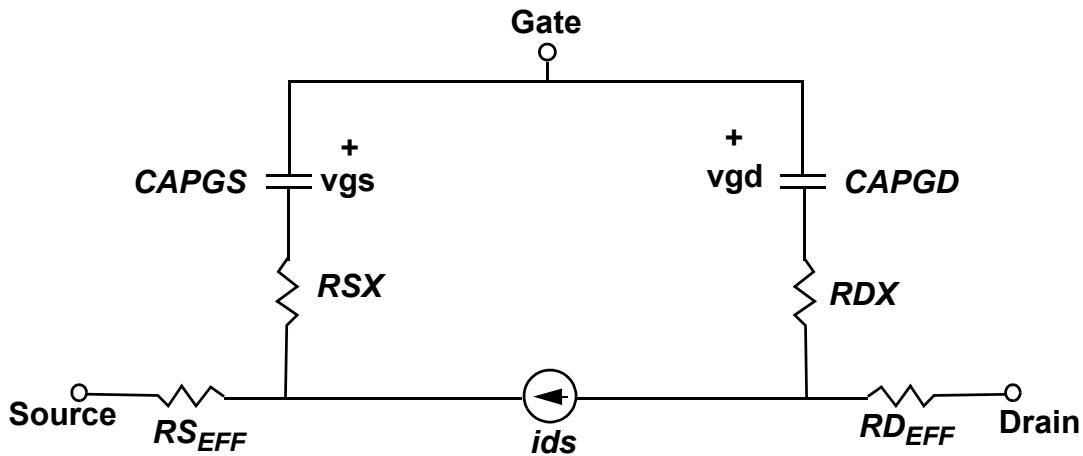


Figure 25-1. TFT Equivalent Circuit for DC and Transient Analysis

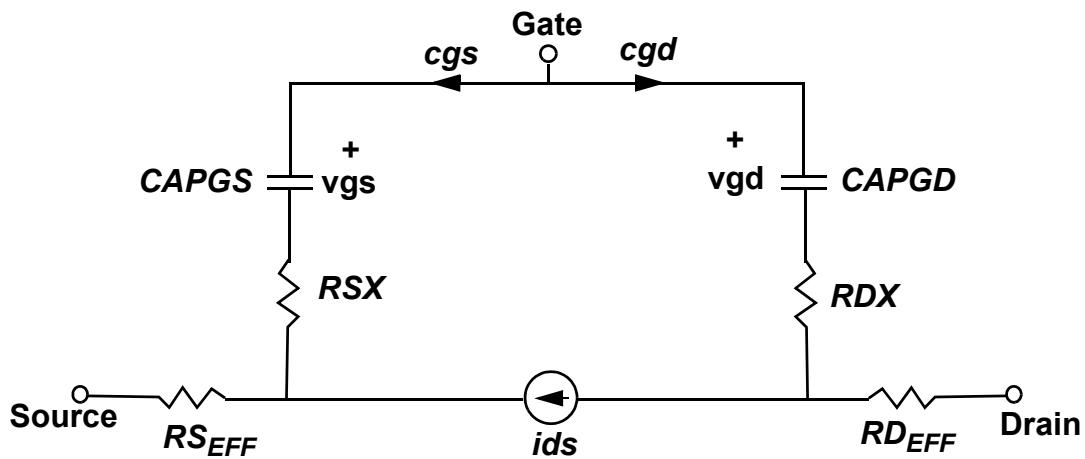


Figure 25-2. TFT Equivalent Circuit for AC Analysis

3.0 DC Current Equations

3.1 Drain Current

$$I_{ds} = I_{leakage} + I_{ab}$$

$$I_{ab} = g_{ch} V_{dse} (1 + LAMBDA \cdot V_{ds})$$

$$V_{dse} = \frac{V_{ds}}{\left[1 + \left(\frac{V_{ds}}{V_{sat}} \right)^M \right]^{\frac{1}{M}}}$$

$$V_{sat} = \alpha_{sat} V_{gte}$$

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(RS + RD)}$$

$$g_{chi} = qn_s W \cdot \frac{MUBAND}{L}$$

$$n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}}$$

$$n_{sa} = \frac{EPSI \cdot V_{gte}}{q \cdot TOX} \left(\frac{V_{gte}}{V_{aat}} \right)^{GAMMA}$$

$$n_{sb} = n_{so} \left(\frac{t_m}{TOX} \cdot \frac{V_{gfbe}}{V0} \cdot \frac{EPSI}{EPS} \right)^{\frac{2 \cdot V0}{V_e}}$$

$$n_{so} = N_c t_m \frac{V_e}{V0} \exp \left(-\frac{DEF0}{V_{th}} \right)$$

$$N_c = 3.0 \cdot 10^{25} m^{-3}$$

$$V_e = \frac{2 \cdot V0 \cdot V_{tho}}{2 \cdot V0 - V_{th}}$$

$$t_m = \sqrt{\frac{EPS}{2q \cdot GMIN}}$$

$$V_{gte} = \frac{VMIN}{2} \left[1 + \frac{V_{gt}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gt}}{VMIN} - 1 \right)^2} \right]$$

$$V_{gt} = V_{gs} - V_T$$

$$V_{gfbe} = \frac{VMIN}{2} \left[1 + \frac{V_{gfb}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gfb}}{VMIN} - 1 \right)^2} \right]$$

$$V_{gfb} = V_{gs} - VFB$$

$$I_{leakage} = I_{hl} + I_{min}$$

$$I_{hl} = IOL \left[\exp \left(\frac{V_{ds}}{VDSL} \right) - 1 \right] \exp \left(-\frac{V_{gs}}{VGSL} \right) \exp \left[\frac{EL}{q} \left(\frac{1}{V_{tho}} - \frac{1}{V_{th}} \right) \right]$$

$$I_{min} = SIGMA0 \cdot V_{ds}$$

3.2 Temperature Dependence

$$V_{tho} = k_B \cdot \frac{TNOM}{q}$$

$$V_{th} = k_B \cdot \frac{TEMP}{q}$$

$$V_{aat} = VAA \exp \left[\frac{EMU}{q \cdot GAMMA} \left(\frac{1}{V_{th}} - \frac{1}{V_{tho}} \right) \right]$$

$$V_T = VTO + KVT(TEMP - TNOM)$$

$$\alpha_{sat} = ALPHASAT + KASAT(TEMP - TNOM)$$

3.3 Capacitance

$$C_{gs} = C_f + \frac{2}{3} C_{gc} \left[1 - \left(\frac{V_{sate} - V_{dse}}{2V_{sate} - V_{dse}} \right) \right]$$

$$C_{gd} = C_f + \frac{2}{3} C_{gc} \left[1 - \left(\frac{V_{sate}}{2V_{sate} - V_{dse}} \right)^2 \right]$$

$$C_f = 0.5 \cdot EPS \cdot W$$

$$C_{gs} = q \frac{dn_{sc}}{dV_{gs}}$$

$$n_{sc} = \frac{n_{sac} n_{sbc}}{n_{sac} + n_{sbc}}$$

$$n_{sac} = \frac{EPSI \cdot V_{gte}}{q \cdot TOX}$$

$$n_{sbc} = n_{sb}$$

3.4 Access Resistance Calculation

ACM = 0

If ($NRS \cdot RSH > 0$)

$$Rseff = NRS \cdot RSH + RSC$$

else:

$$Rseff = RS + RSC$$

If ($NRD \cdot RSH > 0$)

$$Rdeff = NRD \cdot RSH + RDC$$

else:

$$Rdeff = RD + RDC$$

ACM = 1

$$Rseff = (LD + LDIF) \cdot SCALM / Weff \cdot RS + (NRS \cdot RSH + RSC)$$

$$Rdeff = (LD + LDIF) \cdot SCALM / Weff \cdot RD + (NRD \cdot RSH + RDC)$$

ACM = 2 or 3

If NRS given then as above,

$$Rseff = (LD + LDIF) \cdot SCALM / Weff \cdot RS + (NRS \cdot RSH + RSC)$$

else:

$$Rseff = RSC + HDIF \cdot WMLT \cdot SCALM \cdot RSH + \\ (LD + LDIF) \cdot \frac{SCALM}{Weff} \cdot RS$$

If **NRD** given then as above,

$$R_{deff} = (LD + LDIF) \cdot SCALM / W_{eff} \cdot RD + (NRD \cdot RSH + RDC)$$

else:

$$R_{deff} = RDC + HDIF \cdot WMLT \cdot SCALM \cdot RSH + \\ (LD + LDIF) \cdot \frac{SCALM}{W_{eff}} \cdot RD$$

3.5 Overlap Capacitance Calculation

$$W = W \cdot SCALE \cdot WMLT + XW \cdot SCALM$$

If **CGSO** is given, then:

$$\text{GateSourceOVERLAP CAP} = W \cdot \frac{CGSO}{SCALM}$$

else:

$$\text{GateSourceOVERLAP CAP} = W \cdot (LD + METO) \cdot \frac{COX}{SCALM}$$

If **CGDO** is given, then:

$$\text{GateDrainOVERLAP CAP} = W \cdot \frac{CGDO}{SCALM}$$

else:

$$\text{GateDrainOVERLAP CAP} = W \cdot (LD + METO) \cdot \frac{COX}{SCALM}$$

4.0 Model Parameters

Nr.	Name	Description	Default	Units
1	ALPHASAT	Saturation modulation parameter	0.6	-
2	CGDO	Gate-drain overlap capacitance per meter channel width	0.0	F/m
3	CGSO	Gate-source overlap capacitance per meter channel width	0.0	F/m
4	DEF0	Dark Fermi level position	0.6	eV
5	DELTA	Transition width parameter	5	-
6	EL	Activation energy of the hole leakage current	0.35	eV
7	EMU	Field effect mobility activation energy	0.06	eV
8	EPS	Relative dielectric constant of substrate	11	-
9	EPSI	Relative dielectric constant of gate insulator	7.4	-
10	GAMMA	Power law mobility parameter	0.4	-
11	GMIN	Minimum density of deep states	1E23	$\text{m}^{-3}\text{eV}^{-1}$
12	IOL	Zero bias leakage current parameter	3E-14	A
13	KASAT	Temperature coefficient of ALPHASAT	0.006	$^{\circ}\text{C}$
14	KVT	Threshold voltage temperature coefficient	-0.036	V°C
15	LAMBDA	Output conductance parameter	0.0008	1/V
16	M	Knee shape parameter	2.5	-
17	MUBAND	Conduction band mobility	0.001	m^2/Vs
18	RD	Drain resistance	0.0	μ
19	RS	Source resistance	0.0	μ
20	RDX	Resistance in series with CAPGD	0	Ω
21	RSX	Resistance in series with CAPGS	0	Ω
22	RDSMOD	Selector for extrinsic parasitics Rd and Rs	0	-
23	SIGMA0	Minimum leakage current parameter	1E-14	A
24	TNOM	Parameter measurement temperature	25	$^{\circ}\text{C}$
25	TOX	Thin-oxide thickness	1E-7	m
26	V0	Characteristic voltage for field effect mobility	0.12	V
27	VAA	Characteristic voltage for field effect mobility	7.5E3	V
28	VDSL	Hole leakage current drain voltage parameter	7	V
29	VFB	Flat band voltage	-3	V
30	VGSL	Hole leakage current gate voltage parameter	7	V

Nr.	Name	Description	Default	Units
31	VMIN	Convergence parameter	0.3	V
32	VTO	Zero-bias threshold voltage	0.0	V

4.1 Parasitic Parameters (Access Resistance and Overlap Capacitance Parameters)

Nr.	Name	Description	Default	Units
1	ACM	Area Calculation Method	0	
2	RDC	Additional drain resistance due to contact resistance	0	
3	RSC	Additional source resistance due to contact resistance	0	
4	HDIF	Length of heavily doped diffusion from contact to lightly doped region	0	HDIF*SCALM
5	LD	Lateral diffusion into channel from source and drain diffusion	0.75 * XJ	LD*SCALM
6	LDIF	Length of lightly doped diffusion adjacent to gate	0	LDIF*SCALM
7	WMLT	Width diffusion layer shrink reduction factor	1	
8	XJ	Metallurgical junction depth	0	
9	SCALM	Scale factor for model parameters	1	
10	METO	Fringing field factor for gate to source and gate to drain overlap capacitance	0	METO*SCALM
11	WD	Lateral diffusion into channel from bulk along width	0	WD*SCALM
12	COX	Oxide capacitance	1	COX/SCALM^2
13	LMLT	Length shrink factor	0	
14	XW	Accounts for masking and etching effects in Weff calculation	0	XW*SCALM
15	XL	Accounts for masking and etching effects in Leff calculation	0	XL*SCALM

**Note**

If **RDSMOD=0** then the effect of R_d and R_s will be taken in the equation of the current (I_{ds}).

If **RDSMOD=1** then the effect of R_d and R_s will be taken into consideration independently from the equation of the current (I_{ds}).

4.2 Printing and Plotting Output States

Printing or plotting a state from the A-Si TFT RPI States structure. If a state from the list below is to be monitored by the user, the user has to type in the netlist for a given transistor M1 to monitor, for example Gm:

- .PLOT DC S (M1->Gm) for DC or
- .PLOT AC S (M1->Gm) for AC or
- .PLOT TRAN S (M1->Gm) for TRAN

The same is applied to the following list of states:

State	Description
<i>Ids</i>	Channel current
<i>Gm</i>	Transconductance
<i>Gds</i>	Channel conductance
<i>vt_tft</i>	Threshold voltage
<i>vgt</i>	Gate overdrive voltage
<i>vdsat</i>	Drain saturation voltage
<i>Qgdav</i>	Gate-drain average charge
<i>cgd</i>	Gate-drain capacitance
<i>Qgsav</i>	Gate-source average charge
<i>cgs</i>	Gate-source capacitance

Chapter 26

HiSIM Model

1.0 Introduction

HiSIM (Hiroshima University STARC IGFET Model) MOSFET model is a complete MOSFET surface potential model for circuit simulation based on the drift-diffusion approximation. The HiSIM model is implemented in Eldo as LEVEL=66.

The most important advantage of the drift-diffusion approximation is the unified description of device characteristics for all bias conditions. Under the gradual-channel approximation all device characteristics are described analytically by channel-surface potentials at the source side and at the drain side. These surface potentials are functions of applied voltages on four terminals; the gate voltage V_{gs} , the drain voltage V_{ds} , the bulk voltage V_{bs} and the earthed source. All phenomena such as short-channel and reverse-short-channel effects are therefore treated as results of the surface potential modification.

Since the surface potentials are implicit functions of applied voltages, iteration procedures are required in addition to global time-step iteration in circuit simulation. Therefore specific attention is paid on calculating the surface potentials with enough accuracy even with small CPU time. Up to now validity of HiSIM has been tested for the channel length down to $0.1\mu\text{m}$ with the pocket-implanted technology. Though all descriptions are given for the n-channel MOSFET, they are also valid for the p-channel case.

Modeled features:

- General Characteristics: determined by physics
- symmetry at $V_{ds}=0$ (drift-diffusion approximation).

- mobility-field dependences (Universal mobility model.)
- temperature dependences of bandgap, phonon scattering and saturation velocity.
- channel-length modulation. (inclusion of lateral-electric field)
- capacitances (charges controlled by applied voltages, calculated from the surface potential values.)
- Gate tunneling current.
- GIDL (Gate-Induced Drain Leakage) and GISL (Gate-Induced Source Leakage) Currents.

Characteristics Caused by Scaling: determined by technology

- short-channel effects
- reverse short-channel effects
 - retrograded
 - pocket implant
- quantum-mechanical effect
- gate-poly depletion effect
- Narrow-Channel Effects (Threshold Voltage shift, Mobility Reduction and Leakage Transistor “Hump in Ids”).

1.1 Version selection

The different versions, HiSIM1.0.2, HiSIM1.1.2, and HiSIM1.2.0 are accessible through the model parameter **VERSION**. By default, HiSIM1.2.0 (**VERSION=120**) is selected. Below is a table showing the different HiSIM versions selection.

Parameter Value	HiSIM Version
VERSION=120	HiSIM1.2.0 (Default)
VERSION=112	HiSIM1.1.2
VERSION=102	HiSIM1.0.2

It is recommended to use version 1.2.0 as earlier versions (1.1.2 and 1.0.2) are less stable and prone to numerical problems and errors.

1.2 Documentation



User's can access the full documentation of the HiSIM Model for further information by visiting the following website:
<http://www.starc.jp/kaihatu/pdgr/hisim/hisim.html>

2.0 Model Parameters

Table 26-1. HiSIM Model Parameters

Name	Description	Default	Min	Max	Units
TOX	Oxide thickness	5n			m
XLD	Gate-overlap length	0	0	50n	m
XWD	Gate-overlap width	0	0	100n	m
XQY	Distance from drain junction to maximum electric field point	0	0	50n	m
XPOLYD	Difference between gate-poly and design length	0			m
XDIFFD	Difference between gate-poly and design width	0			m
TPOLY	Height of gate poly-SI	0			m
NSUBC	Substrate-impurity concentration	1×10^{17}	1×10^{16}	1×10^{19}	cm^{-3}
VFBC	Flat-band voltage	-1.0	-1.2	-0.8	V
LP	Pocket penetration length	15n	1n	300n	m
NSUBP	Maximum pocket concentration	1×10^{17}	1×10^{17}	1×10^{20}	cm^{-3}

Table 26-1. HiSIM Model Parameters

Name	Description	Default	Min	Max	Units
KAPPA	Dielectric constant for gate-oxide	3.9			
SCP1	Short-channel coefficient 1 for pocket	0	0	200	
SCP2	Short-channel coefficient 2 for pocket	0	0	200	V ⁻¹
SCP3	Short-channel coefficient 3 for pocket	0	0	1m	V ⁻¹ m
PARL1	Strength of lateral-electric-field gradient	1.0			
PARL2	Depletion width of channel/contract junction	0	0	50n	m
SC1	Short-channel coefficient 1	0	0	200	
SC2	Short-channel coefficient 2	0	0	200	V ⁻¹
SC3	Short-channel coefficient 3	0	0	1m	V ⁻¹ m
WFC	Threshold voltage reduction	0	0	1x10 ⁻⁶	Fcm ⁻² m ⁻¹
W0	Minimum gate width	0			log(cm)
QME1	Coefficient for quantum mechanical effect	40p			Vm ⁻²
QME2	Coefficient for quantum mechanical effect	300p			V
QME3	Coefficient for quantum mechanical effect	0			m
PGD1	Strength of poly depletion	10m	0	20m	
PGD2	Threshold voltage of poly depletion	1.0	0	1.0	V
PGD3	V _{ds} dependence of poly depletion	0.8	0	1.0	
RS	Source-contact resistance	80μ	0	100μ	VA ⁻¹ m
RD	Drain-contact resistance	80μ	0	100μ	VA ⁻¹ m
RPOCK1	Resistance coefficient caused by the potential barrier	0.1m	0	10	V ² A ^{-RPOCP1} μm ^{1-RPOCP2}
RPOCK2	Resistance coefficient caused by the potential barrier	100m	0	500m	V
RPOCP1	Resistance coefficient caused by the potential barrier	1	0	5	
RPOCP2	Resistance coefficient caused by the potential barrier	0.5	0	5	
BGTMPI	Bandgap narrowing	90.25μ			eVK ⁻¹
BGTMPII	Bandgap narrowing	100n	-5μ	5μ	eVK ⁻²
VMAX	Maximum saturation velocity	7MEG	1MEG	100MEG	cms-1
MUECB0	Coulomb scattering	300	1.0	1K	cm ² V ⁻¹ s ⁻¹

Table 26-1. HiSIM Model Parameters

Name	Description	Default	Min	Max	Units
MUECB1	Coulomb scattering	30	1.0	1K	$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$
MUEPH0	Phonon scattering	300m			
MUEPH1	Phonon scattering	25K	100	1MEG	$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ (Vcm^{-1}) ^{MUEPH0}
MUEPH2	Mobility reduction	0	0	100K	$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ (Vcm^{-1}) ^{MUEPH0} /log(cm)
MUETMP	Temperature dependence of phonon scattering	1.5	1.0	2.0	
MUESR0	Surface-roughness scattering	2.0	1.0	2.0	
MUESR1	Surface-roughness scattering	2×10^{15}	1×10^{13}	1×10^{17}	$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ (Vcm^{-1}) ^{MUESR0}
NDEP	Coefficient of effective-electric field	1.0			
NINV	Coefficient of effective-electric field	0.5			
NINVD	Modification of NINV	1n	0	20m	V^{-1}
BB	High-field-mobility degradation	2.0(nMOS) 1.0(pMOS)			
VOVER	Velocity overshoot effect	10m	0	500m	$\text{cm}^{\text{VOVERP}}$
VOVERP	L_{eff} dependence of velocity overshoot	100m	0	500m	
CLM1	Hardness coefficient of channel/contact junction	0.7	0.5	1.0	
CLM2	Coefficient for Q_B contribution	2	1	2	
CLM3	Coefficient for Q_I contribution	1	1	5	
SUB1	Substrate current coefficient 1	10			V^{-1}
SUB2	Substrate current coefficient 2	20			V
SUB3	Substrate current coefficient 3	0.8			
GIDL1	GIDL current coefficient 1	5 μ			$\text{AV}^{-3/2}\text{C}^{-1}\text{m}$
GIDL2	GIDL current coefficient 2	1MEG			$\text{V}^{-2}\text{m}^{-1}\text{F}^{-3/2}$
GIDL3	GIDL current coefficient 3	300m			
GLEAK1	Gate leakage current coefficient 1	10K			$\text{AV}^{-3/2}\text{C}^{-1}$
GLEAK2	Gate leakage current coefficient 2	20MEG			$\text{V}^{-2}\text{m}^{-1}\text{F}^{-3/2}$
GLEAK3	Gate leakage current coefficient 3	300m			
GLPART1	Partitioning ratio of gate leakage current	0	0	1	
GLPART2	Partitioning ratio of gate leakage current	0	0	1	

Table 26-1. HiSIM Model Parameters

Name	Description	Default	Min	Max	Units
WVTHSC	Short-channel effect at the STI edge	0			
NSTI	Substrate-impurity concentration at the STI edge	1×10^{17}			cm ⁻³
WSTI	Width of the high-field region at STI	0			m
VZADD0	Symmetry conservation coefficient	10m			V
PZADD0	Symmetry conservation coefficient	5m			V
JS0	Saturation current density	1×10^{-4}			Am ⁻²
JS0SW	Sidewall saturation current density	0			Am ⁻¹
NJ	Emission coefficient	1.0			
NJSW	Sidewall emission coefficient	1.0			
XTI	Junction current temperature exponent coefficient	3.0			
CJ	Bottom junction capacitance per unit area at zero bias	5×10^{-4}			Fm ⁻²
CJSW	Source/drain sidewall junction capacitance grading coefficient per unit length at zero bias	5×10^{-10}			Fm ⁻¹
CJSWG	Source/drain sidewall junction capacitance per unit length at zero bias	5×10^{-10}			Fm ⁻¹
MJ	Bottom junction capacitance grading coefficient	0.5			
MJSW	Source/drain sidewall junction capacitance grading coefficient	0.33			
MJSWG	Source/drain gate sidewall junction capacitance grading coefficient	0.33			
PB	Bottom junction build-in potential	1.0			V
PBSW	Source/drain sidewall junction build-in potential	1.0			V
PBSWG	Source/drain gate sidewall junction build-in potential	1.0			V
VDIFFJ	Diode threshold voltage between source/drain and substrate	0.5			V
NFALP	Contribution of the mobility fluctuation	1×10^{-16}			cms
NFTRP	Ratio of trap density to attenuation coefficient	10G			V ⁻¹ cm ⁻²
CIT	Capacitance caused by the interface trapped carriers	0			Fcm ⁻²
EF	Power for frequency	0			

Table 26-1. HiSIM Model Parameters

Name	Description	Default	Min	Max	Units
PTHROU	Correction for steep subthreshold swing	0	0	0.1	

Table 26-2. Model Selector Parameters

Parameter	Description	Default
CORSRD	Contact resistances Rs and Rd are included and equations are solved iteratively	0
COOVLP	Overlap capacitance model is selector	0
COISUB	Substrate current Isub selector	0
COIIGS	Gate current Igate selector	0
COGIDL	GIDL current IGIDL selector	0
COGISL	GISL current IGISL selector	0
CONOIS	1/f noise SIds selector	0
STI	Leakage current Ids, STI selector	0
COCGSO	Gate-source overlap capacitance selector	0
COCGDO	Gate-drain overlap capacitance selector	0
COADOV	Lateral field induced and overlap charges/capacitances are added to intrinsic ones	1
COSMBI	Effective bias for smoothing conductances at high voltage ranges for Vds, Vgs and Vbs is selected	0
Eldo specific selector		
CHKINTCALC	Allow issuing warnings for negative conductance and large overshoot during iterations	0

2.1 Printing and Plotting Output States

If a state from the list below is to be monitored by the user, the user has to type in the netlist for a given transistor M1 to monitor, for example Gm:

- .PLOT DC S (M1 ->Gm) for DC or
- .PLOT AC S (M1 ->Gm) for AC or
- .PLOT TRAN S (M1 ->Gm) for TRAN

The same is applied to the following list of states:

State	Description
<i>IDS</i>	Channel current
<i>GDS</i>	Channel conductance
<i>GM</i>	Channel transconductance dId_s/dV_{gs}
<i>GMBS</i>	Channel transconductance dId_s/dV_{bs}
<i>IBS</i>	Bulk/Source diode current
<i>GBS</i>	Bulk/Source diode conductance
<i>IBD</i>	Bulk/Drain diode current
<i>GBD</i>	Bulk/Drain diode conductance
<i>ISUB</i>	Substrate current
<i>GBGS</i>	dI_{sub}/dV_{gs}
<i>GBDS</i>	dI_{sub}/dV_{ds}
<i>GBBS</i>	dI_{sub}/dV_{bs}
<i>IGATEB</i>	Gate/Bulk current
<i>GGBGS</i>	dI_{gateb}/dV_{gs}
<i>GGBDS</i>	dI_{gateb}/dV_{ds}
<i>GGBBS</i>	dI_{gateb}/dV_{bs}
<i>IGATES</i>	Gate/Source current
<i>GGSGS</i>	dI_{gates}/dV_{gs}
<i>GGSDS</i>	dI_{gates}/dV_{ds}
<i>GGSBS</i>	dI_{gates}/dV_{bs}
<i>IGATED</i>	Gate/Drain current
<i>GGDGS</i>	dI_{gated}/dV_{gs}
<i>GGDDS</i>	dI_{gated}/dV_{ds}
<i>GGDBS</i>	dI_{gated}/dV_{bs}
<i>IGIDL</i>	I_{gidl} current
<i>GGIDLGS</i>	dI_{gidl}/dV_{gs}
<i>GGIDLDS</i>	dI_{gidl}/dV_{ds}
<i>GGIDLBS</i>	dI_{gidl}/dV_{bs}
<i>IGISL</i>	I_{gisl} current
<i>GGISLGD</i>	dI_{gisl}/dV_{gd}
<i>GGISLSD</i>	dI_{gisl}/dV_{sd}
<i>GGISLBD</i>	dI_{gisl}/dV_{bd}

State	Description
<i>QGSO</i>	Gate/Source overlap charge
<i>CGSO</i>	Gate/Source overlap capacitance
<i>QGDO</i>	Gate/Drain overlap charge
<i>CGDO</i>	Gate/Drain overlap capacitance
<i>QGBO</i>	Gate/Bulk overlap charge
<i>CGBO</i>	Gate/Bulk overlap capacitance
<i>VON</i>	Threshold voltage
<i>VDSAT</i>	Saturation voltage
<i>QBS</i>	Bulk/Source junction charge
<i>CAPBS</i>	Bulk/Source junction capacitance
<i>QBD</i>	Bulk/Drain junction charge
<i>CAPBD</i>	Bulk/Drain junction capacitance
<i>QG</i>	Intrinsic Gate charge
<i>QD</i>	Intrinsic Drain charge
<i>QS</i>	Intrinsic Source charge
<i>QB</i>	Intrinsic Bulk charge
<i>CBG</i>	*
<i>CBD</i>	*
<i>CBS</i>	*
<i>CGG</i>	*
<i>CGD</i>	*
<i>CGS</i>	*
<i>CDG</i>	*
<i>CDD</i>	*
<i>CDS</i>	*
<i>CSG</i>	*
<i>CSD</i>	*
<i>CSS</i>	*
<i>TOTNOISE</i>	Total noise
<i>THERMNOISE</i>	Thermal noise
<i>FLKNOISE</i>	Flicker noise



* C_{xy} refers to the derivative of the intrinsic charge on node x with respect to the voltage on node y .

Chapter 27

Surface-Potential-Based Compact MOSFET Model

1.0 Introduction

SP is a generic compact MOSFET model developed at The Pennsylvania State University. It is surface-potential-based, free from unphysical behavior often associated with more traditional models and contains a relatively small number of parameters. The HiSIM model is implemented in Eldo as LEVEL=67.

The development of SP is based on solution of several long standing problems of compact MOSFET modeling. Consequently SP is a surface potential based model that does not contain iterative loops or channel segmentation in both the intrinsic and the extrinsic submodels.

Features:

- F s-based, substrate referenced
- Analytical (non-iterative) computation of F s from accumulation to inversion
- Symmetric with respect to source-drain interchange, no gds derivative singularity
- Physically based modeling of small-geometry effects via lateral field gradient
- DC, quasi-static and non-quasi-static models are consistent
- Accumulation region modeling is physics-based

- F s-based modeling of the overlap regions
- Physics-based gate and substrate current models
- Simple expressions for key variables in all regions of operation, obtained using “symmetric linearization” concept
- Quantum mechanical effects and polysilicon depletion
- Thermal, 1/f and channel-induced gate noise models; “Excessive” thermal noise is physically modeled

2.0 Part I—Core Model

2.1 General Comments

This part contains a summary of the new surface-potential-based model SP [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18]. To simplify the presentation we exclude some minor details of the model implementation.

The main features of SP are as follows:

- SP is surface-potential-based.
- Surface potential is computed via extremely accurate non-iterative approximation valid in all regions of operation (including accumulation). There are no iteration loops anywhere in the program implementation.
- SP includes an engineering model of the bias dependence for the lateral field gradient, which traditionally is either neglected or is assumed to be bias-independent.
- Intrinsic charge model is based on the drain current model. Accumulation region [trans]capacitances are modeled physically.
- SP automatically satisfies benchmark tests including Gummel symmetry test. In order to accomplish this we use symmetric linearization of the bulk charge [3].

- Gm/Id ratio is modeled correctly. As a consequence SP produces correct simulation results for the R2R circuit.
- SP includes all major short-channel effects.

This summary describes the core model consisting of drain current and intrinsic charges. The extrinsic charge models, as well as noise and substrate current models are being developed right now and are not included.

In addition to the model summary this document includes a brief derivation of a simple model for the lateral gradient factor in “[Simple Model of the Lateral Gradient Factor](#)” on page 27-37 and some simulation results in “[Intrinsic Charges](#)” on page 27-20.

Terminology

Local model parameters: appear in the model formulation below. Some of them must be scaled with the device geometry. They are sufficient for representing device characteristics of a single transistor. SP core model contains 28 local parameters which are listed in “[Core Model Local Parameters](#)” on page 27-42.

Global model parameters: these include those of the local parameters which do not scale with geometry and the scaling parameters which are used to introduce the geometry dependence of the remaining local parameters. SP core model global parameters are listed in “[Core Model Global Parameters](#)” on page 27-43.

Note that some parameters are both local and global (e.g. MU0) and that only local parameters are used in the model formulation. This simplifies both the model description and the parameter extraction procedure.

The scaling equations are given in “[Scaling Equations](#)” on page 27-44.

2.2 Structure of the Core Model (Order of Computations)

- Compute fixed combinations of the model parameters
- Perform voltage conditioning

- Terminal flip (if $V_{ds} < 0$)
- V_{bs} , V_{bd} clamping to assure $V_{bs} < \phi_b$, $V_{bd} < \phi_b$
- Compute lateral gradient factor
- Compute surface potential ϕ_{ss} (at the source end of the channel) and related variables
- Compute effective drain-source voltage
- Compute ϕ , $\phi_{sd} = \phi_{ss} + \phi$
- Compute mid-point surface potential ϕ_m and related variables
- Introduce QM and polysilicon depletion corrections Evaluate drain current
- Compute intrinsic charges

2.3 Bias-Independent Variables

Thermal voltage

$$V_t = k_B T A B S / q$$

Oxide capacitance (corrected for narrow-channel effects)

$$C_{OX} = \epsilon_{OX} / T O X$$

Effective doping

$$N S U B = N S U B \left[1 + \frac{L P K T}{L_{mu}} (1 - e^{-L_{mu}/Y P K T}) \right]$$

Body factor

$$\gamma = \sqrt{2q\epsilon_{st}N S U B / C_{OX}}$$

Normalized body factor

$$G = \gamma / \sqrt{V_t}$$

Bulk potential

$$\phi_b = V_t \ln(NSUB/n_i)$$

Constant for computing effective vertical field

$$E_{eff0} = 10^{-8} \cdot C_{OX} / \epsilon_{si}$$

Variable used to introduce polysilicon depletion effect

$$kp = 2C_{OX}^2 V_t / q\epsilon_{si} NP$$

Variable used to introduce quantum correction

$$q_q = 16.1 QMC(TOX^2 \cdot 10^{20} \cdot V_t \cdot TABS)^{-1/3}$$

2.4 Additional Notations

Surface Potentials

ϕ_s = surface potential

ϕ_{ss} = surface potential at the source end of the channel

ϕ_{sd} = surface potential at the drain end of the channel

$$\phi = \phi_{sd} - \phi_{ss}$$

Normalized surface potentials

$$x = \phi_s / V_t$$

$$x_s = \phi_{ss} / V_t$$

$$x_d = \phi_{sd} / V_t$$

$$\varphi = \phi / V_t$$

Normalized gate bias

$$x_g = (V_{gb} - V_{fb}) / V_t$$

Functions

$$MINA(a, b, c) = \frac{1}{2}[a + b - \sqrt{(a - b)^2 + c}]$$

$$MAXA(a, b, c) = \frac{1}{2}[a + b + \sqrt{(a - b)^2 + c}]$$

$$\sigma(a, c, \tau) = \frac{a\upsilon}{\mu + \frac{\upsilon}{\mu}c\left(\frac{c^2}{3} - a\right)}$$

where

$$\upsilon = a + c$$

and

$$\mu = \frac{\upsilon^2}{\tau} + \frac{c^2}{2} - a$$

2.5 Lateral Gradient Factor

Traditionally, lateral gradient factor

$$f = 1 - \frac{\epsilon_{si}}{qNSUB} \left(\frac{\partial^2 \phi_s}{\partial y^2} + \frac{\partial^2 \phi_s}{\partial z^2} \right)$$

is either set to be 1 (gradual-channel approximation) or assumed to be bias-independent. In SP, we include the reduction of the lateral field gradient (i.e. the increase of f) with the surface potential via semi-empirical equation.

$$f = f_0(1 + B_f \phi_f)$$

where

$$f_0 = \frac{F_0}{1 + B_f V_{sbx1} + (C_f V_{dsx} + A_f V_{sbx1})(1 + DF \cdot C_f V_{dsx} + EF \cdot A_f V_{sbx1}) + g(V_{dsx})} + 0.01$$

where

$$g(V_{dsx}) = GDS1 \cdot V_{dsx}^2 + GDS2 \cdot \sqrt{V_{dsx}}$$

$$V_{dsx} = \sqrt{V_{ds}^2 + 0.01 - 0.1}$$

$$V_{sbx1} = MAXA(V_{sbx}, 0, 10^{-4})$$

$$V_{sbx} = V_{sb} + \frac{1}{2}(V_{ds} - V_{dsx})$$

The essential features of this expressions are (i) linear $f(\phi_f)$ dependence and (ii) decrease of f with V_{ds} and V_{bs} . A simple model leading to the equation for f above is presented in “[Simple Model of the Lateral Gradient Factor](#)” on page 27-37.

The functional form of V_{dsx} is motivated by the smoothing functions introduced in MOS9 and subsequently used in other compact models. Introduction of variable V_{dsx} and V_{sbx} assures:

$$\left(\frac{\partial f}{\partial V_{ds}} \right)_{V_{ds}=0} = 0$$

This condition is imposed in order to satisfy the Gummel symmetry test. For the same reason surface potential $\phi_f = x_f V_t$ corresponds to the imref splitting $\phi_n = V_{sbx}$ rather than to $\phi_n = V_{sb}$. A more subtle point is that ϕ_f is computed with less precision than surface potentials ϕ_{ss} and ϕ_{sd} . Indeed, evaluations of ϕ_{ss} and ϕ_{sd} requires that f be known (see “[Analytical Approximation for the Surface Potential](#)” on page 27-39). In contrast, ϕ_f has to be evaluated before f is computed.

It turns out that the following simple approximation for x_f is sufficient to account for the increase of f (i.e. the reduction of $\partial^2\phi_s/\partial y^2$) with the gate drive.

$$x_f = \eta_f + \sigma \left(\frac{a_f}{1 - B_t G^2}, \frac{c_f}{1 - B_t G^2}, \tau \right)$$

where

$$B_t = (f_0 - 0.01)B_f V_t$$

$$\eta_f = MINA(x_{subf}, \tilde{x}_o + 3, 5)$$

$$x_{subf} = \frac{x_{gc}^2}{x_{gc}^2 + \frac{1}{2}G^2 f_0 + G \left[B_t x_{gc}^2 + f_0 x_{gc} + \left(\frac{G f_0}{2} \right)^2 \right]^{1/2}}$$

$$x_{gc} = MAXA(x_g, 0, 50)$$

$$\tilde{x}_0 = (2\phi_b + V_{sbx})/V_t$$

$$\tau = \tilde{x}_0 - \eta_f + \ln(a_f/G^2)$$

$$a_f = (x_{gc} - \eta_f)^2 - G^2(f_0 + B_t \eta_f)$$

$$c_f = 2(x_{gc} - x_f) + G^2(f_0 + 2B_t \eta_f)$$

2.6 Surface Potential ϕ_{ss} (at the Source End of the Channel) and Related Variables

In “Analytical Approximation for the Surface Potential” on page 27-39, we present an approximate analytical solution for the surface potential in the form

$$x = \theta(V_{gb}, \phi_n)$$

where the normalized imref splitting

$$\phi_n = (F_p - F_n)/q$$

In particular

$$x_s = \theta(V_{gb}, V_{sb})$$

In the process of computing surface potential, the following variables are computed as well:

$$E_s = \exp(-x_s)$$

$$\Delta_s = \Delta_{ns}/(E_s)$$

$$D_s = (E_s^{-1} - E_s - 2x_s)\Delta_{ns}$$

where

$$\Delta_{ns} = \frac{1}{f} \exp(-x_{ns})$$

and

$$x_{ns} = (2\phi_b + V_{sb})/V_t$$

In the code, the evaluation of E_s , Δ_s and Δ_{ns} is carefully ordered to avoid over/underflow problems.

After evaluating surface potential x_s , one computes normalized inversion charge at the source

$$V_1 = \frac{G_f^2 V_t D_s}{x_{gs} + G_f S_s}$$

where

$$S_s = \sqrt{P_s}$$

$$P_s = x_s - 1 + E_s$$

$$x_{gs} = G_f \sqrt{D_s + P_s}$$

and

$$G_f = G \sqrt{f}$$

Note that while $x_{gs} = x_g - x_s$, using the equation for V_I above reduces the numerical noise for V_{gs} close to V_{fb} .

Series resistance

$$R_t = \frac{R_{t1}(1 + RB \cdot V_{sbx})}{1 + R_g V_1}$$

Series resistance factor

$$\rho = MU0(C_{OX}/L)R_t V_1$$

Effective vertical field

$$E_{eff} = E_{eff0}(q_b + \eta_\mu V_1)$$

$$q_b = V_t G_f S_s$$

where $\eta_\mu = 1/2$ for n-channel and $1/3$ for p channel MOSFET's.

Effective mobility at the source end of the channel

$$\mu_s = \frac{MU0 \cdot \mu_x}{1 + (\mu_E \cdot E_{eff})\theta_{MU} + CS \frac{q^2 b}{(V_1 + q_b)^2} + \rho}$$

The variable

$$\mu_s = (1 + X_{cor} \cdot V_{sbx}) / (1 + 0.2 X_{cor} \cdot V_{sbx})$$

where the term $(1 + X_{cor} \cdot V_{sbx})$ introduces non-universality essential for devices with significant Coulomb scattering. The denominator assures that μ_x does not exceed 5 for extreme (and unphysical) V_{sbx} that may occur during SPICE convergence process.



V_1 and μ_s are “temporary variables”. Eventually these will be changed to assure the symmetry of the model. Also, $\rho = 0$ if external model of series resistance is used.

2.7 Effective Drain-Source Voltage

“Saturation voltage”

$$V_{dsat} = \phi_{sat} - V_t \ln \left[1 + \frac{\phi_{sat}(\phi_{sat} - 2a_{sat}V_t)}{G_f^2 \Delta_s V_t^2} \right]$$

where

$$a_{sat} = x_{gs} + \frac{1}{2} G_f^2$$

In particular

$$\phi_{sat} = \frac{2\phi_0\phi_2}{\phi_0 + \phi_2 + \sqrt{(\phi_0 + \phi_2)^2 - 3.96\phi_0\phi_2}}$$

$$\phi_2 = \frac{V_t G_f^2 \Delta_s S_0}{a_{sat} + \sqrt{a_{sat}^2 - G_f^2 \Delta_s S_0}}$$

$$\phi_0 = \psi_0 \frac{V_c + \frac{V_2}{4} + \psi_0 \left(\frac{1}{8} + \frac{\delta^2}{2} \right)}{V_c + V_2 \delta (1 - \delta) + \psi_0 \delta^2}$$

$$\delta = \frac{\Psi_0}{\Psi_0 + A_s V_c}$$

$$\Psi_0 = \frac{2V_2}{1 + \frac{V_2}{4V_c} + \sqrt{1 + \frac{V_2}{V_c} + \left(\frac{V_2}{4V_c}\right)^2}}$$

$$V_2 = (V_1/\alpha_s) + V_t$$

$$V_c = \frac{u_{sat}L}{\mu_s}$$

$$u_{sat} = \frac{VSAT}{1 + K_{sm} \cdot w_{sat}}$$

$$w_{sat} = \frac{100V_1(1 + STX \cdot V_{sbx})}{100 + V_1(1 + STX \cdot V_{sbx})}$$

and

$$\alpha_s = 1 + \frac{G_f(1 - E_s)}{2S_s}$$

Effective drain-source voltage

$$V_{dsc} = \frac{V_{ds}}{\left[1 + (V_{ds}/V_{dsat})a_x\right]^{1/a_x}}$$

2.8 Surface Potential ϕ_{ss} (at the Drain End of the Channel) and Related Variables

Surface potential at the drain end of the channel $\phi_{sd} = x_d V_t$ where

$$x_d = \theta(V_{gb}, V_{sb} + V_{dse})$$

However, as a matter of convenience we use the above equation only when

$$x_g > x_{g23} = G \sqrt{f_{23}(x_{23} - 1)}$$

where

$$f_{23} = f_0 + B_t x_{23}$$

and

$$x_{23} = \begin{cases} (\phi + V_{sb})/V_t & \text{for } V_{sb} \geq 0 \\ (\phi_b + 0.5V_{sb})/V_t & \text{for } V_{sb} < 0 \end{cases}$$

For $x_g < x_{g23}$, it is more efficient to compute x_s then determine normalized drain-source surface potential difference $\varphi = \phi/V_t$ and finally compute $x_d = x_s + \varphi$. An approximate analytical solution for φ in the region $x_g < x_{g23}$ is given in “Evaluation of $\phi = \phi_{sd} - \phi_{ss}$ for $x_g < x_{g23}$ ” on page 27-41.

In the process of computing surface potential x_d , the following variables are computed as well:

$$E_d = \exp(-x_d)$$

$$D_d = (E_d^{-1} - E_d - 2x_d)\Delta_{nd}$$

where

$$\Delta_{nd} = \frac{1}{f} \exp(-x_{nd})$$

$$x_{nd} = (2\phi_b + V_{sb} + V_{dse})/V_t$$

2.9 Mid-Point Surface Potential ϕ_m and Related Variables

Midpoint (subscript “m”) is defined as corresponding to a surface potential

$$\phi_m = \frac{1}{2}(\phi_{ss} + \phi_{sd})$$

The following variables are used

$$x_m = \frac{1}{2}(x_s + x_d)$$

$$E_m = \sqrt{E_s E_d}$$

$$D_m = \frac{1}{2}(D_s + D_d) + \frac{1}{8}\varphi^2 \left(E_m - \frac{2}{G_f^2} \right)$$

$$P_m = x_m - 1 + E_m$$

$$x_{gm} = G_f \sqrt{D_m + P_m}$$

and

$$S_m = \sqrt{P_m}$$

Normalized inversion charge

$$V_m = \frac{G_f^2 V_t D_m}{x_{gm} + G_f S_m}$$

Linearization coefficient

$$\alpha = 1 + \frac{G_f(1 - E_m)}{2S_m}$$

Series resistance

$$R_t = \frac{R_{t1}(1 + RB \cdot V_{sbx})}{1 + R_g V_m}$$

Series resistance factor

$$\rho = MU0(C_{OX}/L)R_t V_m$$

Effective vertical field

$$E_{eff} = E_{eff0}(q_b + \eta_\mu V_m)$$

$$q_b = V_t G_f S_m$$

where $\eta_\mu = 1/2$ for n-channel and $1/3$ for p channel MOSFETs.

Effective mobility

$$\mu_m = \frac{MU0 \cdot \mu_x}{1 + (\mu_E \cdot E_{eff})^{\theta_{MU}} + Cs \frac{q_b^2}{(V_m + q_b)^2} + \rho}$$

2.10 Quantum-Mechanical Corrections

In SP quantum-mechanical (QM) correction are introduced based on the method described in “Additional Notations” on page 27-5. The difference is that in “Additional Notations” on page 27-5 we have only considered the most common case $\phi_s \geq 3V_t$ which is of interest for the charge-sheet models. The equations given below are conditioned for a wide voltage range. Furthermore, we develop QM corrections directly for $x_m = \phi_m/V_t$ and $\varphi = (\phi_{sd} - \phi_{ss})/V_t$. This is preferable to correcting ϕ_{ss} and ϕ_{sd} , especially in the case when φ is a small difference of two larger variables. In what follows superscript “(0)” refers to variables uncorrected for QM effects.

For

$$x_g \geq 0 \text{ (i.e. for } V_{gb} \geq V_{fb})$$

$$x_m = x_m^{(0)} + v_{QM}$$

and

$$\varphi = \varphi^{(0)} \frac{k_m(\bar{D} + d_0)}{d + k_m \bar{D} a_{QM}}$$

where

$$u_{QM} = \frac{q_{QM}}{p_{QM} - q_{QM}/p_{QM}}$$

$$q_{QM} = G_f^2 D_m^{(0)} \Delta e'_g$$

$$\Delta e'_g = g_{QMP} \Delta e_g$$

$$\Delta e_g = q_q x_{gm}^{2/3}$$

$$g_{QMP} = \frac{D_m^{(0)}}{D_m^{(0)} + P_m^{(0)}}$$

$$p_{QM} = 2x_{gm} + G_f^2 [1 - E_m^{(0)} + D_m^{(0)} a_{QM}]$$

$$a_{QM} = 1 + \frac{2\Delta e'_g}{3x_{gm}}$$

$$k_m = \exp(a_{QM} u_{QM} - \Delta e'_g)$$

$$\bar{D} = \frac{D_s + D_d}{2}$$

$$d_0 = 1 - E_m^{(0)} + 2x_{gm} G_f^2$$

$$d = d_0 + (E_m^{(0)} - 2/G_f^2) u_{QM}$$

For $x_g < 0$

$$x_m = x_m^{(0)} - \frac{\Delta e'_g \phi_m^2}{\phi_m^2 + \frac{0.04}{1 + 3|\phi_m|}}$$

There is no correction for ϕ . This form is introduced to eliminate the singularity or unphysical behavior near $V_{gb} = V_{fb}$. Coefficients 0.04 and 3 are not affected by model parameters and are fixed. In addition to correcting ϕ_m and x_m , QM effects are introduced into

$$D_m = k_m D_m^{(0)}$$

and variables P_m , x_{gm} , which are given by expressions above but with x_m corrected for QM effects.

2.11 Polysilicon Depletion

In SP polysilicon depletion is described essentially using the technique of “Structure of the Core Model (Order of Computations)” on page 27-3. The equations are conditioned to provide smooth device characteristics for a wide voltage range but at present the poly effects are only included for $v_{gb} > V_{fb}$. The normalized poly surface potential at midpoint

$$x_{pm} = k_p \left[\frac{x_{gm}^{(0)}}{1 + \eta_p^{-1}} \right]^2$$

where k_p is given in section “Bias-Independent Variables” on page 27-4 and

$$\eta_p = [1 + k_p x_{gm}^{(0)}]^{-1/2}$$

In this section superscript “(0)” indicates that the variable is not corrected for poly depletion effect. As in section “Quantum-Mechanical Corrections” on page 27-15, poly corrections are introduced into $x_m = \phi_m / V_t$ and $\phi = (\phi_{sd} - \phi_{ss})$ rather than into ϕ_{ss} and ϕ_{sd} directly. The corrected midpoint surface potential is

$$x_m = x_m^{(0)} + u_p$$

where

$$u_p = \frac{q}{p - q/p}$$

$$p = 2[x_{gm}^{(0)} - x_{pm}] + G_f^2[1 - E_m^{(0)} + D_m^{(0)}]$$

and

$$q = x_{pm}[x_{pm} - 2x_{gm}^{(0)}]$$

The correction to normalized surface potential difference φ is as follows

$$\varphi = \varphi^{(0)} \frac{k_m(d_0 + \bar{D})}{d + k_m \bar{D}}$$

where d_0 with a different meaning of “(0)” as explained above,

$$d = 1 - E_m^{(0)} - 2\eta_p x_{gm} / G_f^2$$

$$k_m = \exp(u_p)$$

In addition to changing the surface potentials, poly correction affects the linearization of inversion charge and intrinsic charges. The expressions in sections 12 and 13 include these corrections. The case of no poly effect can be recovered by setting $\eta_p = 1$. While physically this corresponds to NP tending to ∞ , in SP eliminating poly effects is formally prescribed by setting NP = 0 in the parameter file.

2.12 Drain Current Computation

Velocity saturation factor L_{sat}

$$V_c = L_{eff} \mu_{sat} / \mu_m$$

$$u_{sat} = \frac{VSAT}{1 + K_{sm} w_{sat}}$$

$$w_{sat} = \frac{100 V_m (1 + STX \cdot V_{sbx})}{100 + V_m (1 + STX \cdot V_{sbx})}$$

This form assures that $w_{sat} < 100$ and $u_{sat} > 0.3 VSAT$ during convergence process where V_m can be unphysically high.

$$\delta = \frac{\phi}{\phi + A_s V_c}$$

$$L_{sat} = \frac{\delta \phi \mu_m}{u_{sat}}$$

Channel length modulation factor L_{CLM}

$$L_{CLM} = \delta L_{q2d} \ln[1 + CLM3 \cdot (V_{ds} - \phi)]$$

Drain current

$$I_d = \frac{\mu_m W C_{OX} (V_m + \alpha V_t) \phi}{L_{red} + L_{sat}}$$

where the inversion charge linearization (including polysilicon depletion effect)

$$\alpha = \eta_p + \frac{G_f (1 - E_m)}{2 S_m}$$

and the “reduced channel length”

$$L_{red} = \frac{L}{1 + L_{CLM}/L}$$

2.13 Intrinsic Charges

All charges are normalized to WLC_{ox}

Gate charge

$$Q_G = x_{gm} V_t + \frac{\eta_p \phi}{2} \left(\frac{\phi r_L}{6H} - 1 + r_L \right)$$

where

$$H = \frac{V_m/\alpha + V_t}{1 + L_{sat}/L_{red}}$$

and

$$r_L = L_{red}/L$$

Inversion layer charge

$$|Q_I| = r_L (V_m + \alpha \phi^2 / 12H) + Q_{CLM}$$

$$Q_{CLM} = (1 - r_L)(V_m - 0.5\alpha\phi)$$

Drain charge (computed using Ward-Dutton partition)

$$|Q_D| = \frac{1}{2} r_L^2 \left\{ V_m - \frac{\alpha \phi}{6} \left[1 - \frac{\phi}{2H} - \frac{1}{5} \left(\frac{\phi}{2H} \right)^2 \right] \right\} + \frac{1}{2} Q_{CLM} (1 + r_L)$$

Source charge

$$|Q_s| = |Q_I| - |Q_D|$$

Bulk charge

$$|Q_B| = Q_G - |Q_I|$$

2.14 Examples (Simulation Results)

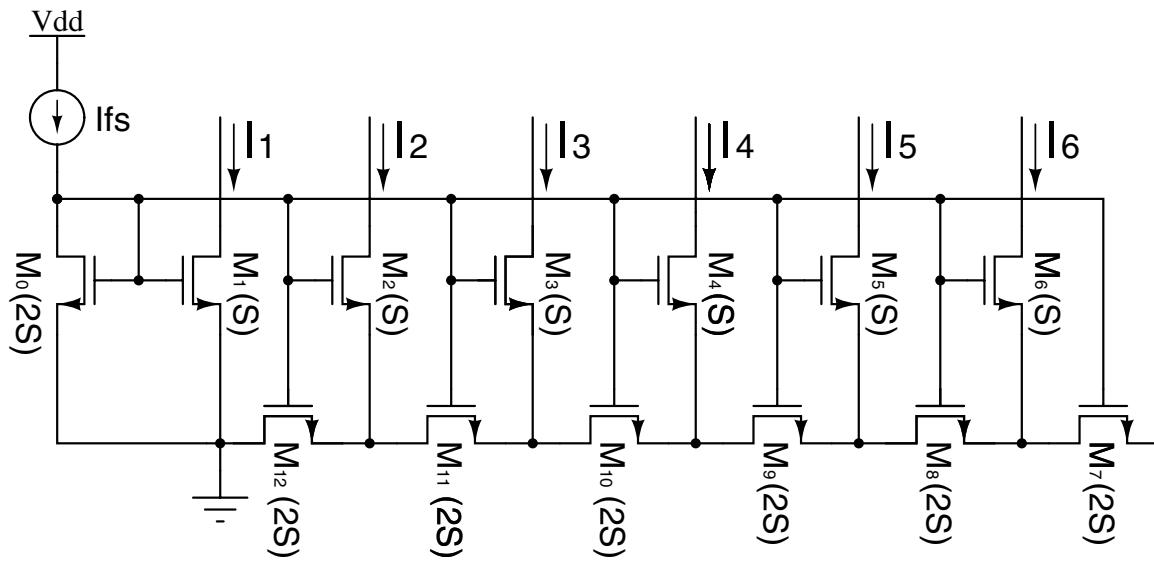


Figure 27-1. R2R Circuit

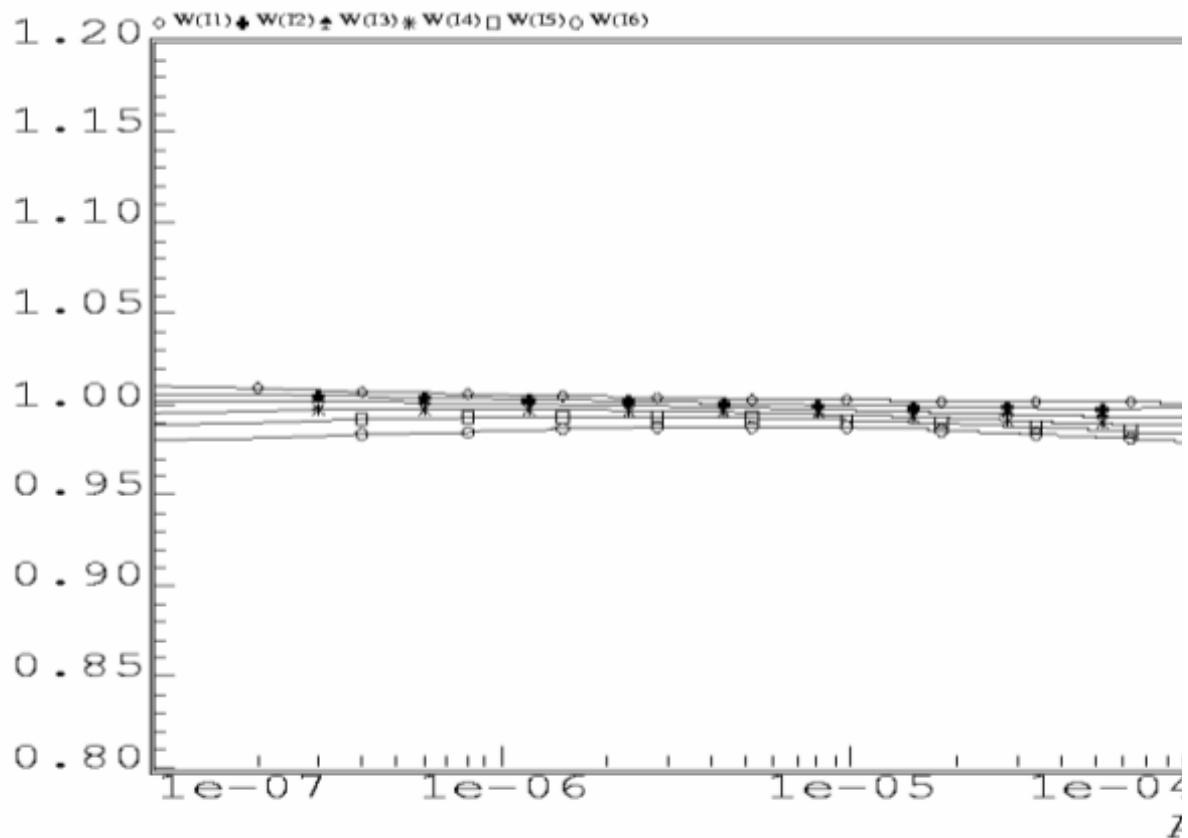
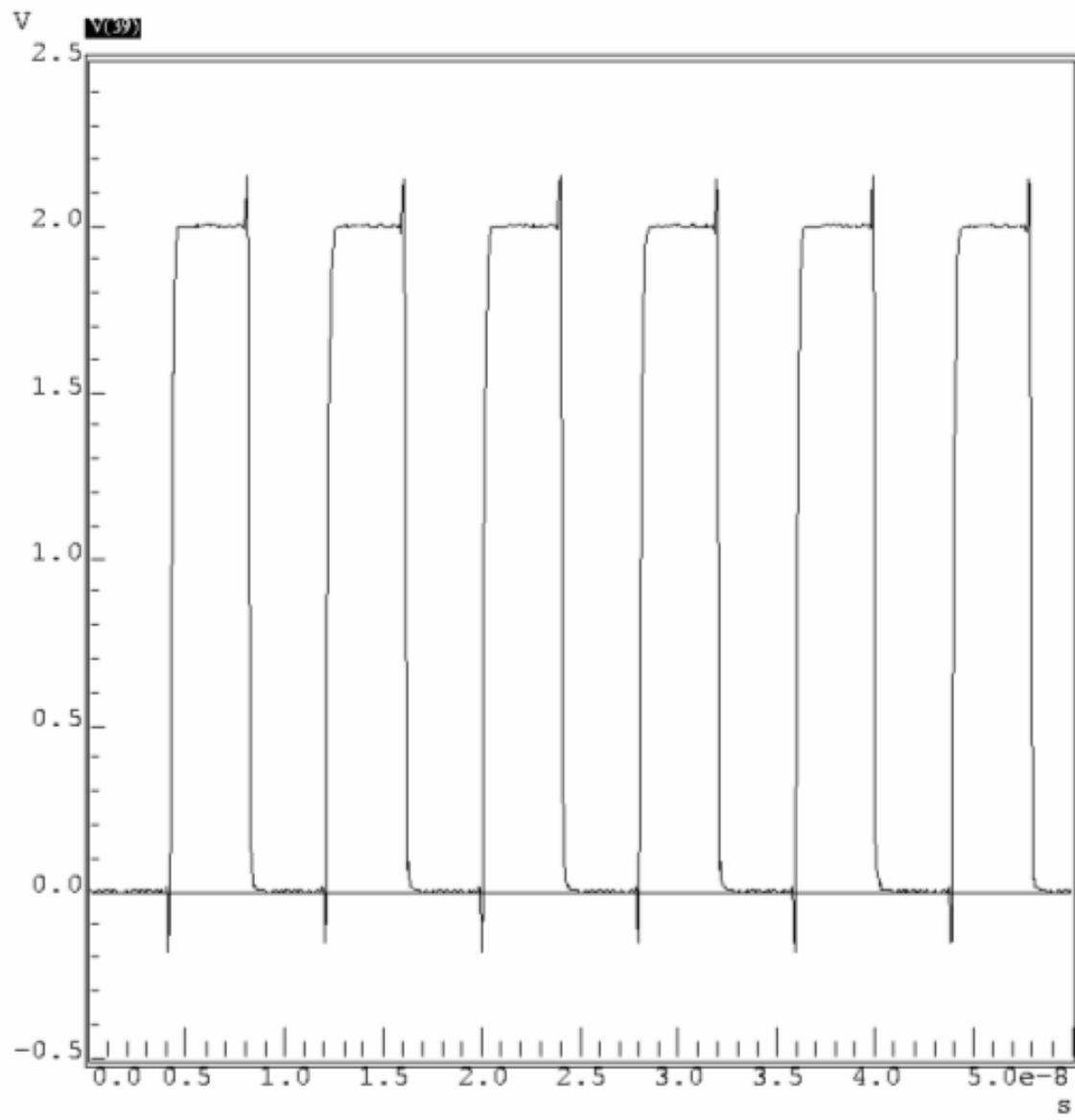


Figure 27-2. Simulation results for R2R Circuit. Different curves correspond to I_1/I_{fs} , $2I_2/I_{fs}$, ..., $2^6I_6/I_{fs}$. $W/L=8/30\mu m$, $16/30\mu m$



**Figure 27-3. Simulation results for a 39-stage ring oscillator
W/L=0.6/0.2 μ m**

3.0 Part II—Extrinsic Model

3.1 General Comments

This part summarizes the extrinsic SP model, which at present includes overlap charges, gate current, substrate current, and noise sources models. The main features of the SP extrinsic model are as follows:

- The surface potential in the overlap regions is evaluated using a newly developed streamlined analytical approximation.
- The physical modelling of the overlap charge is enabled by the availability of the surface potential in the overlap regions.
- Gate current model is physically based.
- A new formulation of the substrate current is developed to achieve the asymptotically correct behavior in the subthreshold region without using smoothing functions.
- The description of parameters, variables, and other notations in the summary of the intrinsic model is not repeated in this document.

3.2 Bias-Independent Variables

Overlap capacitance

$$C_{oxov} = \epsilon_{ox}/TOXOV$$

Overlap body factor

$$\gamma_{ov} = \sqrt{2q\epsilon_{Si}NOV/C_{oxov}}$$

Normalized overlap body factor

$$G_{ov} = \gamma_{ov}/\sqrt{V_t}$$

Tunnelling current density constant

$$J_0 = \frac{qm_0 k_B^2 TABS^2}{2\pi^2 h^3} = 1.082 \times 10^{11} \times \left(\frac{TABS}{300}\right)^2$$

Channel tunnelling current density exponential constant (dimensionless)

$$B = 2TOX(2qm_0 X_B)^{1/2}/h = 6.831 \times 10^9 TOX \sqrt{X_B}$$

Overlap tunnelling current density exponential constant (dimensionless)

$$B_{ov} = 2TOXOV(2qm_0 X_B)^{1/2}/h = 6.831 \times 10^9 TOXOV \sqrt{X_B}$$

Auxiliary variable of gate current model

$$\alpha_b = E_g/(2q) + \phi_b$$

The Si/SiO₂ conduction band o.set, $X_B = 3.1\text{V}$.

3.3 Additional Notations

ϕ_{sov} surface potential in the source overlap region

ϕ_{dov} surface potential in the drain overlap region

$V_{oxm} = V_{gd} - V_{fb} - \phi_m$ oxide voltage in the potential mid-point

$V_{oxovs} = V_{gd} - \phi_{dov}$ oxide voltage in the source overlap region

$V_{oxovd} = V_{gd} - \phi_{dov}$ oxide voltage in the drain overlap region

3.4 Streamlined Surface Potential Approximation

The availability of the surface potential in the overlap regions is essential to the physical modelling of the charge and gate current components. In this section, a streamlined analytical approximation of the surface potential is presented. It excludes the effects of minority carriers and consequently is even simpler and more efficient than the one employed in the channel region.

In what follows,

$$\xi = 1 + G_{ov}/\sqrt{2}$$

and

$$x_{margin} = 10^{-7}\xi$$

For $|x_g| \leq x_{margin}$

$$x = x_g/\xi$$

For $x_g < -x_{margin}$ proceed in the following steps,

$$y_g = -x_g$$

$$z = 1.25y_g/\xi$$

$$\eta = (1/2)\left\{z + 10 - [(z - 6)^2 + 64]^{1/2}\right\}$$

$$a = (y_g - \eta)^2 + G_{ov}^2(\eta + 1)$$

$$c = 2(y_g - \eta) - G_{ov}^2$$

$$\tau = -\eta + \log(a/G_{ov}^2)$$

$$y_0 = \eta + \sigma(a, c, \tau)$$

$$\Delta_0 = \exp(y_0)$$

$$p = 2(y_g - y_0) + G_{ov}^2(\Delta_0 - 1)$$

$$q = (y_g - y_0)^2 + G_{ov}^2(y_0 - \Delta_0 + 1)$$

$$x = -y_0 - \frac{2q}{p + \sqrt{p^2 - 2q(2 - G_{ov}^2 \Delta_0)}}$$

For $x_g > x_{margin}$ compute

$$x_1 = 1.25$$

$$x_{g1} = x_1 + G_{ov} \sqrt{\exp(-x_1) + x_1 - 1}$$

$$\bar{x} = (x_g/\xi)[1 + x_g(\xi x_1 - x_{g1})/x_{g1}^2]$$

$$\bar{E} = \exp(\bar{x})$$

$$\omega = 1 - \bar{E}$$

$$x_0 = x_g + G_{ov}^2/2 - G_{ov}(x_g + G_{ov}^2/4 - \omega)^{1/2}$$

$$\Delta_1 = \exp(-x_0)$$

$$p = 2(x_g - x_0) + G_{ov}^2(1 - \Delta_1)$$

$$q = (x_g - x_0)^2 + G_{ov}^2(x_0 + \Delta_1 - 1)$$

$$x = \frac{2q}{p + \sqrt{p^2 - 2q(2 - G_{ov}^2 \Delta_1)}}$$

In the code, the evaluation of Δ_0 and Δ_1 is carefully ordered to avoid over/underflow problems.

3.5 Extrinsic Charge Model

The source and drain overlap regions are modelled as MOS capacitors.

The charge of the source overlap region

$$Q_{sov} = W_{eff} \cdot LOV \cdot C_{oxov}(V_{gs} - \phi_{sov})$$

The charge of the drain overlap region

$$Q_{dov} = W_{eff} \cdot LOV \cdot C_{oxov}(V_{gd} - \phi_{dov})$$

The charge of the bulk overlap region

$$Q_{bov} = L_{eff} \cdot CGBO \cdot V_{gb}$$

Inner fringe charge correction

$$\Delta Q_G = \Delta Q_s - \Delta Q_D$$

$$\Delta Q_s = IFKJ(1 + IFCJV_{sb})(IFVBI + V_{sb} - \phi_{ss})^{1/2}$$

$$\Delta Q_D = IFKJ(1 + IFCJV_{db})(IFVBI + V_{db} - \phi_{sd})^{1/2}$$

Outer fringe charge

$$Q_{ofs} = W_{eff} \cdot CF \cdot V_{gs}$$

$$Q_{ofd} = W_{eff} \cdot CF \cdot V_{gd}$$

The terminal charges are given by

$$Q_G = Q_G^{(i)} + Q_{sov} + Q_{dov} + \Delta Q_G + Q_{ofs} + Q_{ofd}$$

$$Q_S = Q_s^{(i)} - Q_{sov} + \Delta Q_S - Q_{ofs}$$

$$Q_D = Q_D^{(i)} - Q_{dov} + \Delta Q_D - Q_{ofd}$$

where superscript (i) indicates the value given by the intrinsic (“core”) SP model.

3.6 Gate Current Model

The tunnelling gate current of MOSFET is physically modeled. The total gate current (I_g) is given by,

$$I_g = I_{gc} + I_{gsov} + I_{gdov}$$

Channel contribution

$$I_{gc} = I_{gc0} i_{gc}$$

$$I_{gc0} = W_{eff} L_{eff} J_{gc}$$

$$J_{gc} = J_0 F_s \exp \left\{ B \left[-GC1 + \frac{U_{oxm}}{X_B} \left(GC2 + \frac{GC3 \cdot U_{oxm}}{X_B} \right) \right] \right\}$$

$$U_{oxm} = \sqrt{V_{oxm}^2 + 10^{-6}}$$

Here, F_s is the supply function describing the difference of the population of carriers across the oxide in the mid-potential point, given by

$$F_s = \ln \left[\frac{1 + \Delta_{Si}}{1 + \Delta_{Si} \exp(-V_{gs}/V_t)} \right]$$

$$\Delta_{Si} = \exp[(\phi_{ss} - \alpha_b - V_x + \psi_t)/V_t]$$

$$\psi_t = MINA(0, V_{ox} + D, 0.001)$$

$$D = GC0 \cdot V_t$$

$$i_{gc} = (1 - b) \frac{\sinh(x)}{x} + b \cosh(x) \quad (b)$$

$$x = \phi/(2u_0)$$

$$b = u_0/H$$

$$u_0 = X_B / (GC2 + 2GC3 \cdot U_{oxm} / X_B)$$

Source-drain partition

The partition of the gate current in the channel area into the source and drain is essential for the MOSFET compact modelling, which is accomplished in SP using the symmetrical linearization method. The drain portion is given by

$$I_{gcd} = I_{gc0} i_{gcd}$$

$$i_{gcd} = \frac{i_{gc}}{2} - B_g \sinh(x) - A_g \frac{\sinh(x)}{x} \left[\coth(x) - \frac{1}{x} \right] \quad (c)$$

$$A_g = (1 - 3b + 3b^2)/2$$

$$B_g = b(1 - b)/2$$

and the source portion is given by

$$I_{gcs} = I_{gc} - I_{gcd}$$

The Equations for i_{gc} and i_{gcd} above are written in a form that shows that there are no singularity at $x = 0$. Their implementation in the code is simpler and more efficient.

Source overlap region contribution

$$I_{gssov} = W_{eff} \cdot LOV \cdot J_{gssov}$$

$$J_{gssov} = J_0 F_{sov} \exp \left\{ B_{ov} \left[-GC1 + \frac{U_{oxovs}}{X_B} \left(GC2 + \frac{GC3 \cdot U_{oxovs}}{X_B} \right) \right] \right\}$$

$$U_{oxovs} = \sqrt{V_{oxovs}^2 + 10^{-6}}$$

The supply function, F_{sov} , describing the difference of the population of carriers across the oxide in the source overlap region, given by

$$F_{sovs} = \ln \left[\frac{1 + \Delta_{Siovs}}{1 + \Delta_{Siovs} \exp(-V_{gs}/V_t)} \right]$$

$$\Delta_{Siovs} = \exp[(3.0 + \phi_{sov} + \psi_{tovs})/V_t]$$

$$\psi_{tovs} = MINA(0, V_{oxovs} + GC0 \cdot V_t, 0.01)$$

Drain overlap region contribution

$$I_{gdov} = W_{eff} \cdot LOV \cdot J_{gdov}$$

$$J_{gdov} = J_0 F_{sovd} \exp \left\{ B_{ov} \left[-GC1 + \frac{U_{oxovd}}{X_B} \left(GC2 + \frac{GC3 \cdot U_{oxovd}}{X_B} \right) \right] \right\}$$

$$U_{oxovd} = \sqrt{V_{oxovd}^2 + 10^{-6}}$$

The supply function, F_{sovd} , describing the difference of the population of carriers across the oxide in the drain overlap region, given by

$$F_{sovd} = \ln \left[\frac{1 + \Delta_{Siovd}}{1 + \Delta_{Siovd} \exp(-V_{gd}/V_t)} \right]$$

$$\Delta_{Siovd} = \exp[(3.0 + \phi_{dov} + \psi_{toud})/V_t]$$

$$\psi_{toud} = MINA(0, V_{oxovd} + GC0 \cdot V_t, 0.01)$$

By setting $SW_IGATE \neq 1$, gate current model is turned off.

3.7 Substrate Current Model

The substrate current of MOSFET due to impact ionization is given by

$$I_b = iia_1 \exp[-iia_2/(V_{ds} - iia_3\phi)] \cdot I_d$$

$$iia_1 = IIA1 + IIA1L(1/LREF - 1/L_{eff})$$

$$ii a_2 = IIA2[1 + ii a_4(\sqrt{V_x + 2\phi_b} - \sqrt{2\phi_b})]$$

$$ii a_3 = IIA3 + IIA3L(1/LREF - 1/L_{eff})$$

$$ii a_4 = IIA4 + IIA4L(1/LREF - 1/L_{eff})$$

3.8 Total Terminal Currents

The effects of I_b and I_g on the gate, source, drain and body components are as follows

$$I_G = I_{gc} + I_{gsov} + I_{gdov}$$

$$I_S = I_S^{(i)} - (1 - IIPARTITION)I_b - I_{gcs}S_g(x_g) - I_{gsov}$$

$$I_D = I_D^{(i)} + I_b - I_{gcd}S_g(x_g) - I_{gdov}$$

$$I_B = I_B^{(i)} - IIPARTITION \cdot I_b - I_{gc}(1 - S_g(x_g))$$

where $I_S^{(i)}$, $I_D^{(i)}$ and $I_B^{(i)}$ are terminal currents produced by the intrinsic (“core”) SP model and

$$S_g(x_g) = \frac{1}{2} \left(1 + \frac{x_g}{\sqrt{X_g^2 + \epsilon}} \right)$$

The computation of the impact ionization current can be turned on/off by setting parameter SW_IMPACT.

3.9 Noise

Channel thermal noise

$$S_{I_d^2} = \frac{4k_B \cdot TABS}{L_{red}^2} \left(\mu_m Q_{inv} + NDELT A \frac{I_d \phi}{E_{crit}^2} \right)$$

$$Q_{inv} = W_{eff} L_{eff} C_{ox} (Q_I - Q_{CLM})$$

$$E_{crit} = VSAT / \mu_m$$

Flicker noise

$$S_{I_d^2}(f) = S_{I_d^2}(drift) + S_{I_d^2}(diff)$$

$$S_{I_d^2}(drift) = \frac{C_{ox} \phi_t I_d \mu_m}{\alpha_m \gamma_{FN} L_{red}^2 f^{NEF}}$$

$$\{ [NOIC \cdot (V_m - 2 \cdot V_*) + B^* - u_n V_*] \alpha_m \phi$$

$$+ (A^* - 2B^* \cdot V_* + 3 \cdot NOIC \cdot V_*^2) \ln(q_+/q_-) \}$$

$$S_{I_d^2}(drift) = \frac{C_{ox} \phi_t I_d \mu_m \phi_t}{\gamma_{FN} L_{red}^2 f^{NEF}}$$

$$[(NOIC + u_n) \alpha_m \phi + (B^* - 2 \cdot NOIC \cdot V_*) \ln(q_+/q_-)]$$

$$\gamma_{FN} = 10^{10} [m^{-1}]^{-1}$$

$$V_* = \phi_t \left(1 + \frac{G}{2 \sqrt{x_m + 10^{-6}}} \right)$$

1. In BSIM3 model, $\gamma_{FN} = 10^8 \text{ m}^{-1}$, whereas in BSIM4, $\gamma_{FN} = 10^{10} \text{ m}^{-1}$
 $\text{NOIA}_{SP} = \text{NOIA}_{BSIM4} = 10^2 \text{NOIA}_{BSIM3}$
 $\text{NOIB}_{SP} = \text{NOIB}_{BSIM4} = 10^2 \text{NOIB}_{BSIM3}$
 $\text{NOIC}_{SP} = \text{NOIC}_{BSIM4} = 10^2 \text{NOIC}_{BSIM3}$

$$A^* = NOIA \cdot q^2 / C_{ox}^2$$

$$B^* = NOIB \cdot q / C_{ox}$$

$$u_n = (A^* - B^* V_* + NOIC \cdot V_*^2) / (q_+ q_-)$$

$$q_+ = \frac{(V_*)}{2} + V_m + \alpha_m \phi$$

$$q_- = \frac{(V_*)}{2} + V_m - \alpha_m \phi$$

Series resistances thermal noise

$$S_{R_D} = 4kT/r_{drain}$$

$$S_{R_S} = 4kT/r_{source}$$

$$S_{R_G} = 4kT/r_{gate}$$

where

$$r_{drain} = RSH \cdot NRD$$

$$r_{source} = RSH \cdot NRS$$

$$r_{gate} = RGSH \frac{W_{drawn}}{L_{drawn} \cdot NF}$$

Channel induced gate noise

$$S_{I_G^2} = DV DZ \cdot \frac{TABS \cdot 16k_B \pi^2 f^2 W_{eff} C_{ox} L_{red}^3}{\mu_m \alpha_m H^3} \left[\frac{\phi^4}{1728H^2} - \phi^2 \left(\frac{1}{720} + \frac{H}{144H} \right) + \frac{HH}{12} \right]$$

where

$$H = \frac{V_m/\alpha - V_t L_{sat}/L_{red}}{1 + L_{sat}/L_{red}}$$

Cross correlation coefficient

$$S_{I_g I_d} = j \frac{TABS \cdot 8k_B \pi f W_{eff} C_{ox} L_{red}}{H^2} \left(\frac{H\phi}{12} - \frac{\phi^3}{144H} \right)$$

$$c = \frac{S_{I_g I_d}}{\sqrt{S_{I_g}^2 \cdot S_{I_d}^2}}$$

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5.0 Simple Model of the Lateral Gradient Factor

We present a motivation behind the equation for f in “Lateral Gradient Factor” on page 27-6. Assuming position independent

$$f = 1 - \frac{\epsilon_{si}}{qNSUB} \frac{\partial^2 \phi_s}{\partial y^2}$$

is equivalent to a parabolic $f(y)$ dependence

$$\phi_s = a(y - y_0)^2 + \phi_f$$

where a , y_0 and ϕ_f are functions of the terminal voltages and

$$f = 1 - \frac{2\epsilon_{si}a}{qNSUB}$$

With reference to boundary conditions

$$\phi_s(0) = V_{sb} + V_{bi}$$

$$\phi_s(L) = \phi_s(0) + V_{ds}$$

one finds

$$a = \frac{\xi}{L^2} \left(2 + \frac{V_{ds}}{\xi} + 2 \sqrt{1 + \frac{V_{ds}}{\xi}} \right)$$

where

$$\xi = V_{sb} + V_{bi} - \phi_f$$

In view of the approximate nature of this analysis it is appropriate to linearize $a(V_{ds})$ dependence by neglecting V_{ds} under the square root in the equation for a above. This preserves correct form for both $V_{ds} = 0$ and for $V_{ds} \gg \xi$. Then from the equation for f above

$$f = 1 - \frac{8\epsilon_{si}}{qN_{sub}L^2} \left(V_{sb} + V_{bi} - \phi_f + \frac{V_{ds}}{4} \right)$$

This is equivalent to the equation for f in “[Lateral Gradient Factor](#)” on page 27-6 with

$$f_0 = 1 - \frac{8\epsilon_{si}}{qN_{sub}L^2} \left(V_{sb} + V_{bi} + \frac{V_{ds}}{4} \right)$$

and

$$F_0 B_f = \frac{8\epsilon_{si} V_t}{qN_{sub}L^2}$$

A simple derivation presented here ignores the $f(W)$ dependence $\left[\frac{\partial^2 \phi_s}{\partial z^2} \right]$ term is dropped in the first equation for f above] and predicts a rather simple $f(L)$ dependence. This necessitates the introduction of empirical factors in section 5. In addition, variables x_f , V_{sbx} and V_{dsx} were introduced to satisfy the Gummel symmetry test. However, the main feature of the last equation for f above which is a linear $f(\phi_f)$ dependence is quite physical and is implemented in SP. The decrease

of f with V_{ds} and V_{sb} predicted by the equation for f_0 above is linear and may result in negative f for large V_{ds} and V_{sb} . Hence the function form of f_0 is changed to the equation for f_0 in “[Lateral Gradient Factor](#)” on page 27-6 in order to assure $f_0 > 0$ for arbitrary large terminal voltages.

6.0 Analytical Approximation for the Surface Potential

The results presented here extend our earlier work to arbitrary V_{gs} . In what follows

$$\xi = 1 + \frac{G_f}{\sqrt{2}}$$

x_{g23} and x_{23} are given by equations for x_g and x_{23} in “[Surface Potential \$\phi_{ss}\$ \(at the Drain End of the Channel\) and Related Variables](#)” on page 27-12.

For $|x_g| < x_{margin}$

$$x = x_g / \xi$$

For $x_g < -x_{margin}$, proceed in the following steps

$$y_g = -x_g$$

$$z = 1.25y_g / \xi$$

$$\eta = (1/2) \left\{ z + 10 - [(z - 6)^2 + 64]^{1/2} \right\}$$

$$a = (y_g - \eta)^2 + G_f^2(\eta + 1)$$

$$c = 2(y_g - \eta) - G_f^2$$

$$\tau = -\eta + \ln(a/G_f^2)$$

$$y_0 = \eta + \sigma(a, c, \tau)$$

$$\Delta_0 = \exp(y_0)$$

$$\Delta_1 = 1/\Delta_0$$

$$p = 2(y_g - y_0) + G_f^2[\Delta_0 - 1 + \Delta_n(2 - \Delta_0 - \Delta_1)]$$

$$q = (y_g - y_0)^2 + G_f^2[y_0 - \Delta_0 + 1 + \Delta_n(\Delta_0 - \Delta_1 - 2y_0)]$$

$$x = -y_0 - \frac{2q}{p + \sqrt{p^2 - 2q\{2 - G_f^2[\Delta_0 + \Delta_n(\Delta_1 - \Delta_0)]\}}}$$

For $x_{margin} < x_g < x_{g23}$ compute

$$\bar{x} = (x_g/\xi)[1 + x_g(\xi x_{23} - x_{g23})/x_{g23}^2]$$

$$\bar{E} = \exp(-\bar{x})$$

$$\omega = 1 - \bar{E} - \Delta_n(\bar{E}^{-1} - \bar{E} - 2\bar{x})$$

$$x_0 = x_g + G_f^2/2 - G_f(x_g + G_f^2/4 - \omega)^{1/2}$$

$$\Delta_0 = \exp(x_0)$$

$$\Delta_1 = 1/\Delta_0$$

$$p = 2(x_g - x_0) + G_f^2[1 - \Delta_1 + \Delta_n(\Delta_0 + \Delta_1 - 2)]$$

$$q = (x_g - x_0)^2 - G_f^2[x_0 + \Delta_1 - 1 + \Delta_n(\Delta_0 - \Delta_1 - 2x_0)]$$

$$x = x_0 + \frac{2q}{p + \sqrt{p^2 - 2q\{2 - G_f^2[\Delta_1 + \Delta_n(\Delta_0 - \Delta_1)]\}}}$$

Finally, for $x_g > x_{g23}$ equations for Δ_0 and x directly above remain unchanged, but instead of above x_0 is computed as follows:

$$x_{sub} = x_g + G_f^2/2 - G_f(x_g + G_f^2/4 - 1)^{1/2}$$

$$\eta = MINA(x_{sub}, x_n + 0.5 + 2.5f_s, 5)$$

$$a = (x_g - \eta)^2 - G_f^2\eta + G_f^2$$

$$c = 2(x_g - \eta) + G_f^2$$

$$\tau = x_n - \eta + \ln(a/G^2)$$

$$x_0 = \eta + \sigma(a, c, \tau)$$

7.0 Evaluation of $\phi = \phi_{sd} - \phi_{ss}$ for $x_g < x_{g23}$

We use normalized variable $\varphi = \phi/V_t$ which satisfies equation

$$\varphi^2 - 2x_{gs}\varphi = G_f^2 J(\varphi)$$

where

$$J_\varphi = \varphi + E_s(e^{-\varphi} - 1) + \Delta_{ns}[E_s^{-1}(ke^\varphi - 1) - E_s(ke^{-\varphi} - 1) - 2x_s(k - 1) - 2k\varphi]$$

E_s is given by the equation for E_s in “Surface Potential ϕ_{ss} (at the Source End of the Channel) and Related Variables” on page 27-8 and

$$k = \exp(-V_{dse}/V_t)$$

Variables E_s , Δ_{ns} and D_s used below are defined in “Surface Potential ϕ_{ss} (at the Source End of the Channel) and Related Variables” on page 27-8.

The approximate solution of the equation for $\varphi^2 - 2x_{gs}\varphi$ which we use for $x_g < x_{g23}$ is given by

$$\varphi = 2q/(p + \sqrt{p^2 - 4\xi q})$$

where

$$q = G_f^2(1-k)D_s$$

$$p = 2x_{gs} + G_f^2\{1 - E_s + k[\Delta_s + \Delta_{ns}(E_s - 2)]\}$$

and

$$\xi = 1 - 0.5G_f^2[E_s + k\Delta_{ns}(E_s^{-1} - E_s)]$$

Equation for φ above is used for $x_g < x_{g23}$ but remains accurate well above x_{g23} . Hence the problem of matching with expression $\phi = \phi_{sd} - \phi_{ss}$ used for $x_g > x_{g23}$ does not arise.

8.0 Core Model Local Parameters

Effective channel dimensions: L, W

Oxide thickness: TOX

Channel doping: N_{sub}

Flat-band voltage: V_{fb}

Mobility model: MU0, μ_E , θ_{MU} , CS, X_{cor}

Saturation velocity model: u_{sat}, A_s, K_{sm}, STX

Lateral field gradient parameters: F_0 , A_f , B_f , C_f , DF, EF

Channel-length modulation: CLM3, L_{q2d}

Series resistance model: R_{t1} , R_g , RB

Triode-saturation transition parameter: a_X

Polysilicon gate doping: NP

Quantum correction magnitude: QMC

Subthreshold slope parameter: cT

9.0 Core Model Global Parameters

Parameters TOX, DF, EF, MU0, CS, CLM3, STX, NP, QMC and RB are both local and global. They are described in the section above.

Geometry (channel length): DL0, DLL, DLW

Geometry (channel width): DW0, DWL, DWW, DWP

Flat-band voltage: FB0, FB1, FB2

Reverse short-channel effect: FB3, FB4, FB5, FB6, FB7

Substrate doping: NSUB, LPKT, NPKT, YPKT, VNSUB, NSLP

Mobility: MU1, MU1W, MU2, MU3, NU0, NUL, NUW

Saturation velocity, including gate bias dependence: VSAT, ST0, ST1

Triode to saturation transition: AS0, ASL, S0

Velocity field relation: GH0, GH1, GH2, GH3, GH4

Lateral Gradient Factor: FL1, FL2, AF0, AFL, BFL, CF0, CFL, KL, KW

Channel-length modulation: CLM0, CLM1, CLM2, GDL

Series resistance: R0, R1, R2, R3, R4, R5, R6

subthreshold slope (scaling of interface state density): ITL

10.0 Scaling Equations

The drawn channel dimensions are denoted as L_{DR} , W_{DR} (in m) or as $L_{DR,\mu\text{m}}$, $W_{DR,\mu\text{m}}$ (in μm). The minimum device dimensions for a given technology are L_{REF} , W_{REF} (in m) or $L_{REF,\mu\text{m}}$, $W_{REF,\mu\text{m}}$ (in μm).

Effective channel length in μm

$$L_{\mu\text{m}} = L_{DR,\mu\text{m}} - DL0 - DLL \cdot A_L - DLW \cdot B_W$$

where

$$A_L = \frac{1}{L_{REF,\mu\text{m}}} - \frac{1}{L_{DR,\mu\text{m}}}$$

$$B_W = \frac{1}{W_{REF,\mu\text{m}}} - \frac{1}{W_{DR,\mu\text{m}}}$$

Effective channel length in m

$$L = 10^{-6} L_{\mu\text{m}}$$

Effective channel width in μm

$$W_{\mu\text{m}} = W_{DR,\mu\text{m}} - DW0 - DWL \cdot A_L - DWW \cdot B_W - DWP \cdot A_L \cdot B_W$$

Effective channel width in m

$$W = 10^{-6} W_{\mu\text{m}}$$

Flat-band voltage (which in SP includes reverse short-channel effect if any)

$$V_{fb} = FB0 + \frac{FB1}{W_{mu}} + \frac{FB2}{W_{mu}^2} + \Delta V_{RSE}$$

$$\Delta V_{RSE} = \left(1 + \frac{FB3}{W_{mu}} + \frac{FB4}{W_{mu}^2} \right) \cdot \left(\frac{FB5}{L_{DR, \mu m}} + \frac{FB6}{L_{DR, \mu m}^2} + \frac{FB7}{L_{DR, \mu m}^3} \right)$$

Drift velocity local parameters

$$K_{sm} = ST0 + ST1 \cdot B_W$$

$$A_s = \left(GH0 + \frac{GH1}{L_{mu}} + \frac{GH2}{L_{mu}^2} \right) \cdot \left(1 + \frac{GH3}{W_{mu}} \right) + \frac{GH4}{L_{mu}^2 W_{mu}^2}$$

Local parameters for the lateral field gradient

$$F_0 = 1 - \frac{FL1}{L_{mu}} - \frac{FL2}{L_{mu}^2}$$

$$A_f = \left(AF0 + \frac{AFL}{L_{mu}^2} \right) \cdot C_{LW}$$

$$B_f = \min \left\{ \frac{BFL}{L_{mu}^2}, \frac{1 - F_0}{F_0 + 0.01} \right\}$$

$$C_f = \left(CF0 + \frac{CFL}{L_{mu}^2} \right) \left(1 + KL \cdot \frac{A_L}{L_{mu}} \right) C_{LW}$$

and

$$C_{LW} = \frac{1}{1 + KW/W_{mu}}$$

Mobility model parameter

$$\mu_E = MU1 \left(1 + \frac{MU1 W}{W_{mu}} \right)$$

$$\theta_{MU} = MU2 \left(1 + \frac{MU3}{W_{mu}} \right)$$

Mobility model parameter (correction for "non-universality")

$$X_{cor} = NU0 + \frac{NUL}{L_{mu}} (1 + NUW \cdot W_{mu})$$

Bias-independent part of the series resistance

$$R_{t1} = R0 + R1 \cdot A_L + R2 \cdot B_W + R3 \cdot A_L \cdot B_W$$

Constant used to describe gate bias dependence of the series resistance

$$R_g = R4 + R5 \cdot A_L + R6 \cdot W_{\mu m}$$

Triode-saturation transition variable

$$a_x = \frac{AS0}{1 + ASL/L_{mu}}$$

Characteristic length of the quasi-2D theory

$$L_{q2d} = (1 + GDL \cdot L_{mu})(CLM0 + CLM1 \cdot A_L + CLM2 \cdot B_W) \sqrt{2 \cdot 10^{-7} \epsilon_{si} / C_{OX}}$$

Subthreshold slope parameter

$$cT = 1 + \frac{T_n}{TABS} \cdot \left(IT0 + \frac{ITL}{L_{mu}^2} \right)$$

11.0 Ranges of SP Parameters

In what follows $L_{MIN}(W_{MIN})$ is a minimum drawn channel length (width) for a particular parameter set. L_{MIN} and W_{MIN} are selected by users before extracting model parameters and can be set as minimum channel length for a modelled process or below that if extrapolation to smaller geometries is intended. Reducing L_{MIN} or W_{MIN} narrows down the allowed range of some parameters.

The following notations are used in the tables below.

$$A_{mr} = \frac{1}{L_{MIN,\mu m}} - \frac{1}{L_{REF,\mu m}} + 10^{-10}$$

$$B_{mr} = \frac{1}{W_{MIN,\mu m}} - \frac{1}{W_{REF,\mu m}} + 10^{-10}$$

Table 27-1. Process parameters group

Parameter	Unit	Description	Default	MIN	MAX
IT0	none	Interface states scaling factor	0	0	2
ITL	μm^2	Interface states scaling factor	0	a	
LPKT	μm	Pocket length	0	- 3/4 $P_L L_{MIN,\mu m}$	$9L_{MIN,\mu m}$
NP ^b	cm^{-3}	Polysilicon doping	10^{22}	$\max(3 \cdot 10^{19}, 80/TOX^2)$	none
NPKT	μm	Effective doping parameter	1.0	0	2
NSLP	1/V	Effective doping parameter	0	0	2
NSUB	cm^{-3}	Substrate doping	$5 \cdot 10^{17}$	10^{16}	$5 \cdot 10^{18}$
QMC	None	QM correction factor	0	0	$\min(0.6, 3 \cdot 10^{26} \cdot TOX/NSUB)$
TOX	m	Oxide thickness	$4 \cdot 10^{-9}$	10^{-9}	$2 \cdot 10^{-7}$
VNSUB	V	Effective doping parameter	0	none	
YPKT	μm	Effective doping parameter	0.001	0.001	none

a. Instead of clamping **ITL**, **SP** forces cT to be in [0, 2].

b. Setting **NP**=0 or **NP** > $10^{28} m^{-3}$ turns off polysilicon depletion effect.

At present, PL = 0.2.

Table 27-2. Effective geometry group

Parameter	Unit	Description	Default	MIN	MAX
DL0	μm	Channel length offset	0	a	
DLL	μm^2	Channel length adjustment (L)	0		
DLW	μm^2	Channel length adjustment (W)	0		
DW0	μm	Channel width offset	0	b	
DWL	μm^2	Channel width adjustment (L)	0		
DWW	μm^2	Channel width adjustment (W)	0		
DWP	μm^3	Channel width perimeter factor	0		

a. Instead of limiting the values of **DL0**, **DLL** and **DLW**, SP sets the channel length offset as:

$$DL_{\mu\text{m}} = DL0 + DLL \cdot A_L + DLW B_W$$

and the effective channel length (in μm) as: $L_{\mu\text{m}} = \max \{ L_{DR,\mu\text{m}} - DL_{\mu\text{m}}, P_L L_{MIN,\mu\text{m}} \}$

b. Instead of limiting parameter values of **DW0**, **DWL**, **DWW** and **DWP**, SP sets the channel width offset as: $DW_{\mu\text{m}} = DW0 + DWL \cdot A_L + DWW \cdot B_W + DWP \cdot A_L \cdot B_W$

and the effective channel length (in μm) as: $W_{\mu\text{m}} = \max \{ W_{DR,\mu\text{m}} - DW_{\mu\text{m}}, P_W W_{MIN,\mu\text{m}} \}$

At present, $P_W = 1/4$.

Table 27-3. Mobility group

Parameter	Unit	Description	Default	MIN	MAX
MU0	cm^2/Vs	Low-field mobility	500	0.01	105
NU0	V^{-1}	Non-universality factor	0	0	1
NUL	μm	Non-universality factor(L)	0	a	
NUW	μm^{-1}	Non-universality factor(W)	0		
MU1	m/V	Magnitude of the vertical field dependence	0.5	0	$5 \cdot 10^8 \text{TOX}$
MU1W	μm	Scaling parameter (W)	0	$-0.9 P_W W_{MIN,\mu\text{m}}$	$0.9 P_W W_{MIN,\mu\text{m}}$
MU2	None	Sharpness of the vertical field dependence	1.5	0	3
MU3	μm	Scaling parameter(W)	0	$-0.9 P_W W_{MIN,\mu\text{m}}$	$0.9 P_W W_{MIN,\mu\text{m}}$
CS	None	Coulomb scattering	0	0	10

a. Instead of limiting **NU0**, **NUL** and **NUW**, SP sets: $X_{cor} = \max \{ X_{cor}, 0 \}$

Table 27-4. Series resistance group

Parameter	Unit	Description	Default	MIN	MAX
R0	$\Omega \cdot m$	Fixed component of series resistance	$2 \cdot 10^{-3}$	a	
R1	$\Omega \cdot m \cdot \mu m$	Scaling factor(L)	0		
R2	$\Omega \cdot m \cdot \mu m$	Scaling factor(W)	0		
R3	$\Omega \cdot m \cdot \mu m^2$	Scaling factor(L,W)	0		
R4	V^{-1}	Gate bias dependence	0	0	None
R5	$\mu m/V$	Scaling factor(L) for gate bias dependence	0.02	$- PL / 2 R_4 L_{MIN,\mu m}$	$R_4 / 2 A_{mr}$
R6	$\mu m/V$	Scaling factor(W) for gate bias dependence	0	b	
RB	V^{-1}	Back bias factor	0	0	1.0

a. Instead of limiting the values of **R0**, **R1**, **R2** and **R3**, SP sets:

$$R_{tl} = \max\{R_0 + R_1 \cdot A_L + R_2 \cdot B_W + R_3 \cdot A_L \cdot B_W, 0\}$$

b. Instead of limiting the value of **R6**, SP sets: $R_g = \max\{R_4 + R_5 \cdot A_L + R_6 \cdot W_{\mu m}, 0\}$

Table 27-5. Velocity saturation group

Parameter	Unit	Description	Default	MIN	MAX
VSAT	m/s	Saturation velocity	80,000	50,000	150,000
ST0	V^{-1}	Gate bias dependence of saturation velocity	0	0	0.3
ST1	$\mu m/V$	Adjustment of saturation velocity (W)	0	$ST1_{min}$	$ST1_{max}$
				a	
STX	V^{-1}	Back bias dependence of saturation velocity	0	0	1
GH0	None	Grotjohn/Hoffinger (GH)factor	0.5	0.05	5
GH1	μm	GH Scaling parameter (L^{-1})	0	b	
GH2	μm^2	GH Scaling parameter (L^{-2})	0		
GH3	μm^3	GH Scaling parameter ($L^{-2}W^{-1}$)	0		
GH4	μm^4	GH Scaling parameter ($L^{-2}W^{-2}$)	0		
AS0	None	Transition from triode to saturation	12	6	100

Table 27-5. Velocity saturation group

ASL	None	Scaling factor(L) for triode-saturation transition	0.6	c	
S0	None	V _{dsat} adjustment	0.98	0.9	0.99

a. ST1_{min} = - min{((0.3 - ST0) / B_{mr}, ST0 · W_{MIN,μm}}; ST1_{max} = min{((0.3 - ST0)W_{MIN,μm}, ST0 / B_{mr}}

b. Instead of limiting the values of **GH1**, **GH2**, **GH3** and **GH4**, SP forces A_s to be in the range [0.05, 5]:

$$A_s = \min\left\{5, \max\left[0.05, \left(GH0 + \frac{GH1}{L_{\mu m}} + \frac{GH2}{L_{\mu m}^2}\right)\left(1 + \frac{GH3}{W_{\mu m}}\right) + \frac{GH4}{L_{\mu m}^2 W_{\mu m}^2}\right]\right\}$$

c. Instead of limiting the value of **ASL**, SP forces a_x to be in the range [2,20]: a_x = min{20, max{2, a_x}}

Table 27-6. Flat-band voltage group

Parameter	Unit	Description	Default
FB0	V	V _{fb} for long wide devices (L, W → ∞)	-1
FB1	V · μm	Scaling parameter (W ⁻¹)	0
FB2	V · μm ²	Scaling parameter (W ⁻²)	0
FB3	μm	RSE parameter (W ⁻¹)	0
FB4	μm ²	RSE parameter (W ⁻²)	0
FB5	V · μm	RSE parameter (L ⁻¹)	0
FB6	V · μm ²	RSE parameter (L ⁻²)	0
FB7	V · μm ³	RSE parameter (L ⁻³)	0

There are no limits on flat-band voltage parameters.

Table 27-7. Lateral gradient factor group

Parameter	Unit	Description	Default	MIN	MAX
FL1	μm	Scaling parameter for F ₀	0.1	a	
FL2	μm ²	Scaling parameter for F ₀	0.01		
AF0	V ⁻¹	Scaling parameter for A _f	0.004	0	10
AFL	μm ² /V	Scaling parameter for A _f	0	-AF0 · P _L ² L _{MIN,μm} ²	10
BFL	μm ² /V	Scaling parameter for B _f	0.015	0	10
CF0	V ⁻¹	Scaling parameter for C _f	0.0005	0	10

Table 27-7. Lateral gradient factor group

CFL	$\mu\text{m}^2/\text{V}$	Scaling parameter for C_f	0.01	$-\text{CF}_0 \cdot P_L^2 L_{\text{MIN},\mu\text{m}}^2$	10
GDS1	none	Vds dependence of Gds slope	0	b	0
GDS2	none	Vds dependence of Gds slope	0	0	none
KL	μm^2	Scaling parameter for C_{LW}	0	$-KLO^c$	KLO
KW	μm	Scaling parameter for C_{LW}	0	$-0.9P_W W_{\text{MIN},\mu\text{m}}$	10
DF	None	Sharpness of $f(V_{ds})$ dependence	0	0	3
EF	None	Sharpness of $f(V_{sb})$ dependence	0	0	3

a. Instead of limiting the values of **FL1** and **FL2**, SP forces F_0 to be in the range [0.001, 1]:

$$F_0 = \min\{1, \max\{0.001, F_0\}\}$$

b. Instead of limiting the values of **GDS1** and **GDS2**, SP forces $\frac{\partial}{\partial V_{dsx}} \left(\frac{F_0}{f_0} - 1 - B_f V_{sbx1} \right) > 0$

$$c. KLO = \min\{3.6L_{\text{MIN},\mu\text{m}}^2, 0.9L_{\text{MIN},\mu\text{m}}/A_{mr}\}$$

Table 27-8. Channel length modulation group

Parameter	Unit	Description	Default	MIN	MAX
CLM0	None	L_{q2d} parameter	0.1	0	10
CLM1	μm	L_{q2d} scaling parameter(L)	0	$-1/2 CLM0 \cdot L_{\text{MIN},\mu\text{m}}$	$\min\{10, CLM0/2A_{mr}\}$
CLM2	μm	L_{q2d} scaling parameter(W)	0	$-1/2 CLM0 \cdot W_{\text{MIN},\mu\text{m}}$	$\min\{10, CLM0/2B_{mr}\}$
CLM3	V^{-1}	Logarithm dependence factor	10	0	1000
GDL	μm^{-1}	Scaling parameter(L)	0	0	0.9

12.0 Temperature dependence (-55 to 150)

SP uses up to 13 temperature coefficients

Flat-band voltage: TK VFB0, TK VFBL, TK VFBW, TK VFBP.

Mobility: TK MU0, TK MUW, TK MUL, TK MUP, TK MU1, TK THM, TK CS.

Saturation velocity: TK VS, TK AS.

Coefficients TK VFBL, TK VFBW, TK VFBP, TK MUL, TK MUP and TK AS are expected to be zero for mature processes.

The default values and ranges for temperature coefficients are given in the table below.

Table 27-9. Temperature coefficients

Parameter	Unit	Description	Default	MIN	MAX
TK VFB0	None	$V_{fb}(T)$ parameter	0	None	None
TK VFBL	μm	$V_{fb}(T)$ scaling parameter(L)	0	None	None
TK VFBW	μm	$V_{fb}(T)$ scaling parameter(W)	0	None	None
TK VFBP	μm^2	$V_{fb}(T)$ scaling parameter(LW)	0	None	None
TK MU0	None	MU0(T) parameter	1.5	a	
TK MUL	μm	MU0(T) scaling parameter(L)	0		
TK MUW	μm	MU0(T) scaling parameter(W)	0		
TK MUP	μm^2	MU0(T) scaling parameter(LW)	0		
TK MU1	None	$\mu_E(T)$ parameter	0		
TK THM	None	$\theta_{mu}(T)$ parameter	0	-5	5
TK CS	None	CS(T) parameter	0	-5	5
TK VS	K^{-1}	VSAT(T) parameter	0	-0.005	0.005
TK AS	μm	$A_s(T)$ parameter	0	0	0.1

a. Instead of limiting **TK_MU0**, **TK_MUL**, **TK_MUW** and **TK_MUP**, SP sets:

$$n_{\mu 0} = \min \left\{ 5, \max \left[-5, \frac{\Delta T}{T_n} \left(\frac{TKMUL}{L_{mu}} + \frac{TKMUW}{W_{mu}} + \frac{TKMUP}{L_{mu}M_{mu}} \right) \right] \right\}$$

13.0 Extrinsic Model Parameters

Table 27-10. Overlap Charge Parameters

Parameter	Unit	Description	Default	MIN	MAX
TOXOV	m	Overlap oxide thickness	TOX	10^{-9}	2×10^{-7}
NOV	cm ⁻³	Overlap doping	$5 \cdot 10^{19}$	10^{18}	$5 \cdot 10^{20}$
LOV	m	Overlap length	0	0	LMIN
IFKJ	C/V ^{1/2}	Fringe capacitance parameter	0	0	None
IFCJ	1/V	Fringe capacitance parameter	0	0	None
IFVBI	V	Built in potential	1.2	a	None
CF	F/m	Out fringe capacitance per unit width	0	none	
CGBO	F/m	Bulk overlap capacitance per unit length	0	none	

a. Instead of limiting the minimum value of **IFVBI**, SP forces: **IFVBI** + $V_{sb} - f_{ss} > 0$

Table 27-11. Gate Current Parameters

Parameter	Unit	Description	Default	MIN	MAX
GC0	none	Tunnelling energy adjustment	0	-10	10
GC1	none	Gate current overall level	1	0	10
GC2 ^a	none	$\log I_{gate} - V_g$ slope	1	0	10
GC3	none	$\log I_{gate} - V_g$ curvature	0	-2	2

a. In SP code if **GC3** < 0, then is modified as follows: $u_0 = X_B / (\text{GC2} + 2\text{GC3} \cdot z_g)$
 $z_g = \text{MINA}(U_{oxm} / X_B, -\text{GC2} / 2\text{GC3}, 1e - 6)$; where

$$\text{MINA}(a, b, c) = \frac{1}{2}[a + b - \sqrt{(a - b)^2 + c}]$$

Table 27-12. GIDL parameters

Parameter	Unit	Description	Default	MIN	MAX
AGIDL	none	GIDL coefficient	0.7	0.0	-

Table 27-12. GIDL parameters

BGIDL	V	Tunnelling barrier adjustment	28	1	100
CGIDL	V^{-1}	Lateral field dependence	0.007	0	1
BK GIDL	K^{-1}	Temperature dependence	0	0	1

Table 27-13. Impact Ionization Substrate Current Parameters

Parameter	Unit	Description	Default	MIN	MAX
IIA1	none	Substrate current parameter	1	0	20
IIA2	V	Substrate current parameter	10	1	20
IIA3	none	Substrate current parameter	0.5	0.1	1.0
IIA4	$V^{-1/2}$	Substrate current parameter	0	0	1
IIA1L	m	Substrate current scaling parameter	0	-1	1
IIA3L	m	Substrate current scaling parameter	0	-1	1
IIA4L	$mV^{1/2}$	Substrate current scaling parameter	0	-1	1
IIPARTITION	none	Partition parameter	0	0	1

Table 27-14. Noise Parameters

Parameter	Unit	Description	Default	MIN	MAX
NDELTA	none	Thermal noise parameter	0	0	10
NOIA	$m^{-3}V^{-1}C^{-1}$	Flicker noise parameter	3×10^{22}	0	none
NOIB	$m^{-1}V^{-1}C^{-1}$	Flicker noise parameter	4×10^7	0	
NOIC	$mV^{-1}C^{-1}$	Flicker noise parameter	0	0	
NEF	none	Flicker noise parameter	1	0	2
DVDZ	none	Channel-induced gate noise parameter	1	0	10

Table 27-15. Series Resistances Parameters

Parameter	Unit	Description	Default	MIN	MAX
RSH	Ω/square	Source-drain sheet resistance	0	0	none
RGSH	Ω/square	Gate sheet resistance	0	0	
NRS	none	Number of squares in source	1	0	
NRD	none	Number of squares in drain	1	0	
NF	none	Number of fingers	1	1	

Table 27-16. Extrinsic Model Switches

Switch	Description	Default
SW_IGATE	=1 turn on gate current computation; ≠1 turn off gate current computation	0
SW_IMPACT	=1 turn on impact ionization current computation; ≠1 turn off impact ionization current computation	0

14.0 Printing/Plotting SP States

States are printed/plotted using the syntax:

```
.print S (Mx->STATE)
```

Quantity	Description
IDS	Channel Current
GM	
GDS	
GBS	
II	Impact Ionization full current
IBD_II	II bulk-drain component
DIBD_II_VGS	

DIBD_II_VDS	
DIBD_II_VBS	
ISD_II	II source-drain component
DISD_II_VGS	
DISD_II_VDS	
DISD_II_VBS	
IBDJ	Parasitic bulk-drain junction diode current
DIBDJ_VBD	
IBSJ	Parasitic bulk-source junction diode current
DIBSJ_VBS	
IGCS	Gate current source component
DIGCS_VGS	
DIGCS_VDS	
DIGCS_VBS	
IGCD	Gate current drain component
DIGCD_VGS	
DIGCD_VDS	
DIGCD_VBS	
IGCB	Gate current bulk component
DIGB_VGS	
DIGB_VDS	
DIGB_VBS	
IGSOV	Gate current source overlap component
DIGSOV_VGS	
DIGSOV_VDS	

DIGSOV_VBS	
IGDOV	Gate current drain overlap component
DIGDOV_VGS	
DIGDOV_VDS	
DIGDOV_VBS	

The following 6 states will always give zero output unless the access resistors have a value.

Quantity	Description
IDINT_D	Drain access resistor current
GDACC	1/ Drain access resistor
ISINT_S	Source access resistor current
GSACC	1/ Source access resistor
IGINT_G	Gate access resistor current
GGACC	1/ Gate access resistor

Charges and capacitances:

Quantity	Description
QG	Gate charge
CGG	
CGD	
CGS	
QD	drain charge
CDG	
CDD	
CDS	

QS	source charge
CSG	
CSD	
CSS	
QDGFI	Drain-Gate internal fringing charge
CDGFRI	
QSGFRI	Source-Gate internal fringing charge
CSGFRI	
QDJ	drain-bulk parasitic diode charge
CDGJ	
CDDJ	
CDSJ	
QSJ	source-bulk parasitic diode charge
CSGJ	
CSDJ	
CSSJ	
QSGOV	Source-gate overlap charge
CSGOV	
CSDOV	
CSSOV	
QDGOV	Drain-gate overlap charge
CDGOV	
CDDOV	
CDSOV	
QSGFRO	Source-Gate external fringing charge

CSGFRO	
CSDFRO	
CSSFRO	
QDGFRO	Drain-Gate external fringing charge
CDGFRO	
CDDFRO	
CDSFRO	

Noise states:

Quantity	Description
THNOI	Channel Thermal noise
FLNOI	Channel flicker noise
GTHNOI	Induced gate-channel noise
COR_IGID	Correlated gate-drain noise
TOT_THERM	Total thermal noise (Channel + induced gate + correlation term)

The following 3 states will always give zero output unless the access resistors have a value.

Quantity	Description
RDNOI	Drain access resistor noise
RGNOI	Gate access resistor noise
RSNOI	Source access resistor noise

OP Printed Values

Drain-Source current and derivatives.

Ids	Gm	Gds	Gbs
-----	----	-----	-----

Impact ionization current and derivatives (only enabled in case SW_IMPACT parameter is > 1).

II	ibd_ii	dibd_ii_vgs	dibd_ii_vds	dibd_ii_vbs
isd_ii	disd_ii_vgs	disd_ii_vds	disd_ii_vbs	Ibdj
dibdj_vbd	Ibsj	dibsj_vbsv		

Gate current and derivatives (only enabled in case SW_IGATE parameter is > 1).

Igcs	digcs_vgs	digcs_vds	digcs_vbs	Igcd
digcd_vgs	digcd_vds	digcd_vbs	Igcb	digb_vgs
digb_vds	digb_vbs	Igsov	digsov_vgs	digsov_vds
digsov_vbs	Igdov	digdov_vgs	digdov_vds	digdov_vbs

Access resistors.

Idint_d	Gdacc	Isint_s	Gsacc	Igint_g
Ggacc				

Charges and capacitances.

Qg	Cgg	Cgd	Cgs	Qd
Cdg	Cdd	Cds	Qs	Csg
Csd	Css	Qdgfri	Cdgfri	Qsgfri
Csgfri	Qdj	Cdgj	Cddj	Cdsj
Qsj	Csgj	Csdj	Cssj	Qsgov

Csgov	Csdov	Cssov	Qdgov	Cdgov
Cddov	Cdsov	Qsgfro	Csgfro	Csdfro
Cssfro	Qdgfro	Cdgfro	Cddfro	Cdsfro

Noise components (only enabled when Noise analysis is specified).

Flicker Noise	Thermal Noise	Gate induced Noise	Correlated Gate-Channel Thermal Noise
RD Noise	RS Noise	RG Noise	

Chapter 28

BTA HVMOS Model

1.0 Introduction

HV (High-Voltage) MOS transistor model is based on the BSIM3v3 model. Major enhancements include current-crowding effect at high gate bias, asymmetric source-drain structure, self-heating, and more flexible gate-dependent output characteristics. Like BSIM3v3, the HVMOS transistor model also allows the binning option to achieve even higher accuracy. The binning equation is given by:

$$P = P_0 + \frac{P_l}{L_{eff}} + \frac{P_w}{W_{eff}} + \frac{P_p}{L_{eff} \cdot W_{eff}}$$



Note

Eldo defaults **LMIN** and **WMIN** to 1×10^{-6} m if the user did not specify these parameters. To avoid mistakes in finding the correct models, please set the **LMIN** and **WMIN** values in your model cards.

1.1 HVMOS License

The HVMOS model is a proprietary model of BTA Technology. To use the BTA HVMOS model, a license for Eldo from Mentor Graphics is required, *as well as* a license for the HVMOS model from BTA.

To setup the BTA license daemon for the HVMOS library, please refer to BTA's "License Installation and Management User Guide."

1.2 BTA HVMOS v2.0

The list below describes the improvements made in BTA HVMOS v2.0 over previous versions:

1. BTA HVMOS v2.0 supports the temperature dependence of the diode junction capacitance model. Both the unit area junction capacitance and built-in potential are now temperature dependent.

$$\delta T = T - T_{nom}$$

$$Cj(T) = Cj(T_{nom}) \times (1 + Tcj \times \delta T)$$

$$Pb(T) = Pb(T_{nom}) - Tpb \times \delta T$$

$$Cjsw(T) = Cjsw(T_{nom}) \times (1 + Tcjsw \times \delta T)$$

$$Pbsw(T) = Pbsw(T_{nom}) - Tpbsw \times \delta T$$

$$Cjswg(T) = Cjswg(T_{nom}) \times (1 + Tcjswg \times \delta T)$$

$$Pbswg(T) = Pbswg(T_{nom}) - Tpbswg \times \delta T$$

where T is the circuit temperature, T_{nom} is the nominal model temperature. The alias names for Tcj , Tpb , $Tcjsw$ and $Tpbsw$ are CTA , PTA , CTP and PTP , respectively. If $Tcjswg$ is not given, its default value is $Tcjsw$. If $Tpbswg$ is not given, its default value is $Tpbsw$.

2. BTA HVMOS v2.0 supports XL and XW for $Leff$, $Weff$, $Leffcv$ and $Weffcv$ calculations.

$$Leff = Ldrawn - 2 \times \delta L + XL$$

$$Weff = Wdrawn - 2 \times \delta W + XW$$

$$Leffcv = Ldrawn - 2 \times \delta Lcv + XL$$

$$Weffcv = Wdrawn - 2 \times \delta Wcv + XW$$

The units of XL and XW are meters.

3. BTA HVMOS v2.0 improves the self-heating effect.
4. The parameter, **HVMOSVER**, is available to maintain backward compatibility. For example,

HVMOSVER=2.0 for this version of HVMOS, this model will have the enhanced self-heating effect as listed above. For the previous version, **HVMOSVER=1.0**.

5. Problem fix on the implementation of P_{Rt} , the temperature coefficient of R_{dsW} .

2.0 Model Parameters

Nr.	Name	Description	Default	Units	Binned
1	TNOM	Temperature at which parameters were extracted	27.0	°C	No
2	TOX	Gate oxide thickness		m	No
3	WINT	Width offset fitting parameter from I-V without bias	2.7×10^{-7}	m	No
4	LINT	Length offset fitting parameter from I-V without bias	0.0	m	No
5	LL	Coefficient of length dependence for length offset	0.0	m^{Lln}	No
6	LLN	Power of length dependence for length offset	1.0		No
7	LW	Coefficient of width dependence for length offset	0.0	m^{Lwn}	No
8	LWN	Power of width dependence for length offset	1.0		No
9	LWL	Coefficient of length and width cross term for length offset	0.0	$m^{Lwn+Lln}$	No
10	WL	Coefficient of length dependence for width offset	0.0	m^{Wln}	No
11	WLN	Power of length dependence for width offset	1.0		No
12	WW	Coefficient of width dependence for width offset	0.0	m^{Wwn}	No
13	WWN	Power of Width dependence for width offset	1.0		No
14	WWL	Coefficient of length and width cross term for width offset	0.0	$m^{Wwn+Wln}$	No
15	MOBMOD	Mobility model selector	2		No
16	CAPMOD	Capacitance model selector	2		No

Nr.	Name	Description	Default	Units	Binned
17	CGBO	Gate bulk overlap capacitance per unit channel length	1×10^{-10}	Fm ⁻¹	No
18	CGDO	Non-LDD region drain-gate overlap capacitance per unit channel width	1×10^{-10}	Fm ⁻¹	No
19	CGSO	Non-LDD region source-gate overlap capacitance per unit channel width	1×10^{-10}	Fm ⁻¹	No
20	DLC	Channel length reduction on one side, used in CV model	1×10^{-7}	m	No
21	DWC	Channel width reduction on one side, used in CV model	1×10^{-7}	m	No
22	DELTACC	Parameter in Vfb smooth function used in CV model	0.1		No
23	CJ	Bottom junction capacitance per unit area	5×10^{-4}	Fm ⁻²	No
24	PB	Bottom built-in potential	1.0	V	No
25	MJ	Bottom junction capacitance grading coefficient	0.5		No
26	CJSW	Source/Drain side junction capacitance per unit length along the field oxide side	5×10^{-10}	Fm ⁻¹	No
27	PBSW	Source/Drain side junction built-in potential along the field oxide side	1.0	V	No
28	MJSW	Source/Drain side junction capacitance grading coefficient along the field oxide side	0.33		No
29	CJSWG	Source/Drain side junction capacitance per unit length along the gate oxide side	CJSW	Fm ⁻¹	No
30	PBSWG	Source/Drain side junction built-in potential along the gate oxide side	PBSW	V	No
31	MJSWG	Source/Drain side junction capacitance grading coefficient along the gate oxide side	MJSW		No
32	XPART	Charge partition selector	0.0		No
33	PLRTY	Device operation model selector: 1= forward mode 2= reverse mode			No
34	VTH0	Threshold voltage of large device @Vbs=0	0.548	V	Yes
35	K1	First order body effect coefficient	0.631	V ^{0.5}	Yes
36	K2	Second order body effect coefficient	-0.018		Yes
37	K3	Narrow width coefficient	0.0		Yes
38	K3B	Body effect coefficient of K3	0.0	V ⁻¹	Yes

Nr.	Name	Description	Default	Units	Binned
39	NLX	Lateral non-uniform doping parameter	0.0	m	Yes
40	DVT0	First coefficient of short channel effect on Vth	0.2648		Yes
41	DVT1	Second coefficient of short channel effect on Vth	0.2212		Yes
42	DVT2	Body-bias coefficient of short channel effect on Vth	-0.402	V ⁻¹	Yes
43	NCH	Channel doping concentration	1.6×10 ¹⁶	cm ⁻³	Yes
44	U0{F,R}	Mobility at temperature=TNOM	647.9(N) 250.0(P)	cm ² (Vs) ⁻¹	Yes
45	UA{F,R}	First-order mobility degradation coefficient	2.18×10 ⁻⁹	mV ⁻¹	Yes
46	UB{F,R}	Second order mobility degradation coefficient	1×10 ⁻²¹	(mV ⁻¹) ²	Yes
47	UC{F,R}	Body-effect of mobility degradation coefficient mobmod=1 mobmod=2 mobmod=3	-3.35×10 ⁻¹⁰ (mobmod=2)	mV ⁻² V ⁻¹ V ⁻¹	Yes
48	XJ	Junction depth	1×10 ⁻⁷	m	Yes
49	W0	Narrow width parameter	0.0	m	Yes
50	AGS	Gate bias coefficient of Abulk	1×10 ⁻⁹	V ⁻¹	Yes
51	A1	First non-saturation effect parameter	0.0	V ⁻¹	Yes
52	A2	Second non-saturation effect parameter	1.0		Yes
53	B0	Bulk charge effect coefficient for channel width	1×10 ⁻⁸	m	Yes
54	B1	Bulk charge effect width offset	0.0	m	Yes
55	RDW	Parasitic resistance per unit width on the drain side	100.0	Ω-mmWr	Yes
56	RSW	Parasitic resistance per unit width on the source side	0.0	Ω-mmWr	Yes
57	PRWG	Gate bias effect coefficient of RDW and RSW	0.0	V ⁻¹	Yes
58	PRWB	Body bias effect coefficient of RDW and RSW	0.0	V ^{1/2}	Yes
59	WR	Width offset from Weff for RD and RS calculation	1.0		Yes
60	A0{F,R}	Bulk charge effect coefficient	0.1		Yes
61	KETA{F,R}	Body-bias coefficient of bulk charge effect	-0.047	V ⁻¹	Yes
62	VSAT{F,R}	Saturation velocity	1×10 ⁵	ms ⁻¹	Yes

Nr.	Name	Description	Default	Units	Binned
63	DVSAT{F,R}	Velocity degradation coefficient	0.015	V ⁻²	Yes
64	DVSATB{F,R}	Body effect coefficient of DVSAT	0.0	V ⁻³	Yes
65	DWG	Coefficient of gate bias dependence of Weff	0.0	mV ⁻¹	Yes
66	DWB	Coefficient of body bias dependence of Weff	0.0	mv ^{-1/2}	Yes
67	ALPHA0	The first parameter of impact ionization current	0.0	mV ⁻¹	Yes
68	BETA0	The second parameter of impact ionization current	30.0	V	Yes
69	RTH	Self-heating effect coefficient	0.0	(AV) ⁻¹	Yes
70	RTHB	Coefficient of body bias dependence of RTH	0.0	V ^{-1/2}	Yes
71	RTHG	Coefficient of gate bias dependence of RTH	0.0	V ⁻¹	Yes
72	PCLM{F,R}	Channel length modulation parameter of Rout	1.0		Yes
73	PCLMG{F,R}	Gate bias coefficient of PCLM	5.0	V ^{-1.5}	Yes
74	PCLMB{F,R}	Body bias coefficient of PCLM	0.0	V ⁻¹	Yes
75	PDIBLC1{F,R}	First DIBL effect parameter of Rout	0.001		Yes
76	PDIBLC2{F,R}	Second DIBL effect parameter of Rout	0.001		Yes
77	PDIBLG{F,R}	Gate bias dependence coefficient of DIBL parameter	5.0		Yes
78	PDIBLCB{F,R}	Body bias dependence coefficient of DIBL parameter	0.0	V ⁻¹	Yes
79	DROUT	Channel length dependence coefficient of DIBL parameter of Rout	1.2		Yes
80	PSCBE1{F,R}	First parameter of substrate current body effect on Rout	3.1×10 ⁹	Vm ⁻¹	Yes
81	PSCBE2{F,R}	Second parameter of substrate current body effect on Rout	1.2×10 ⁻⁵	Vm ⁻¹	Yes
82	PSCBEG	Gate bias coefficient of PSCBE1	0.0		Yes
83	ELM	Elmore constant of the channel	4.1×10 ⁷		Yes
84	DELTA	Effective Vds parameter	0.01		Yes
85	ETA0{F,R}	DIBL coefficient in the subthreshold region	0.01		Yes
86	ETAB{F,R}	Body bias coefficient for the subthreshold DIBL effect	0.0	V ⁻¹	Yes
87	VOFF	Offset voltage in the subthreshold region of a large size device	-0.086	V	Yes
88	NFACTOR	Subthreshold swing factor	1.831		Yes

Nr.	Name	Description	Default	Units	Binned
89	CDSC	Drain/Source to channel coupling capacitance	0.0	Fm ⁻²	Yes
90	CDSCB	Body bias sensitivity of CDSC	0.0	F(Vm ²) ⁻¹	Yes
91	CDSCD	Drain bias sensitivity of CDSC	0.0	F(Vm ²) ⁻¹	Yes
92	CIT	Interface trap capacitance	0.0	Fm ⁻²	Yes
93	DUB	DIBL coefficient exponent in subthreshold region	0.05		Yes
94	A0CV{F,R}	Bulk charge effect coefficient in CV model	0.1		Yes
95	QGVD0{F,R}	Bulk charge	1.0		Yes
96	CLC	Constant term for the short channel VC model	1×10 ⁻⁷	m	Yes
97	CLE	Exponential term for the short channel CV model	0.6		Yes
98	CF	Fringing field capacitance	0.0	Fm ⁻¹	Yes
99	CKAPPA	Coefficient for lightly doped region overlap capacitance fringing field capacitance	0.6	Fm ⁻¹	Yes
100	CGD1	Lightly doped drain-gate region overlap capacitance	1×10 ⁻²⁰	Fm ⁻¹	Yes
101	CGS1	Lightly doped source-gate region overlap capacitance	1×10 ⁻²⁰	Fm ⁻¹	Yes
102	KT1	Temperature coefficient for threshold voltage	-0.11	V	Yes
103	KT1L	Channel length dependence of the temperature coefficient for threshold voltage	0.0	Vm	Yes
104	KT2	Body-bias coefficient of Vth temperature effect	0.022		Yes
105	UTE	Mobility temperature exponent	-1.5		Yes
106	UA1{F,R}	Temperature coefficient of UA	4.31×10 ⁻⁹	mV ⁻¹	Yes
107	UB1{F,R}	Temperature coefficient of UB	-7.61×10 ⁻¹⁸	(mV ⁻¹) ²	Yes
108	UC1{F,R}	Temperature coefficient of UC : mobmod=1 mobmod=2 mobmod=3	-0.056×10 ⁻¹¹ (mobmod=2)	mV ⁻² V ⁻¹ V ⁻¹	Yes
109	PRT	Temperature coefficient of RDSW	0.0	Ωmm	Yes
110	AT{F,R}	Temperature coefficient for saturation velocity	3.3×10 ⁴	ms ⁻¹	Yes
111	AT1{F,R}	Temperature coefficient for DVSAT	0.0	V ⁻²	Yes
112	TCJ (CTA)	Temperature coefficient for CJ	0.0	°K ⁻¹	No

Nr.	Name	Description	Default	Units	Binned
113	TPB (PTA)	Temperature coefficient for PB	0.0	V°K ⁻¹	No
114	TCJSW (CTP)	Temperature coefficient for CJSW	0.0	°K ⁻¹	No
115	TPBSW (PTP)	Temperature coefficient for PBSW	0.0	V°K ⁻¹	No
116	TCJSWG	Temperature coefficient for CJSWG	TCJSW	°K ⁻¹	No
117	TPBSWG	Temperature coefficient for PBSWG	TPBSW	V°K ⁻¹	No
118	XL	Channel length offset	0.0	m	No
119	XW	Channel width offset	0.0	m	No
120	HVMOSVER	HVMOS version selection for backward compatibility	2.0		No

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