austriamicrosystems

0.35µm CMOS C35 Matching Parameters

Document Number: ENG - 228

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1. Introduction

1.1. Revision

Change Status of Pages (including short description of change)

Rev. 1.0	Affected pages:	1 to 12	(February 2003)
Subject of change: first version of mismatch parameter specification			

1.2. Process Family

This document is valid for the following 0.35µm CMOS processes:

Process name	No. of masks	CMOS core module *	POLY1-POLY2 capacitor module **	5 Volt module	High resistive poly module	Metal 4 module	Thick Metal module	MET2-METC capacitor module
C35B3C0	14	x	x					
C35B3C1	17	x	x	x				
C35B4C3	20	x	x	x	x	x		
C35B4M3	21	x	x	x	x		x	x

*) **CMOS core module**
consists of p-substrate, single poly, triple metal and 3.3 Volt process.
) **POLY1-POLY2 capacitor module
consists of p-substrate, double poly (RPOLY2 resistor), triple metal and 3.3 Volt process.

1.3. Related Documents

Description	Document Number
0.35µm CMOS C35 Process Parameters	Eng - 182
0.35µm CMOS C35 Design Rules	Eng - 183
0.35µm CMOS C35 Noise Parameters	Eng - 189
0.35µm CMOS C35 RF SPICE Models	Eng – 188

1.4. Process parameter description

CHARACTERISATION PARAMETERS are provided to increase the knowledge about the process behaviour. They are not under 100% statistical control because they require extra large test structures (e.g. parasitic capacitors) or time consuming measurement procedures (e.g. temperature coefficients). These data are extracted from special process control monitor (PCM) test structures and do not lead to wafer reject in case of failure.

Note: Characterisation parameters are extracted from typical wafers only, therefore no corner models are available. It is strongly recommended that a design shall rely only on pass/fail parameters.

2. Matching Parameters

2.1. Introduction

This document presents fundamental parameters describing the matching behaviour of MOS transistors, resistors and capacitors. All matching parameters are characterisation parameters and represent typical values only.

The matching parameters describe the short distance matching - the matching of two identically designed elements located close to each other.
The stochastic mismatch between two parameters P1 and P2 measured at two identically designed elements is defined as the standard deviation of the normal distribution for

1. absolute differences $\Delta P = (P1 - P2)$ [mV]
(for threshold voltages)

or

2. relative differences $\frac{\Delta P}{P} = \frac{200 \cdot (P1 - P2)}{(P1 + P2)}$ [%]
(for transistor currents, resistors, capacities).

We assume that all ΔPi values are normally distributed with a variance σ^2 (squared standard deviation). The estimator μ of the distribution mean is close to zero – indicating a low fraction of systematic mismatch - except in the case of strong process parameter gradients or layout related asymmetries.

2.1.1. Model used for evaluation of measured data

Matching measurements are performed for MOS transistors, resistors and capacitors. The following Pelgrom model describes the dependency of parameter matching on two identically designed devices on their area (W·L):

$$\sigma(P1 - P2) = \frac{A\_P}{\sqrt{W \cdot L}}$$

where A_P is the process-dependent matching parameter describing the area dependence.

2.1.2. Model used for matching simulation

Additionally, final matching parameters are extracted for MOS transistors. These parameters are used for simulator model implementation and Monte Carlo simulation.

2.2. MOS Transistor Matching Parameters

2.2.1. Matching Parameter Extraction / Simulator Implementation

Matching parameters are determined by fitting a suitable mismatch model to the measured data $\sigma(\Delta ID/ID)$ of each device size. The variances of the relative matching deviations are fitted by a non-linear optimisation procedure. The resulting parameters give an optimal fitting result for the whole measured biasing region (see section Characteristic Curves).
A linear regression is applied to the fitting parameters to calculate the area dependence A_P of the matching parameters.

$$\sigma(\Delta P) = \frac{A\_P}{\sqrt{W \cdot L}}$$

The simulator model implementation for the Monte Carlo simulation includes the parameter A_P_{sim}. The implementation is done by using extended sub-circuit device models. Since the simulation model describes the variation of a single device parameter, the value $A\_P_{sim} = A\_P/\sqrt{2}$ is used assuming statistically independent parameters.

Final matching parameters are extracted for

VT	threshold voltage
K	current gain factor

CHARACTERISATION PARAMETERS		
Parameter	**A_VT**	**A_K**
Unit	mV µm	% µm
NMOS	8.2	0.2
PMOS	14.9	0.4
NMOSM	13.2	0.2
PMOSM	22.7	0.6
Note	1	1

2.3. Resistor Matching Parameters

The resistor matching is described by

$$\sigma\left(\frac{\Delta R}{R}\right) = \frac{A\_R}{\sqrt{W \cdot L}}$$

CHARACTERISATION PARAMETERS	
Parameter	**A_R**
Unit	% µm
RPOLY2	12
RPOLYH	7
Note	2

2.4. Capacitor Matching Parameters

The capacitor matching is described by

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{A\_C}{\sqrt{W \cdot L}}$$

CHARACTERISATION PARAMETERS	
Parameter	**A_C**
Unit	% µm
CPOLY	1.2
Note	3

3. Notes / Measurement Conditions

Note 1 **Drain-current matching**

The measurements of ID are performed at
VDS=3V and VGS=0.5 - 3.5V for N/PMOS
VDS=5V and VGS=0.5 - 5.5V for N/PMOSM

Note 2 **Resistor matching**

The resistance measurements are performed at constant power (1mW) for different resistor dimensions (W, L).

Note 3 **Capacitor matching**

Due to the very low capacitances a direct measurement and calculation of mismatch parameters are not possible. Therefore a floating gate measurement technique with a source follower on the (floating) middle node of a capacitive voltage divider is used. By applying different input voltages (0.5V to 4.5V) and measuring the corresponding output voltages at the source of the p-channel transistor a slope S_1 is determined. After exchanging the nodes of the voltage divider a second slope S_2 is measured. The resulting capacitor mismatch is defined by

$$\frac{\Delta C}{C} = 2 \cdot \frac{S1 - S2}{S1 + S2} = 2 \cdot \frac{C1 - C2}{C1 + C2}$$

4. Characteristic Curves

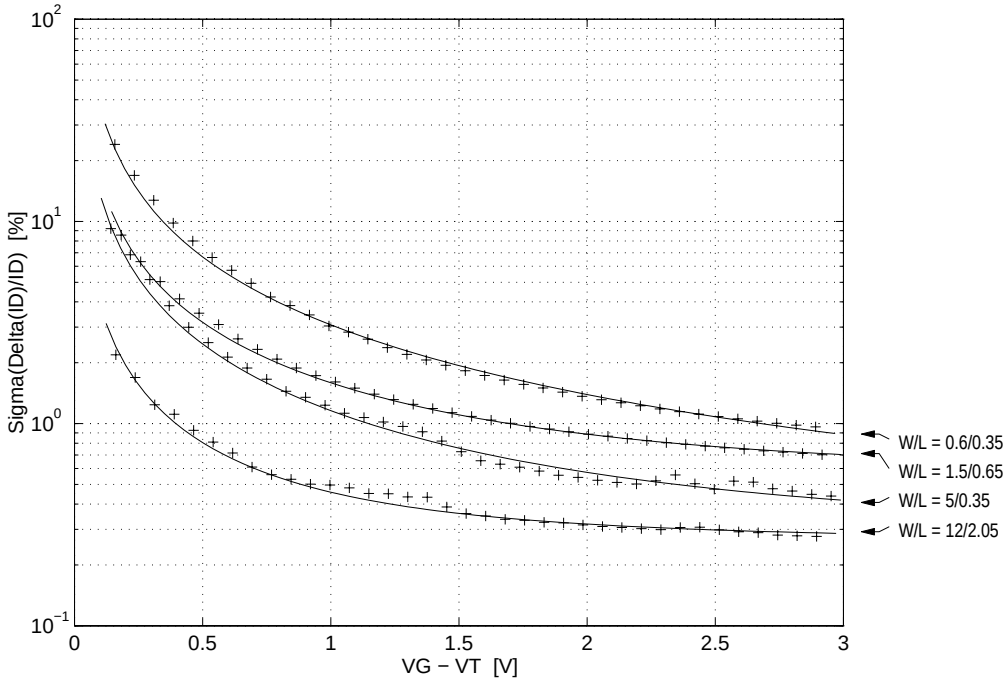

Fig. 4.1 NMOS relative drain current mismatch vs. VG-VT, +...measurement, —...mismatch model

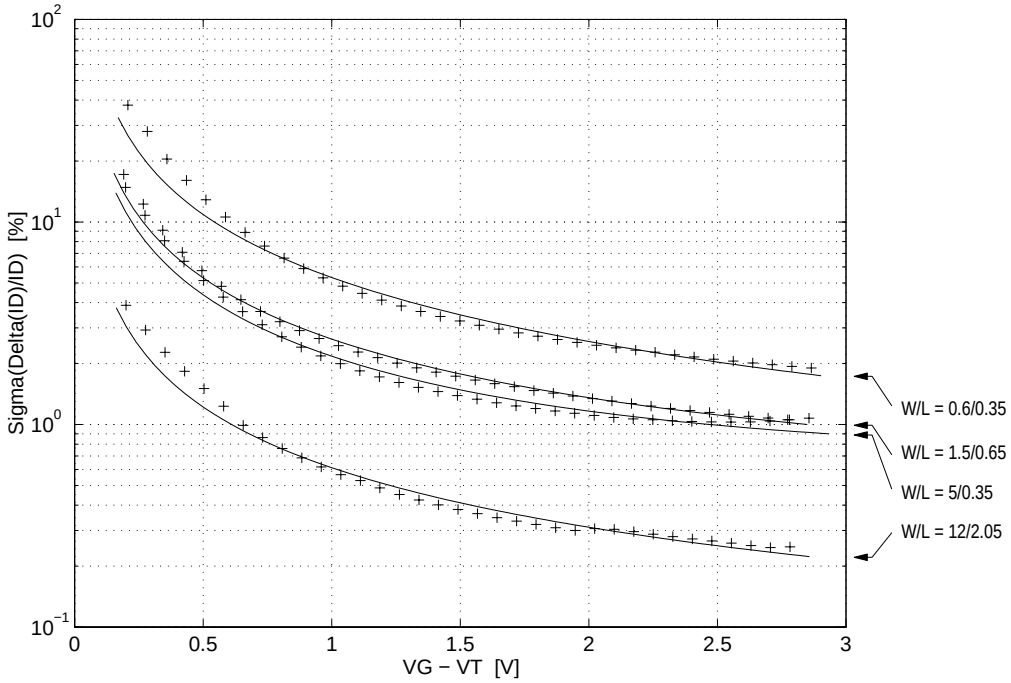

Fig. 4.2 PMOS relative drain current mismatch vs. VG-VT, +...measurement, —...mismatch model

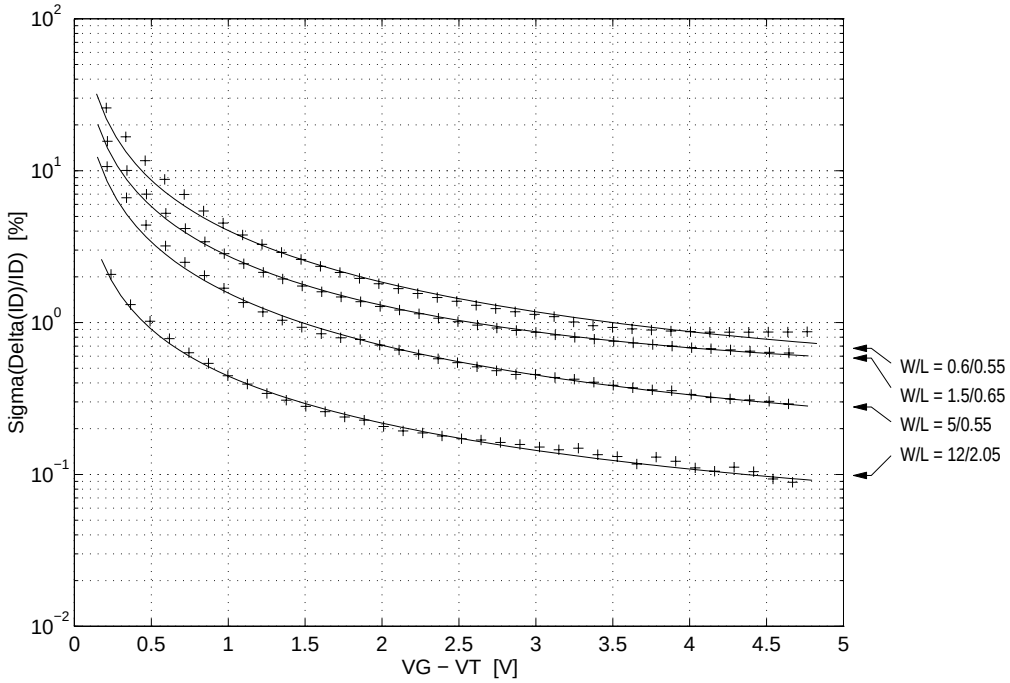

Fig. 4.3 NMOSM relative drain current mismatch vs. VG-VT, +...measurement, —...mismatch model

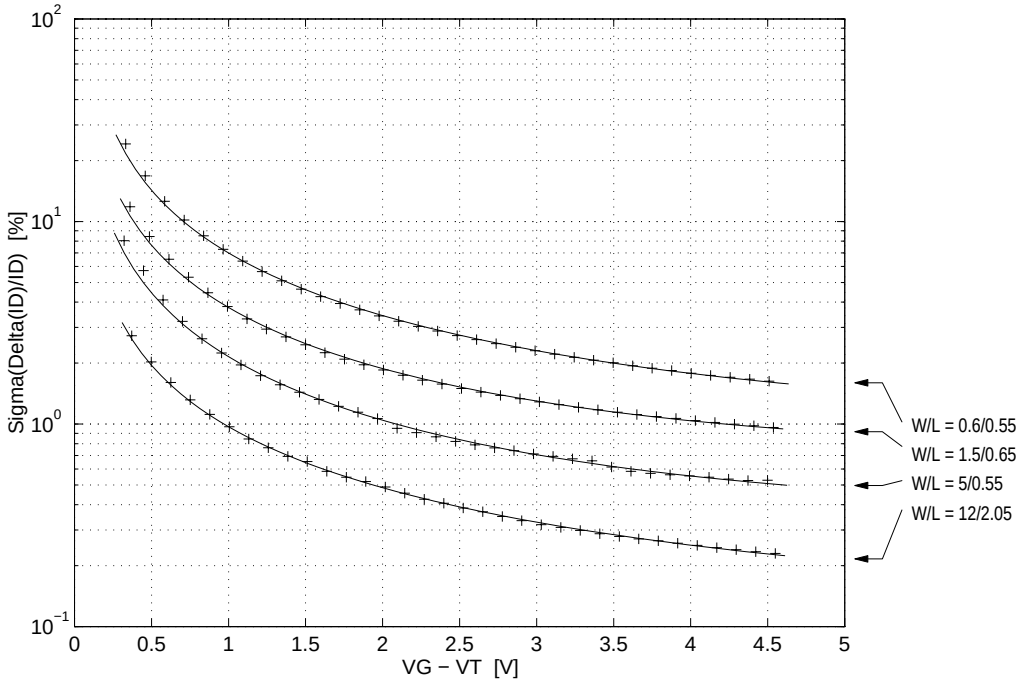

Fig. 4.4 PMOSM relative drain current mismatch vs. VG-VT, +...measurement, —...mismatch model

5. Circuit Simulators and Models

The models are supported and qualified for the specified simulator revision. Previous simulator versions are also supported, for detailled questions please contact us at tips@austriamicrosystems.com .

Simulator	MOS Model	
	BSIM3v3 level 53	Matching
Spectre/SpectreS	4.4.6	4.4.6

The following models are supported for all simulators mentioned above:

bipolar transistors:	BJT Gummel-Poon
diodes:	D level 1
resistors:	R / JFET level 1
capacitors:	C
Zener diode:	SUBCKT

Updates of model revisions can be found in the “Simulation Parameters” section of the HIT-Kit link on our technical web server: http://asic.austriamicrosystems.com

Updates of netlist formats can be found in the “Netlist Formats” section of the HIT-Kit link on our technical web server: http://asic.austriamicrosystems.com

Updates of simulation parameters can be downloaded from the “Download Area” of our technical web server: http://asic.austriamicrosystems.com

Mismatch models for Monte Carlo simulation are provided as part of the Cadence HIT-Kit. A tutorial on Monte Carlo simulation using Spectre/Cadence is provided in the “Statistical Circuit Simulation” section of the HIT-Kit link on our technical web server: http://asic.austriamicrosystems.com

6. Support

For questions on process parameters please refer to:

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