Hw 3. (CSE3080)

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1. [40 points]
A small 16-bit address space special-purpose processor may be equipped with one of two tiny direct-mapped caches, C1 or C2, each of which has a total capacity of 64 bytes. C1 has a blocksize of 4 bytes (which corresponds to the size of an integer on this system) while C2 has a blocksize of 16 bytes.
(a) What are the cache parameters (m, C, B, E, S, t, s, b) for C1 and C2?
(b) Consider that the following sequence of addresses are read, (where the size of the data path equals the blocksize): BA00, BA04, AA08, BA05, AA14, AA11, AA13, AA38, AA09, AA0B, BA04, AA2B, BA05, BA06, AA09, AA11.
For each cache option, specify which references are hits and which are misses, and show the final data content of the cache.

(a) C1. → m C B E S t s b. ($2^s=S$, $2^b=B$.)

m	C	B	E	S	t	s	b
16	64	4	1	16	10	4	2

memory address size. C=BES. t+s+b=m.

address 16-bit
direct → line 1m → E=1 → block size → 4bytes.
Capacity → 64 byte.

C2 → m C B E S t s b. ($2^s=S$, $2^b=B$.)

m	C	B	E	S	t	s	b
16	64	16	1	4	10	2	4

memory address size. C=BES. t+s+b=m.

address 16-bit
direct → line 1m → E=1 → block size → 16bytes
Capacity → 64 byte.

(b) C1.

	m	t	s	b.	Cache hit?
① BA00 →	1011 1010 0000 0000.				M
BA04 →	1011 1010 0000 0100				M
AA08 →	1010 1010 0000 1000				M
BA05 →	1011 1010 0000 0101				H
AA14 →	1010 1010 0001 0100				M
AA11 →	1010 1010 0001 0001				M
AA13 →	1010 1010 0001 0011				H.
AA38 →	1010 1010 0011 1000				M
AA09 →	1010 1010 0010 0001				H
AA0B →	1010 1010 0010 0011				H
BA04 →	1011 1010 0000 0100				H
AA2B →	1010 1010 0010 1011				M
BA05 →	1011 1010 0000 0101				H
BA06 →	1011 1010 0000 0110				H
AA09 →	1010 1010 0010 0001				H
AA11 →	1010 1010 0010 0011				H

tag bits. valid bits.

Cache

Set 0	1011 1010 00	*BA00	*BA01	*BA02	*BA03
Set 1	1011 1010 00	*BA04	*BA05	*BA06	*BA07
Set 2	1010 1010 00	*AA08	*AA09	*AA0A	*AA0B
Set 3					
Set 4	1010 1010 00	*AA10	*AA11	*AA12	*AA13
Set 5	1010 1010 00	*AA14	*AA15	*AA16	*AA17
Set 6					
Set 10	1010 1010 00	*AA28	*AA29	*AA2A	*AA2B
Set 14	1010 1010 00	*AA38	*AA39	*AA3A	*AA3B

	m	C	B	E	S	t	s	b
$C_1 \rightarrow$	16	64	16	1	4	10	2	4

(b)

	t	S	b	Cache hit?
① BA00 →	1011 1010 00	00	00 0 0	M
BA04 →	1011 1010 00	00	01 0 0	H
BA08 →	1010 1010 00	00	10 0 0	M
BA09 →	1011 1010 00	00	01 0 1	M
AA14 →	1010 1010 00	01	01 0 0	M
AA11 →	1010 1010 00	01	00 0 1	H
AA13 →	1010 1010 00	01	00 1 1	H
AA28 →	1010 1010 00	11	10 0 0	M
AA09 →	1010 1010 00	00	10 0 1	M
AA0B →	1010 1010 00	00	10 1 1	H
BA04 →	1011 1010 00	00	01 0 0	M
AA2B →	1010 1010 00	10	10 1 1	M
BA05 →	1011 1010 00	00	01 0 1	H
BA06 →	1011 1010 00	00	01 1 0	H
AA09 →	1010 1010 00	00	10 0 1	M
AA11 →	1010 1010 00	01	00 0 1	H

	valid bit	tag bits	
set 0	1	1010101000	*AA00 – *AA0F
set 1	1	1010101000	*AA10 – *AA1F
set 2	1	1010101000	*AA20 – *AA2F
set 3	1	1010101000	*AA30 – *AA3F

Content of the cache.

2. [40 points]

Given a cache with parameters little m = 32, little b = 8, little s = 8 and E = 4.

Assume that:

sizeof(element)	= 8 bytes
@x[256]	= AAAA0000
@y[256]	= AABB0000
@a[512]	= AAAA8000
@b[512]	= AABB8000

value1 and value2 are in registers

Use the code segment:

```
for i = 0 to 255
    value1 = x[ i ] × y[ i ]
    for j = 0 to 1
        value2 = a[ i×2+j ] + b[ i×2+j ]
```

i=0. 0 1 — 2 3 — 4 5

(a) Fully describe the cache in terms of the cache parameters discussed in class.
(b) What is the hit rate for each of x, y, a and b?
(c) What is the overall hit rate?
(d) What are the cache contents after 1 iteration of the " i " loop?
(e) What are the cache contents after the completion of the " i " loop?

t s b

x AAAA 0000 0000 0000 0000
y AABB 0000 0000 0000 0000
a AAAA 1000 0000 0000 0000
b AABB 1000 0000 0000 0000

(a) m C B E S t s b.
32 2^{18} 256 4 256 16 8 8

Sizeof(elem) = 8byte. (2^3) (2^2) (2^8)

X[0]: miss
X[1-31]: Hit

(b)

Ask	Get	set	Cache hit.		hit rate
X[0]	X[0-31]	0	M	line 1	X: 31/32
Y[0]	Y[0-31]	0	M	line 2	y: 31/32
X[32]	X[32-63]	1	M	line 1	a: 31/32
⋮					b: 31/32
X[224]	X[224-255]	7	M	line 1	
Y[224]	Y[224-255]	7	M	line 2.	
a[0]	a[0-31]	128	M	line 1	
b[0]	b[0-31]	128	M	line 2	
a[1]	a[0-31]	128	H	line 1	
b[1]	b[0-31]	128	H	line 2	
⋮					
a[32]	a[32-63]	129	M	line 1	
⋮					
a[480]	a[480-511]	143	M	line 1	
b[480]	b[480-511]	143	M	line 2	

(c). i=0. X:M Y:M — j=0, 1 — M,M H,H

i=1 — H H — j=2,3

i=15 — j=30,31 — M,H

i=16 — j=32,33 — M,M

i=31 — j=62,63 — H,H.

$$1 - \frac{6}{32\times2+64\times2} = 1 - \frac{6}{64+128} = 1 - \frac{6}{192} = 1 - \frac{1}{32} = \frac{31}{32}$$

(d) X[0-31]
Y[0-31]
a[0-31]
b[0-31]

(e) X[0-255]
Y[0-255]
a[0-511]
b[0-511]

(d) Set 0 → X[0-31] line 1
Set 0 → Y[0-31] line 2
Set 128 → a[0-31] line 1
Set 128 → a[0-31] line 2

more detail.

(e) Set 0 → X[0-31] line 1
Set 0 → Y[0-31] line 2
Set 1 → X[32-63] line 1
Set 1 → Y[32-63] line 2
⋮
Set 11 → X[224-255] line 1
Set 11 → Y[224-255] line 2

Set 128 → a[0-31] line 1
→ b[0-31] line 2
⋮
Set 143 → a[480-511] line 1
→ b[480-511] line 2

3. [20 points]
Which of the following cache hierarchies will provide better AMAT?

Hierarchy A	hit time (cycles)	hit rate
L1 cache	2	25%
L2 cache	10	80%
L3 cache	80	95%
Main memory	500	

Hierarchy B	hit time (cycles)	hit rate
L1 cache	2	50%
L2 cache	5	65%
L3 cache	20	80%
Main memory	500	

A. AMAT: $2+0.75(10+0.2(80+0.05(500)))=\frac{101}{4}=25.25$

25
105
21
31
93/4

B. AMAT: $2+0.5(5+0.35(20+0.2(500)))=\frac{51}{2}=25.5$

100
120
42
47
47/2

1
12
35
60
36
420

∴ A가 B AMAT이 작기 때문에 B가 좋은 성능을 낸다.