Latch and Flip Flops

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Storage Elements

- **A storage element**
  - ✓ It can maintain a binary state indefinitely (as long as power is delivered to the circuit)
- **Type of storage element**
  - ✓ Latch: operate with signal level (rather than signal transition)
    - Level sensitive device
    - Building blocks of flip-flops
  - ✓ Flip-flop: controlled by a clock transition
    - Clock edge-sensitive device

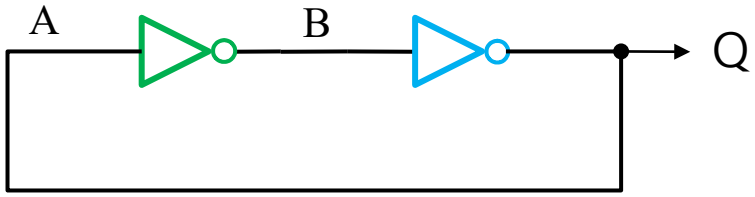
Simple Memory Element

- **Two inverters with feedback loop**
  - ✓ There are two nodes, A and B
  - ✓ Two possible states
    - A=0, B=1
    - A=1, B=0

- How can we change the state of the circuit?

Simple Memory Element

- **How can we change the state of the circuit?**
  - ✓ (1) Replace inverters with NORs
  - ✓ (2) We can control the input of NOR gate to change the state of the circuit



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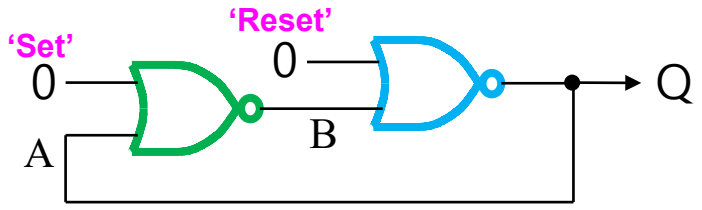

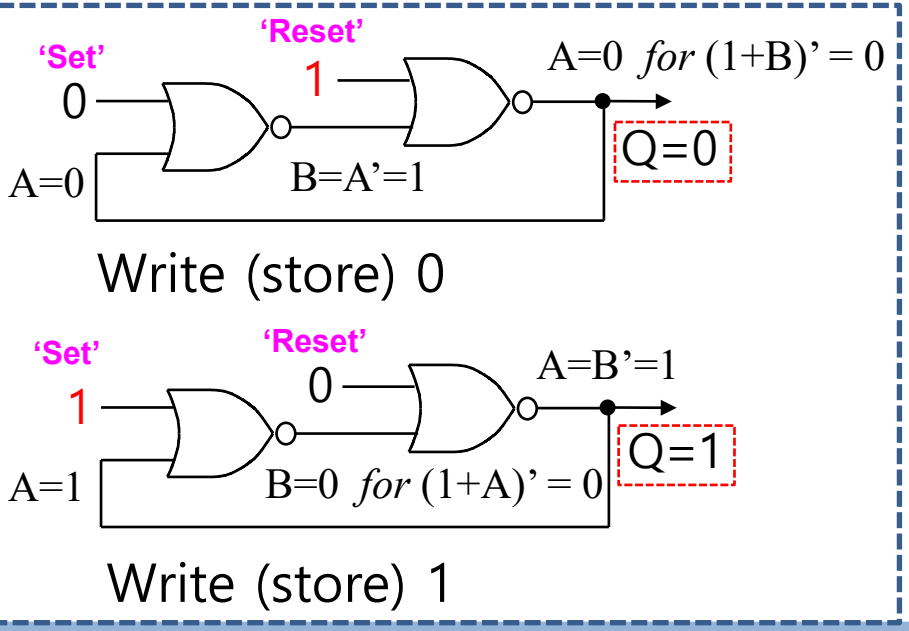

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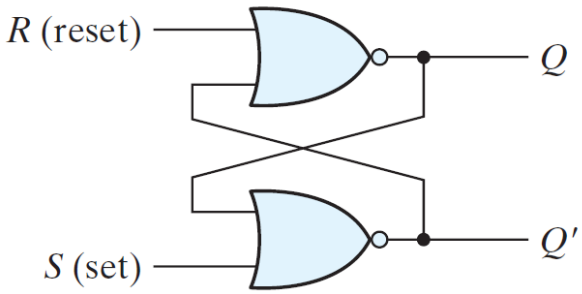
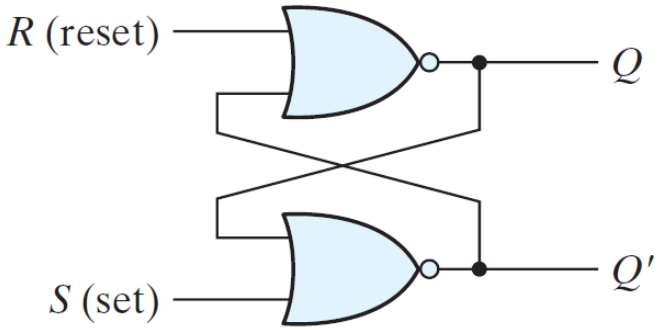


→ Latch

Latch

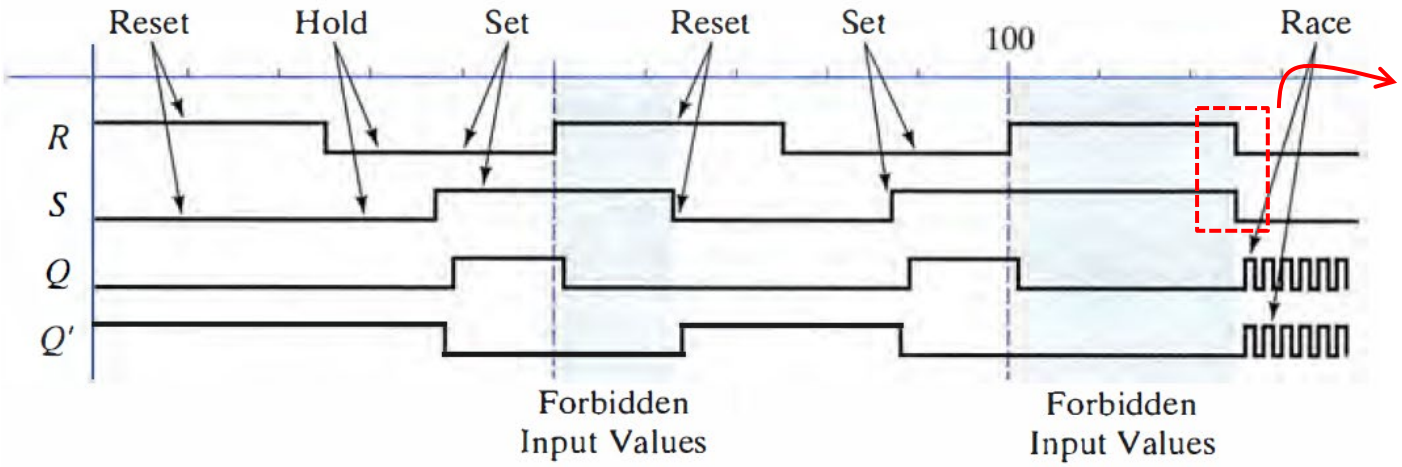
- **SR latch (Set/Reset latch)**
  - ✓ Cross-coupled circuit with NOR gates



<Logic diagram>

S	R	Q	Q′
0	0	Hold	Hold
0	1	0	1
1	0	1	0
1	1	Forbidden	Forbidden

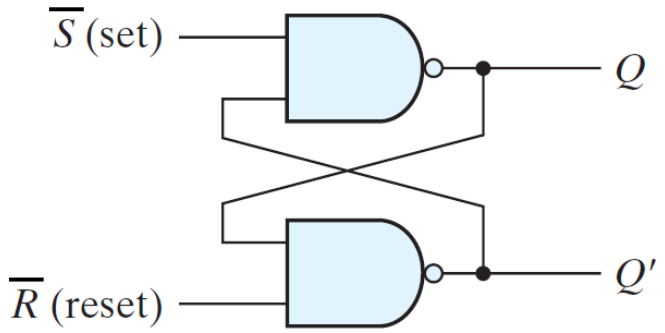
<Functional truth table>



*State change from SR=11 to SR=00 at the same time is strongly forbidden → oscillation occurs

Latch

- **SR latch (Set/Reset latch)**
  - ✓ Cross-coupled circuit with NAND gates

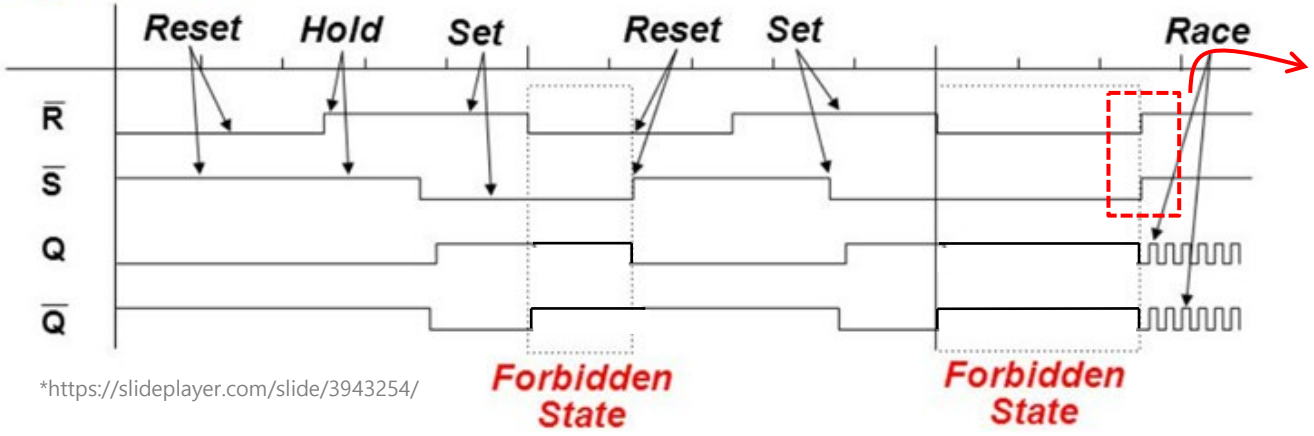


*Active low input **<Logic diagram>**

S R	$\bar{S}$ $\bar{R}$	Q	Q′
0 0	1 1	Hold	Hold
0 1	1 0	0	1
1 0	0 1	1	0
1 1	0 0	Forbidden	Forbidden

<Functional truth table>

Timing Waveform

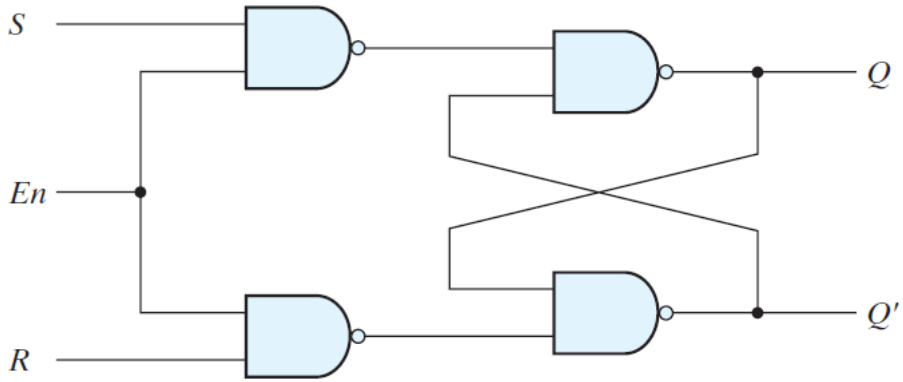


*https://slideplayer.com/slide/3943254/

*State change from SR=11 to SR=00 ($\bar{S}\bar{R} = 00$ *to* $\bar{S}\bar{R} = 11$) at the same time is strongly forbidden → oscillation occurs

Latch

- **Gated SR latch (Set/Reset latch)**
  - ✓ Cross-coupled circuit with NAND gates



*Active high input

<Logic diagram>

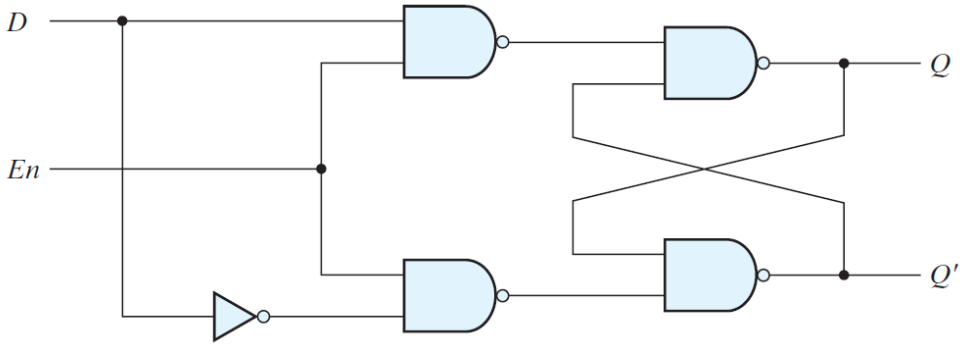
En	S	R	Q	Q'
0	X	X	Hold	Hold
1	0	0	Hold	Hold
1	0	1	0	1
1	1	0	1	0
1	1	1	Forbidden	Forbidden

<Functional truth table>

- ✓ **'En'** acts as an enable signal for the other two inputs
  - En=0 case, the circuit remains in its current state, not in Reset.

Latch

- **D latch (Transparent latch)**
  - ✓ One way to eliminate the undesirable condition (SR=11) is to ensure that inputs S and R are never equal to '1' at the same time → D latch *D means 'data'
  - ✓ If 'En'=1, output Q changes depends on the input
    - Q=0 @ D=0
    - Q=1 @ D=1



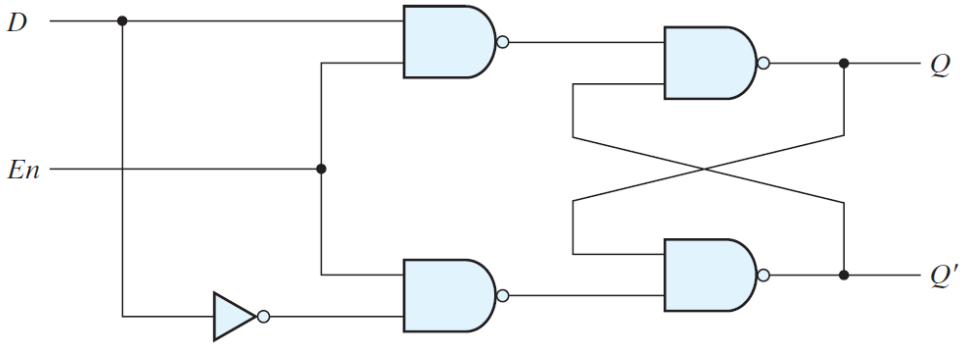
<Logic diagram>

En	D	Q	Q'
0	X	Hold	Hold
1	0	0	1
1	1	1	0

<Functional truth table>

Latch

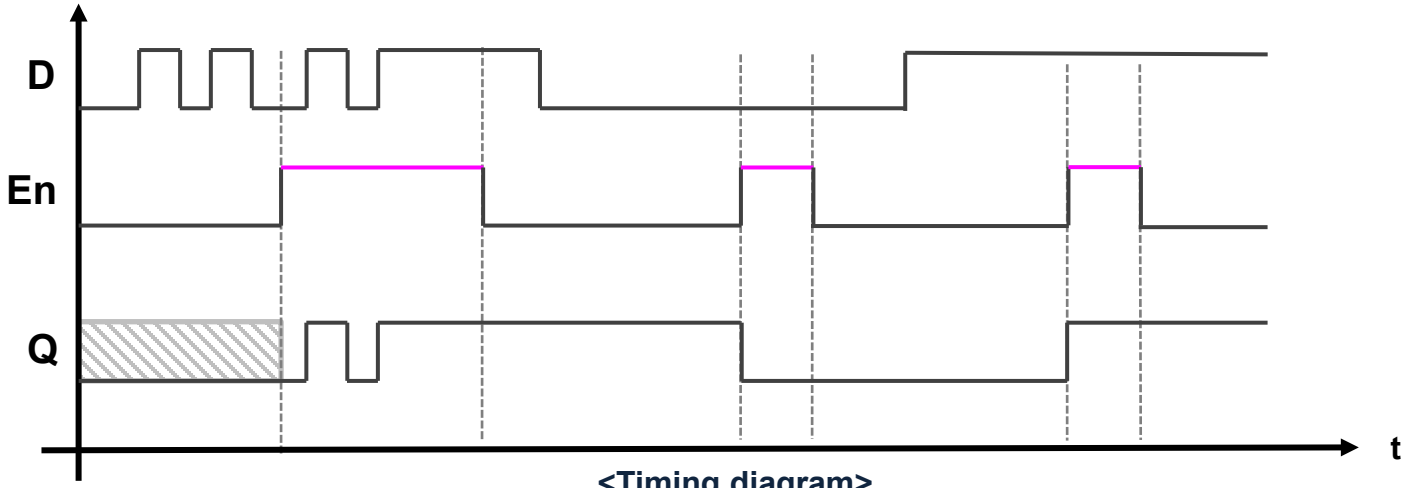
- **D latch (Transparent latch)**
  - ✓ Timing diagram



<Logic diagram>

En	D	Q	Q'
0	X	Hold	Hold
1	0	0	1
1	1	1	0

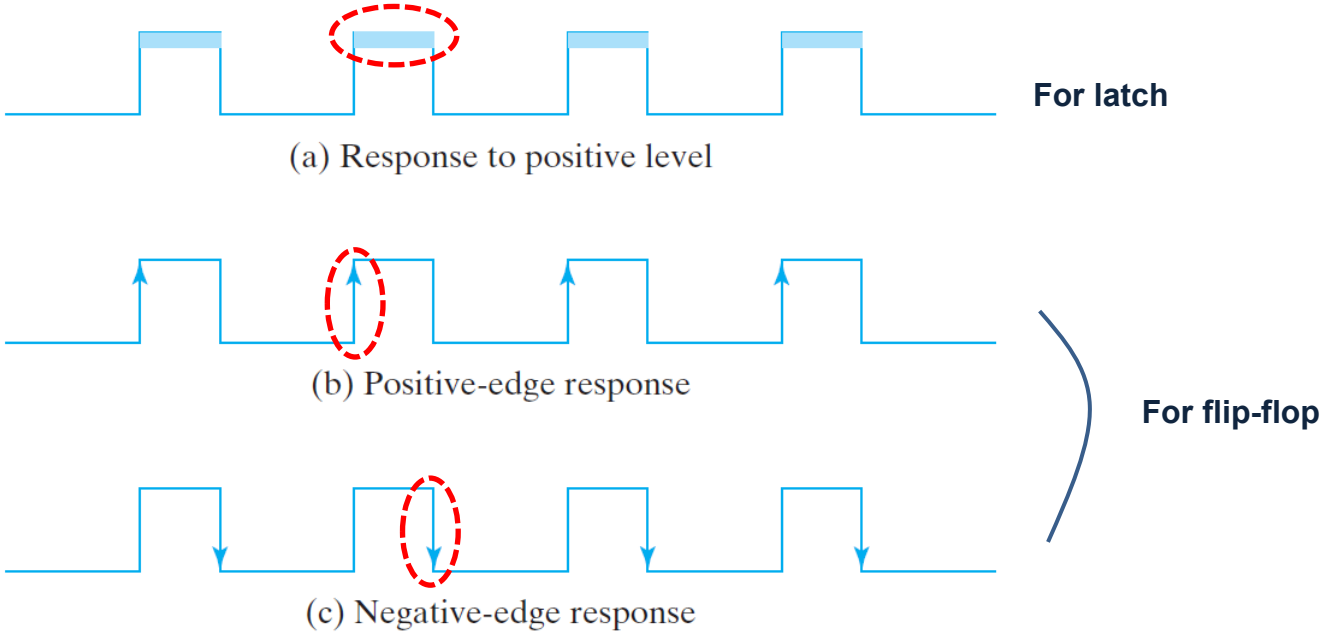
<Functional truth table>



<Timing diagram>

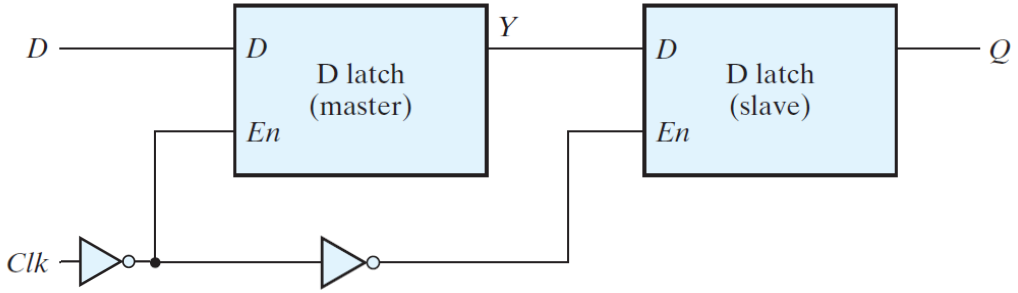
Flip Flops

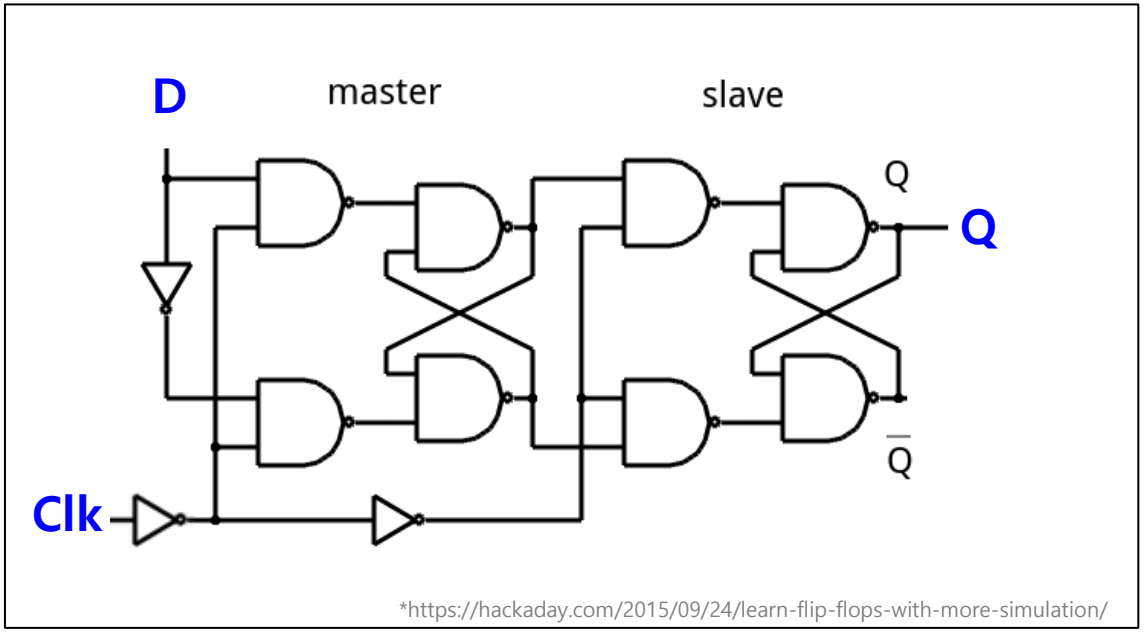
- **Clocked binary storage device**
  - ✓ Output will only change on the transition of the clock
  - ✓ So it is referred to as edge-triggered circuit
    - 1) positive-edge triggered
    - 2) negative-edge triggered



Flip Flops

- **D flip-flop**
  - ✓ Master-slave architecture: using two D-latches

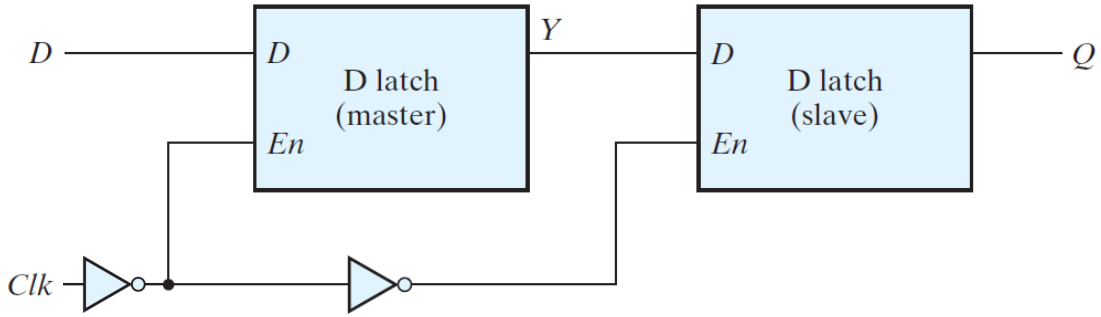




*https://hackaday.com/2015/09/24/learn-flip-flops-with-more-simulation/

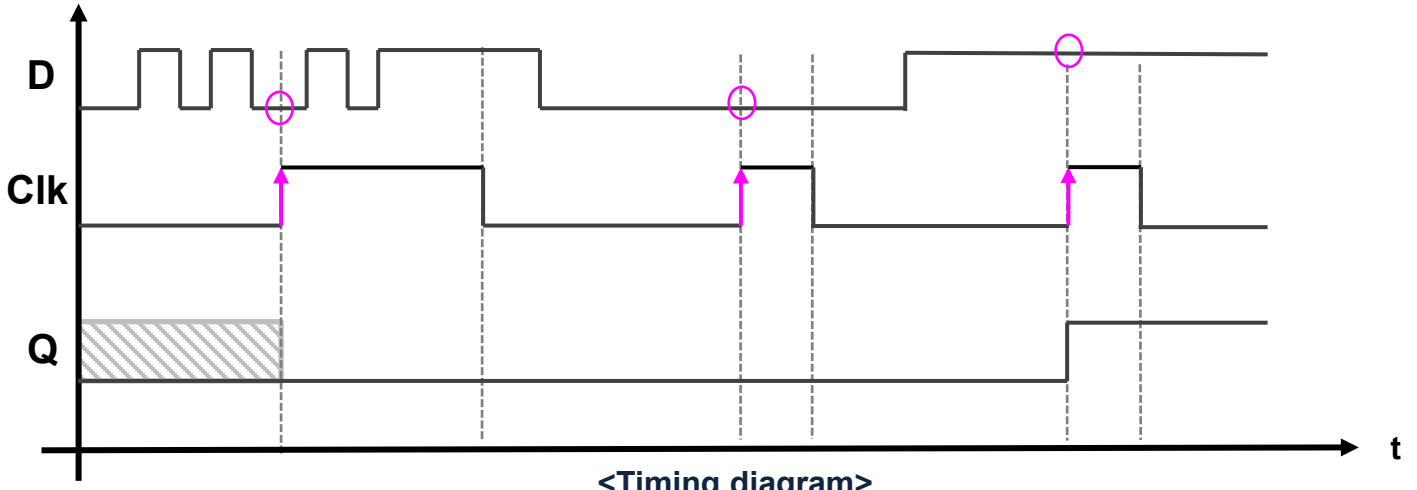
Flip Flops

- **D flip-flop**
  - ✓ Timing diagram



Clk	D	$Q_{(t+1)}$
0 or 1	X	Hold
↑	0	0
↑	1	1

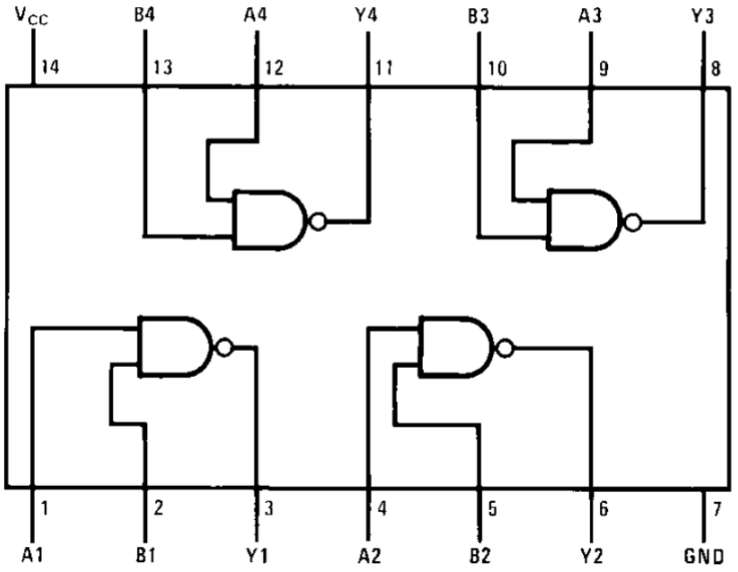
<Positive edge triggered type>



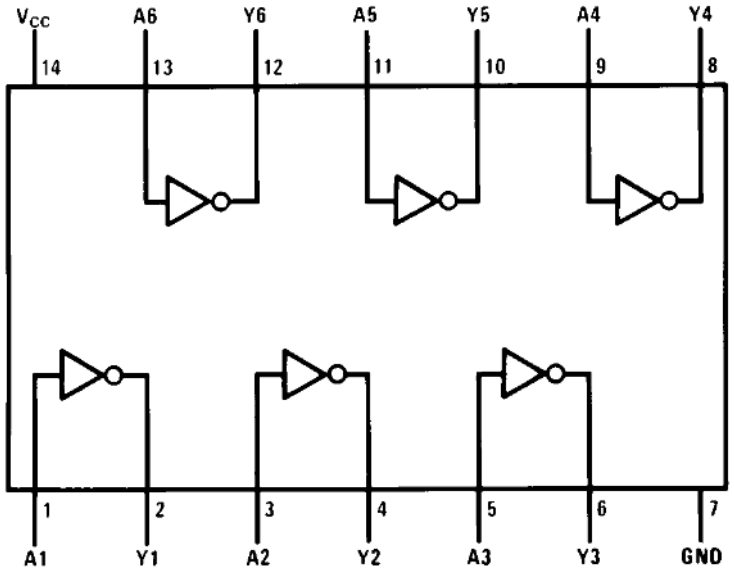
<Timing diagram>

ICs

7400



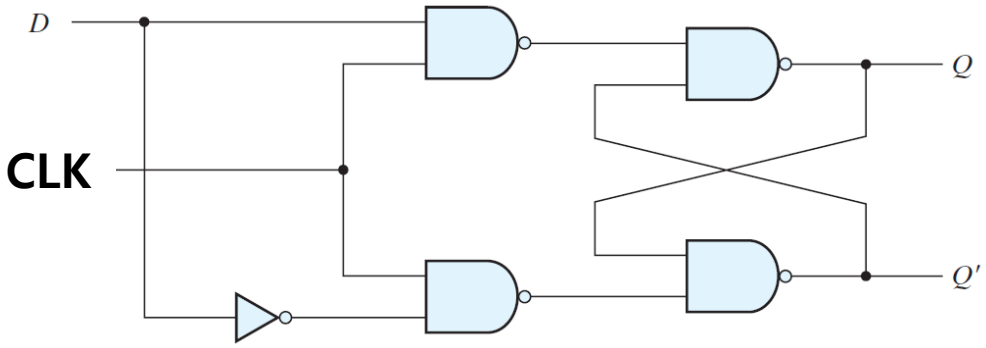
7404



실험 1

- **NAND based SR-latch를 활용한 D-latch 설계 (74LS00, 74LS04 사용)**
  - ✓ CLK (AWG ch1)
    - Type: Square, Freq: 1KHz, Amp: 2.5V, Offset: 2.5V
    - Symmetry: 50%, phase: 0°
  - ✓ D (AWG ch2)
    - Type: Square, Freq: 500Hz, Amp: 2.5V, Offset: 2.5V
    - Symmetry: 50%, phase: 45°
  - ✓ EEboard Oscilloscope로 파형 측정 (y축:2V/div, x축: 0.5ms/div)
    - Ch1: CLK, ch2: D, ch3: Q
    - DC coupling mode로 측정

*Waveform SW에서 설정 및
Ch1, Ch2 *synchronization* 하기



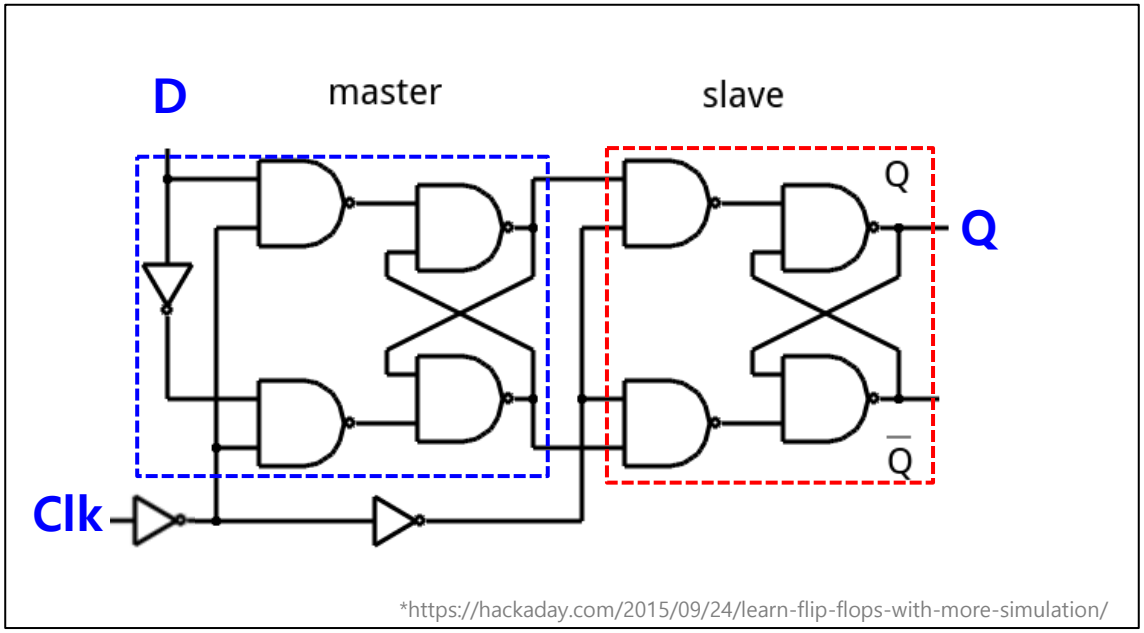
<Logic diagram>

CLK	D	Q	Q'
0	X	Hold	Hold
1	0	0	1
1	1	1	0

<Functional truth table>

실험 2

- **D-latch-based rising edge triggered D Flip-Flop 설계**
  - ✓ 입력 신호 및 오실로스코프 setting은 이전과 동일
  - ✓ EEboard Oscilloscope로 파형 측정 (y축:2V/div, x축: 0.5ms/div)
    - Ch1: CLK, ch2: D, ch3: Q
    - DC coupling mode로 측정



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