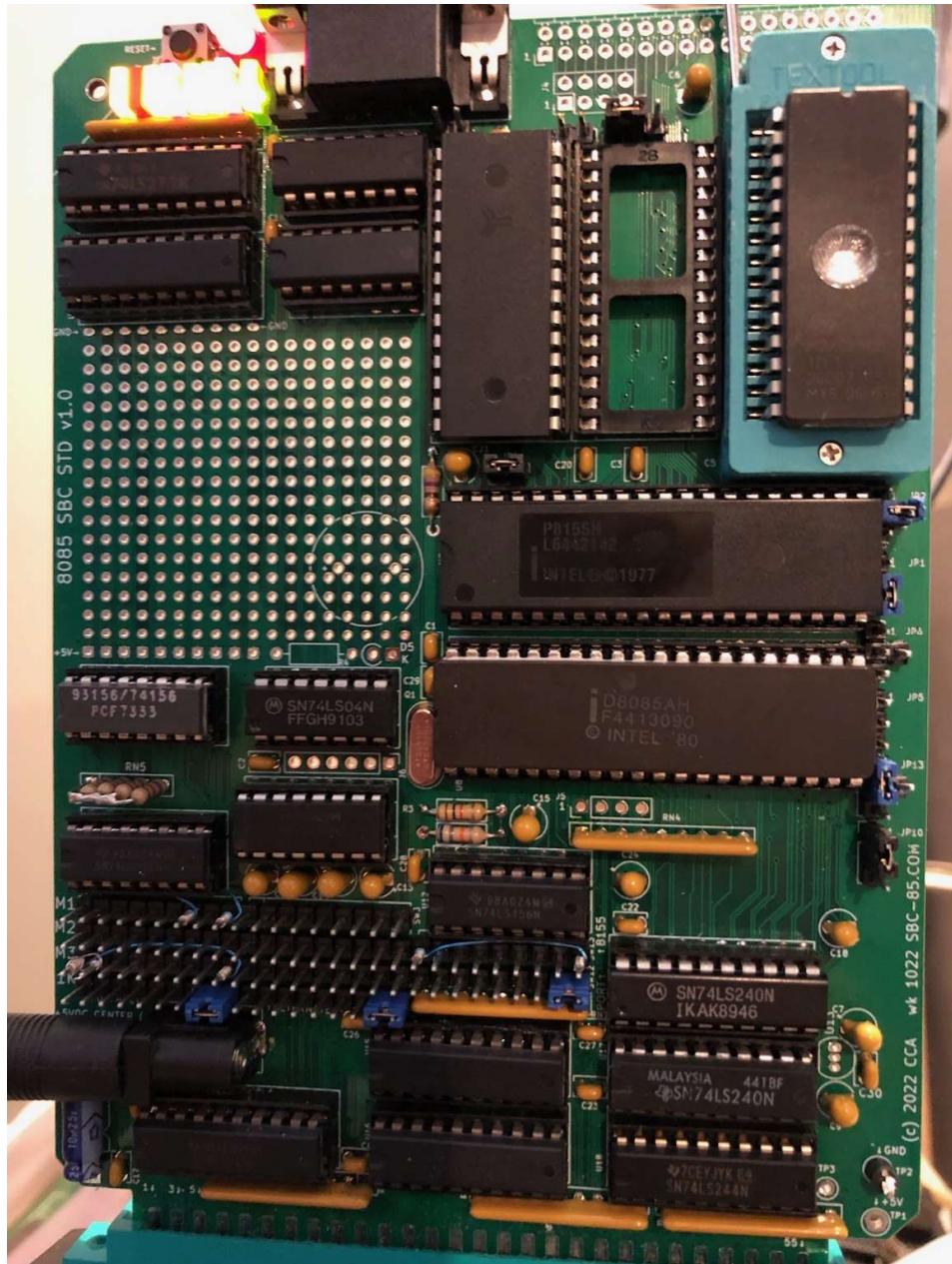


STD Bus 8085 Single Board Computer

This user's guide for the STD-85 Single Board Computer

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Notation:

Pin numbers. Pin numbers are given as **ID.pin**. for example, Pin 5 of connector X3 is given as **X3.5**. IC7 pin 21 is given as **IC7.21**.

Logic Levels. Lines having a signal that is active low is given with either an asterisk or a slash following the signal name. For example, **CS8/** and **CS11*** both refer to signals that are active when at 0V or logic low.

Terminology:

Most abbreviations will be spelled out when they are first used. However, the more commonly used terms are described in the **Definitions of Terms and Notations** at the end of the document.

STD-85 DESCRIPTION

The STD-85 is an 8085 based Single Board Computer designed to operate on the STD bus. As such, it contains all elements required for stand-alone operation including the processor, Random Access Memory (RAM) and Read Only Memory (ROM or EPROM). The SBC-85 also includes an RS232 Serial port with a female DB9 connector for communication with a terminal. Finally, the board includes an expansion bus for insertion into a STD backplane.

The primary components on the STD-85 are as follows:

U8 - 8085 Microprocessor operating at 3MHz

M1, M2, M3 – JEDEC 28-pin Memory Sockets (clearance around M3 allows for ZIF socket installation)

U7 – 8155 RAM, I/O, Timer

U9 – MAX232 TTL / RS232 Level Shifter

U4 – 74LS573 Low Byte Address Latch

U2, U5, U12 – 74LS156 1-of-8 Memory Map Decoders

U14, U15, U16, U17, U18, U19 – Bus Drivers / Transceivers

Additional ‘glue logic’ includes the following:

U1 – 74LS273 Octal Latch Onboard Port (OBP)

U6 – 74LS32 Quad 2-Input OR

U10 – 74LS07 Quad 2-Input AND

U11 – 74LS04 HEX Inverter

CIRCUIT DESCRIPTION

8085

The 8085 microprocessor needs only +5VDC and an oscillator input to operate. On the STD-85, the oscillator input is provided by Q1 which is a 6.144MHz crystal. The 8085 immediately begins fetching instructions from address 0x0000 upon power up, however the power up must be somewhat controlled to allow the 8085’s internal charge pump to build sufficient charge before the CPU fetches its first instruction. Because of this, the 8085 needs a slight delay in the release of its *ResetIN** after power up. This is accomplished by the RC circuit which is a 56K (R2) bleed into a 1uF (C15) capacitor and/or with the power supervisory circuit U13. After power is applied, this RC circuit takes around 80 uS to reach a logic high on *RESETIN**, and releasing the CPU from reset. Likewise the power supervisory circuit holds the 8085 *RESETIN** asserted unless the +5V rail is above 4.85V to hold/put the processor in reset during power up or upon power fail.

Once out of reset, the CPUs operation is controlled by its *READY*, *HOLD*, and *TRAP* inputs. The *READY* is primarily intended as a means of an external circuit pausing the CPUs operation so it can “catch-up”, e.g., so slow memory or a slow I/O port can stop the CPU until it can complete a requested action. Therefore, for the CPU to operate the *READY* must be TRUE, or logic one. This is accomplished by (4.7K) pull-up resistor RN3.4 holding *bREADY* high unless it is being driven by the bus. The *HOLD* input is a similar means of stopping the CPU, but its use is to stop the 8085 from operating in order to allow another device to take control of the system. This is commonly used in systems having multiple CPUs or sub-circuits that operate autonomously such as Direct Memory Access (DMA), Disk Drive Interfaces, etc.

Like the *bREADY*, the *HOLD* must be held inactive for the 8085 to fetch instructions, but in this case *HOLD* is asserted with a logic one, so *HOLD* must be at logic zero for the 8085 to operate. *HOLD* is created (U14.3) by inverting (U14.17) the bus signal *bus Request* (*/bHLDA*) which, when not driven by the bus, is held high by another (4.7K) resistor in RN3.2.

Finally, the 8085’s operation can be interrupted by hardware inputs, namely the *TRAP*, *RST7.5*, *RST6.5*, and *RST5.5* which are all inverted by U14. *RST7.5*, *RST6.5*, and *RST5.5* are brought to a four-position header for user

connections to other onboard signals. *TRAP* is driven by the bus signal *bNMIRQ* (bus Non-Maskable Interrupt ReQuest). Of these, all are disabled when the processor first starts except for the TRAP which cannot be masked or turned off. The *TRAP* input to the 8085 must be held low to prevent the CPU from attempting to fetch an instruction from the memory location 0x0024. **Therefore, for the 8085 to operate the RN2, RN3, and RN4 must be installed.**

ADDRESS LATCH

The 8085 has 16 address lines and can therefore access 2^{16} locations or 65536 address (a.k.a. 64KB) of memory. During each memory access the 8085 first puts all 16 addresses onto the output bus, but the lower 8-bits (AD0-AD7) are only held for a short period before those eight lines are used to transfer the data byte. While the lower address byte is transient, most components require that the lower 8 address bits be continuously available throughout the machine instruction. This is accomplished by U4 which is an 8-bit (octal) latch which takes the transient input of AD0-AD7 and creates a sustained A0-A7. AD0-AD7 are latched on the falling edge of the 8085's Address Latch Enable (*ALE*) signal. In operation, the 8085 puts the lower address byte on AD0-AD7 and raises the *ALE* signal and the AD0-AD7 logic levels exit the latch on Q1-Q8 onto the A0-A7 address lines. After enough time is given for these signals to propagate and stabilize, the 8085 lowers the *ALE* signal and the values are latched onto the A0-A7 signals. When combined with the A8-A15 signals, which the 8085 is still holding, the rest of the system now has a sustained A0-A15 address.

ADDRESS DECODING

As the 8085 microprocessor outputs addresses for memory locations or I/O ports, a portion of the circuit known as an *address decoder* determines which addresses are in which component. As its name implies, the address decoder uses the address output from the 8085 onto the A0-A15 address bus and compares this address to the system *address map*. As the result of the comparison, while there may be several components connected to the same data bus, only a single device will be selected to communicate with the CPU.

Default / Alternate Address Maps

The STD-85 has two address configuration called DEFAULT and ALTERNATE (or SWAP). The selection of which map is currently enabled is controlled by the least significant "SWAP" bit of the onboard port U1. Setting the LSBit enables the SWAP address map, clearing the bit enables the DEFAULT address map.

U2 and U5 are one of eight decoders whose output is controlled by the high three address bits, i.e., A13, A14, and A15. Each of these decoders therefore break the entire addressable address range into eight 8K address blocks as follows:

A15	A14	A13	Starting Address	Ending Address	Output Select	Output Pin
0	0	0	0x0000	0x1FFF	Q0b	9
0	0	1	0x2000	0x3FFF	Q1b	10
0	1	0	0x4000	0x5FFF	Q2b	11
0	1	1	0x6000	0x7FFF	Q3b	12
1	0	0	0x8000	0x9FFF	Q0a	7
1	0	1	0xA000	0xbFFF	Q1a	6
1	1	0	0xC000	0xdFFF	Q2a	5
1	1	1	0xE000	0xFFFF	Q3a	4

The select output of U2 and U5 are simultaneously controlled by A15, A14, and A13 but their respective Eb2 enable inputs are used to make the outputs of U2 and U5 mutually exclusive. When the default address map is being used, Eb2 (U6.15) is low and the outputs of U5 control the memory mapping. When the alternate (SWAP) memory map is being used, U5 is disabled and the Eb2 input of U2 is taken low to allow U2 to control the memory mapping. As the final result, at any particular memory address, exactly one of the 16 outputs of U2 and U5 will be taken low.

The eight output of U2 and the eight outputs of U5 are each connected in parallel to the address map selection switches (or wire wrap pins). For the default memory map these are SW2, SW6, SW8, and SW10 which select the address mapping for memory sockets M1, M2, M3 and the further divided 1K address block described later. Likewise, for the alternate map these are SW3, SW7, SW9, and SW11. The common pin of each of these switches are connected together for each socket, e.g., for M1 the common output of SW2 and SW3 are tied together and are used to control the enabling of that socket.

To configure when an particular memory socket is selected, i.e., the address space for M1, M2, M3, and the 1K blocks, the switch for that address block is closed or a wirewrap jumper is installed between the common pin and the desired address block from U2 (default address) and U5 (alternate address). More than one address block can be

selected to allow multiple 8K blocks to enable a particular device. Normally these address blocks will be coterminous, but that is left up to the user. The only requirement is that each of the address blocks may only be tied to the output of one switch in that map, e.g., the address block 0x0000-0x1FFF may only be claimed in SW2, SW6, SW8 or SW10 for the default map and (simultaneously) only be claimed by one of SW3, SW7, SW9, or SW11 for the alternate map. To be clear, since the default and alternate maps are mutually exclusive, any memory block address can be claimed once in each mapping.

As an example, to assign memory address block from 0x0000 to 0x7FFF to M1 in the default map, close SW2.1, SW2.2, SW2.3, and SW2.4. (or wirewrap jumpers between pins 1,2,3,4 and pin 9). To assign this same address block to M2 in the alternate map, close SW7.1, SW7.2, SW7.3, and SW7.4. In the same manner, the remaining address blocks can be assigned to the other memory sockets and the 1K blocks for both the default and the alternate memory maps.

The net result of all this address selection is that for any specific address, at most one of the four select lines leaving the mapping array (*/1K_DECODE*, */M1_DECODE*, */M2_DECODE*, */M3_DECODE*) will be asserted at any time. It is possible, and acceptable, that no onboard memory is selected so none of the four selection lines are asserted.

The final aspect of this design is that the outputs of the U2 and U5 decoders are open collector which is what allows the multiple address selection outputs to be connected together. These outputs are pulled up using resistor network RN5.

In addition to the eight 8K address blocks, the fourth selection made by SW10 and SW11 is further decoded into 1K address blocks using the next three address bits, i.e., address lines A12, A11, and A10 feeding U12. In the same manner of selecting the 8K memory blocks, these 1K memory blocks are selected by closing switches in SW12 and SW13 for the On Board Port (OBP) and the onboard 8155 respectively.

The four decode selections (*/M1_DECODE*, */M2_DECODE*, */M3_DECODE* and */1K_DECODE*) are further gated with the */IO_M* signal (U6A, U6B, U6C) to enable the memory sockets only during a memory bus cycle, and with */IO_M* (U6D) enable the onboard port only during a I/O cycle.

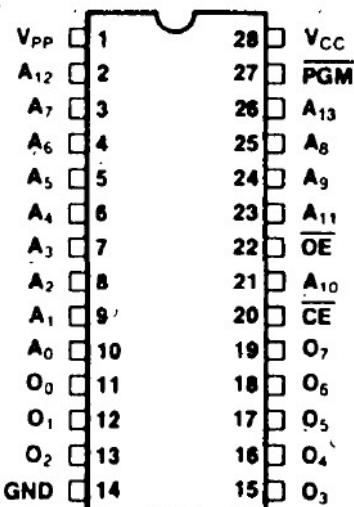
The three enable signals are provided directly to M1, M2, and M3 to enable the memory chips. However, to latch data into the onboard port, the onboard port select (*/OBP_SEL*) is further gated with the write strobe (*/WR*) to create a rising clock edge into U1.

UNIVERSAL EPROM SOCKETS

Nearly from the very beginning, the industry recognized that the ever-increasing availability of larger and larger ROM devices was going to be problematic if a standard was not adopted. The design scheme resulted in the "Universal Site" Socket concept in-which all future ROMs, PROMs, and EPROMs would have pin mapping such that, with minor adjustments, the different sizes of EPROMS were compatible if bottom justified in the socket. The following graphic (lifted from the 1984 Intel Memory Components Handbook) is a typical example. The 27128 is shown in the center and the function of each pin on the left and the right is shown in the corresponding table on each side. This concept was eventually standardized by the Joint Electron Device Engineering Council (JEDEC) and the socket referred to as the JEDEC 28-Pin Universal Memory Socket.

27128A

27256	2764A	2732A	2716
V _{PP}	V _{PP}		
A ₁₂	A ₁₂		
A ₇	A ₇	A ₇	A ₇
A ₆	A ₆	A ₆	A ₆
A ₅	A ₅	A ₅	A ₅
A ₄	A ₄	A ₄	A ₄
A ₃	A ₃	A ₃	A ₃
A ₂	A ₂	A ₂	A ₂
A ₁	A ₁	A ₁	A ₁
A ₀	A ₀	A ₀	A ₀
O ₀	O ₀	O ₀	O ₀
O ₁	O ₁	O ₁	O ₁
O ₂	O ₂	O ₂	O ₂
Gnd	Gnd	Gnd	Gnd



2716	2732A	2764A	27256
V _{CC}	V _{CC}	V _{CC}	V _{CC}
PGM	N.C.	A ₁₄	A ₁₄
A ₈	A ₈	A ₈	A ₈
A ₉	A ₉	A ₉	A ₉
V _{PP}	A ₁₁	A ₁₁	A ₁₁
OE	OE/V _{PP}	OE	OE
A ₁₀	A ₁₀	A ₁₀	A ₁₀
CE	CE	CE	CE
O ₇	O ₇	O ₇	O ₇
O ₆	O ₆	O ₆	O ₆
O ₅	O ₅	O ₅	O ₅
O ₄	O ₄	O ₄	O ₄
O ₃	O ₃	O ₃	O ₃

NOTE: INTEL "UNIVERSAL SITE"-COMPATIBLE EPROM PIN CONFIGURATIONS ARE SHOWN IN THE BLOCKS ADJACENT TO THE 27128A PINS.

For example, pin 28 (top right) is not present on the 2716 or 2732, is the power input on the 2764, 27128, and 17256 whereas pin 26 (third from top right) is actually pin 24 on a 2716 or 2732 which it is their power input.

UNIVERSAL SITES ARE BOTTOM JUSTIFIED- When a memory device having fewer pins than the socket, it must be bottom justified, i.e., pin 1 of the EPROM is placed in pin 3 of the socket.

Each of the three memory sockets M1, M2, and M3 are JEDEC 28-pin universal sockets, and each has three configuration jumpers associated with that socket to configure the socket as required for the desired device. For clarity, these jumpers are referred to by the pin number of the socket which they are attached. For example M1.27 is controlled by JP2 which selects one of A14, +5V, or WR*. The same signal on M2 is JP6 and on M3 is JP13.

M1, M2, M3 Jumper Settings

Pin	M1	M2	M3	2732	2764	27128	27256	27512	6264	28C256	62256
Pin 1	JP3	JP9	JP7	Open	1-2	1-2	1-2	---	Open	A14	A14
Pin 26	JP1	JP5	JP10	2-3	Open	1-2	1-2	---	2-3		
Pin 27	JP2	JP6	JP13	Open	2-3	2-3	1-2	2-3	2-4		

Pin 1, Power or No Connection

JP3, JP9, and JP7 are installed to connect pin 1 of M1, M2, or M3 respectively to +5V and left open to allow M1, M2, or M3 pin 1 to float. For the 2732 and 6264 this jumper is removed. For 2764s thru 27256 the jumper is installed. On M3 this jumper also allows provides a connection to A15 (JP7.2 – JP7.3) when a 27512 is installed.

Pin 26 Power or A13

JP1, JP5, and JP10 are installed in position 2-3 to connect pin 26 to +5V, i.e., to connect pin 24 of the 2732 to power. When using 2764s, pin 26 is unused and the jumper is removed entirely. When using 27128s or a 27257 the jumper is installed between 1-2 to connect address line A13. When using 6264 RAMs, the jumper is installed in position 2-3 to enable CE2

Pin 27 +5V, WR*, or A14

JP2, JP6, and JP13 are 1-of-3 jumpers used to determine control of pin 27. Since pin 27 is not connected in a 2732, the actual position of JP6 is not applicable for a 2732. For a 2764 and 27128 pin 27 is the Program* pin which must be taken high for normal reads so JP6 is installed 2-3 to connect pins 27 to +5V. When using 27256 in M1, M2 or M3, pin 27 must be controlled by Address line A14 to internally decode the EPROM, so the jumper is installed in position

1-2. For RAMs, pin 27 must be controlled by the system Write signal WR* so the jumper is installed between positions 2-3.

STD BUS Interface

A key requirement of the STD Bus is the driving or release of the backplane Address, Data, and control lines depending on which card is controlling the bus for that specific bus cycle. U15, U16, half of U17, and U19 determine the control of the bus and specific control signals. Of these, we will begin by describing the control of the address and data lines.

"Normally" the data transceivers will drive the onboard address and data lines onto the STD backplane as inputs to the other cards in the system. However, when the address is not mapped as on-board, it is presumed to be off-board. During an offboard read, the direction of the data transceivers (U19) for the data bus are reversed, and off board data is driven from the STD backplane onto the STD-85 data bus. The direction of U19 is determined by the RECEIVE_/DRIVE signal into U19.1 such that when this signal is in RECEIVE mode the direction of the transceiver is from bus to onboard (A->B) and when in the DRIVE direction the transceiver is from onboard to bus (A<-B).

This *RECEIVE_/DRIVE* signal is created by the glue logic U10, U11A, U11B, and U3A. During any bus access where the memory address has been decoded as *on-board* memory, one of the four memory enables /M1_CE, /M2_CE, /M3_CE, or /8155_CE will be asserted (logic low). These are logically ANDed together (U10A, U10B, U10C) to create an /ONBOARD_CS which will be asserted when the memory access is onboard. This signal is inverted and logically OR'd with the Read (/RD) signal to create an /OFFBOARD_READ signal which is asserted (low) when the memory being read is off-board. For most bus states, this is simply inverted to create the *RECEIVE_/DRIVE* signal described in the last paragraph that then drives STD bus data onto this board.

The net result is that address and data are driven onto the STD bus under all bus cycles except when it is an offboard address and then the offboard device is expected to drive data onto the STD data bus where the data transceiver U19 will drive the data onboard to the 8085. However, there are the Interrupt Request and Bus Request (HOLD) exceptions described in the following paragraphs.

Interrupt Request Cycle

When the INTR input to the 8085 is asserted, this is an indication that another device needs to jamb an instruction onto the data bus. When the 8085 receives this interrupt request (INTR) and ready for the next opcode, the 8085 will assert the interrupt acknowledge (/INTA) signal. The output of U10D will go low just as if it were an off-board read and the data transceiver U19 will be flipped to drive data from the STD Bus onto the onboard data bus. In this manner, an external interrupt controller can redirect the 8085 by feeding the 8085 a RST or a CALL instruction during the first machine state of an opcode fetch. If the instruction is a CALL, the 8085 will subsequently assert the /INTA signal to retrieve the call address from the data bus.

Bus Request Cycle

Another dedicated input to the 8085 is the HOLD signal which is asserted by another device to request full control of the bus and associated control signals. After the 8085 has determined this request has been asserted, it will perform some housekeeping duties and then assert the hold acknowledge (HLDA) signal to indicate it is ready to relinquish the bus control to the requesting device. The 8085 HLDA (U8.38) is inverted by U17.11 to create the bus Hold Acknowledge (/bHLDA) signal which is again inverted to create the buffered Hold Acknowledge signal (bufHLDA). This signal (bufHLDA) directly enables the outputs of the bus drivers U15, U16, and U19 for the low address, high address, and data. When bufHLDA is asserted (logic high) the output of these three transceivers becomes high-impedance to allow another device to fully control these signals. The "a" halves of U17 and U18 are also tri-stated, so the off-board device can also drive the control signals /bALE, /bIORQ, /bS0, /bS1, /bINTA, /bMEMRQ, /bRD, and /bWR.

Per the STD Bus recommended practices, all signal lines are pulled to +5V through a 4.7K resistor (RN1, RN2, RN3, RN4).

SERIAL INTERFACE

The utility of any single board computer is severely limited if it does not have a means of communication with a terminal or external device. For this reason, Intel included two serial communication lines in the base 8085, eliminating the need for an additional UART or USART component. These are the Serial Output Data (SOD) and Serial Input Data (SID) lines. Depending on the preferred communication standard, code is used in the 8085 to create or "bit-bang" a serial stream. In the case of the SBC-85, this is RS-232 which is a bipolar serial stream consisting of a starting bit, data bits, stop bit, and parity bit. No other hardware handshaking is used on the SBC-85. To create the bipolar output, a MAX232 (U9) is used which contains an internal charge pump to create the +/- rails necessary to

meet the RS232 standard (+/- 14V typical for the MAX232). The 8085 *SID* and *SOD* lines pass through the MAX232 which inverts and level shifts the signals as required by RS232. With rails in the +/-12V range, the RS232 port on the SBC-85 will eat any TTL device connected to J3. If you want to use a TTL signal on J3, then remove U9 access the *SID* and *SOD* lines directly at the J6 connector. J6 can also be used to access the remaining unused drivers in U9 (cut the traces at TC3 and/or TC4 before using the respective driver).

ONBOARD PORT

The STD-85 includes an 8-bit, write only onboard output port whose output is set to zero upon reset. The address f the port is controlled by switches SW10, SW11, and SW12 with SW10 and SW11 determining the three most significant bits of the port address (A7, A6, A5) and SW12 determining the next lower three bits (A4, A3, A2). The lowest two bits are not decoded so the port is active regardless of these two bits. This means no other port should have the same upper six bits since this on board port actually consumes four addresses (those ending in 00, 01, 10, 11).

The least significant bit of the port data determines which memory map is active. When this bit is at logic zero (0V) the default memory map is used and when the LSBit is at logic one (+5V) the alternate memory map is used. The most significant bit energizes the onboard mini-speaker. The output is inverted and connected to the negative terminal of the speaker, so when this bit is at logic low the speaker is de-energized, when at logic true the speaker is energized. The other output bits of the onboard port control the LEDs with the LED being illuminated when the output is at logic low.

POWER INPUT

The STD-85 operates on +5VDC and is fitted with a 2.1mm x 5.5mm barrel connector with the tip positive. A well regulated +5VDC power supply should be used to power the STD-85 either through the barrel connector or through the expansion bus. Vcc specifications on the 8085 are +5VDC +/- 10%. Depending on how much current is going out the I/O port and onto the bus, the SBC-85 will take about 1A of current. Power provided to the barrel connector is connected directly to the STD Bus power rails, so this connector can also be used to power the STD backplane and, within limits, other boards in the system.

COMPONENTS

JUMPERS AND CONNECTORS

J2 is a 34 position header with the 8155 (U7) I/O pins and J4 onboard wirewrap patch pins to take onboard signals off board.

J3 RS-232 DB9

J5 Provides wirewrap access to /INTR7.5, /INTR6.5, and /INTR5.5 inputs as well as the Timer Out (/TO) from the 8155.

J6 Provides wirewrap access to the 8085 *SID* and *SOD* as well as unused drivers in the MAX232 driver U9

J9 +5VDC power inlet barrel connector. Tip positive

J10 v.1.1+ Provides bits 3, -6 to the ejector edge for offboard use such as memory page swap

JP1 M1 pin 26 configuration

JP2 M1 pin 27 configuration

JP3 M1 pin 1 configuration

JP4 is installed to allow the system CLK signal as the timer input to the 8155 U7.3 or may be wire wrapped from another source.

JP5 M2 pin 26 configuration

JP6 M2 pin 27 configuration

JP7 M3 pin 1 configuration

JP9 M2 pin 1 configuration

JP10 M3 pin 26 configuration

JP13 M3 pin 27 configuration

Test Points

TP2 Ground test point
TP1 +5V bus test point

Diodes / LEDs

D1 Board +5V power indicator
D2 indicates default memory in use
D3 indicates alternate (swap) memory is in use
D4 v1.1+ provides open-collectorish pulldown of /bRST. NOTE DIODE ORIENTATION IS INCORRECT
D5 Freewheeling diode for speaker
B1-B6 indicators for the onboard port (OBP). V1.06 LED opposite bit logic, v1.1+ LED matches bit logic

RESISTORS

R1 current limiting resistor for D1 (~500 ohms adjust for desired LED brightness)
R2 charging resistor for reset RC
R3 discharge resistor for reset switch
R4 current limiting resistor for speaker (600 ohms)
RN1, RN2, RN3, RN4, RN8 bus pull resistors (4.7K)
RN6 current limiting resistors for B1-B6, D2, D3 (~500 ohms, adjust for desired LED brightness)

SWITCHES

SW1 Resets the CPU by taking the *RESET IN** to ground
SW2 Memory Socket M1 default address selection
SW3 Memory Socket M1 alternate address selection
SW6 Memory Socket M2 default address selection
SW7 Memory Socket M2 alternate address selection
SW8 Memory Socket M3 default address selection
SW9 Memory Socket M3 alternate address selection
SW10 1K Block default address selection
SW11 1K Block alternate address selection
SW12 Onboard Port address selection
SW13 Onboard 8155 address selection

UNUSED COMPONENTS

U18 (v1.06) 1b, 2b, 3b; (v1.1) 2b, 3b
RN3 pin 8
RN4 (v1.06) pins 8, 9; (v1.1) pins 4, 5, 9

Trace Cut Points

TC1 ties the STD Bus signal /IOEXP to ground (unasserted)
TC2 ties the STD Bus signal /MEMEX to ground (unasserted)
TC3, TC4 tie the unused inputs of U9 to ground
TC5, TC6 tie the unused inputs of U3C and U3D to +5V
TC8, TC9 tie the unused inputs of U14 to +5V
TC7, TC10, (v1.06) tie the unused inputs of U18 to ground
TC11, TC12 tie the unused inputs of U18 to ground

TC13 ties the “b” output enable to the /RST signal so the /bRST signal is tri-stated during system reset (as recommended in later STD Bus Best Practice Documents)

ASSEMBLY NOTES AND PROCEDURES – Most of these are important (or useful)

- If you receive a board that does not have gold fingers, the sharp finger corner may damage the contacts on the backplane. This can be accomplished using a utility knife followed by filing or sanding (sand paper on a flat surface) to create a 45° chamfer on both edges. **If you insert the sharp edge into the PCI connectors on the backplane, it WILL damage the connector.** [Video](#)

- For most footprints on the PCB, pin 1 is identified as the square pad.
- When buying components, this is my general advice—in almost all cases I design for the 74LS family. If you can find components in the 74LS, great. If not, try the 74ALS family, 74F, or 74HCT which are all TTL compatible with the 74LS. (Note that the 74HC is NOT TTL).
- Tantalum capacitors in KiCAD have pin 1 of the footprint as the positive terminal, however footprints for LEDs are the opposite and have pin 2 as positive. For both LEDs and the polarized capacitors, if one lead is longer than the other that is the positive lead (anode on LEDs).
- If using wire wrap headers for the memory selection array, somehow make the common pin different, e.g., longer, gold plated, etc., to help differentiate when that selection header ends and the next begins.

MODIFICATIONS to UPDATE REVISIONS

DIAGNOSTIC NOTES

Hot or Dead MAX232-

- Check the charge pump capacitors are correctly installed (polarized)

REVISIONS

v1.0 First produced board week 1022

v1.1 First produced board week 3222

- Added inverters to onboard port LEDs so on/off LED illumination matches true/false bit logic
- Changed nomenclature on address map from default/swap to default/alternate.
- Flipped offboard headers to match general order of SBC-85 and MCS-85 boards
- Bring portion of onboard port I/O to ejector edge of board for memory segment control
- Changed RN6 value (LEDs) to 470 ohm
- Change pseudo tristate bRST* to diode pull down with D4 but managed to put D4 in backwards
- Drive control through U18 bMEMEX and bIOEXP from onboard port

Future Change Requests

- Correct orientation of D4
- Narrow finger tab to 91.7mm
- Larger chamfer on finger tab outside corners
- Correct crystal frequency on schematic to 6.144 MHz

COMPONENT PLACEMENT – SCHEMATICs -- BOM

Component placement, schematics, and the bill of materials are on the following pages in **reverse** chronological order. Higher resolution PDF schematics are available on the BitsOfTheGoldenAge.org project website.

Note that in the schematics, M1, M2, and M3 are ‘universal sites’ and the actual memory used is bottom justified if the chip has fewer pins than the socket. This means for a 2732, for example, 2732 pin 1 is in pin 3 of the socket, 2732 pin 24 is in pin 26 of the socket. Each pin on the IC is two pins higher when looking at the schematic. The graphic in an earlier section titled *Universal EPROM Sockets* may be a useful reference.

V1.1

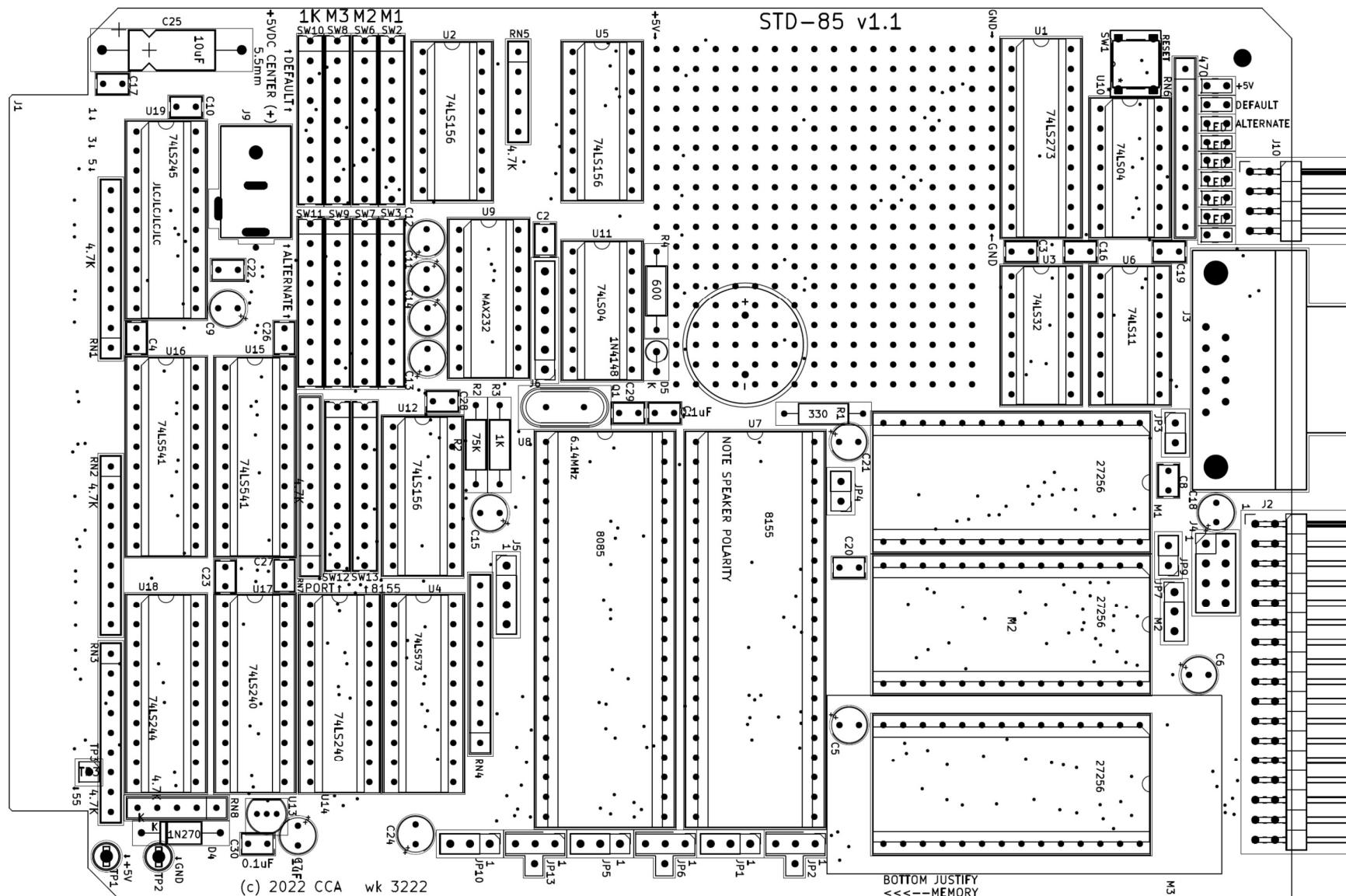
STD-85 8085 CPU v1.1 BOM

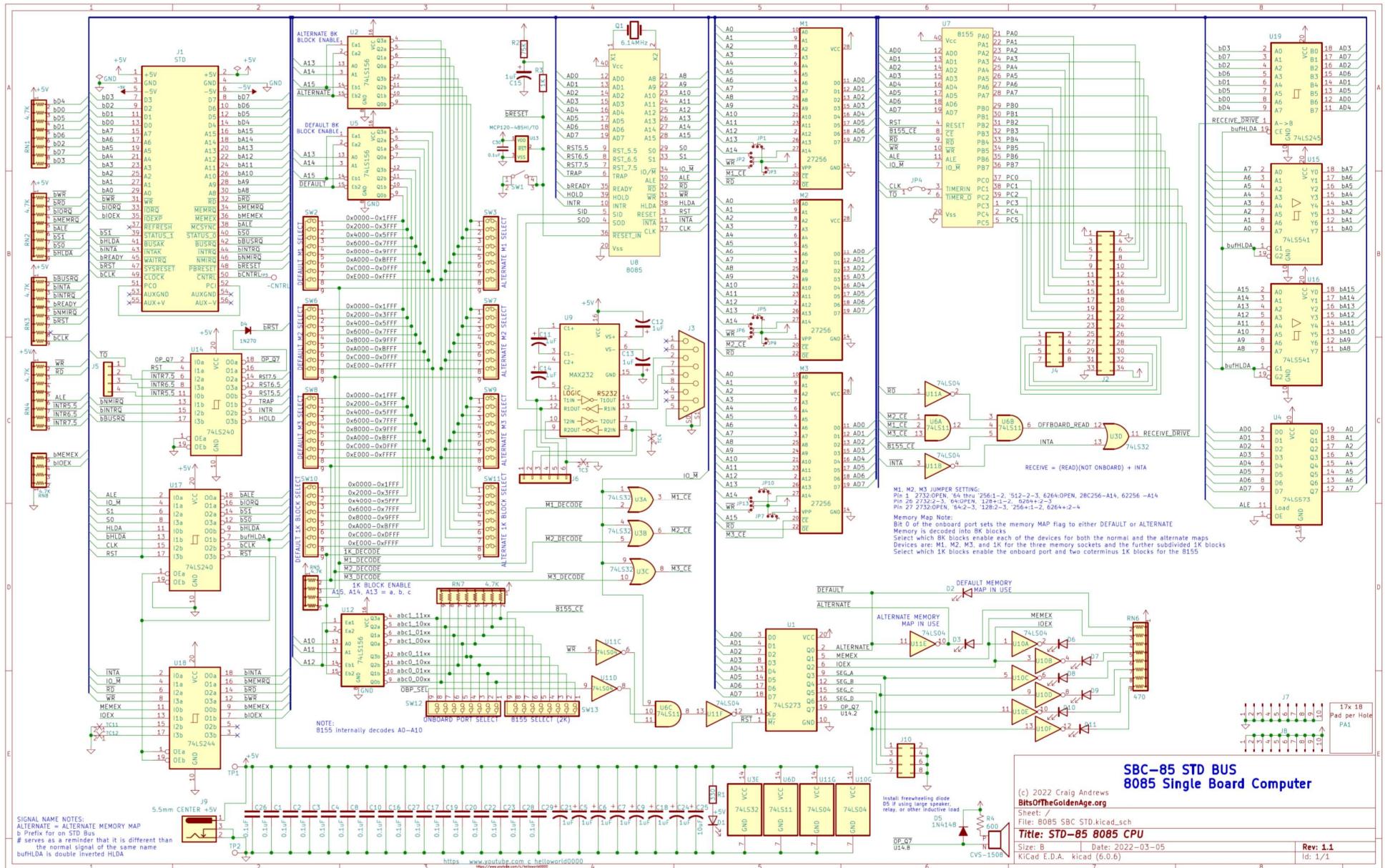
QTY	Name	Value Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
16	C1, C2, C3, C4, C8, C10, C16, C17, C19, C20, C22, C23, C26, C27, C28, C29	100nF CAP CER 0.1UF 50V Z5U RADIAL KEMET	kemet	C315C104M5U5TA	399-4151-ND
13	C5, C6, C7, C9, C11, C12, C13, C14, C15, C18, C24, C25, C21	1μF Conformal Coated Tantalum Capacitors 35V Radial 8Ohm	avx	TAP105M035SCS	478-5812-ND
6	B1, B2, B3, B4, B5, B6,	LED		SSL-LX2573AD	67-1045-ND
3	D1, D2, D3	LED			
1	D4	IN270 (germanium or other low Vf diode)			
1	D5*	1N4148			
4	J1, JP5, JP7, JP10	CONN HEADER VERT 3POS 2.54MM	Sullins connector Solution	PREC003SAAN-RC	S1012EC-03-ND
3	JP2, JP6, JP13	CONN HEADER VERT 4 POSITION (1 OF 3 T)			
3	JP3, JP4, JP9	CONN HEADER VERT 2 POSITION 2.54MM			
1	J1	STC-85 CPU v1.0 CARD	BitsOfTheGoldenAge.ORG		
1	J2	CONN HEADER VERT or R/A 34 POS 2.54MM	Sullins connector Solution		
1	J3	9 Position D-Sub Receptacle R/A, Female Sockets Connector	Amphenol ICC	D09S13A4GX00LF	609-1484-ND
2	J4*,J10*	CONN HEADER VERT 8POS 2.54MM	Sullins connector Solution		
1	J5*	CONN HEADER VERT 4POS 2.54MM	Sullins connector Solution		
1	J6*	CONN HEADER VERT 6POS 2.54MM			
1	J9*	Power Barrel Connector Jack 2.10mm ID (0.083"), 5.50mm OD (0.217") Through Hole, Right Angle	CUI	PJ-050AH	CP-050AH-ND
	J10				
1	TP2*	PC TEST POINT .065 HOLE COMPACT BLACK	keystone electronics	5006	36-5006-ND
1	TP1*	PC TEST POINT .065 COMPACT RED	keystone electronics	5005	36-5005-ND
1	Q1	6.144MHz Crystal HC49/US	CTS frequency controls	ATS061B	CTX899-ND
1	R1	RES 330 OHM 1/4W 5% AXIAL	stackpole	CF14JT330R	CF14JT330RCT-ND
1	R2	RES 75K OHM 1/4W 5% AXIAL	stackpole	CF14JT75K0	CF14JT75K0CT-ND
1	R3	RES 1K OHM 1/4W 5% AXIAL	stackpole	CF14JT1K00	CF14JT1K00CT-ND
1	R4	RES 600 OHM 1/4W 5% AXIAL	stackpole	CF14JT600R	CF14JT600RCT-ND
5	RN1, RN2, RN3, RN4, RN7	8 x 4.7K resistor network, SIP common rail	4609X-101-472LF	Bourns Inc.	4609X-101-472LF-ND
2	RN5, RN8	4 x 4.7K resistor network, SIP common rail	4605X-101-472LF	Bourns Inc.	4605X-101-472LF-ND

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QTY	Name	Value	Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
1	RN6		8 x 470 ohm resistor network, SIP common rail	4609X-101-471LF	Bourns Inc.	4609X-101-471LF-ND
1	SW1		Tactile Switch SPST-NO Top Actuated Through Hole 0.1A 32V	TE Connectivity	1825910-7	450-1804-ND
10	SW2, SW3, SW6, SW7, SW8, SW9, SW10, SW11, SW12, SW13		8 position SIP switch (9 pin) (OR 9-pin wire wrap header, OR solder jumpers)	STV08	TE Connectivity ALCOSWITCH Switches	450-1640-ND
1	U1	74LS273				
3	U2, U5, U12	74LS156				
1	U3	74LS32		Texas Instruments	SN74LS32N	296-1658-5-ND
1	U4	74LS573		Texas Instruments	SN74HCT573N	296-1621-5-ND
1	U6	74LS11				
1	U7	8155				
1	U8	8085				
1	U9		IC TRANSCEIVER FULL 2/2 16DIP MAX232	Texas Instruments	MAX232N	296-1402-5-ND
2	U10, U11	SN74LS04		Texas Instruments	SN74LS04N	296-1629-5-ND
1	U13*		Supervisory Circuit MCP120-485HI/TO	Microchip Technology	MCP120-485HI/TO	MCP120-485HI/TO-ND
2	U14, U17	74LS240				
2	U15, U16	74LS541				
1	U18	74LS244				
1	U19	74LS245				
2	M1, M2	2732-27256, 6264-62256				
1	M3	2732-27512, 6264-62512				
1	SPKR*	CVS-1508		CUI Devices	CVS-1508	102-2498-ND
3	U3, U6, U11	14-pin DIP Socket				
3	U2, U5, U12	16-pin DIP Socket				
8	U1, U4, U14, U15, U16, U17, U18, U19	20-pin DIP Socket 0.3"				
2	M1, M2	28-pin DIP Socket				
1	M3*	28-pin ZIF DIP socket				
2	U7, U8	40-pin DIP Socket				
7		CONN JUMPER SHORTING .100"			QPC02SXGN-RC	S9337-ND
1	AC/DC DESKTOP ADAPTER 5V 20W*	Power Supply 2.1mm x 5.5mm 5V 20W TIP Positive		Phihong USA	PSAC30U-050L6	993-1343-ND
*	Optional Component					

V1.1 Component Placement





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Nov. 27, 22

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V1.06

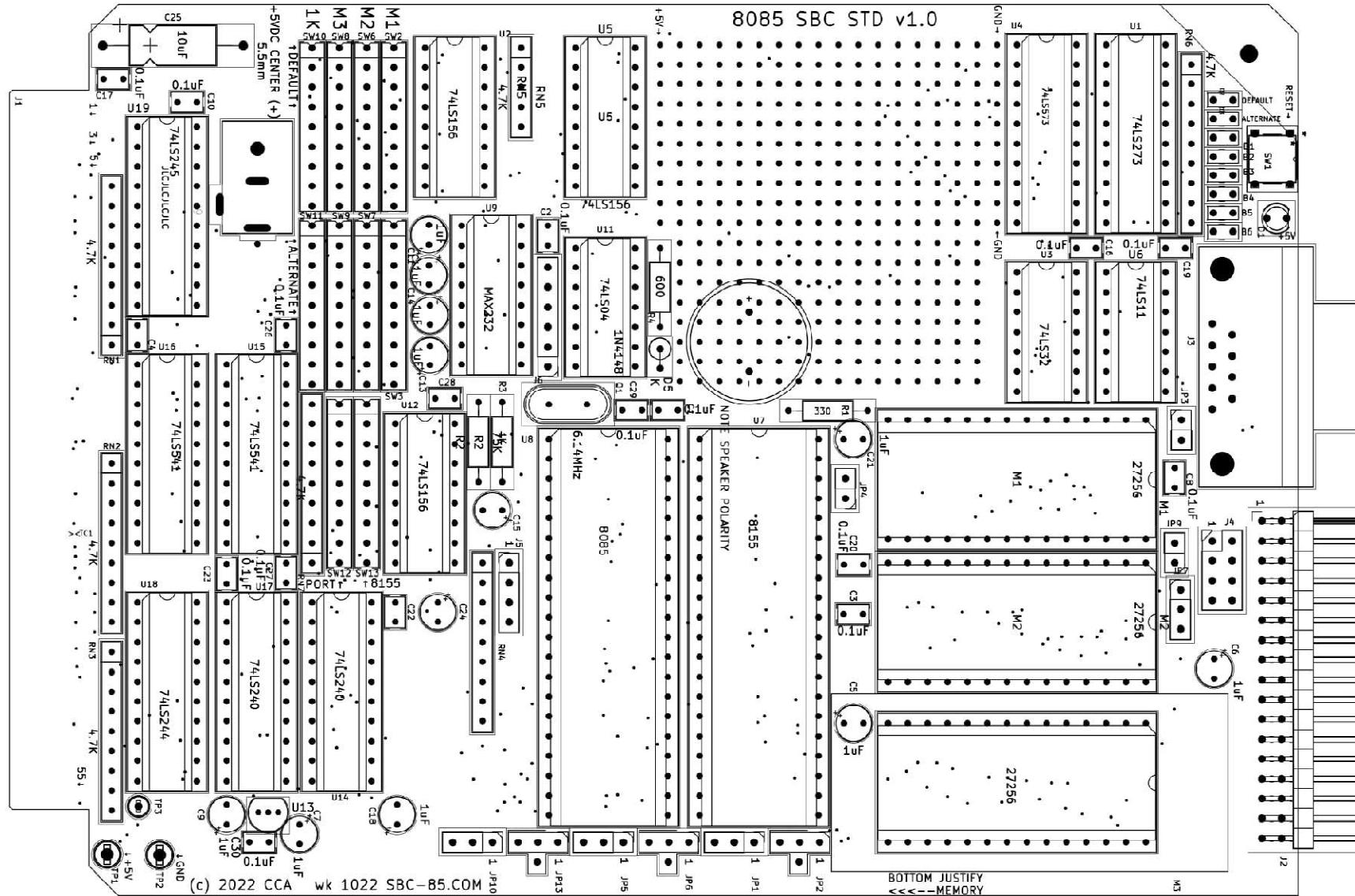
STD-85 8085 CPU v1.06 BOM

QTY	Name	Value Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
16	C1, C2, C3, C4, C8, C10, C16, C17, C19, C20, C22, C23, C26, C27, C28, C29	100nF CAP CER 0.1UF 50V Z5U RADIAL KEMET	kemet	C315C104M5U5TA	399-4151-ND
13	C5, C6, C7, C9, C11, C12, C13, C14, C15, C18, C24, C25, C21	1μF Conformal Coated Tantalum Capacitors 35V Radial 8Ohm	avx	TAP105M035SCS	478-5812-ND
6	B1, B2, B3, B4, B5, B6,	LED		SSL-LX2573AD	67-1045-ND
3	D1, D2, D3	LED			
1	D5*	1N4148			
4	J1, JP5, JP7, JP10	CONN HEADER VERT 3POS 2.54MM	Sullins connector Solution	PREC003SAAN-RC	S1012EC-03-ND
3	JP2, JP6, JP13	CONN HEADER VERT 4 POSITION (1 OF 3 T)			
3	JP3, JP4, JP9	CONN HEADER VERT 2 POSITION 2.54MM			
1	J1	STC-85 CPU v1.0 CARD	BitsOfTheGoldenAge.ORG		
1	J2	CONN HEADER VERT or R/A 34 POS 2.54MM	Sullins connector Solution		
1	J3	9 Position D-Sub Receptacle R/A, Female Sockets Connector	Amphenol ICC	D09S13A4GX00LF	609-1484-ND
1	J4*	CONN HEADER VERT 8POS 2.54MM	Sullins connector Solution		
1	J5*	CONN HEADER VERT 4POS 2.54MM	Sullins connector Solution		
1	J6*	CONN HEADER VERT 6POS 2.54MM			
1	J9*	Power Barrel Connector Jack 2.10mm ID (0.083"), 5.50mm OD (0.217") Through Hole, Right Angle	CUI	PJ-050AH	CP-050AH-ND
1	TP2*	PC TEST POINT .065 HOLE COMPACT BLACK	keystone electronics	5006	36-5006-ND
1	TP1*	PC TEST POINT .065 COMPACT RED	keystone electronics	5005	36-5005-ND
1	Q1	6.144MHz Crystal HC49/US	CTS frequency controls	ATS061B	CTX899-ND
1	R1	RES 330 OHM 1/4W 5% AXIAL	stackpole	CF14JT330R	CF14JT330RCT-ND
1	R2	RES 75K OHM 1/4W 5% AXIAL	stackpole	CF14JT75K0	CF14JT75K0CT-ND
1	R3	RES 1K OHM 1/4W 5% AXIAL	stackpole	CF14JT1K00	CF14JT1K00CT-ND
1	R4	RES 600 OHM 1/4W 5% AXIAL	stackpole	CF14JT600R	CF14JT600RCT-ND
5	RN1, RN2, RN3, RN4, RN7	8 x 4.7K resistor network, SIP common rail	4609X-101-472LF	Bourns Inc.	4609X-101-472LF-ND
1	RN5	4 x 4.7K resistor network, SIP common rail	4605X-101-472LF	Bourns Inc.	4605X-101-472LF-ND
1	RN6	8 x 470 ohm resistor network, SIP common rail	4609X-101-471LF	Bourns Inc.	4609X-101-471LF-ND
1	SW1	Tactile Switch SPST-NO Top Actuated Through Hole 0.1A 32V	TE Connectivity	1825910-7	450-1804-ND

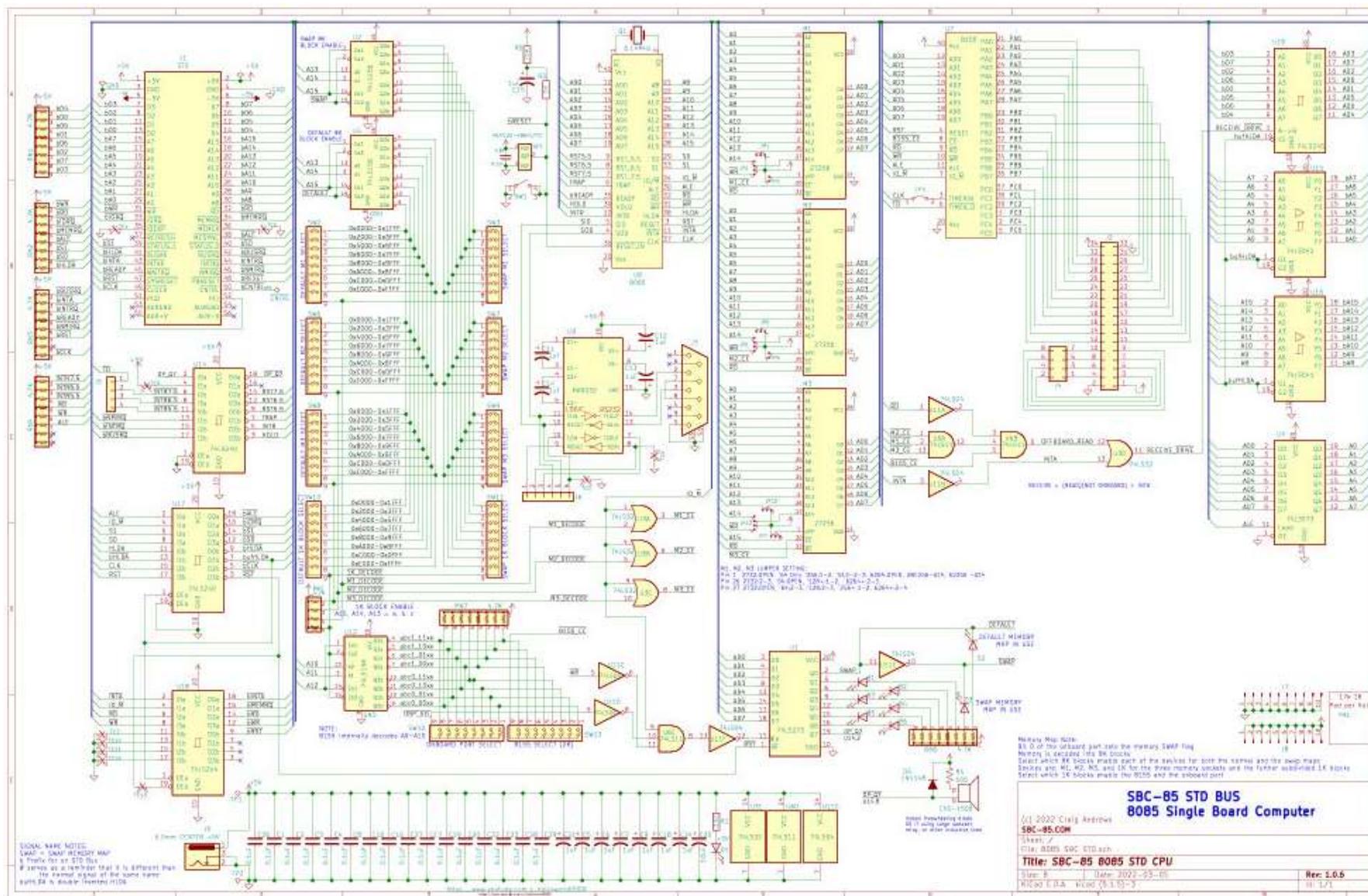
STD-85 8085 CPU v1.06 BOM

QTY	Name	Value	Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
10	SW2, SW3, SW6, SW7, SW8, SW9, SW10, SW11, SW12, SW13		8 position SIP switch (9 pin) (OR 9-pin wire wrap header, OR solder jumpers)	STV08	TE Connectivity ALCOSWITCH Switches	450-1640-ND
1	U1		74LS273			
3	U2, U5, U12		74LS156			
1	U3		74LS32	Texas Instruments	SN74LS32N	296-1658-5-ND
1	U4		74LS573	Texas Instruments	SN74HCT573N	296-1621-5-ND
1	U6		74LS11			
1	U7		8155			
1	U8		8085			
1	U9		IC TRANSCEIVER FULL 2/2 16DIP MAX232	Texas Instruments	MAX232N	296-1402-5-ND
1	U11		SN74LS04	Texas Instruments	SN74LS04N	296-1629-5-ND
1	U13*		Supervisory Circuit MCP120-485HI/TO	Microchip Technology	MCP120-485HI/TO	MCP120-485HI/TO-ND
2	U14, U17		74LS240			
2	U15, U16		74LS541			
1	U18		74LS244			
1	U19		74LS245			
2	M1, M2		2732-27256, 6264-62256			
1	M3		2732-27512, 6264-62512			
1	SPKR*		CVS-1508	CUI Devices	CVS-1508	102-2498-ND
3	U3, U6, U11		14-pin DIP Socket			
3	U2, U5, U12		16-pin DIP Socket			
8	U1, U4, U14, U15, U16, U17, U18, U19		20-pin DIP Socket 0.3"			
2	M1, M2		28-pin DIP Socket			
1	M3*		28-pin ZIF DIP socket			
2	U7, U8		40-pin DIP Socket			
7			CONN JUMPER SHORTING .100"		QPC02SXGN-RC	S9337-ND
1	AC/DC DESKTOP ADAPTER 5V 20W*		Power Supply 2.1mm x 5.5mm 5V 20W TIP Positive	Phihong USA	PSAC30U-050L6	993-1343-ND
*	Optional Component					

V1.06 Component Placement



V1.06 schematic



Definitions of Terms and Notation

0xF

Hex Interpretation of 4 binary bits (nibble), in this example HEX F which is 1111 in binary

0xFF

Hex Interpretation of 8 binary bits (byte), in this example HEX FF which is 1111 1111 in binary

0xFFFF

Hex Interpretation of 16 binary bits or Word (two bytes). In this example HEX FFFF is the interpretation of the binary value 1111 1111 1111 1111

Address Decoding

The process (decoding) or part of the circuit (decoder) that determines which addresses are assigned to which memory or I/O device and, typically, results in the enabling of one specific memory or I/O device on the board or system.

An

Individual Address Line where n is 0-15

ADn

Individual Multiplexed Address / Data line where n is 0-8

BOM

Bill of Materials

Buffer (also driver)

A device that ‘re-drives’ or buffers a signal to unload (or separate from) the original signal. One direction (see also transceiver)

Byte

8-bits

Component Side

The ‘top’ of the PC board where the components are mounted. On the SBC-85 this is the side with the bulk of the silkscreen and the component numbers and footprints.

Contention (e.g., bus contention or signal contention)

A condition where two or more devices are simultaneously attempting to drive the same signal or bus. Technically, I suppose ‘contention’ only occurs when they disagree as to what the status of the signal or bus should be, e.g., one is pulling high while the other is pulling low but neither is enjoying the situation.

CS/ or CS*

Chip Select (reverse, a.k.a., negative logic) where a logic LOW (0v) is active

Decoding (Memory or I/O)

The process of determining which specific device should be enabled given any memory or I/O address.

EPROM

Erasable Programmable, Read Only Memory. A non-volatile memory device that can repeatedly be erased (generally by exposing to a UV light source) and field programmed. Compare to ROM, PROM, and EEPROM

EEPROM

Electrically Erasable Programmable, Read Only Memory. A non-volatile memory device that can repeatedly be erased and programmed, typically in-circuit. Compare to ROM, PROM, and EPROM

JEDEC Socket

Joint Electron Device Engineering Council standardized memory socket that can be configured to accept any JEDEC compliant memory chip within the design range of the socket.

I/O

Input / Output

I/O Mapped I/O

An address decoding scheme where the I/O ports are mapped using the address lines AND requiring that the *IO/M* signal be at logic LOW*. In this configuration, a port instruction such as OUT 23H would write only to the I/O port that decodes to address 23H. The instruction LDA 2323H will only read from the memory location at 2323H. See also *Memory Mapped I/O*.

LSB

Least Significant Byte. On a multibyte word this is the byte with the least weight, i.e., the furthest towards the right. E.g., the '34' in the word 0x1234

LSBit

Least Significant Bit. The bit with the least weight, i.e., the furthest towards the right. E.g., in the byte 11111110 the least significant bit is the '0'

Memory Mapped I/O

An address decoding scheme where the I/O ports are intermixed and use the same addresses as memory and the *IO/M* signal is not used*. In this configuration, there is no differentiation between memory and I/O. As an example, a port instruction such as OUT 23H will write not only to the I/O port that decodes to address 23H but it would write to the memory location at 2323H. Likewise, the instruction LDA 2323H will read the contents of Port 23H. The advantage of memory mapped I/O is that any memory instructions can be used to access I/O ports. The disadvantage is that I/O port addresses must be set to not overlap with any memory locations. See also *I/O Mapped I/O*.

MSB

Most Significant Byte. On a multibyte word this is the byte with the highest weight, i.e., the furthest towards the left. E.g., the 'AB' in the word 0A12. Be careful not to confuse a leading zero as the MSB such as in the byte 0A3H where the leading zero is required for many assemblers

MSBit

Most Significant Bit. The bit with the most weight, i.e., the furthest towards the left. E.g., in the byte 10000000 the most significant bit is the '1'.

Nibble

4-bits, half a byte.

OBP

On Board Port.

On

Logic TRUE or active. May be HIGH (+5V) or LOW (0V)

Off

Logic FALSE or inactive. May be HIGH (+5V) or LOW (0V)

o.c. (Open Collector or Open Drain)

A form of device output where the driving device can only pull the logic level low (e.g., to 0V in TTL). Since no output can drive the circuit, multiple open collector outputs can be tied together. Typically a pull-up resistor takes the circuit to logic one (+5V) if none of the open collector outputs are actively pulling the circuit low.

PROM

Programmable Read Only Memory. A non-volatile memory device that can be field programmed, and is typically One Time Programmable (OTP). Compare to ROM, EPROM, and EEPROM

ROM

Read Only Memory. A non-volatile memory device that is (typically) factory masked to create its internal bit pattern. Compare to PROM, EPROM, and EEPROM

Sandbox

An expansion or prototype area for free-range creators to play and express themselves.

SBC

Single Board Computer, i.e., a system which contains the processor and any memory (RAM & ROM) required to fully operate.

STD Bus

Standard Bus. A backplane based bus created by Pro-Log and Mostek, primarily for process control.

SW_n

Switch where n is the switch identifier

SID

Serial Input Data (8085 pin 5)

SOD

Serial Output Data (8085 pin 4)

Solder Side

The 'bottom' of the PC board

Transceiver

A bi-directional buffer, i.e., a device that 're-drives' or buffers a signal to unload (or separate from) the original signal. The transceiver can either drive the signal from A to B or from B to A depending upon the state of the direction input (usually labelled something obvious like *DIR* or *A->B*). See also *buffer*.

Tri-State (or 3-state)

A form of device output where the output can be released into the high-impedance state where it is not driven high or low by the output device. When an output is in the tri-state mode, that device output is no longer controlling the output circuit which then allows another device to control the circuit.

Un

Integrated Circuit ID n. *Un.m* would be pin m on IC n.

UART

Universal Asynchronous Receiver Transmitter. A serial port controller that autonomously handles asynchronous serial communication e.g., RS232

Universal Site

A term used to reference a socket (usually memory) that can be used with multiple devices.

USART

Universal Synchronous Asynchronous Receiver Transmitter. A serial port controller that autonomously handles either synchronous or asynchronous serial communication e.g., RS232.