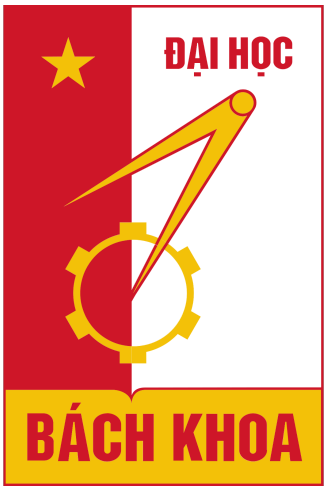
HANOI UNIVERSITY OF SCIENCE AND TECHNOLOGY
SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING



DESIGN SPECIFICATION

LAB5

Simulation of simple connection between 2 UARTs

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Ha Noi, June 2023

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1 UART

1.1 Top Module

Figure 1 depicts the top module of an simple UART interface.

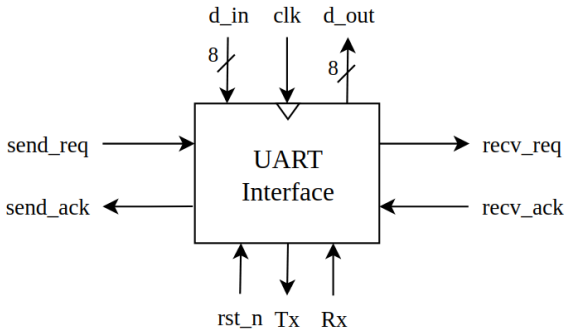

Figure 1: UART top module

1.2 Port Description

Table 1 shows port description of UART interface.

Signal	Width	I/O	Description
clk	1	Input	Built-in 50MHz clock
rst_n	1	Input	Global reset signal active low
d_in	8	Input	Parallel input from CPU to UART
d_out	8	Output	Parallel output from UART to CPU
Tx	1	Output	Serial data that UART sends
Rx	1	Input	Serial data that UART receives
send_req	1	Input	Signal from CPU to start sending data
send_ack	1	Output	Signal from UART to indicate that data are sent
recv_req	1	Output	Signal is sent by UART to request receive data
recv_ack	1	Input	Signal from UART to indicate that all data are received

Table 1: Port description of UART interface

1.3 Functional Descriptions

1. Tx

- In IDLE state, **send_req** and **Tx** is always 1 and **send_ack** is always 0.
- When **send_req** is cleared to 0: Load 8-bit input from **d_in** then start transmit data via **Tx**. **send_req** remaining 0 until the end of transmission.
- A frame is including 1 start bit (0), 8 data bits and 1 stop bit (1). Data will be transmitted serial, bit by bit through **Tx** with frequency Tbaud (might not similar with frequency of clock).
- After transmit all 10 bits in a frame, **send_req** will be set to 1 again and a tick will be produced in **send_ack** signal.

2. Rx

- UART will detect the start bit in **Rx** signal and start receiving data through **Rx**, **recv_req** will be clear.
- Notice that we try to get the data in the middle of each symbol width (to improve the accuracy) and shift it into a register.
- After receiving all 10 bits in a frame, **recv_req** will be set to 1 again and UART will eliminate start bit, stop bit to get 8-bit data and send 8-bit data to **d_out** output port

1.4 Flow Chart

Figure 2 depicts the flow chart for both Tx and Rx algorithm.

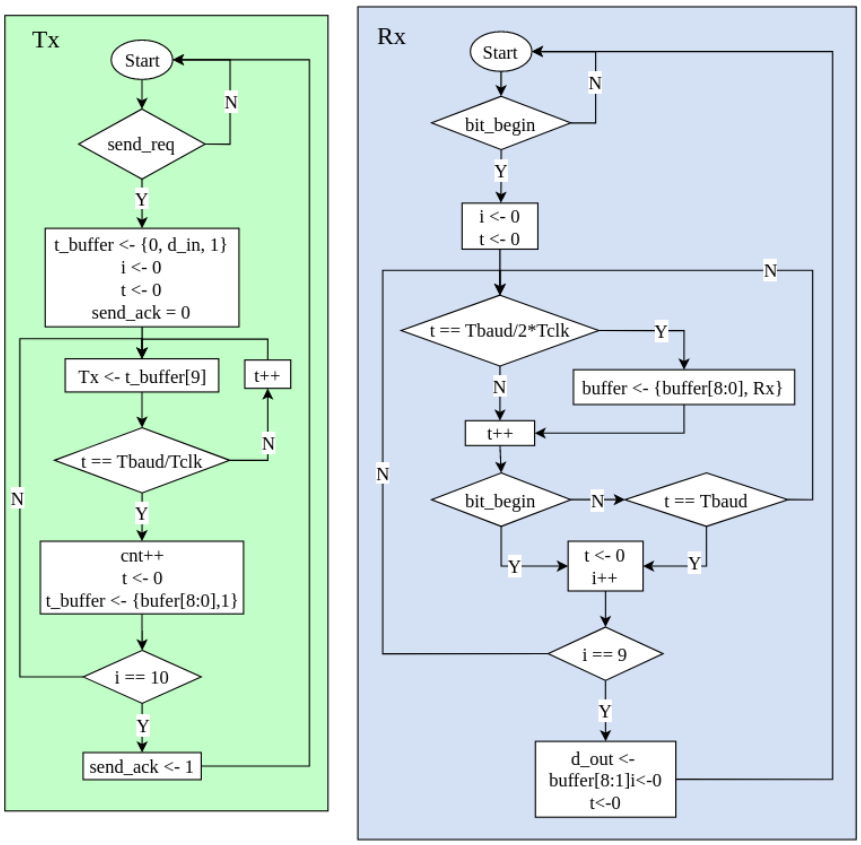

Figure 2: Flow chart of UART Tx and Rx

1.5 FSM and FSMD

Figure 3 and 4 depicts the FSM and FSMD model for both Tx and Rx.

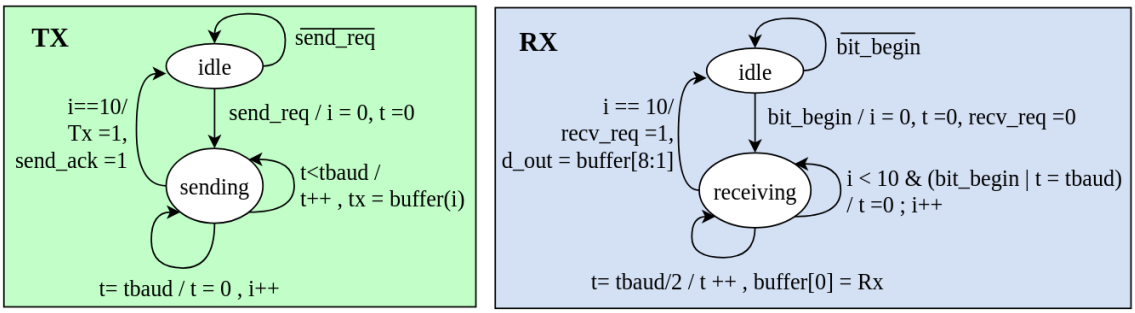

Figure 3: FSM for UART Tx and Rx

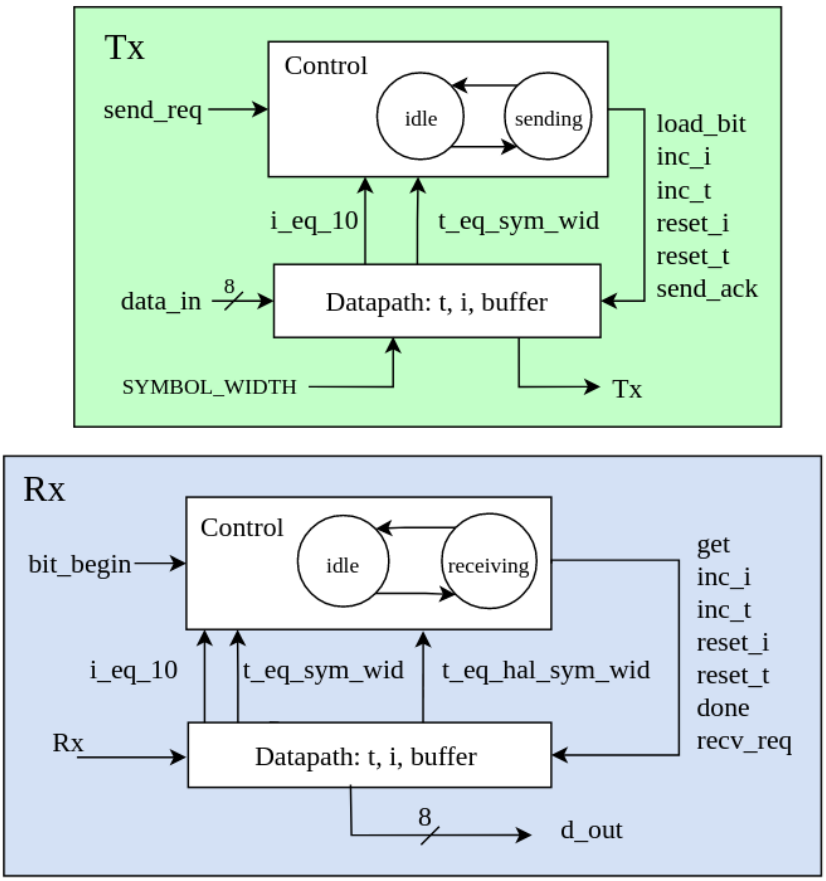

Figure 4: FSMD model for UART Tx and Rx

2 Lab 5

2.1 Overall Connection

Figure 5 depicts lab 5 module's connection. In lab 5, we will using 2 UART, connect them together as the following figure. Then we will simulation the comunication (transmit and receive data) between those 2 UARTs.

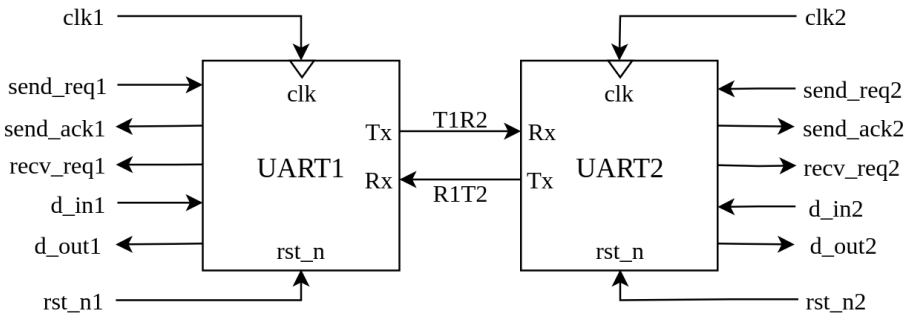

Figure 5: Lab 5 connection

2.2 Timing Diagram

Figure 6 is simulated wave form at some specific time of lab 5 system.

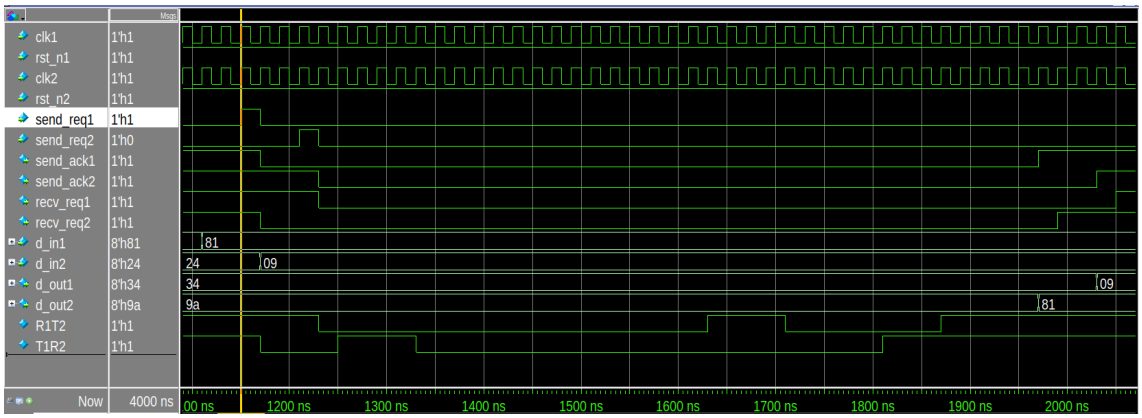

Figure 6: Timing diagram of system simulated in lab 5