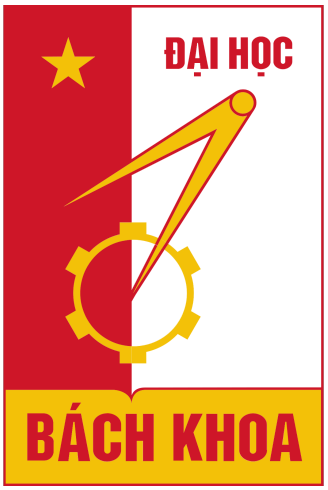
HANOI UNIVERSITY OF SCIENCE AND TECHNOLOGY
SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING



DESIGN SPECIFICATION

LAB3

7-segmant Century Digital Clock

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Ha Noi, May 2023

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1 Top module

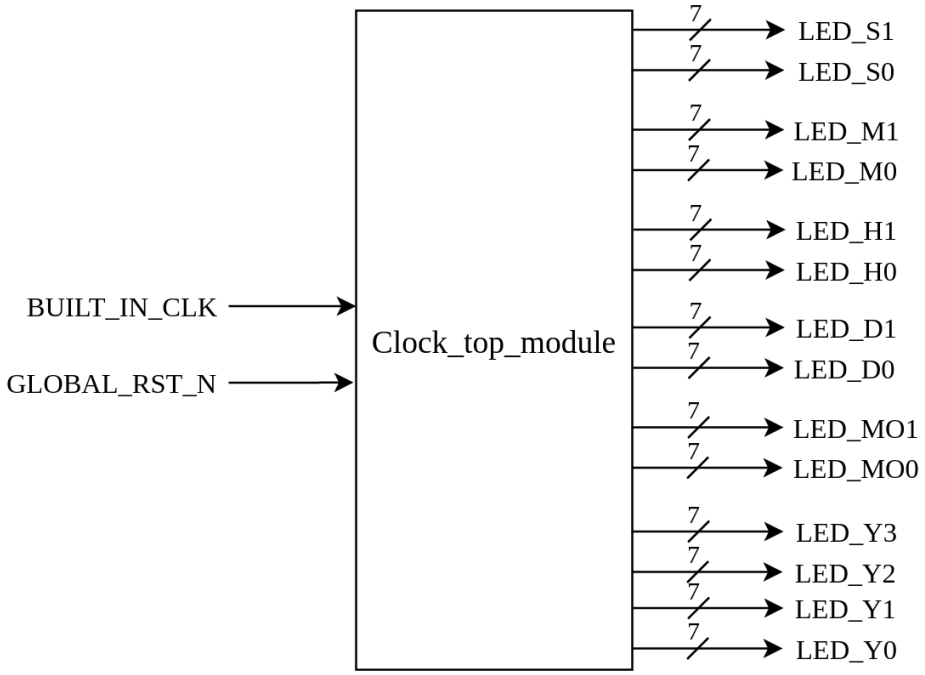

Figure 1: TOP module

I modularized the top module into smaller modules to count and display seconds, minutes, hours, days, months and years seprately. The waveform for those module will be provide in **appendix A**.

2 Port description

Signal name	Width	I/O	Description
BUILT_IN_CLK	1	Input	Built-in clock (50MHz) of DE2-115 FPGA Board
GLOBAL_RST_N	1	Input	Global reset active low (hard reset)
LED_S1	7	Output	Decode tens of seconds
LED_S0	7	Output	Decode units of seconds
LED_M1	7	Output	Decode tens of minutes
LED_M0	7	Output	Decode units of minutes
LED_H1	7	Output	Decode tens of hours
LED_H0	7	Output	Decode units of hours
LED_D1	7	Output	Decode tens of days
LED_D0	7	Output	Decode units of days
LED_MO1	7	Output	Decode tens of months
LED_MO0	7	Output	Decode units of months
LED_Y3	7	Output	Decode thousands of years
LED_Y2	7	Output	Decode hundreds of years
LED_Y1	7	Output	Decode tens of years
LED_Y0	7	Output	Decode units of years

Table 1: Port description of top module

3 Functional Descriptions

- BUILT_IN_CLK is provided to the module, then is divided to 1Hz clock for all module
- When clock starts counting: 2 LED LED_S1 and LED_S0 which display seconds increasing over real-time. When it reaches 10, LED_S0 (represents units of seconds) returns to 0, and LED_S1 light for the tens of seconds increases by 1 unit. When it reaches 6, LED_S1 which represents tens of seconds returns to 0, and the LED_M0 (the units of minutes) increases by 1 unit.
- 2 LED LED_M1 and LED_M0 behave similar with LED_S1 and LED_S0.

- When 2 LED represent hours display 24, they both return to 0, and LED_D0 will increases by 1 unit. When it reaches 10, it returns to 0, and LED_D1 increases by 1 unit. Similarly with 2 LEDs represent months and 4 LEDs represent years

4 Timing Diagram

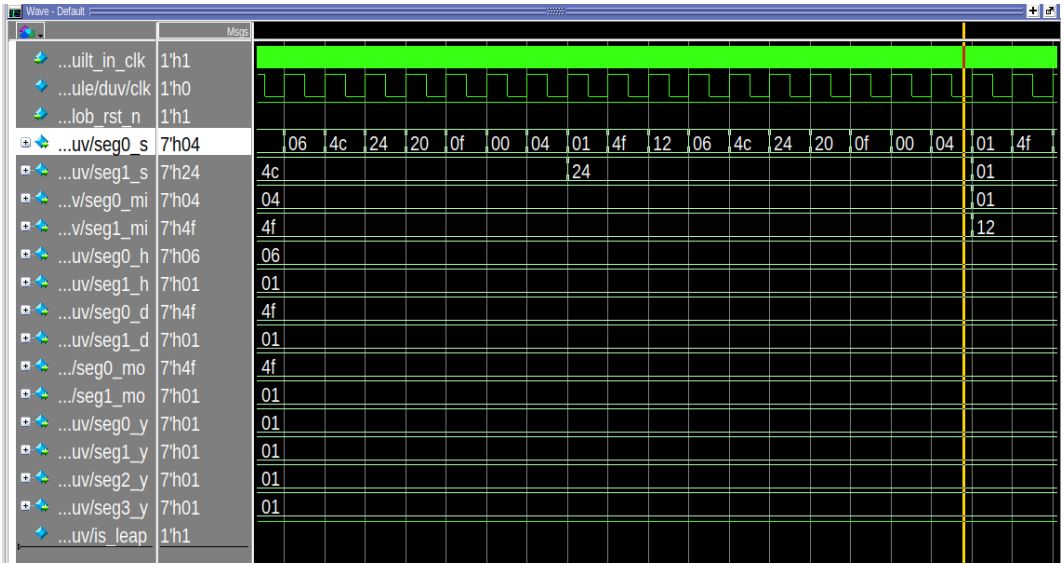

Figure 2: Timing Diagram of top module

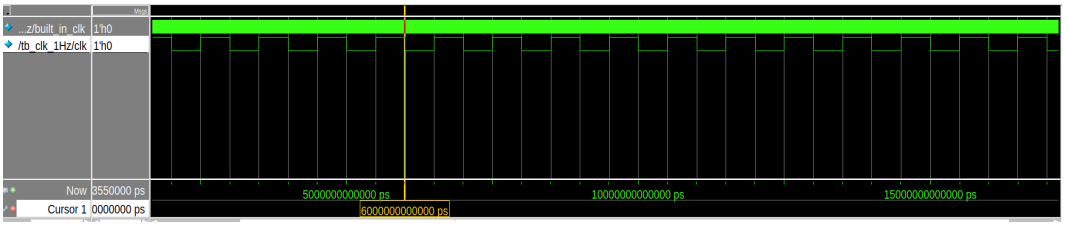

Figure 3: Timing Diagram of clk_1hz (generate 1hz clk from 50MHx clk) module

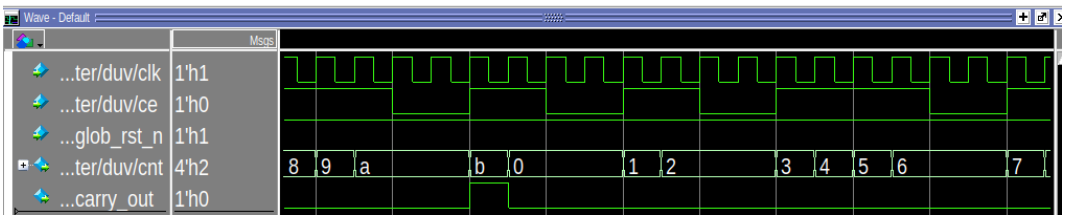

Figure 4: Timing Diagram of counter module

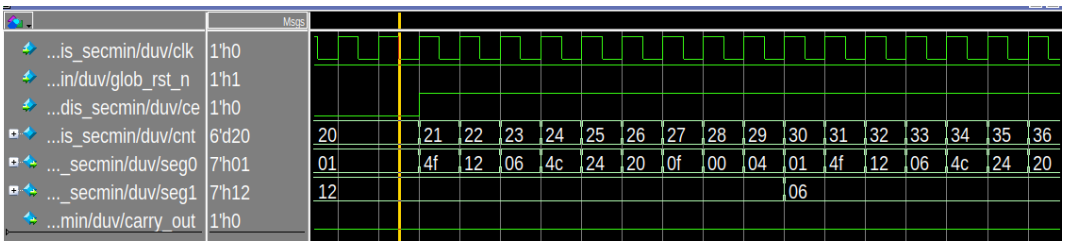

Figure 5: Timing Diagram of count and display seconds/minutes module

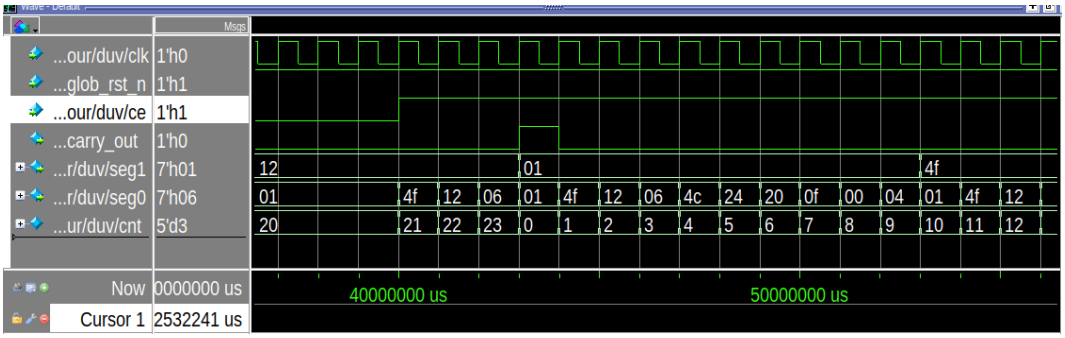

Figure 6: Timing Diagram of count and display hours module

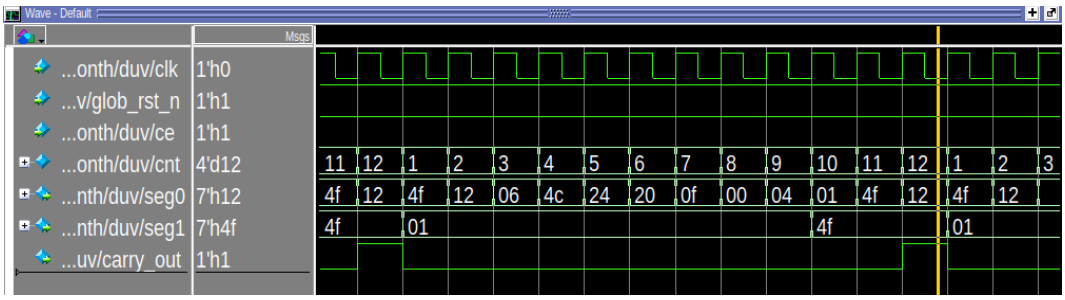

Figure 7: Timing Diagram of count and display months module

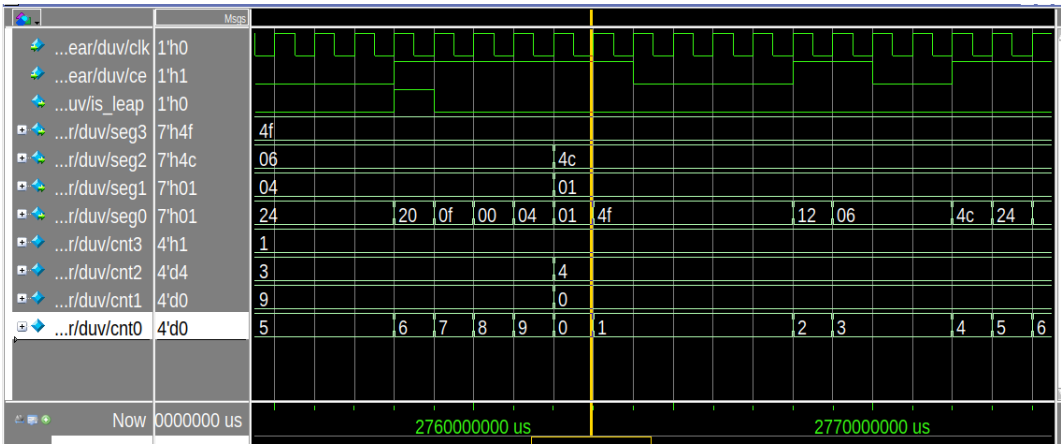

Figure 8: Timing Diagram of count and display years module