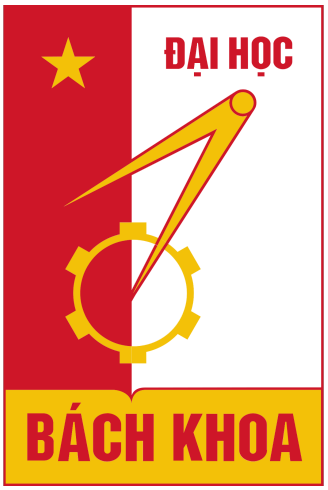
HANOI UNIVERSITY OF SCIENCE AND TECHNOLOGY
SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING



DESIGN SPECIFICATION

LAB4

Traffic Light Highway - Country Control System

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1 Top module

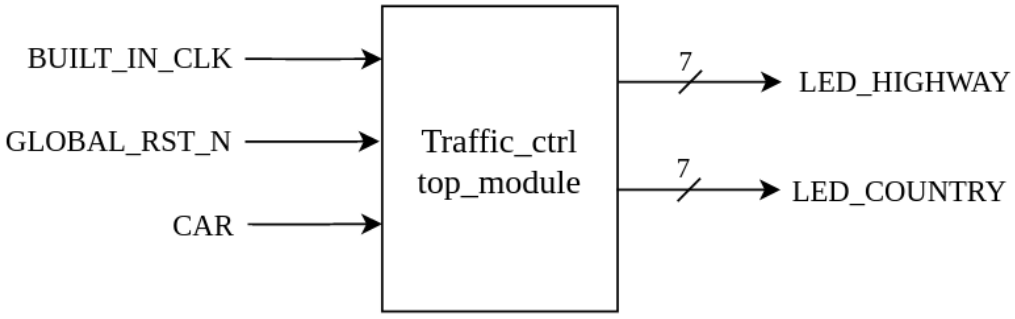

Figure 1: TOP module

I modularized the top module into smaller modules: timer (to count from 0 to t second when receive start signal), highway (module to control led in highway), country (module to control led in country). The block diagram is mentioned in **appendix A**.

2 Port description

Signal name	**Width**	**I/O**	**Description**
BUILT_IN_CLK	1	Input	Built-in clock (50MHz) of DE2-115 FPGA Board
GLOBAL_RST_N	1	Input	Global reset active low (hard reset)
CAR	1	Input	Signal from sensor (HIGH if there are cars in country road)
LED_HIGHWAY	7	Output	7-segment LED represents highway's traffic light: 0 = Green, 1 = Yellow, 2 = Red
LED_COUNTRY	7	Output	7-segment LED represents country's traffic light: 0 = Green, 1 = Yellow, 2 = Red

Table 1: Port description of top module

3 Functional Descriptions

- The highway is prioritized: always keeps Green when there is no car in country road. Country road's light always keeps Red
- If there are cars in country road:
  - **CAR** will be set HIGH, then traffic light in highway will be Green in T (seconds) then turns into Yellow in t (seconds) and finally turns into Red.

  - When traffic light in highway turns into Red, the light in country road turns Green at the same time and stays Green for T (seconds).
  - After that, country road's traffic light turns into Yellow in t (seconds) and finally turns back to Red.
  - When traffic light in country turns into Red, the light in country road turns Green at the same time and repeats the process.

- For testing in FPGA, we decode states of traffic lights, are displayed by 7 segment LEDs **LED_HIGHWAY** and **LED_COUNTRY**:
  - 0 = Green
  - 1 = Yellow
  - 2 = Red

4 Timing Diagram

To verification the system , I use random input method. Figure 2 is simulated wave form at some specific time.

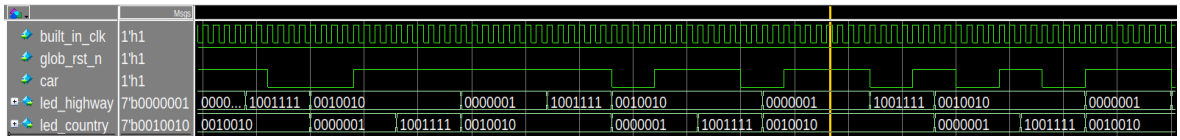

Figure 2: Timing Diagram of top module

A Block Diagram

Figure 3 depicts how submodules interactive with each others in the system.

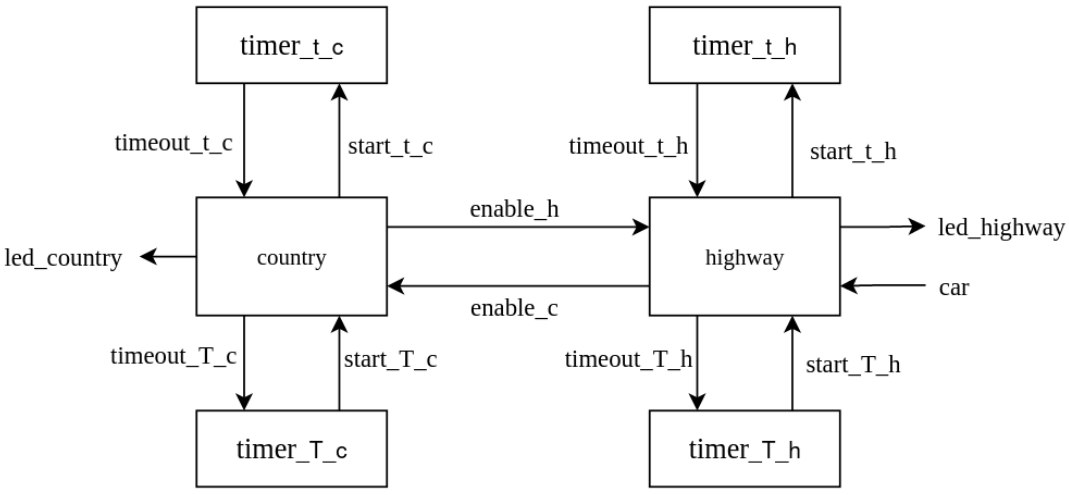

Figure 3: Block Diagram of the system

B FSM Diagram

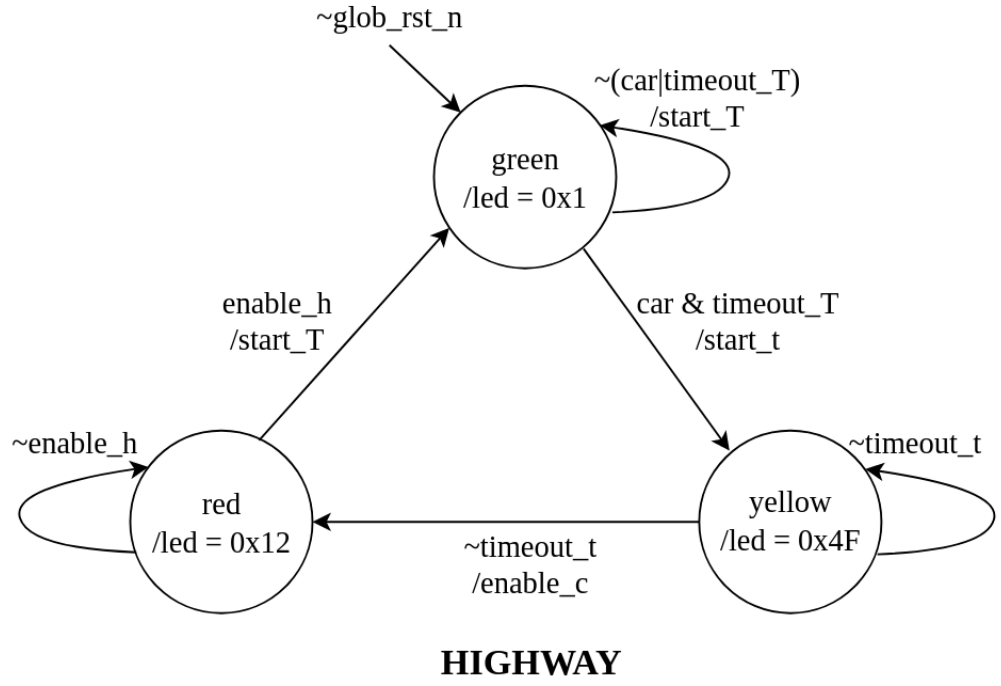

Figure 4: FSM Diagram for submodule control highway's traffic light

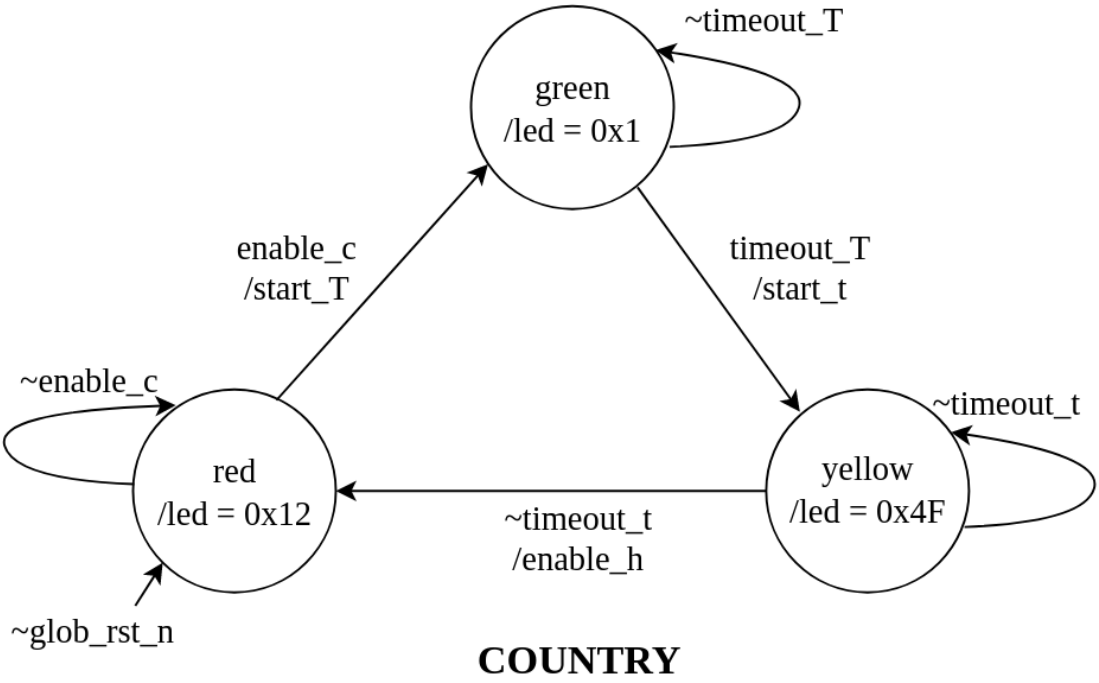

Figure 5: FSM Diagram for submodule control country's traffic light