POSSESION OF MOBILES IN EXAM IS UFM PRACTICE.

Name _____ _____ **Enrollment No.**____ _____

Jaypee Institute of Information Technology, Noida

T2 Examination, 2022
B. Tech., IV Semester

Course Title: Digital Systems/Introduction to Digital Systems Maximum Time: 1 Hr
Course Code: 18B11EC213/15B11EC314 Maximum Marks: 20

CO1. Familiarize with the fundamentals of number system, Boolean algebra and Boolean function minimization techniques.
CO2. Analyze and design combinational circuits using logic gates.
CO3. Analyze state diagram and design sequential logic circuits using flip flops.
CO4. Understand the classification of signals and systems and learn basic signal operations and Fourier analysis.
CO5. Understand various steps involved in digitization and transmission of a signal.

Q1. Realize the following Boolean expression using minimum number of 2:4 decoder(s) and logic gates: F (A, B, C, D) = Σ m (1, 2, 5, 6, 8, 9) |3, CO2|

Q2. Design a 3-bit magnitude comparator using 1-bit magnitude comparator as a block, which has two inputs A and B each of 3-bit and produces three outputs G, L and E for A > B, A < B and A = B, respectively. |3, CO2|

Q3. Draw the logic diagram of a 4-bit register with D flip-flops and four 4:1 multiplexers with mode selection inputs S_1 and S_0. The register operates according to the following function table: |4, CO3|

S_1	S_0	Description
0	0	No change
0	1	Complement of the four outputs
1	0	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data

Q4. Convert SR flip-flop to T flip-flop. |3, CO3|

Q5. Design a mod-6 synchronous binary up counter using T flip-flops. |4, CO3|

Q6. Design an asynchronous BCD down counter using JK flip-flops with its timing diagram. |3, CO3|