Analog and Digital ~~Gates~~ ckts.

Crucio Nareiso, Damasklas Arthur.] Physics.

Universal Gates:

* Analog ckt: refers to a continuously changing variable.
* Any adjacent point can be taken on the DC load line.
* A sinusoidal input (~) is the best example.

* Digital ckt: is a two-state operation i.e. high or low.
* Only specified points are taken on the ~~power~~ load line.
* A square wave (⎍⎍⎍⎍) is the best input in it.

Gate:

Universal Gates.

NOT gate, OR gate & AND gate (Basic Gates)

* Gates are the digital ckts having 1 or many inputs but only 1 output.
* Logic ckts are designed by the combination of different gates in different ways.
* The logic ckts are named so as they stimulate the mental process.

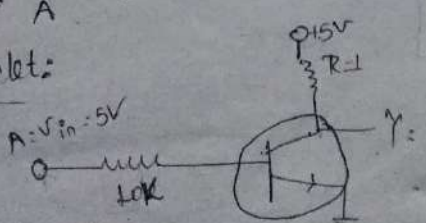
~~Not~~ NOT gate:

Symbol: A → $Y = \bar{A}$

Truth Table:

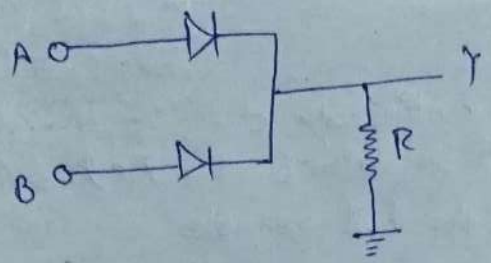
A	Y
0	1
1	0

Logic ckt:

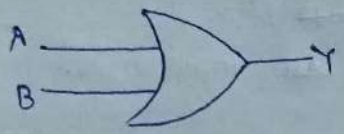


OR gate:
(Using diodes):

Logic ckt



Logic symbol

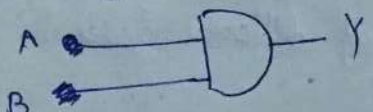


Truth table.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

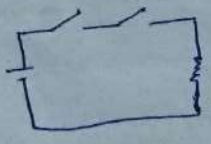
AND gate:

Logic symbol

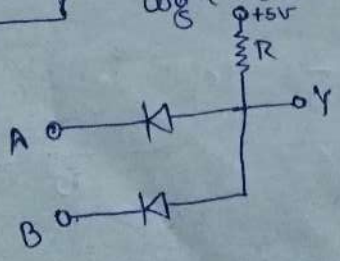


Truth table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



Logic ckt:



Boolean Algebra

* De Morgan attempted to find a link between the logic and the mathematics but failed.
* George Boolean introduced the idea bet^n the logic and the mathematics.
* Finally Shanon used the logic telecommunication switching circuits.

NOT gate

According to Boolean, $Y = \overline{A}$

$= \overline{0} = 1$

$= \overline{1} = 0$

OR gate

For A and B as inputs, Y = A OR B

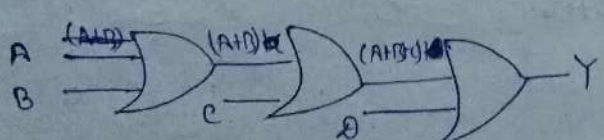
According to Boolean, Y = A + B

AND gate

Y = A AND B

A/c to Boolean, $Y = A \cdot B$

Boolean Equations



$\therefore Y = A + B + C + D$

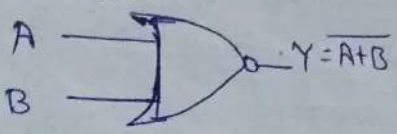
Double Inversion

$$\overline{\overline{A}} = A \Rightarrow \overline{\overline{0}} = 0 \; ; \; \overline{\overline{1}} = 1 .$$

De. Morgan's Theorem

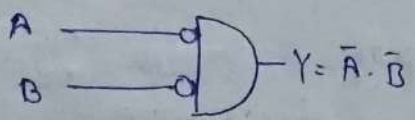
* First theorem

NOR gate ($\overline{A+B}$)



A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Bubbled AND gate. ($\bar{A} \cdot \bar{B}$)

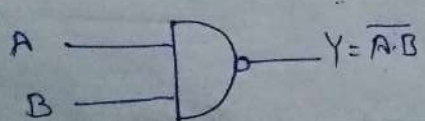


A	B	$Y = \bar{A} \cdot \bar{B}$
0	0	1
0	1	0
1	0	0
1	1	0

NOR gate is equivalent to a bubbled AND gate.

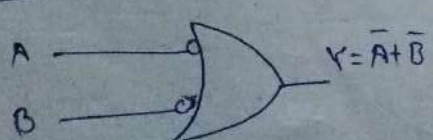
* Second Theorem

NAND gate ($\overline{A \cdot B}$)



A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Bubbled OR gate



A	B	$Y = \bar{A} + \bar{B}$
0	0	1
0	1	1
1	0	1
1	1	0

NAND gate is equivalent to bubbled OR gate.

i.e. $\overline{A \cdot B} = \bar{A} + \bar{B}$

Boolean Laws and Theorems

1. Commutative Laws.

$A+B = B+A$

$A \cdot B = B \cdot A$

2. Associative Law.

$A+(B+C) = (A+B)+C$

$A \cdot BC = AB \cdot C$

3. Distributive Law

$A(B+C) = AB+AC$

$A+BC = (A+B)(A+C)$

4. $A+0 = A$

$A+1 = 1$

$A+A = A$

$A+\bar{A} = 1$

$\bar{\bar{A}} = A$

$A \cdot 1 = A$

$A \cdot 0 = 0$

$A \cdot A = A$

$A \cdot \bar{A} = 0$

5. $\overline{A+B} = \bar{A} \cdot \bar{B}$

$\overline{A \cdot B} = \bar{A} + \bar{B}$

6. Absorption Theorem

$A + AB = A$

$A \cdot (A+B) = A$

$A + \bar{A}B = A + B$

$A \cdot (\bar{A}+B) = A \cdot B$

*Duality theorem

a. OR $\longleftrightarrow$ AND

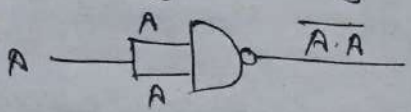
b. 0 $\longleftrightarrow$ 1

Universal Gates

NAND and NOR gates are regarded as the universal gates. These are so called as the basic gates (NOT, OR & AND) are derived form.

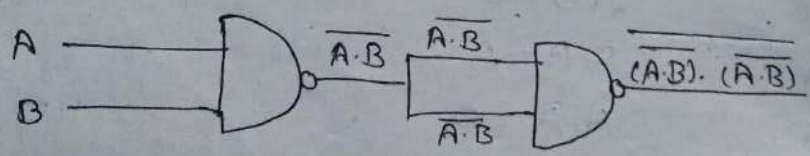
NAND gate:

To get NOT gate:



$Y = \bar{A} \Rightarrow$ NOT gate

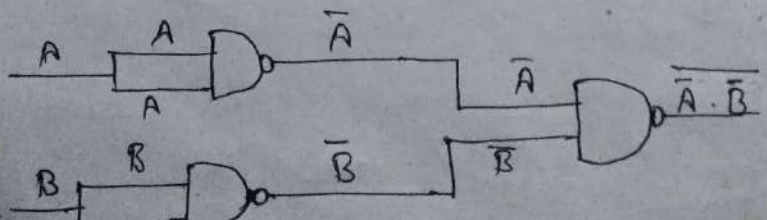
To get AND gate:



$= A \cdot B$

$\Rightarrow$ AND gate.

To get OR gate:



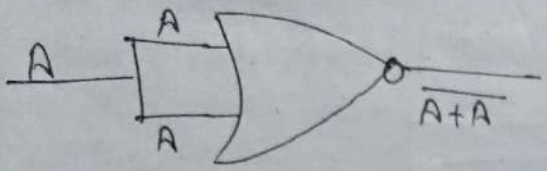
$Y = \bar{A} + \bar{B}$

$= A + B$

= OR gate

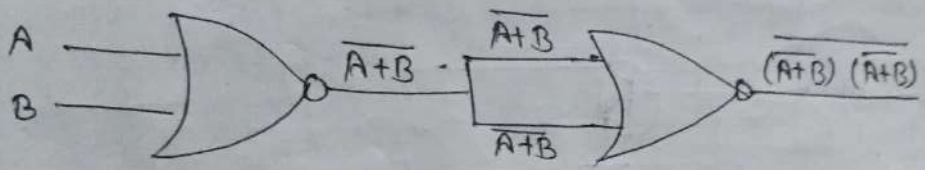
NOR gate:

To gate NOT gate:



$Y = \overline{A} \Rightarrow$ NOT gate

To gate ~~NOT~~ OR gate:

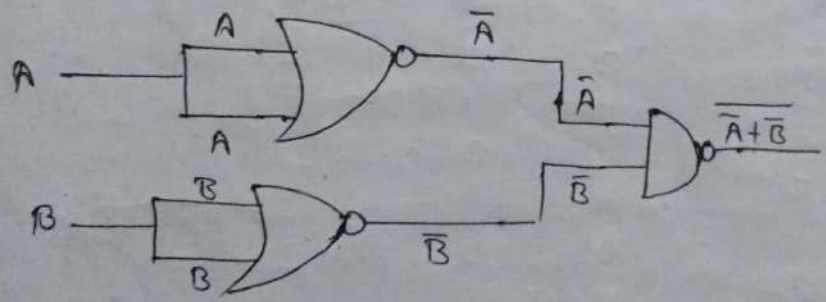


$Y = \overline{\overline{A+B}}$

$= A+B$

$=$ OR gate

To get AND gate:



$Y = \overline{\overline{A}} \cdot \overline{\overline{B}}$

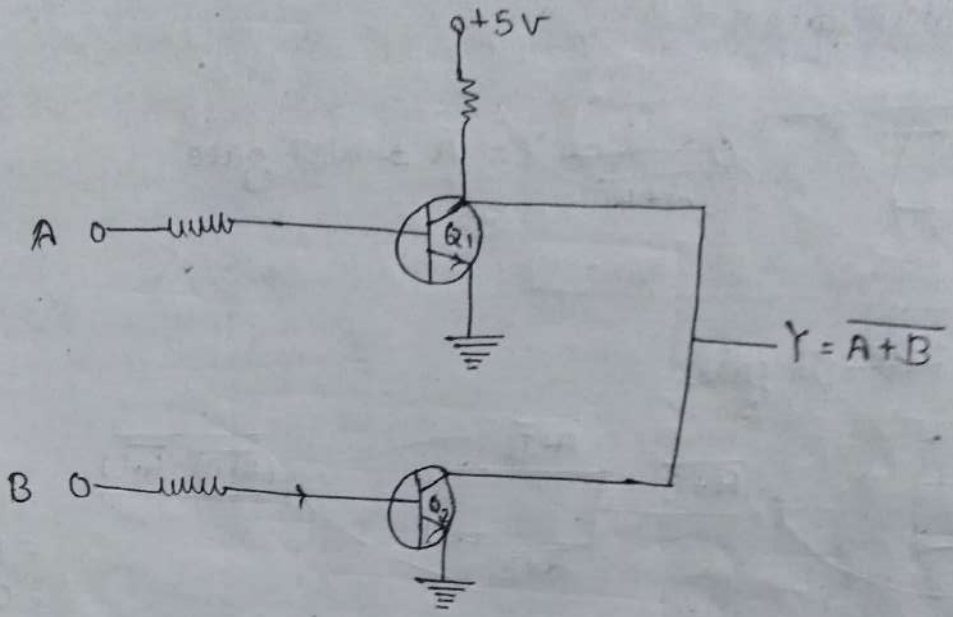
$= A \cdot B$

$\Rightarrow$ AND gate.

* RTL logic gate:

* → RTL refers to a resistor transistor logic family of gates. A well known RTL logic ckt is outlined in the figure.

P.T.O.


+5V
A
B
Q1
Q2
Y = $\overline{A+B}$

NOR gate:

The RTL logic circuit for NOR gate has been outlined in the figure. The resistor, transistor (doping constitutes the RTL logic)

The NOR gate output can be proved with the help of a truth table:

First entry:

A = 0 , B = 0.

When both entries are kept zero (i.e. grounded), there is no voltage drop across R_B and hence no current is constituted thereby keeping the transistors off. The supplied voltage across R_c appears across as an output i.e. Y = 1.

Second entry:

A = 0 ; B = 1

For A = 0, the first transistor Q_1 is ~~no current~~ remains off as there is no current flow on the base.

For B = 1, there is base current on the second transistor Q_2, it becomes ON and the voltage drop across R_c goes to ground there by giving Y = 0

Third entry:

A = 1 ; B = 0.

For B = 0, Q_2 remains off in the same way as in the 2nd entry.

For A = 1, there is base current on the first transistor Q_1, it becomes on and the voltage drop across R_c goes to ground. Thereby giving Y = 0

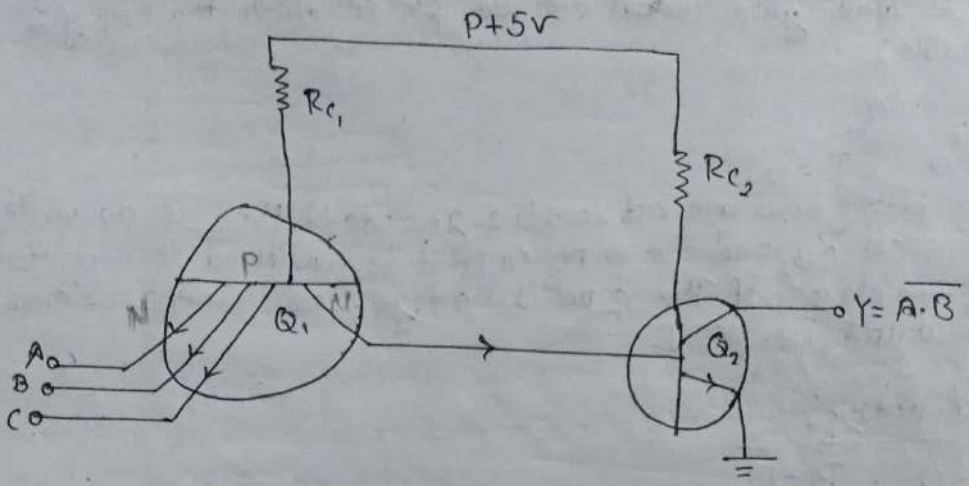
Last entry:

A = 1 ; B = 1.

Both the transistors begin to conduct due to the flow of base current. Hence, supply voltage drop across R_c becomes grounded. Hence, output Y = 0

TTL NAND Gate:

* Deduced by the Texas company at around 1964.
* Easier to use, cheap, small size & modern circuiting.



A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

The TTL NAND Gate has been shown in the fig. The transistor Q_1 is a multiemitter transistor having three emitters with inputs A, B & C separately.

The functioning of the NAND gate can be described as in the following entries.

Let one of the inputs is ~~high~~ low (say A = +0V), the base emitter junction of Q_1 is forward biased and the supply voltage across R_c, goes to the ground & hence base collector junction becomes reversed biased. As a result, the second transistor Q_2 remains off. Hence, voltage drop across R_c, appears in the output yeilding Y high. i.e; Y=1.

The same situation appears when any two of the inputs are grounded or all the three inputs are grounded.

When all the inputs are kept high, (A=B=C=+5V), the base emitter junction is now reversed biased, only the base collector junction of Q_1 becomes forward biased. Thereby making Q_2 transistor ~~off~~ ON.

Hence, voltage drop of the supply across R_c, goes to the ground yeilding Y output low i.e., Y=0 and we write;

$$Y = \overline{ABC}$$

Memory Circuits

Under memory circuits, here we focus attention on and over flip-flop ckt.

A flip-flop is a bistable electronic ckt that has two stable states. i.e. 0 & 1. (eg 0V & 5V).

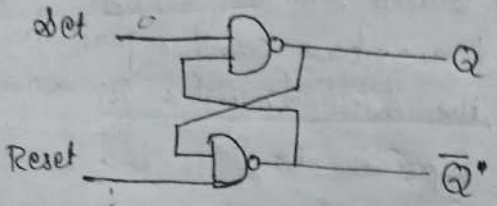
It is called a memory device because the output once ~~stored~~ set remains same unless something is done after it.

Flip-flops are of two types (here)

① Reset - set flipflop (RS Flip Flop) or Latch.

② Data Flipflop (or D flip flop)

RS Flip-Flop.



The RS flip-flop ckt is shown in the fig. The memory funct of such a device to store information has been described with the help of the following entries:

Set S=1, R=1. The case is forbidden (ambiguious).

Let S=0, the output yields Q=1, $\bar{Q}$=0

Here, Q=1 is the information saved.

The information has been saved as Q=1.

To delete the data, we can't use (change) S.

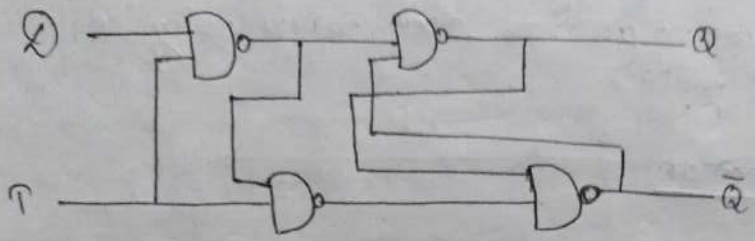
Now, to change the data saved, we keep R=0.

$\therefore$ Q=0 , $\bar{Q}$=1.

This data has been reset that can't be altered using R.

To change the value to the new one, again, we use set functions. Hence, it works.

The Data Flip-Flop (D - Flip Flop)



The D-Flip Flop ckt using the NAND gate is shown in the figure. The last section is the latch studied earlier. Here, D is the information fed to the ckt & T is the controller that controls the response to the ckt on the data fed.

If T=1, there is data yeilding in the output.

If T=0, it can't do anything and the data remains in the previous stage.

Let D=1, T=1. The output Q=1, $\bar{Q}$=0. (Describe yourself)

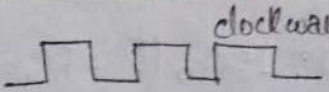
the data fed has been saved in the output.

If T=0, it remains unchanged and stays in previous case.

To change the data, D=0, T=1 → Q=0; $\bar{Q}$=1

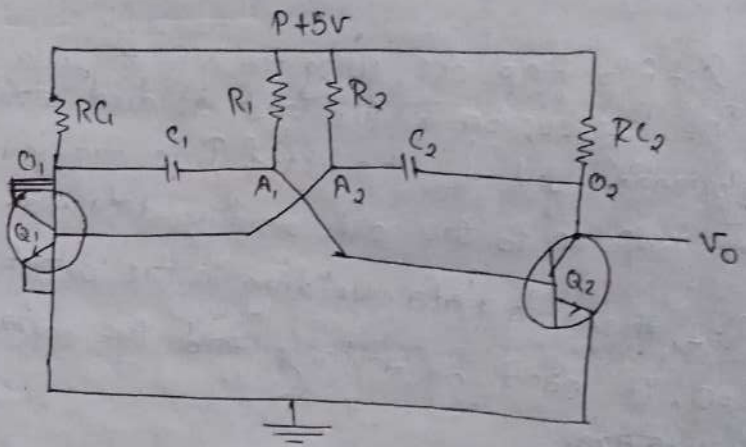
If T=0, it remains in previous case.

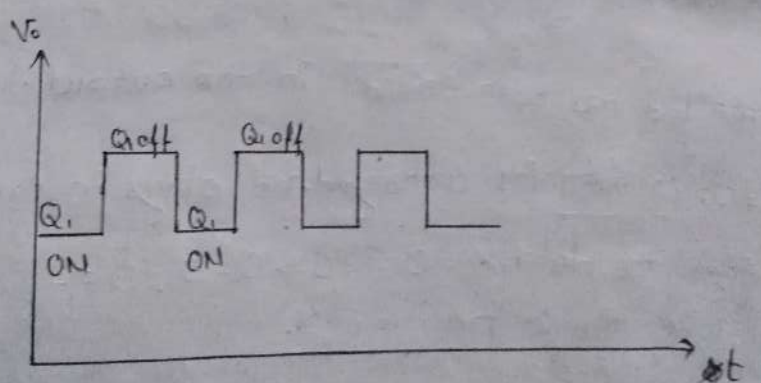
Clock circuits



* Clock circuits are used to run the computer ckts in digital devices.
* Multivibrators are used to generate clock waves using the principle of negative feedback.

Astable multivibrator





The astable multivibrator to generate a clock wave is shown in the fig: Though the two transistors Q_1 and Q_2 have the same parameters in the respect, there is some unbalance and one of the two becomes active first.

Let us have Q_1 transistor is ON first due to the full charge on C_2. The O_1 point now becomes virtual ground point and hence point A_1 is -ve w.r.to the point O_1. Hence, the PN junction of Q_2 is reverse biased and remains OFF, with zero output, VC_1

At the same time, C_1 is charged due to the potential drop at R_1. and when it is fully charged, the output VC_1 now becomes high. Eventually, Q_2 is forward biased; becomes ON and O_2 is found to have in virtual ground. A_2 hence is -ve w.r.to the point O_2 and hence Q_1 being reverse biased becomes off with zero output in VC_1. Again, C_2 goes on changing by the voltage drop at R_2, becomes fully charged with VC_2 high, eventually Q_1 becomes ON and similar process is carried out onwards. Finally, a clock ~~becomes~~ wave hence is generated.

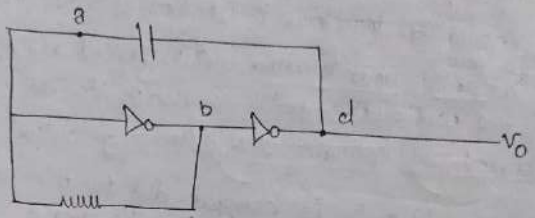
Here,
charging time is, $t_1 = 0.69 R_1 C_1$
and $t_2 = 0.69 R_2 C_2$

$\therefore$ Total times, $T = t_1 + t_2$
$= 0.69 R_1 C_1 + 0.69 R_2 C_2$

For $R_1 = R_2 = R$, $C_1 = C_2 = C$;
$T = 1.38 RC$

Hence, $f = \frac{1}{T}$ is the duty cycle.

IC free Running Clock source:



Let initially, point 'a' is ~~checked at~~ kept at zero potential
i.e, $V_a = 0V$

By the action of an inverter, a point b is at high potential
i.e, $V_b = 5V$

And thereby $V_d = V_o = 0V$. The capacitor as shown in the first net work goes on charging becomes fully charged with $V_a = 5V$.

Now, by the action of inverter,

$V_b = 0V$ & $V_d = V_o = 5V$.

It is because the capacitor discharges yielding high output.

Hence, the generation of the clock wave.

Pg-500

27.1. Make the appropriate ~~law~~ truth tables to prove the following distributive law of boolean algebra.

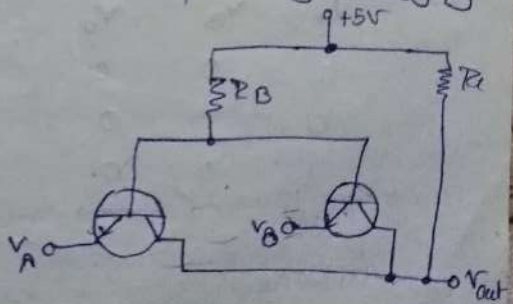
$$A(B+C) = AB + AC.$$

→ Soln,

Truth table:

A	B	C	(B+C)	AB	AC	AB+AC	A(B+C)
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	0	1	1	1
1	1	0	1	1	0	1	1
1	1	1	1	1	1	1	1

27.6 Analyze the circuit shown in fig. Determine the logic function performed by the circuit by making justifying the appropriate truth table.



→

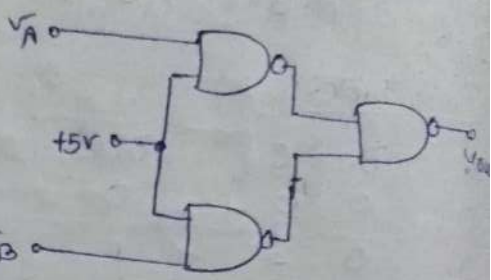
V_A	V_B	V_o
0	0	0
0	1	0
1	0	0
1	1	1

AND gate

27.9

(a) Find the truth table for the circuit shown in fig. What logic function does the circuit perform?

(b) What logic function will the circuit perform if the constant +5V input to the first two gates is changed to ground potential?



→

V_A	V_B	V_o
0	0	0
0	1	1
1	0	1
1	1	1

(a) OR gate

→

V_A	V_B	V_o
0	0	0
0	1	0
1	0	0
1	1	0

(b) None

27.10

HW

27.10

(a) Find the truth table for the circuit of fig. 27-32. What logic function does the circuit perform? (b) What logic function does the circuit perform if the common grounded input to the first two NOR gates is changed to +5 V?

→ Soln,

The truth table for given circuit diagram is;

V_A	V_B	V_o
0	0	0
0	1	0
1	0	0
1	1	1.

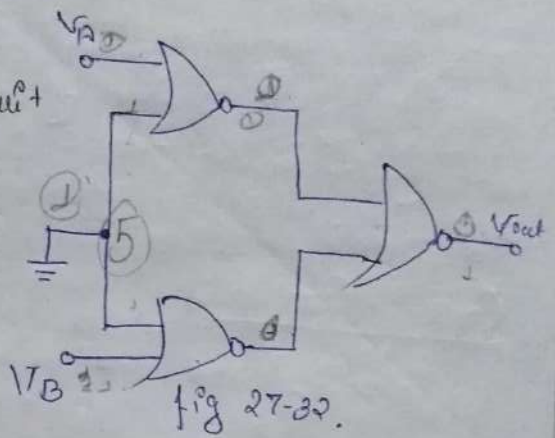


fig 27-32.

This truth table also satisfies the ~~&~~ ~~two~~ logic gate for AND gate.

a) ∴ the ~~logic~~ circuit perform the AND function.

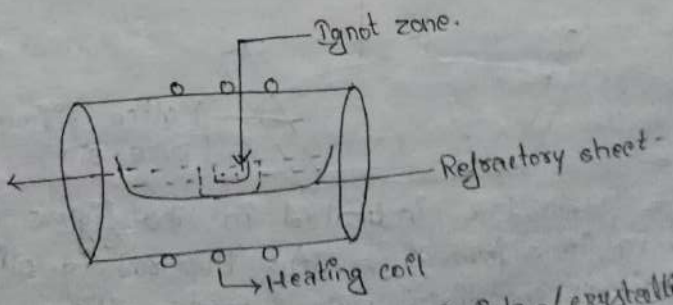
b).

V_A	V_B	V_o.
0	0	1
0	1	1
1	0	1
1	1.	1

⇒ None

Silicon Purification (Zone Refining):

* Si is the fundamental basis for the microelectronics devices that is easily available in the nature.
* SiO_2, $SiHCl_3$ & $SiCl_4$ are the forms of silicon.
* Using chemical decompositions, one gets Si from these compounds mentioned.
* The Si obtained hence has impurities concentrated as one atom per million atoms.
* The molten form of Si obtained hence is solidified called ignot. An ignot is polycrystallize in nature and has crystals with different orientations.
* The removal of the impurity present hence is the method of zone refining.
* The final pure form is termed as seed crystal.



The zone refining is based on the principle of crystallization of NaCl soln in water. The solubility of impurity atoms has higher value.

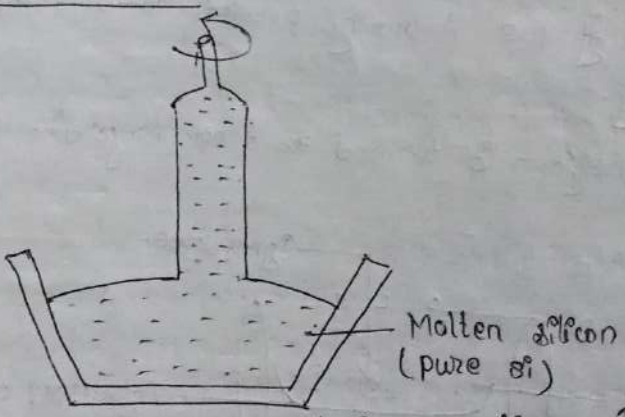
The ignot is kept inside a cylindrical furnance in a crucible. The furnace is set up using the heating coils as shown in the fig.. The molten state is slowly exerted out so that it begins to solidify leaving behind the impurity in the other end.

On repeting for several times the same process, finally we get pure form of solidified silicon by removing the molten part. such part is termed as seed crystal.

Crystal Growth:

Following are the methods:

1. Czochralski method:



The method is indicated in the figure. The aped crystal in in a form of a long thin rod is dipped inside a crucible containing pure & molten silicon.

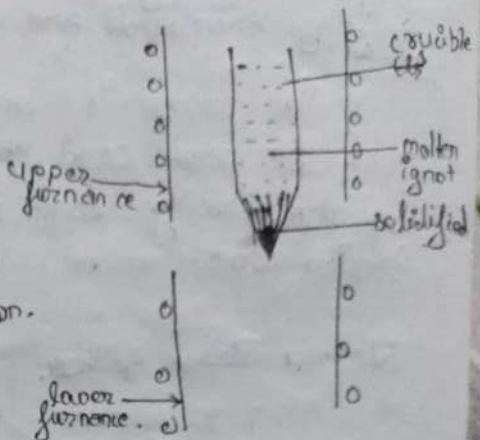
The rod is taken slowly ~~and~~ out rounding it in anticlockwise direction as shown

The emerging seed crystal becomes large in size that goes on solidifying. The rate of rotation and

it's upwards motion is determined using Hit & Trial method.

(ii) The Bridgman - Stockbarger method:

The detailed description is outlined in the fig. The upper furnance is kept at slightly above the temperature of the melting point of the silicon while the lower furnance is kept slightly below the temperature of melting point of silicon.



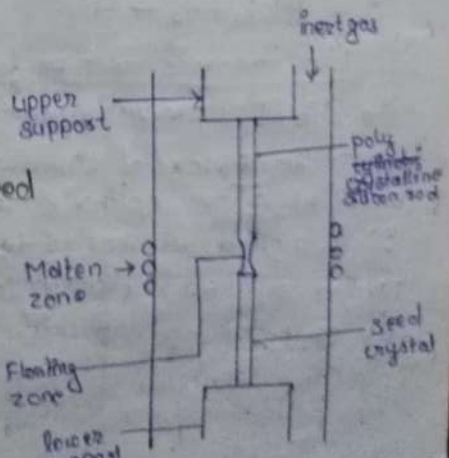
The ignot now is kept in the crucible of conical shape. Inside the upper furnance, it is in the molten state & on falling towards the lower ~~furnance~~ goes on solidifying from the conical tip leaving the impurities above in the molten part.

Finally cutting down the upper suspended part one gets pure form in the shape of conical tip.

(iii) Floating-zone method:

The description is outlined in the fig.. The upper rod is supported with the upper supporter while the lower seed crystal developed as a result of this technique is supported by the lower supporter.

The inactive arrangement is made in an inert gas environment. Hence, it removes the difficulty of mixing up of Si in the wall of crucible as in the above two



methods as the crucible is made up of SiO_2.

The heating coil melts the middle zone that goes on shifting downwards and solidifying in pure form.

The process is carried out for sometimes so that one gets the pure seed ~~caught~~ crystal. The two rods are held by the floating zone according to the principle of surface tension force.

Vapour Phase Epitaxy.

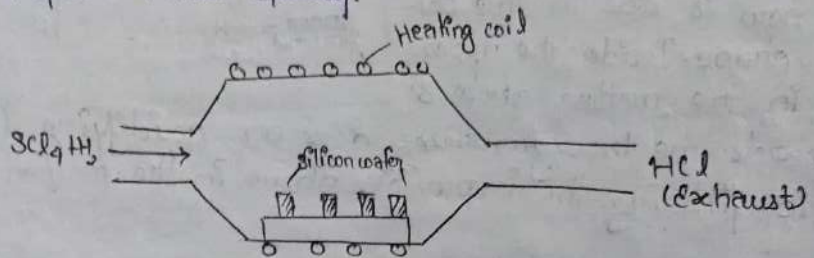


fig: Arrangement for growing Si layers on silicon wafers by epitaxial growth.

$SiCl_4 + H_2 \rightarrow HCl$.

It is the another type for the crystal growth needed for the chip (IC) production commercially.

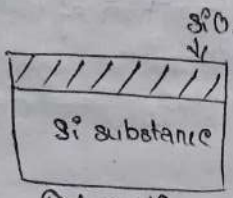
An aprox. of 10μm - 24μm of thickness can be deposited as silicon epitaxial layer on a substrate (wafer). The Si is melted at around ~~to~~ 1000°c to 1200°c using the heating coil as indicated in the fig. The vapour is coated on the Si wafer and the unwanted material as exhaust is thrown out (here HCl).

Process of IC Production:

Following are the methods generally employed during the manufacture of IC:

They are epitexial growth, oxidation, oxide removal, pattern definition, dropping and interjunction connection.

1. Oxidation



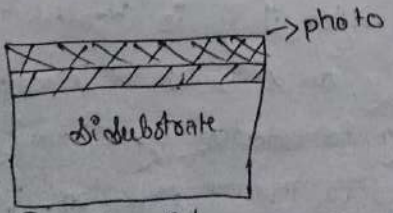
(i) formation of SiO_2

A definite thickness of the SiO_2 layer is constructed at the top of the Si substance. It is done by heating the substance at high temperature (1000°c - 1200°c) in presence of oxygen or vapour. The formation of layer of SiO_2 depends upon time of heating, composition ~~and~~ of the constituent gases in the environment.

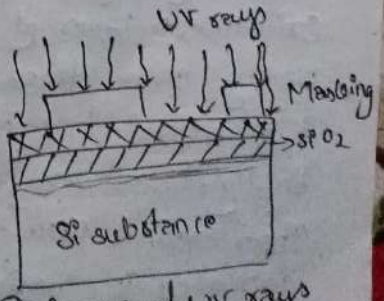
The main reason of SiO_2 deposition is:-

i. It acts as an open windows for the impurities on silicon.
ii. It saves the P-N material from contamination.
iii. ~~It~~ The dopant can't easily penetrate through SiO_2 as compared to silicon.

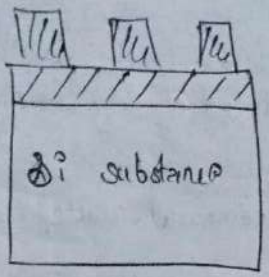
2. Photolithography (Photoresist):



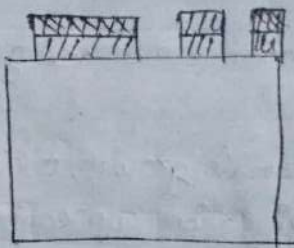
(ii) Photoresist



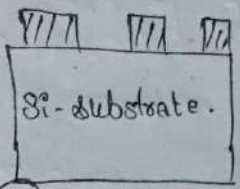
(iii) Expose of UV rays



(iv) selected photoresist removed



(v) treating with HF - resulting in formation of windows in SiO_2 layer.



(vi) Ready to dop by washing photoresist.

(3) Oxidation

A thin layer of SiO_2

(4) Pattern definition

It is the process of locating the exact point on which doping of impurities is to be made. A technique of photolithography (or masking) is done during the process. After Oxidation, a layer of photoresist is deposited on it. It is done by placing some drops of photoresist chemicals on SiO_2 layer and it is rotated in a high speed. After it, it is heated so that finally it adheres permanently on SiO_2 as photoresist layer. Then desired place of doping is selected by masking as indicated in the fig. on exposing the UV-radiation, the chemical

structure of the exposed and unexposed parts ~~after~~ alter separately, using some suitable chemicals, the photoresist under masking is removed due to its separate chemicals composition on UV-ray. The SiO_2 layer on the unexposed parts (masking) is now removed on treating it with HF solution finally, the remaining photoresist on the exposed parts (unwashed) is washed away.

The resulting form is ready for doping with impurities.

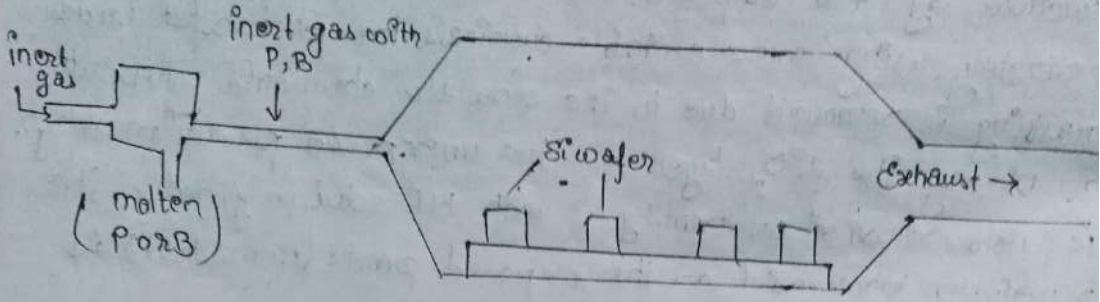
Dopping:

It is the process of injecting the impurities (pentavalent or trivalent atoms) on the fabricated semiconductor after the pattern is defined.

It consists of a two methods;

(1) Diffusion:

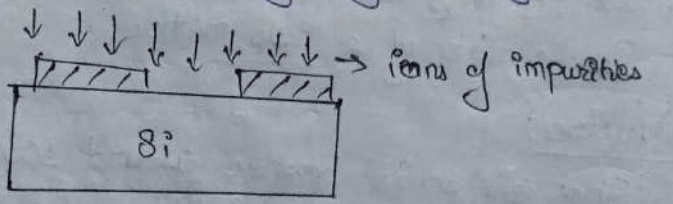
The silicon is heated around 1000°c. The atoms (a few) exite leaving behind the lattice points as valant sites. The impurities (P or B) to be injected in the form of gas with inert gas environment is diffused into the silicon material. Such impurities go and attach at the lattice sides and finally spread over the bulk of the silicon material. It is found at 1000°c for 1 hour time, the impurities level increases by 1 µm thickness.

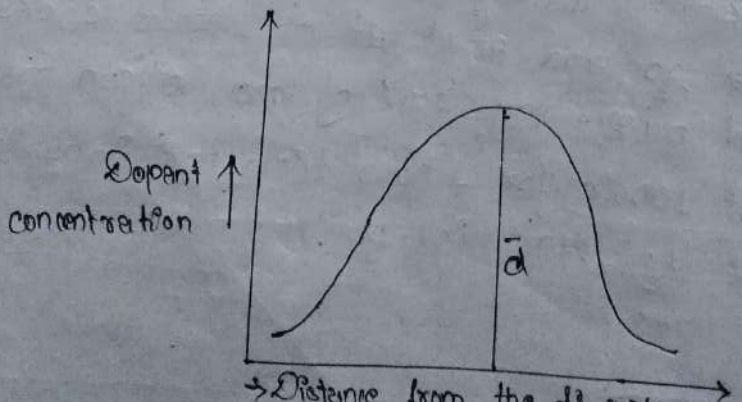


The case of gaseous impurities such as diborane (B_2H_6) and phosphorus trifluoride (PF_3), ~~iota~~ inert gas is not required.

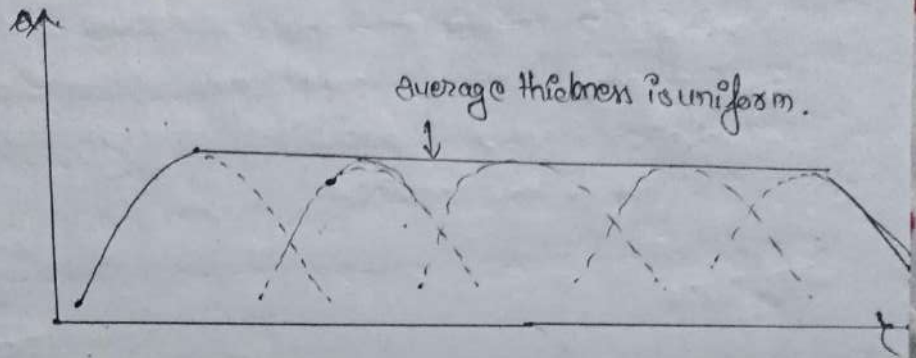
(iii) Ion implantation:

The ions of the impurities are accelerated over the silicon material in the presence of high voltage.





(Gaussian distribution of the dopant on $\bar{d}$)



The distribution of the impurities on si is not uniform and is Gaussian in nature. On repeating over several times, we find almost a thick line on the peaks that indicates an approximate of uniformity on the Gaussian distribution.

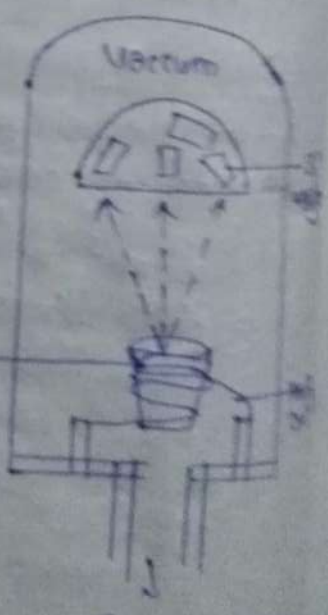
* Since ions are accelerated at high voltage, it constitutes a current that can be controlled. It is the advantage over diffusion.
* Another advantage over diffusion is that it doesn't collapse the internal configuration of the silicon species

Sometimes when current increases, we apply the process of annealing to save the silicon.

Electronic Component Connection in a Chip:

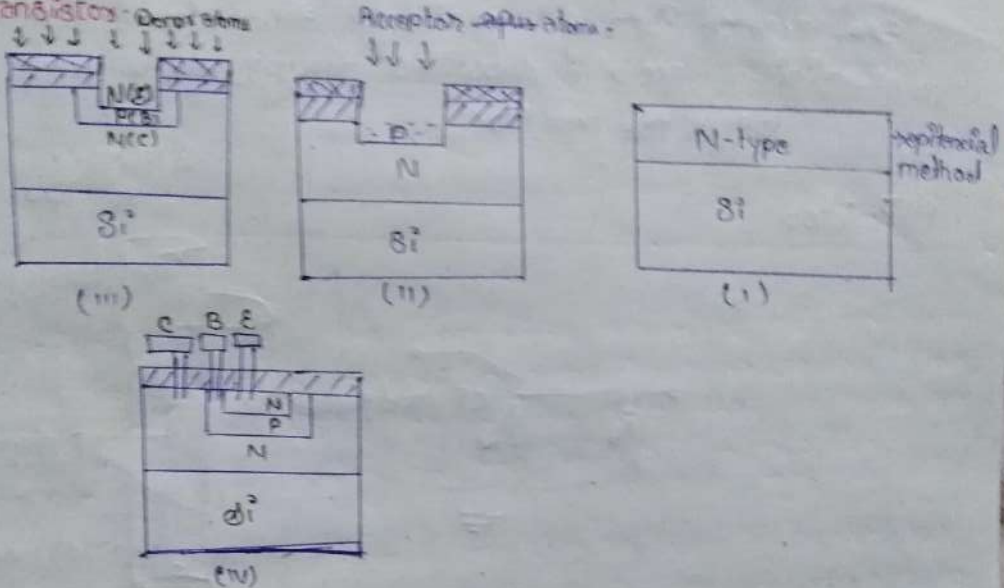
The ionised aluminium in a crucible is heated using coil as shown in the figure. The vapour form of the aluminium is created to produce 'Al' ions. metals connection on chip wafers al planetary.

This entire apparatus is enclosed in an evacuated chamber to avoid from the possible explosion & combination of O_2 gas.



Electronic Component Dopping as a chip:

(i) Transistors



Followings are the methods employed:

(i) An N-type epitaxial layer is made on Silicon substrate (fig (i)).

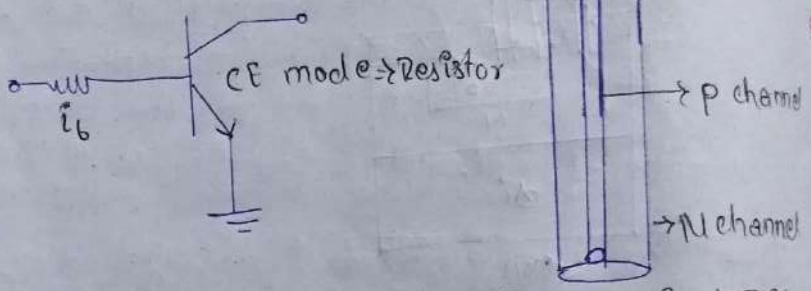
(ii) Photolithography is made (coating of SiO_2, deposition of photoresist, UV expose after masking and opening of the windows) and finally the pattern is obtained (fig ii). Then the acceptor atoms are diffused on the pattern selected on the N layer. It is the P region.

(iii) Again the technique of photolithrophy is made on the top and finally a small pattern to dop donor atoms is selected out. The donor atoms are now diffused. It acts as N layer and acts as the emitter for the transistor. The P region acts as the base and the initial N layer acts as the collector.

(iv) For the electronic component connection, again the photolithography is made and three windows on N, P & N regions are created. Then as mentioned ~~above~~ already, the ions aluminium vapour is deposited through the windows.

Hence, the transistor

ii) Resistor



A shallow diffusion of p-type of materials through an N-channel is made. The resulting channel is reverse biased so that there is small current flow thereby forming a resistor.

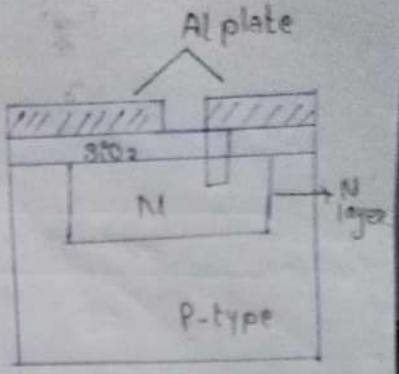
The resistance designed hence depends on the channel length, its cross-sectional area and it's doping concentration. ~~Since~~

Since the size of the IC itself is small, we can't design a high resistance value in the manner like this. In such a case a transistor in the CE mode is constructed and the resistance is measured on the basis of base current flow.

Capacitor:

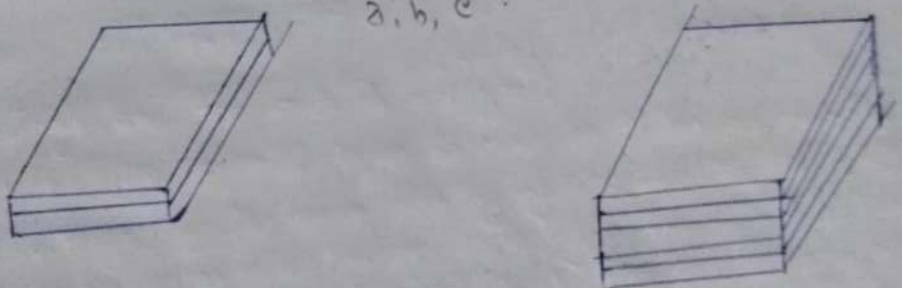
A capacitor consists of two metal plates separated by an insulating medium.

Here, inside the chip, N epi layer acts one metal ~~bridge~~ plate connected with the aluminium plate. The oxide layer (SiO_2) acts as the insulating medium and wide aluminium next layer on the top acts for the second metal plate.



Fabrication of IC:

The detailed description of the IC fabrication method is outlined in the fig. a, b, c.



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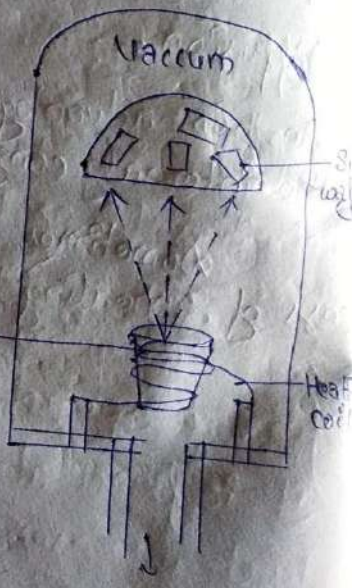
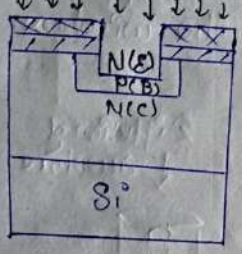


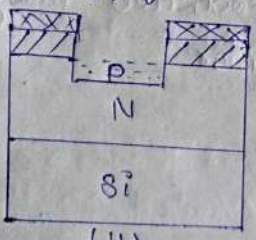
Electronic Component Dopping as a chip:

(i) Transistor: Donor atoms

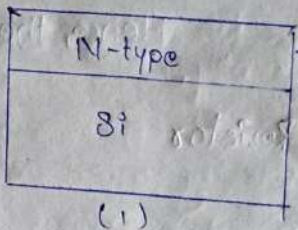


(III)

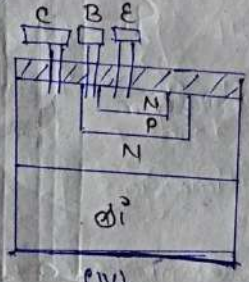
Acceptor impurity atoms.



(II)



(I)



(IV)

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(I) An N-type epitaxial layer is made on Silicon substrate (fig (I)).

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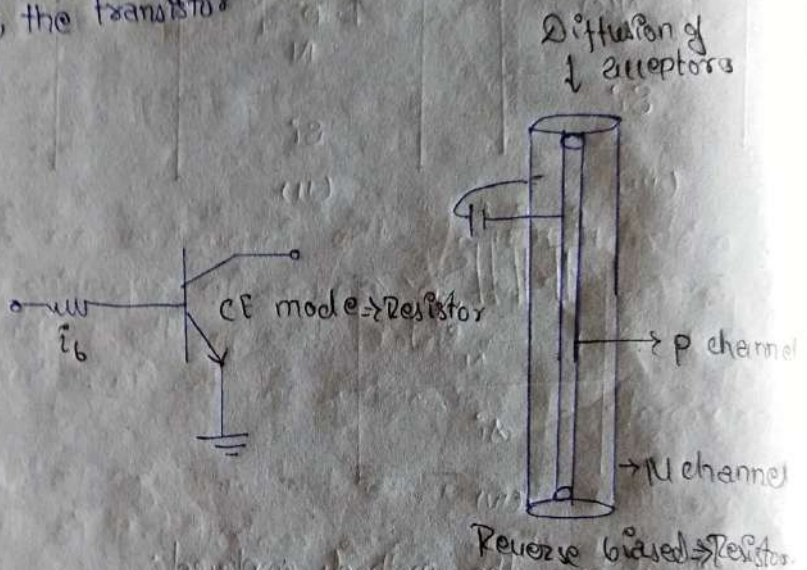

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The resistance designed hence depends on the channel length, its cross-sectional area and it's doping concentration. ~~Since~~

Since the size of the IC itself is small, we can't design a high resistance value in the manner like this. In such a case, a transistor in the CE mode is constructed and the resistance is measured on the basis of base current flow.

Therefore,

$$N_e = (N_e N_h)^{1/2} = 2\left(\frac{2\pi KT}{h^2}\right)^{3/2} (m_e^* m_h^*)^{3/4} e^{-E_g/2KT} \quad \ldots (**)$$

Hence, the result doesn't show the presence of E_F.

Evaluation of Fermi Energy level (E_F):

The fermi energy is the demarcation line that separates the filled and the unfilled energy states. The probability of the electron in it is $1/2$.

To find the fermi energy, let us equate the eqn (*) and (**). we get,

$$\text{i.e. } 2\left(\frac{2\pi m_e^* KT}{h^2}\right)^{3/2} \cdot e^{\frac{E_F - E_g}{KT}} = 2\left(\frac{2\pi KT}{h^2}\right)^{3/2} (m_e^* m_h^*)^{3/4} e^{-\frac{E_g}{2KT}}$$

$$\Rightarrow \frac{e^{\frac{E_F - E_g}{KT}}}{e^{\frac{-E_g}{2KT}}} = \frac{m_e^{*3/4}}{m_e^{*3/2}} (m_h^*)^{3/4}$$

$$\Rightarrow e^{E_F/KT} = \left(\frac{m_h^*}{m_e^*}\right)^{3/4} e^{\frac{E_g}{2KT}}$$

Taking, $\log_e (\ln)$ on both sides,

$$\frac{E_F}{KT} = \frac{3}{4} \ln\left(\frac{m_h^*}{m_e^*}\right) + \frac{E_g}{2KT}$$

$$\therefore E_F = \frac{E_g}{2} + \frac{3}{4} KT \ln\left(\frac{m_h^*}{m_e^*}\right)$$

Let e be required expression

At $T=0K$, $E_F = E_g/2$

At $T>0K$, and $m_h^* = m_e^*$ in intrinsic semiconductor,

$$E_F = \frac{E_g}{2} \quad \text{because } \ln 1 = 0$$

At ordinary temperature,

$$E_F = \frac{E_g}{2} \quad ; \text{if } m_n^* \times m_e^* \text{ fairly differ.}$$

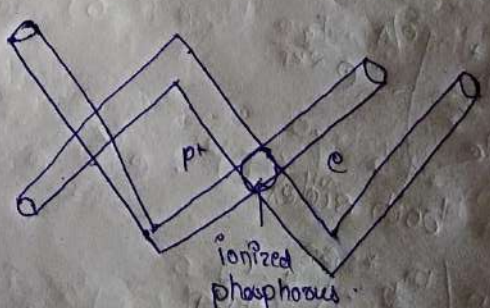
It is because $\ln x$ is a slowly varying function.

Extrinsic semiconductor

N-type semiconductor

Pentavalent atoms such as phosphorus is dopped. The surplus of extra fifth electron is loosely bound that require a little energy.

The required energy is found either by Bohr's hydrogen atom model by free electron model of quantum theory.



i.e. the necessary energy $= \frac{e^4 m}{8\epsilon_0^2 h^2} = 13.6 eV$.

For silicon, $m_e^* = 0.31 m_e$.

$$\varepsilon_0 \longrightarrow \epsilon = 12\varepsilon_0$$

$$\therefore \frac{e^4 m_e^*}{8(12)\varepsilon_0^2 h^2} = 0.029 \text{ eV}$$

At absolute OK temperature, the energy level occupied by such electrons obtained from the donors ~~electrons~~ atoms is the donor energy level (E_D). It is 10^{-2} eV below the bottom of the conduction band.

Hence a slight rise of temperature above the OK temperature is sufficient to raise these electrons to the conduction band and hence increase the conductivity of the N-type semiconductors.

P-type semiconductors.

Trivalent atoms such as aluminium is doped. There is lack of a single electron to form the four covalent bonds with the semi-conductifying materials. These shortage of electron acts as a strong centre of attraction for the hole and is regarded as the hole.

The hole hence accepts the electron from the nearby semi-conducting atom and hence the trivalent atoms are regarded as the acceptor atoms. At absolute OK temperature the energy level occupied by such atoms (or electrons) is called the acceptor energy level, E_A.